

Compal confidential

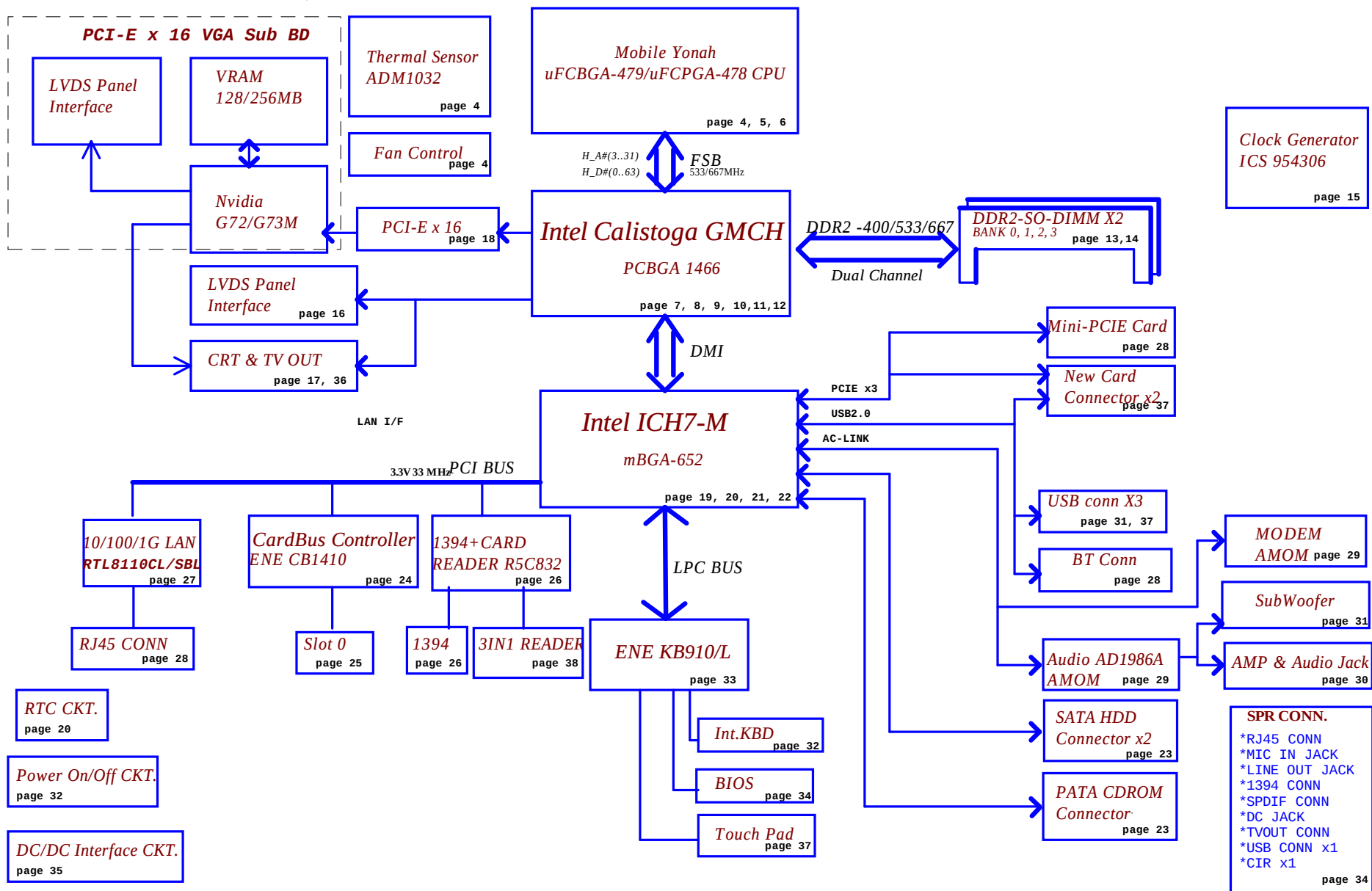
IGL50/51 Schematics Document

Mobile Yonah uFCPGA with Intel Calistoga_GM/PM+ICH7-M core logic

2006-05-15

REV:0.1

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	
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				Size	Document Number
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[illegible]

PCI DEVICES

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS CB1410	AD20	2	PCI_PIRQA#
CARD READER & 1394 R5C832	AD22	0	PCI_PIRQG# PCI_PIRQH#
LAN CONTROLLER RTL8110SBL/CL	AD17	3	PCI_PIRQF#

LANE	DEVICE
1	Express Card
2	Mini Card

PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	JP810
4	RIGHT SIDE
5	CMOS
6	RIGHT SIDE

DEVICE	ADDRESS R/W
KB910/L (SM1-Pulled-Up 5V)	
AT24C16AN	A3/A2 H
SMART BATTERY	17/16 H
KB910/L (SM2-Pulled-Up 3.3V)	
ADM1032AR	99/98 H
G7xM (I2CC-Pulled-Up 3.3V)	
G781-1 (RESERVED)	9B/9A
ICH7M SM Bus	
ICS9LP3R325AKLFT	D3/D2 H (3.3V)
DDR II DIMM0	A1/A0 H (3.3V)
DDR II DIMM1	A3/A2 H (3.3V)
Express Card	NC (2.5V)
Mini-Express	NC (2.5V)

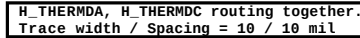
MARK	FUNCTION
@	NC FOR ALL
EXP@	PCI-E-NEW CARD
BT@	BLUE TOOTH
UMA@	Internal 945GM
VGA@	External 67xm
SUBWOOFER@	SUBWOOFER
HGT30@	HGT30
CB@	PCMIA/CARD BUS
GIGA@	8110SBL(SCL)Giga LAN
10/100@	8110CL 10/100Mb LAN

State S4 : STD S5 : S0FT OFF	power plane +B LD03 LD05	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2VS +1.8VS +1.5VS +VGA CORE +1.2VS +0.9VS +CPU CORE +VCCP
S0	0	0	0	0
S1	0	0	0	0
S3 : STR	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

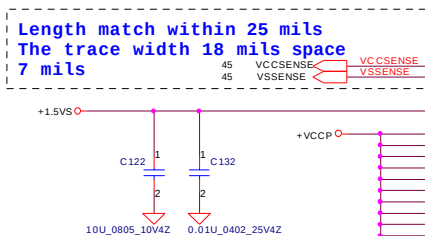
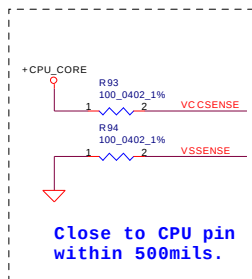
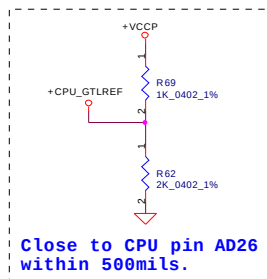
MB ID	P NAME
0	IGL-50
1	IGL-51

ID	MB REV#	R115(Rb)	Vab
0	R0.1 (EVT)	0	0
1	R0.2 (DVT)	8.2K	0.25'
2	R0.3 (PVT)	18K	0.50'
3	R1.0 (MP)	33K	0.82'
4		56K	1.19'
5		100K	1.65'
6		200K	2.20'
7		NC	3.30'

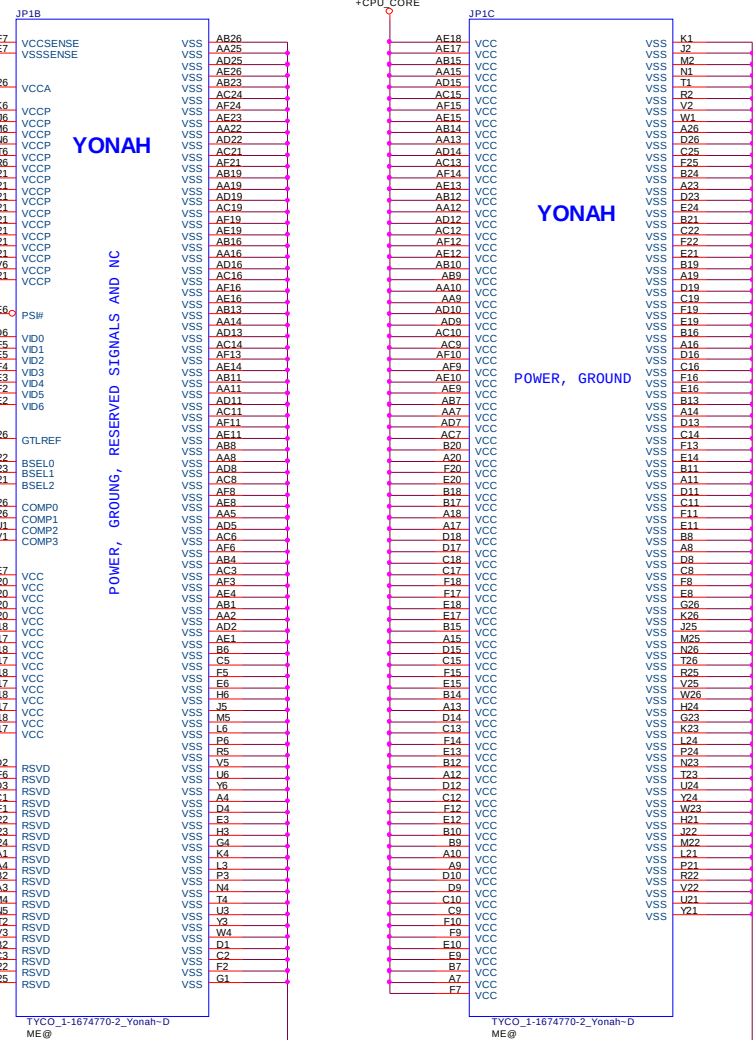
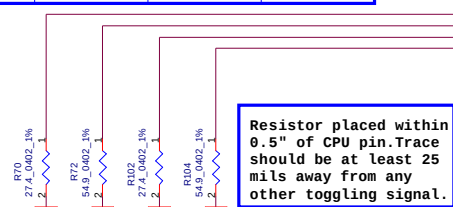
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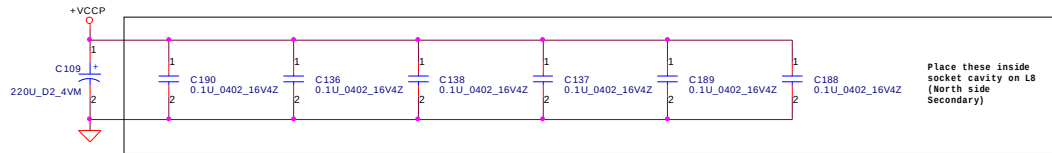
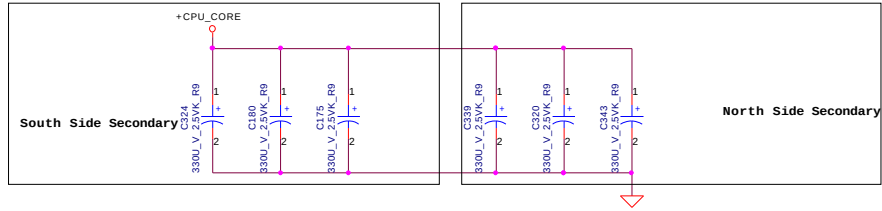
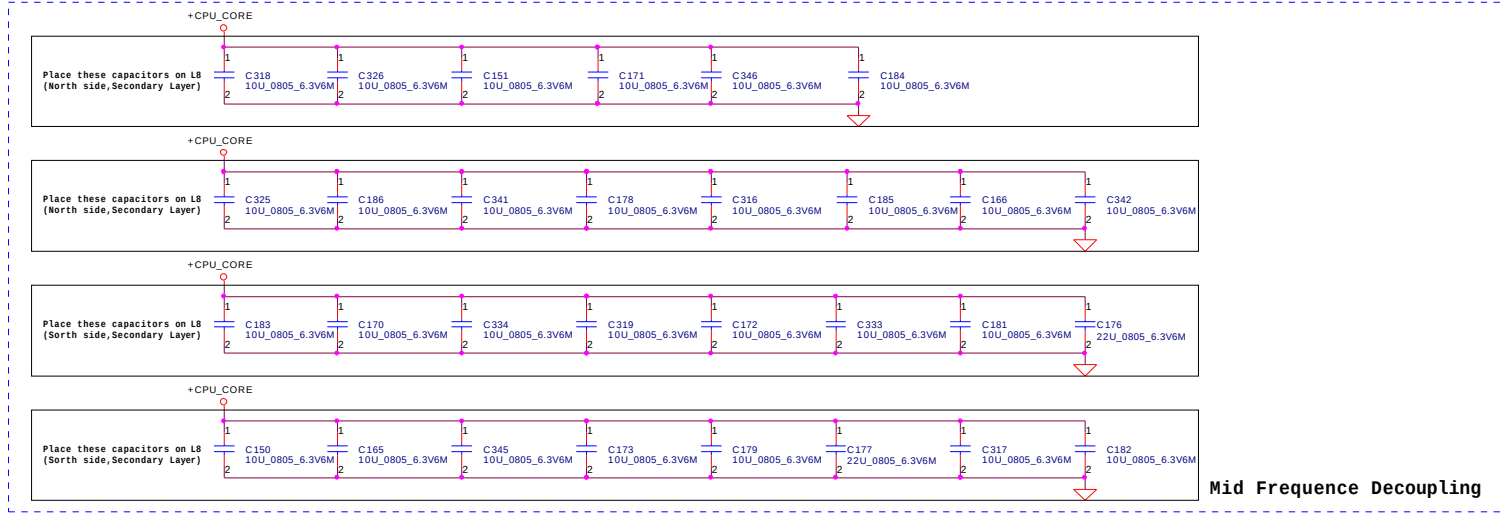


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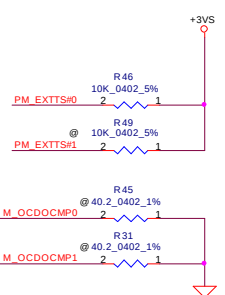
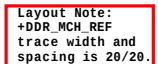


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

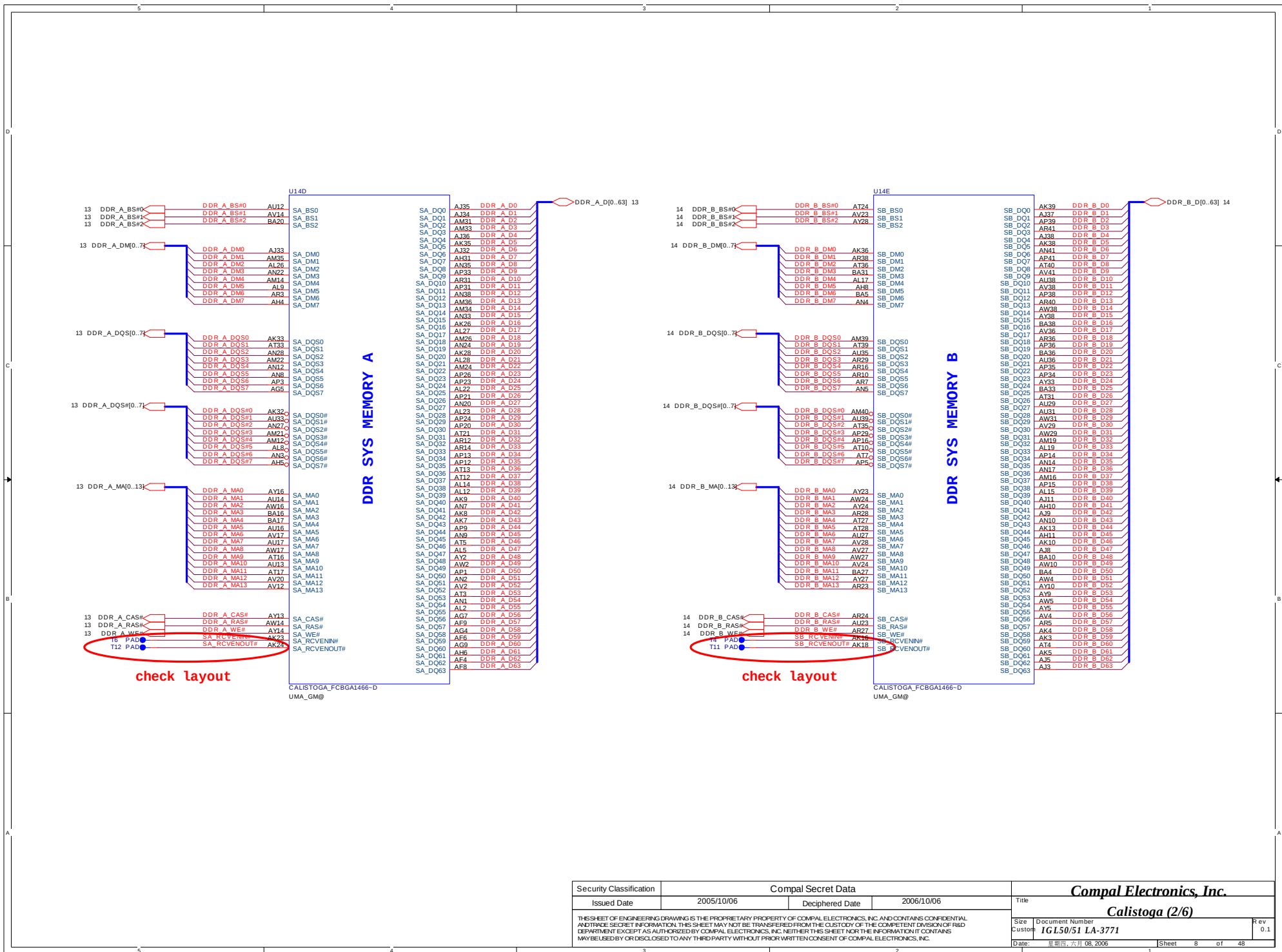




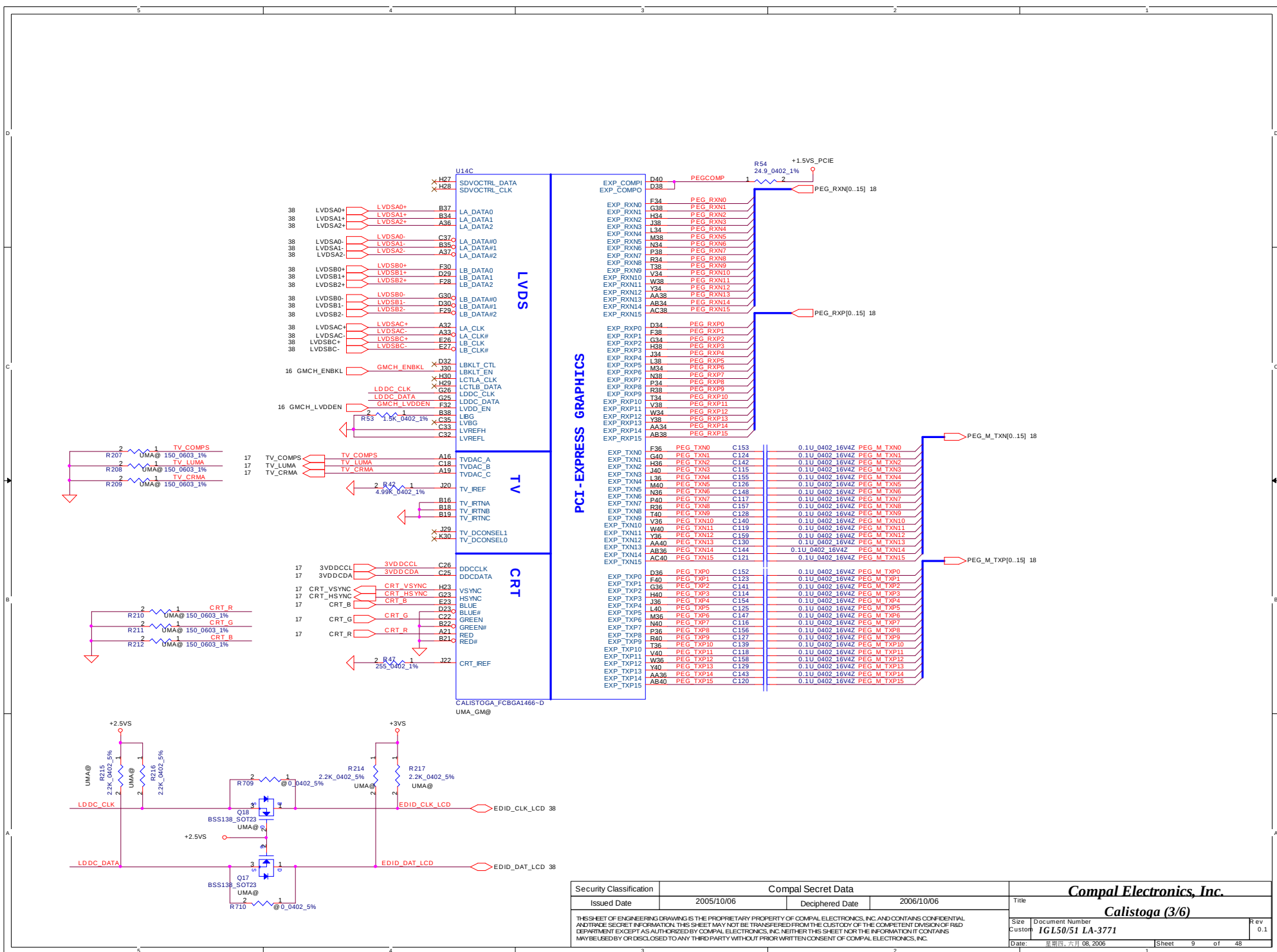
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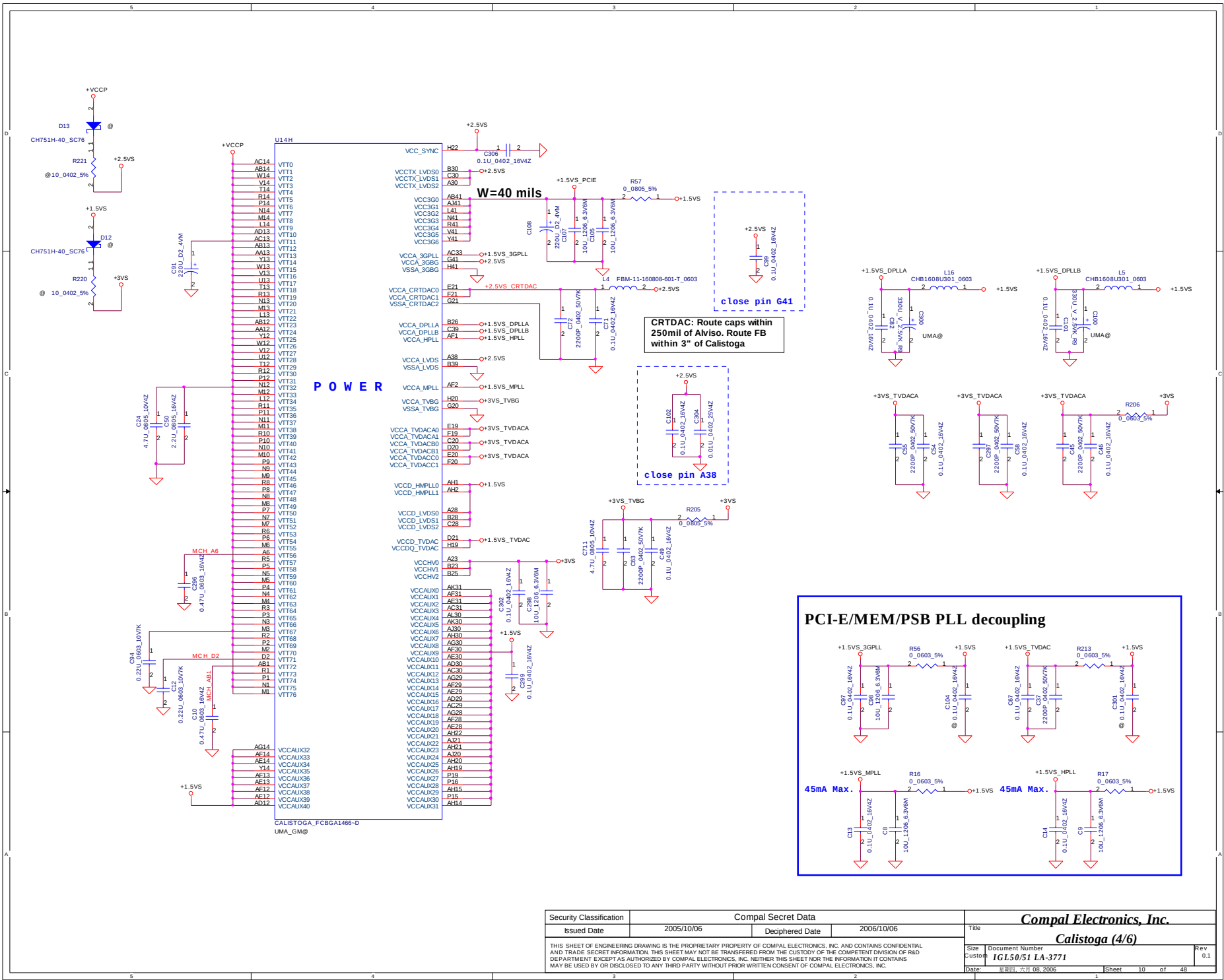


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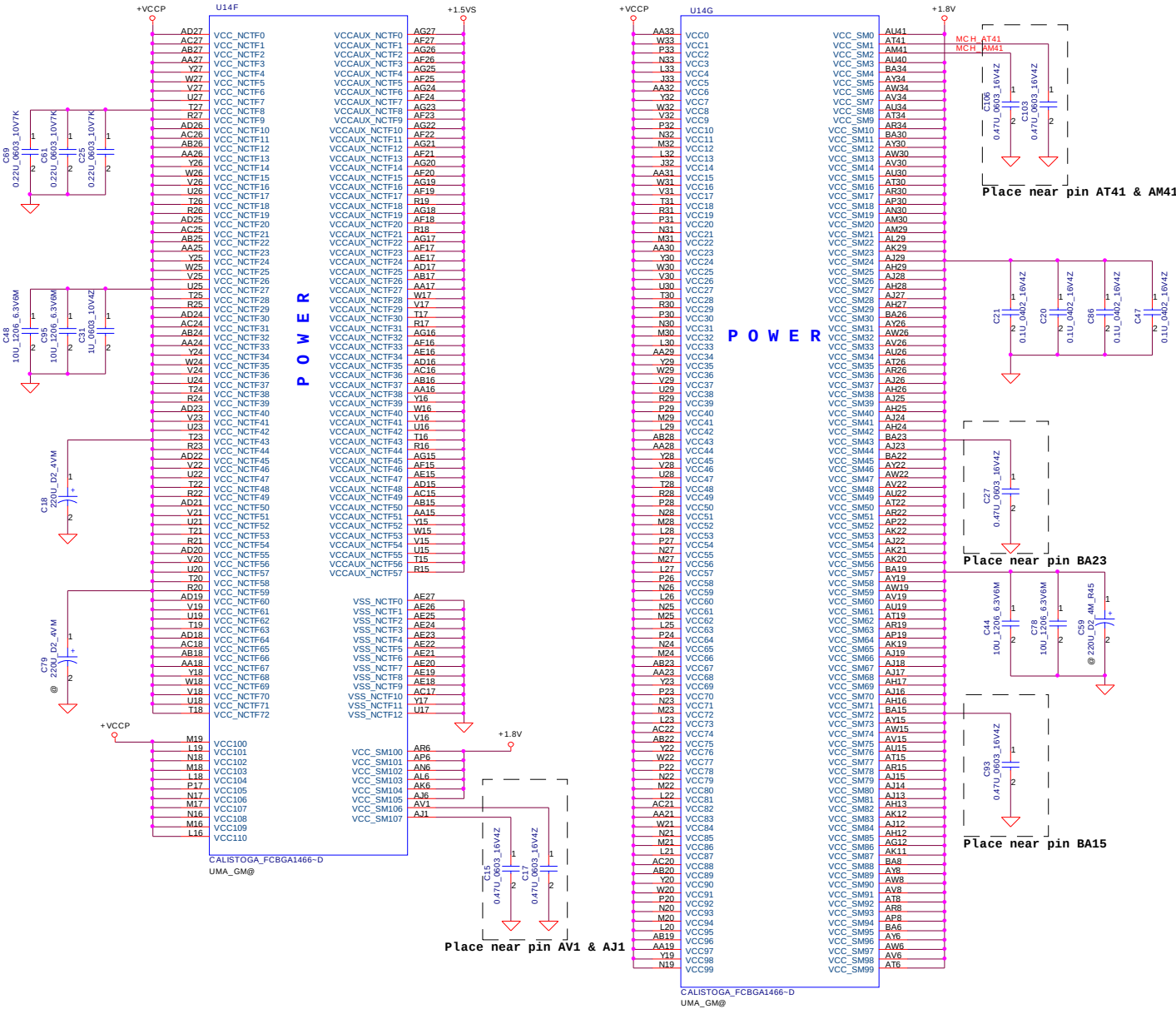
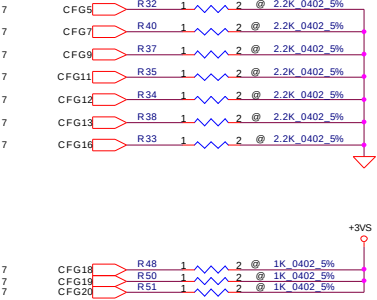


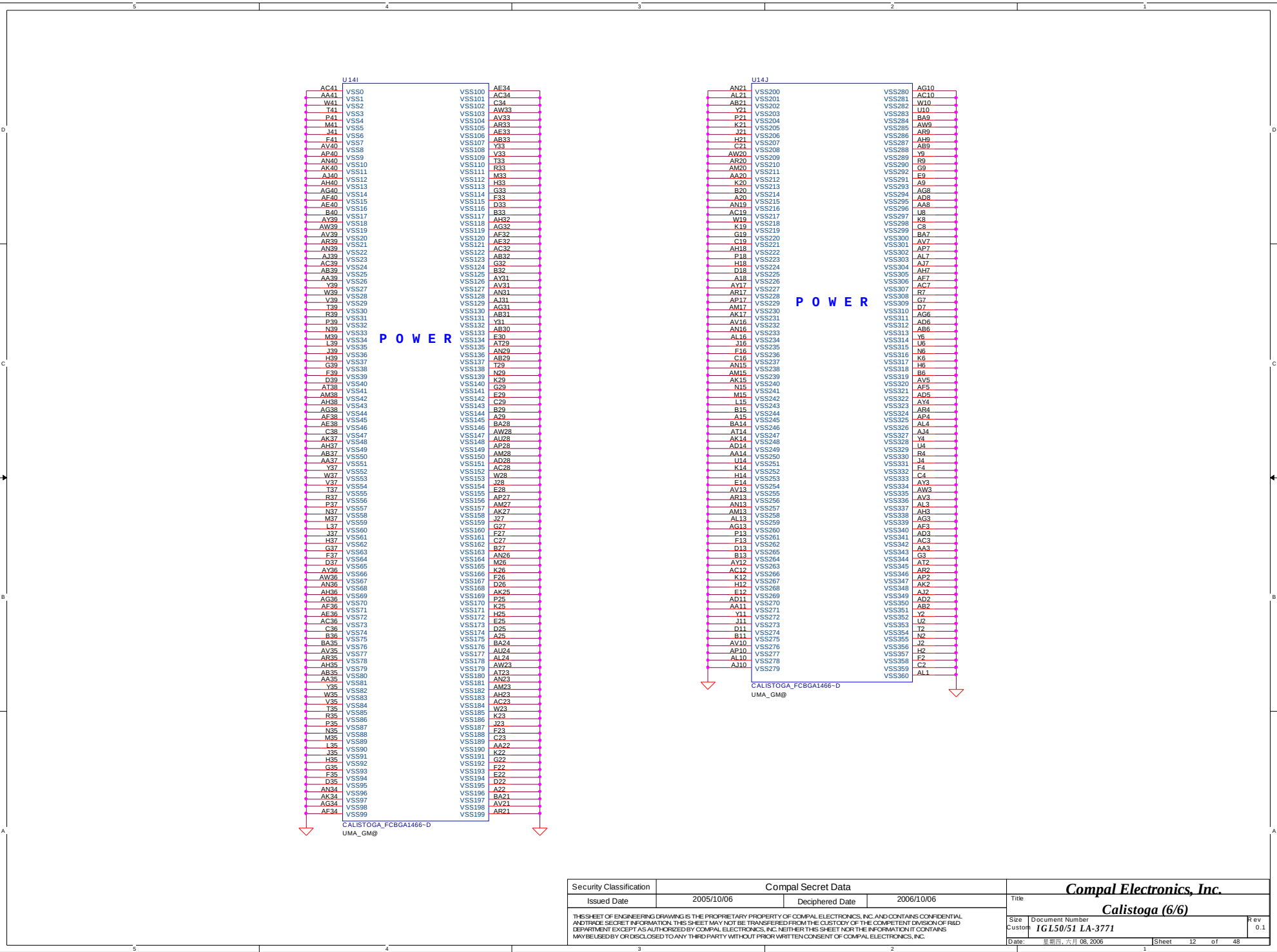


Strap Pin Table

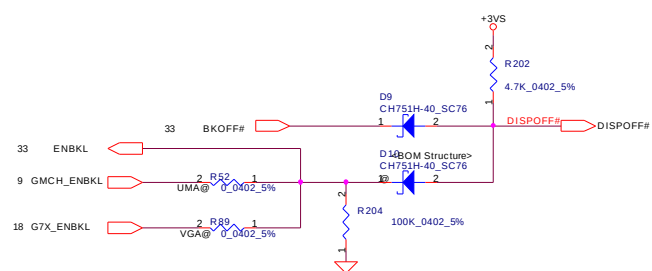
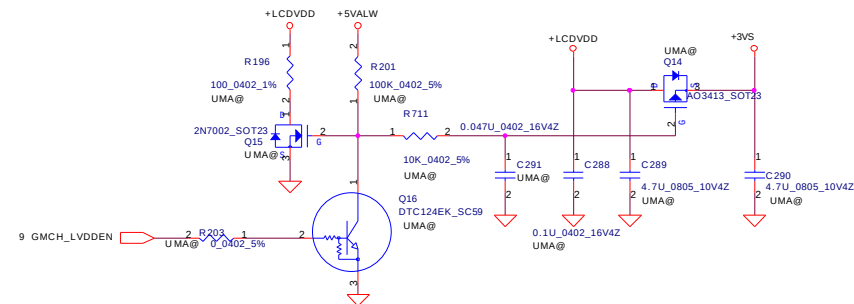
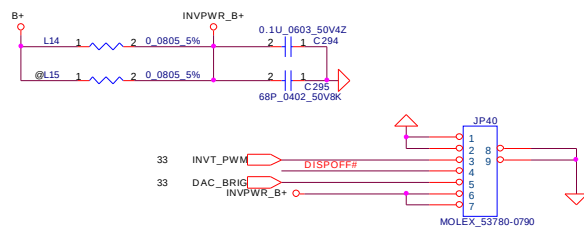
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU* (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG66	0 = Reserved PSB 4X CLK Enable 1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG10 CFG18	10 = 1.05V* (Default) 01 = 1.5V
CFG19	0 = No SDVO Device Present * (Default) 1 = DMI Lane Reversal
SDVO_CTRLDATA	1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.

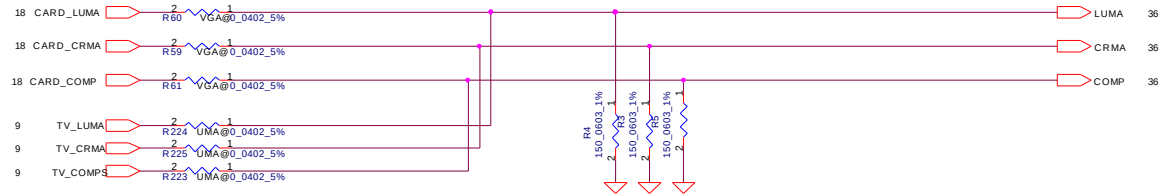




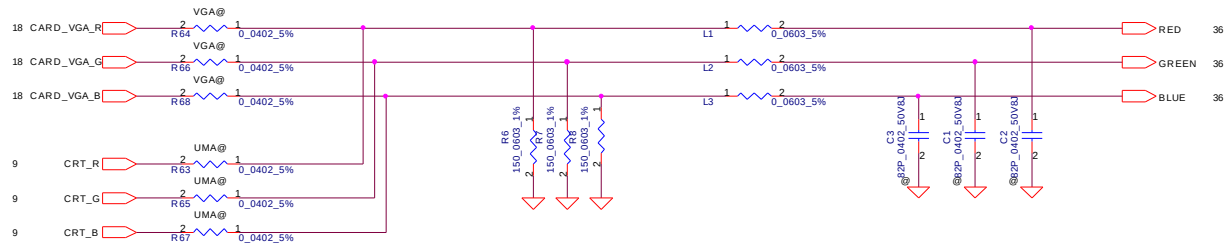




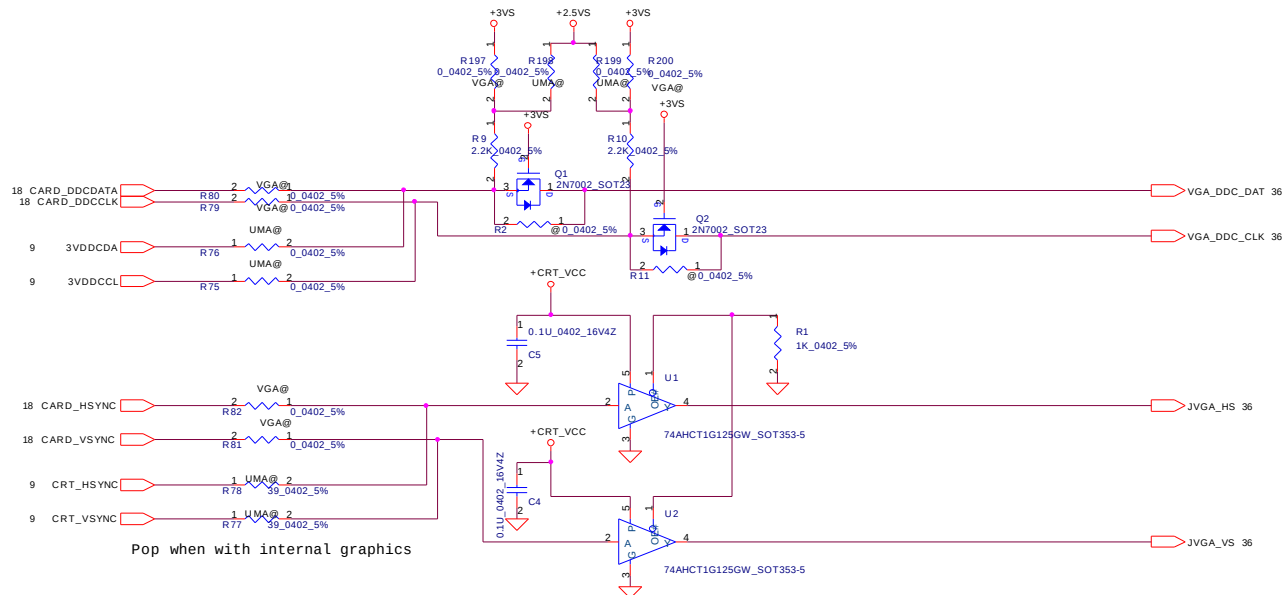
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TV-OUT Conn.

Pop when with internal graphics

CRT Conn.

Pop when with internal graphics

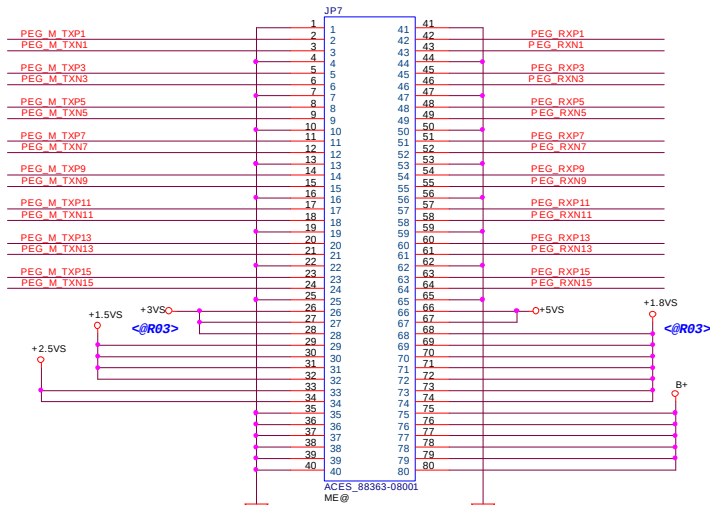


Pop when with internal graphics

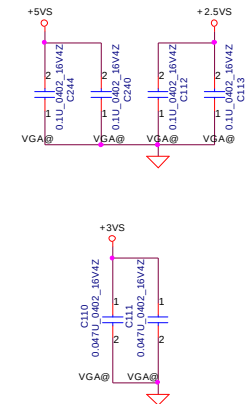
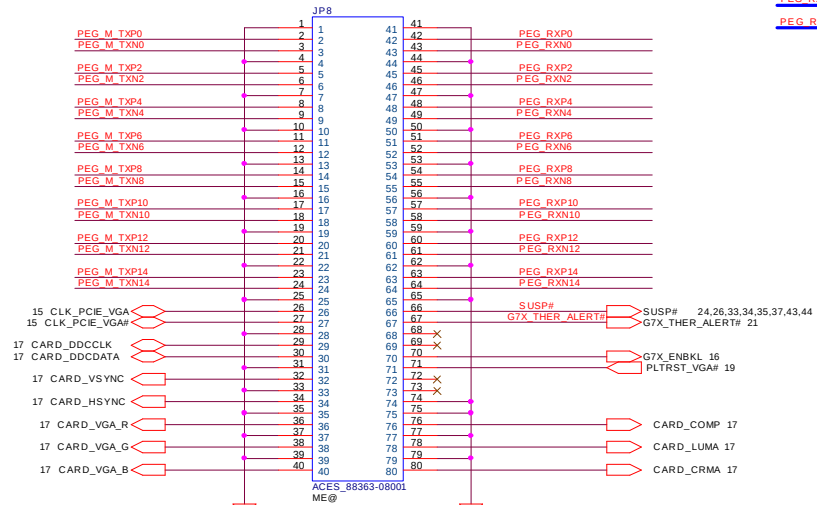
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MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V

PEG_M_TXP[0..15] PEG_M_TXP[0..15] 9
PEG_M_TXN[0..15] PEG_M_TXN[0..15] 9
PEG_RXP[0..15] PEG_RXP[0..15] 9
PEG_RXN[0..15] PEG_RXN[0..15] 9



< New Add Pin.28 for +3VS, Pin.68 for +1.8VS @R03 >

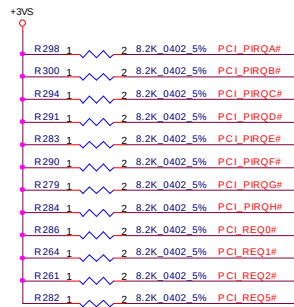
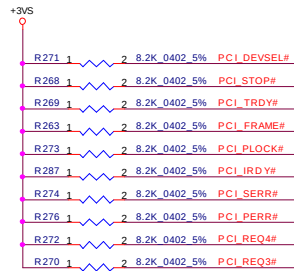


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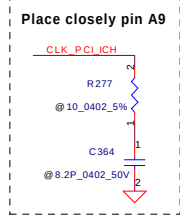
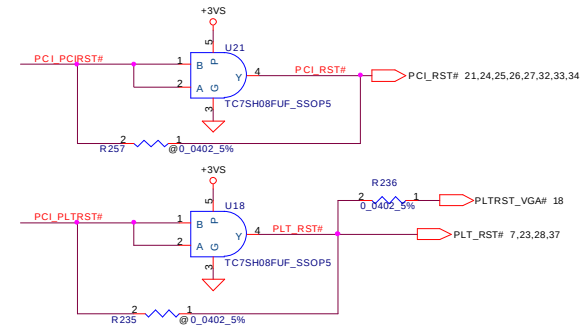
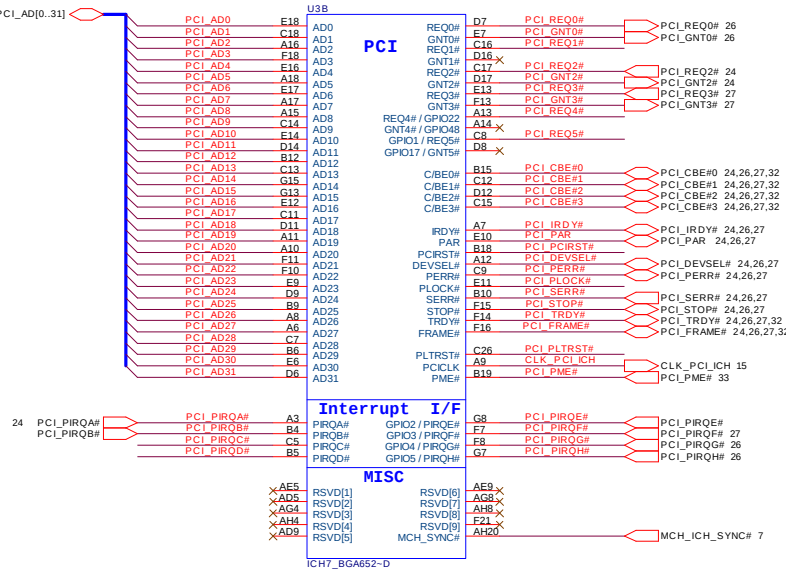
VGA/B connector

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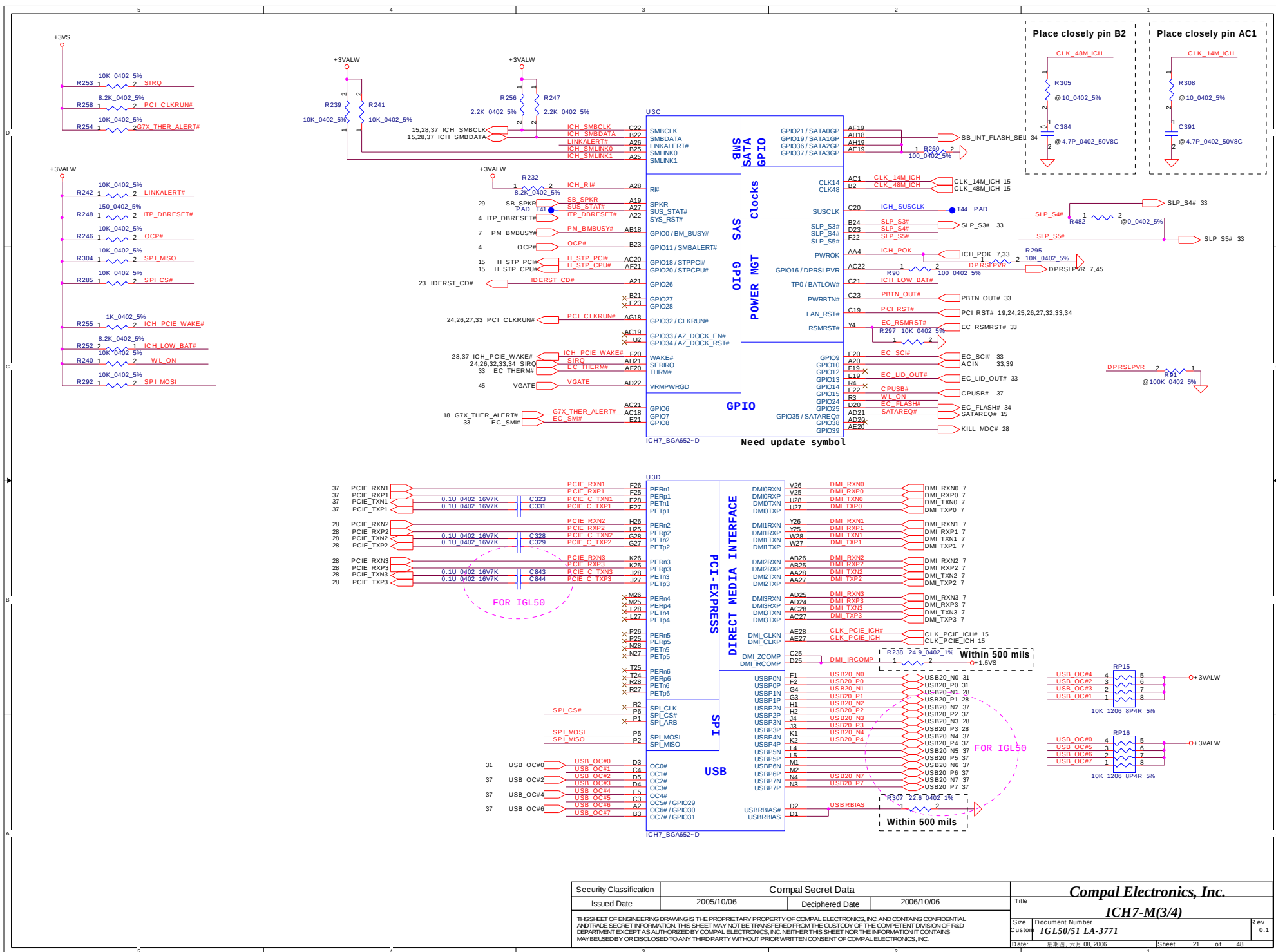


24,26,27,32 PCI_AD[0..31]

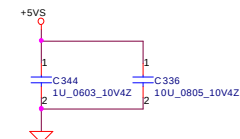
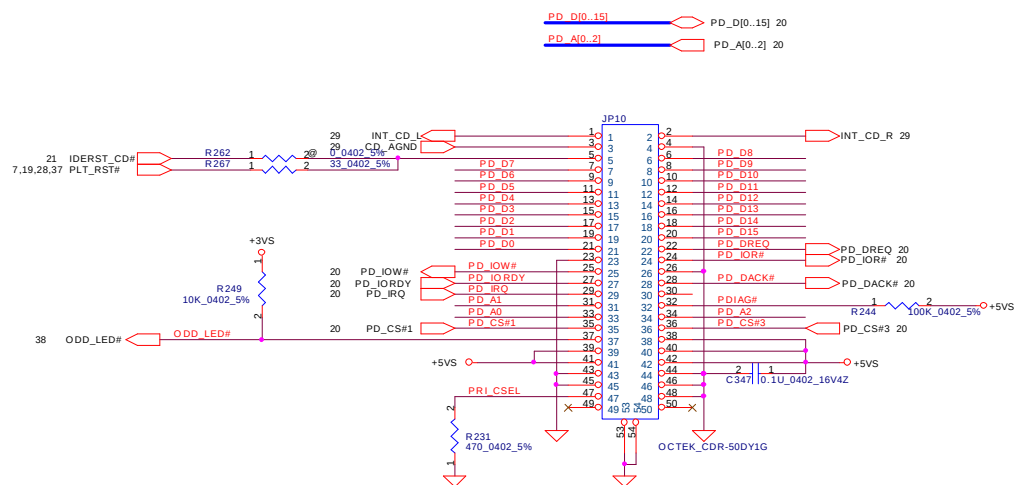
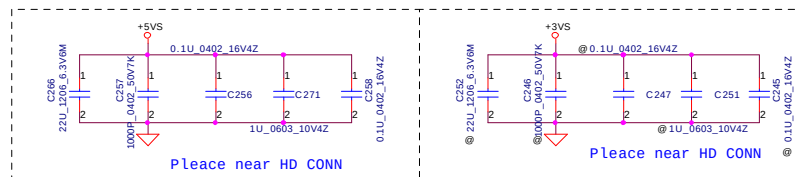
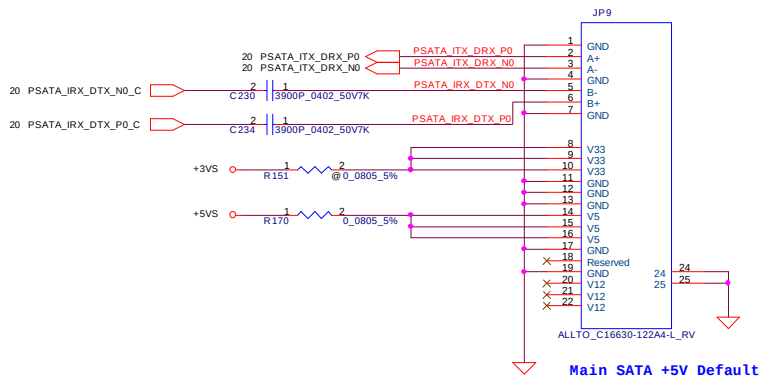


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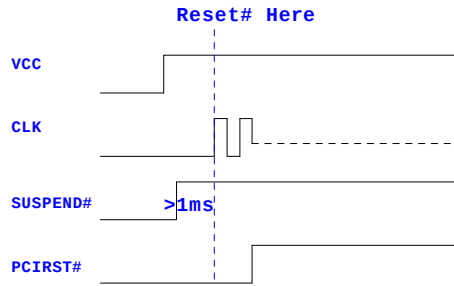


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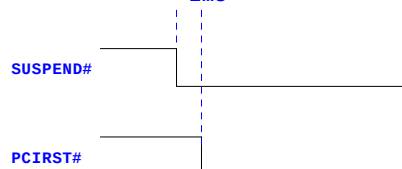


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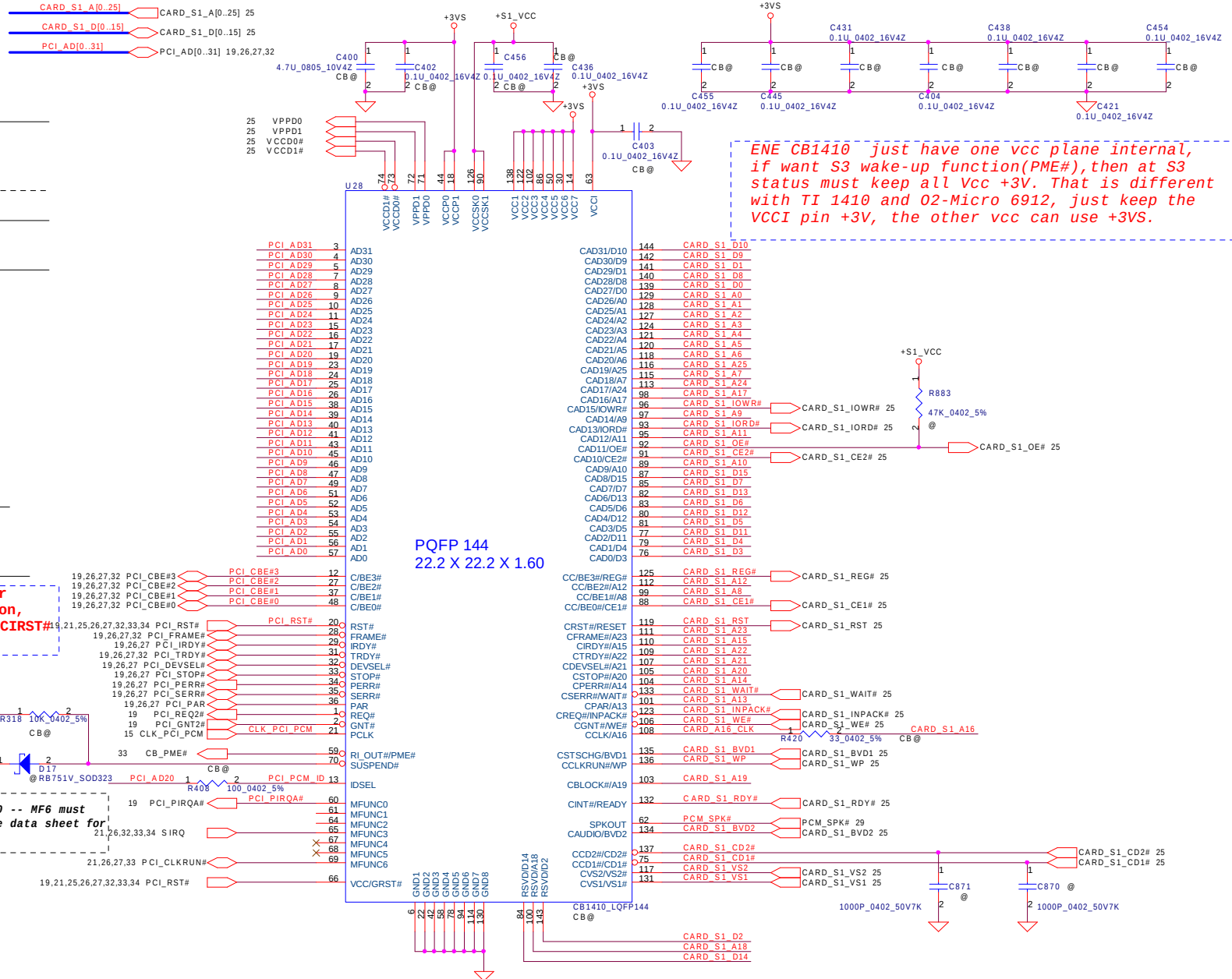
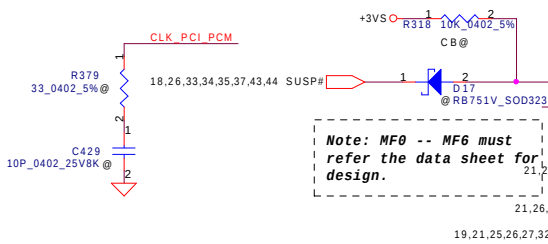
Power on RESET#



Entry S3



SUSPEND# will gate the PCIRST# or GRST#, so need S3 wake up function, SUSPEND# must be LOW ahead the PCIRST# about 1ms.

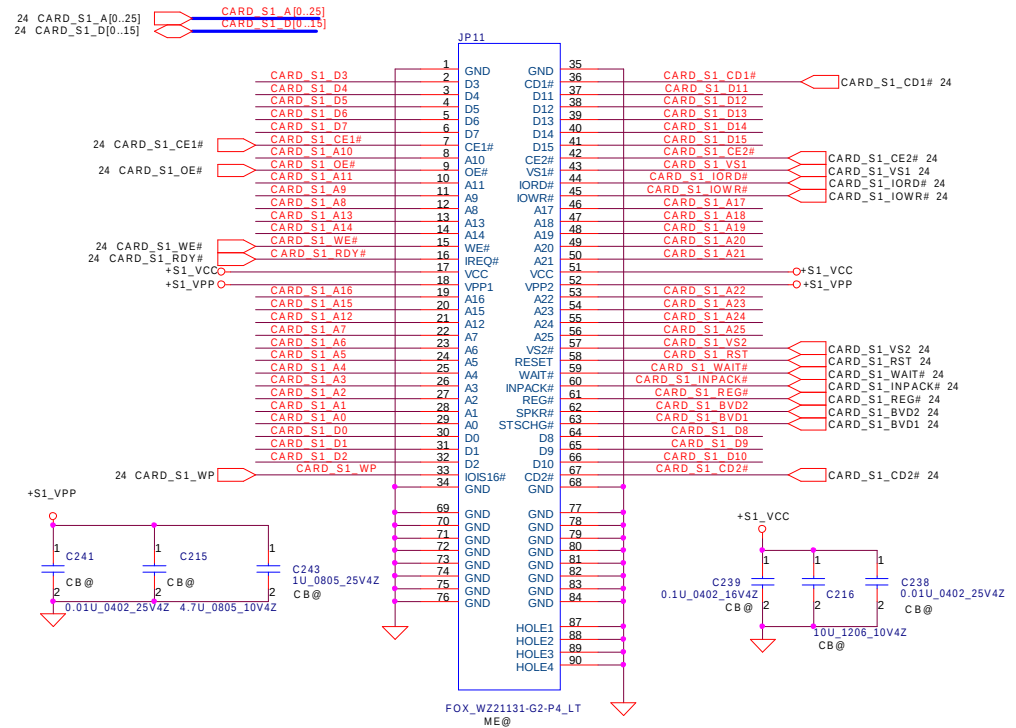
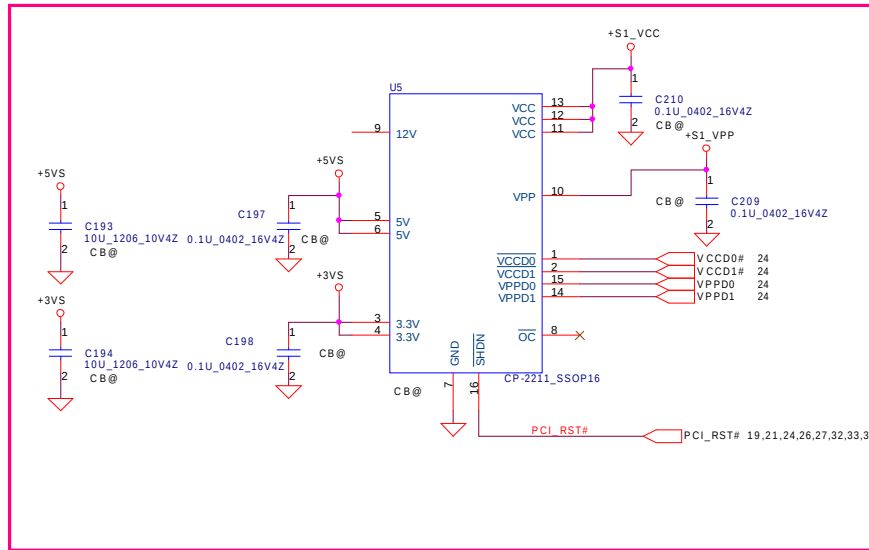


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PROPRIETARY NOTE

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PCMCIA Power Controller



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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title	
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Size		Document Number		Rev	
Cust		I9GL50/51 LA-3771		0.1	
Date		2006/10/06		Sheet 25 of 48	

R5C832

SD,MMC,MS,XD multi-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			XDCD1#	
MDIO02			XDCD#	
MDIO03	SDWP#		XDR/B#	
MDIO04	SDPWR0	MMCPWR	MSWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLD#	MSLED#	XDLED#
MDIO07			MSEXTCK	
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCLK	MMCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1		MSCDAT1	XDCDAT1
MDIO12	SDCDAT2		MSCDAT2	XDCDAT2
MDIO13	SDCDAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLLE
MDIO19				XDALE

Function set pin define

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card

Layout Note: Place close to R5C832 and Shield GND for SDCLK, MSCLK

Layout Note: Place close to R5C832 and Shield GND for SD, CLK

Solve MS Duo Adaptor short problem

Layout Note: Shield GND for CBS, CLK, INTERNAL and CBS, CLK

Layout Note: Shield GND for IEEE1394, TPA and TPB

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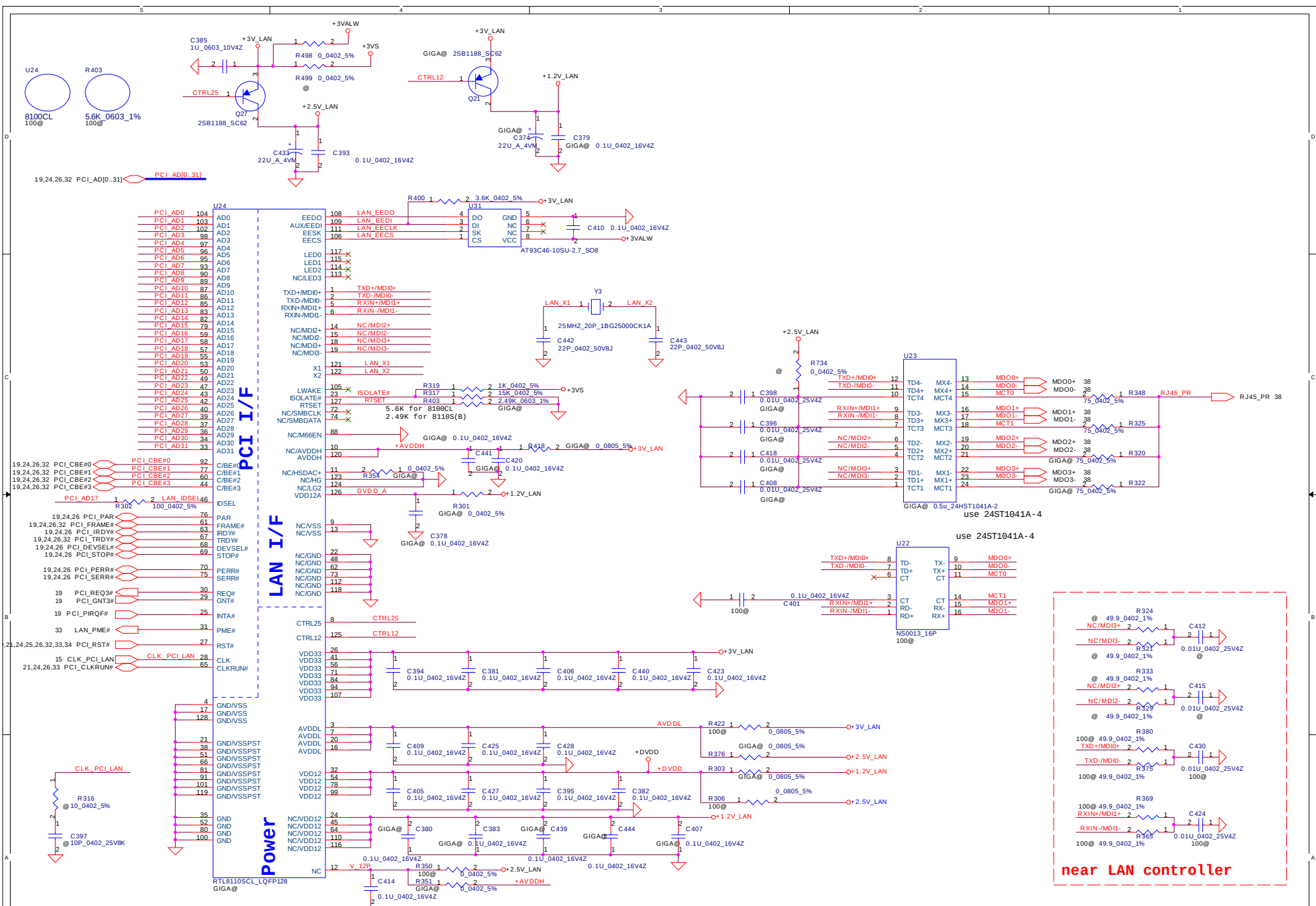


Compal Electronics, Inc.

1394+3 in 1 Card

HGT30/31 LA3061

Date: 2005.08.05 Sheet: 26 of 48



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Issued Date		2005/10/06	Deciphered Date	2006/10/06	Title		
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					Size	Document Number	Rev
					Cust	1GL50/51 LA-3771	0.1
					Date:	星期四, 六月 08, 2006	
					Sheet	27	of 48

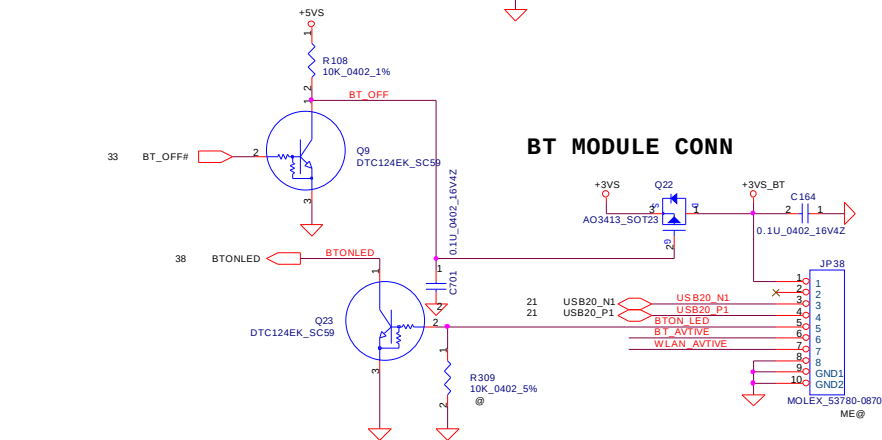
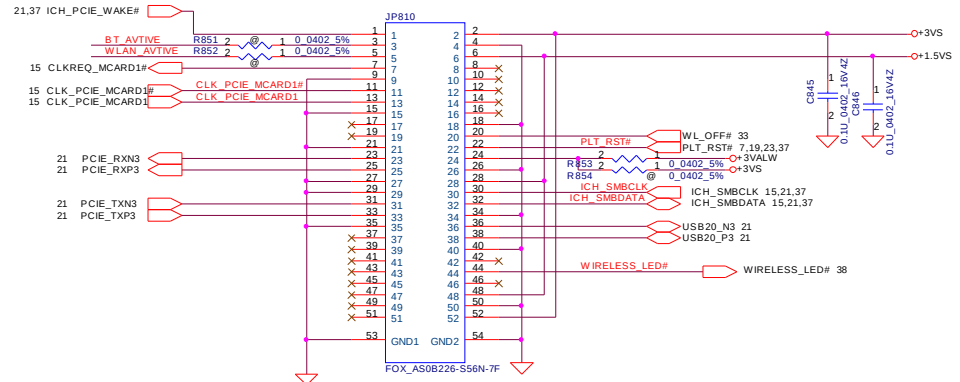
near LAN controller

Compal Electronics, Inc.

LAN CONTROLLER

Size: 100mm x 100mm
Customer: IGL50/51 LA-3771

Mini-Express Card(Slot 2-WLAN)



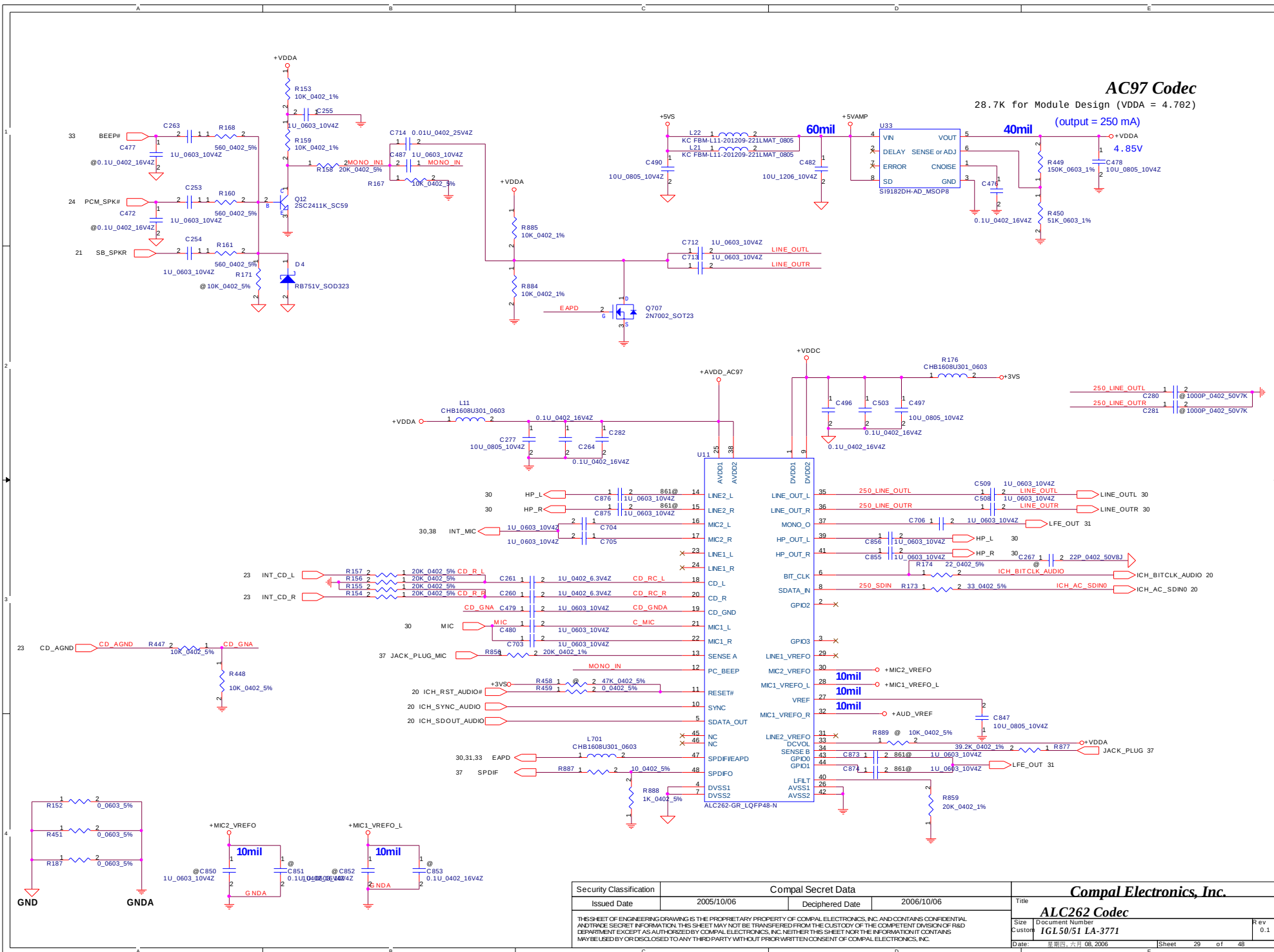
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title	Mini Card / MDC CONN
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				Custom	1GL50/S1A-3771
Date: 星期日, 六月 08, 2006				Sheet	28 of 48

AC97 Codec

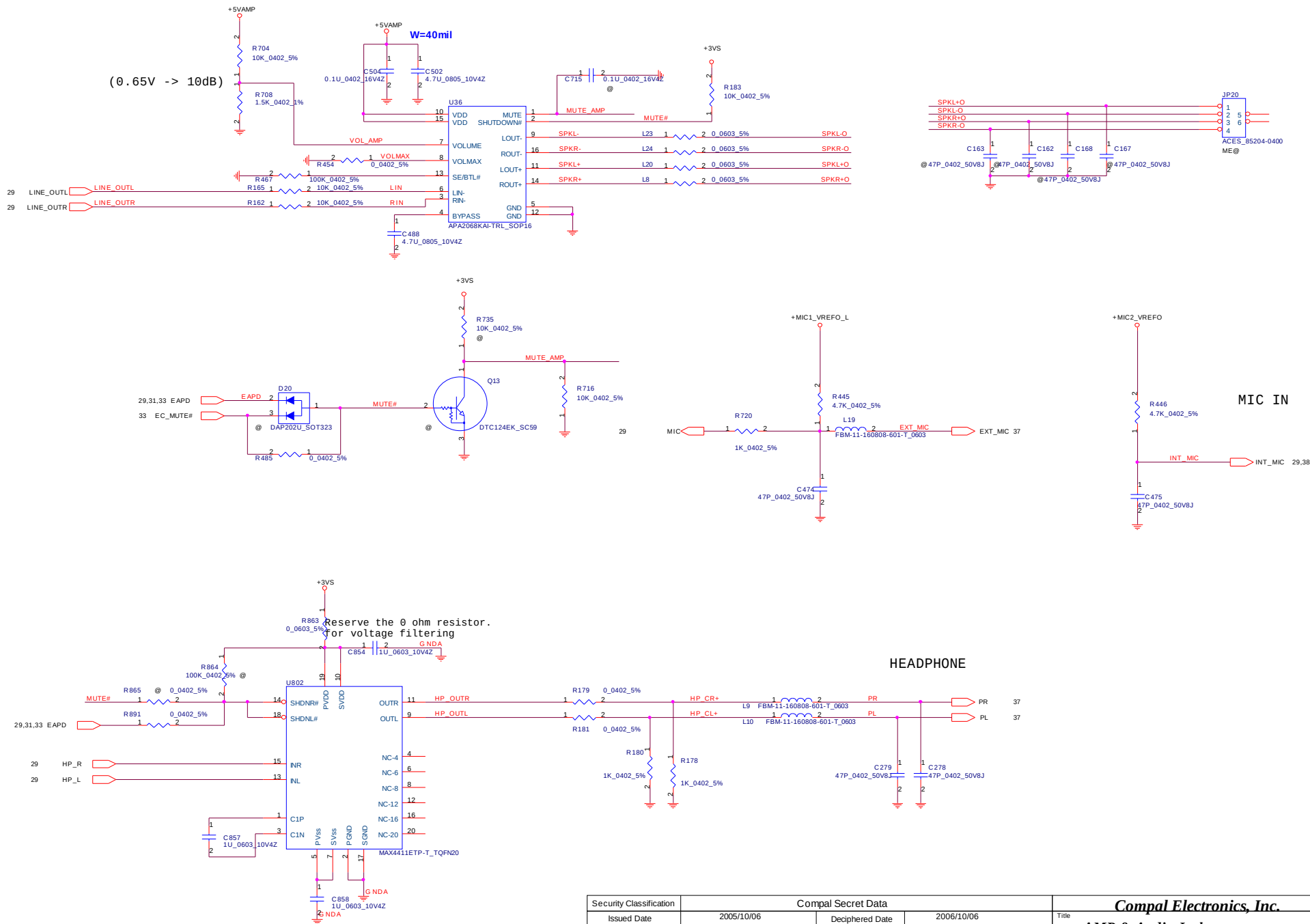
28.7K for Module Design (VDDA = 4.702)

(output = 250 mA)

4.85V



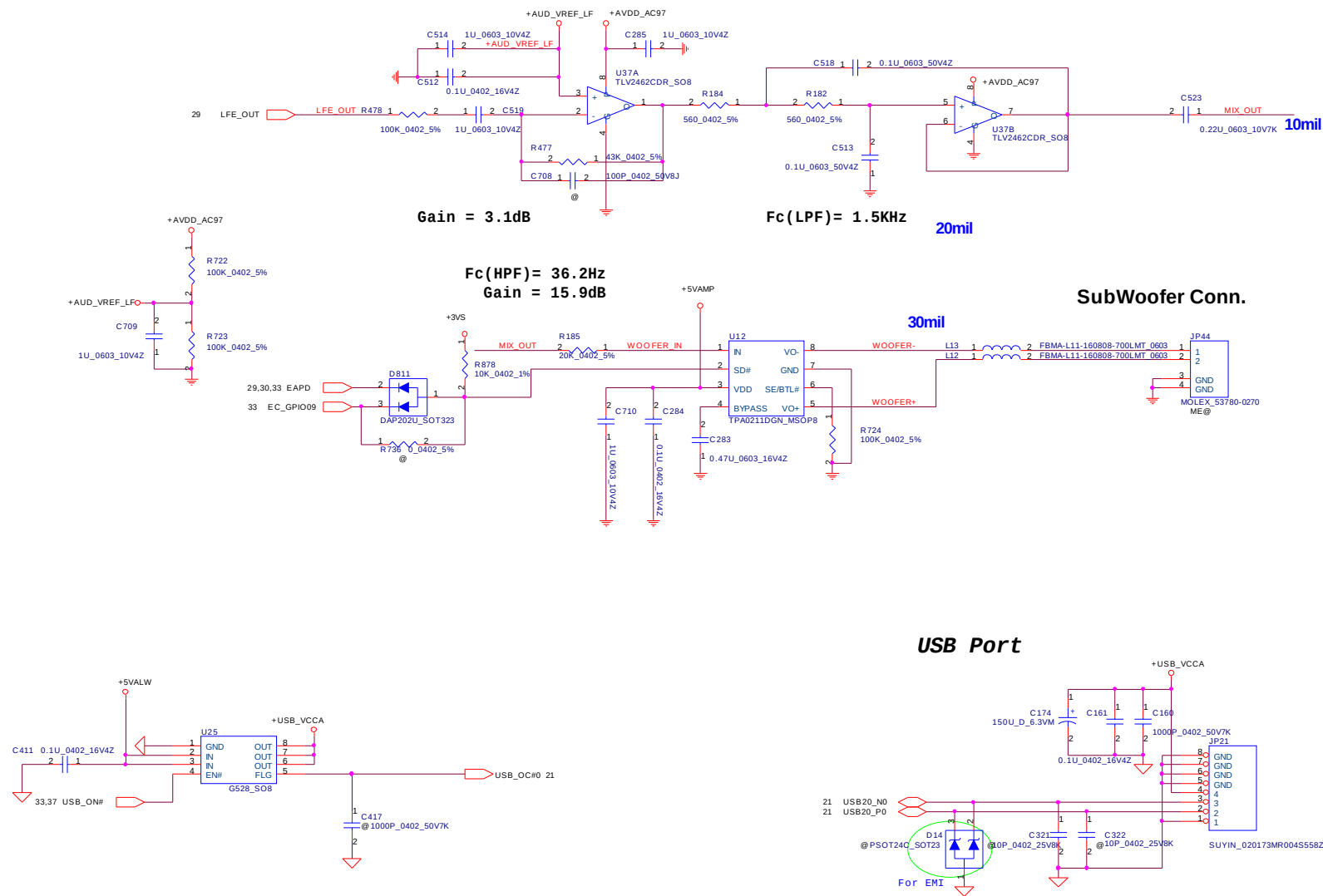
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2005/10/06		2006/10/06		ALC262 Codec	
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		Customer		IGL50/51 LA-3771	
		Date		Rev	
		2006/06/08		0.1	
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Compal Electronics, Inc.	
AMP & Audio Jack	
Size	Document Number
Custom	IGL50/51 LA-3771
Date:	Rev 0.1
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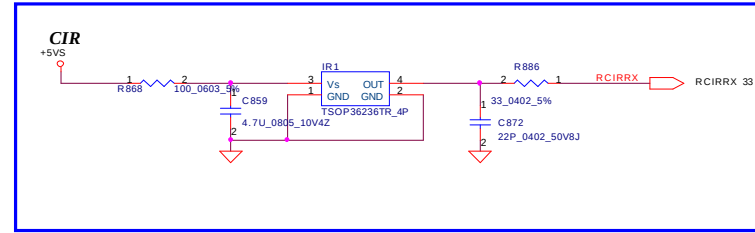
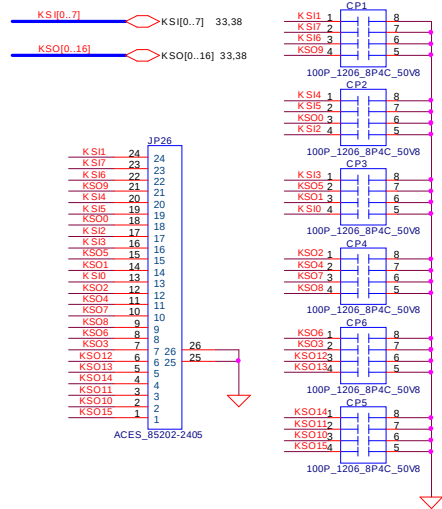
SUBWOOFER (Reserved for C38)

WOOFER@

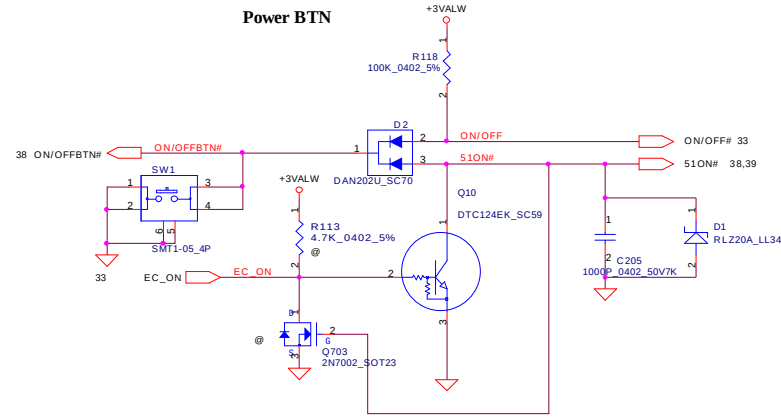


Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2006/10/06	
2005/10/06		2006/10/06		Compal Electronics, Inc.	
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1GL50/51 LA-3771		0.1		Date: 星期四, 六月 08, 2006	
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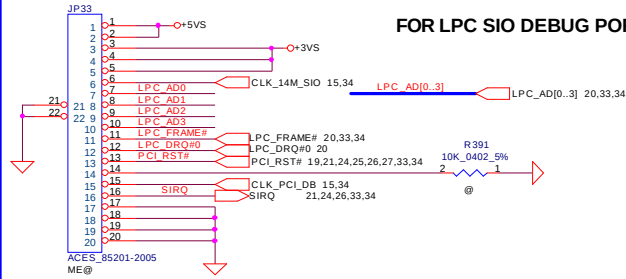
INT_KBD CONN.(TYPE "D" KB)



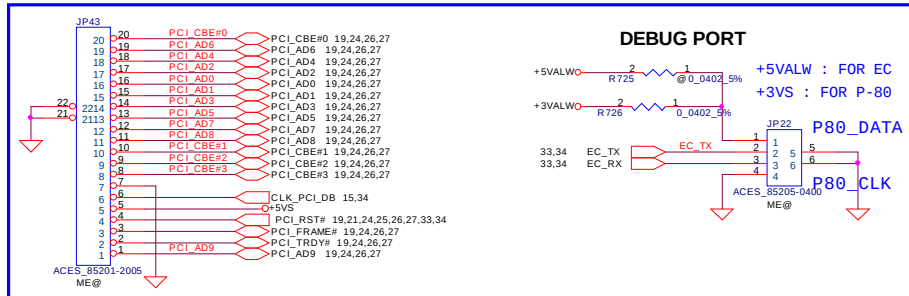
Power BTN



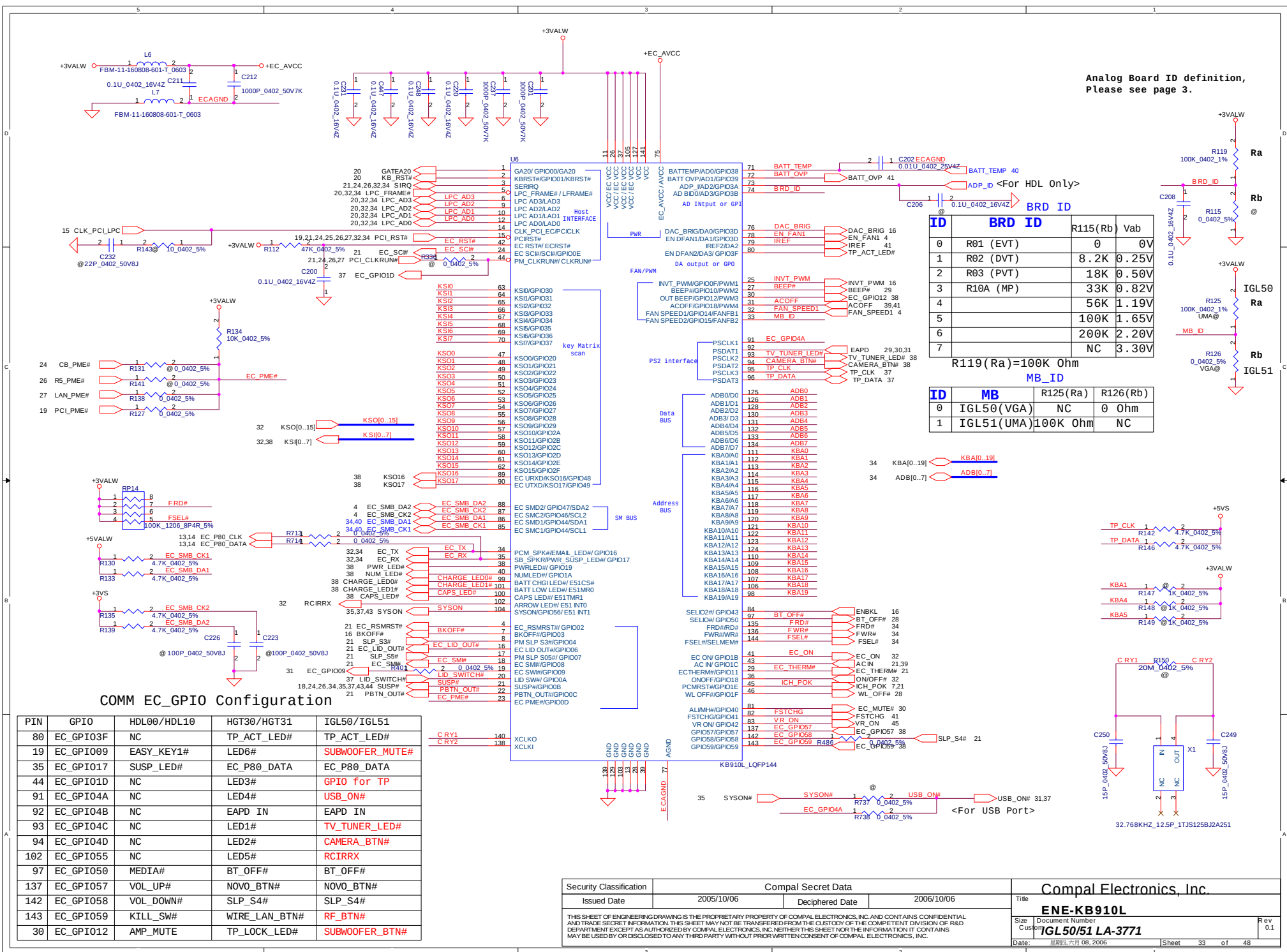
FOR LPC SIO DEBUG PORT

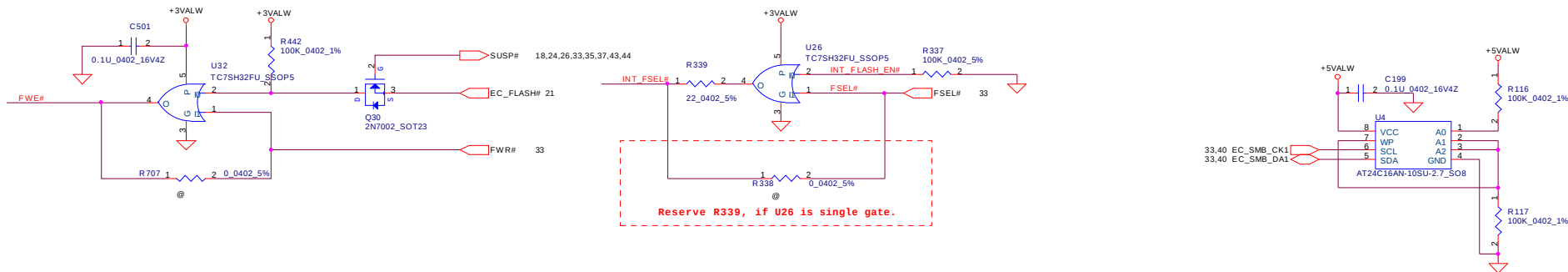


DEBUG PORT



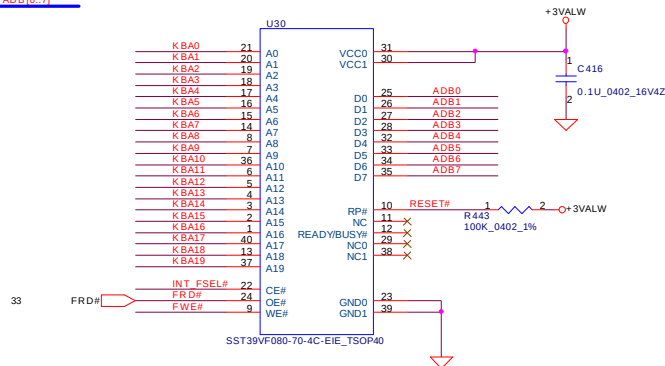
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2005/10/06		2006/10/06		KBD,ON/OFF,T/P,LED/B,DEBUG	
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				IGL50/51 LA-3771	
				Rev	
				0.1	
				Date: 星期日, 六月 08, 2006	
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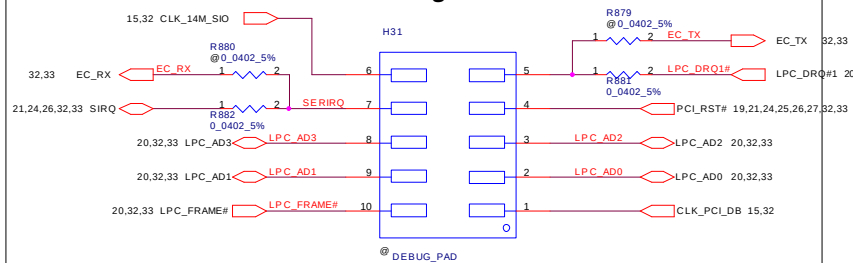


33 KBA[0..19] KBA[0..19]
 33 ADB[0..7] ADB[0..7]

1MB Flash ROM



New LPC Debug Pad ---- MB side



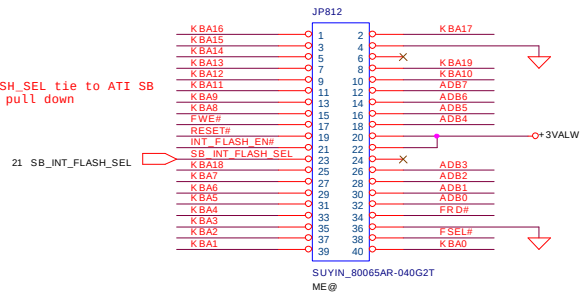
Under DDR ME Assignment Area

Keep Resistor near Debug Pad and in the same side

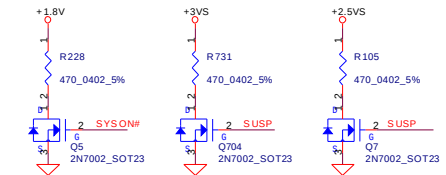
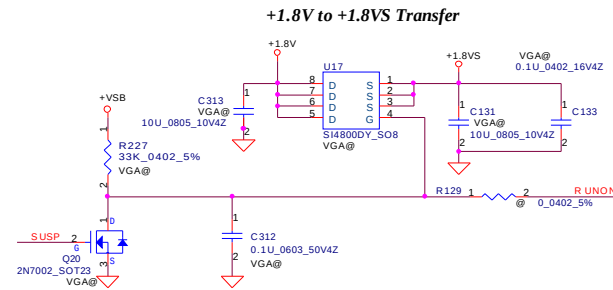
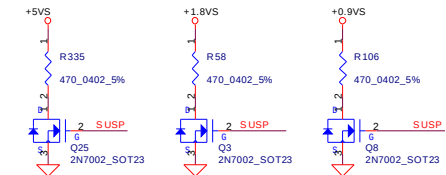
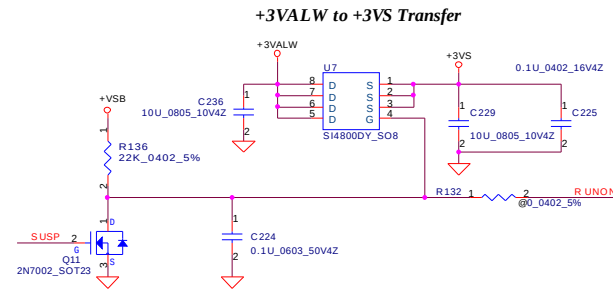
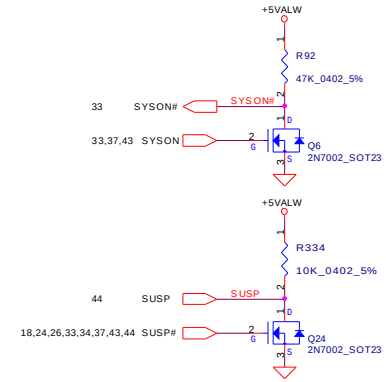
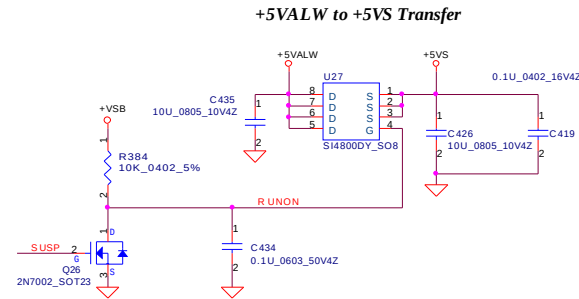
Standard side DIMM ---- Pin 1 near DIMM

Reverse side DIMM ---- Pin 1 keep away DIMM

Change to small socket for ROM part

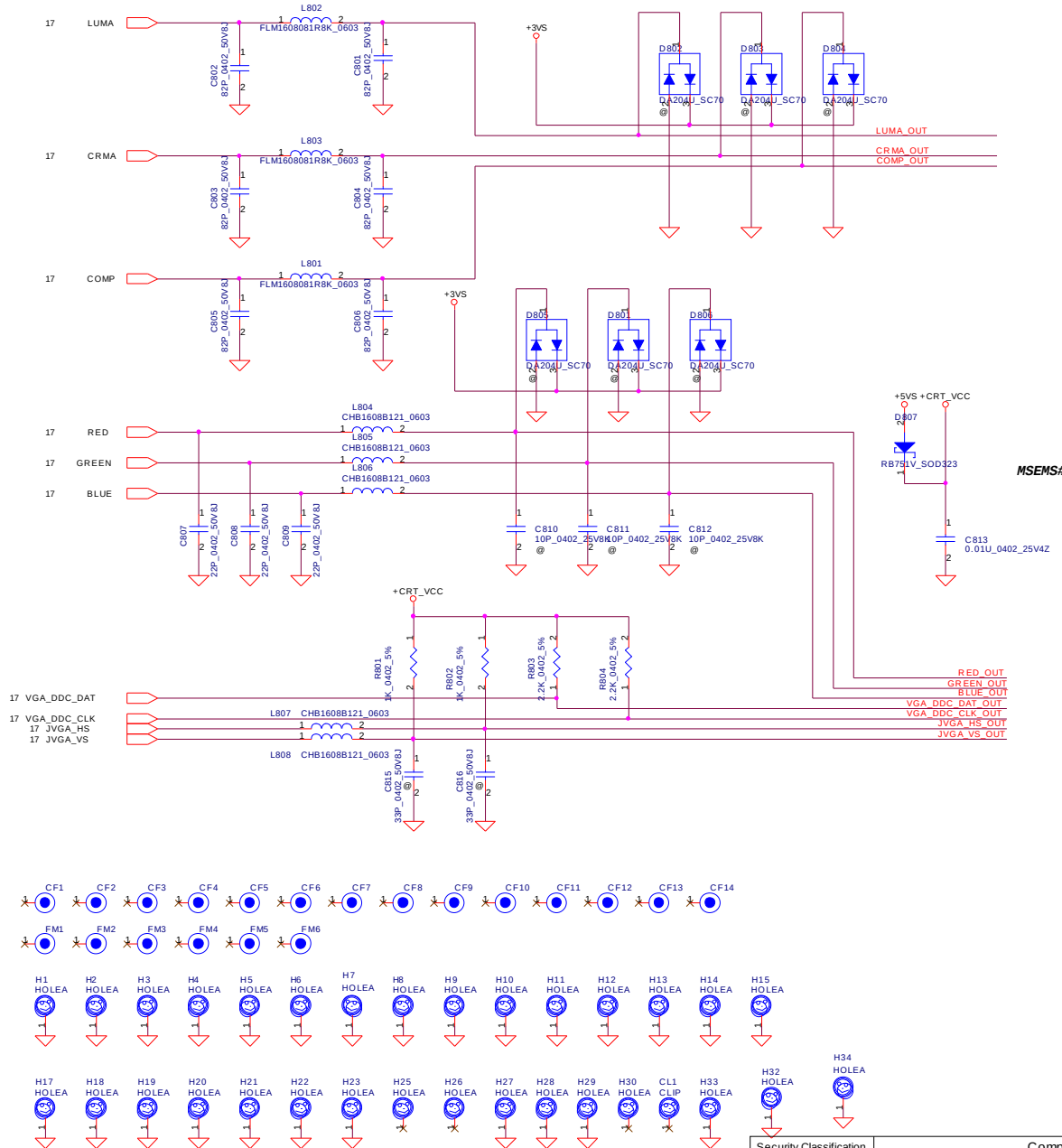


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Size	Custom	Document Number	Rev	
		1GL50/51 LA-3771	0.1	
Date:	星期四, 六月 08, 2006	Sheet	34	of 48



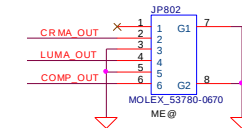
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title
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Size	Document Number	Rev		0.1
Custom	1GL50/51 LA-3771	Date		星期四, 六月 08, 2006
		Sheet	35	of 48

CLOSE TO JTVOUT1

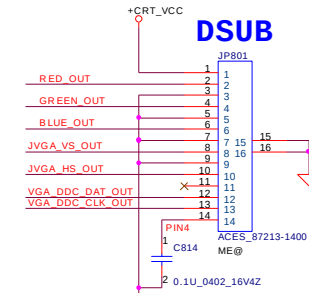


VGA I/O PORT Connector

S-VIDEO



DSUB



PIN ASSIGMENT

PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYNC			
9	10	GND			
10	13	HSYNC			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			

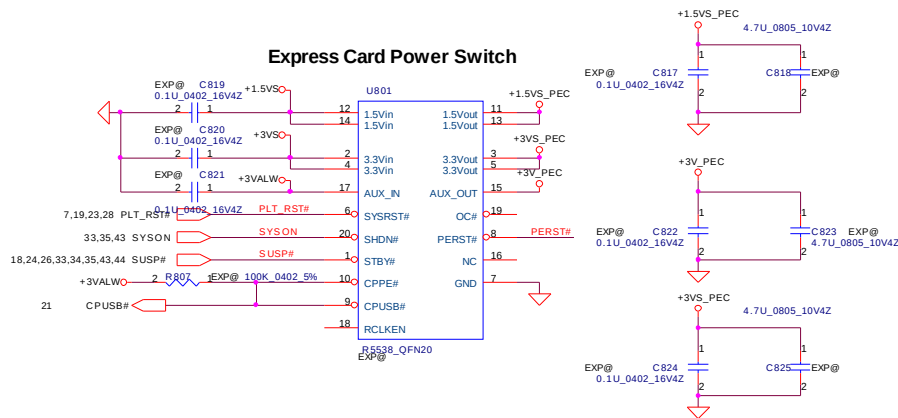
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Document Number
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Date: 星期日, 六月 08, 2006				Sheet 36 of 48

Compal Electronics, Inc.

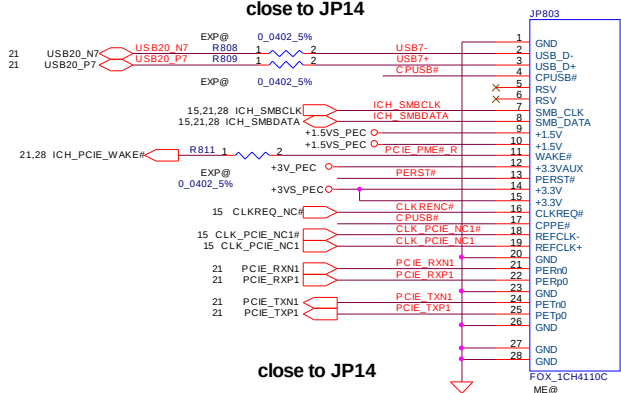
CRT & TVout Connector

IGL50/51 LA-3771

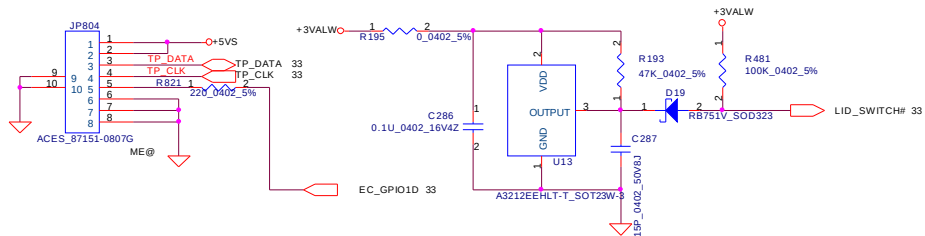
NEW CARD FOR C38



close to JP14

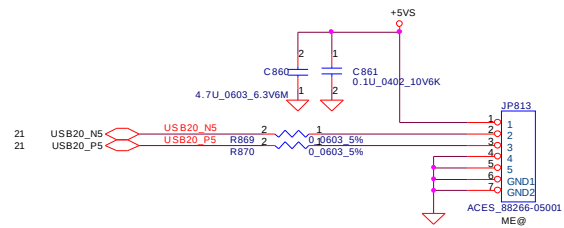


T/P Board



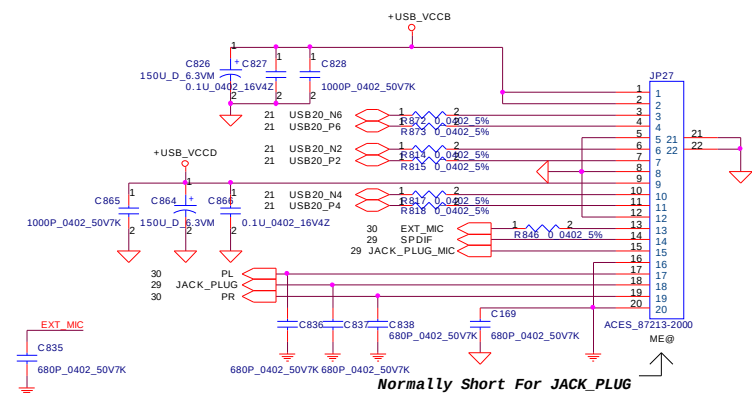
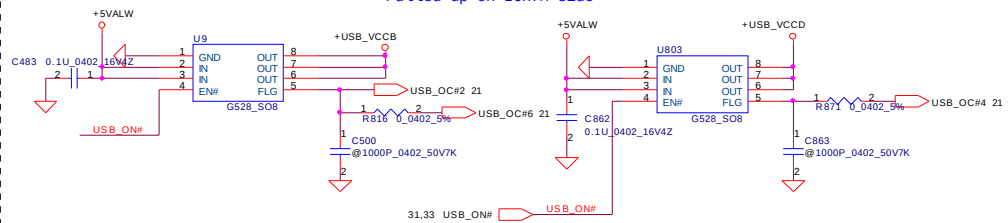
LID Switch

CMOS Camera Conn



USB board

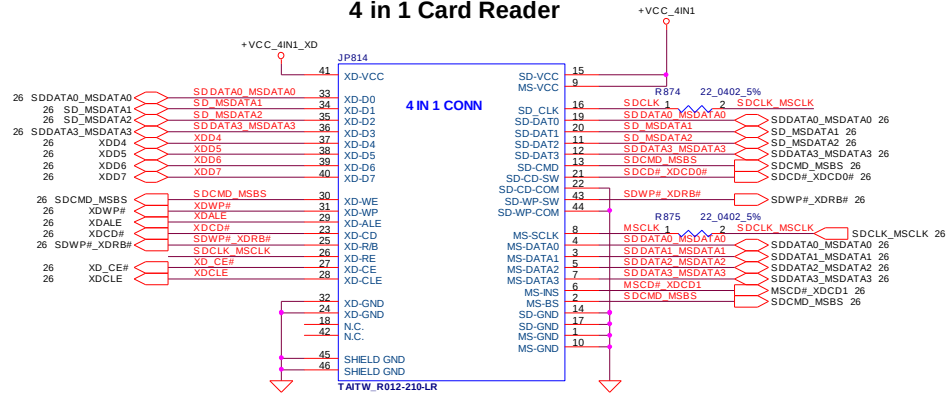
Pulled up on ICH7M side



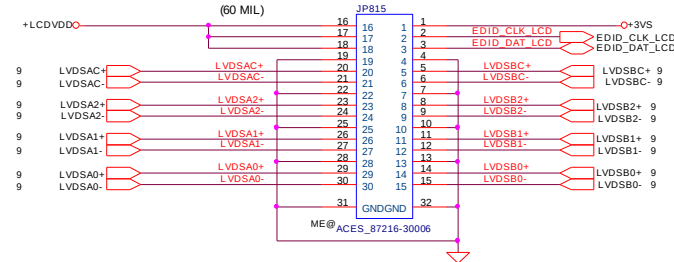
C835 ~ C838 For EMI Solution

Security Classification		Compal Secret Data		Compal Electronics, Inc. INDICATE LED	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	Rev. 0.
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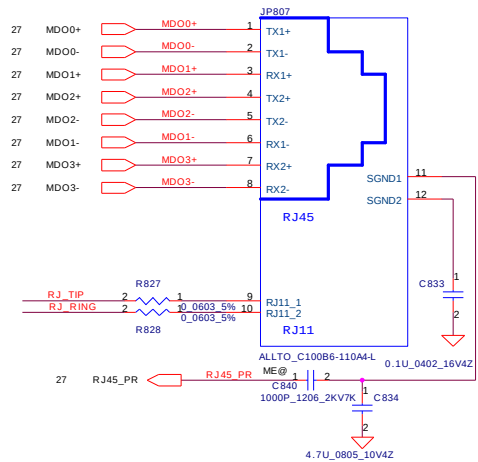
4 in 1 Card Reader



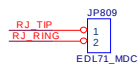
UMA LCD/PANEL Conn.



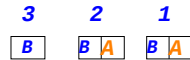
RJ11+RJ45 CONN



MDC CONN



LED Indicator



Wireless / Bluetooth LED

BATT_CHG_LED#

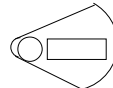
BATT_LOW_LED#

STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

Function

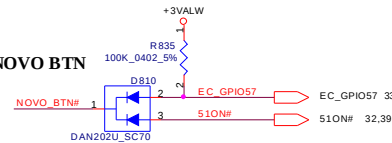
KEY Matrix	K016	K017
KSI0	DW-UP	DW-DOWN
KSI1	DW-ENTER	MUTE

Dial Wheel



NOVA_BTN#

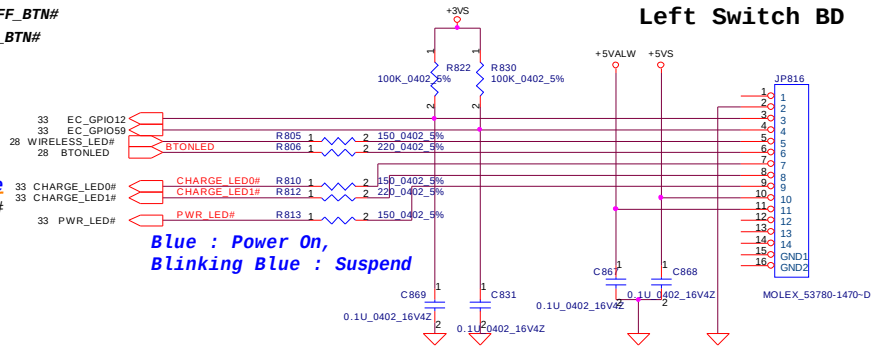
NOVO BTN



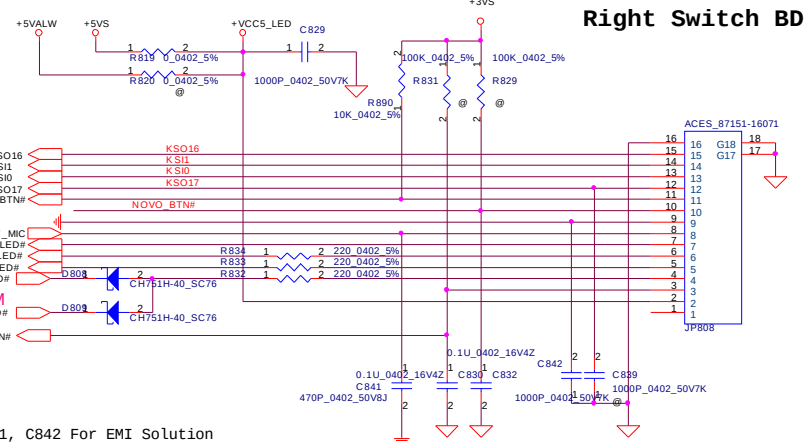
SUBWOOFER_ON/OFF_BTN#

RF_ON/OFF_BTN#

Left Switch BD

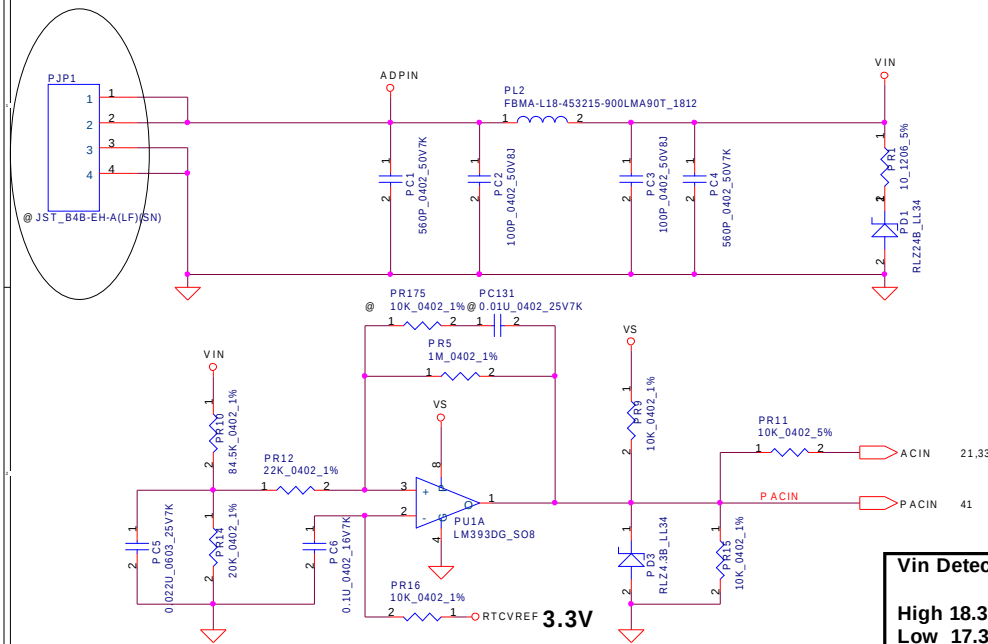


Right Switch BD

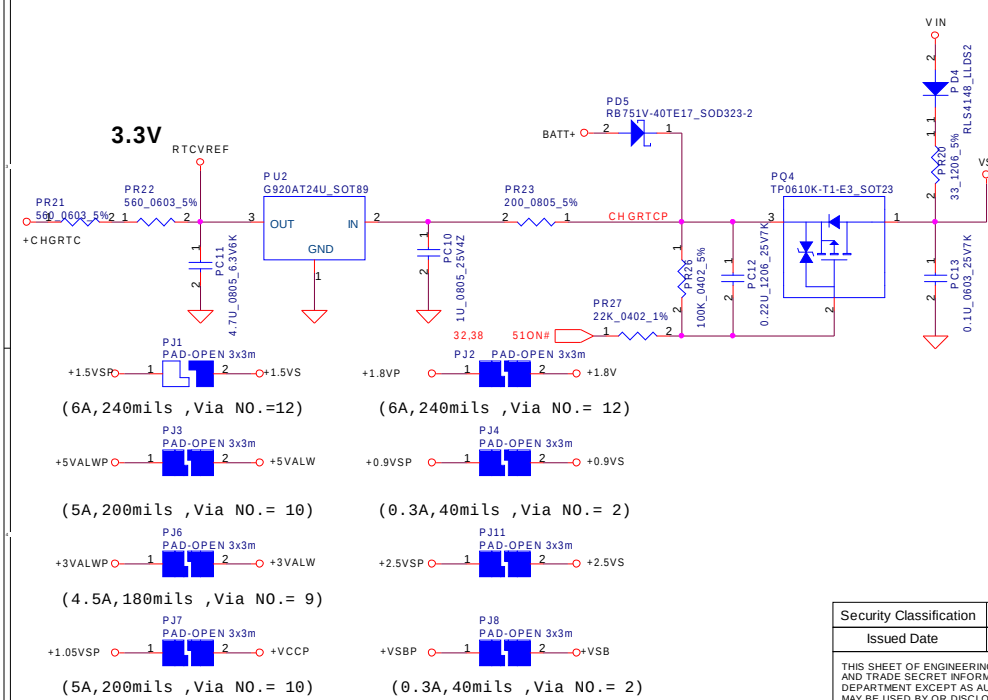


C839, C841, C842 For EMI Solution

Security Classification	Compal Secret Data	Title	INDICATE LED
Issued Date	2005/03/10	Deciphered Date	2006/03/10
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		Custom	ICL 50/51 LA-3771
		Date	Rev 0.1
		Sheet	38 of 48

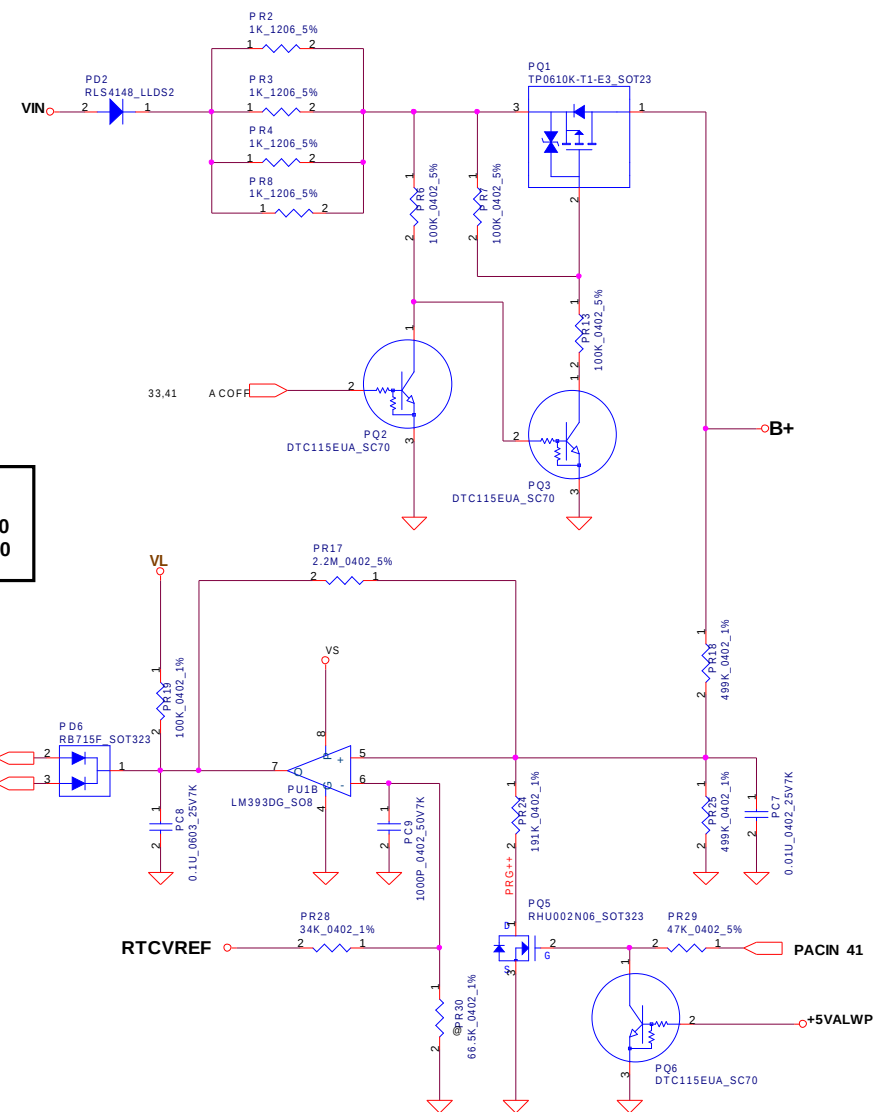


Vin Detector			
High	18.384	17.901	17.430
Low	17.370	16.907	16.630

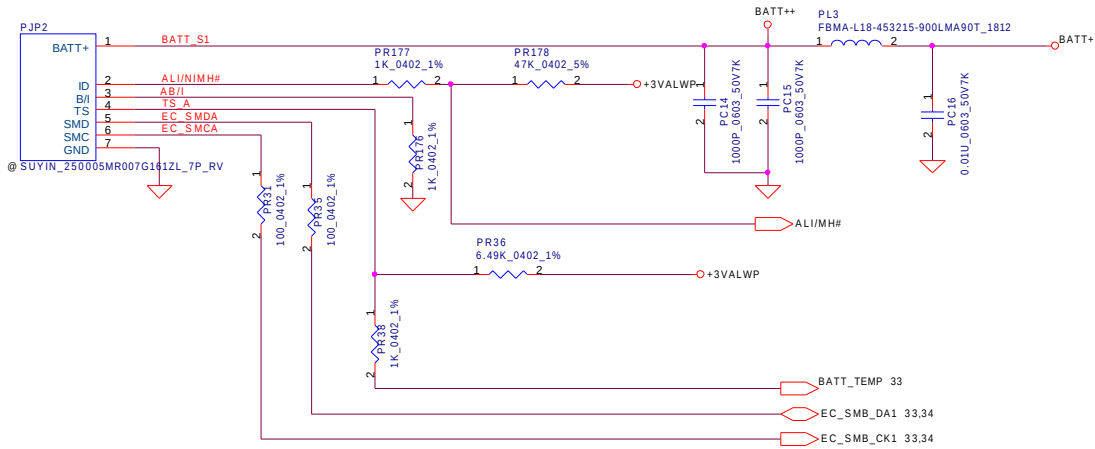


ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.620V	14.853V	15.245V
L-->H	15.534V	15.970V	16.421V

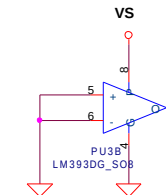
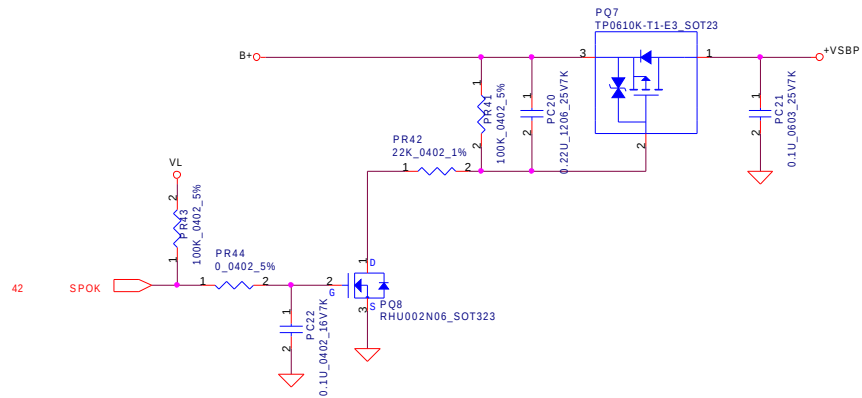
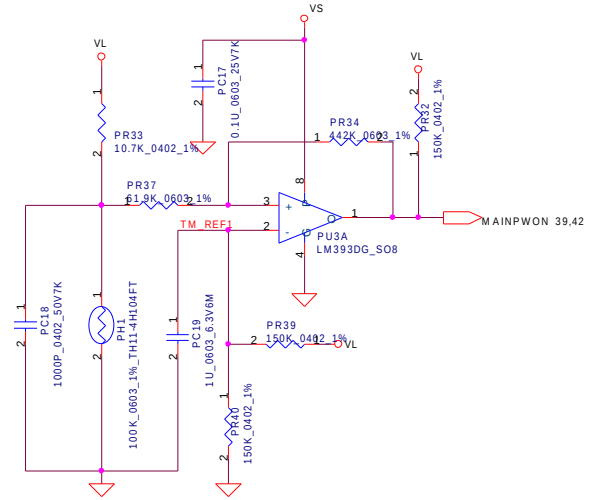
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.169V	6.231V	6.361V
L-->H	7.168V	7.349V	7.537V



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PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C

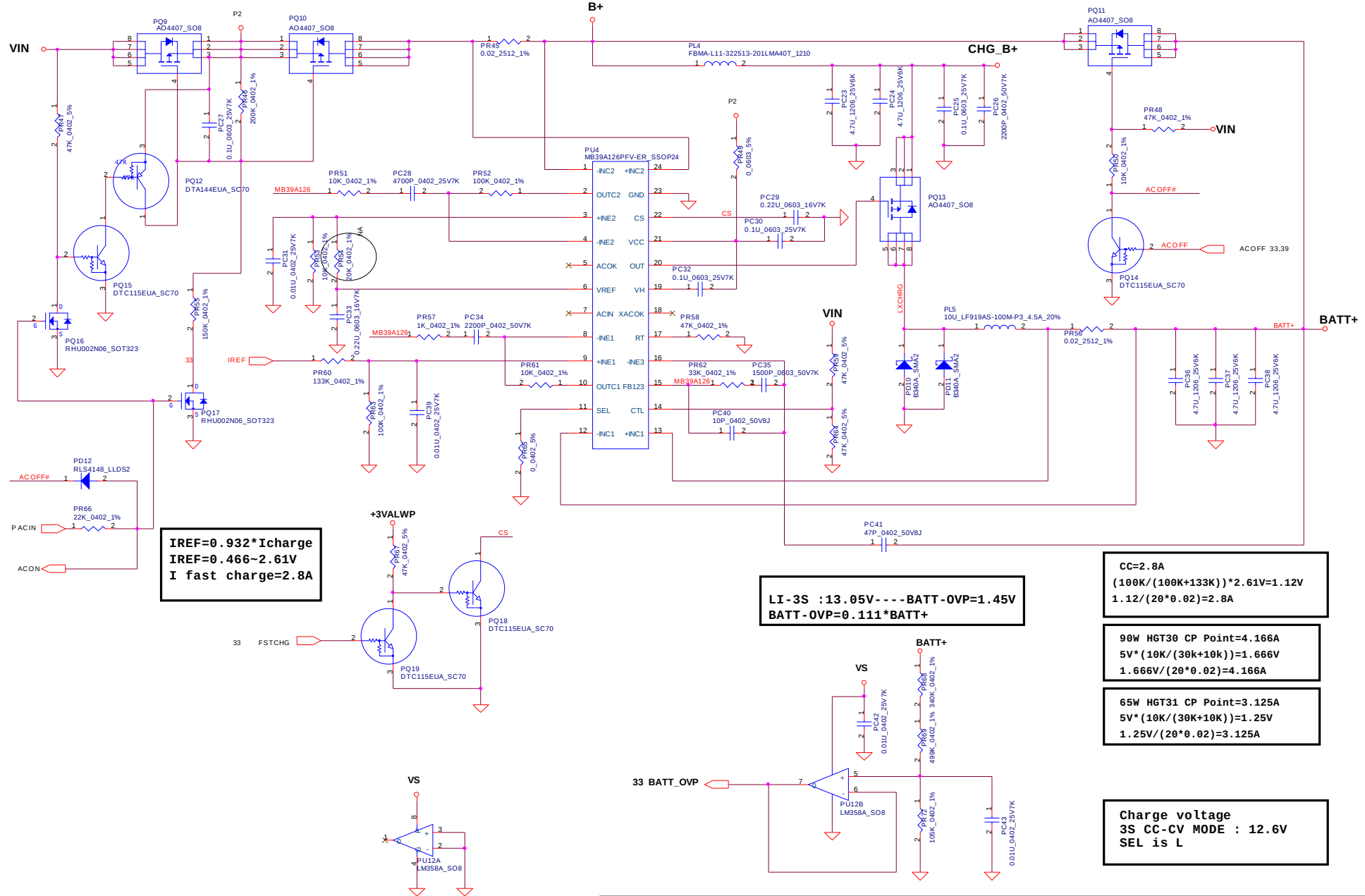


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Size	B	Document Number		Date:	Rev
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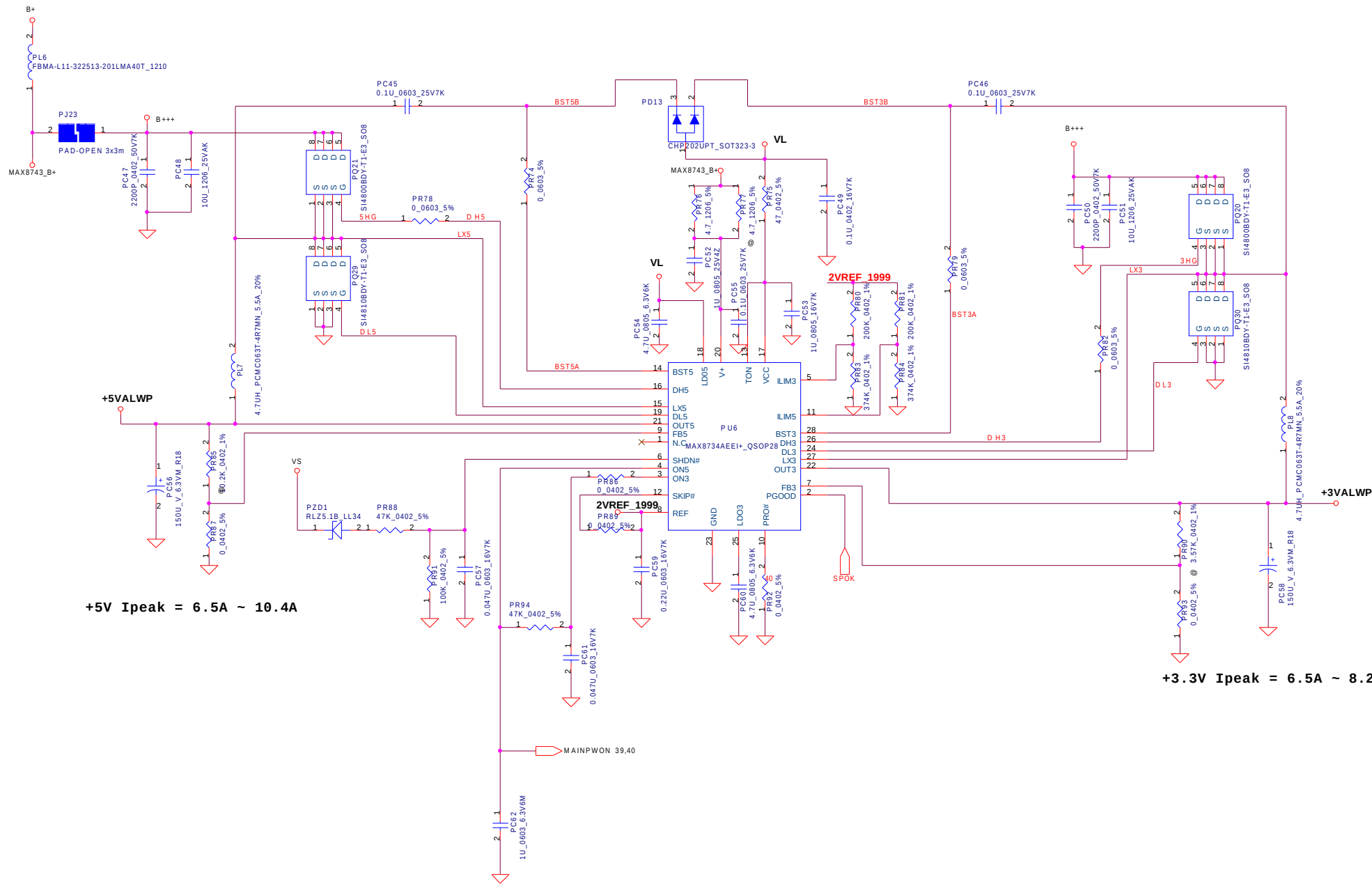
65W PR45=0.02_2512_1% PR54=30K_0402_1% Iadp=0~3.125A
90W PR45=0.02_2512_1% PR54=20K_0402_1% Iadp=0~4.166A

Fosc=14100/Rt=14100/47=300KHz

Charger

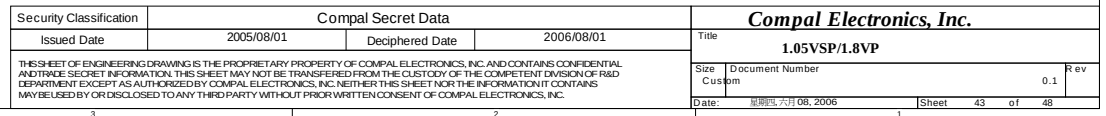


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				PWR-Charger		
Size	Document Number				Rev	
B					0.1	
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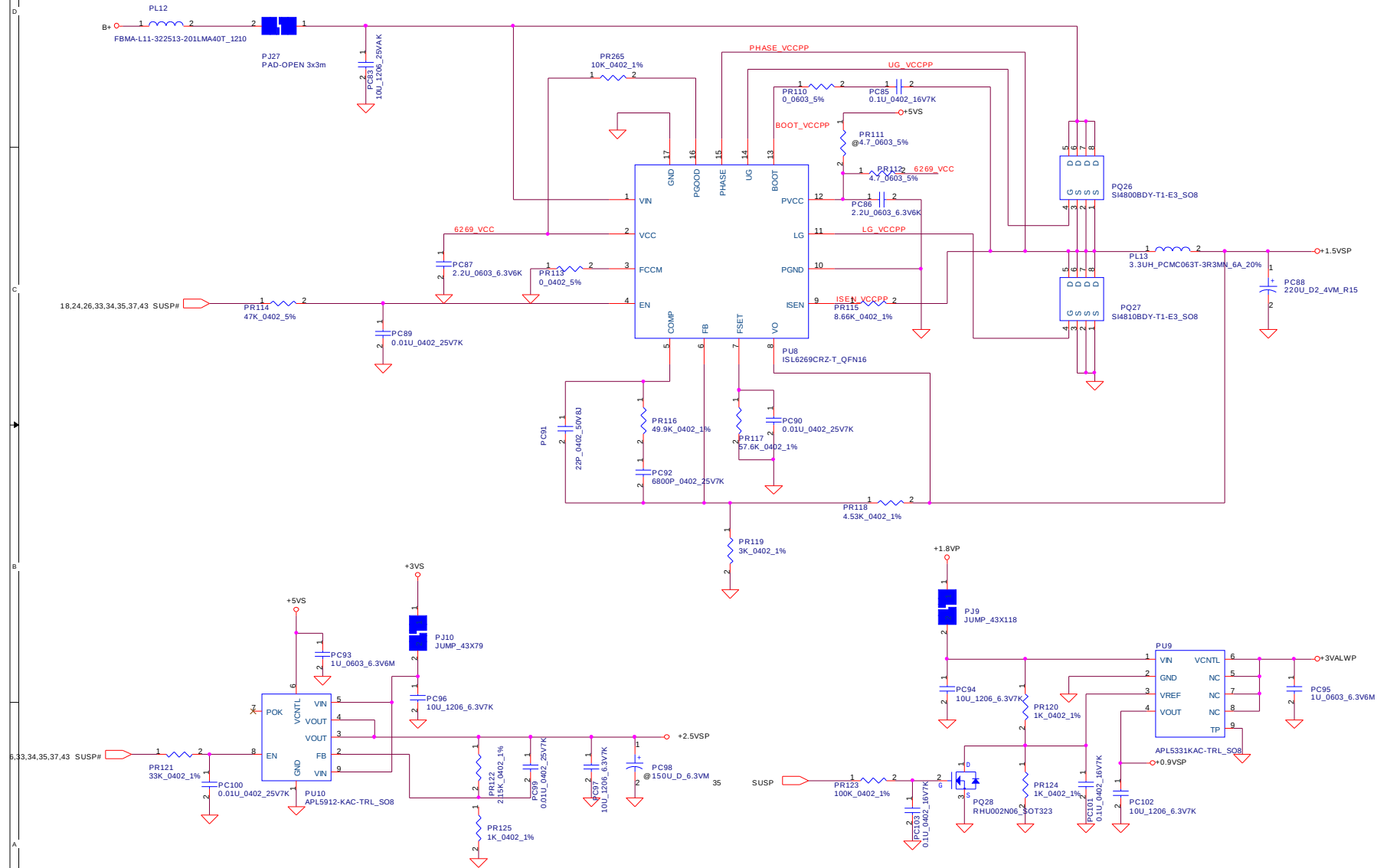


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+1.05VSP Ilimit=6.33A~10.03A



+1.5VSP Ilimit = 9.38A-12.5A



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				Custom	0.1
				Date	Rev
				2005/08/08	0.1
				Sheet	44 of 48

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
8							
9							

Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG #	Modify List	B.Ver #	Phase
1					0.2	DVT
2					0.2	DVT
3					0.2	DVT
4					0.2	DVT
5					0.2	DVT
6					0.2	DVT
7					0.2	DVT
8					0.2	DVT
9					0.2	DVT
10					0.2	DVT
11					0.2	DVT

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Title			
PIR			
Size	Document Number		Rev
	HGT30/31 LA-3061		0.0
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Item	Fixed Issue	Rev.	PG #	Modify List	B.Ver #	Phase
12					0.3	PVT
13					0.3	PVT
14					0.3	PVT
15					0.3	PVT
16					0.3	PVT

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Title		
PIR		
Size	Document Number	Rev
	HGT30/31 LA-3061	0.0
Date:	日期 1, 六月 08, 2006	Sheet 48 of 48