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NEW71/91 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M
NV N11P-GV2H

2009-12-23

REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

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Title: Cover Page

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

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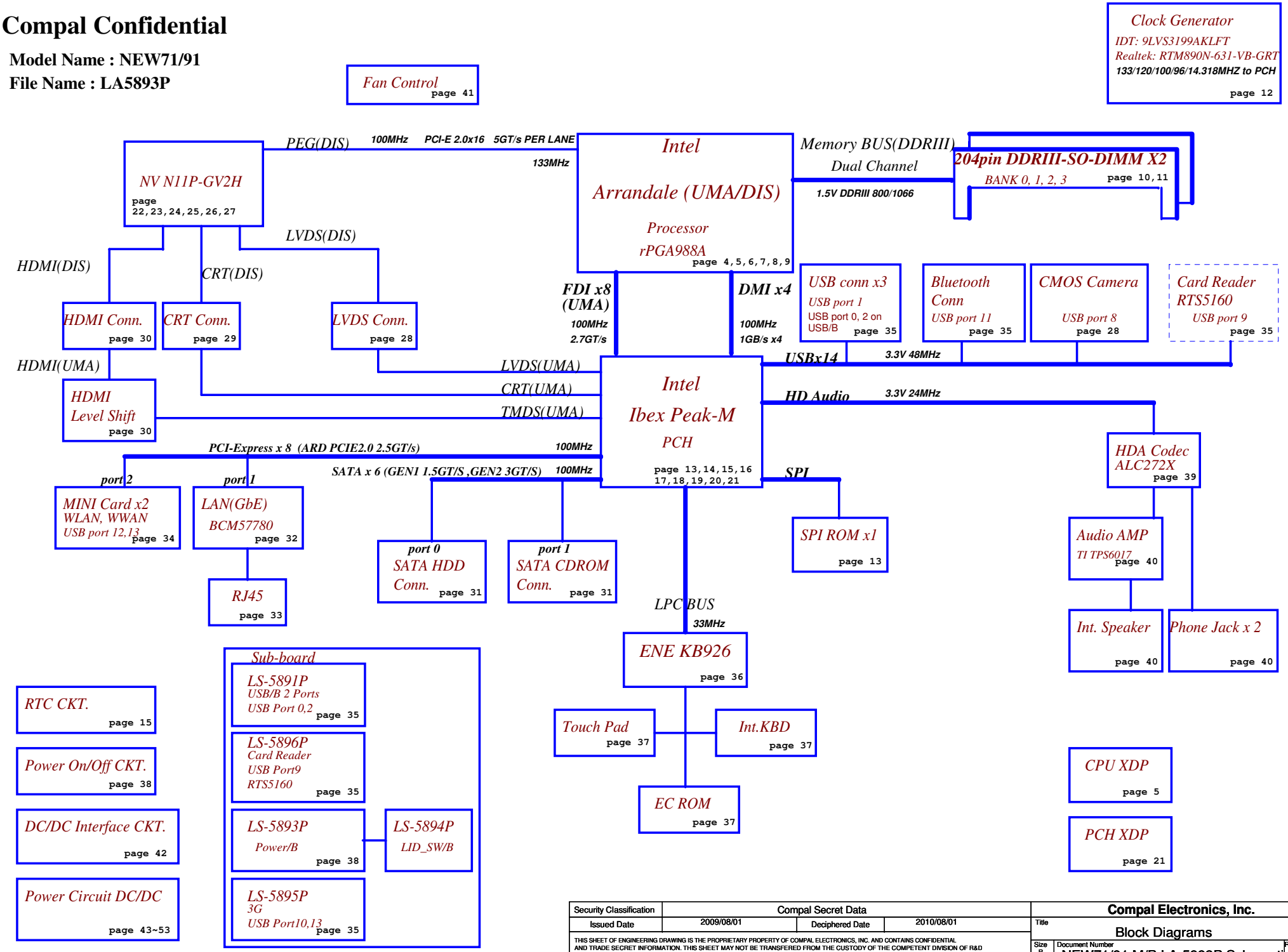
Model Name : NEW71/91
File Name : LA5893P



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Config	
NEW71 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,XDP@
NEW91 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,91@,X7621@,XDP@

VRAM BOM Config

X7621@: X76198BOL21 ALT. GROUP PARTS 1G SAM

X7622@ X76198BOL22 ALT. GROUP PARTS 1G HYN

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
XDP	XDP@
NonSG	NonSG@
NEW71	71@
NEW91	91@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

VRAM P/N :
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

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Title: Notes List

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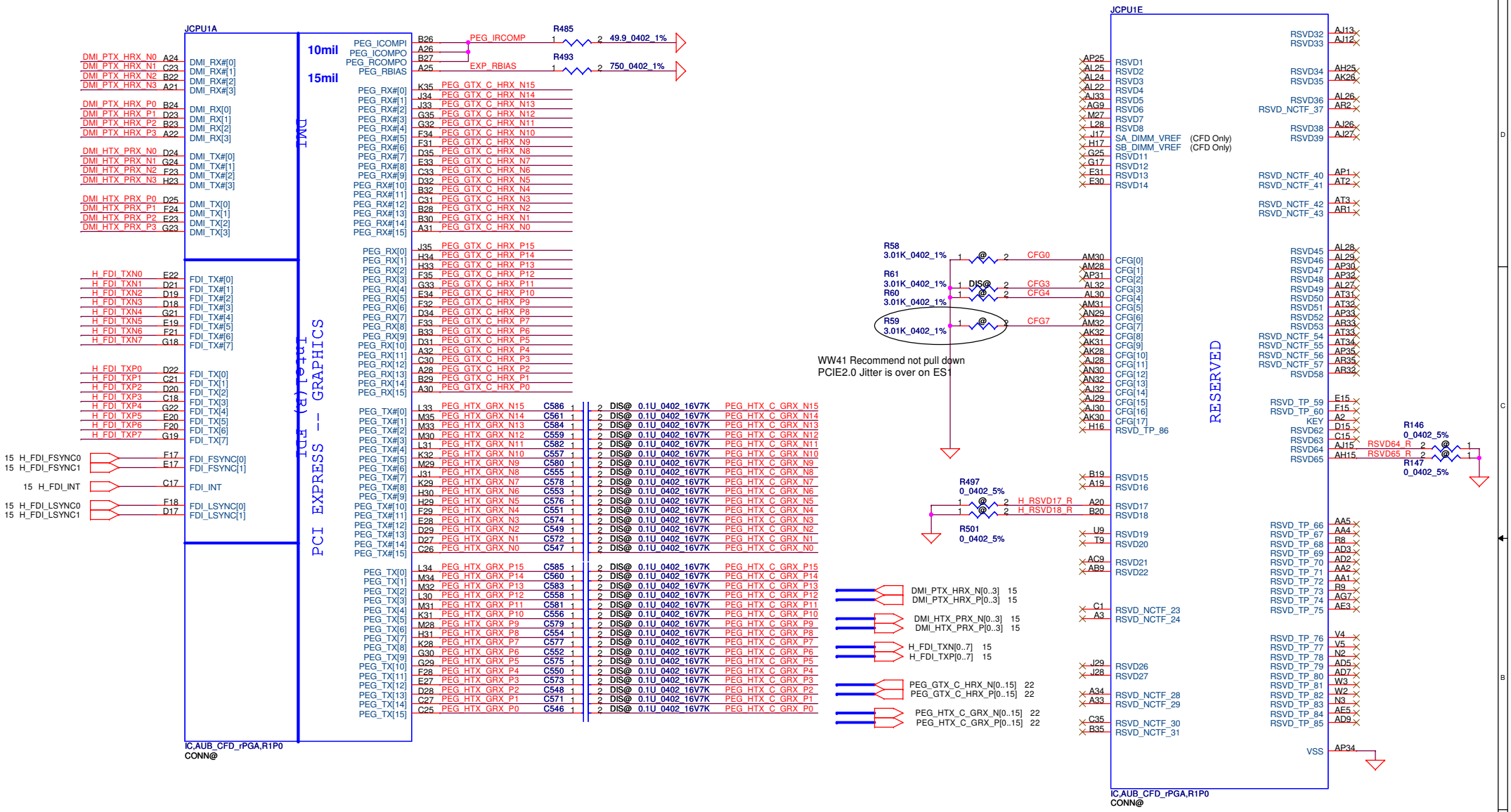

eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Title: PROCESSOR (1/6) DMI,FDI,PEG

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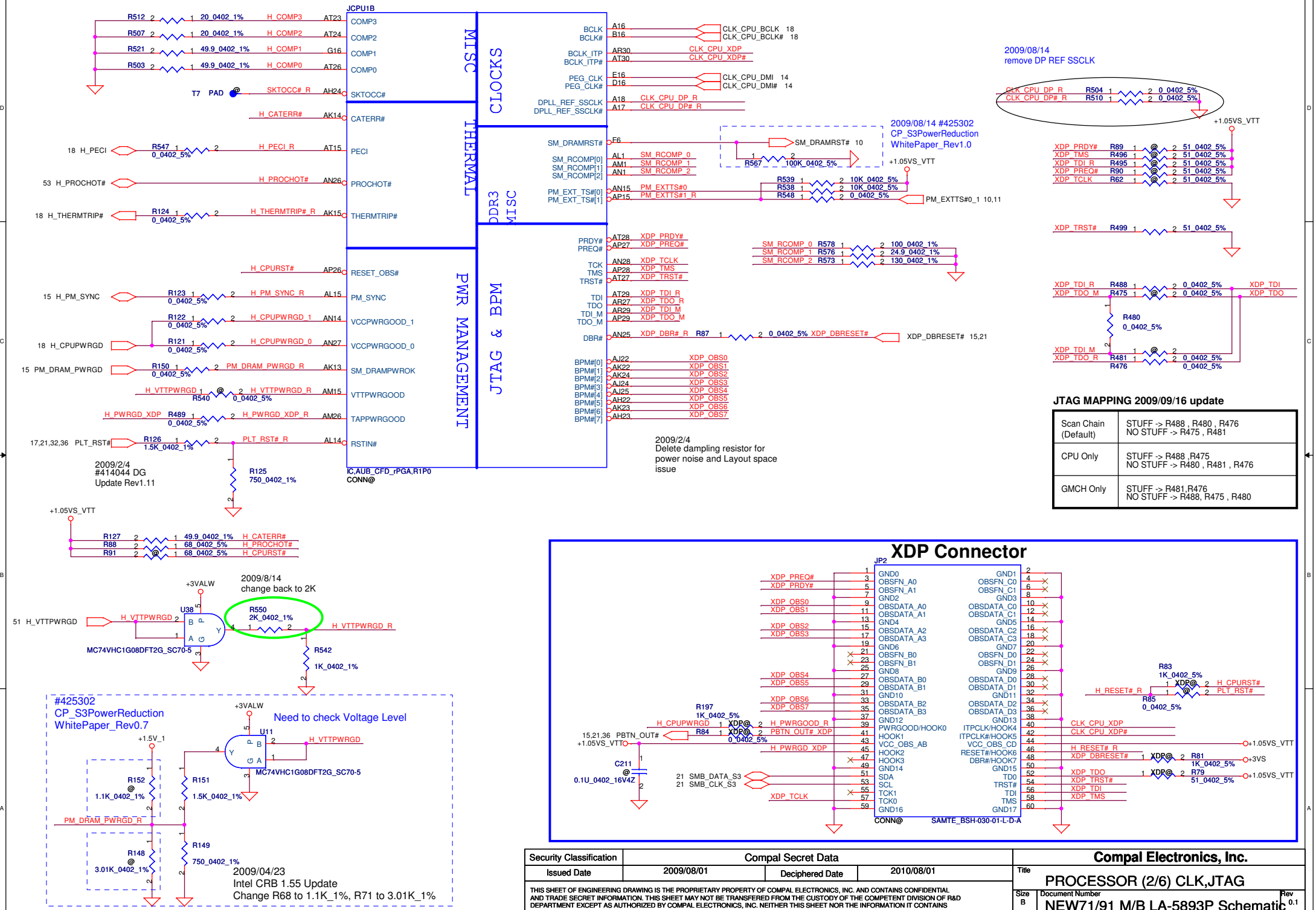

JTAG MAPPING 2009/09/16 update

Scan Chain (Default)	STUFF -> R488 , R480 , R476 NO STUFF -> R475 , R481
CPU Only	STUFF -> R488 ,R475 NO STUFF -> R480 , R481 , R476
GMCH Only	STUFF -> R481,R476 NO STUFF -> R488, R475 , R480

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Title: PROCESSOR (2/6) CLK,JTAG

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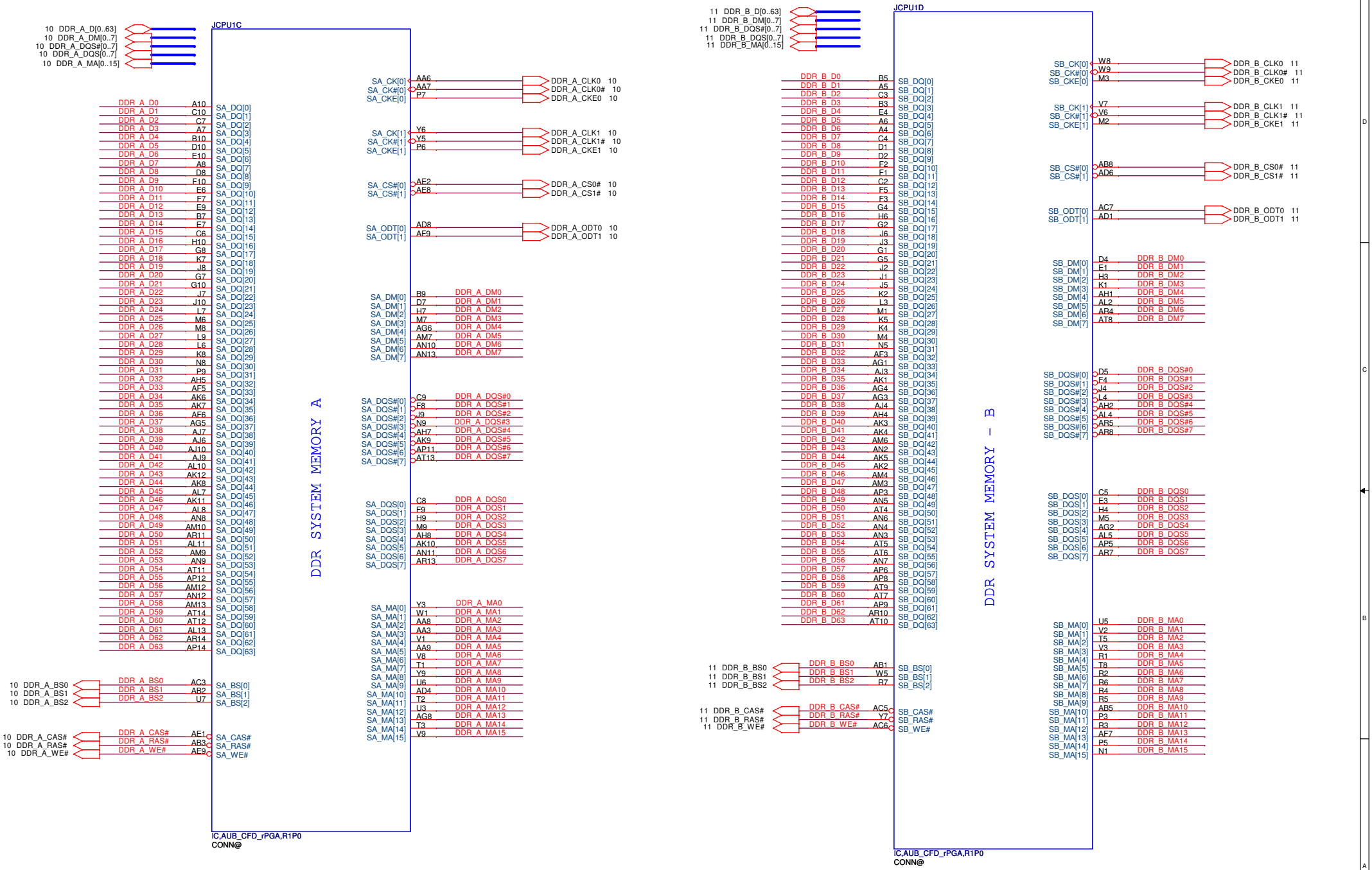

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Title: PROCESSOR (3/6) DDRIII

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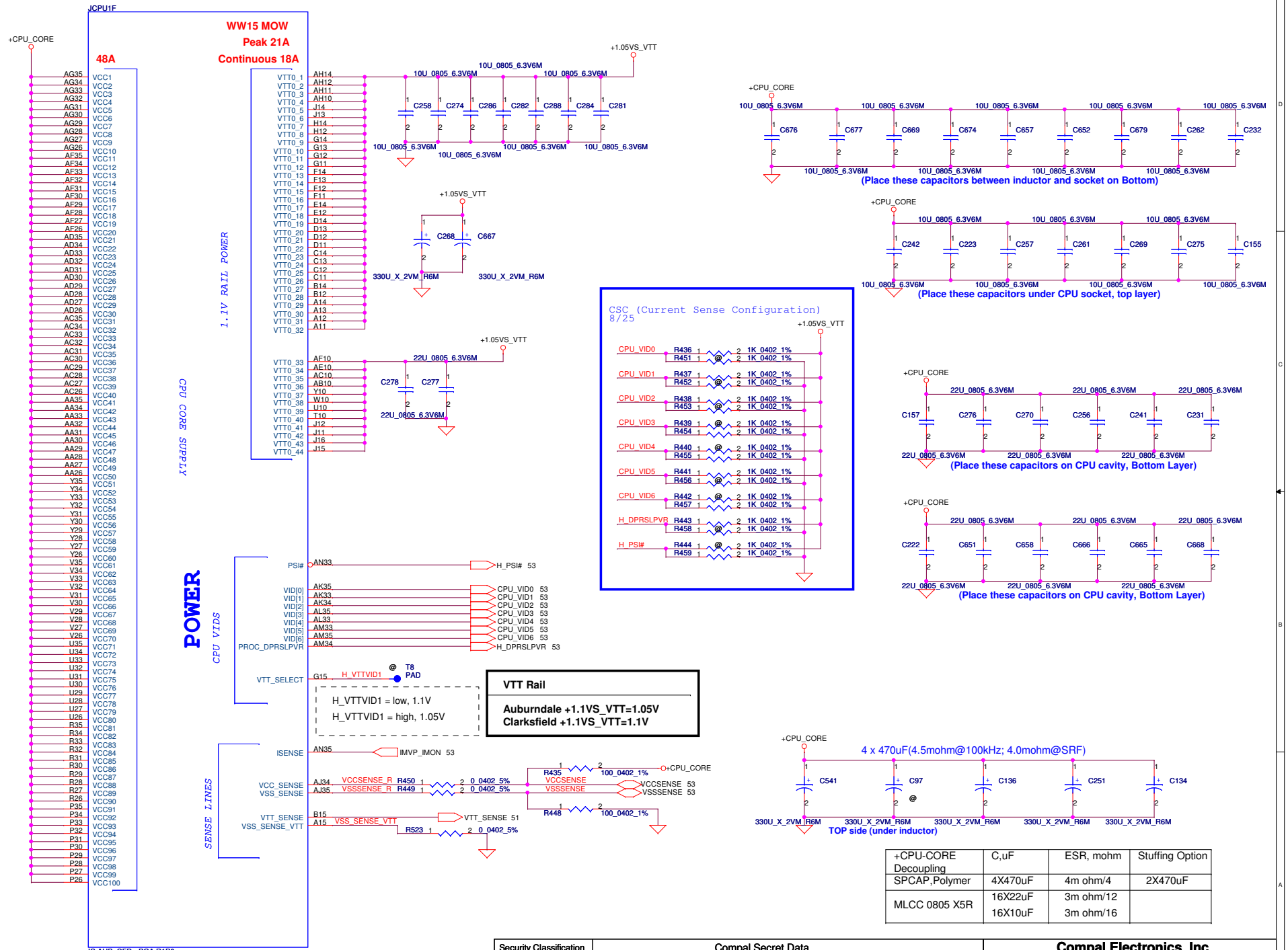

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

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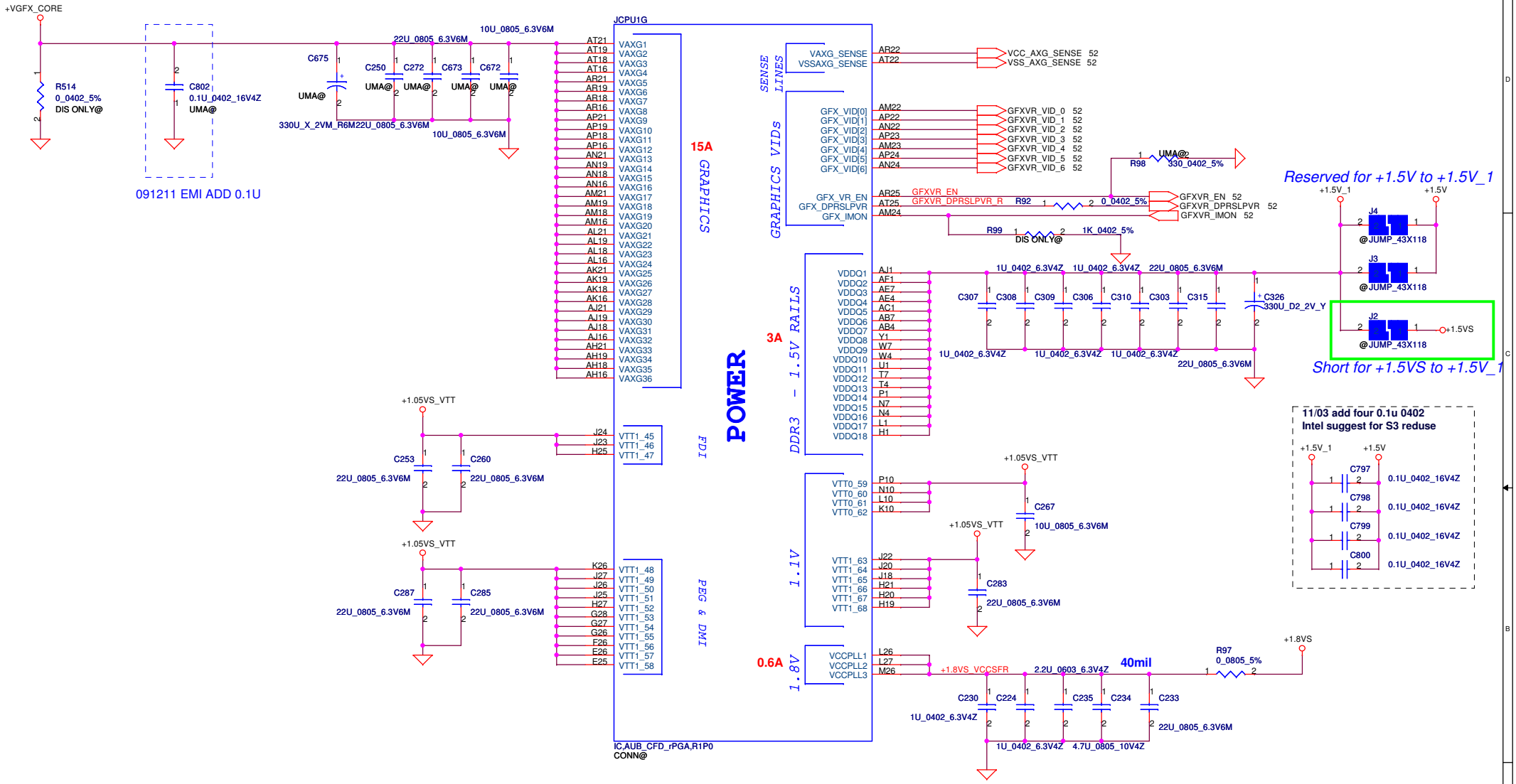

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Title: PROCESSOR (5/6) PWR

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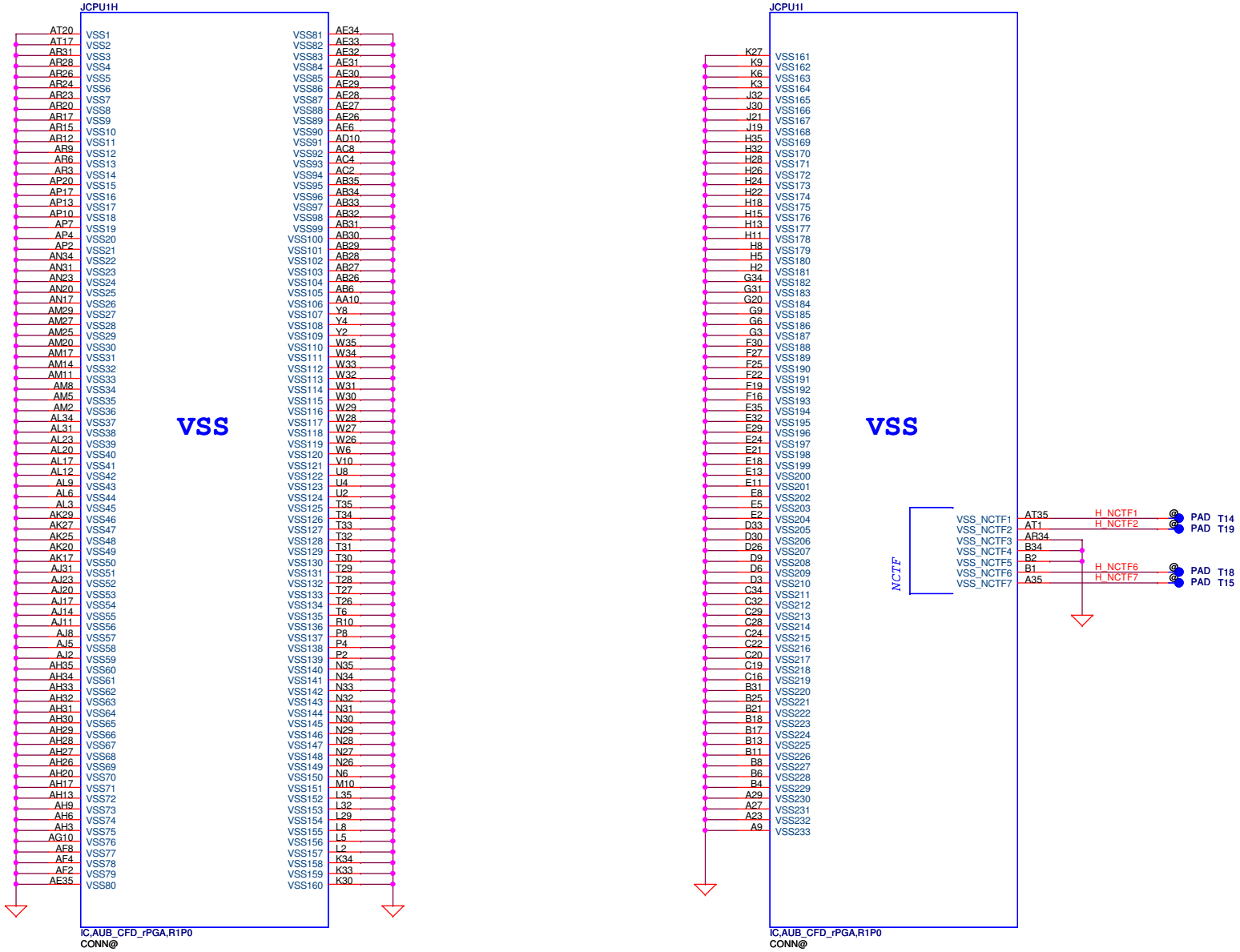

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Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

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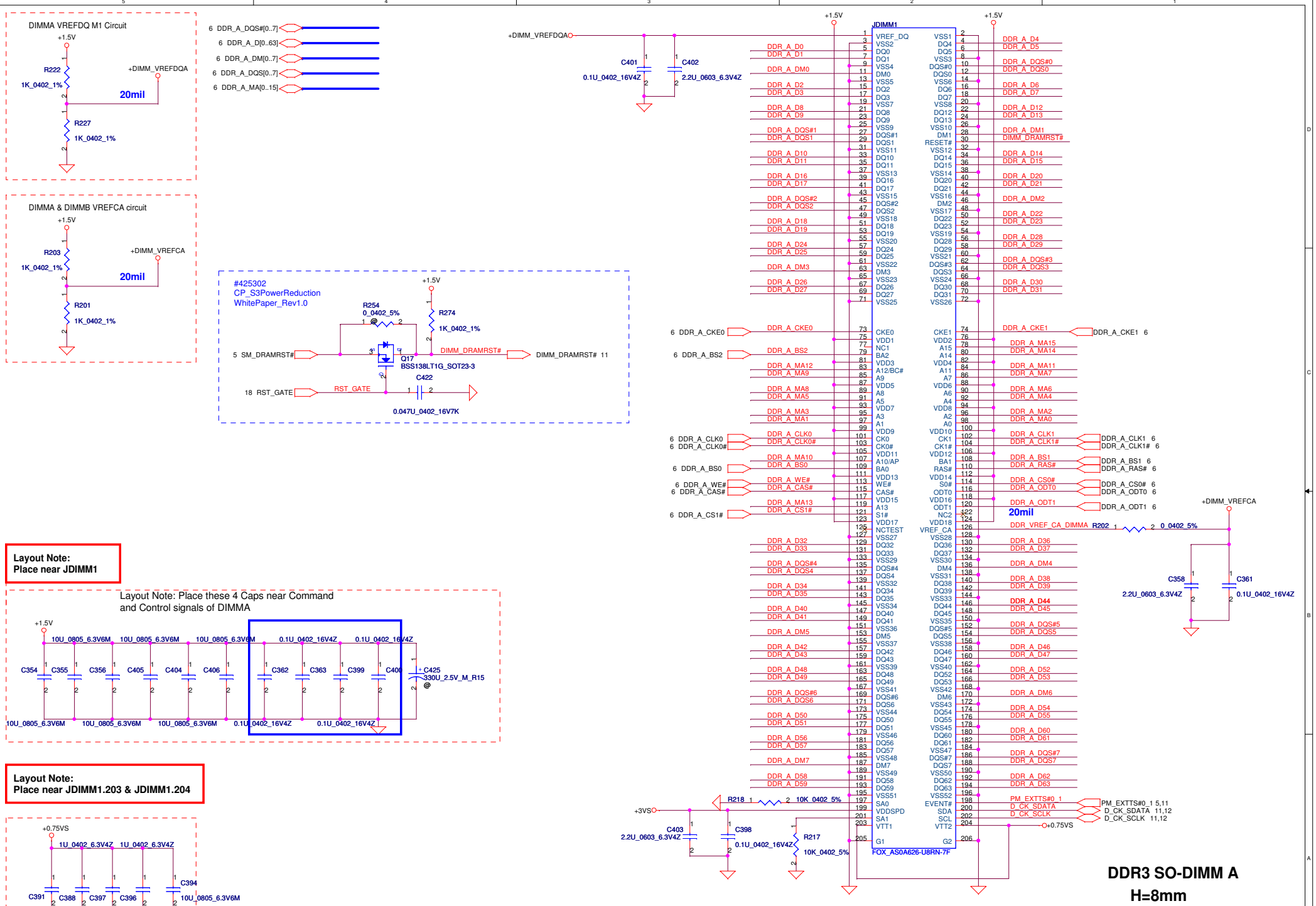

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Title: DDRIII-SODIMM SLOT1

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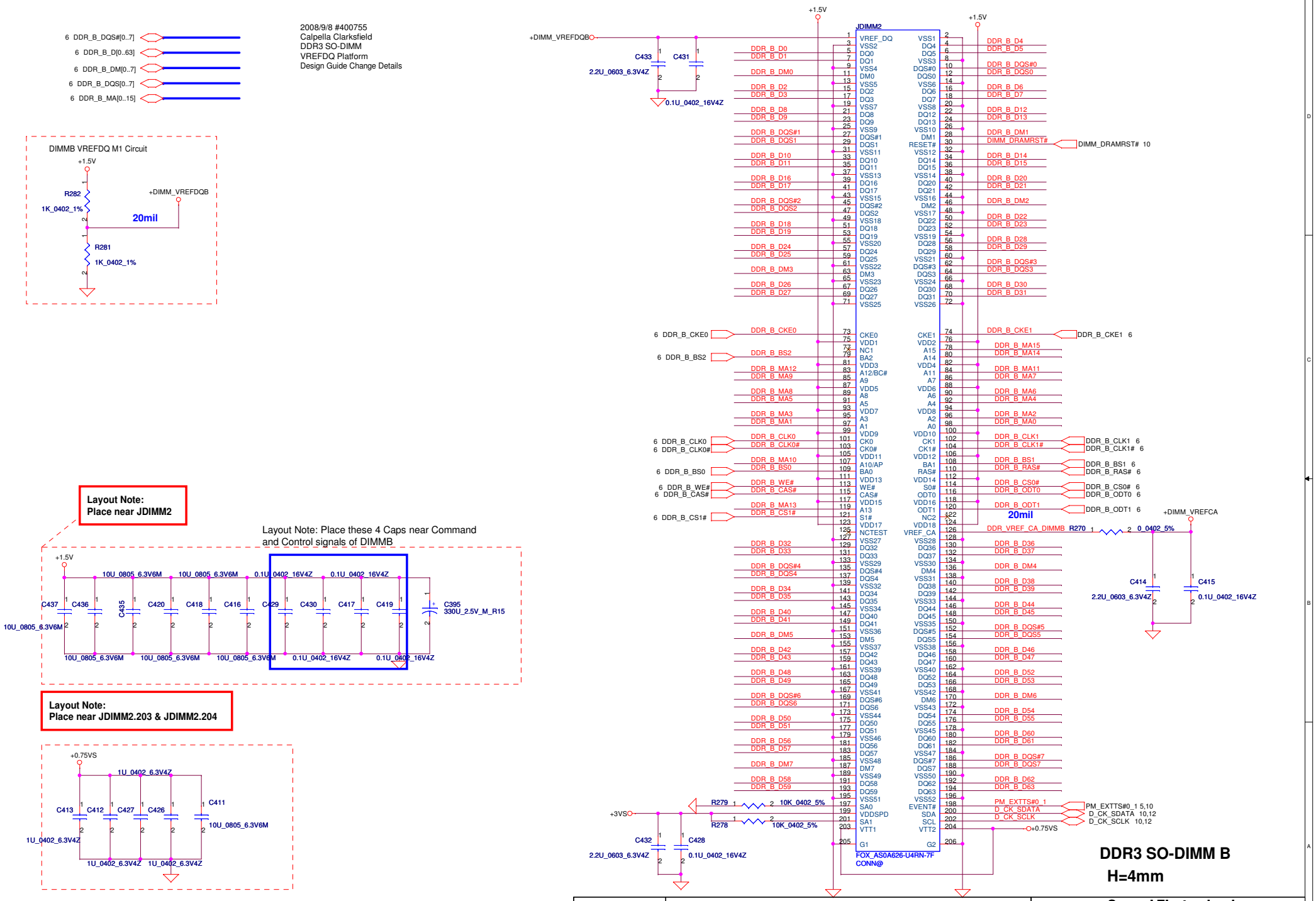

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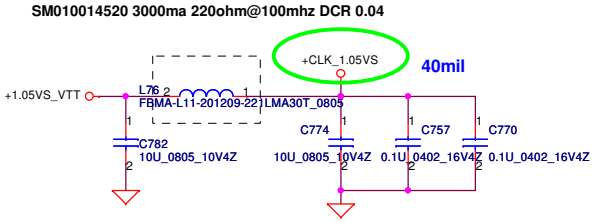
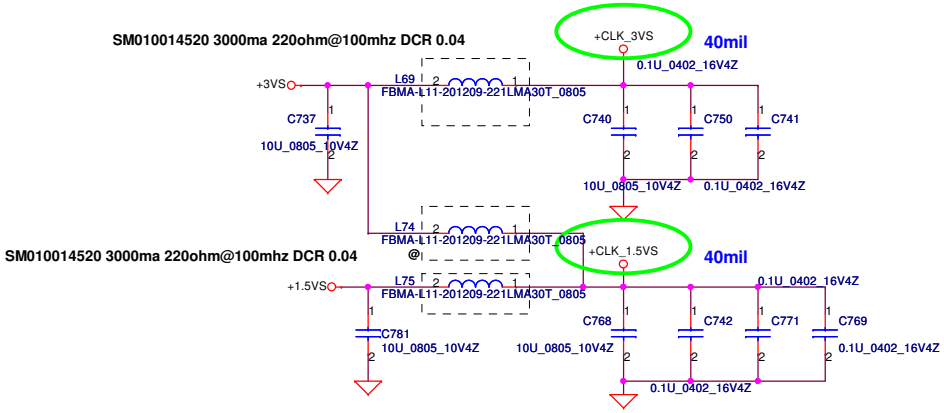
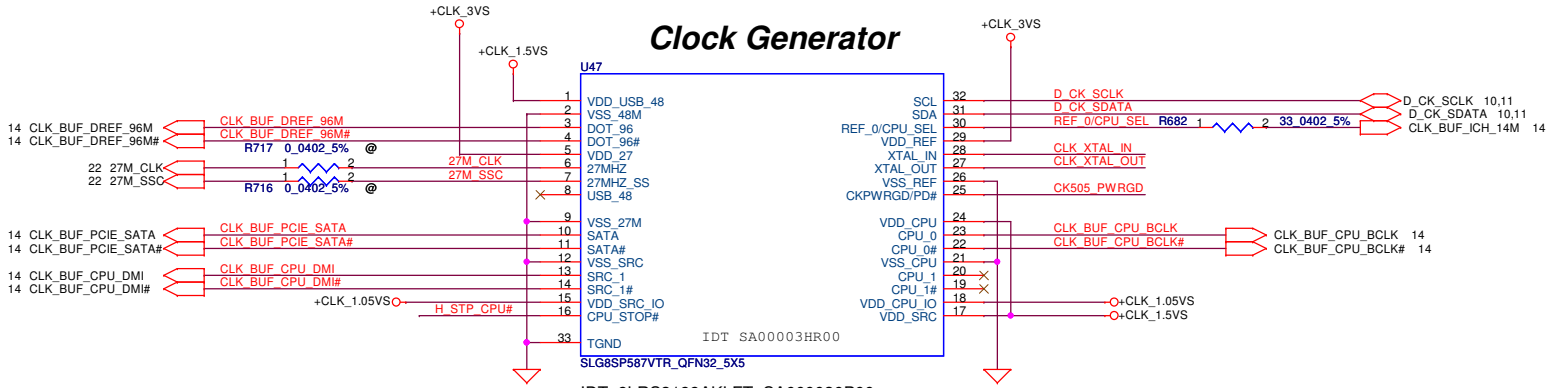




Clock Generator



IDT: 9LRS3199AKLFT, SA000030P00

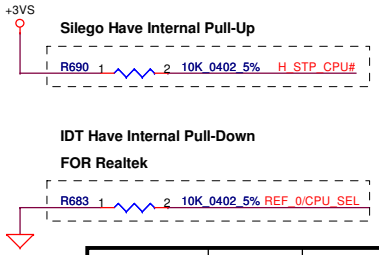
SILEGO: SLG8SP587V(WF), SA00002XY10

Low Power:

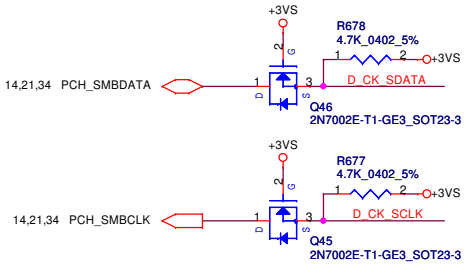
IDT: 9LVS3199AKLFT, SA00003HR00

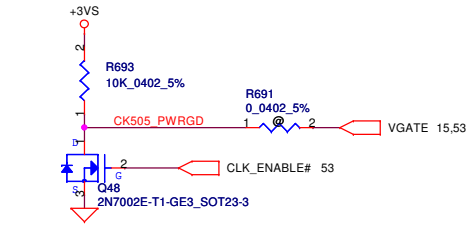
Realtek: RTM890N-631-VB-GRT, SA00003HQ10

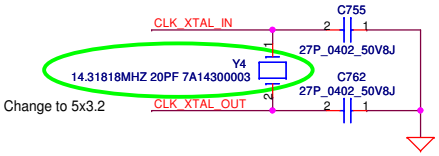
IDT 9LVS3199AKLFT NC



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz







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Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

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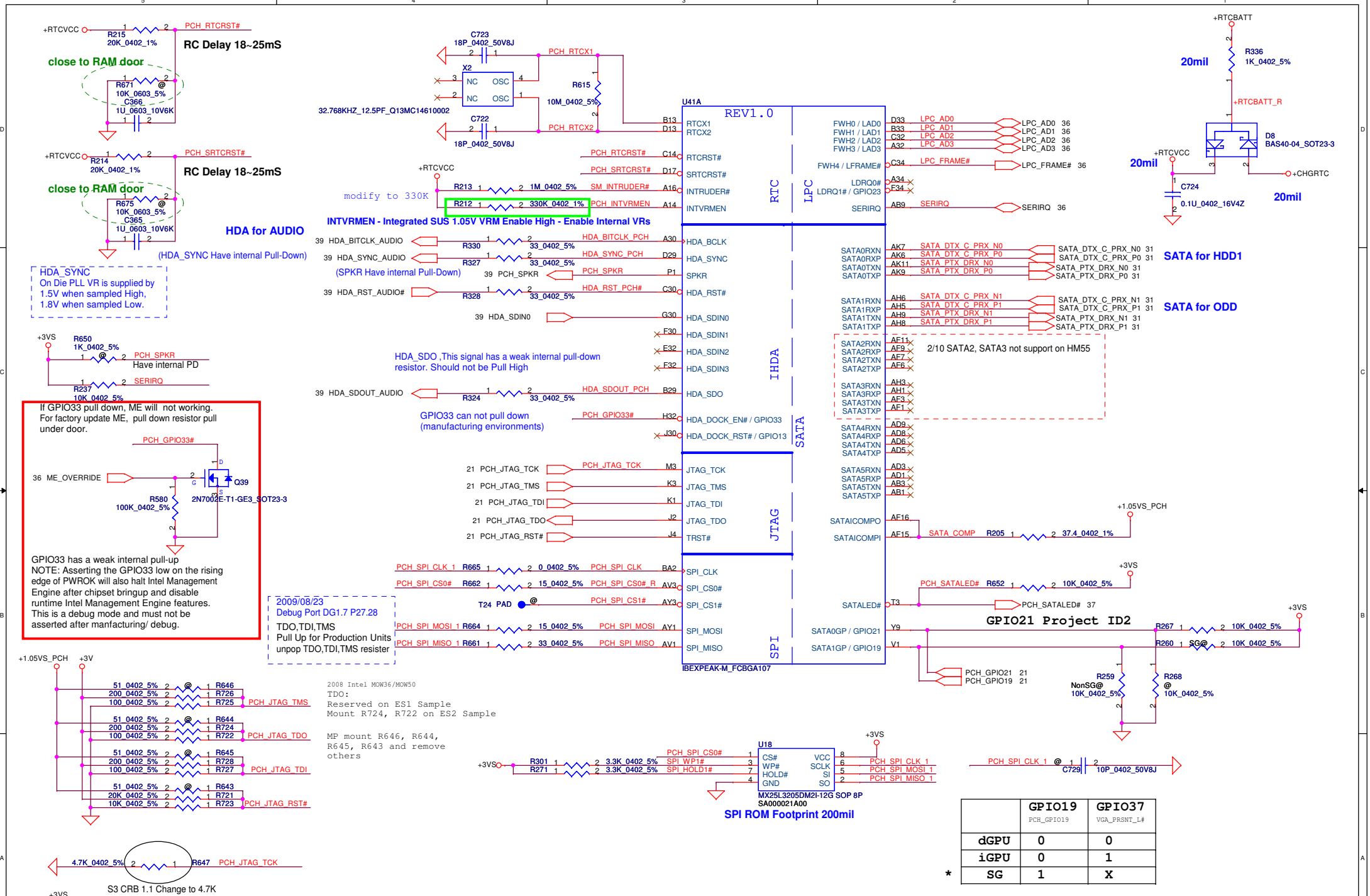

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
* SG	1	X

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Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

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Date: Tuesday, December 22, 2009 | Sheet 13 of 56

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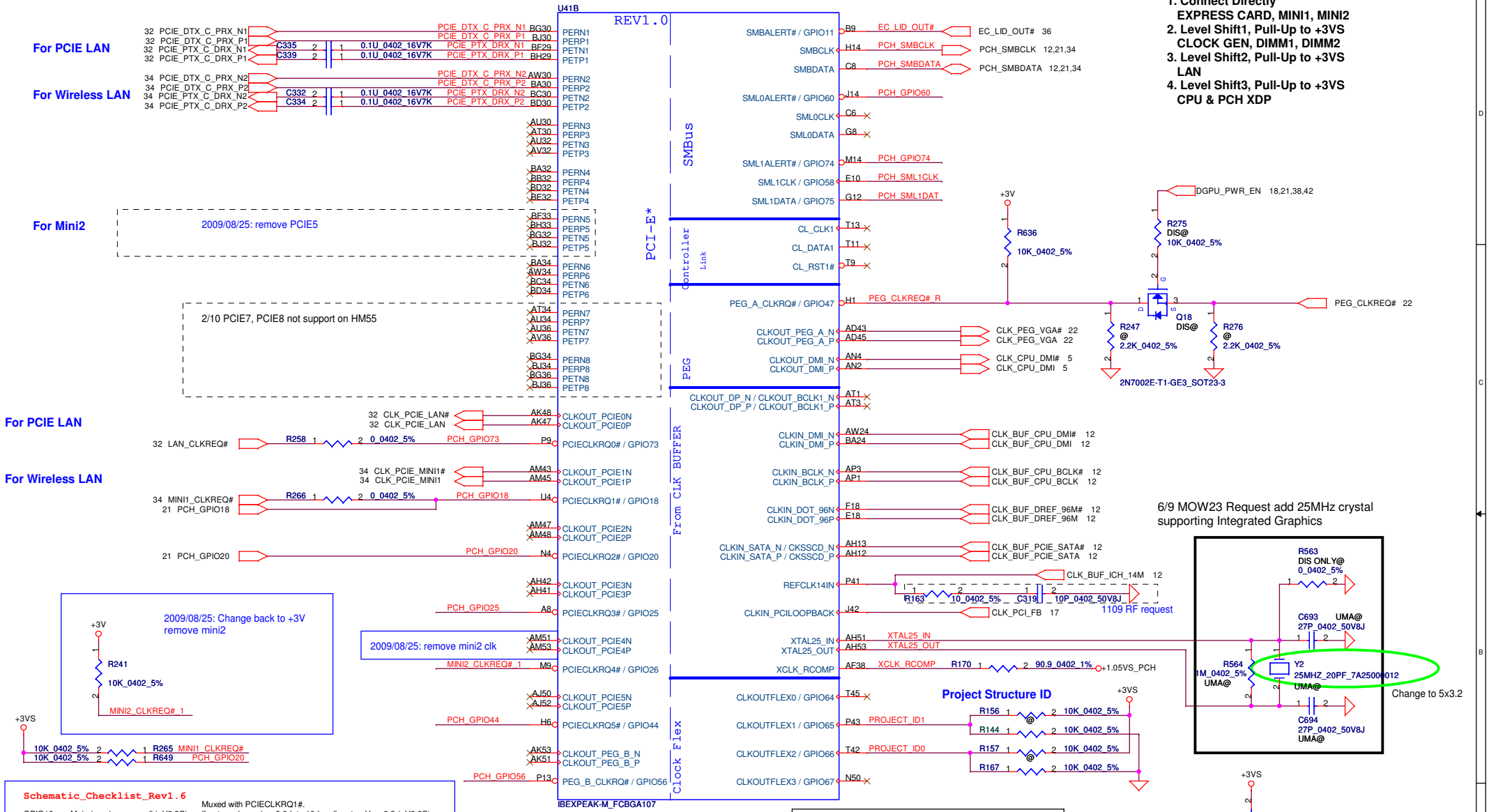

Schematic_Checklist_Rev1.6

GPIO18	Main (core) power well (+V3.3S)	Muxed with PCIECLKRQ1#. If not used, requires 8.2-k to 10-k pull-up to +Vcc_3.3 (+V3.3S)
GPIO25	Resume (Sus) well (+V3.3A)	Muxed with PCIECLKREQ3# If not used, requires 8.2-k to 10-k pull-up to +V3.3A rail.

Project Structure

GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
0	0	0	NEW70
0	0	1	NEW80
0	1	0	NEW90
* 1	0	0	NEW71/91

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Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

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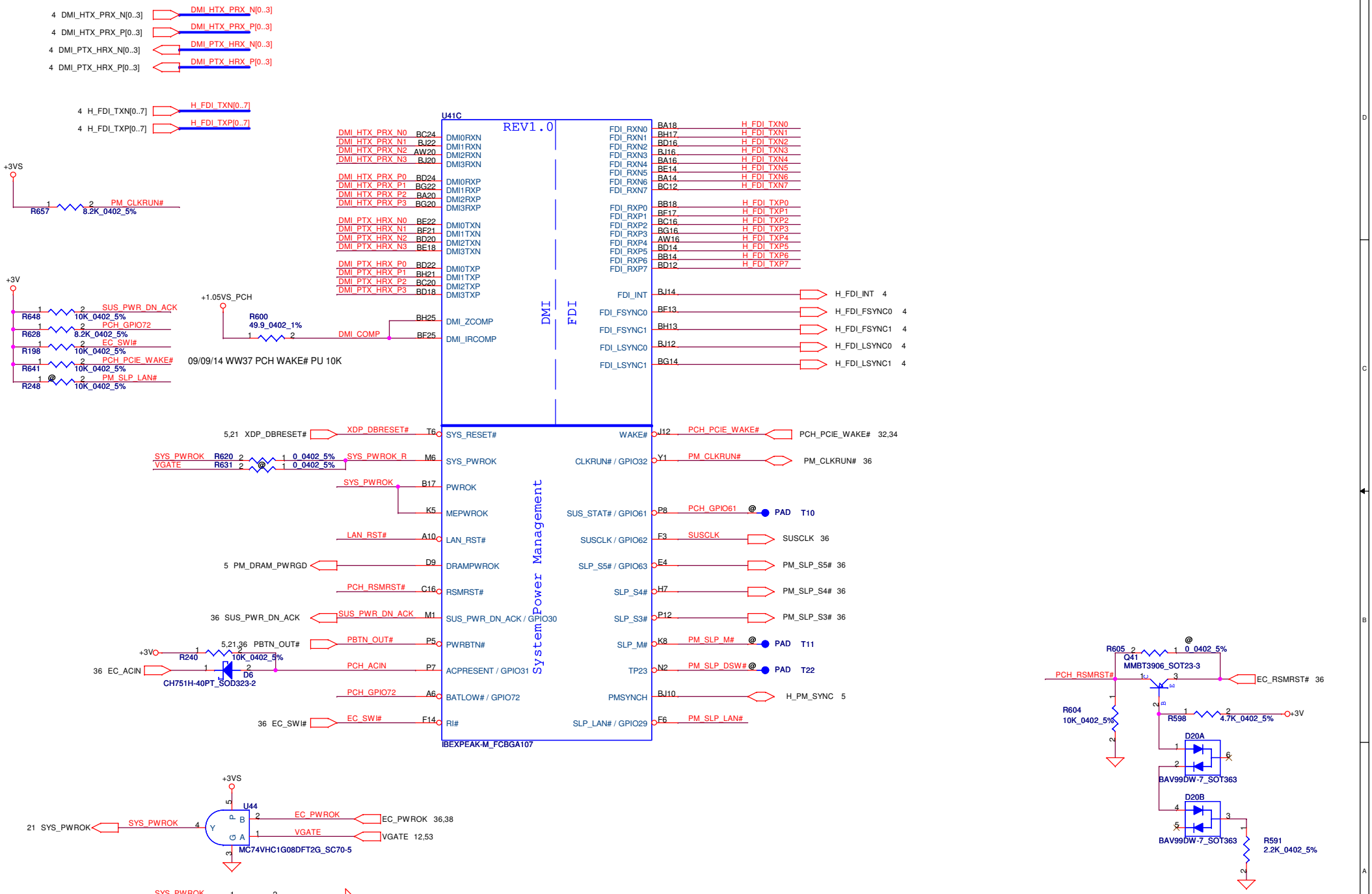
Date: Tuesday, December 22, 2009 | Sheet 14 of 56



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Issued Date	2009/08/01	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

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Date: Tuesday, December 22, 2009 | Sheet 15 of 56

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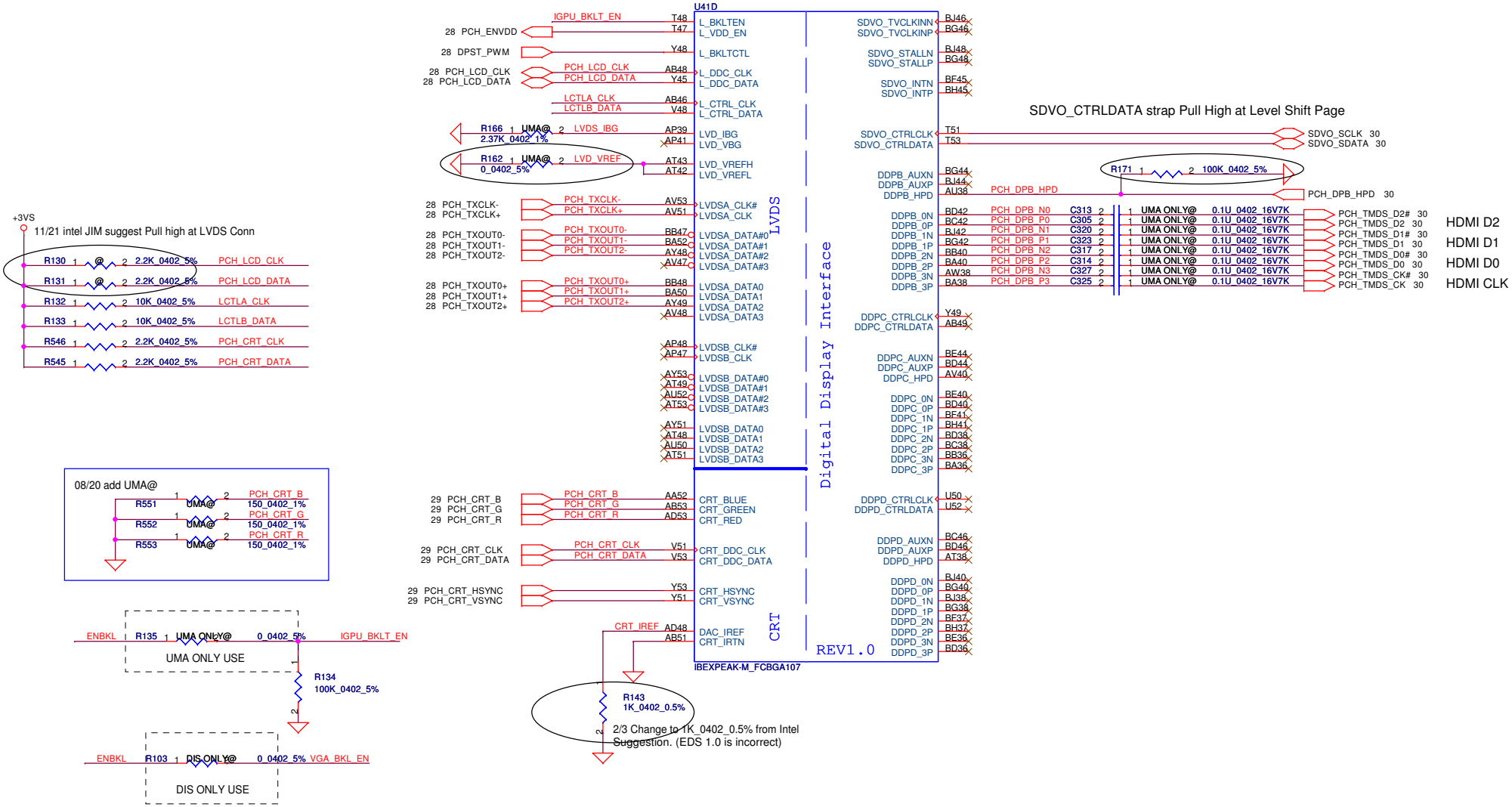

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Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

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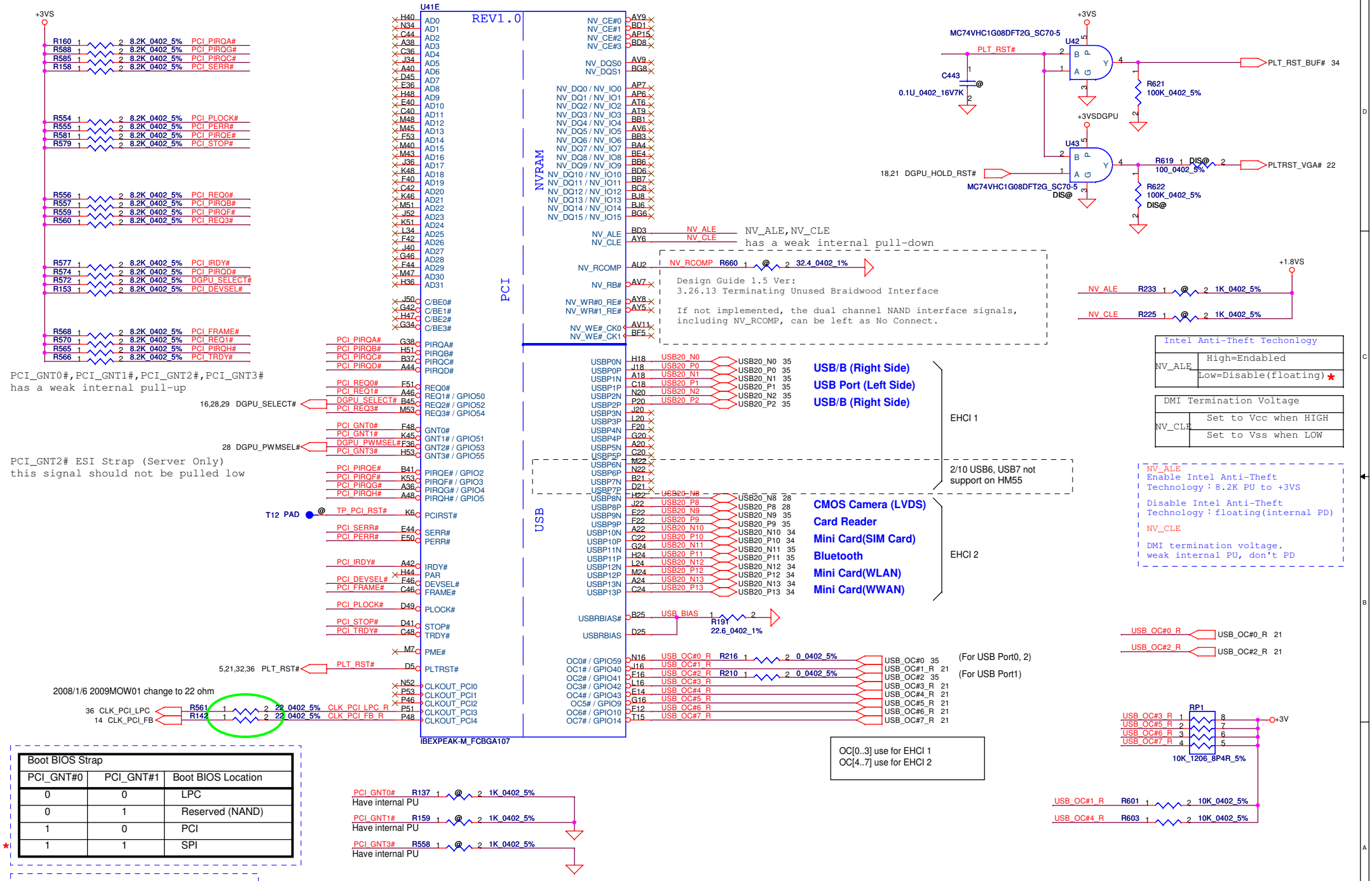
Date: Tuesday, December 22, 2009 | Sheet 16 of 56



Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default ★

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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

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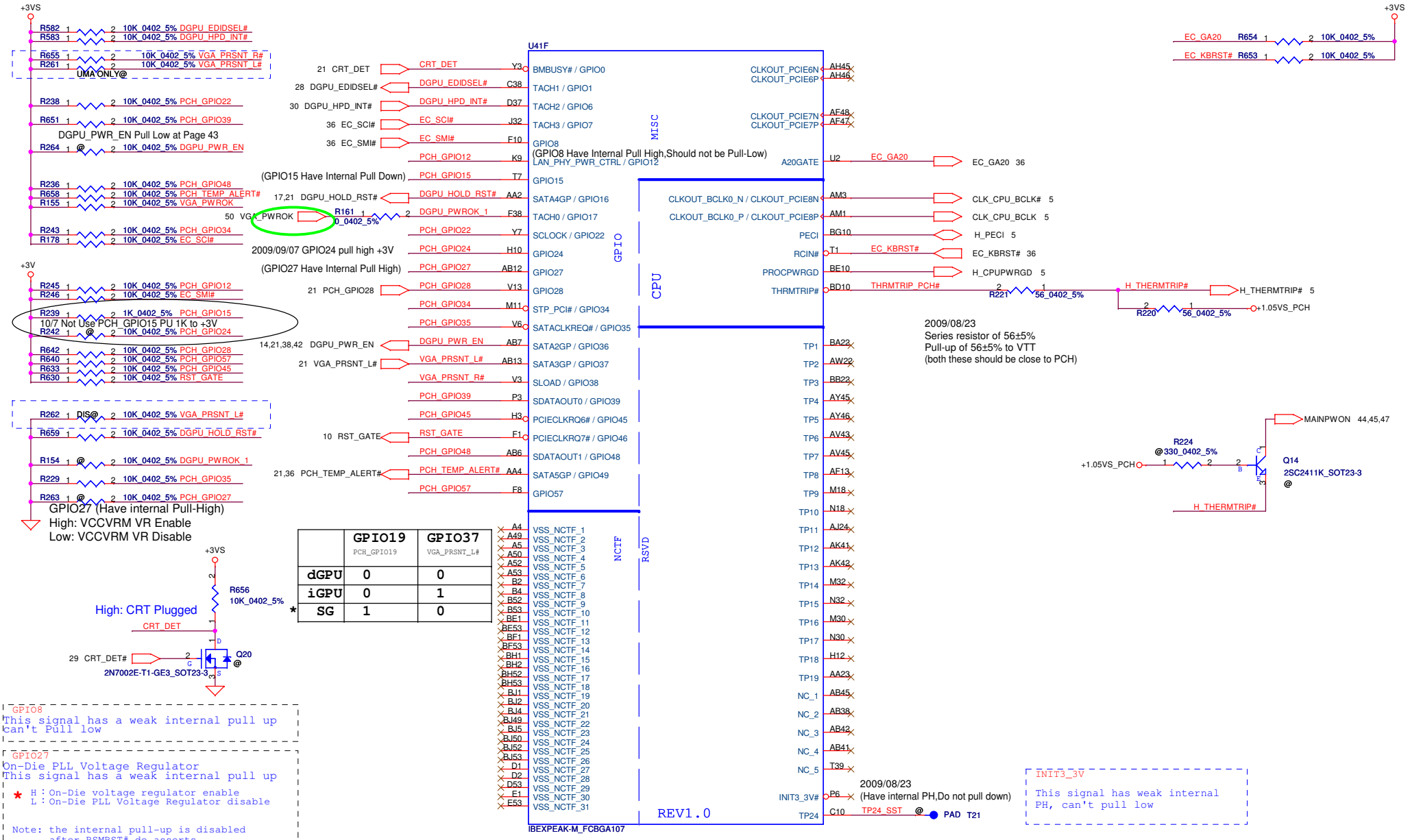

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	0

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Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

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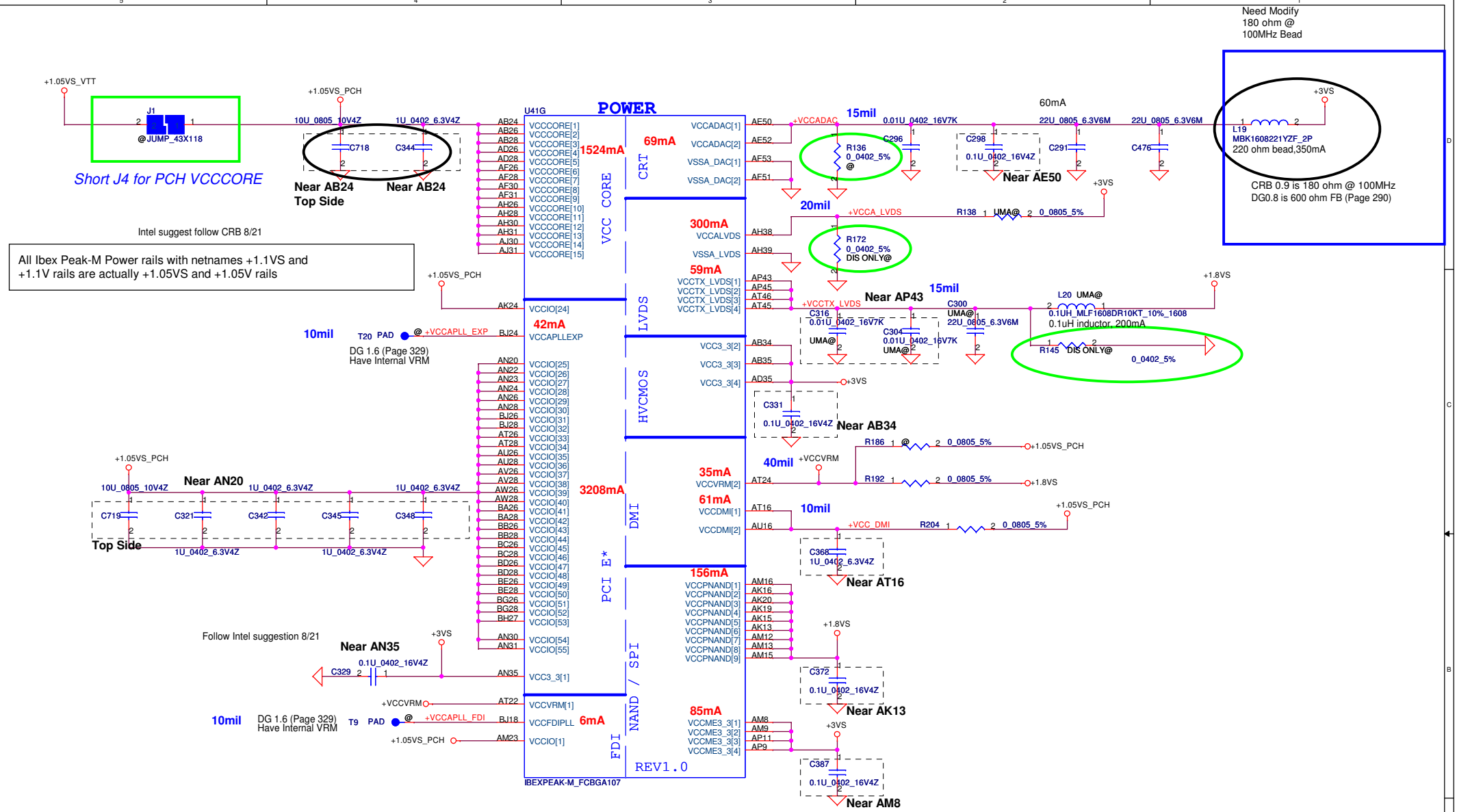
Date: Tuesday, December 22, 2009 | Sheet 18 of 56



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Compal Electronics, Inc.

Title: PCH (7/9) PWR

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Date: Friday, December 18, 2009 | Sheet 19 of 56

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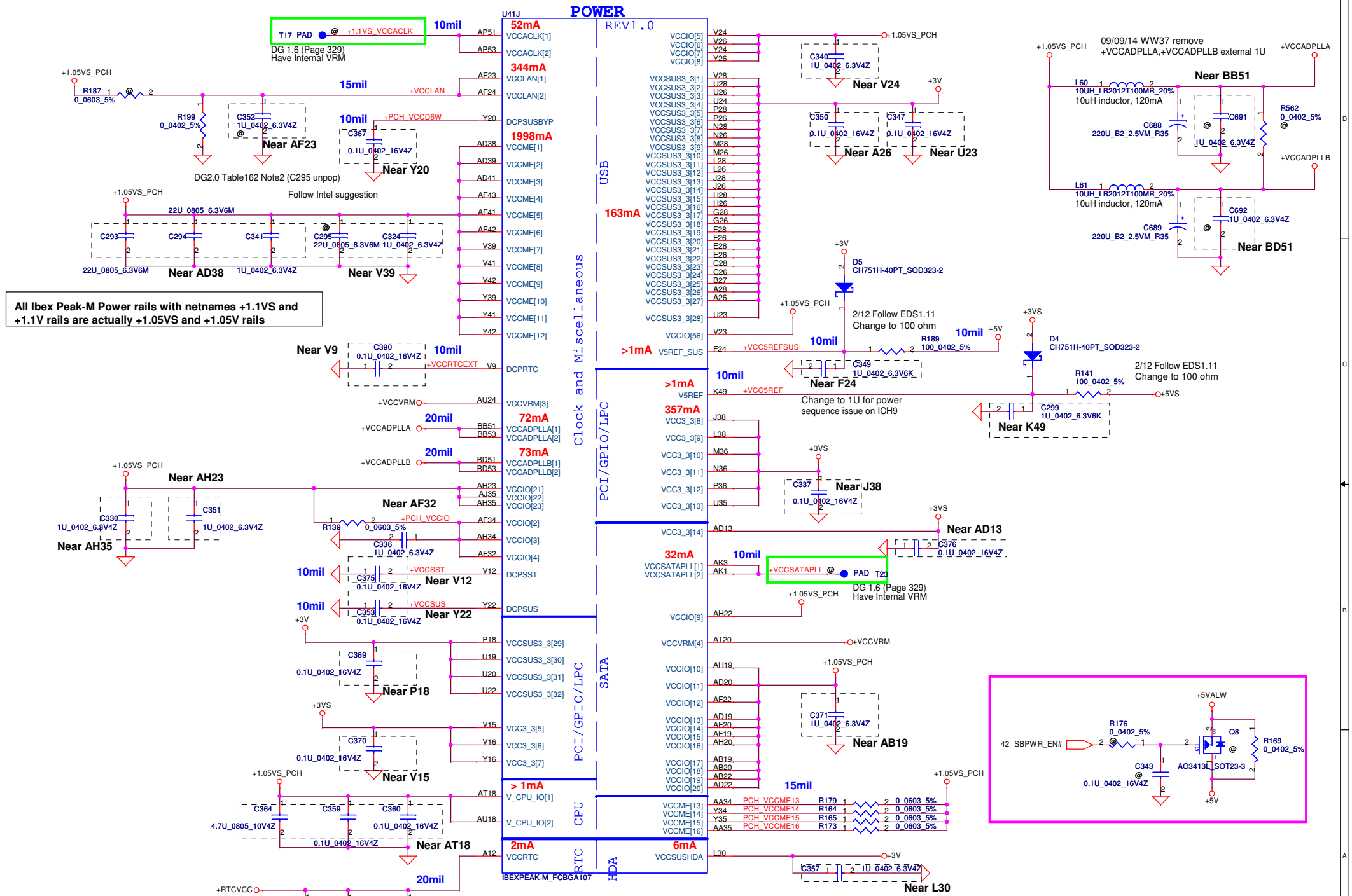

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Compal Electronics, Inc.

Title: PCH (8/9) PWR

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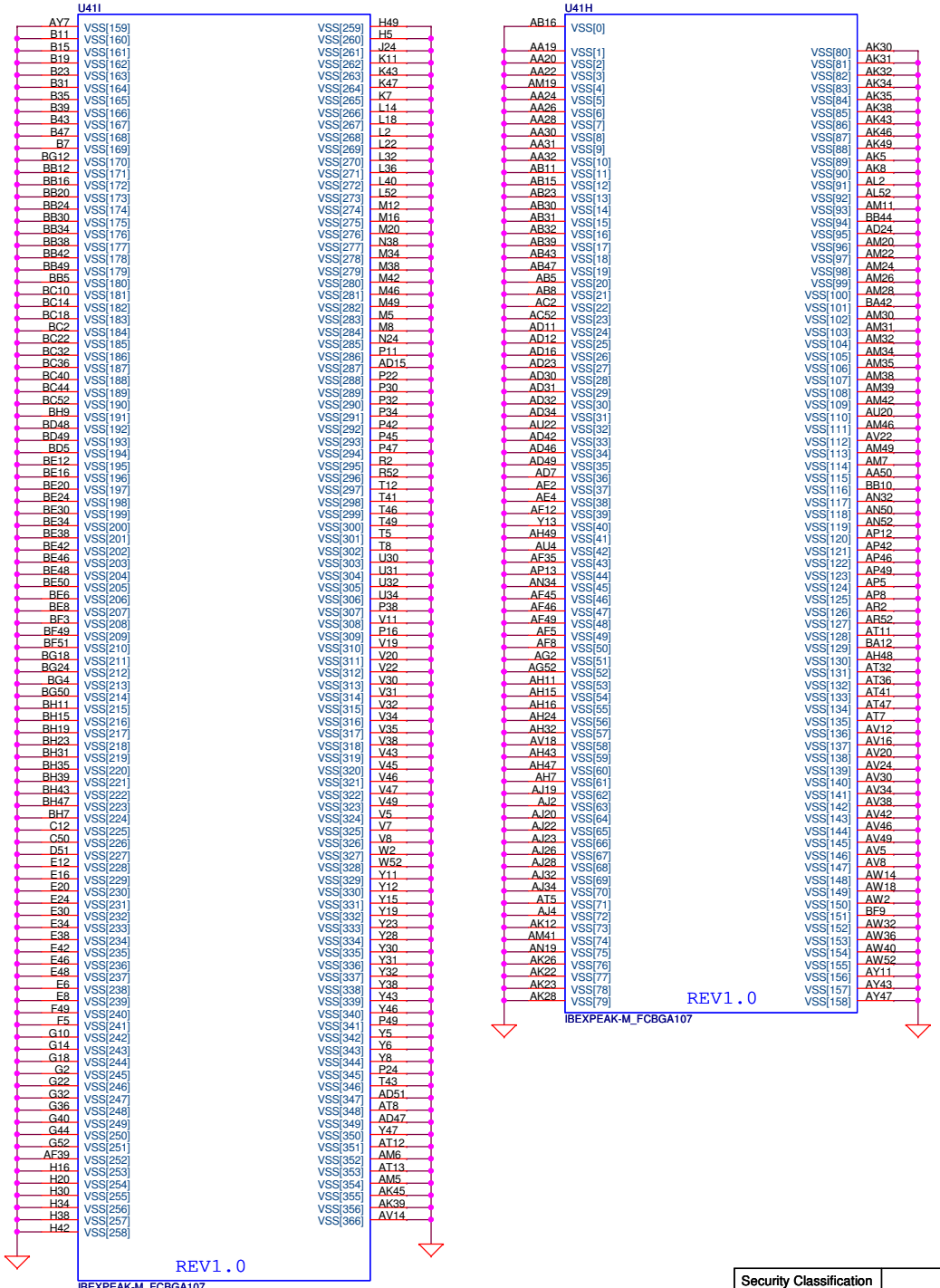
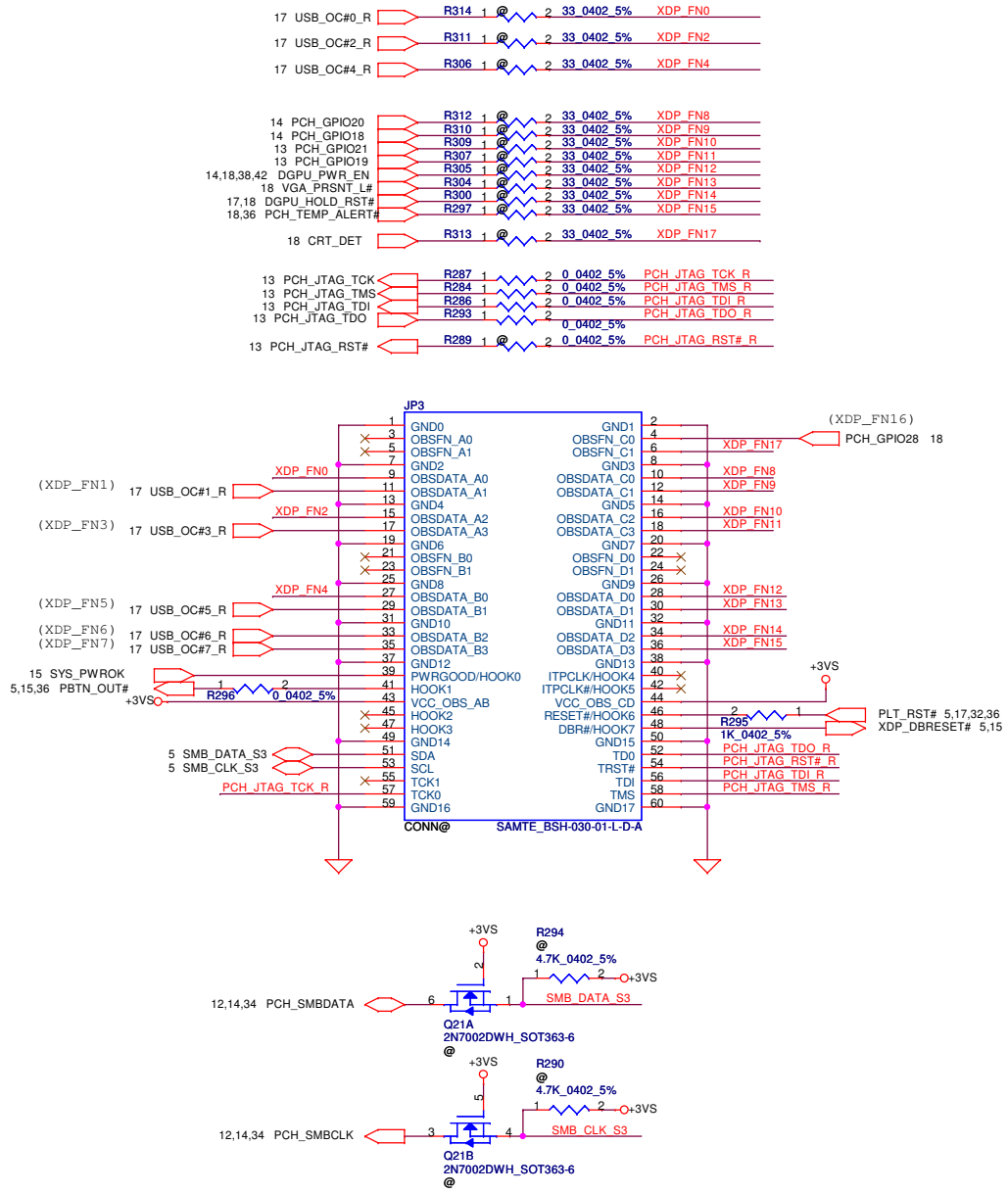
Date: Tuesday, December 22, 2009 | Sheet 20 of 56

PCH XDP Port





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Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

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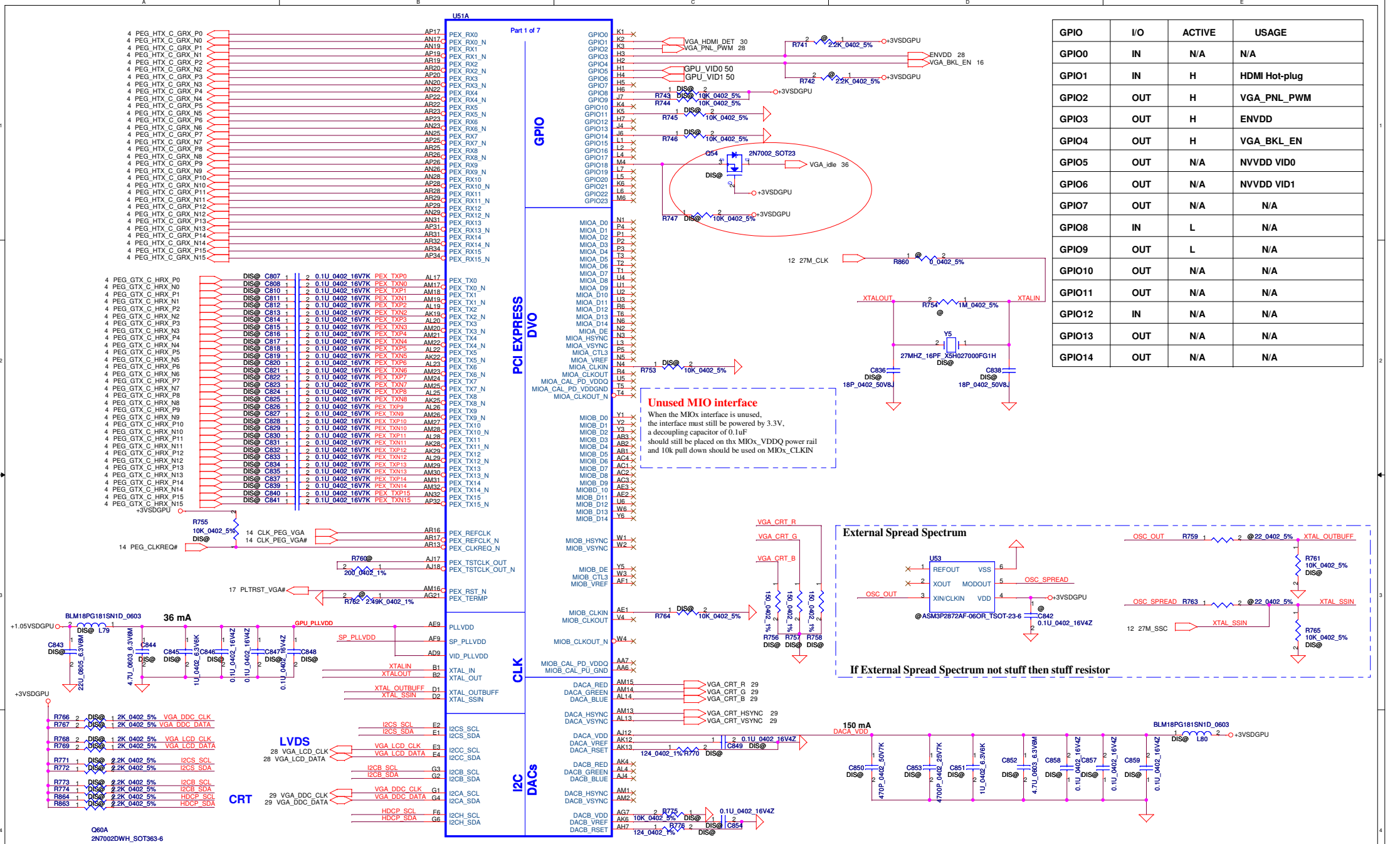

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

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Compal Electronics, Inc.

Title: N11P-GV2H PEG I2C

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

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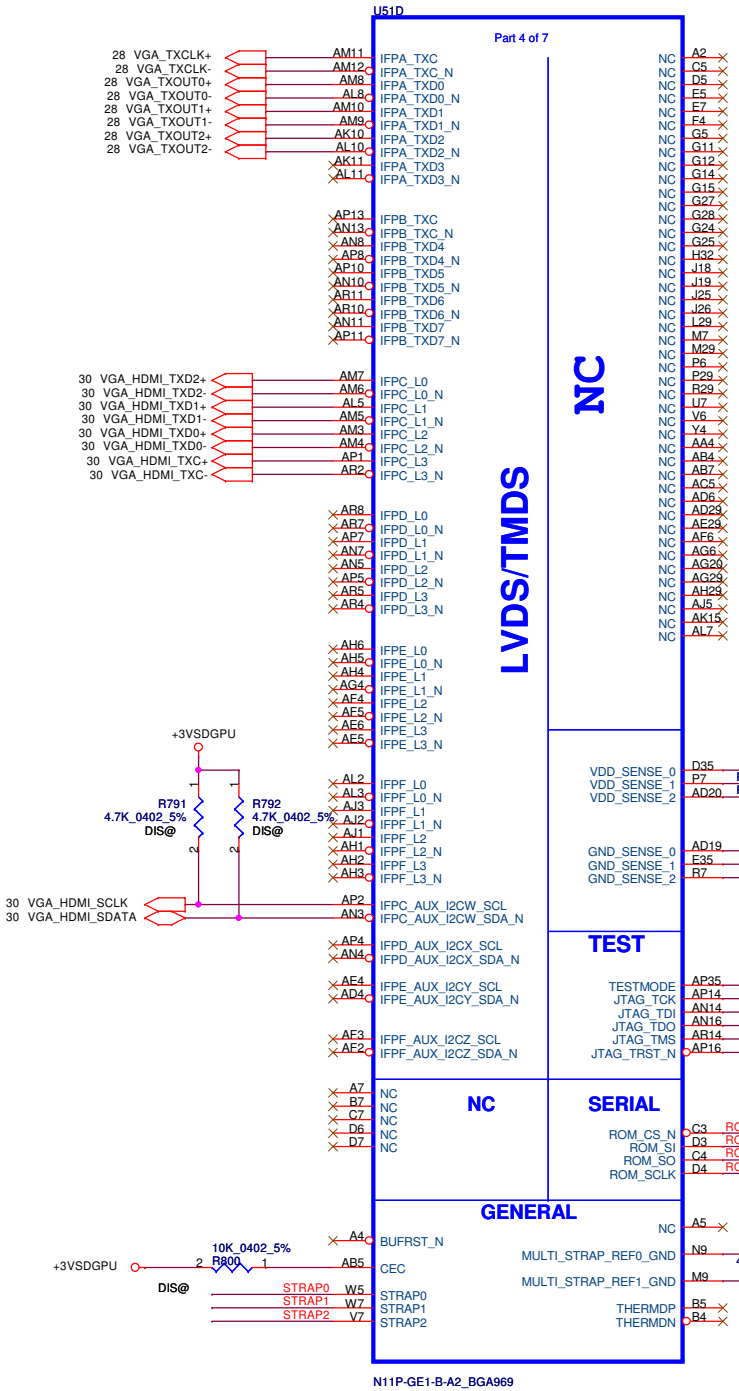
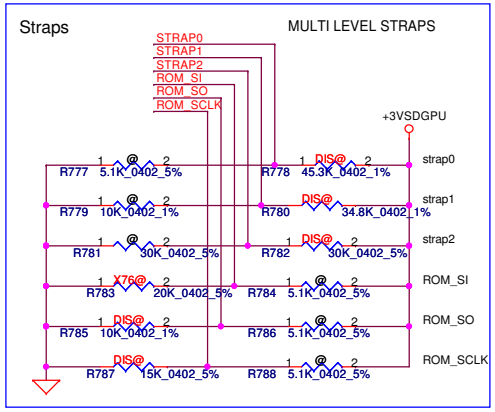
Mode E Command Mapping GB2-128 Package Femi	Mode C Command Mapping GB1-128 Package	Data Bit	0..31	32..63
FBx_CMD3	FBx_CMD0		CKE_L	
FBx_CMD8	FBx_CMD1		A8	A8
FBx_CMD2	FBx_CMD2		CS0_L*	
FBx_CMD21	FBx_CMD3		A7	A6
FBx_CMD24	FBx_CMD4		A2	A1
FBx_CMD23	FBx_CMD5		A11	A9
FBx_CMD26	FBx_CMD6		A5	A4
FBx_CMD7	FBx_CMD7		A0	A12
FBx_CMD15	FBx_CMD8		CAS*	CAS*
FBx_CMD13	FBx_CMD9		BA1	A3
FBx_CMD4	FBx_CMD10		A9	A11
FBx_CMD18	FBx_CMD11			CS0_H
FBx_CMD29	FBx_CMD12		BA0	BA0
FBx_CMD27	FBx_CMD13		BA2	A15
FBx_CMD6	FBx_CMD14		A3	BA1
FBx_CMD17	FBx_CMD15			CS1_H
FBx_CMD19	FBx_CMD16			ODT_H
FBx_CMD22	FBx_CMD17		A4	A5
FBx_CMD12	FBx_CMD18		A13	A14
FBx_CMD28	FBx_CMD19		WE*	A10
FBx_CMD10	FBx_CMD20		A1	A2
FBx_CMD25	FBx_CMD21		A10	WE*
FBx_CMD9	FBx_CMD22		A12	A0
FBx_CMD1	FBx_CMD23		CS1_L*	
FBx_CMD11	FBx_CMD24		RAS*	RAS*
FBx_CMD0	FBx_CMD25		ODT_L	
FBx_CMD5	FBx_CMD26		A6	A7
FBx_CMD16	FBx_CMD27			CKE_H
FBx_CMD20	FBx_CMD28		RST	RST
FBx_CMD14	FBx_CMD29		A14	A13
FBx_CMD30	FBx_CMD30		A15	BA2
FBx_CMD31				
			LOW	HIGH



20091217
For layout convenient del R789 and R795



20091214 Modify	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix SA000032420	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K

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Compal Electronics, Inc.

Title: N11P-GV2H LVDS

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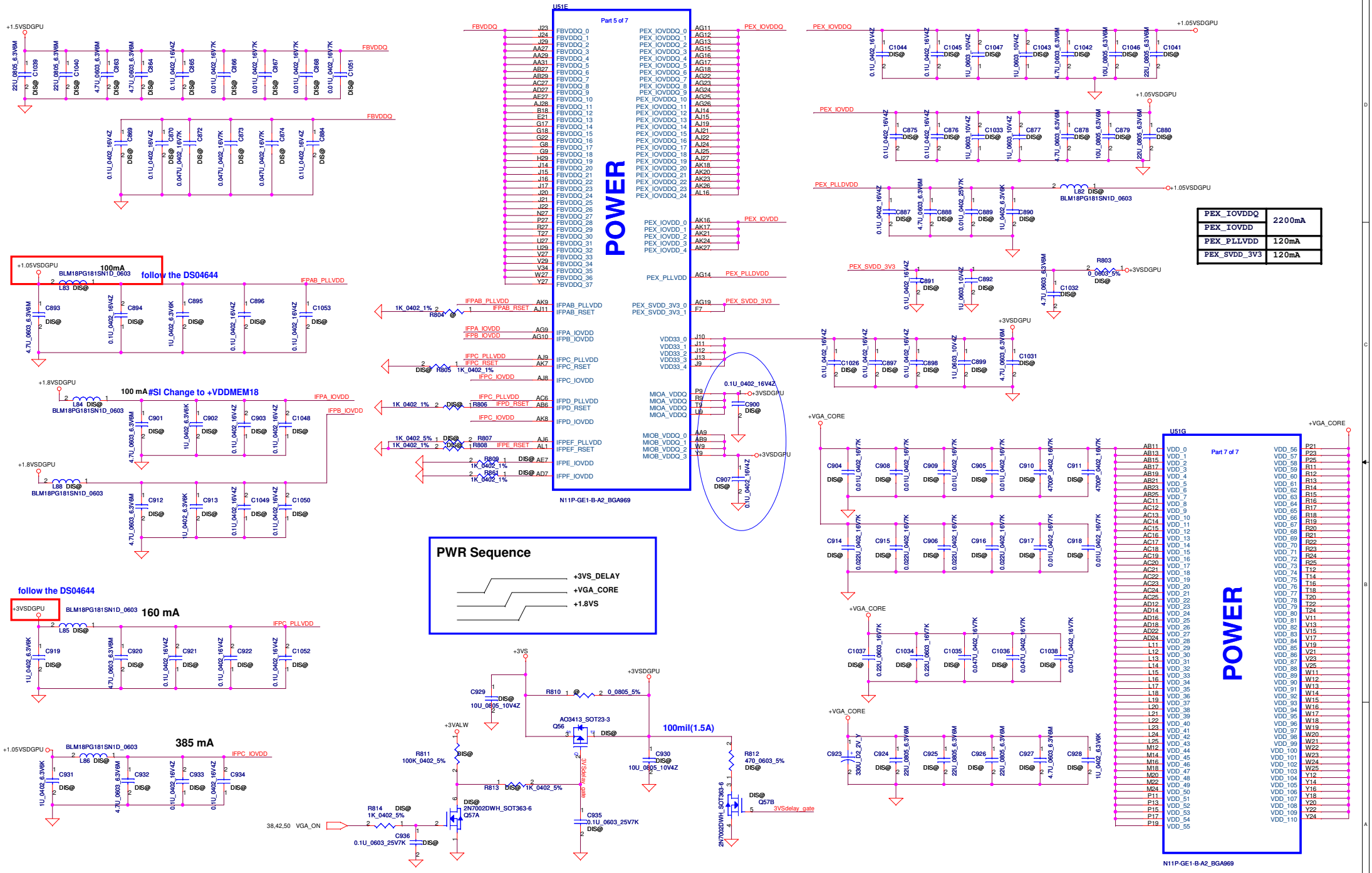

PEX_IOVDDQ	2200mA
PEX_IOVDD	
PEX_PLLVDD	120mA
PEX_SVDD_3V3	120mA

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Compal Electronics, Inc.

Title: **N11P-GV2H POWER & GND**

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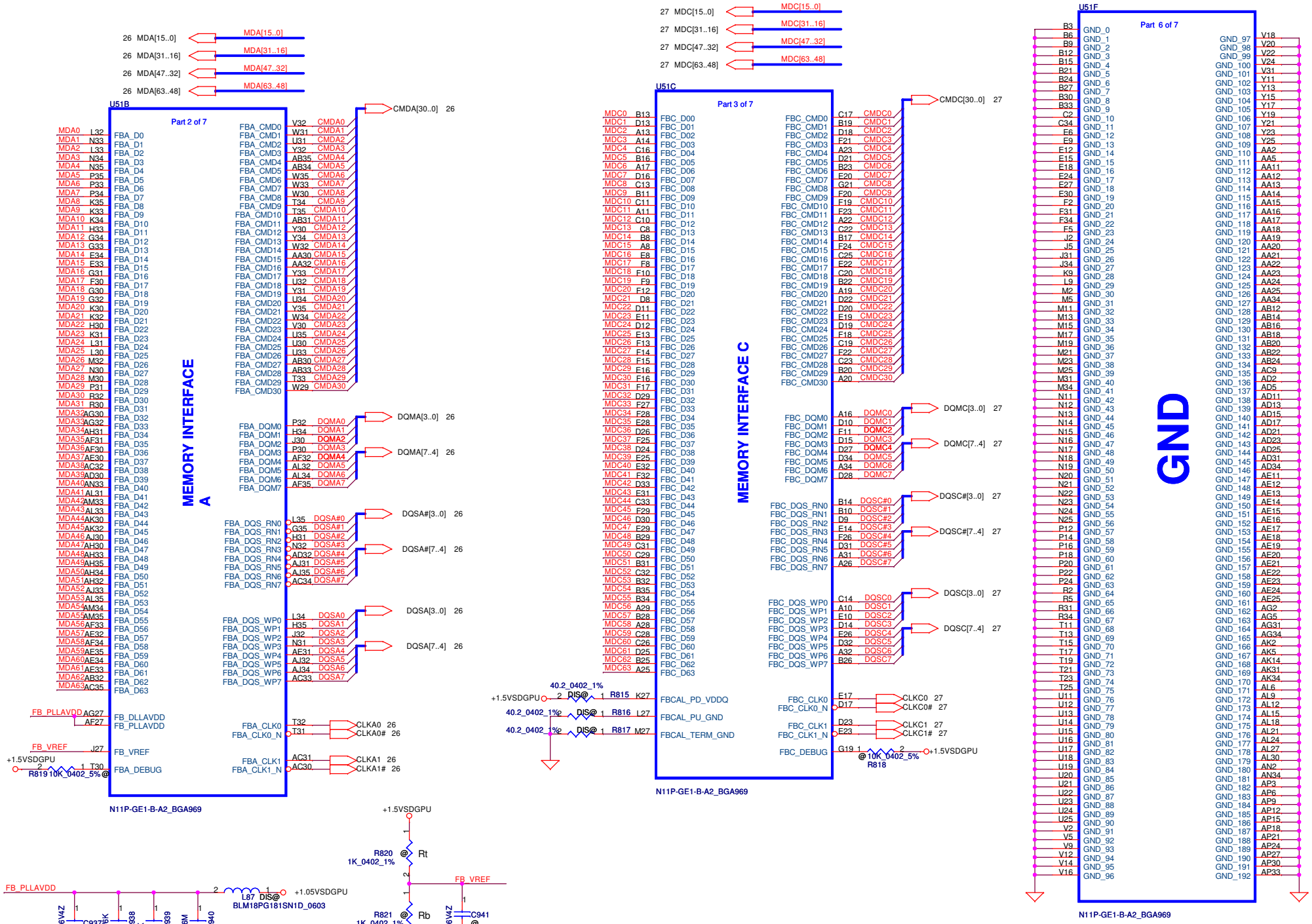

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Compal Electronics, Inc.

Title: **N11P-GV2H VRAM**

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 25 of 56

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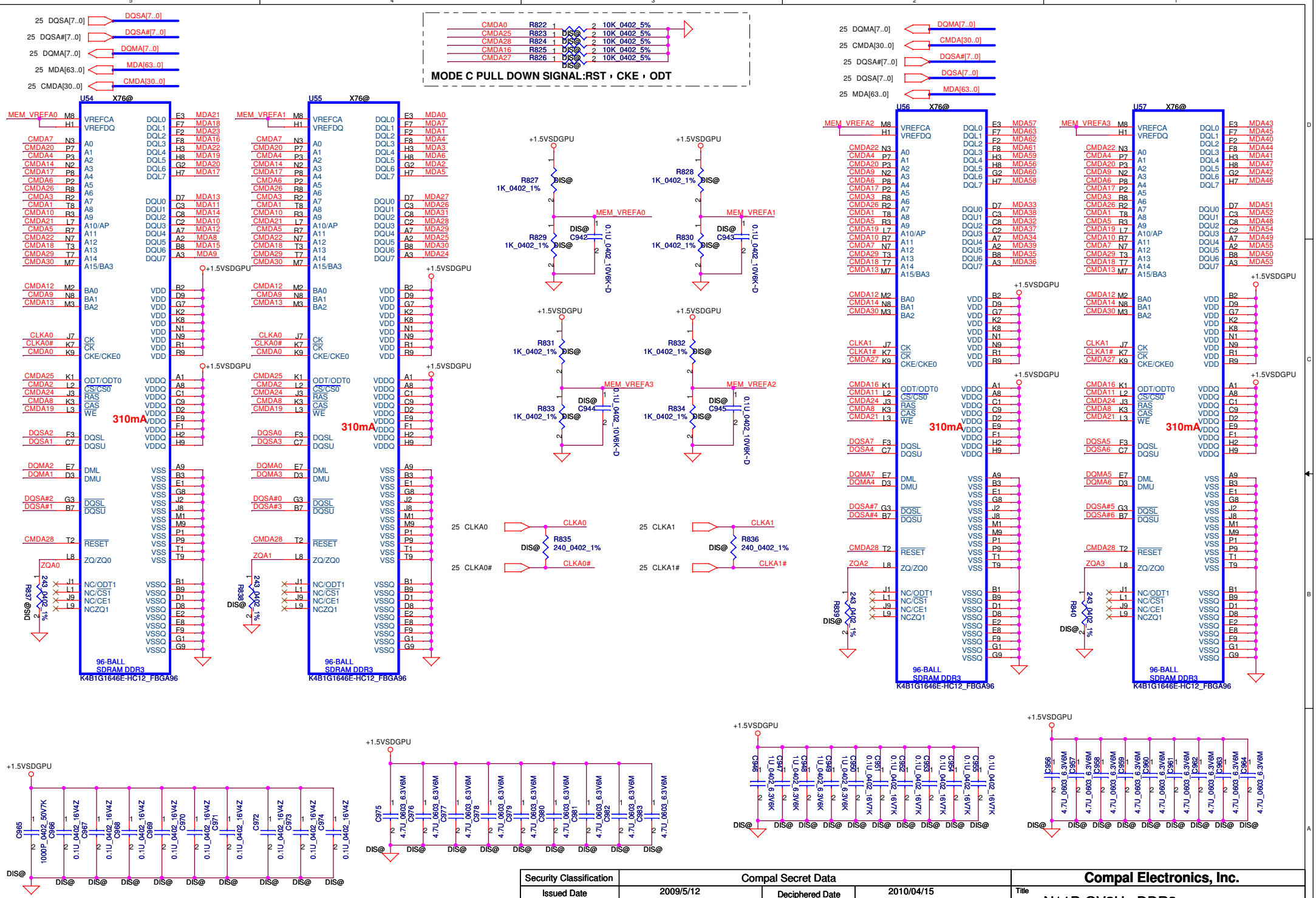

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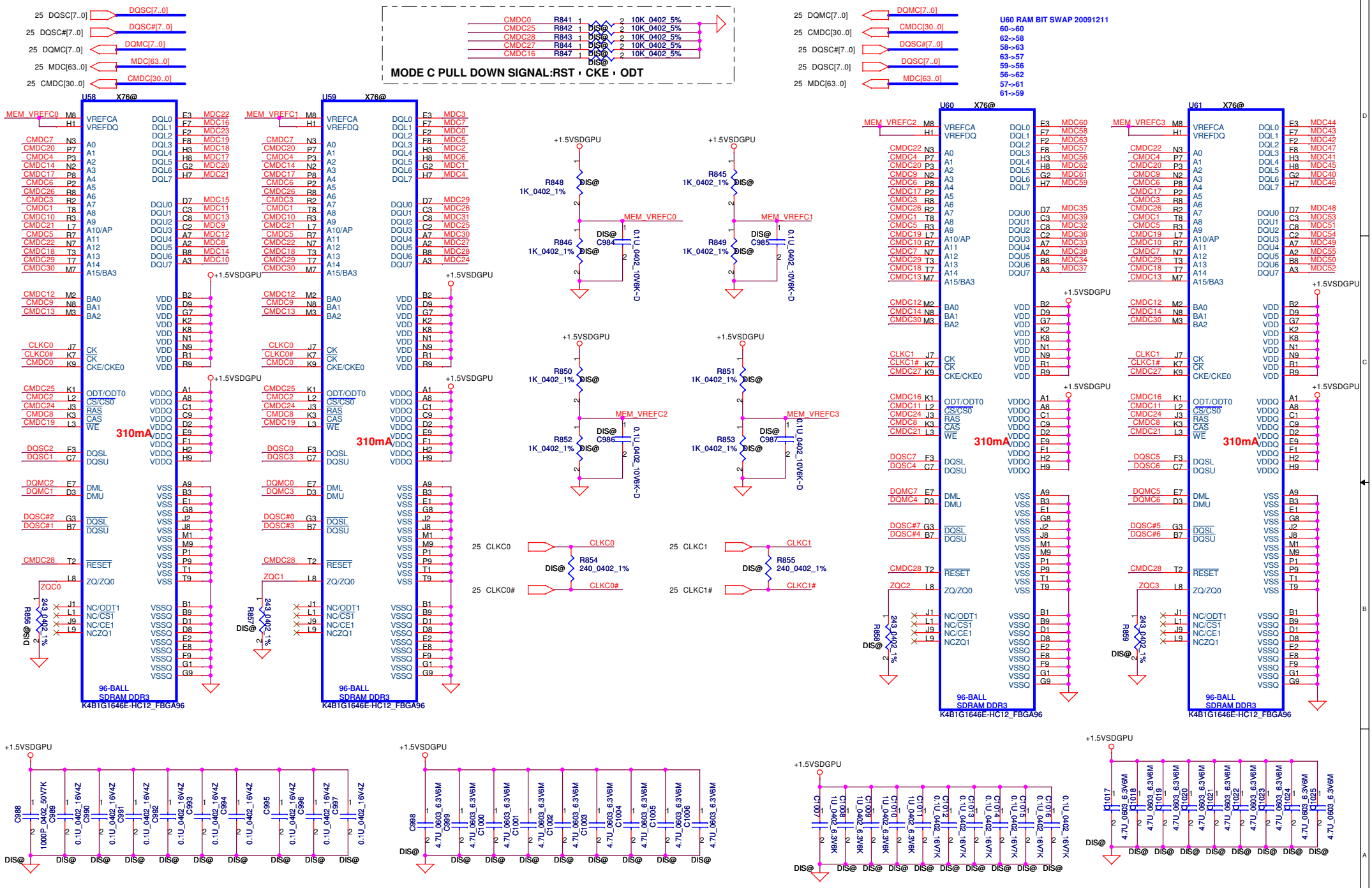
Compal Electronics, Inc.

Title: N11P-GV2H gDDR3

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev

Date: Tuesday, December 22, 2009 | Sheet 26 of 56



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Compal Electronics, Inc.

Title: N11P-GV2H gDDR3

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 27 of 56

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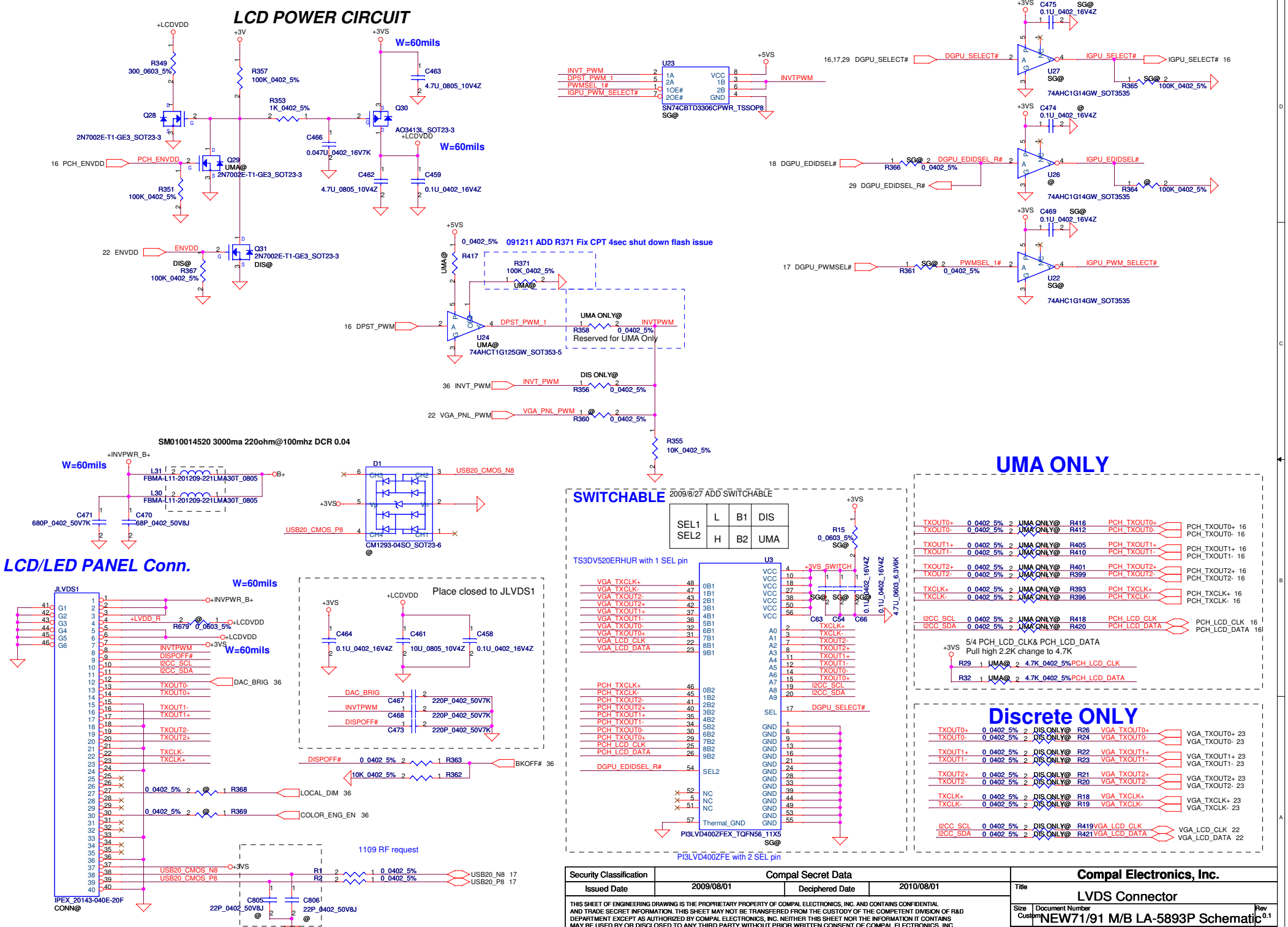
LCD POWER CIRCUIT



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Compal Electronics, Inc.

Title: LVDS Connector

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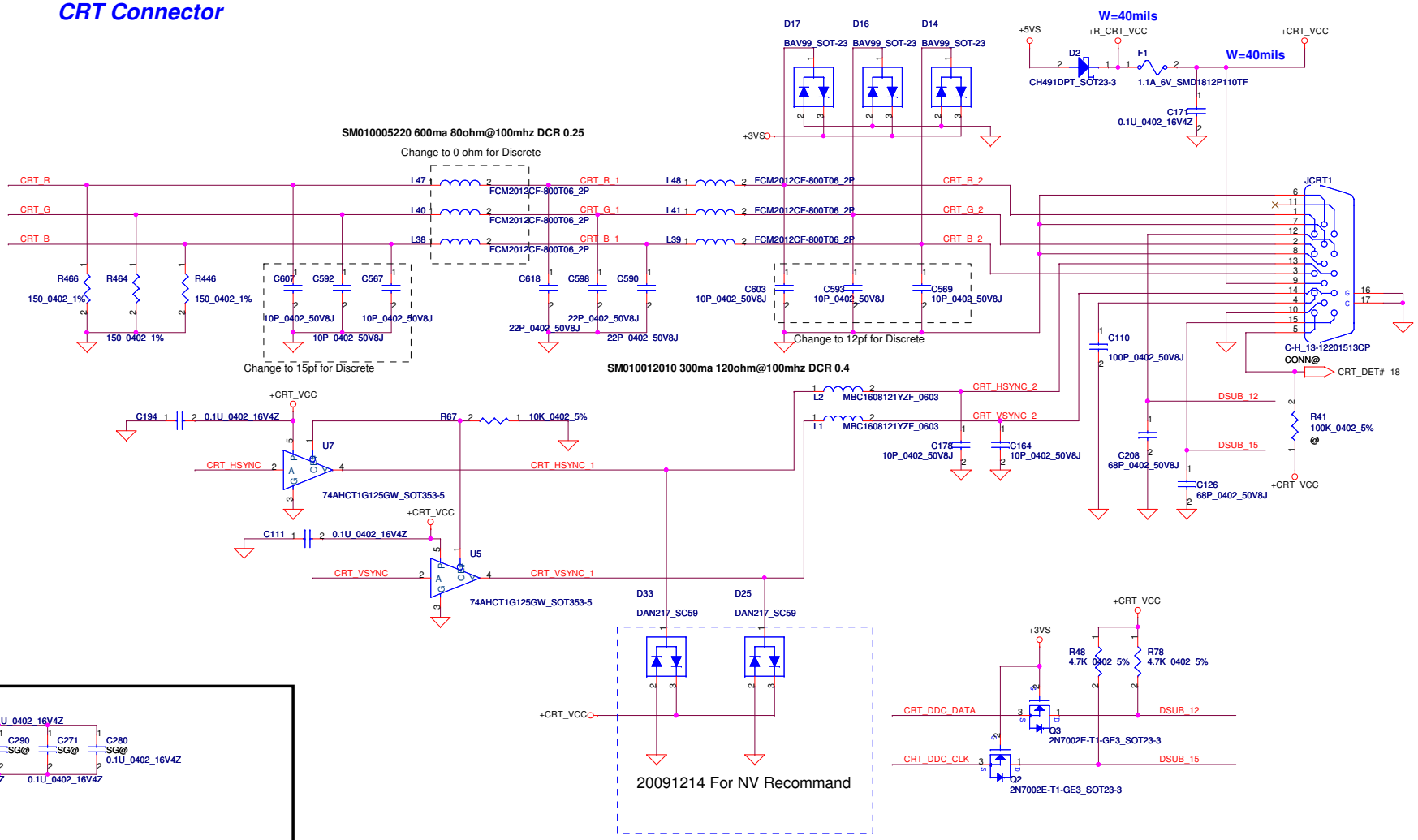
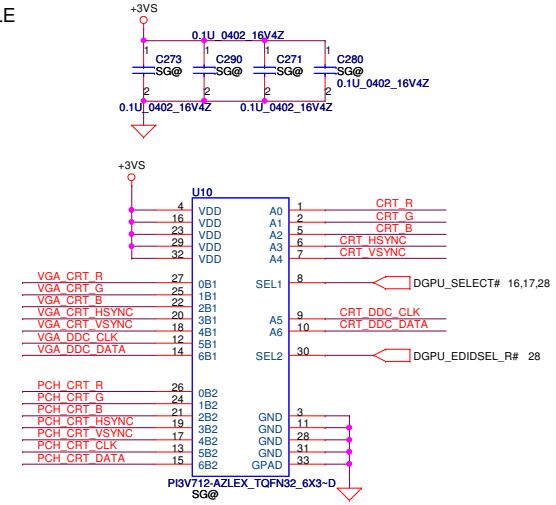
CRT Connector



SWITCHABLE

2009/08/27



L	B1	DIS
H	B2	UMA

Discrete only

22 VGA_CRT_R	VGA_CRT_R	R537	2	DIS ONLY@	0 0402 5%	CRT_R
22 VGA_CRT_G	VGA_CRT_G	R535	2	DIS ONLY@	0 0402 5%	CRT_G
22 VGA_CRT_B	VGA_CRT_B	R533	2	DIS ONLY@	0 0402 5%	CRT_B
22 VGA_CRT_HSYNC	VGA_CRT_HSYNC	R531	2	DIS ONLY@	0 0402 5%	CRT_HSYNC
22 VGA_CRT_VSYNC	VGA_CRT_VSYNC	R529	2	DIS ONLY@	0 0402 5%	CRT_VSYNC
22 VGA_DDC_CLK	VGA_DDC_CLK	R527	2	DIS ONLY@	0 0402 5%	CRT_DDC_CLK
22 VGA_DDC_DATA	VGA_DDC_DATA	R526	2	DIS ONLY@	0 0402 5%	CRT_DDC_DATA

VGA_DDC_DATA and VGA_DDC_CLK Pull high at Page22

UMA only

16 PCH_CRT_R	PCH_CRT_R	R536	2	UMA ONLY@	0 0402 5%	CRT_R
16 PCH_CRT_G	PCH_CRT_G	R534	2	UMA ONLY@	0 0402 5%	CRT_G
16 PCH_CRT_B	PCH_CRT_B	R532	2	UMA ONLY@	0 0402 5%	CRT_B
16 PCH_CRT_HSYNC	PCH_CRT_HSYNC	R530	2	UMA ONLY@	0 0402 5%	CRT_HSYNC
16 PCH_CRT_VSYNC	PCH_CRT_VSYNC	R528	2	UMA ONLY@	0 0402 5%	CRT_VSYNC
16 PCH_CRT_CLK	PCH_CRT_CLK	R544	2	UMA ONLY@	0 0402 5%	CRT_DDC_CLK
16 PCH_CRT_DATA	PCH_CRT_DATA	R543	2	UMA ONLY@	0 0402 5%	CRT_DDC_DATA

PCH DDC PU 2.2K on Page 17

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 29 of 56

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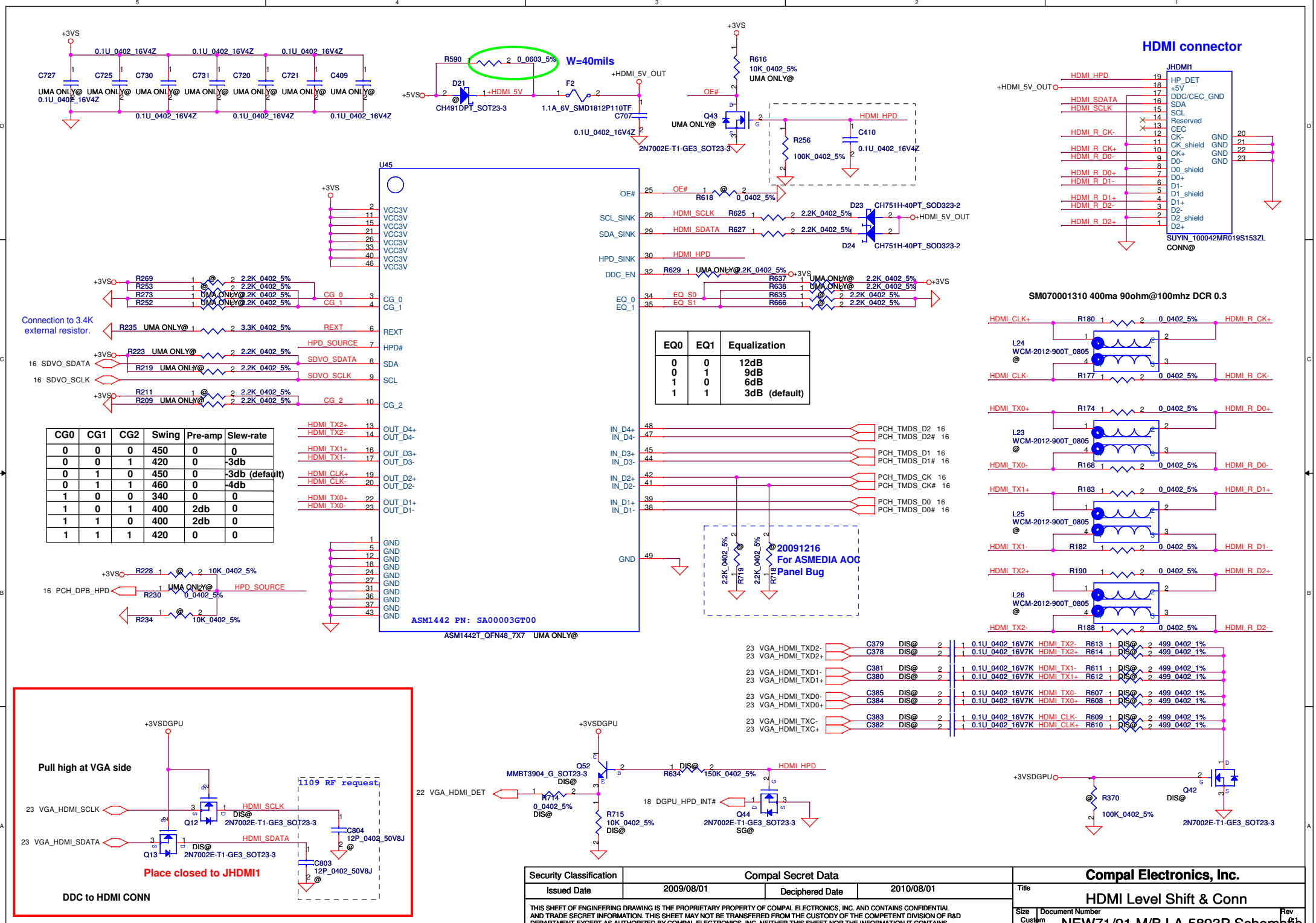
GRATIS - FOR FREE



EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

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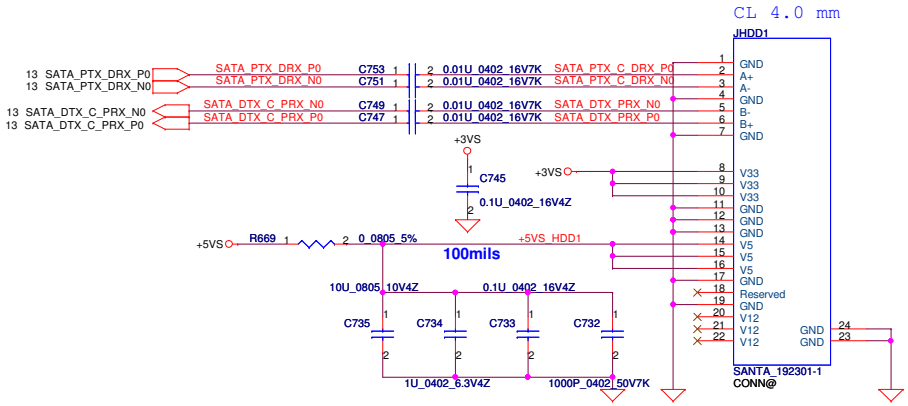
Compal Electronics, Inc.

Title: HDMI Level Shift & Conn

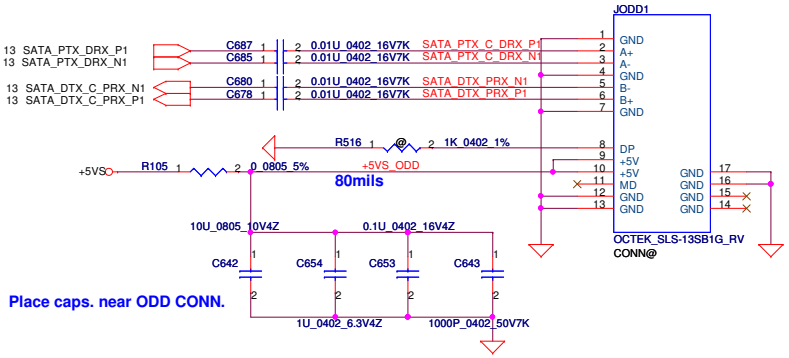
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 30 of 56

SATA HDD1 Conn.



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 31 of 56

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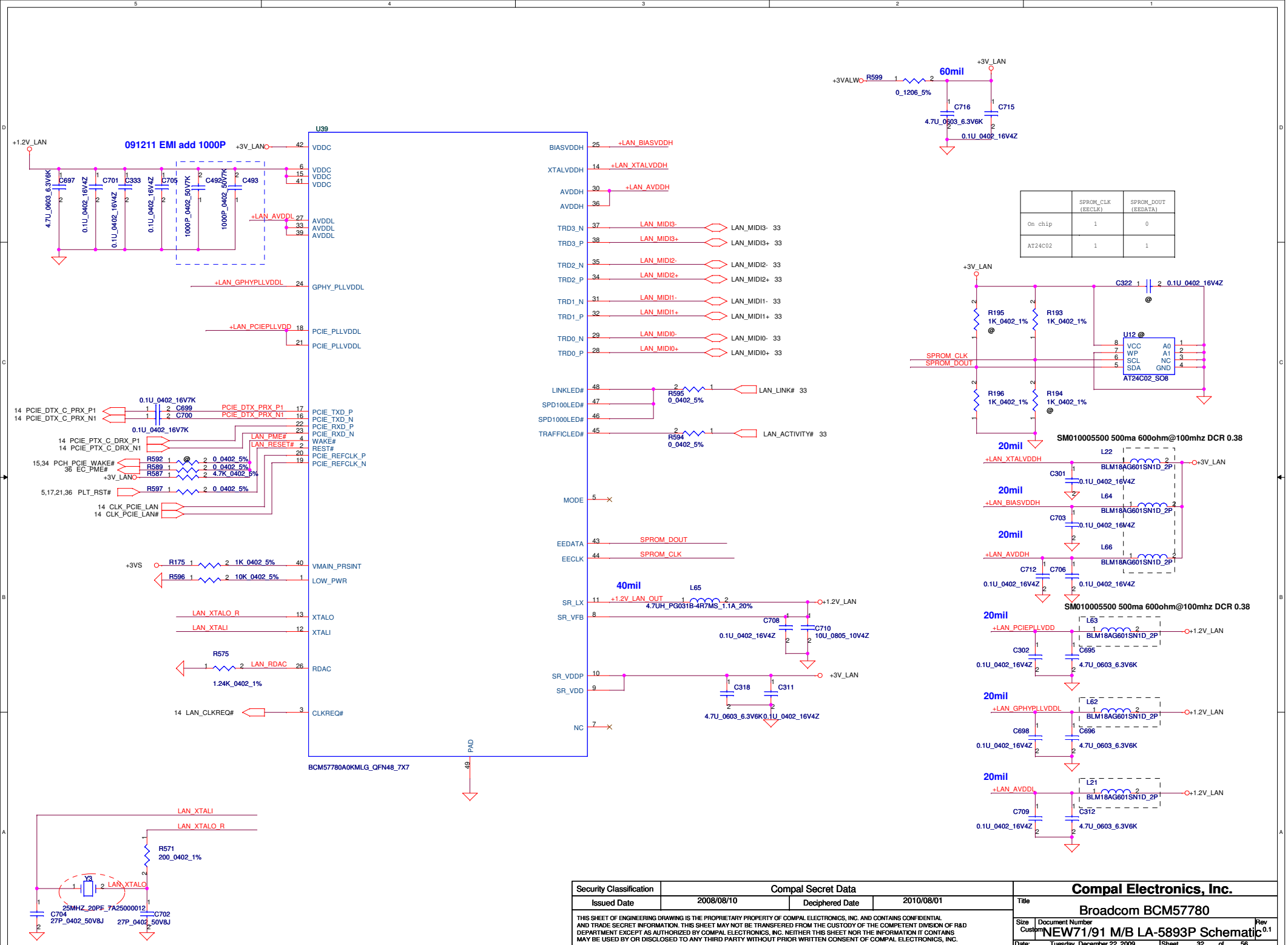
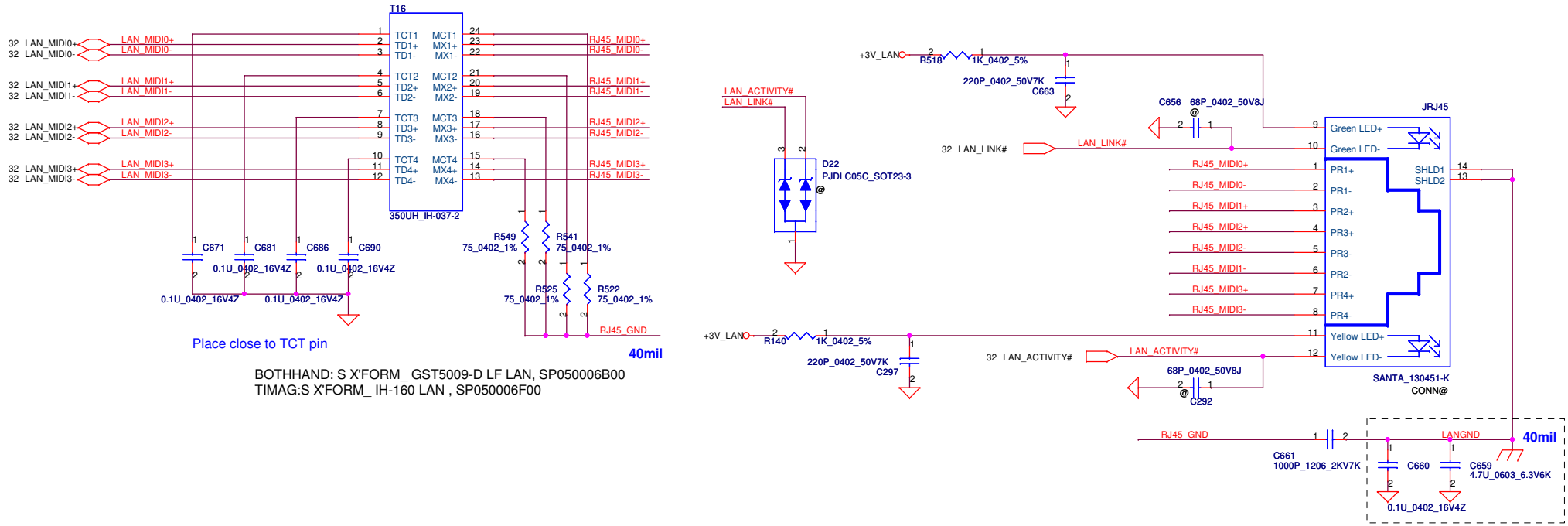


	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

LAN Connector



BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

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Issued Date	2008/08/10	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 33 of 56

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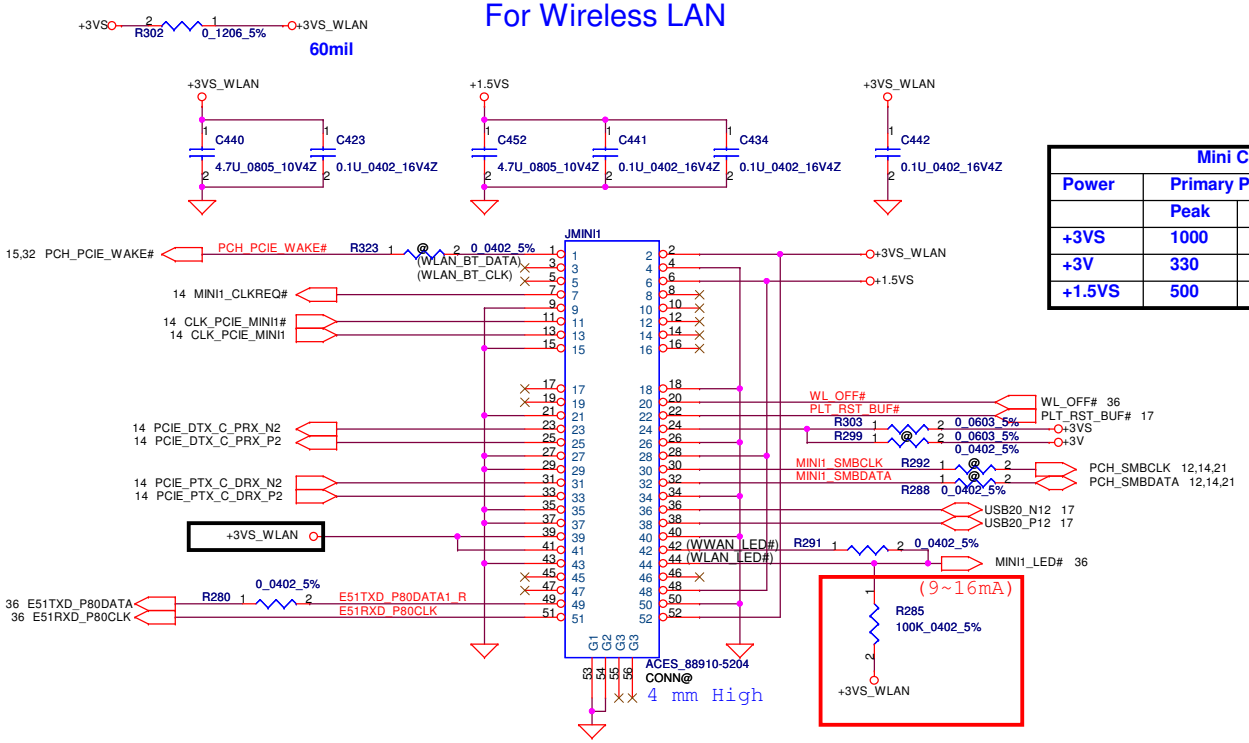
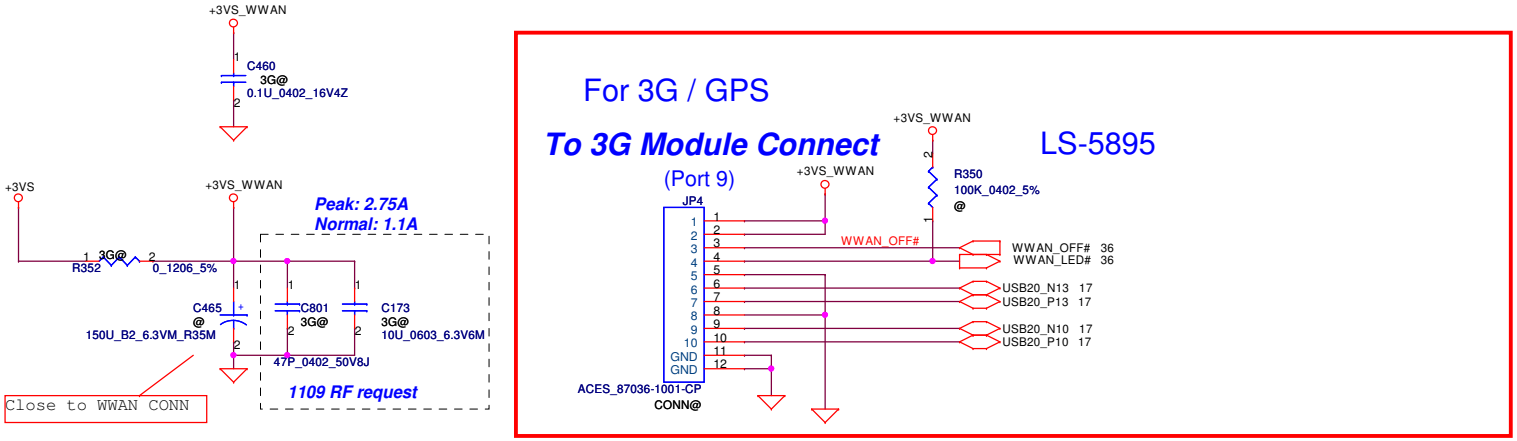
For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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Issued Date	2008/08/10	Deciphered Date	2010/08/01

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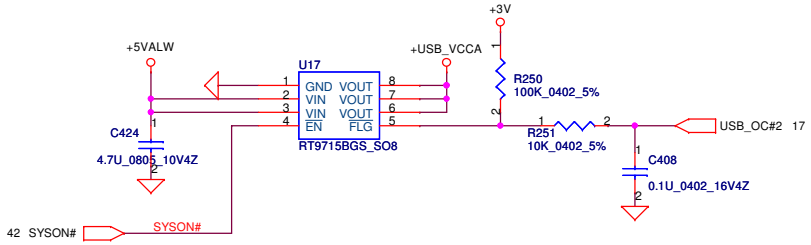
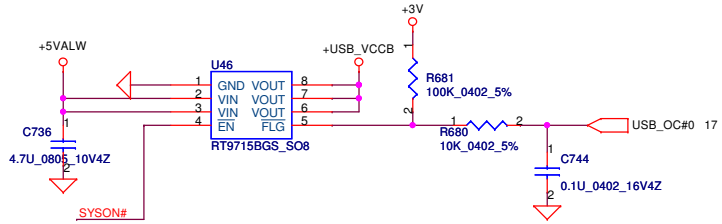
Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

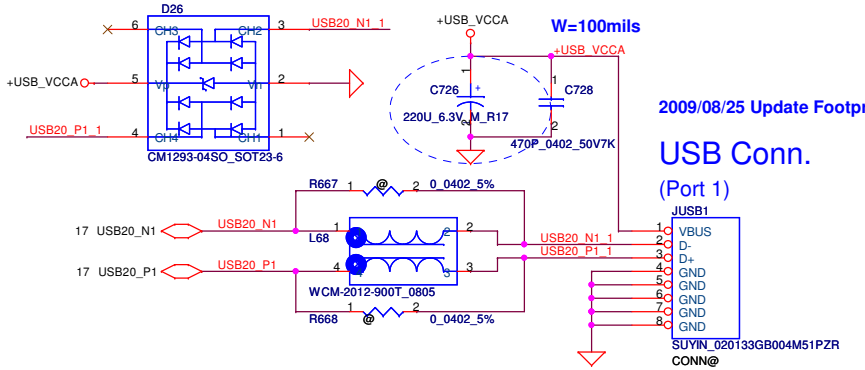
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 34 of 56





2009/08/14 CHANGE cap



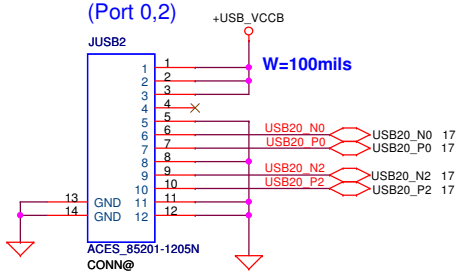
2009/08/25 Update Footprint(follow NAL00)

USB Conn.

(Port 1)

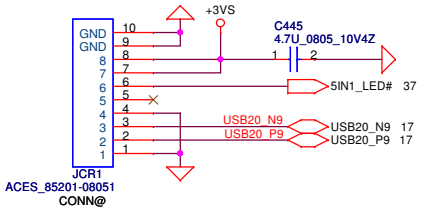
USB/B Conn. LS-5891

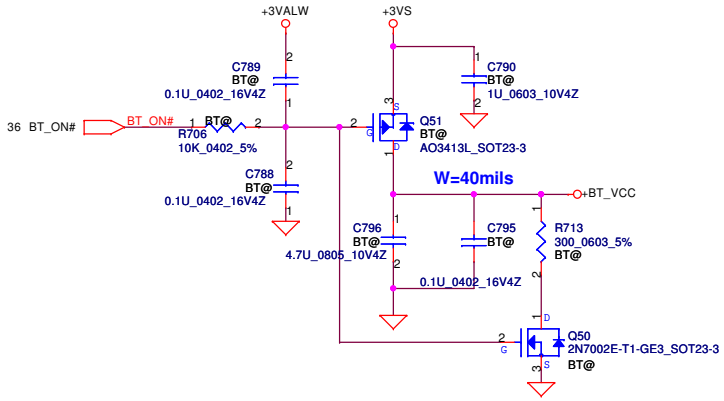
(Port 0,2)



2009/08/24 CHANGE Conn to FFC Type

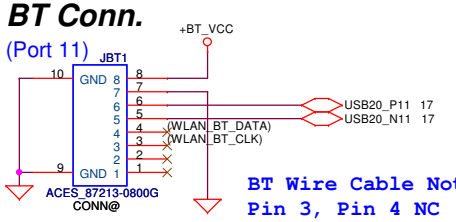
Card Reader Conn. LS-5896





BT Conn.

(Port 11)



BT Wire Cable Note:
Pin 3, Pin 4 NC

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Compal Electronics, Inc.

Title: USB / BT / USBB

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Thursday, December 24, 2009 | Sheet 35 of 56

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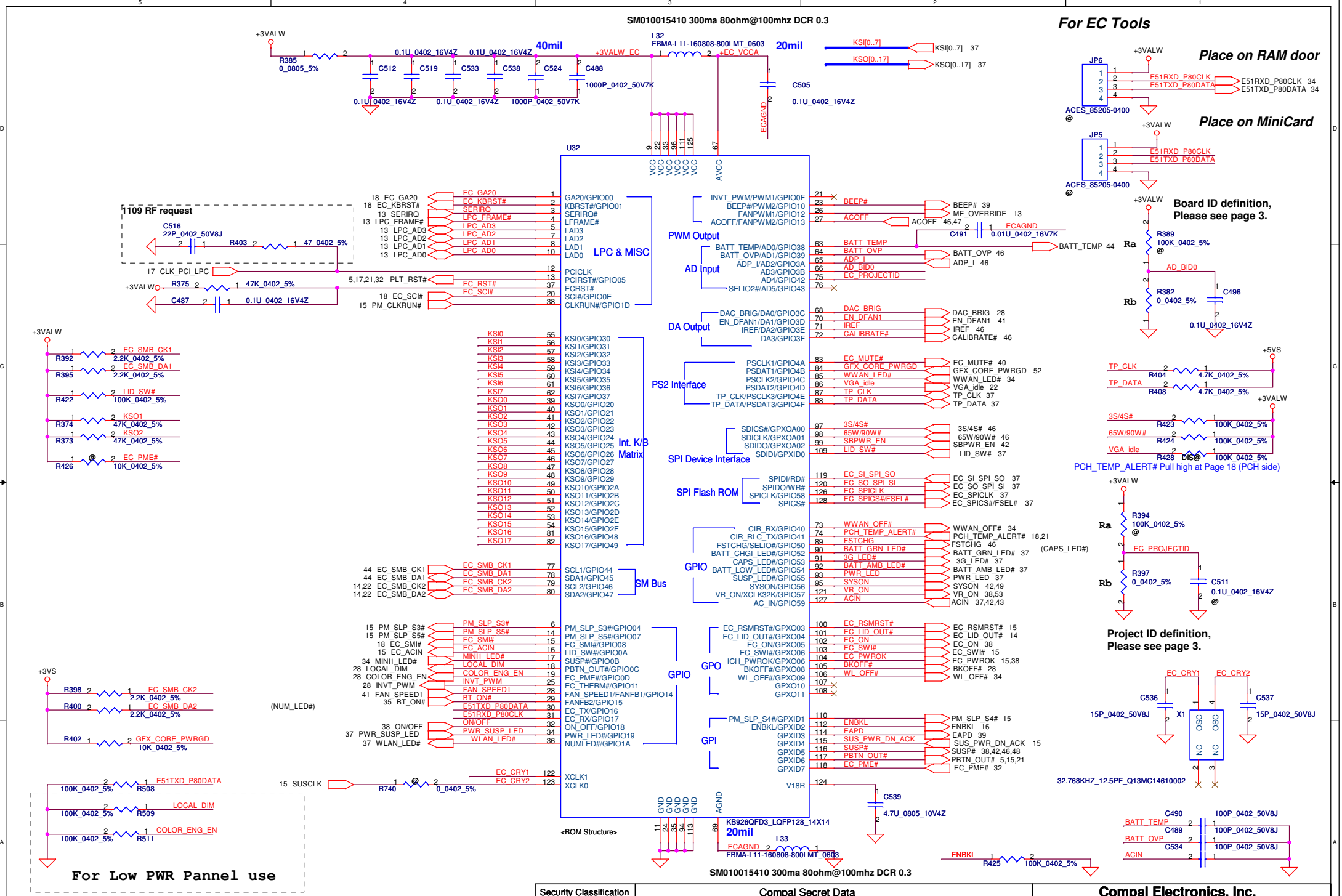

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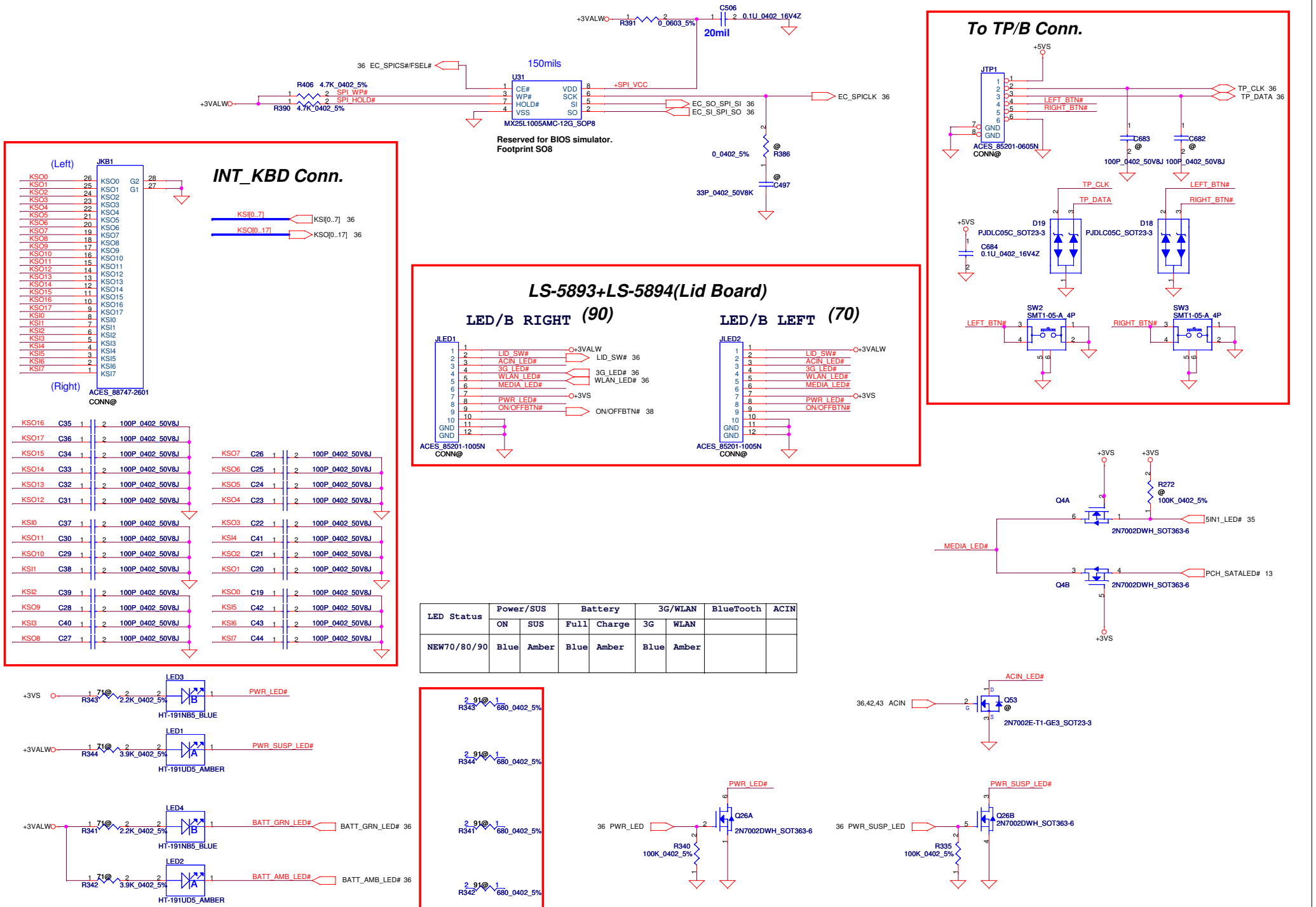
Compal Electronics, Inc.

Title: EC ENE KB926

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 36 of 56



LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 37 of 56

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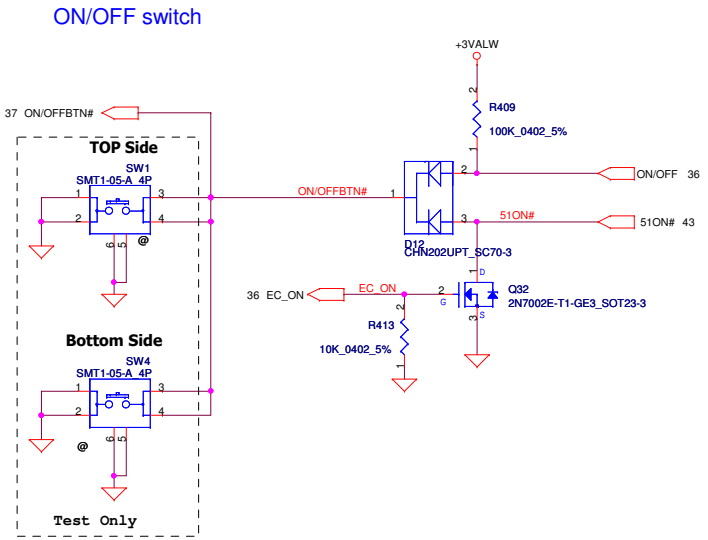
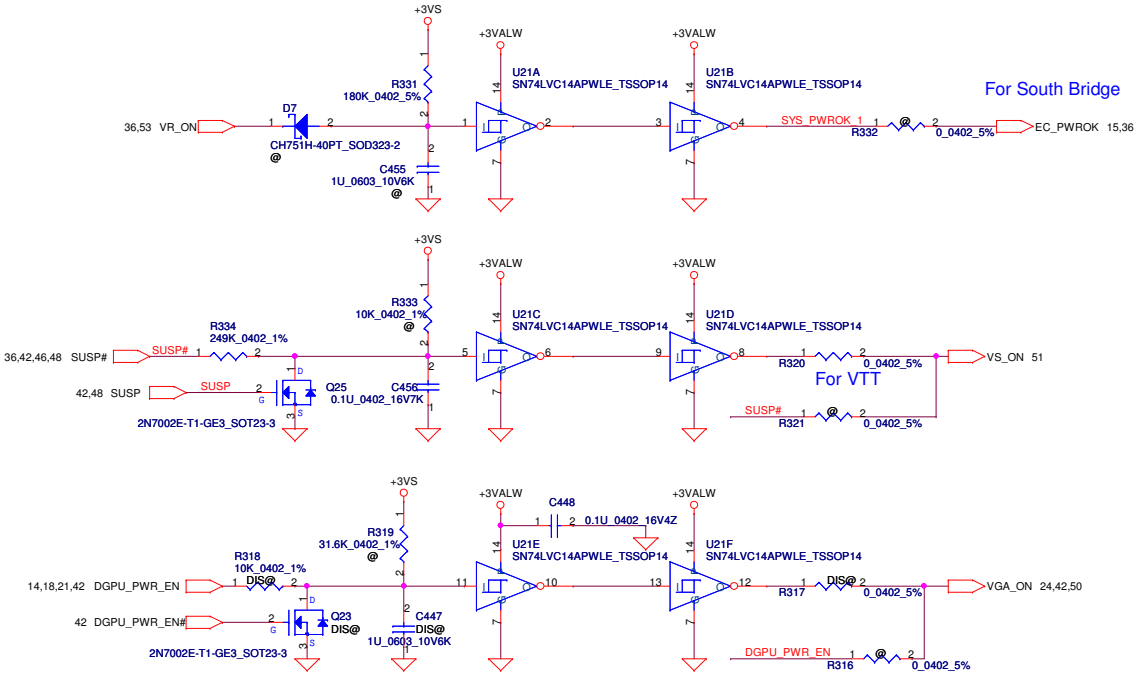
Power Button



Power ON Circuit



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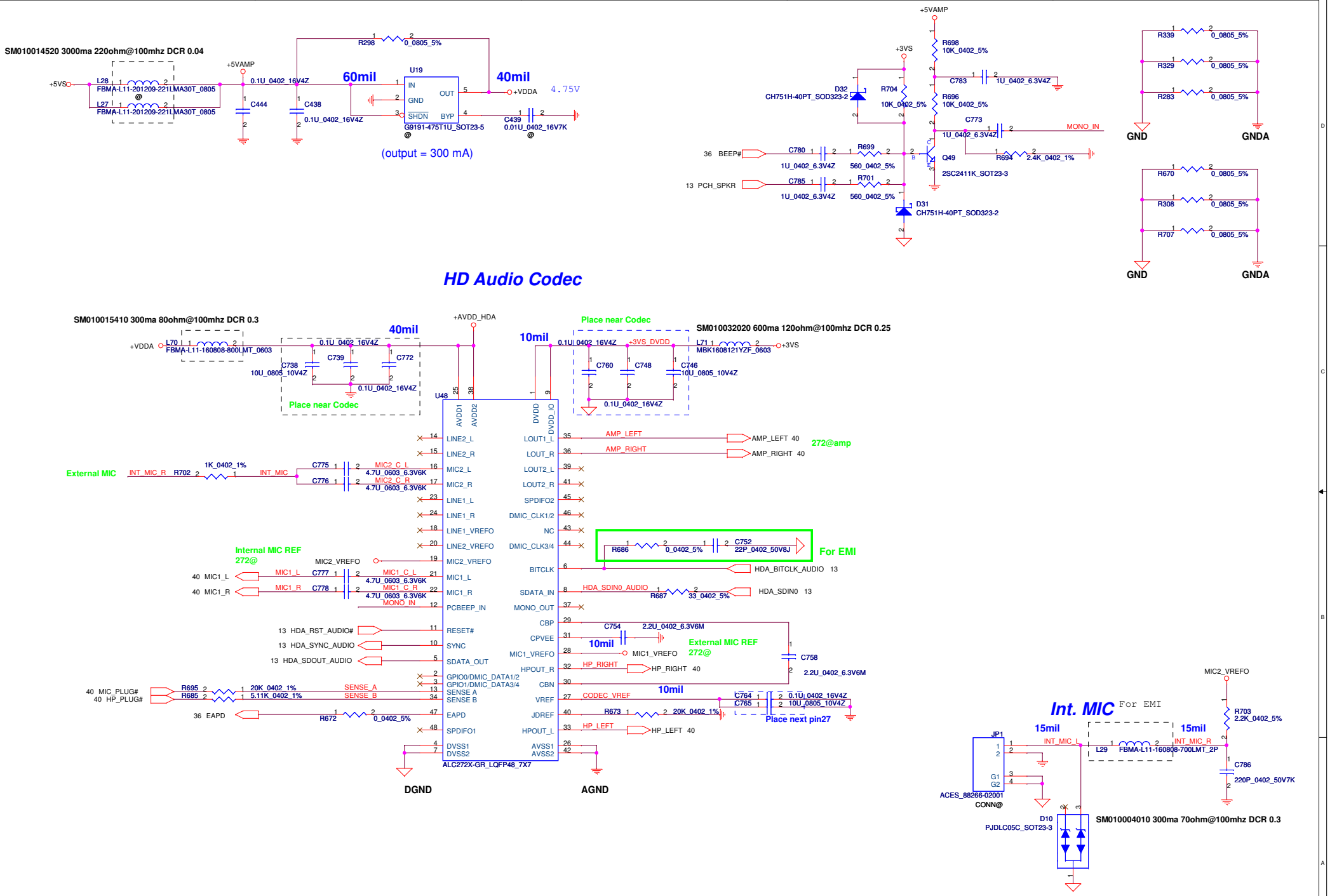
Compal Electronics, Inc.

Title: Power OK

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 38 of 56



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Compal Electronics, Inc.

Title: HD Audio Codec ALC272X

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

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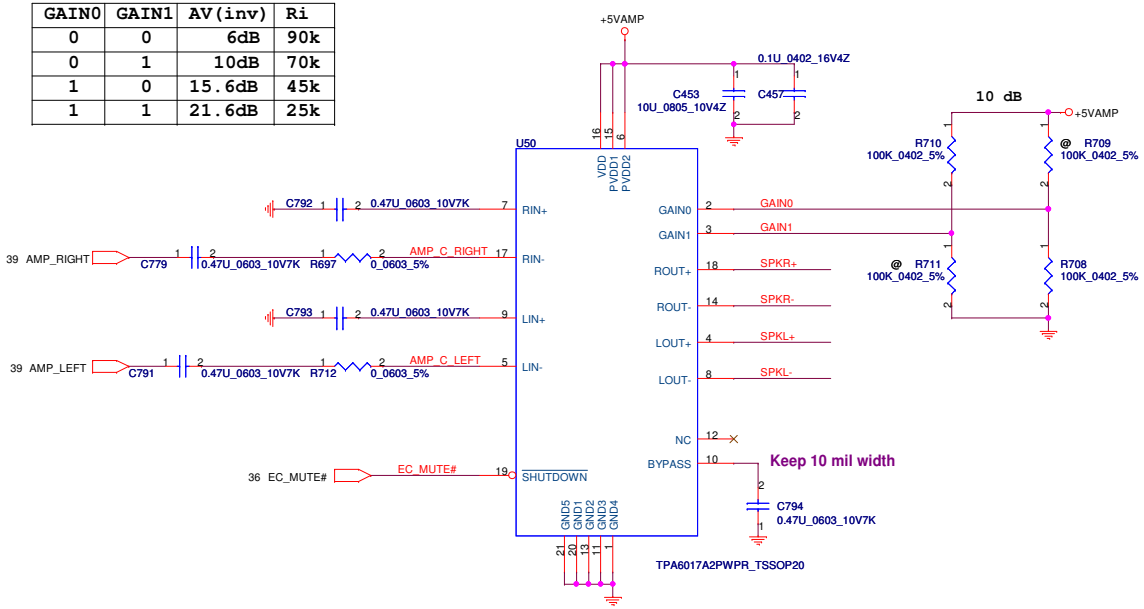
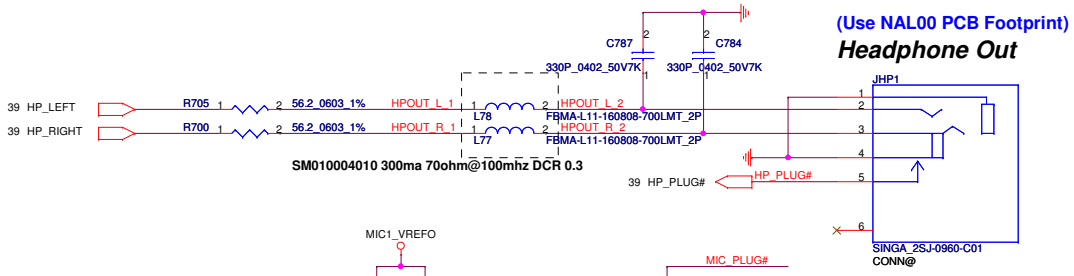
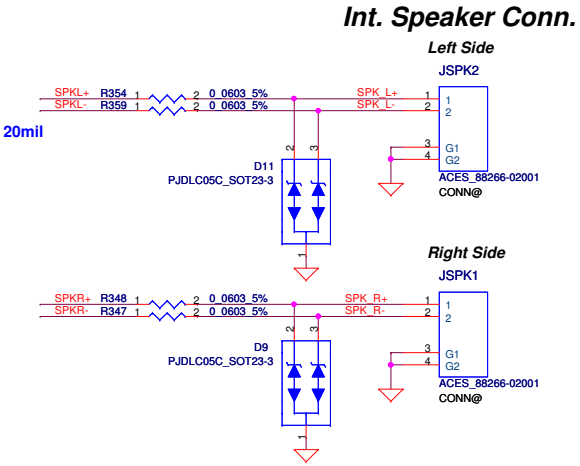
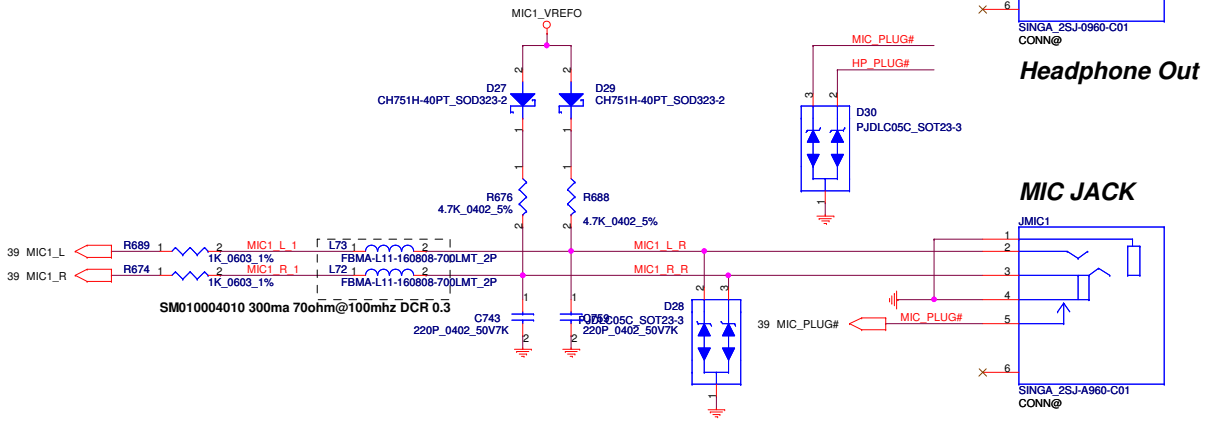
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k









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Issued Date	2008/08/10	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: Amplifier & Audio Jack

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

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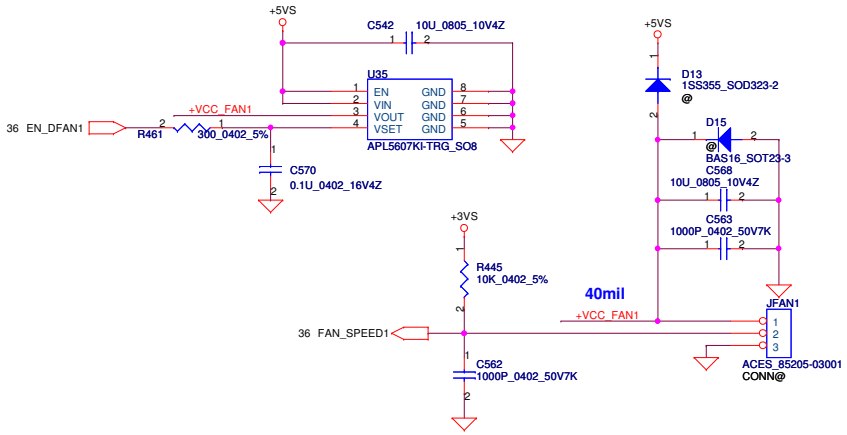
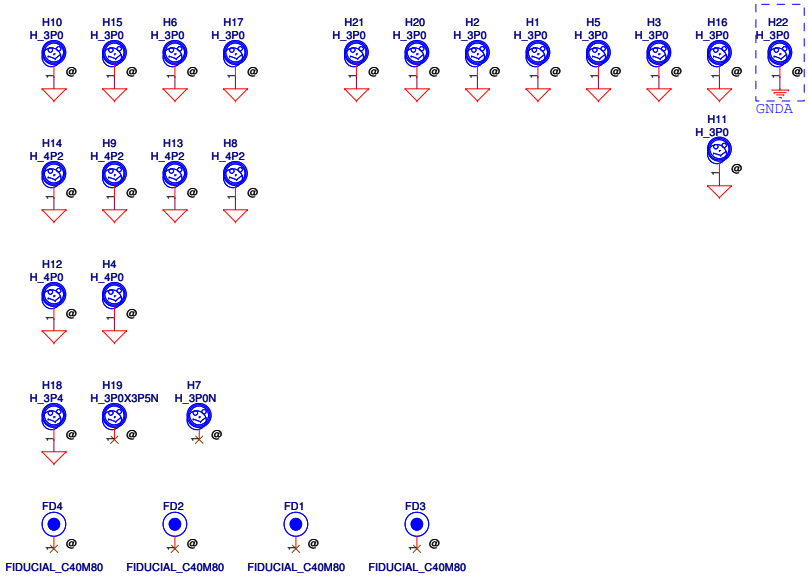
FAN1 Conn





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Compal Electronics, Inc.

Title: FAN & Screw Hole

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

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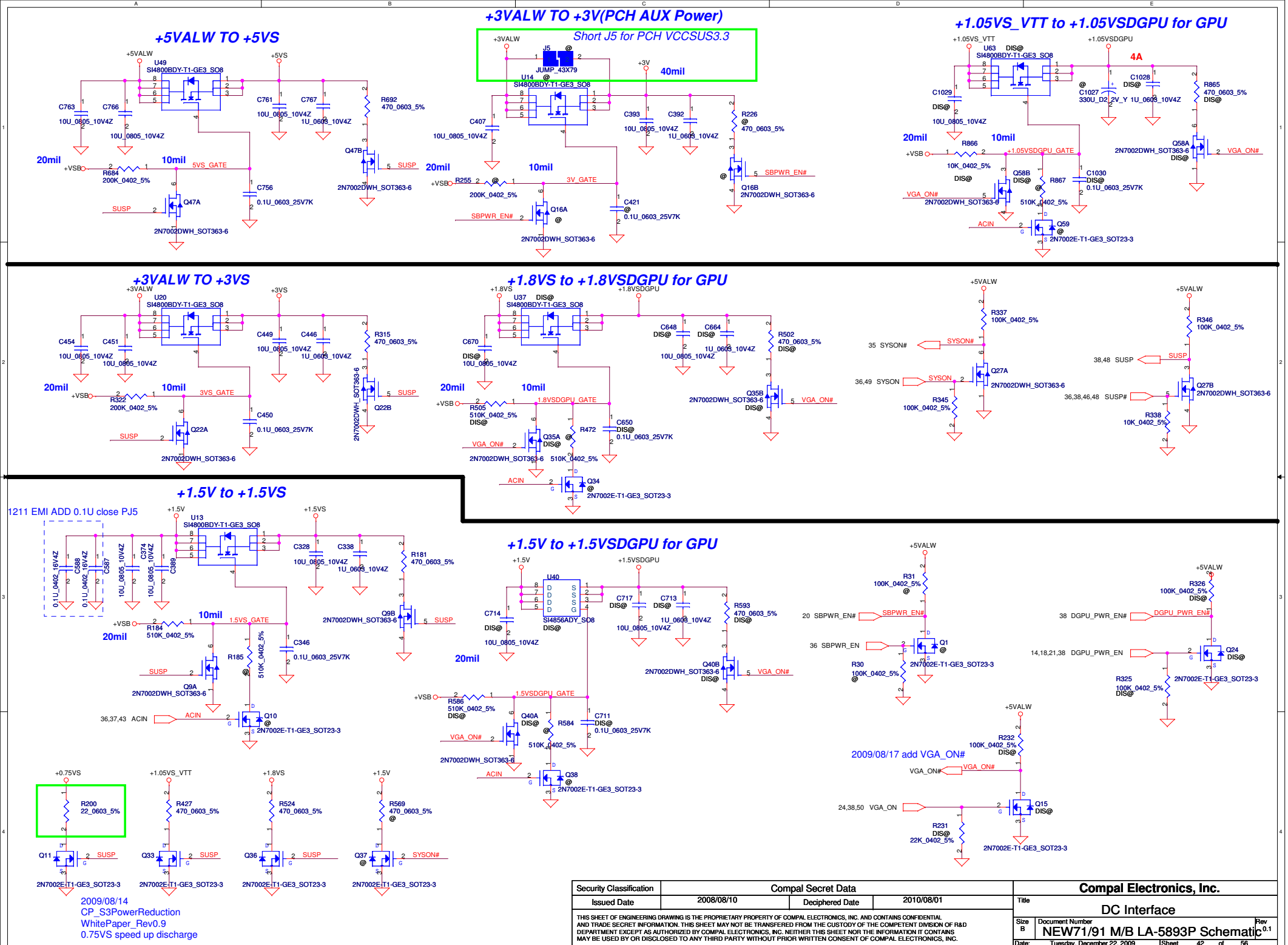
+5VALW TO +5VS
+3VALW TO +3V(PCH AUX Power)
Short J5 for PCH VCCSUS3.3
+1.05VS_VTT to +1.05VSDGPU for GPU
+3VALW TO +3VS
+1.8VS to +1.8VSDGPU for GPU
+1.5V to +1.5VS
1211 EMI ADD 0.1U close PJ5
+1.5V to +1.5VSDGPU for GPU
2009/08/17 add VGA_ON#
2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge
Security Classification
Compal Secret Data
Issued Date
2008/08/10
Deciphered Date
2010/08/01
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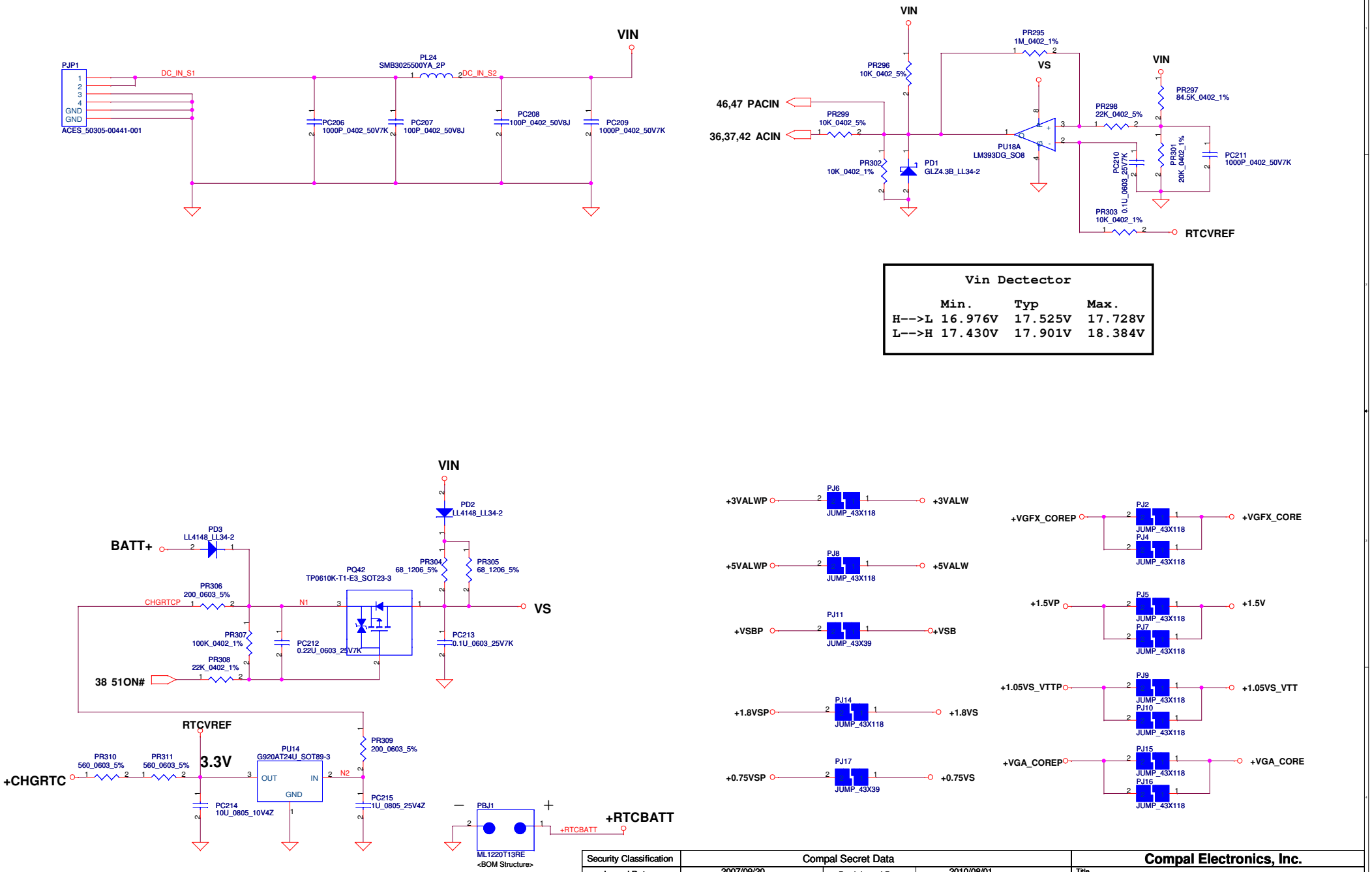
Compal Electronics, Inc.
Title
DC Interface
Size
B
Document Number
NEW71/91 M/B LA-5893P Schematic
Rev
0.1
Date: Tuesday, December 22, 2009
Sheet 42 of 56



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: **DCIN & DETECTOR**

Size: Custom | Document Number: NEW71 | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 43 of 56

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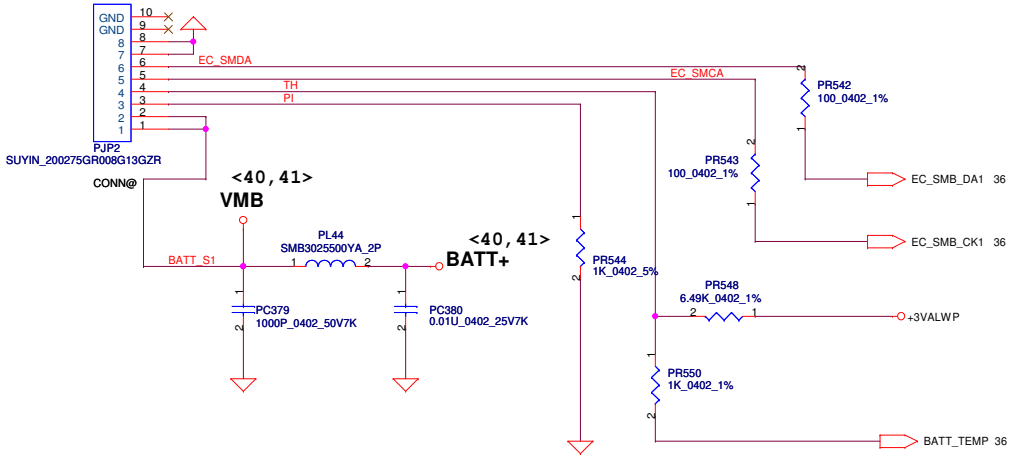
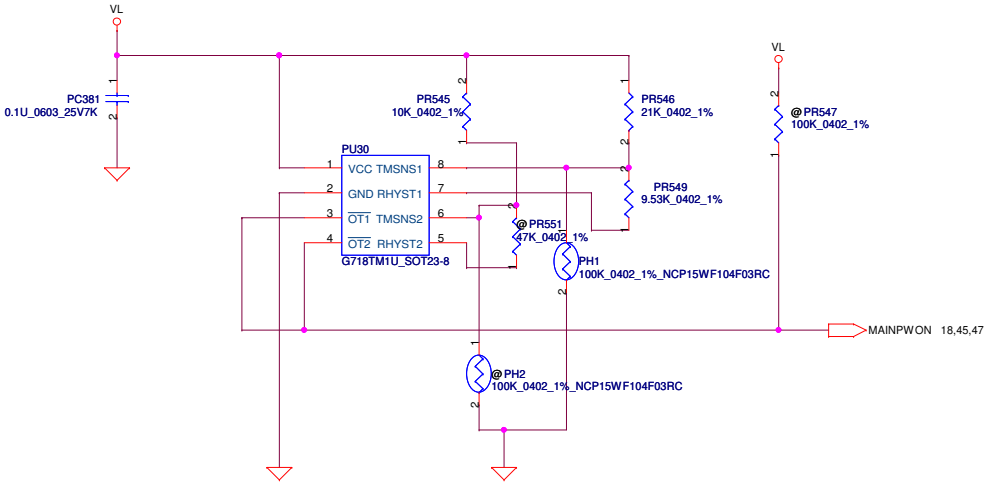
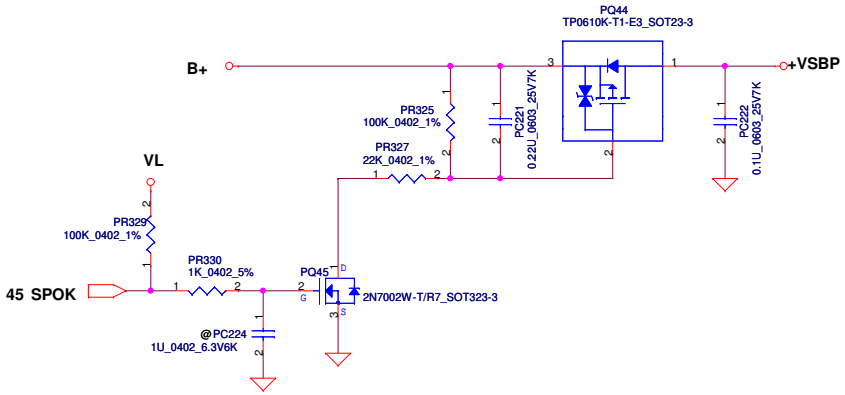


PH1 under CPU botten side :

CPU thermal protection at 92 degree C





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Issued Date	2007/09/20	Deciphered Date	2010/08/01

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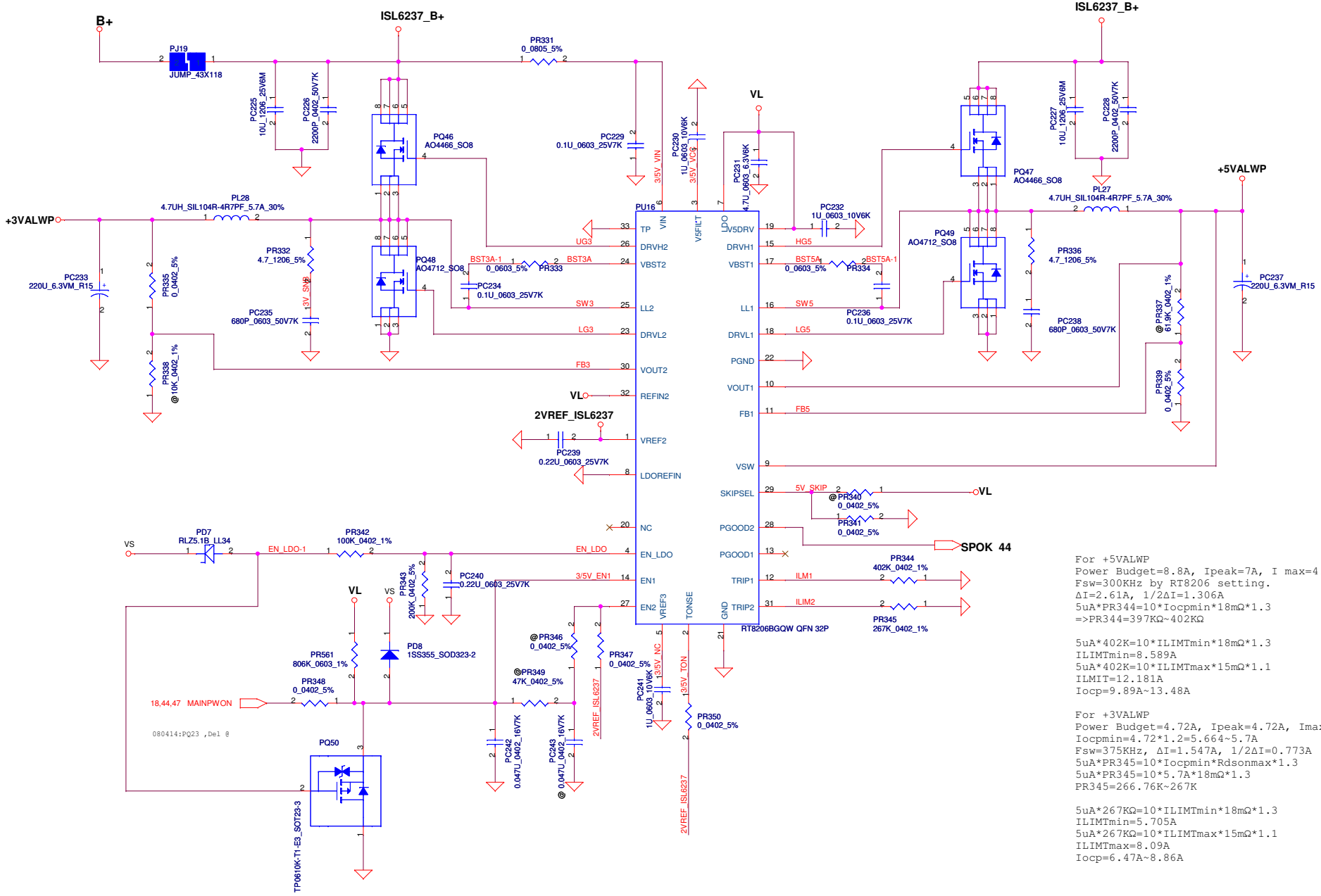
Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size: Custom | Document Number: NEW71 | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 44 of 56



For +5VALWP
Power Budget=8.8A, Ipeak=7A, I max=4.9A
Fsw=300KHz by RT8206 setting.
ΔI=2.61A, 1/2ΔI=1.306A
5uA*PR344=10*Iocpmin*18mΩ*1.3
=>PR344=397KΩ~402KΩ

5uA*402K=10*ILIMTmin*18mΩ*1.3
ILIMTmin=8.589A
5uA*402K=10*ILIMTmax*15mΩ*1.1
ILMIT=12.181A
Iocp=9.89A~13.48A

For +3VALWP
Power Budget=4.72A, Ipeak=4.72A, Imax=4A
Iocpmin=4.72*1.2=5.664~5.7A
Fsw=375KHz, ΔI=1.547A, 1/2ΔI=0.773A
5uA*PR345=10*Iocpmin*Rdsonmax*1.3
5uA*PR345=10*5.7A*18mΩ*1.3
PR345=266.76K~267K

5uA*267KΩ=10*ILIMTmin*18mΩ*1.3
ILIMTmin=5.705A
5uA*267KΩ=10*ILIMTmax*15mΩ*1.1
ILIMTmax=8.09A
Iocp=6.47A~8.86A

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: NEW71 | Rev: 0.1

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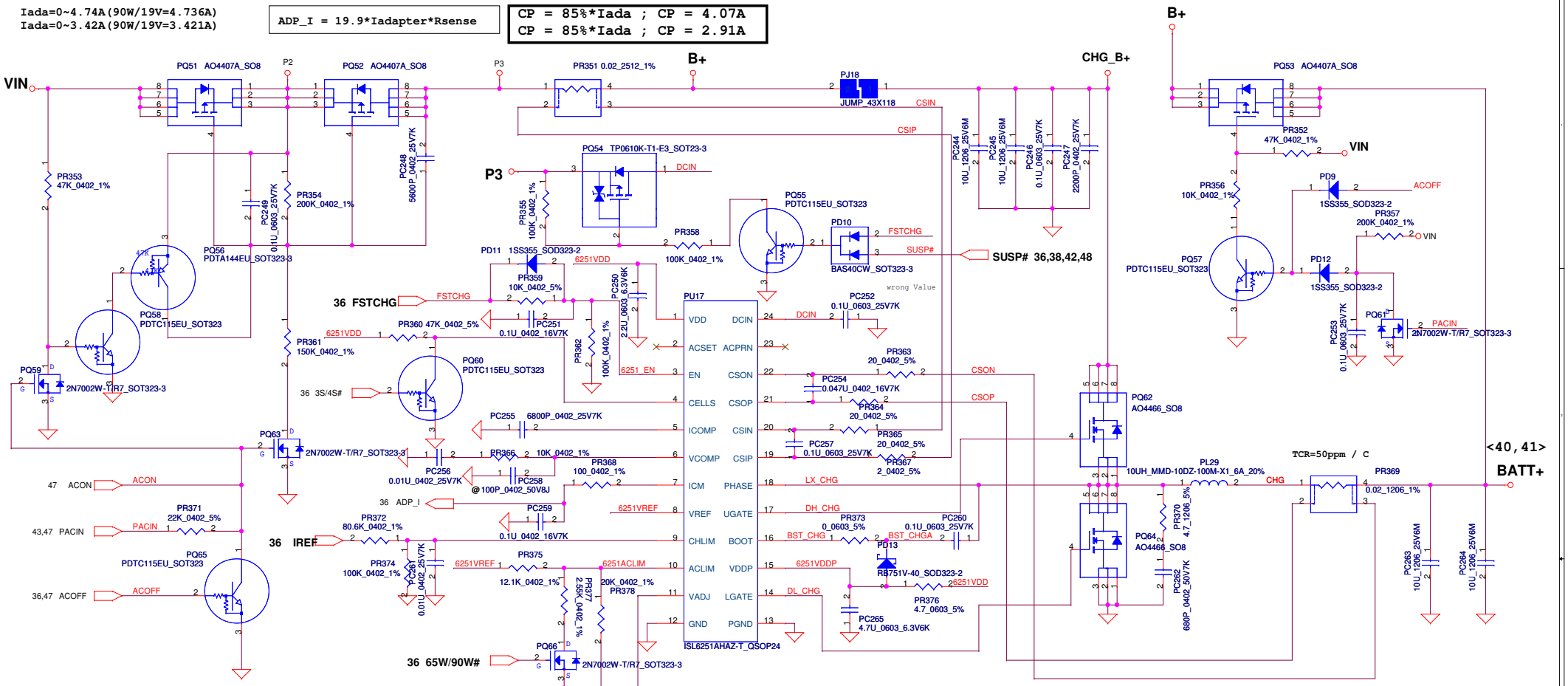
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
Iref=0.7224*Ichanrge
kI=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

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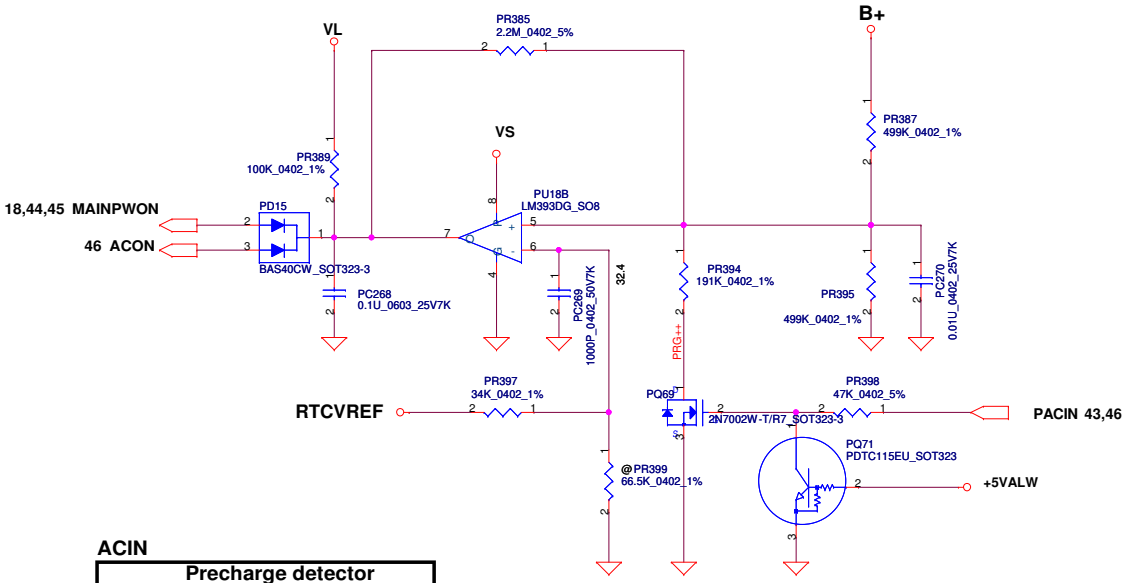
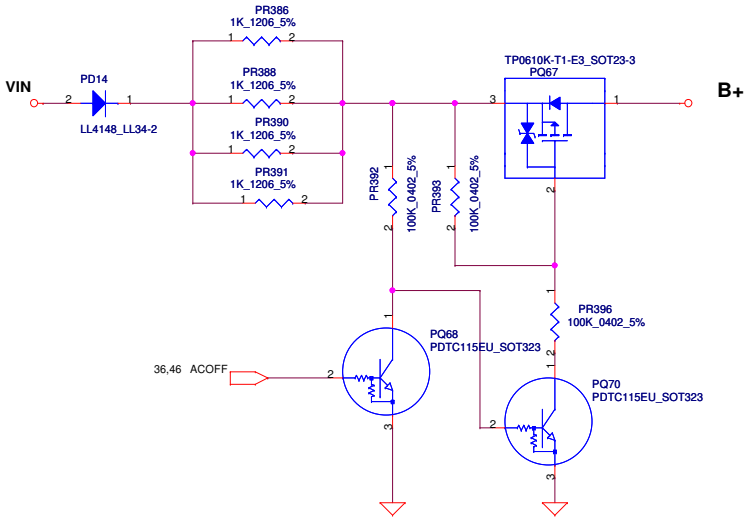
Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NEW71 | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 46 of 56





ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: **PRECHARGE**

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Date: Tuesday, December 22, 2009 | Sheet 47 of 56

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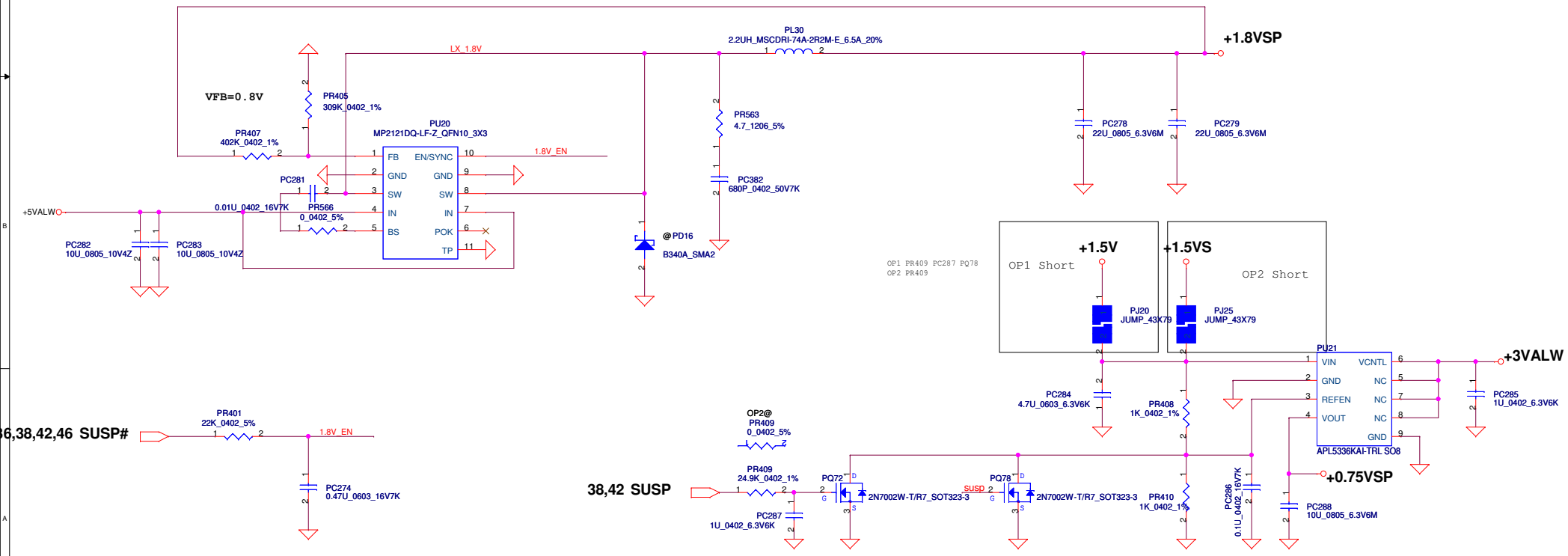

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

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Title: **+1.8VSP/+0.75VSP**

Size	Document Number	Rev
Custom	NEW71	0.1

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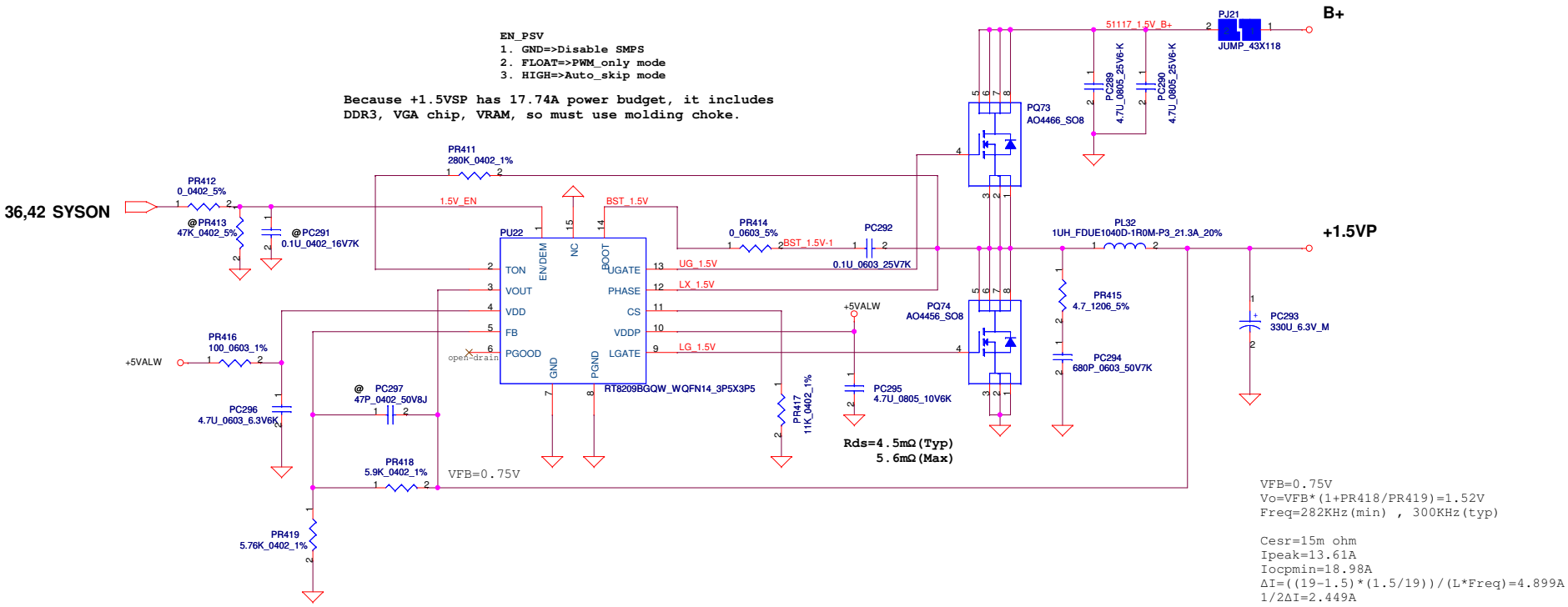

VFB=0.75V
Vo=VFB*(1+PR418/PR419)=1.52V
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=13.61A
Iocpmin=18.98A
ΔI=((19-1.5)*(1.5/19))/(L*Freq)=4.899A
1/2ΔI=2.449A

Iocp=18.09A~29.13A

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: **1.5VP**

Size: Custom | Document Number: *NEW71* | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 49 of 56

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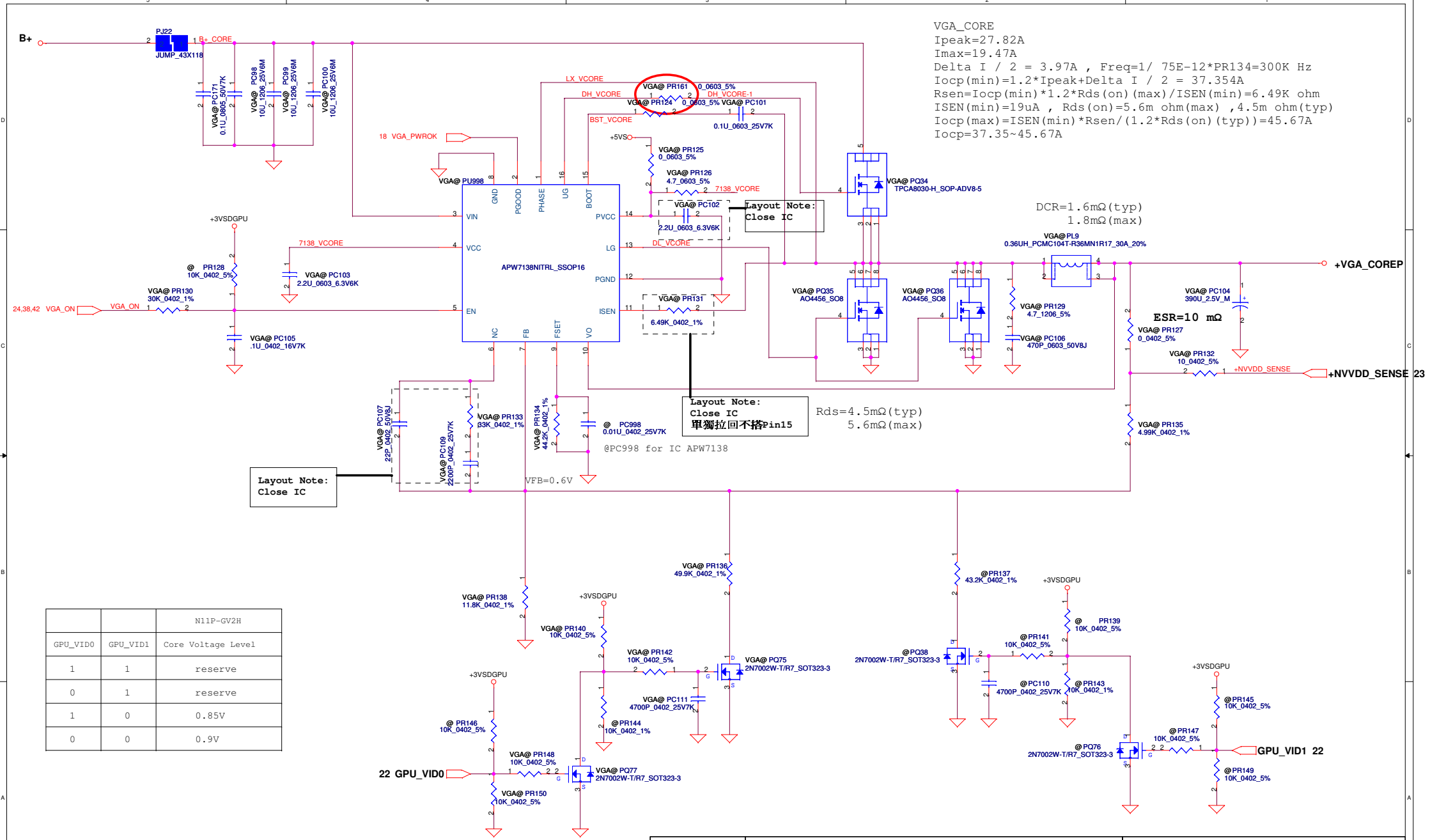

VGA_CORE
Ipeak=27.82A
Imax=19.47A
Delta I / 2 = 3.97A , Freq=1/ 75E-12*PR134=300K Hz
Iocp(min)=1.2*Ipeak+Delta I / 2 = 37.354A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=6.49K ohm
ISEN(min)=19uA , Rds(on)=5.6m ohm(max) ,4.5m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=45.67A
Iocp=37.35~45.67A

DCR=1.6mΩ(typ)
1.8mΩ(max)

		N11P-GV2H
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	reserve
0	1	reserve
1	0	0.85V
0	0	0.9V

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

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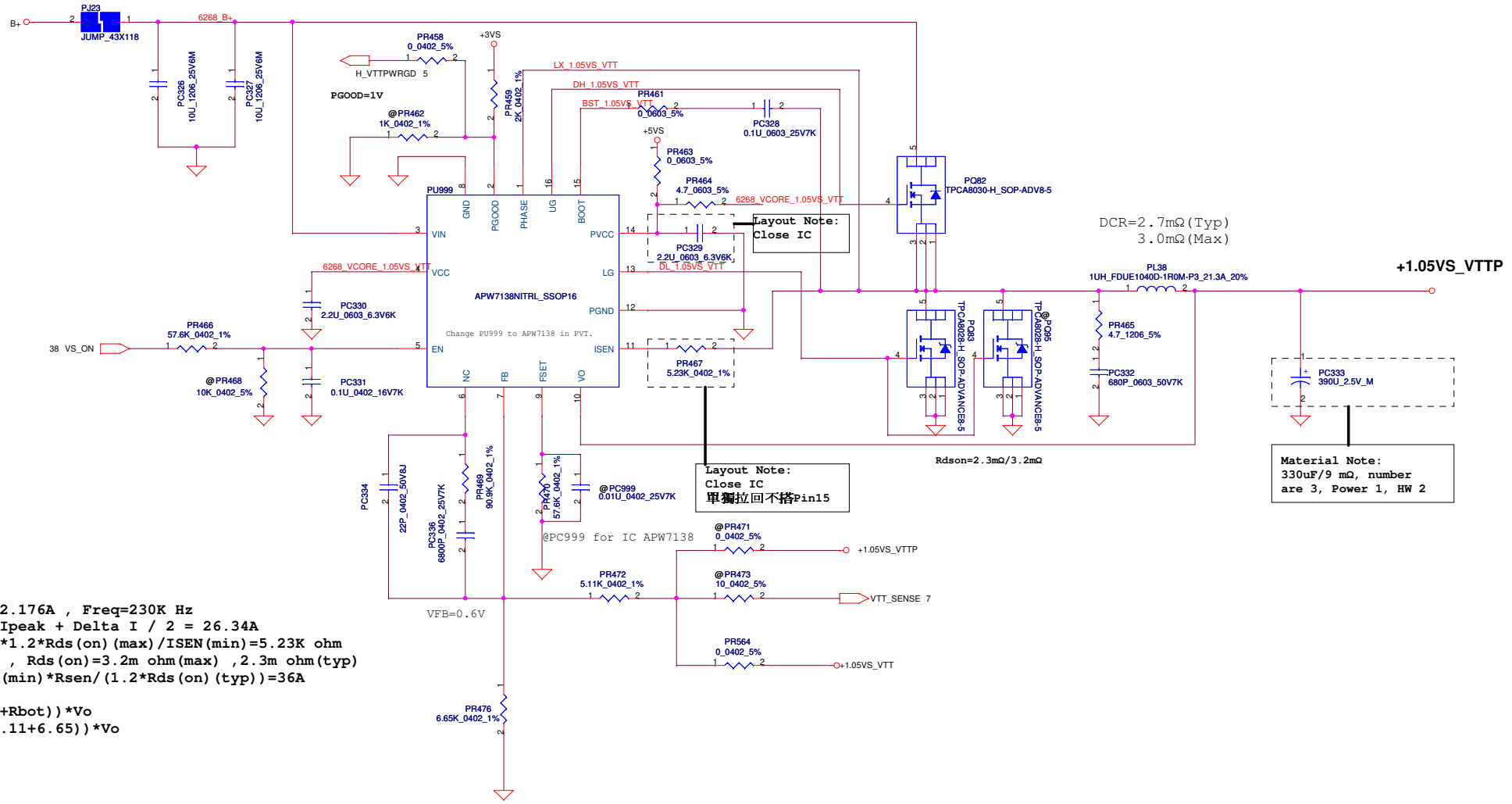
Compal Electronics, Inc.

Title: VGA_COREP

Size: Custom | Document Number: NEW71 | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 50 of 56




```
+1.05VS_VTT
Ipeak=20.14A
Imax=14.10A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=1.2*Ipeak + Delta I / 2 = 26.34A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=5.23K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=36A
Iocp=26.34~36A
Vref=(Rb/(Rtop+Rbot))*Vo
=>0.6=(6.65/(5.11+6.65))*Vo
Vo=1.061V
```

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: +1.05VS_VTTP

Size: Custom | Document Number: NEW71 | Rev: 0.1

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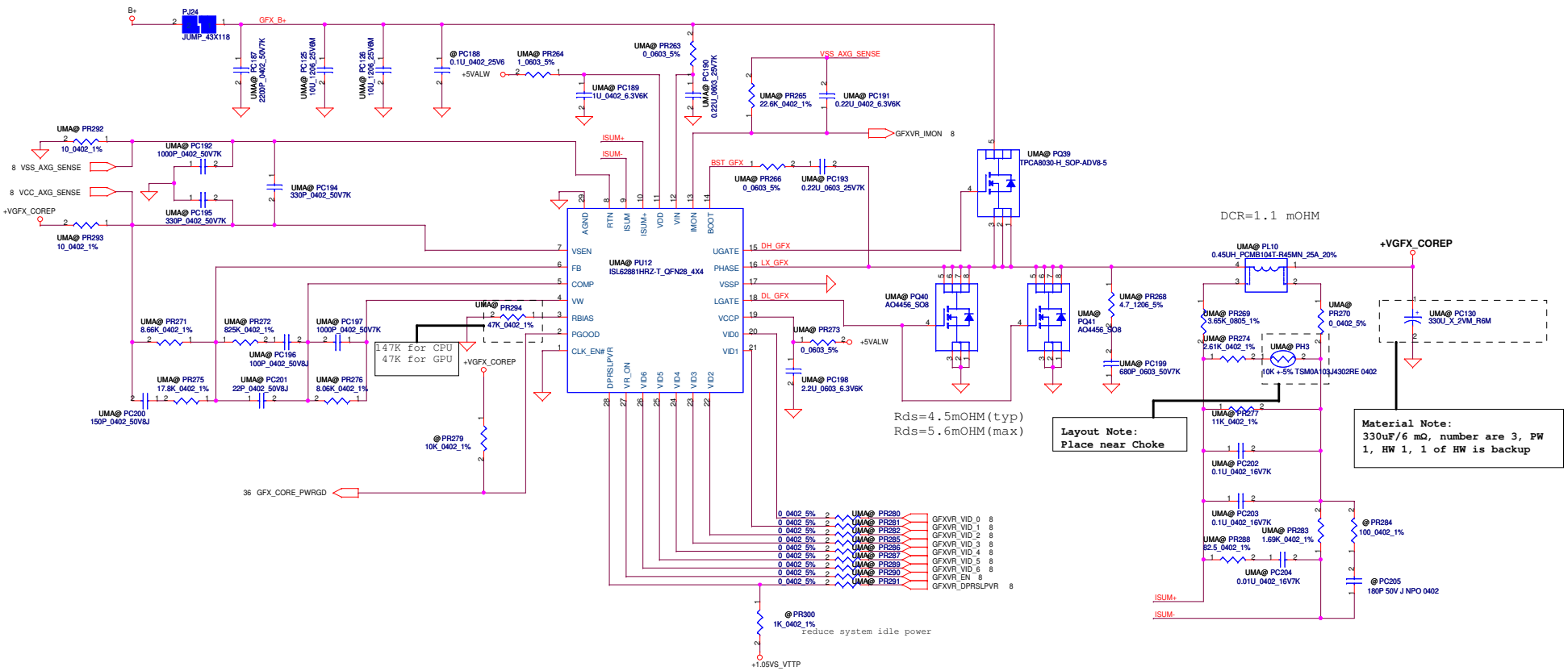
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/4/15	Deciphered Date	2010/08/01	Title: GFX_COREP
				Size: C; Document Number: NEW71; Rev: 0.1
				Date: Tuesday, December 22, 2009; Sheet 52 of 56

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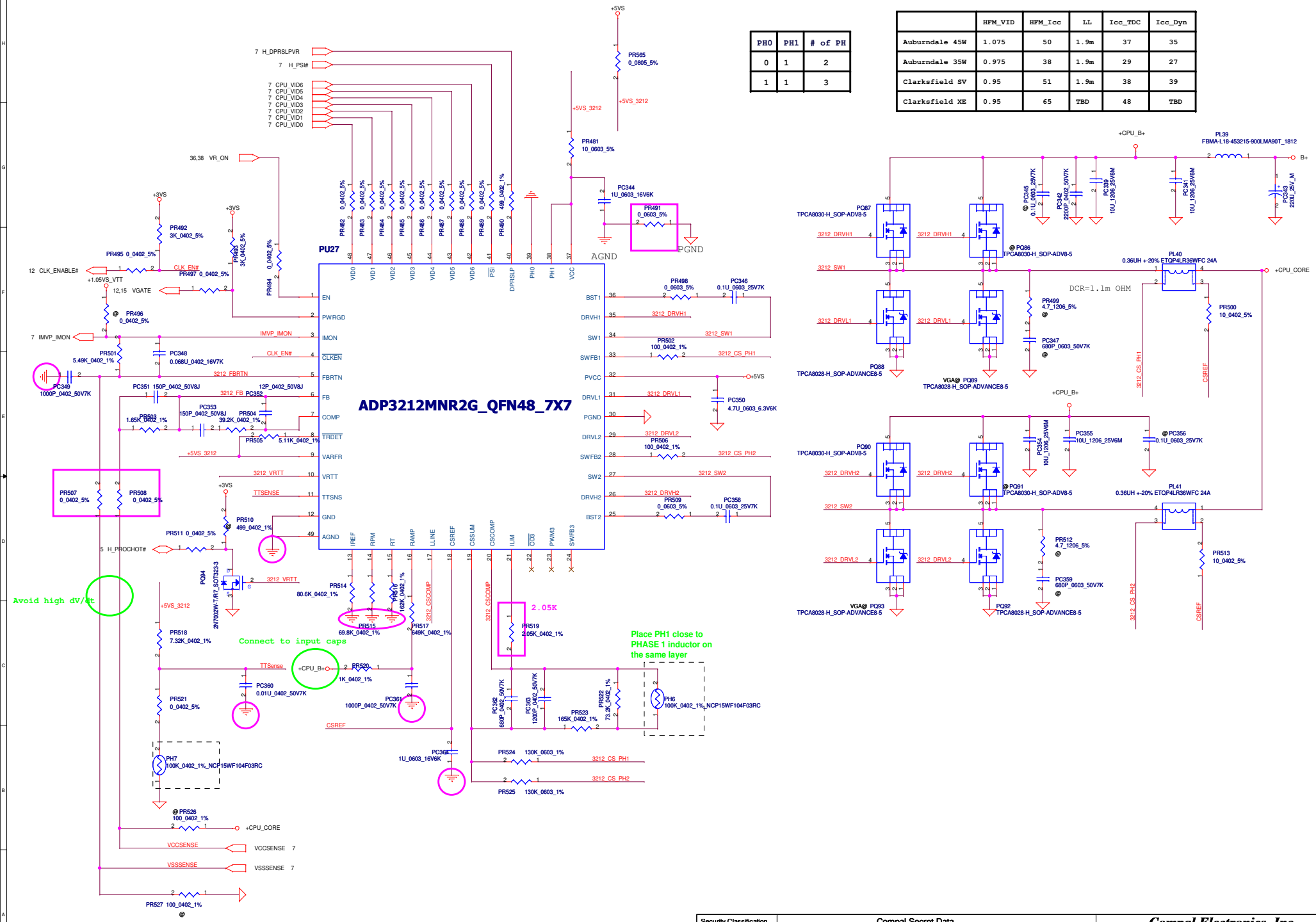
PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: **CPU_CORE**

Size: C | Document Number: **NEW71/91 M/B LA-5893P Schematic** | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 53 of 56

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00(DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU commond design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail commond design.	For VTT Power rail commond design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12 13	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
14	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004O80(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280. Delete PC273 SE075103K80 PC275 SE000000I10	2009-1029	to DVT
17	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC272 SE107475K80, PC271 SE107105M80 Delete PR401 and PR403 SD028220280, PC274 SE026474K80	2009-1029	to DVT
18	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Change PR196 from SD034442280 to SD034365280. Change PL14 from SL200000V00 to SH000005680	2009-1029	to DVT
19	+VGA_COREP, OVP issue.	Because if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
20	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N SO8)	2009-1029	to DVT
21	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7686DP-T1-E3 1N POWERPAK SO8)	2009-1029	to DVT
22	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323)	2009-1029	to DVT
23	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

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