

14" & 15.6" ULV + GS45 Block Diagram

<http://hobi-elektronika.net>

Rev: X01



POWER			
1.5VSUS & 0.75VTT (RT8207A)	PG 32	CHARGER (MAX8731A))	PG 29
CPU CORE(ADP3211A)	PG 31	1.05_VCCP(OZ8116)	PG 30
RUN POWER SW	PG 33	Power Button	PG 27
AC/BATT CONNECTOR	PG 34		

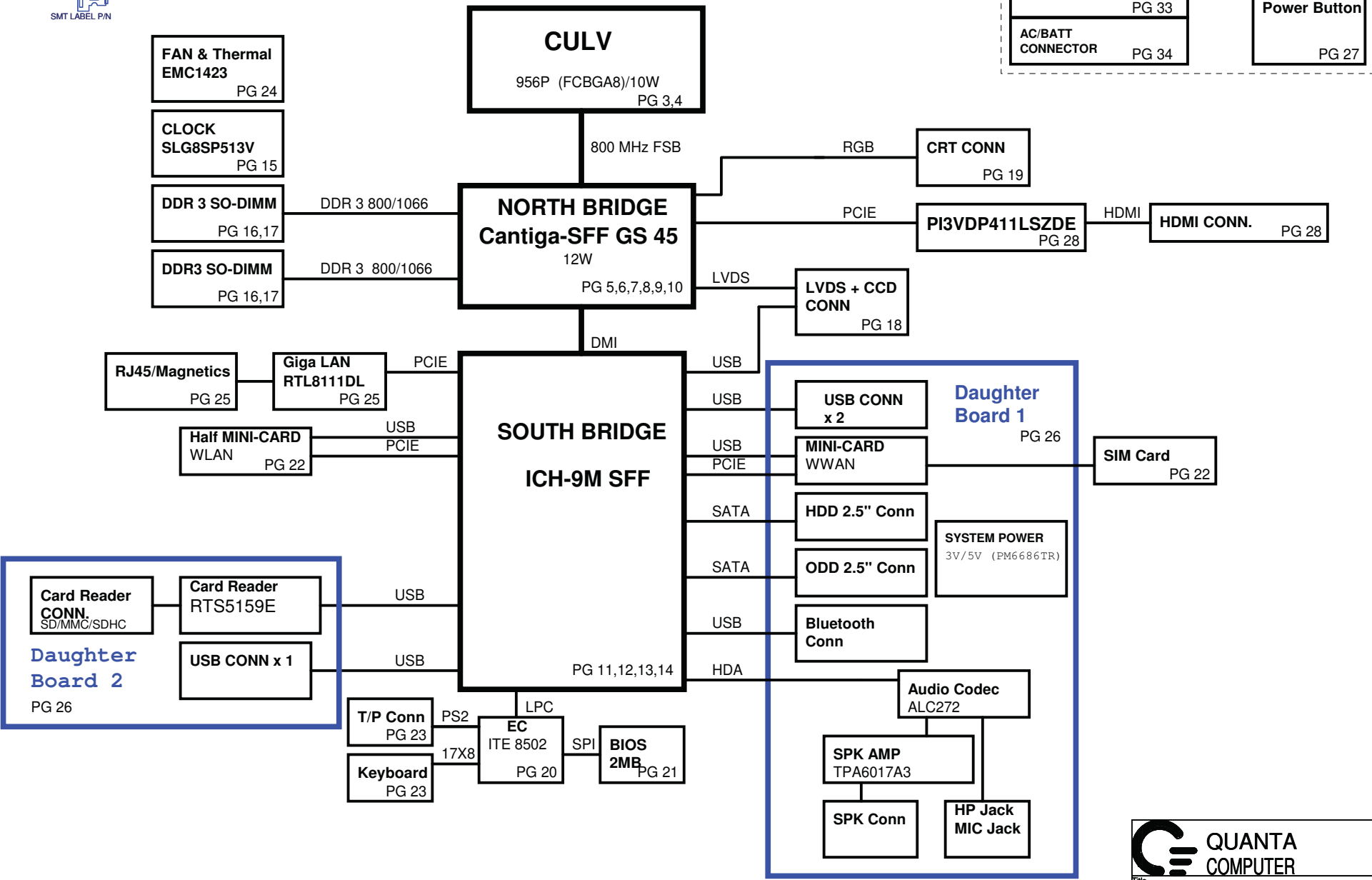
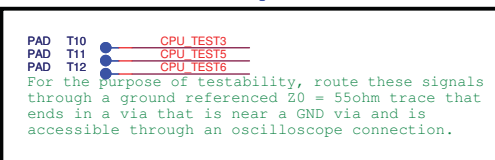


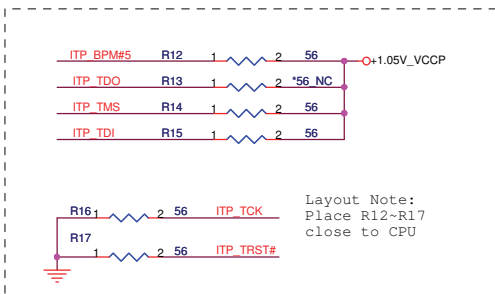
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18	LCD/CCD
19	CRT
20	SIO(ITE8502)
21	FLASH/RTC
22	WLAN/SIM CONN.
23	TP/KB
24	FAN/THERMAL
25	LAN RTL8111+RJ45
26	IO BOARD CONN.
27	POWER SWITCH
28	HDMI
29	CHARGE MAX8731A
30	1.05VCCP
31	CPU_ADP3211A
32	1.5VSUS & 0.75VTT
33	Run Power Switch
34	DCin & Batt
35	SMBUS BLOCK
36	PAD&SCREW&SPRING

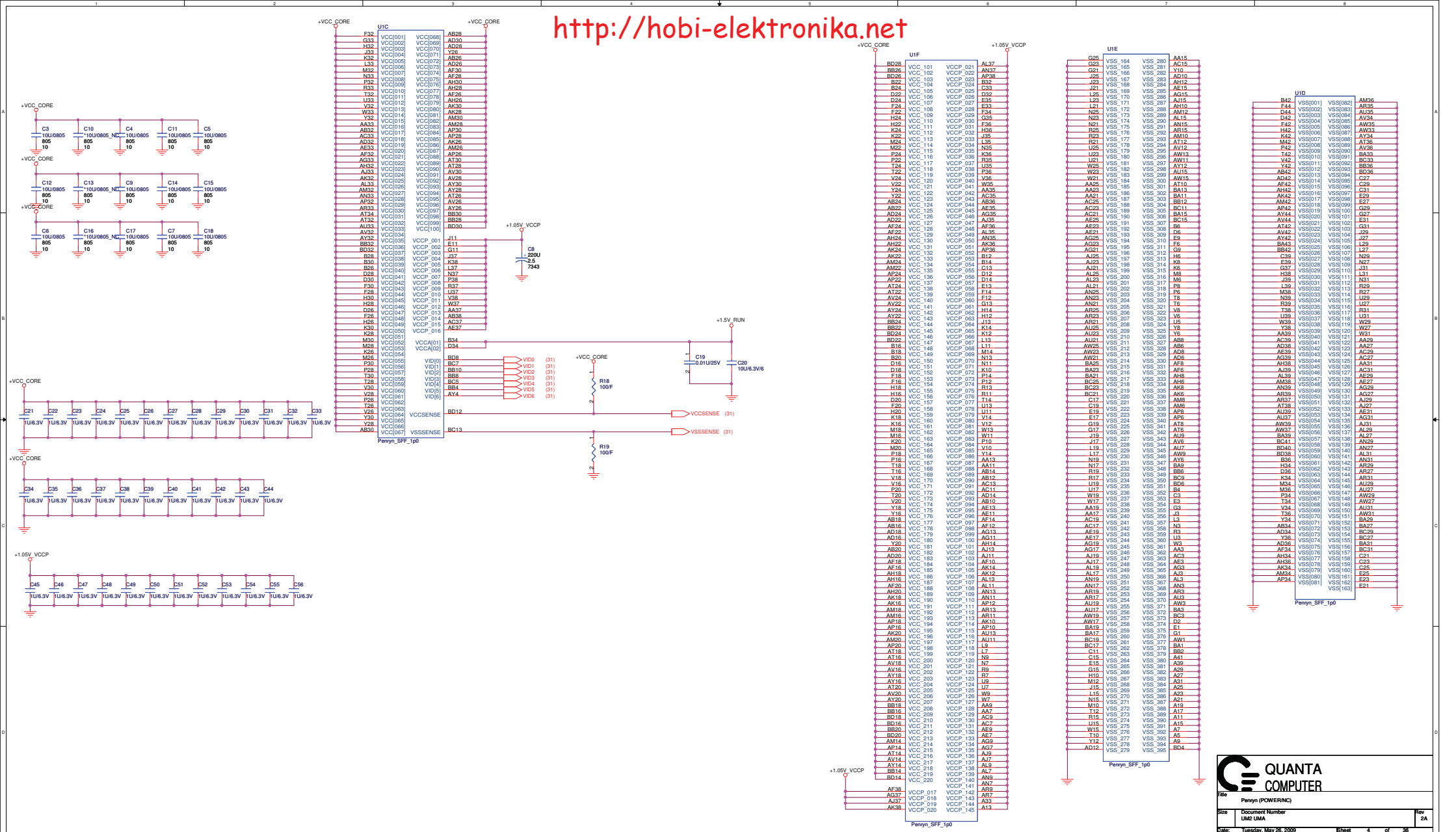
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38,52,53	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
⏏ 8731AGND	46	
⏏ AGND_0.9V	49	
⏏ AGND_DC/DC	52	
⏏ AGND_DC2	48	
⏏ AGND_DDR	49	
⏏ AGND_ISL6260	51	
⏏ GND	ALL	

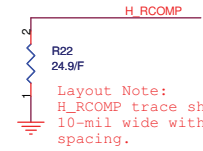
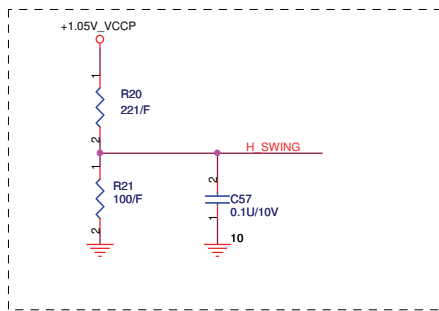


AJSLSB5VVT01 CPU (956P) SU9400 1.4G SLB5V(BGA)WIN B/S
AJSLGFMTT03 CPU (956P) SU3500 1.4G SLGFM(BGA)WIN BSQ
AJSLGS8VT03 CPU (956P) SU2700 1.3G SLGS8(BGA)WIN BSQ

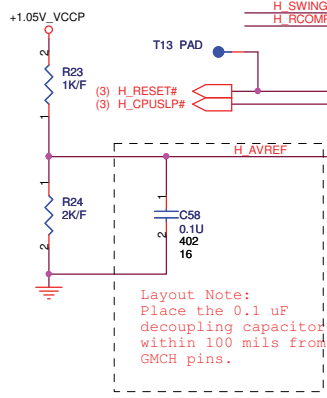




(3) H_D#[0..63] H_D#[0..63]



Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.



Layout Note:
Place the 0.1 uF
decoupling capacitor
within 100 mils from
GMCH pins.

H_D#0	J7	H_D# 0
H_D#1	H6	H_D# 1
H_D#2	L11	H_D# 2
H_D#3	J3	H_D# 3
H_D#4	H4	H_D# 4
H_D#5	G3	H_D# 5
H_D#6	K10	H_D# 6
H_D#7	K12	H_D# 7
H_D#8	L1	H_D# 8
H_D#9	M10	H_D# 9
H_D#10	M6	H_D# 10
H_D#11	N11	H_D# 11
H_D#12	L7	H_D# 12
H_D#13	K6	H_D# 13
H_D#14	M4	H_D# 14
H_D#15	K4	H_D# 15
H_D#16	P6	H_D# 16
H_D#17	W9	H_D# 17
H_D#18	V6	H_D# 18
H_D#19	V2	H_D# 19
H_D#20	P10	H_D# 20
H_D#21	W7	H_D# 21
H_D#22	N9	H_D# 22
H_D#23	P4	H_D# 23
H_D#24	U9	H_D# 24
H_D#25	V4	H_D# 25
H_D#26	U1	H_D# 26
H_D#27	W3	H_D# 27
H_D#28	V10	H_D# 28
H_D#29	U7	H_D# 29
H_D#30	W11	H_D# 30
H_D#31	U11	H_D# 31
H_D#32	U11	H_D# 32
H_D#33	AC9	H_D# 33
H_D#34	Y4	H_D# 34
H_D#35	Y10	H_D# 35
H_D#36	AB6	H_D# 36
H_D#37	AA9	H_D# 37
H_D#38	AB10	H_D# 38
H_D#39	AA1	H_D# 39
H_D#40	AC3	H_D# 40
H_D#41	AC7	H_D# 41
H_D#42	AD12	H_D# 42
H_D#43	AB4	H_D# 43
H_D#44	Y6	H_D# 44
H_D#45	AD10	H_D# 45
H_D#46	AA11	H_D# 46
H_D#47	AB2	H_D# 47
H_D#48	AD4	H_D# 48
H_D#49	AE7	H_D# 49
H_D#50	AD2	H_D# 50
H_D#51	AD6	H_D# 51
H_D#52	AE3	H_D# 52
H_D#53	AG9	H_D# 53
H_D#54	AG7	H_D# 54
H_D#55	AE11	H_D# 55
H_D#56	AK6	H_D# 56
H_D#57	AF6	H_D# 57
H_D#58	AJ9	H_D# 58
H_D#59	AH6	H_D# 59
H_D#60	AF12	H_D# 60
H_D#61	AH4	H_D# 61
H_D#62	AJ7	H_D# 62
H_D#63	AE9	H_D# 63

HOST

H_A# 3	L15	H_A#3
H_A# 4	B14	H_A#4
H_A# 5	C15	H_A#5
H_A# 6	D12	H_A#6
H_A# 7	F14	H_A#7
H_A# 8	G17	H_A#8
H_A# 9	B12	H_A#9
H_A# 10	J15	H_A#10
H_A# 11	D16	H_A#11
H_A# 12	C17	H_A#12
H_A# 13	D14	H_A#13
H_A# 14	K16	H_A#14
H_A# 15	F16	H_A#15
H_A# 16	B16	H_A#16
H_A# 17	C21	H_A#17
H_A# 18	D18	H_A#18
H_A# 19	J19	H_A#19
H_A# 20	J21	H_A#20
H_A# 21	B18	H_A#21
H_A# 22	D22	H_A#22
H_A# 23	G19	H_A#23
H_A# 24	J17	H_A#24
H_A# 25	L21	H_A#25
H_A# 26	L19	H_A#26
H_A# 27	G21	H_A#27
H_A# 28	D20	H_A#28
H_A# 29	K22	H_A#29
H_A# 30	F18	H_A#30
H_A# 31	K20	H_A#31
H_A# 32	F20	H_A#32
H_A# 33	F22	H_A#33
H_A# 34	B20	H_A#34
H_A# 35	A19	H_A#35

H_ADS#	F10	H_ADS# (3)
H_ADSTB# 0	A15	H_ADSTB#0 (3)
H_ADSTB# 1	C19	H_ADSTB#1 (3)
H_BNR#	C9	H_BNR# (3)
H_BPRI#	B8	H_BPRI# (3)
H_BREQ#	C11	H_BREQ# (3)
H_DEFER#	E5	H_DEFER# (3)
H_DBSY#	D6	H_DBSY# (3)
HPLL_CLK	AH10	CLK_MCH_BCLK# (15)
HPLL_CLK#	AJ11	CLK_MCH_BCLK# (15)
H_DPWR#	G11	H_DPWR# (3)
H_DRDY#	H2	H_DRDY# (3)
H_HIT#	C7	H_HIT# (3)
H_HITM#	F8	H_HITM# (3)
H_LOCK#	A11	H_LOCK# (3)
H_TRDY#	D8	H_TRDY# (3)

H_DINV# 0	L9	H_DINV#0 (3)
H_DINV# 1	N7	H_DINV#1 (3)
H_DINV# 2	AA7	H_DINV#2 (3)
H_DINV# 3	AG3	H_DINV#3 (3)

H_DSTBN# 0	K2	H_DSTBN#0 (3)
H_DSTBN# 1	N3	H_DSTBN#1 (3)
H_DSTBN# 2	AA3	H_DSTBN#2 (3)
H_DSTBN# 3	AF4	H_DSTBN#3 (3)

H_DSTBP# 0	L3	H_DSTBP#0 (3)
H_DSTBP# 1	M2	H_DSTBP#1 (3)
H_DSTBP# 2	Y2	H_DSTBP#2 (3)
H_DSTBP# 3	AF2	H_DSTBP#3 (3)

H_REQ# 0	J13	H_REQ#0 (3)
H_REQ# 1	L13	H_REQ#1 (3)
H_REQ# 2	C13	H_REQ#2 (3)
H_REQ# 3	G13	H_REQ#3 (3)
H_REQ# 4	G15	H_REQ#4 (3)

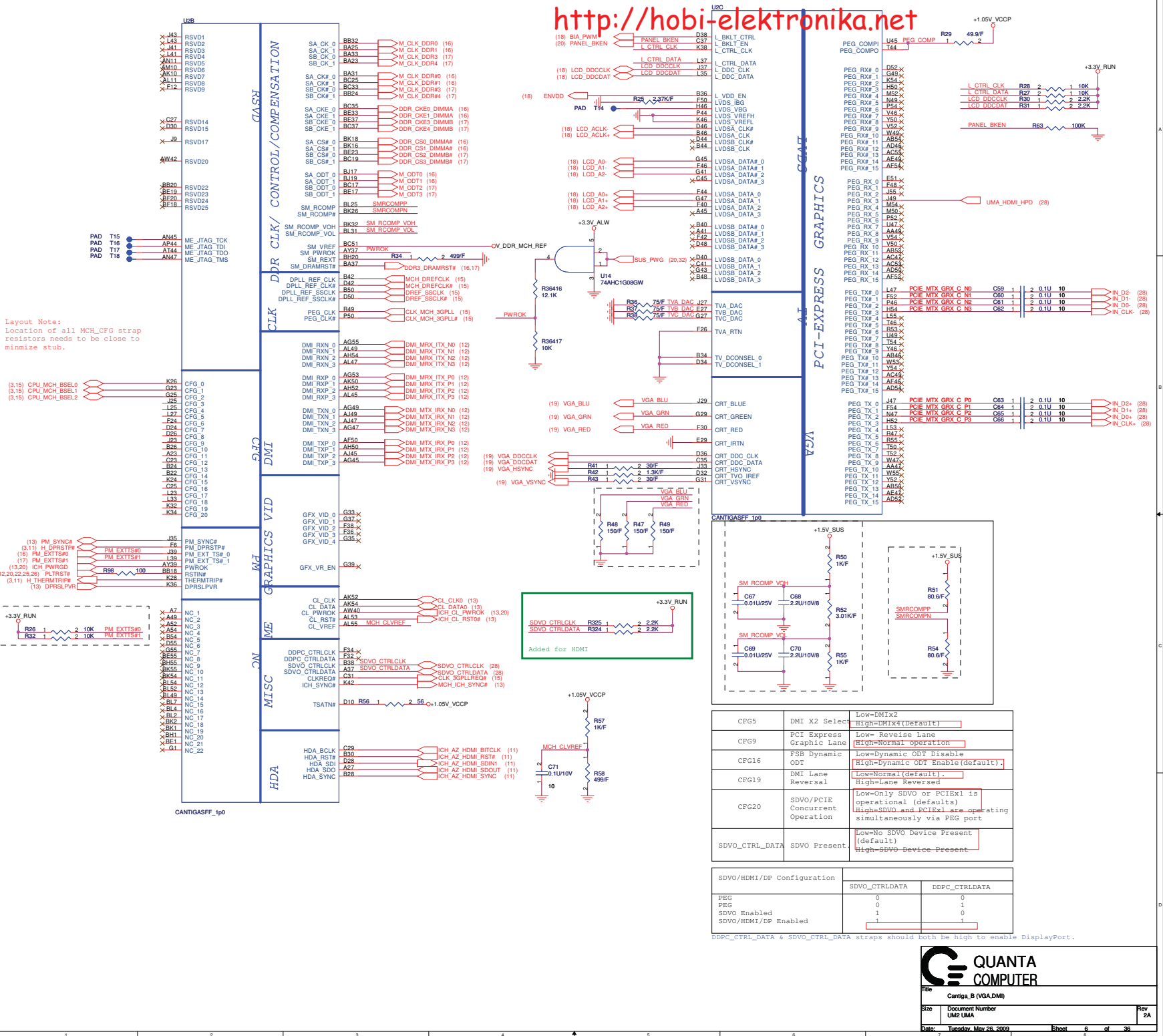
H_RS# 0	F4	H_RS#0 (3)
H_RS# 1	F2	H_RS#1 (3)
H_RS# 2	G7	H_RS#2 (3)

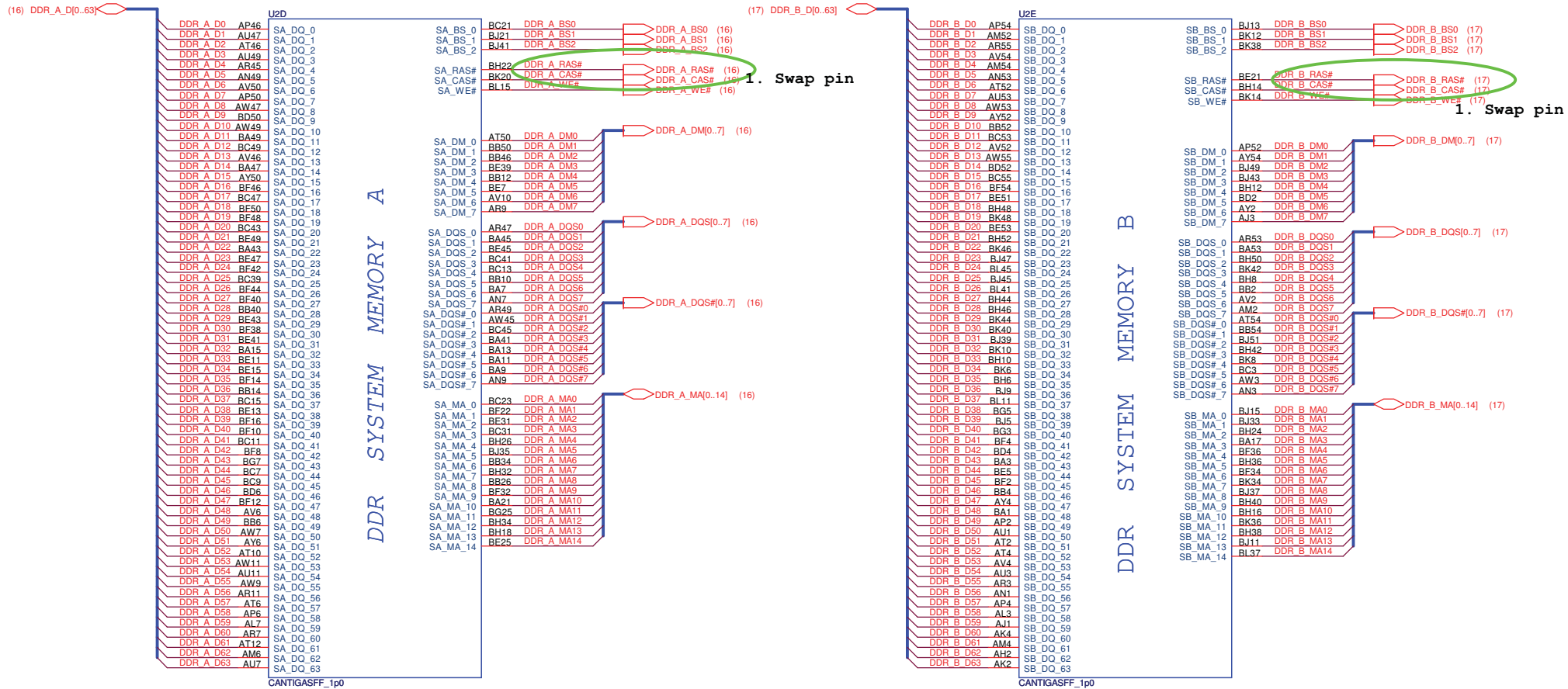
H_SWING
H_RCOMP

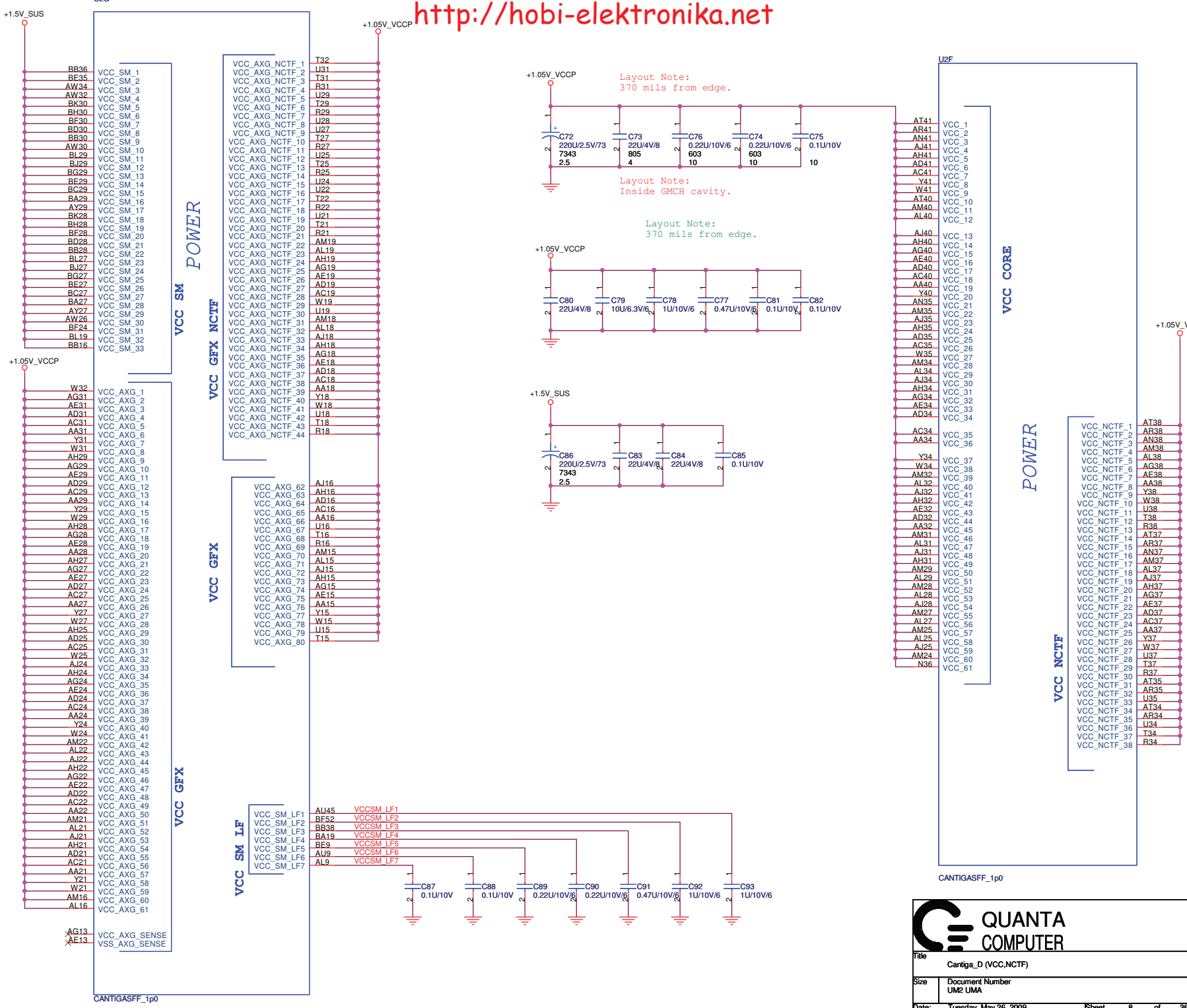
H_CPURST#
H_CPUSLP#

H_AVREF
H_DVREF

CANTIGASFF_1p0







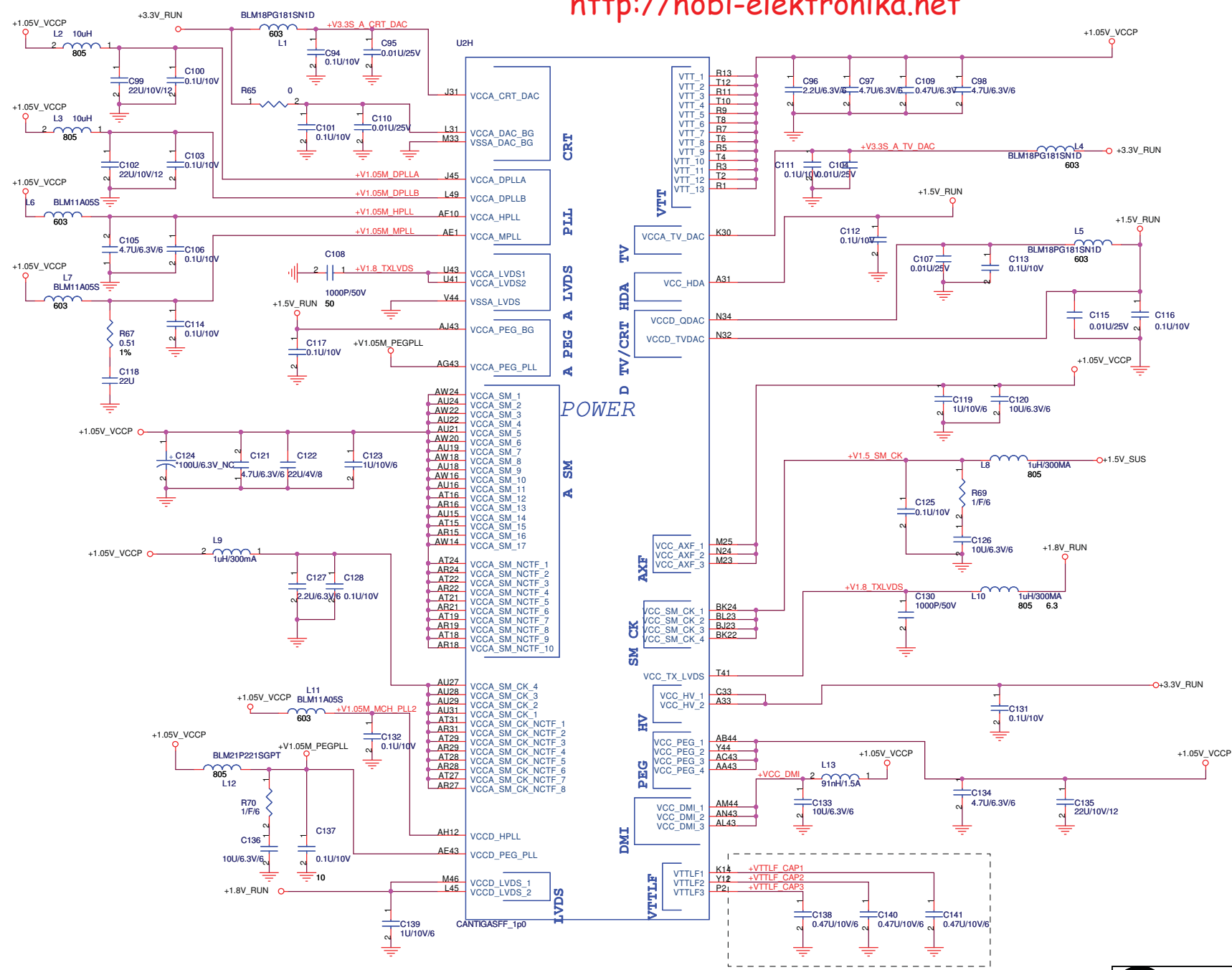


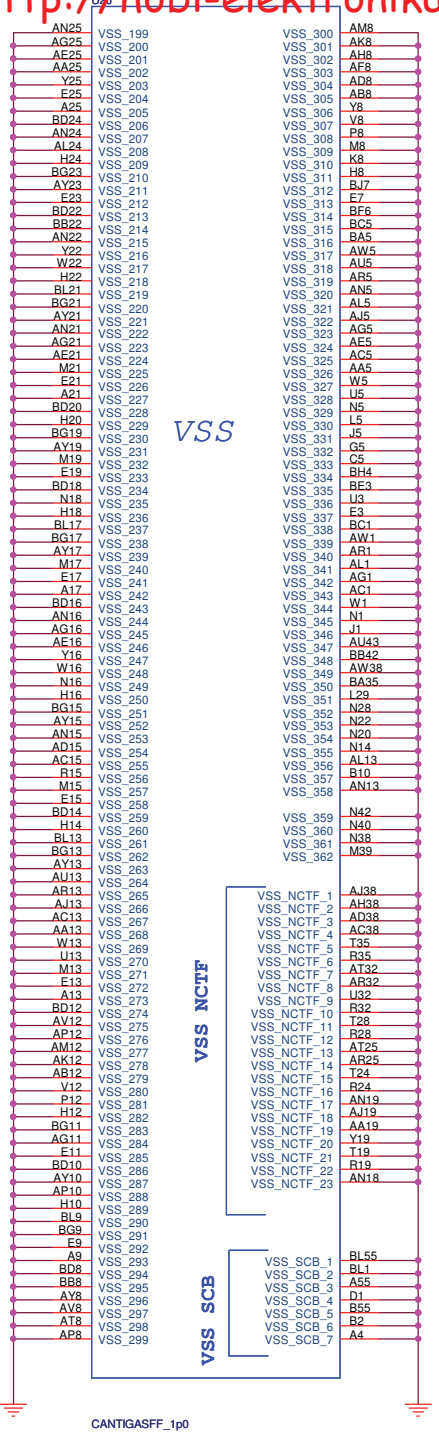
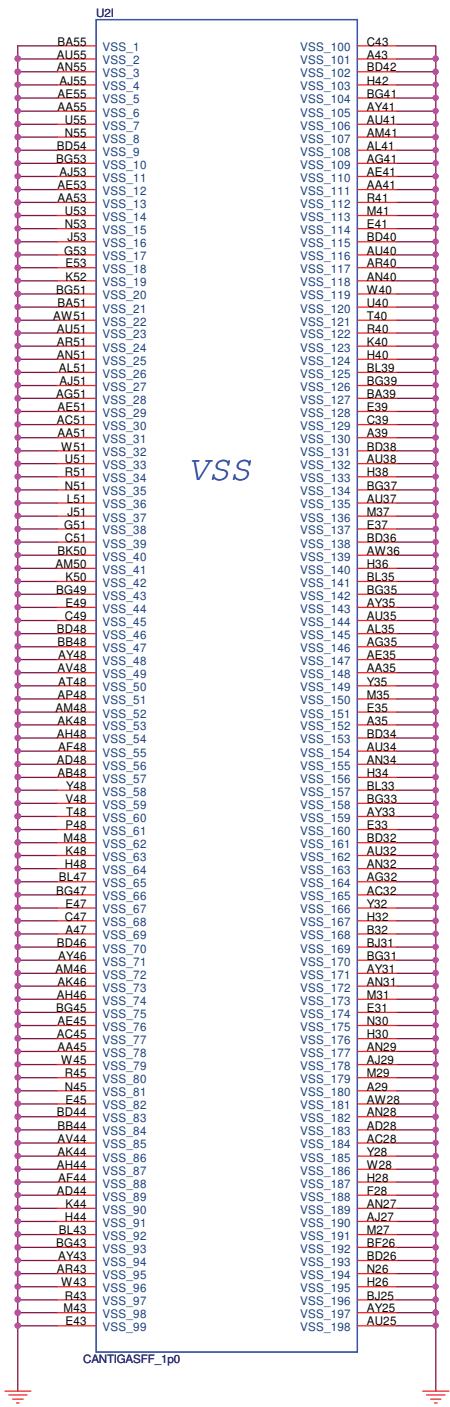
QUANTA
COMPUTER

TitleCantiga_D (VCC,NCTF)

SizeDocument NumberUM2 UMARev2A

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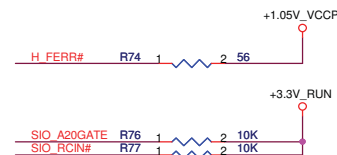
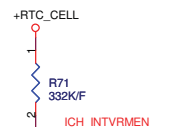
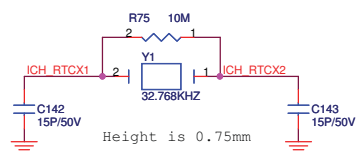
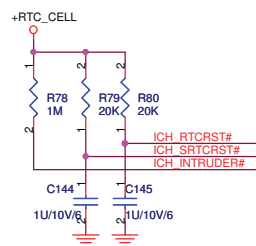




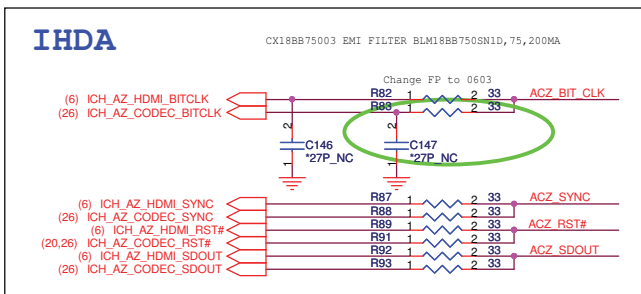
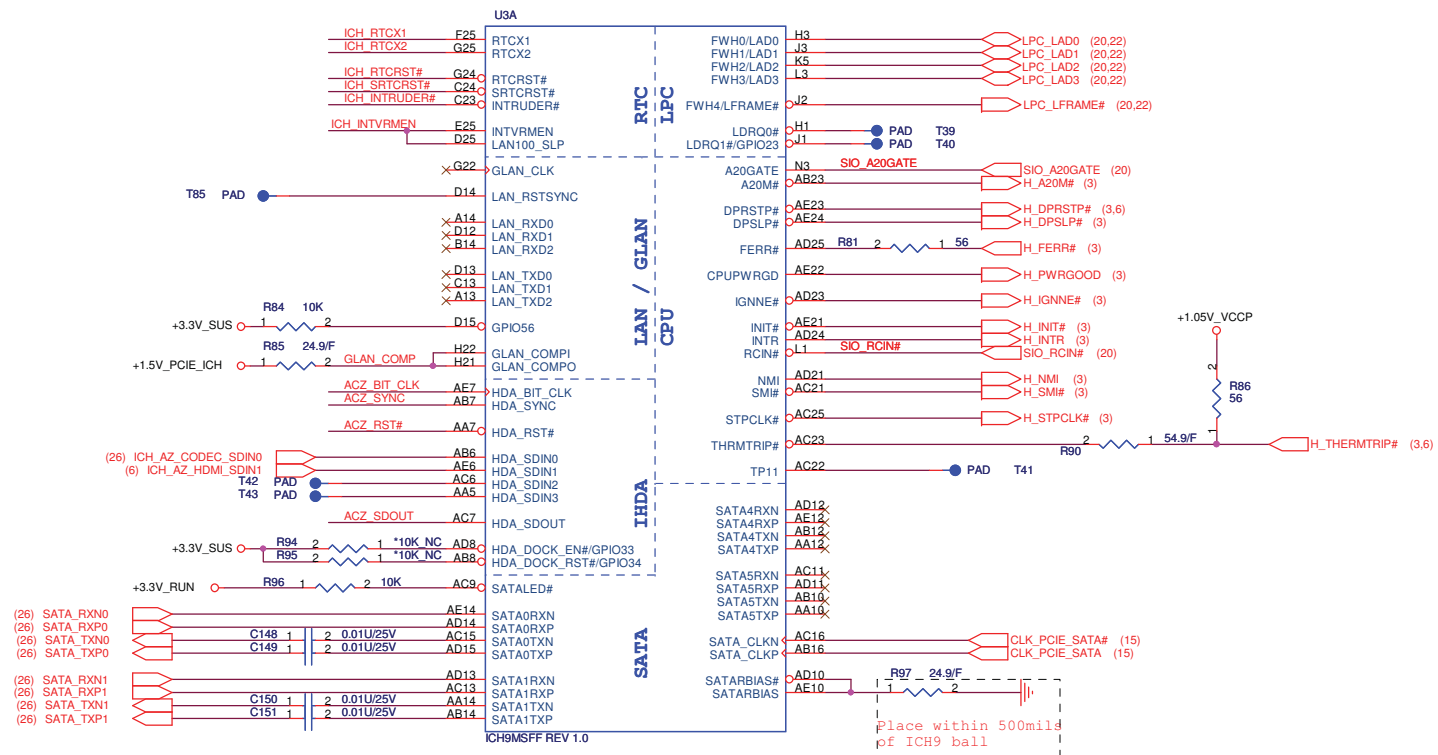


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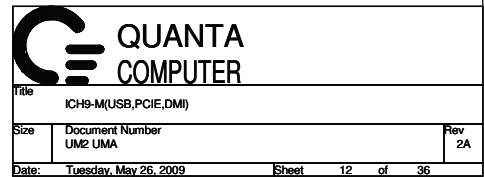
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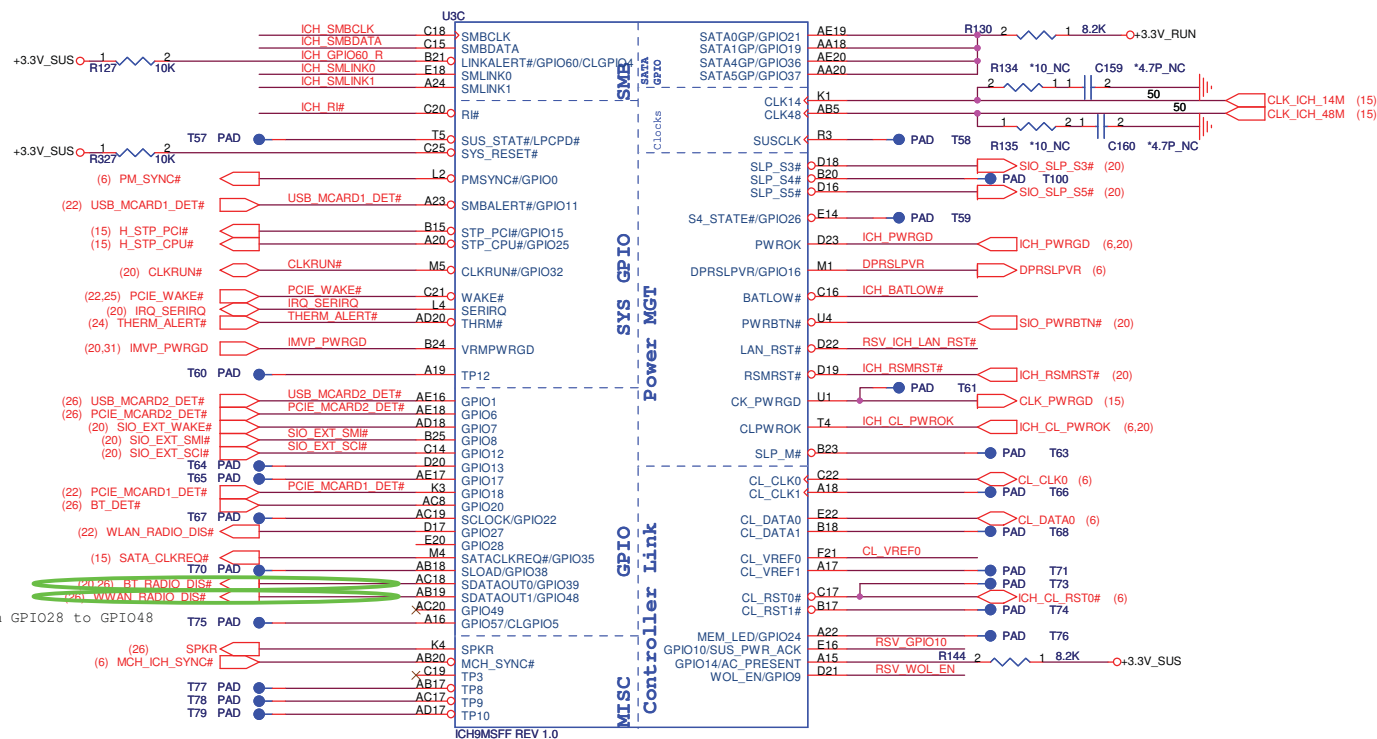
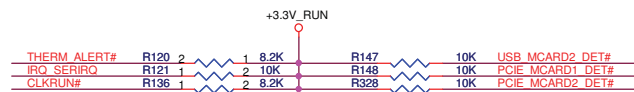


(Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)



ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)





13. change WWAN_RADIO_DIS# from GPIO28 to GPIO48

Address D2

for
issue.

ICH_SMBDATA

ICH_SMBCLK

MEM_SDATA (16,17,22,26)

MEM_SCLK (16,17,22,26)

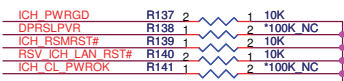
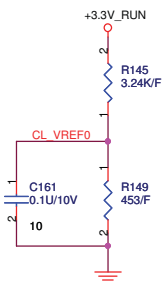
+3.3V_RUN

+3.3V_RUN

Q2
2N7002W-7-F

Q3
2N7002W-7-F

RP6
2.2KΩ2



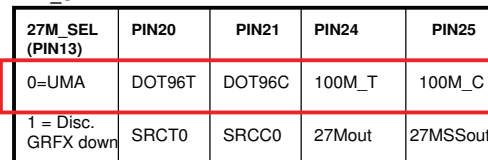
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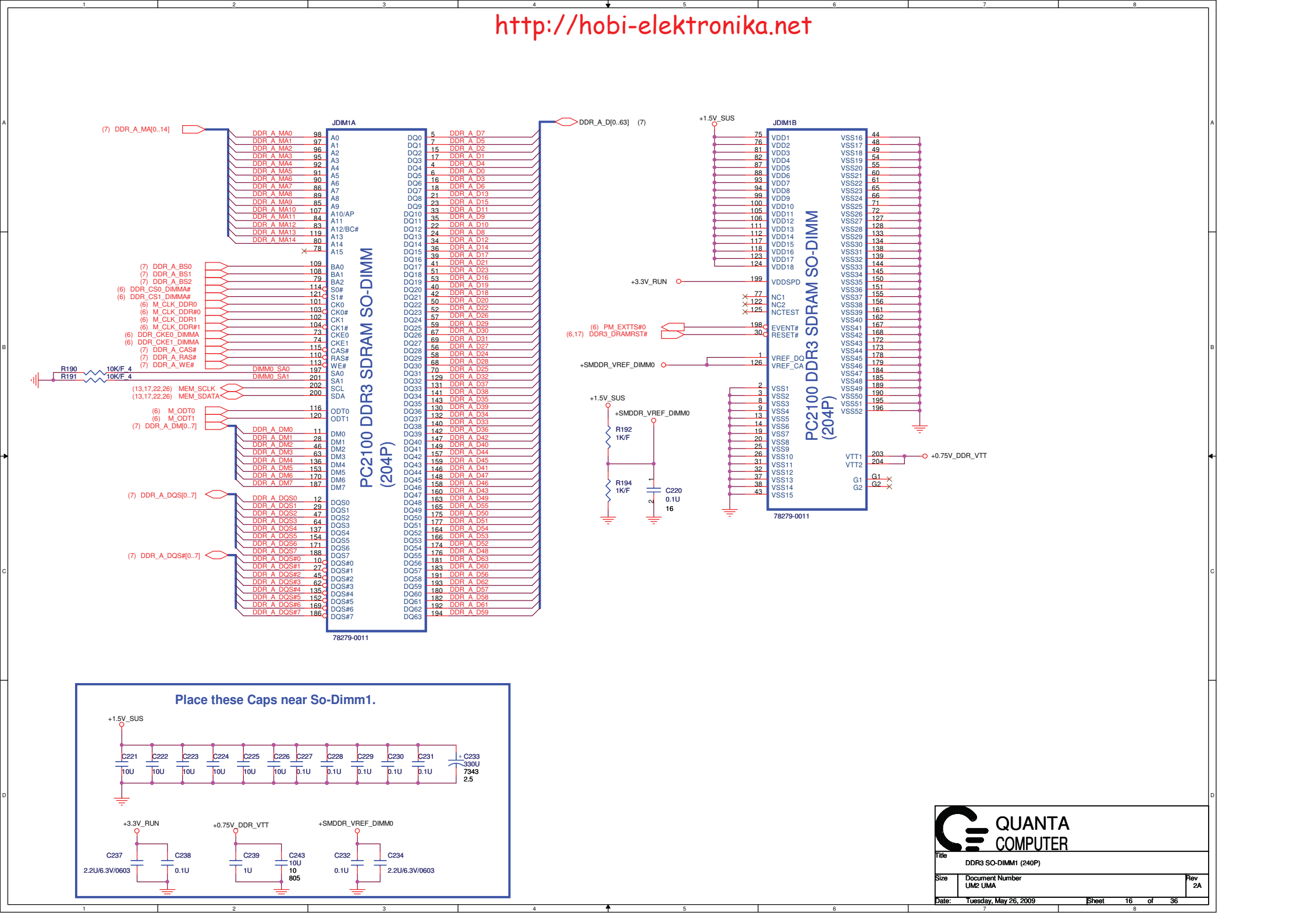
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78279-0011

PC2100 DDR3 SDRAM SO-DIMM (240P)

PC2100 DDR3 SDRAM SO-DIMM (240P)

78279-0011

Place these Caps near So-Dimm1.

+1.5V_SUS

+3.3V_RUN

+0.75V_DDR_VTT

+SMDR_VREF_DIMM0

C221 10U

C222 10U

C223 10U

C224 10U

C225 10U

C226 0.1U

C227 0.1U

C228 0.1U

C229 0.1U

C230 0.1U

C231 0.1U

C233 330U

C237 2.2U/6.3V/0603

C238 0.1U

C239 1U

C243 10U

C242 10U

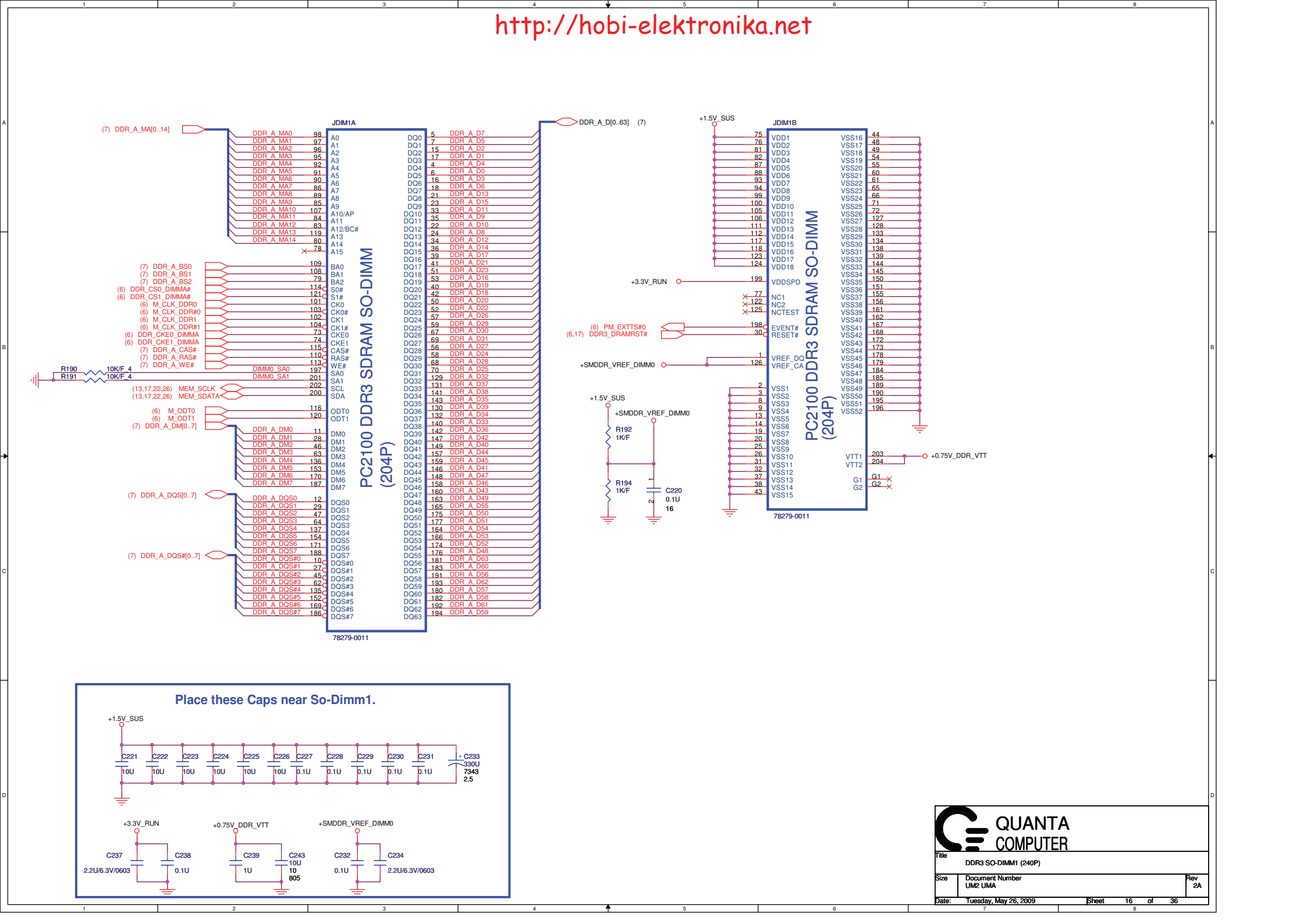
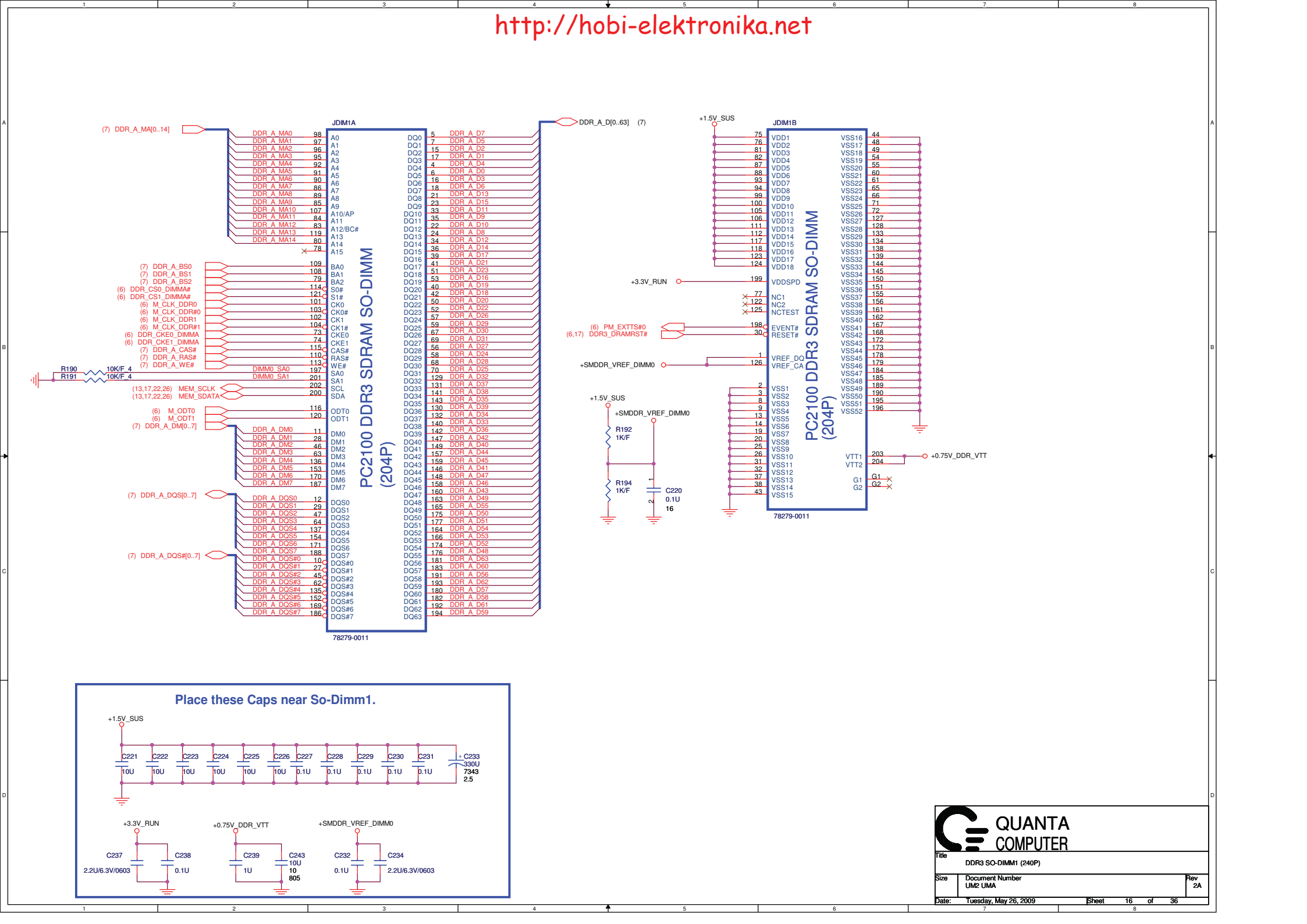
C234 2.2U/6.3V/0603

QUANTA COMPUTER

Title: DDR3 SO-DIMM1 (240P)

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PC2100 DDR3 SDRAM SO-DIMM (240P)

Place these Caps near So-Dimm1.

Capacitor Placement Details:

- +1.5V_SUS:** C221 (10U), C222 (10U), C223 (10U), C224 (10U), C225 (10U), C226 (0.1U), C227 (0.1U), C228 (0.1U), C229 (0.1U), C230 (0.1U), C231 (0.1U), C233 (330U), C234 (7343 2.5).
- +3.3V_RUN:** C237 (2.2U/6.3V/0603), C238 (0.1U).
- +0.75V_DDR_VTT:** C239 (1U), C243 (10U 805).
- +SMDDR_VREF_DIMM0:** C232 (0.1U), C234 (2.2U/6.3V/0603).

QUANTA COMPUTER

Title: DDR3 SO-DIMM1 (240P)

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Place these Caps near So-Dimm1.

+1.5V_SUS

C221 10U, C222 10U, C223 10U, C224 10U, C225 10U, C226 0.1U, C227 0.1U, C228 0.1U, C229 0.1U, C230 0.1U, C231 0.1U, C233 330U, 7343 2.5

+3.3V_RUN

C237 2.2U/6.3V/0603, C238 0.1U

+0.75V_DDR_VTT

C239 1U, C243 10U, 805

+SMDDR_VREF_DIMM0

C232 0.1U, C234 2.2U/6.3V/0603

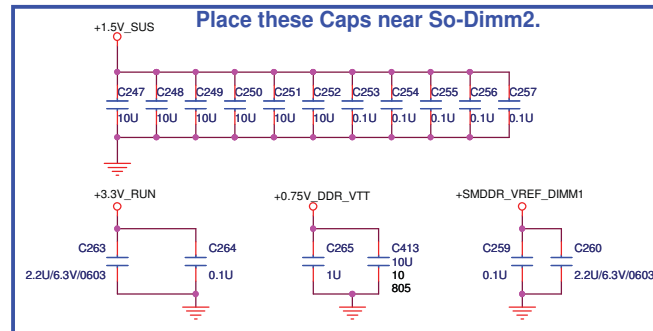
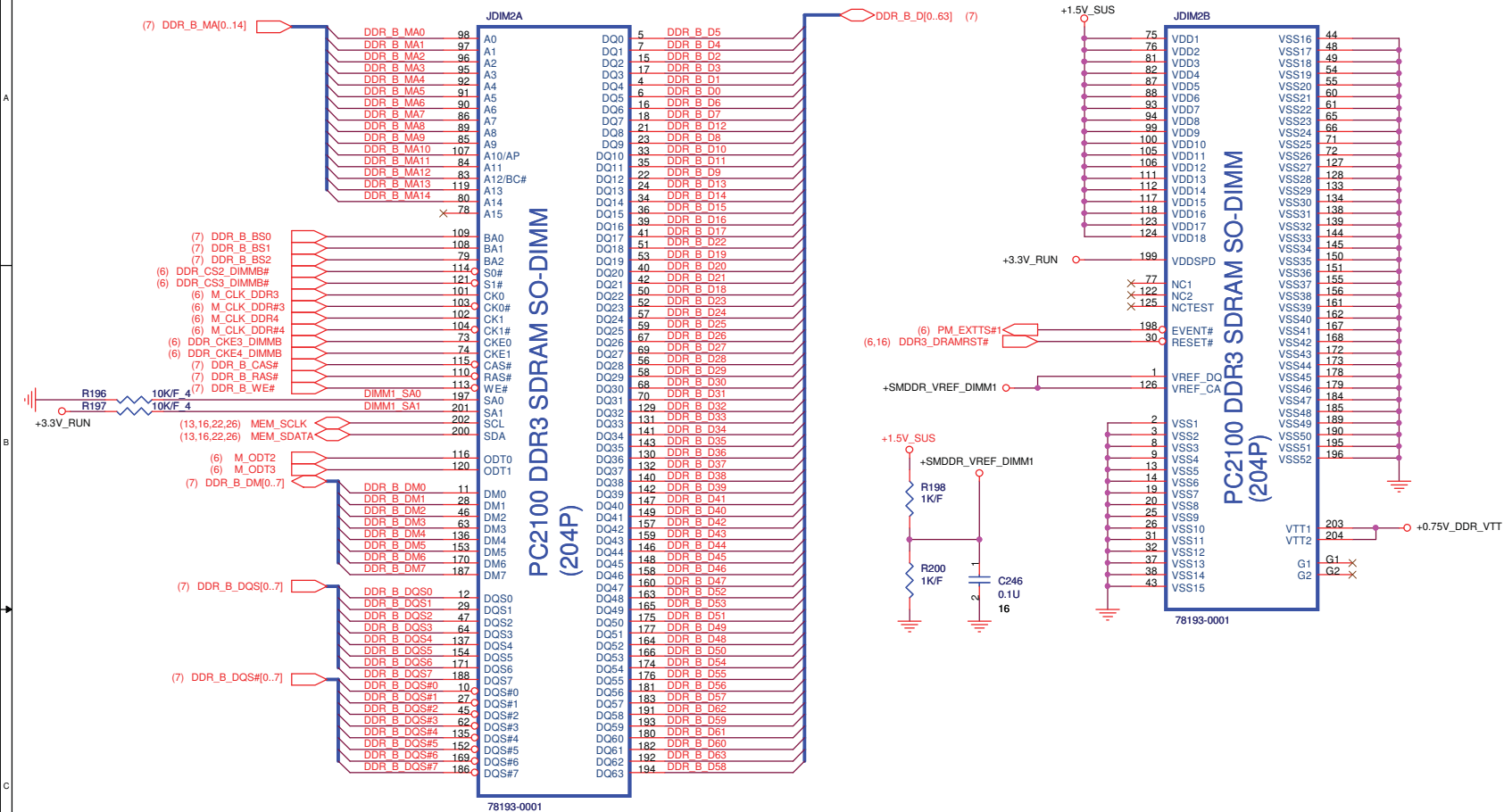
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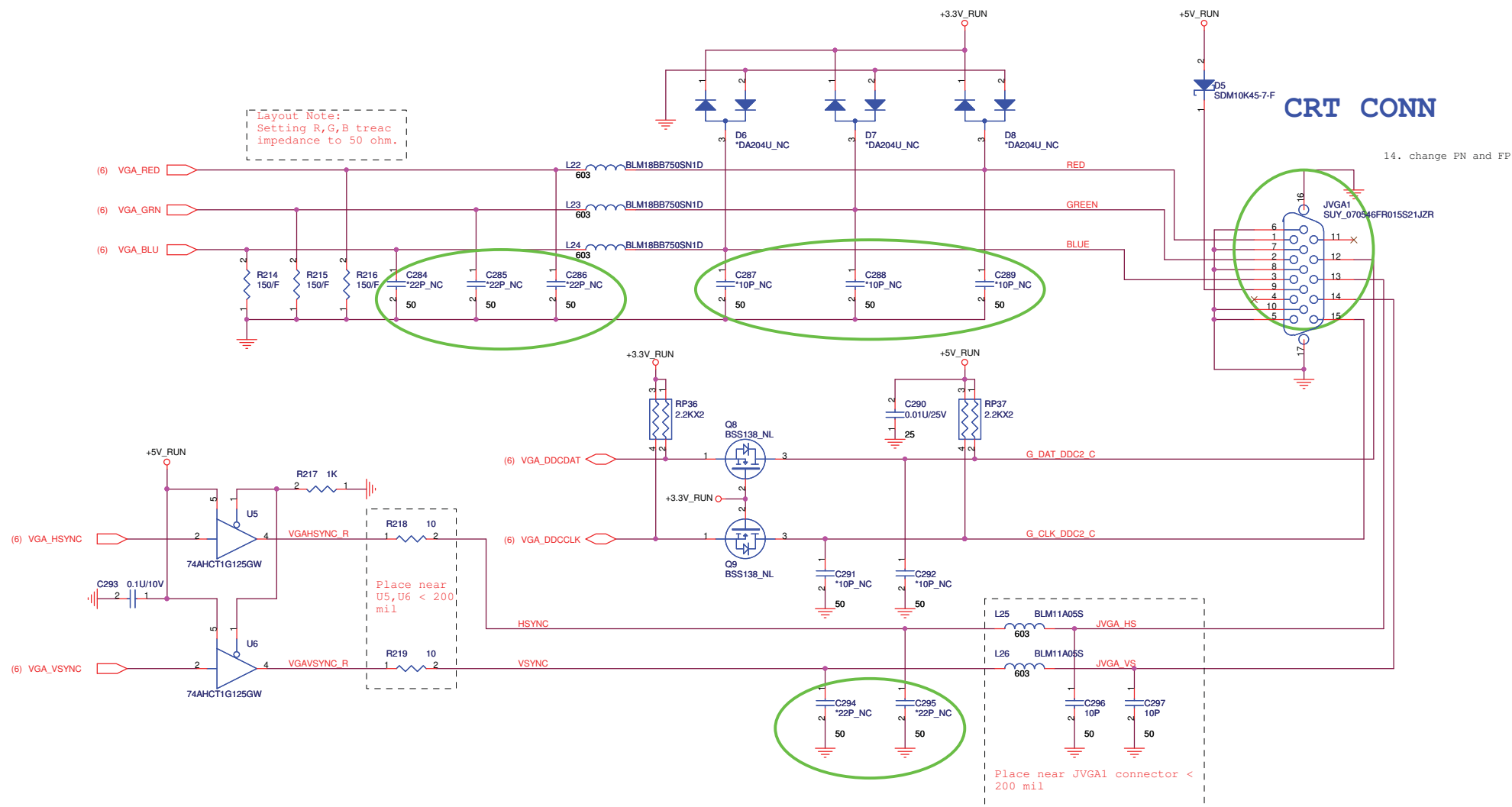
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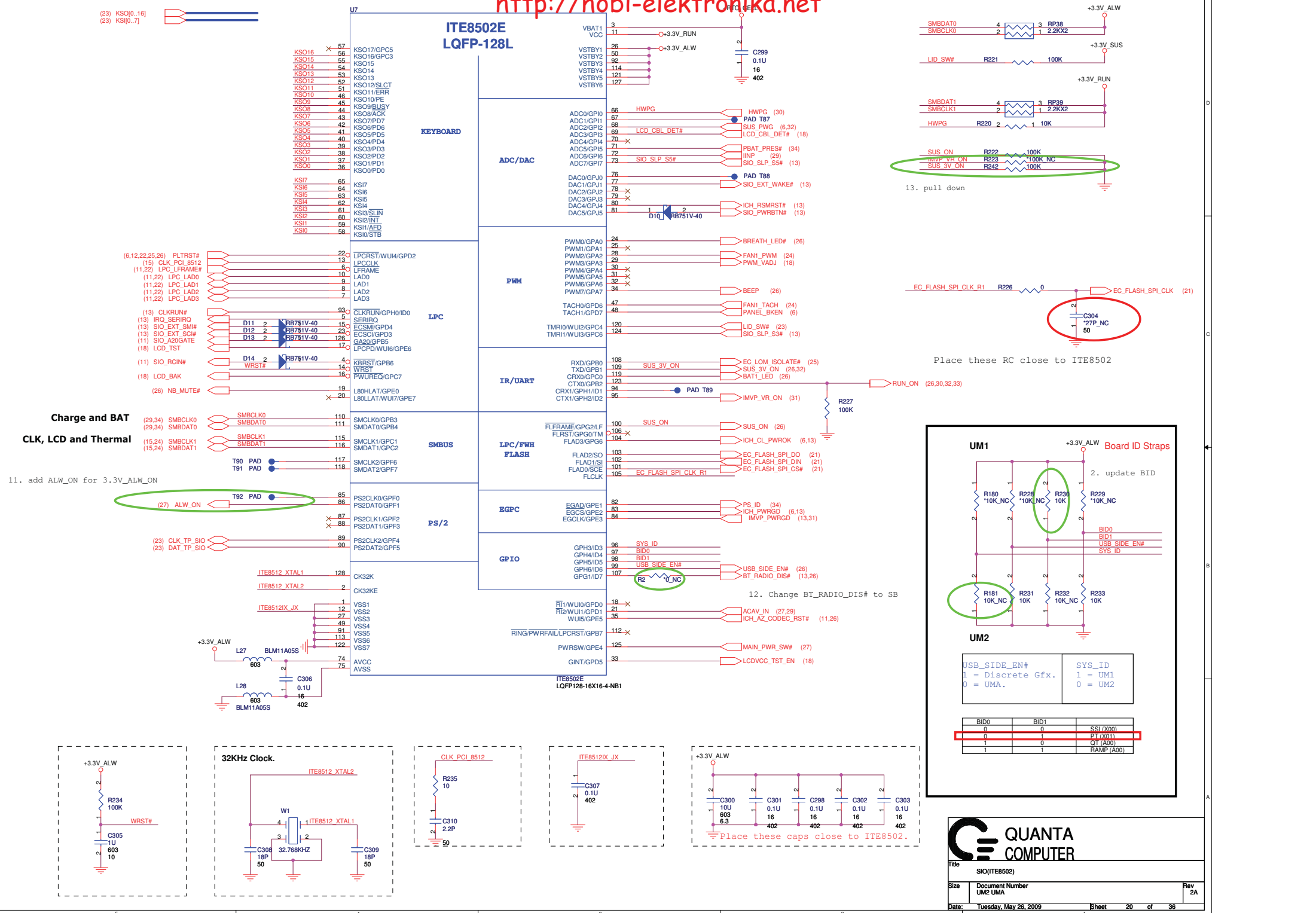
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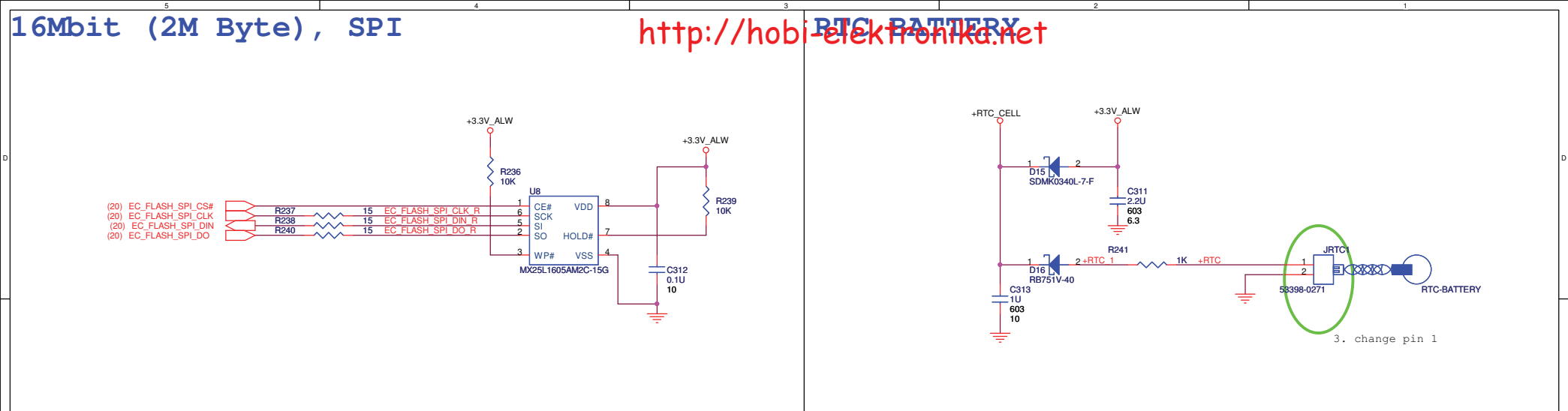
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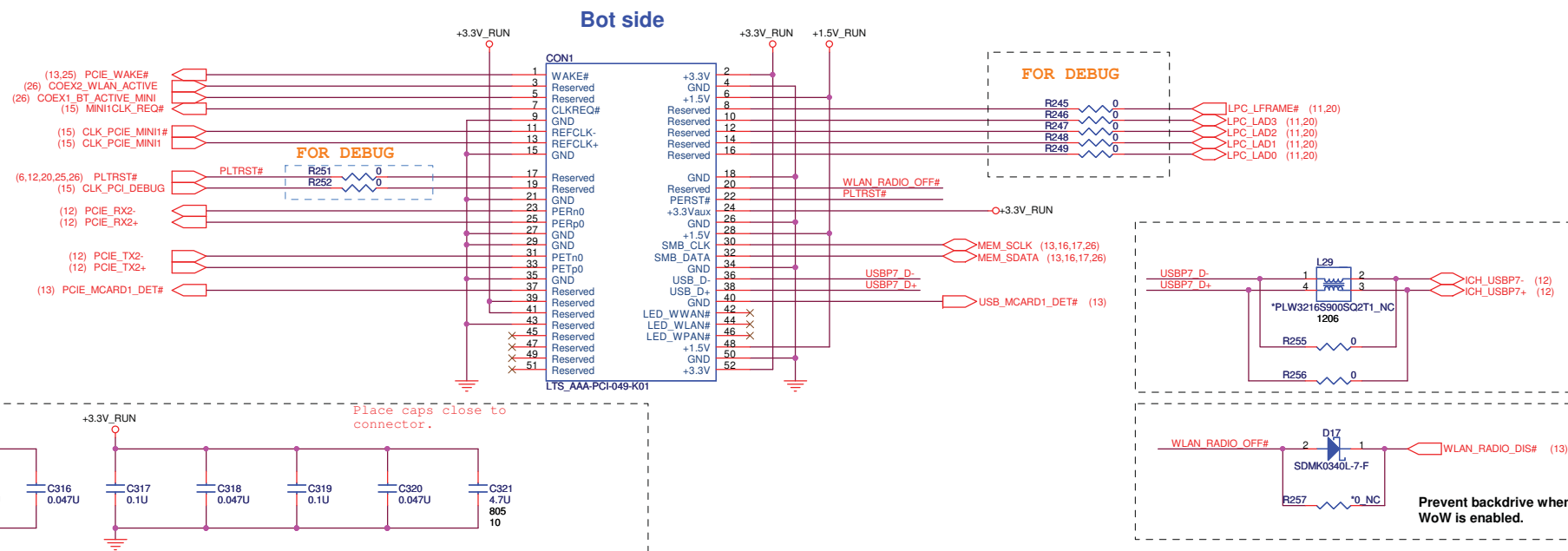
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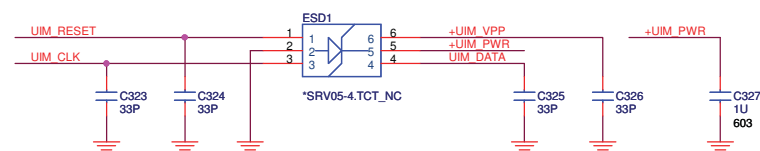
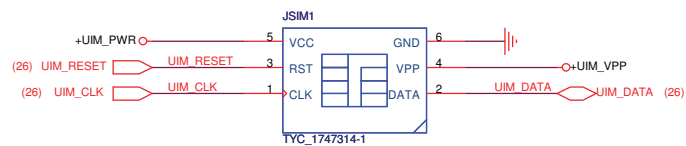








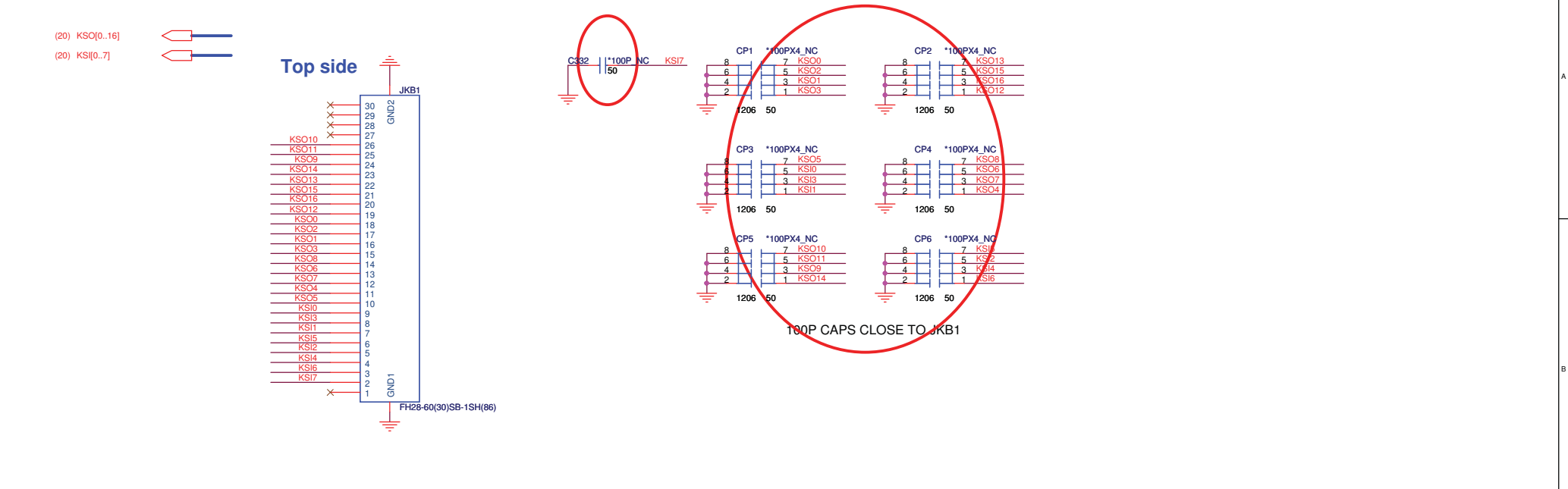
SIM CONN



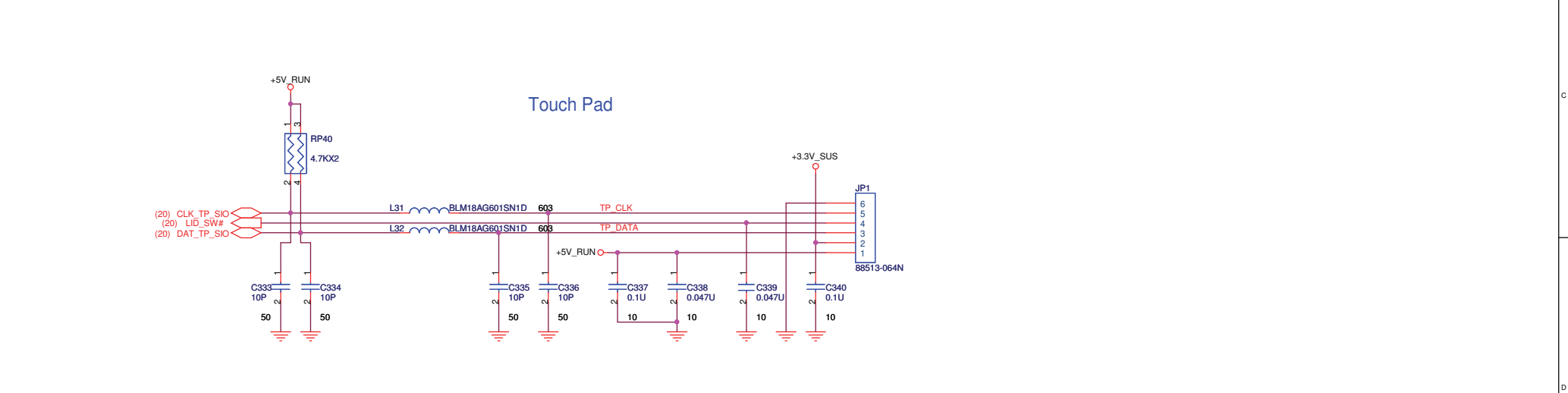
layout note:10 mil trace and 20 mil space for SIM card
and UIM_PWR use 20mil
Place as close as possible to WWAN connector

KEYBOARD CONN

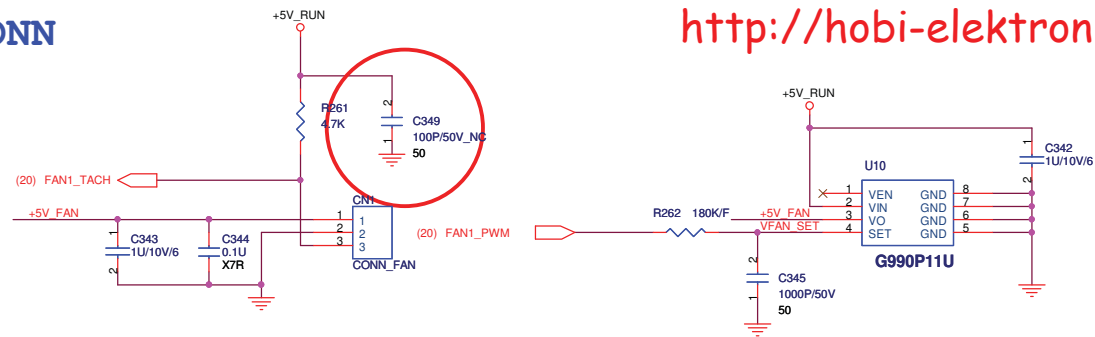
<http://hobi-elektronika.net>



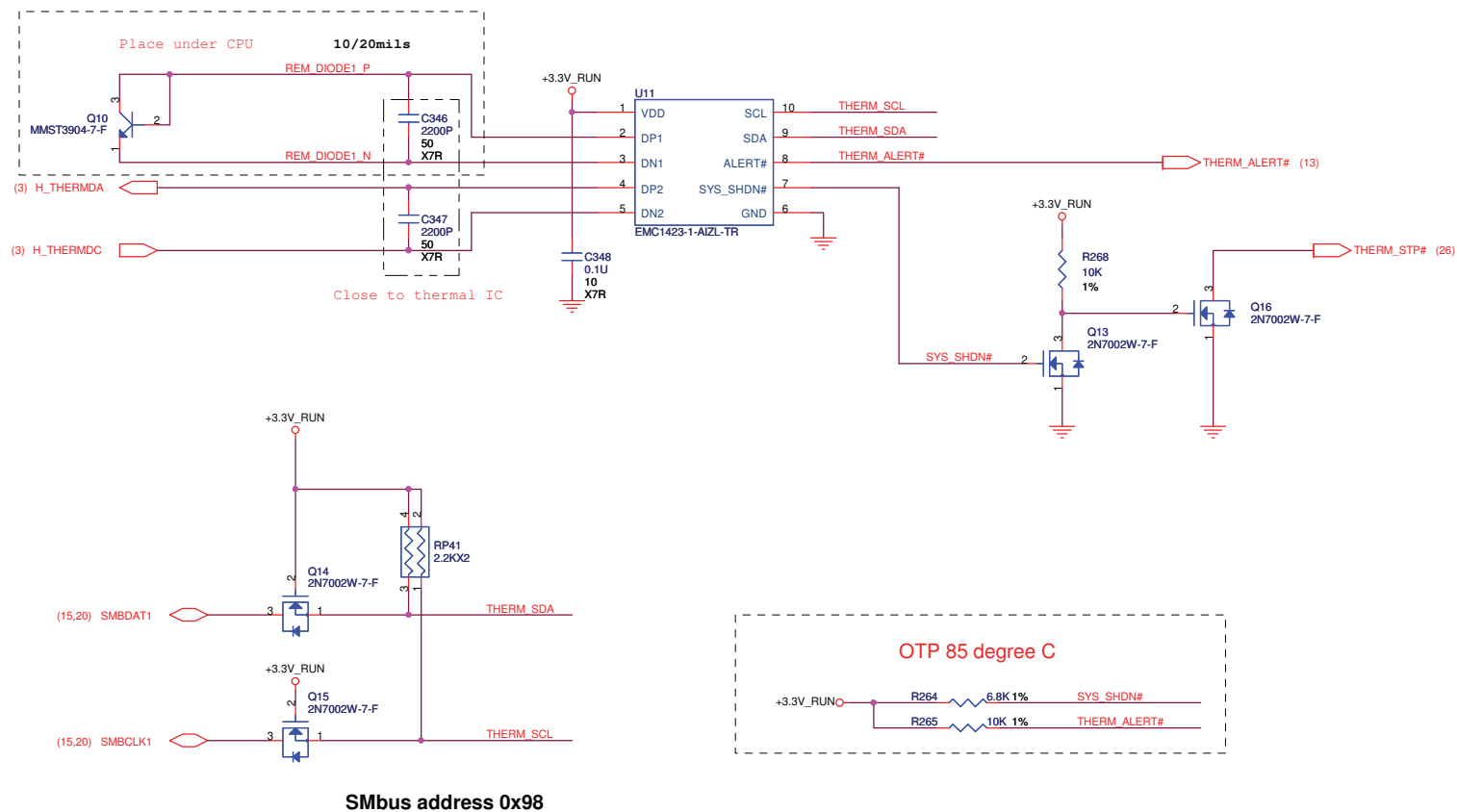
Touch Pad CONN



<http://hobi-elektronika.net>



THERMAL IC



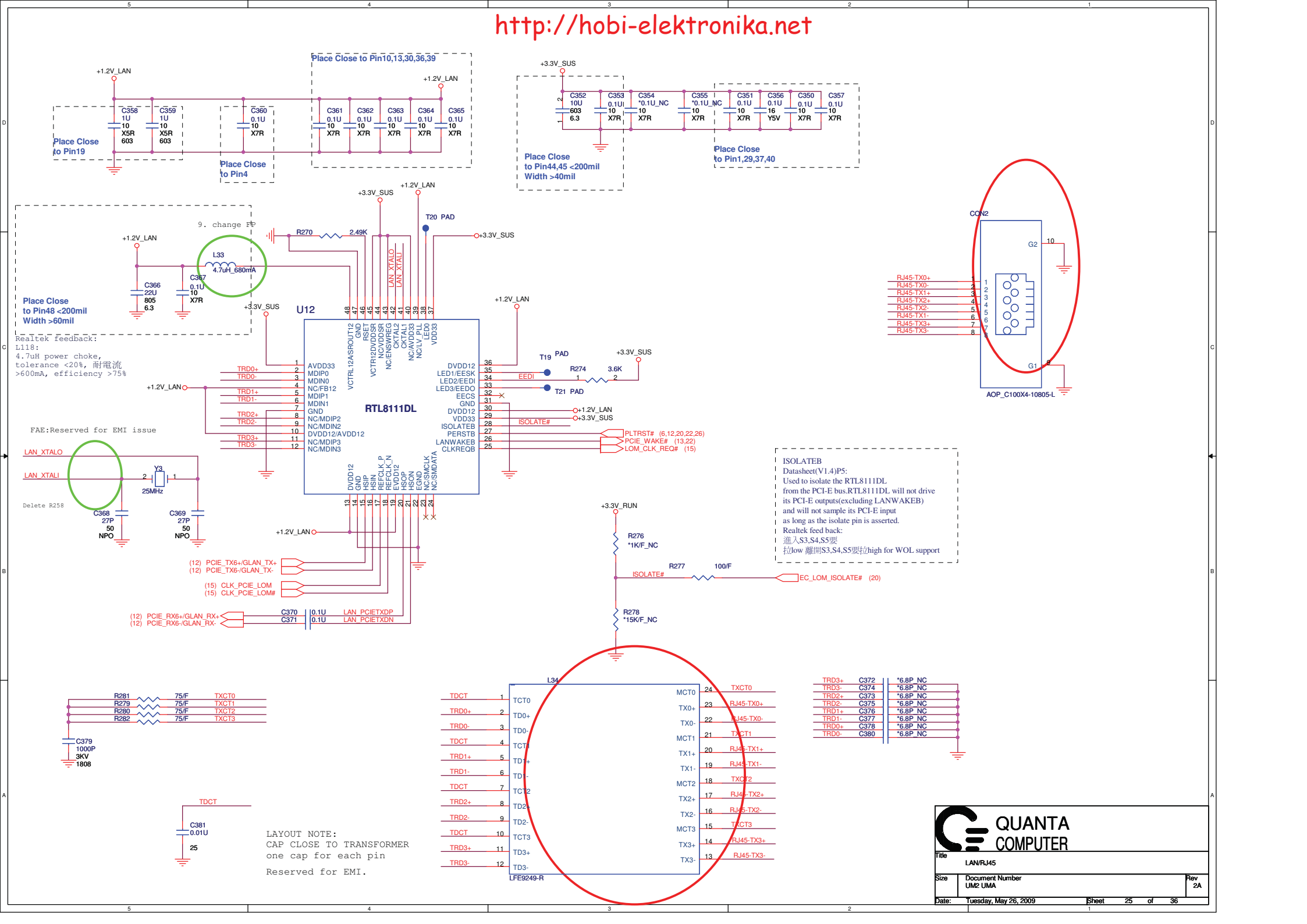
Title FAN & THERMAL

Size	Document Number UM2 UMA
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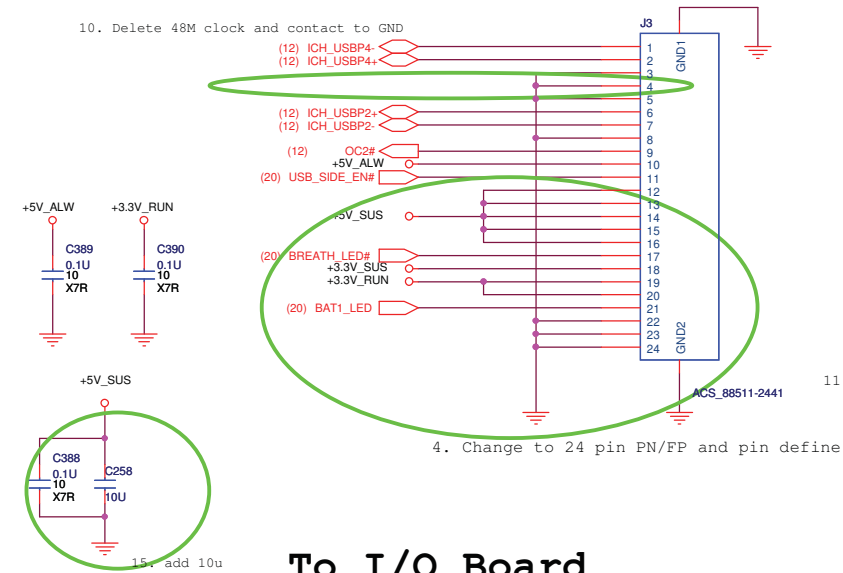
Rev
2A



To CardReader Board

Cable connect to DB directly

DB need to reverse pin definition with MB

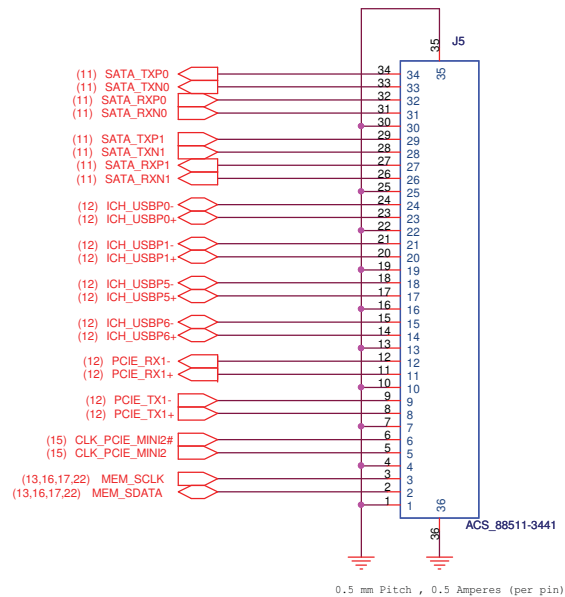


To I/O Board

Cable connect to DB directly

DB need to reverse pin definition with MB

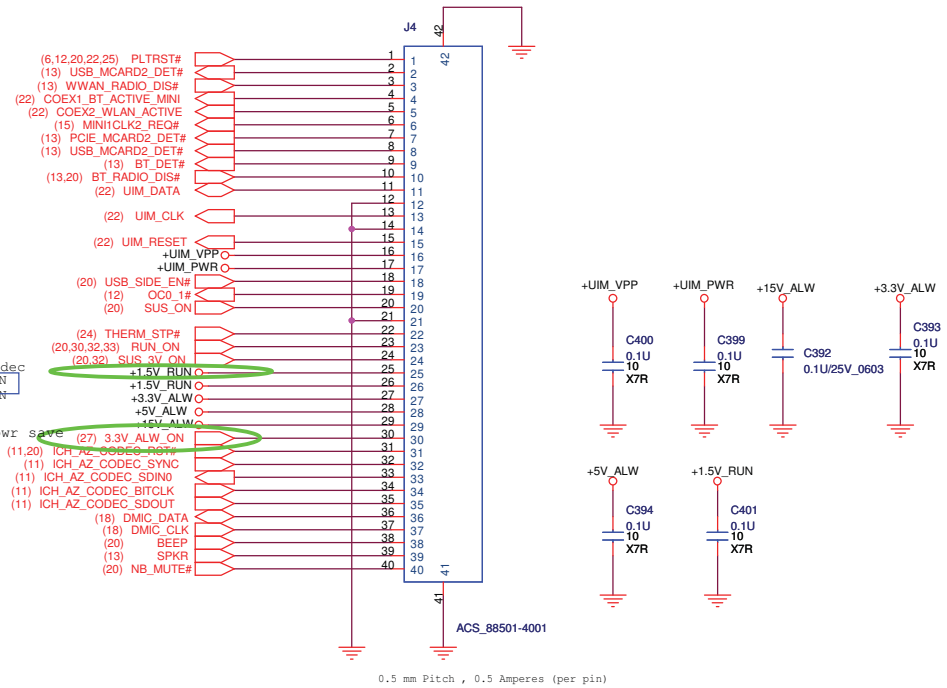
Zo=95



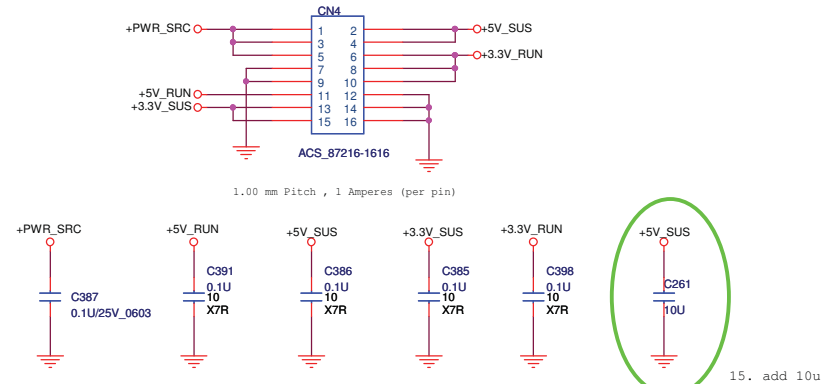
To I/O Board

FFC connect to DB with one turn

DB need to follow pin definition with MB

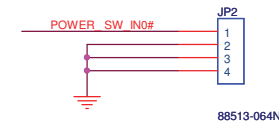


To I/O Board

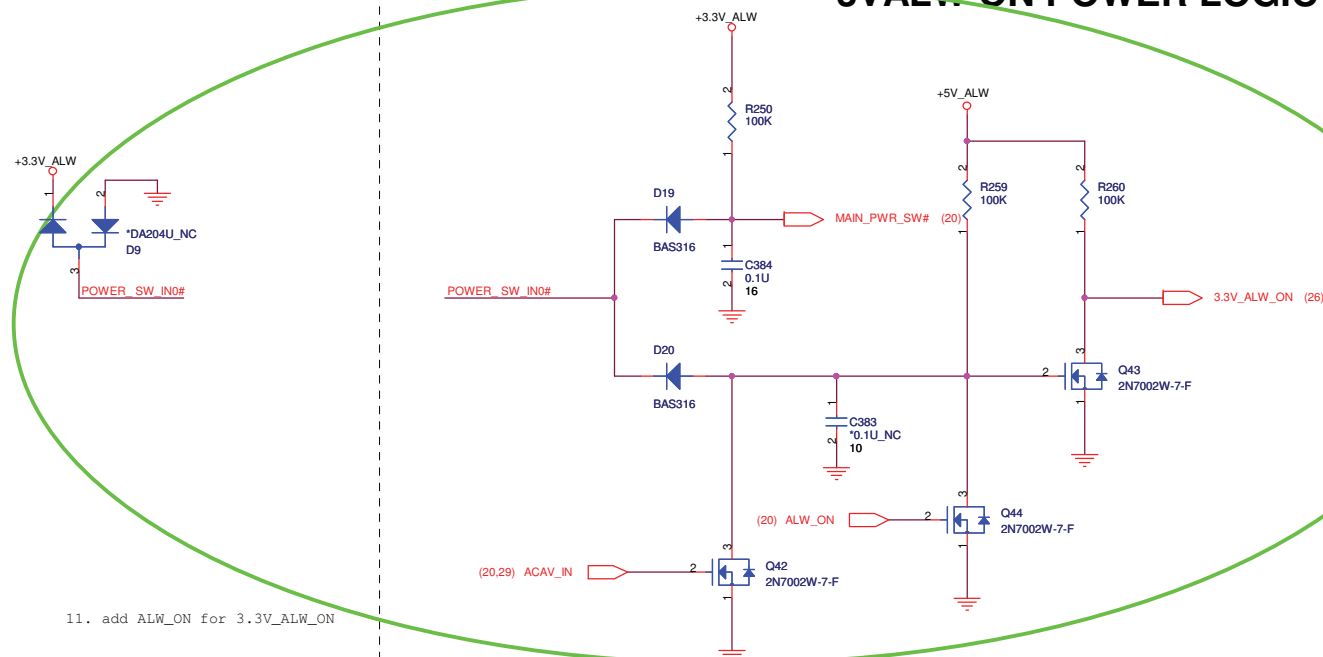


Title		
IO BOARD		
Size	Document Number	Rev
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Dash board connector



3VALW ON POWER LOGIC



Title
POWER SWITCH

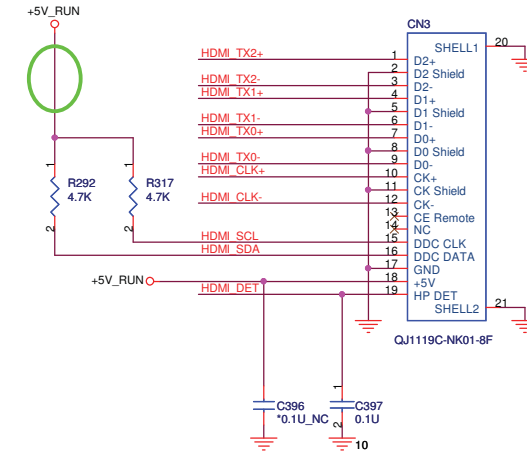
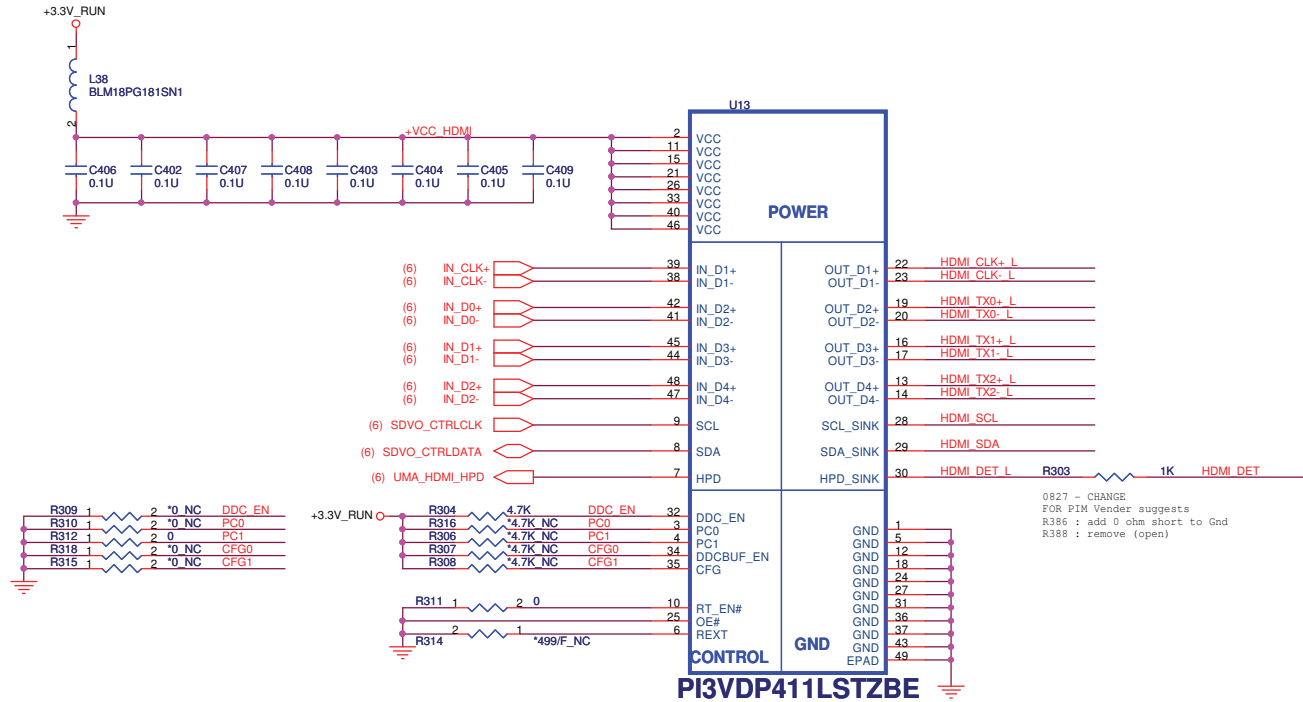
Size
Document Number
UM2 UMA

Rev
2A

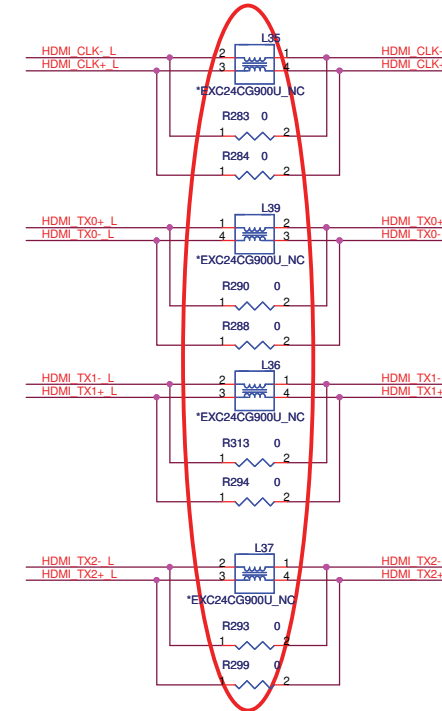
Date: Tuesday, May 26, 2009

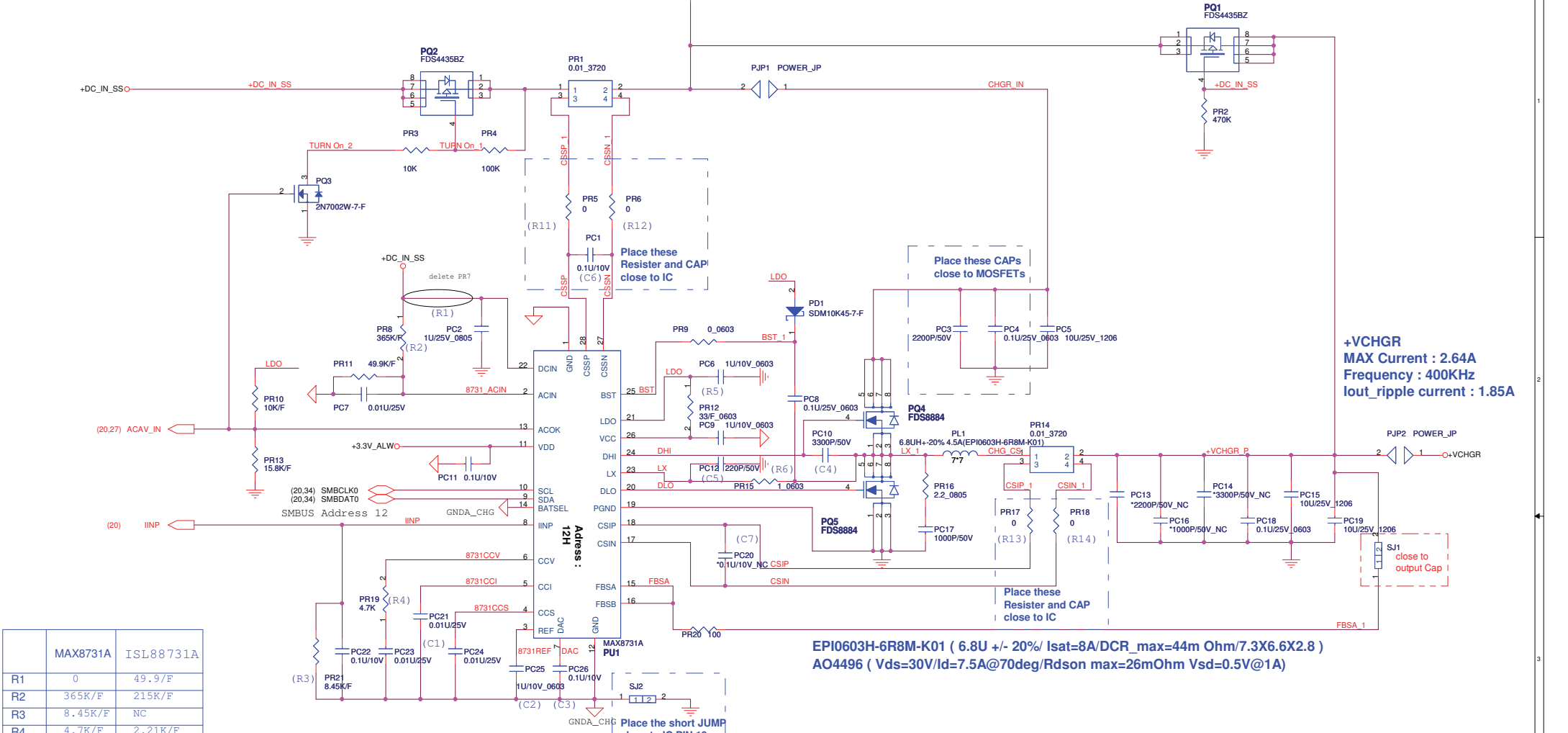
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HDMI Connector



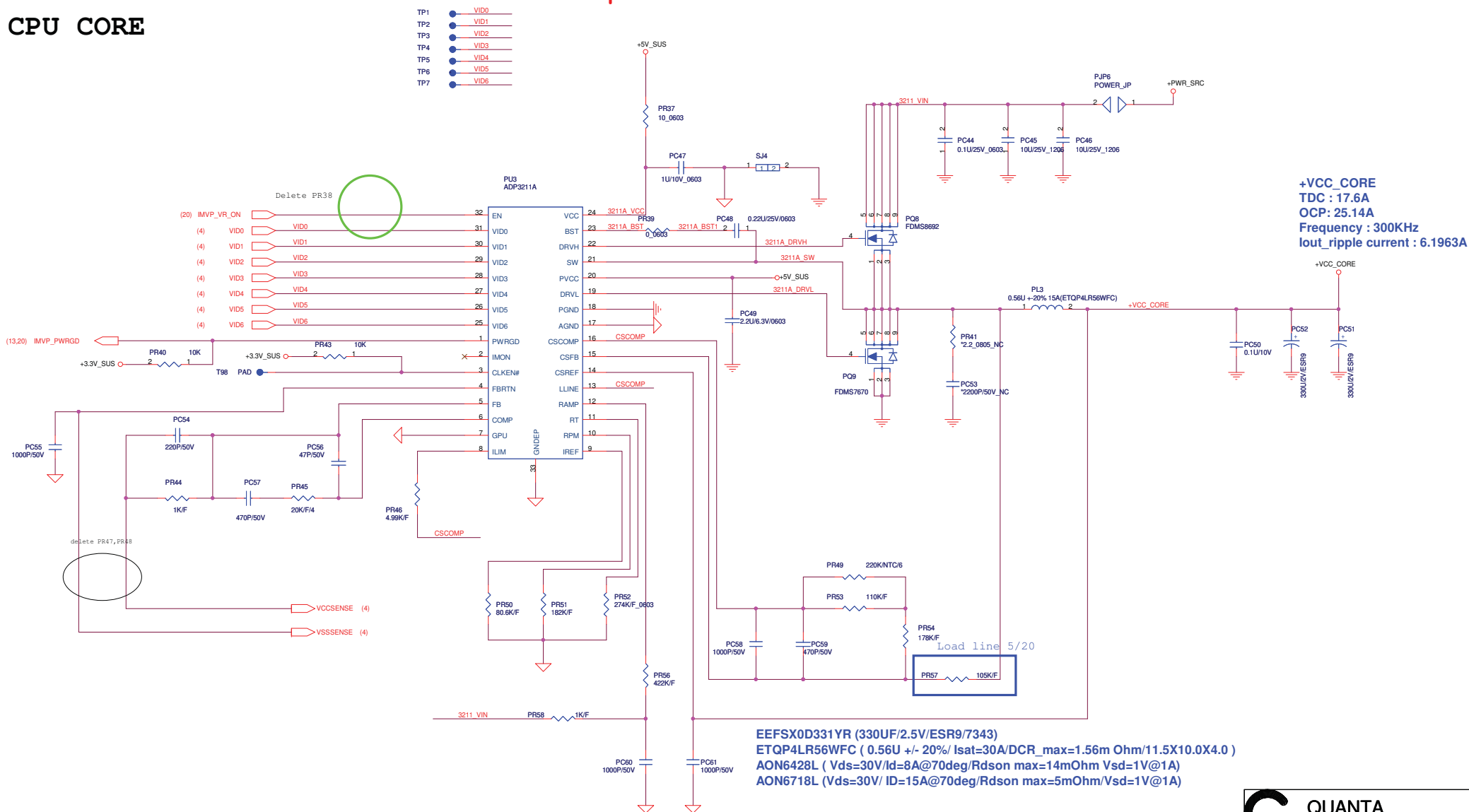
Reserve for EMI and close to HDMI CONN

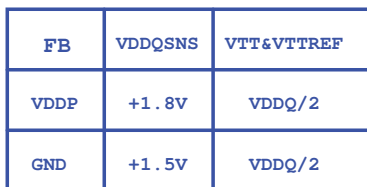




+VCHGR
MAX Current : 2.64A
Frequency : 400KHz
Iout_ripple current : 1.85A

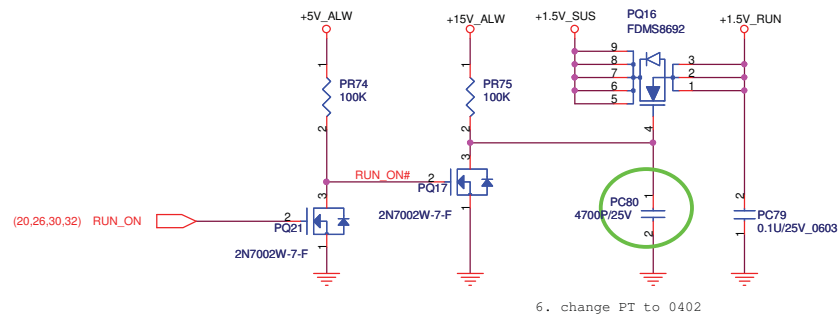






+1.5V_RUN

Max current(TDC) : 1.6A



+1.8V_RUN

Max current (TDC) -> 105mA
For UMA

