

# Compal confidential

## Schematics Document

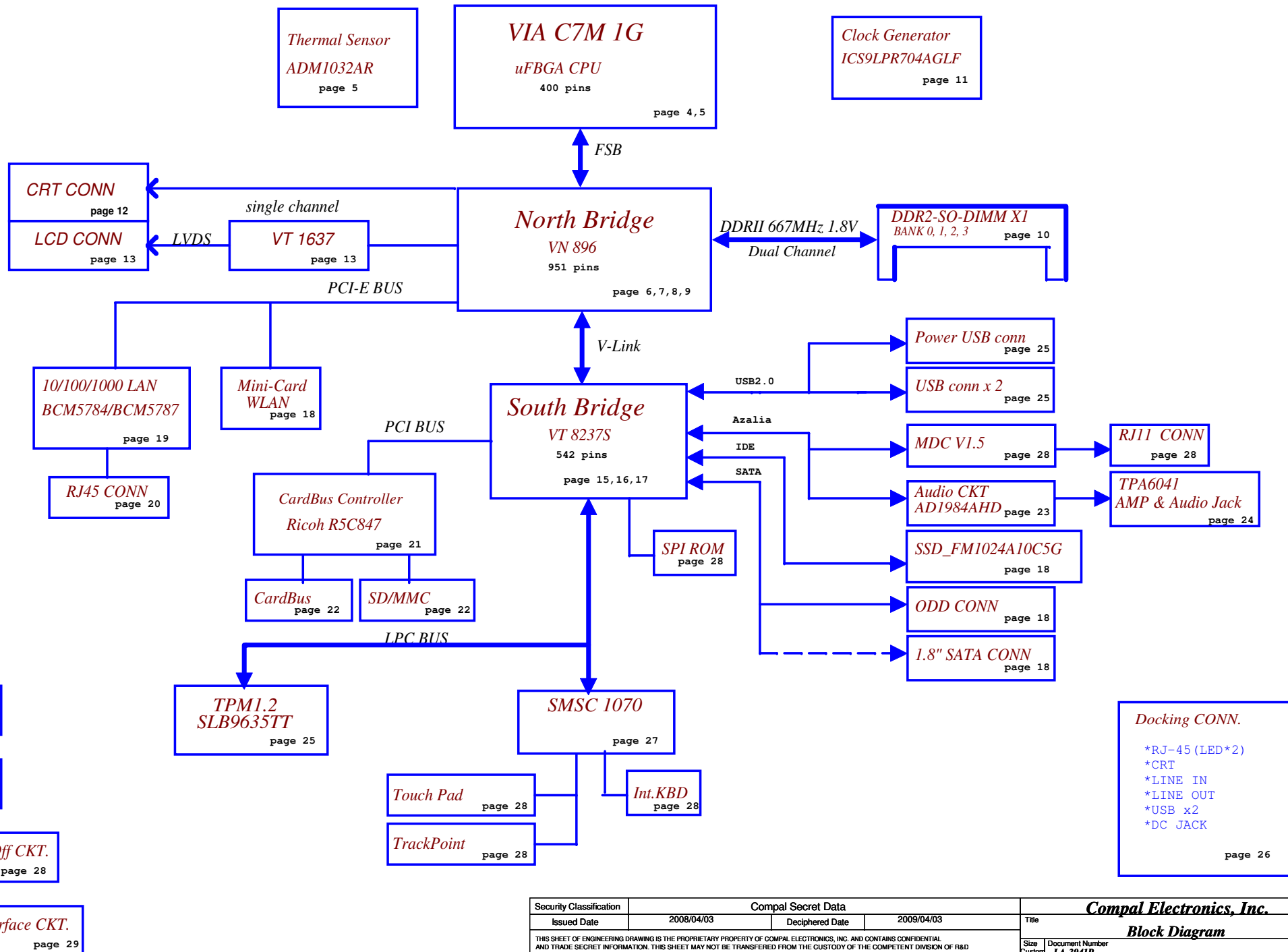
Mobile C-7M uFBGA with  
VIA 896 NB & 8237S SB

2008-04-03

REV:1.0



Security Classification	Compal Secret Data			Title <b>Compal Electronics, Inc.</b>		
Issued Date	2008/04/03	Deciphered Date	2009/04/03	Size		Rev
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LED  
page 28

RTC CKT.  
page 15

Power On/Off CKT.  
page 28

DC/DC Interface CKT.  
page 29

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Title			<b>Compal Electronics, Inc.</b>	
Size			<b>Block Diagram</b>	
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Docking CONN.  
\*RJ-45 (LED\*2)  
\*CRT  
\*LINE IN  
\*LINE OUT  
\*USB x2  
\*DC JACK  
page 26

## Voltage Rails

power plane / State	+B LDO3 LDO5	+5VALW +3VALW +1.5VALW	+1.8V	+5VS +3VS +1.8VS +1.5VS +1.6VS_NB +CPU_CORE +VCCP +0.9VS +VCCA
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

○ MEANS ON    ✗ MEANS OFF

## PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS	AD19	0	A,B,C

## SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD	CAP SENSOR
SMB_EC_CK1 SMB_EC_DAI	EC	✓	✗	✗	✗	✗	✗	✗
Cap_CLK Cap_DAT	EC	✗	✗	✗	✗	✗	✗	✓
SB_SMCLK SB_SMDATA	SB	✗	✓	✓	✓	✓	✗	✗
LCD_CLK LCD_DAT	NB	✗	✗	✗	✗	✗	✓	✗

## Install below 43 level BOM structure for ver. 0.6

DEBUG@ : means just build when PCIE port 80 CARD function enable. *Remove before MP*

NO1394@ : means just build without 1394 function

5787@ : means just build when 5787 function enable.

SSC@ : means just build when LVDS SS function enable.

## Install below 45 level BOM structure for ver. 0.6

45@ : means just put it in the BOM of 45 level.

## Reserve below BOM structure for ver. 0.6

@ : means just reserve , no build

CONN@ : means ME part.

BT@ : means just build when BT function enable. *Install at DB-1 only*

NOSSC@ : means just build when LVDS SS function disable.

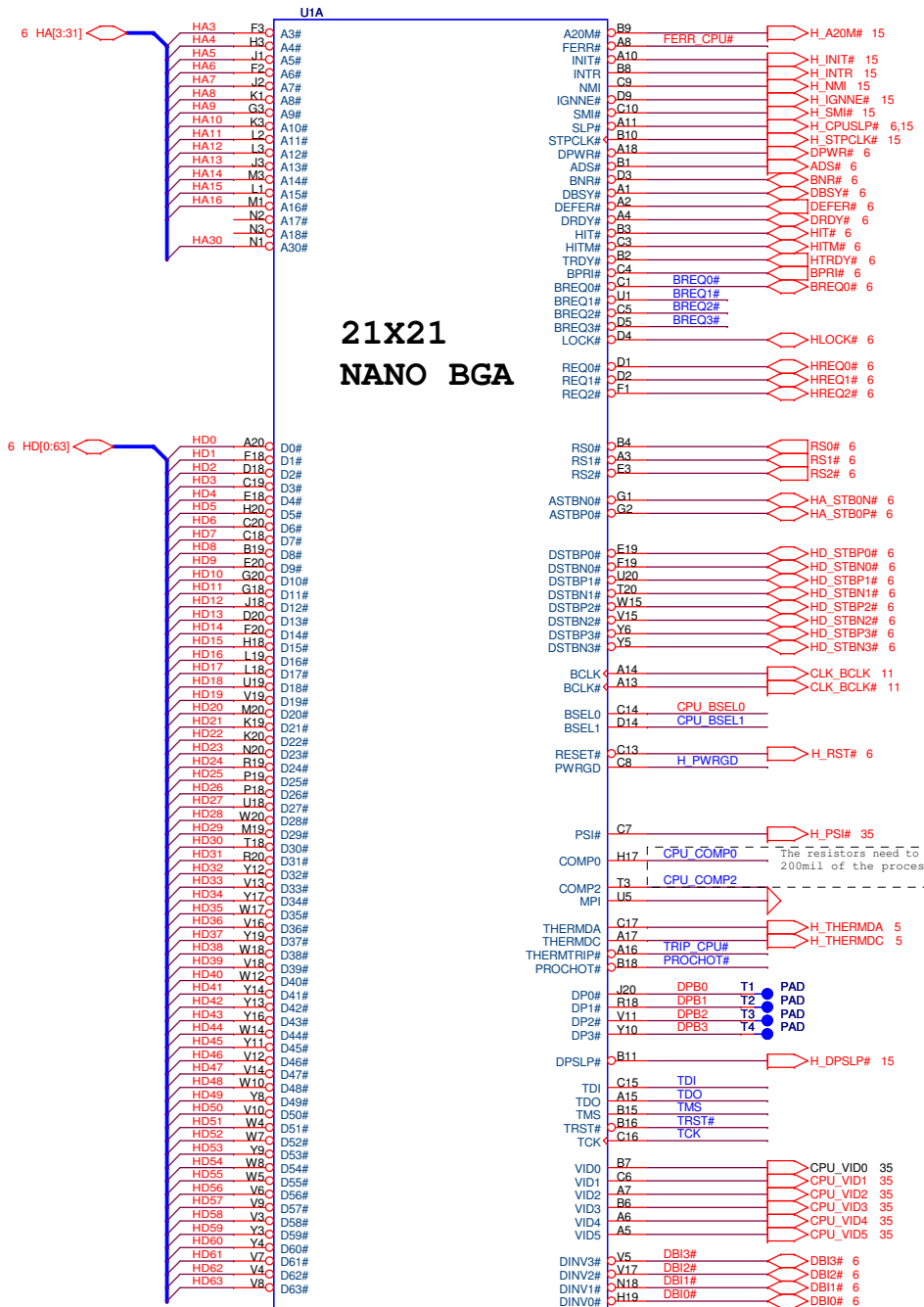
5784@ : means just build when 5784 function enable.

TPM@ : means just build when TPM function enable. *Install at DB-2, SI-1 only*

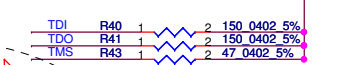
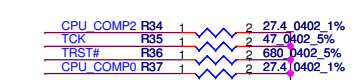
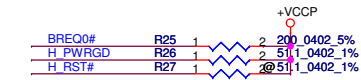
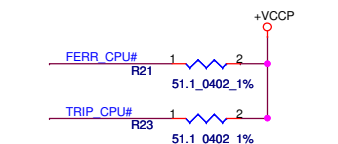
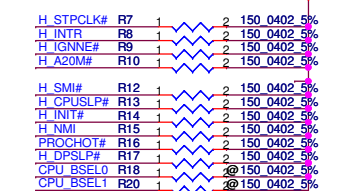
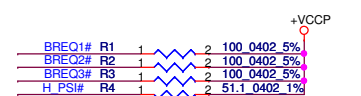
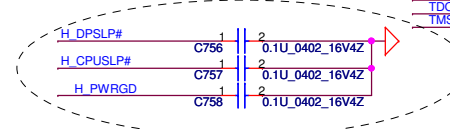
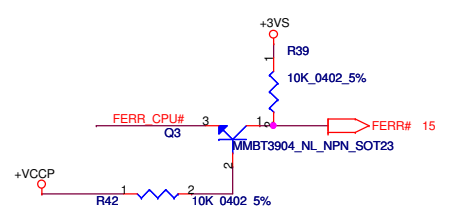
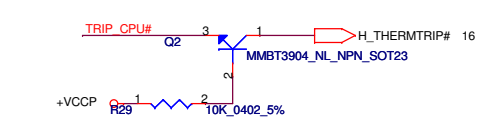
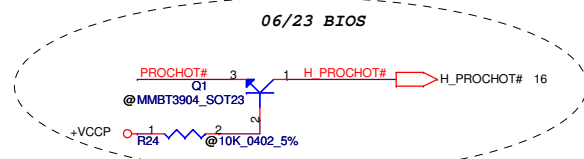
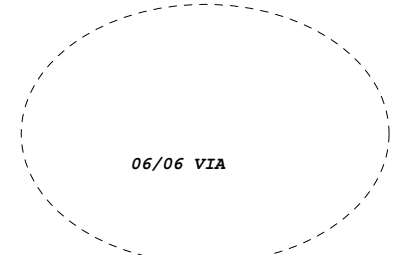
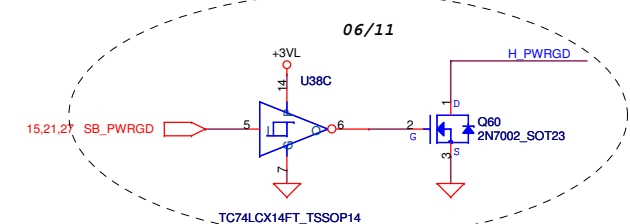
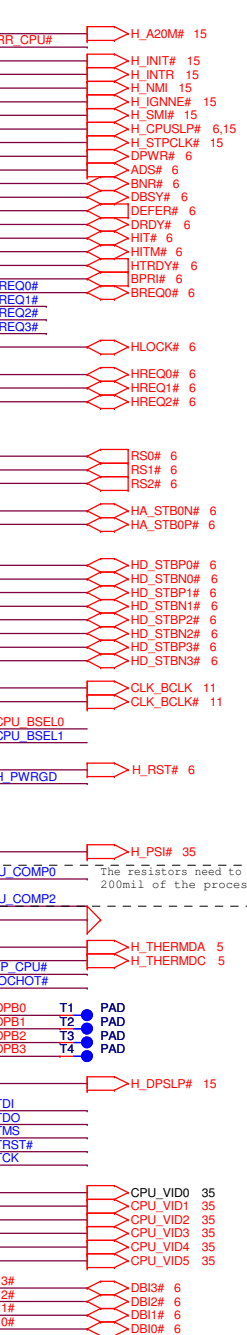
1394@ : means just build when 1394 function enable. *Remove before MP*

HDD@ : means just build when 1.8" SATA HDD function enable. *Remove before MP*

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**21X21  
NANO BGA**



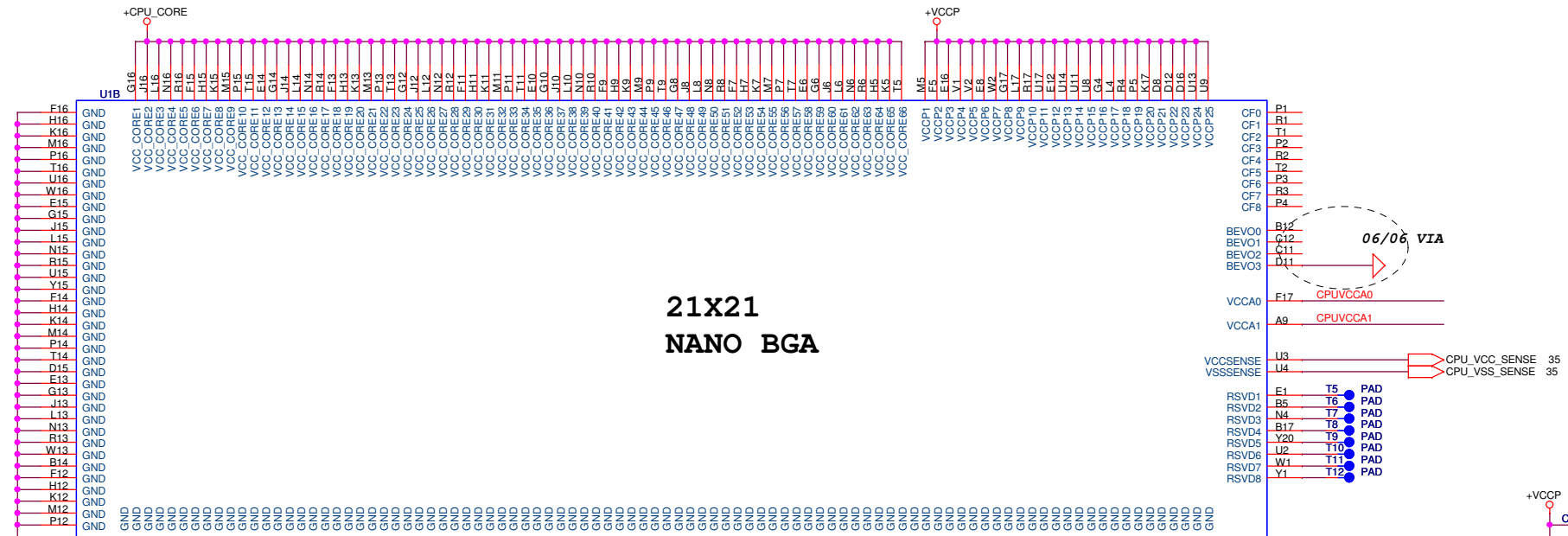
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<b>Compal Electronics, Inc.</b>		
<b>CPU PART1</b>		
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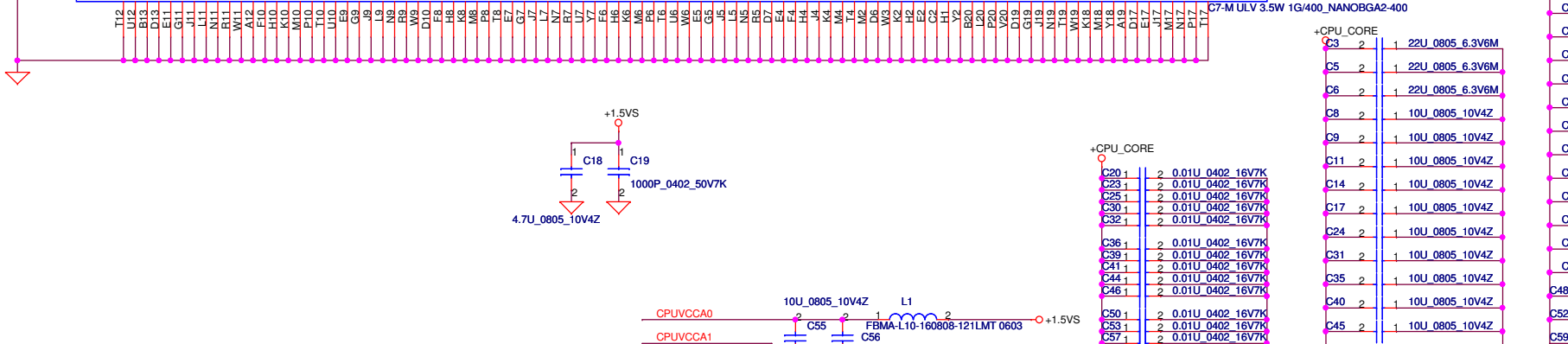


PCB 038 LA-3941P REV1 M/B

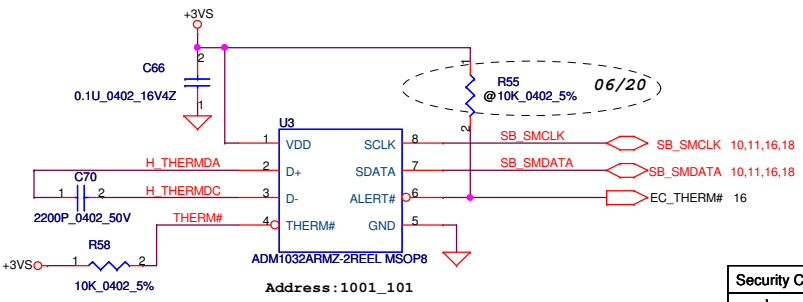


**21X21  
NANO BGA**

C7-M LULV 3.5W 1G/400\_NANO BGA2-400



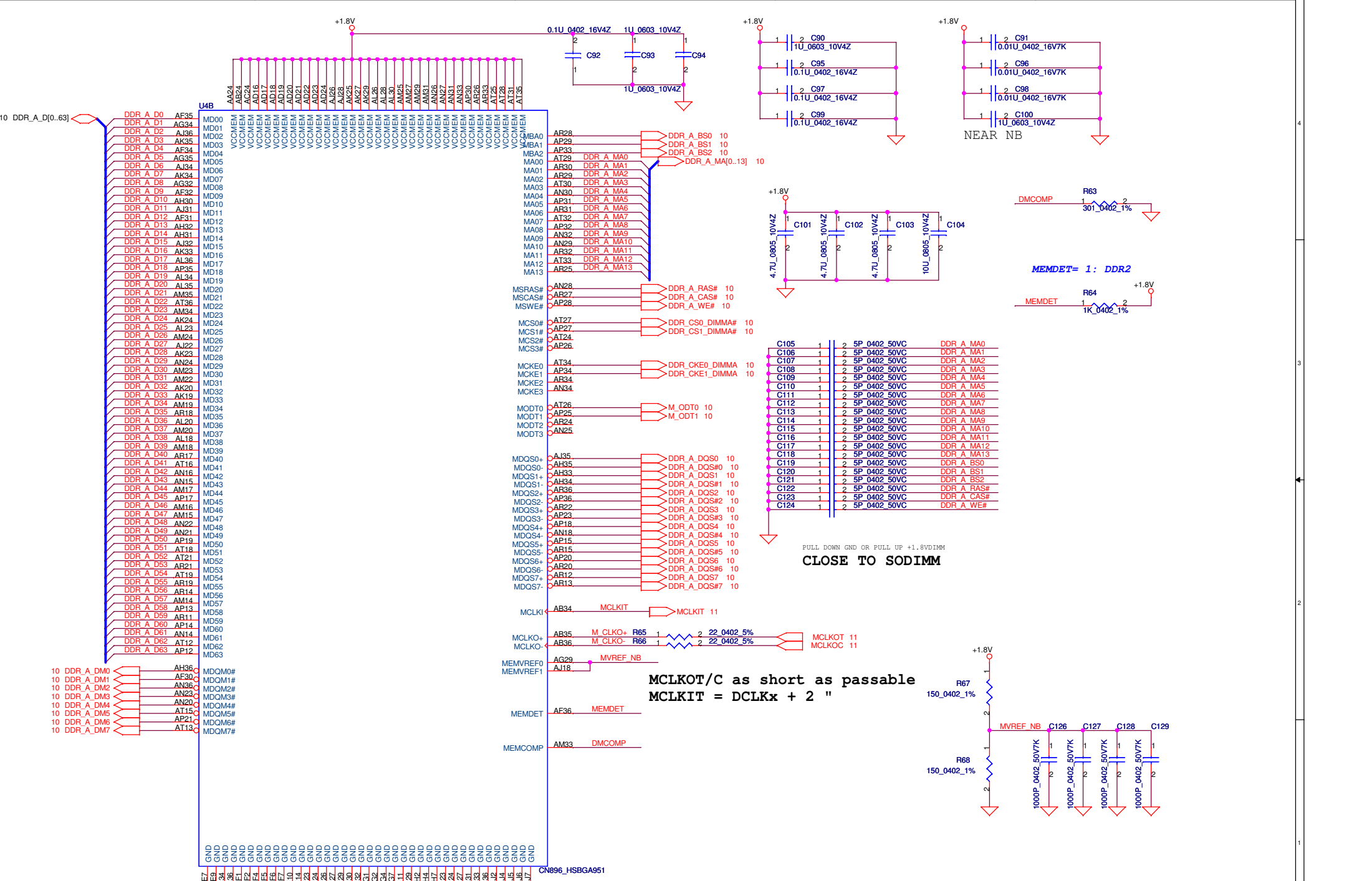
**Thermal Sensor ADM1032**



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<b>Compal Electronics, Inc.</b>		
<b>CPU PART2</b>		
Size	Document Number	Rev
C	<b>LA-3941P</b>	1.0
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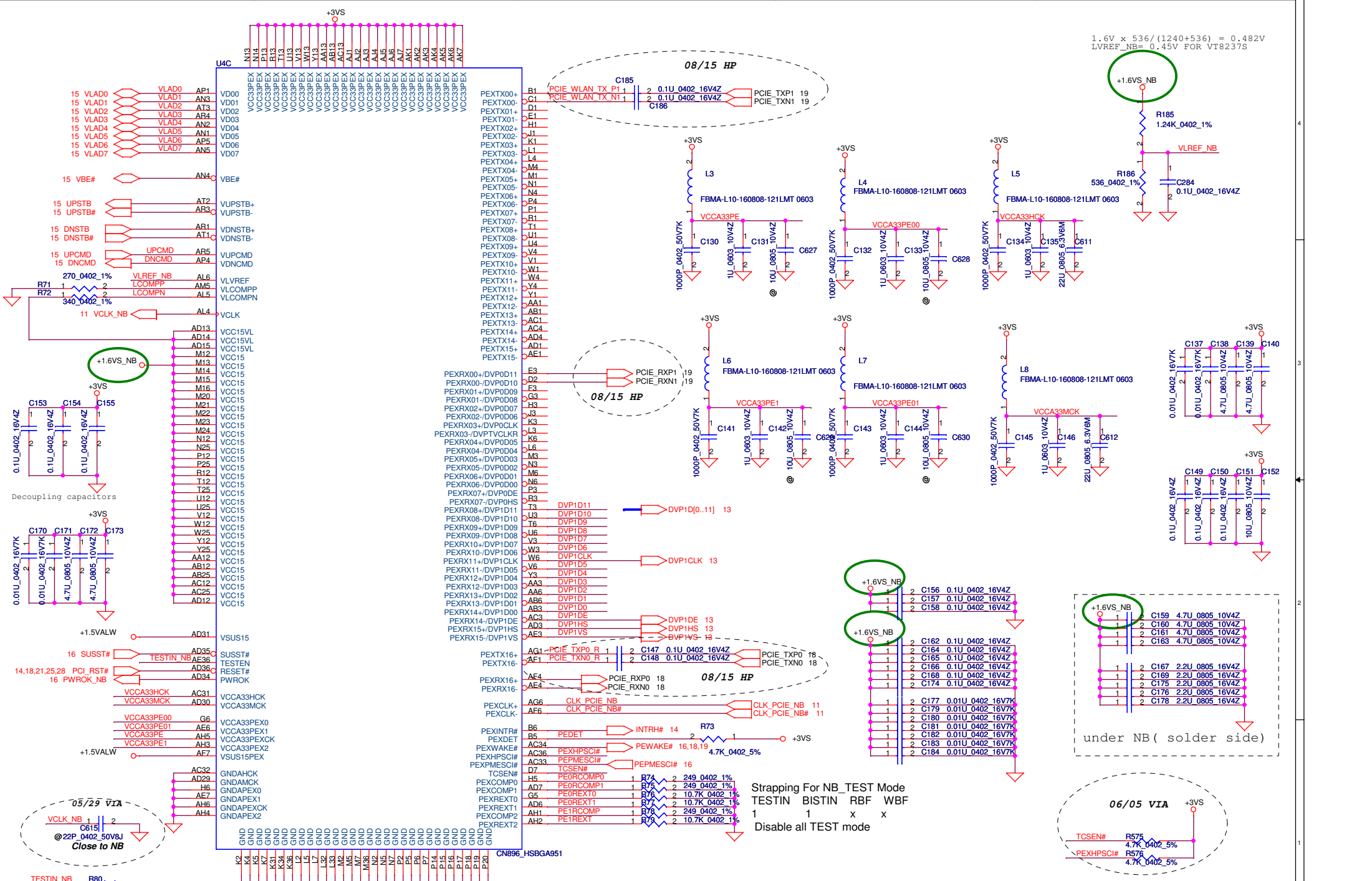




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Title			Compal Electronics, Inc.	
Document Number			DRAM	
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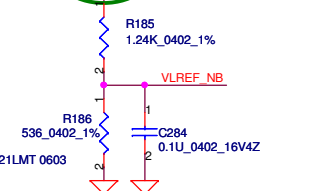




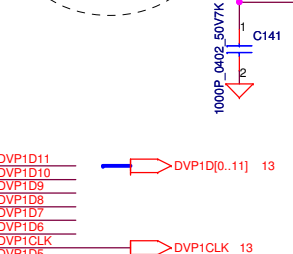
$$1.6V \times 536 / (1240 + 536) = 0.482V$$

$$LVREF\_NB = 0.45V \text{ FOR VT8237S}$$

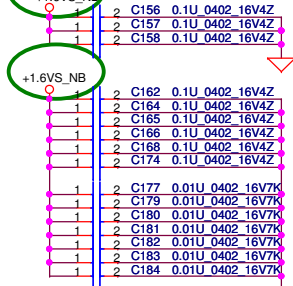
+1.6VS\_NB



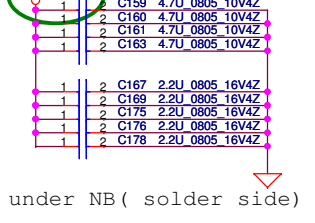
08/15 HP



+1.6VS\_NB

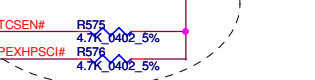


+1.6VS\_NB



under NB (solder side)

06/05 VIA



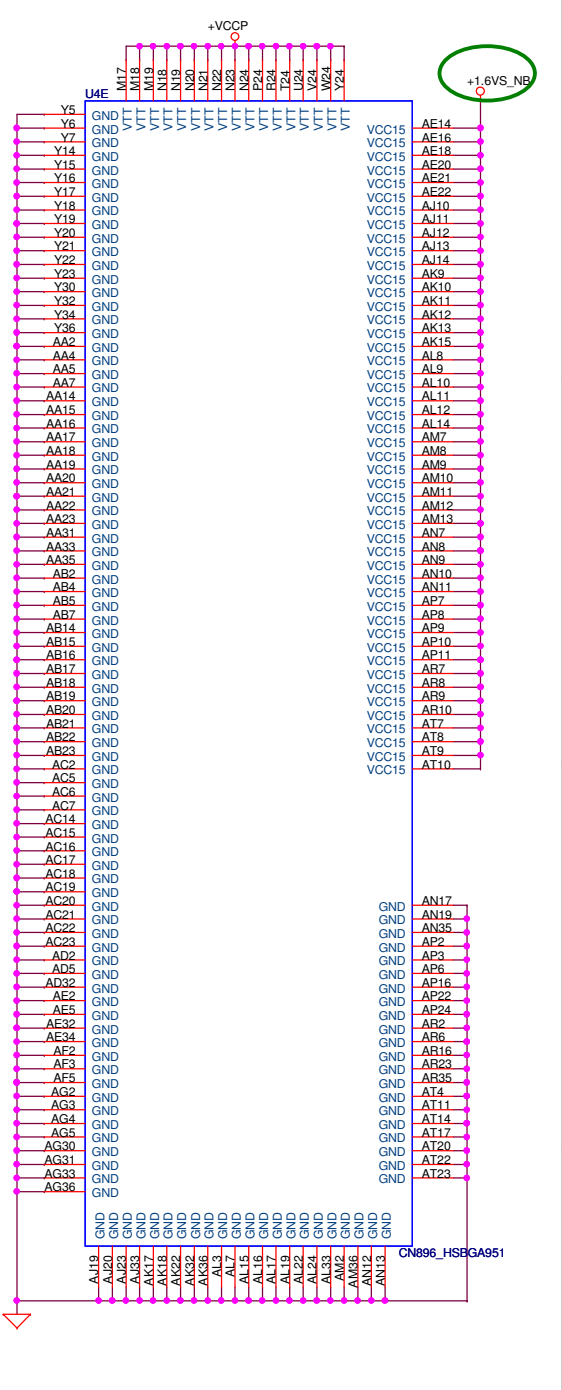
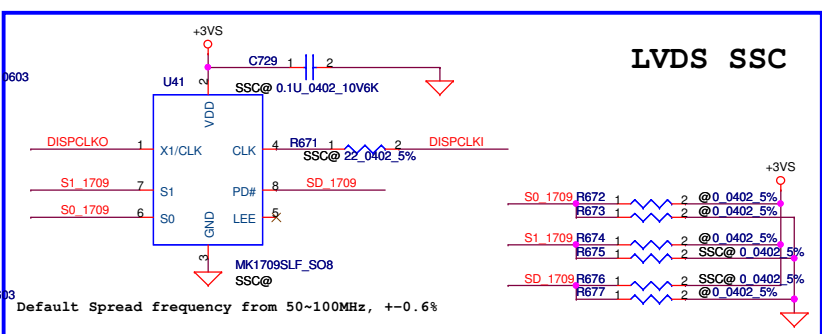
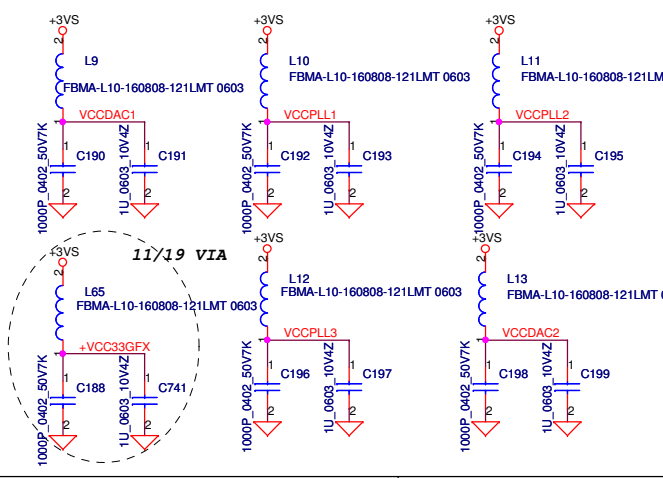
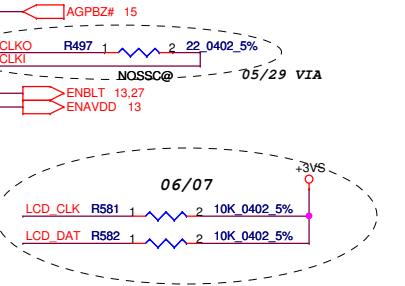
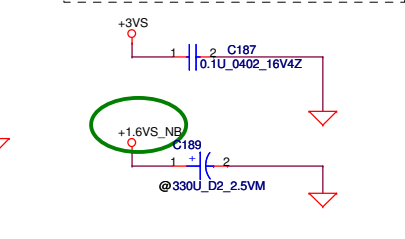
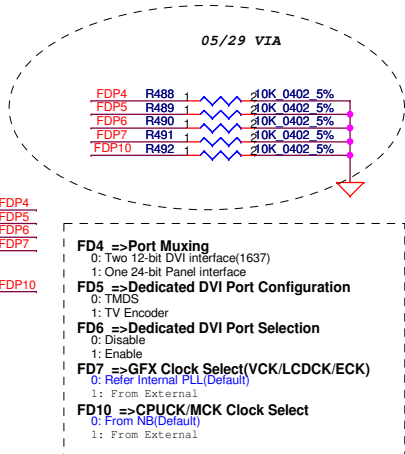
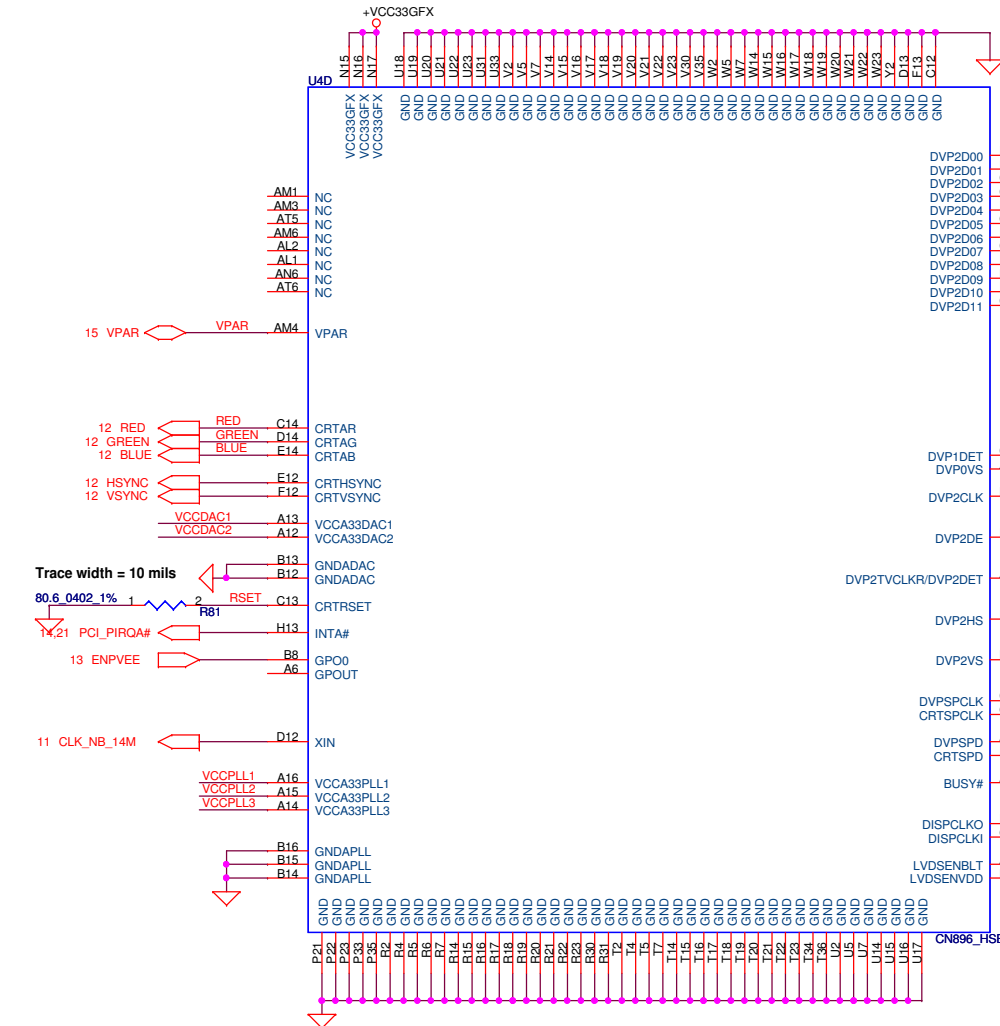
Strapping For NB\_TEST Mode  
TESTIN BISTIN RBF WBF  
Disable all TEST mode

CN896\_HSBGA951

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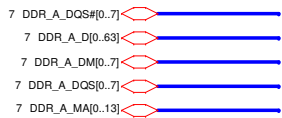
Compal Electronics, Inc.			
GFX			
Title	GFX		
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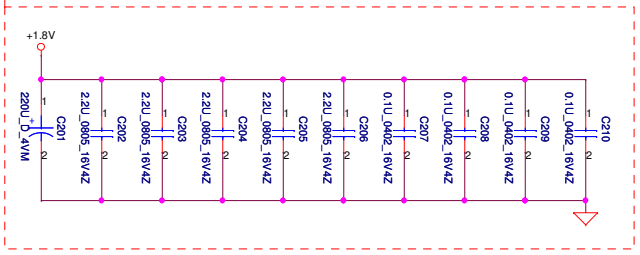


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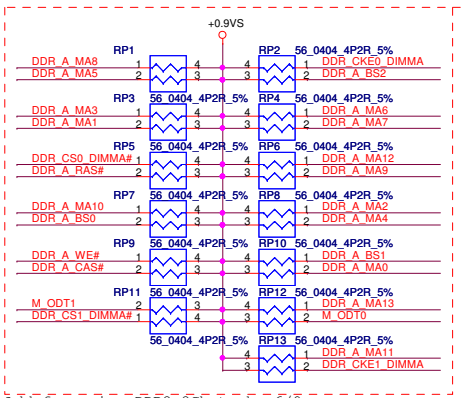
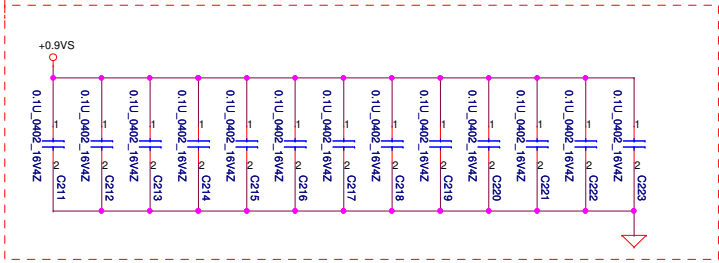
<b>Compal Electronics, Inc.</b> <b>DISPLAY</b>	
Title	
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**Layout Note:**  
Place near JP9

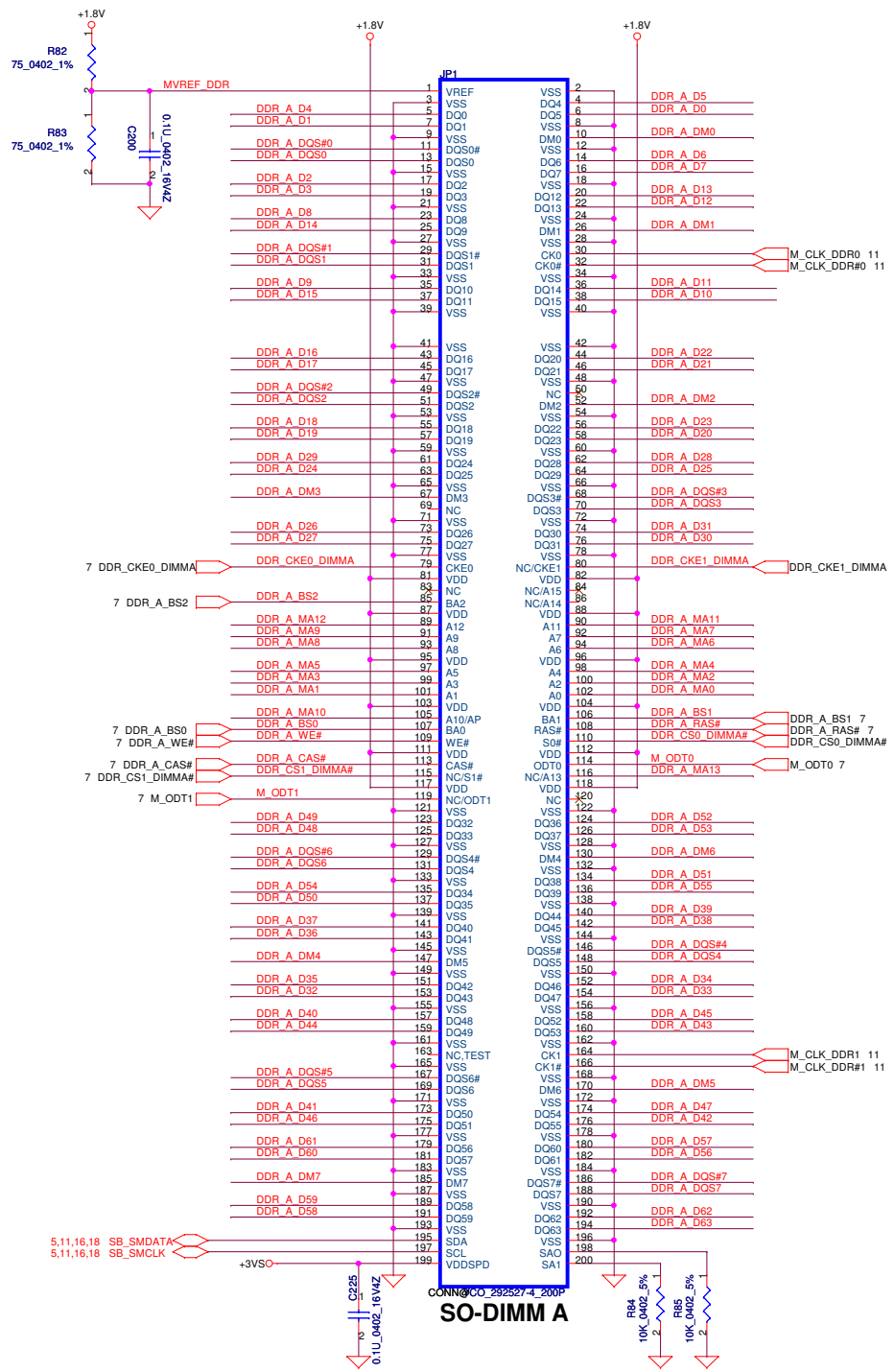


**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



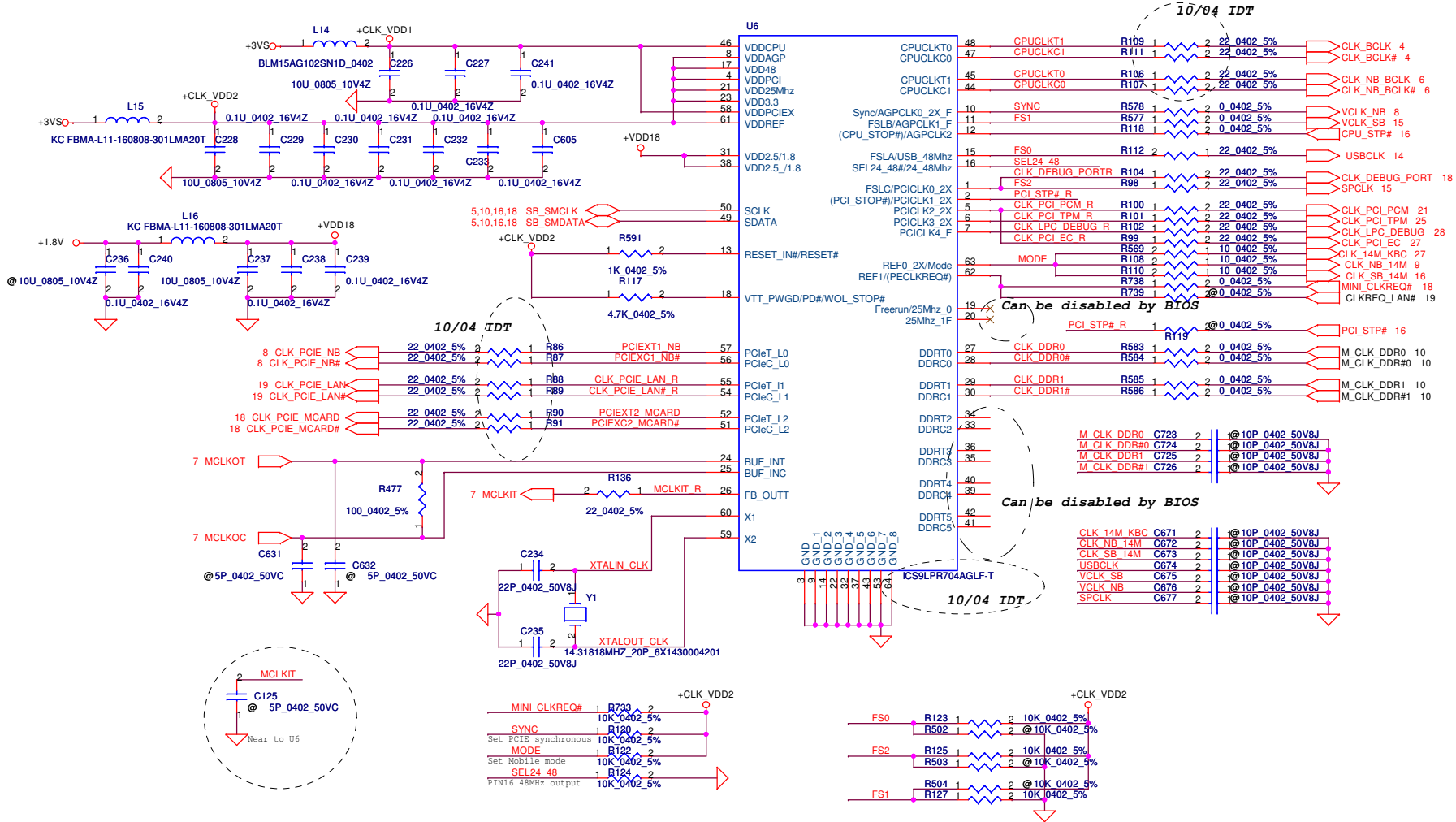
**Layout Note:**  
Place these resistor closely JP9, all trace length Max=1.5"

Add for using DDR2 2Gb tech. 6/9



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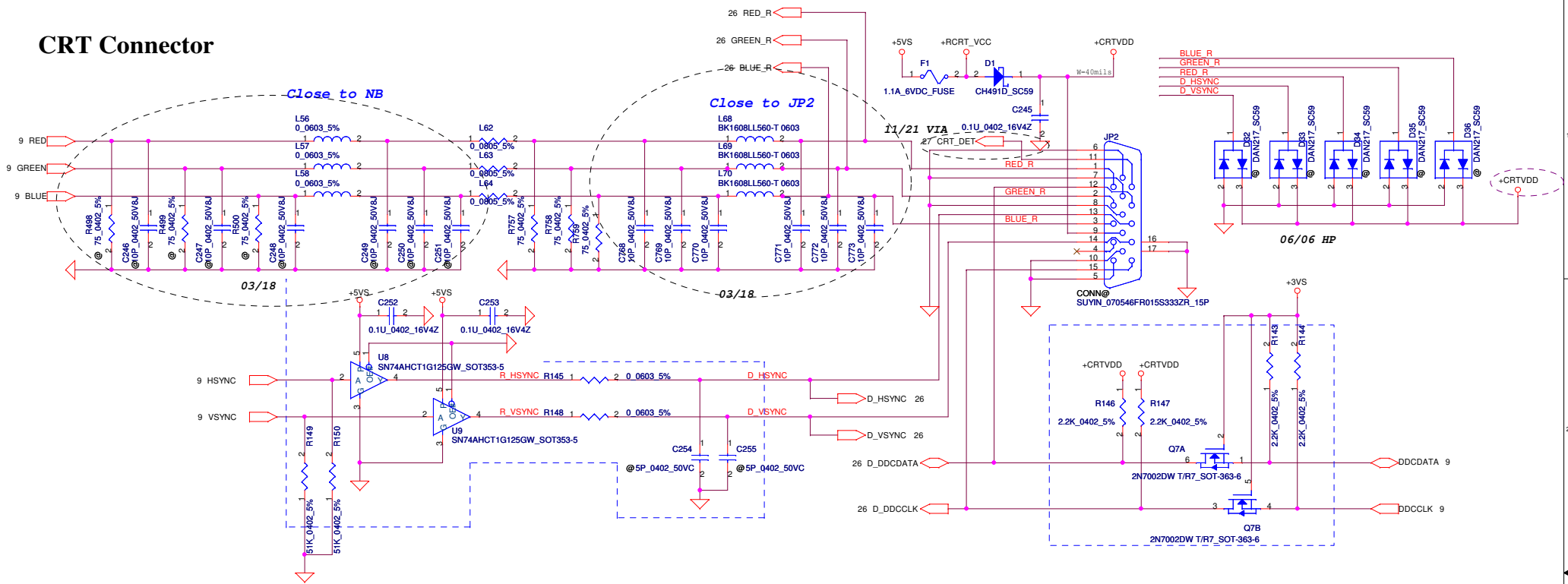
# Clock Generator



FSL2	FSL1	FSL0	CPU	SRC	PCI	REF	USB
*1	*0	*1	100.00	100.00	33.33	14.318	48.000
0	1	0	200.00	100.00	33.33	14.318	48.000

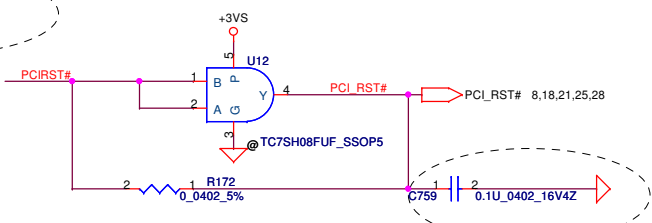
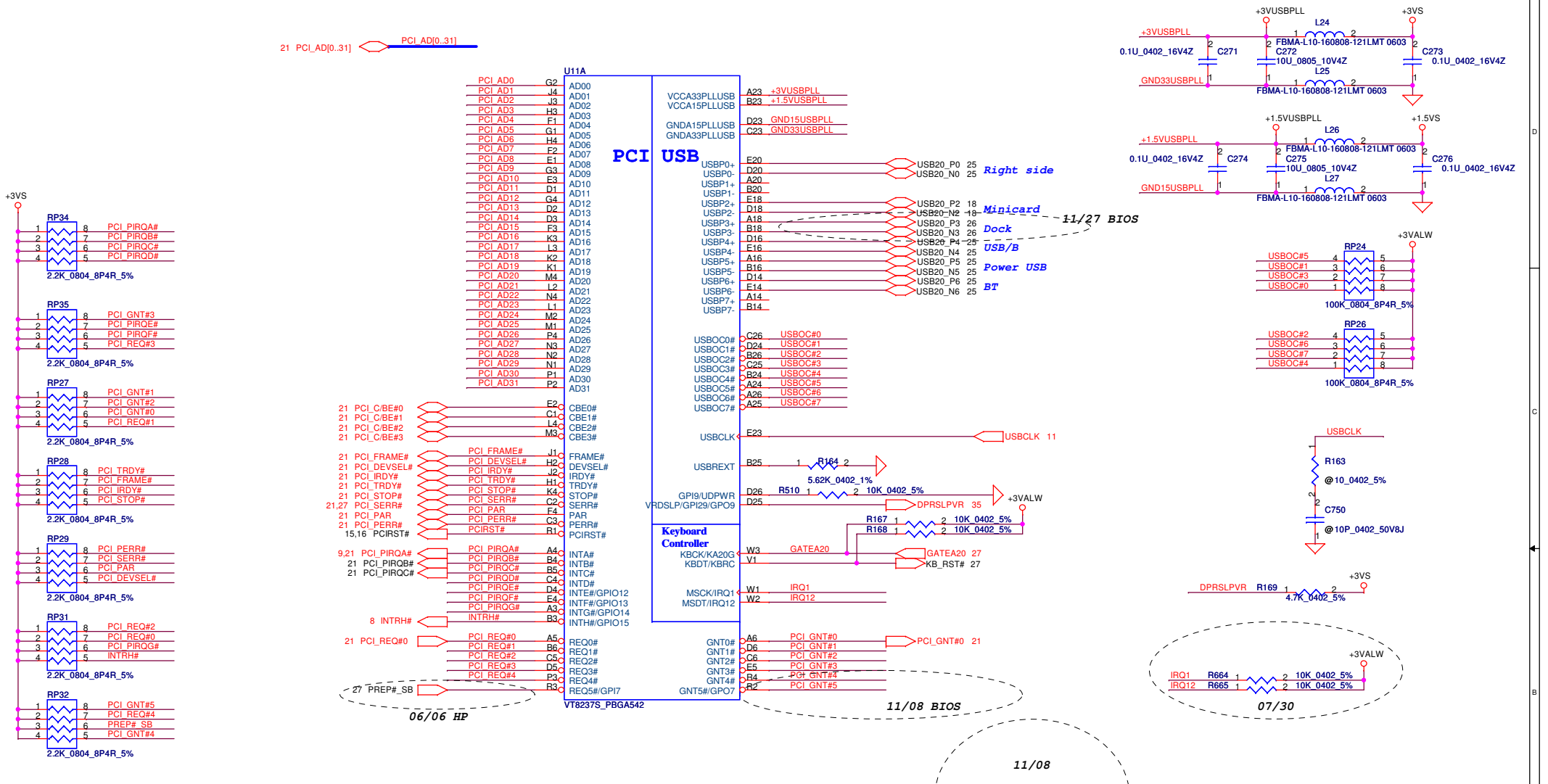
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# CRT Connector

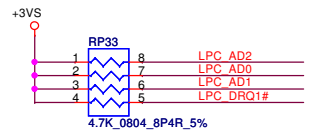
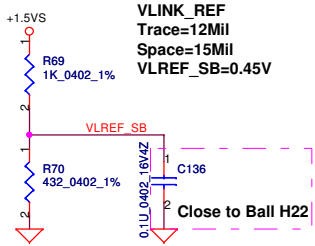
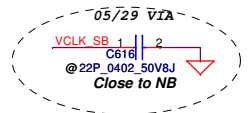


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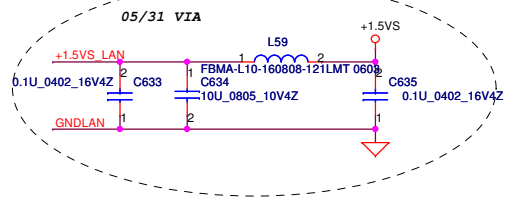
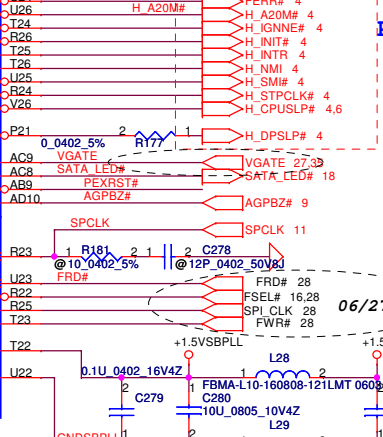
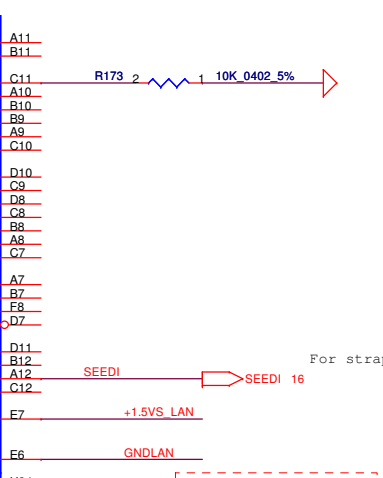
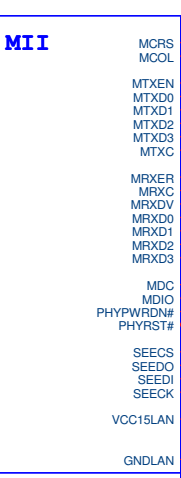
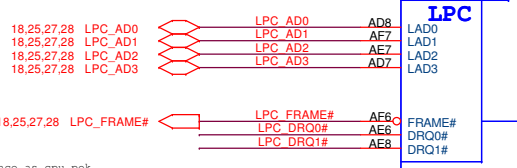
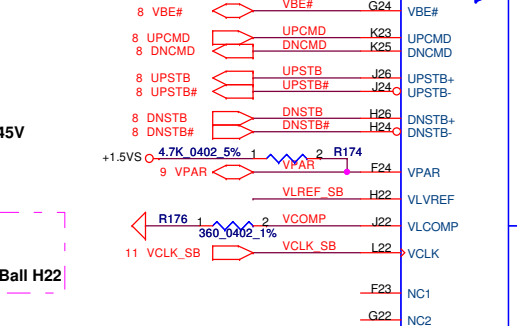
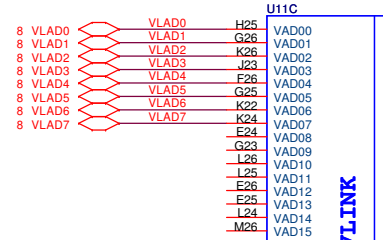
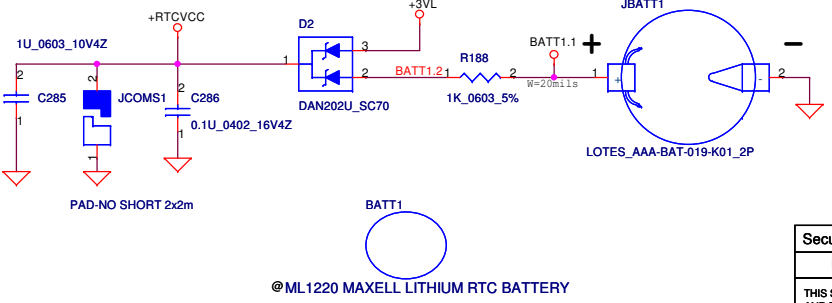
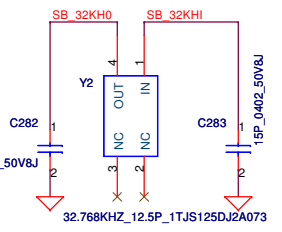
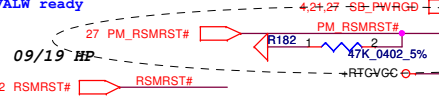


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Size	Document Number	Rev		1.0	
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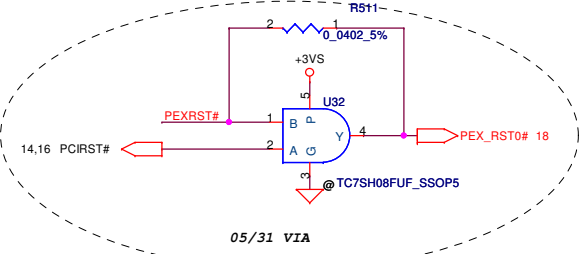
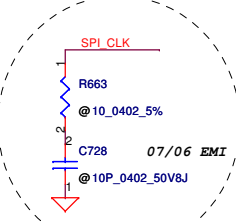
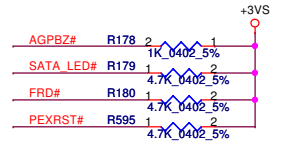


Control by EC  
Delay 50ms after +3VALW ready

The same power sequence as cpu\_pok



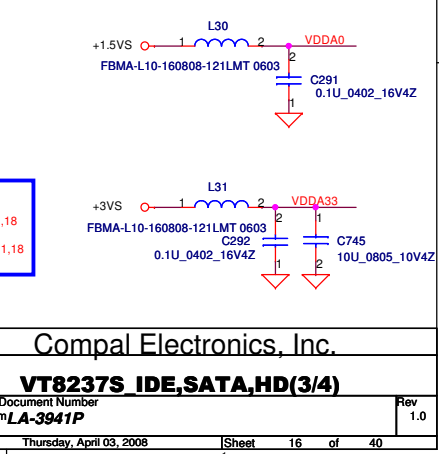
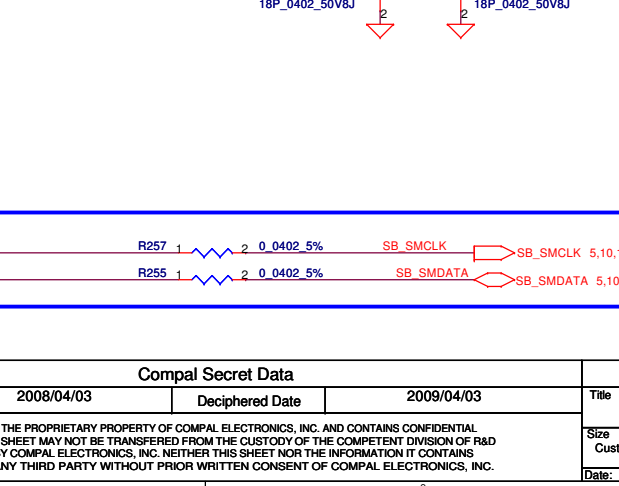
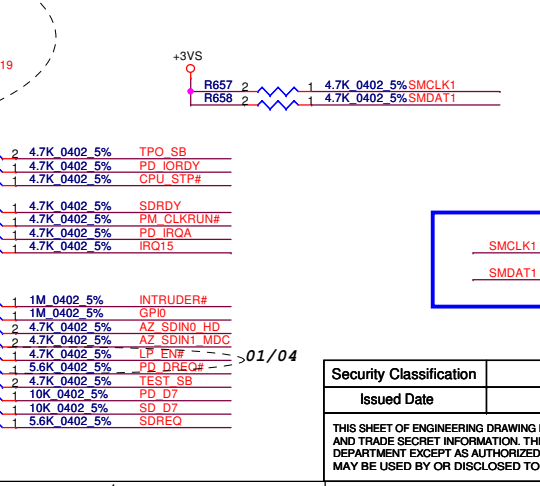
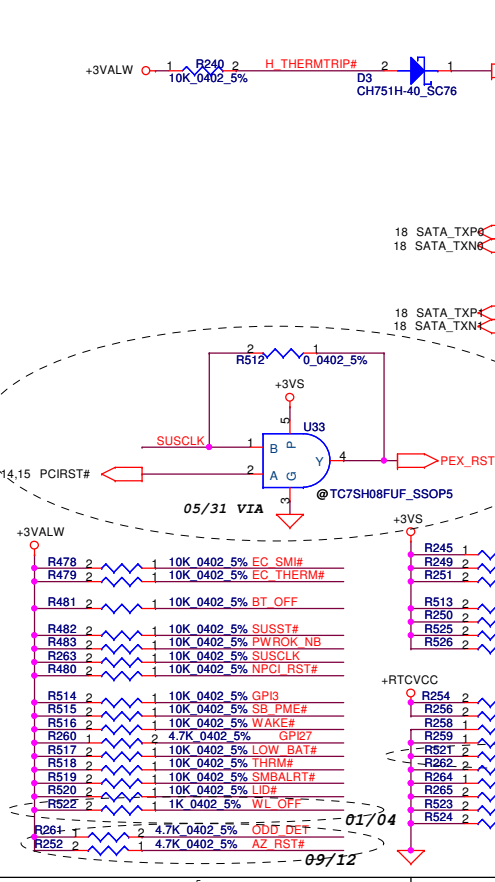
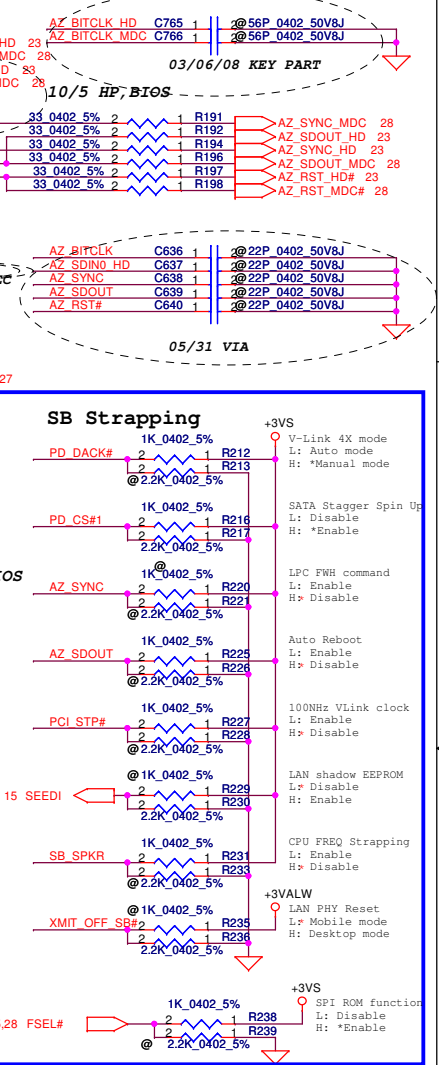
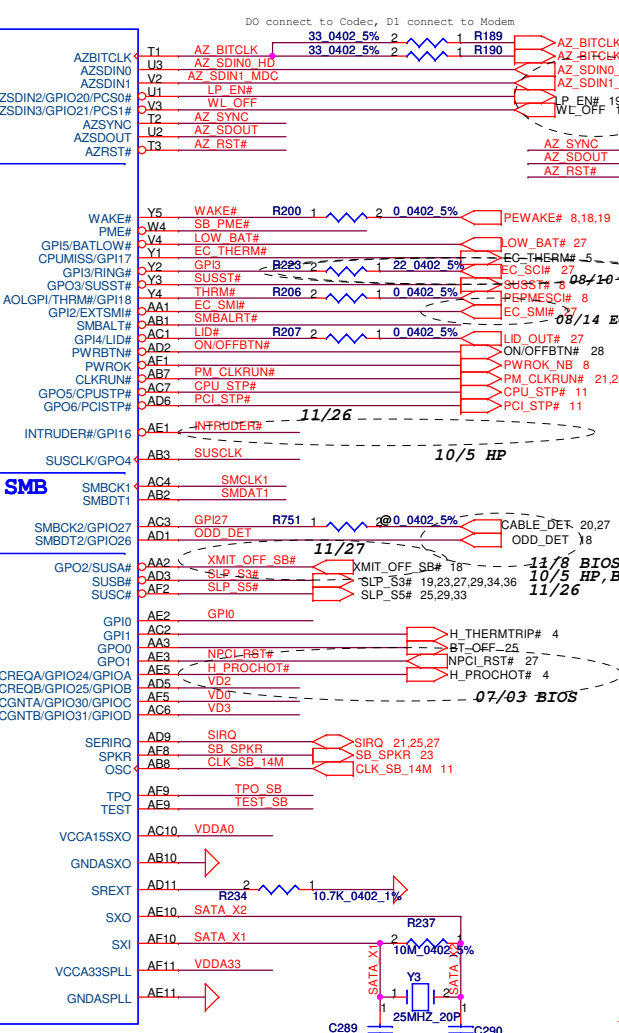
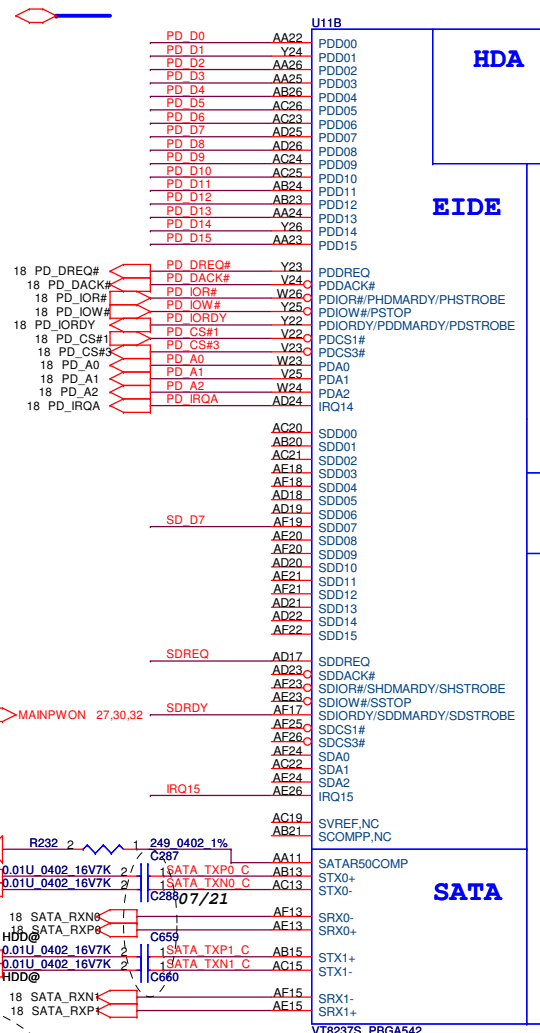
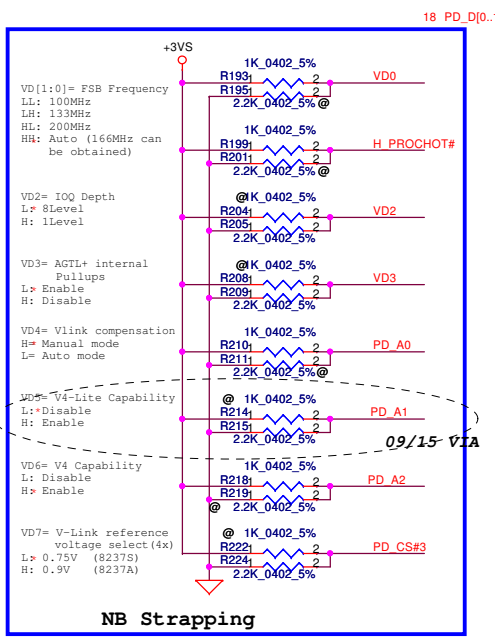
Pull-high on CPU side



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Title			
VT8237S_VL,LPC,CPU,LAN(2/4)			
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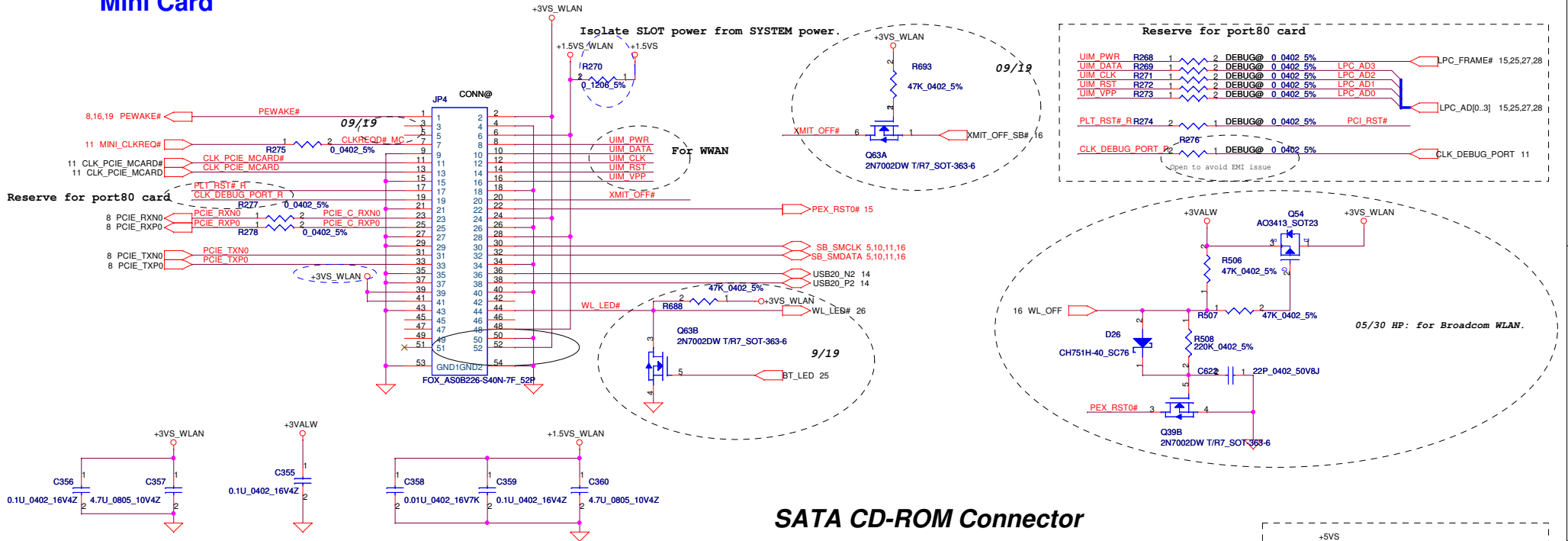


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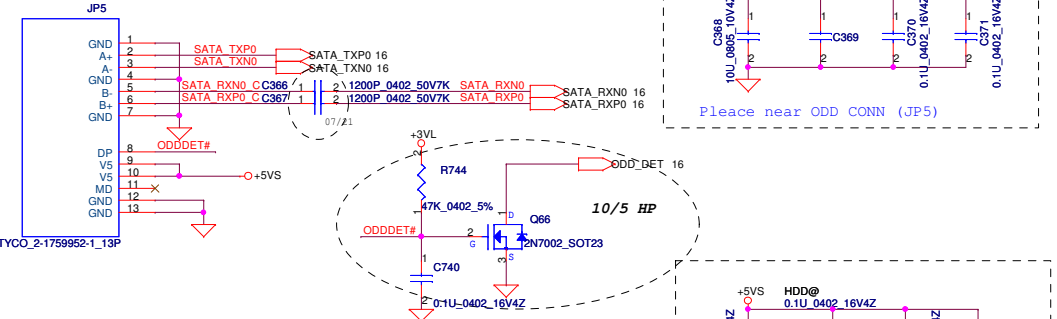
Compal Electronics, Inc.			
<b>VT8237S IDE,SATA,HD(3/4)</b>			
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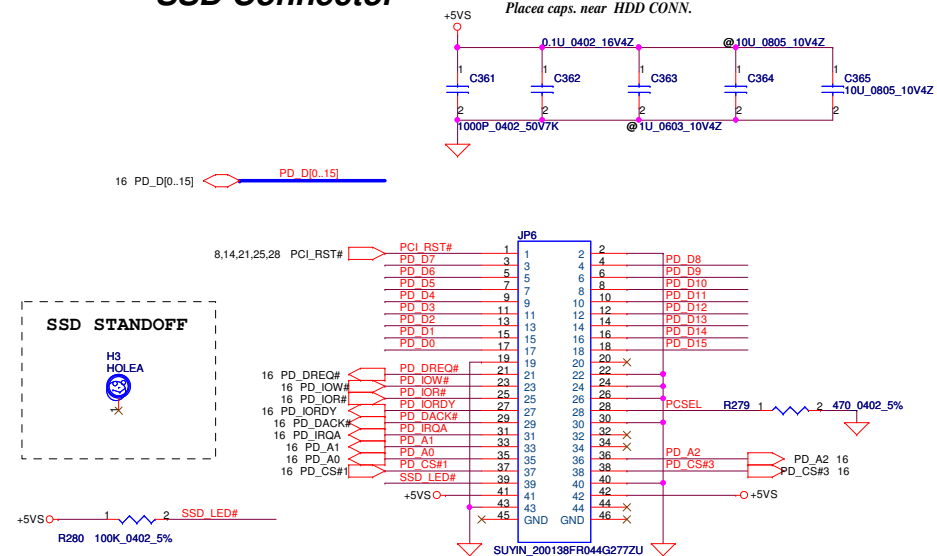
# Mini Card



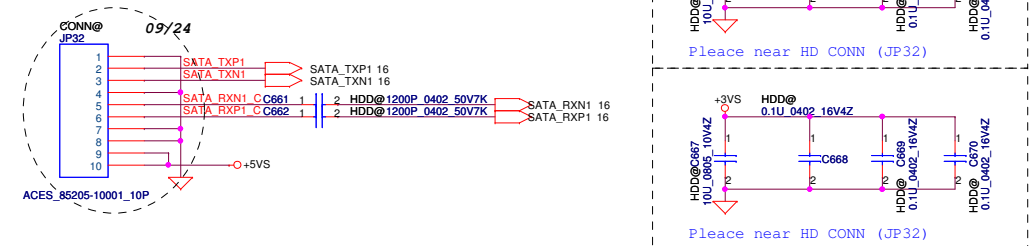
## SATA CD-ROM Connector



## SSD Connector

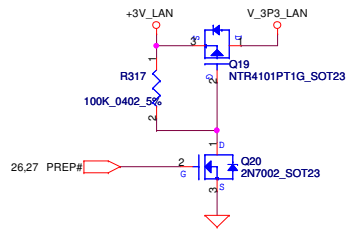
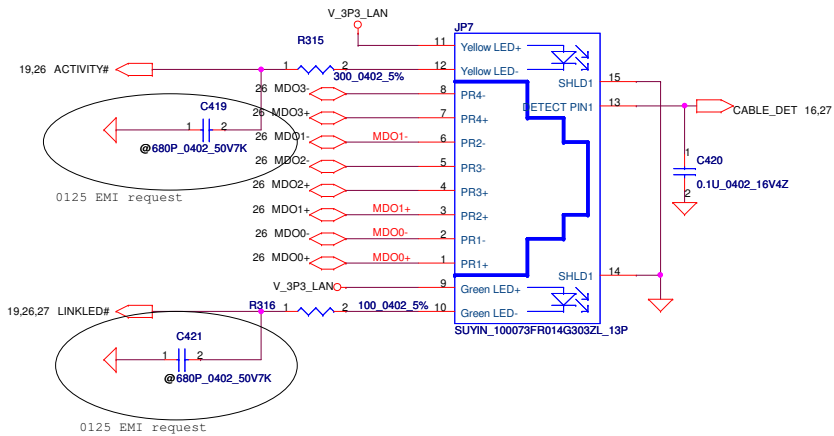
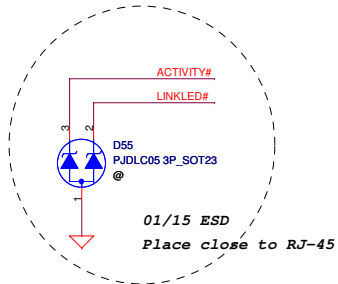
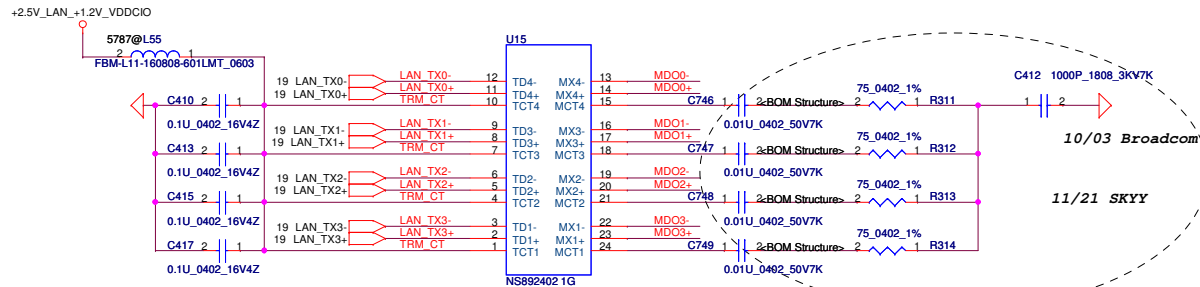


## 1.8" SATA HDD CONN

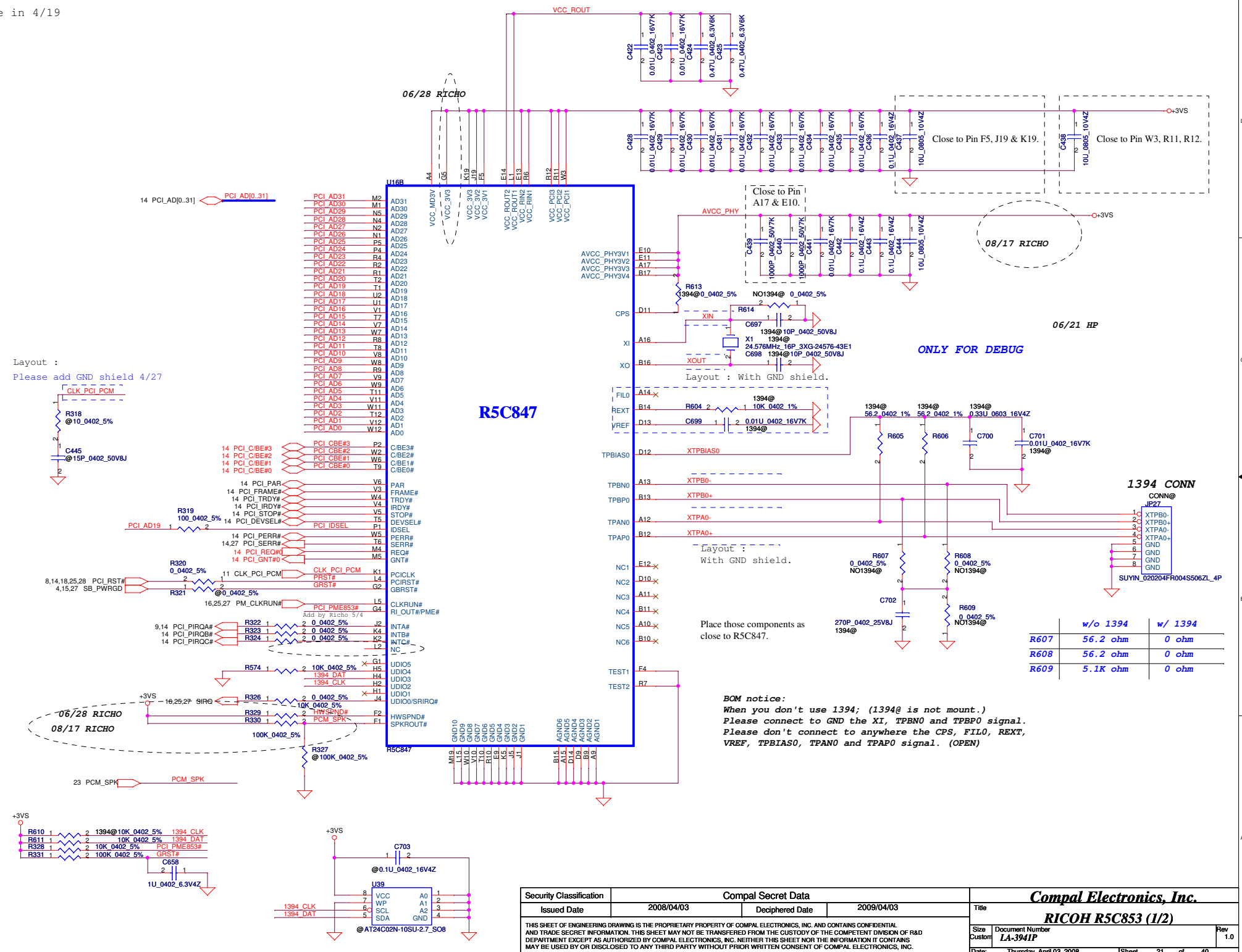


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Layout :  
Please add GND shield 4/27

ONLY FOR DEBUG

Place those components as close to R5C847.

**BOM notice:**  
When you don't use 1394; (1394@ is not mount.)  
Please connect to GND the XI, TPBNO and TPBP0 signal.  
Please don't connect to anywhere the CPS, FILO, REXT, VREF, TPBIAS0, TPANO and TPAP0 signal. (OPEN)

	w/o 1394	w/ 1394
R607	56.2 ohm	0 ohm
R608	56.2 ohm	0 ohm
R609	5.1K ohm	0 ohm

PCI AD31	M2	AD31
PCI AD30	M1	AD30
PCI AD29	N5	AD29
PCI AD28	N4	AD28
PCI AD27	N2	AD27
PCI AD26	N1	AD26
PCI AD25	P5	AD25
PCI AD24	P4	AD24
PCI AD23	R4	AD23
PCI AD22	R2	AD22
PCI AD21	R1	AD21
PCI AD20	T2	AD20
PCI AD19	U2	AD19
PCI AD18	T1	AD18
PCI AD17	U1	AD17
PCI AD16	V1	AD16
PCI AD15	T7	AD15
PCI AD14	V7	AD14
PCI AD13	W7	AD13
PCI AD12	R8	AD12
PCI AD11	T8	AD11
PCI AD10	V8	AD10
PCI AD9	W8	AD9
PCI AD8	R9	AD8
PCI AD7	V9	AD7
PCI AD6	W9	AD6
PCI AD5	V7	AD5
PCI AD4	V11	AD4
PCI AD3	W11	AD3
PCI AD2	T12	AD2
PCI AD1	V12	AD1
PCI AD0	W12	AD0

PCI CBE#3	P2	C/BE#3
PCI CBE#2	W2	C/BE#2
PCI CBE#1	W6	C/BE#1
PCI CBE#0	T9	C/BE#0

PCI PAR	V3	PAR
PCI FRAME#	W4	FRAME#
PCI TRDY#	W4	TRDY#
PCI IRDY#	V4	IRDY#
PCI STOP#	V5	STOP#
PCI DEVSEL#	T5	DEVSEL#
PCI IDSEL	P1	IDSEL#
PCI PERR#	W5	PERR#
PCI SERR#	T6	SERR#
PCI REQ#	M4	REQ#
PCI GNT#	M5	GNT#

PCI PME#	L5	CLKRUN#
PRST#	G2	PRST#
GRST#	G2	GRST#
CLK_PCI_PCM	K1	CLK_PCI_PCM
PM_CLKRUN#	G4	CLKRUN#

PCI INTA#	J2	INTA#
PCI INTB#	K4	INTB#
PCI INTC#	K2	INTC#
NC	L2	NC

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		2009/04/03

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RICOH R5C853 (1/2)		
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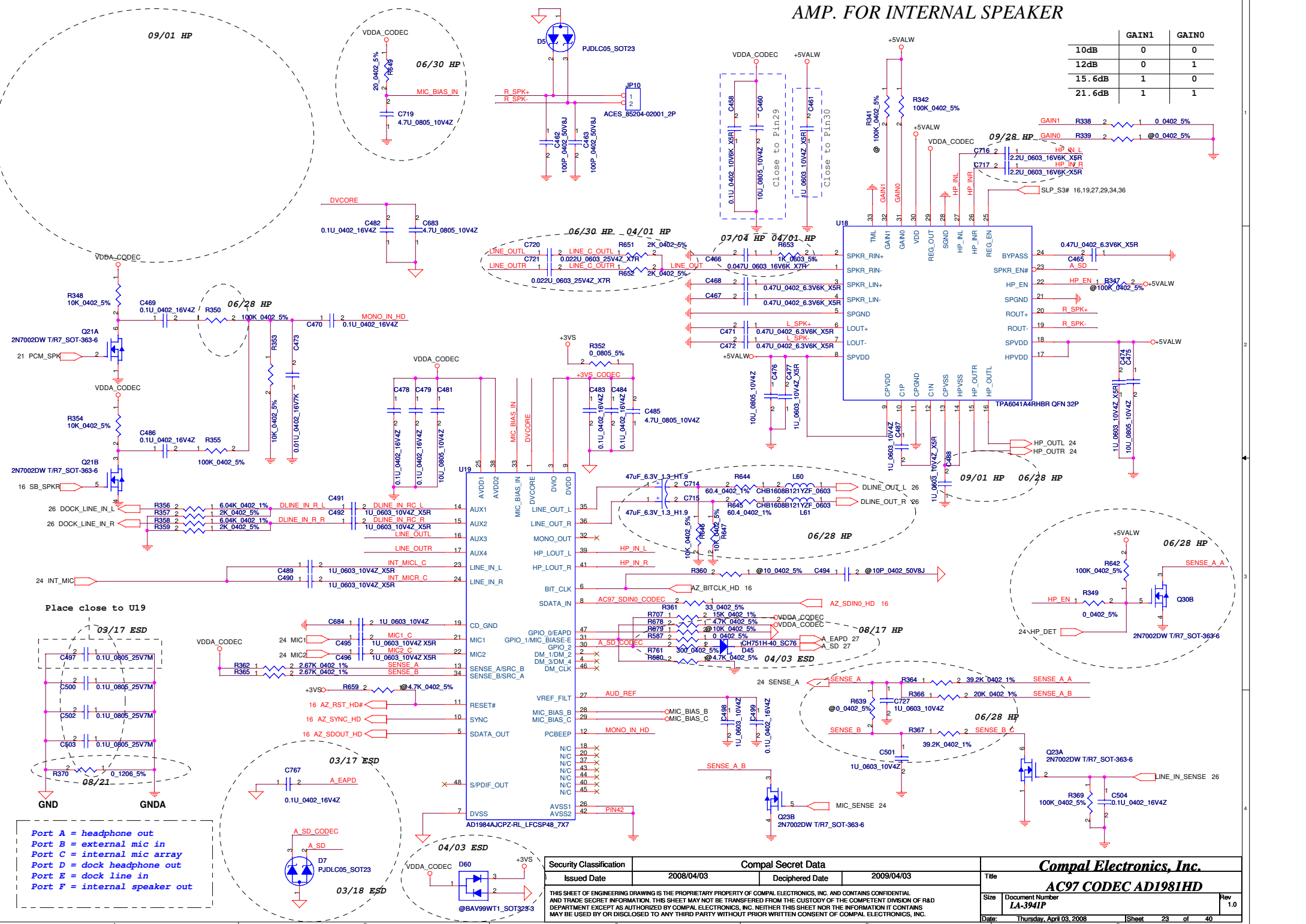






# AMP. FOR INTERNAL SPEAKER

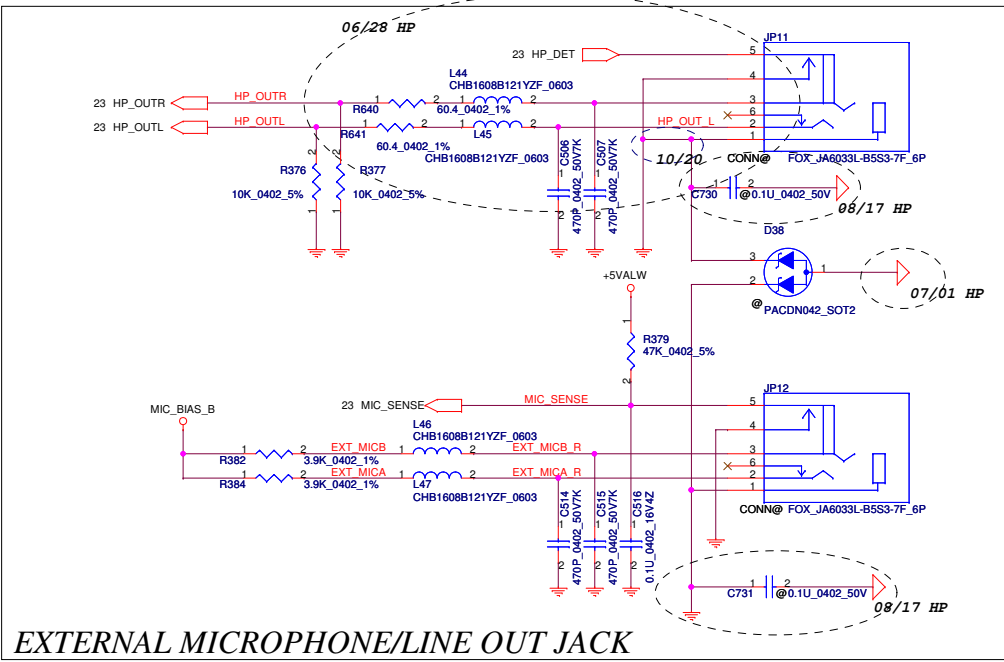
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10dB	0	0
12dB	0	1
15.6dB	1	0
21.6dB	1	1



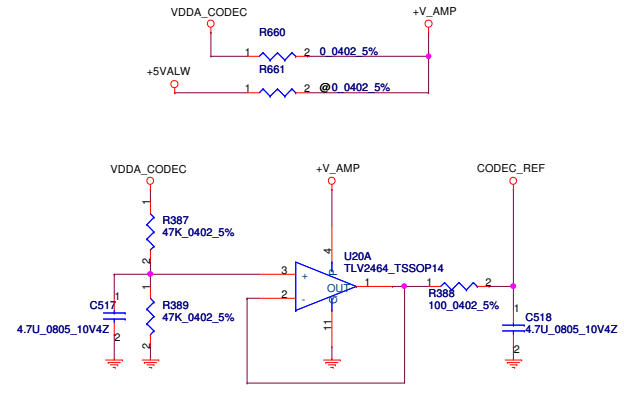
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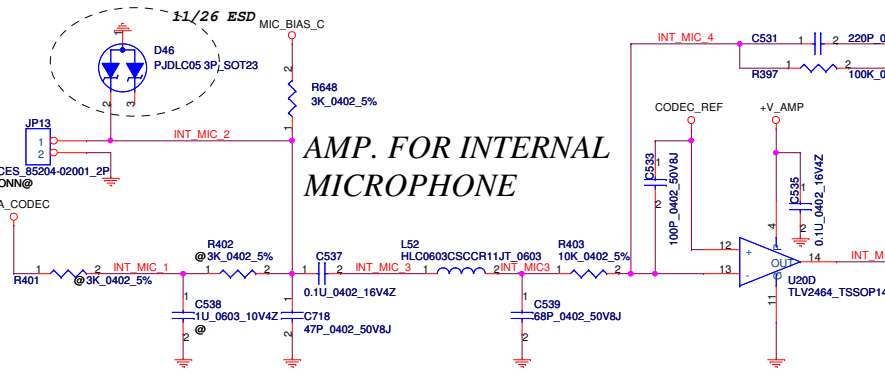
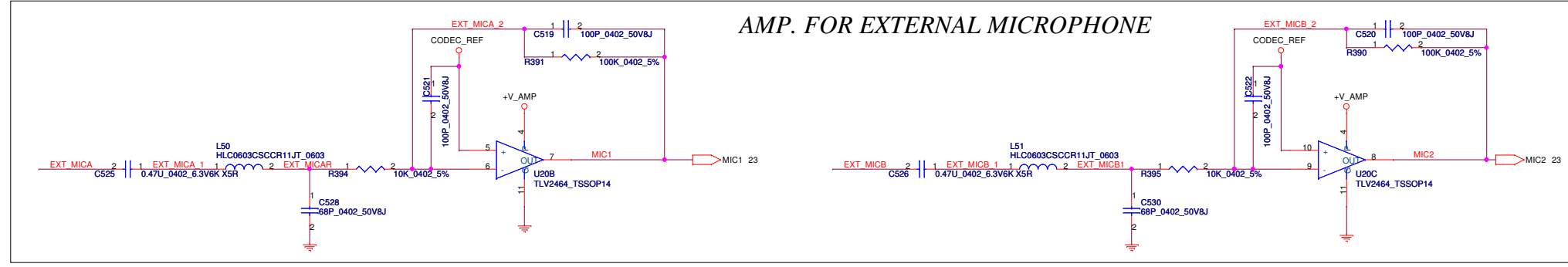
Title		
<b>Compal Electronics, Inc.</b> <b>AC97 CODEC AD1981HD</b>		
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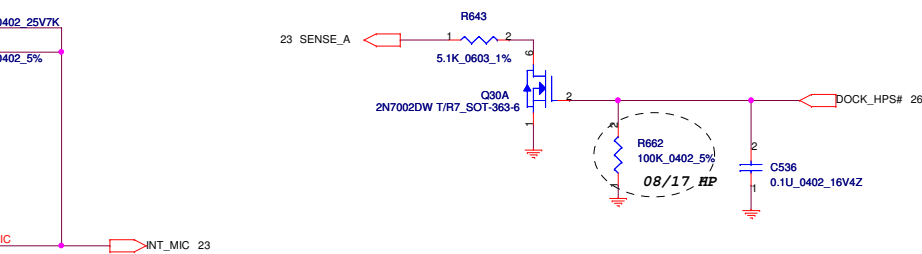
EXTERNAL MICROPHONE/LINE OUT JACK



AMP. FOR EXTERNAL MICROPHONE

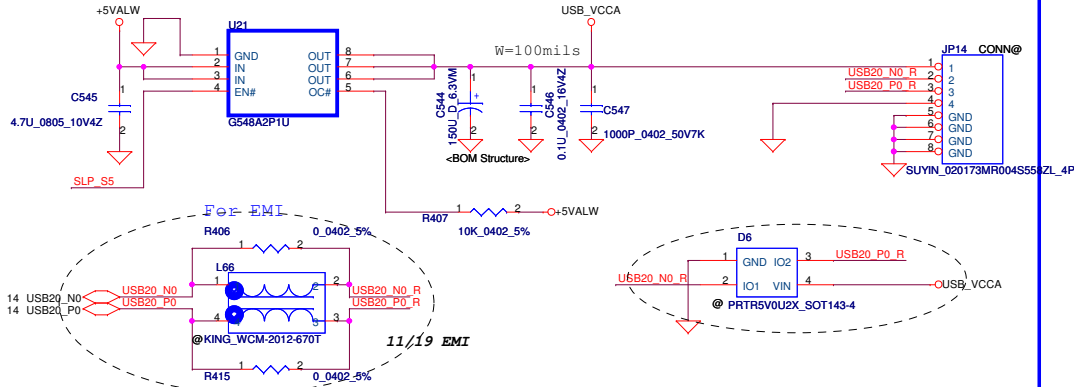


AMP. FOR INTERNAL MICROPHONE

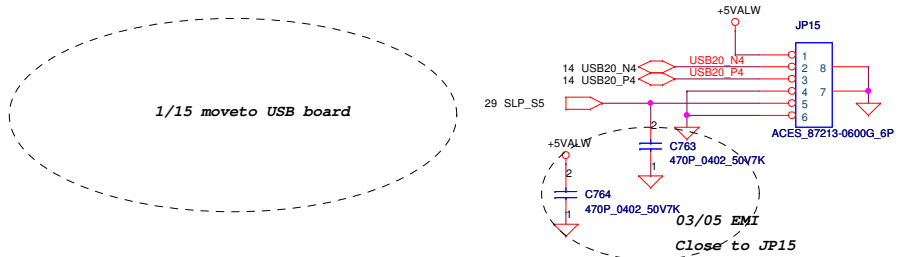


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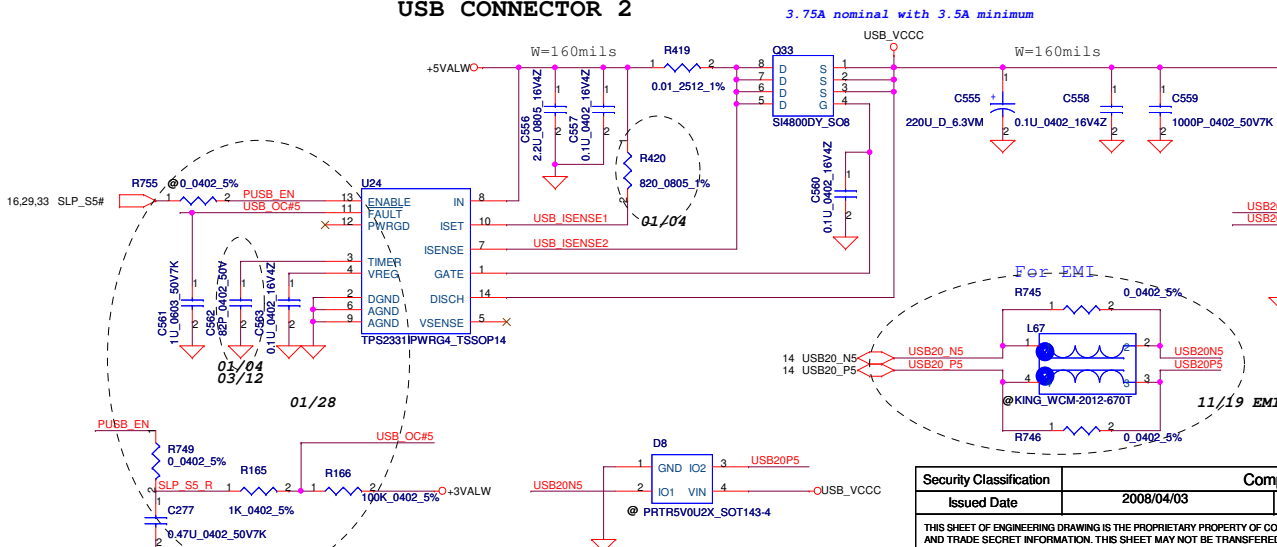
### USB CONNECTOR 0



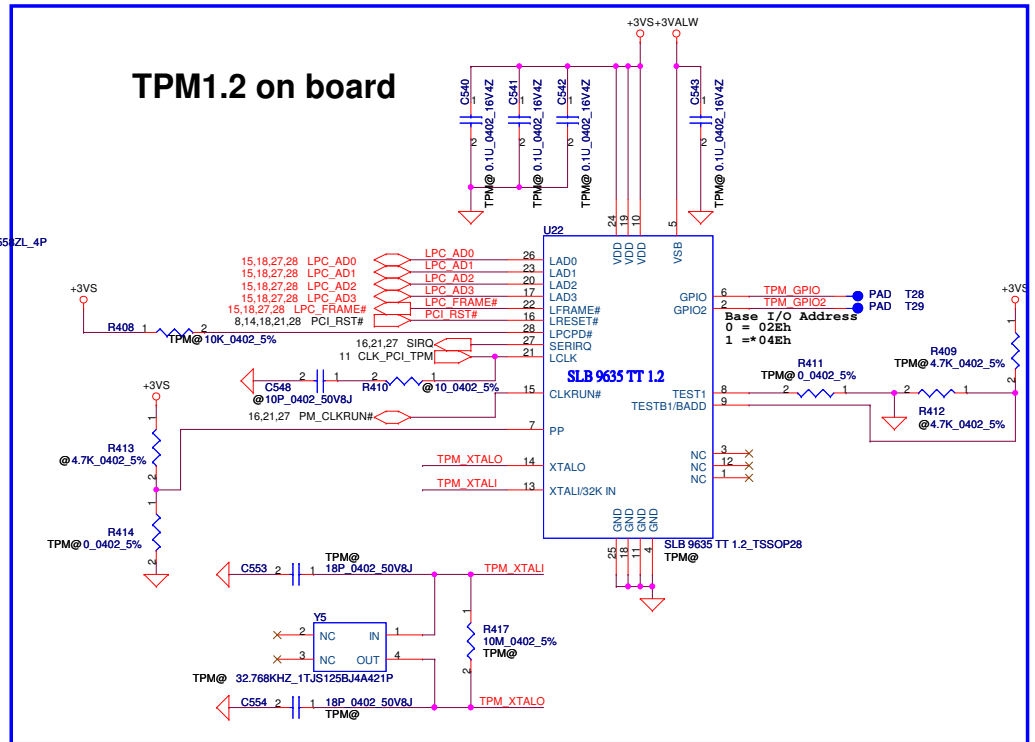
### USB/B CONNECTOR



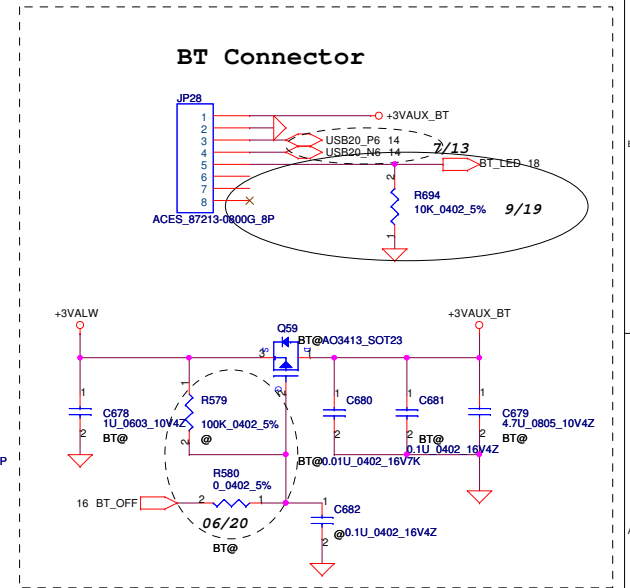
### USB CONNECTOR 2



### TPM1.2 on board

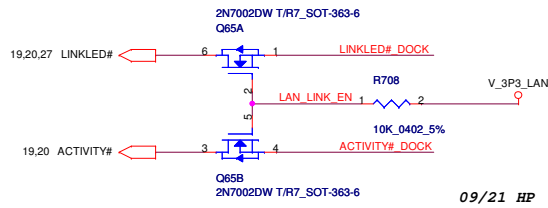
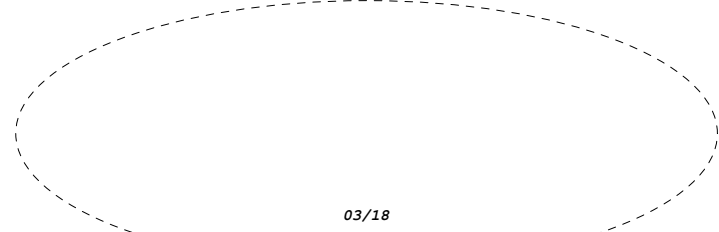
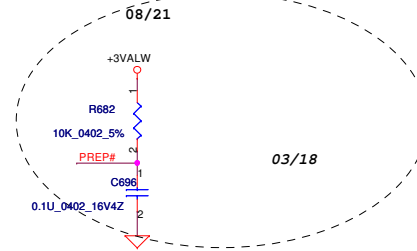
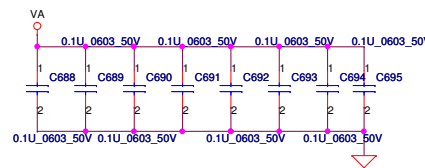
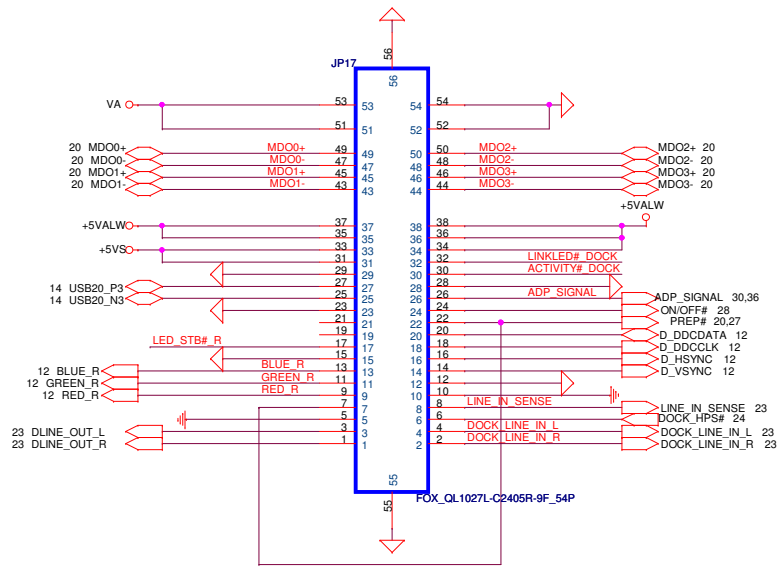


### BT Connector



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# DOCKING CONNECT

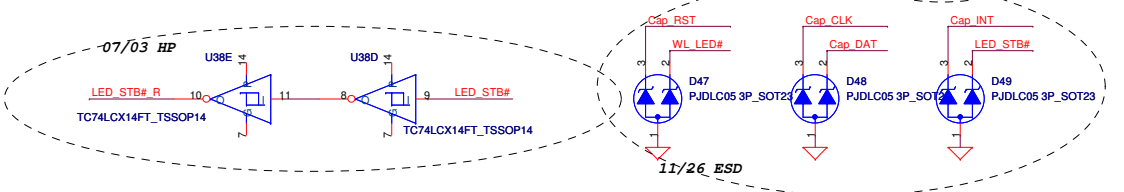
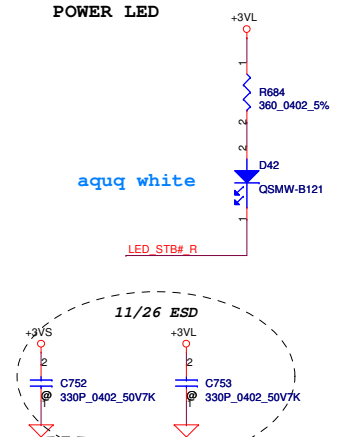
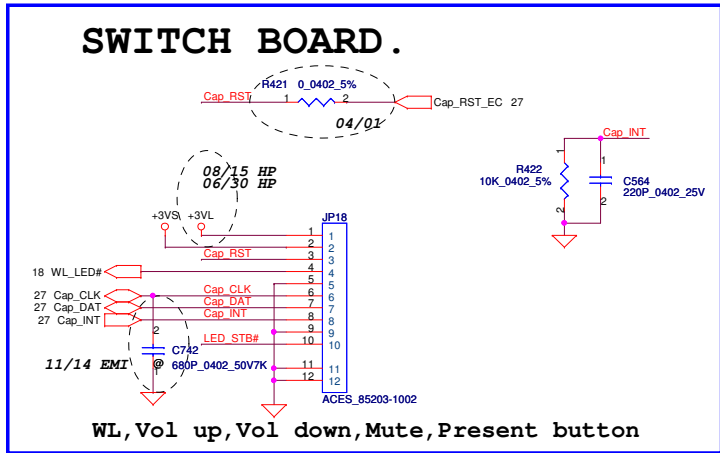
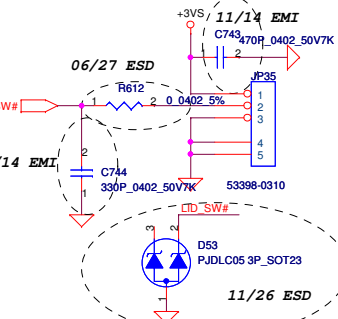
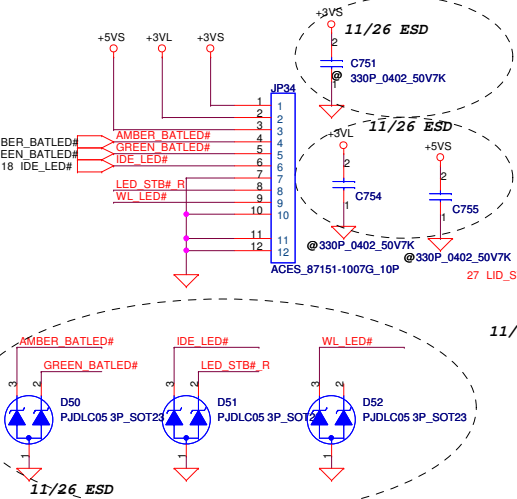


## LED BOARD.

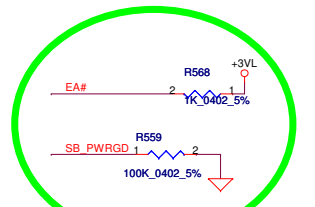
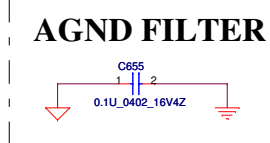
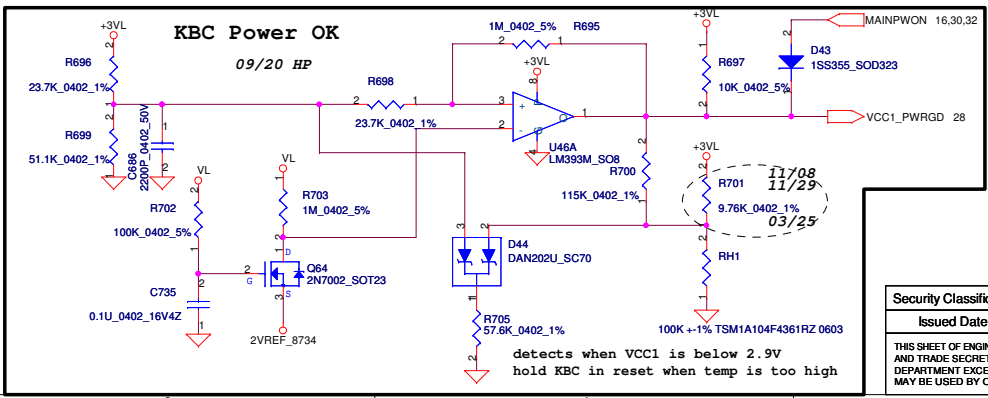
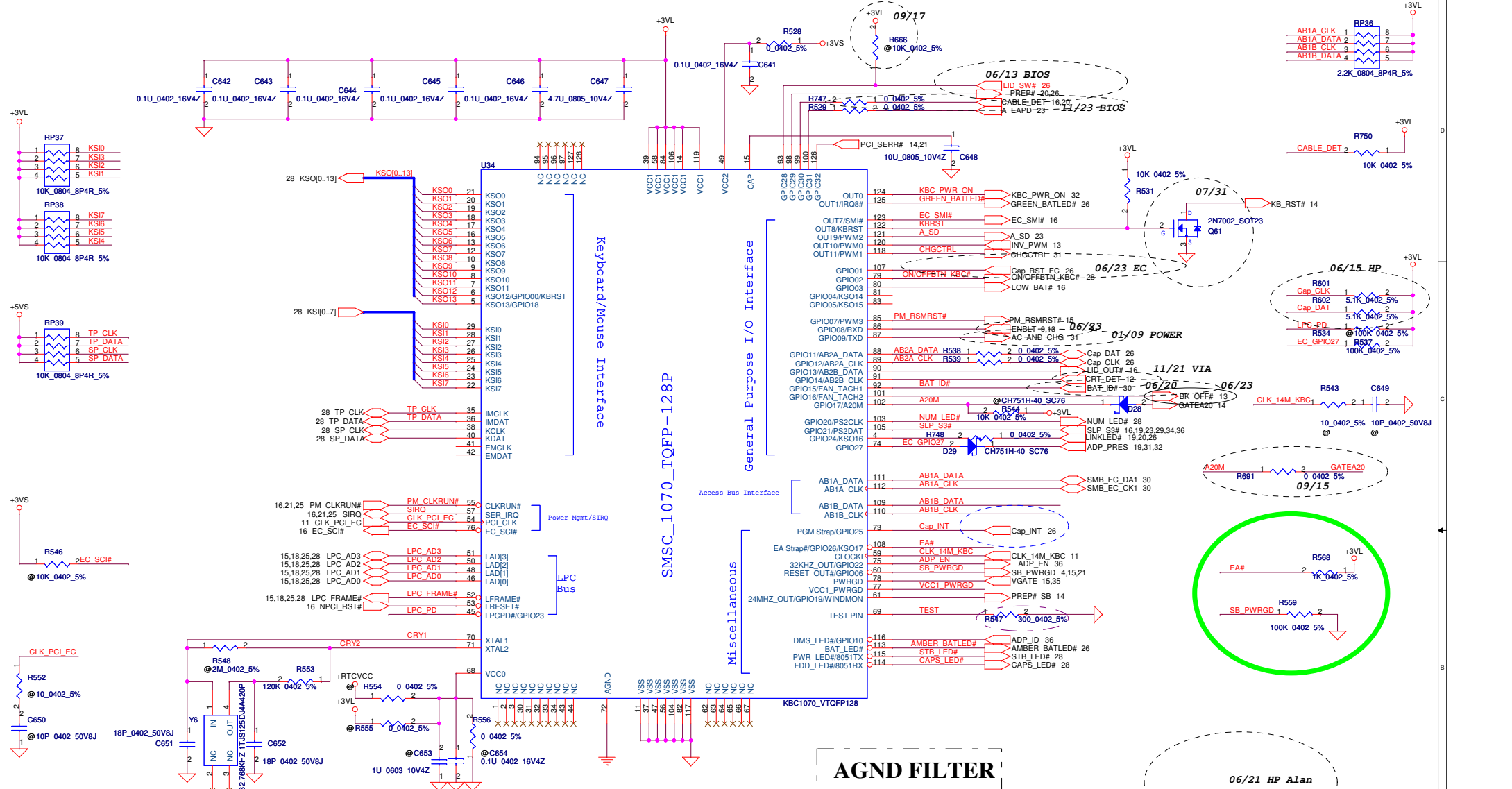
## LID SWITCH BOARD.

## SWITCH BOARD.

## POWER LED



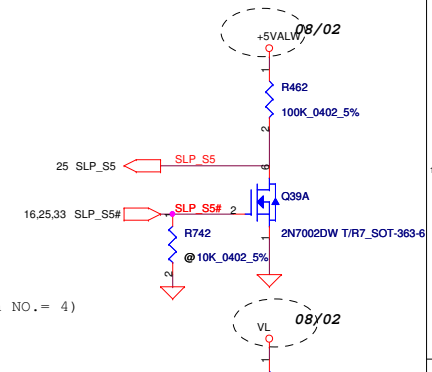
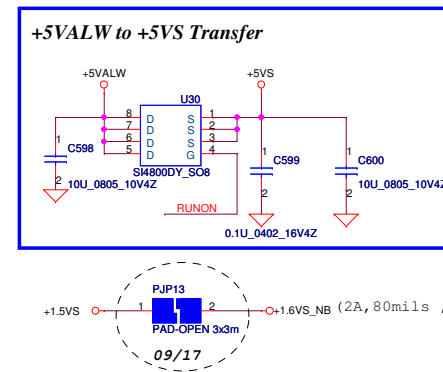
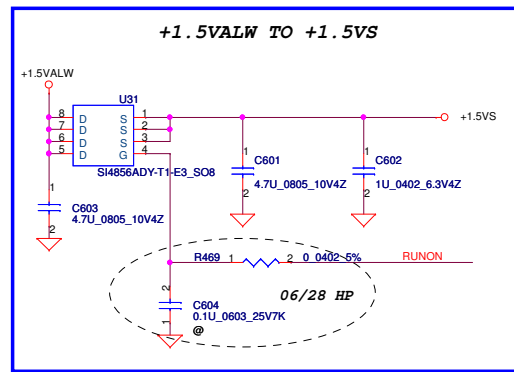
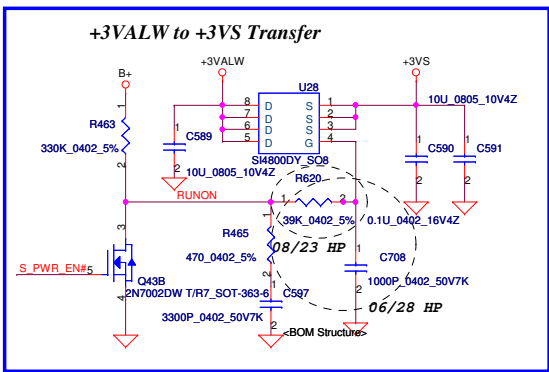
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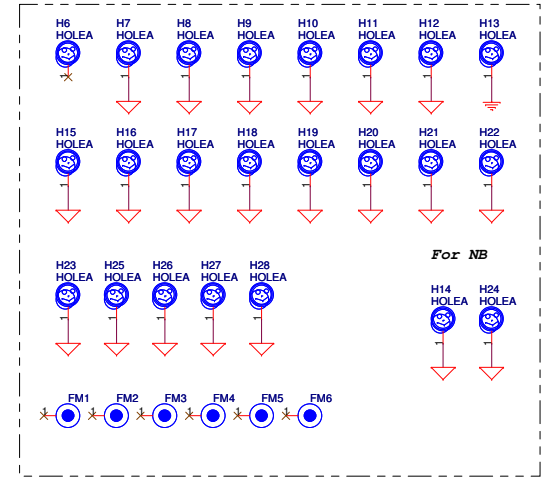
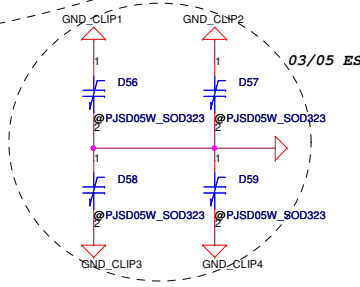
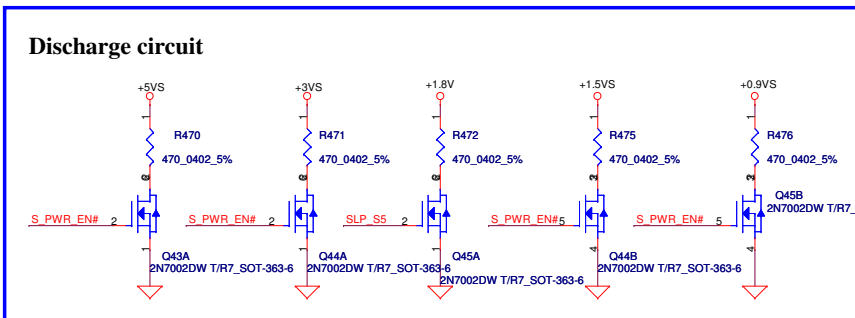
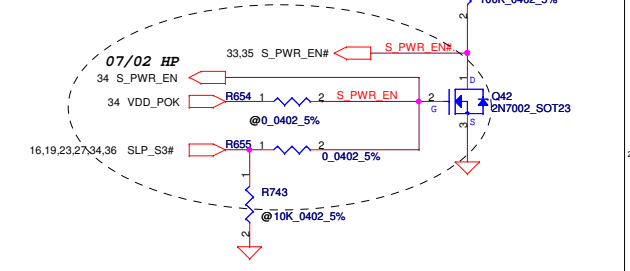
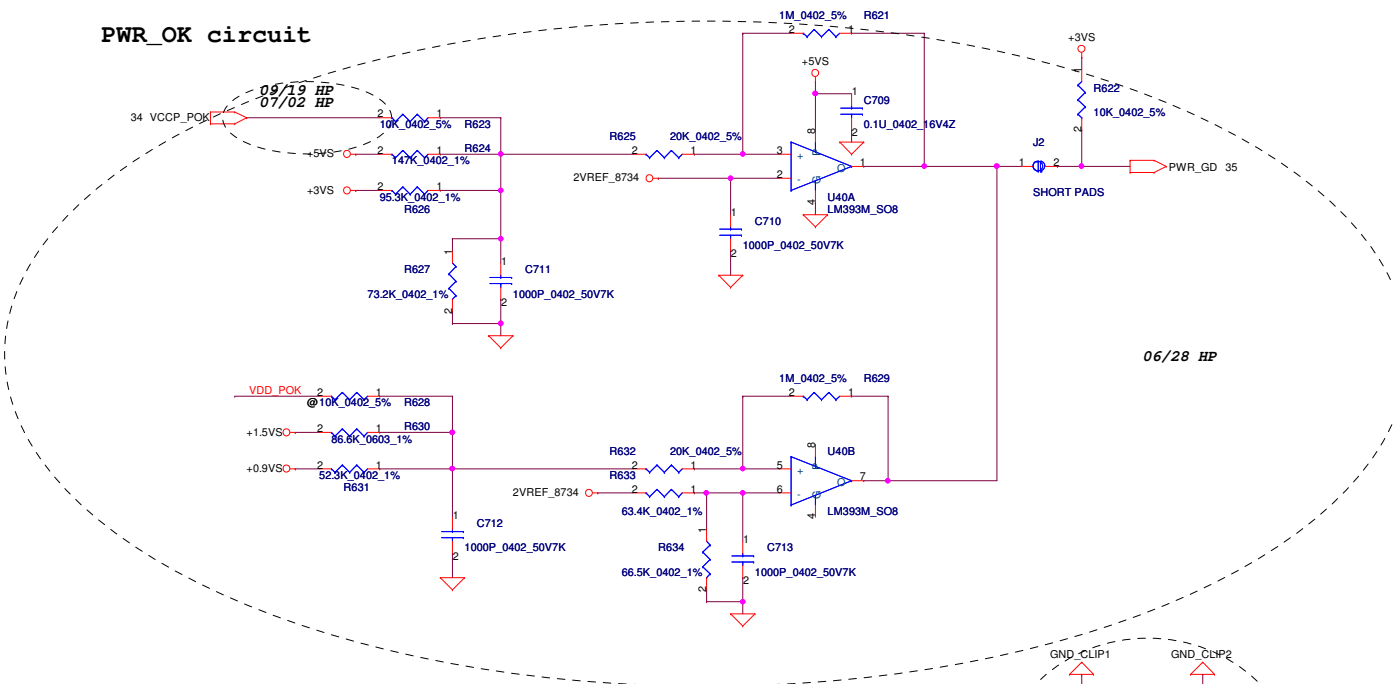
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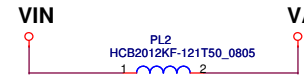
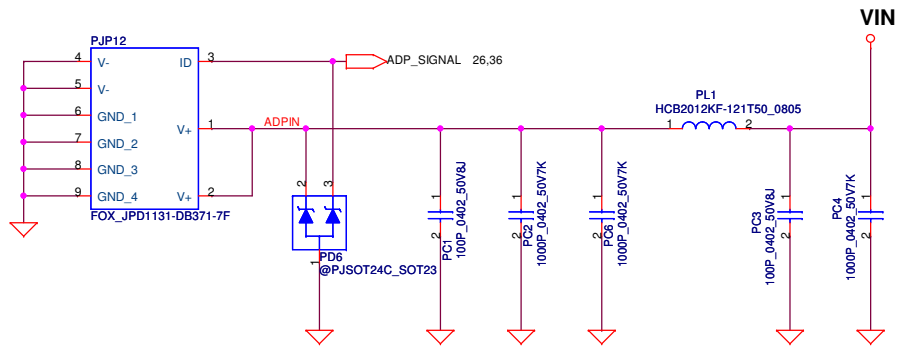


### PWR\_OK circuit

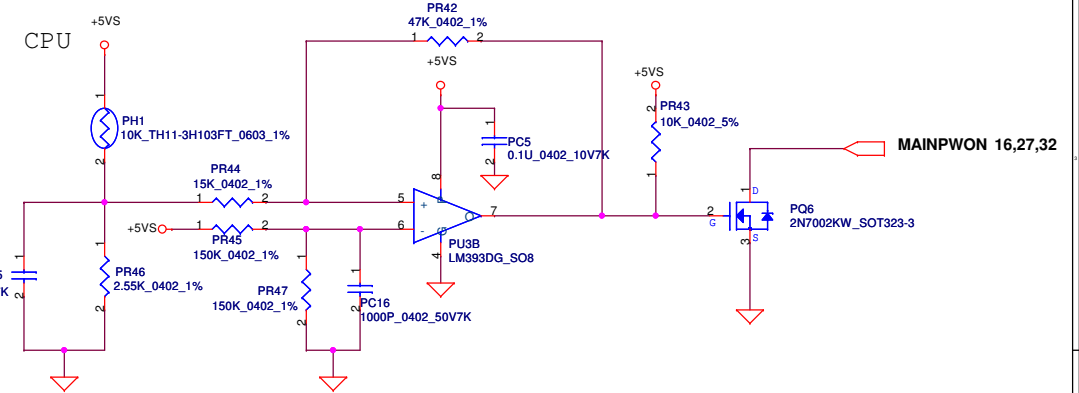
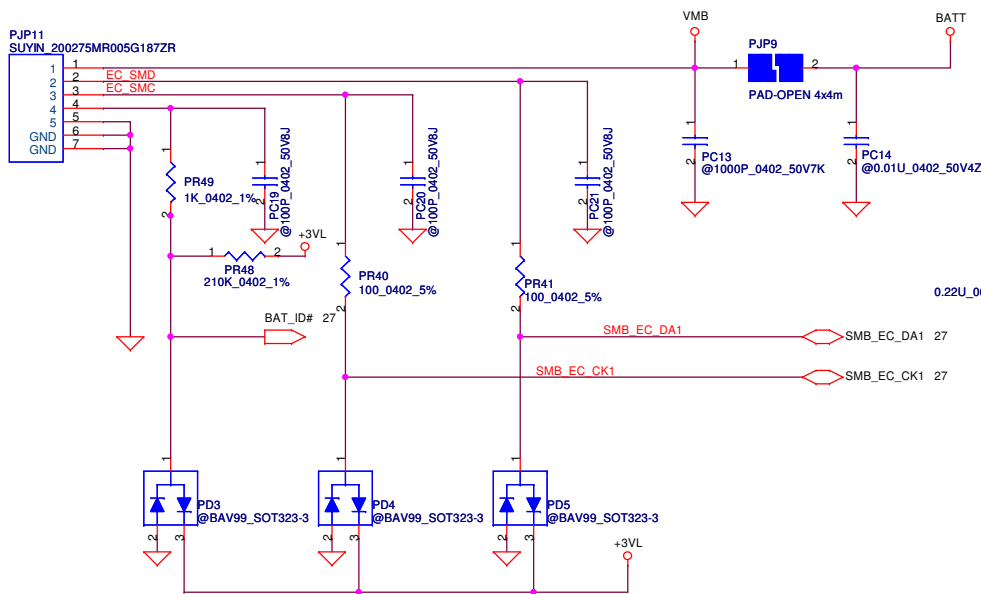


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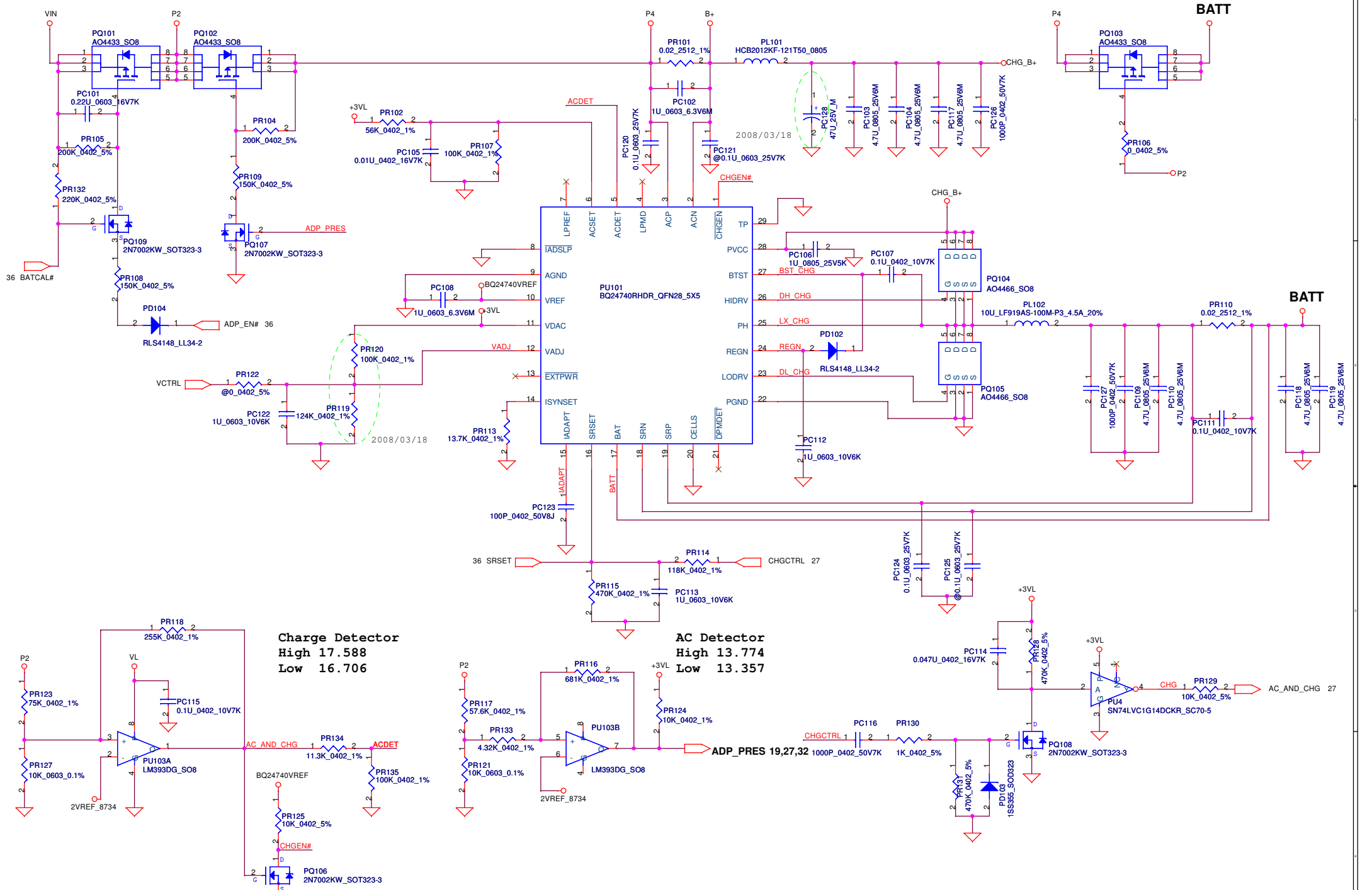




PH1 under CPU bottom side :  
 CPU thermal protection at 90 +/- 3 degree C  
 Recovery at 47 +/- 3 degree C



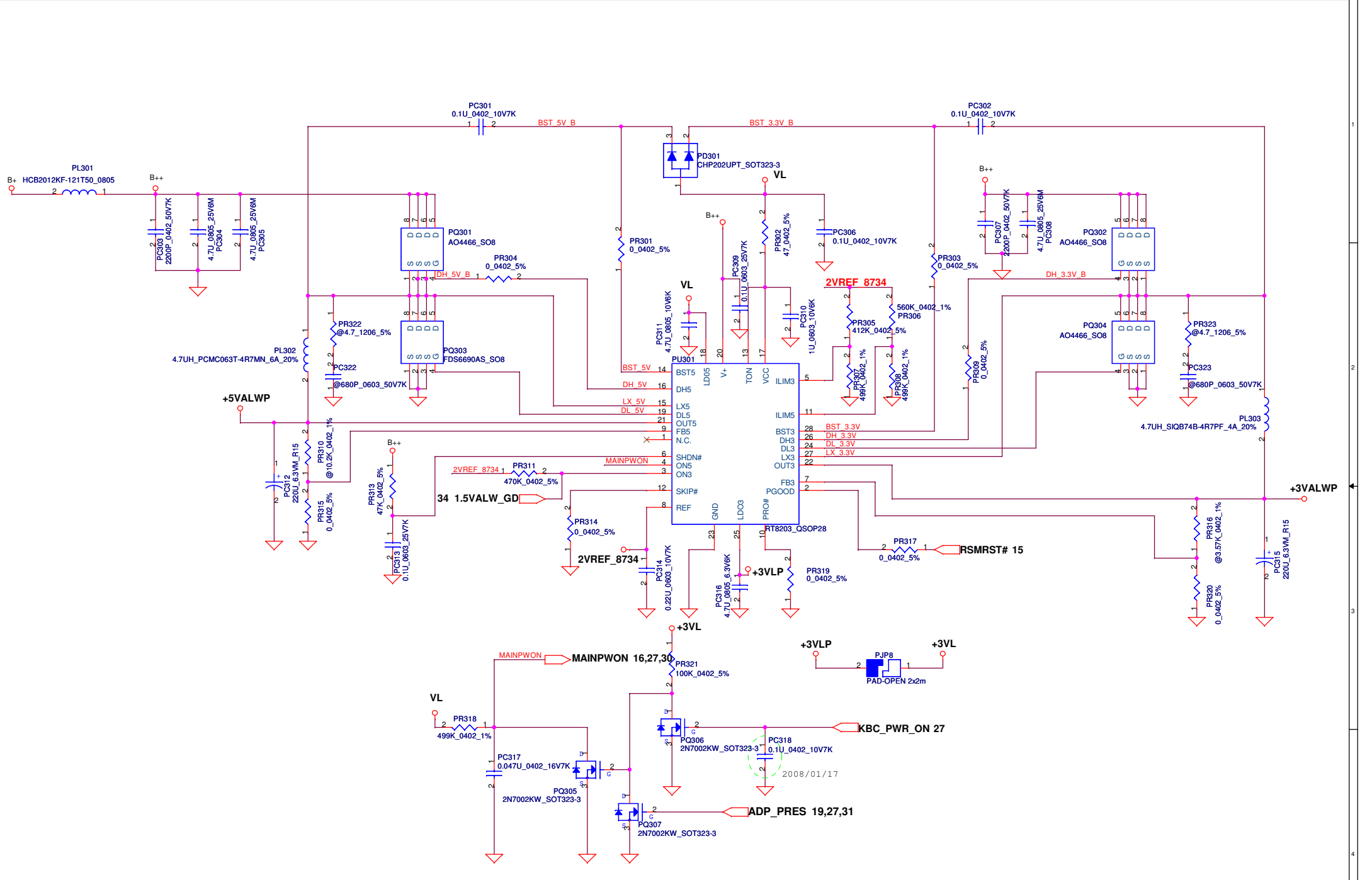
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Issued Date	2008/04/03	Deciphered Date	2009/04/03	DC Connector/CPU_OTP	
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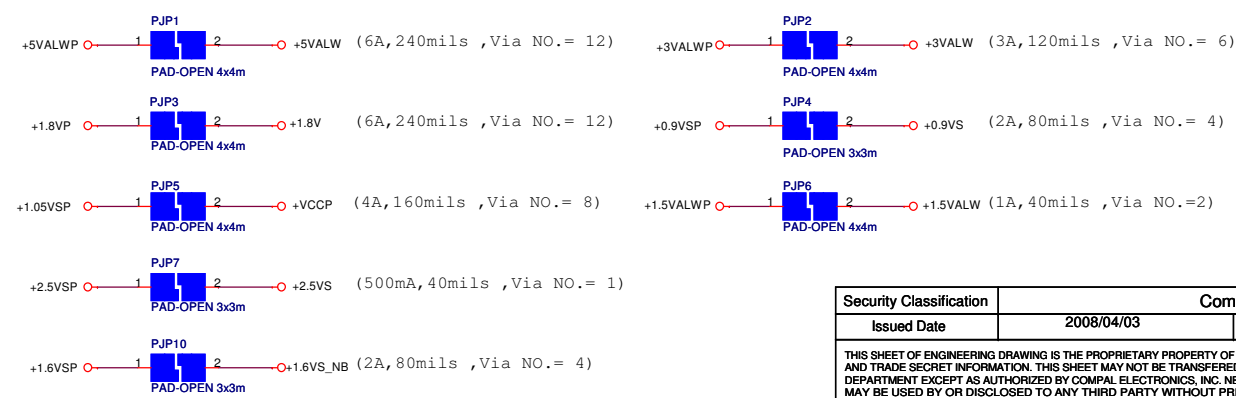
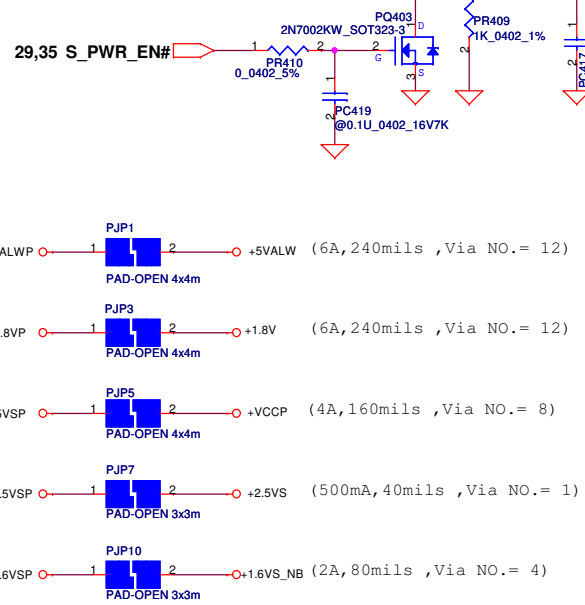
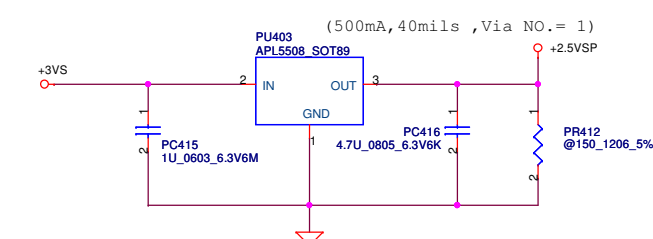
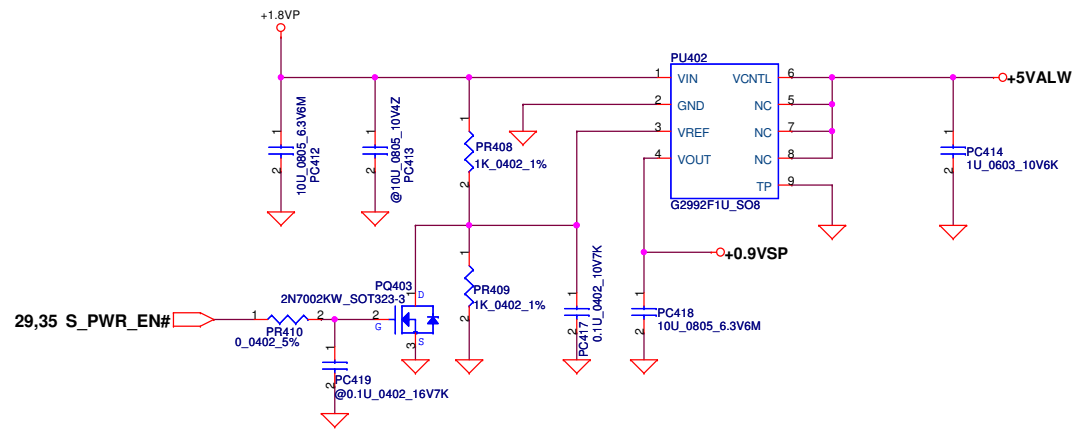
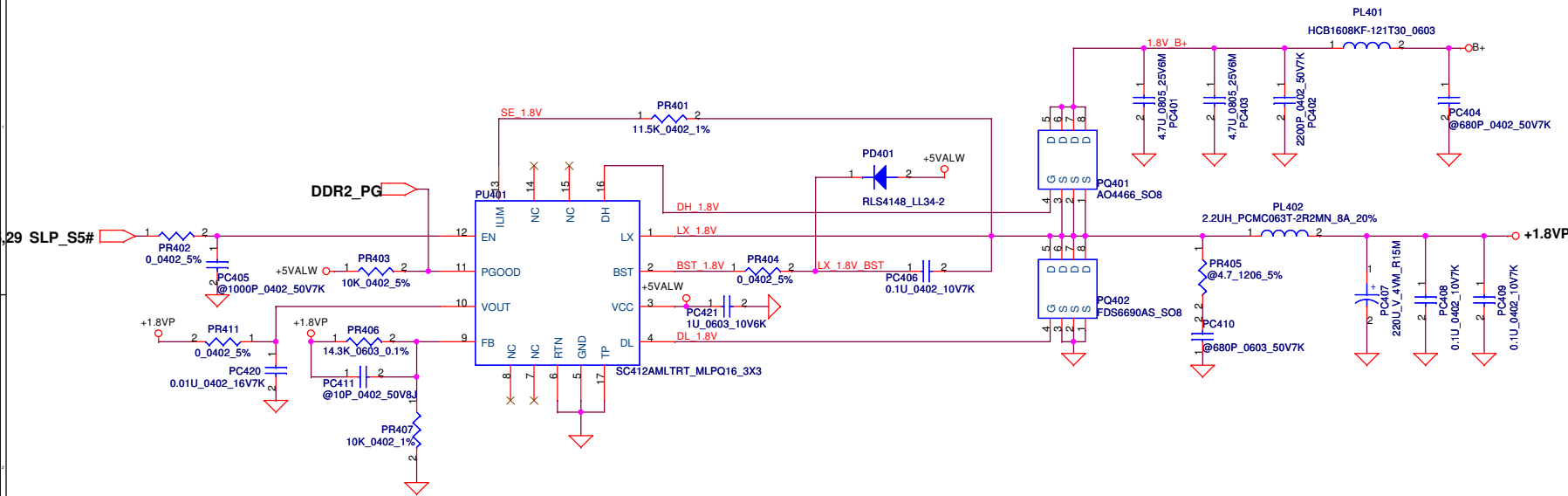
**Charge Detector**  
 High 17.588  
 Low 16.706

**AC Detector**  
 High 13.774  
 Low 13.357

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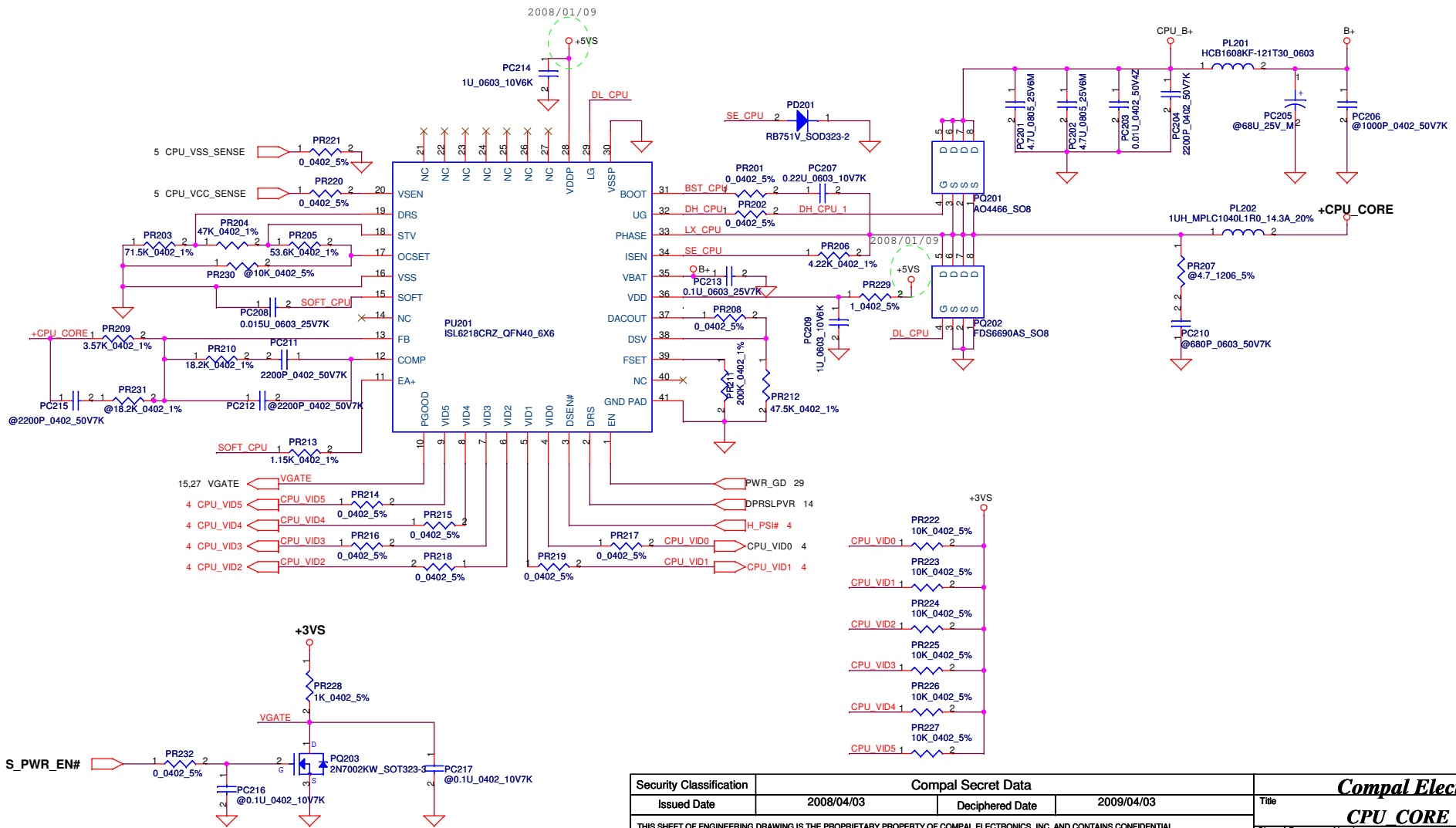


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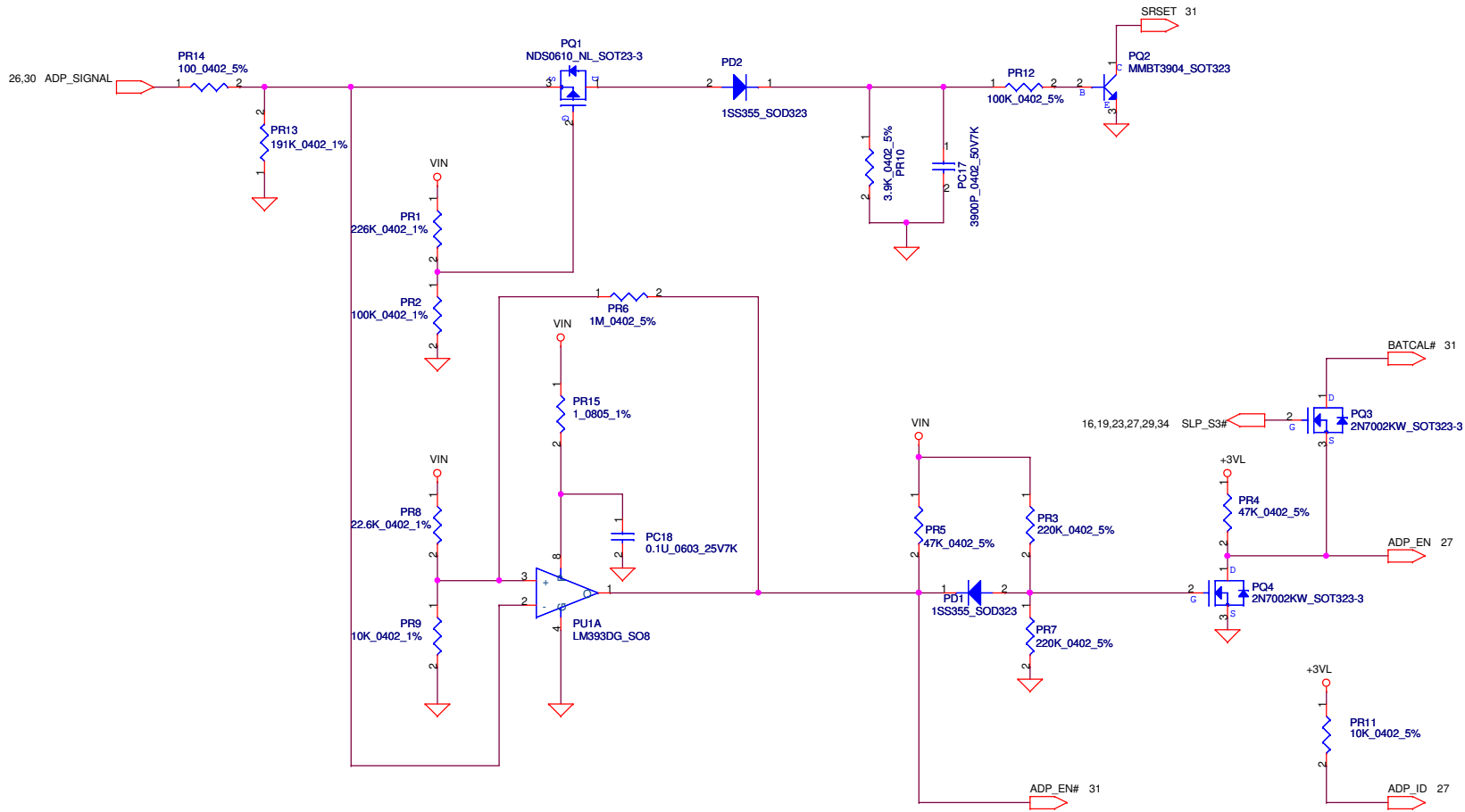


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Compal Electronics, Inc.

ADP OCP

LA-394IP

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# Version Change List (P. I. R. List) for Power Circuit (1)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	Page35	CPU_CORE	2007/06/13	Compal	Add VID pull high resistors	Add PR222-PR227 and connect to +3VS for VID0~5	PreDB-->DB1
2	Page36	ADP_OCP	2007/06/15	HP	Add ADP_OCP circuit	Add ADP_OCP circuit	PreDB-->DB1
3	Page32 Page34	3.3VALWP/5VALWP 1.05VSP/1.5VALWP/ 1.6VSP	2007/06/28	HP	Fine tune ALWP Power Sequence	5VALWP-->1.5VALWP-->3.3VALWP	PreDB-->DB1
4	Page35	CPU_CORE	2007/06/28	HP	Fine tune CPU_CORE Power Sequence	Change the EN of PU201 from VCCP_POK to PWR_GD	PreDB-->DB1
5	Page34	1.05VSP/1.5VALWP/ 1.6VSP	2007/06/28	HP	Fine tune +1.05VSP Power Sequence	Change PR514 from 0 to 20K Install PC514 as 0.1uf	PreDB-->DB1
6	Page31	Charger	2007/07/02	Compal	Fine tune the charger current contorl	Change PR114 from 2.49K to 24.9K Change PR115 from 10K to 100K Change PC113 from 0.01uf to luf	PreDB-->DB1
7	Page33	1.8VP/0.9VSP/ 2.5VSP	2007/07/02	Compal	Fine tune +0.9VSP Power Sequence	Change signal of PR410.1 from VDD_POK# to S_PWR_EN#	PreDB-->DB1
8	Page34	1.05VSP/1.5VALWP/ 1.6VSP	2007/07/02	HP	Install the pull high resistor and change the pull high level	Install PR516 as 10K Reconnect PR516.1 from +3VALW to +5VALW	PreDB-->DB1
9	Page34	1.05VSP/1.5VALWP/ 1.6VSP	2007/07/02	HP	Fine tune +1.05VSP Power Sequence	Change signal of PR514.2 from VDD_POK# to S_PWR_EN#	PreDB-->DB1
10	Page35	CPU_CORE	2007/07/02	HP	Add VGATE control circuit	Add PR228 as 4.7K Add PQ203 as 2N7002KW	PreDB-->DB1
11	Page36	ADP_OCP	2007/07/02	HP	Fine tune the smart adpater function	1. Add PR14 as 10K between PR13 and GND Change PR13 from 191K to 181K Reconnect the node of PR6.1 and PU1.3 to the connected node of PR13 and PR14 2. Change PR12 from 10K to 100K	PreDB-->DB1
12	Page31	Charger	2007/07/05	compal	Modify charger circuit after review by TI	1. Add PC119 as 4.7uf Reconnect PC109 and PC110 from BATT to the connected node of PL102 and PR110 2. Add PC120 and PC121 as 0.1uf 3. Change PR113 from 150K to 39K	PreDB-->DB1
13	Page35	CPU_CORE	2007/07/05	compal	Modify CPU regulator circuit after review by Intersil	1. Add PR229 as 1 ohm 2. Add PC213 as 0.1uf 3. Add PC214 as luf 4. Reserve PR230, PR231, PC215 and PC216 5. Add PR232 as 0 ohm 6. Add PD402 as RB751V 7. Change PR228 from 4.7K to 1K 8. Chagne PR203 from 60.4K to 71.5K 9. Chagne PR204 from 2.94K to 47K 10. Chagne PR205 from 82.5K to 53.6K 11. Chagne PR206 2.49K to 4.22K 12. Chagne PR208 2.74K to 0 ohm	PreDB-->DB1

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# Version Change List (P. I. R. List) for Power Circuit (2)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
14	Page31	Charger	2007/08/16	Compal	1. For TI's suggestion 2. Add resistor divider for OVP function of charger 3. Add charging voltage control circuit	1. Add PC124 as 0.1uf Reserve PC125 Add PC123 as 100pf Connect Pin8 (IADSLP) to GND 2. Add PR134 and PR135 3. Add PR119 as 100K Add PR120 as 143K Reserve PR122 Reserve PC122	DB1-->DB2
15	Page36	ADP_OCP	2007/08/17	Compal	1. Prevent spike or reverse voltage 2. For E-STAR, increase the resistor divider in propotional	1. Add PR15 as 47 ohm Add PC18 as 0.1uf Add PD3 as 1N4148 2. Change PR1 and PR8 from 22.6K to 226K Change PR2 and PR9 as 100K	DB1-->DB2
16	Page31	Charger	2007/08/17	HP	Reserve ESD protection diode for BAT_ID	Reserve PD7	DB1-->DB2
17	Page31	Charger	2007/08/20	Compal	1. Fine tune resistor divider for CHGCTRL 2. Fine tune resistor divider for Constant Power point 3. Fine tune the AC detector	1. Change PR114 from 24.9K to 118K Change PR115 from 100K to 470K 2. Change PR102 from 4.22K to 56K Change PR107 from 10K to 100K 3. Change PR118 from 133K to 255K	DB1-->DB2
18	Page30	DC Connector/ CPU_OTP	2007/11/22	Compal	Rename "BAT_ID" to "BAT_ID#" to indicate this signal is low active.	Rename "BAT_ID" to "BAT_ID#".	SI1-->SI2
19	Page30	DC Connector/ CPU_OTP	2007/11/22	Compal	For EMI requestion.	Add PC6 and PC126 as 1000pf	SI1-->SI2
20	Page31 Page30	Charger DC Connector/ CPU_OTP	2007/11/22	Compal	Follow SKYY	1. Reserve PC19, PC20, PC21 as 100P_0402_50V8J 2. Add PR49 as 1K_0402_1% 3. Change PR48 from 10K_0402_5% to 210K_0402_1%	SI1-->SI2
21	Page35	CPU_CORE	2007/11/22	HP	Re-connect the regulator power from +5VS to +5VALW	Re-connect the regulator power from +5VS to +5VALW	SI1-->SI2
22	Page31	Charger	2007/11/29	HP	Correct the connection of signal SRSET	Reconnect the signal "SRSET" from PU101.6 to PU101.16	SI1-->SI2
23	Page34	1.05VSP/ 1.5VALWP/1.6VSP	2007/11/29	HP	The power plane of VIA chipset is changed from +1.6VS to +1.5VS, and the +1.5VS could be generated from +1.5VALW.	Remove all the related component of +1.6VSP	SI1-->SI2
24	Page31	Charger	2007/11/29	Compal	Solve the noise issue when battery is charged at some charging current.	Change PR113 from 39K to 13.7K	SI1-->SI2
25	Page35	CPU_CORE	2008/01/09	Compal	Solve the S3 resume shutdown issue.	Re-connect PR229.2 and PC214.1 from +5VALW to +5VS	SI2-->PV
26	Page31	Charger	2007/01/16	Compal	For EMI requirement	Add PC127 as 0.1u	SI2-->PV
27	Page32 Page35	3.3VALWP/5VALWP CPU_CORE	2007/01/17	Compal	For Safety requirement	1. Add PC318 as 0.1uF 2. Reserve PC217	SI2-->PV
28	Page32	3.3VALWP/5VALWP	2007/01/18	HP	Fine tune the sequence of +3VALW and +1.5VALW	Reserve PR520	SI2-->PV
29	Page31	Charger	2008/03/18	HP	Raise the charge voltage	Change PR120 from 143K to 100K, Change PR119 from 100K to 124K	PV-->PVR
30	Page31	Charger	2008/03/18	HP	For wavy issue	Add PC128 as 47u_25V	PV-->PVR

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# EE PIR list

## DB Build:

08/10/2007

Page 9 -Reserve LVDS SSC.  
 Page 13 - change C258 from 0.1u to 0.47u for LCD power sequence  
 Page 14 - Add a 10K PU for IRQ1/IRQ12  
 Page 16 - change EC\_SCI# from GPIO to GPI3  
 Page 16 - change C287, C288, C659 and C660 from 3900pF to 0.01pF for SATA  
 Page 16 - change R522 from PU to PL for minicard power  
 Page 18 - change C366, C367, C661 and C662 from 3900pF to 1200pF for SATA  
 Page 18 - reverse SSD pin  
 Page 20 - update LAN LINK LED circuit  
 Page 27 - Add 2N7002 to reverse KB\_RST#  
 Page 29 - Install R655 and remove R645 for power sequence

08/15/2007

Page 8 -Swap PCIE channel for minicard and LAN.  
 Page 16 -tie EC\_SMI# from EC pin123 to GPI2/EXTSMI# of SB  
 Page 22 -modify the footprint of SD socket to meet vendor new drawing.  
 Page 26 -modify the power rail of cap sense board (JP18) from +3VALW to +3VL.

08/20/2007

Page 12 -Reserve L62, L63, L64 for CRT fine tune.  
 Page 23 -Install R370 for internal speaker issue.  
 Page 26 -Add quick switch for dock CRT support.

## SI-1 Build:

09/01/2007

Page 23 -remove 6044 supported

09/15/2007

Page 16 -change strpa pin of V4-Lite Capability from enable to disable

09/19/2007

Page 15 -Add the circuit for RSMRST to fix RTC lose issue.  
 Page 18 -Add Q63 for XMIT\_OFF# and BT LED indicator  
 Page 15 -change the RST# pin of TPM from NPCI\_RST# to PCI\_RST# for +3VS leakage issue.  
 Page 26 -add the level shift for DOCK LAN LED.  
 Page 27 -Modify the VCCI\_PWRGD circuit of EC  
 Page 29 -remove the diode of VCCI\_PWRGD  
 Page 29 -Add a jumper for +1.6VS\_NB option

09/24/2007

Page 11 -Modify the clock generator and clock buffer to single clock generator.  
 Page 18 -change SATA CONN from 20pins to 10 pins  
 Page 19,20 -Add 5784 and 5787 co-layout circuit.  
 Page 23 -Add D45 to fix the leakage of A\_SD  
 Page 23 -change R651 and R652 to 0 ohm

09/28/2007

Page 23 -Change C716 and C717 from 1uF to 2.2uF.

10/02/2007

Page 23 -change the gain of AMP from 10dB to 12dB.  
 Page 27 -Change PREP#\_SB from U34.91 to U34.61 to fix the +3VS leakage during S3.

10/08/2007

Page 16 -Swap LP\_EN# and XMIT\_OFF\_SB#, CABLE\_DET and WL\_OFF  
 Page 18 -Add ODD\_DET# circuit.  
 Page 26 -reserve R745 and R746 for EMI.

## SI-2 Build:

11/08/2007

Page 13 -connect R154.2 to +3VALW to fix the white screen issue.  
 Page 13,14 -Set ALS\_EN as low to disable light sensor.  
 Page 24 -Connect JP11.1 to AGND for HP can't play record file issue.  
 Page 26 -Connect JP17.26 from ADP\_ID to ADP\_SIGNAL for DOCK charge issue.  
 Page 27 -Change R701 from 14K to 3.48K for system shut down issue.

11/19/2007

Page 9 -Add L65, C188 and C741 for +VCC33GFX by VIA request.  
 Page 25 -Reserve L66 and L67 for EMI  
 Page 26 -Reserve C742, C743 and C744 for EMI

11/27/2007

Page 14,16 -Change LP\_EN# from GPO7 to GPO2.  
 Page 15 change USB of DOCK from port 7 to port 3  
 Page 16- change ODD\_DET from GPI16 to GPIO26  
 Page 16, 27- change CABLE\_DET from SB to EC GPIO30  
 Page 25-change the enable pin of U24 to SLP\_S5#.  
 Page 26- reserve ESD diode on LID/B, Cap/B and LED/B for ESD  
 Page 27- change the pull high value of battery I2C bus to 2.2K

11/28/2007

Page 13- Change R152 from 1M to 150K and C258 from 0.47u to 0.1u for LCD timing.  
 Page 16- change XMIT\_OFF\_SB# from GPIO20 to GPO2  
 Page 16- change LP\_EN# from GPO2 to GPIO20.  
 Page 16- reserve CABLE\_DET at GPIO27

11/29/2007

Page 27- change R701 to 4.75K to set thermal protect at 85C.  
 Page 29- change C708 to 1000p and change C597 to 3300P.

## PV Build:

12/15/2007

Page 13 -modify the BK\_OFF# circuit to fix Toshiba panel issue  
 Page 13 -reduce the damping resistor of DVP1CLK from 22ohm to 0 ohm for DMW issue

01/04/2008

Page 13 -Add D54 to fix the white screen after flash KBC.  
 Page 16 -change R521 pull low for wake on LAN issue  
 Page 16 -change R522 pull high to disable the power of WLAN  
 Page 25 -change R420 from 1Kohm to 1.8Kohm for USB cradle issue  
 Page 25 -change C562 from 2200pF to 1500pF for system shut down when USB VCC and GND short

01/09/2008

Page 23-Install D45 for mute function  
 Page 27-Connect AC\_AND\_CHG to GPIO9 of EC for AirLine/COMBO adapter

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# EE PIR list

01/17/2008

Page 4,14, 27 -Add 0.1u for ESD at A\_SD,PM\_RSMRST#,SB\_PWRGD,PCI\_RST# ,H\_CPUSLP#,H\_DPSLP# and H\_PWRGD

01/28/2008

Page 25 -modify the value of C561, C562, R420, C277 and R166 for power USB issue.

**PV-R Build:**

03/06/2008

Page 13 -Change D54 to DAP202U for backlight issue

Page 16 -Reserve 56p cap at AZ\_BITCLK\_HD,AZ\_BITCLK\_MDC for key part team request

Page 25 -Add 470p cap at SLP\_S5 and +5VALW of USB/B for EMI

03/12/2008

Page 25 -Change C562 to 82pF for power USB shut down issue.

03/17/2008

Page 23 -Change C497, C500, C502 and C503 to 0 ohm for ESD.

Page 23 -Add C767, D60 and D61 for ESD.

03/18/2008

Page 12 -Add a pi filter near CRT CONN and not install old filter to improve CRT wavy.

Page 13 -chaneg the backlight circuit to make same as SKYY.

Page 23 -Due to D60 and D61 will cause cap mute issue so remove them and add D7 for avoid this issue.

Page 26 -remove quick switch supported to improve CRT wavy issue.

03/19/2008

Page 23 -Change C497, C500, C502 and C503 back to 0.1uF.

03/19/2008

Page 23 -Change C497, C500, C502 and C503 back to 0.1uF.

03/25/2008

Page 26 -Install R421 for EC to reset capsense controller.

Page 27 -change R701 to 9.76K for thermal test G.

**MV Build:**

04/01/2008

Page 23 -Change R651 and R652 to 2K 5% and R 653 to 1K 5%.

04/03/2008

Page 23 -Reserve D60 and install R761 for ESD issue.

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