



# Compal Confidential

## NAWA1 Schematics Document

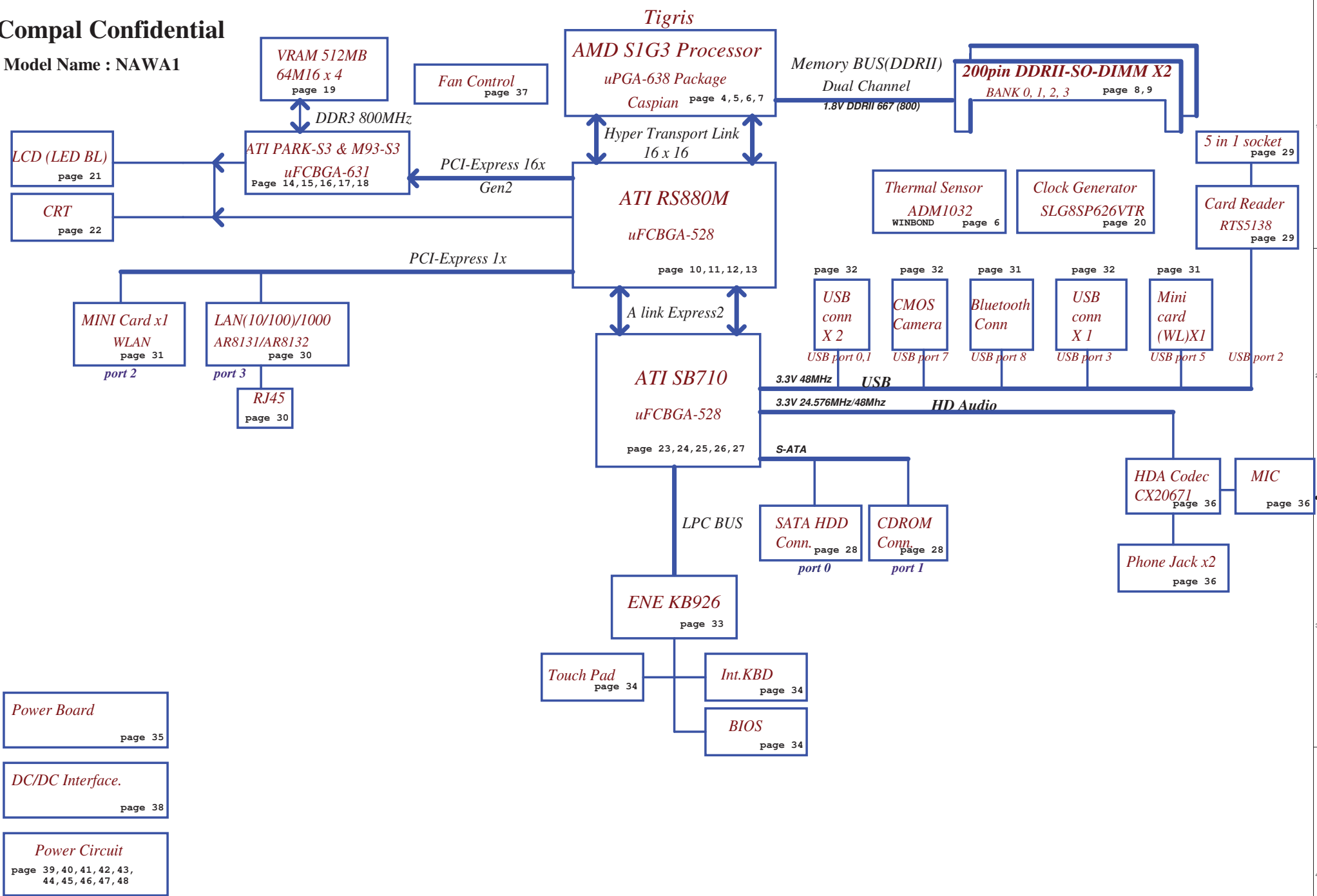
### AMD Tigris: Caspian Processor with RS880M/SB710/Park-S3 & M93-S3

2009-11-26

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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
				Cover Page	
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				Date	Rev
				Thursday, December 10, 2009	1.0
				Sheet	1 of 49

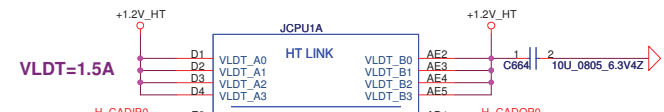
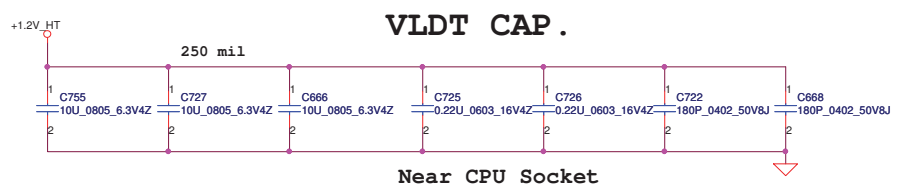
# Compal Confidential

Model Name : NAWA1

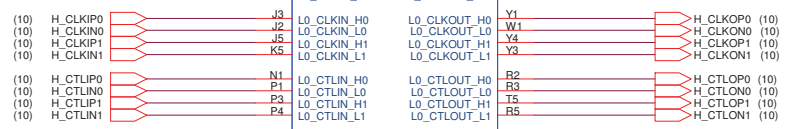


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				Block Diagrams	
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					LA-5971P
				Date:	Thursday, December 10, 2009
				Sheet	2 of 49
				Rev	1.0





H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	H1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	L1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	N2	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15

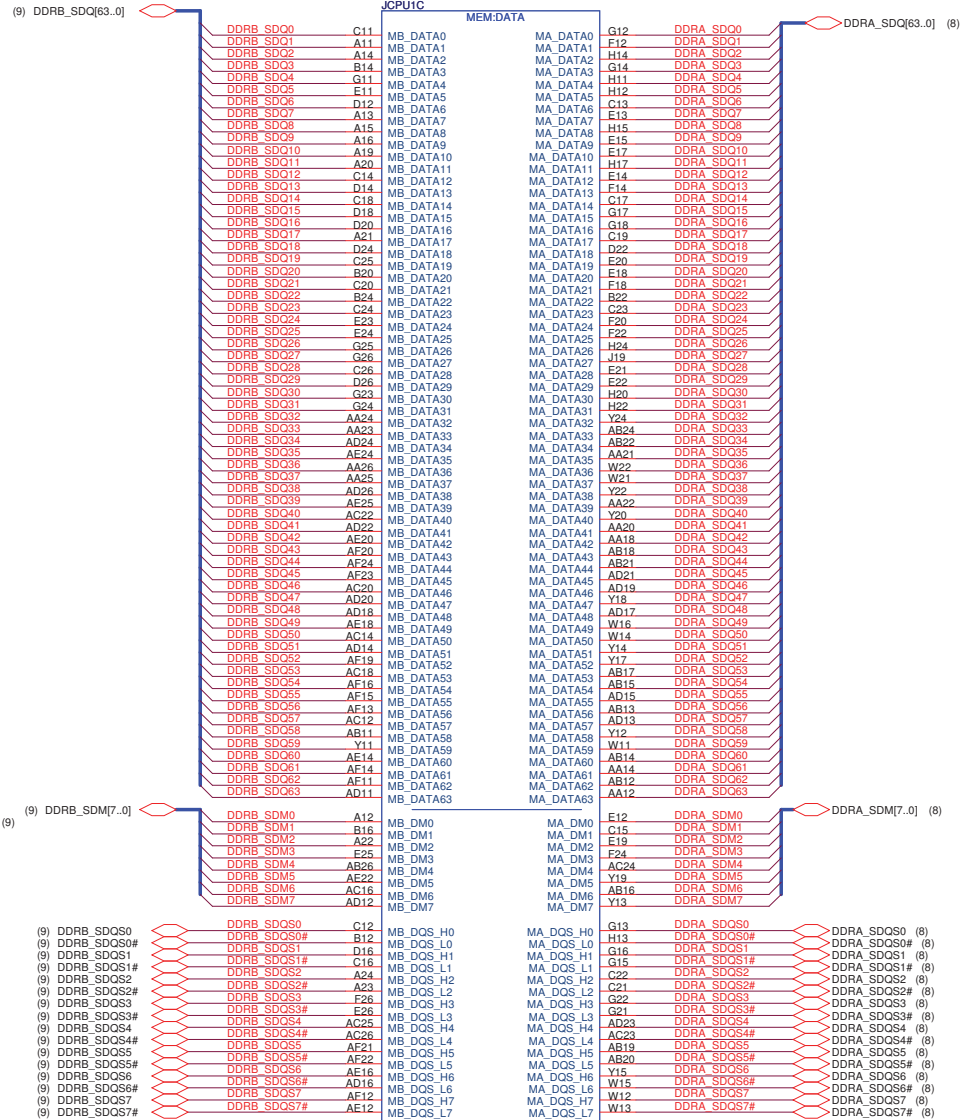
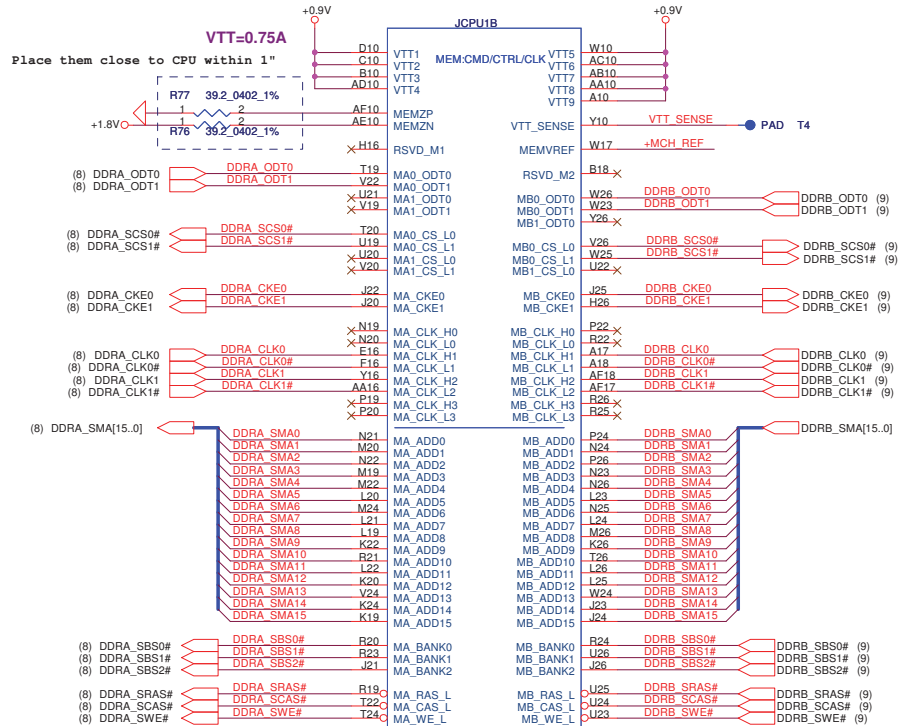
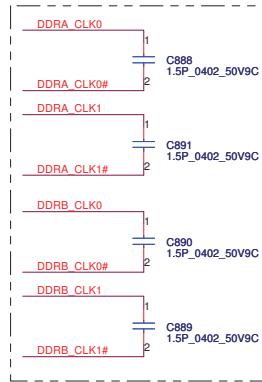
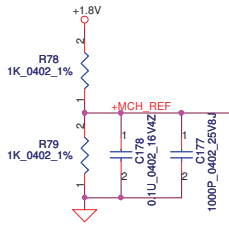


6090022100G\_B ME@

Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	AMD CPU S1G3 HT I/F
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			Rev 1.0	Sheet 4 of 49

# Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR  
WITHIN 1.2 INCH



6090022100G\_B  
ME@

6090022100G\_B  
ME@

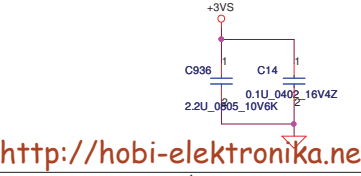
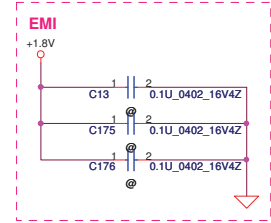
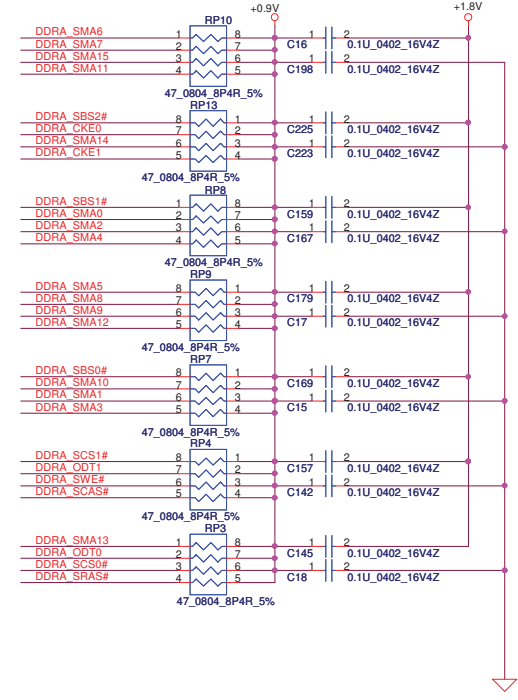
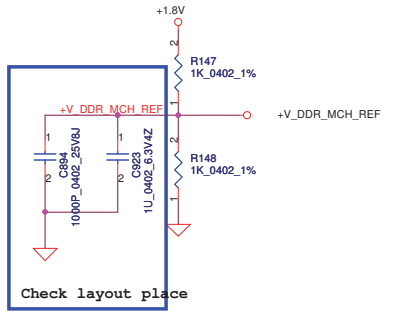
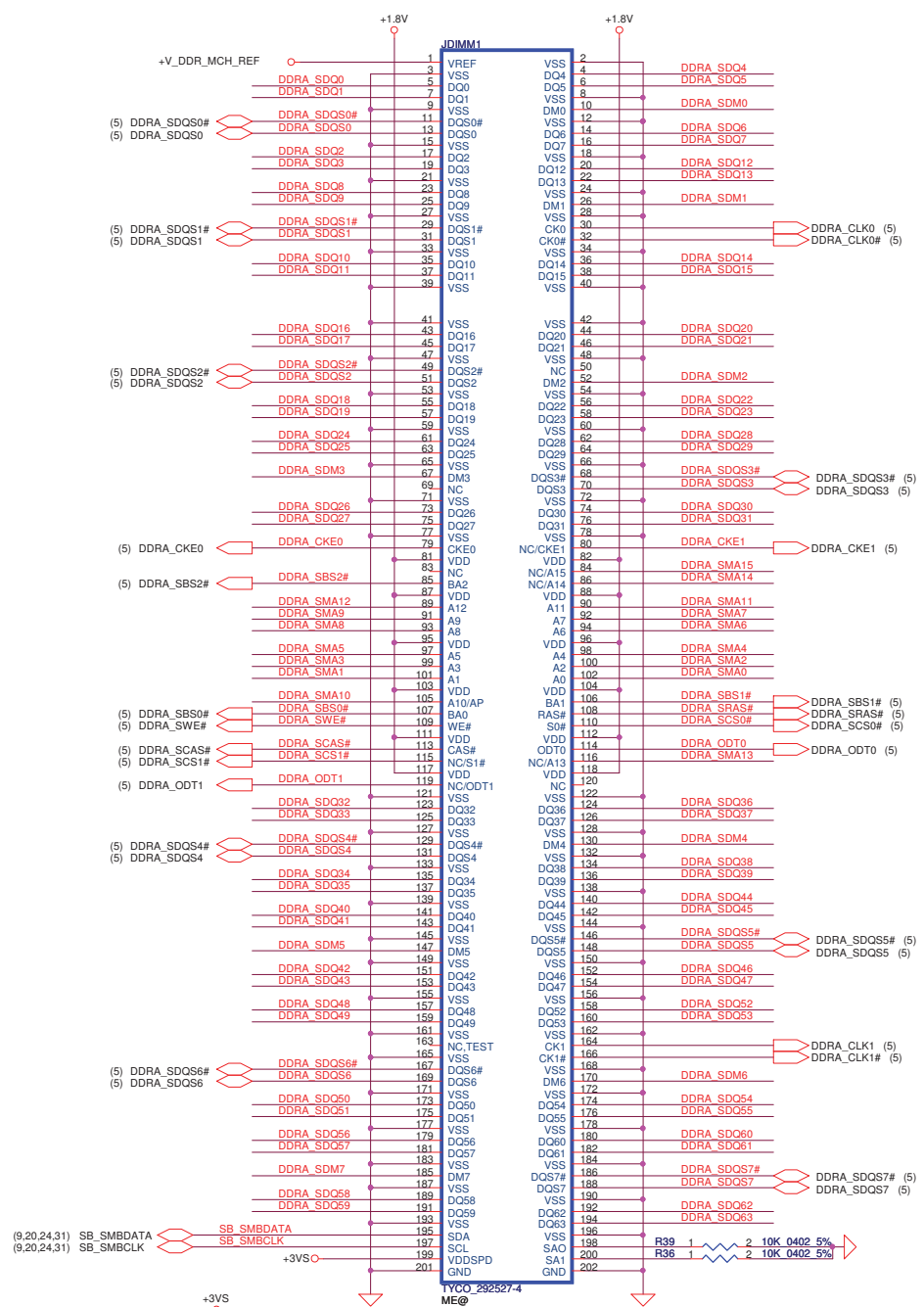
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Title		
AMD CPU S1G3 DDRII I/F		
Size	Document Number	Rev
Custom	LA-5971P	1.0
Date:	Thursday, December 10, 2009	Sheet 5 of 49



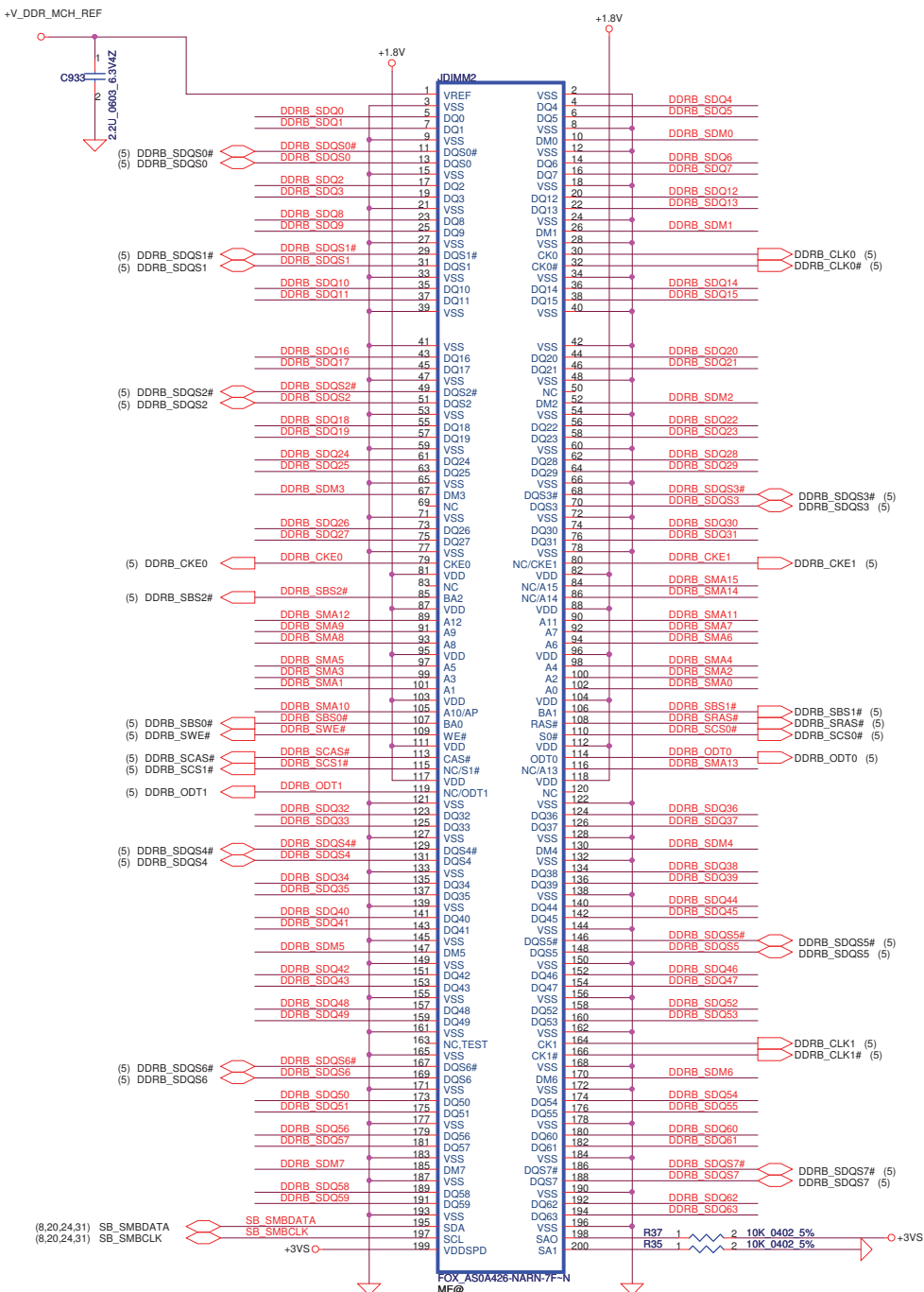




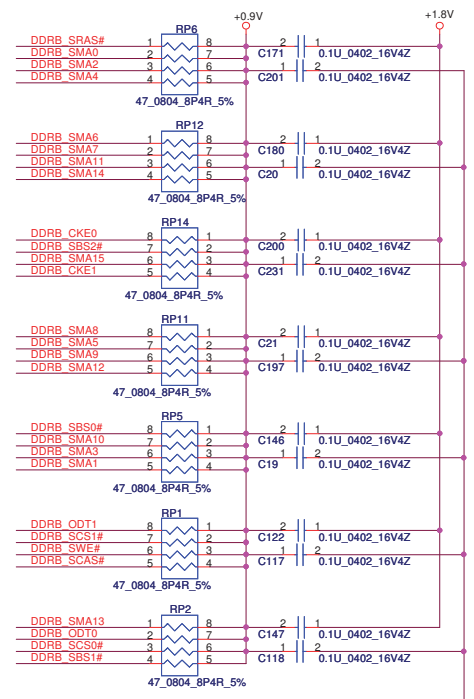
**DIMM1 REV H:5.2mm (BOT)**

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Issued Date	2008/10/06	Deciphered Date	2009/10/06	
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Size	Document Number	Rev		
Custom	LA-5971P	1.0		
Date:	Thursday, December 10, 2009	Sheet	8	of 49





- DDR\_B\_SDO[0..63] (5)
- DDR\_B\_SDM[0..7] (5)
- DDR\_B\_SMA[0..15] (5)



**DIMM2 REV H:9.2mm (BOT)**

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				LA-5971P	Rev 1.0
				Date:	Thursday, December 10, 2009
				Sheet	9 of 49

(14) PCIE\_GTX\_C\_MRX\_P[0..15]  $\longleftrightarrow$  PCIE\_GTX\_C\_MRX\_P[0..15]  
 (14) PCIE\_GTX\_C\_MRX\_N[0..15]  $\longleftrightarrow$  PCIE\_GTX\_C\_MRX\_N[0..15]

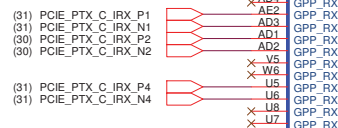
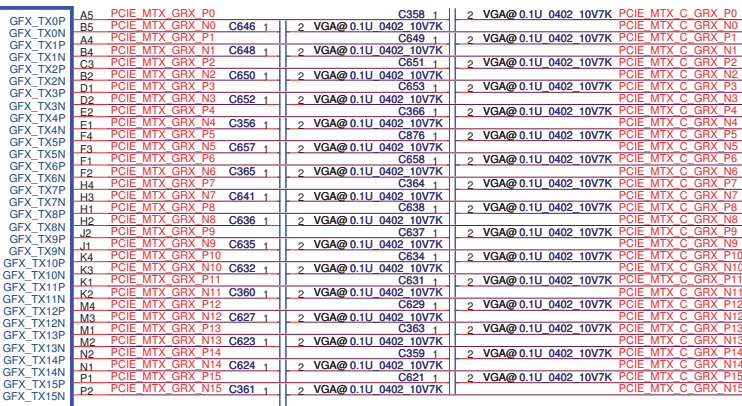
PCIE\_MTX\_C\_GRX\_P[0..15]  $\longleftrightarrow$  PCIE\_MTX\_C\_GRX\_P[0..15] (14)  
 PCIE\_MTX\_C\_GRX\_N[0..15]  $\longleftrightarrow$  PCIE\_MTX\_C\_GRX\_N[0..15] (14)

U20B

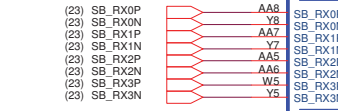
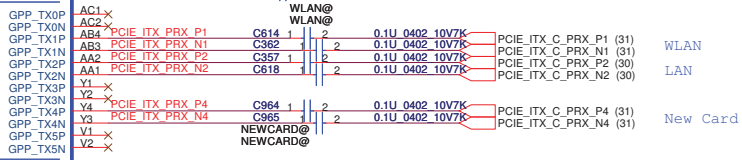


PART 2 OF 6

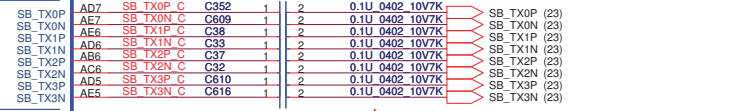
PCIE I/F GFX



PCIE I/F GPP



PCIE I/F SB

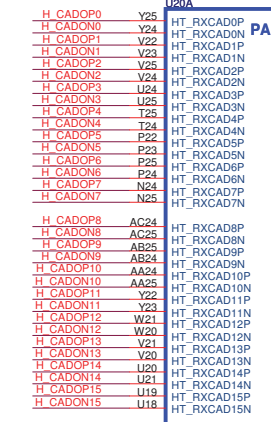
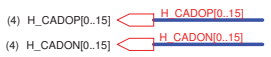


PCE\_CALRP(PCE\_BCALRP)  
PCE\_CALRN(PCE\_BCALRN)

RS880M\_FCBGA528

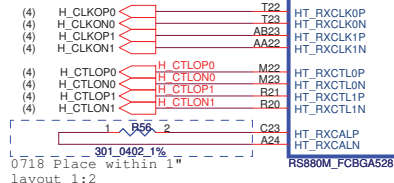
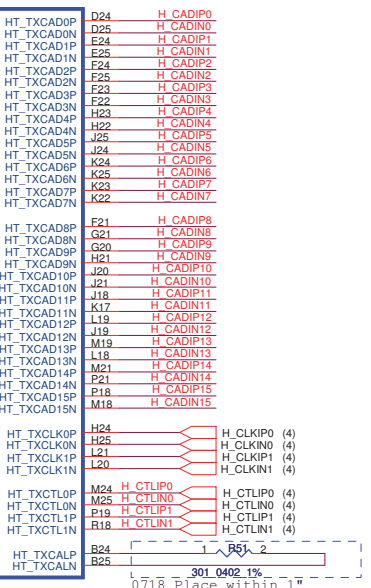
RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



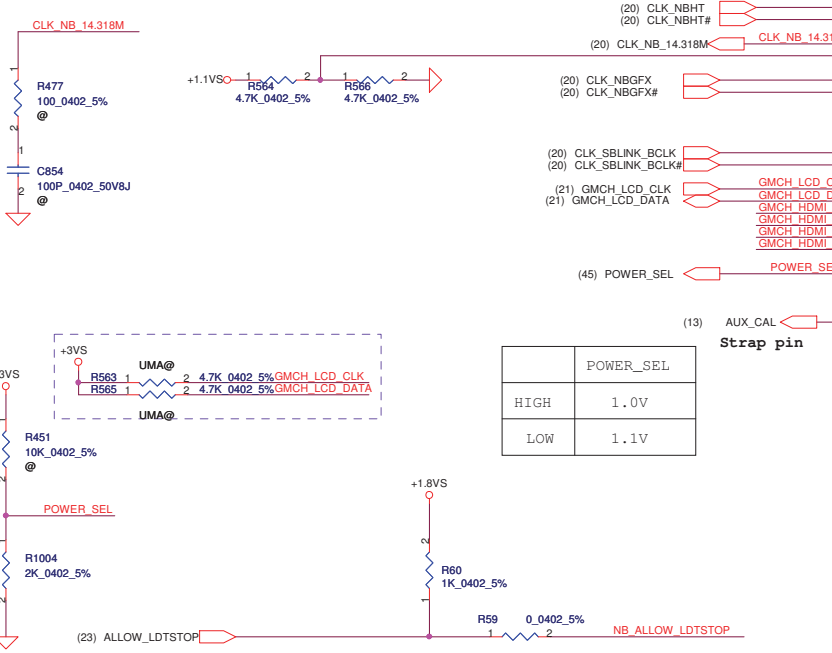
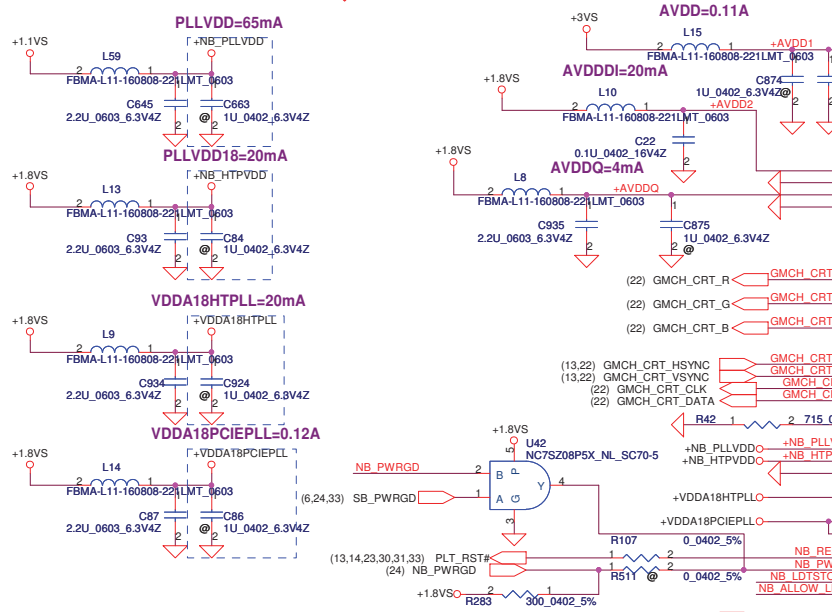
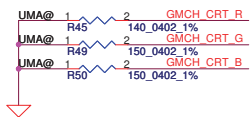
PART 1 OF 6

HYPER TRANSPORT CPU I/F

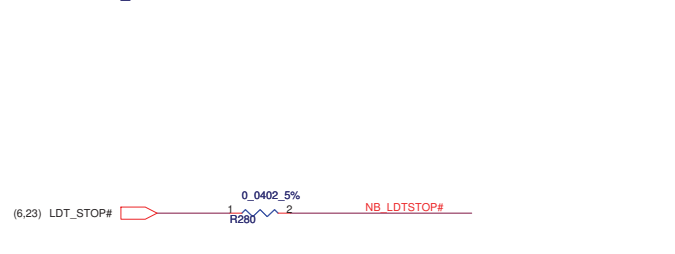
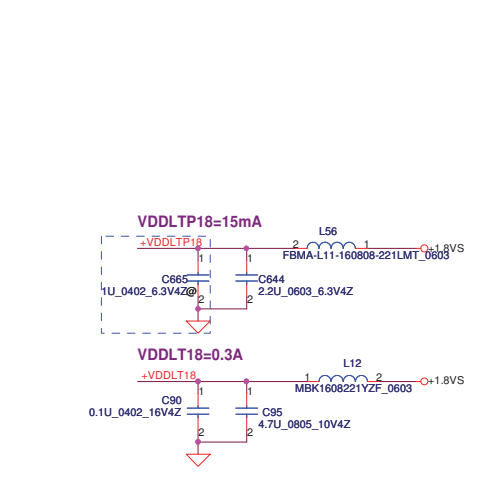
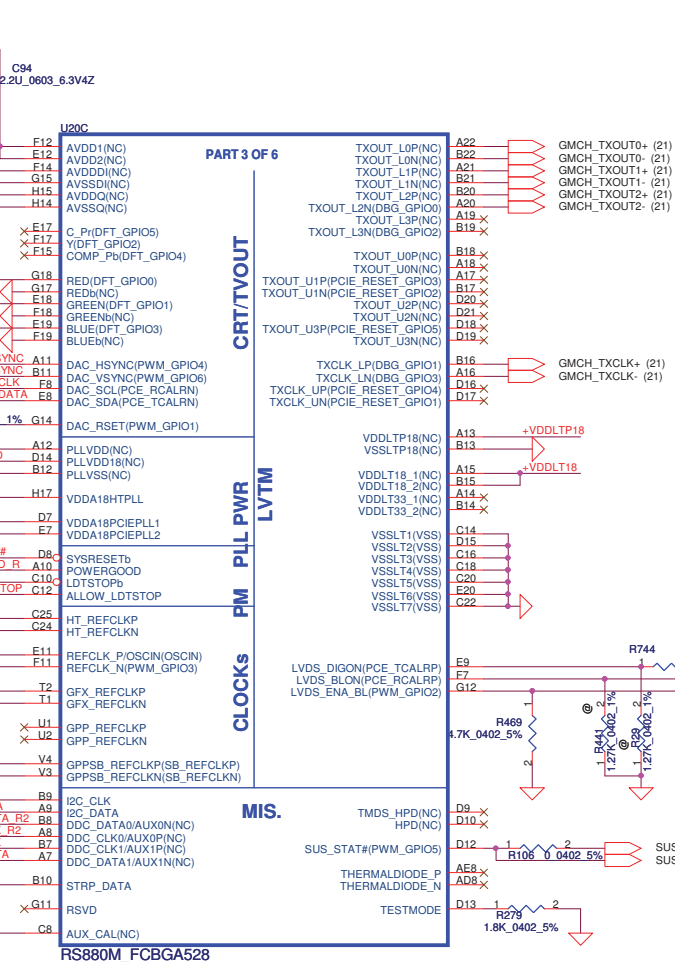


SA00002DR30 S IC 216-0674026 A13 RS780MN FCBGA 0FA  
 SA000032710 S IC 216-0752001 A11 RS880M FCBGA528 0FA

For RS780M A13  
 RED: Connected to GND through two separate 140ohm 1% resistor



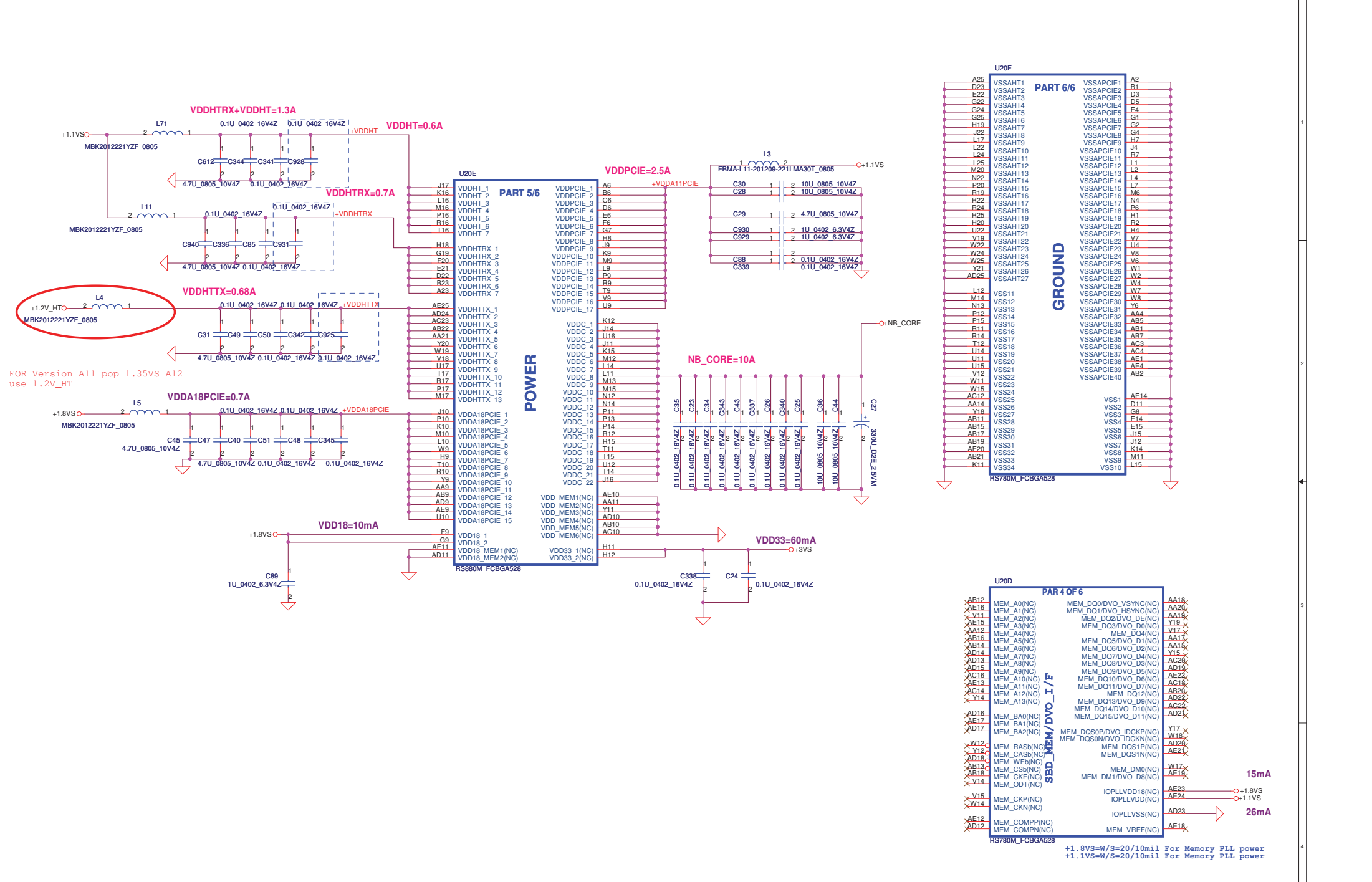
	POWER_SEL
HIGH	1.0V
LOW	1.1V



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Title		
RS880 VEDIO/CLK GEN		
Size	Document Number	Rev
Custom	LA-5971P	1.0
Date:	Thursday, December 10, 2009	Sheet 11 of 49

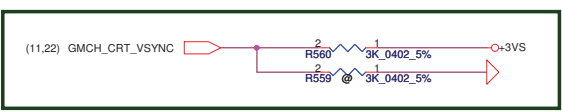


FOR Version A11 pop 1.35VS A12 use 1.2V\_HT

<http://hobi-elektronika.net>

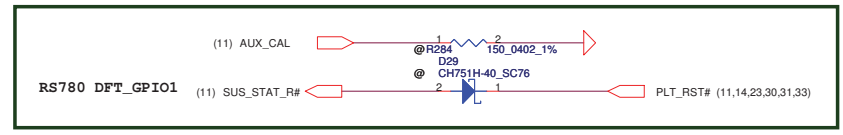
Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	RS880 PWR/GND	
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+1.8V=W/S=20/10mil For Memory PLL power  
+1.1V=W/S=20/10mil For Memory PLL power



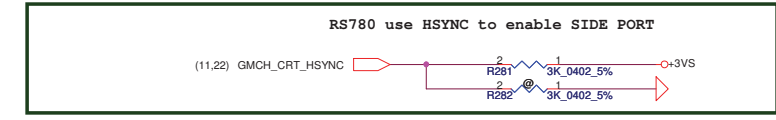
**DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO. (VSYNC)  
 1 : Disable (RS880M)  
 0 : Enable (RS880M)



**DFT\_GPIO1:LOAD\_EEPROM\_STRAPS**

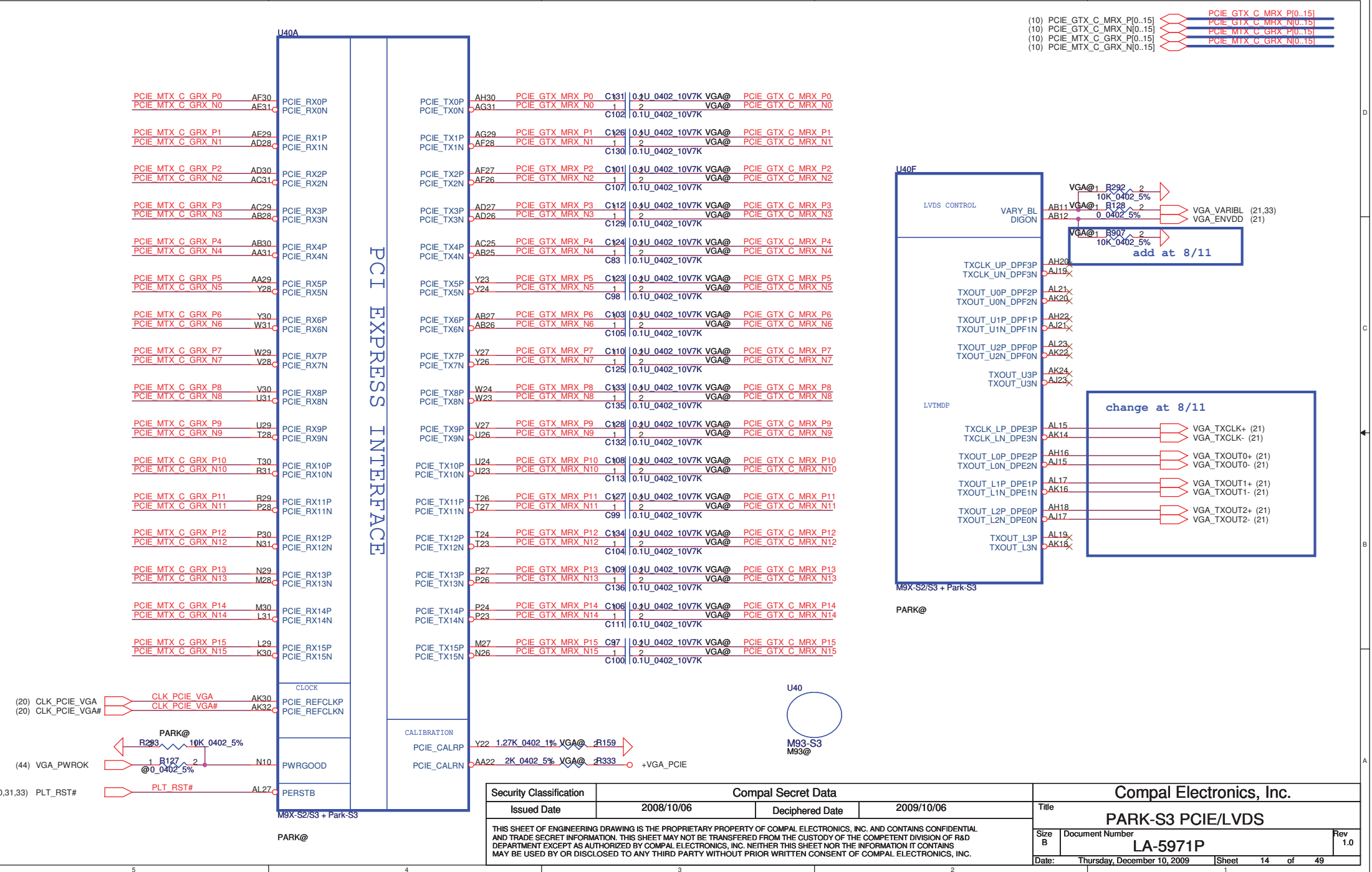
Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
 RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT



**RS780 use HSYNC to enable SIDE PORT**

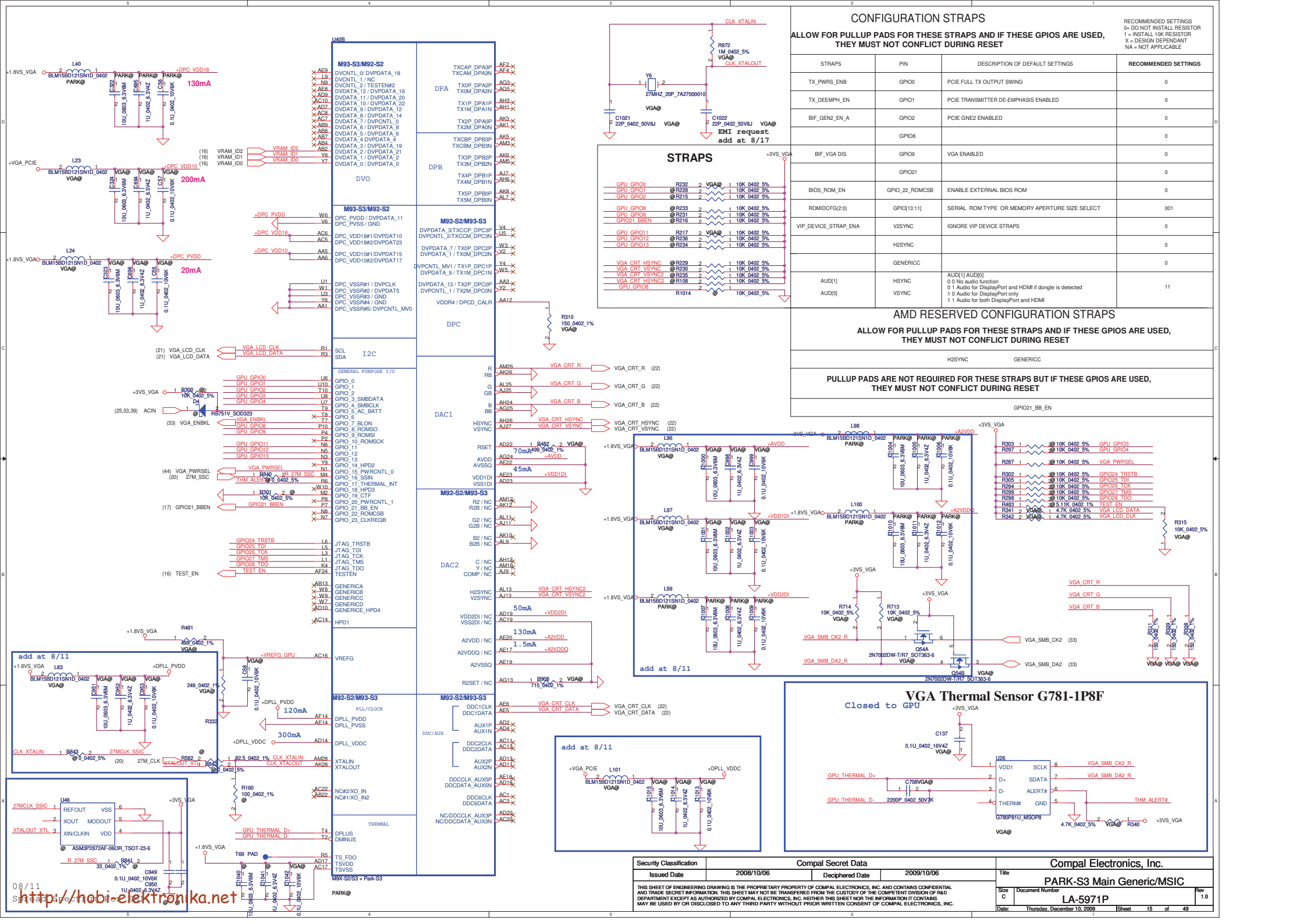
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)  
 0 : Enable (RS880M)  
 1 : Disable (RS880M)

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				LA-5971P	Rev 1.0
				Date: Thursday, December 10, 2009	Sheet 13 of 49



(10) PCIE GTX\_C\_MRX\_P[0..15] → PCIE GTX\_C\_MRX\_P[0..15]  
 (10) PCIE GTX\_C\_MRX\_N[0..15] → PCIE GTX\_C\_MRX\_N[0..15]  
 (10) PCIE\_MTX\_C\_GRX\_P[0..15] → PCIE\_MTX\_C\_GRX\_P[0..15]  
 (10) PCIE\_MTX\_C\_GRX\_N[0..15] → PCIE\_MTX\_C\_GRX\_N[0..15]

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Size B	Document Number			Rev	1.0
				LA-5971P	
Date:	Thursday, December 10, 2009	Sheet	14	of	49



### CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS  
 0= DO NOT INSTALL RESISTOR  
 1= INSTALL 10K RESISTOR  
 X = DESIGN DEPENDANT  
 NA = NOT APPLICABLE

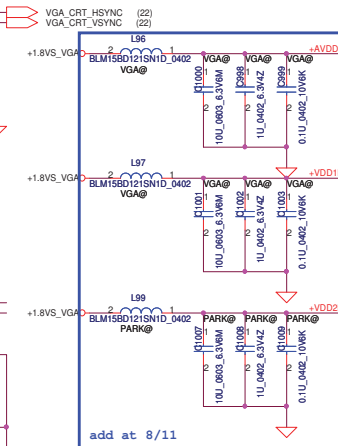
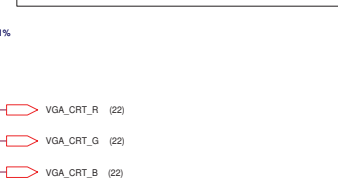
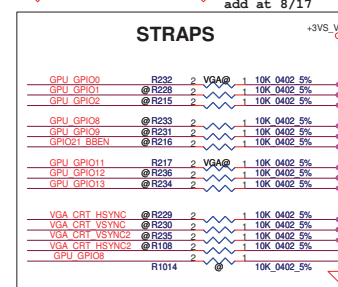
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWR5_ENB	GPIO0	PCIe FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIe GEN2 ENABLED	0
BIF_VGA_DIS	GPIO8	VGA ENABLED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_VGA_DIS	GPIO21	VGA ENABLED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
	H2SYNC		0
	GENERIC		0
AUD[1]	HSYNC	AUD[1] AUDIO[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11
AUD[0]	VSNC		

### AMD RESERVED CONFIGURATION STRAPS

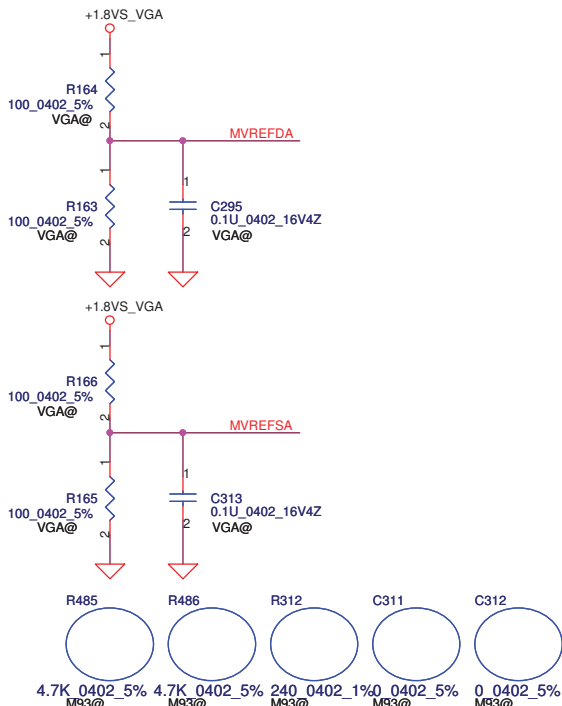
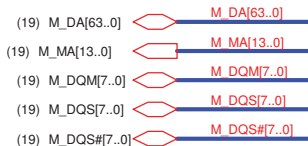
**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
H2SYNC	GENERIC		
GPIO21_BB_EN			

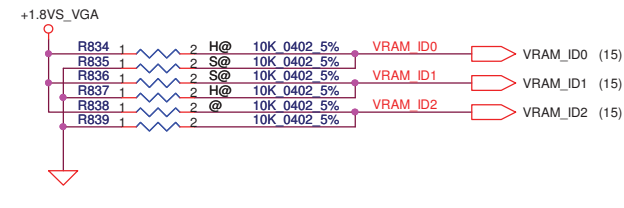
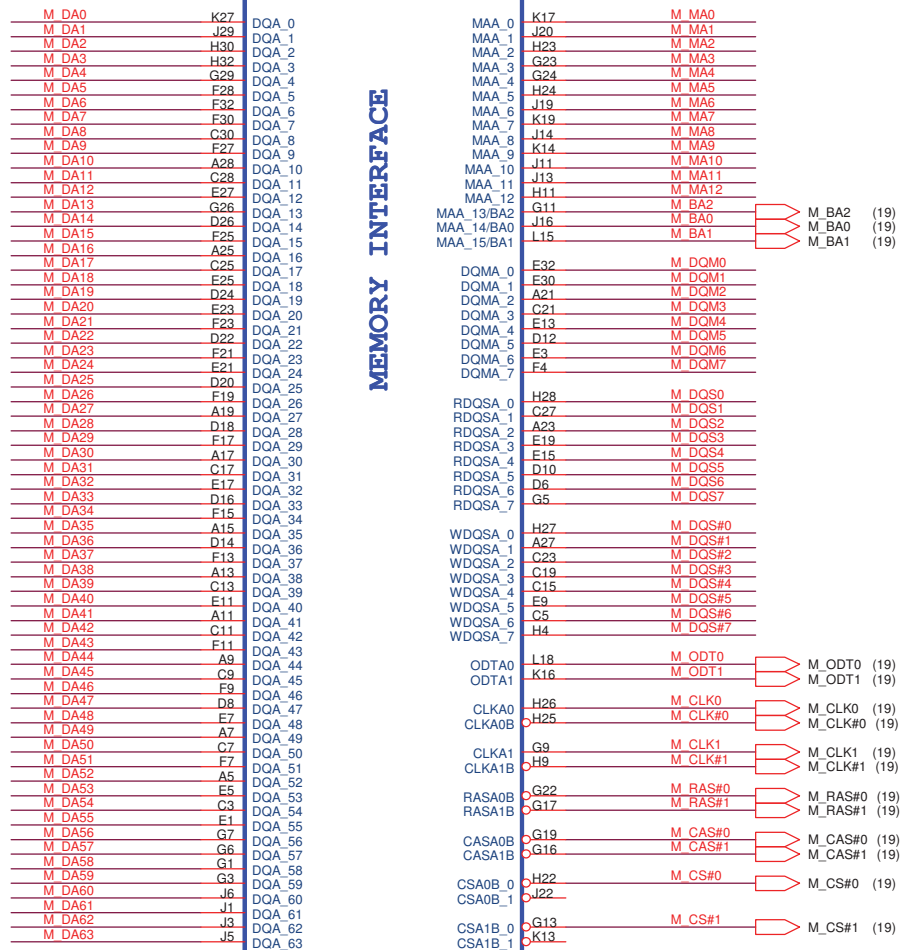
**PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**



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Size	C	Document Number	<b>LA-5971P</b>
Date:	Thursday, December 10, 2009	Sheet	15 of 49

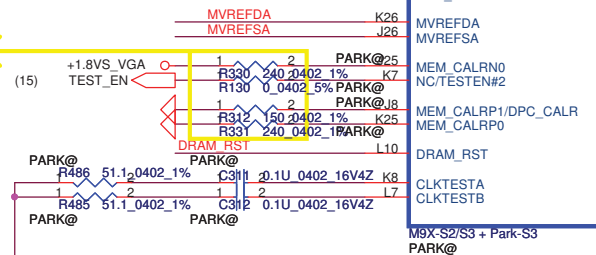
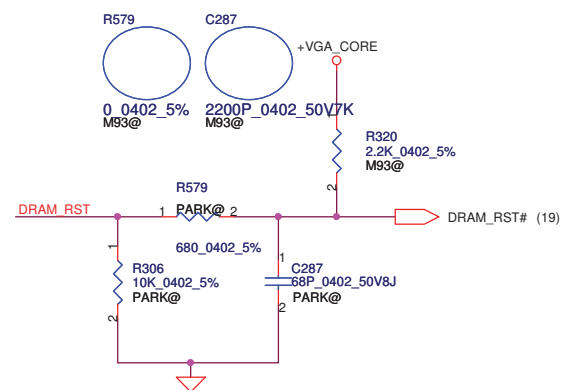


	M93-S3	PARK-S3
R330	NC	240
R130	NC	0/short
R312	240	150
R331	NC	240
	M93-S3	PARK-S3
R485	4.7K	51.1
R486	4.7K	51.1
C311	0/short	0.1uF
C312	0/short	0.1uF



Vendor		VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix	H5TQ1G63BFR-12C	1	0	0
Samsung	K4W1G1646E-HC12	0	1	0

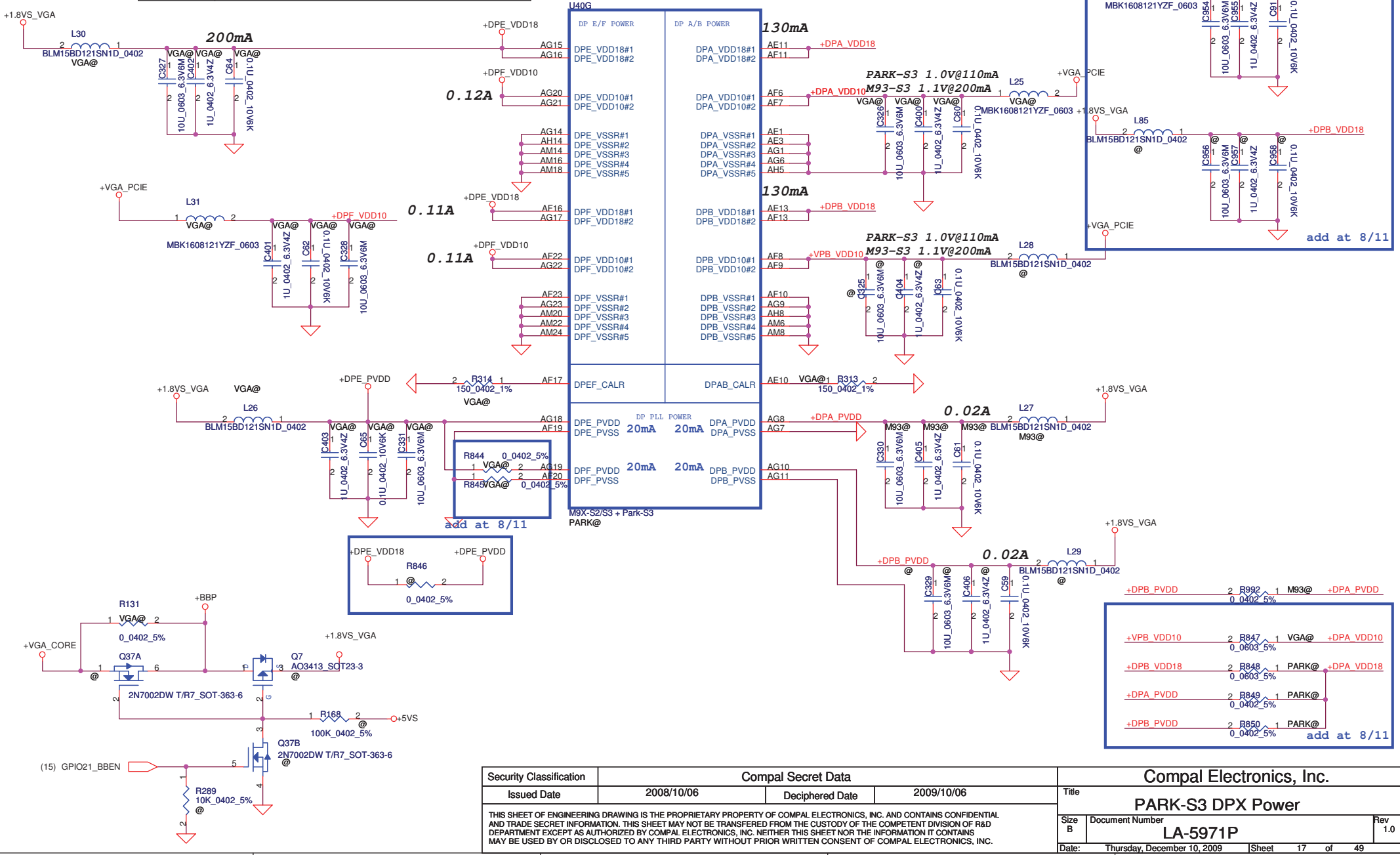
	M93-S3	PARK-S3
R306	NA	10K
R579	0/short	680
R320	2.2K	NA
C287	2.2nF	68pF



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				Size	Document Number
Date:	Thursday, December 10, 2009	Sheet	16	of	49

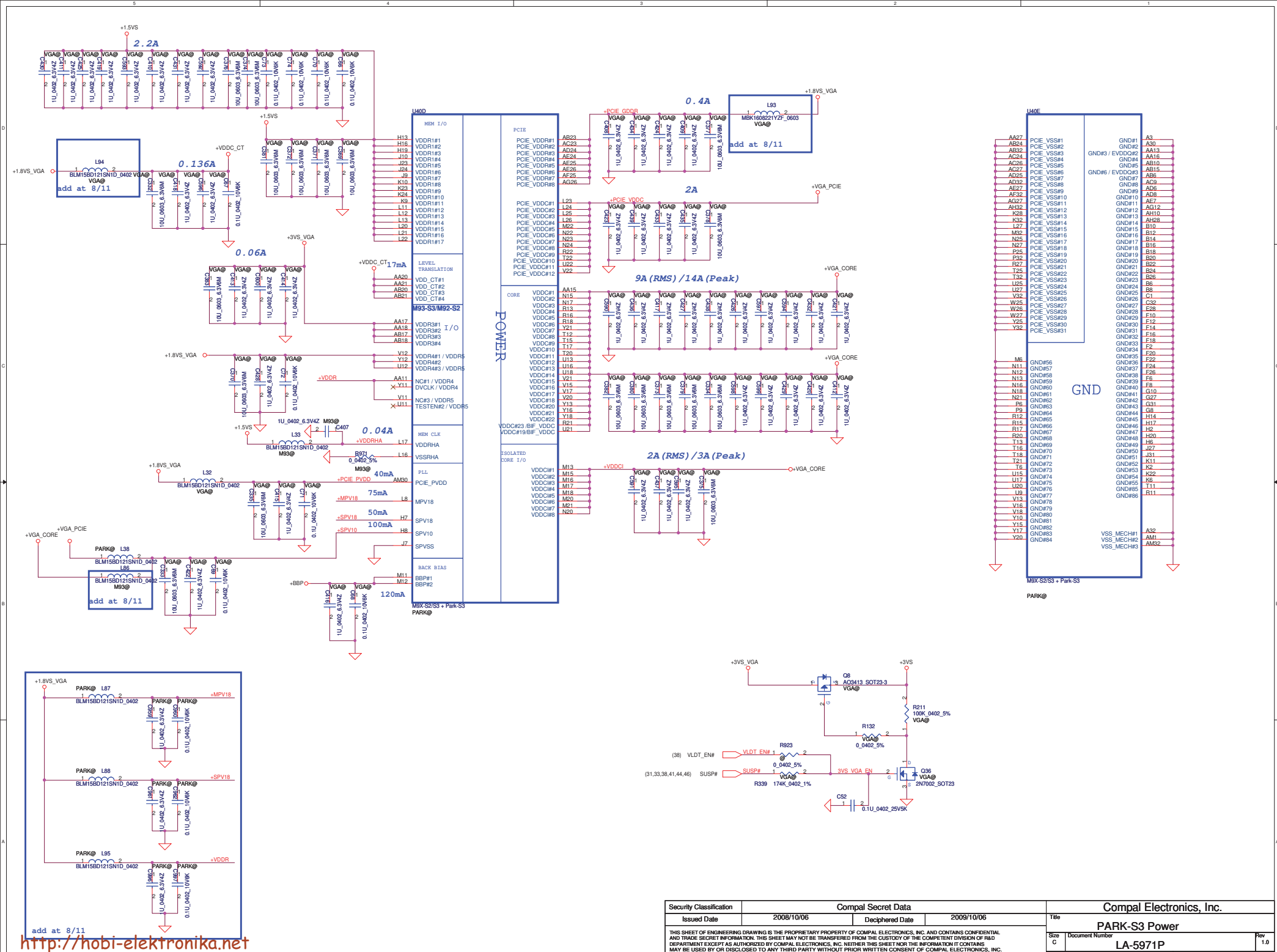


DPE\_VDD10 Park-S3: TMDS/DP=110mA@1.0V : LVDS=120mA@1.0V  
 DPF\_VDD10 M9X-S2/S3: TMDS/DP=170mA@1.1V LVDS=100mA@1.1V



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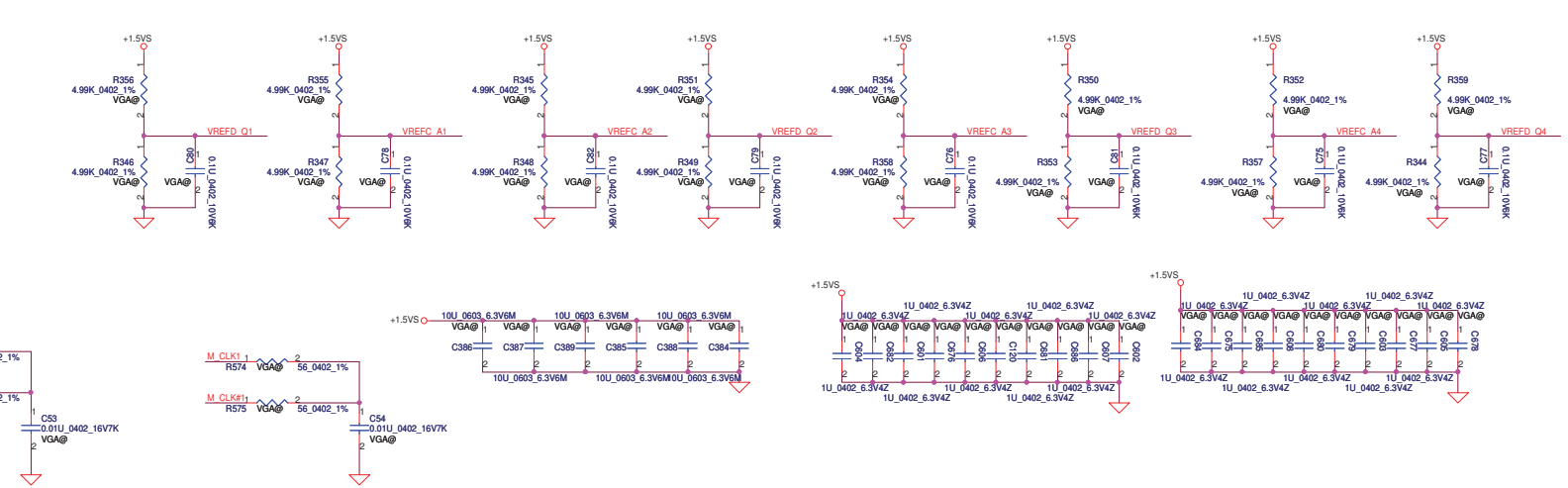
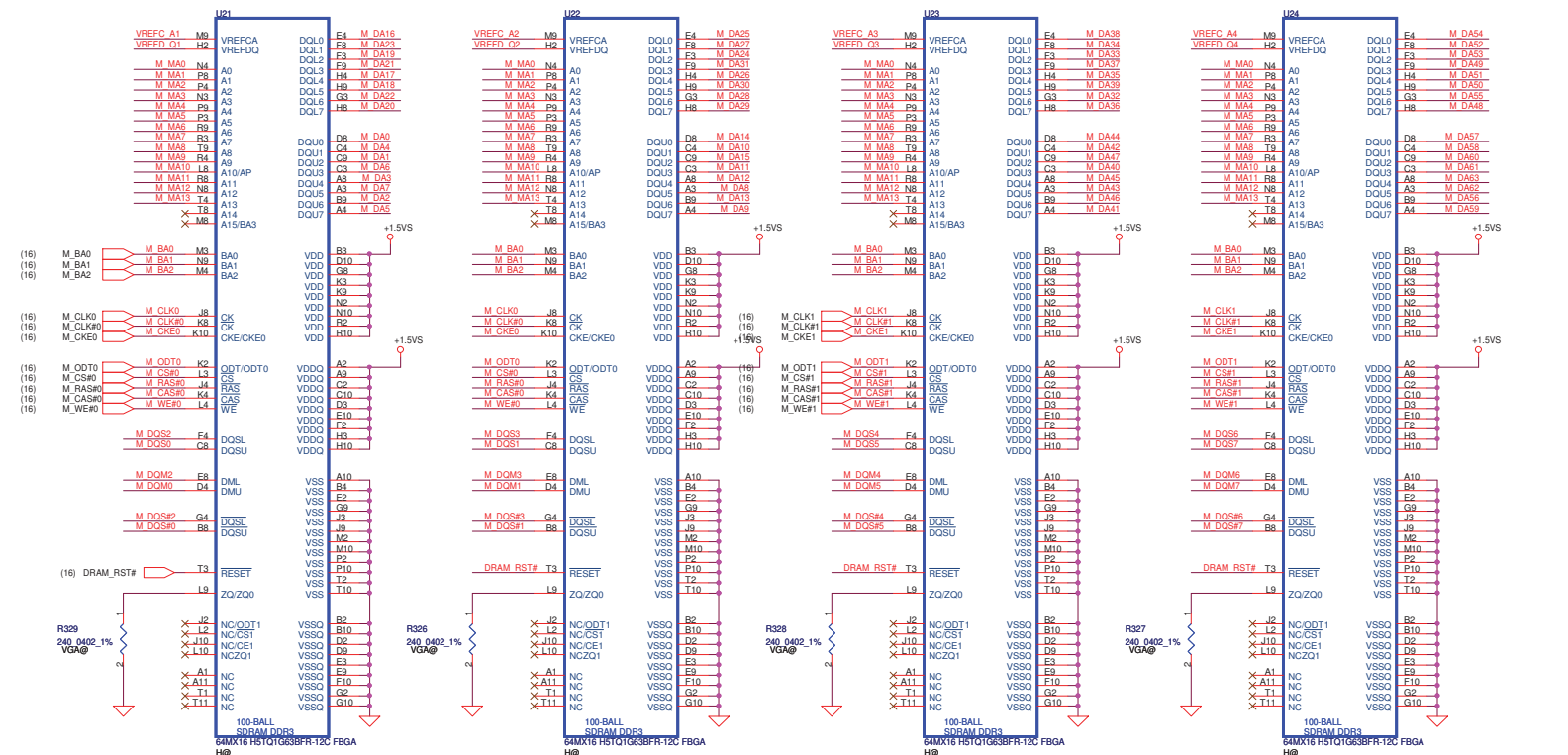
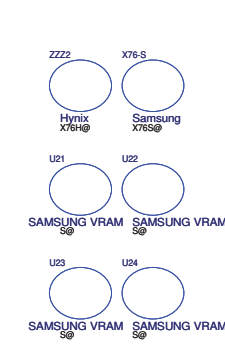
Compal Electronics, Inc.		
Title PARK-S3 DPX Power		
Size B	Document Number LA-5971P	Rev 1.0
Date: Thursday, December 10, 2009	Sheet 17	of 49



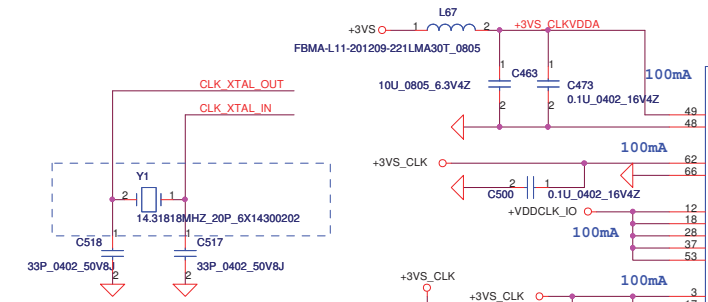
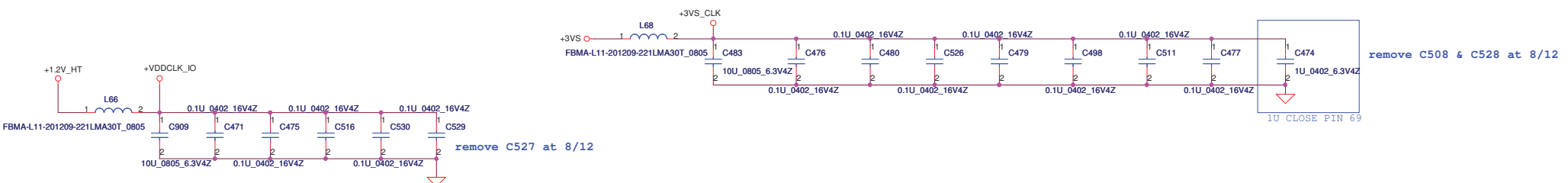
add at 8/11  
<http://hobi-elektronika.net>

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(38) VLDT_ENH#	VLDT_ENH#	(31,33,38,41,44,46)	SUSP#	LA-5971P	
				Date: Thursday, December 10, 2009	
				Sheet 18 of 49	

- (16) M\_DA[63..0] M\_DA[0..63]
- (16) M\_MA[13..0] M\_MA[13..0]
- (16) M\_DQM[7..0] M\_DQM[7..0]
- (16) M\_DQS[7..0] M\_DQS[7..0]
- (16) M\_DQS# [7..0] M\_DQS# [7..0]



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Size	Document Number	Rev	LA-5971P	1.0
Date:	Thursday, December 10, 2009	Sheet	19	of 49

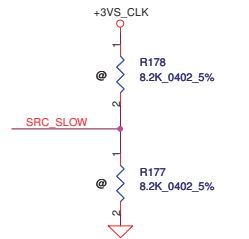
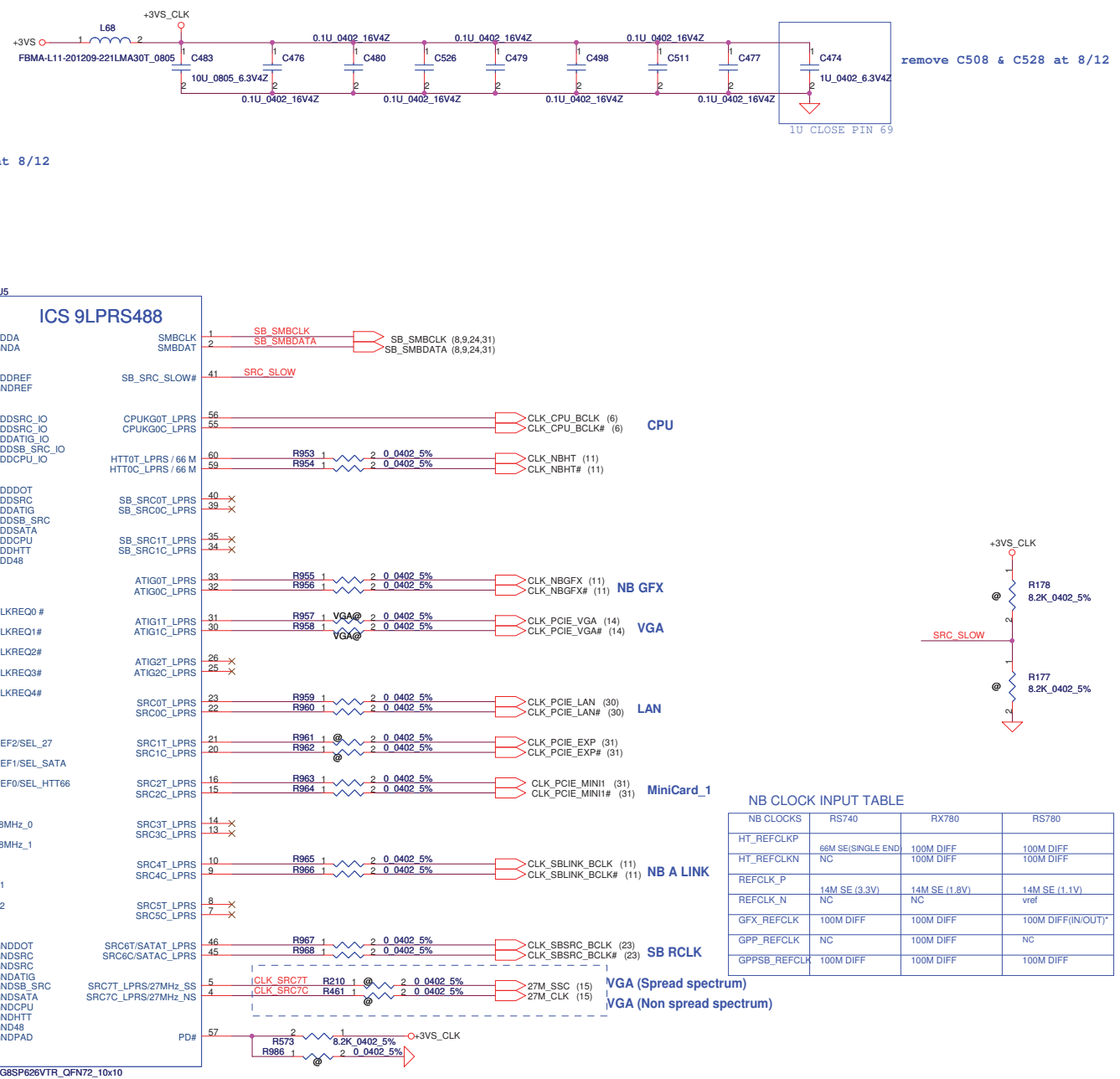
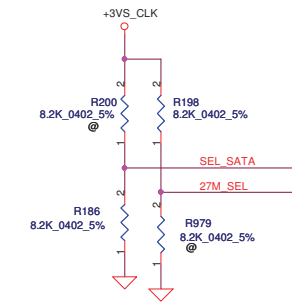
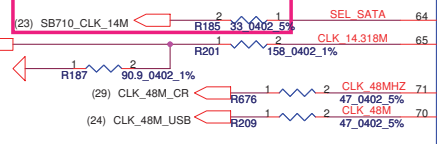


Routing the trace at least 10mil

NEW CARD (31) EXP\_CLKREQ#  
Mini Card1 (31) MIN1\_CLKREQ#

CLK_NB_14318M	
RS780	1.1V 158R/90.0R

For Tigris



NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	68M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN  
2nd (ICS) : SA000023H10 S IC ICS9LPRS488CLKLT MLF 72P CLK GEN

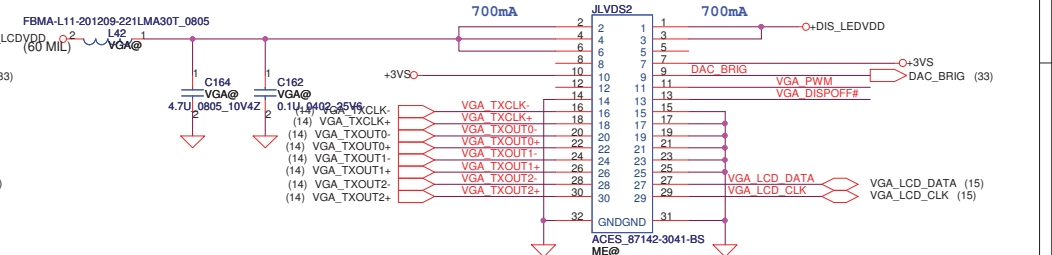
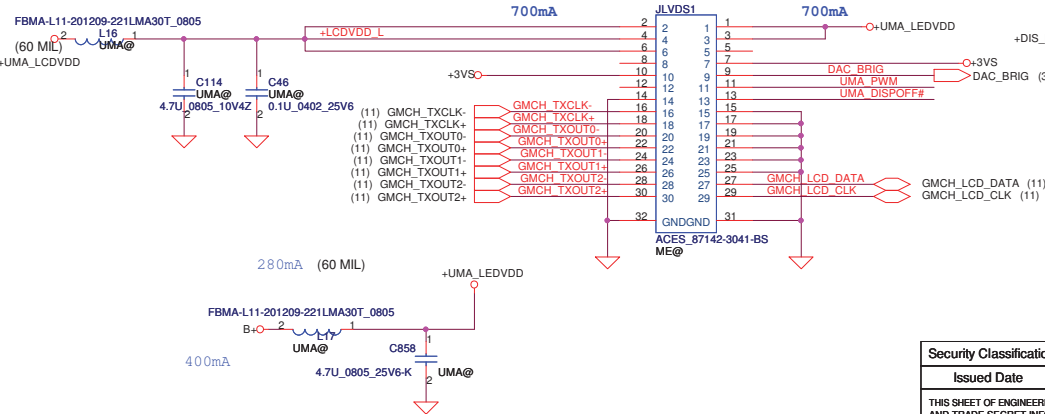
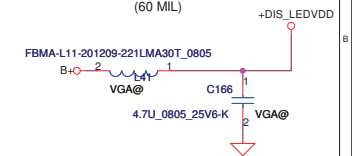
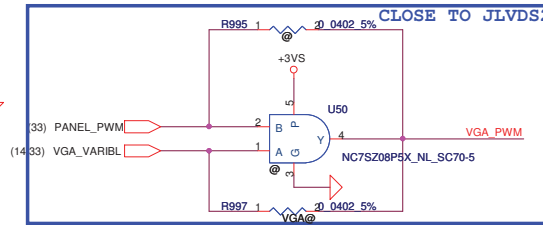
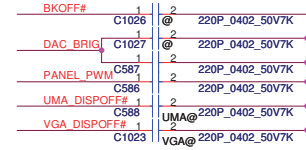
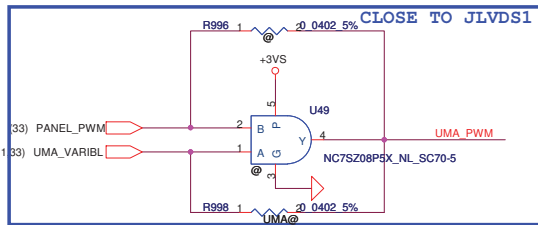
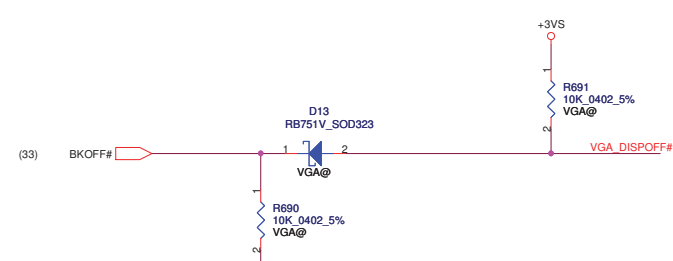
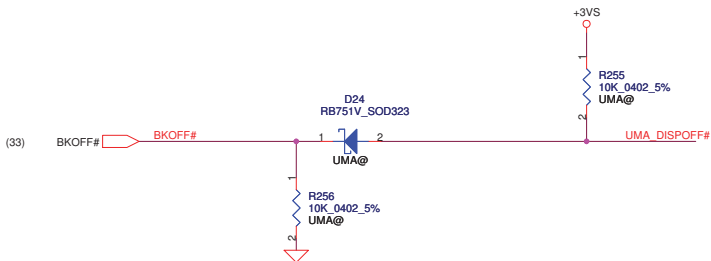
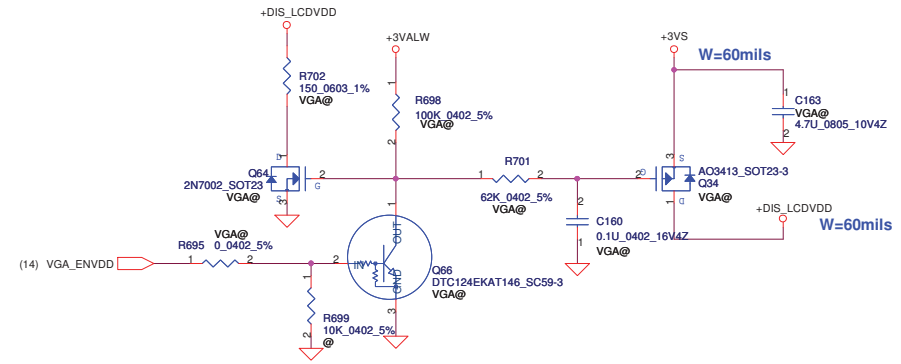
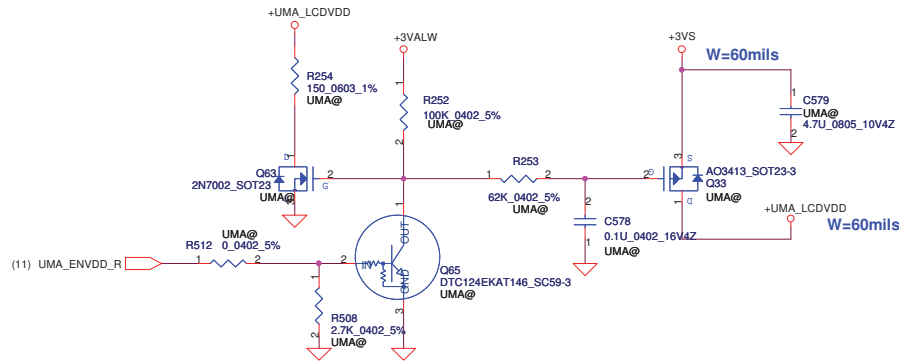
SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1	NON SPREAD 100M SATA SRC6 output
	0*	SPREAD 100M SATA SRC6 output

27M_SEL	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

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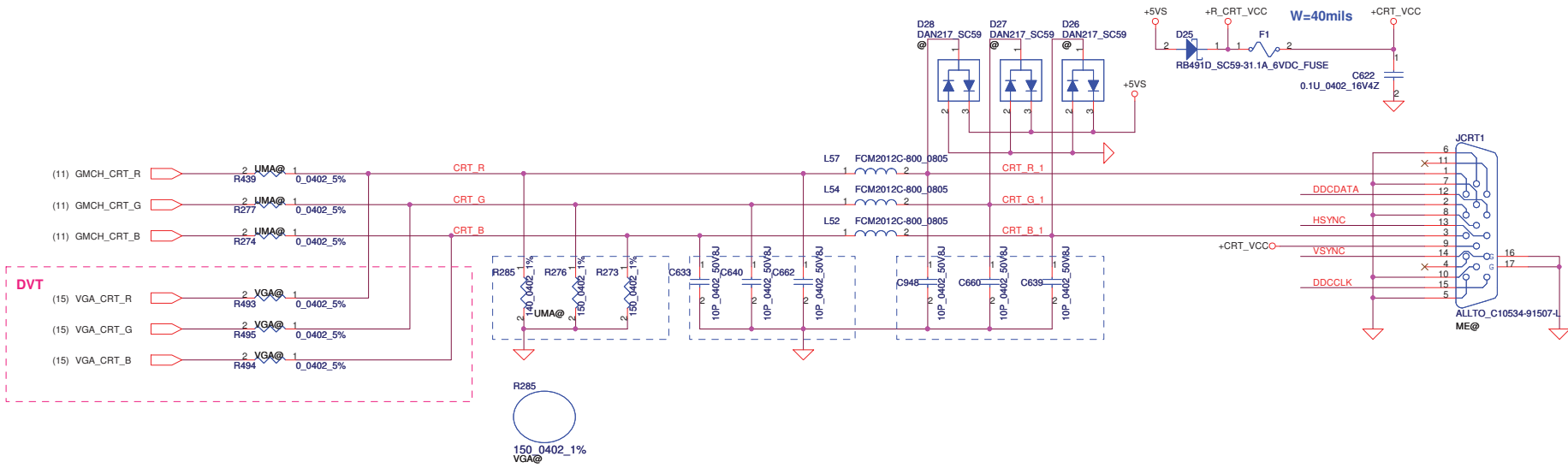
Compal Electronics, Inc.			
Clock generator			
Title	Size	Document Number	Rev
	Custom	LA-5971P	1.0
Date:	Thursday, December 10, 2009	Sheet	20 of 49

# LCD POWER CIRCUIT

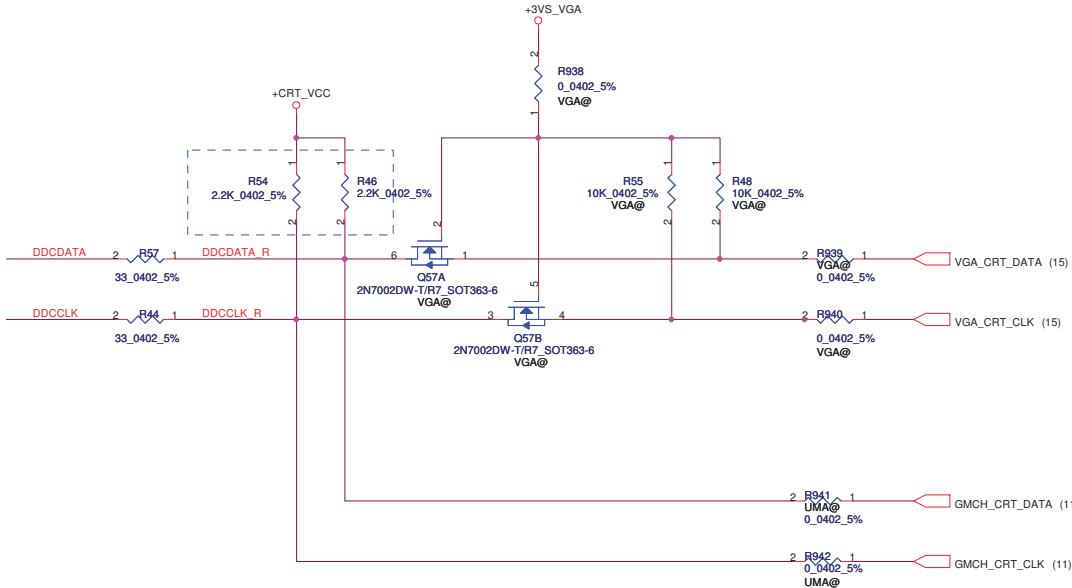
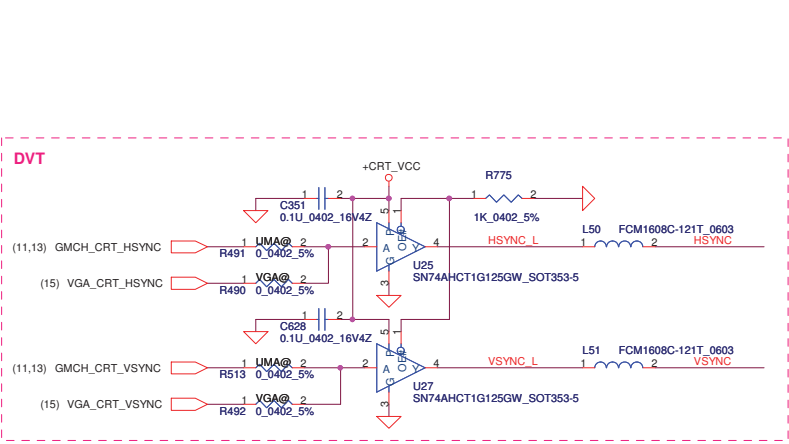


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Size B	Document Number	Date		LA-5971P	Rev 1.0
				Thursday, December 10, 2009	Sheet 21 of 49

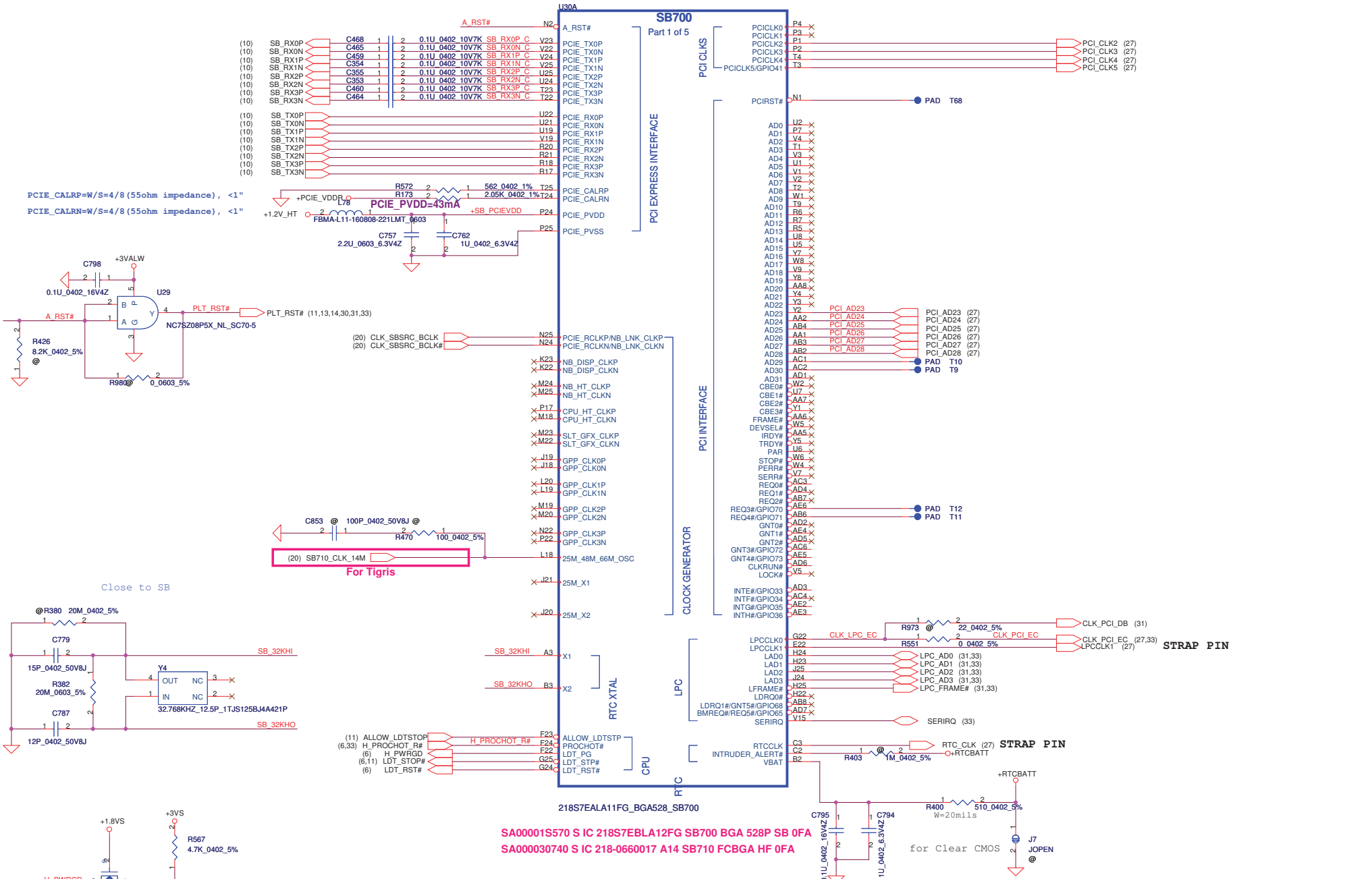
# CRT CONNECTOR



Place closed to chipset

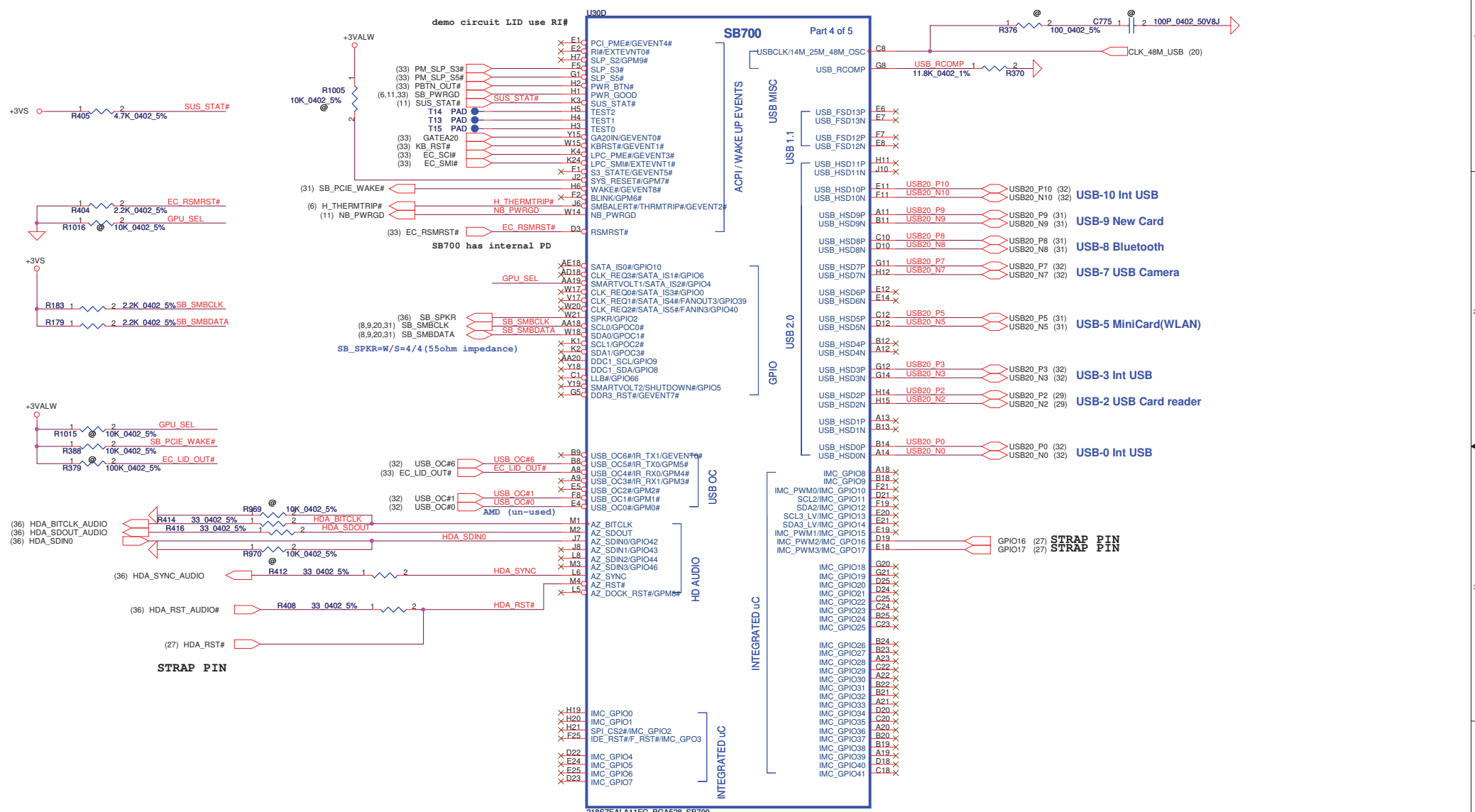


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Issued Date	2008/10/06	Deciphered Date	2009/10/06	CRT Connector	
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				Date:	Thursday, December 10, 2009
				Sheet	22 of 49
				Rev	1.0



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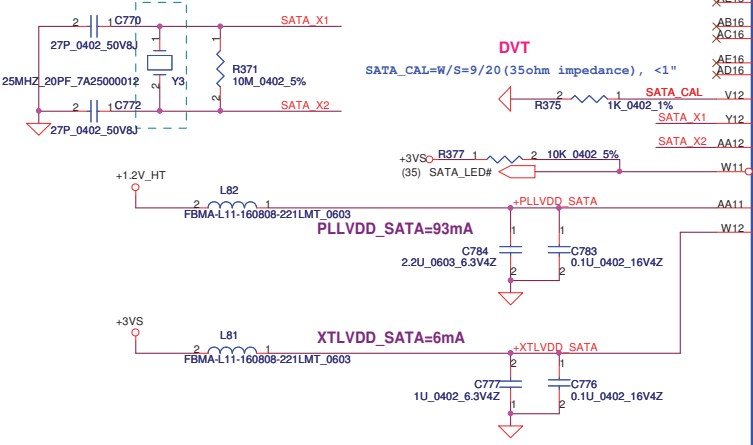
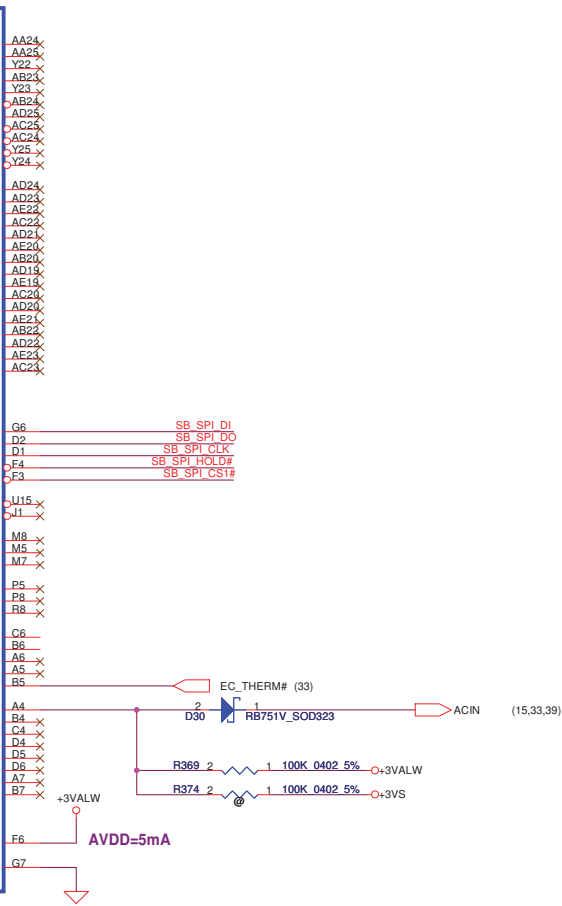
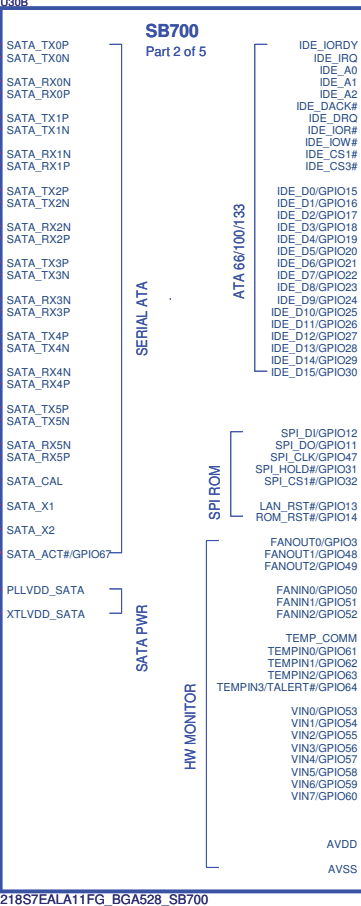
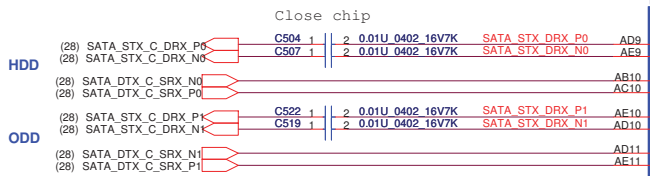
Compal Electronics, Inc.			
Title			
SB710-PCIE/PCI/ACPI/LPC/RTC			
Size	Document Number	Rev	
Custom	LA-5971P	1.0	
Date:	Thursday, December 10, 2009	Sheet	23 of 49



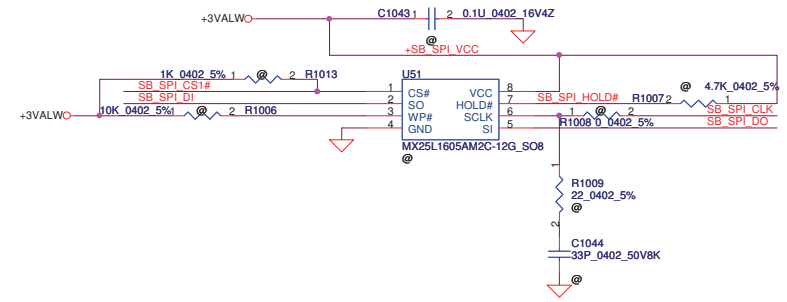
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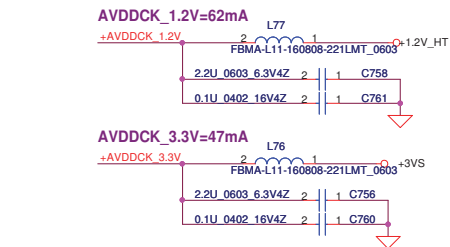
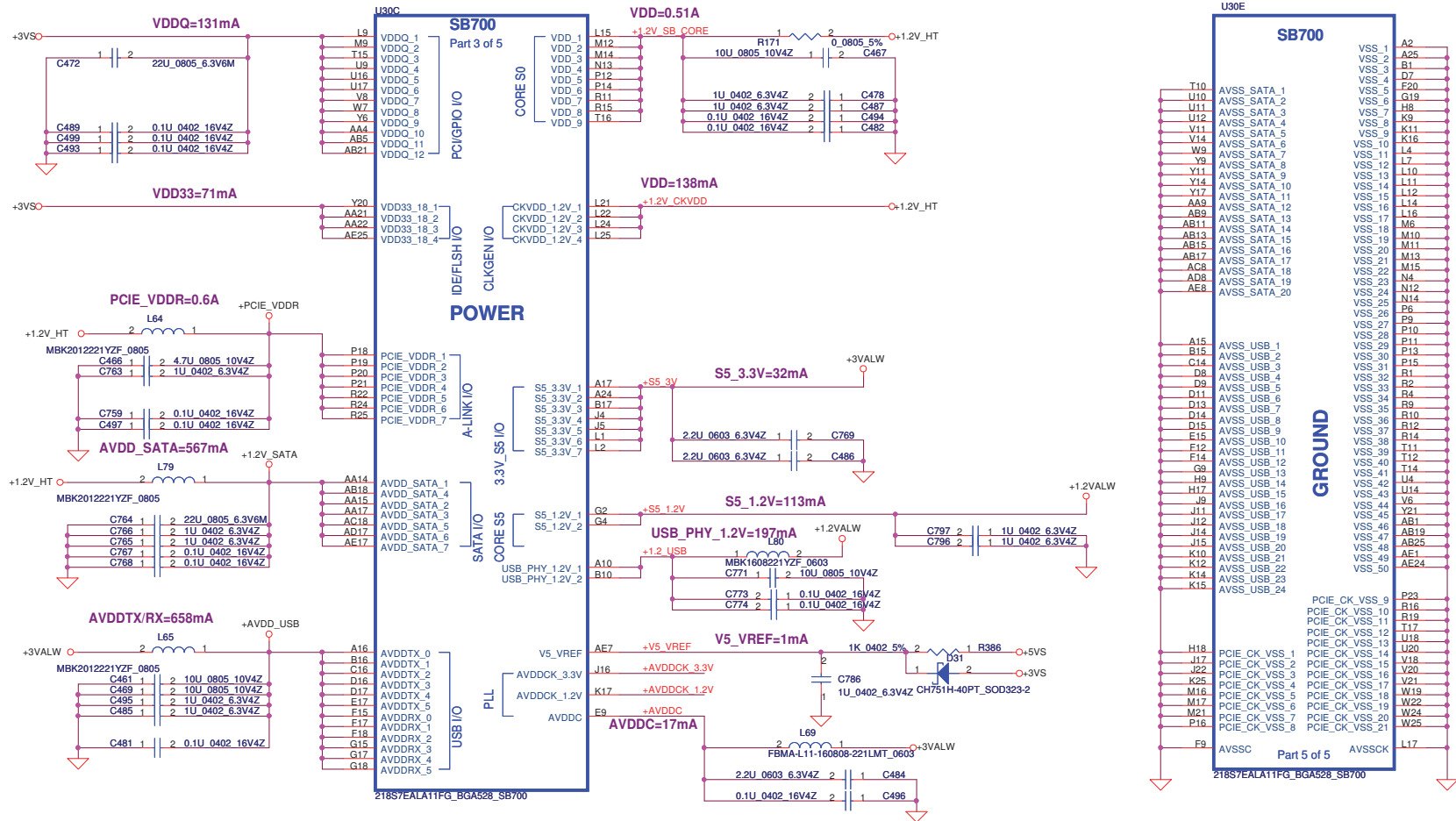
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
				SB710 USB/HD audio	
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		LA-5971P		Date: Thursday, December 10, 2009 E Sheet 24 of 49	





Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller





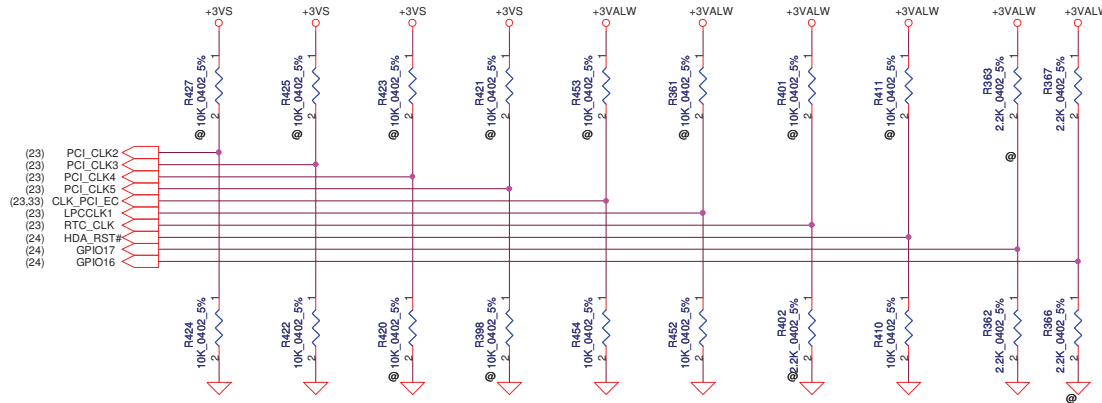
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06
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Compal Electronics, Inc.			
Title <b>SB710 power/GND</b>			
Size	Document Number	Rev	
Custom	LA-5971P	1.0	
Date:	Thursday, December 10, 2009	Sheet	26 of 49

# REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

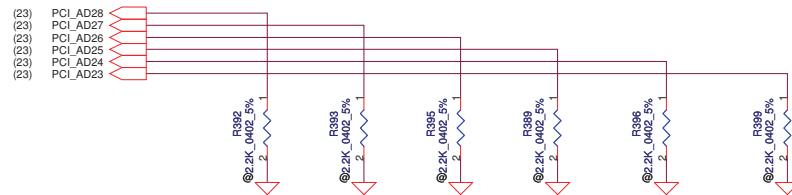
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	<b>INTERNAL RTC</b>  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	<b>L,H = LPC ROM (Default L,NC)</b> L,L = FWH ROM	



# DEBUG STRAPS

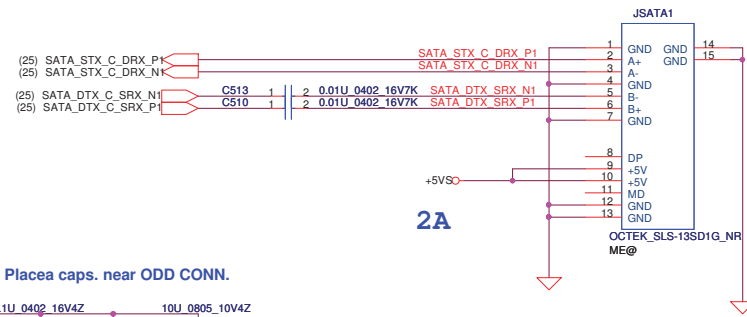
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



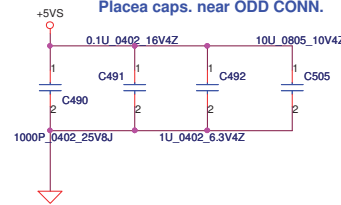
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
				SB710 STRAPS	
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				Date: Thursday, December 10, 2009	Rev 1.0
				Sheet 27	of 49

### SATA ODD Conn.

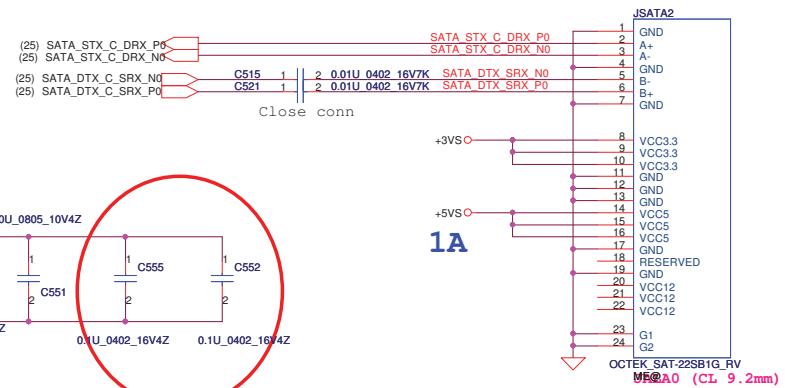


2A

Place caps. near ODD CONN.

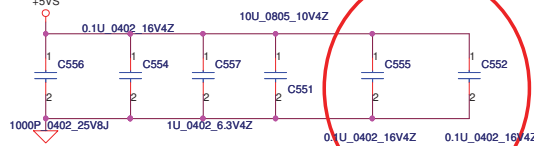
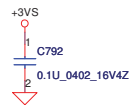


### SATA HDD Conn.



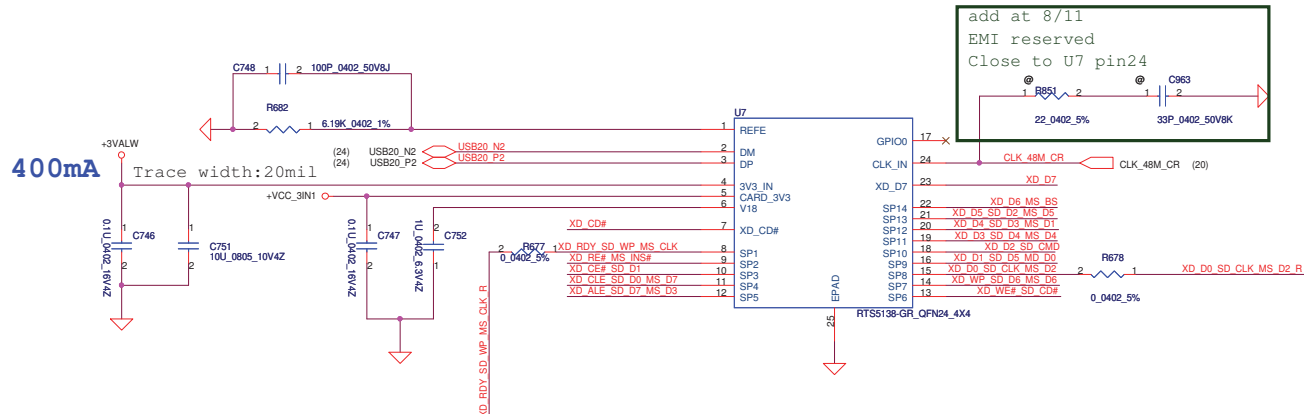
1A

Close conn

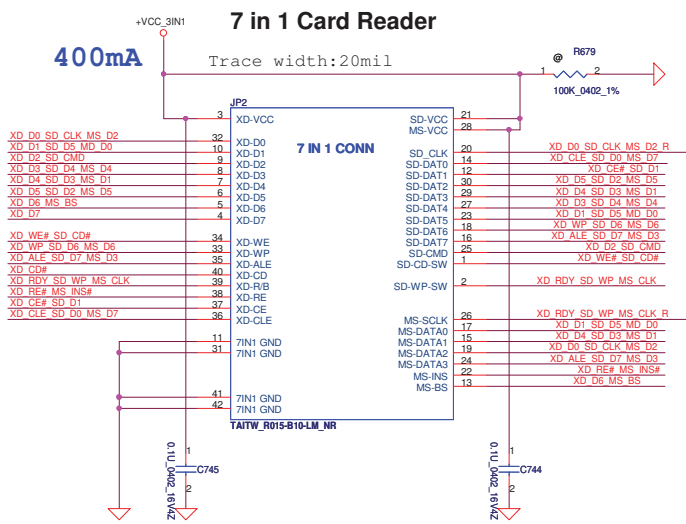
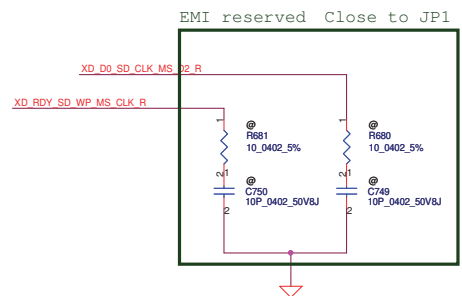


for ESD issue

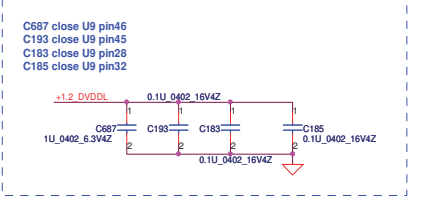
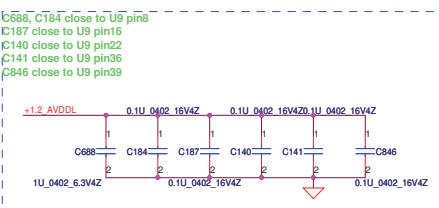
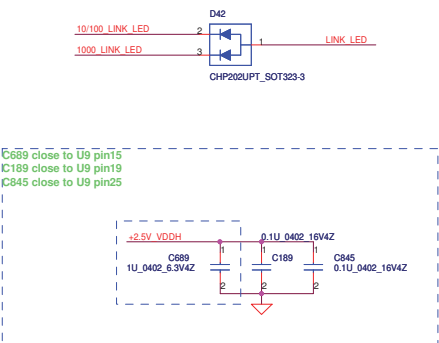
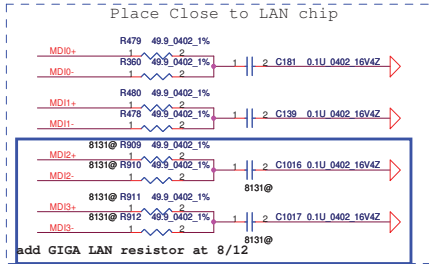
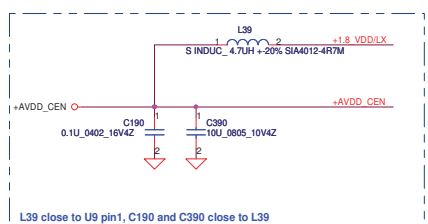
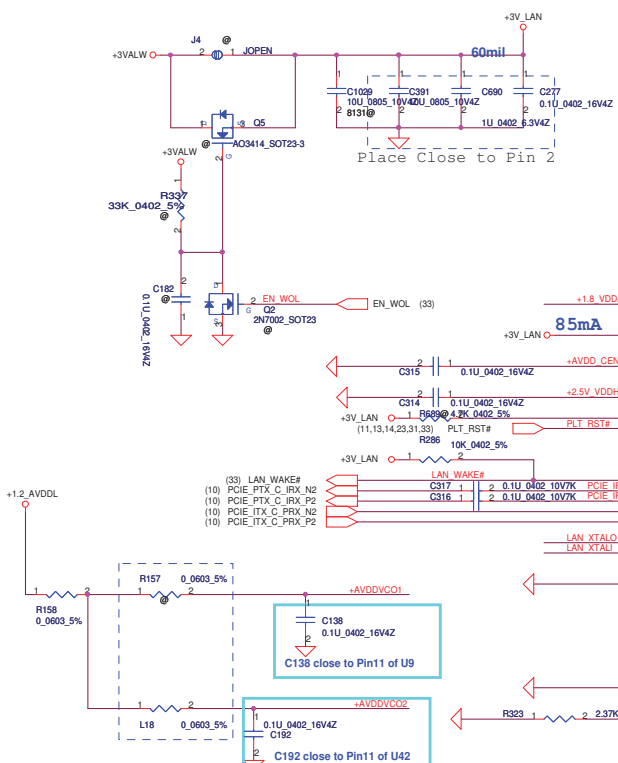
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	
				HDD & ODD Connector	
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				Date: Thursday, December 10, 2009	Rev 1.0
				Sheet 28	of 49



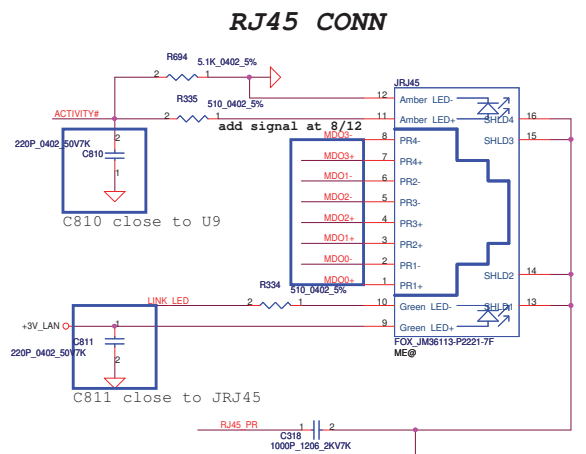
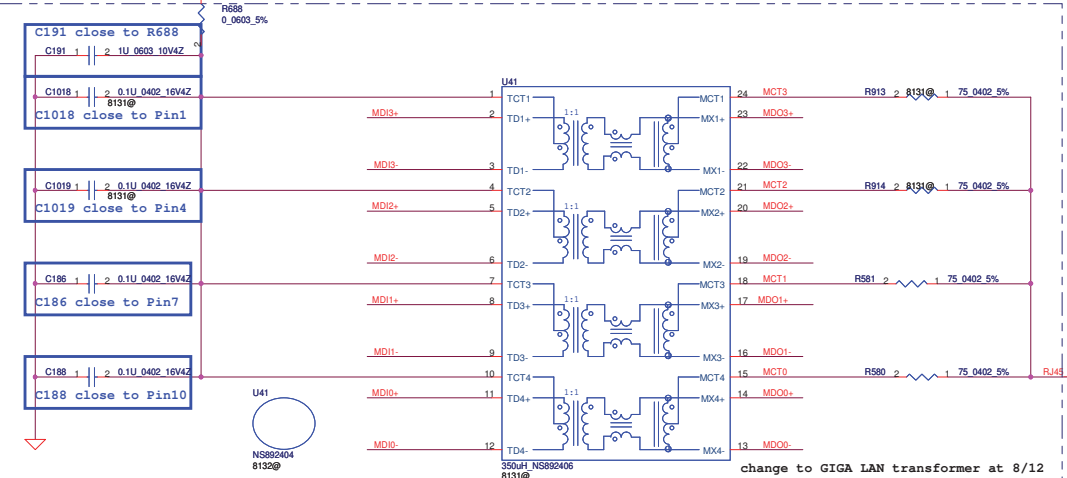
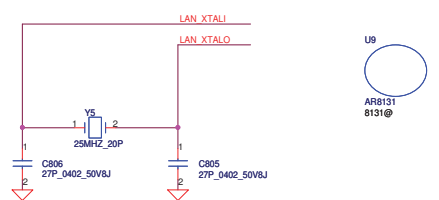
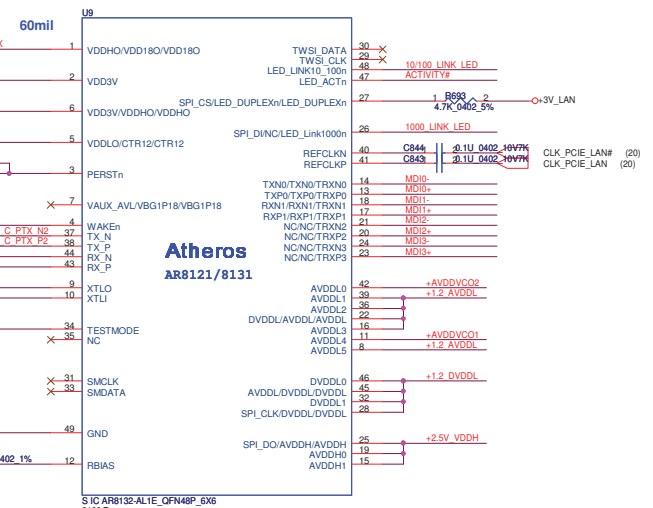
*Card reader(XD/SD/MMC/MS/MS-Pro HD SD)*



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Size	Document Number	Rev		
Custom	<b>LA-5971P</b>	1.0		
Date:	Thursday, December 10, 2009	Sheet	29	of 49



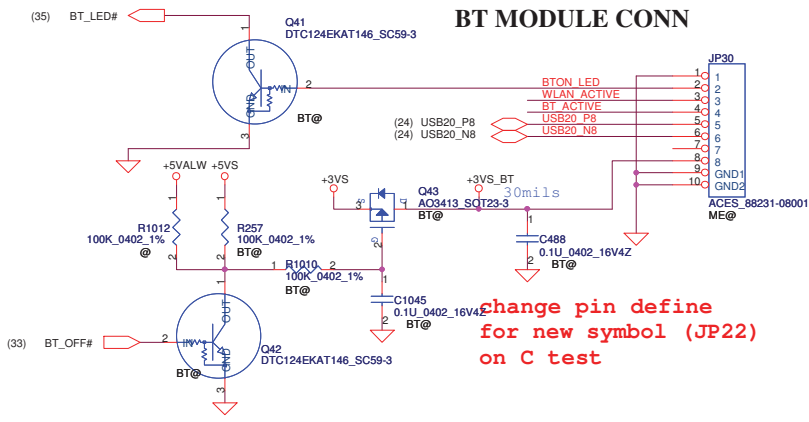
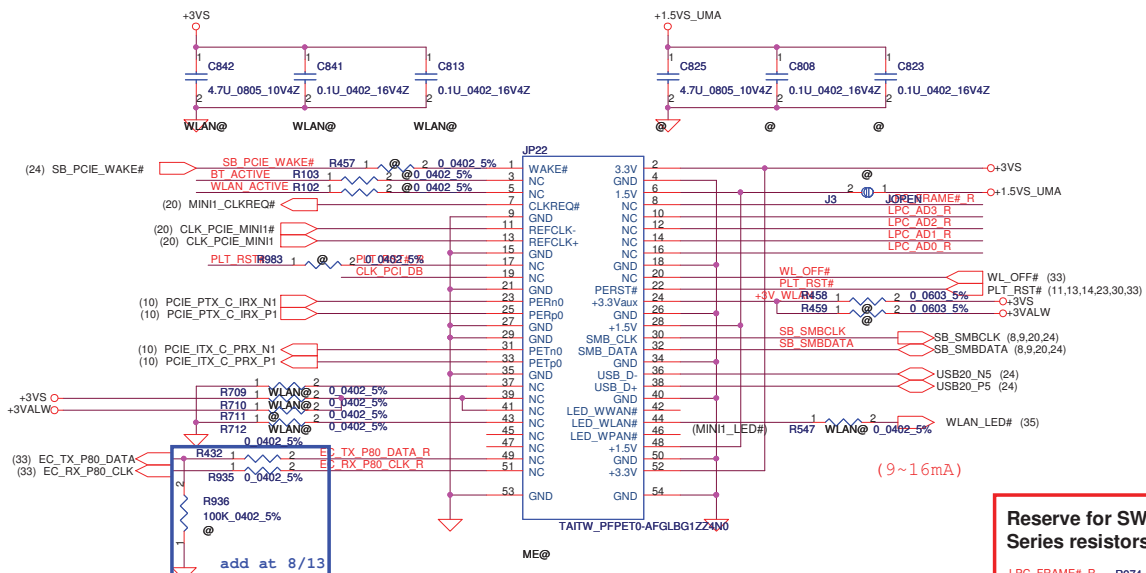
If overclocking, R157, L18 stuffed and R158 removed.  
If not overclocking, R158, L18 suffed and R157 removed.  
AR8131:L18=0ohm (more power saving mode)



<http://hobi-elektronika.net>

Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/16	Deciphered Date	2009/04/16	Atheros AR8132 & LAN CONN
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Document Number				Rev 1.0
LA-5971P				Date: Thursday, December 10, 2009 Sheet 30 of 49

# For Wireless LAN

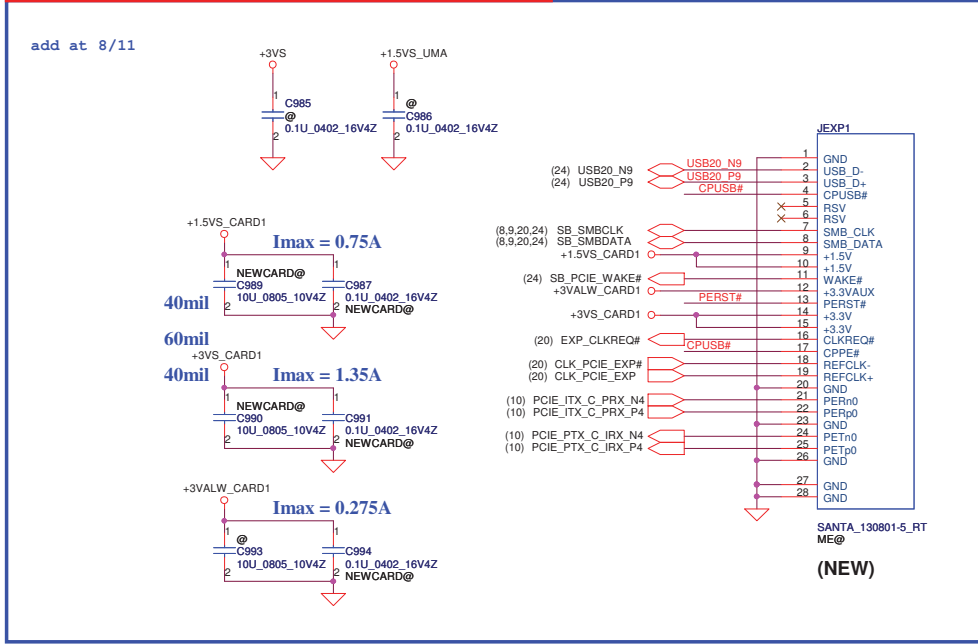
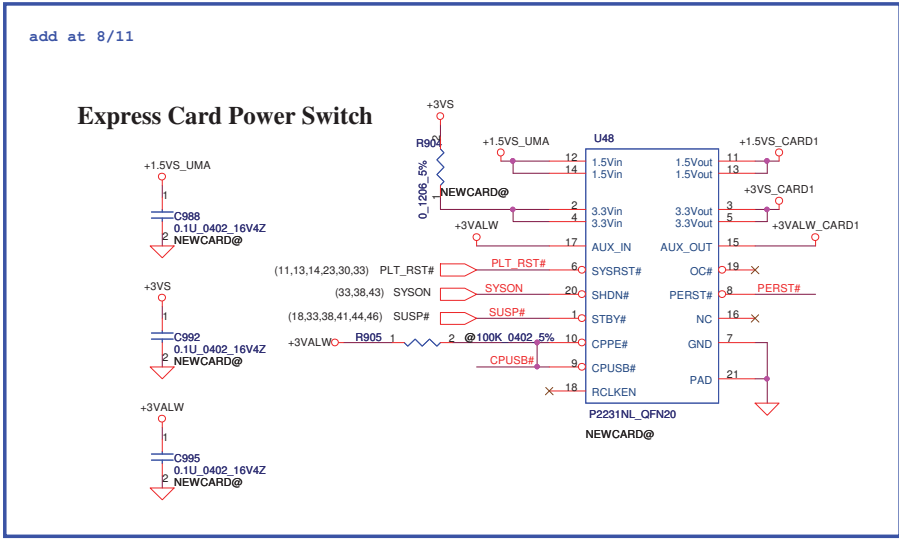


change pin define for new symbol (JP22) on C test

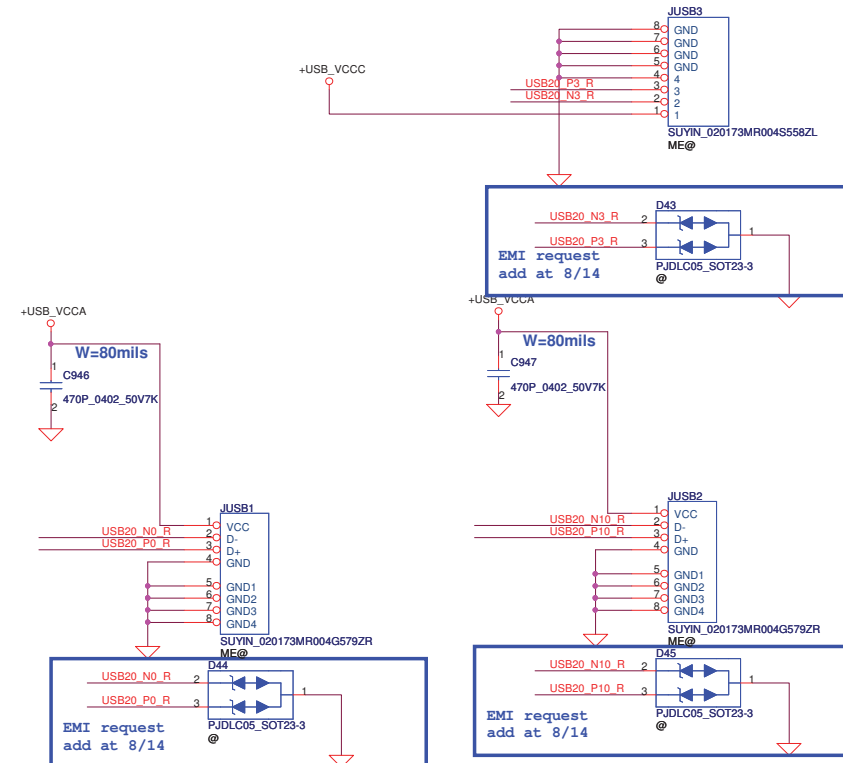
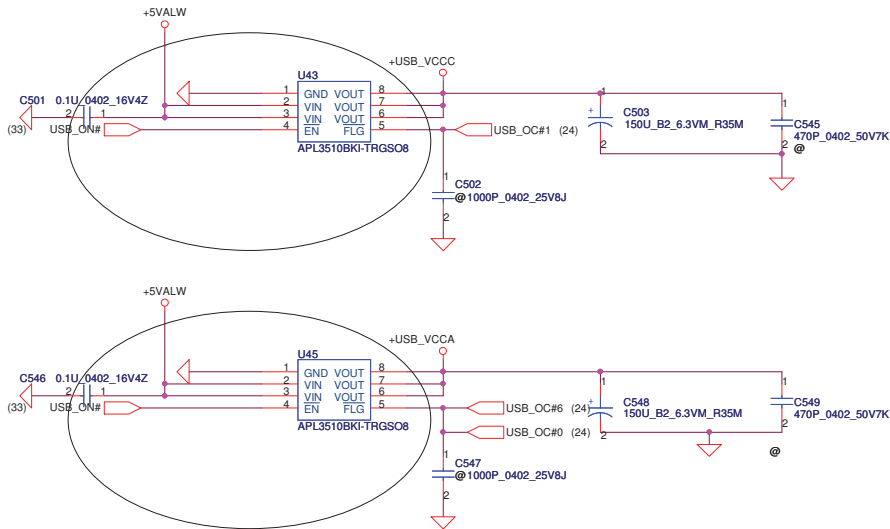
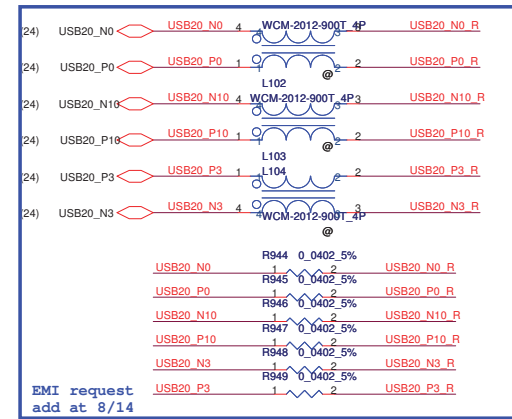
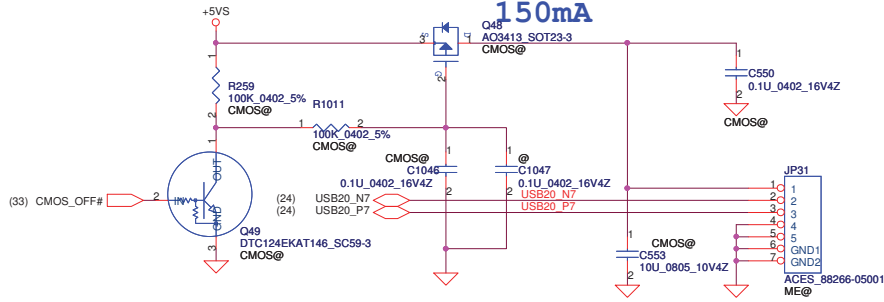
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

**Reserve for SW mini-pcie debug card. Series resistors closed to KBC side.**

LPC_FRAME#_R	R974	1	0.0402 5%	LPC_FRAME#	(23,33)
LPC_AD3_R	R975	1	0.0402 5%	LPC_AD3	(23,33)
LPC_AD2_R	R976	1	0.0402 5%	LPC_AD2	(23,33)
LPC_AD1_R	R977	1	0.0402 5%	LPC_AD1	(23,33)
LPC_AD0_R	R978	1	0.0402 5%	LPC_AD0	(23,33)
CLK_PCI_DB				CLK_PCI_DB	(23)

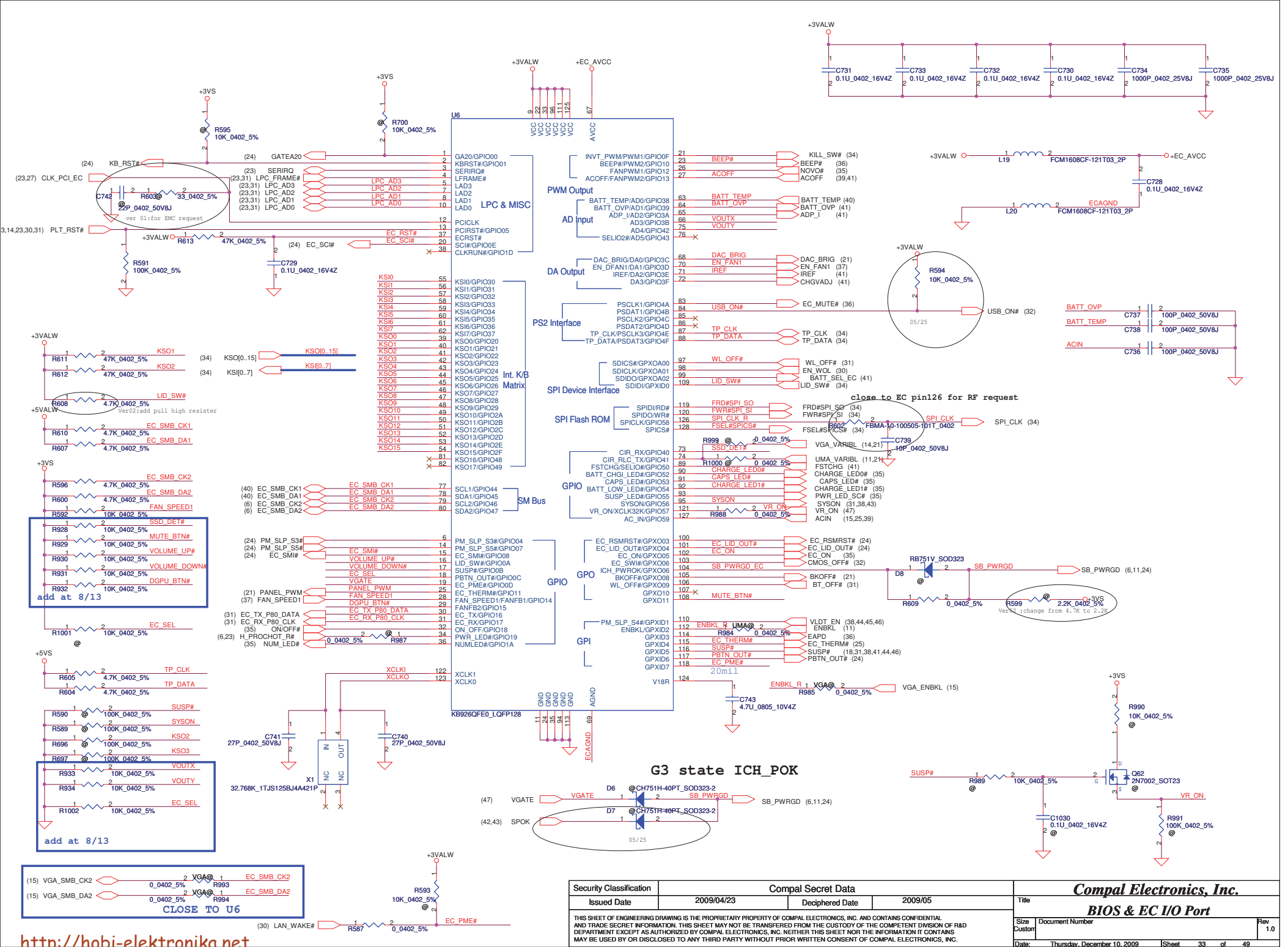


# CMOS Camera Conn

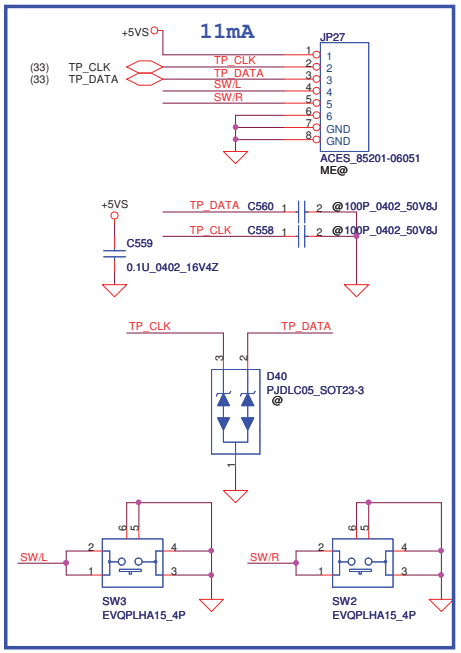
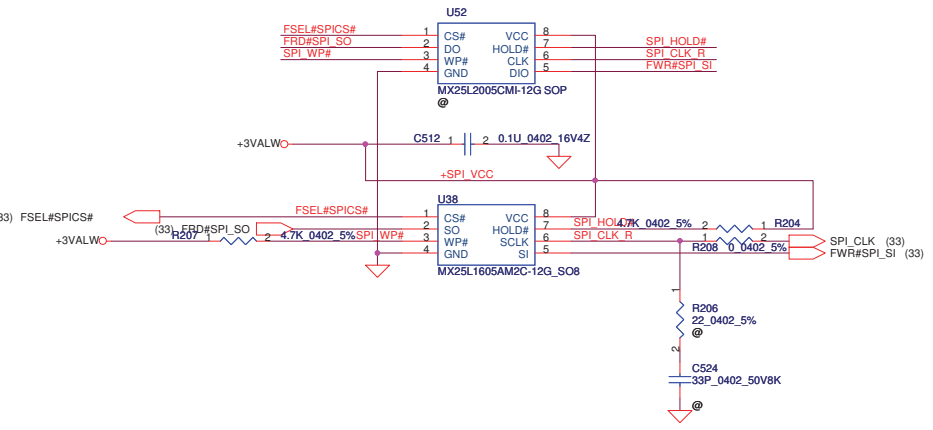


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Issued Date	2008/10/06	Deciphered Date	2009/10/06	BlueTooth / Int USB x2 / eSATA	
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				LA-5971P	Rev 1.0
				Date: Thursday, December 10, 2009	Sheet 32 of 49

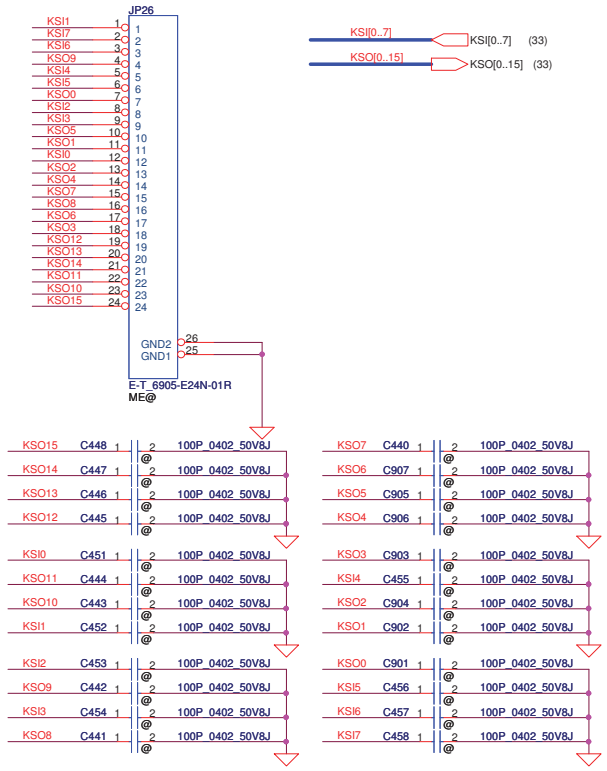




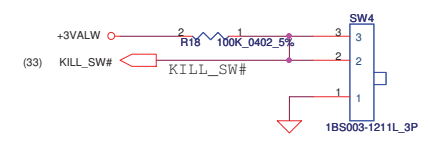
# BIOS(SYS / EC / VGA)



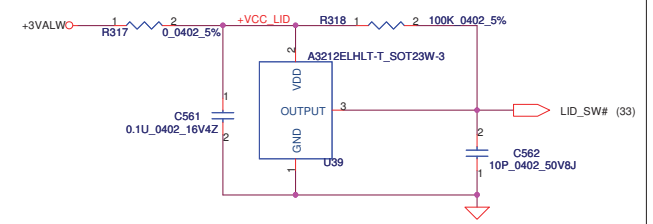
## INT\_KBD Conn.



## Kill Switch



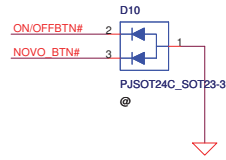
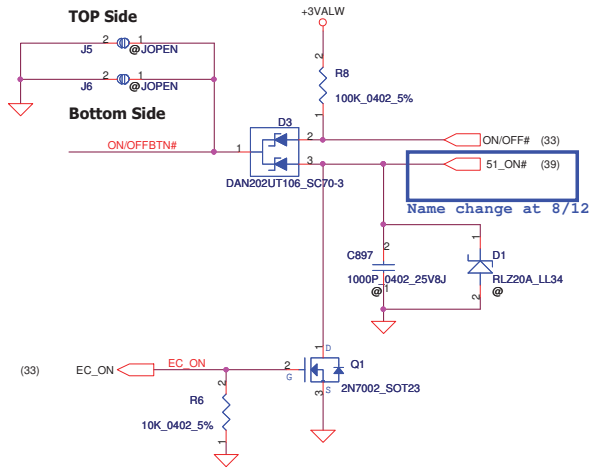
## Lid Switch



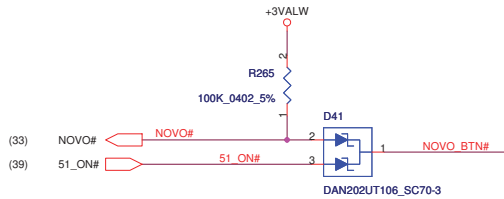
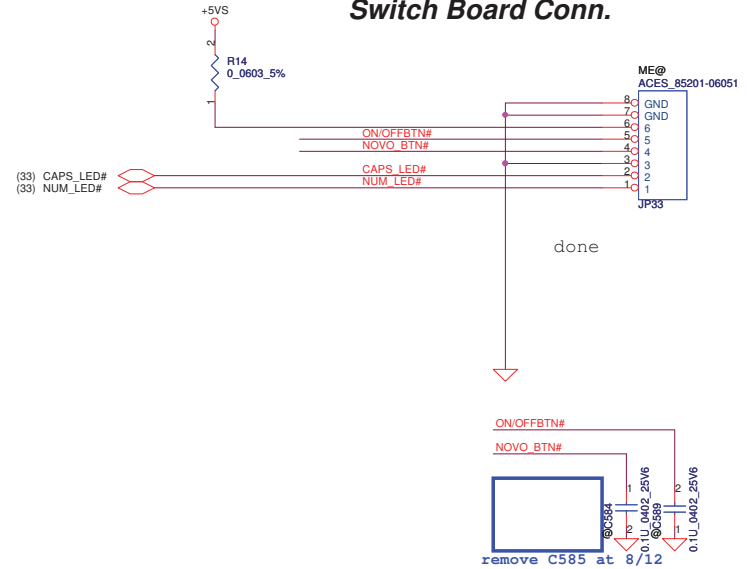
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Document Number			Rev	
B	LA-5971P			1.0	
Date:	Thursday, December 10, 2009	Sheet	34	of 49	

# Power Button

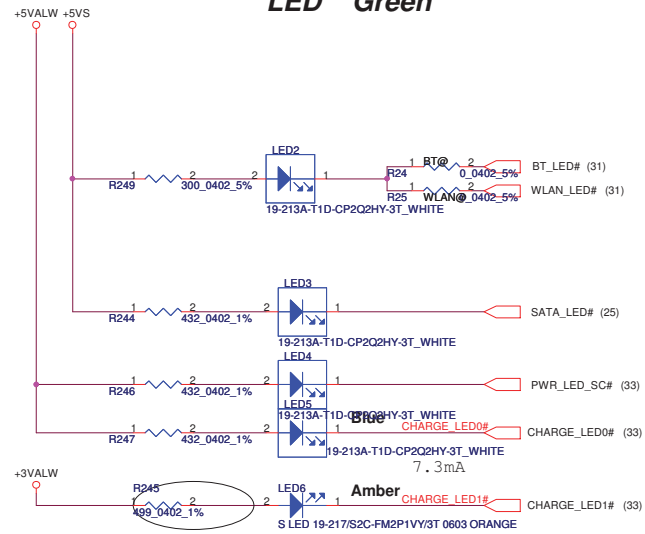
ON/OFF switch



# Switch Board Conn.



# LED Green

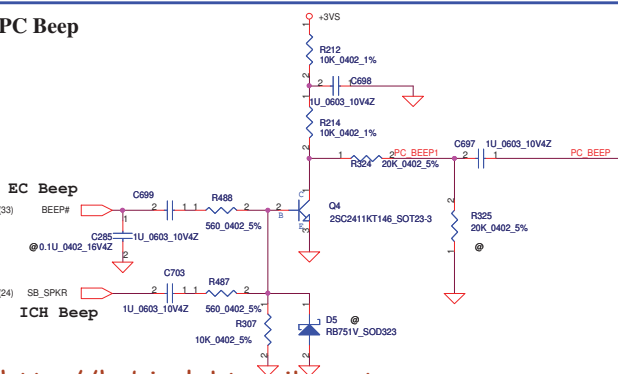
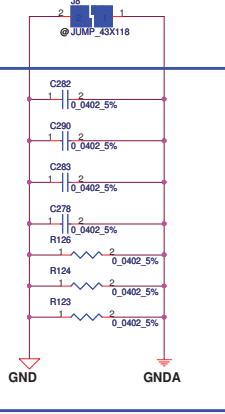
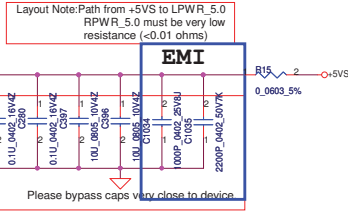
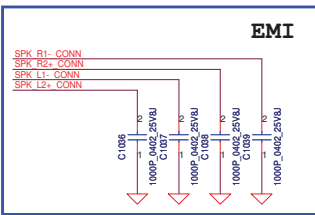
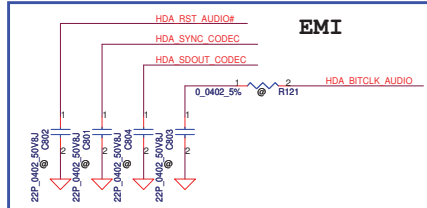
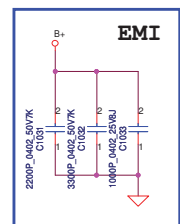
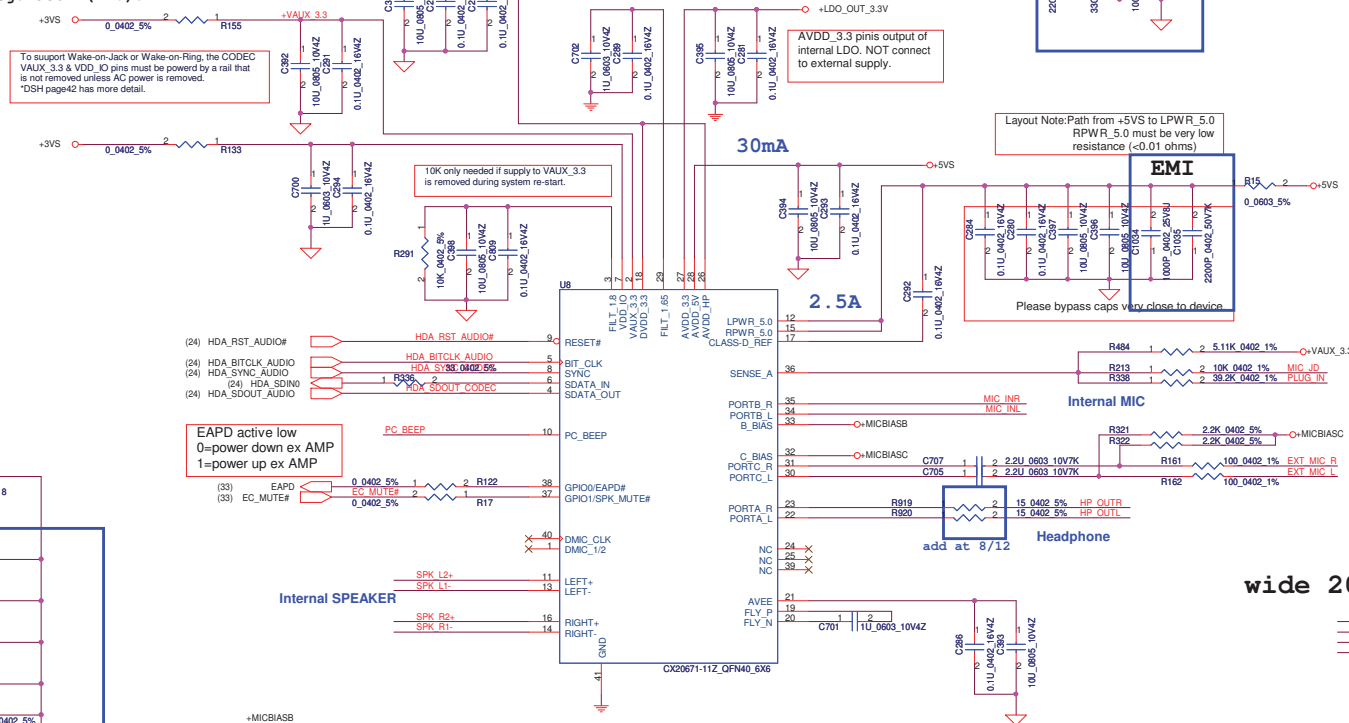


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				LA-5971P	
				Date:	Thursday, December 10, 2009
				Sheet	35 of 49
				Rev	1.0

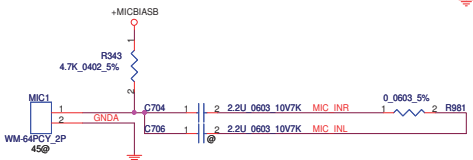
**CX20671**  
**High Definition Audio Codec SoC**  
**With Integrated Class-D Stereo**  
**Amplifier.**

An integrated 5 V to 3.3 V Low-dropout  
voltage regulator (LDO).

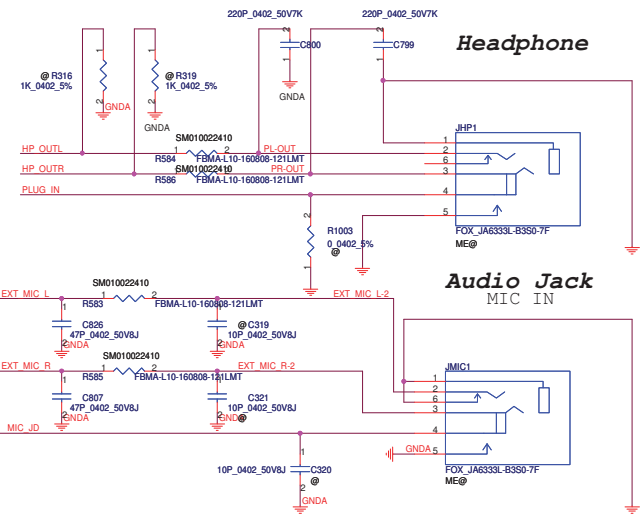
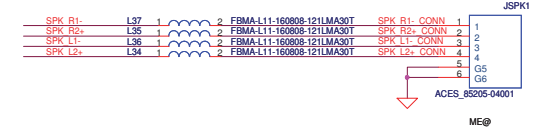
An integrated 3.3 V to 1.8V Low-dropout  
voltage regulator (LDO).



**Audio Jack**

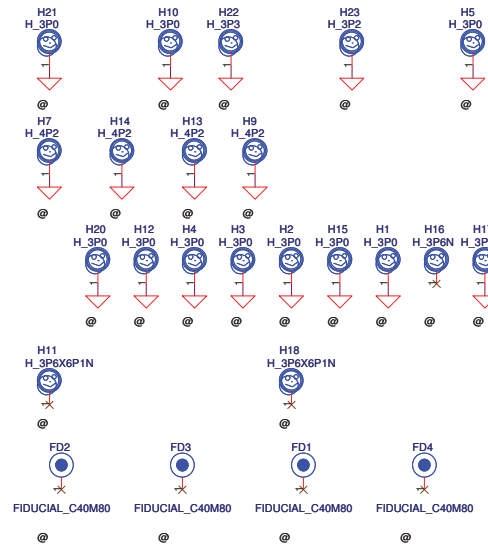
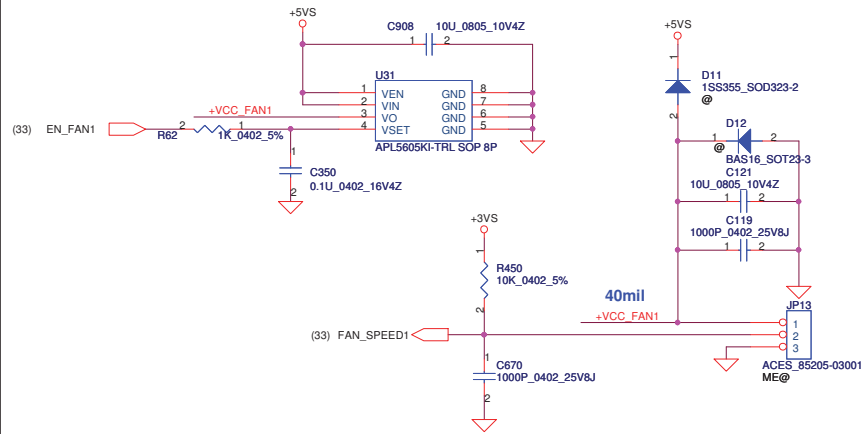


**wide 20MIL**



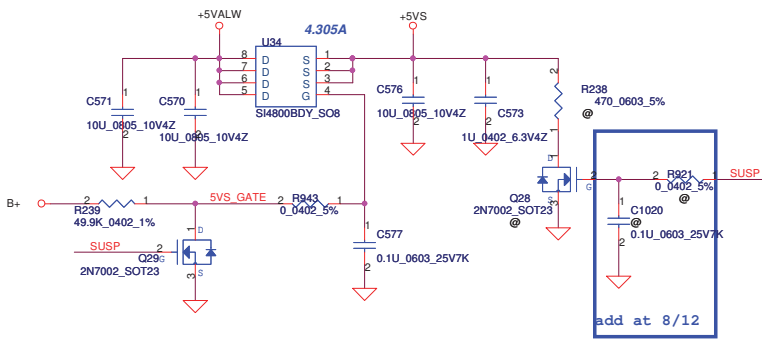
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title
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Size	C	Document Number	LA-5971P	Rev
Date:	Thursday, December 10, 2009	Sheet	36	of 49

### FAN1 Conn

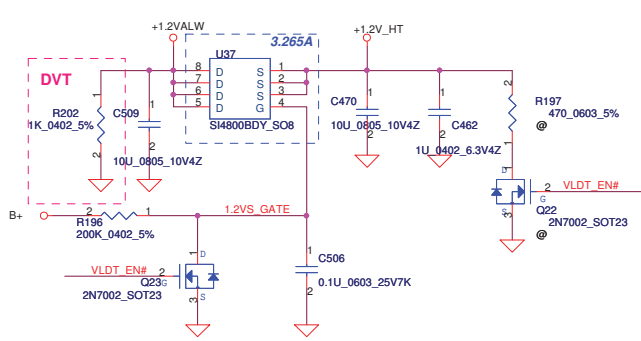


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Size	Document Number			Rev
B	LA-5971P			1.0
Date:	Thursday, December 10, 2009	Sheet	37	of 49

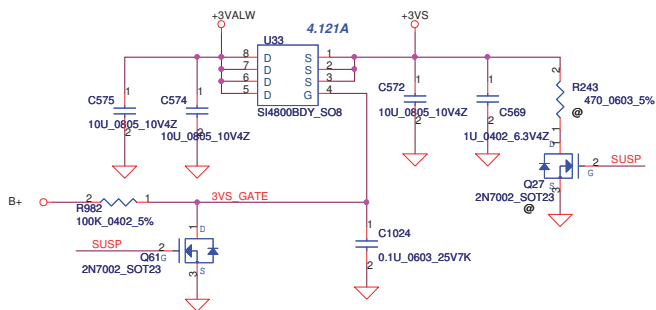
**+5VALW TO +5VS**



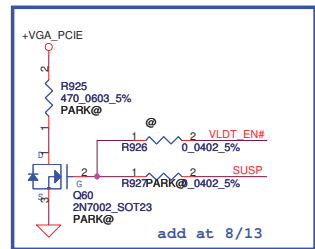
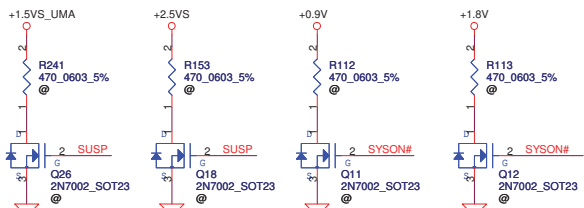
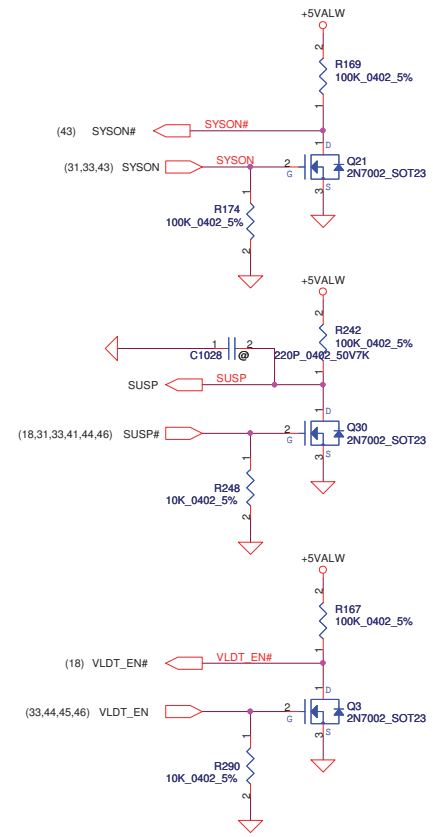
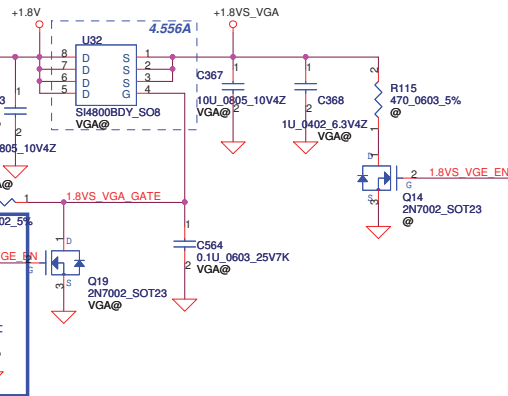
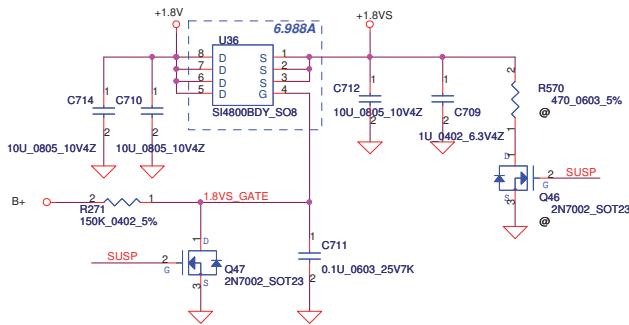
**+1.2VALW TO +1.2V\_HT**



**+3VALW TO +3VS**



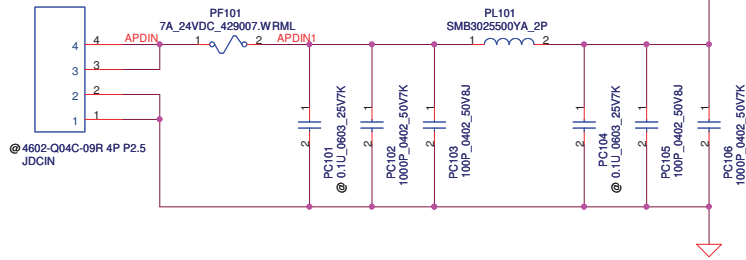
**+1.8V to +1.8VS**



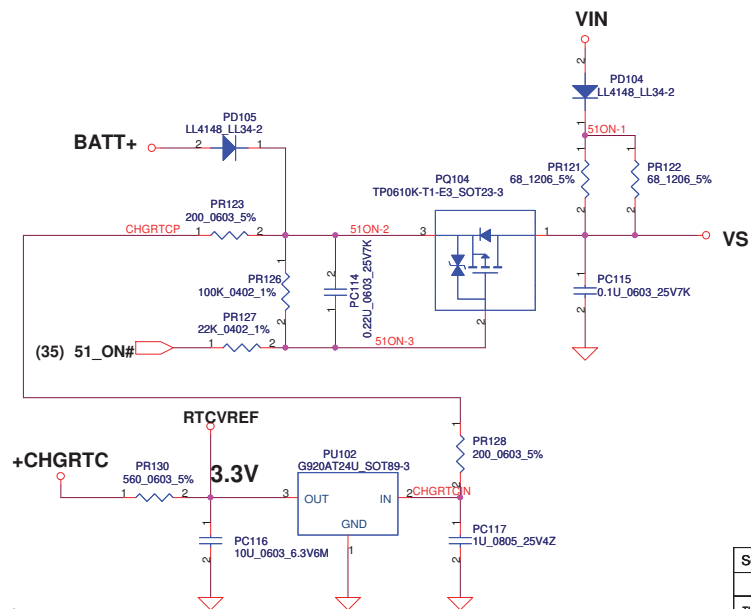
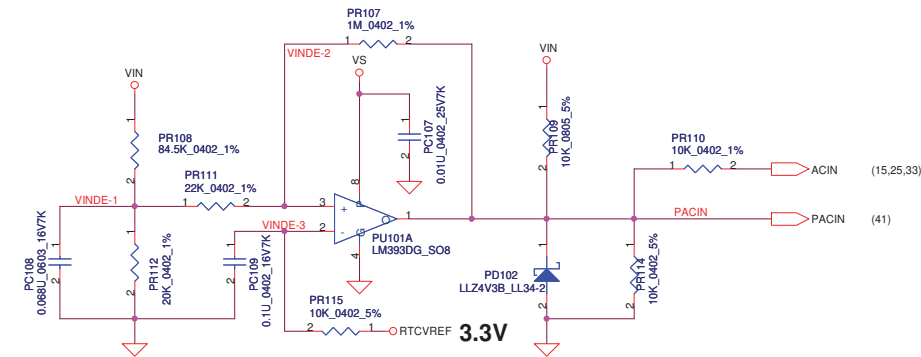
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06
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Compal Electronics, Inc.			
Title <b>DC Interface</b>			
Size B	Document Number <b>LA-5971P</b>	Rev 1.0	
Date:	Thursday, December 10, 2009	Sheet	38 of 49

DC030006J00

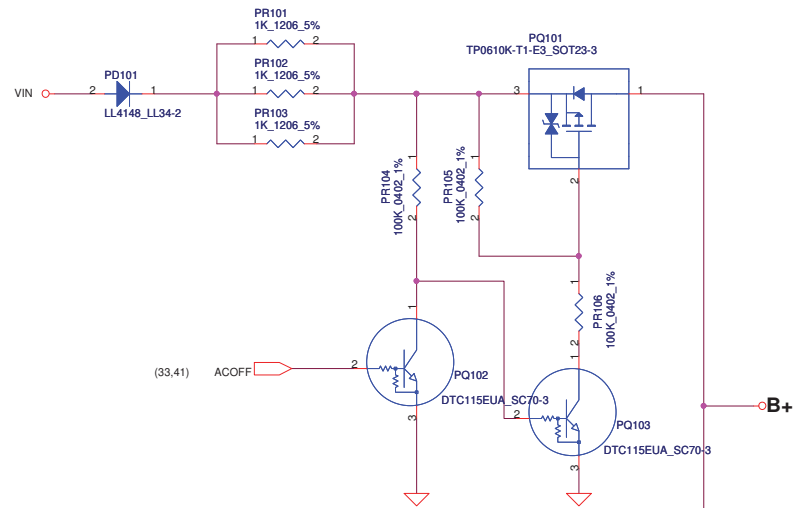


Vin Detector			
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



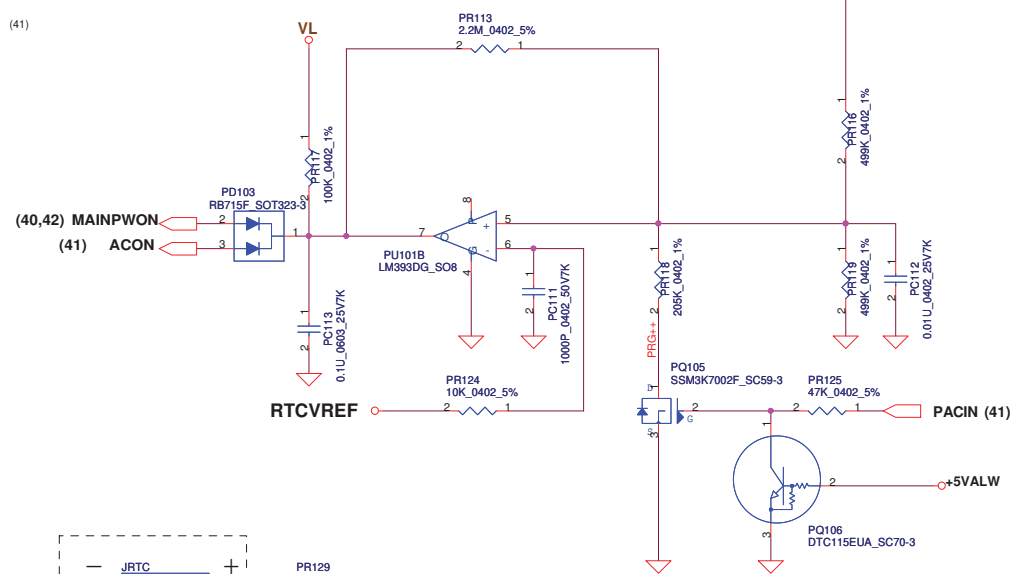
ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

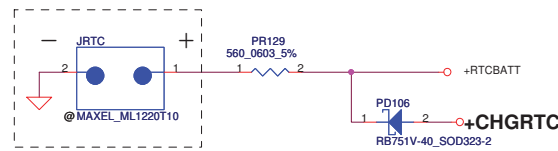


BATT ONLY

Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

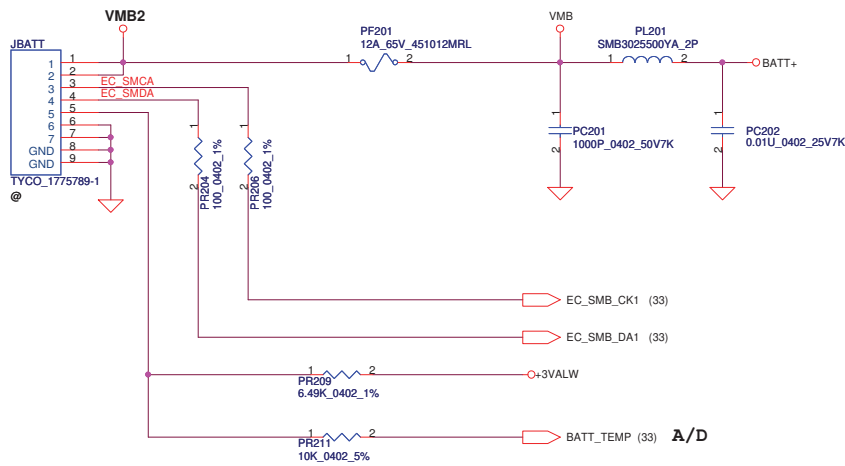


RTC Battery

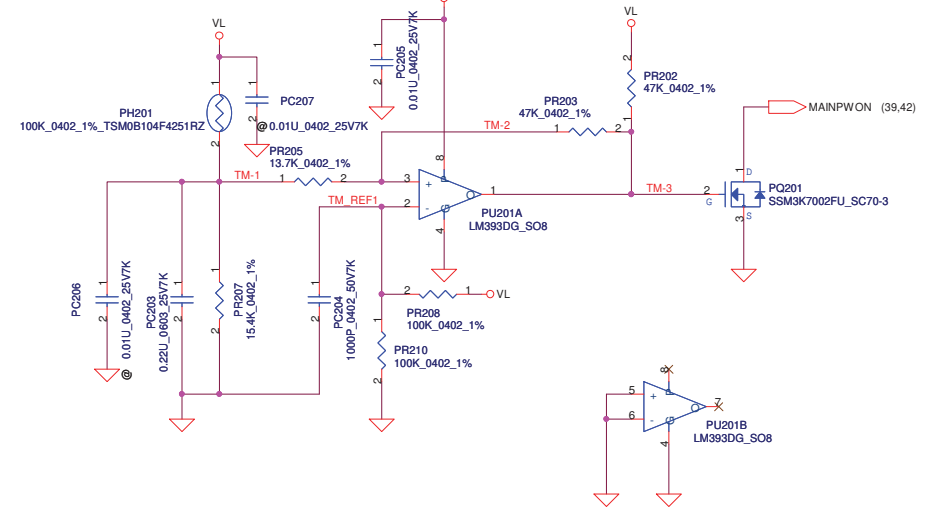


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Title		
DCIN & DETECTOR		
Size	Document Number	Rev
Custom		1.0
Date:	Thursday, December 10, 2009	Sheet 39 of 49

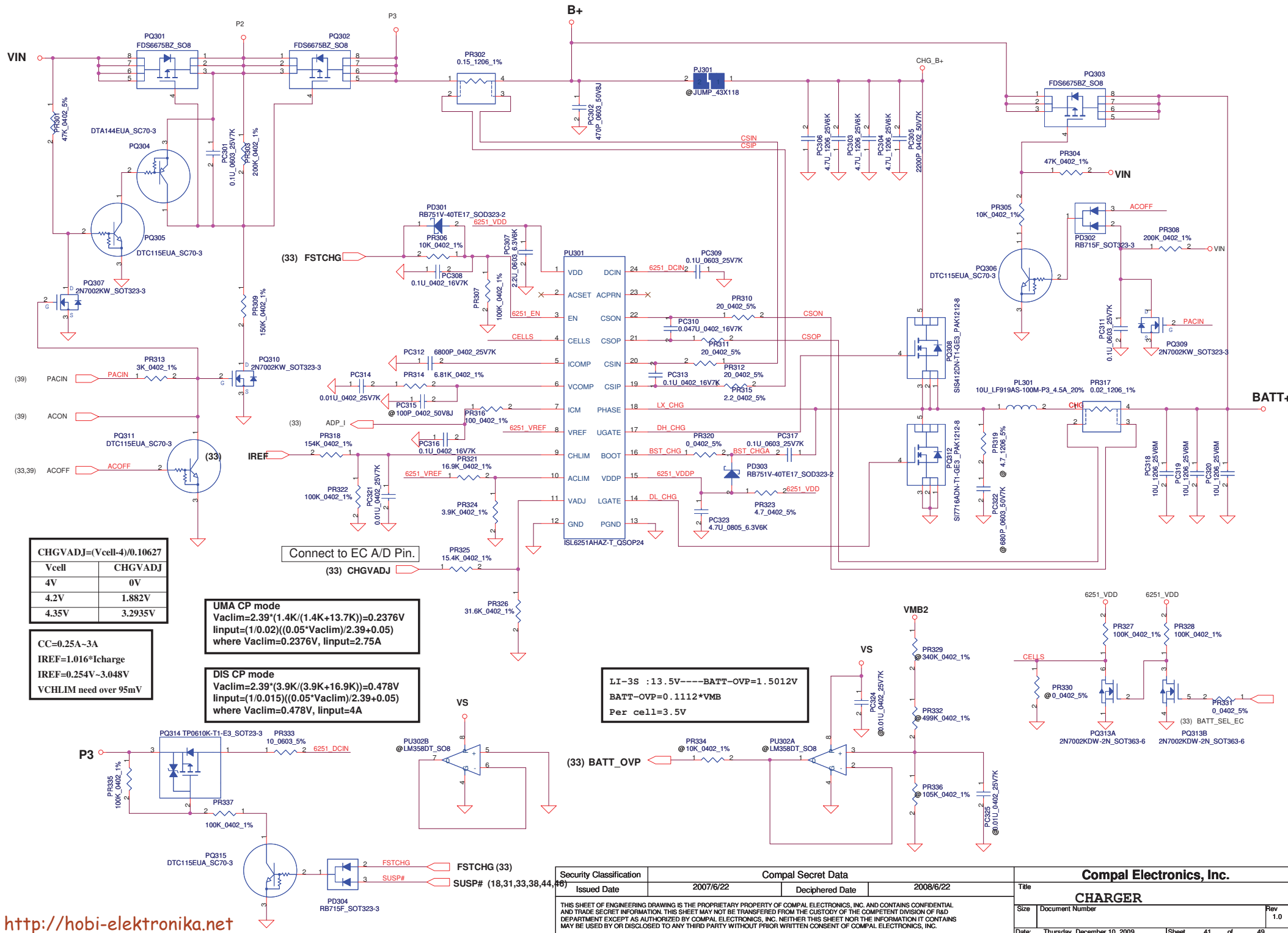


PH1 under CPU botten side :  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



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				Date:	Thursday, December 10, 2009
				Sheet	40 of 49
				Rev	1.0





$CHGVADJ = (V_{cell} - 4) / 0.10627$

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A  
 IREF=1.016\*Icharge  
 IREF=0.254V-3.048V  
 VCHLIM need over 95mV

**UMA CP mode**  
 $Va_{lim} = 2.39 * (1.4K + (1.4K + 13.7K)) = 0.2376V$   
 $in_{put} = (1 / 0.02) * ((0.05 * Va_{lim}) / 2.39 + 0.05)$   
 where  $Va_{lim} = 0.2376V$ ,  $in_{put} = 2.75A$

**DIS CP mode**  
 $Va_{lim} = 2.39 * (3.9K + (3.9K + 16.9K)) = 0.478V$   
 $in_{put} = (1 / 0.015) * ((0.05 * Va_{lim}) / 2.39 + 0.05)$   
 where  $Va_{lim} = 0.478V$ ,  $in_{put} = 4A$

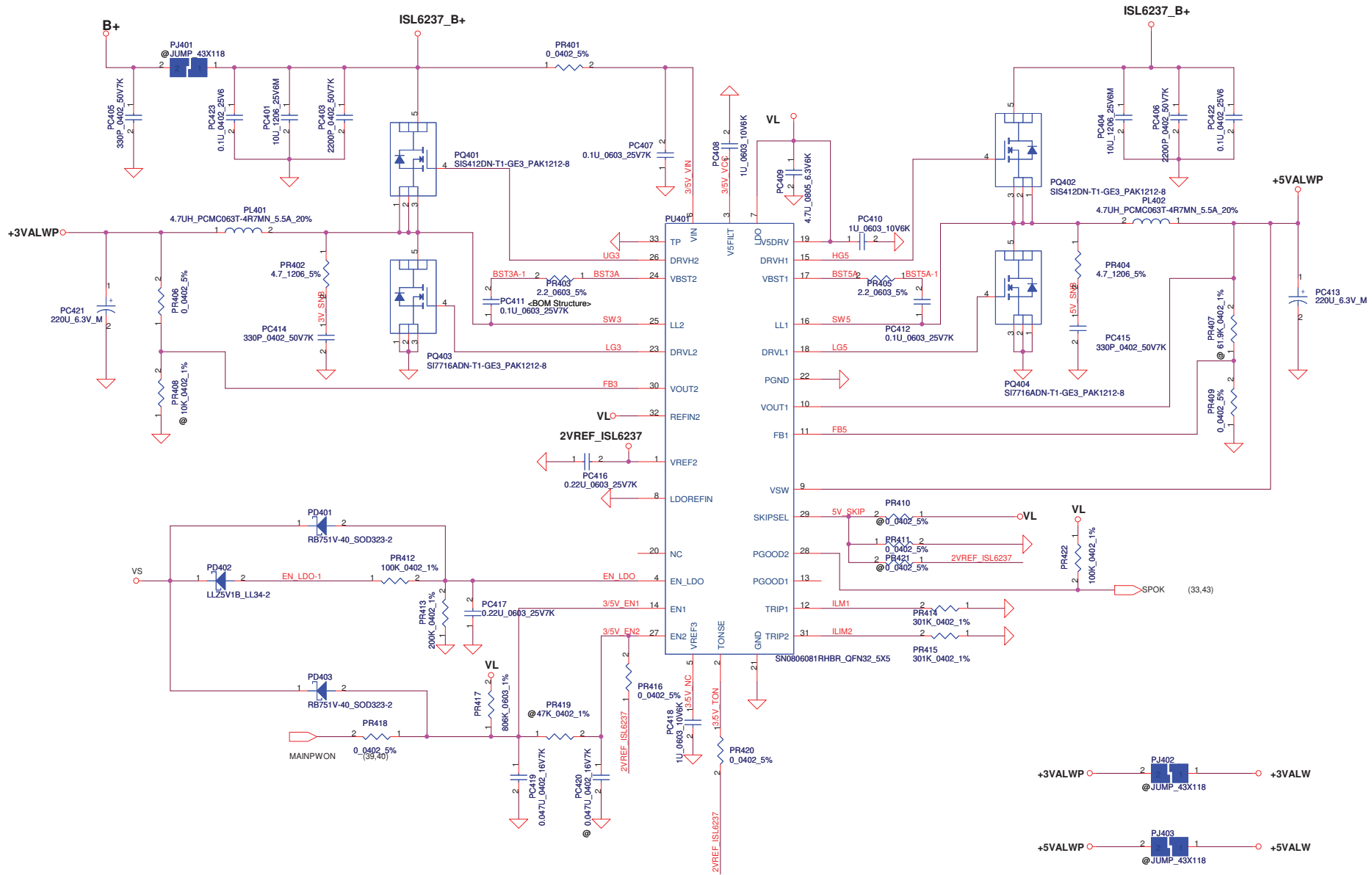
**LI-3S : 13.5V --- BATT-OVP = 1.5012V**  
 $BATT-OVP = 0.1112 * VMB$   
 Per cell = 3.5V

Connect to EC A/D Pin.  
 (33) CHGVADJ

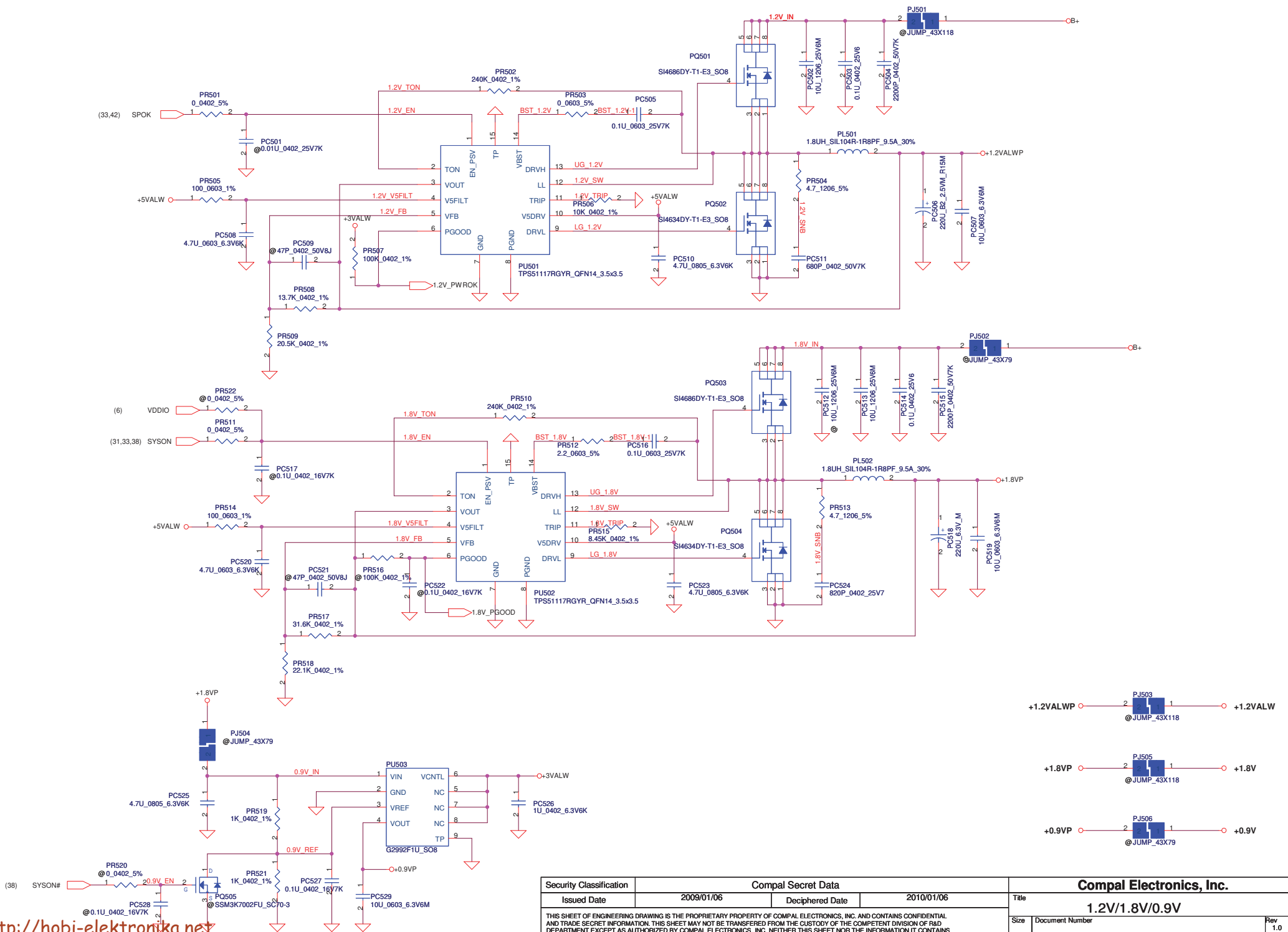
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		2008/6/22

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Title		
<b>CHARGER</b>		
Size	Document Number	Rev
		1.0
Date:	Thursday, December 10, 2009	Sheet 41 of 49



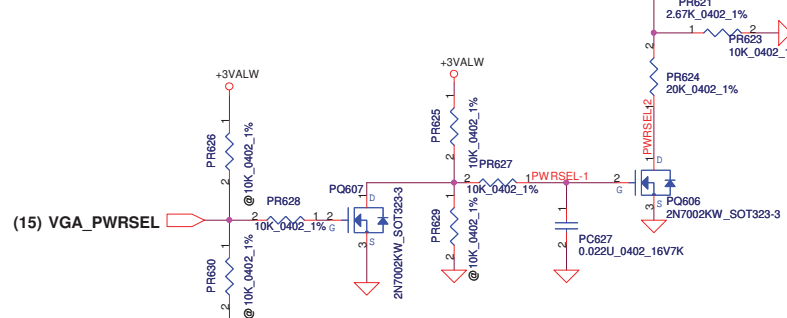
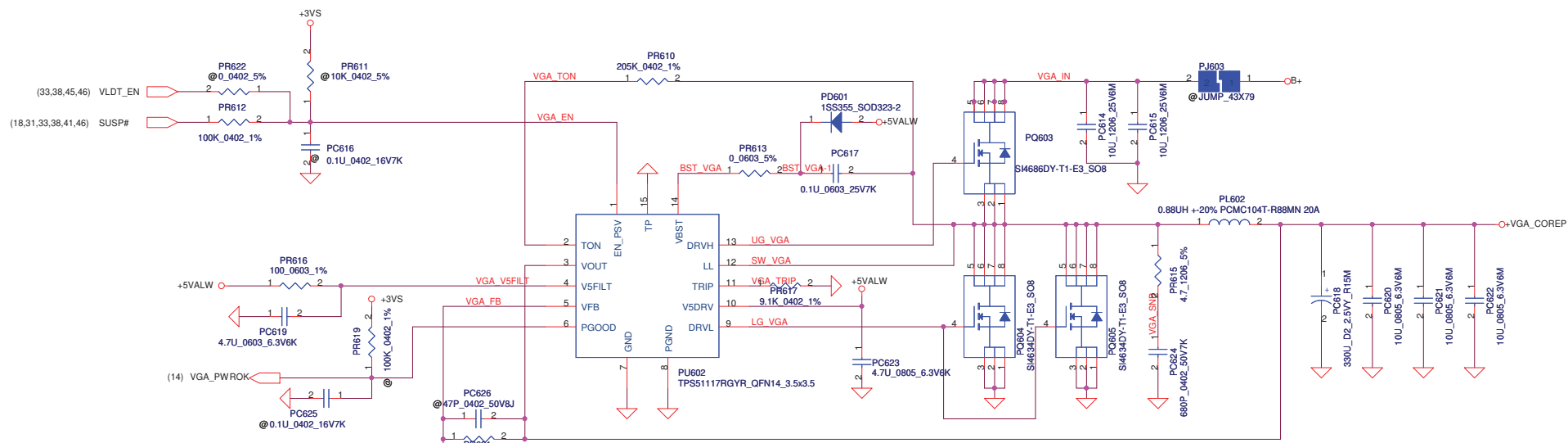
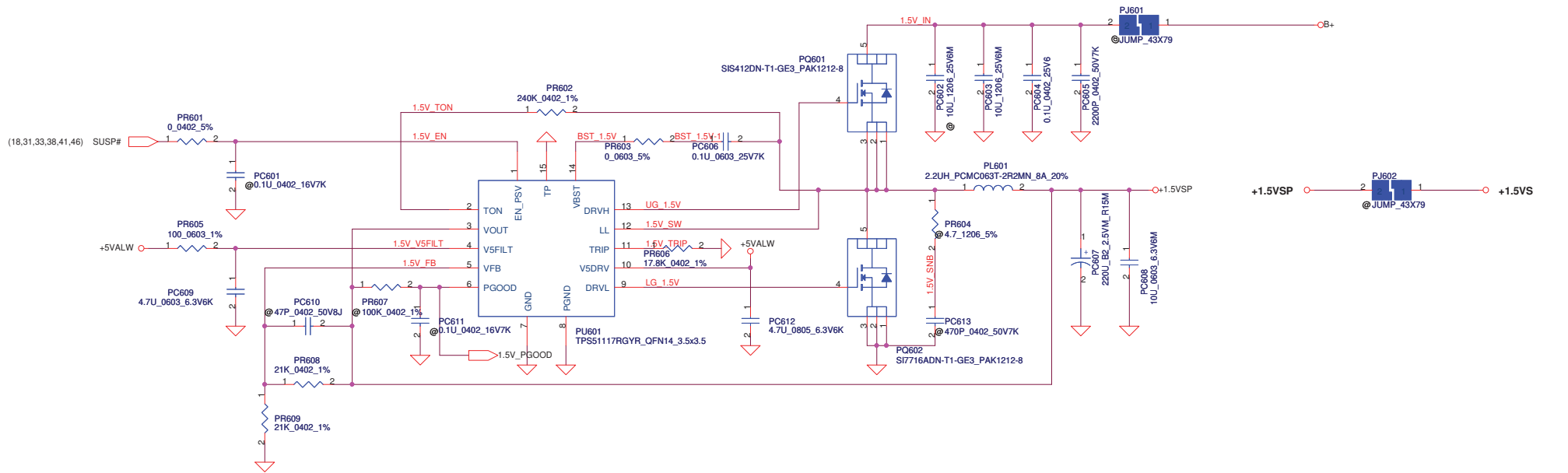
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Date:	Thursday, December 10, 2009	Sheet	42	of 49



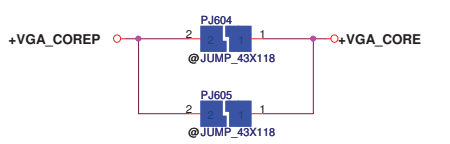
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2009/01/06		2010/01/06		1.2V/1.8V/0.9V	
Size		Document Number		Rev	
				1.0	
Date: Thursday, December 10, 2009   Sheet 43 of 49					

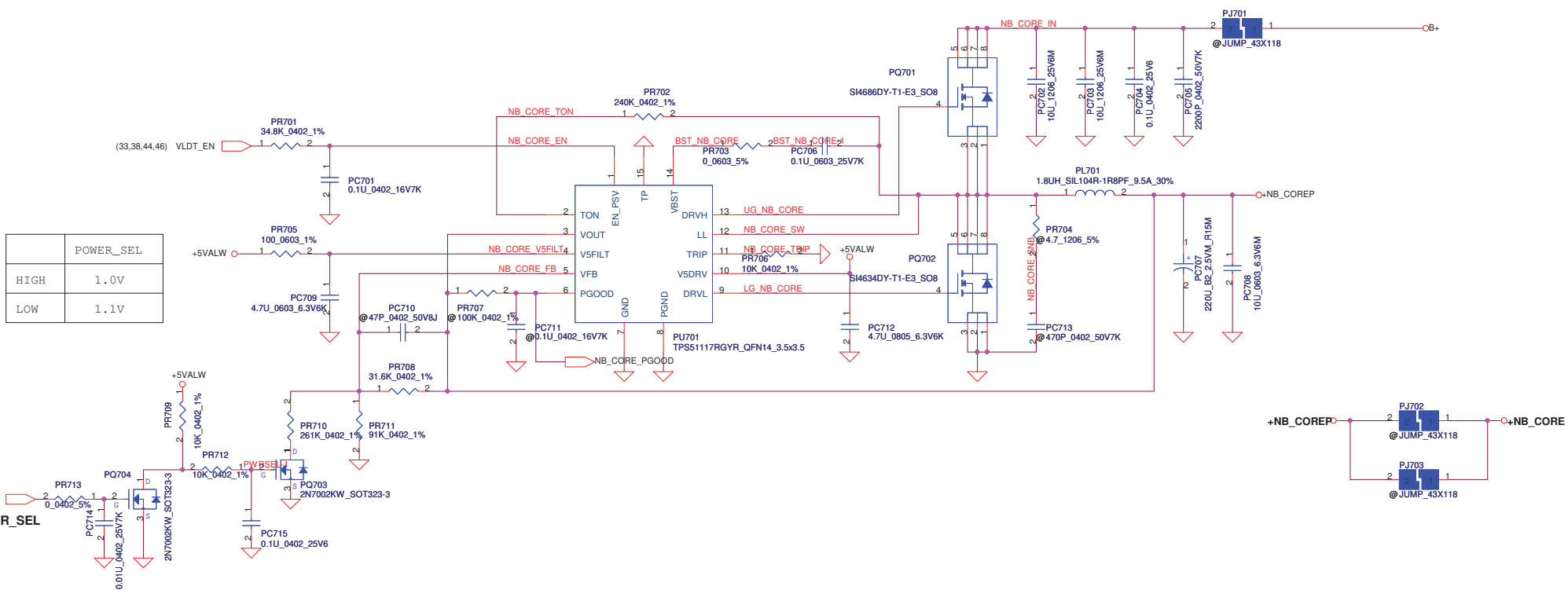
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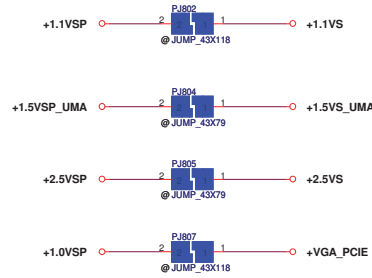
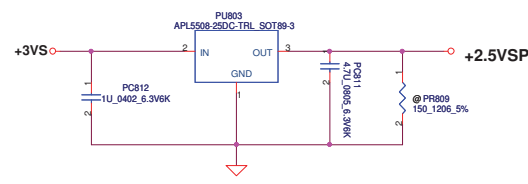
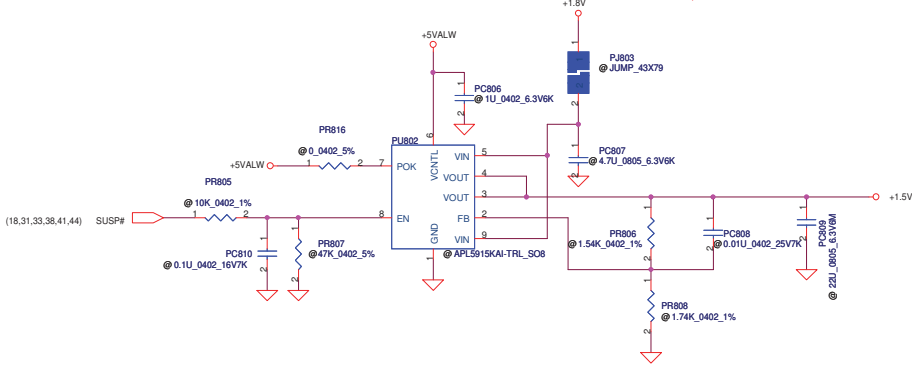
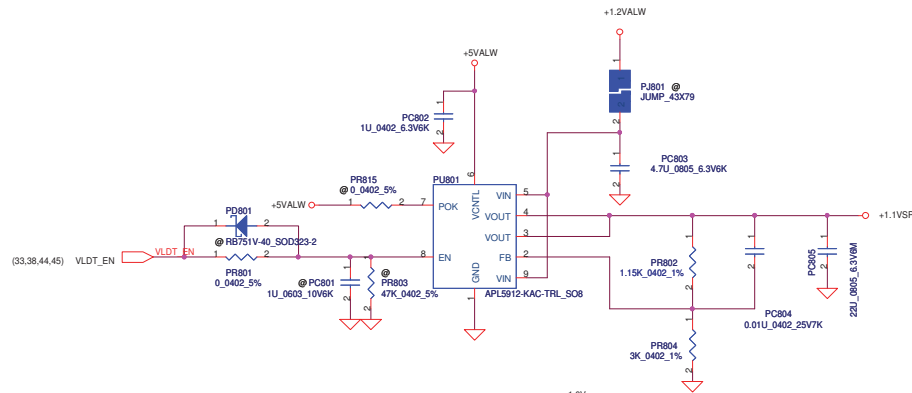
	M93
VGA_PWRSEL	Core Voltage Level
0	1.2 V
1	0.95 V



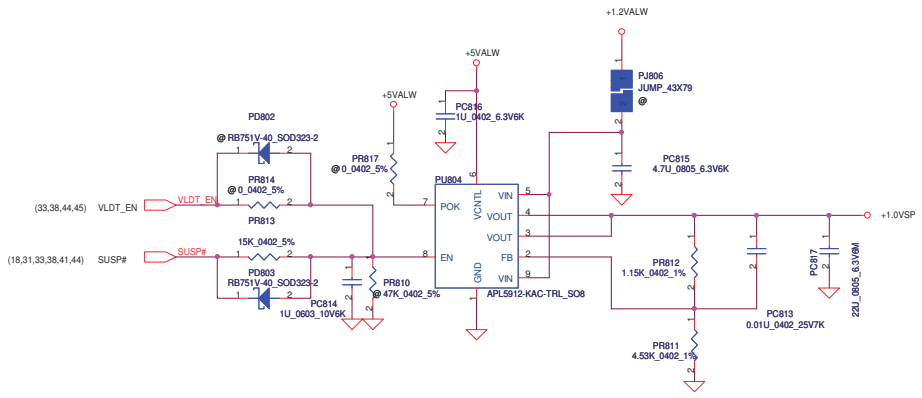
	POWER_SEL
HIGH	1.0V
LOW	1.1V



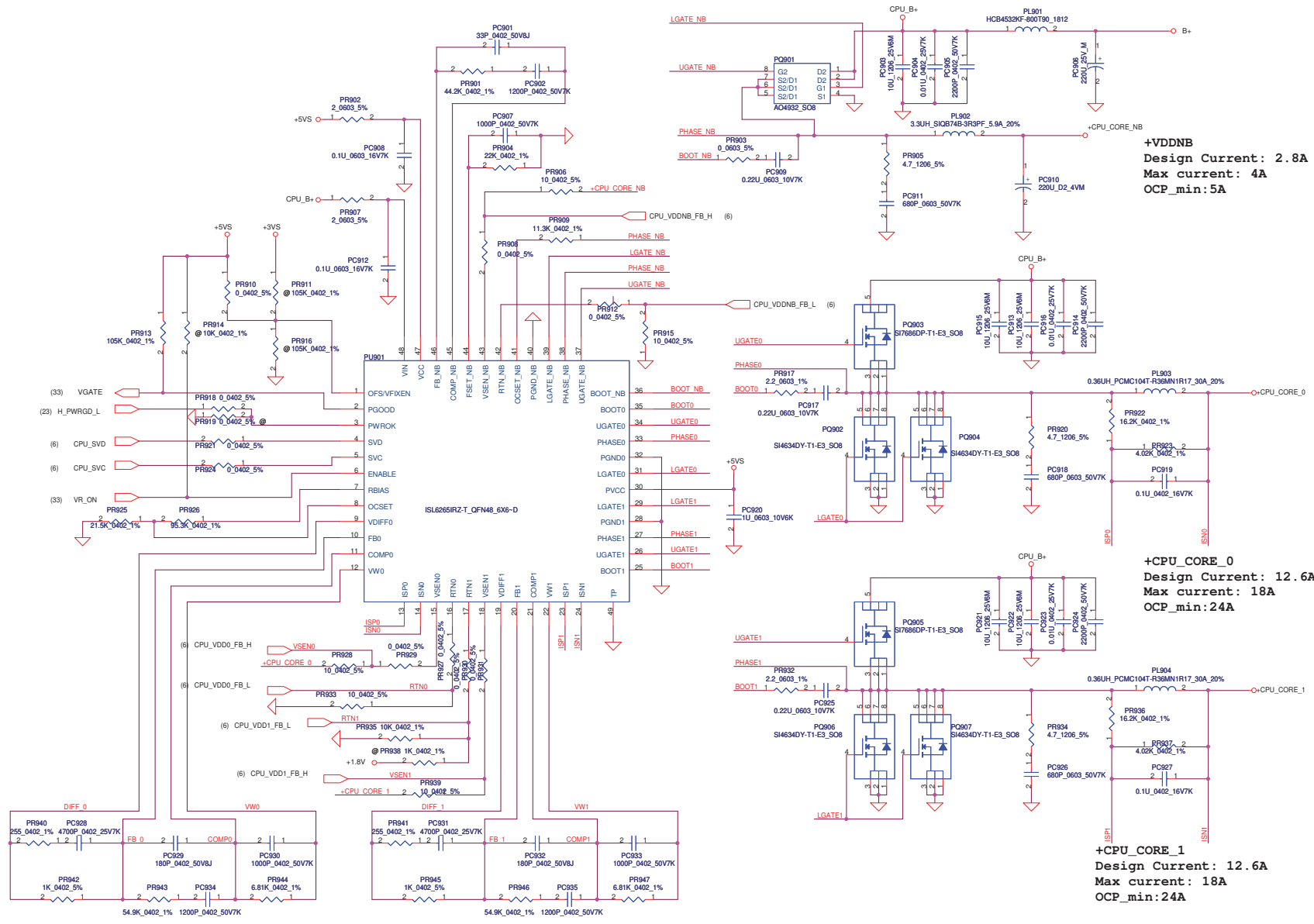
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	Park	M93
VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K



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Date	Thursday, December 10, 2009	Sheet	46	of 49



Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Adjust power sequence for VGA_PCIE by HW request	P46	PR831=15K	2009.10.27	EVT
2	Change PC108 from 1000pF to 0.068uF for issue solution	P39	PC108=0.068uF	2009.11.17	PVT
3	Add snubber R & C and modify boost resistor for 1.8VP	P43	PR512=2.2 ohm;PR513=4.7 ohm;PC524=820pF	2009.11.17	PVT
4	Adjust power sequence	P45	PR701=34.8K,PC701=0.1uF Un-pop PR520,PQ505	2009.12.03	PVT
5					
6					
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Size	Document Number	Rev		1.0	
Custom	LA-5971P	Date:		Thursday, December 10, 2009	
		Sheet		48 of 49	



1. change component AP2301GN to AO3413
2. remove R521, R517, R520 and R518, and reserve U49 , U50, R995, R996, R997 and R998 for experiment Vari-bright function.
3. U6.18 add a pull up resistor R1001 and pull down resistor R1002 for check ENE KB926 version.
4. reserve R999 and R1000 for Vari-bright test.
5. add J8, C1031, C1032, C1033, C1034, C1035, C1036, C1037, C1038 and C1039 for EMI request.
6. Change R583, R584, R585 and R586 Bead from SM010018110 to SM010022410.
7. reserve R1003 for EMI request.
8. Change C633, C640, C662, C948, C660 and C639 to 10pF for EMI rquest.

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