



Part Number = DAZ0J200100

Compal Confidential

K73 Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M1 + GPU Seymour XT-M2

2010-02-22

REV: 0.22

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	V	X	V
FCH_SMCLK0 FCH_SMDAT0	PCH	V	X	X	X	V	X
FCH_SMCLK3 FCH_SMDAT3	PCH	X	X	V	X	X	X

FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI (WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

SCL0, SDA0 (Primary SMBUS in the S0 domain)
 SCL1, SDA1 (Secondary SMBUS supporting ASF)
 SCL2, SDA2 (Primary SMBUS in the S5 domain)
 SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
 SCL4, SDA4 (Primary SMBUS in the S5 domain)

Symbol Note :



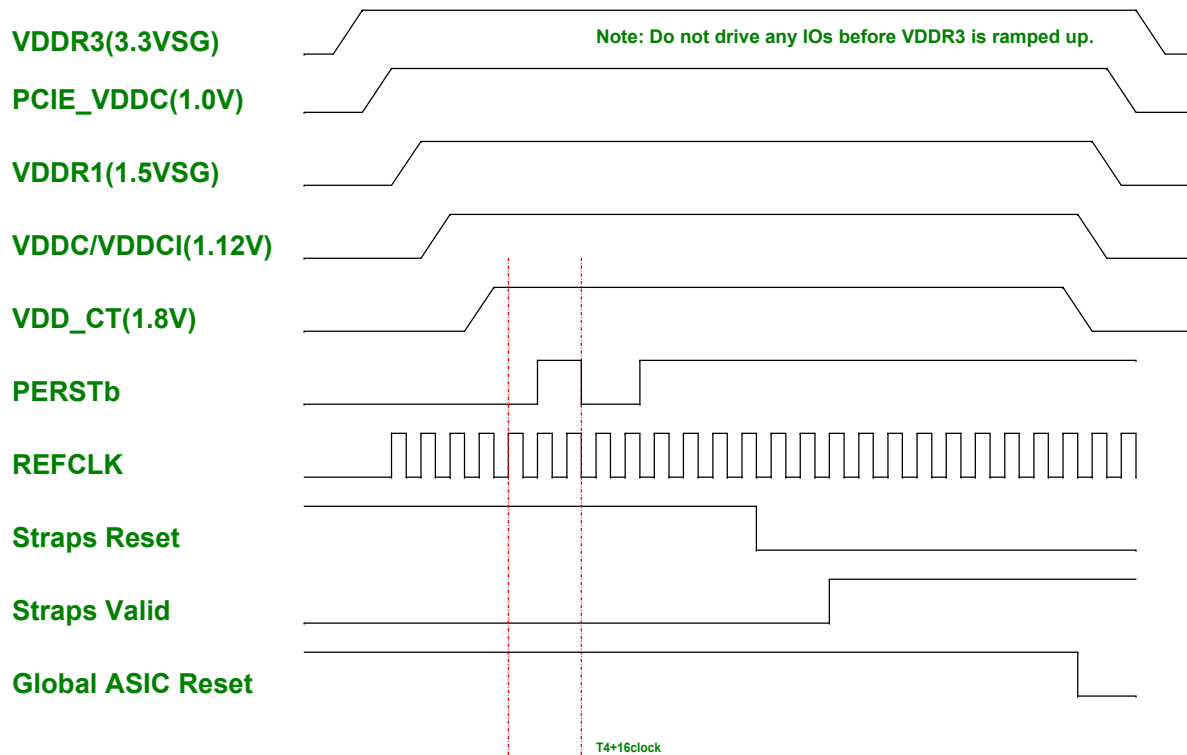
BOM Structure

15@ : E240 1.5GHz
 16@ : E350 1.6GHz
 X76@ : VRAM second source
 LS@ : Level Shift
 NLS@ : non Level Shift
 USB30@ : USB3.0

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Power-Up/Down Sequence

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- VDDR3 should ramp-up before or simultaneously with VDDC.
- For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
- The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



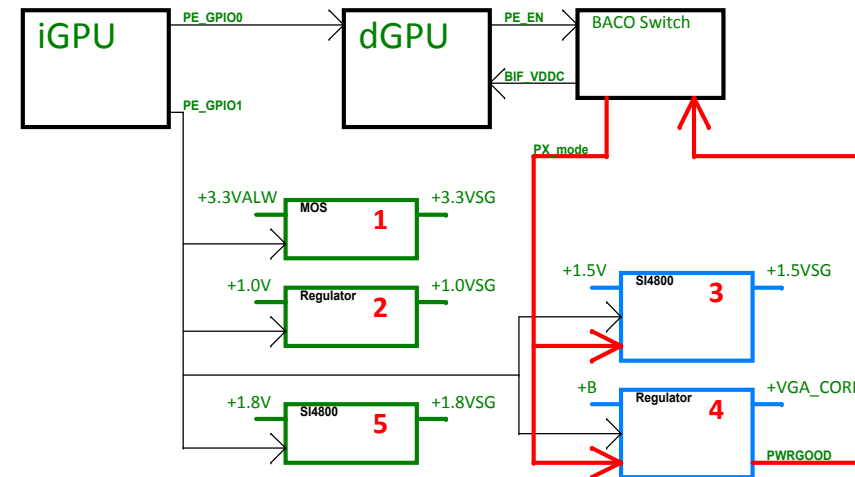
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

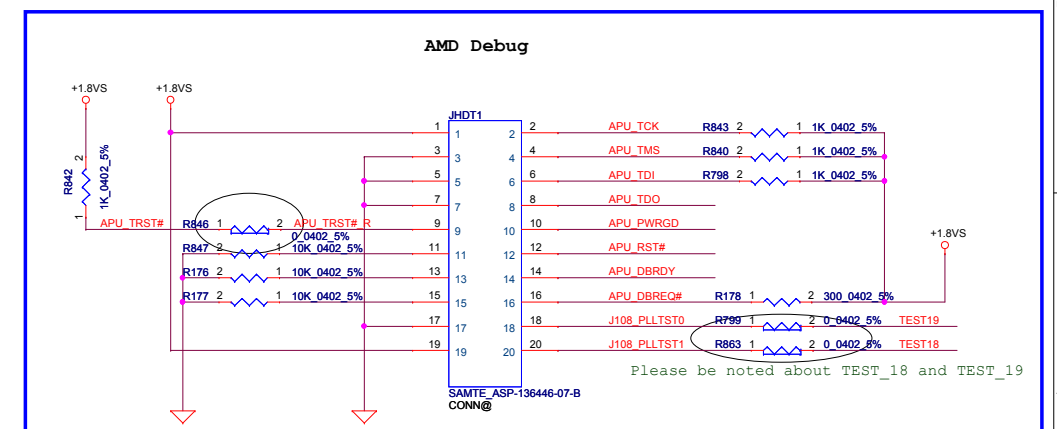
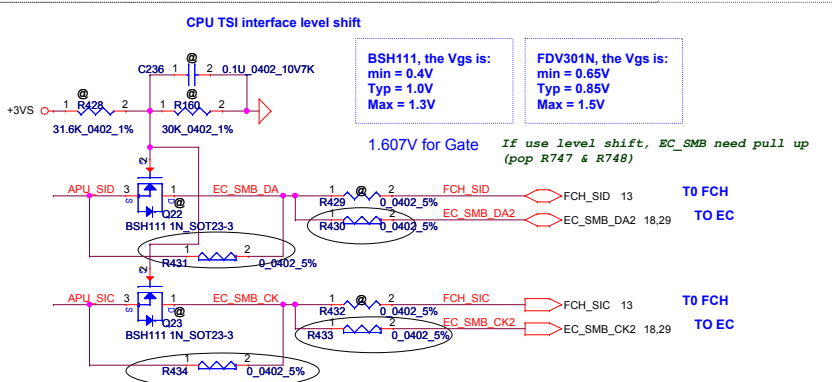
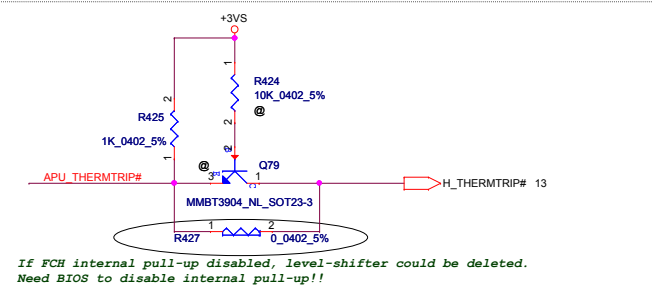
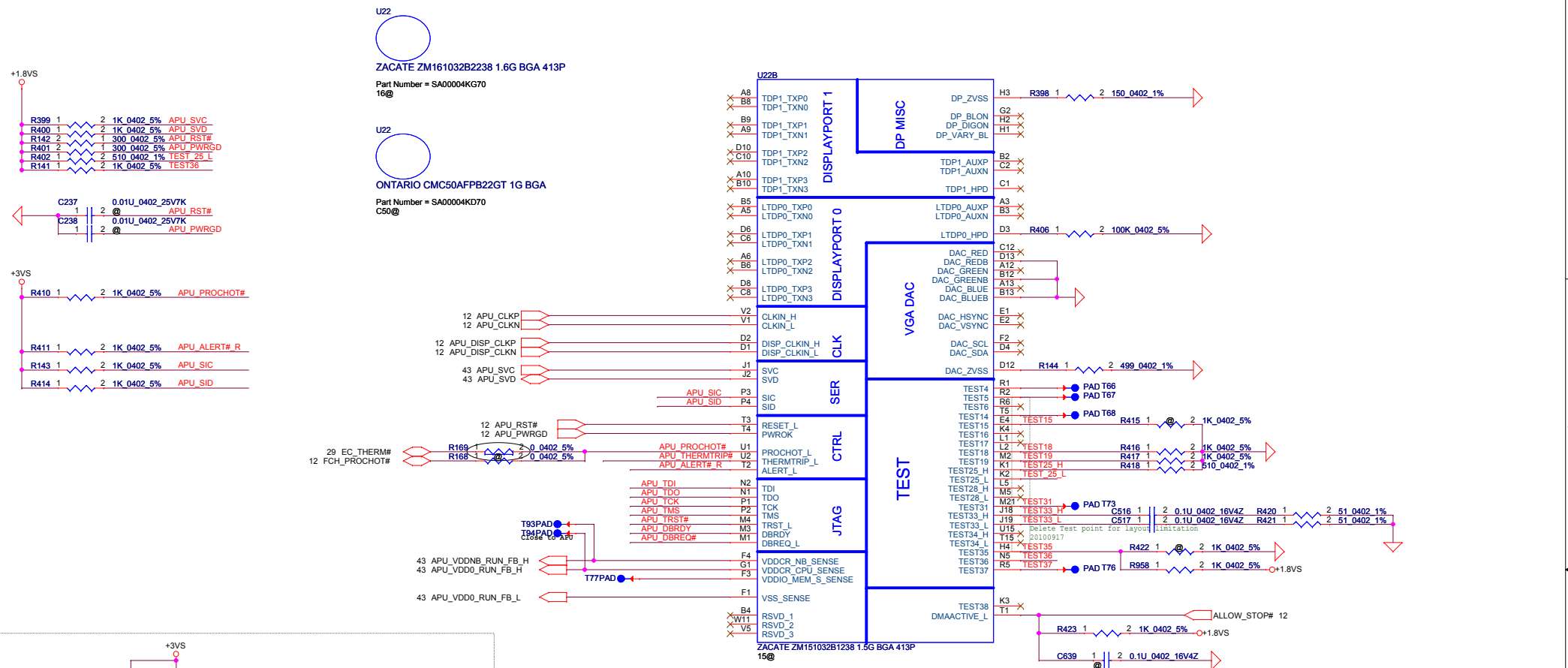
BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
 PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

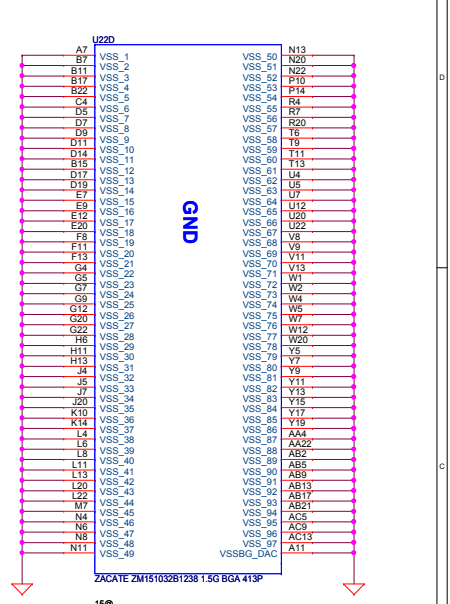
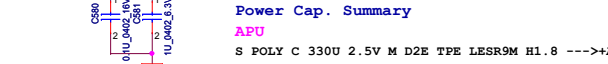
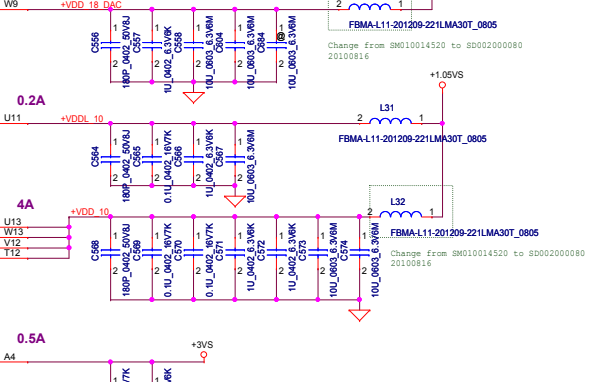
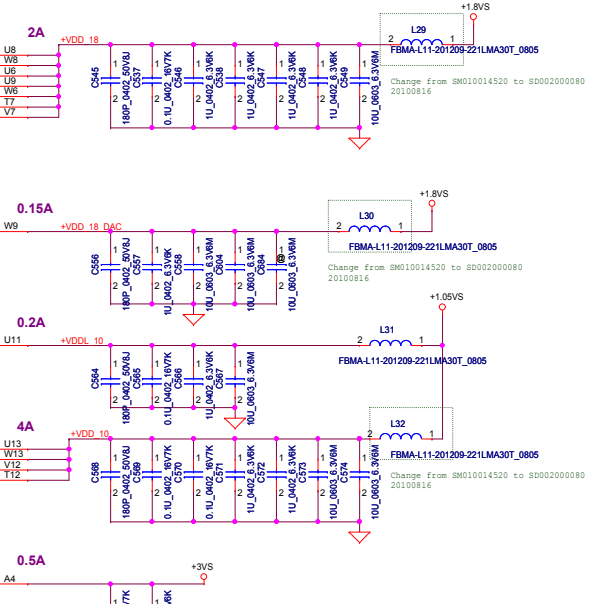
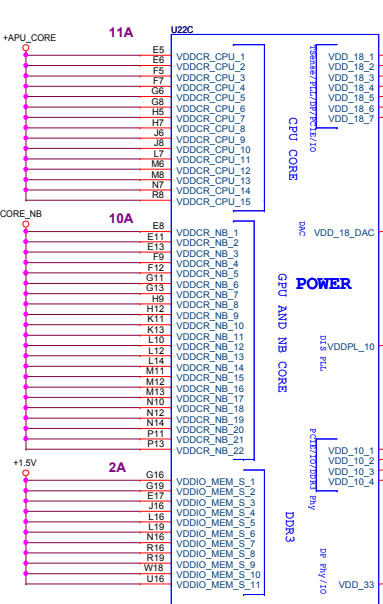
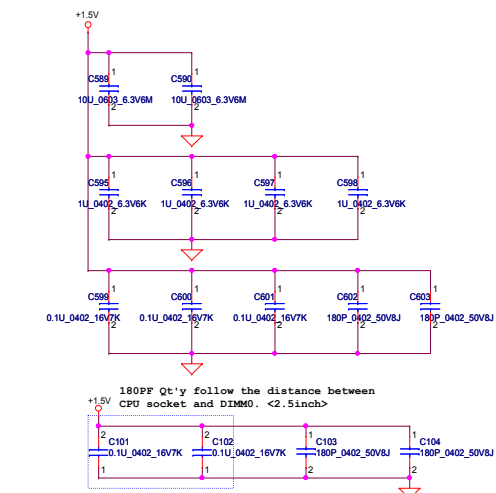
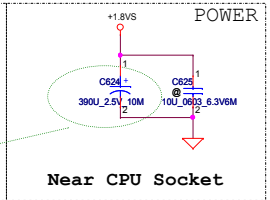
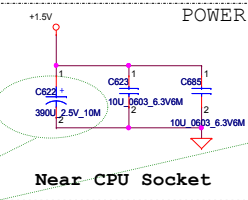
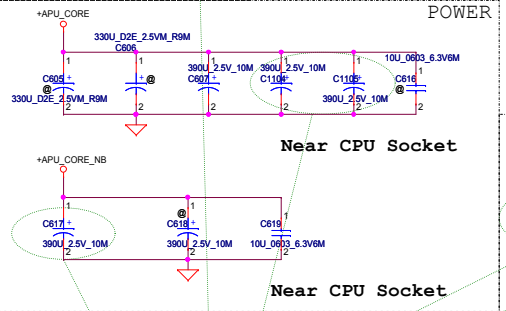
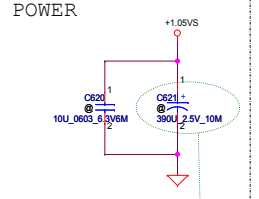
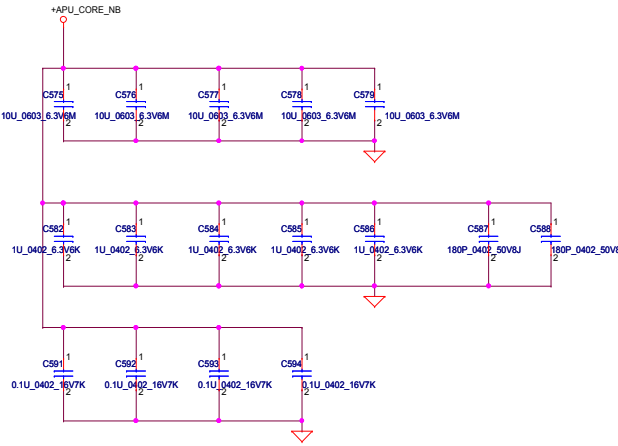
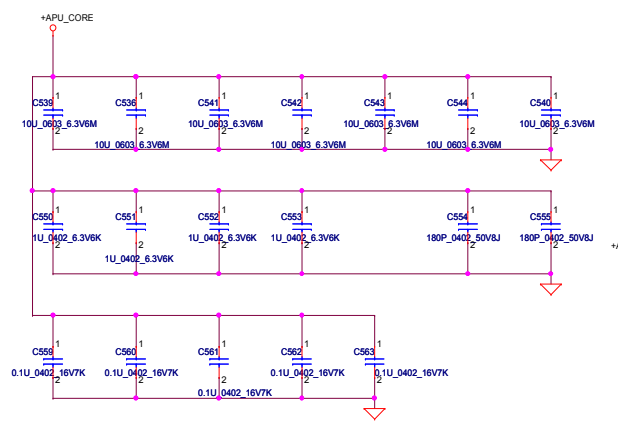
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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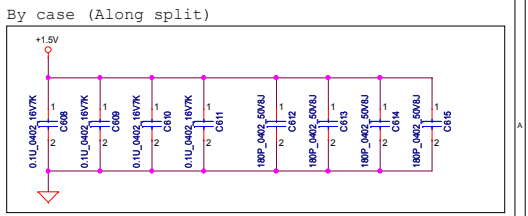


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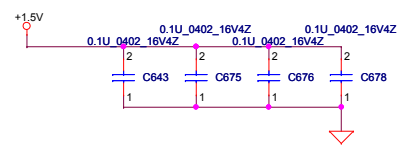
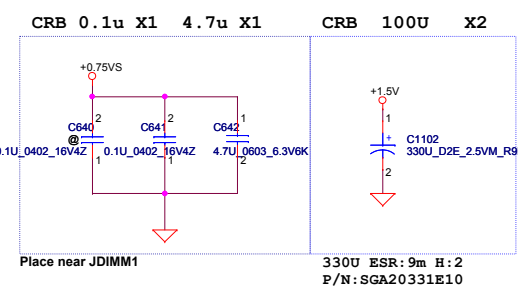
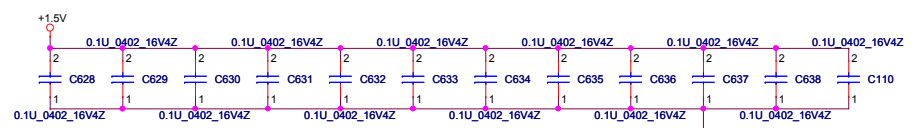
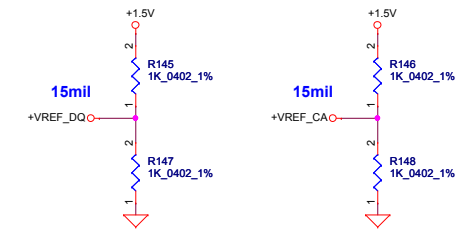
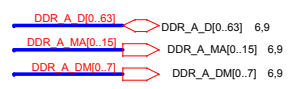
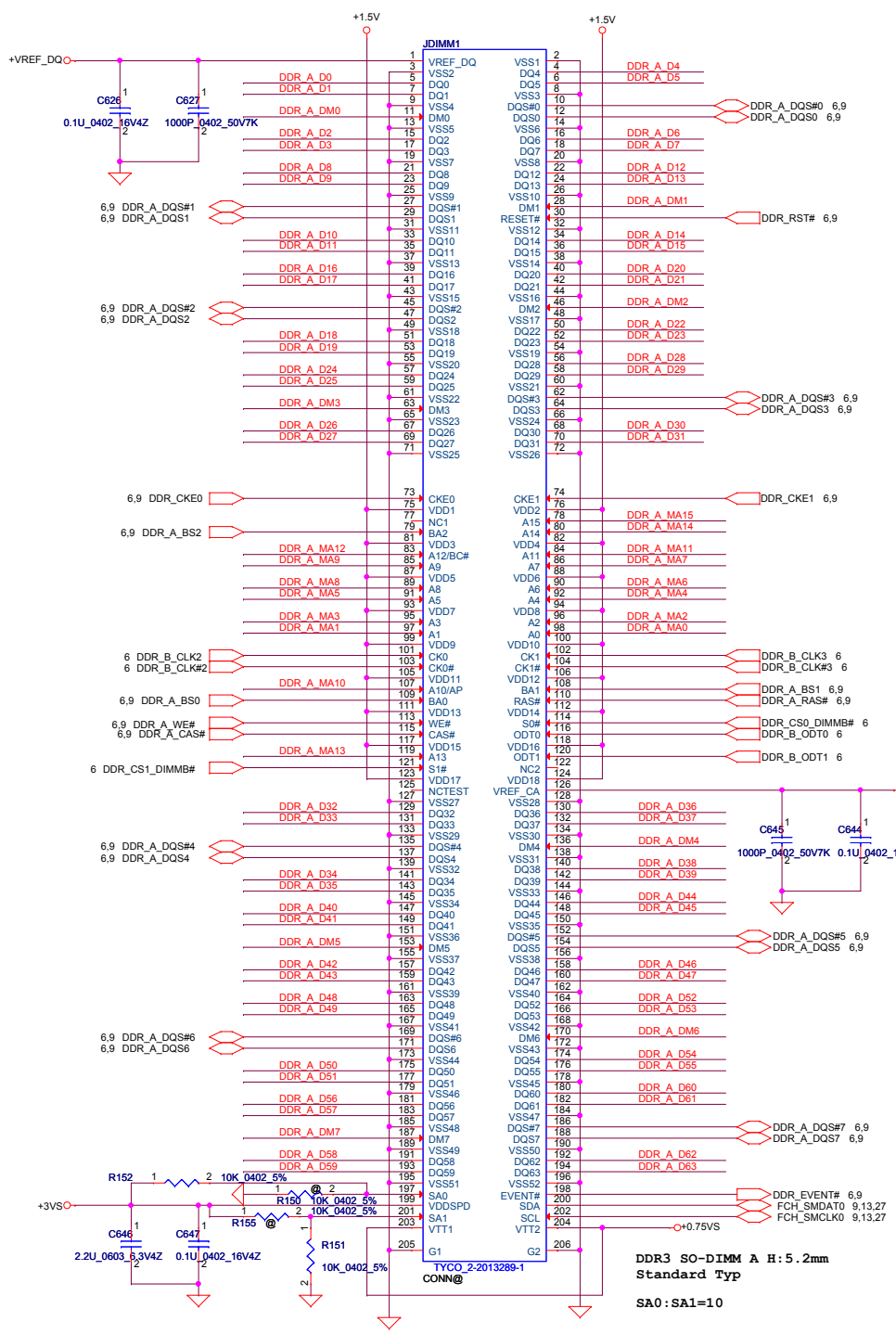
Power Cap. Summary

- APU**
- S POLY C 330U 2.5V M D2E TPE LESR9M H1.8 ---->+APU_CORE (Qty : 3) Unpop:2
- S_A_P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+APU_CORE (Qty : 2) +APU_CORE
- S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 ---->+APU_CORE_NB (Qty : 1)
- S_A_P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+APU_CORE_NB (Qty : 1) +APU_CORE_NB
- S_A_P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.5V (Qty : 1) +1.5V
- S_A_P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.05VS (Qty : 1) +1.05VS
- S_A_P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.8VS (Qty : 1) +1.8VS
- DDR3 Socket**
- S POLY C 330U 2V M X LESR6M SX H1.9 ---->+1.5V (Qty : 1) +1.5V
- FCH**
- S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 ---->+1.1VS (Qty : 1) UMA unpop +1.1VS
- GPU**
- S POLY C 330U 2V M X LESR6M SX H1.9 ---->+VGA_CORE (Qty : 2) Unpop:1
- S_A_P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+VGA_CORE (Qty : 1) +GPU_CORE
- S_A_P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.5VSG (Qty : 1) +1.5VSG
- USB**
- S_A_P_CAP 220U 6.3V M C45 R17M SVPE H4.4 ---->+USB_VCCA (Qty : 1) +USB_VCCA



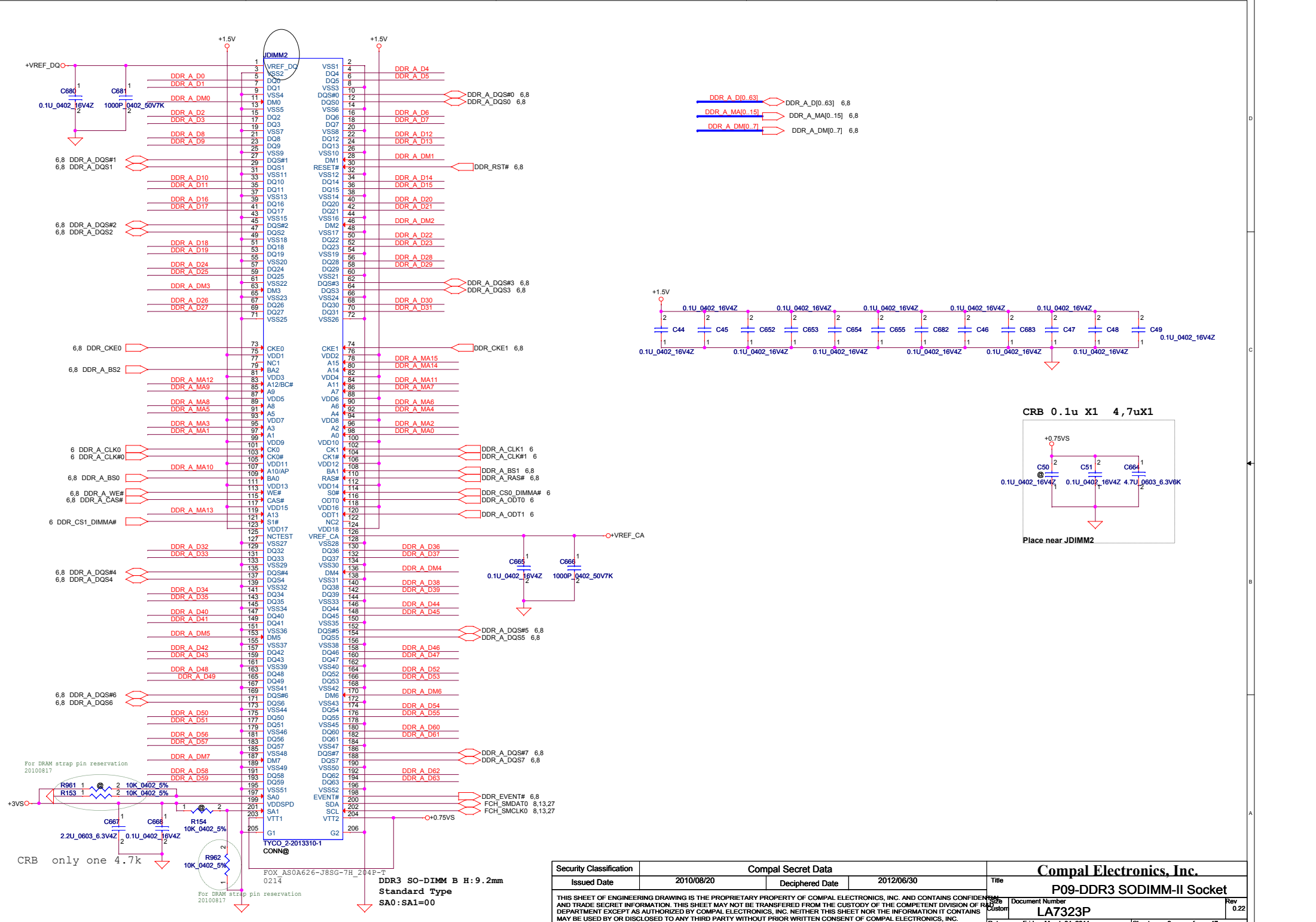
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DDR3 SO-DIMM-A H:5.2mm
Standard Typ
SA0:SA1=10

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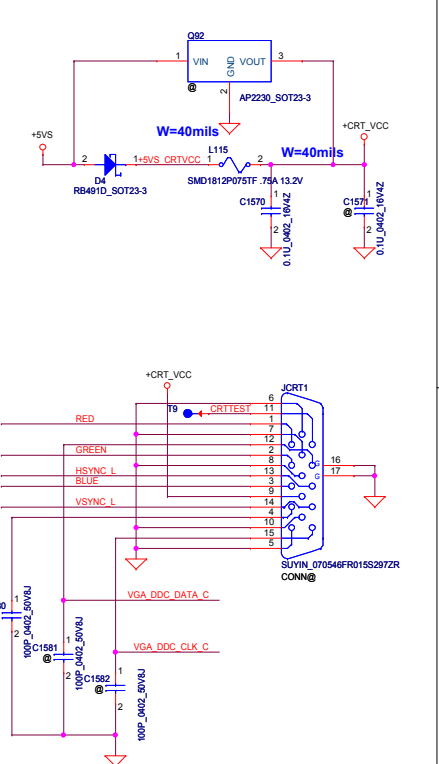
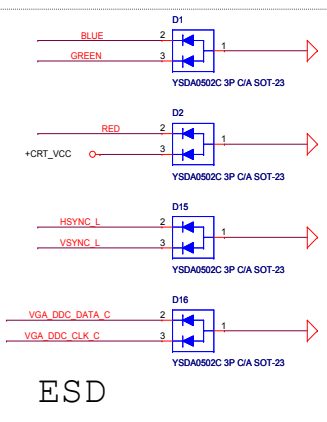
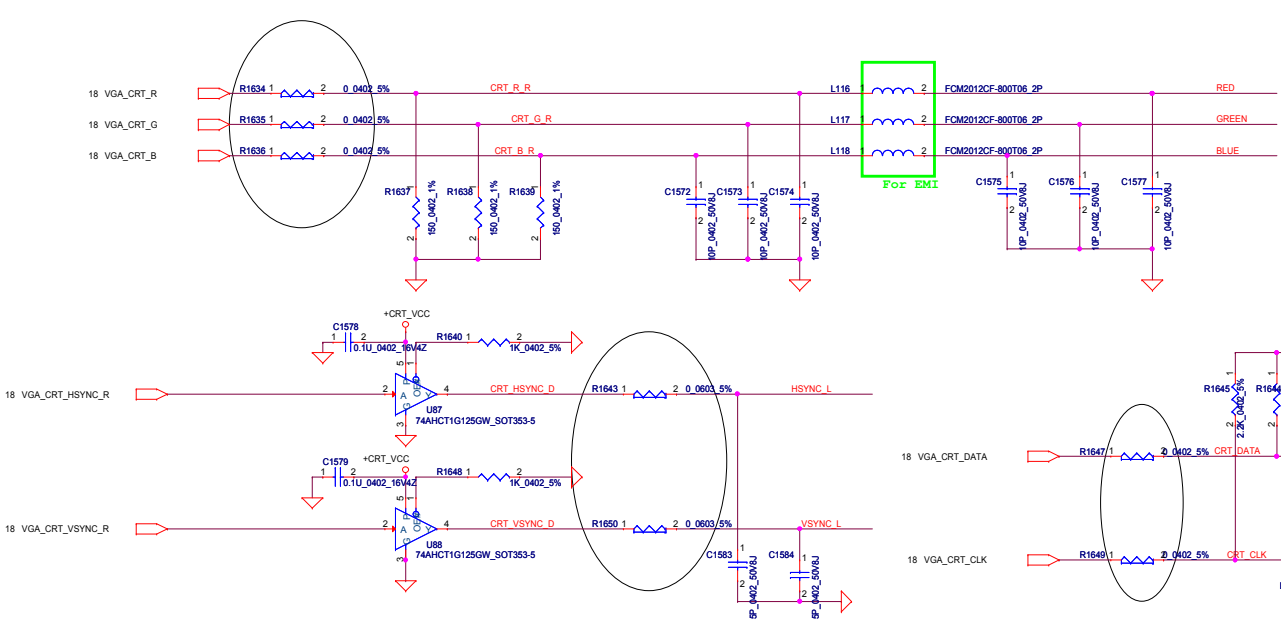
DDR3 SO-DIMM B H:9.2mm
Standard Type
SA0:SA1=00

For DRAM strap pin reservation
20100817

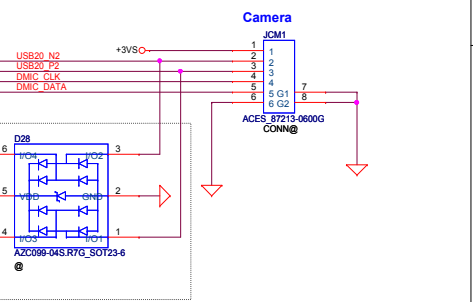
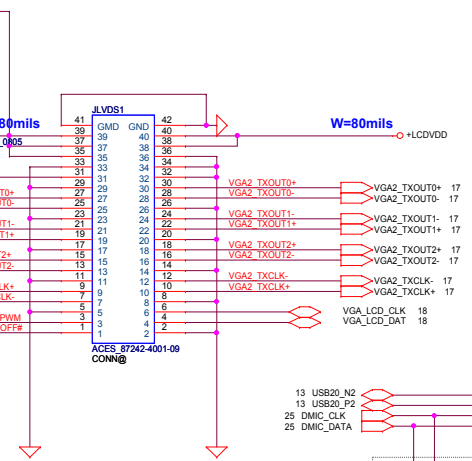
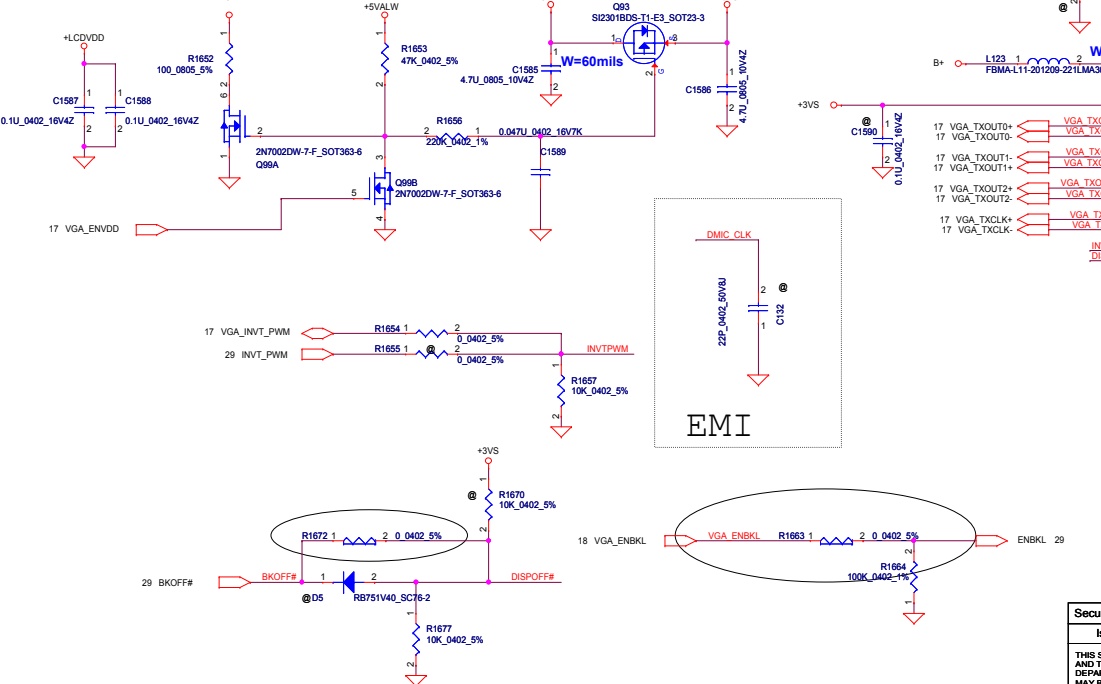
For DRAM strap pin reservation
20100817

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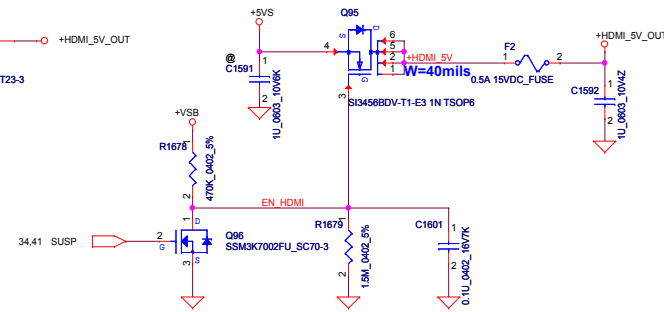
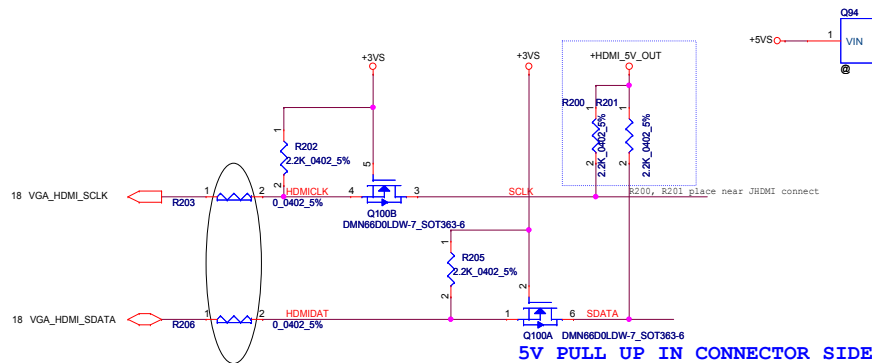
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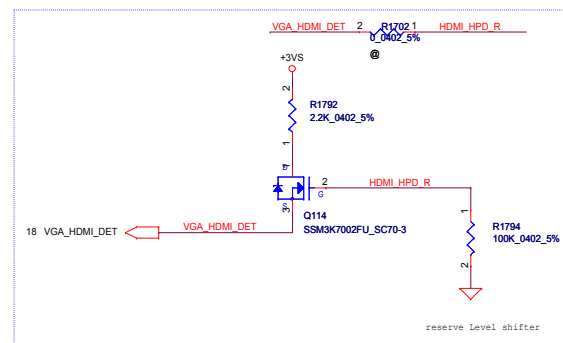
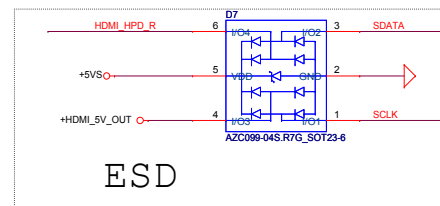
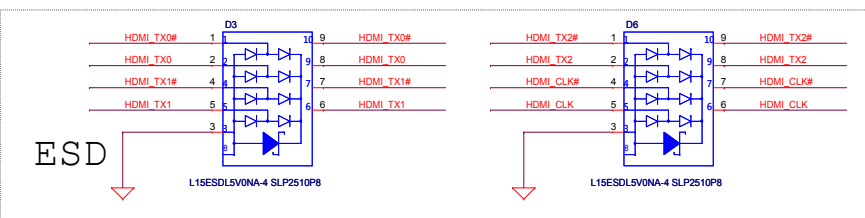
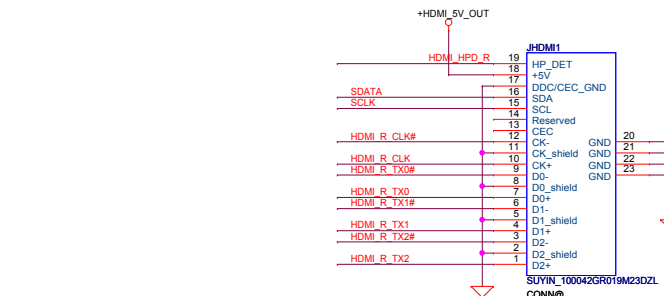
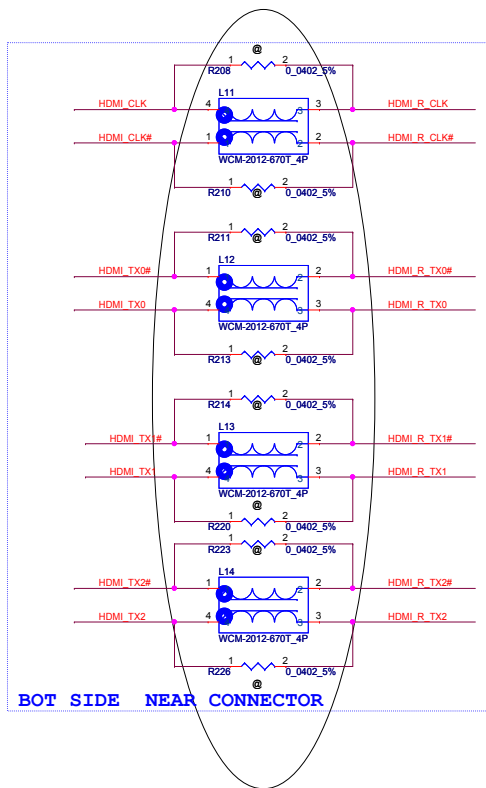
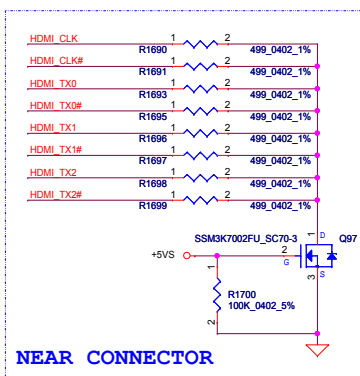
LCD POWER CIRCUIT



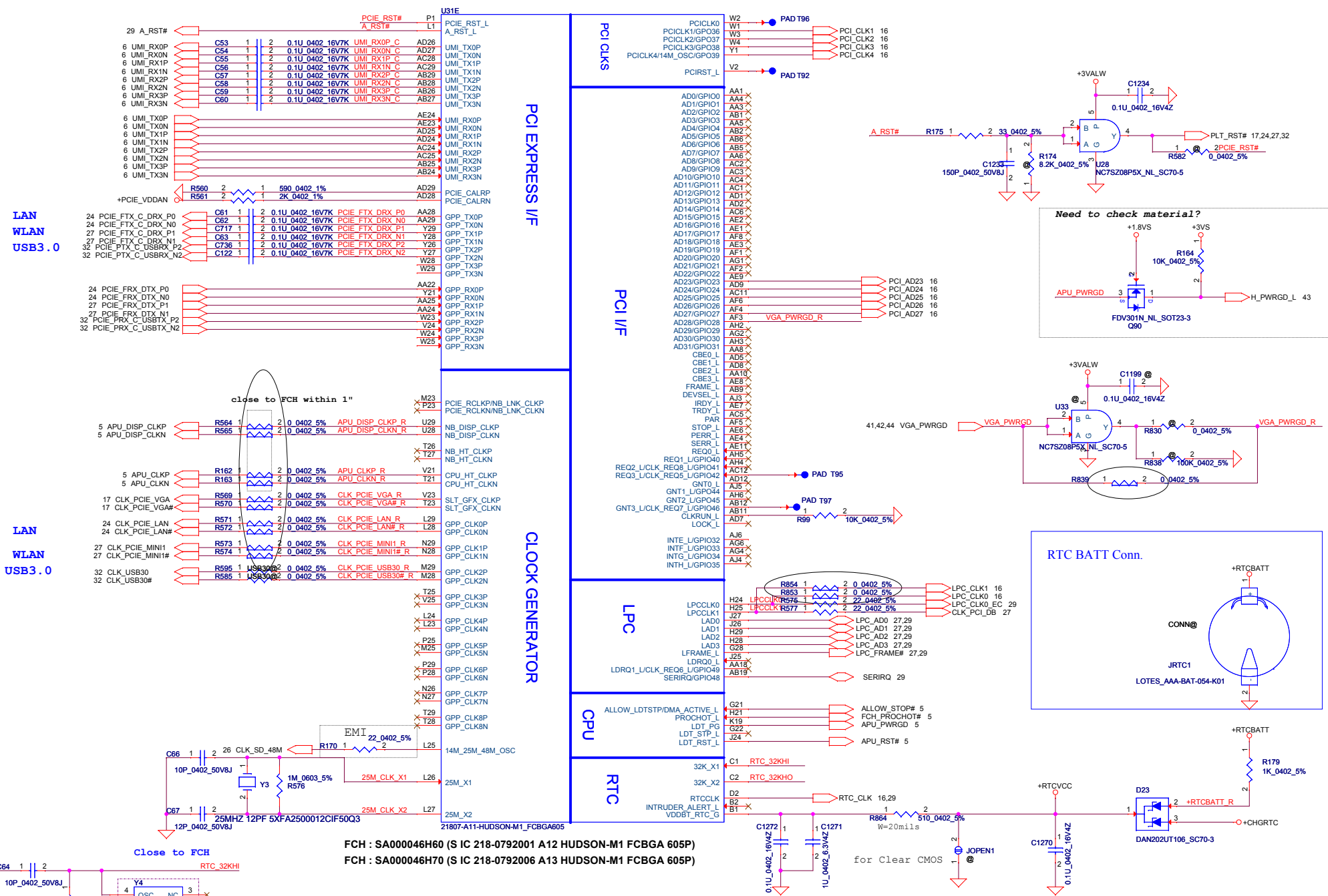
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18	VGA_HDMI_TXC+	C1602	1	2	0.1U_0402_16V7K	HDMI_CLK
18	VGA_HDMI_TXC-	C1603	1	2	0.1U_0402_16V7K	HDMI_CLK#
18	VGA_HDMI_TXD0+	C1604	1	2	0.1U_0402_16V7K	HDMI_TX0
18	VGA_HDMI_TXD0-	C1605	1	2	0.1U_0402_16V7K	HDMI_TX0#
18	VGA_HDMI_TXD1+	C1606	1	2	0.1U_0402_16V7K	HDMI_TX1
18	VGA_HDMI_TXD1-	C1607	1	2	0.1U_0402_16V7K	HDMI_TX1#
18	VGA_HDMI_TXD2+	C1608	1	2	0.1U_0402_16V7K	HDMI_TX2
18	VGA_HDMI_TXD2-	C1609	1	2	0.1U_0402_16V7K	HDMI_TX2#



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FCH : SA000046H60 (S IC 218-0792001 A12 HUDSON-M1 FCBGA 605P)
 FCH : SA000046H70 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 605P)

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Issued Date	2010/08/20	Deciphered Date	2012/06/30	P12-FCH PCIE/PCIACPI/LPC/RTC	
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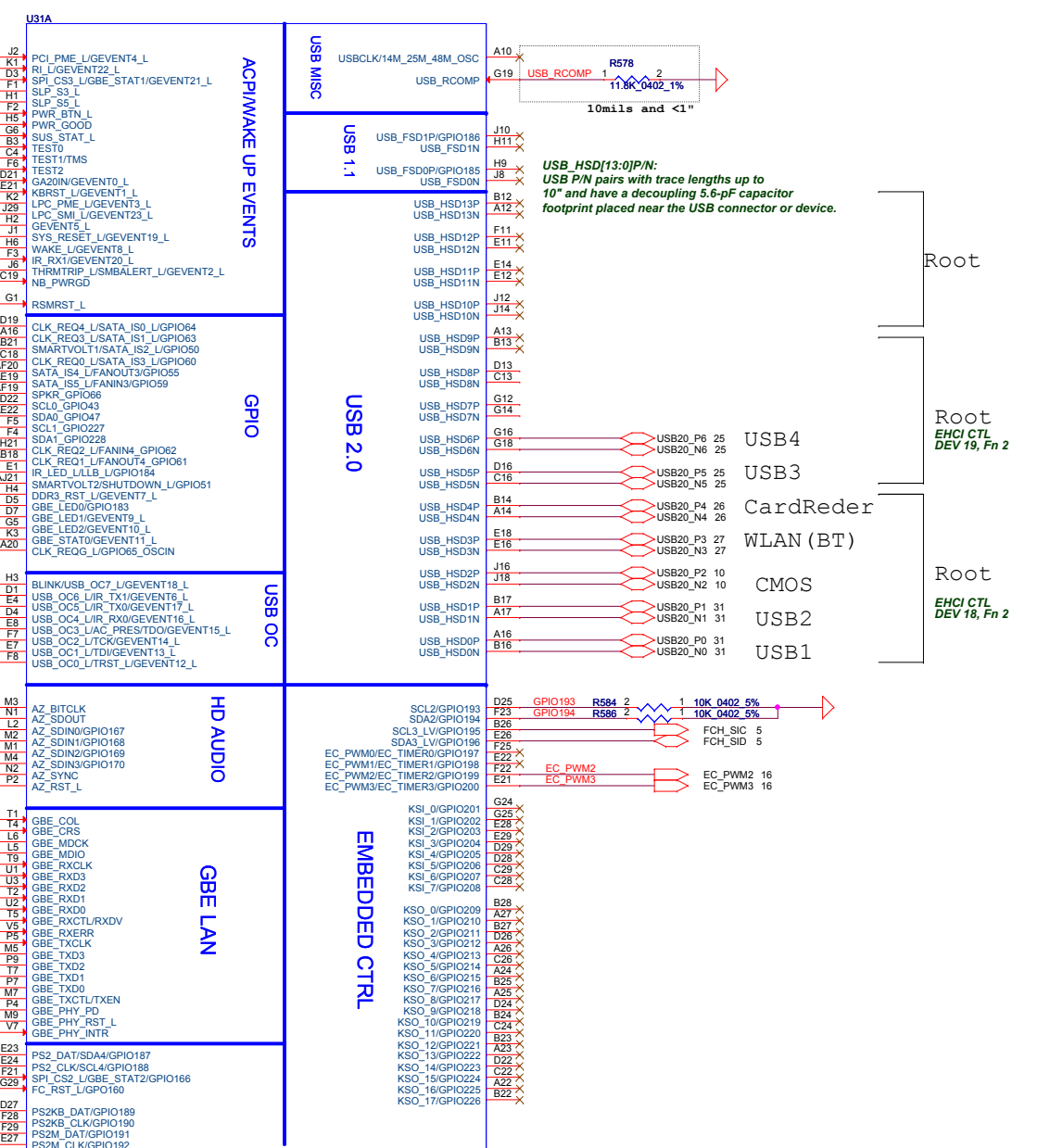
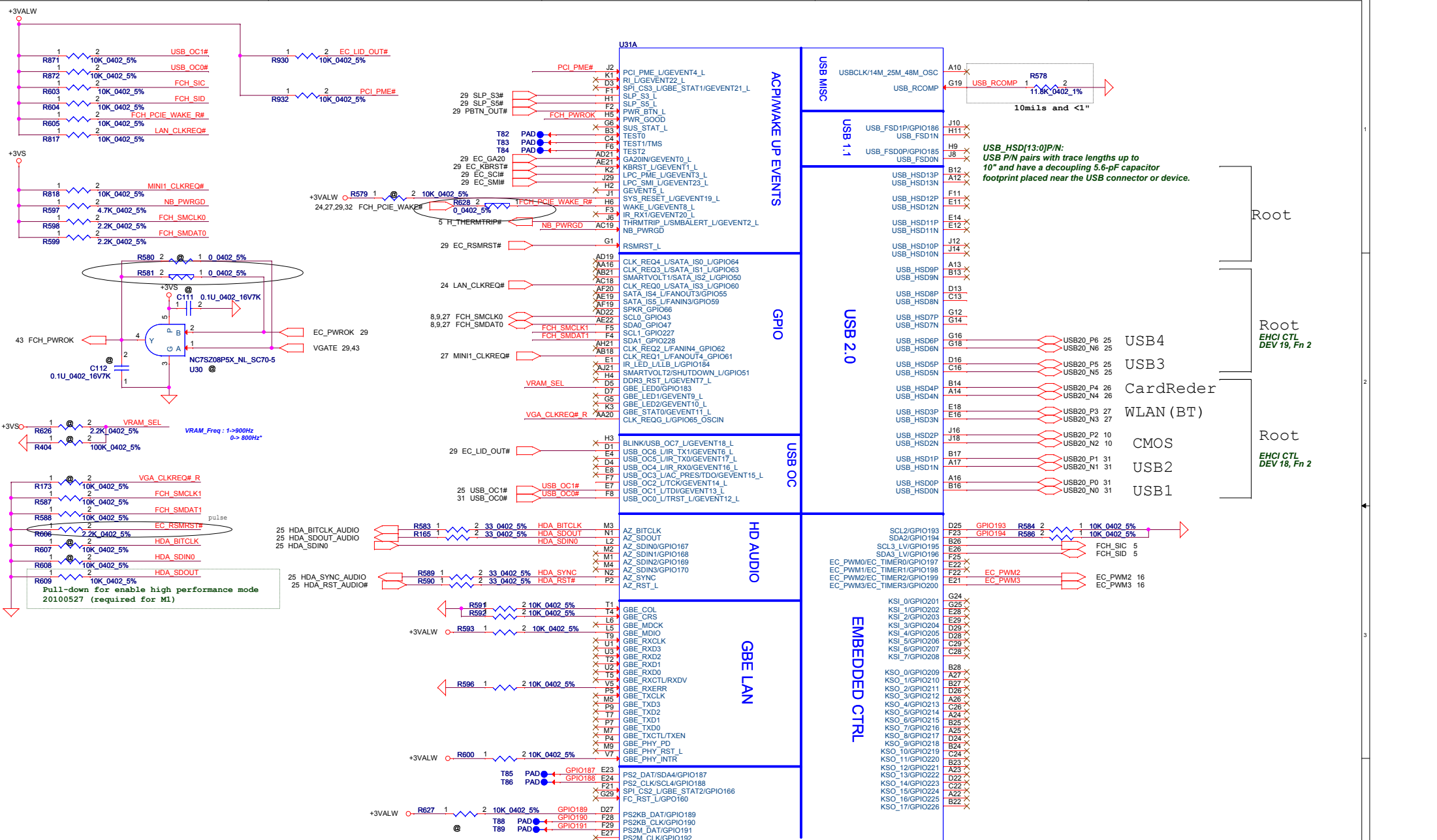
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Document Number LA7323P

Revision Rev 0.22

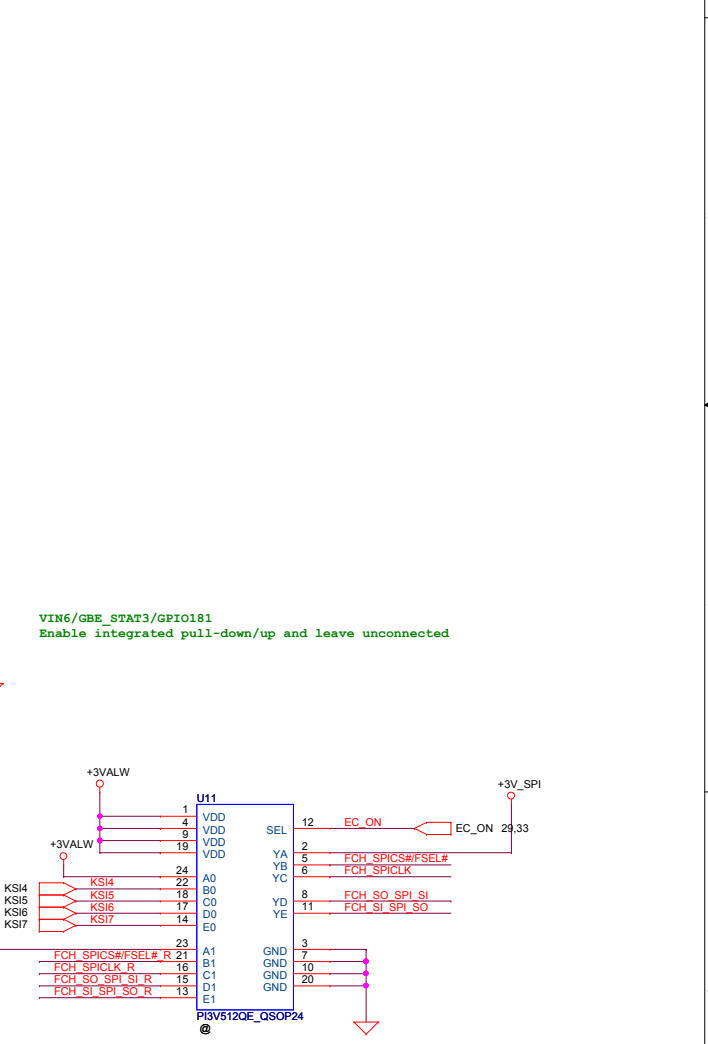
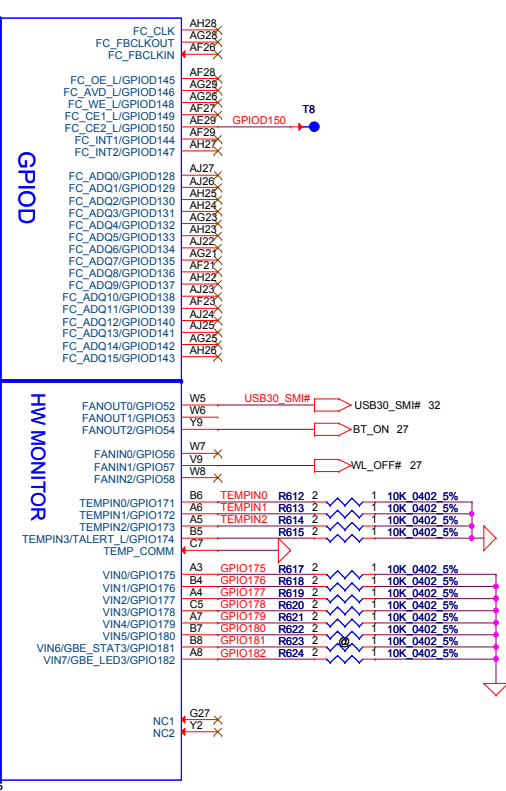
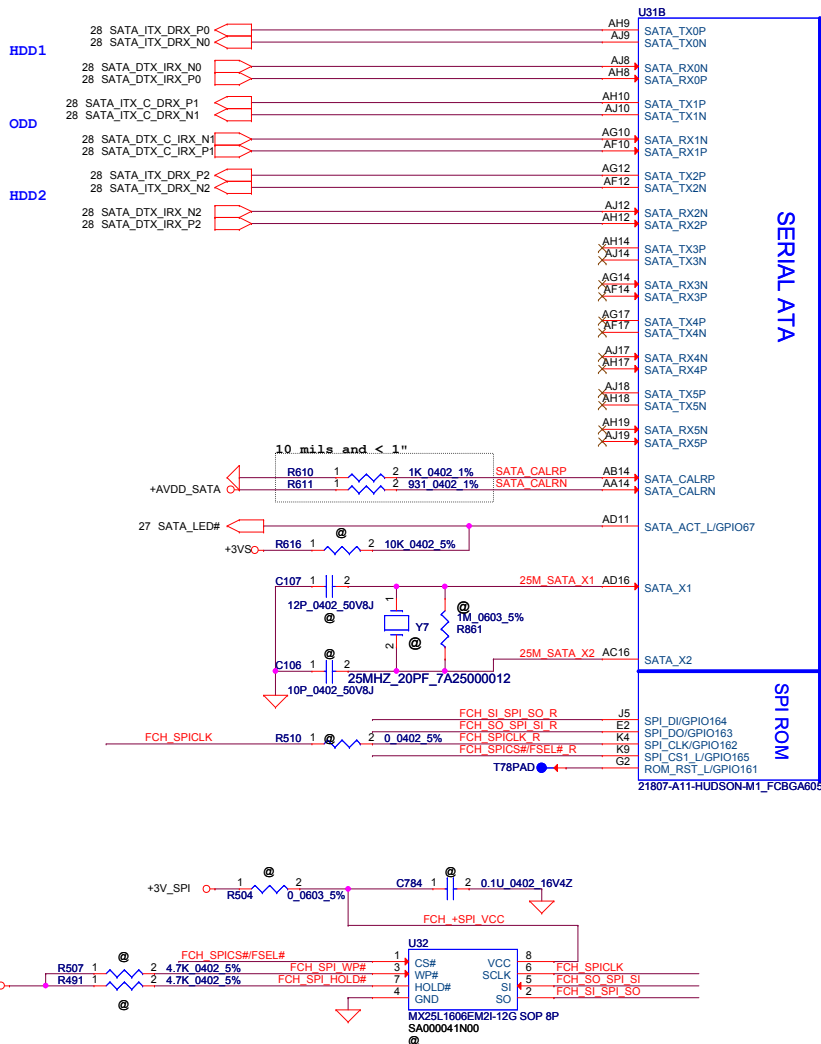
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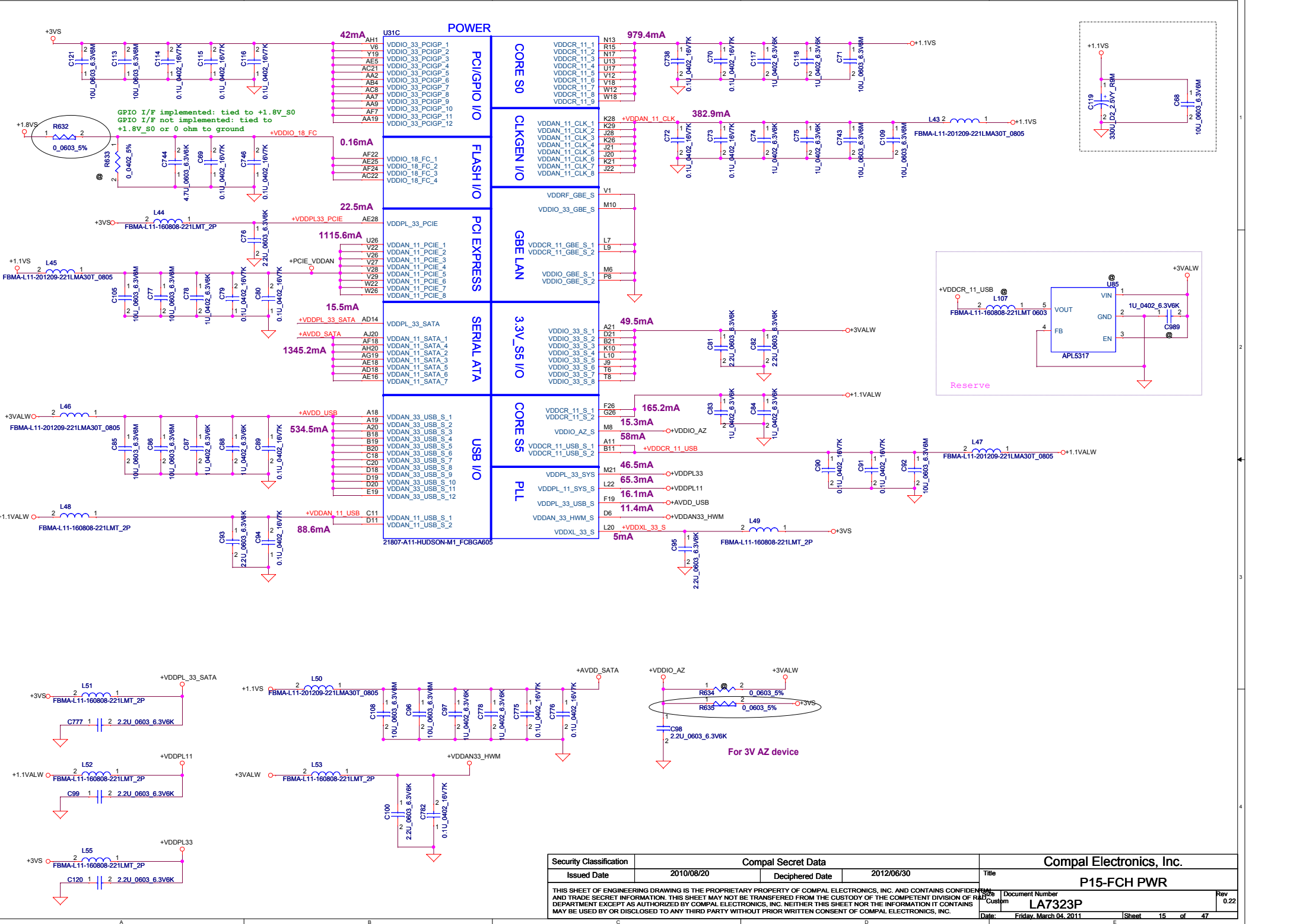
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VIN6/GBE_STAT3/GPIO181
 Enable integrated pull-down/up and leave unconnected

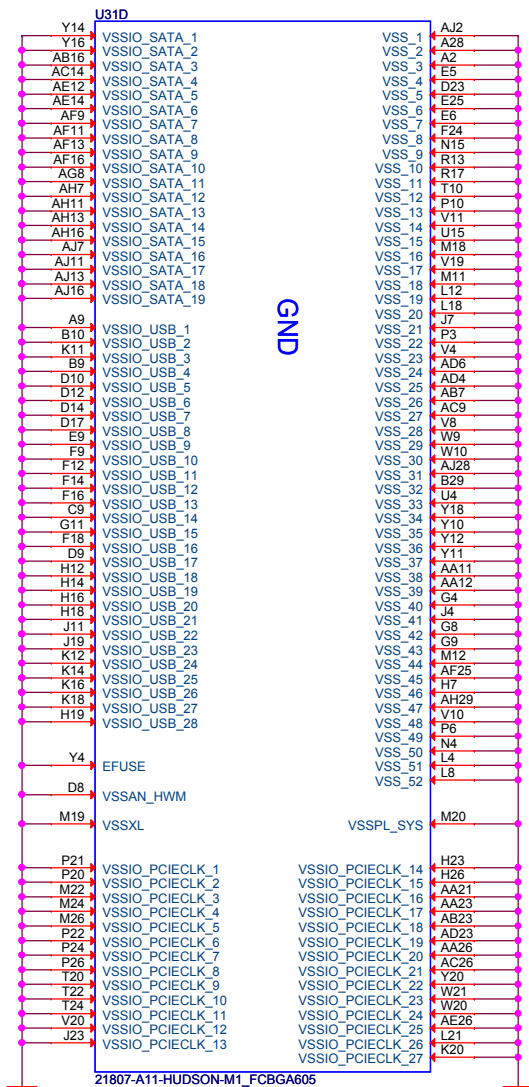
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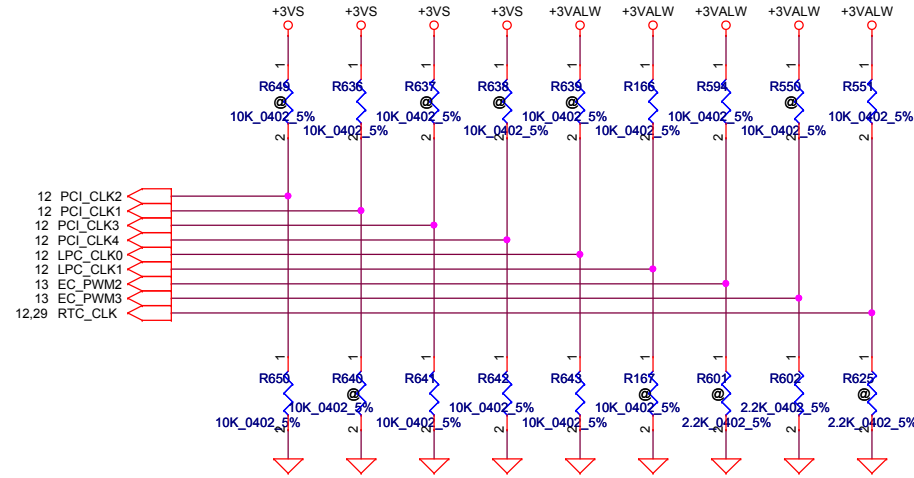


GND

REQUIRED STRAPS

Check Internal PU/PD

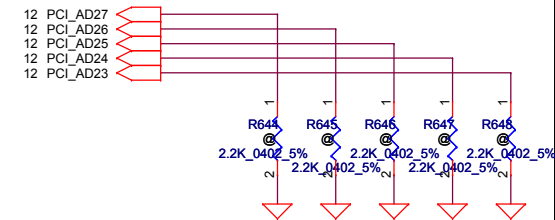
PULL HIGH	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H,L) *
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode ENABLED	SPI ROM(L,H)	



DEBUG STRAPS

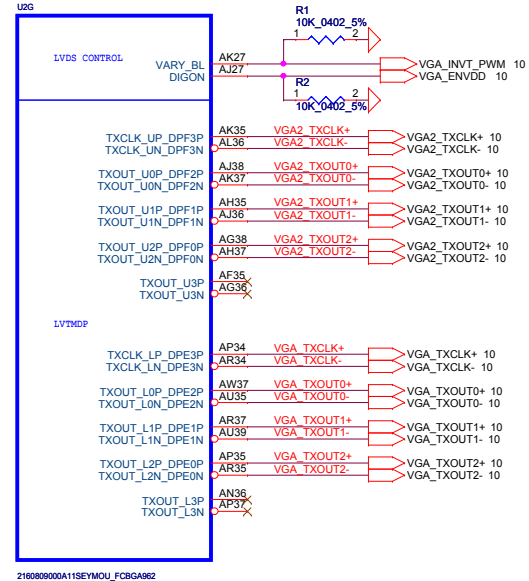
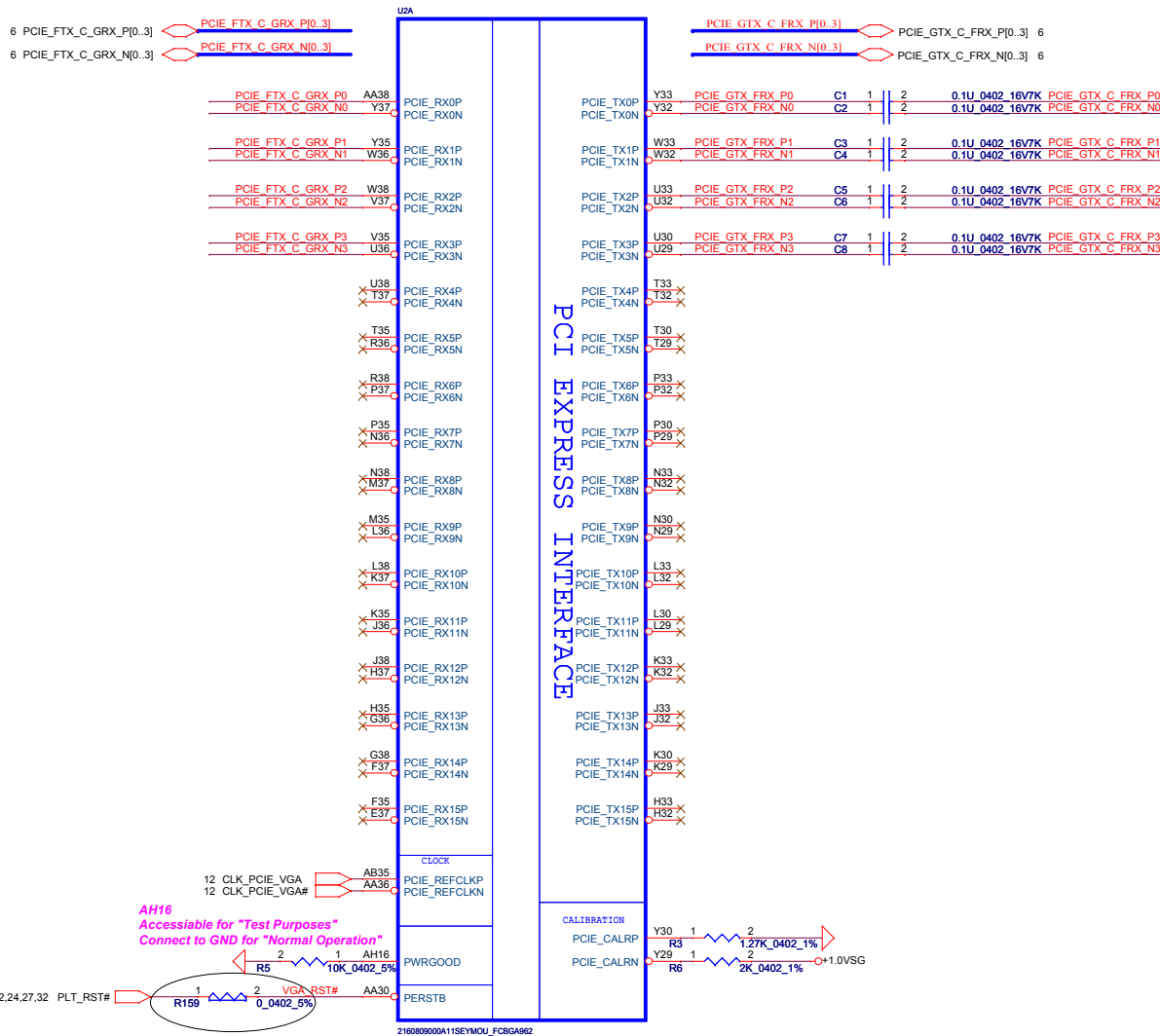
FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PULL HIGH	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
	USE internal PLL generated PLL CLK	ILA AUTORUN Disabled	Selects FC PLL	Disable I2C ROM	Required Setting
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved



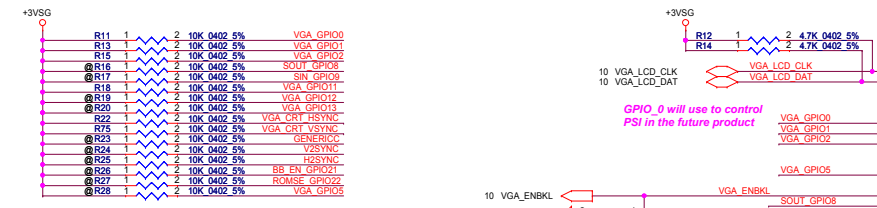
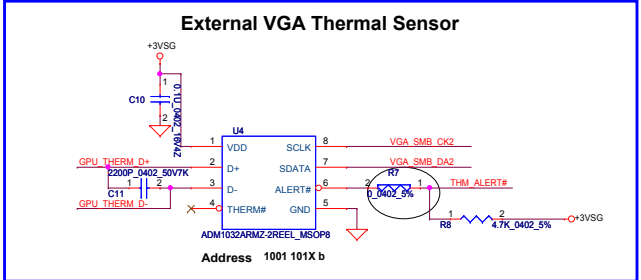
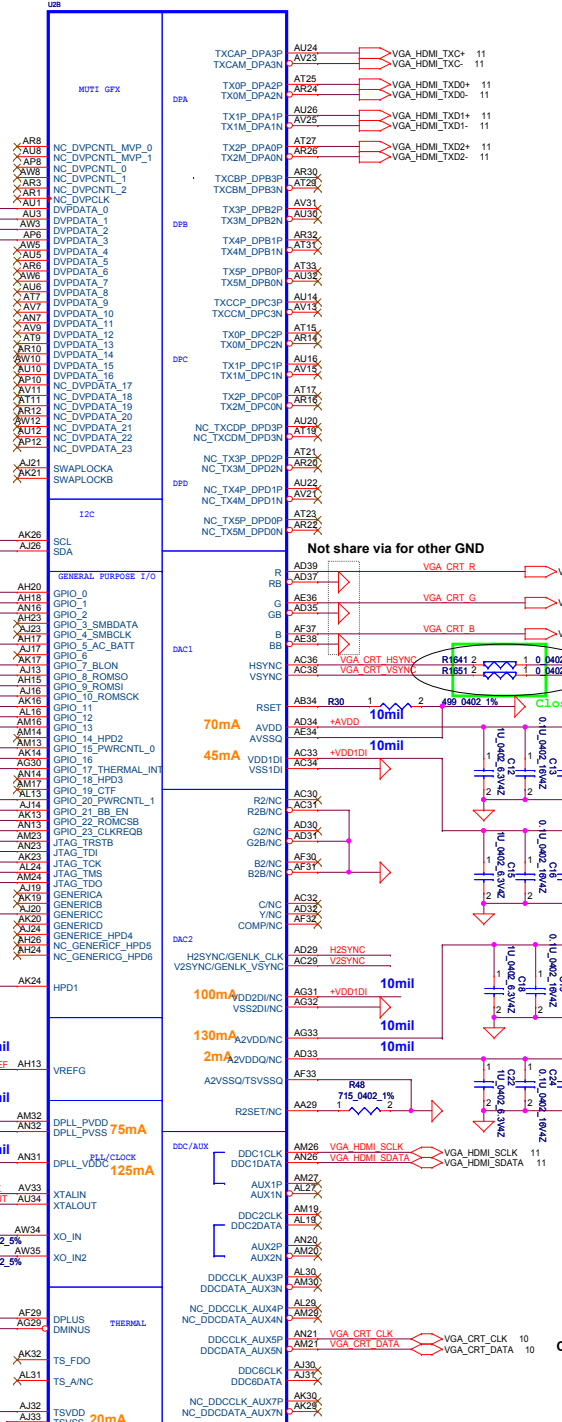
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GFX PCIe LANE REVERSAL



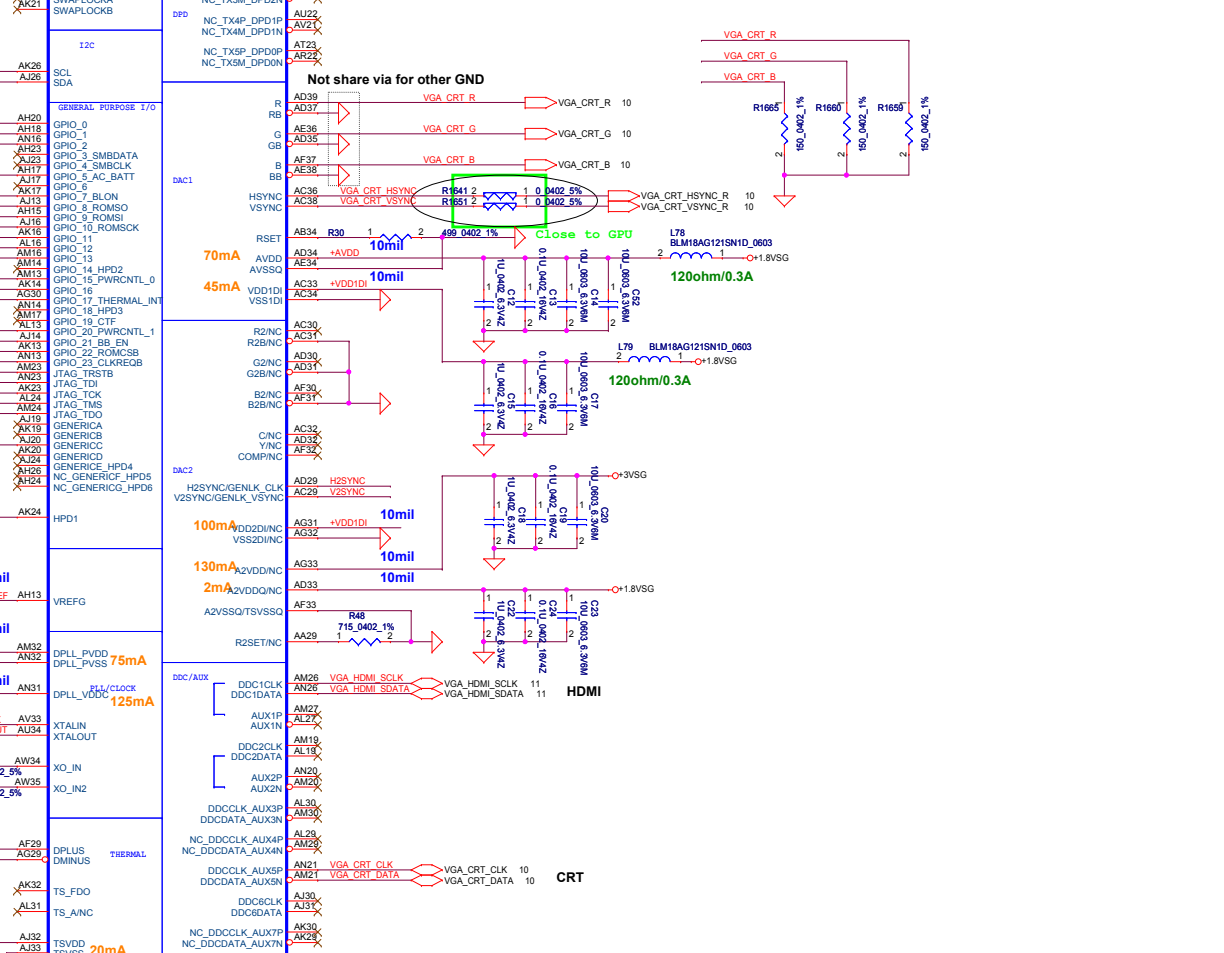
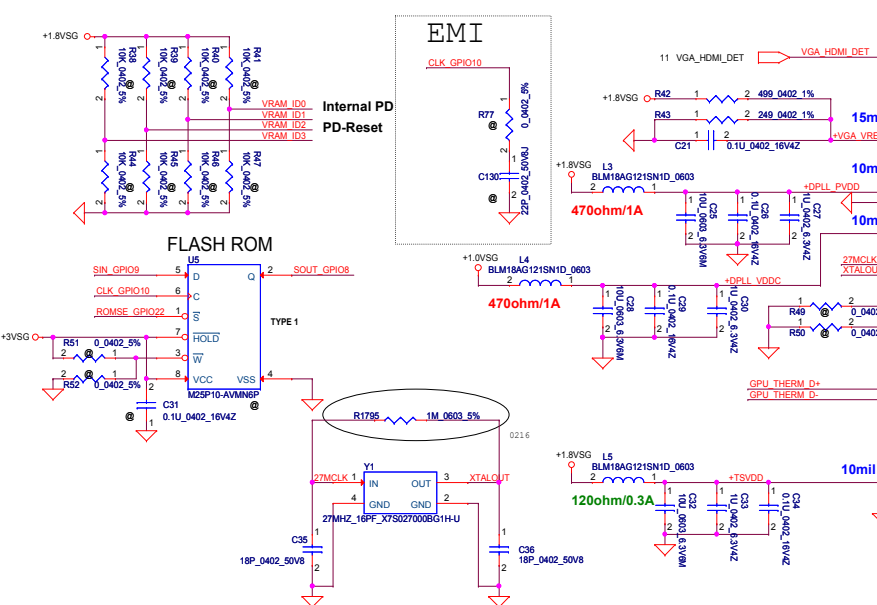
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Strap Name		Pin Straps description <all Internal PD>	Setting
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENE	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO12 GPIO13 GPIO11	GPIO13:12:11 (config 2,1,0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 G T/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK)	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI
	GPIO8 GPIO21 GENERICC GPIO5		

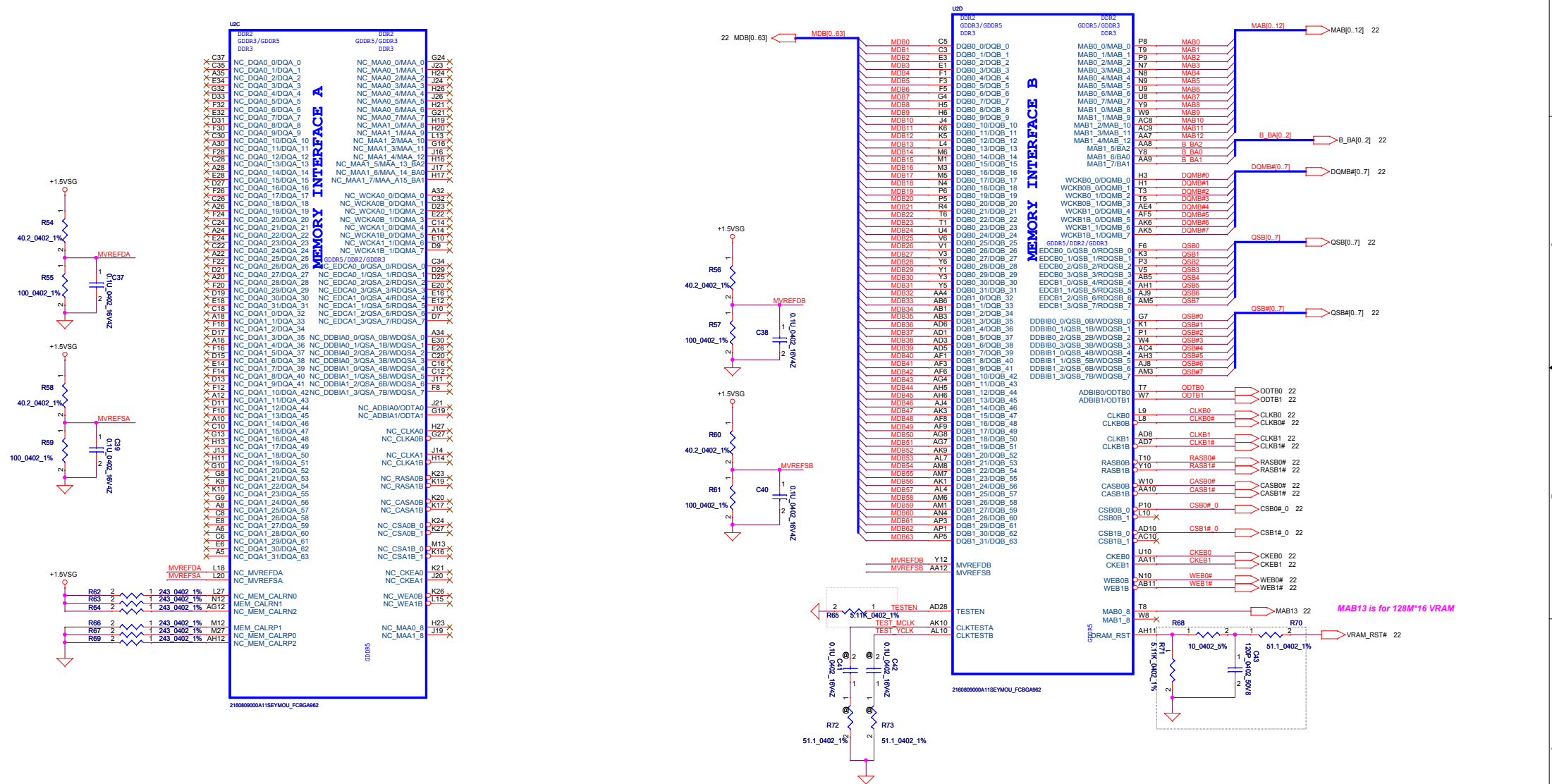


Seymour(XT)

VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung SA00094GS30 64M16 K4W1G1646G-BC11		0	0	0	0
Samsung SA00047QAD0 128M16 K4W2G1646G-BC11		0	0	1	1
Hynix SAU00141S60 64M16 B5TQ1G63DFR-11C		0	1	0	0
Hynix SAU0003Y030 128M16 B5TQ2G63DFR-11C		0	1	0	1

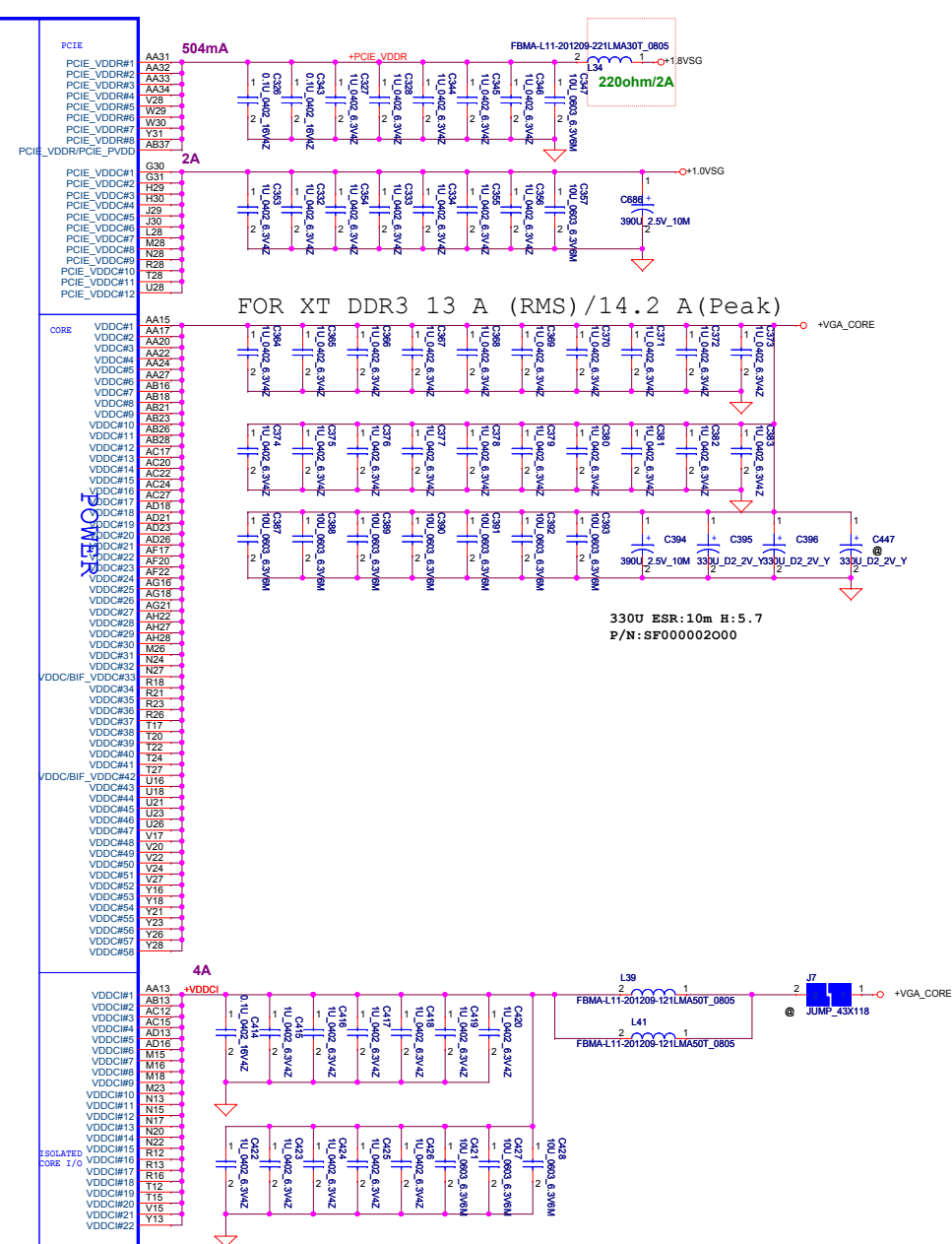
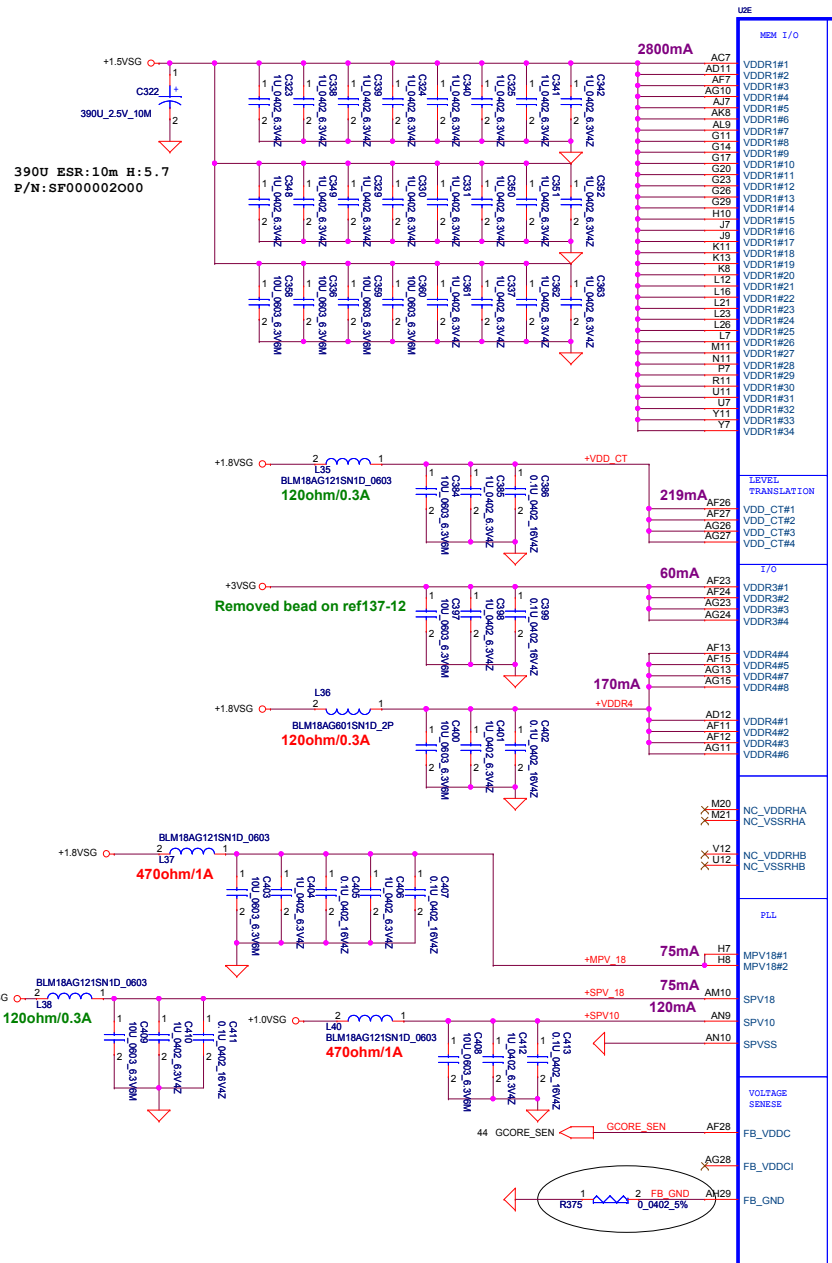


Robson,Seymour only support single channel memory (channel B only)



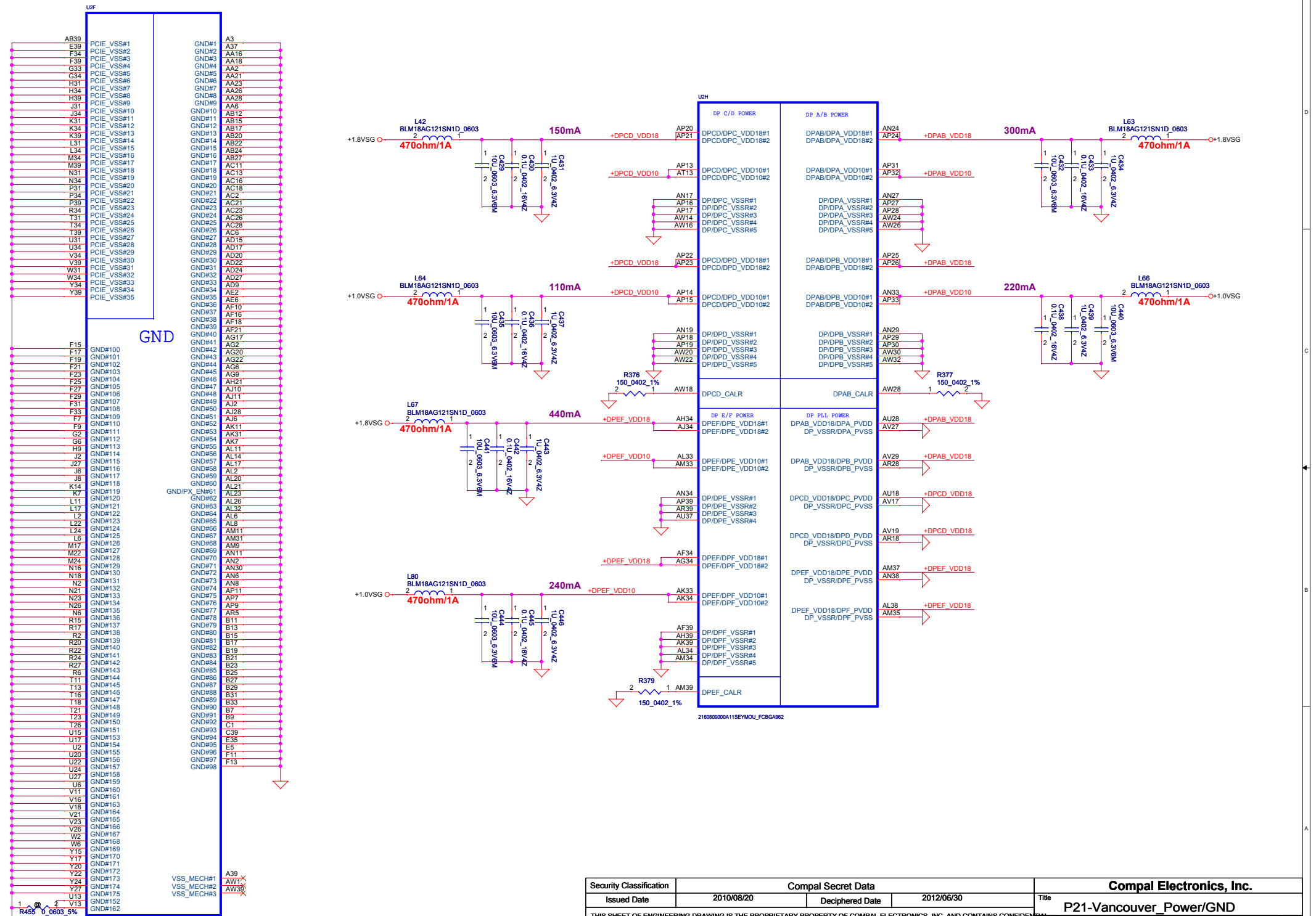
Pin	Signal	Pin	Signal
C37	NC_DQA0_0/DQA_0	G34	NC_MAA0_0/MAA_0
C36	NC_DQA0_1/DQA_1	J23	NC_MAA0_1/MAA_1
A35	NC_DQA0_2/DQA_2	H24	NC_MAA0_2/MAA_2
E34	NC_DQA0_3/DQA_3	J24	NC_MAA0_3/MAA_3
G33	NC_DQA0_4/DQA_4	H25	NC_MAA0_4/MAA_4
D33	NC_DQA0_5/DQA_5	J26	NC_MAA0_5/MAA_5
F32	NC_DQA0_6/DQA_6	H21	NC_MAA0_6/MAA_6
E32	NC_DQA0_7/DQA_7	G21	NC_MAA0_7/MAA_7
D31	NC_DQA0_8/DQA_8	H19	NC_MAA0_8/MAA_8
F30	NC_DQA0_9/DQA_9	H20	NC_MAA0_9/MAA_9
C30	NC_DQA0_10/DQA_10	H20	NC_MAA1_1/MAA_1
A30	NC_DQA0_11/DQA_11	G16	NC_MAA1_2/MAA_10
F28	NC_DQA0_12/DQA_12	H16	NC_MAA1_3/MAA_11
C28	NC_DQA0_13/DQA_13	H16	NC_MAA1_4/MAA_12
E28	NC_DQA0_14/DQA_14	J17	NC_MAA1_5/MAA_13_BA2
D27	NC_DQA0_15/DQA_15	H17	NC_MAA1_6/MAA_14_BA0
F26	NC_DQA0_16/DQA_16	D19	NC_MAA1_7/MAA_15_BA1
C26	NC_DQA0_17/DQA_17	D20	NC_WCKA0_0/DQMA_0
A26	NC_DQA0_18/DQA_18	D23	NC_WCKA0_1/DQMA_1
F24	NC_DQA0_19/DQA_19	E22	NC_WCKA0_2/DQMA_2
C24	NC_DQA0_20/DQA_20	C14	NC_WCKA0B_1/DQMA_3
A24	NC_DQA0_21/DQA_21	A14	NC_WCKA1_0/DQMA_4
E24	NC_DQA0_22/DQA_22	E10	NC_WCKA1_0/DQMA_4
C22	NC_DQA0_23/DQA_23	D19	NC_WCKA1B_1/DQMA_7
A22	NC_DQA0_24/DQA_24	D19	NC_WCKA1B_1/DQMA_7
F22	NC_DQA0_25/DQA_25	C34	GDDR5/DDB2/GDDR3
D22	NC_DQA0_26/DQA_26	D25	NC_EDCA0_0/QSA_0/RDQSA_0
A20	NC_DQA0_27/DQA_27	E20	NC_EDCA0_2/QSA_2/RDQSA_2
F20	NC_DQA0_28/DQA_28	E16	NC_EDCA0_3/QSA_3/RDQSA_3
C20	NC_DQA0_29/DQA_29	E12	NC_EDCA1_0/QSA_4/RDQSA_4
E18	NC_DQA0_30/DQA_30	J10	NC_EDCA1_1/QSA_5/RDQSA_5
C18	NC_DQA0_31/DQA_31	D7	NC_EDCA1_2/QSA_6/RDQSA_6
A18	NC_DQA1_0/DQA_32	D7	NC_EDCA1_3/QSA_7/RDQSA_7
F18	NC_DQA1_1/DQA_33	A34	NC_DDBIA0_0/QSA_8B/WDQSA_0
D17	NC_DQA1_2/DQA_34	E30	NC_DDBIA0_1/QSA_18/WDQSA_1
A16	NC_DQA1_3/DQA_35	C20	NC_DDBIA0_2/QSA_28/WDQSA_2
F16	NC_DQA1_4/DQA_36	C16	NC_DDBIA0_3/QSA_38/WDQSA_3
C16	NC_DQA1_5/DQA_37	C12	NC_DDBIA1_0/QSA_48/WDQSA_4
E14	NC_DQA1_6/DQA_38	J11	NC_DDBIA1_1/QSA_58/WDQSA_5
F14	NC_DQA1_7/DQA_39	F8	NC_DDBIA1_2/QSA_68/WDQSA_6
D13	NC_DQA1_8/DQA_40	F8	NC_DDBIA1_3/QSA_78/WDQSA_7
C13	NC_DQA1_9/DQA_41	J21	NC_ADDBIA0/ODTB0
A12	NC_DQA1_10/DQA_42	G19	NC_ADDBIA1/ODTB1
F12	NC_DQA1_11/DQA_43	H27	NC_CLKA0
D11	NC_DQA1_12/DQA_44	G27	NC_CLKA0B
A10	NC_DQA1_13/DQA_45	J14	NC_CLKA1
F10	NC_DQA1_14/DQA_46	H14	NC_CLKA1B
C10	NC_DQA1_15/DQA_47	K23	NC_RAS0A0
E10	NC_DQA1_16/DQA_48	C19	NC_RAS0A1
H11	NC_DQA1_17/DQA_49	K20	NC_CAS0A0B
G10	NC_DQA1_18/DQA_50	C17	NC_CAS0A1B
F10	NC_DQA1_19/DQA_51	K24	NC_CSA0B_0
G8	NC_DQA1_20/DQA_52	K27	NC_CSA0B_1
K9	NC_DQA1_21/DQA_53	M13	NC_CSA1B_0
K10	NC_DQA1_22/DQA_54	K16	NC_CSA1B_1
G9	NC_DQA1_23/DQA_55	K21	NC_CKEA0
E8	NC_DQA1_24/DQA_56	J20	NC_CKEA1
C8	NC_DQA1_25/DQA_57	K26	NC_WEA0B
A8	NC_DQA1_26/DQA_58	L15	NC_WEA0A
F8	NC_DQA1_27/DQA_59	L15	NC_WEA1B
E8	NC_DQA1_28/DQA_60	H23	NC_MAA0_8
C8	NC_DQA1_29/DQA_61	J19	NC_MAA1_8
A5	NC_DQA1_30/DQA_62		
F5	NC_DQA1_31/DQA_63		

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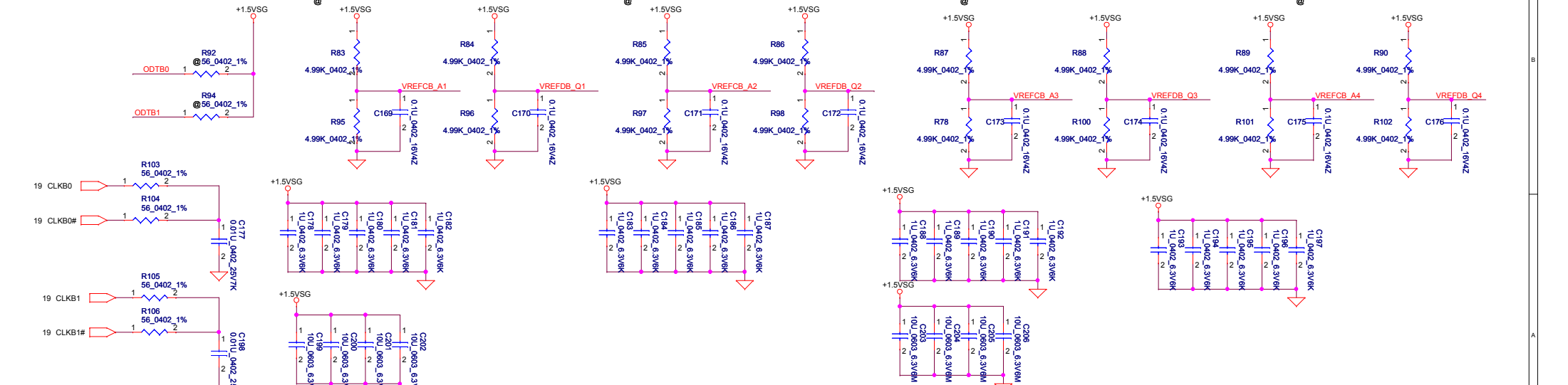
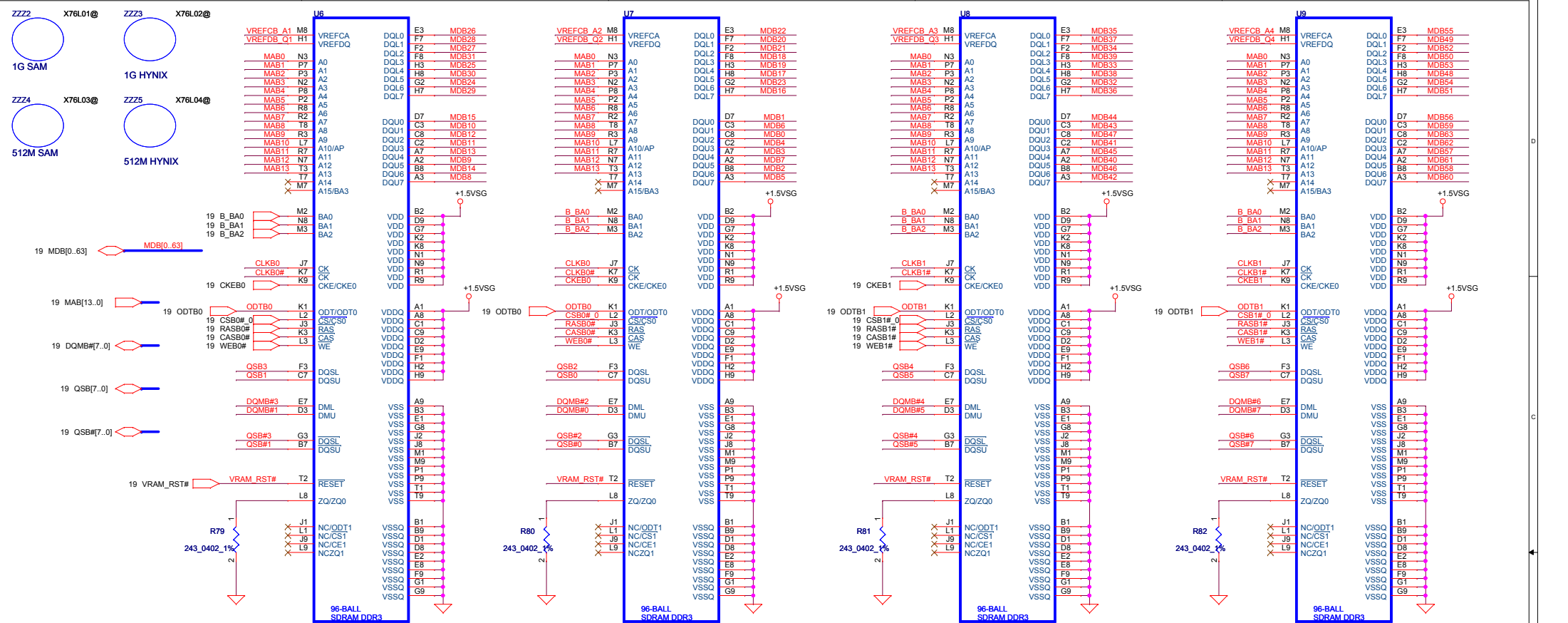


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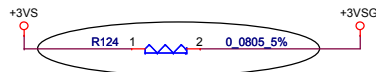


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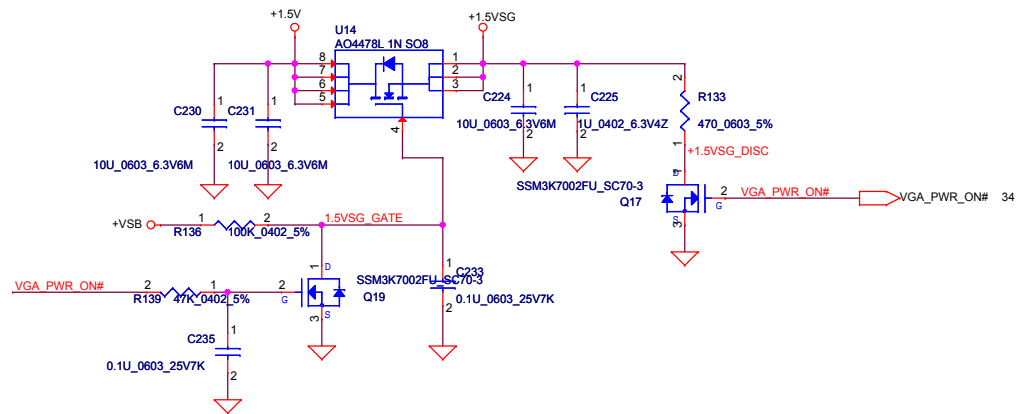
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Delay SUSP# 10ms

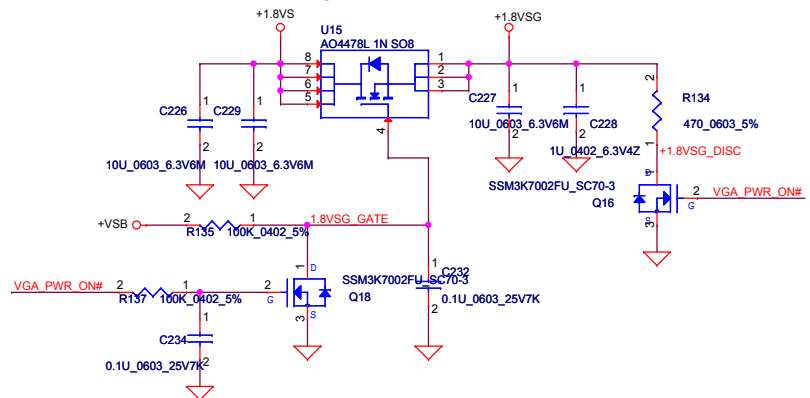


+1.5V TO +1.5VSG

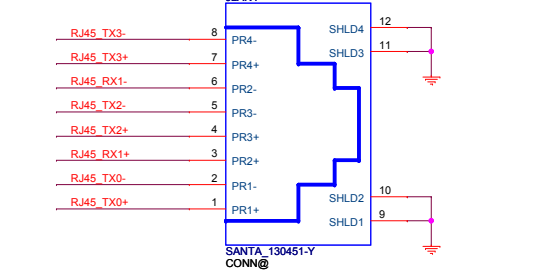
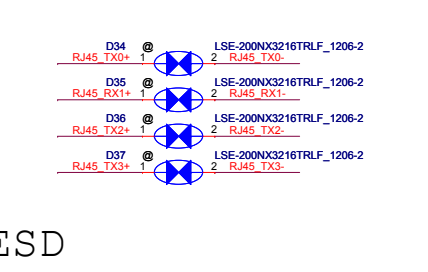
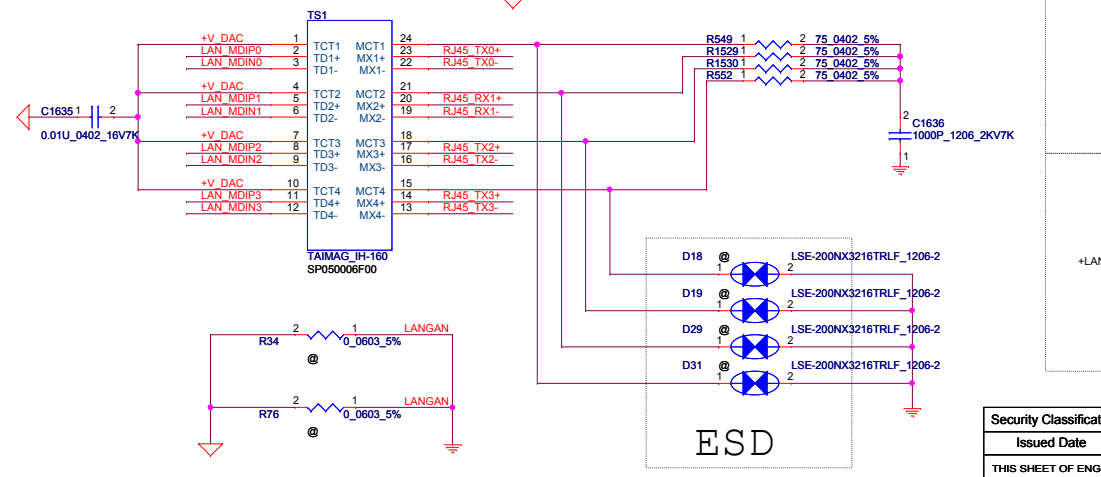
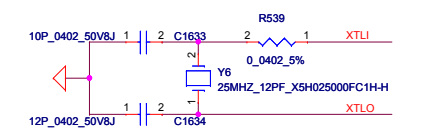
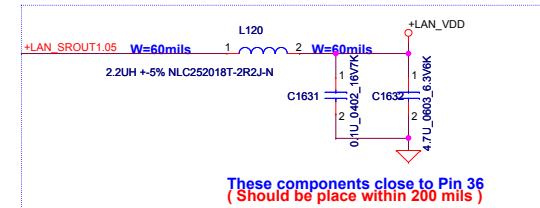
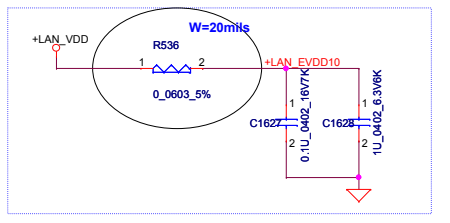
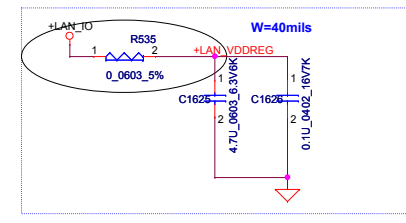
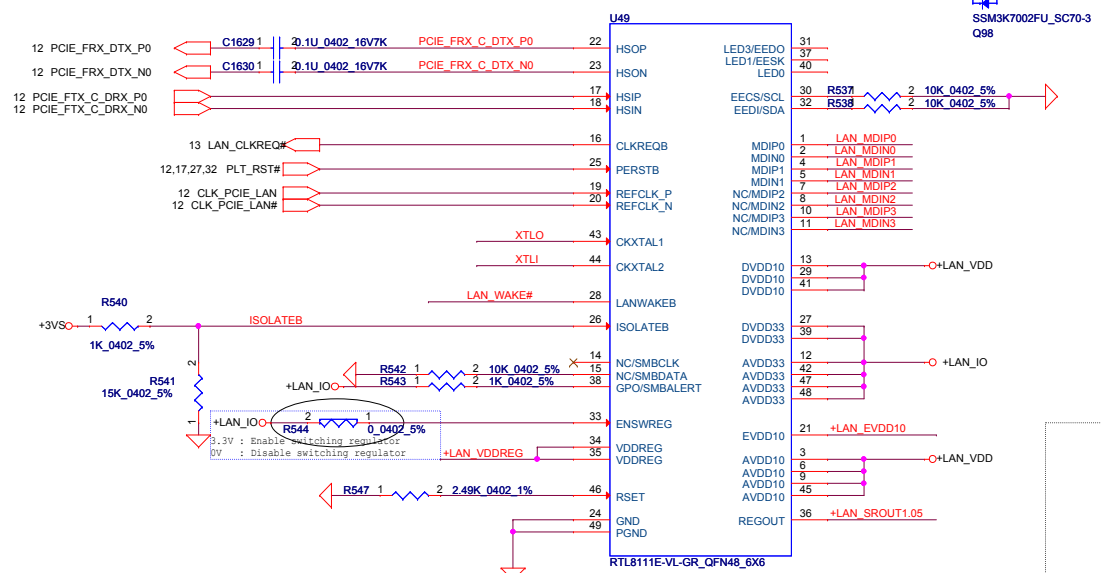
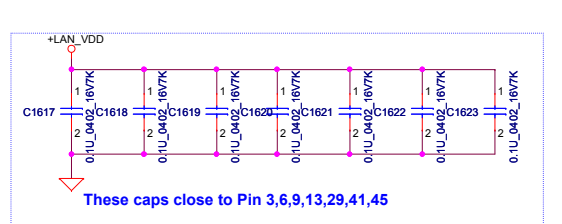
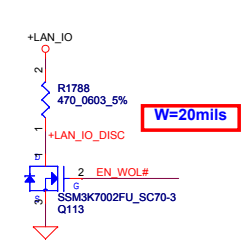
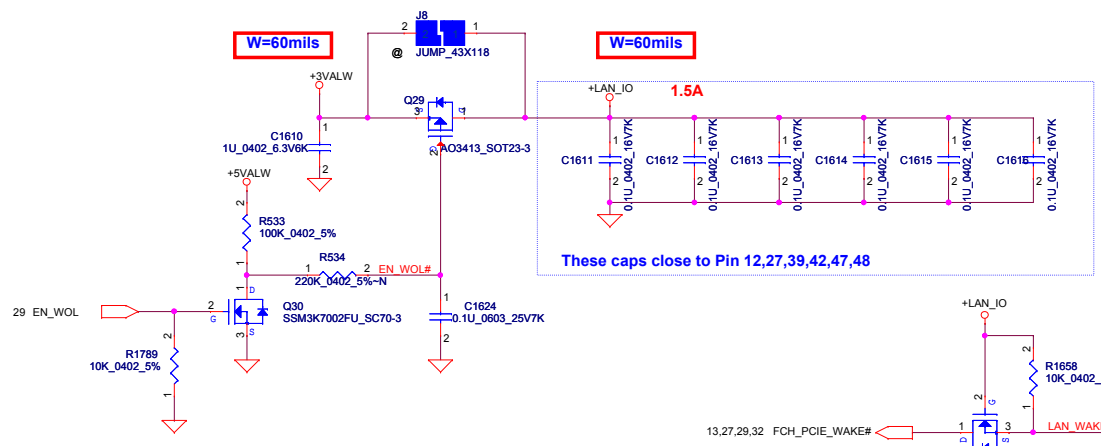


+1.8VS TO +1.8VSG

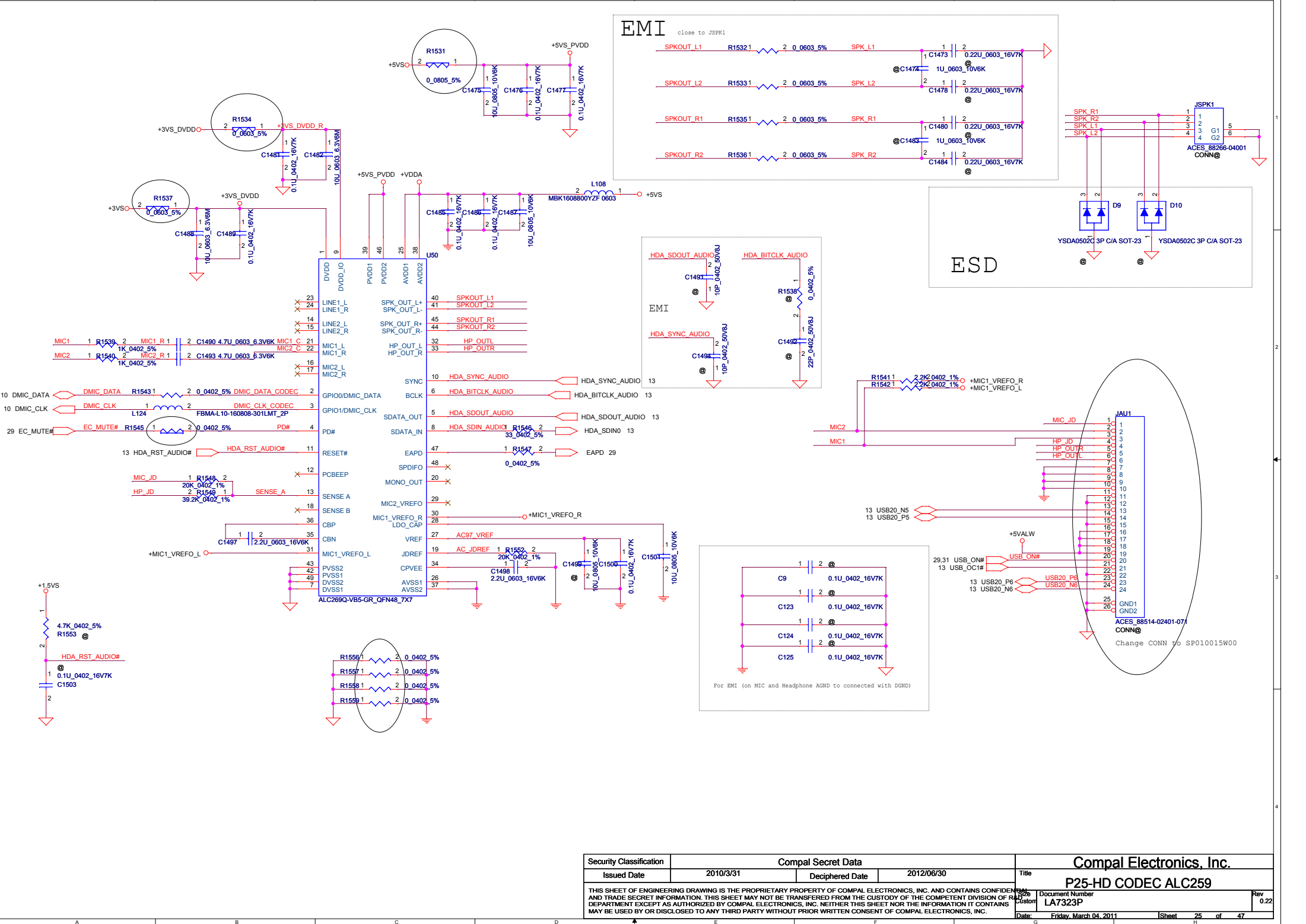
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Document Number				Rev	
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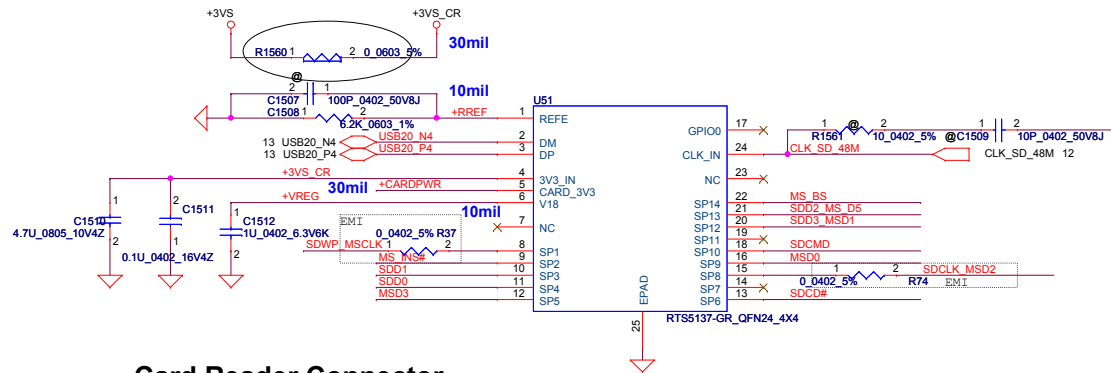


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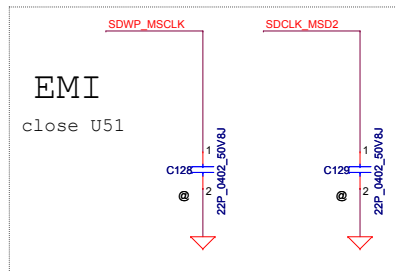
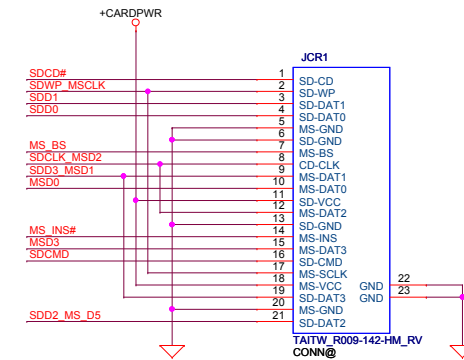
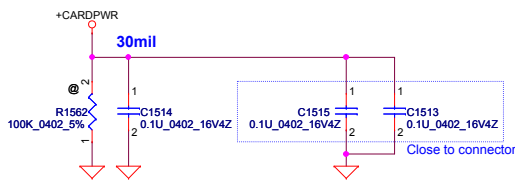
Compal Electronics, Inc.
P25-HD CODEC ALC259

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Card Reader RTS5137 (only SD/MMC/MS function)



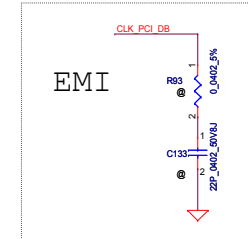
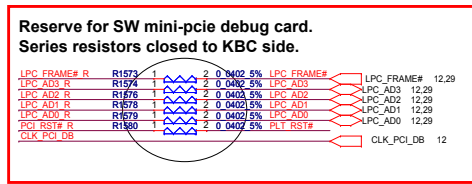
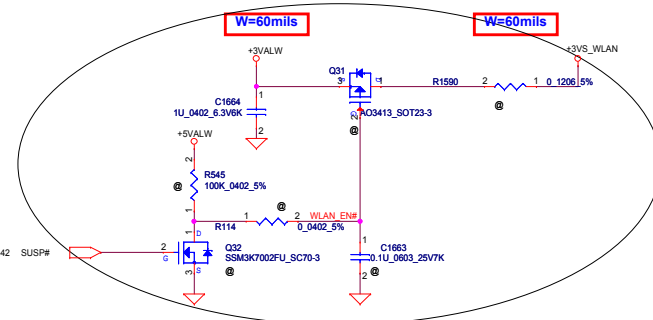
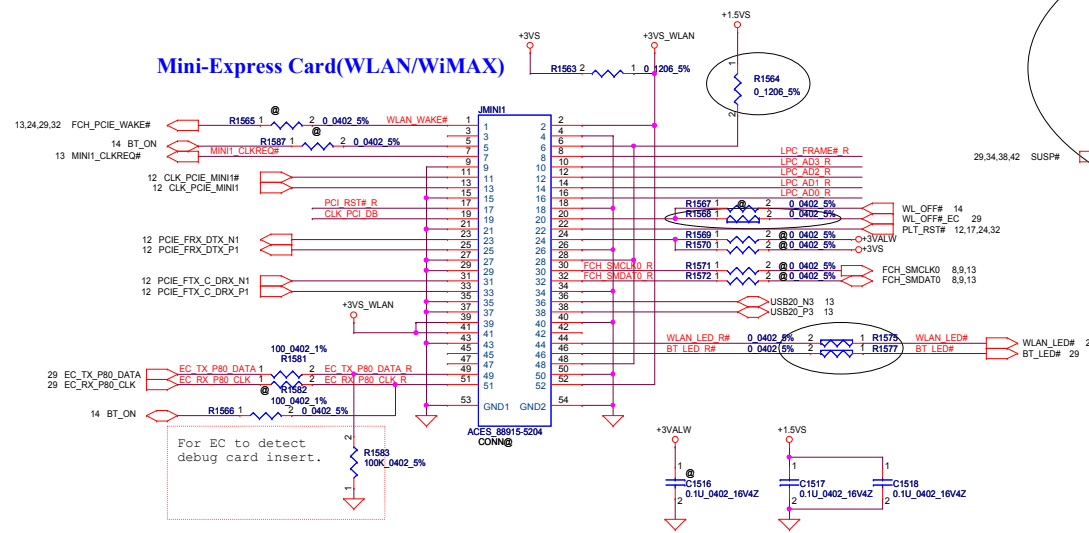
Card Reader Connector



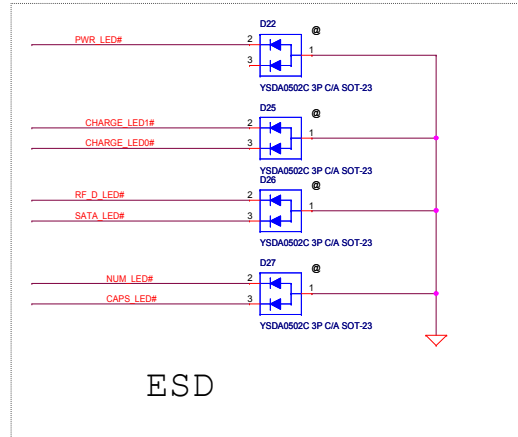
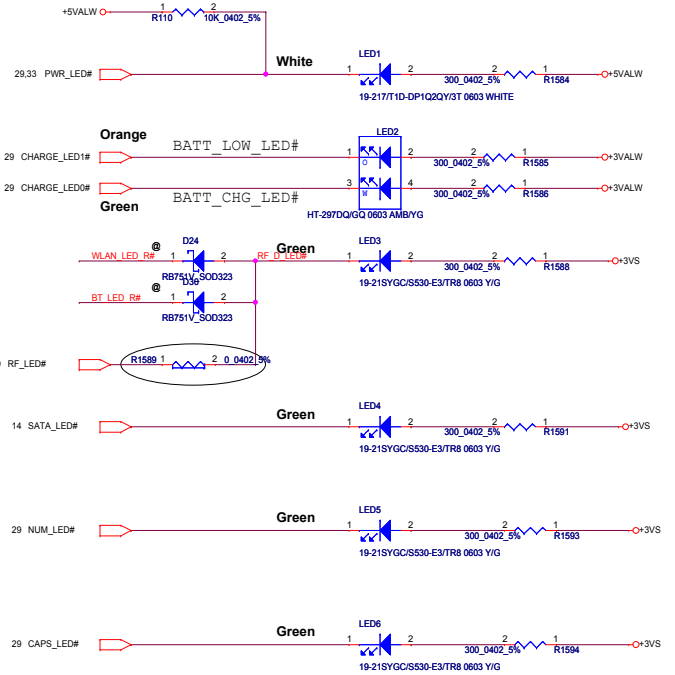
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Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)

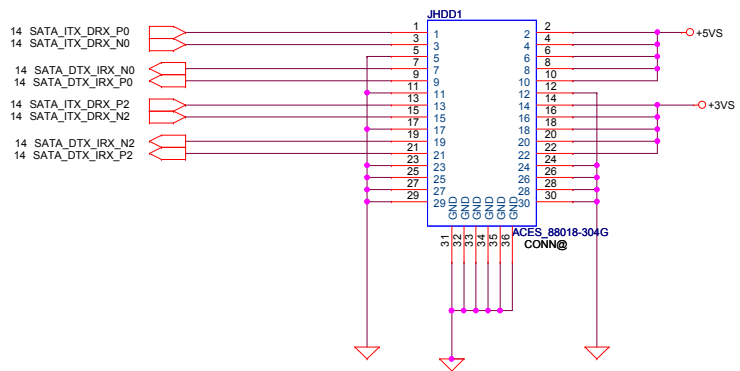


LED

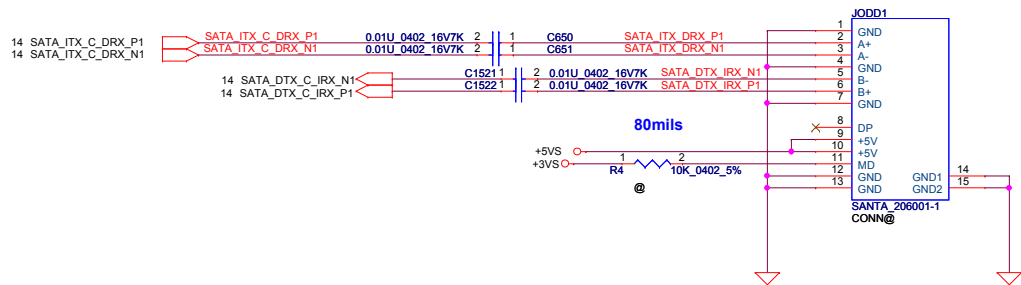


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SATA HDD BTB Conn.

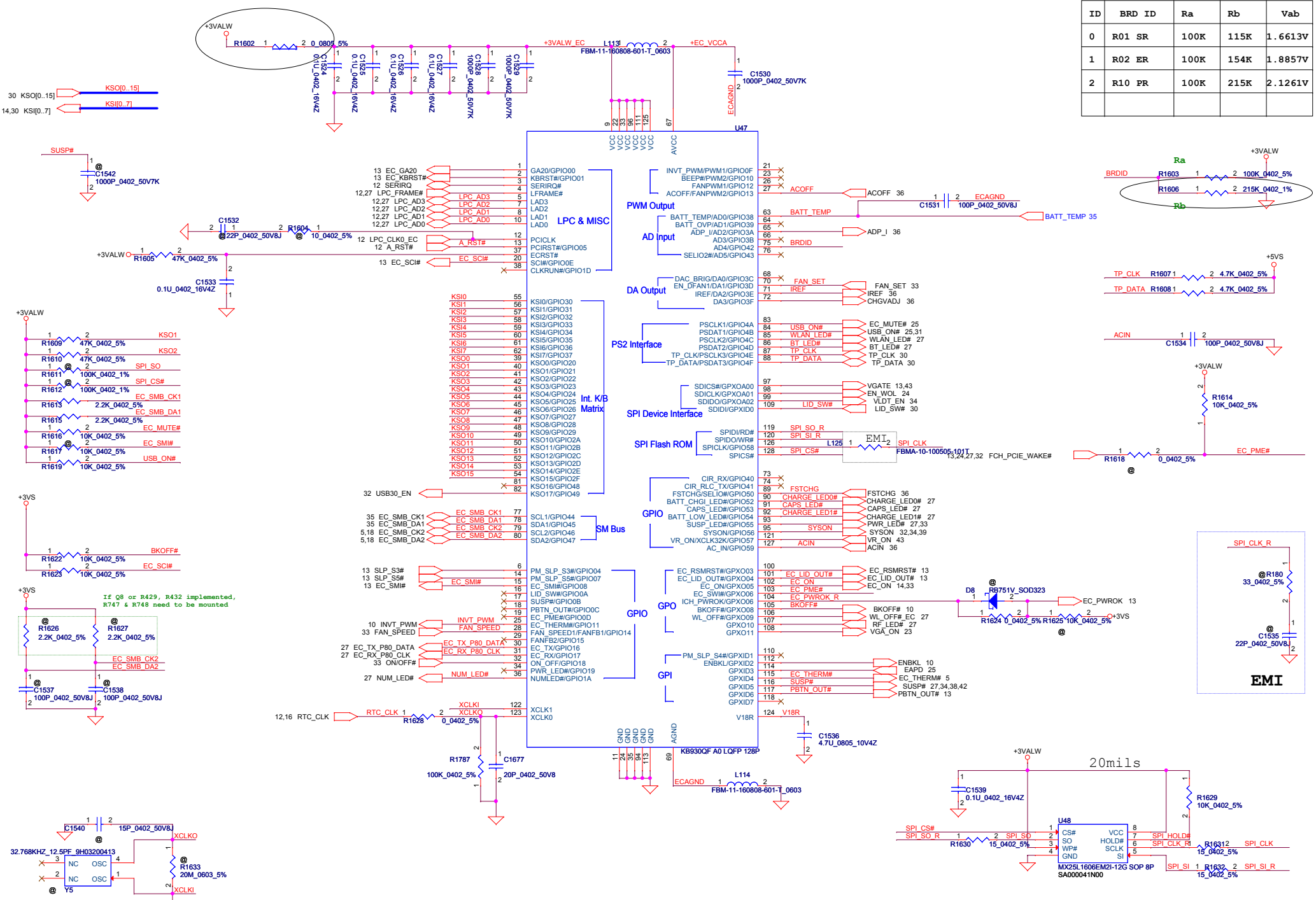


SATA ODD FFC Conn.



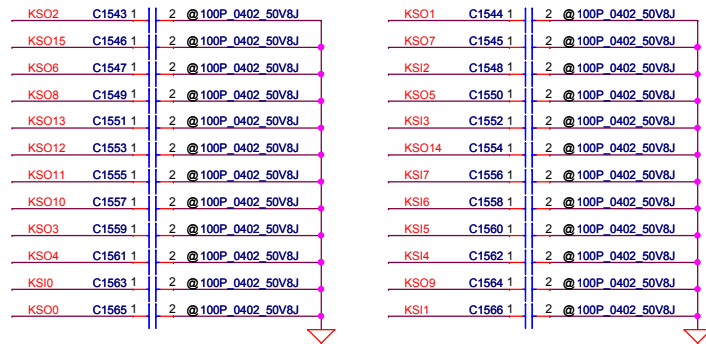
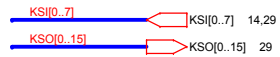
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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	115K	1.6613V
1	R02 ER	100K	154K	1.8857V
2	R10 PR	100K	215K	2.1261V

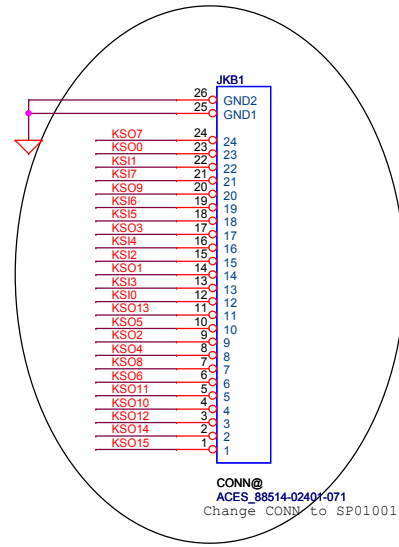


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				P29-BIOS & EC KB930	
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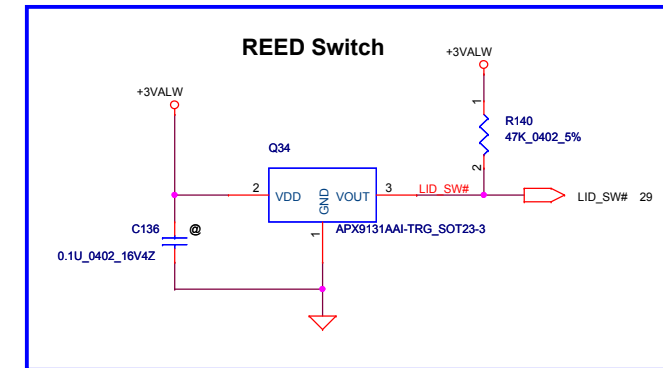
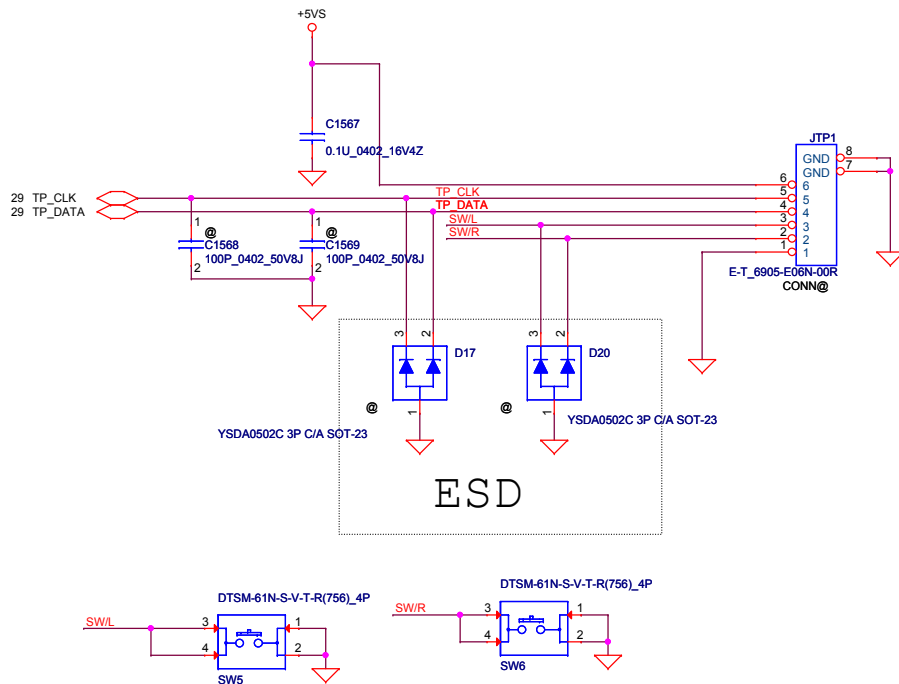
INT_KBD Conn.



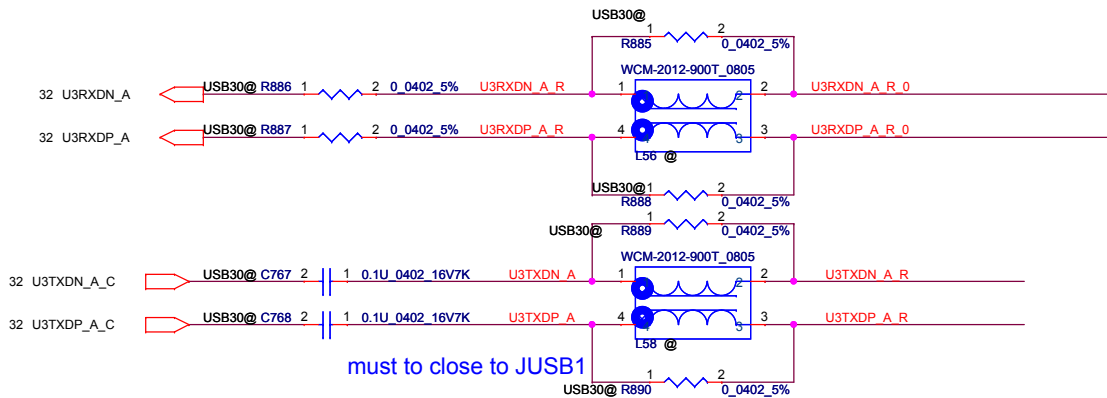
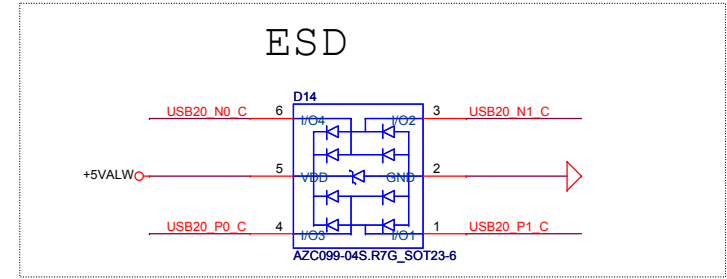
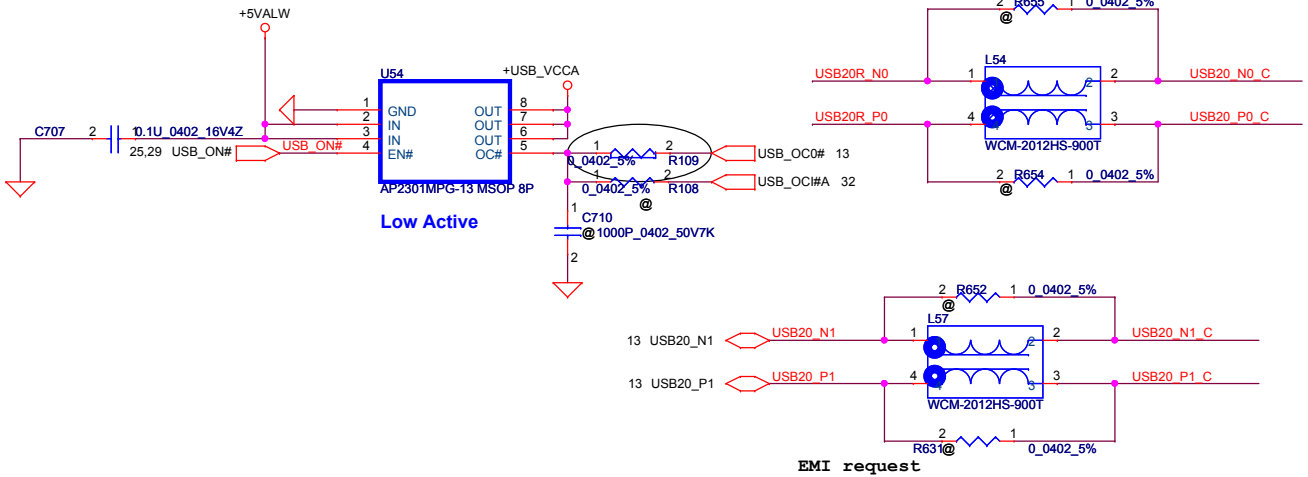
CONN PIN define need double check



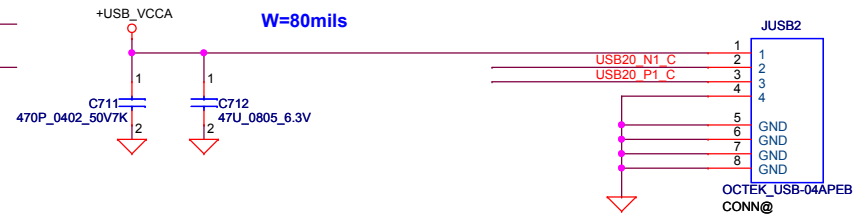
To TP/B Conn.



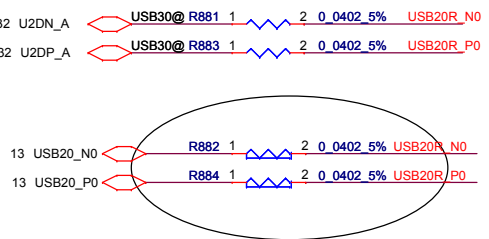
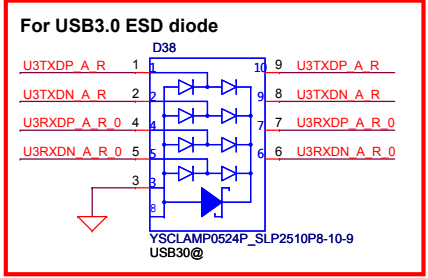
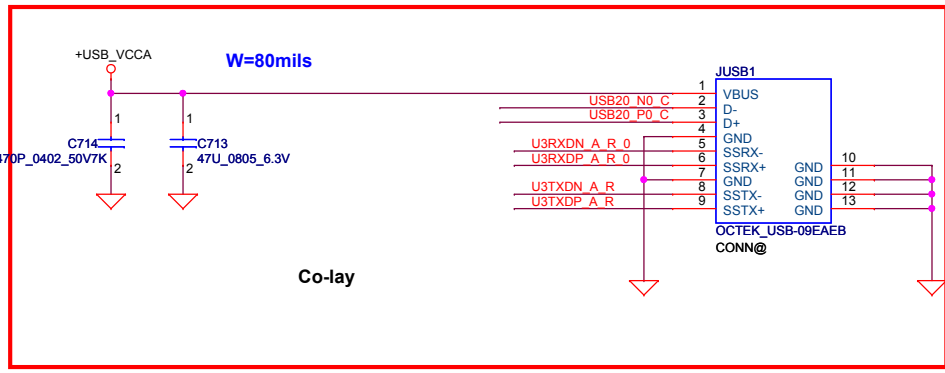
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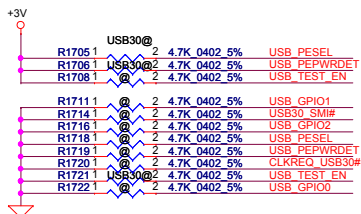
Left USB Conn.



must to close to JUSB1



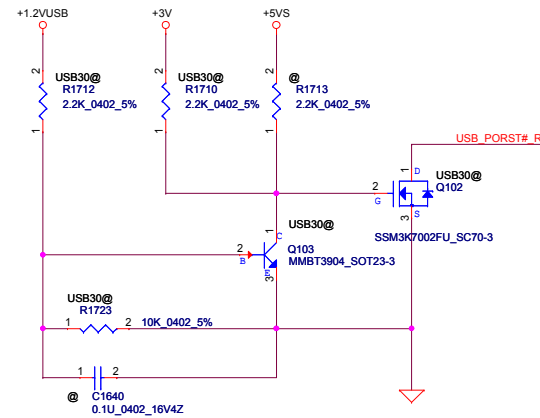
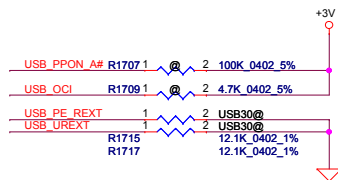
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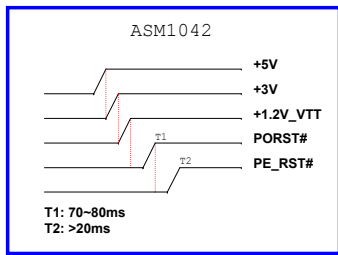
For WAKE Function

USB_PEPWRDET

	R1719	R1706
S1	Mount	@
S3	@	Mount

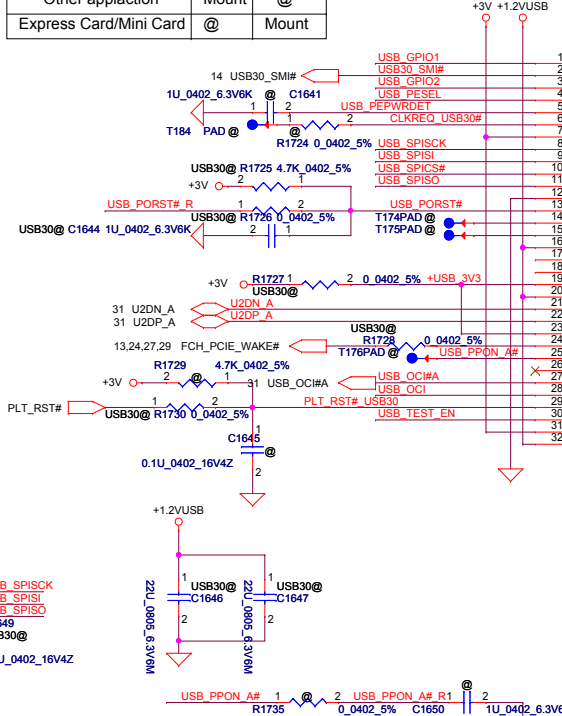
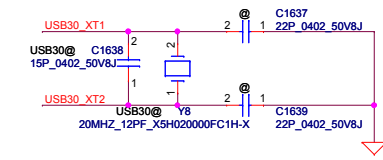


Power Sequence

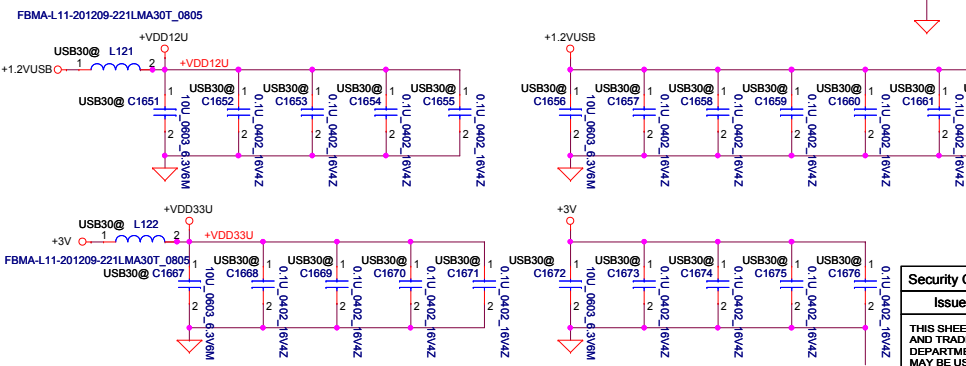
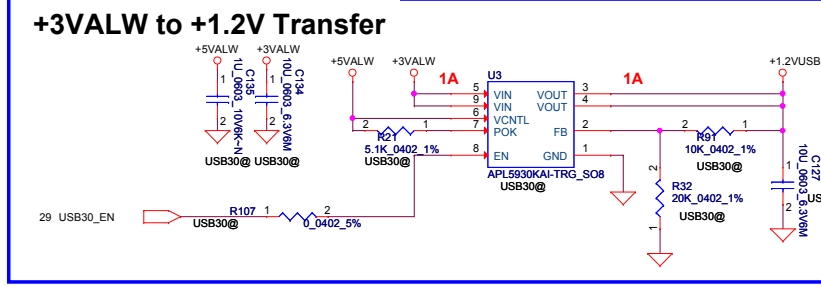
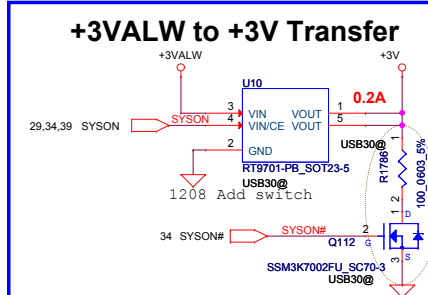
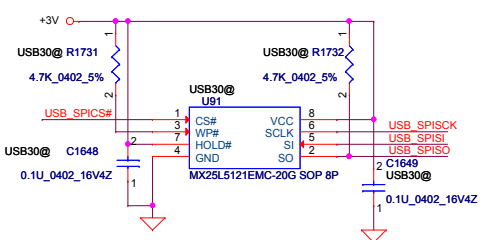


USB_PSEL

	R808	R825
Other appclation	Mount	@
Express Card/Mini Card	@	Mount

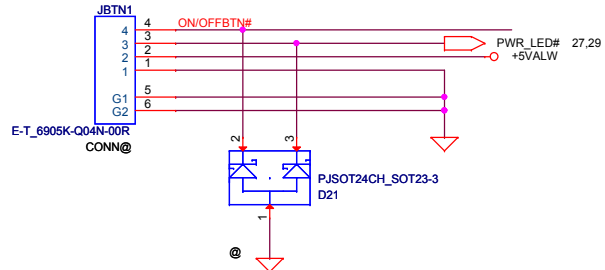
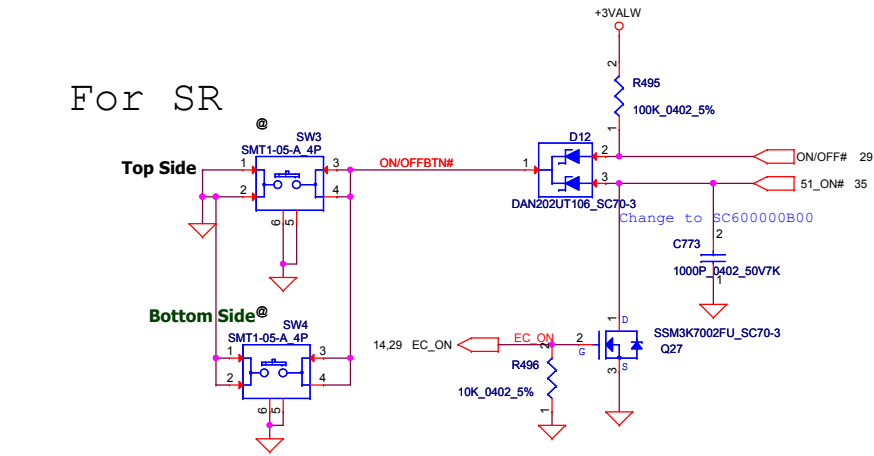


ASM1042 (TQFN 64)

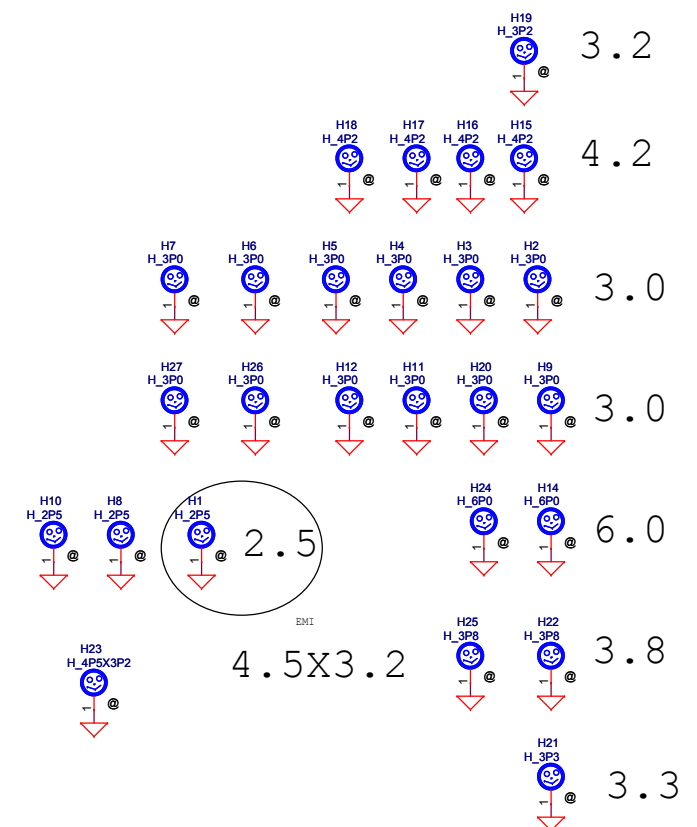
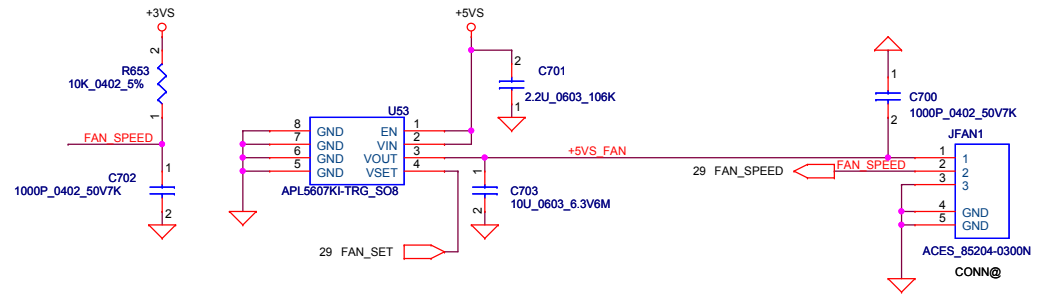


ON/OFF switch Power Button

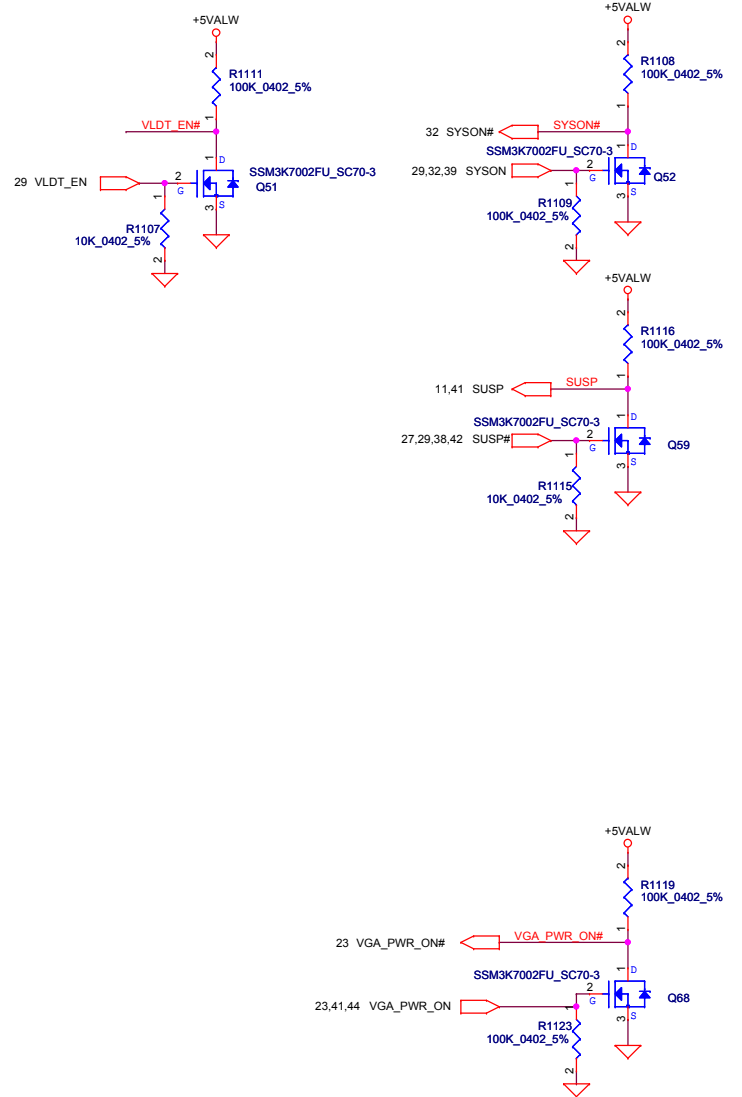
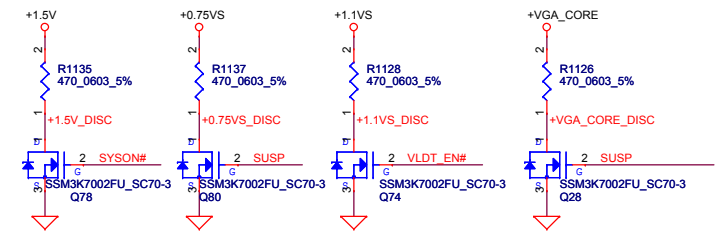
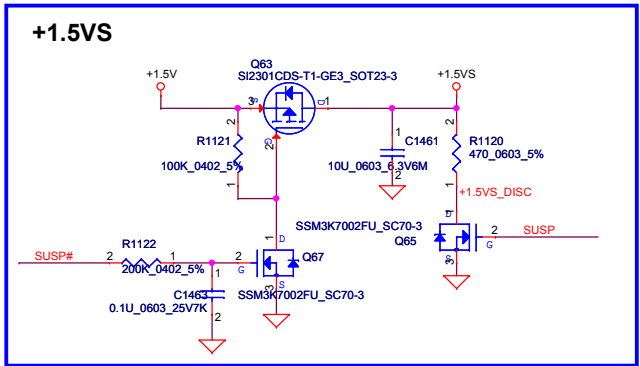
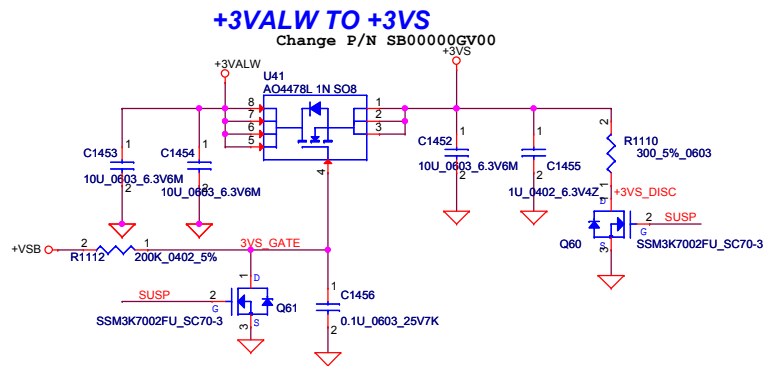
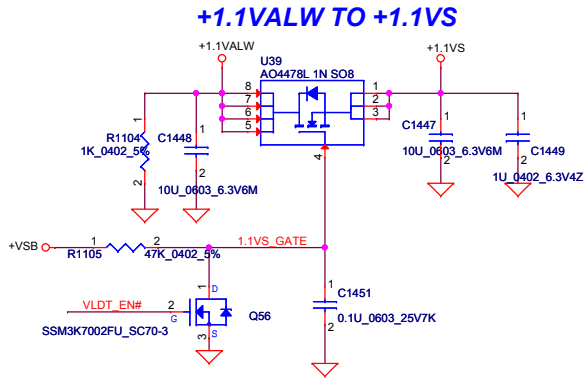
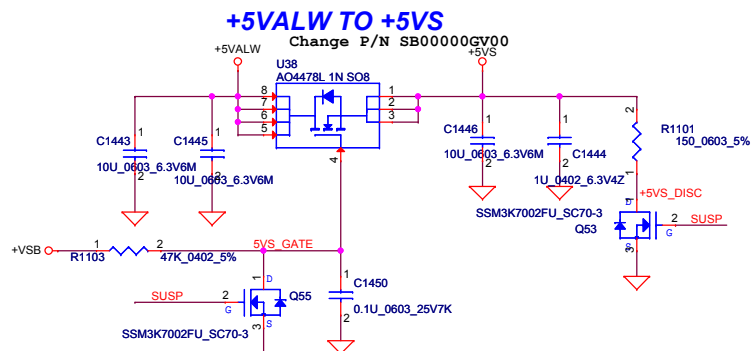
For SR



Fan Control Circuit

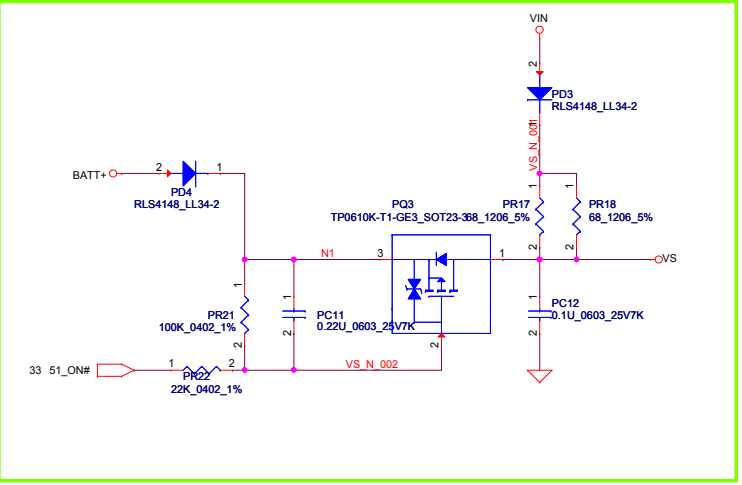
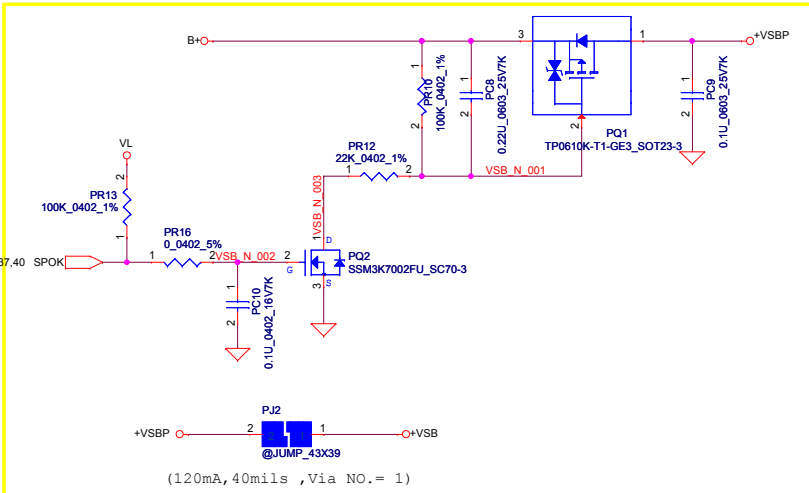
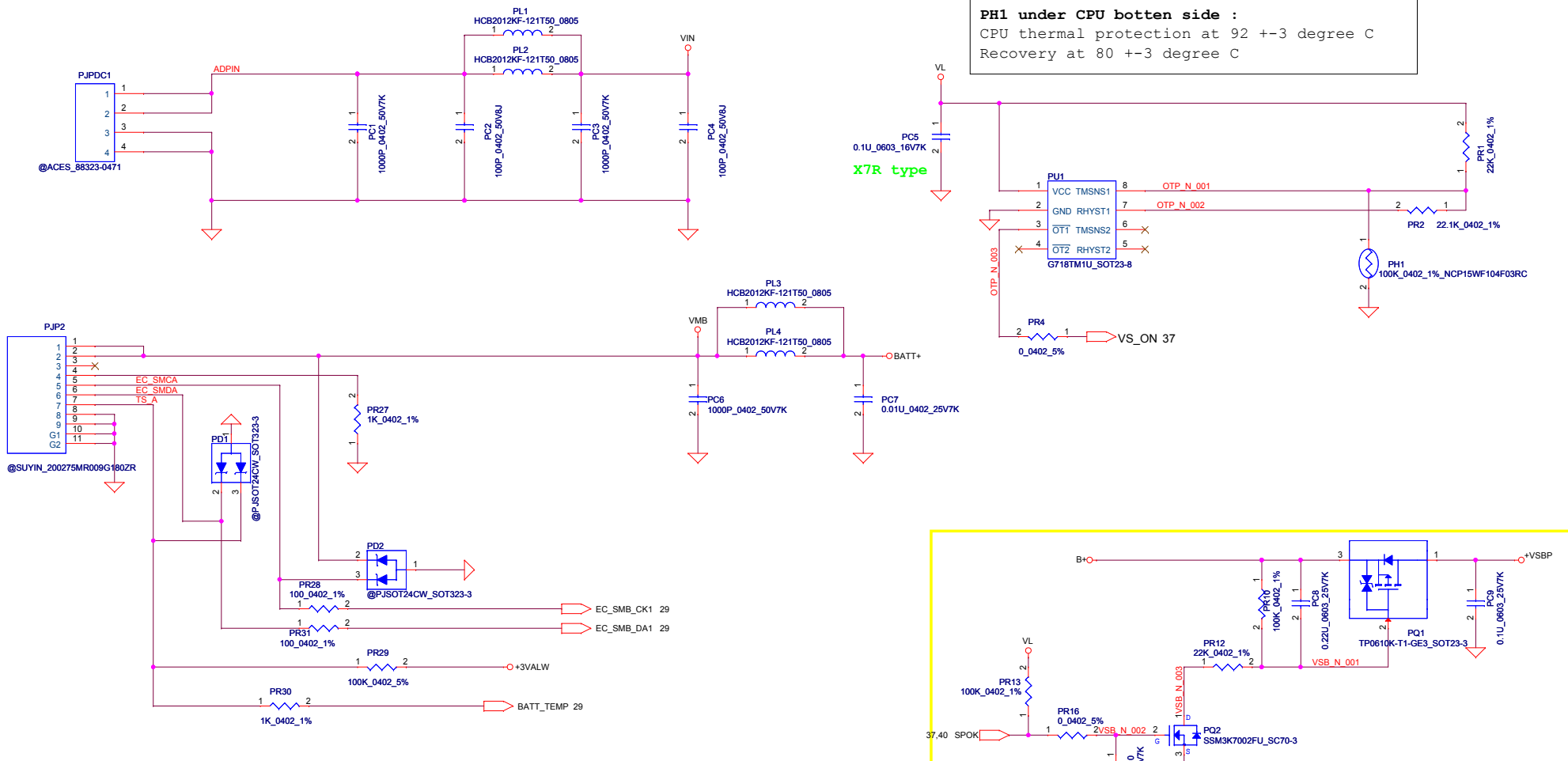


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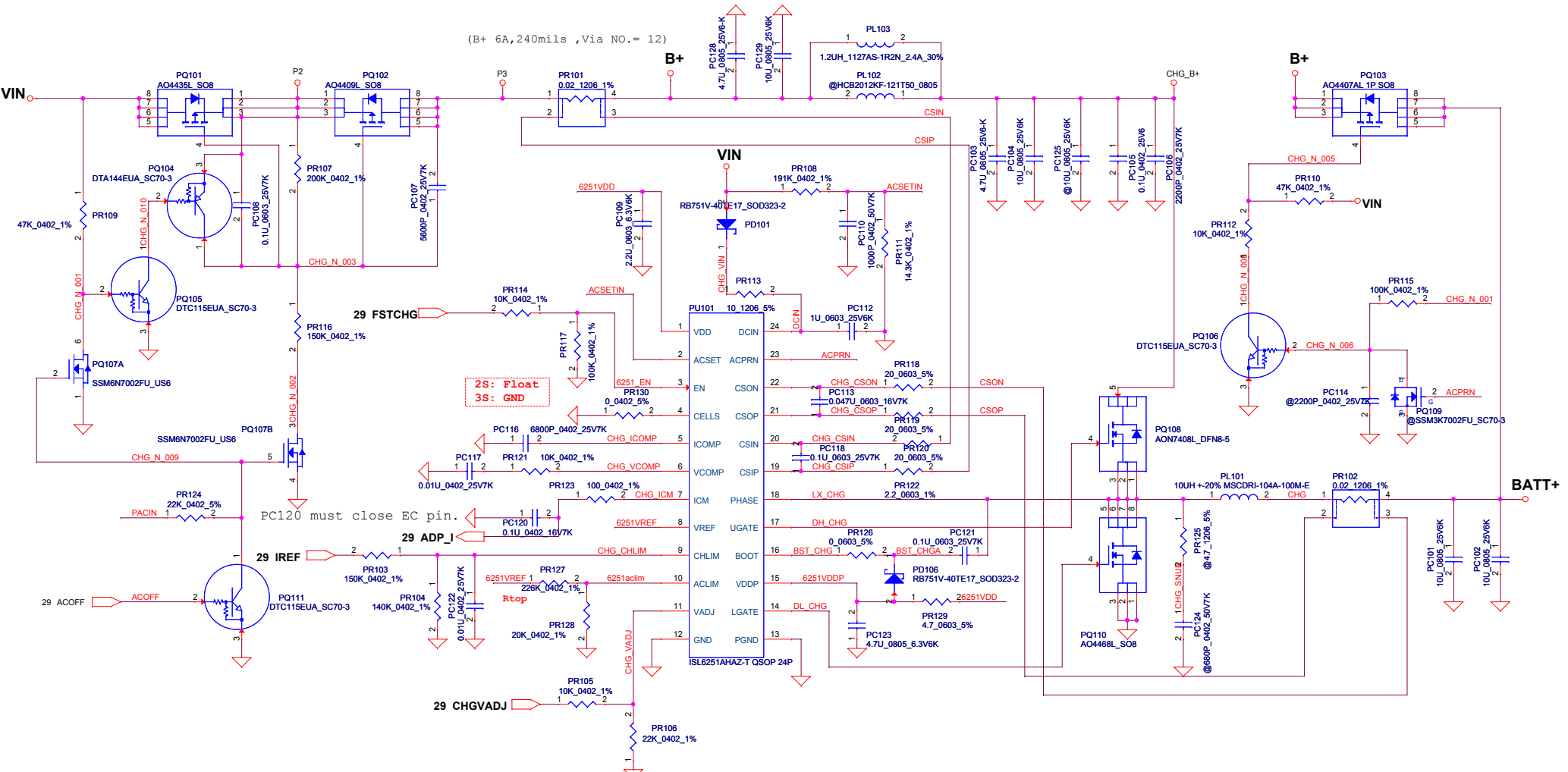
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PH1 under CPU bottom side :
 CPU thermal protection at 92 +/-3 degree C
 Recovery at 80 +/-3 degree C



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				DCIN / BATT CONN / OTP
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(B+ 6A, 240mils, Via NO. = 12)



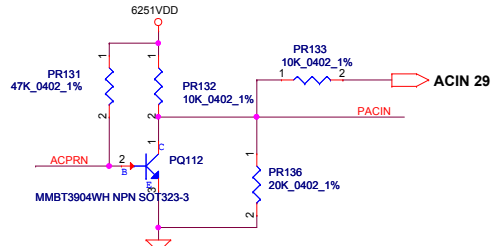
CP= 85%*Iada;
 Iada=0~4.737A(90W); CP=4.03A; where Raccdet=0.020ohm, where Rtop=12.4K
 90W for Dis: Rtop:SD00000AJ80
 Iada=0~3.421A(65W); CP=2.91A; where Raccdet=0.020ohm, where Rtop=226K
 65W for UMA: Rtop:SD034226380
 Astro2010_01_15 need confirm P/N

CP mode
 $V_{acim} = VREF * (Rbot / (Rinternal / (Rtop / (Rinternal + Rbot) / Rinternal))$
 when 90W $V_{acim} = 2.39 * (20K / (152K / (20K / (152K + 12.4K) / 152K)) = 1.44966V$
 when 65W $V_{acim} = 2.39 * (20K / (152K / (20K / (152K + 226K) / 152K)) = 0.38914V$
 $I_{input} = (1 / Raccdet) * ((0.05 * V_{acim} / VREF + 0.05))$
 when 90W, $I_{input} = (1 / 0.02) * (0.05 * 1.44966 / 2.39 + 0.05) = 4.02A$
 when 65W, $I_{input} = (1 / 0.02) * (0.05 * 0.38914 / 2.39 + 0.05) = 2.92A$

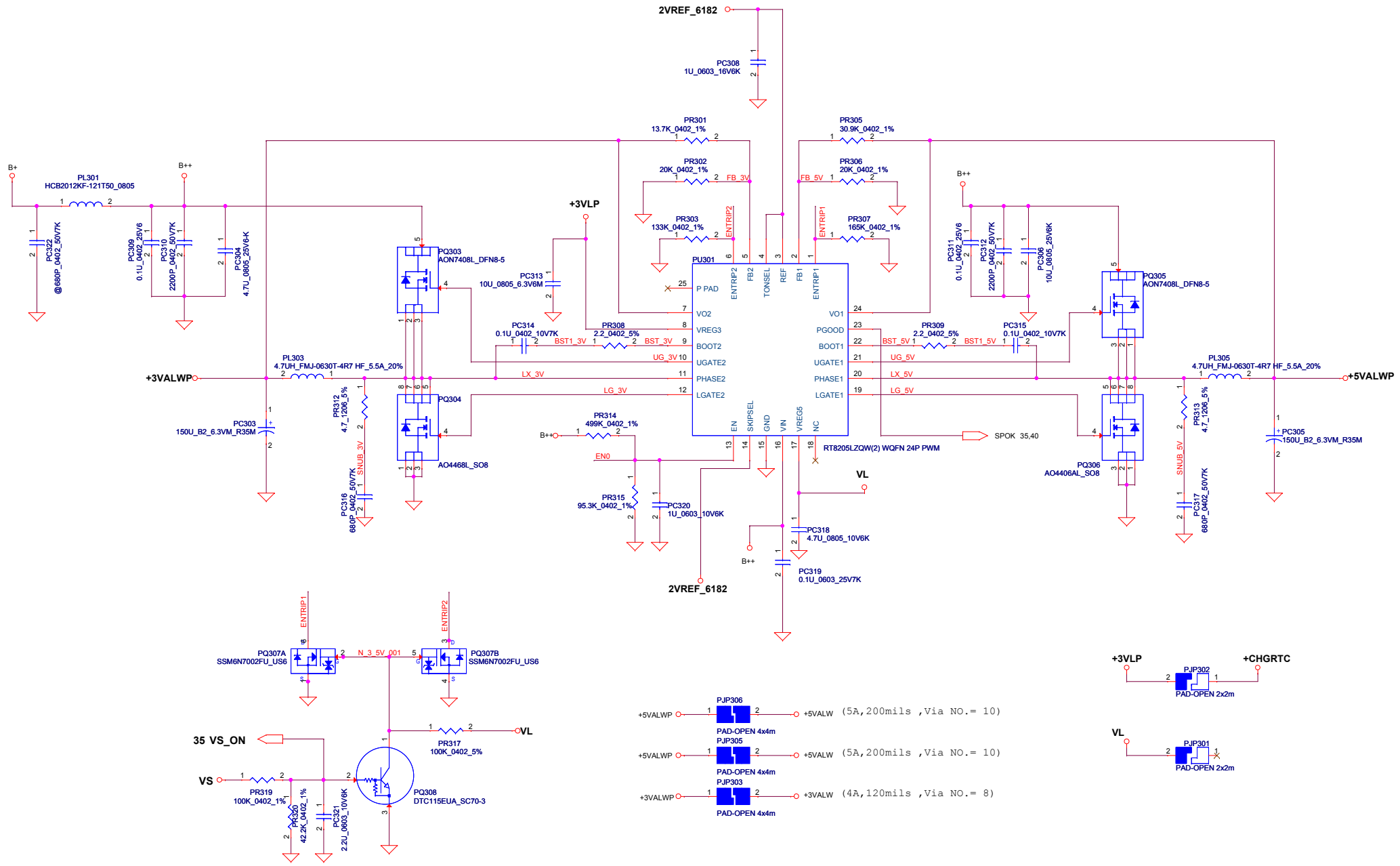
CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

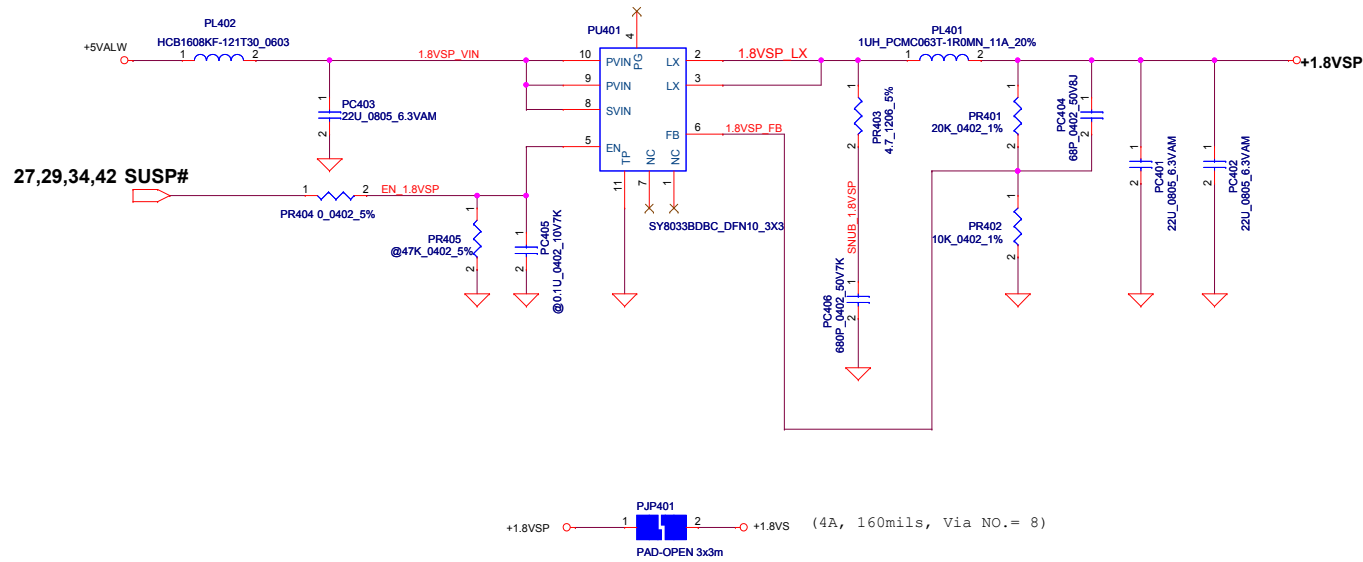


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EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

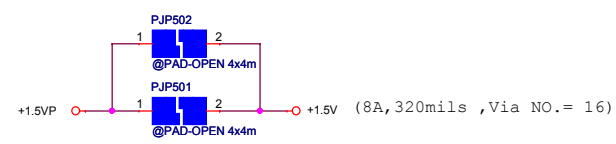
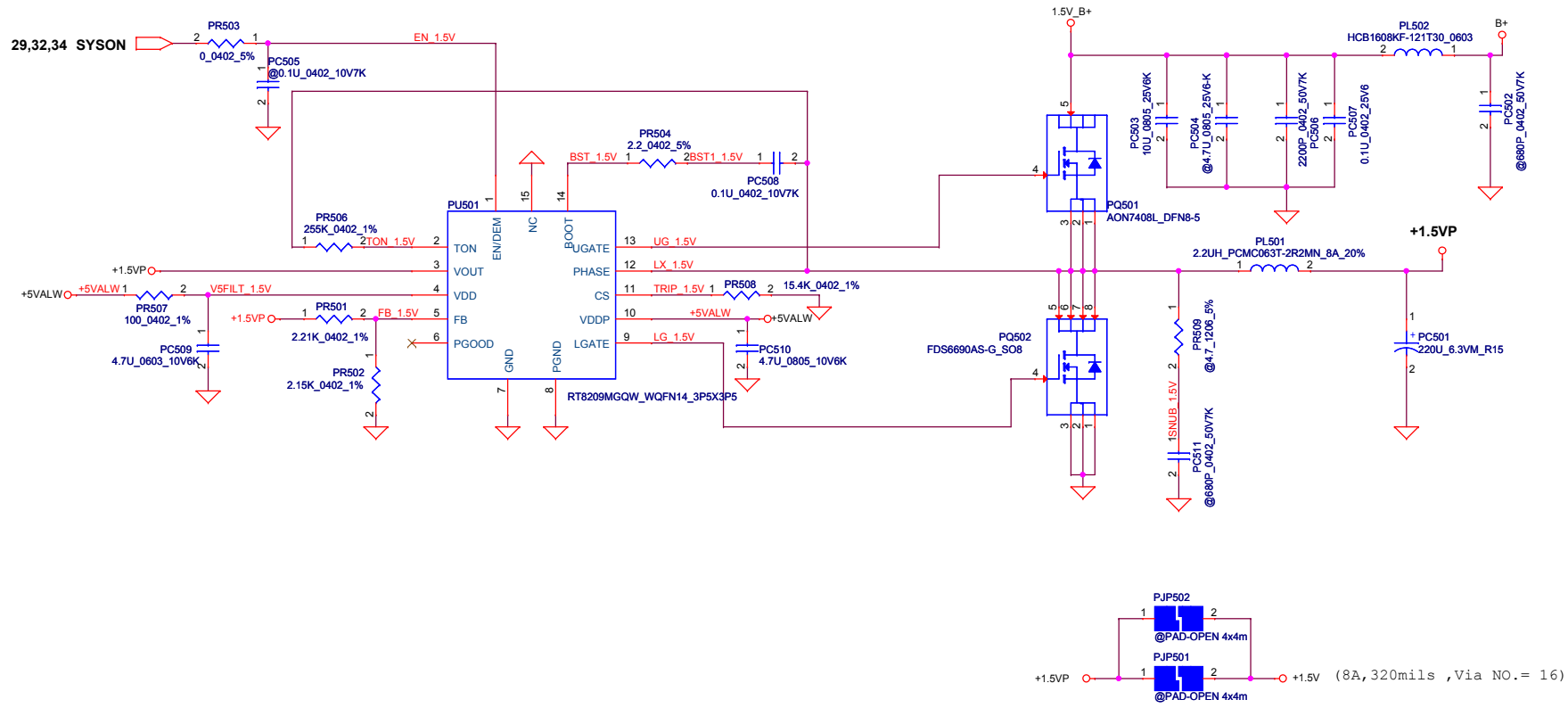
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	3.3VALWP/5VALWP	
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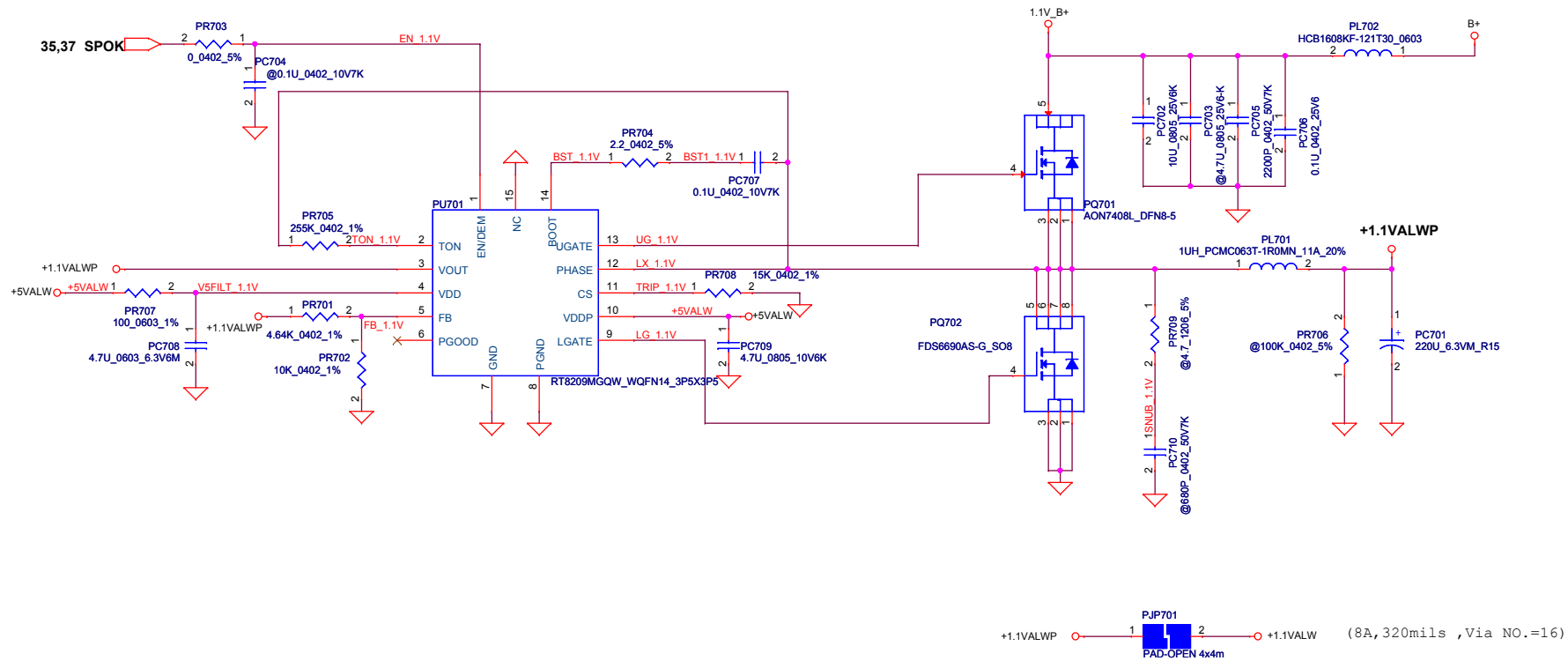
$V_o = 1.8V$ $V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR401/PR402) = 0.6 * (1 + 20K/10K) = 1.8V$

27,29,34,42 SUSP#

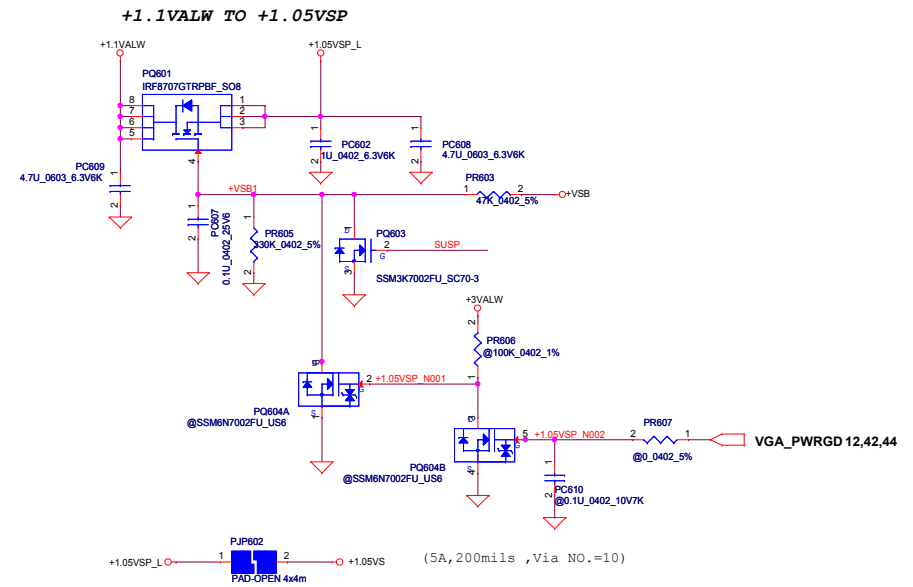
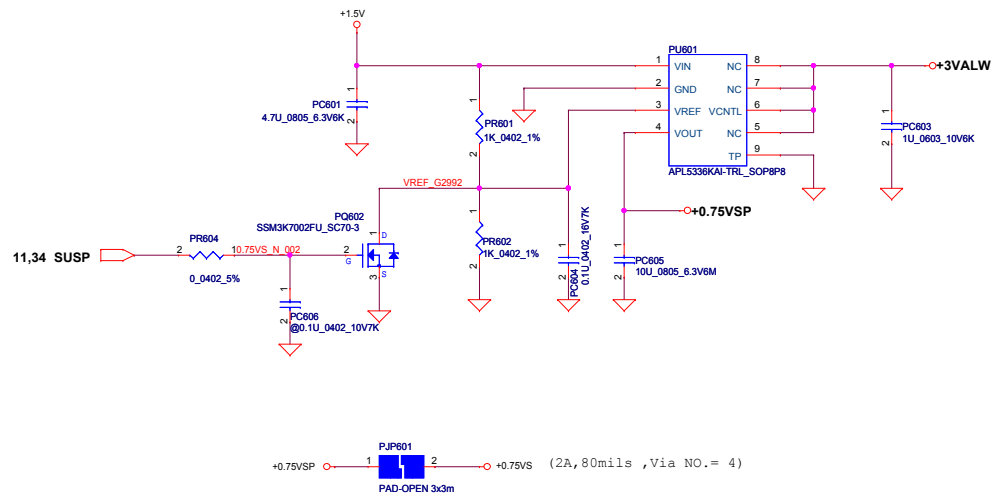
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title
				+1.8VSP
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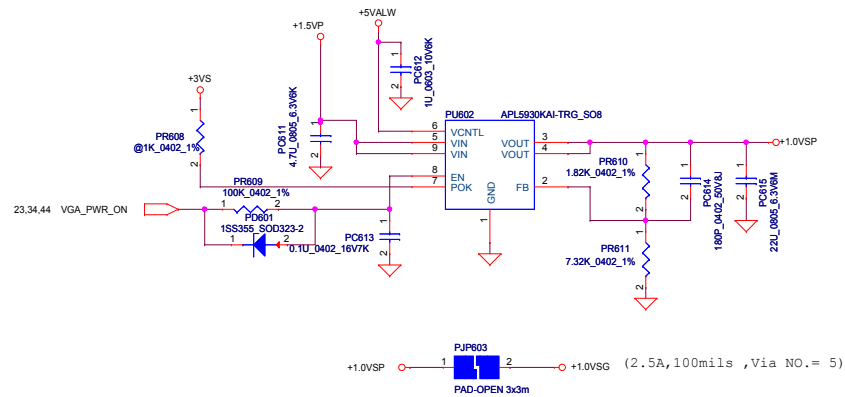
Security Classification		Compal Secret Data		Compal Electronics, Inc. +1.5VP	
Issued Date	2007/05/29	Deciphered Date	2008/05/29		
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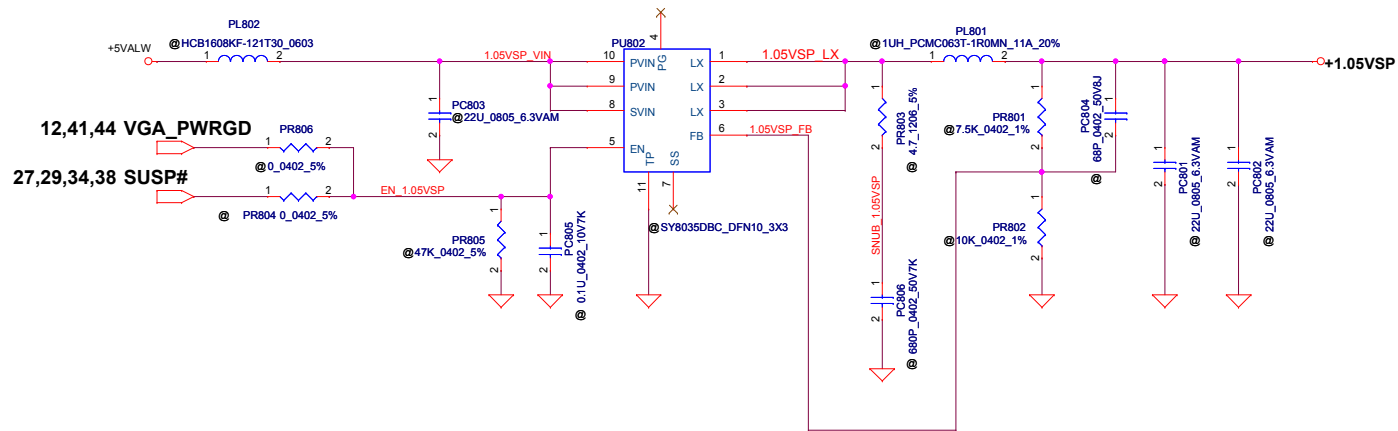
Security Classification	Compal Secret Data			Compal Electronics, Inc. PWR+1.1VALWP	
Issued Date	2009/12/01	Deciphered Date	2010/12/31		
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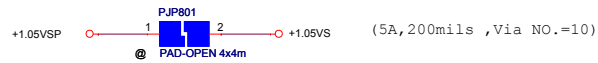
Need to confirm with HW power sequence.



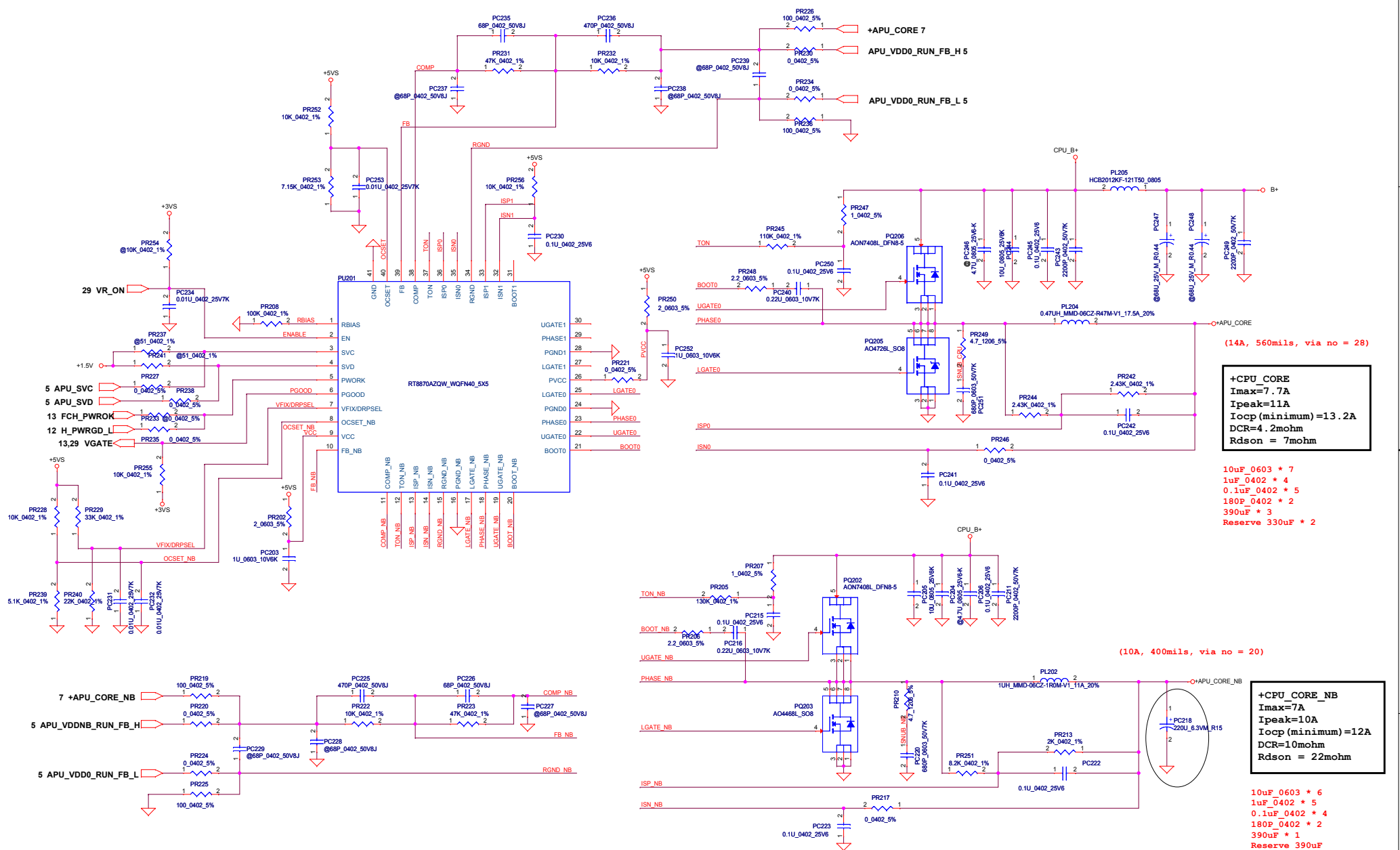
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Issued Date	2006/11/23	Deciphered Date	2007/11/23	Title
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12,41,44 VGA_PWRGD
27,29,34,38 SUSP#



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				+1.8VSP
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(14A, 560mils, via no = 28)

+CPU_CORE
 I_{max}=7.7A
 I_{peak}=11A
 I_{ocp}(minimum)=13.2A
 DCR=4.2mohm
 R_{dson} = 7mohm

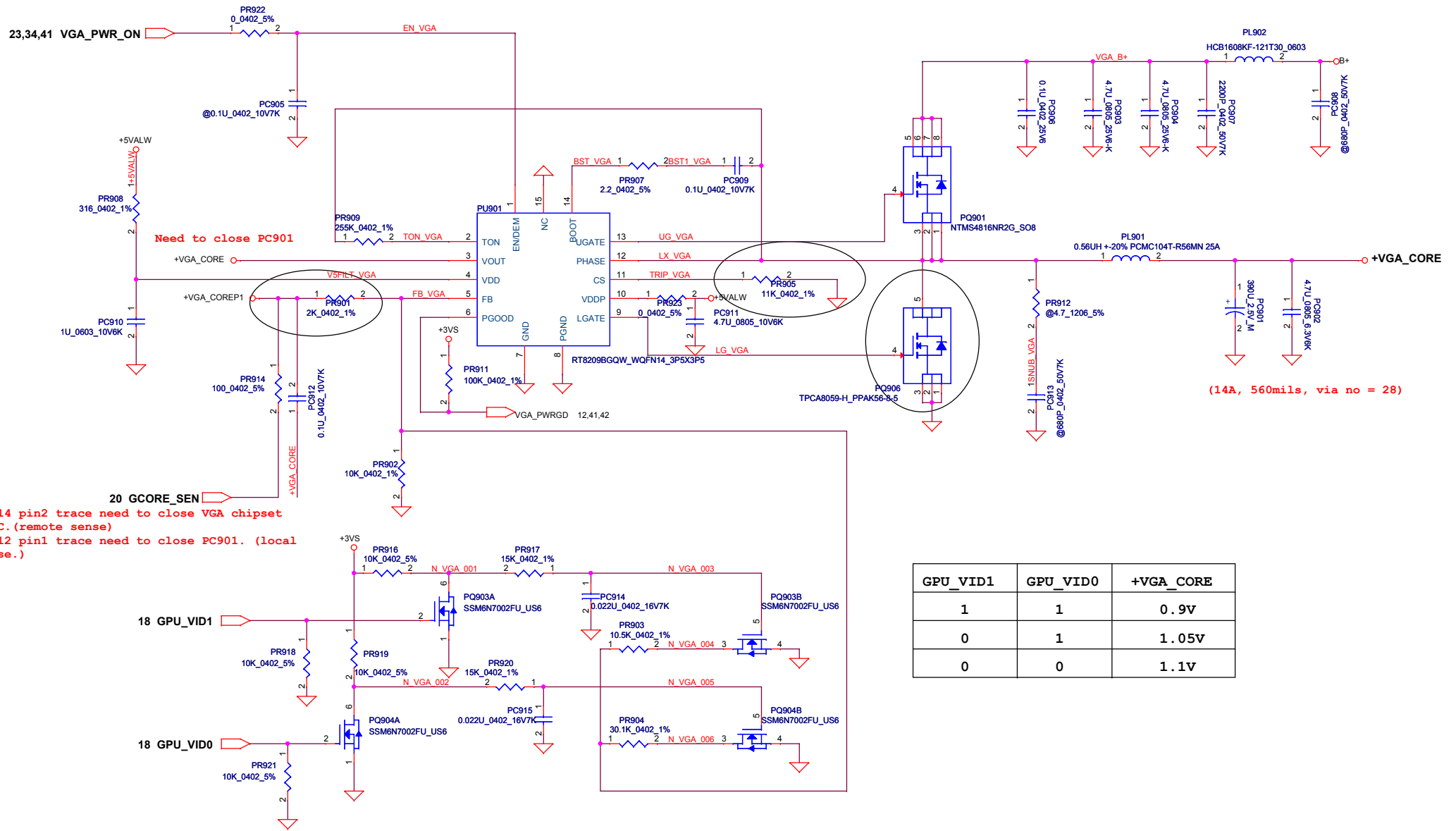
10uF 0603 * 7
 1uF 0402 * 4
 0.1uF 0402 * 5
 180P 0402 * 2
 390uF * 3
 Reserve 330uF * 2

(10A, 400mils, via no = 20)

+CPU_CORE_NB
 I_{max}=7A
 I_{peak}=10A
 I_{ocp}(minimum)=12A
 DCR=10mohm
 R_{dson} = 22mohm

10uF 0603 * 6
 1uF 0402 * 5
 0.1uF 0402 * 4
 180P 0402 * 2
 390uF * 1
 Reserve 390uF

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				PWR-CPU CORE
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

Security Classification	Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Compal Electronics, Inc.
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Size	Document Number	Date		Rev
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		DFB request	0.11	PG#10	change JLVDS1 connector to 40 pin and add JCM1 6pin	12/17	ER
2		EC remove ext crystal	0.11	PG#29	Add R1787 and C1677	12/17	ER
3		DFB request for soldering	0.11	PG#30 PG#33	Change JTP1 and JBTN1 footprint	12/17	ER
4		JUSB2 no function	0.11	PG#31	Update JUSB2 symbol	12/17	ER
5		LID issue	0.11	PG#13	R930 change to pop	12/17	ER
6		LID issue	0.11	PG#29	LID_SW# added a pull up 10Kohm. (R35)	12/17	ER
7		Update Broad ID	0.11	PG#29	Change R1606 to 154Kohm	12/17	ER
8		for BIOS crisis	0.12	PG#14	Add U11	12/17	ER
9		DDR3 SPD	0.12	PG#8	Reserve R152 , R155	12/17	ER
10		For discharge spec	0.13	PG#24	Add R1788 and Q113 discharge schematic	12/17	ER
11		For EMI test	0.2	PG#11	Remove Level Shifter schematic	12/17	ER
12		BIOS change to share ROM	0.2	PG#16 PG#29	Pop R594 and R602 , unpop R601 and R550 change U48 meterial	12/17	ER
13		Fix S3 resume black screen	0.21	PG#6	Add R1790 , R1791 68ohm pull down	02/18	PR
14		DFX request	0.21	PG#11	Update JDIMM2 footprint	02/18	PR
15		Fix S3 resume too long	0.21	PG#18	Add R1795 1M ohm	02/18	PR
16		Fix assembly issue	0.21	PG#29 PG#25	Update JKB1 and JAU1 footprint for ME connector	02/18	PR
17		EMI request	0.22	PG#11	pop L11~L14	02/22	PR
18							
19							
20							
21							
22							
23							
24							
25							
26							
27							

Security Classification		Compal Secret Data		Title	
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POWER SEQUENCE

