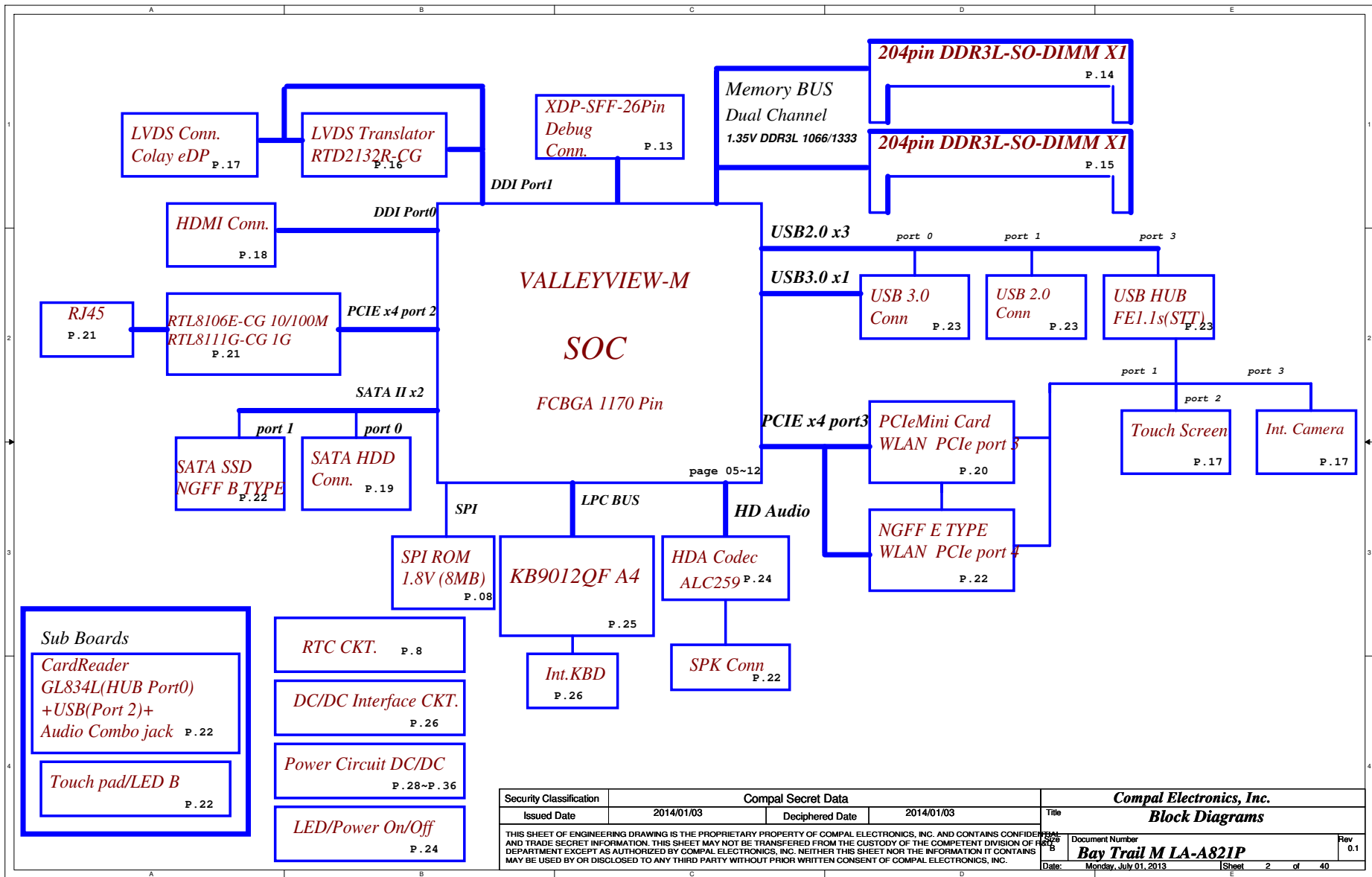


Intel BayTrail-M Platform

Date : 2013/05/22
Version 0.1

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			<small>Date:</small> Monday, July 01, 2013	<small>Sheet</small> 1 of 40



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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
--------	---------

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
TPM	TPM@
Touch Screen	TS@
R short	RS@
Test Point	TEST@

BOM config

PCB P/N
EVT BOM config

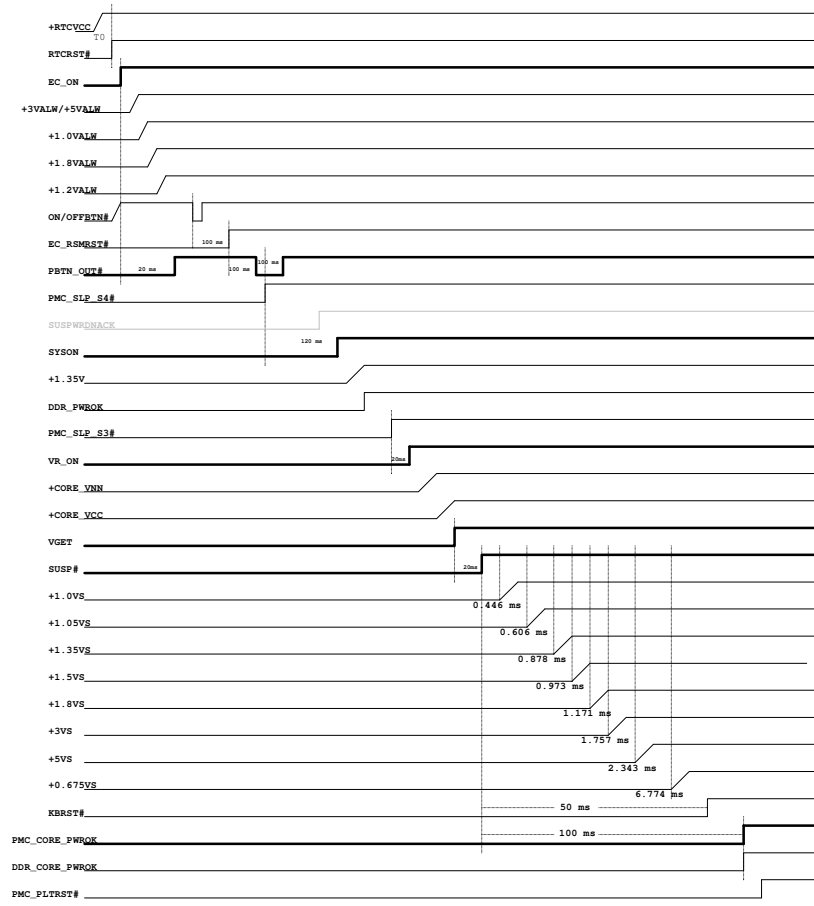
43 level BOM table

43 Level	Description	BOM Structure

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Power ON

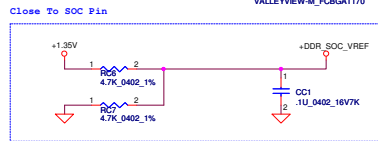
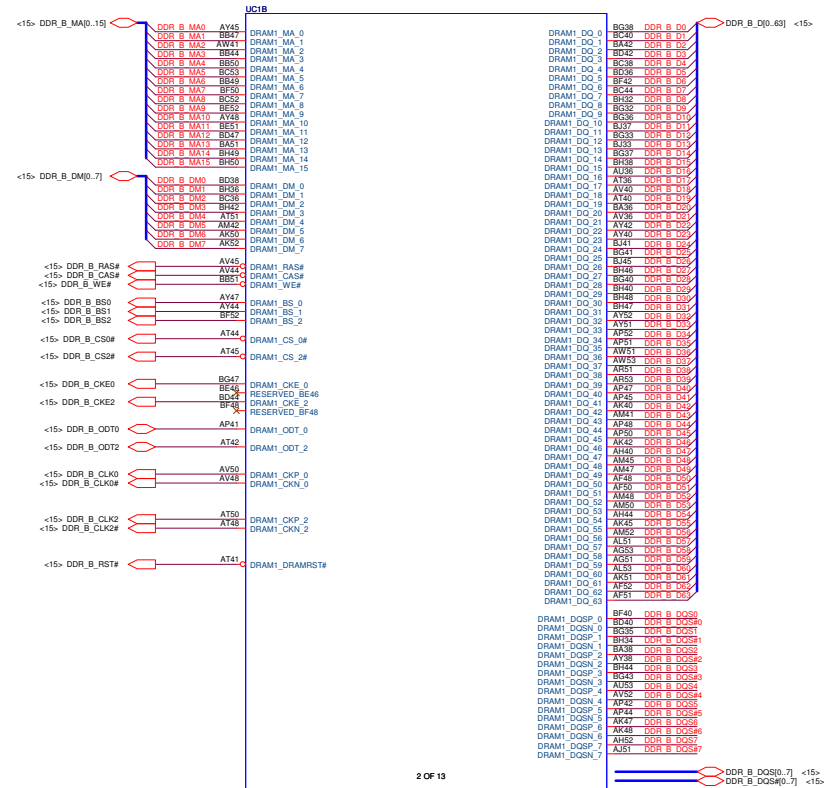
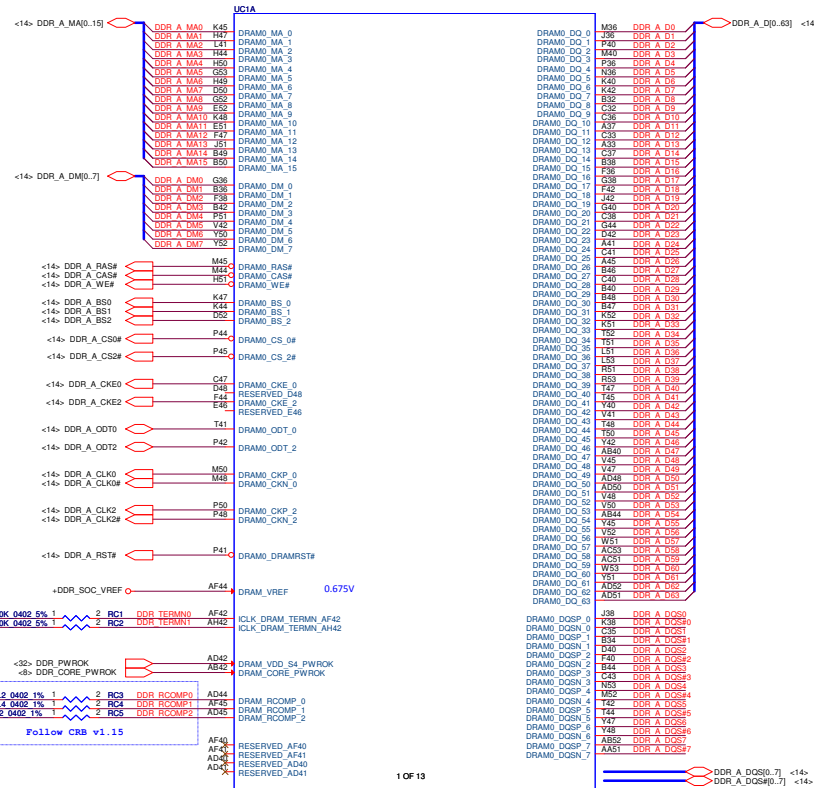


T0: +RTCVCC stable to RTCRST# high > 9ms
 T1: VR ramp up time from 10% to 90% voltage level < 2ms
 T2 :Rail to subsequent rail turn on delay < 2ms
 T3 :+VALWAS stable to EC_RSMRST# high > 10ms
 T4 :+VS rails stable to PMC_CORE_PWROK > TBD

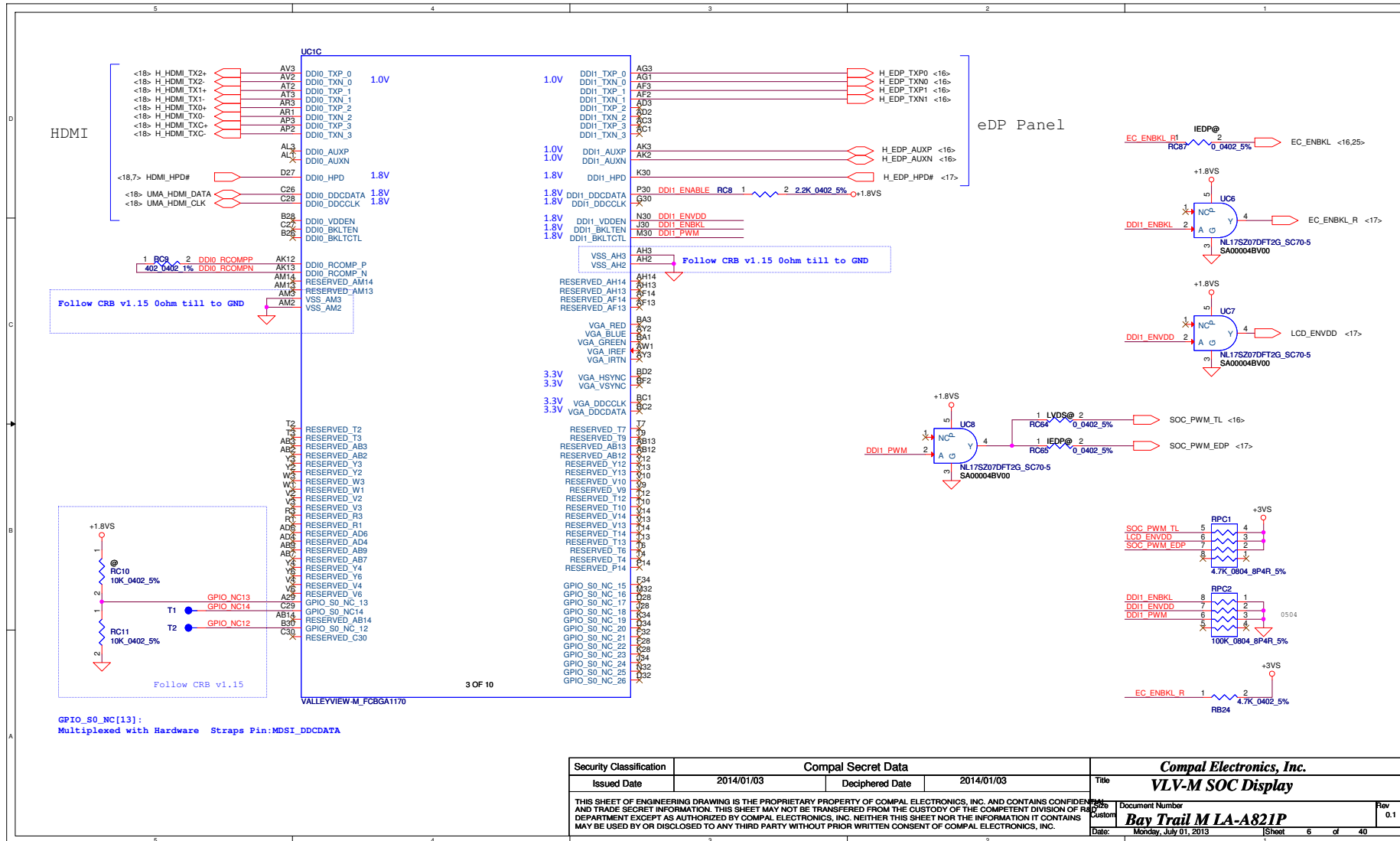
NOTE:
 1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

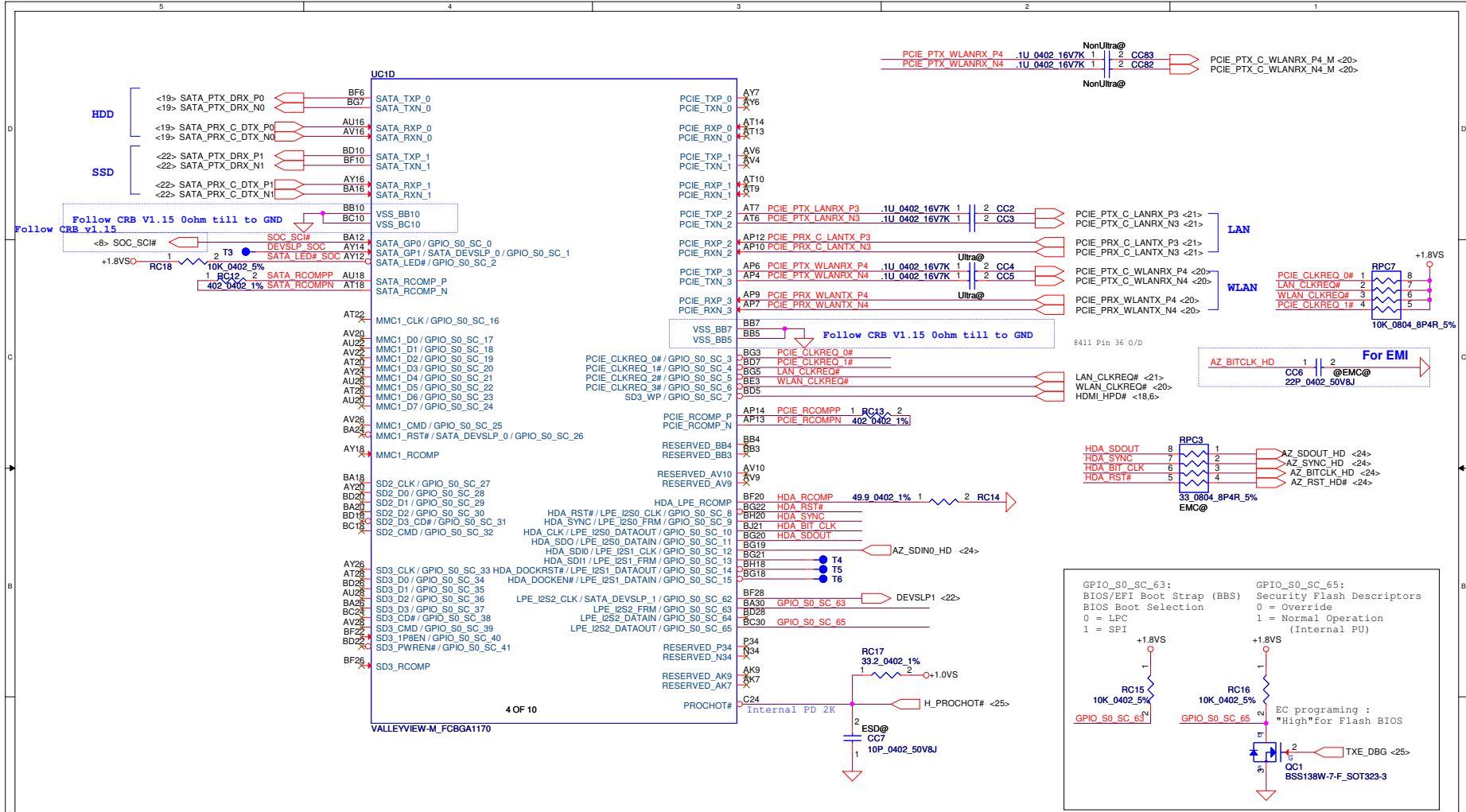
2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

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				Power Sequence	
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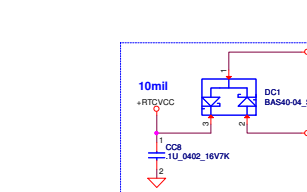
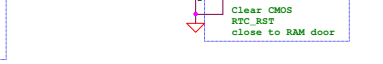
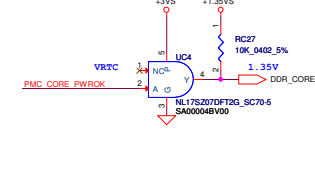
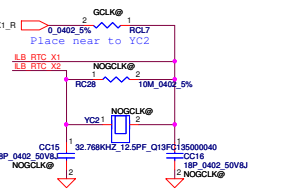
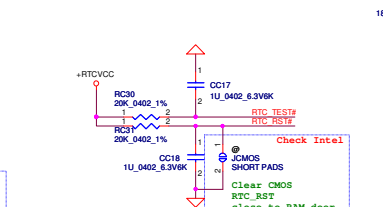
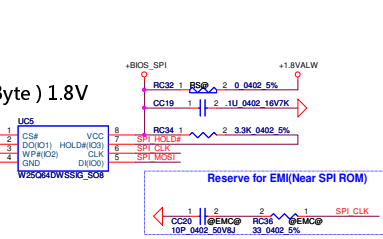
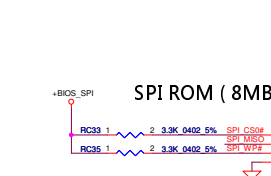
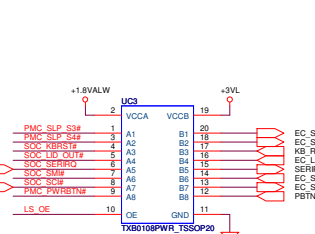
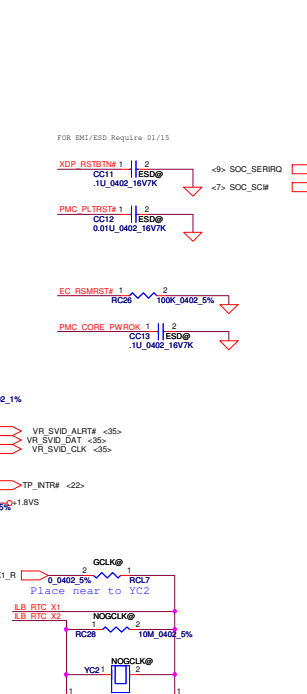
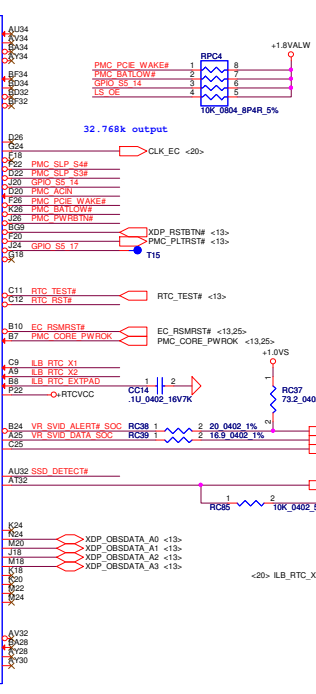
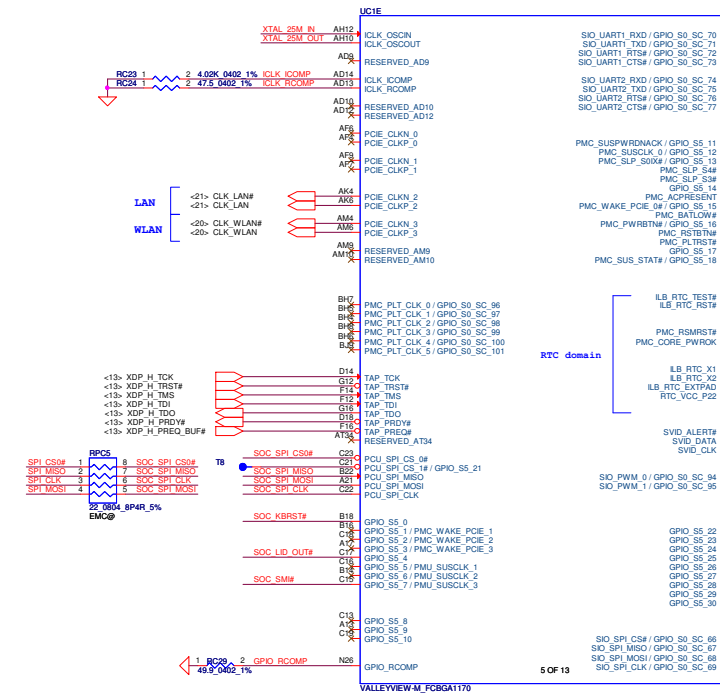
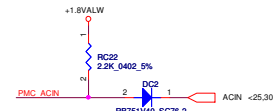
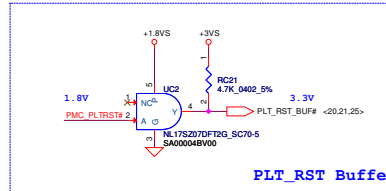
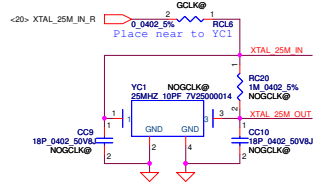
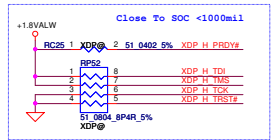


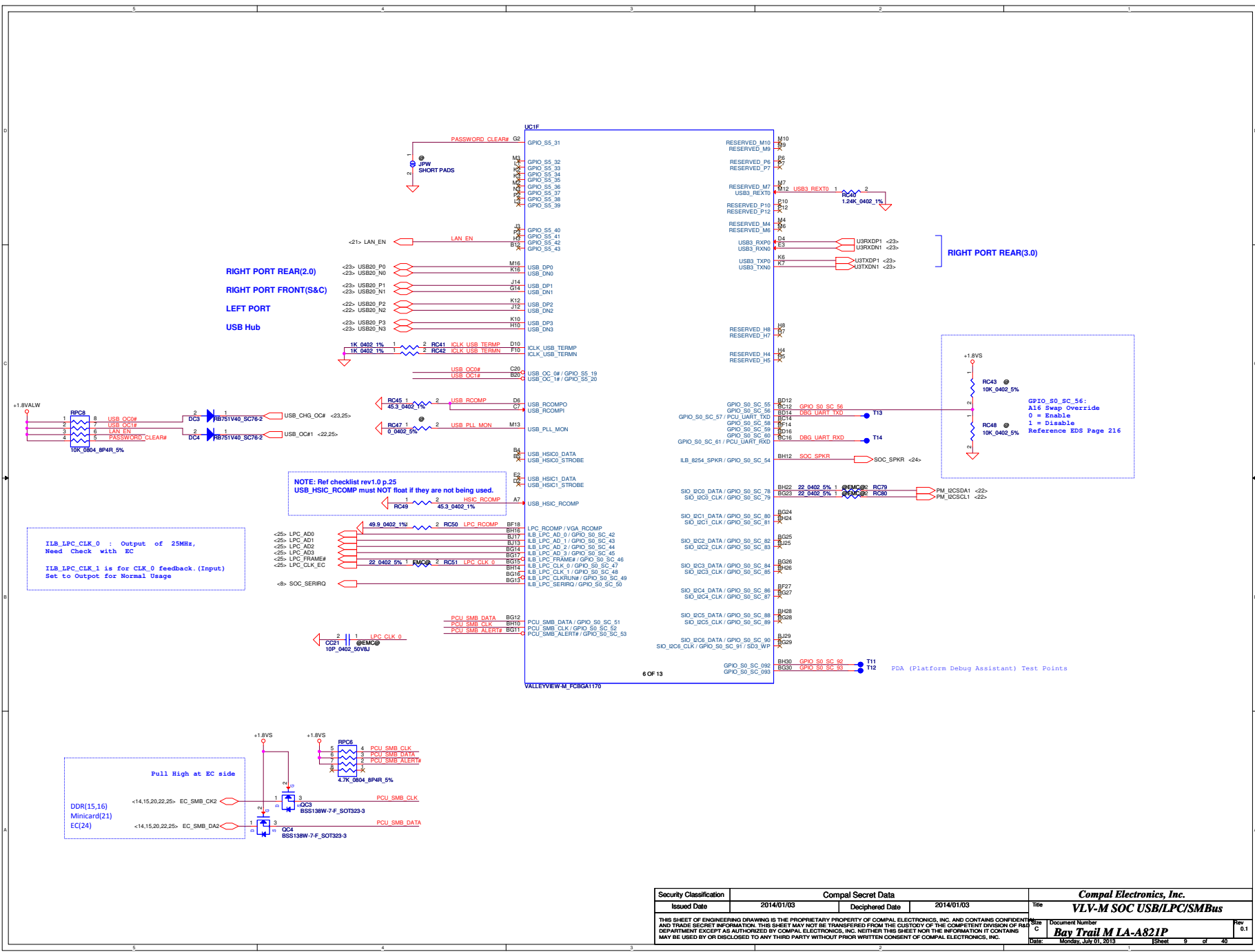
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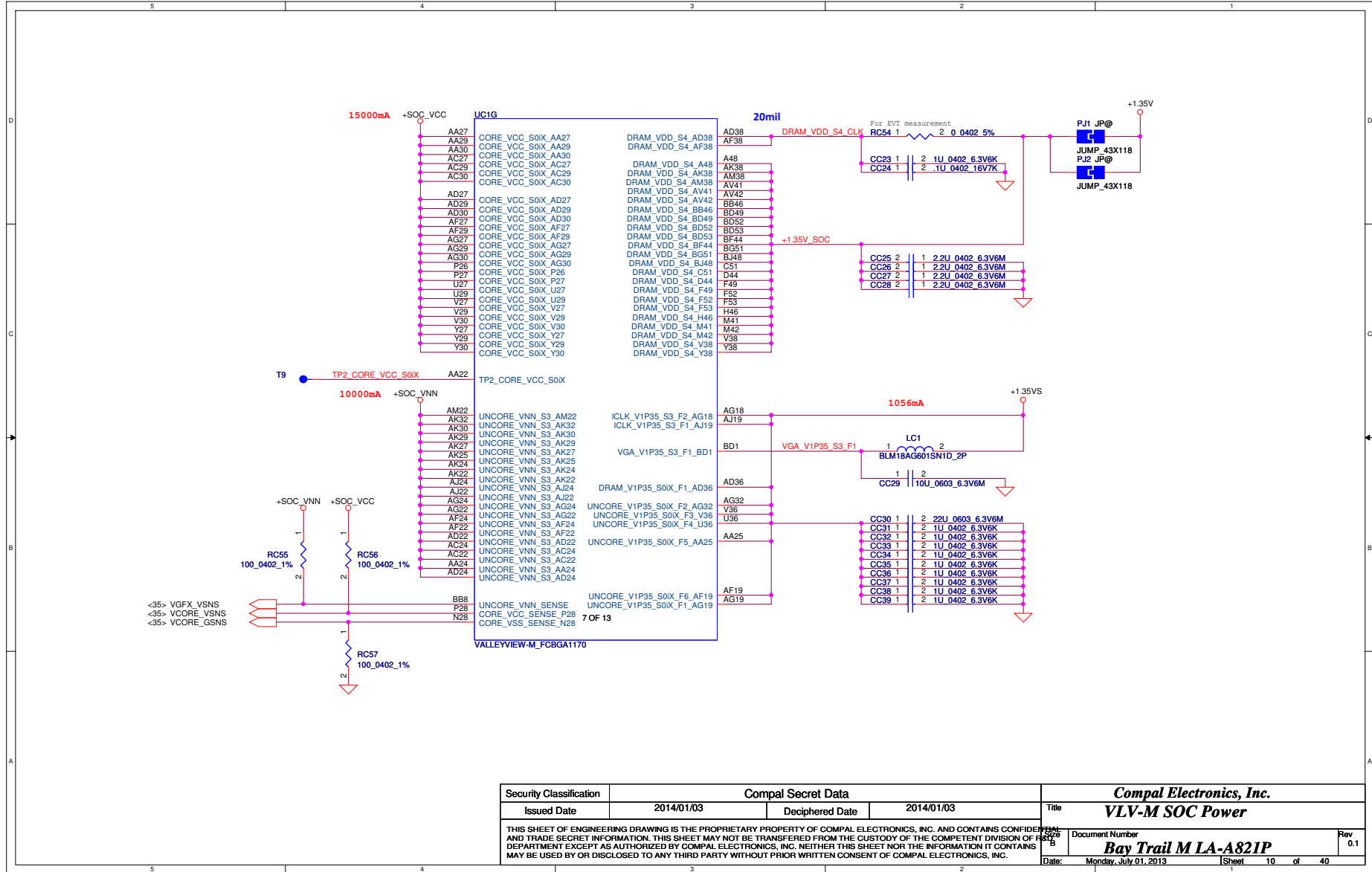


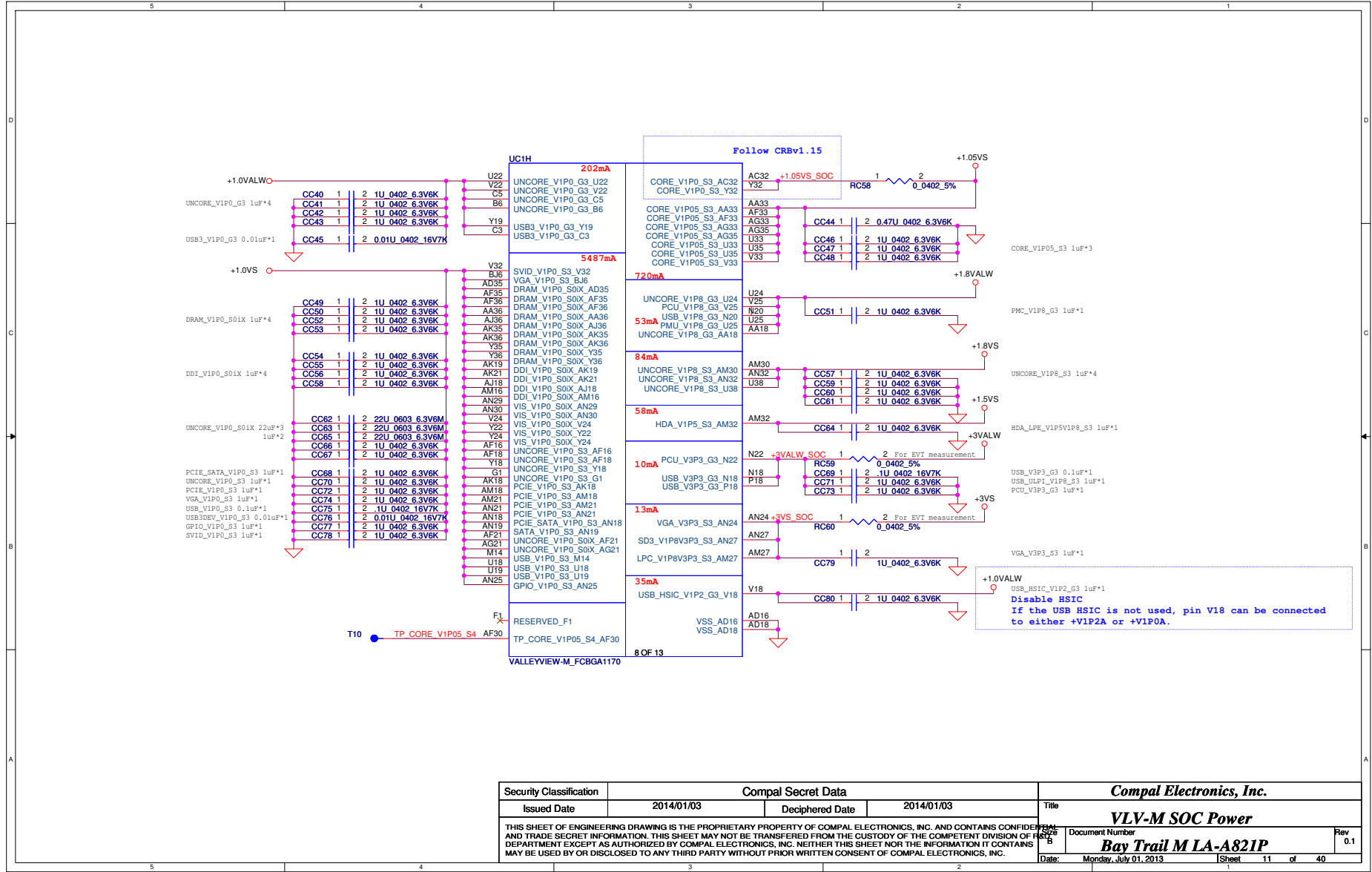
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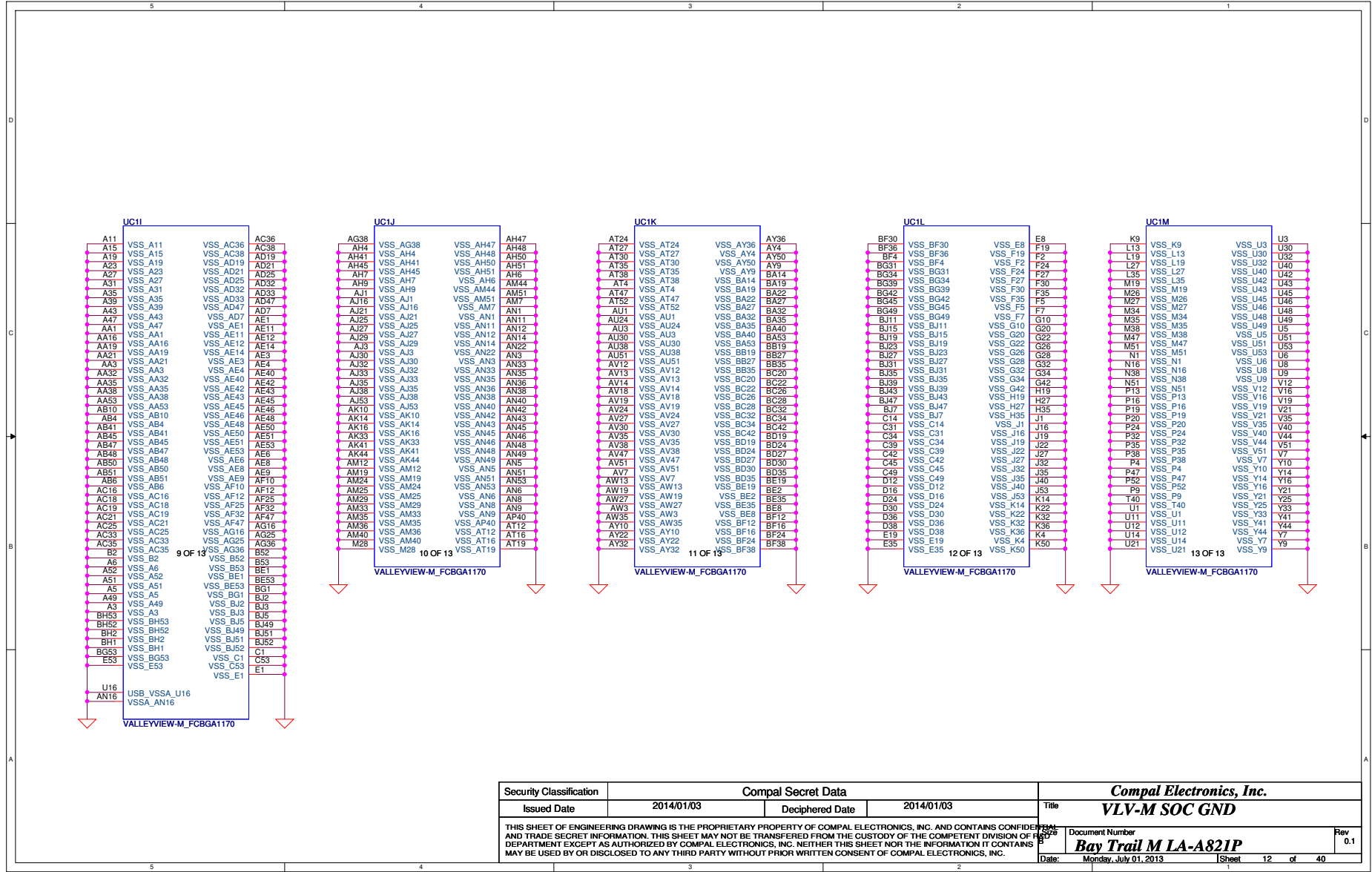


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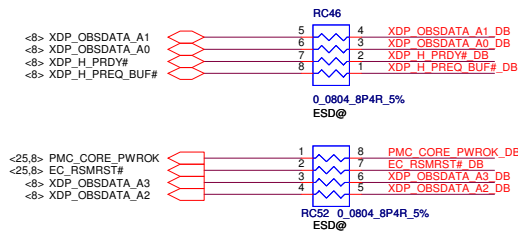
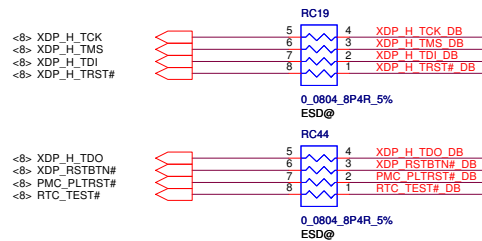
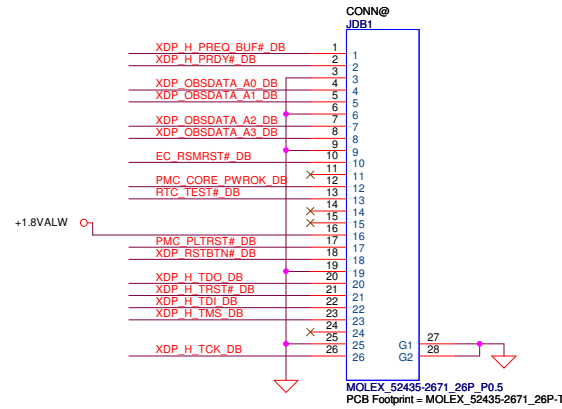
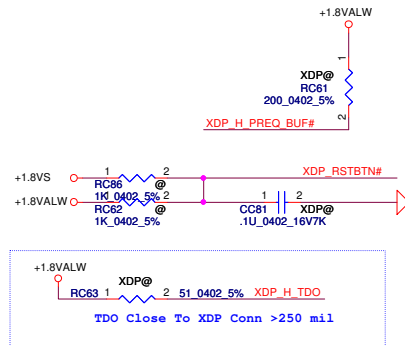
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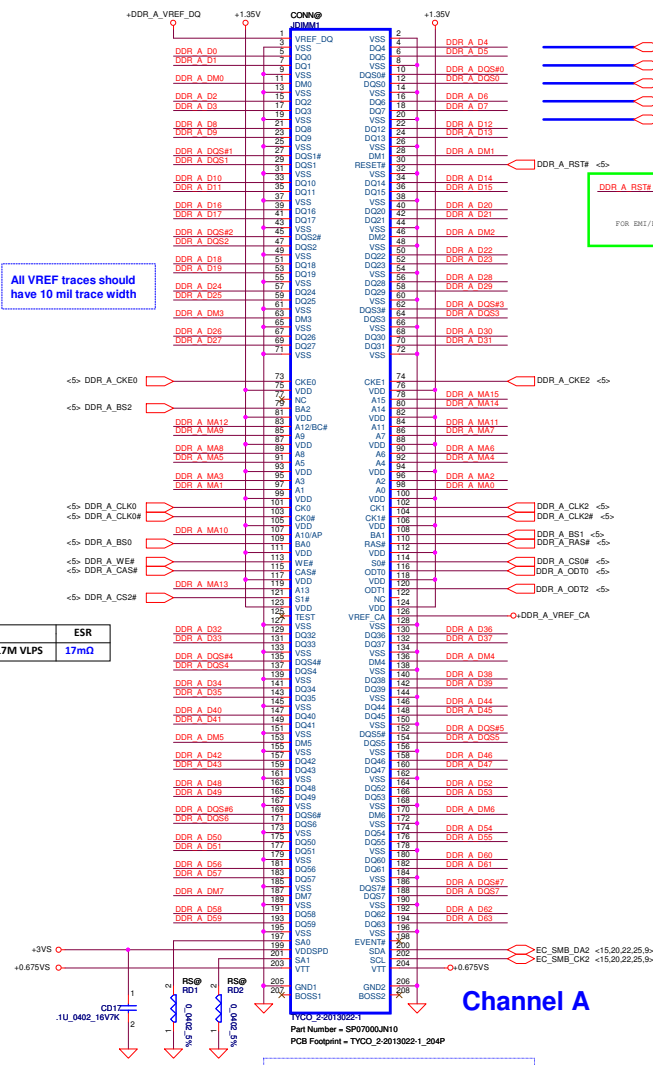
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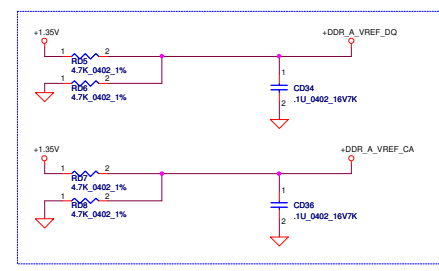
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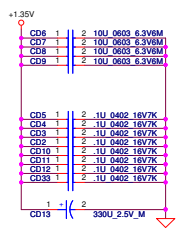
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Signal voltage level = 0.675 V
 PLACE TWO 4.7K RESISTORS CLOSE TO
 DIMM1 ON DIMM_VREF_CA / DIMM_VREF_DQ
 Decoupling caps are needed; one 0.1 µF placed close to VREF pins of each DDR3 SODIMM.

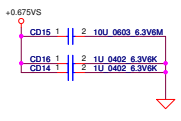


Layout Note:
Place near JDIMM1



All VREF traces should
have 10 mil trace width

Part Number	Description	ESR
SF00002Z00	S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLP5	17mΩ



Layout Note:
Place near JDIMM1.203,204

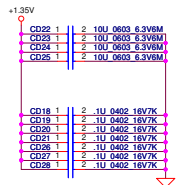
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DIMM_1 STD H:4mm

Channel A

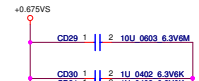
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				Document Number
				Bay Trail M LA-A821P
				Date: Monday, 3/24/2015 15:00:00

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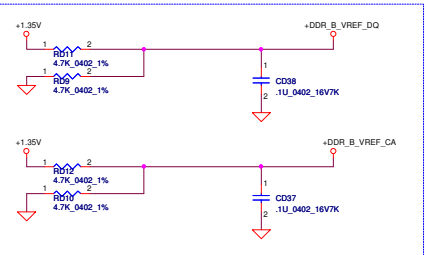
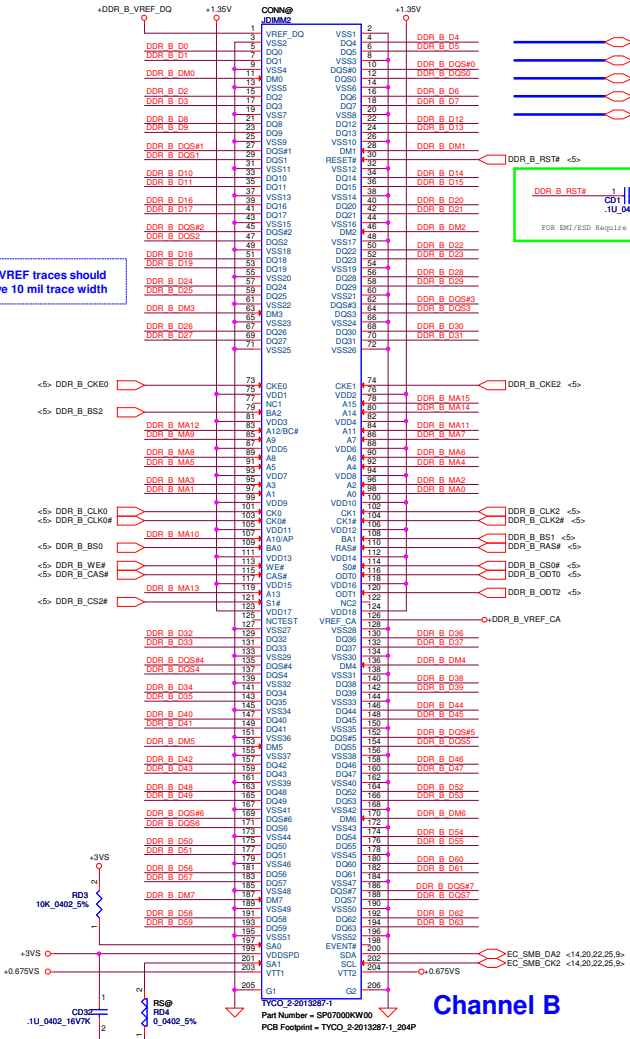
Layout Note:
Place near JDIMM2



All VREF traces should have 10 mil trace width



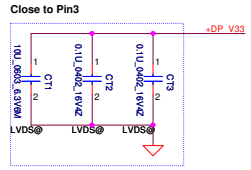
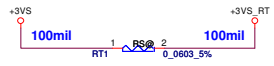
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Channel B

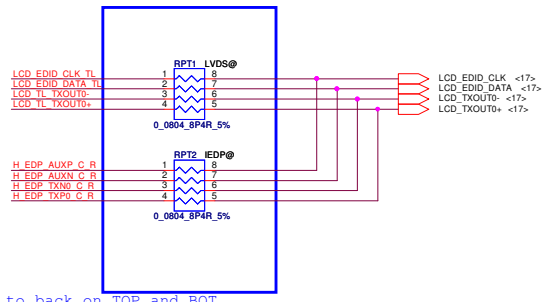
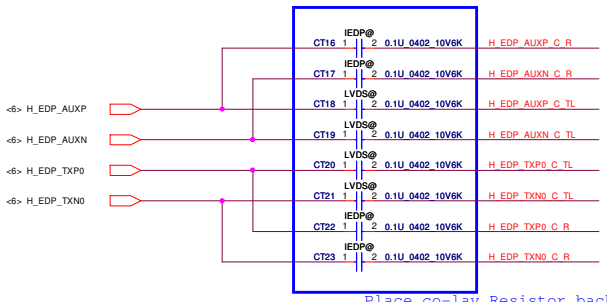
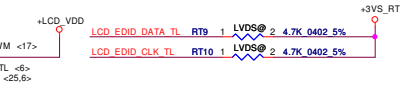
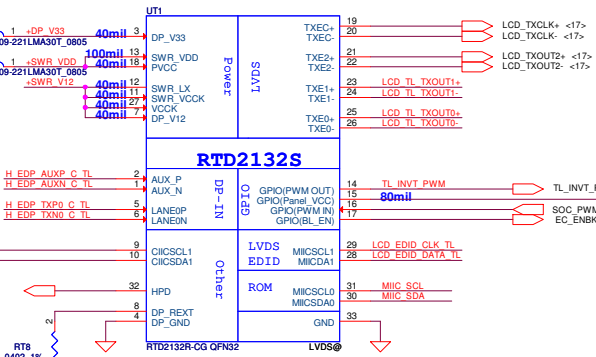
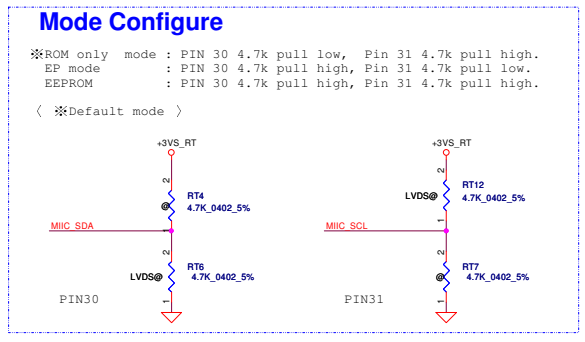
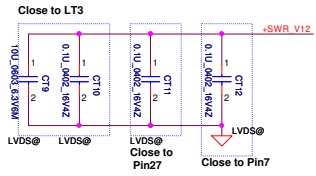
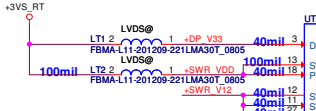
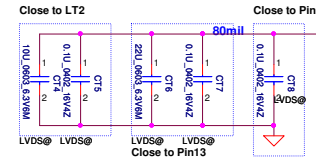
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Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/03	Deciphered Date	2014/01/03	Title
				DDR3L DIMMB
				Document Number
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				Monday, 3/24/2015 15:08
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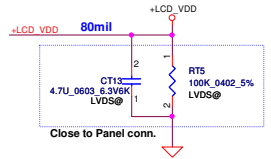


SWR / LDO Mode select

※LDO mode is adopted as default power regulator mode. Also can implement SWR mode by add inductor.



Place co-layer Resistor back to back on TOP and BOT



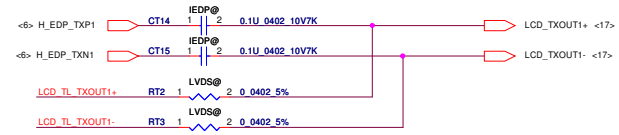
2132S	PIN15	TL_ENVDD
2132R	+LCD_VDD *	

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5-3.3V

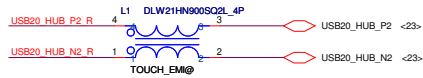
* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132R	
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

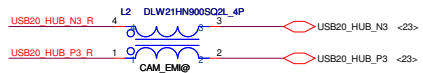


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Size	Document Number	Bay Trail M LA-A821P		Rev	0.1
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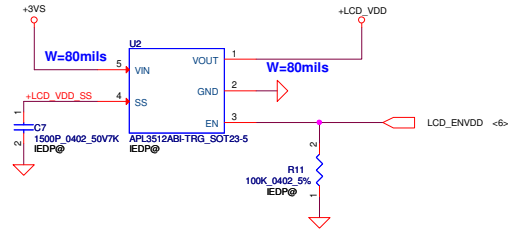
BTO : TOUCH_EMI@



EMI request - Close to JEDP connector

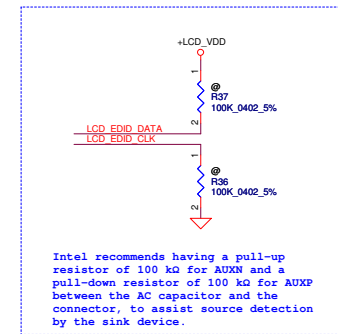
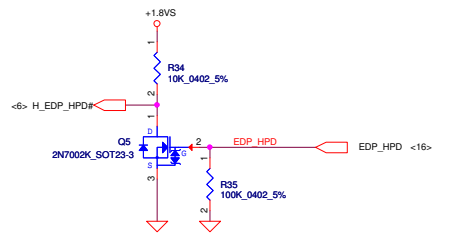
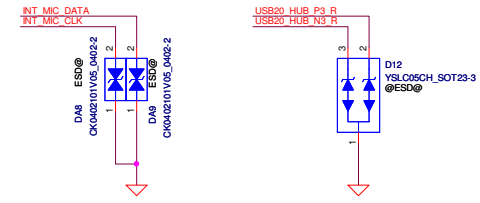
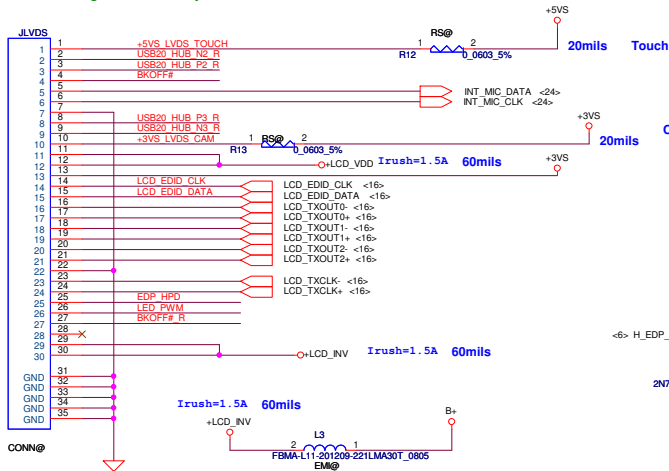


LCD POWER CIRCUIT (For EDP panel only)

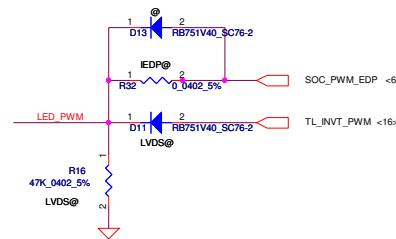
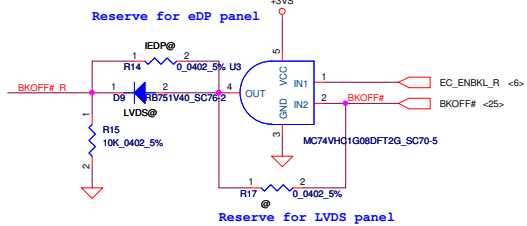


LVDS coloy eDP cable

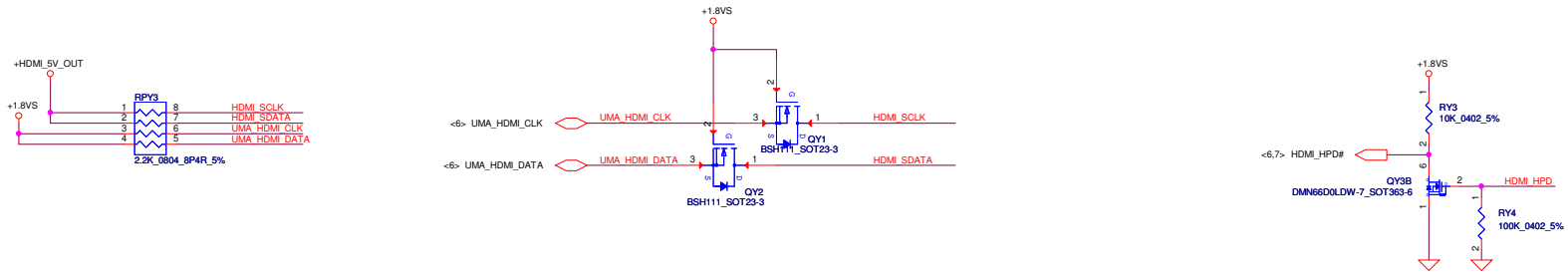
Pin define will be change after ME ready



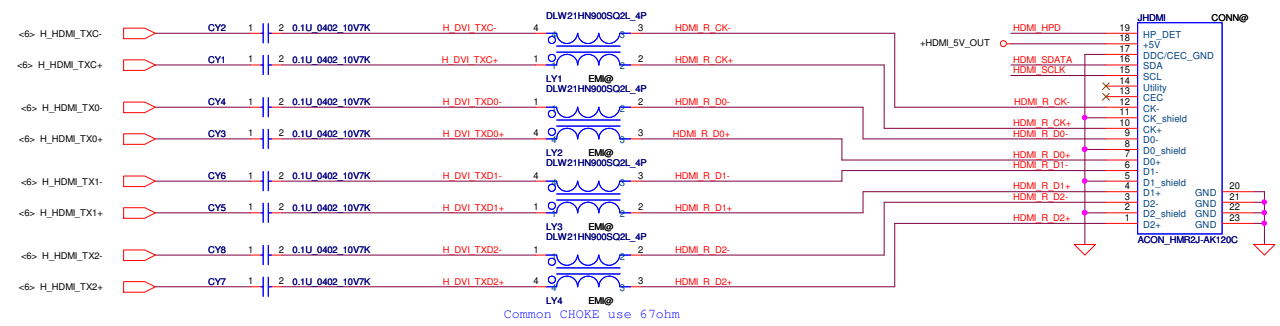
Intel recommends having a pull-up resistor of 100 kΩ for AUXN and a pull-down resistor of 100 kΩ for AUXP between the AC capacitor and the connector, to assist source detection by the sink device.



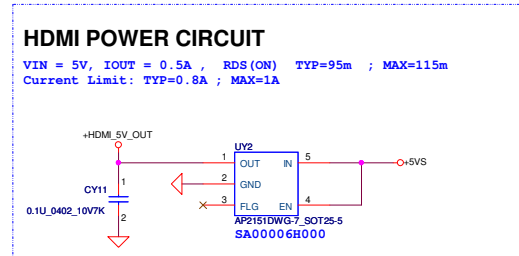
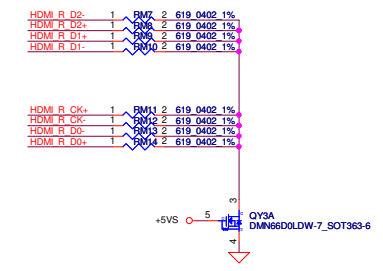
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HDMI Connector

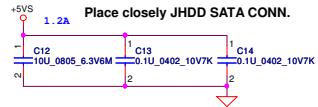
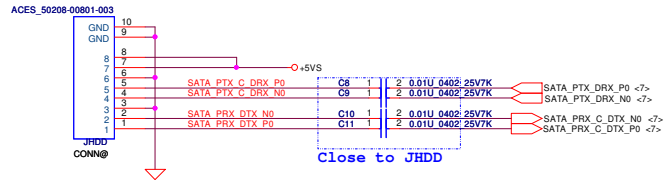


HDMI Royalty
 ZZZ1 HDM45@
 RO000003HM
 HDMI W/Logo + HDCP
 HDMI W/O Logo: RO000001HM
 HDMI W/Logo: RO000002HM
 HDMI W/Logo + HDCP: RO000003HM
 please manually load
 this virtual material to 45@ BOM

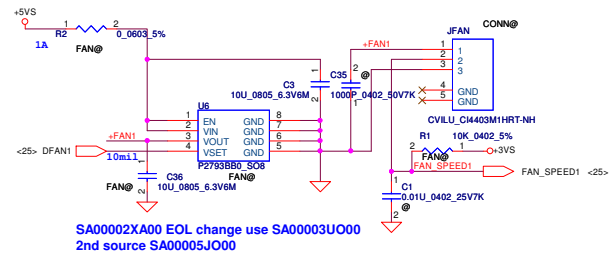


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SATA HDD Conn.

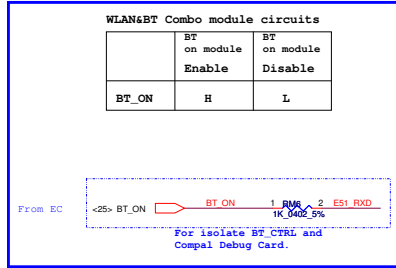
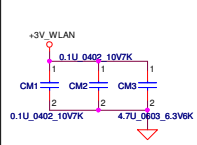


FAN Control Circuit

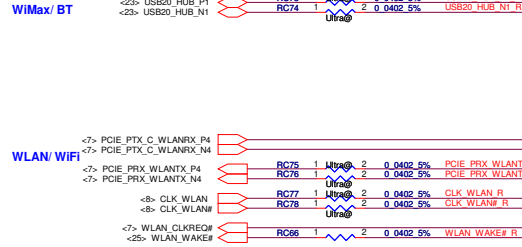


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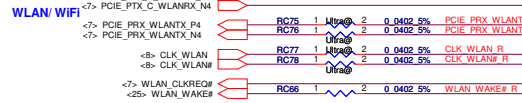
Slot 1 Half PCIe Mini Card-WLAN



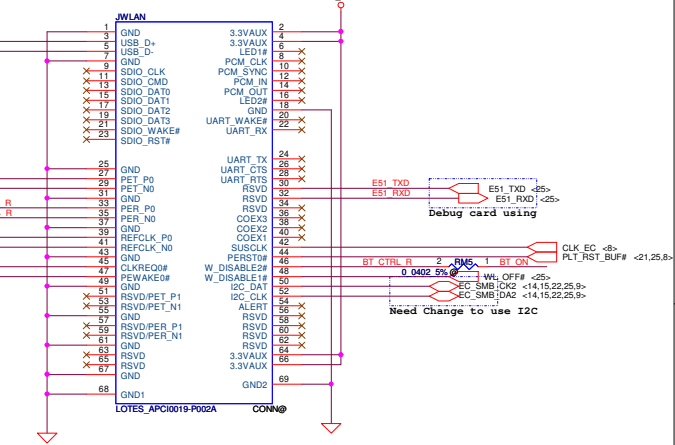
WiMax/ BT



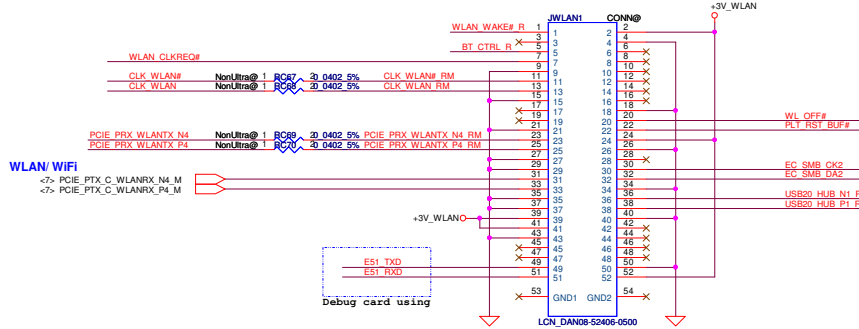
WLAN/ WIFI



NGFF E TYPE for Ultra



Mini PCIE type for Non-Ultra



WLAN/ WIFI



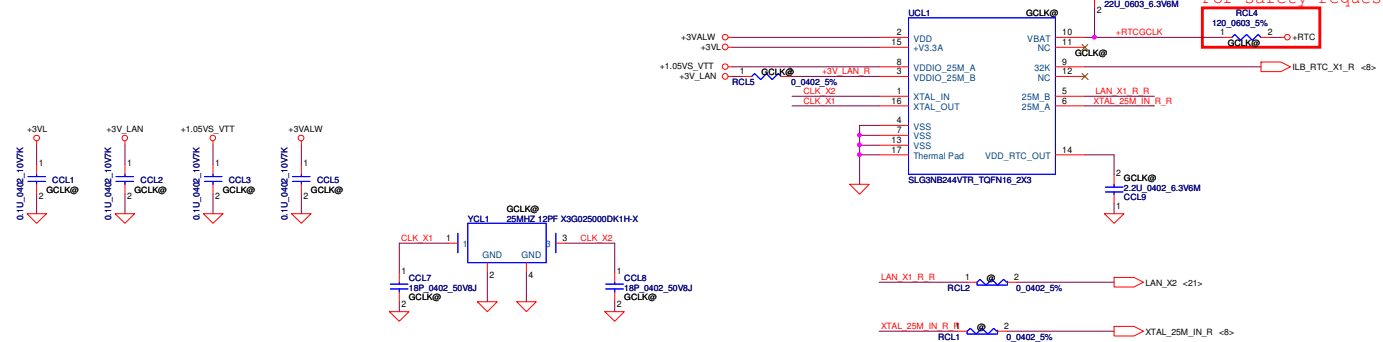
WLAN/ WIFI



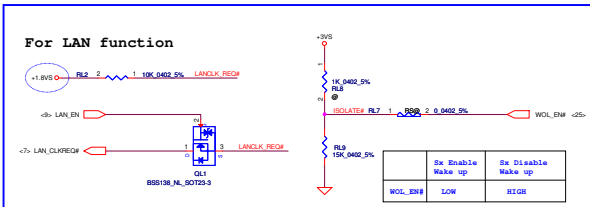
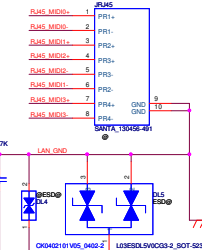
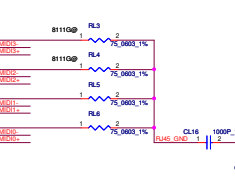
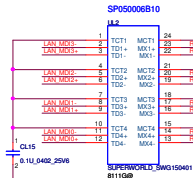
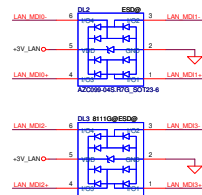
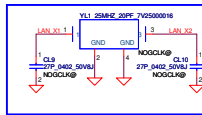
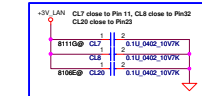
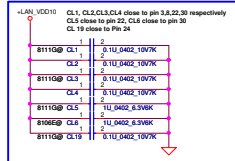
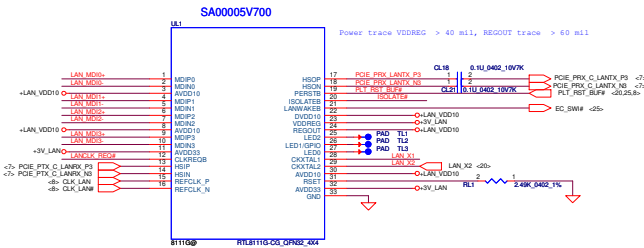
WiMax/ BT



Green Clock



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Compal Electronics, Inc.

+3V_LAN rising time (10%-90%) need > 1ms and <100ms.

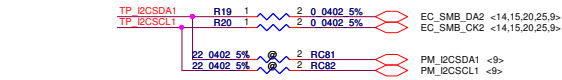
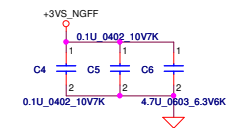
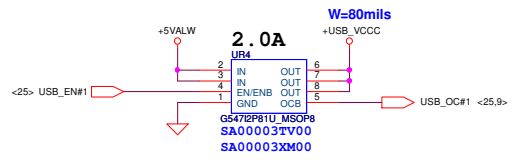
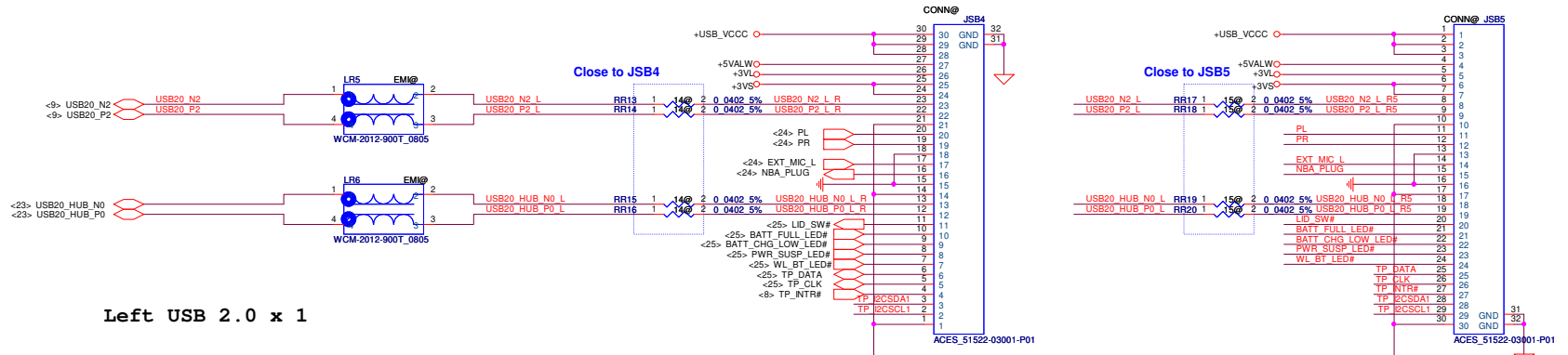
LAN	WOL	LAN_EN	ISOLATER
S0	Sx	S0	Sx
0	0	0	1
0	1	0	1
1	0	1	1
1	1	1	0*

* S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

For ESD, keep close to RJ45 Connector
Change back to connect to LANGND only
on 20130201

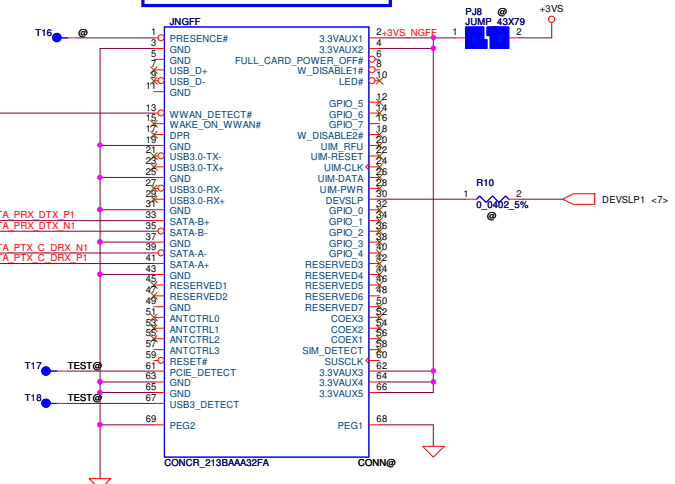


Small board Conn

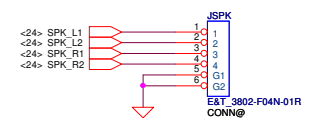


NGFF SSD B Type connector

P/N: SP071212280



SPK Conn.



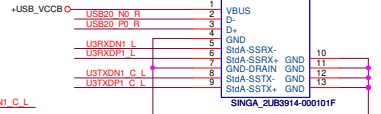
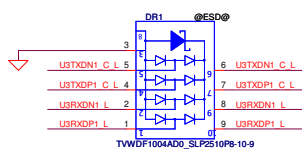
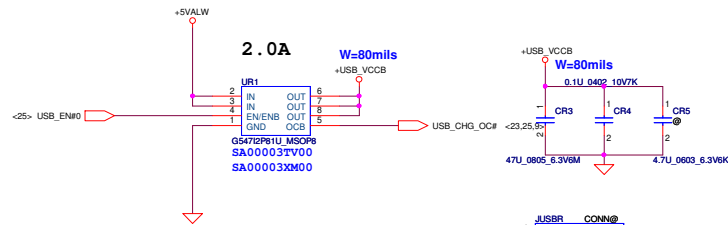
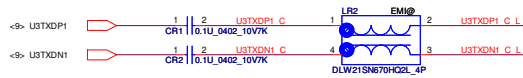
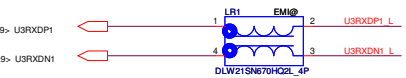
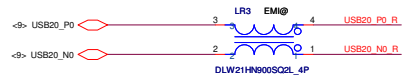
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USB Sleep & Charge

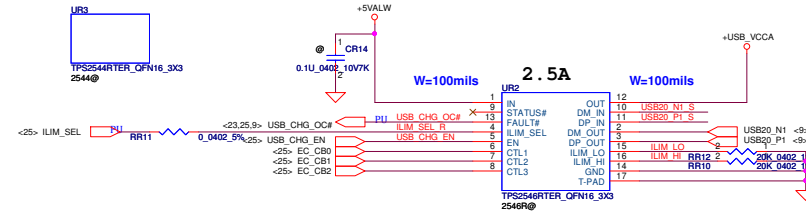
State table for TPS2546RTER

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto	Auto-detection charger mode for Apple device(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	0	1	1	Alternate	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

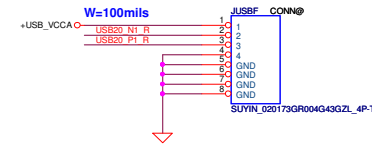
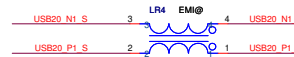
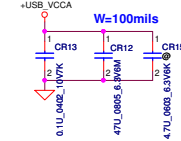
RIGHT REAR USB3.0 CONN.



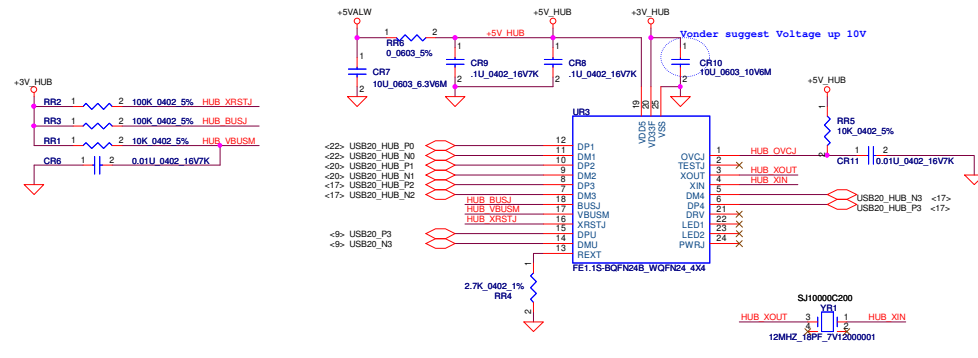
RIGHT FRONT USB 2.0 W/S&C



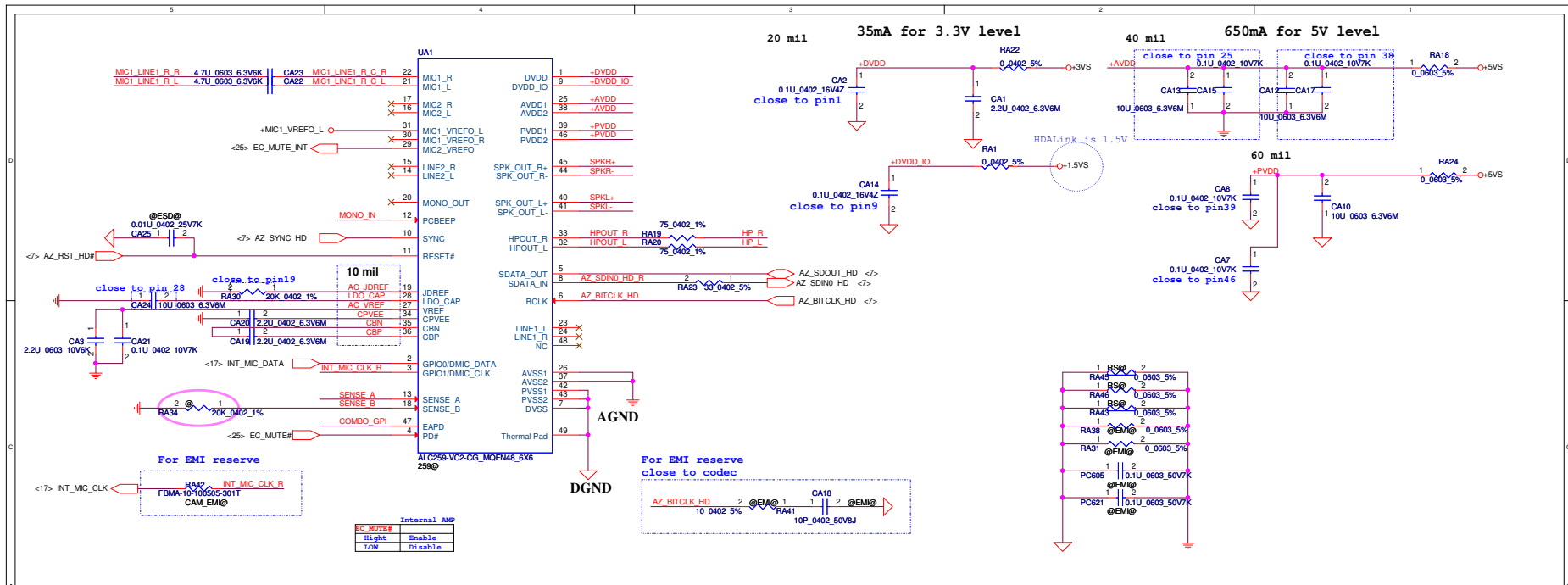
Close to UR2 IN/OUT



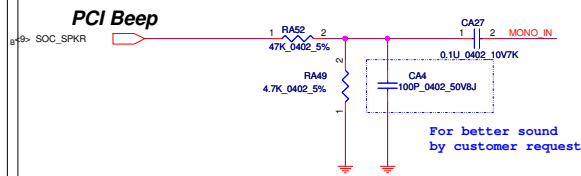
USB 2.0 HUB



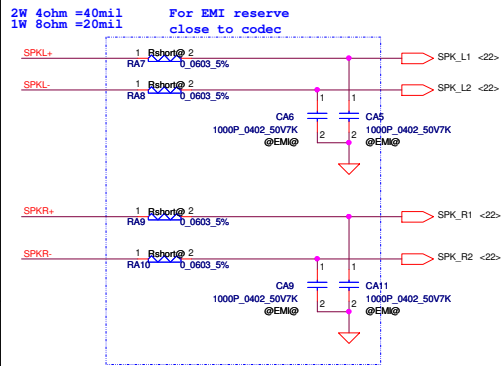
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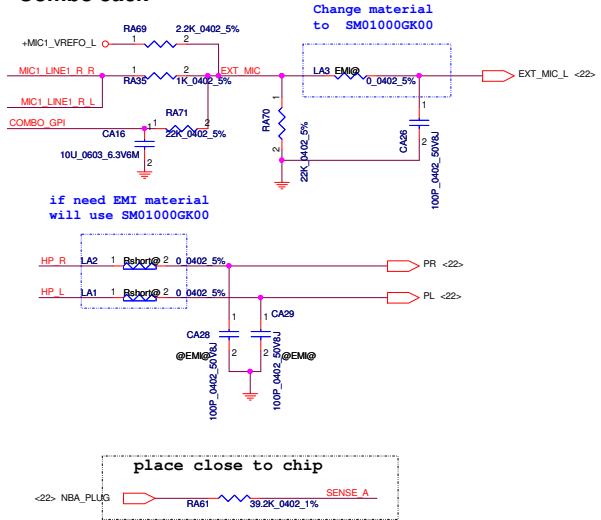
Beep sound



SPK

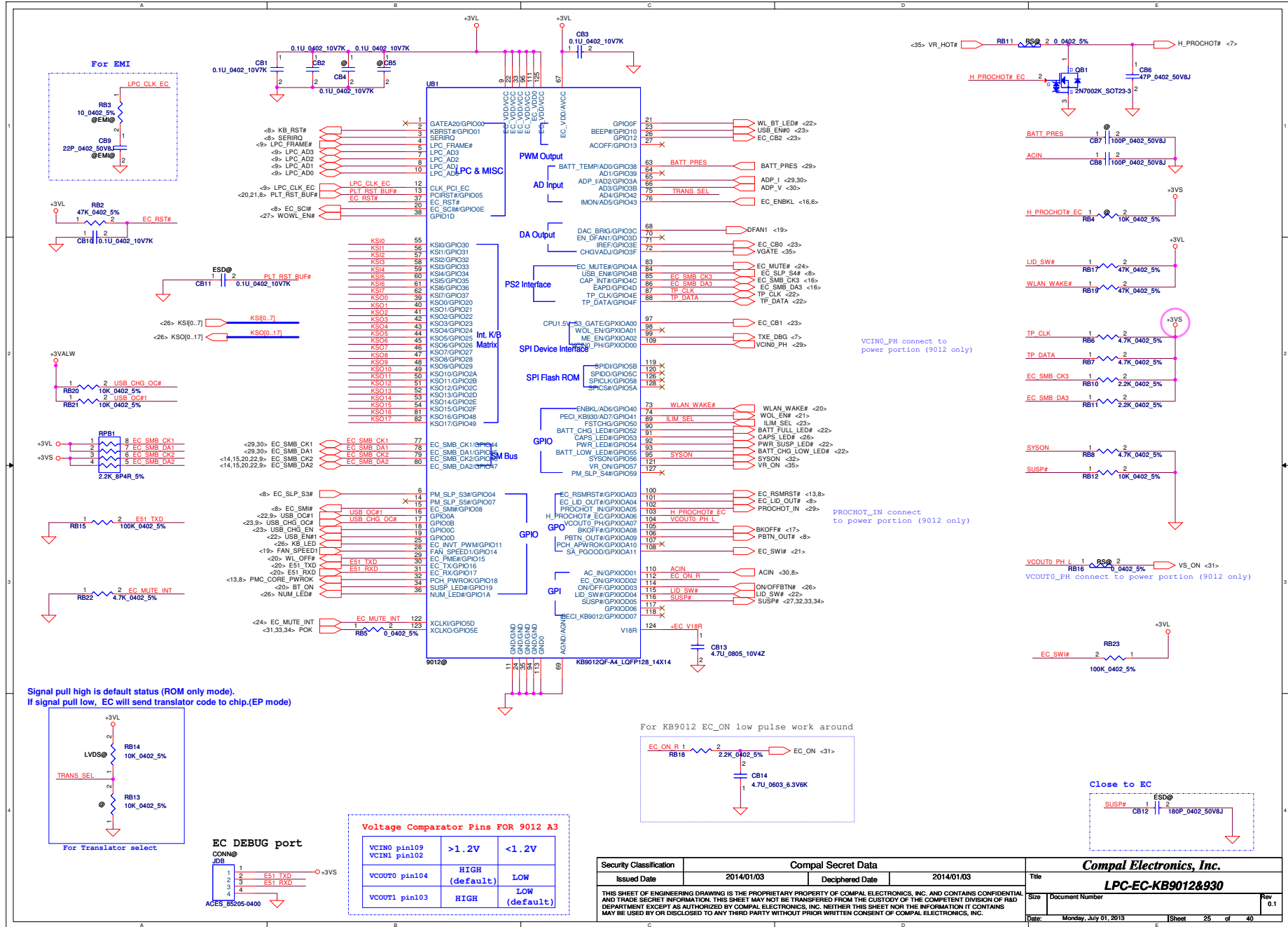


Combo Jack

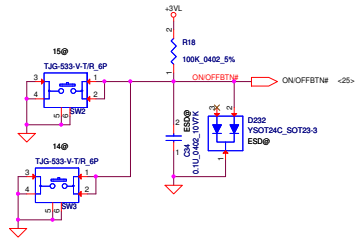


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

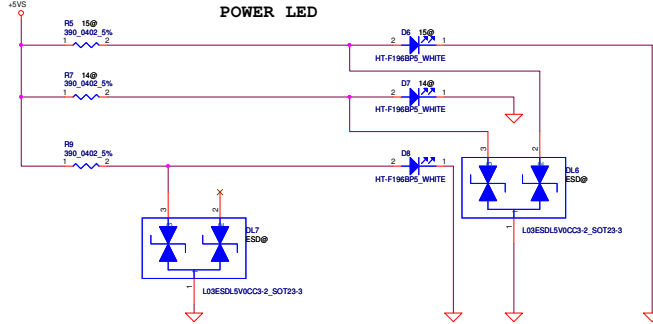
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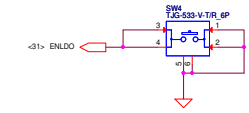
Power Button



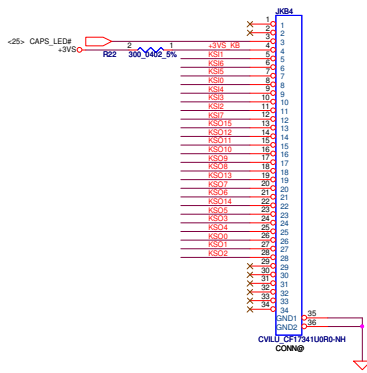
POWER LED



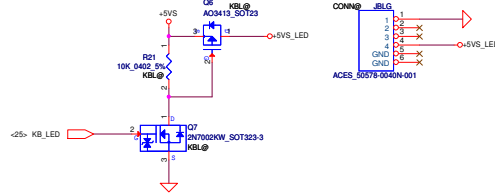
Battery Reset



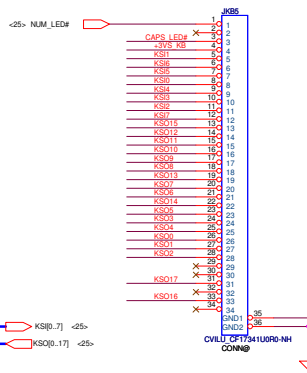
14 " KEYBOARD CONN.



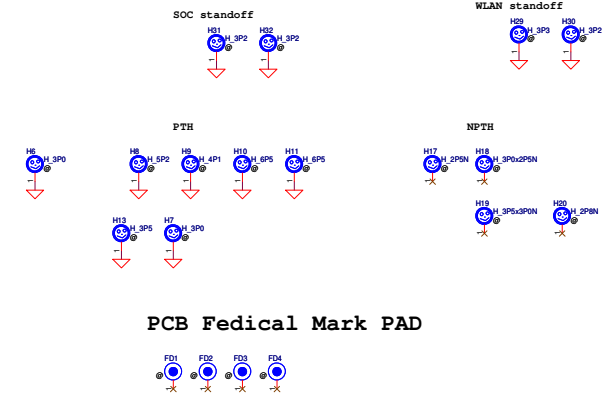
Keyboard LED



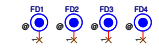
15" KEYBOARD CONN.



Screw Hole



PCB Federal Mark PAD

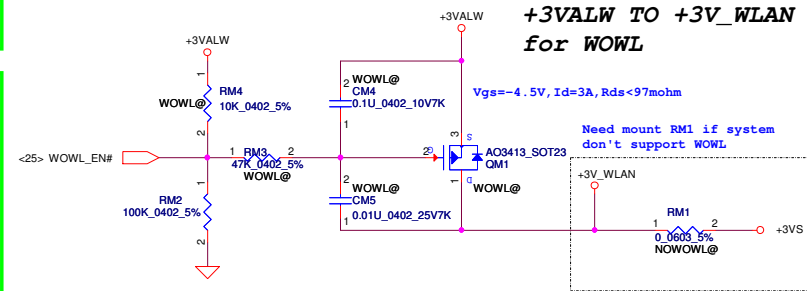
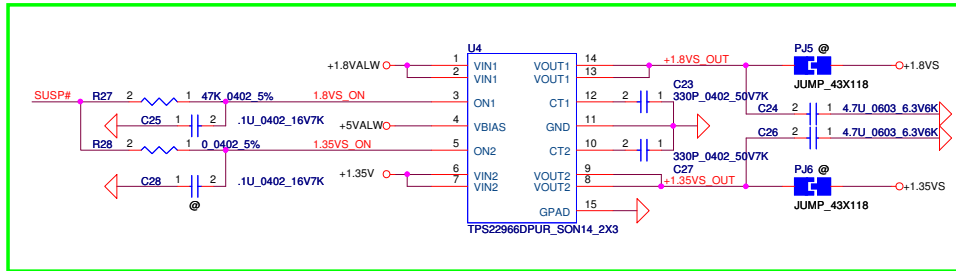
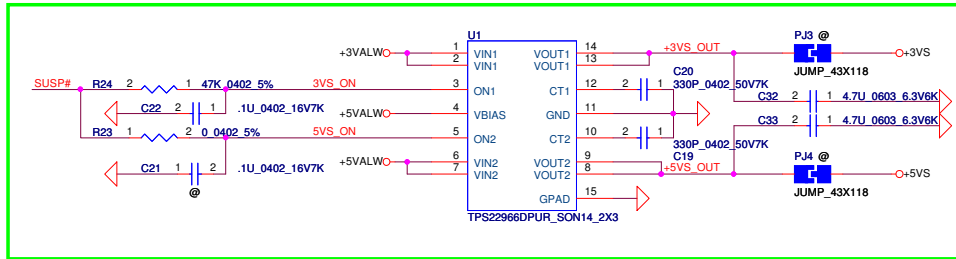


ISPD

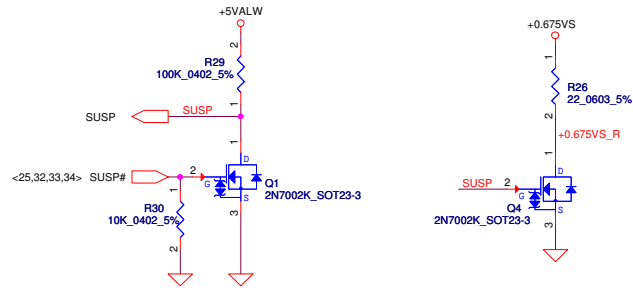
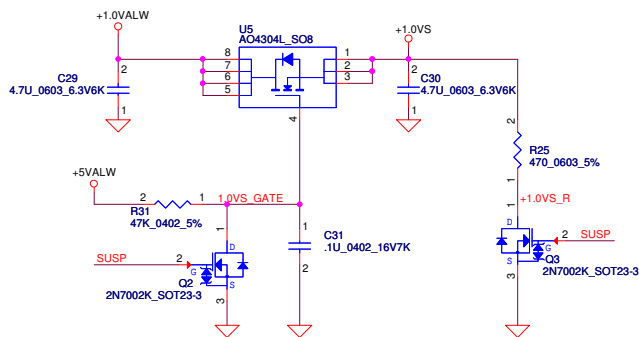


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				TP/ISPD/KB/Screw	
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				Rev	0.1
				Bay Trail M LA-A821P	
				Date	Monday, July 01, 2013

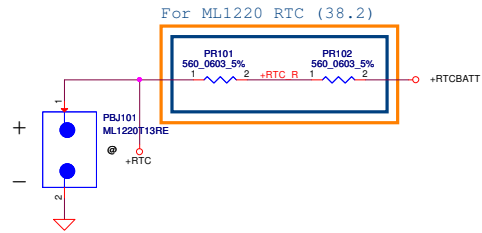
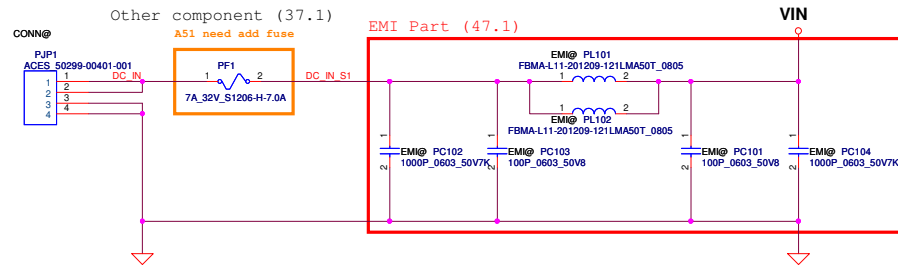
Normal Platform (Not support M-STATE and Deep Sleep)



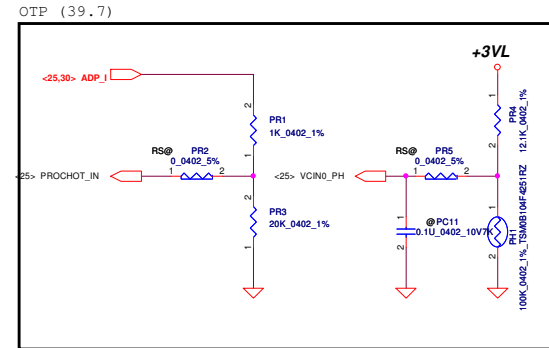
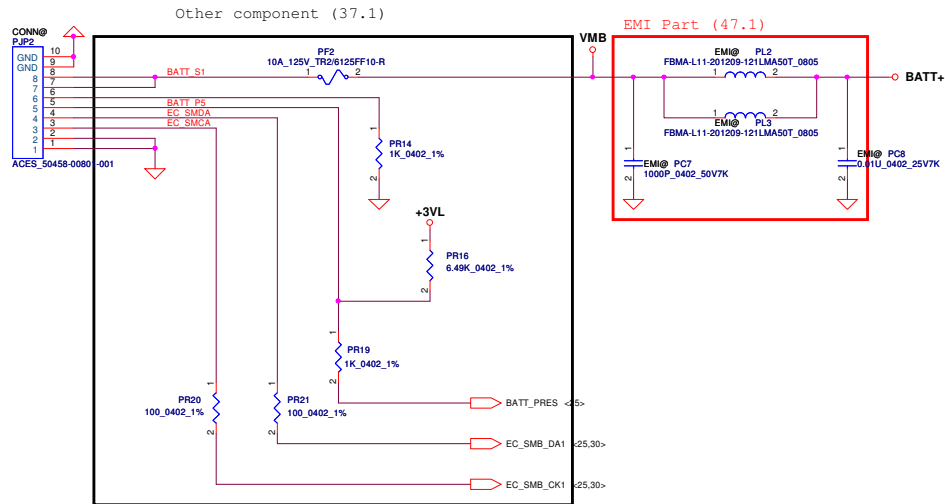
+1.0VALW TO +1.0VS



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			Date	ZRMAA
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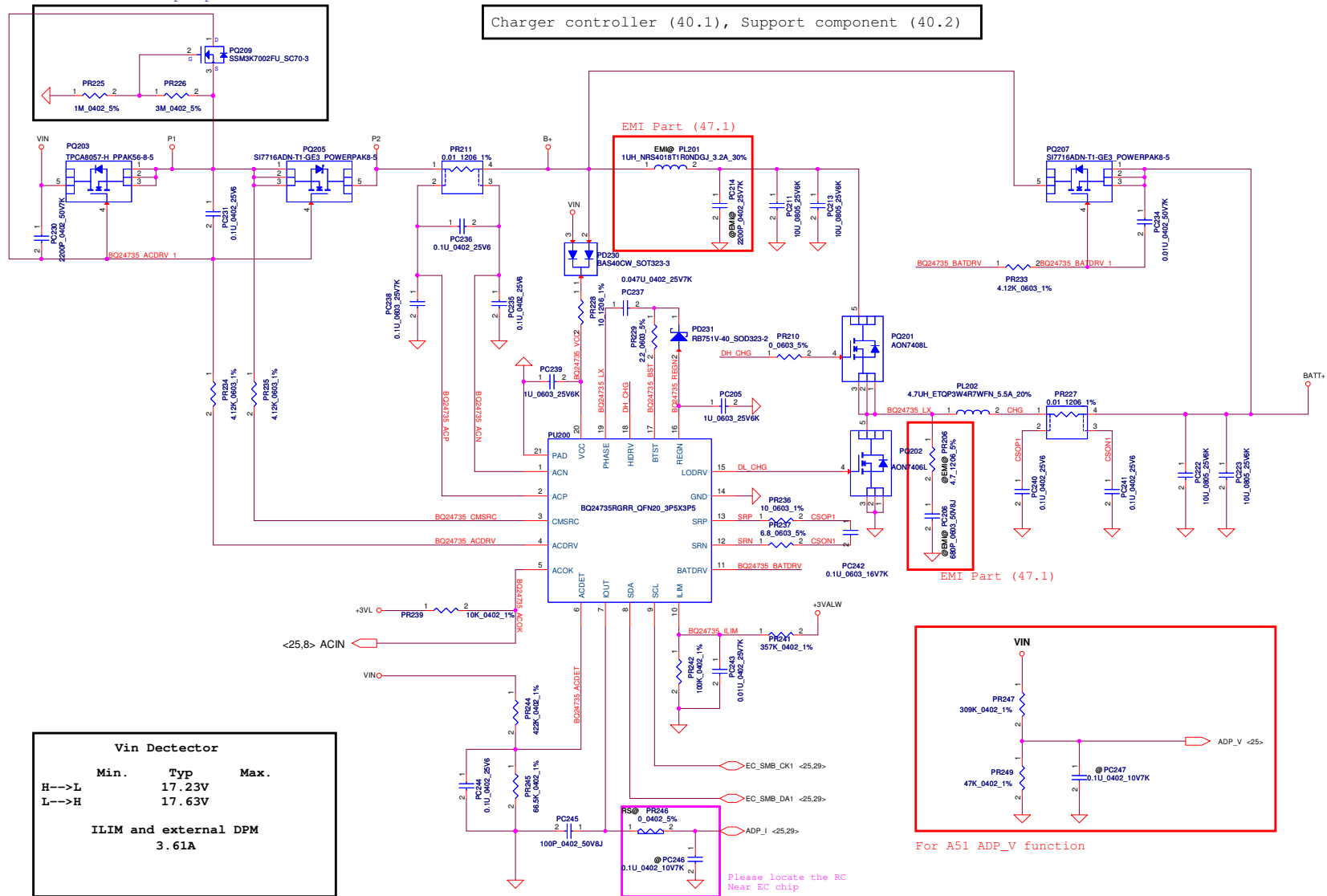
	Initial	Recovery
45W UMA	0.55V	0.43V
75W N14P-GV2	0.90V	0.72V

	Initial	Recovery
CPU OTP	90 C	70 C

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			Date	ZRMAA
			Sheet 29	of 40

for reverse input protection

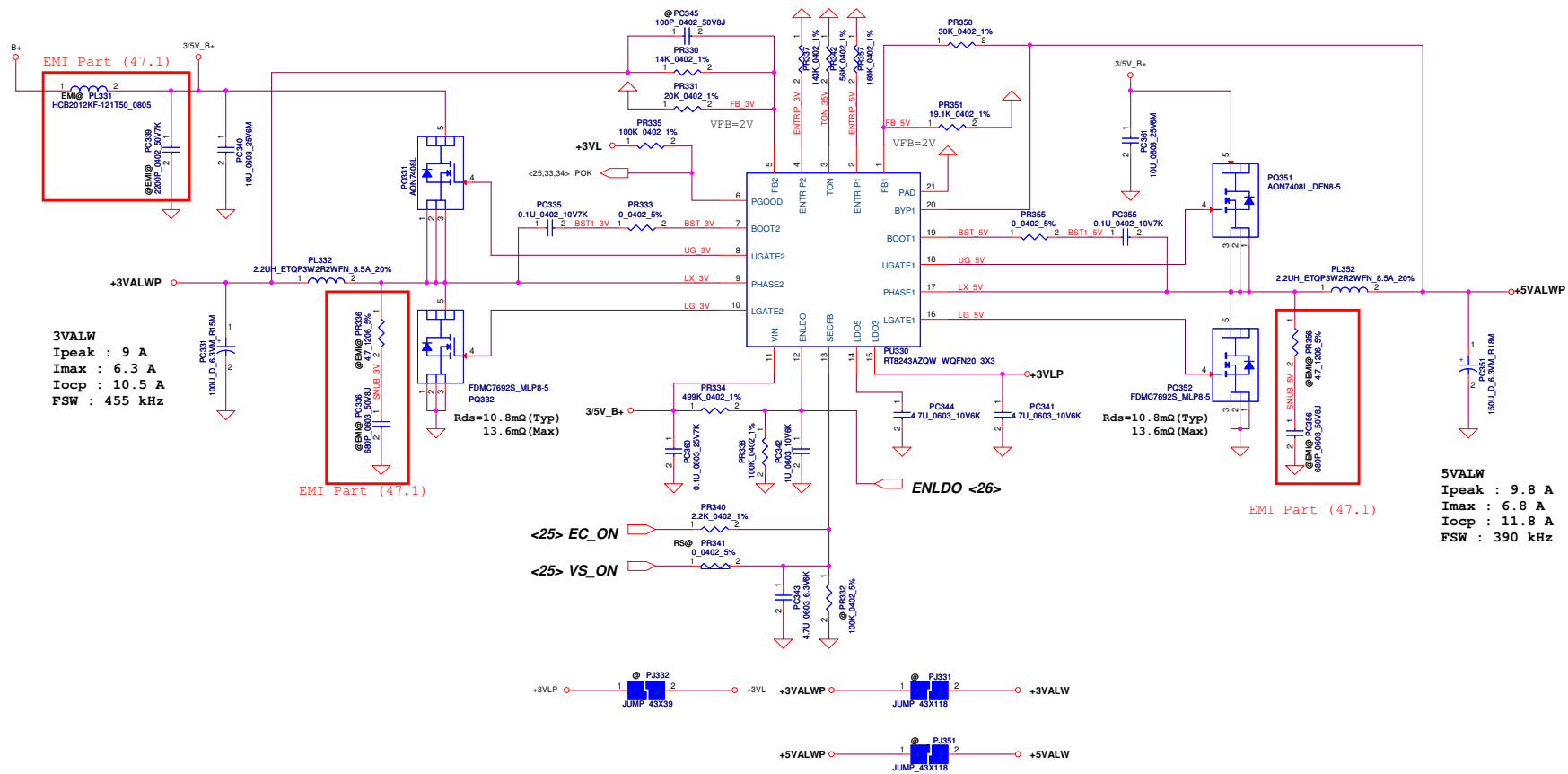
Charger controller (40.1), Support component (40.2)



Vin Detector			
	Min.	Typ.	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
3.61A			

Security Classification	Compal Secret Data		Title	
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Size	Document Number	ZRMMA		Rev 0.1
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3/5VALW controller (35.1), Support component (35.2)

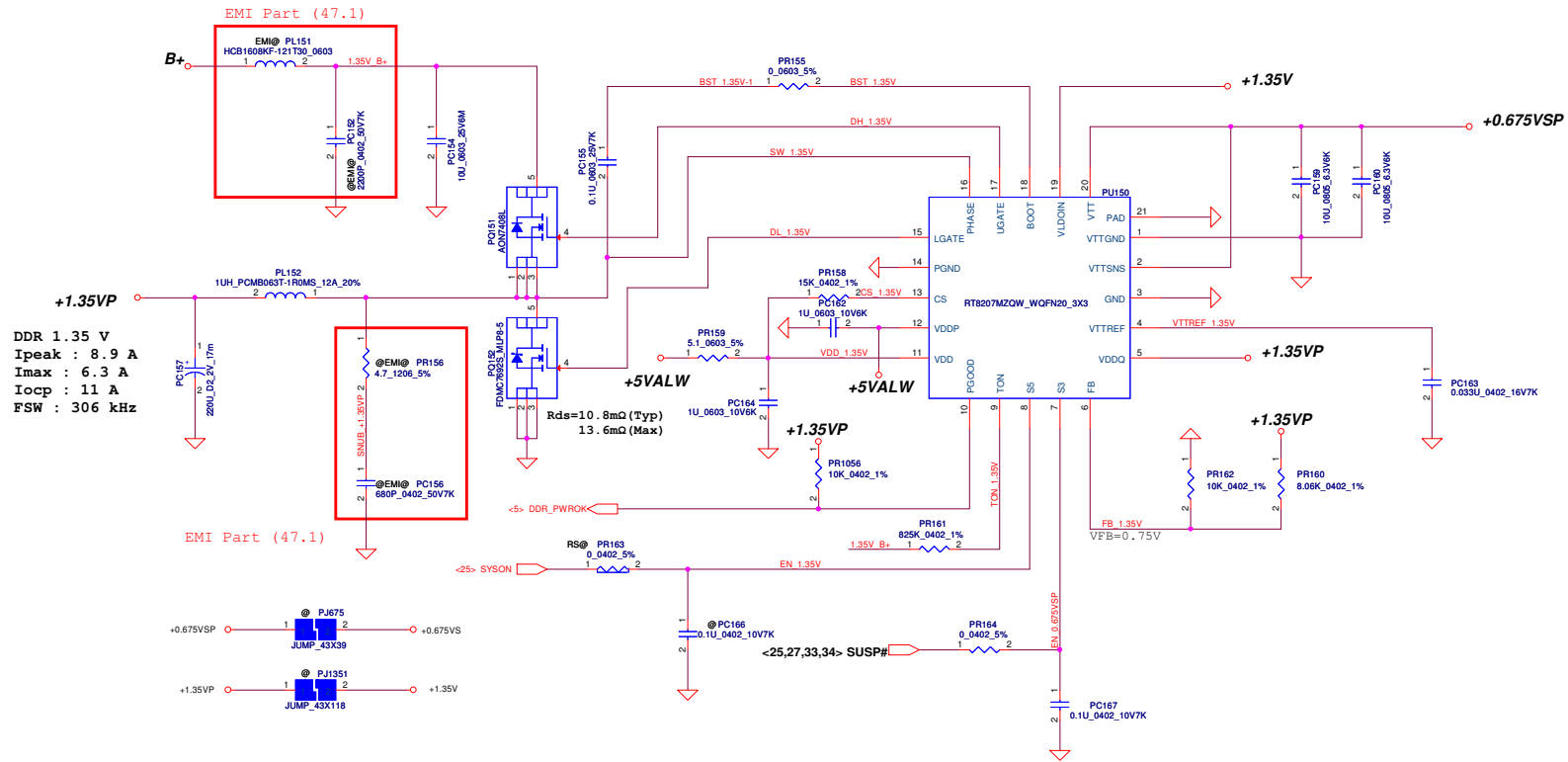


3VALW
 Ipeak : 9 A
 Imax : 6.3 A
 Iocp : 10.5 A
 FSW : 455 kHz

5VALW
 Ipeak : 9.8 A
 Imax : 6.8 A
 Iocp : 11.8 A
 FSW : 390 kHz

Security Classification		Compal Secret Data		Title	
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	ZRMAA				
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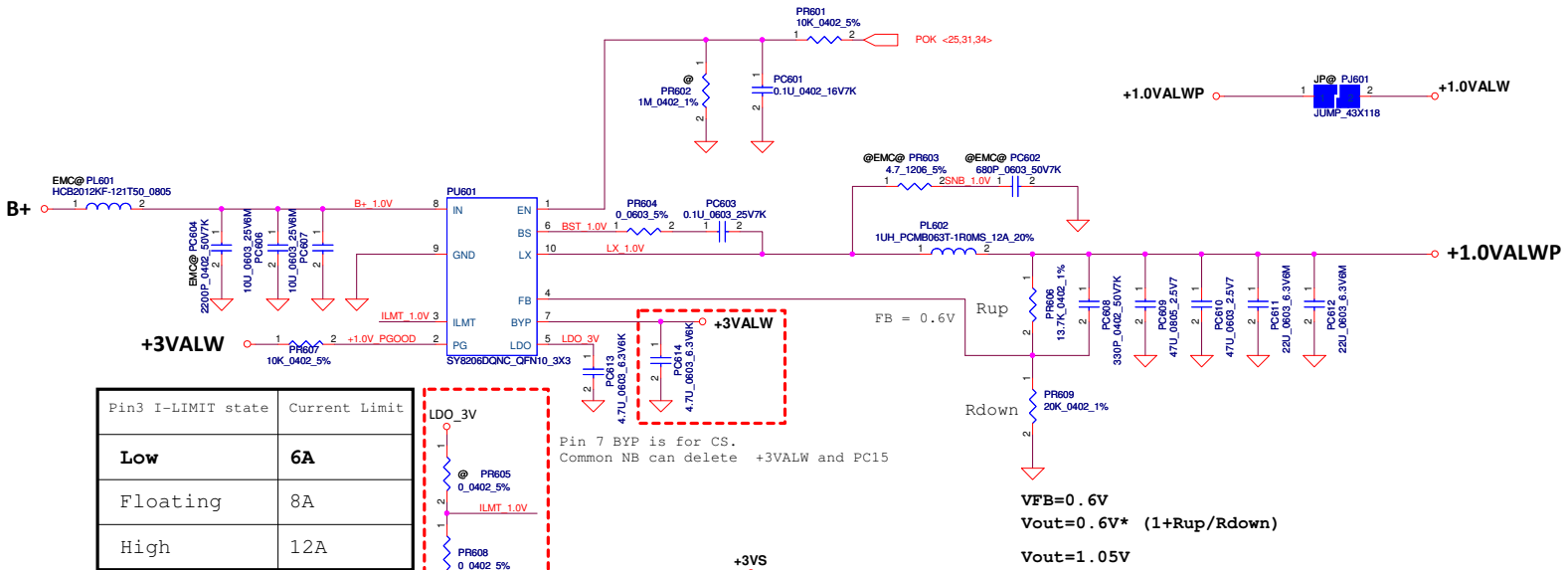
DDR controller (35.3), Support component (35.4)



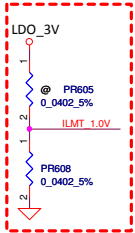
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

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				1.35VP/0.675VSP	
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				Custom	0.1
				ZRMAA	
				Date:	Sheet 32 of 40

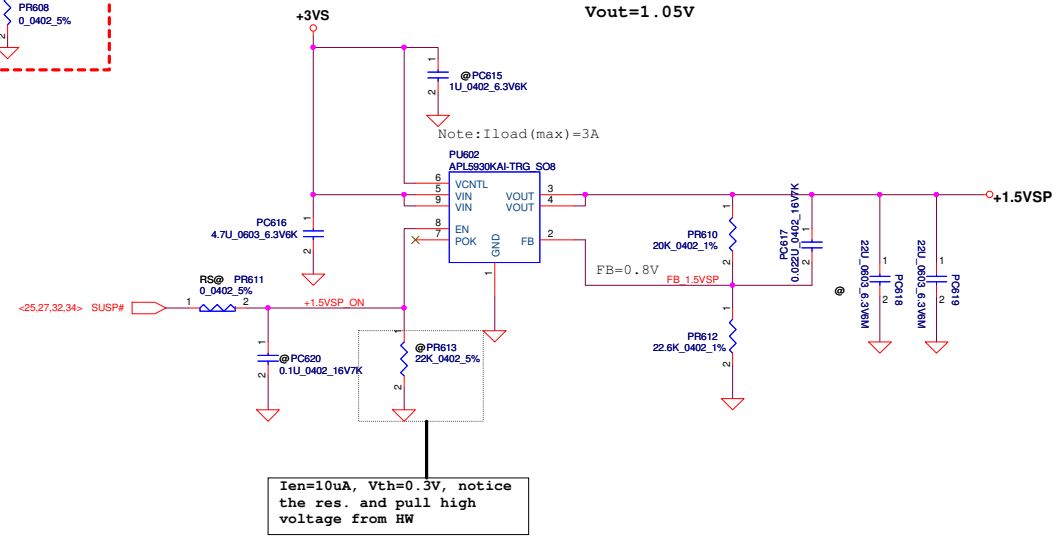


Pin3 I-LIMIT state	Current Limit
Low	6A
Floating	8A
High	12A

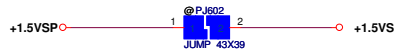


Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

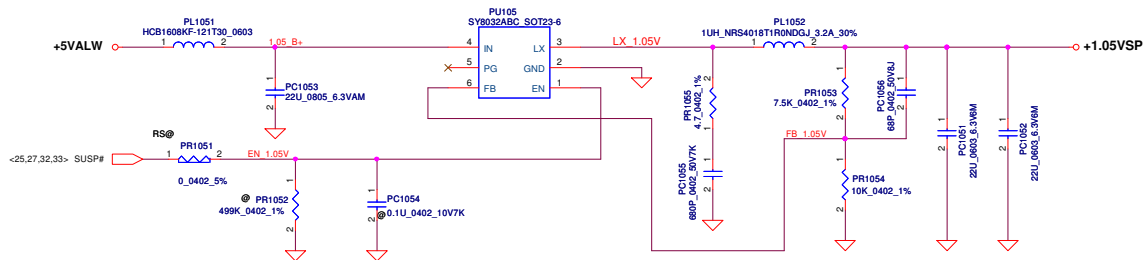
$V_{FB} = 0.6V$
 $V_{out} = 0.6V * (1 + R_{up}/R_{down})$
 $V_{out} = 1.05V$



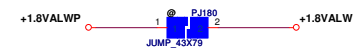
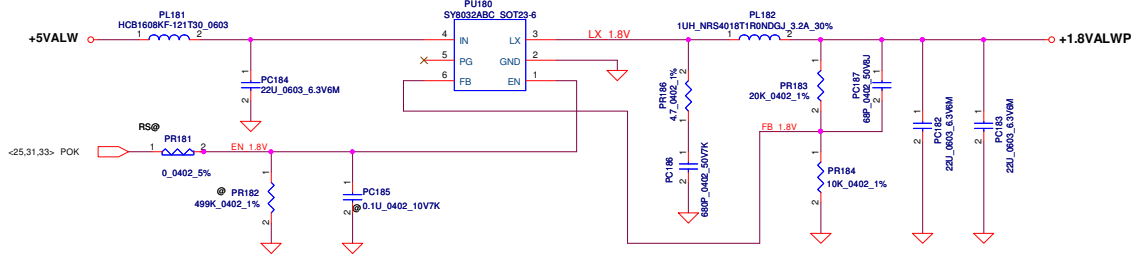
I_{en}=10uA, V_{th}=0.3V, notice the res. and pull high voltage from HW



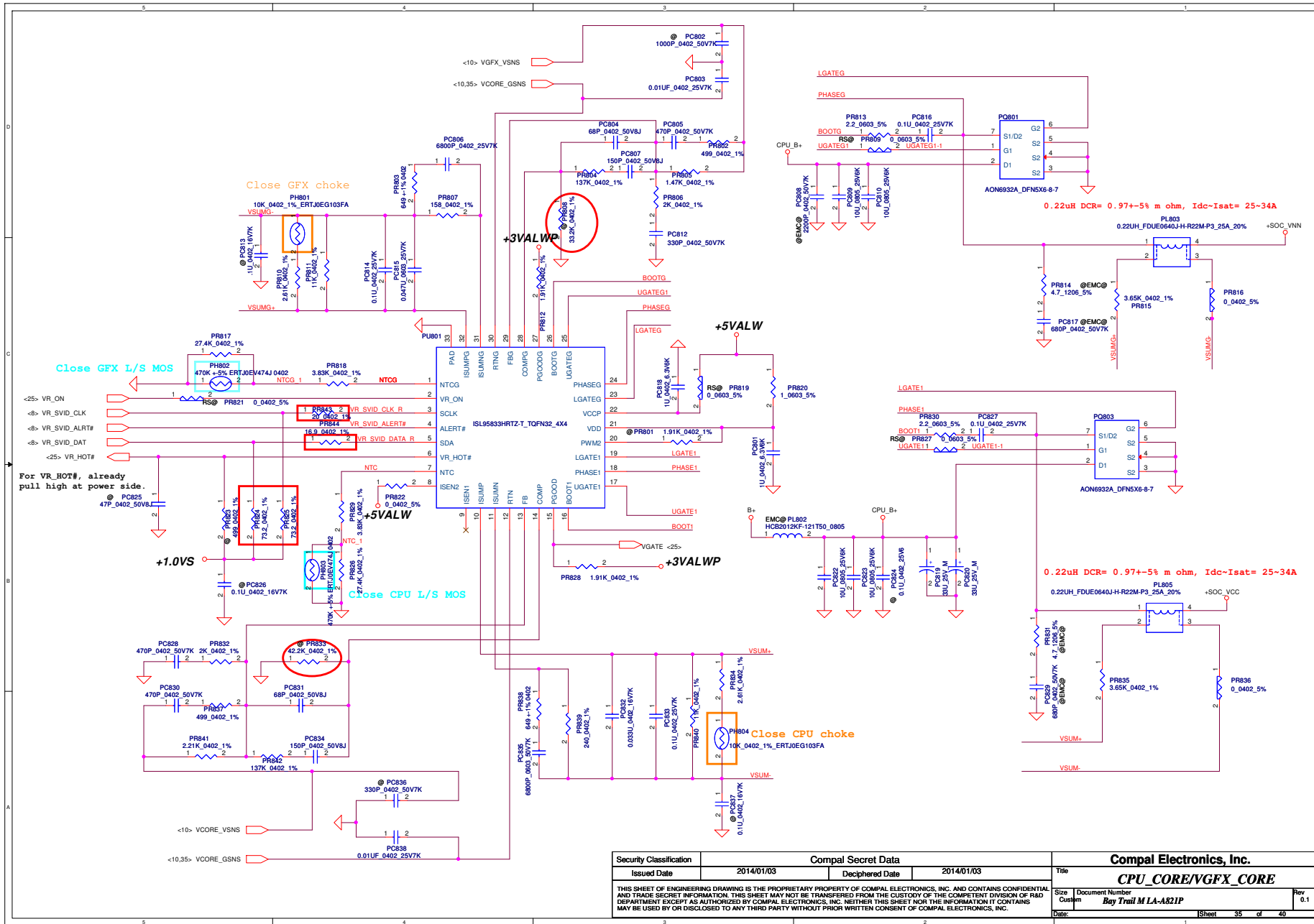
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Document Number	Customer			Date	Rev
V5WE2 M/B LA-9531P Schematic	Monday, July 01, 2013			33	0.1



1.8VS controller (35.15), Support component (35.16)



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				Document Number
				Customer
				Bay Trail M LA-A821P
				Rev
				0.1
				Date
				Monday, July 01, 2013
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				34 of 40

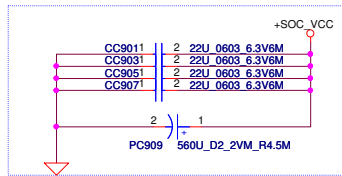


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		2014/01/03

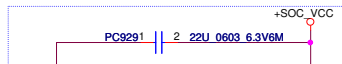
Compal Electronics, Inc.		
CPU_CORE/VGFX_CORE		
Title	Document Number	Rev
	Bay Trail M LA-A821P	0.1

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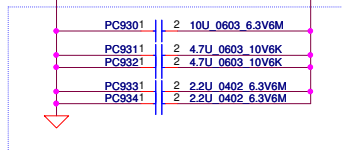
Output Cap



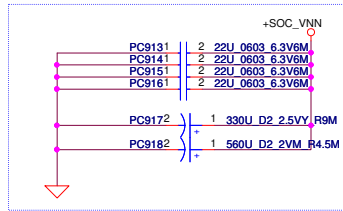
Package Edge Cap



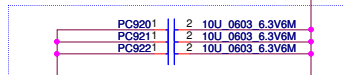
Back Side Cap



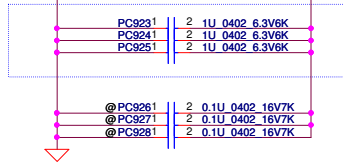
Output Cap



Package Edge Cap



Back Side Cap



Capacitance	Qty	ESR (each)	ESL (each)	Filter	Notes
POSCAP 330 μ F	2	6 m Ω	1.8 nH	Output	1, 2
22 μ F 0805 X5R	4	3 m Ω	0.6 nH	Output	

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Notes
POSCAP 330 μ F	3	6 m Ω	1.8 nH	Output	1, 2
22 μ F 0805 X5R	4	3 m Ω	0.6 nH	Output	

Package Pin Name	Back Side Cap	Package Edge Cap	Comments
CORE_VCC_S0IX	1X0603 10 μ F 2X0402 4.7 μ F 2X0402 2.2 μ F	3X0805 22 μ F	
UNCORE_VNN_S3	3X0402 1 μ F	3X0805 10 μ F	

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