



Part Number = DAZ0K400100

Compal Confidential

K73TA Schematics Document

AMD Sabine

APU Llano / Hudson M3 / Whistler

DIS only

2011-03-08

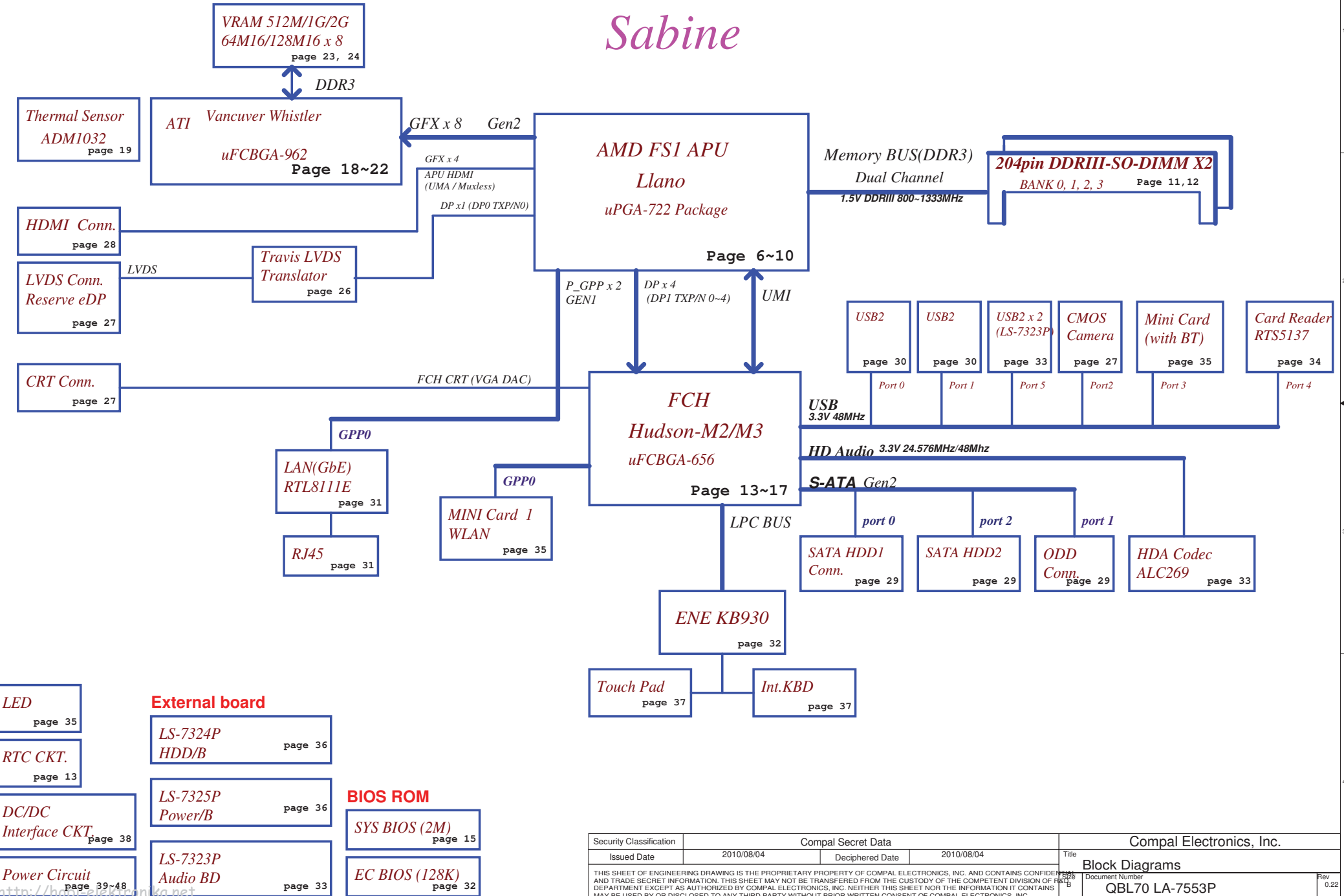
LA-7553P REV: 0.2

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Issued Date	2010/08/04	Deciphered Date	2010/08/04	Title	Cover Page
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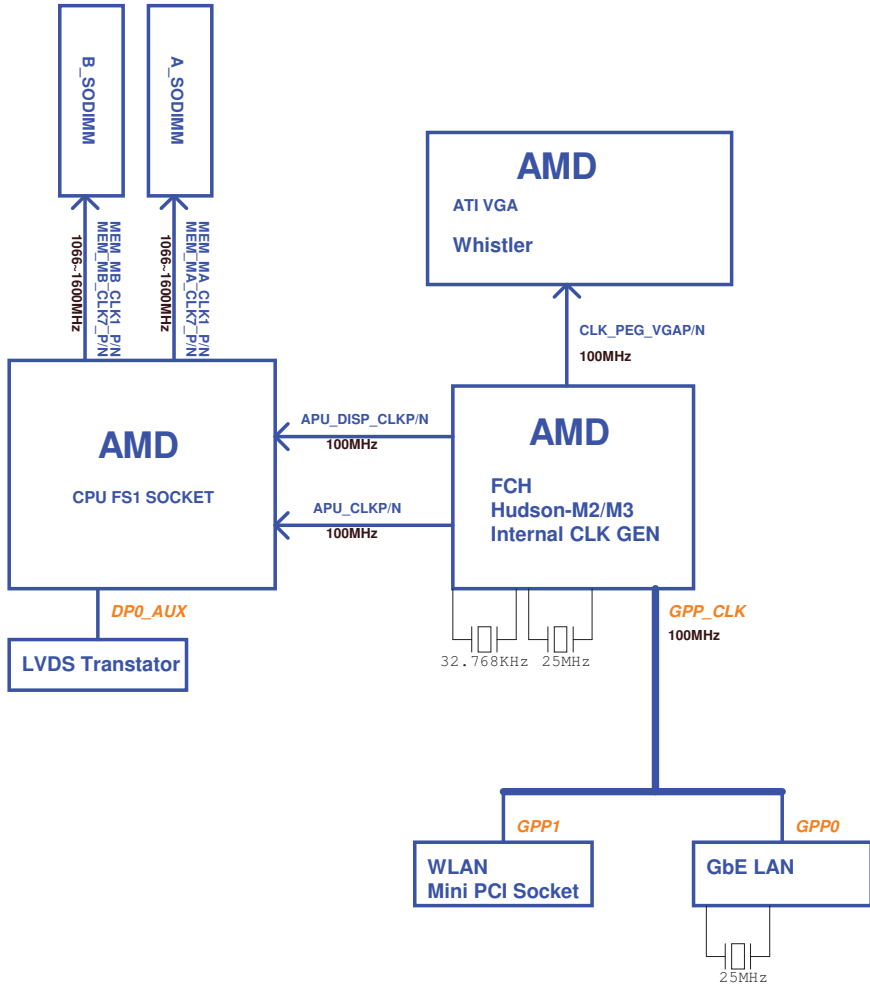
Model Name : QBL70

Sabine

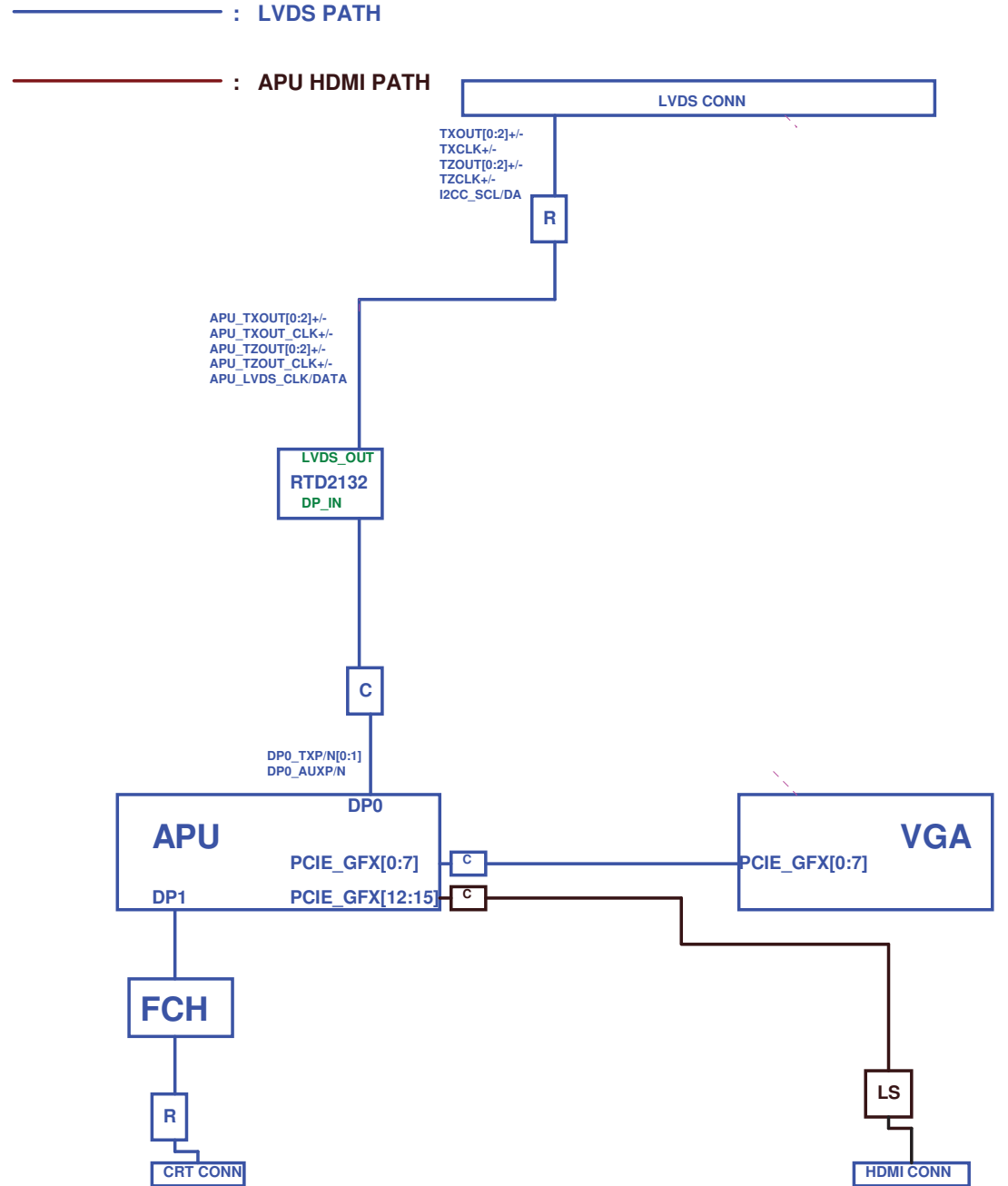


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CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	NA
1	P5WS5
2	P5WH5
3	P7YE5
4	P7YS5
5	NA
6	NA
7	NA

BTO Option Table

BOM Structure	BTO Item
TL@	Translator
VGA@	Use VGA (Mux)
128@	Use VRAM channel A&B
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B







x = 1 is read cmd, x = 0 is write cmd.





External PCI Devices			
Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (VGA)	1001 101X b	9AH



FCH SM Bus 0 address			FCH SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	D0			
DDR DIMM2	1101 001X b	D2			

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18 PCIE_GTX_C_FRX_P0[0..7]  
 18 PCIE_GTX_C_FRX_N0[0..7]  

PCIE_FTX_C_GRX_P0[0..7] 18  
 PCIE_FTX_C_GRX_N0[0..7] 18  

APU To HDMI

 PCIE_FTX_GRX_P[12..15] 28
 PCIE_FTX_GRX_N[12..15] 28

JCPU1A		CONN@	
PCI EXPRESS			
PCIE_GTX_C_FRX_P0 AA8	P_GFX_RXP0	P_GFX_TXP0 AA2	PCIE_FTX_GRX_P0 C917 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0 AA9	P_GFX_RXN0	P_GFX_TXN0 AA3	PCIE_FTX_GRX_N0 C918 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1 Y7	P_GFX_RXP1	P_GFX_TXP1 Y2	PCIE_FTX_GRX_P1 C919 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1 Y8	P_GFX_RXN1	P_GFX_TXN1 Y1	PCIE_FTX_GRX_N1 C920 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2 W5	P_GFX_RXP2	P_GFX_TXP2 Y4	PCIE_FTX_GRX_P2 C921 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2 W6	P_GFX_RXN2	P_GFX_TXN2 Y5	PCIE_FTX_GRX_N2 C922 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_N2
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PCIE_GTX_C_FRX_P5 U5	P_GFX_RXP5	P_GFX_TXP5 V4	PCIE_FTX_GRX_P5 C927 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5 U6	P_GFX_RXN5	P_GFX_TXN5 V5	PCIE_FTX_GRX_N5 C928 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_N5
PCIE_GTX_C_FRX_P6 U8	P_GFX_RXP6	P_GFX_TXP6 U2	PCIE_FTX_GRX_P6 C929 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_P6
PCIE_GTX_C_FRX_N6 U9	P_GFX_RXN6	P_GFX_TXN6 U3	PCIE_FTX_GRX_N6 C930 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_N6
PCIE_GTX_C_FRX_P7 T7	P_GFX_RXP7	P_GFX_TXP7 T2	PCIE_FTX_GRX_P7 C931 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_P7
PCIE_GTX_C_FRX_N7 T8	P_GFX_RXN7	P_GFX_TXN7 T1	PCIE_FTX_GRX_N7 C932 1 2 0.1U 0402 16V7K PCIE_FTX_C_GRX_N7
X RB5	P_GFX_RXP8	T4 X	
X RB6	P_GFX_RXN8	T5 X	
X RB8	P_GFX_RXP9	R2 X	
X RB9	P_GFX_RXN9	R3 X	
X P7	P_GFX_RXP10	P2 X	
X P8	P_GFX_RXN10	P1 X	
X N5	P_GFX_RXP11	P4 X	
X N6	P_GFX_RXN11	P5 X	
N2	P_GFX_RXP12	N2	PCIE_FTX_GRX_P12
N3	P_GFX_RXN12	N3	PCIE_FTX_GRX_N12
M2	P_GFX_RXP13	M2	PCIE_FTX_GRX_P13
M3	P_GFX_RXN13	M1	PCIE_FTX_GRX_N13
L5	P_GFX_RXP14	M4	PCIE_FTX_GRX_P14
L6	P_GFX_RXN14	M5	PCIE_FTX_GRX_N14
L8	P_GFX_RXP15	L2	PCIE_FTX_GRX_P15
L9	P_GFX_RXN15	L3	PCIE_FTX_GRX_N15

For UMA Mux.

To HDMI

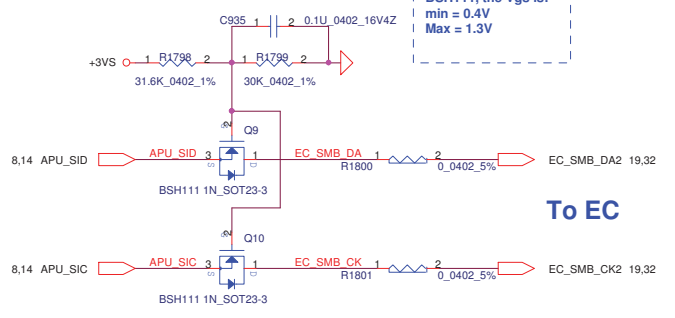
CK

GPP		GLAN	
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31 PCIE_DTX_C_FRX_N0 AC6	P_GPP_RXN0	P_GPP_TXN0 AD5	PCIE_FTX_DRX_N0 C951 1 2 0.1U 0402 16V7K PCIE_FTX_C_DRX_N0 31
X AC8	P_GPP_RXP1	AC2 X	
X AC9	P_GPP_RXN1	AC3 X	
X AB7	P_GPP_RXP2	AB2 X	
X AB8	P_GPP_RXN2	AB1 X	
X AA5	P_GPP_RXP3	AB4 X	
X AA6	P_GPP_RXN3	AB5 X	

DMI-LINK			
13 UMI_MTX_C_FRX_P0 AF8	P_UMI_RXP0	P_UMI_TXP0 AF1	UMI_FTX_MRX_P0 C956 1 2 0.1U 0402 16V7K UMI_FTX_C_MRX_P0 13
13 UMI_MTX_C_FRX_N0 AF7	P_UMI_RXN0	P_UMI_TXN0 AF2	UMI_FTX_MRX_N0 C957 1 2 0.1U 0402 16V7K UMI_FTX_C_MRX_N0 13
13 UMI_MTX_C_FRX_P1 AE6	P_UMI_RXP1	P_UMI_TXP1 AF5	UMI_FTX_MRX_P1 C958 1 2 0.1U 0402 16V7K UMI_FTX_C_MRX_P1 13
13 UMI_MTX_C_FRX_N1 AE5	P_UMI_RXN1	P_UMI_TXN1 AF4	UMI_FTX_MRX_N1 C959 1 2 0.1U 0402 16V7K UMI_FTX_C_MRX_N1 13
13 UMI_MTX_C_FRX_P2 AE9	P_UMI_RXP2	P_UMI_TXP2 AE3	UMI_FTX_MRX_P2 C960 1 2 0.1U 0402 16V7K UMI_FTX_C_MRX_P2 13
13 UMI_MTX_C_FRX_N2 AE8	P_UMI_RXN2	P_UMI_TXN2 AE2	UMI_FTX_MRX_N2 C961 1 2 0.1U 0402 16V7K UMI_FTX_C_MRX_N2 13
13 UMI_MTX_C_FRX_P3 AD8	P_UMI_RXP3	P_UMI_TXP3 AD1	UMI_FTX_MRX_P3 C962 1 2 0.1U 0402 16V7K UMI_FTX_C_MRX_P3 13
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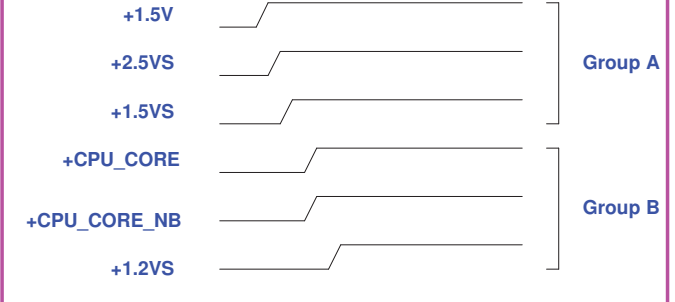
CPU TSI interface level shift



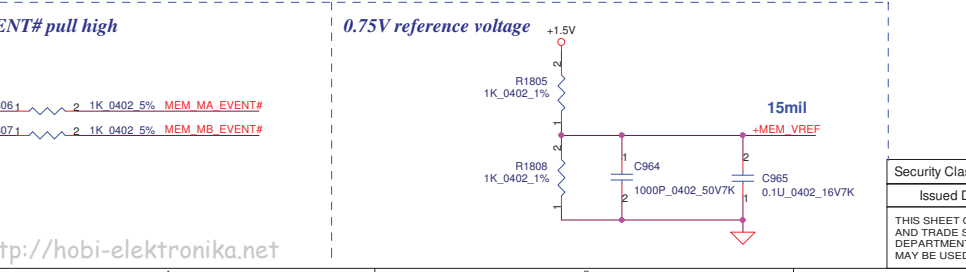
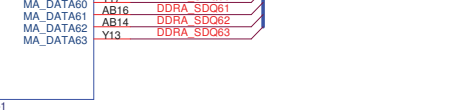
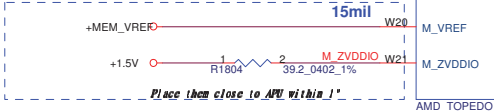
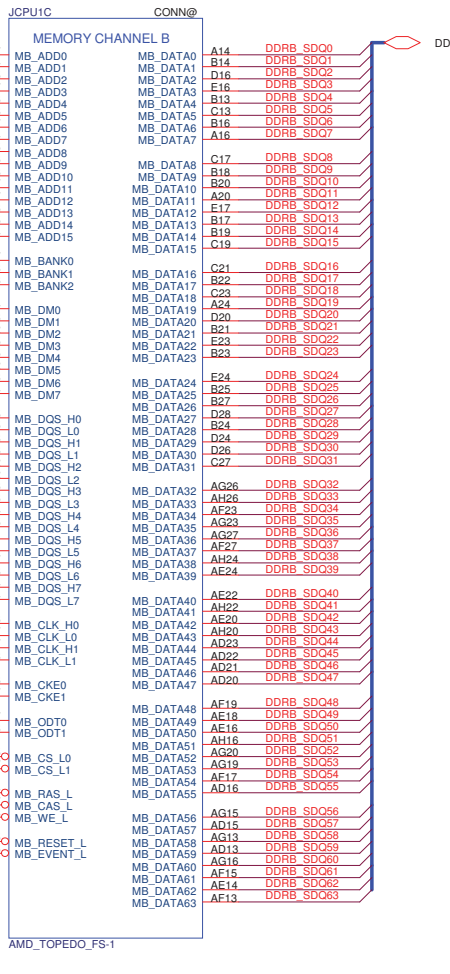
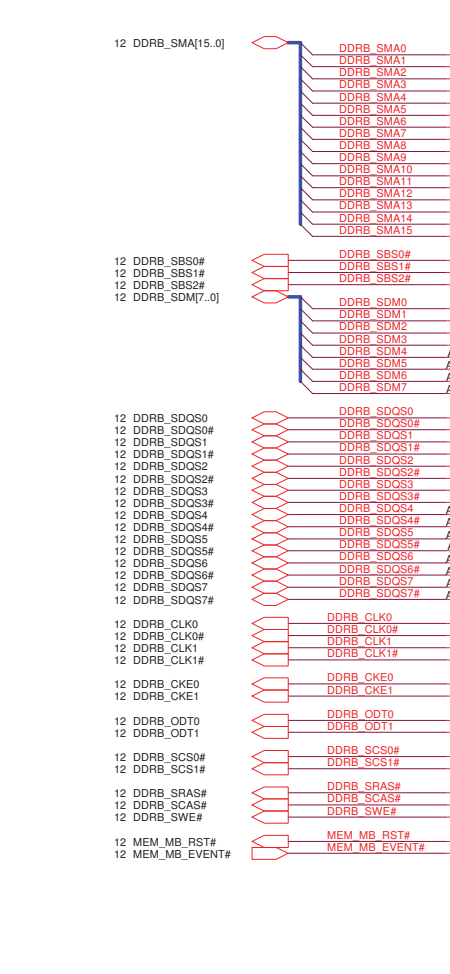
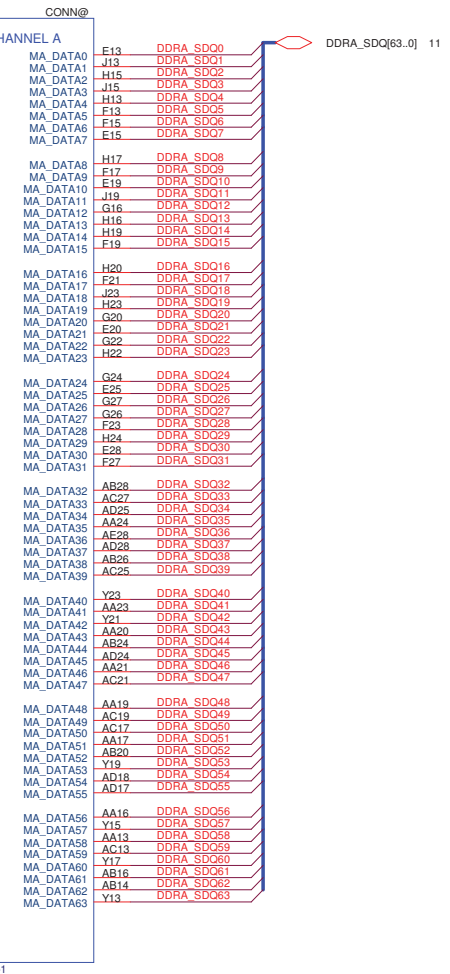
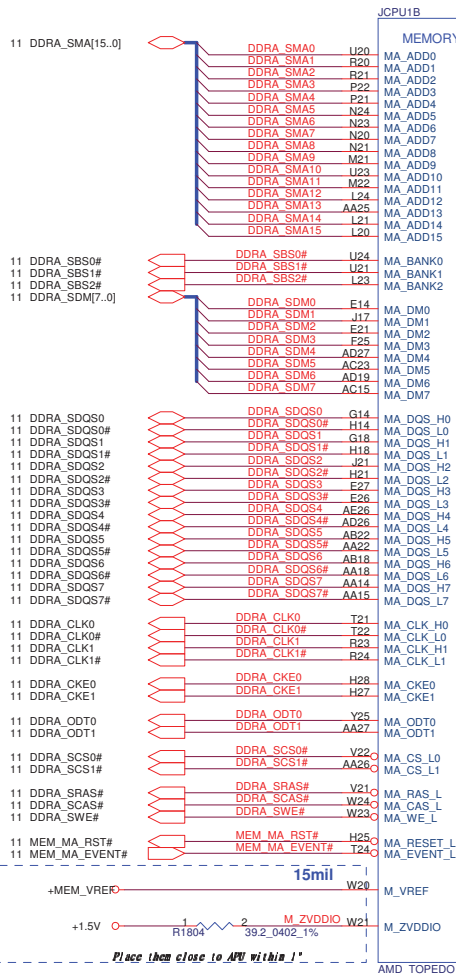
BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

To EC

Power Sequence of APU



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To LVDS Translator

To FCH VGA ML

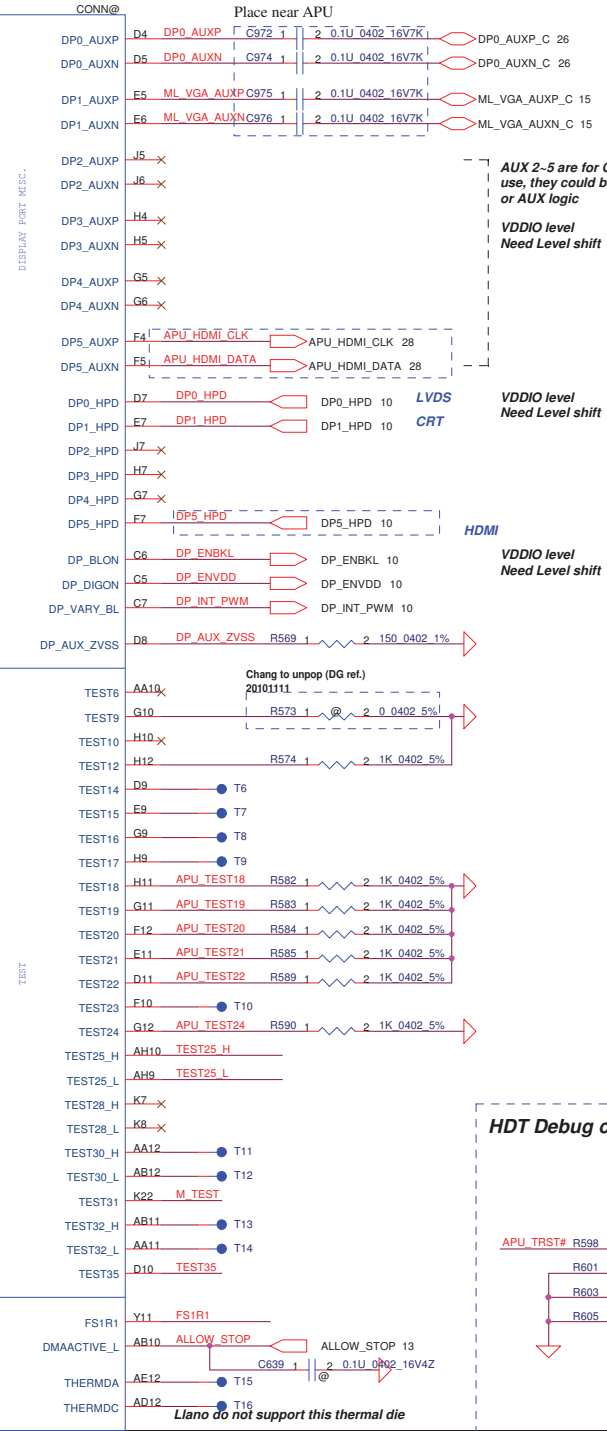
100MHz

100MHz_NSS

Chang to PU +1.5V (DG ref.) 20101111

Close to Header

Route as differential with VSS_SENSE



To LVDS Translator

To FCH

AUX 2-5 are for GFX interface use, they could be selected to I2C or AUX logic

VDDIO level Need Level shift

VDDIO level Need Level shift

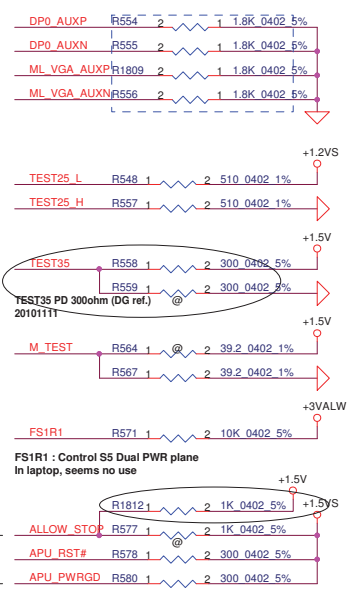
VDDIO level Need Level shift

Chang to unpop (DG ref.) 20101111

HDT Debug conn

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Deciphered Date	2010/08/04

If not used, pins are left unconnected (DG ref.) 20101111



Asserted as an input to force the processor into the HTC-active state

THERMTRIP shutdown temperature: 125 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

MISC

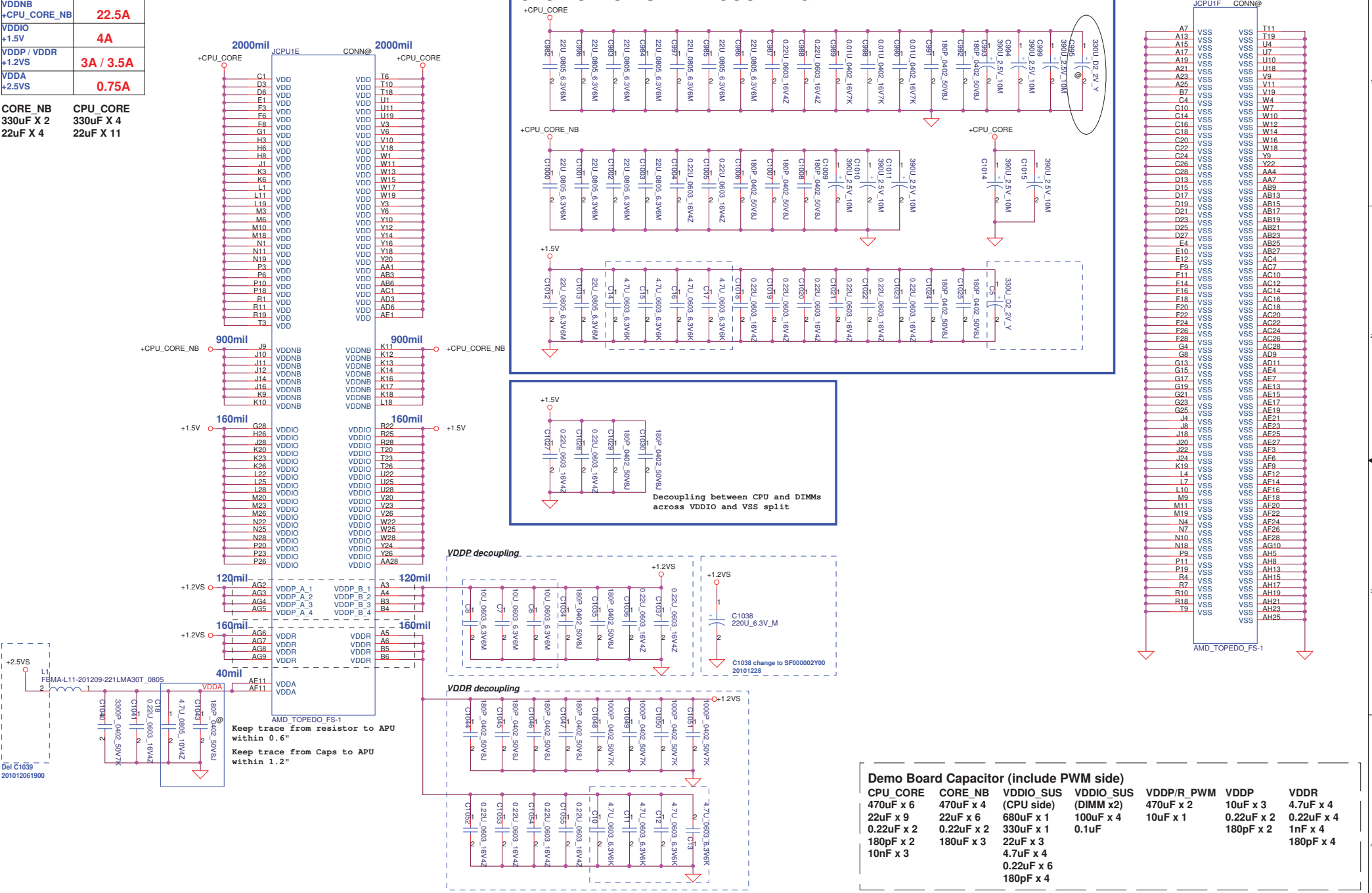
Cut on CPU side, Debug mount

AMD TOPEDO_FS-1	Security Classification	Compal Secret Data	Title	Compal Electronics, Inc.
	Issued Date	2010/08/04	Document Number	AMD FS1 Display / MISC / HDT
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Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB CPU CORE
330uF X 2 330uF X 4
22uF X 4 22uF X 11

CPU BOTTOM SIDE DECOUPLING



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HPD

Translator HPD

From Translator



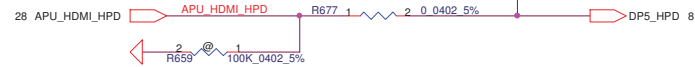
CRT HPD

From FCH

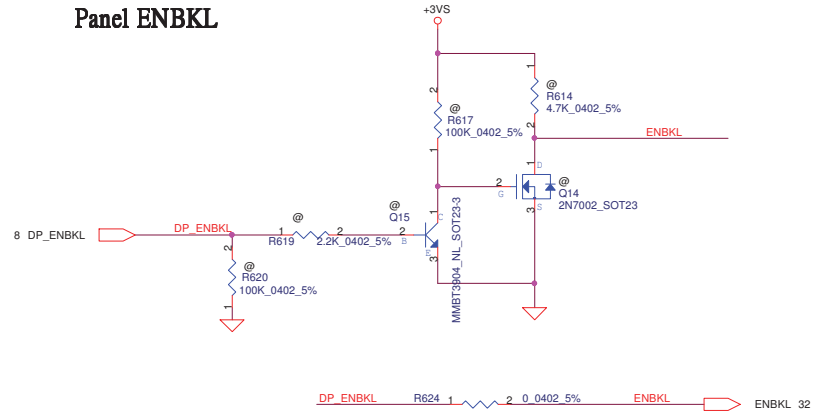


HDMI HPD

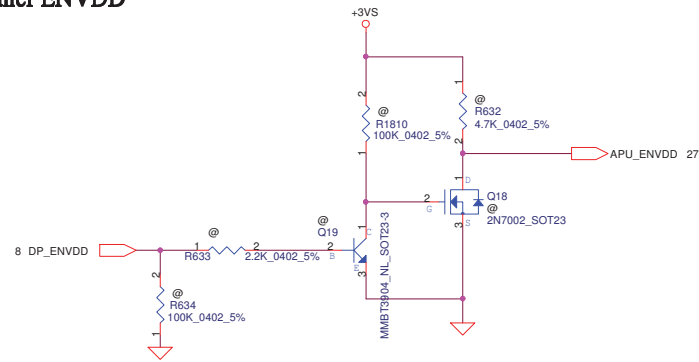
From HDMI Conn



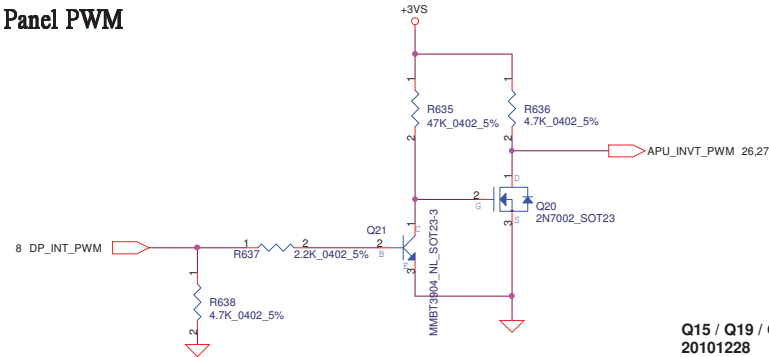
Panel ENBKL



Panel ENVDD

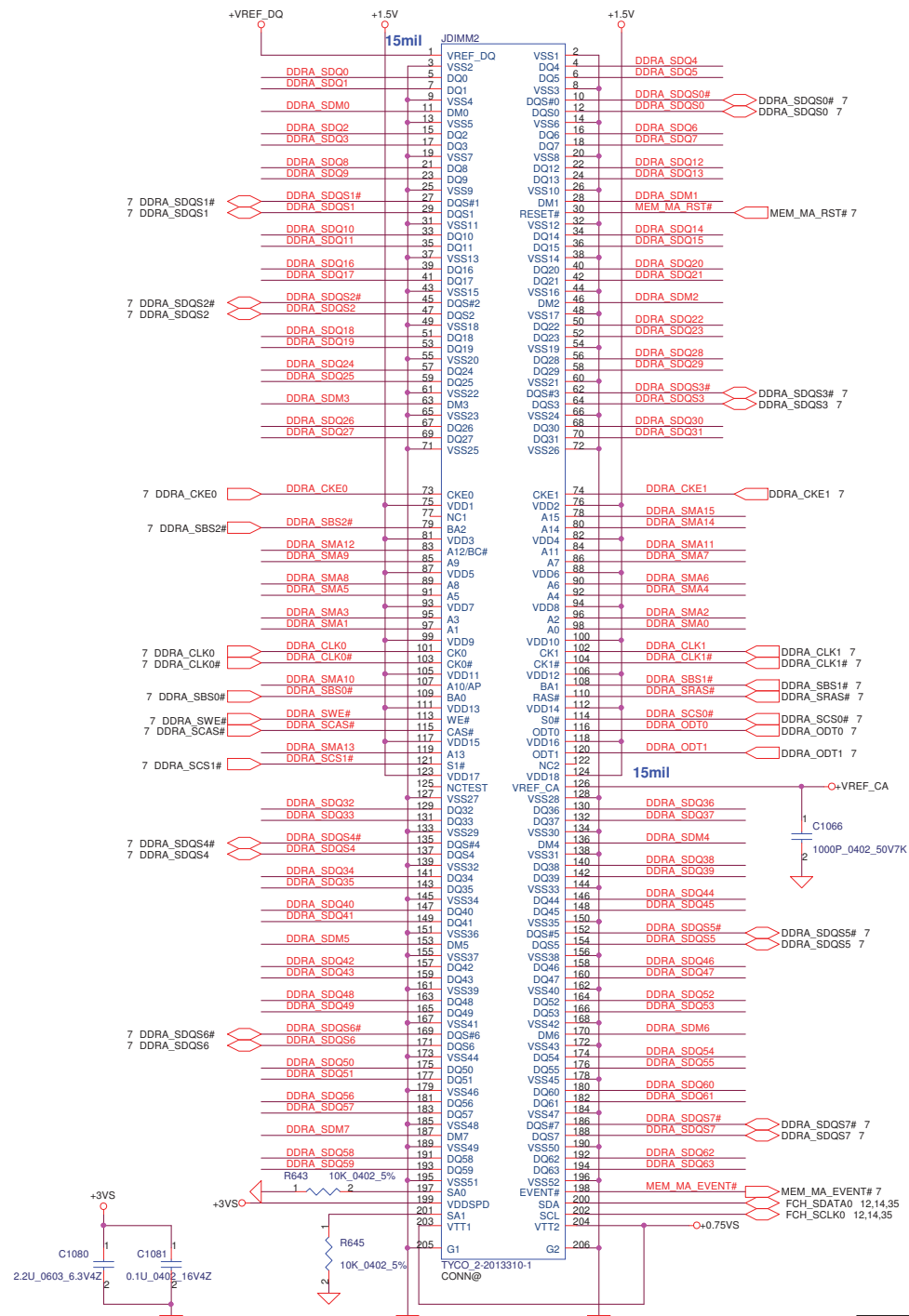


Panel PWM



Q15 / Q19 / Q21 change to SB000006A00
20101228

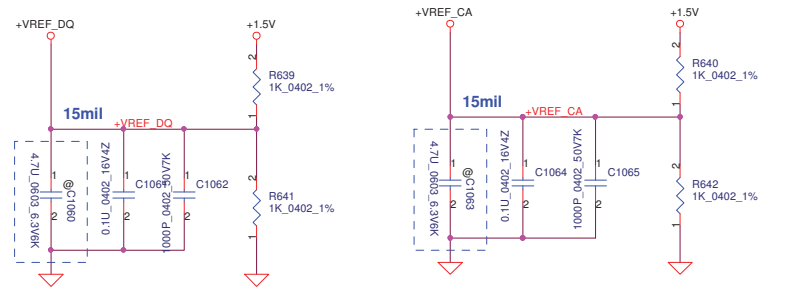
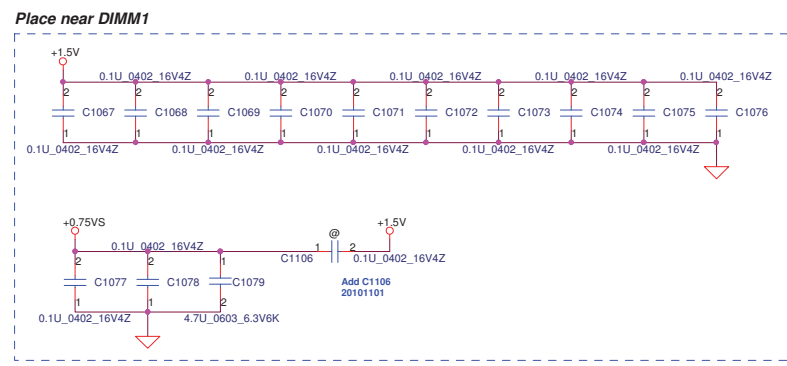
Security Classification	Compal Secret Data			Title	AMD FS1 Singal Level Shifter
Issued Date	2010/08/04	Deciphered Date	2010/08/04	Document Number	QBL70 LA-7553P
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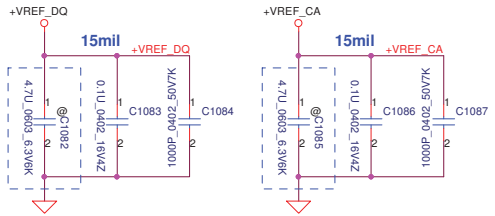
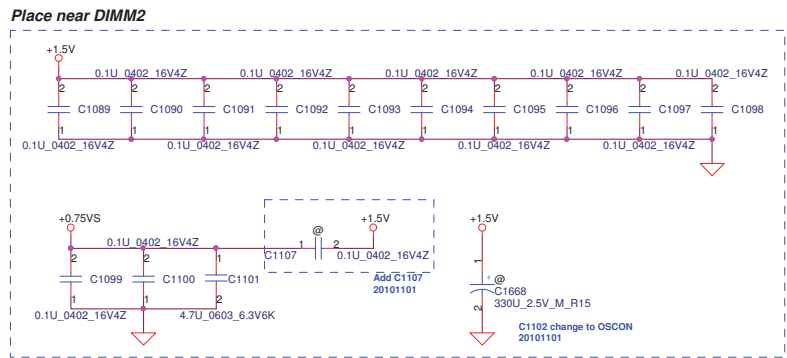
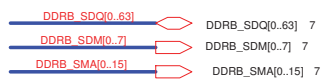
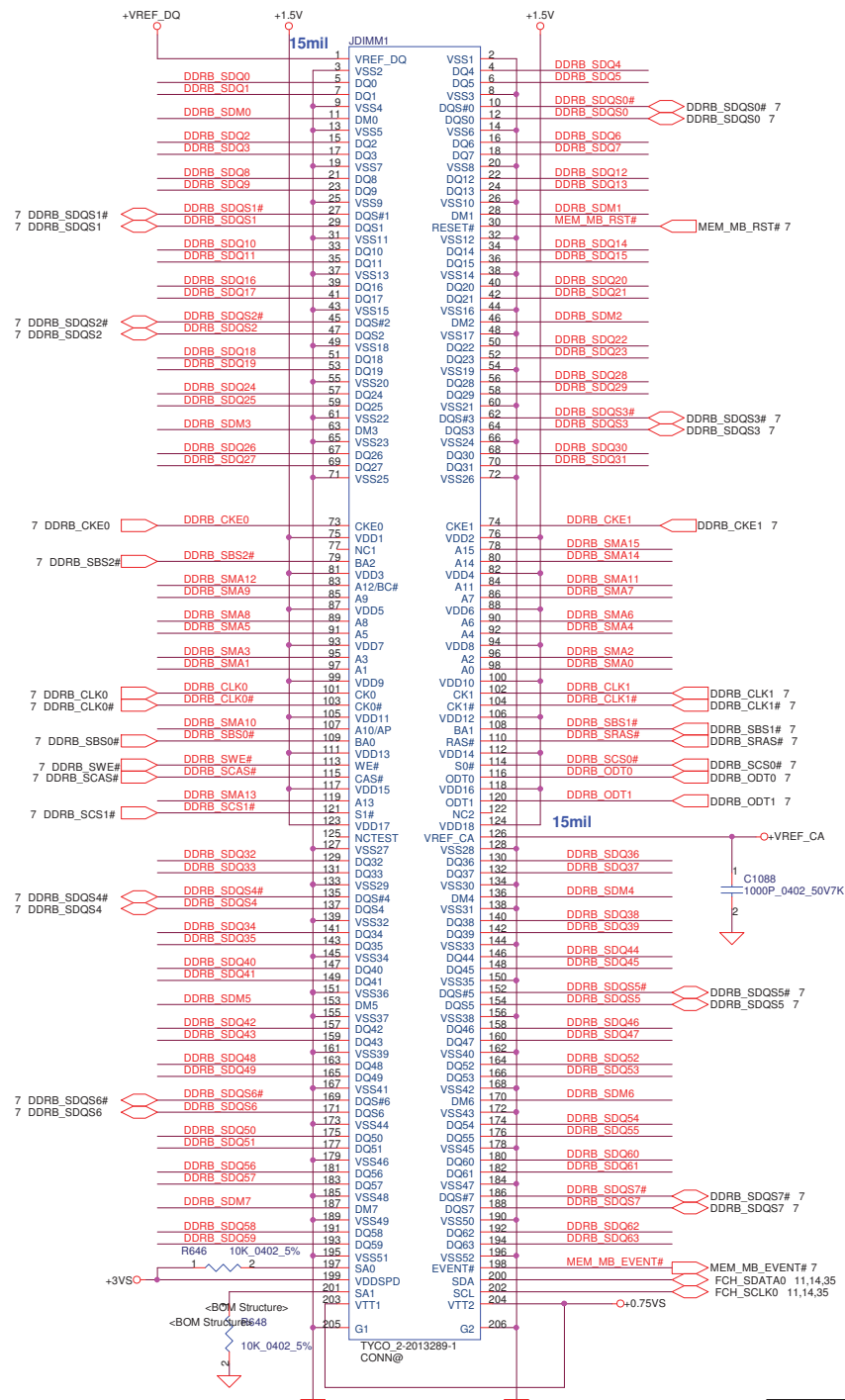
DIMM_A STD H:9.2mm
 <Address: 00>

<http://hobi-elektronik.net>

- DDR_A SDQ[0..63] DDR_A_SDQ[0..63] 7
- DDR_A SDM[0..7] DDR_A_SDM[0..7] 7
- DDR_A SMA[0..15] DDR_A_SMA[0..15] 7

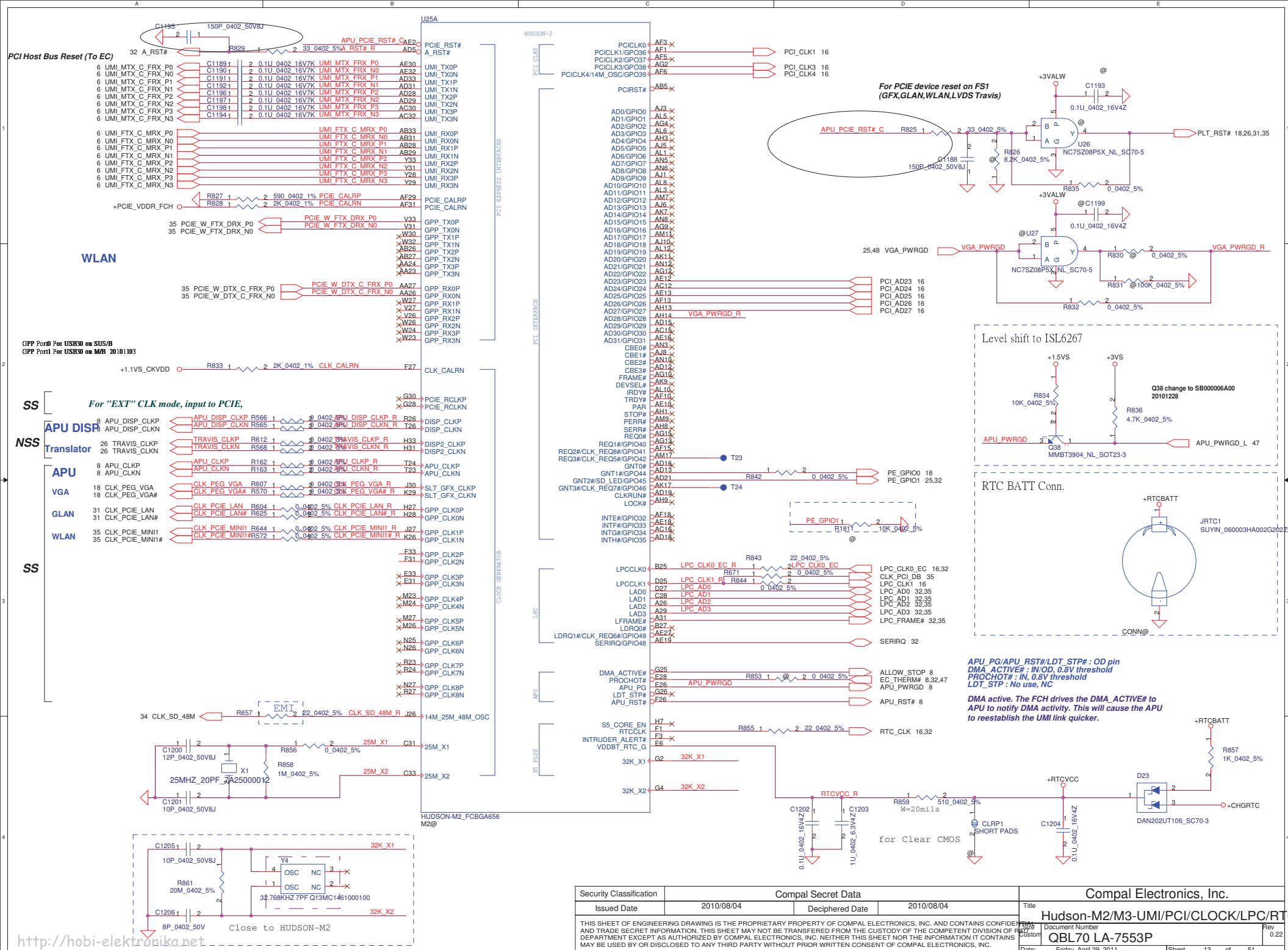


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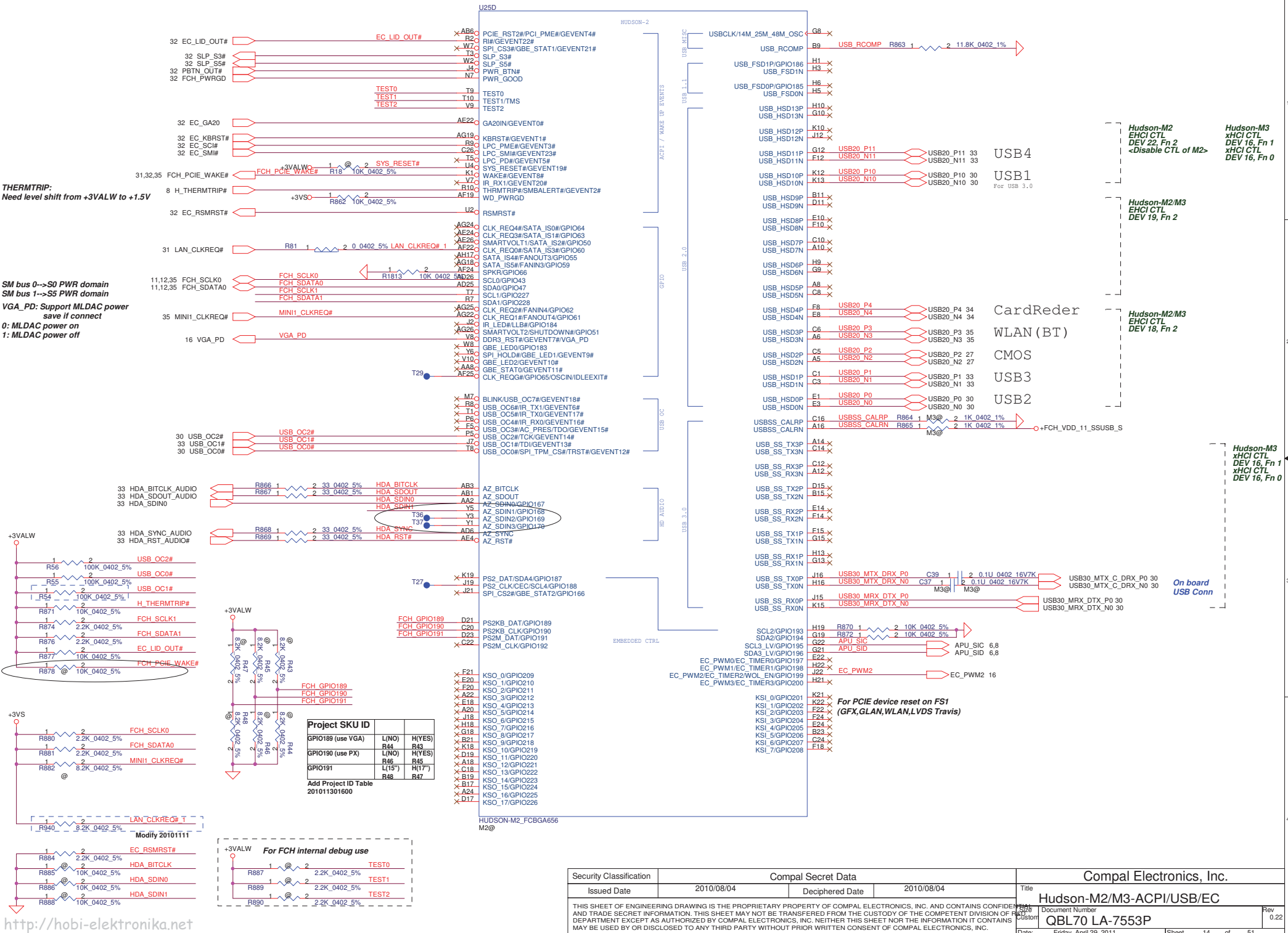
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Document Number	QBL70 LA-7553P	Rev	0.22	Date	Friday, April 23, 2011
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PCIE_RST2 : Reset PCIE device on Hudson2

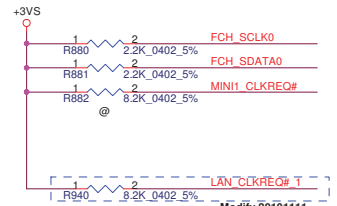
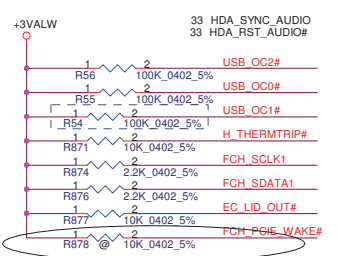


THERMTRIP:
Need level shift from +3VALW to +1.5V

SM bus 0->S0 PWR domain
SM bus 1->S5 PWR domain

VGA_PD: Support MLDAC power
save it connect

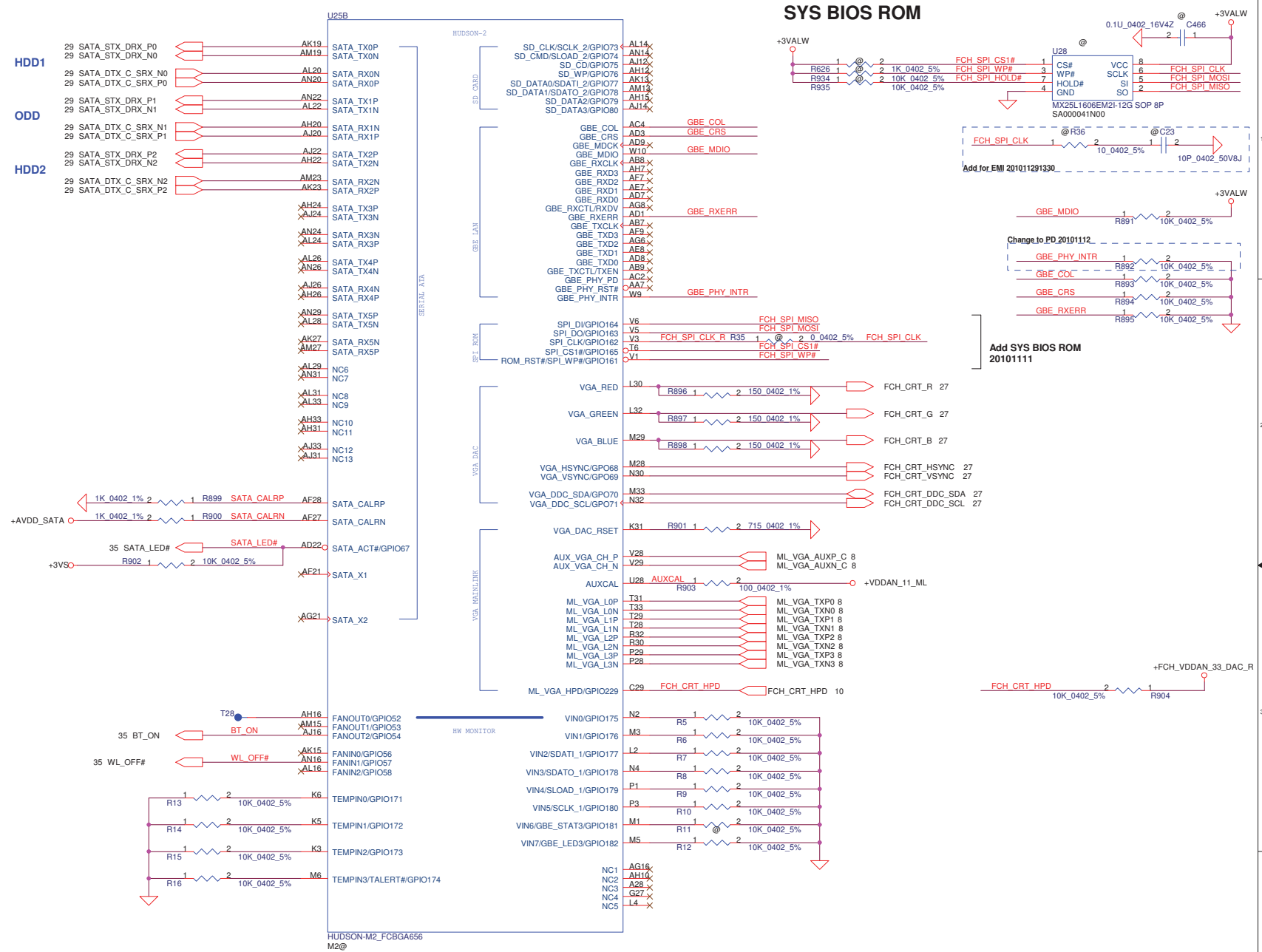
0: MLDAC power on
1: MLDAC power off



Project SKU ID	L(N)O	H(Y)ES
GPIO189 (use VGA)	R44	R45
GPIO190 (use PX)	R46	R45
GPIO191	R48	R47

Add Project ID Table
201011301600

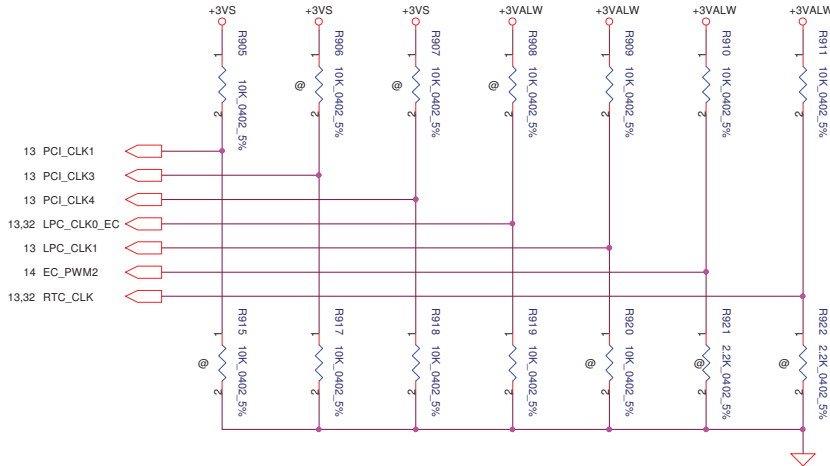
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/04	Deciphered Date	2010/08/04	Title
				Hudson-M2/M3-ACPI/USB/EC
				Document Number
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STRAP PINS

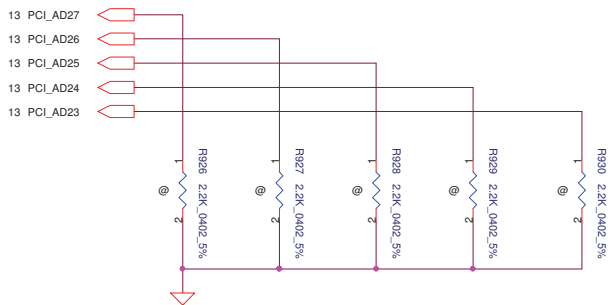
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED



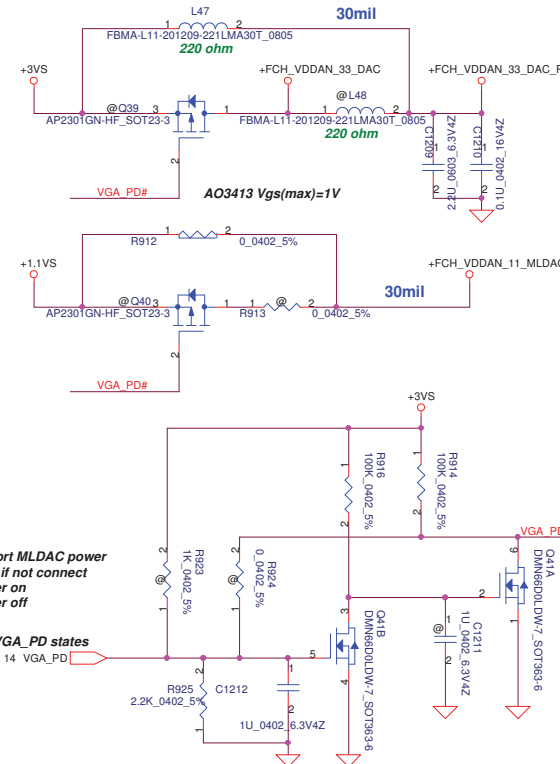
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

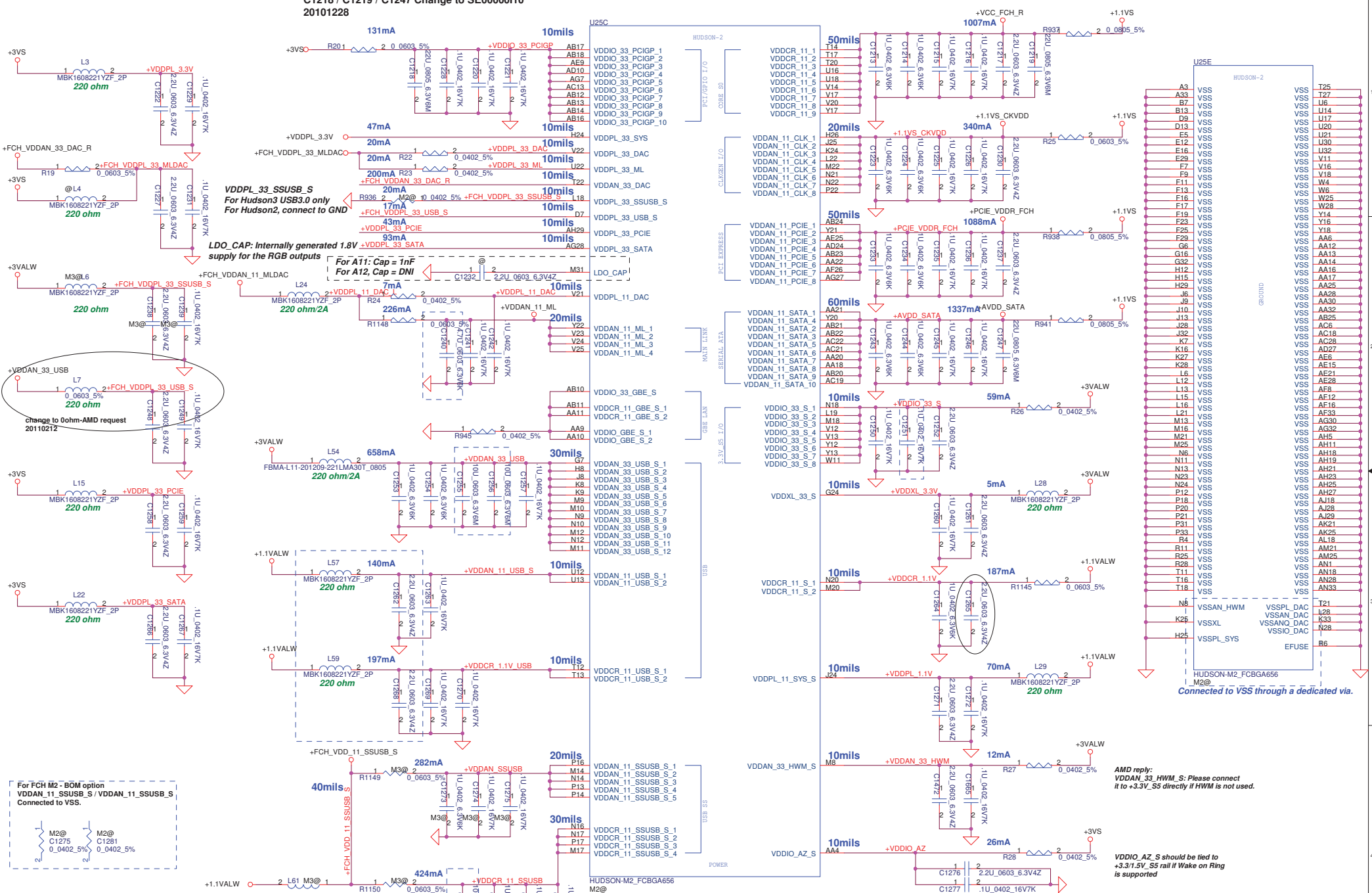
PCI_AD26	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS DEFAULT



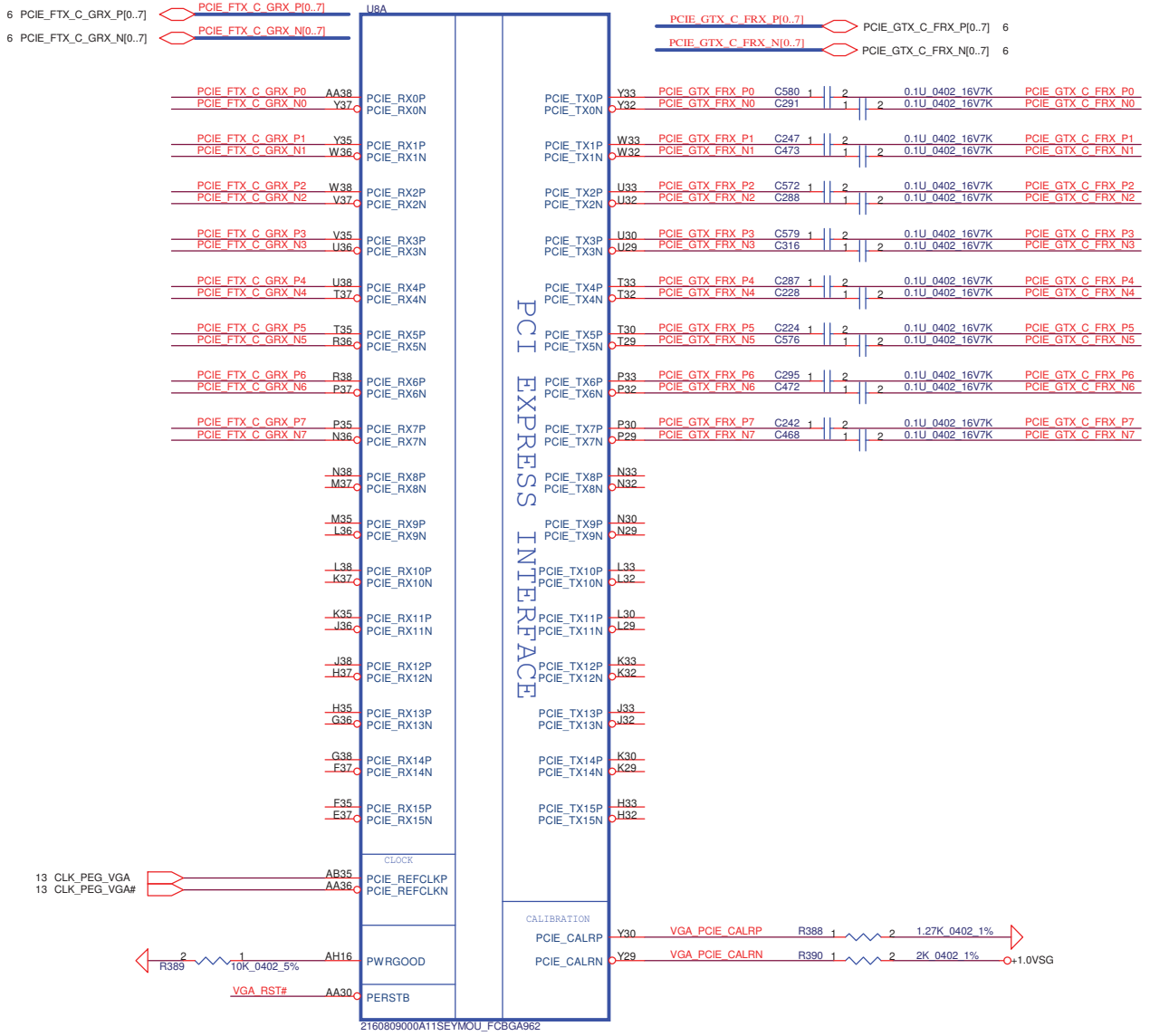
If support ML DAC power down when no VGA plug



C1218 / C1219 / C1247 Change to SE00000110
20101228

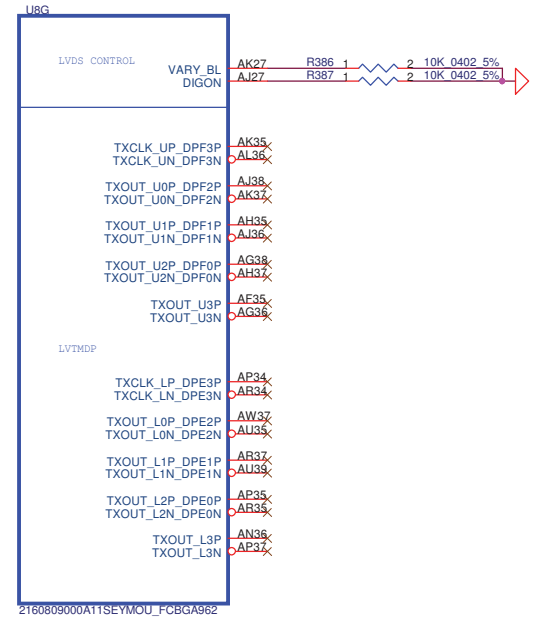


GFX PCIE LANE REVERSAL

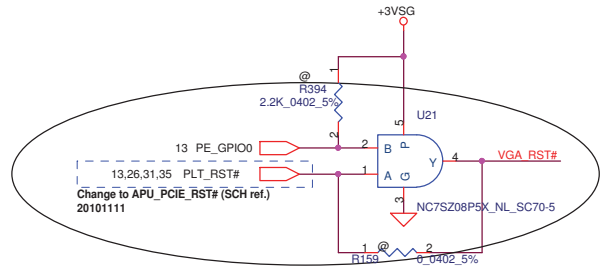


<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need



For UMA Mux.



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Strap Name	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPIO13,12,11 (config 2,1,0) : (Internal PD) a) If BIOS_ROM_EN = 1, then Config[2:0] defines the BIOS ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	memory apertures 128 MB 000 256 MB 001 * 64 MB 010
CONFIG[1]		
CONFIG[0]		
BIOS_ROM_EN	Enable external BIOS ROM device (Internal PD) 0: Diabie, 1: Enable	0
AUD[1]	00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
AUD[0]		
BIF_GEN2_EN	1= Advertises the PCIe device as 2.5 GT/s capable at power-on 1= Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

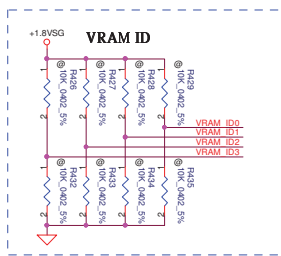
NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Strap Name	Pin Straps description <all internal PD>	Setting
VRAM_ID0	VRAM ID0	0
VRAM_ID1	VRAM ID1	0
VRAM_ID2	VRAM ID2	0
VRAM_ID3	VRAM ID3	0



GPIO5 fast-power reduction: HW control will cause display disturb should use SW method control
GPIO6 voltage control signal, No use can NC!

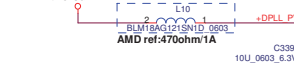
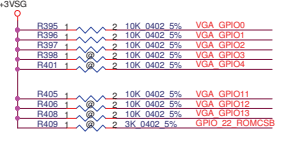
GPIO7 Controls backlight on/off. Active High, need external PD
If GPIO22 High, GPIO 11-13 -> CFG[0:2] Config ROM type, GPU has internal PD

GPIO6,15,16,20 Voltage control signal, GPIO15 no use can NC
Thermal monitor interrupt
Critical temperature fault

Reserved

External BIOS device ON(1)/OFF(0) Inter PD

Internal Debug no use can NC
no use can NC
no use can NC
Stereo Sync no use can NC
For ATI Cross fire no use can NC



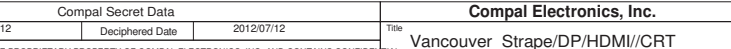
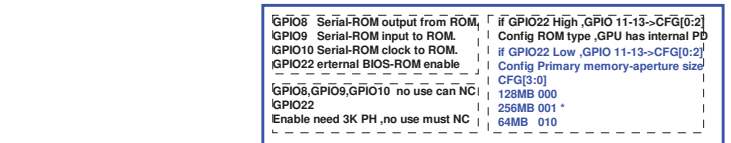
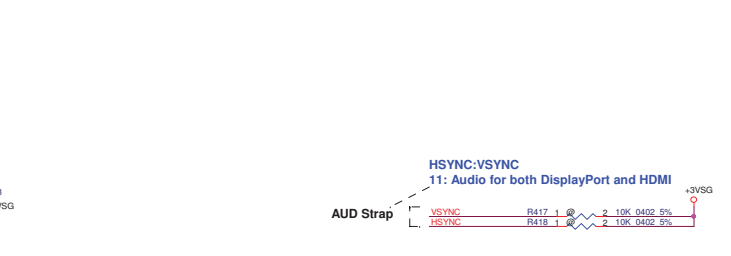
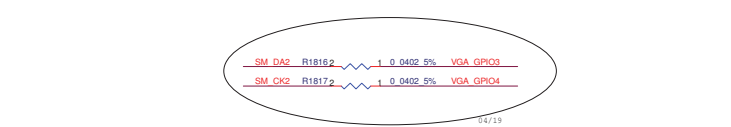
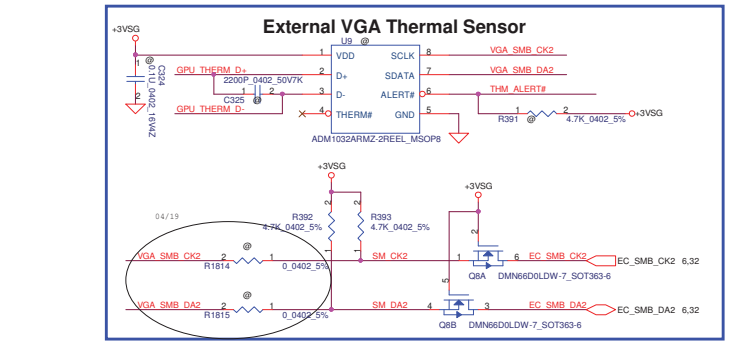
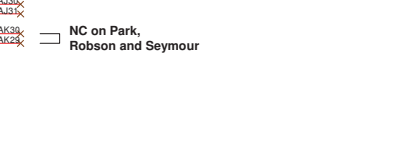
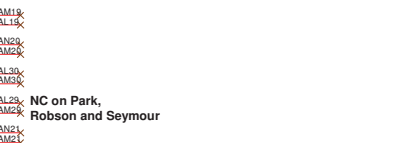
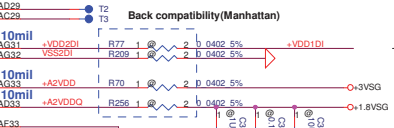
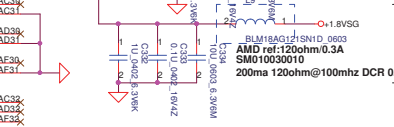
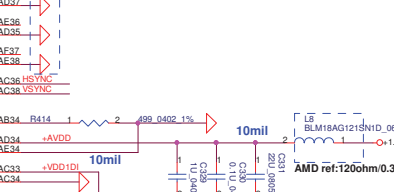
Seymour(XT)

VRAM	Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung BA0004630 64M16 K4W1G1646G-BC11		0	0	0	0
Samsung BA000470A0 128M16 K4W2G1646G-BC11		0	0	0	1
Hynix BA000419S60 64M16 H5TQ1G63DFR-11C		0	1	0	0
Hynix BA00033030 128M16 H5TQ2G63BFR-11C		0	1	0	1

Strap Name	Pin Straps description <all internal PD>	Setting
TXCAP_DPA3P	TXCAP_DPA3P	0
TXCAM_DPA3P	TXCAM_DPA3P	0
TXP_DP_A2P	TXP_DP_A2P	0
TXM_DP_A2P	TXM_DP_A2P	0
TX1P_DPA1P	TX1P_DPA1P	0
TX1M_DPA1P	TX1M_DPA1P	0
TX2P_DPA2P	TX2P_DPA2P	0
TX2M_DPA2P	TX2M_DPA2P	0
TXCBP_DPB3P	TXCBP_DPB3P	0
TXCBM_DPB3P	TXCBM_DPB3P	0
NC_DVPCNK	NC_DVPCNK	0
TX3P_DPB2P	TX3P_DPB2P	0
TX3M_DPB2P	TX3M_DPB2P	0
TX4P_DPB1P	TX4P_DPB1P	0
TX4M_DPB1P	TX4M_DPB1P	0
TX5P_DPB0P	TX5P_DPB0P	0
TX5M_DPB0P	TX5M_DPB0P	0
TX6P_DPC3P	TX6P_DPC3P	0
TX6M_DPC3P	TX6M_DPC3P	0
TX7P_DPC1P	TX7P_DPC1P	0
TX7M_DPC1P	TX7M_DPC1P	0
TX2P_DPC0P	TX2P_DPC0P	0
TX2M_DPC0P	TX2M_DPC0P	0
NC_TXCP_DPDP2P	NC_TXCP_DPDP2P	0
NC_TXCM_DPDP2P	NC_TXCM_DPDP2P	0
NC_TXSP_DPDP0P	NC_TXSP_DPDP0P	0
NC_TXSM_DPDP0P	NC_TXSM_DPDP0P	0

NC on Park, Robson and Seymour

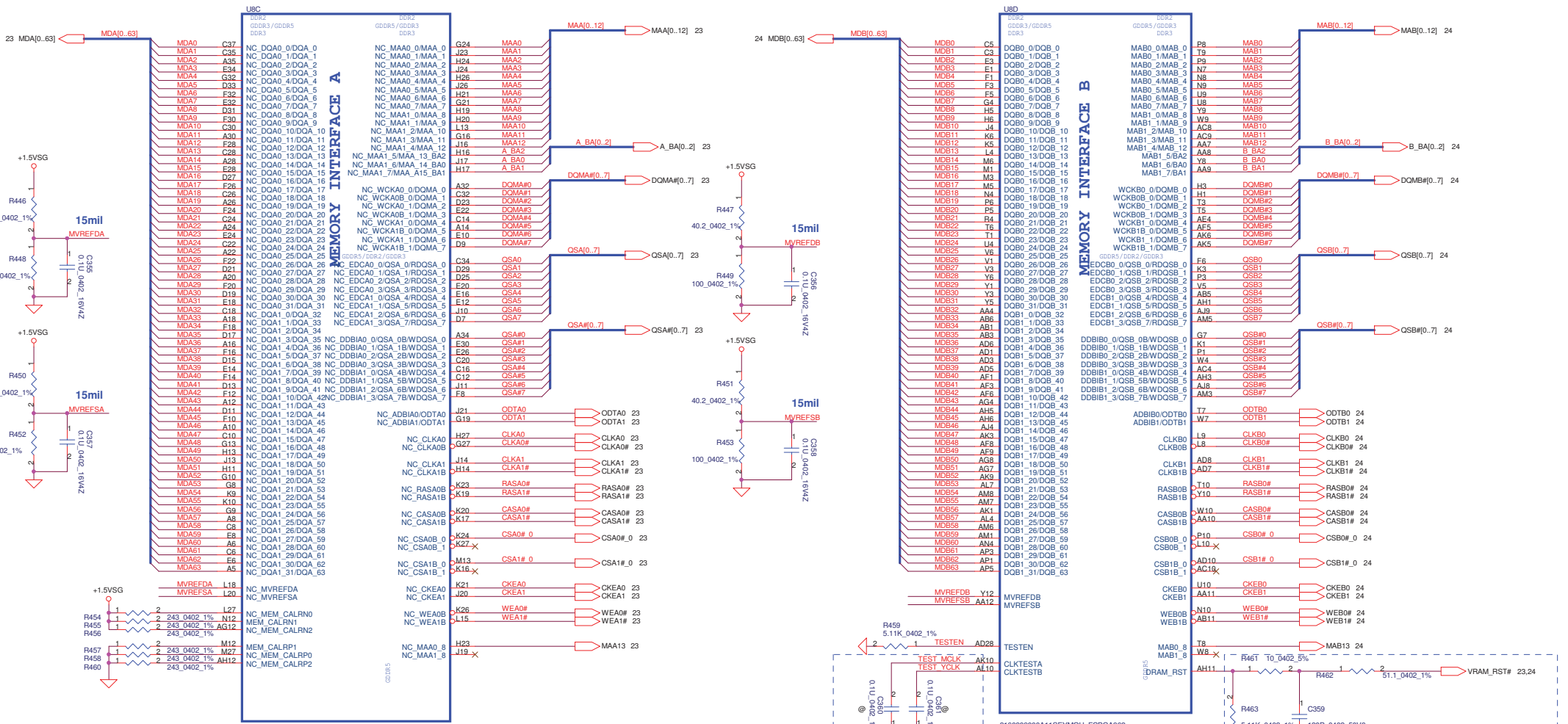
Not share via for other GND



GPIO8 Serial-ROM output from ROM, GPIO9 Serial-ROM input to ROM, GPIO22 Low, GPIO 11-13 -> CFG[0:2] GPIO22 external BIOS-ROM enable

GPIO8, GPIO9, GPIO10 no use can NC
GPIO22 Enable need 3K PH, no use must NC

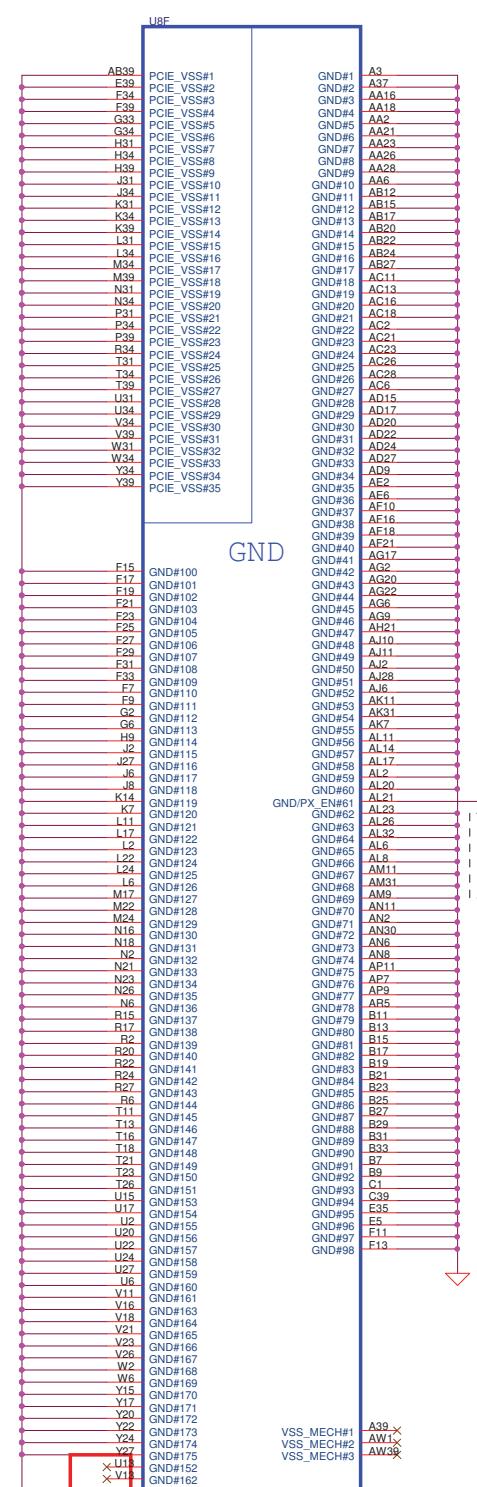
If GPIO22 High, GPIO 11-13 -> CFG[0:2] Config ROM type, GPU has internal PD
If GPIO22 Low, GPIO 11-13 -> CFG[0:2] Config Primary memory-aperture size CFG[3:0] 128MB 000 256MB 001 * 64MB 010



Note:
route 50ohms single-ended
and 100ohms diff
and keep short
REF137-03 suggest

Park&Seymour is single channel for memory (channel B only)

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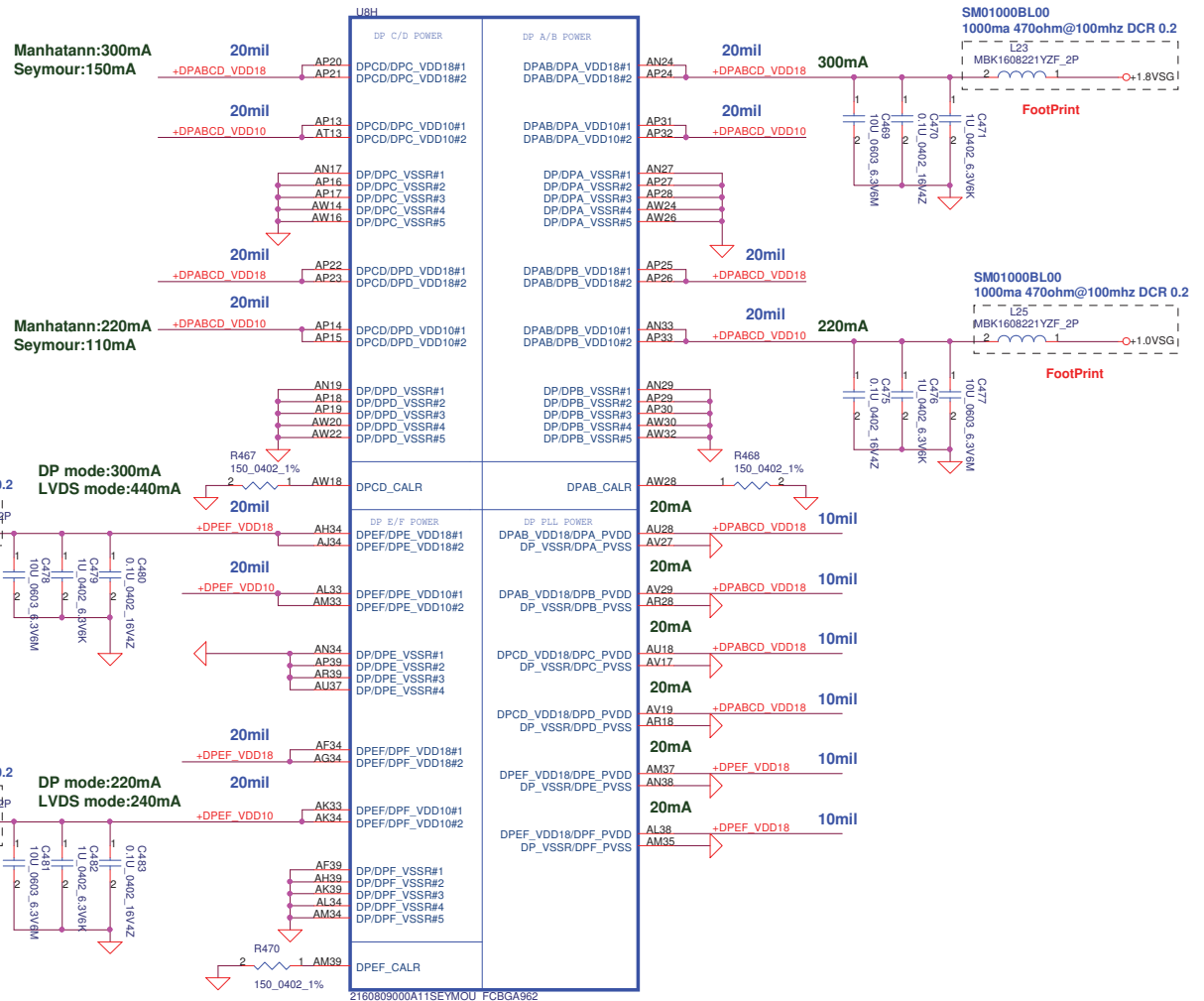


DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
 can combian to DPAB_VDD18
 DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
 can combian to DPCD_VDD18
 (DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
 DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
 can combian to DPEF_VDD18

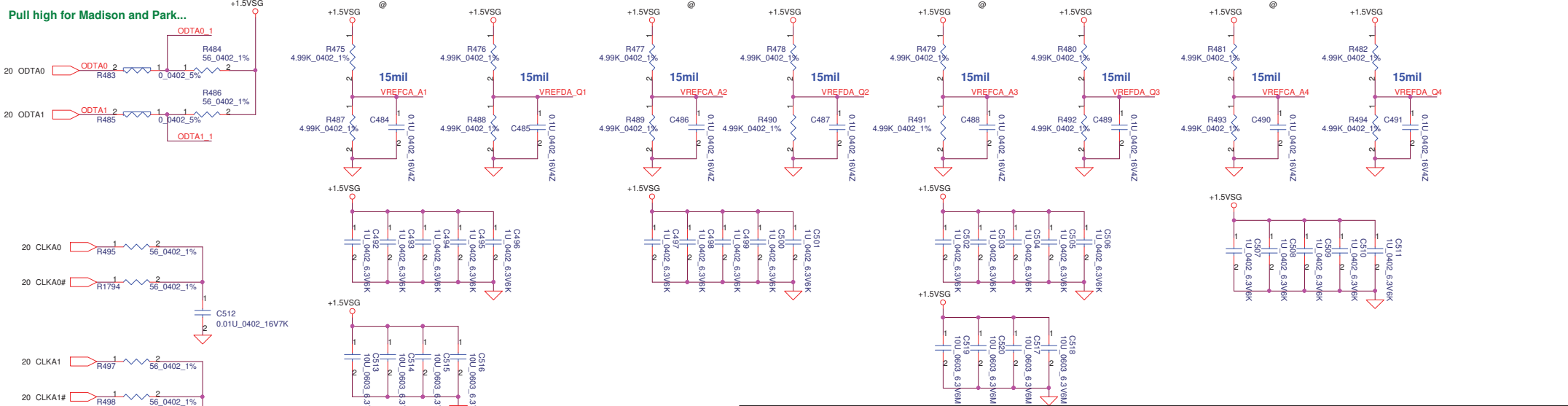
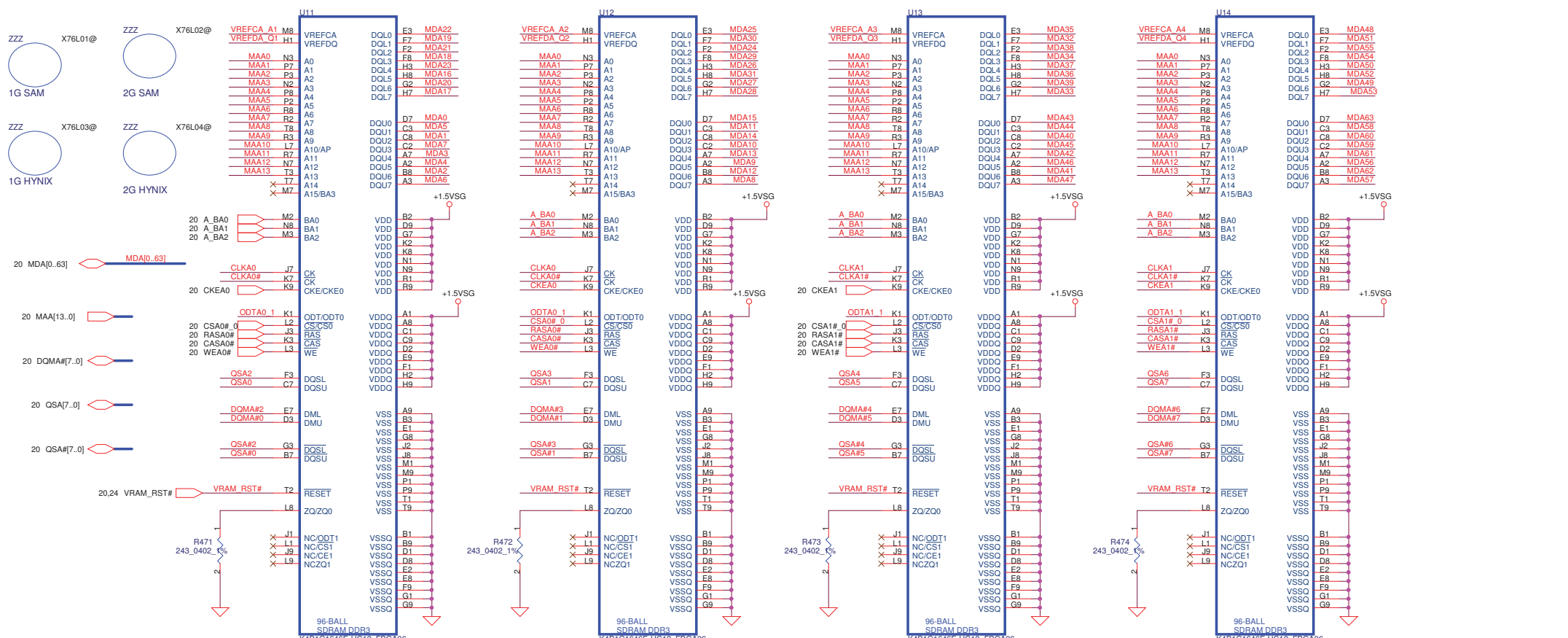
Seymour/Whistler :
 DPA_VDD10,DPB_VDD10
 can combian to DPAB_VDD10
 DPC_VDD10,DPD_VDD10
 can combian to DPCD_VDD10
 DPE_VDD10,DPD_VDD10
 can combian to DPEF_VDD10

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
 (Manhatann should have individual GND)
 where x is A,B,C,D,E,F

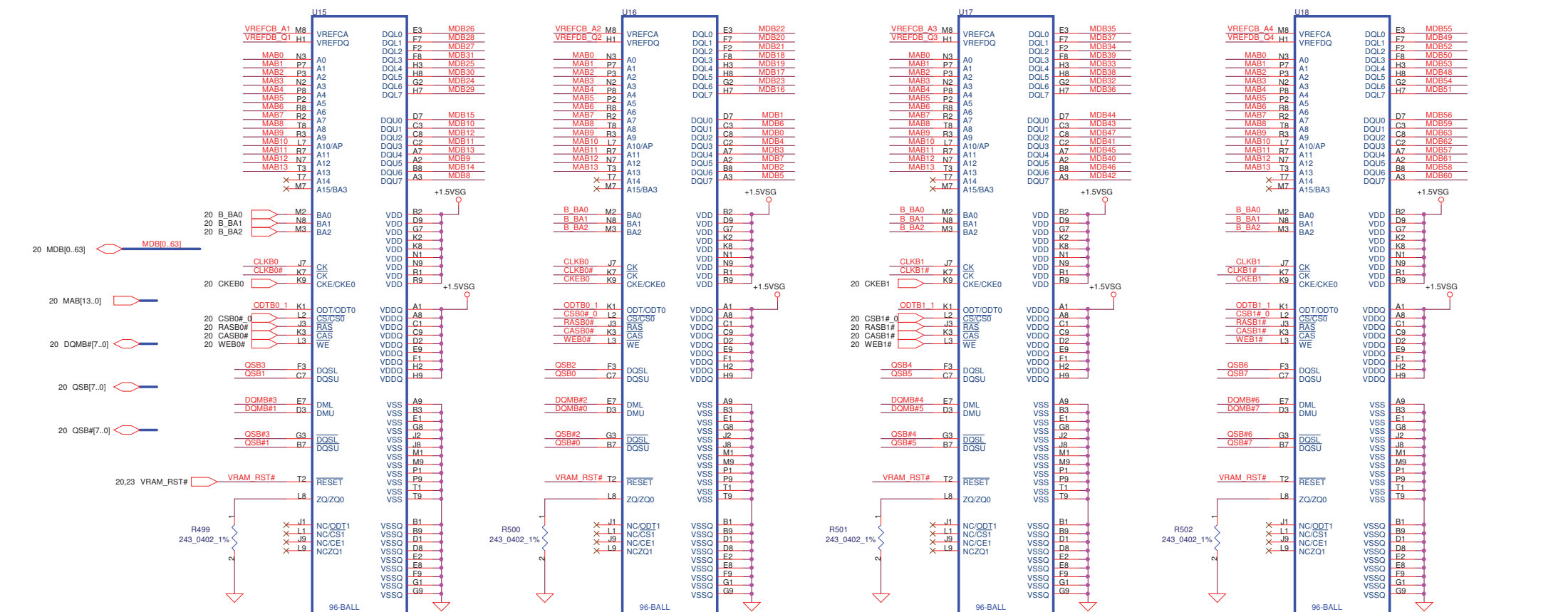
Park/Madison :AL21:left NC
 Seymour/Whistler:
 AL21:PX_EN
 use to control discreate GPU regulators
 for power express BACO mode
 Support BACO:
 output High3.3V:turn off regulators (BACO mode on)
 output Low0V:turn on regulators (BACO mode off)
 need PD resistor
 No support BACO:
 left NC



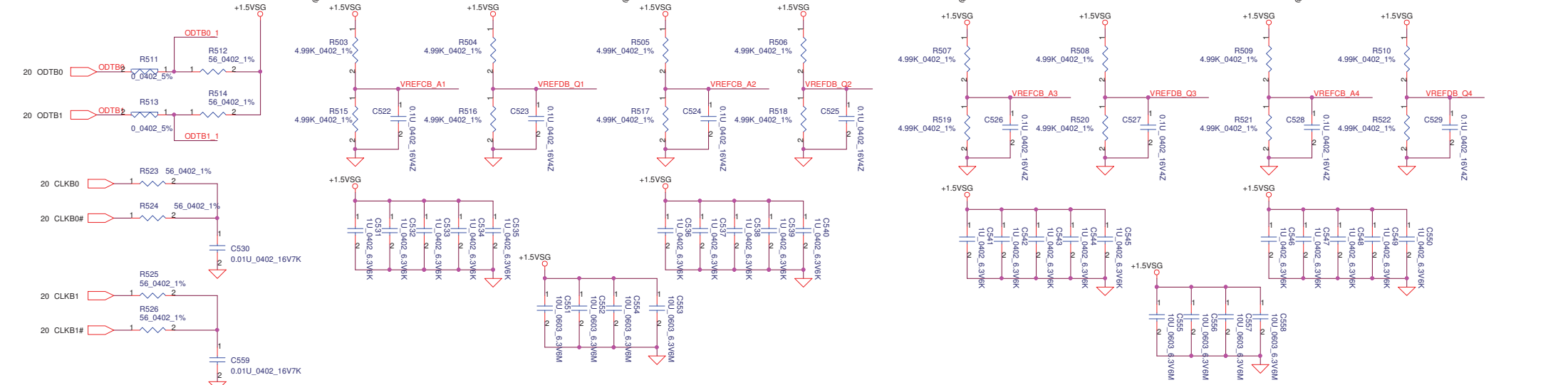
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Issued Date	2010/07/12	Deciphered Date	2012/07/12	VRAM DDR3 / Channel A	
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				QBL70 LA-7553P	0.22
				Date: Friday, April 29, 2011	Sheet 23 of 51

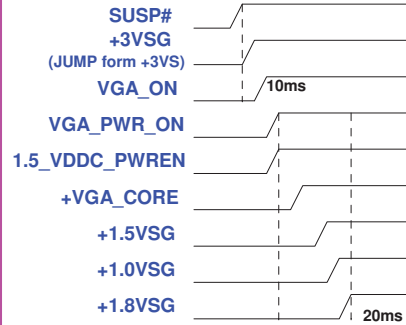


Pull high for Madison and Park...

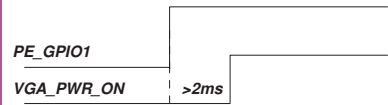


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Issued Date	2010/07/12	Deciphered Date	2012/07/12	Title	VRAM_DDR3 / Channel B
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Date:	Friday, April 29, 2011	Sheet	24	of	51

Power Sequence of Whistler and Seymour



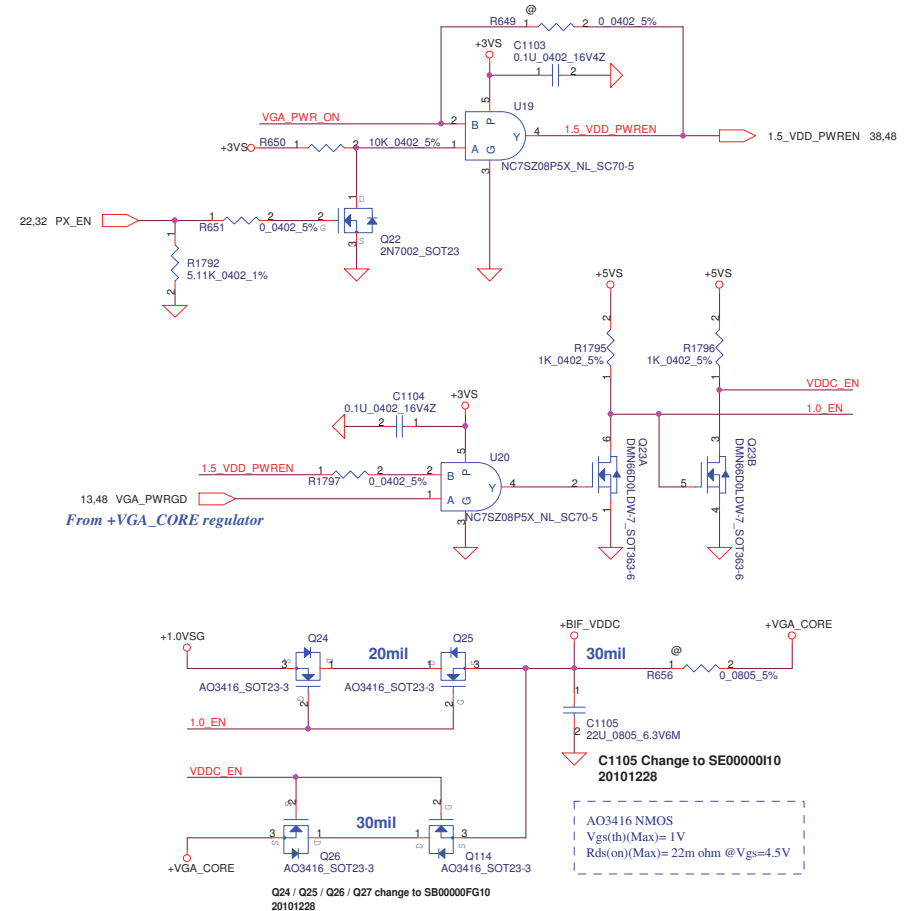
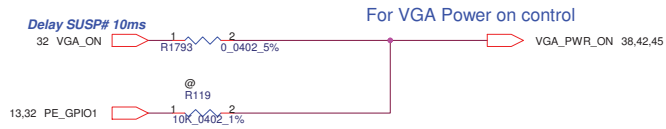
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON



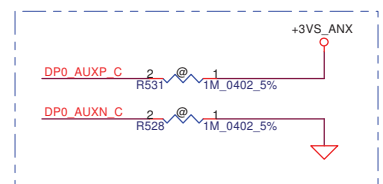
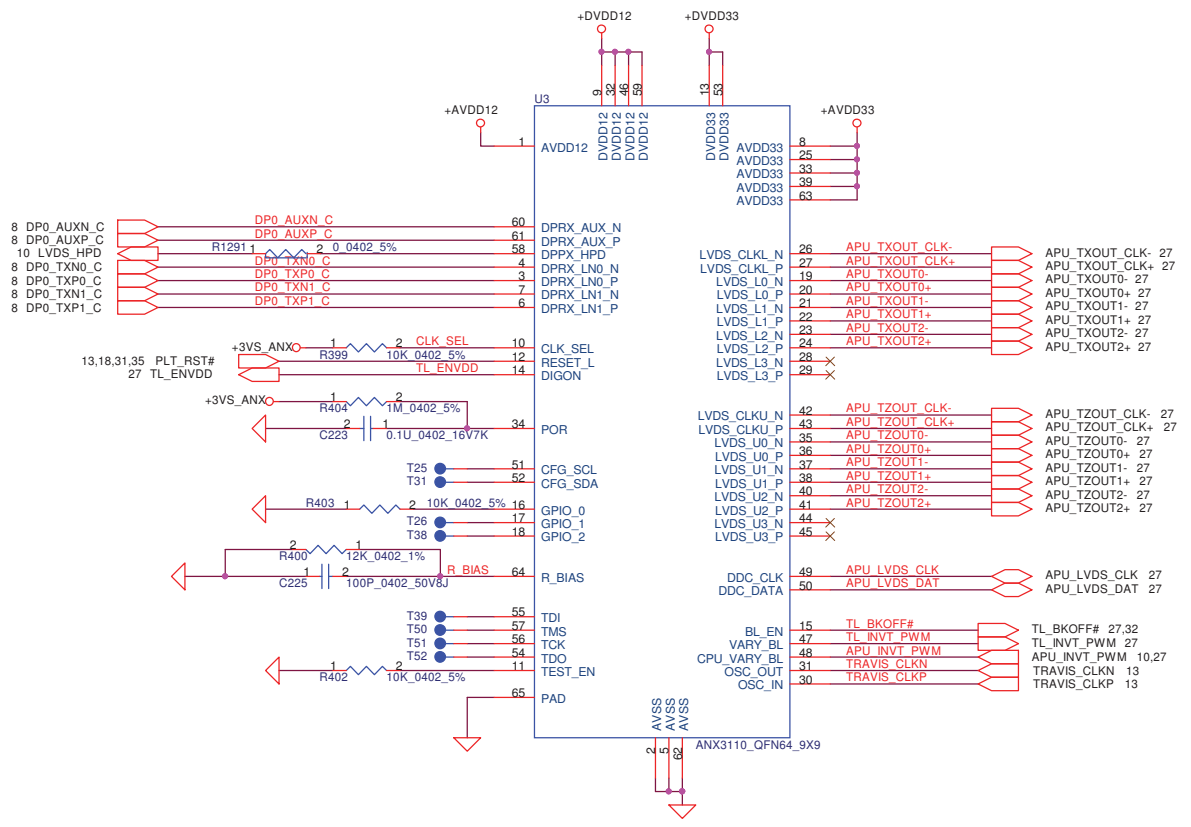
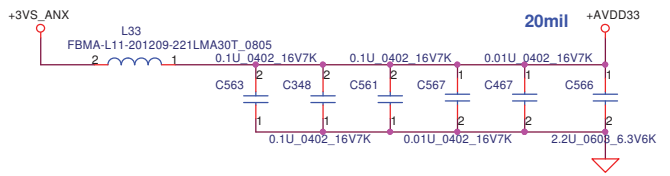
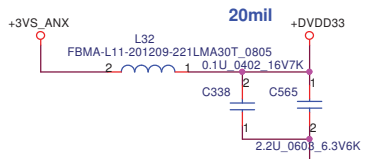
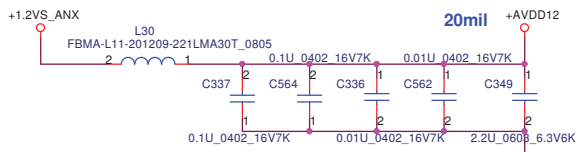
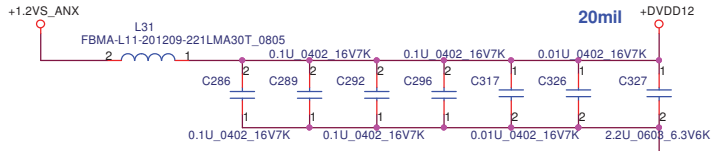
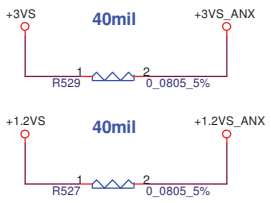
VGA Muxless with BACO Status Mapping table

	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

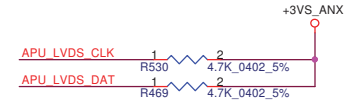
VGA Power Enable Signal Mapping table	
VGA_PWR_ON source signal	Whistler
+3.3VSG	VGA_ON
+1.8VSG	SUSP#
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN



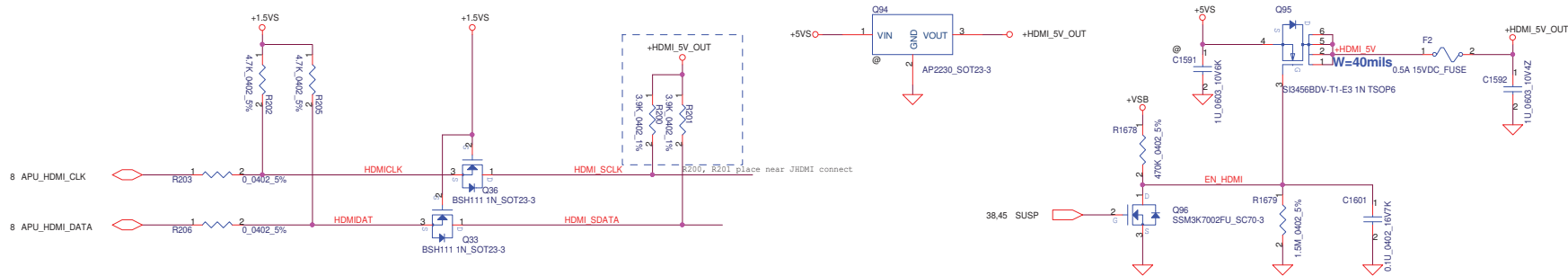
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Issued Date	2010/08/04	Deciphered Date	2010/08/04	Title				VGA power sequence and BACO					
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Place via on each trace bus and let resistor very close the via

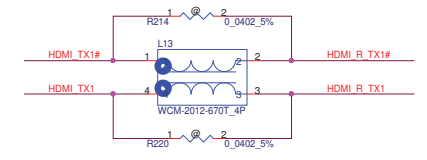
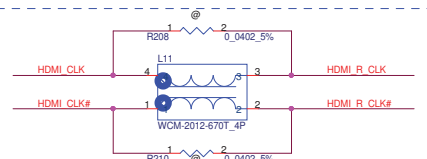
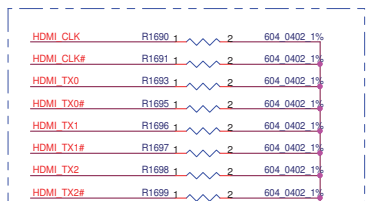
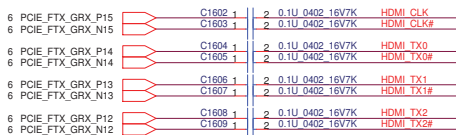


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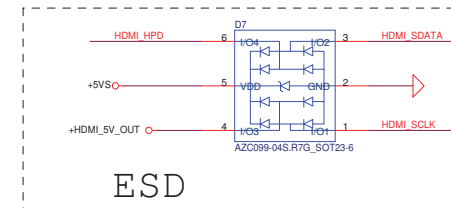
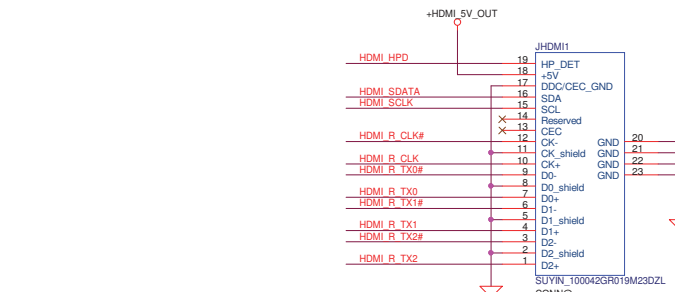
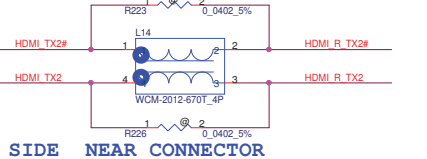


5V PULL UP IN CONNECTOR SIDE

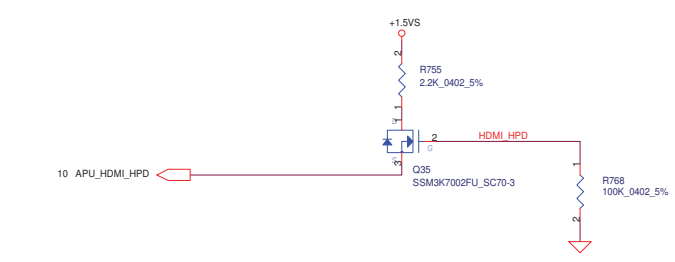
Near the connector



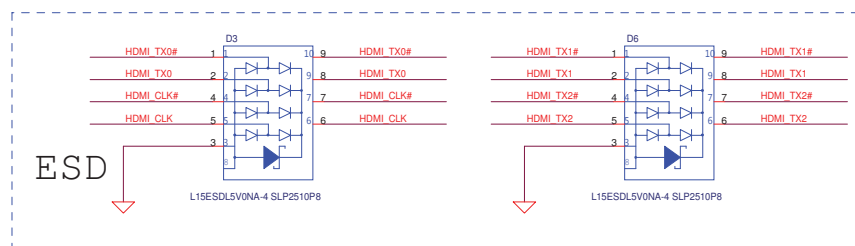
BOT_SIDE_NEAR_CONNECTOR



ESD



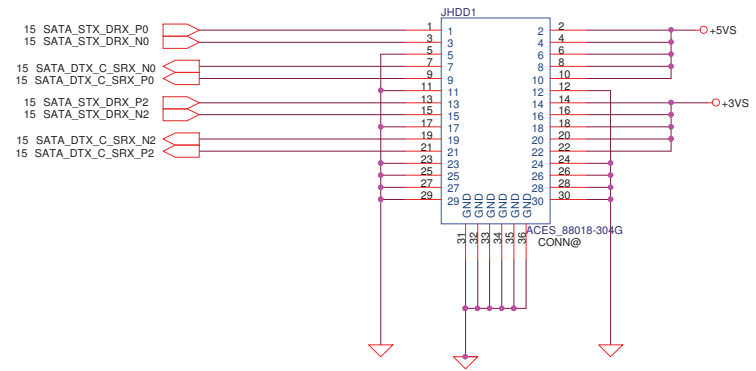
From APU



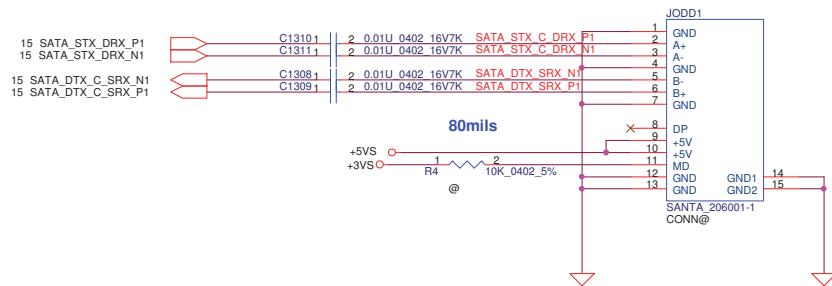
ESD

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				Document Number
				QBL70 LA-7553P
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				0.22
				Date
				Friday, April 29, 2011
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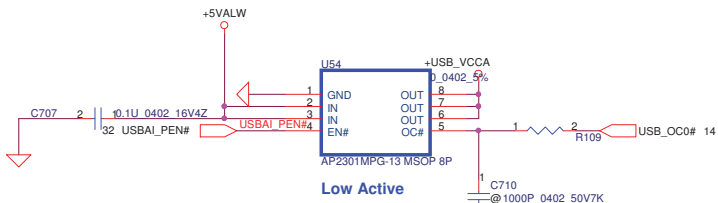
SATA HDD BTB Conn.



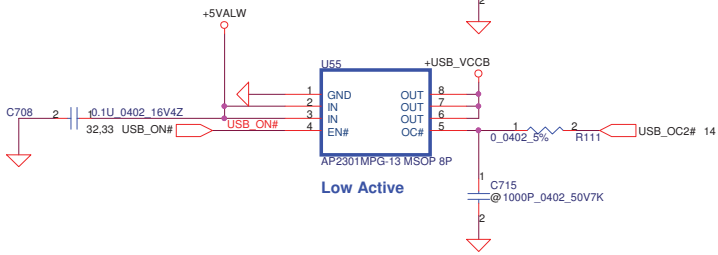
SATA ODD FFC Conn.



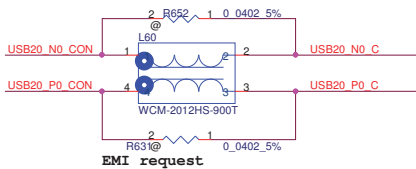
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Issued Date	2010/08/20	Deciphered Date	2012/06/30	P28-HDD & ODD CONN
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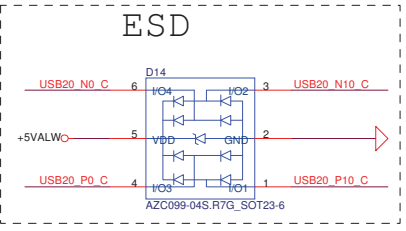
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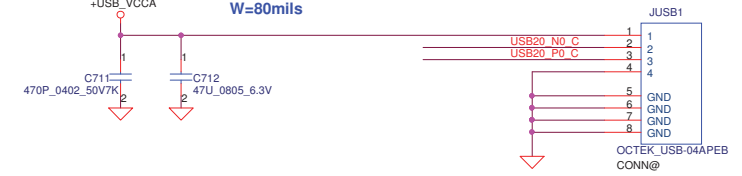
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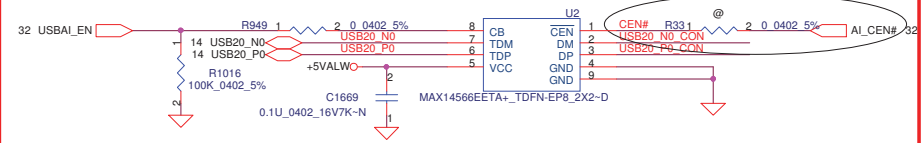
ESD



Left USB Conn.

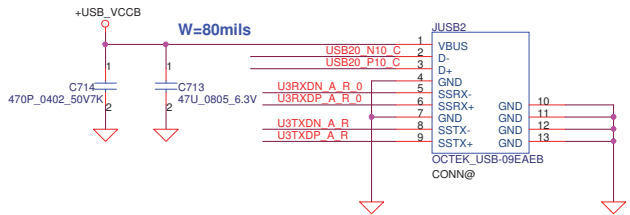
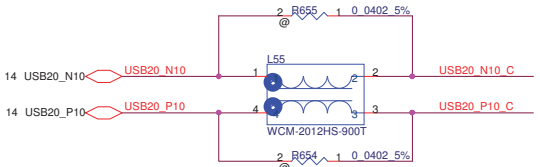
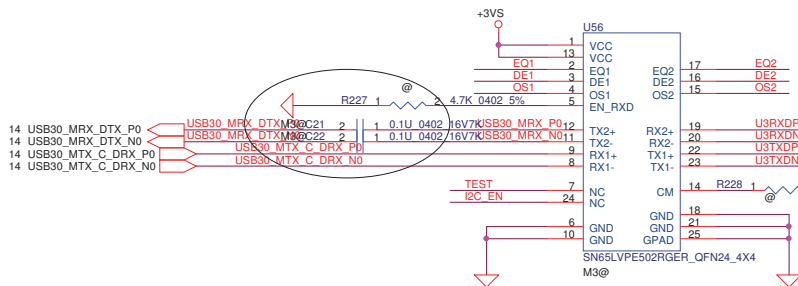


AI CHARGER

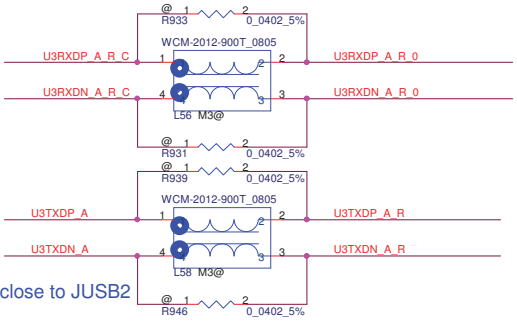
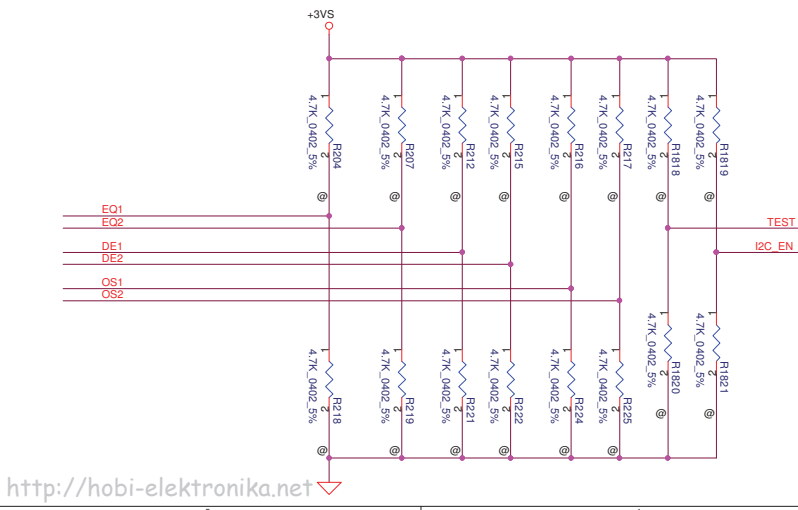
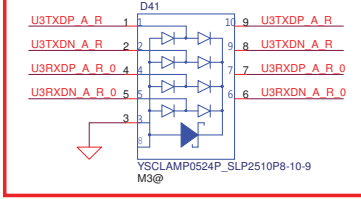


- CB=0 Auto detection charger identification active
- CB=1 Connect DP/DM to TDP/TDM

USB REDRIVER

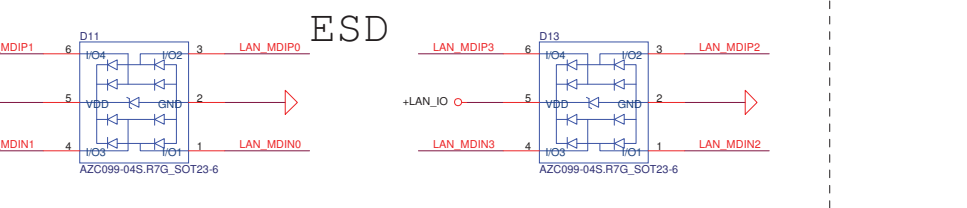
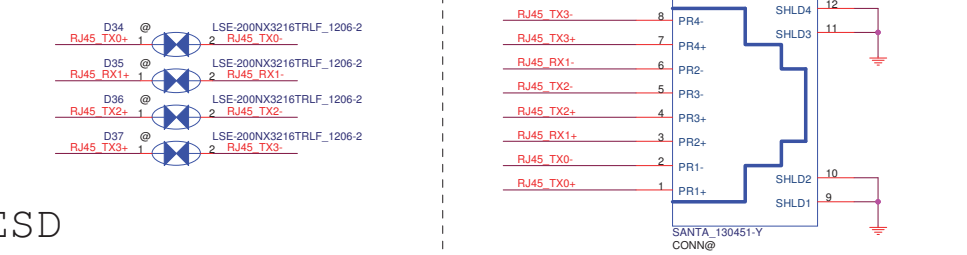
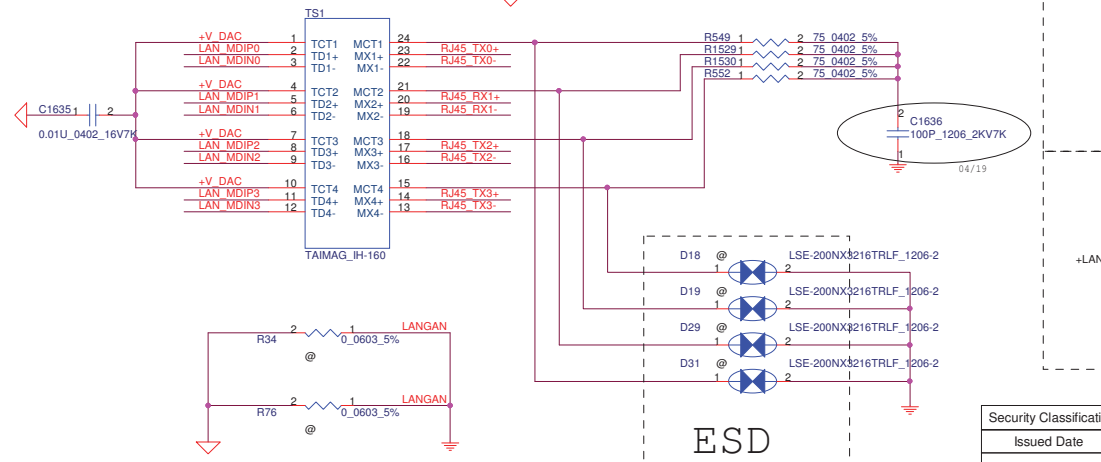
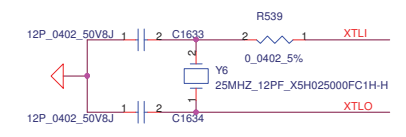
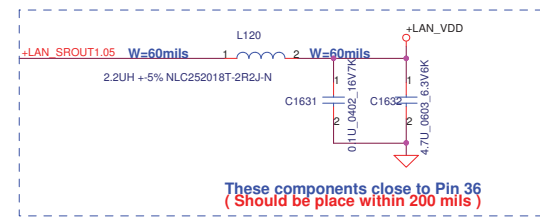
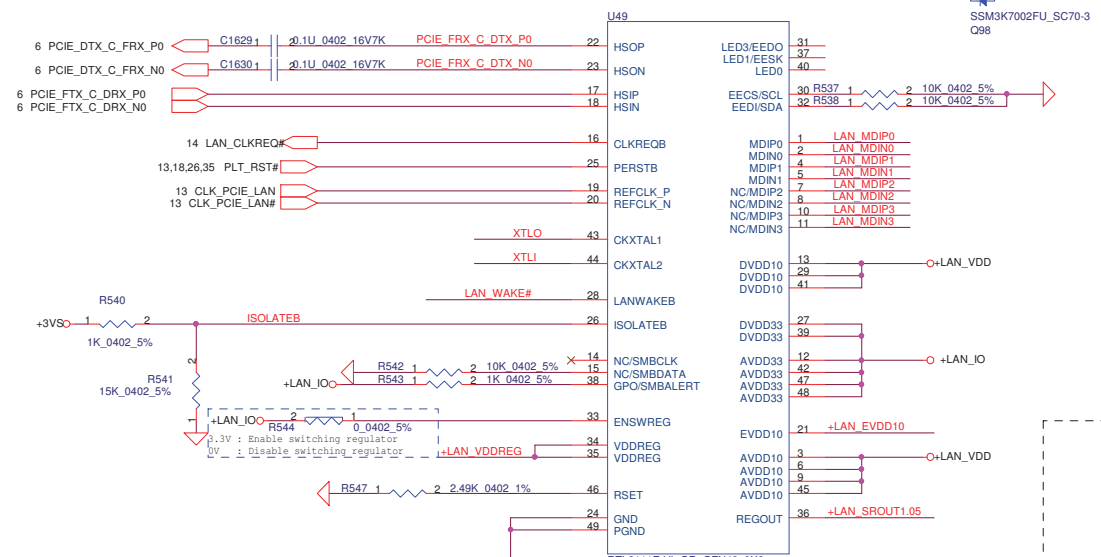
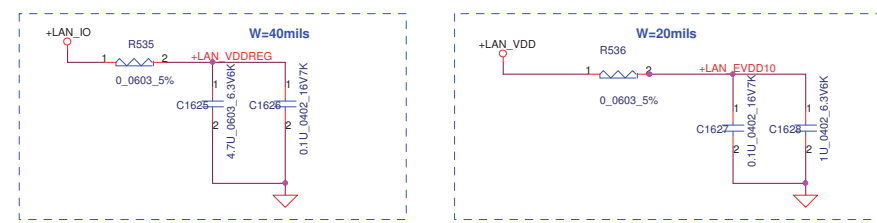
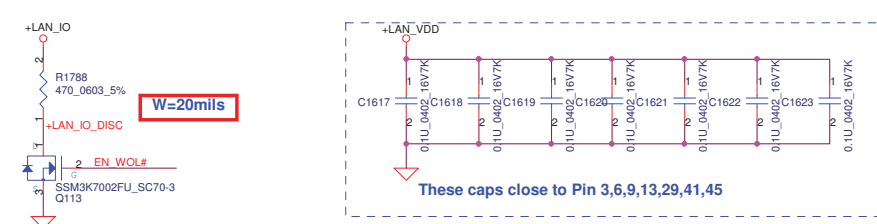
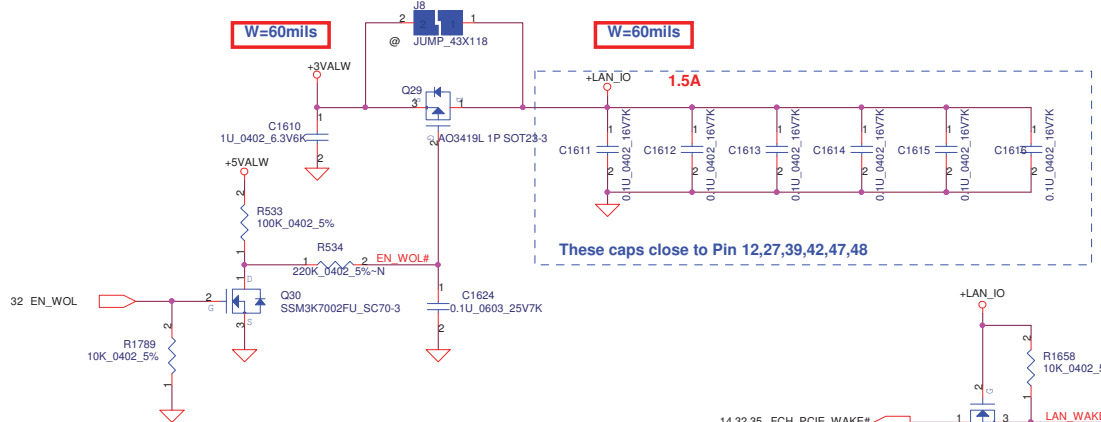


For USB3.0 ESD diode

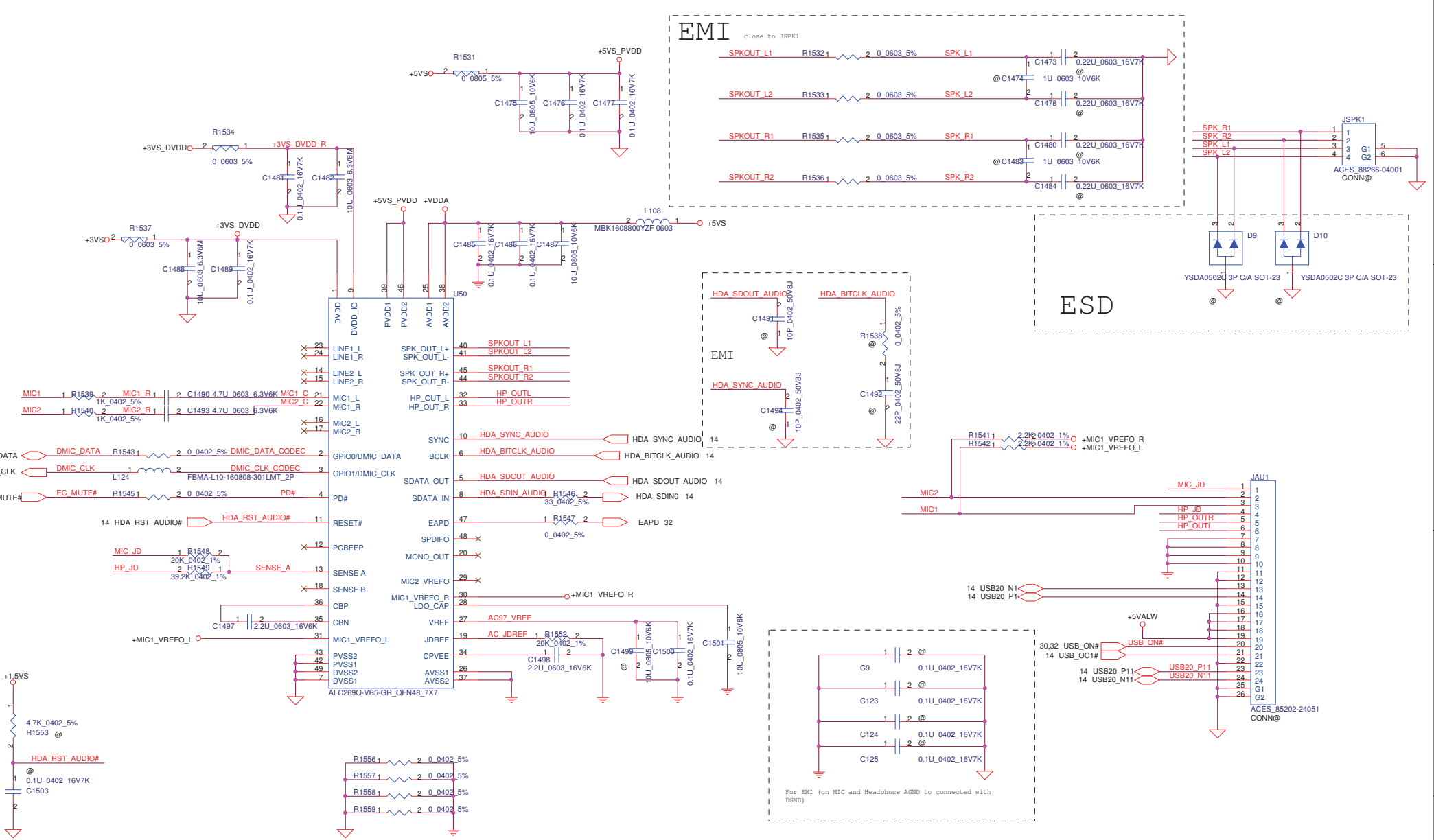


must to close to JUSB2

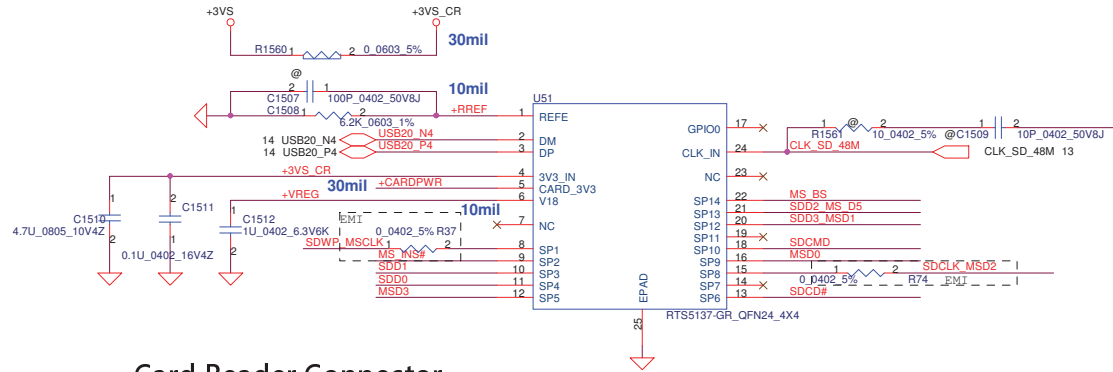
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Issued Date	2010/08/20	Deciphered Date	2012/06/30	Title
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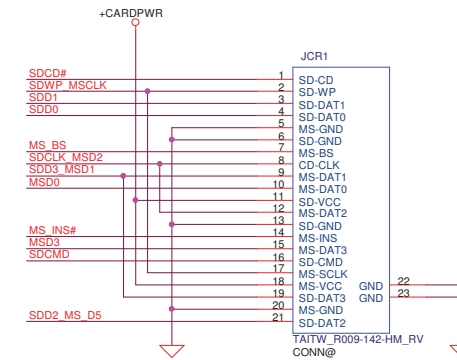
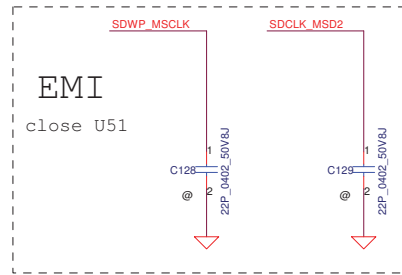
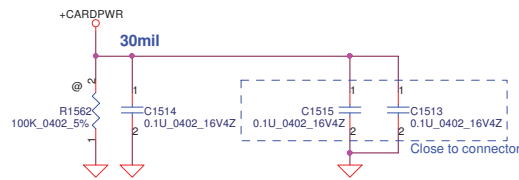
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Card Reader RTS5137 (only SD/MMC/MS function)



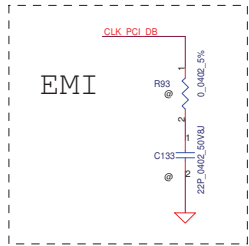
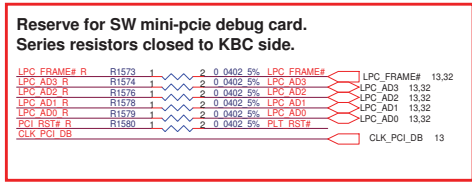
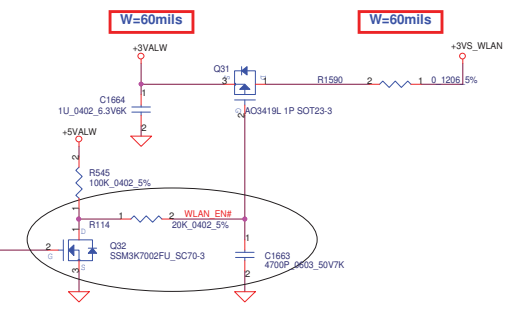
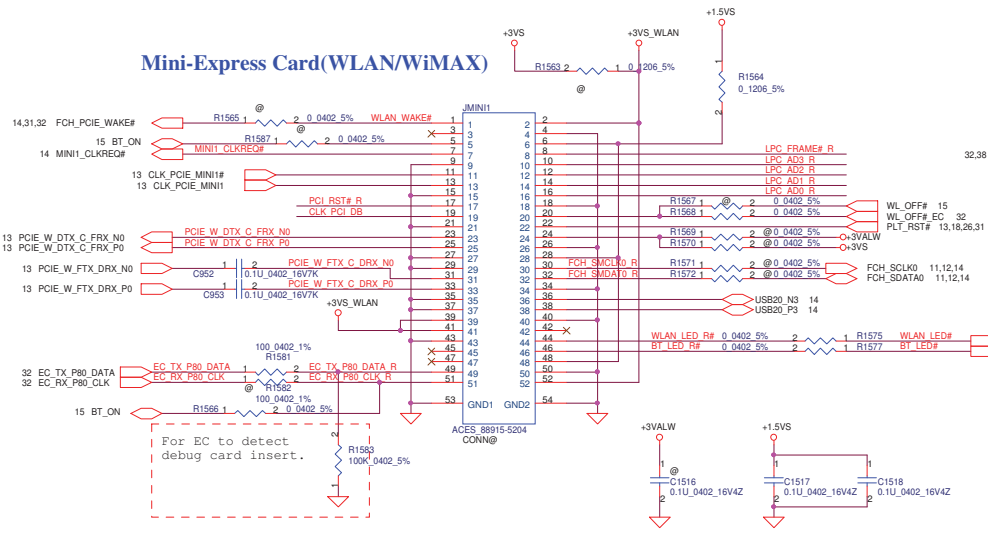
Card Reader Connector



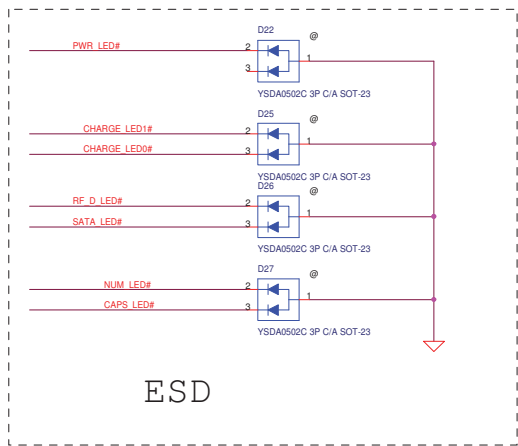
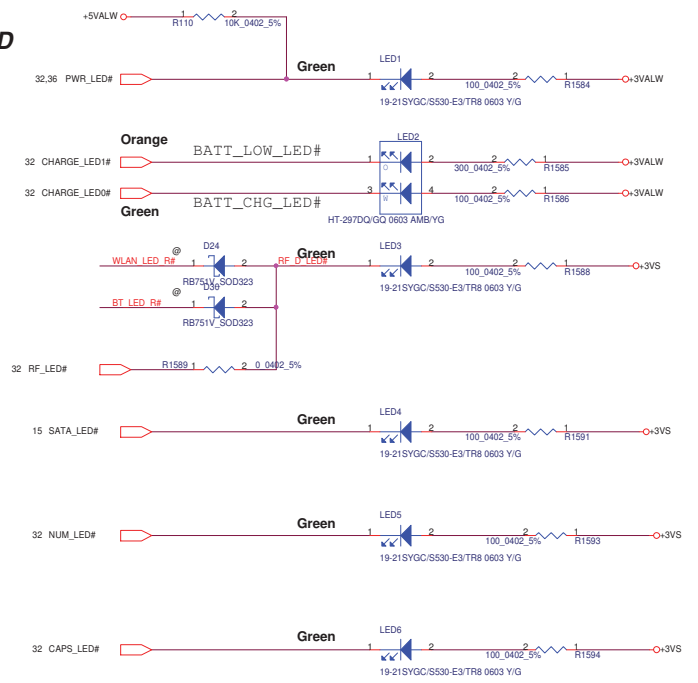
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Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)



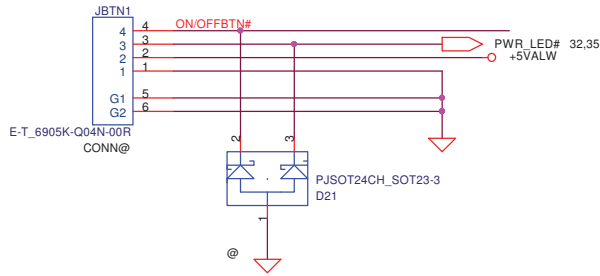
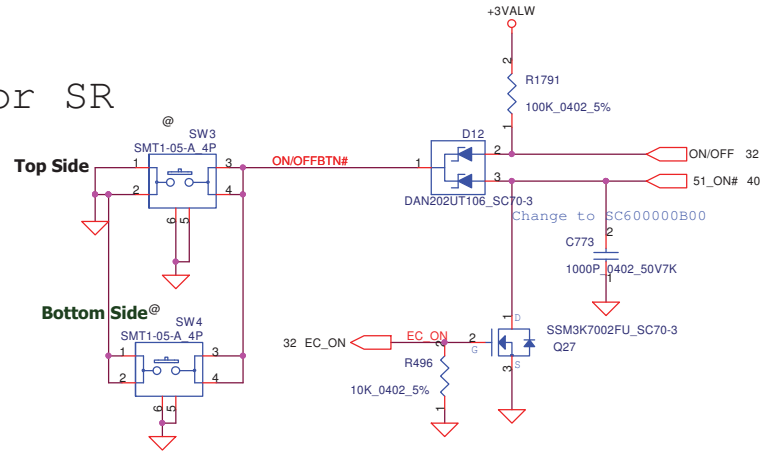
LED



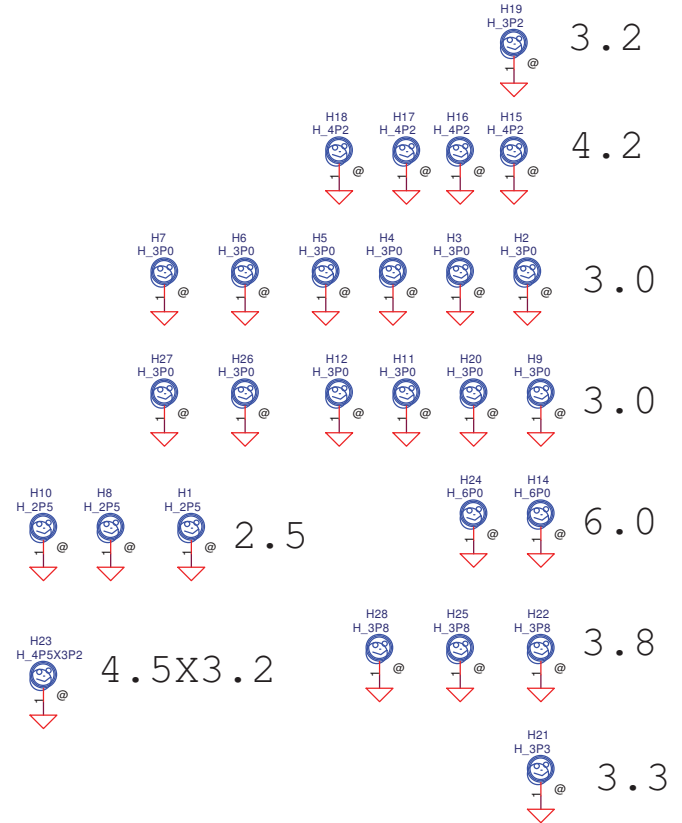
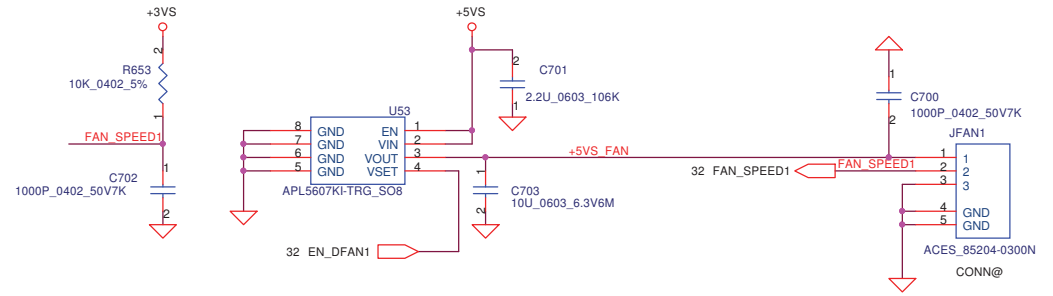
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Issued Date	2010/06/30	Deciphered Date	2012/06/30	P27-Mini PCIe/LED
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ON/OFF switch **Power Button**

For SR



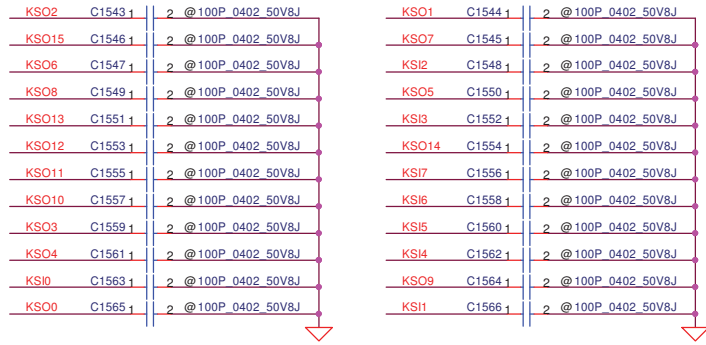
Fan Control Circuit



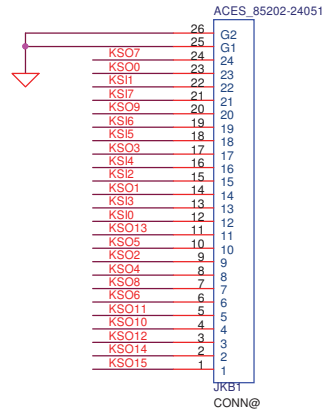
Security Classification	Compal Secret Data		Title	
Issued Date	2010/08/20	Deciphered Date	2012/06/30	P33-Other IO/USB (right)
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				Document Number
				QBL70 LA-7553P
				Rev 0.22
Date: Friday, April 29, 2011		Sheet 36 of 51		

INT_KBD Conn.

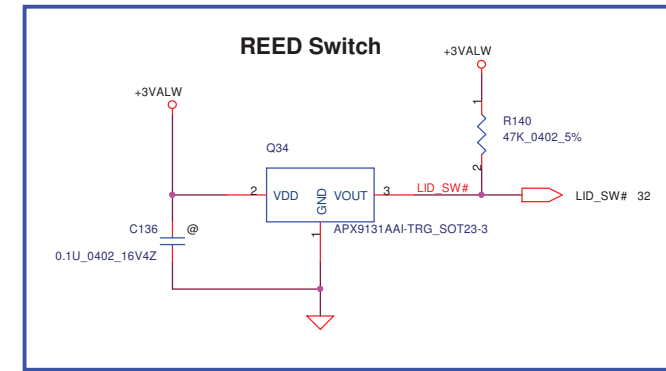
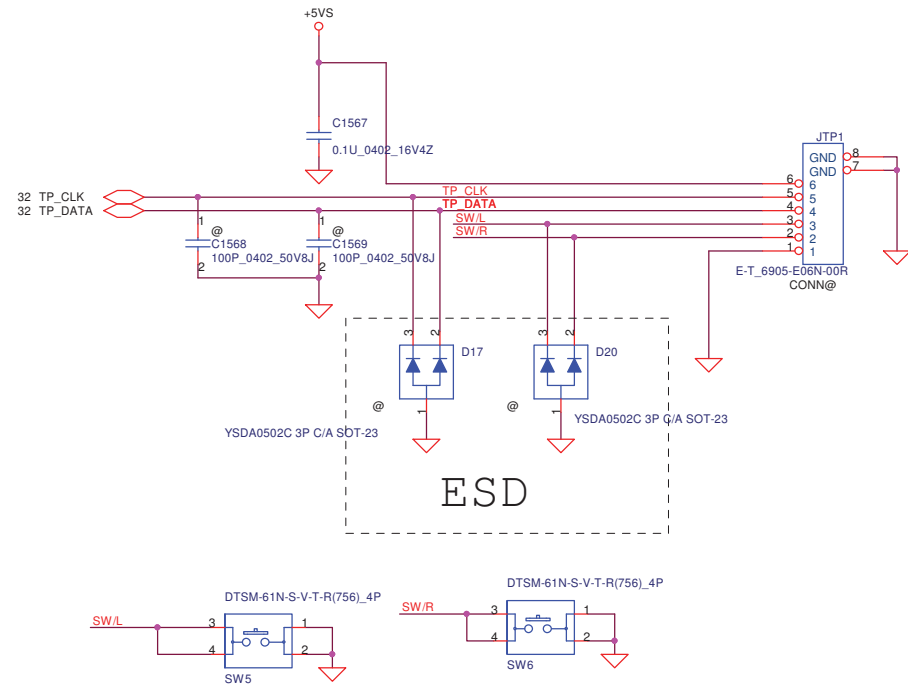
KS[0..7] 32
 KSO[0..15] 32



CONN PIN define need double check

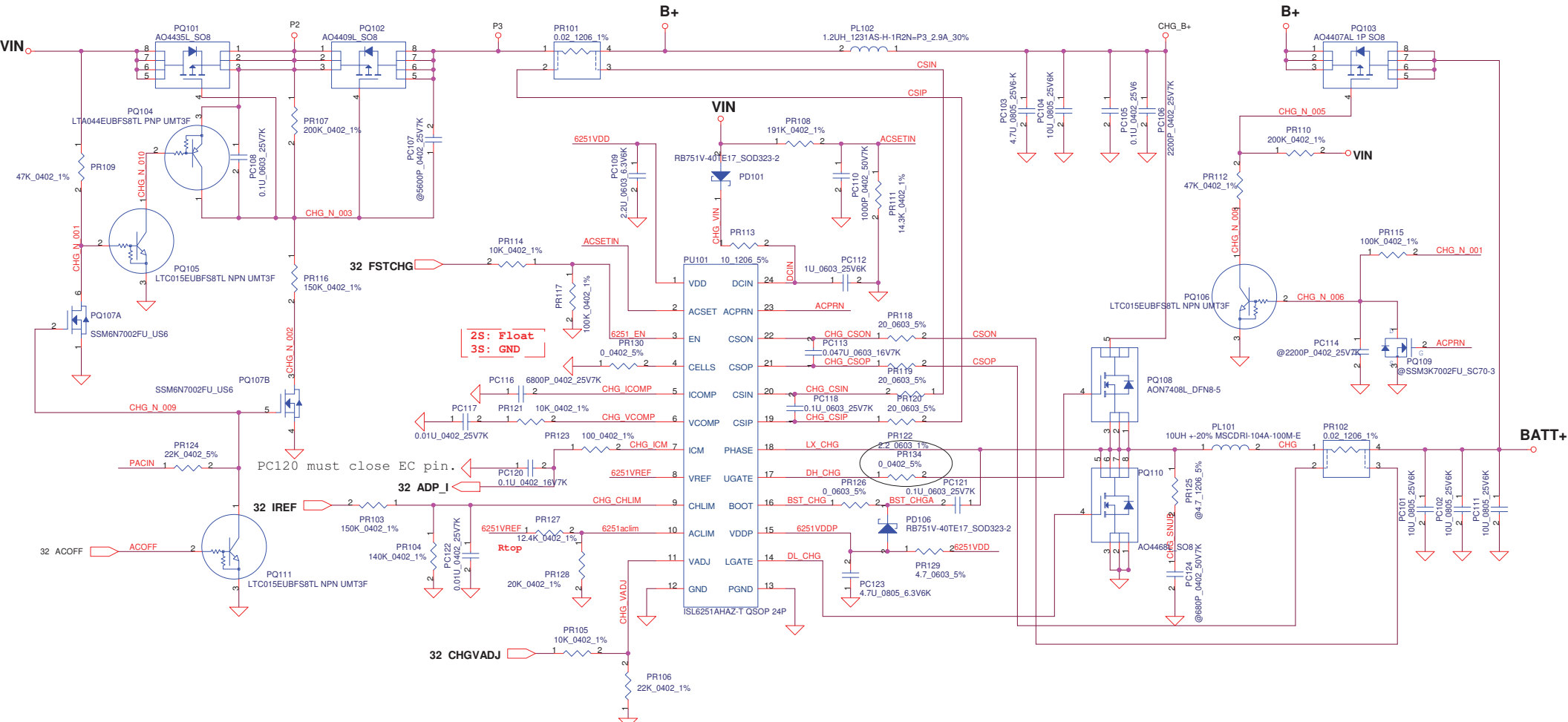


To TP/B Conn.



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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	P30-KB /SW/TP/Lid
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Date:	Friday, April 29, 2011	Sheet	37	of	51

(B+ 6A,240mils ,Via NO.= 12)



2S: Float
3S: GND

32 ADP_I
32 IREF

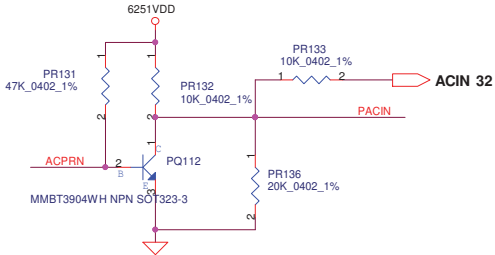
32 CHGVADJ

CP= 85%*Iada;
Iada=0~4.737A (90W); CP=4.03A; where Racdet=0.020ohm, where Rtop=12.4K
90W for Dis: Rtop: SD00000AJ80
Iada=0~3.421A (65W); CP=2.91A; where Racdet=0.020ohm, where Rtop=226K
65W for UMA: Rtop: SD034226380
Astro2010_01_15 need confirm P/N

CP mode
Vaclim=VREF*(Rbot/(Rinternal/(Rtop/(Rinternal+Rbot)/(Rinternal)))
when 90W Vaclim=2.39*(20K/(152K/(20K/(152K+12.4K)/(152K)))=1.44966V
when 65W Vaclim=2.39*(20K/(152K/(20K/(152K+226K)/(152K)))=0.38914V
Iinput=(1/Racdet)*(0.05*Vaclim/VREF+0.05)
when 90W, Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W, Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

CC=0.25A-3A
IREF=1.016*Icharge
IREF=0.254V-3.048V
VCHLIM need over 95mV

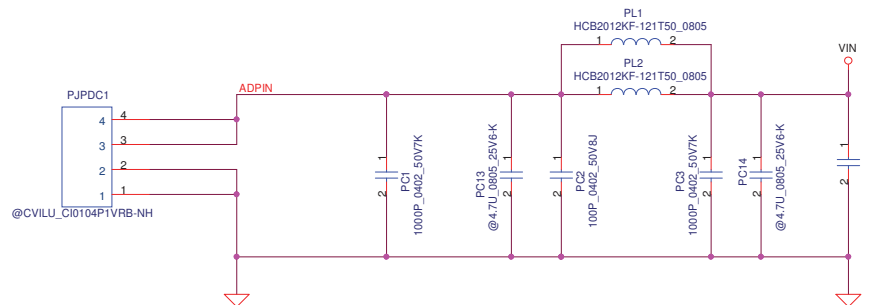
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V



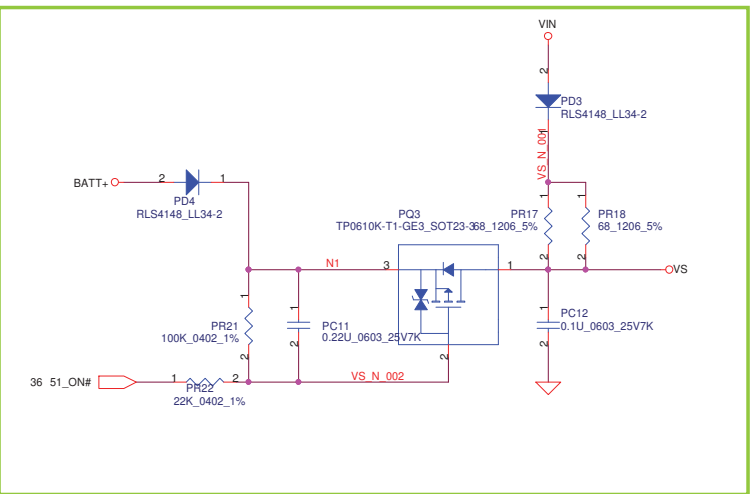
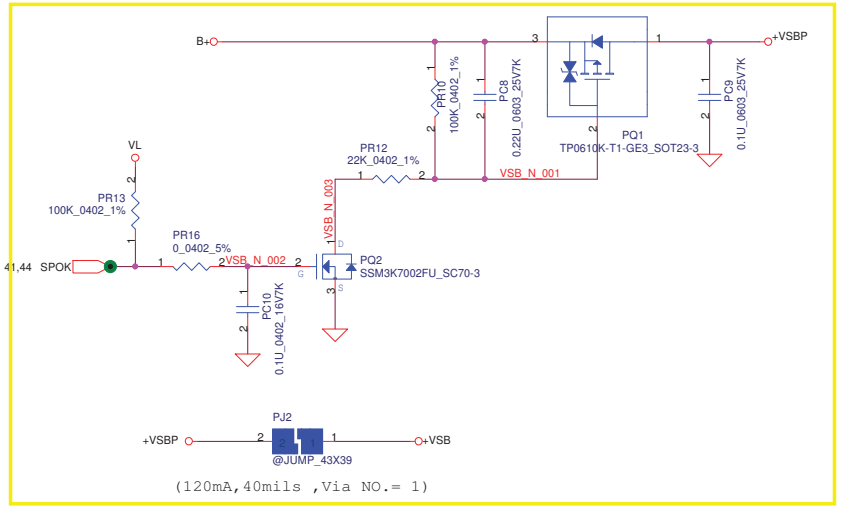
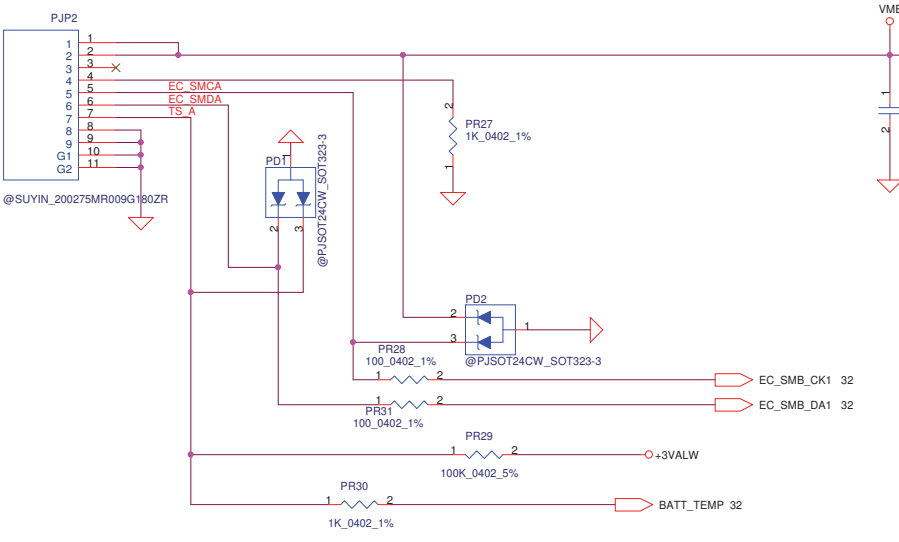
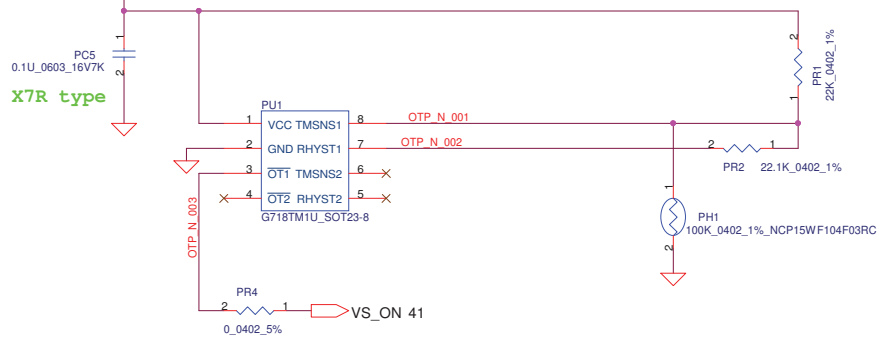
Security Classification	Compal Secret Data	
Issued Date	2009/01/23	Deciphered Date
		2010/01/23

Compal Electronics, Inc.		
Title		
CHARGER		
Size	Document Number	Rev
	NCL61 LA-6321P/M/B	0.1
Date:	Friday, April 29, 2011	Sheet 39 of 49

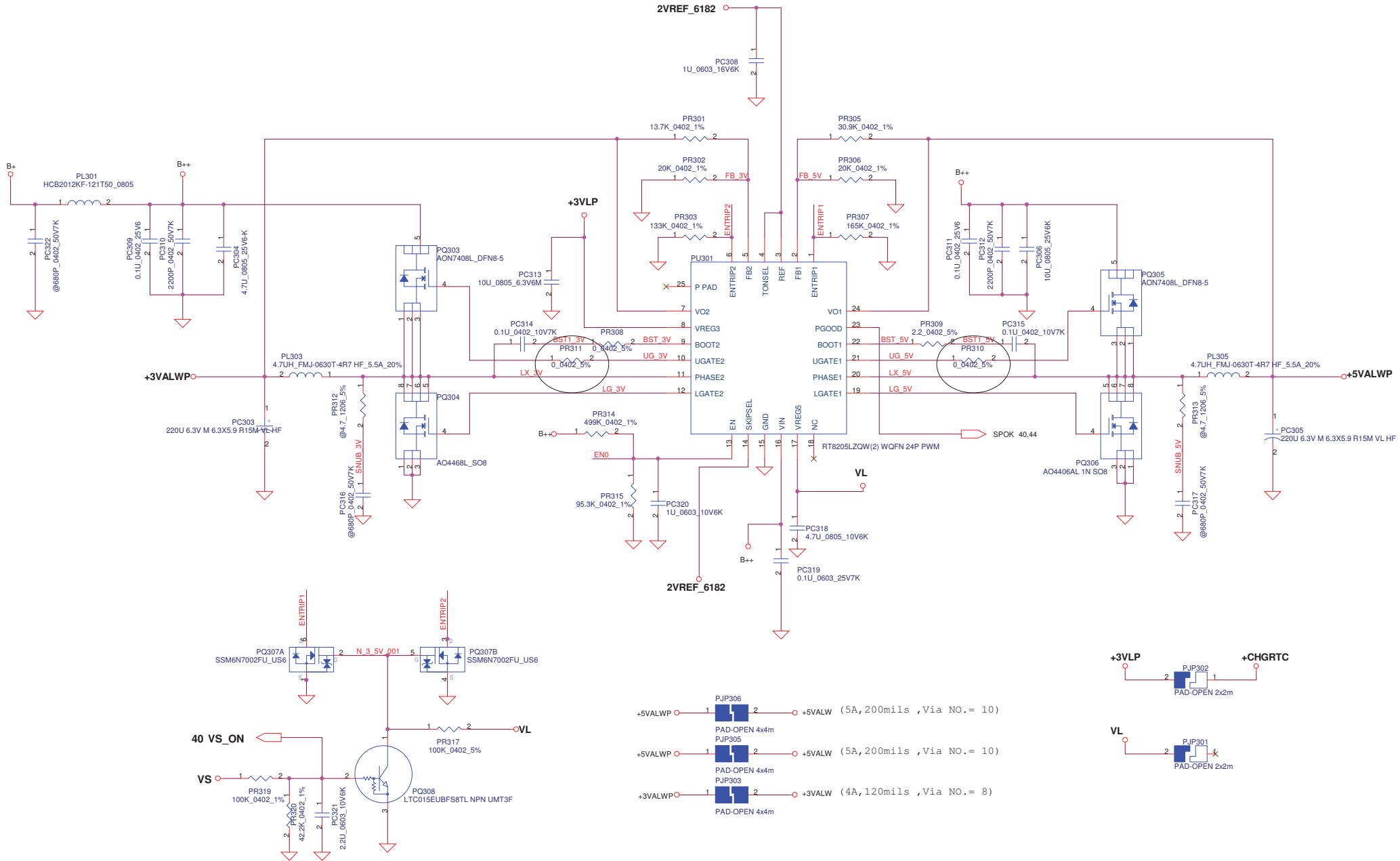
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PH1 under CPU botten side :
 CPU thermal protection at 92 +/-3 degree C
 Recovery at 80 +/-3 degree C



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				DCIN / BATT CONN / OTP
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Size	Document Number	NCL61 LA-632IP M/B		Rev
Date:	Friday, April 29, 2011	Sheet	40	of 49

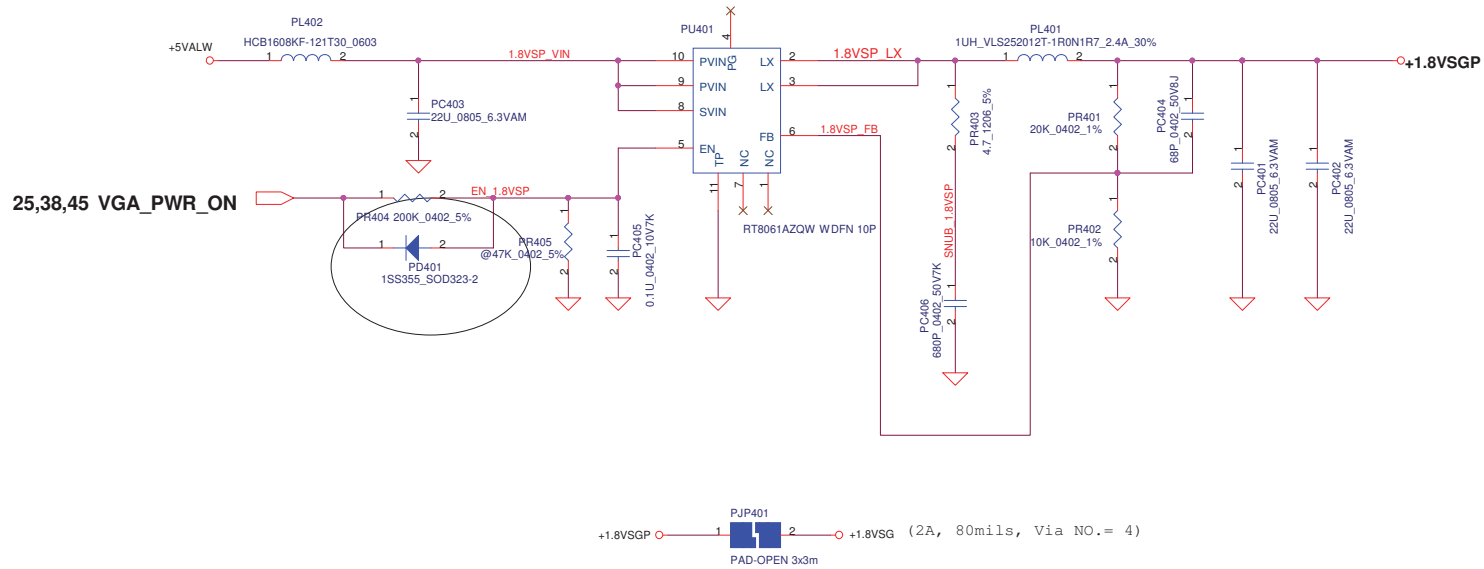


EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

Security Classification	Compal Secret Data	
Issued Date	2007/08/02	Deciphered Date
		2008/08/02

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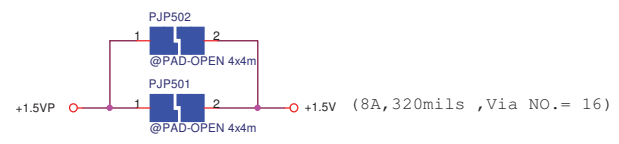
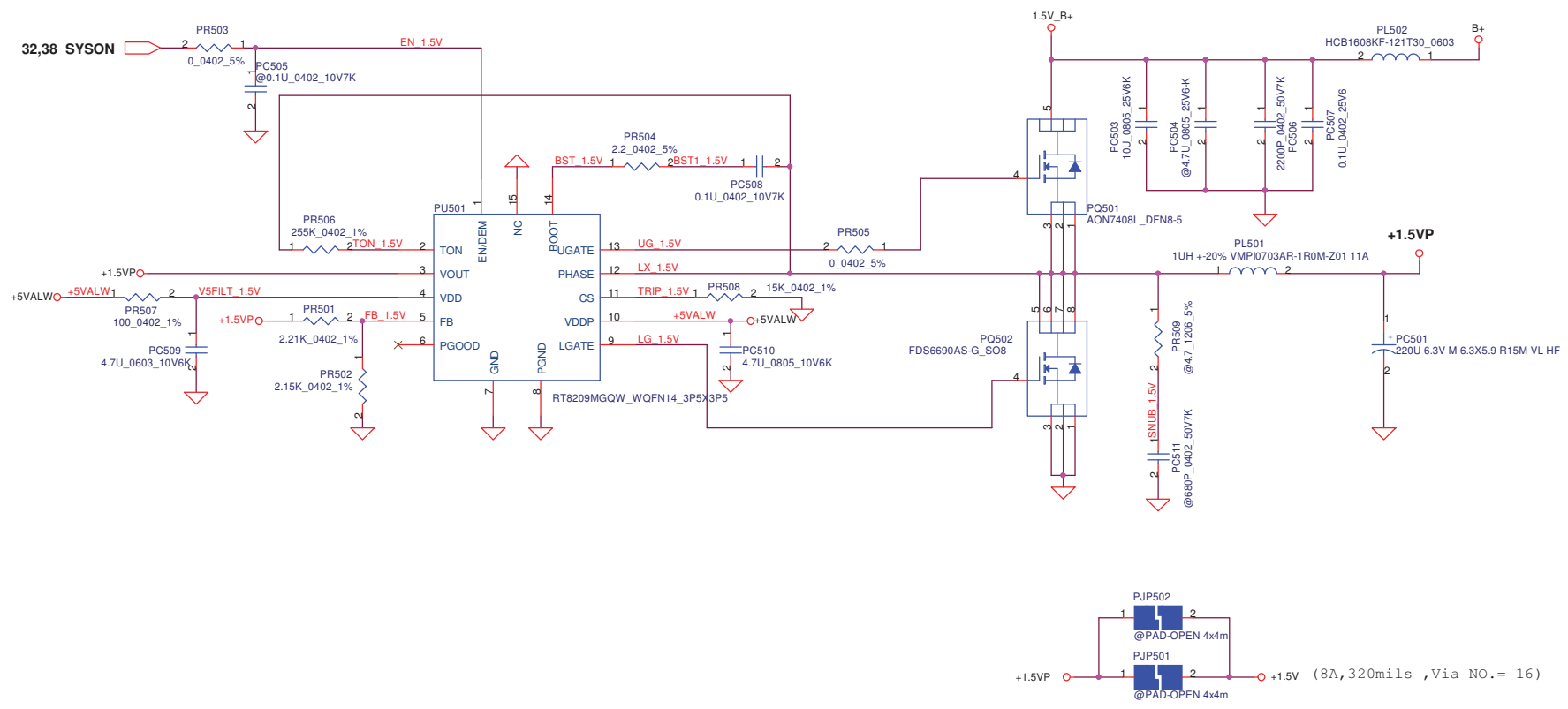
Compal Electronics, Inc.	
3.3VALWP/5VALWP	
Title	Document Number
	LAXXXX
Date	Rev
Friday, April 29, 2011	0.1
Sheet	41 of 49



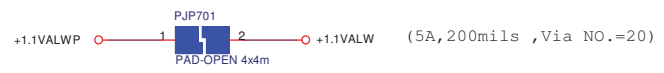
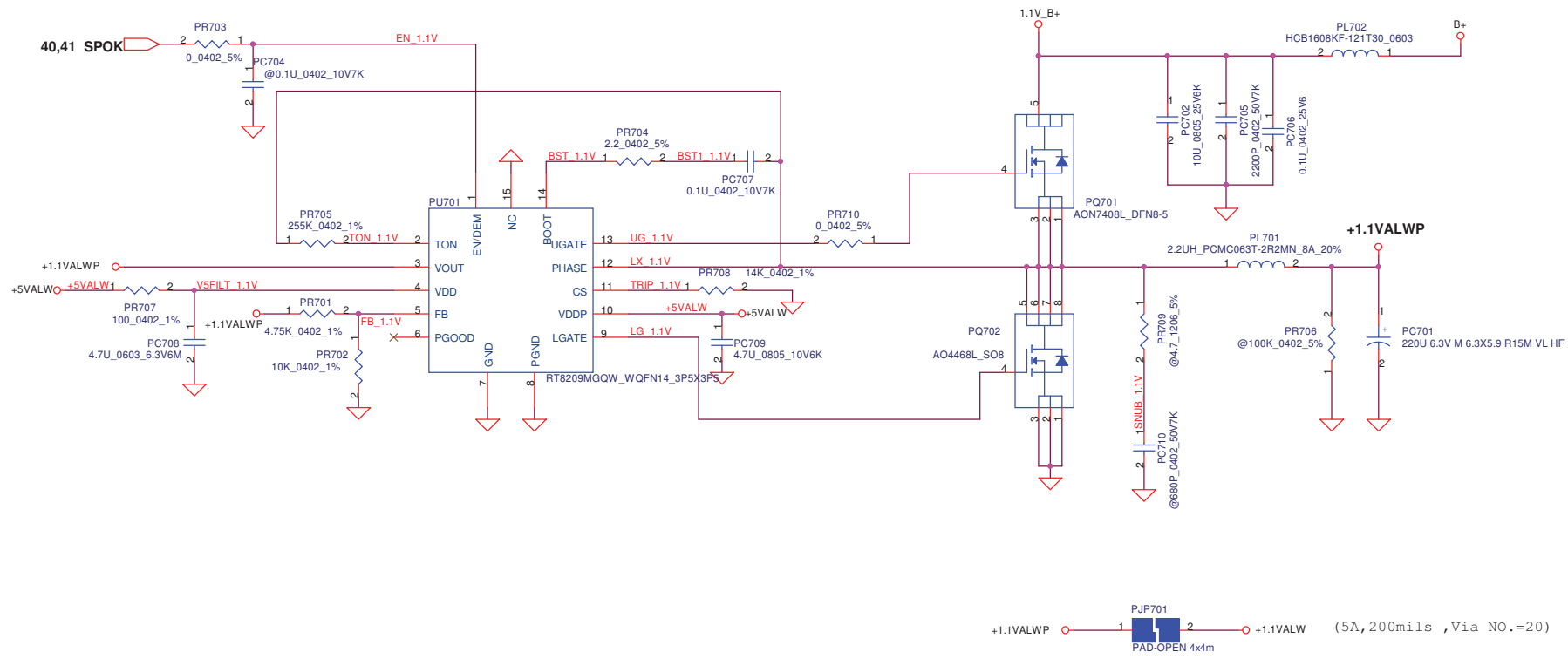
$\langle V_o = 1.8V \rangle \quad V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR401 / PR402) = 0.6 * (1 + 20K / 10K) = 1.8V$

25,38,45 VGA_PWR_ON

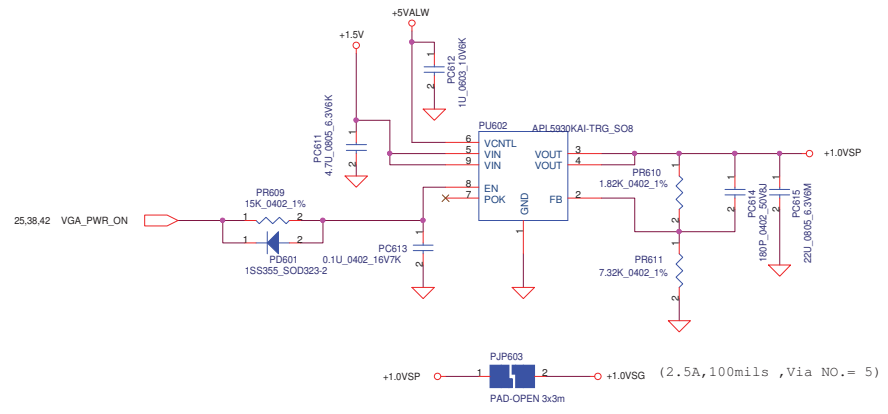
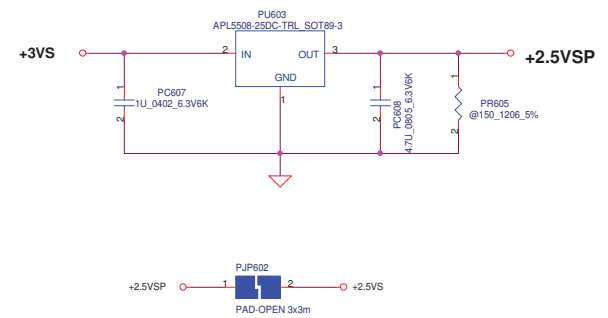
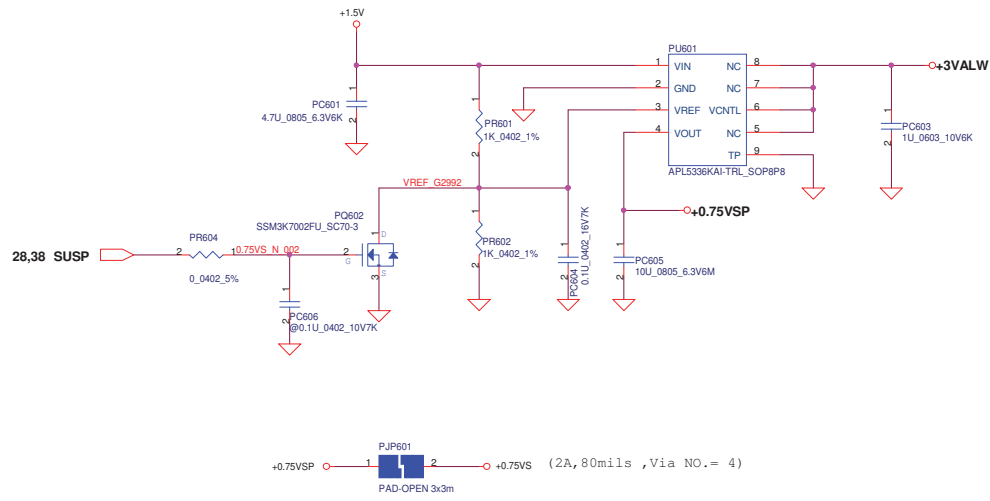
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
				+1.8VSGP	
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Size	Document Number	NCL61 LA-6321P M/B			Rev
					0.1
Date:	Friday, April 29, 2011	Sheet	42	of	49



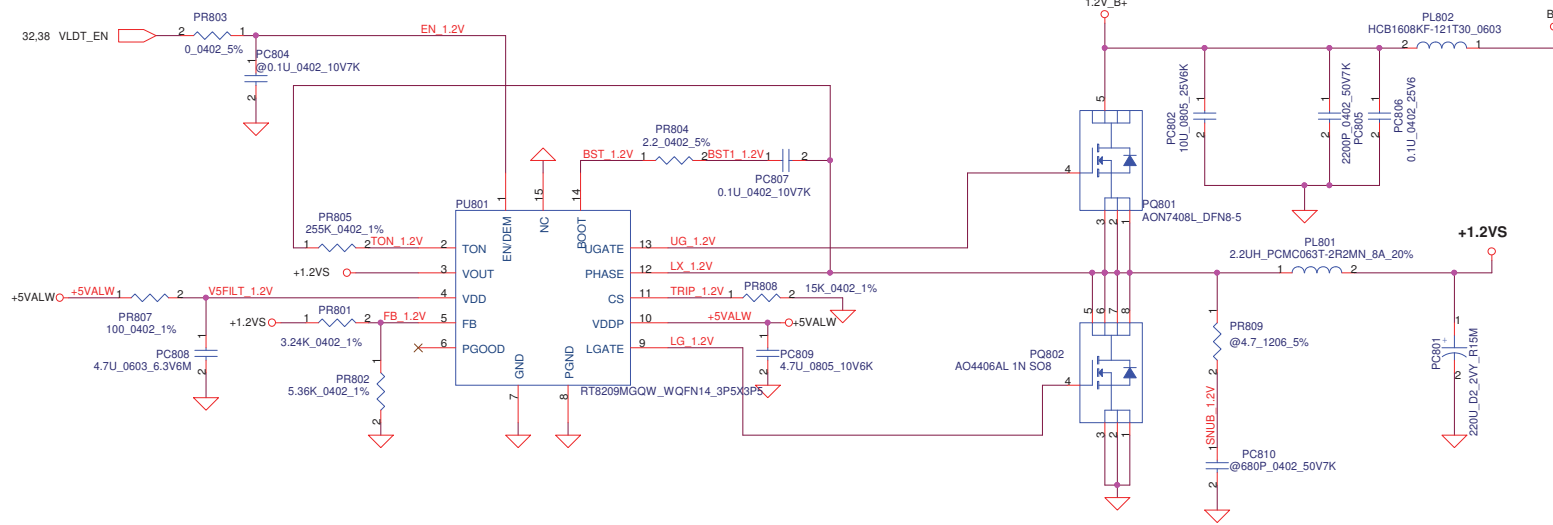
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title	
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Size	Document Number			Rev	
	LAXXXX			0.1	
Date:	Friday, April 29, 2011	Sheet	43	of	49



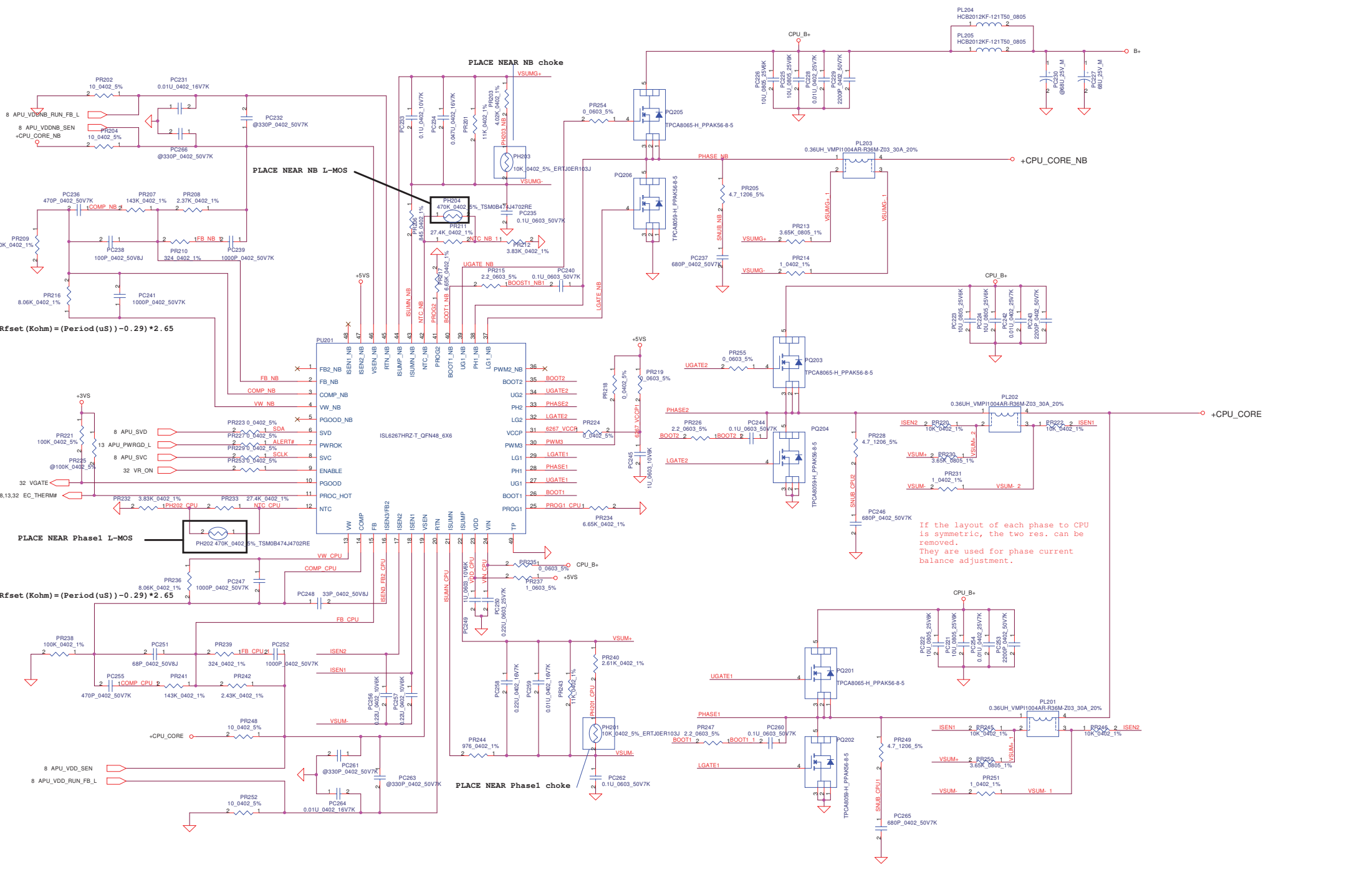
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	PWR+1.1VALWP
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Date:	Friday, April 29, 2011	Sheet	44 of 49	Rev	0.1



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Issued Date	2006/11/23	Deciphered Date	2007/11/23	Compal Electronics, Inc.
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Size	Document Number	Sheet	of	Rev
	LAXXXX	45	of	0.1
Date:	Friday, April 29, 2011	1	Sheet	45 of 49



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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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				NCL61 LA-6321P M/B	
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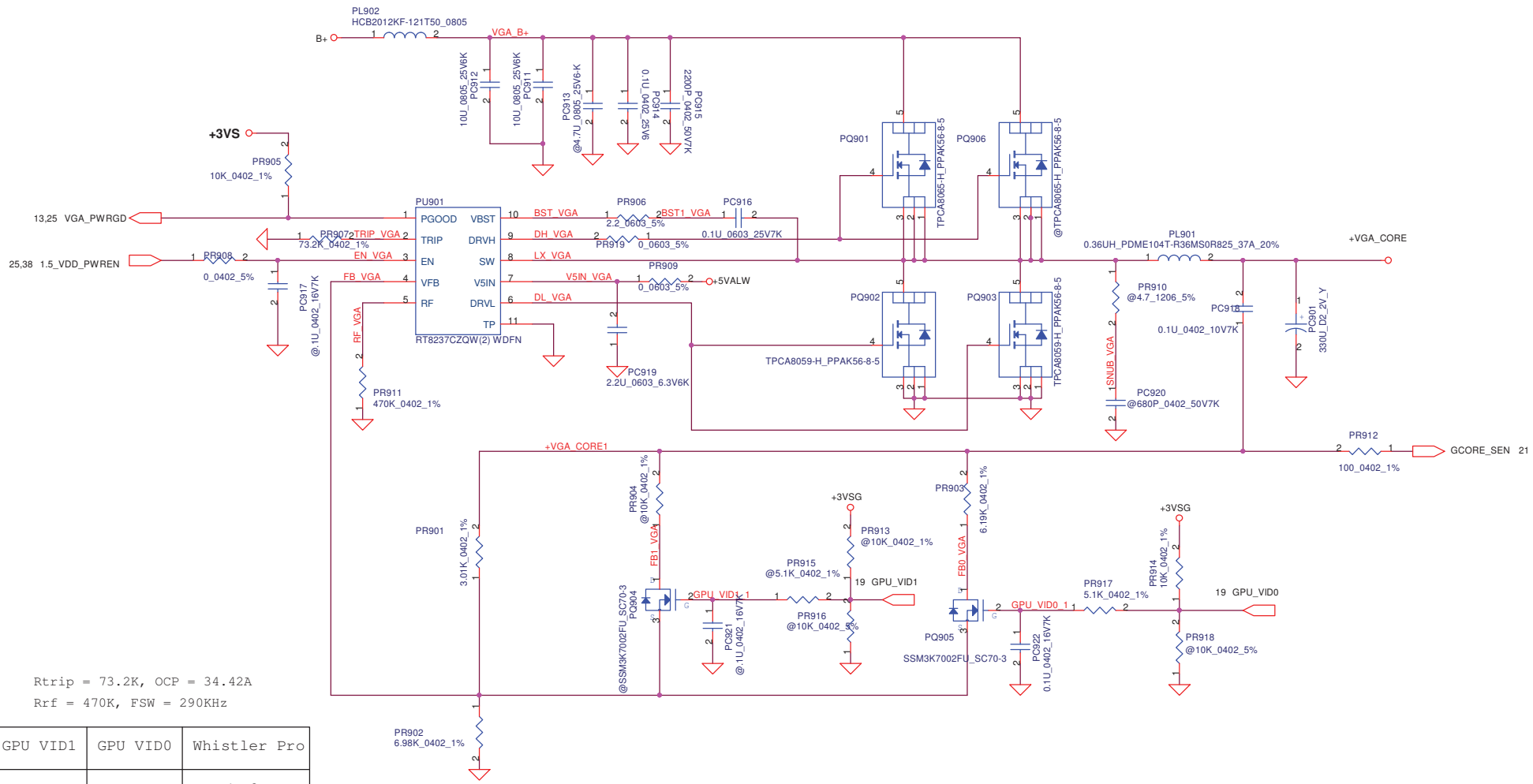


$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{S})) - 0.29 * 2.65$

$R_{fset}(\text{Kohm}) = (\text{Period}(\mu\text{S})) - 0.29 * 2.65$

If the layout of each phase to CPU is symmetric, the two res. can be removed. They are used for phase current balance adjustment.

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				PEQAE LA-7291P M/B	
				Rev	0.1
				Date	Friday, April 29, 2011
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Rtrip = 73.2K, OCP = 34.42A
 Rrf = 470K, FSW = 290KHz

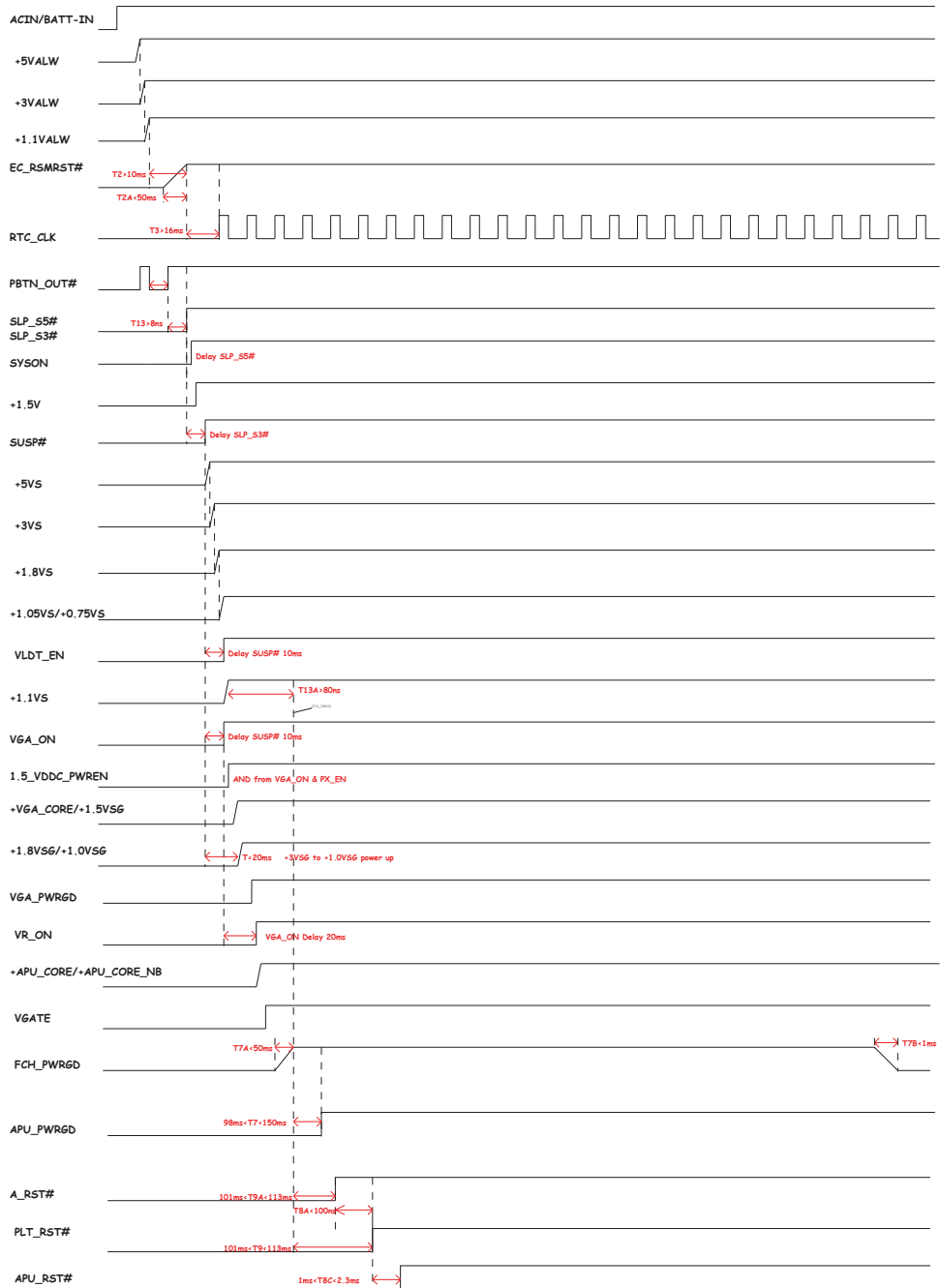
GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

Security Classification		Compal Secret Data		Compal Electronics, Inc. VGA CORE	
Issued Date	2007/05/29	Deciphered Date	200810/11		
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					LAXXXX
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

Security Classification	Compal Secret Data			Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Compal Electronics, Inc.	
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Doc#	Document Number	QBL70 LA-7533P		Rev	024
DATE	Friday, April 29, 2011	Sheet	49	of	61

POWER SEQUENCE



Signal	Value	Unit
T13	> 8	ns
T13A	> 80	ns
T1	> 20	ms
T7A	> 50	ns
T8A	> 100	ns
T9	> 113	ns
T8C	> 2.3	ms

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For AMD request	0.11	PG#26	Translator change to ANX3110	03/15	ER
2		For AI charge function	0.11	PG#34	Add U2 & U55	03/15	ER
3		For PBL70 MEMO	0.11	PG#32	Change LED1 to Green color.	03/15	ER
4		For LED brightness.	0.11	PG#32	Change R1584 to 100 ohm. Change R1586,R1588,R1591,R1592,R1593 to 100 ohm	03/15	ER
5		For LED1 brightness.	0.11	PG#32	Change LED1 power to 3VALW	03/15	ER
6		For USB3.0 & AI charger	0.12	PG#30	USBP0 connect to JUSB1 and USBP10 connect to JUSB2	03/22	ER
7		For LED1	0.12	PG#35	LED1 connect to +3VALW	03/22	ER
8		For +5VS rising time	0.2	PG#38	R1103 change to 47K	03/25	ER
9		For AI charger	0.2	PG#30	U2 reserve CEN# to EC	03/25	ER
10		For AMD spec	0.2	PG#27	R1642 & R1646 change to 4.7K ohm	03/25	ER
11		For share ROM request	0.2	PG#15 PG#16	Unpop U28, R626, R935, R934, R35, C466 Pop R910, unpop R921	03/25	ER
12		For +3VS leakage from CRT	0.21	PG#27	Add Q101, R1644, R1645 Delete R17, R31	03/31	PR
13		For Crystal EA	0.21	PG#13	Y4 change to SJ100007N00	03/31	PR
14		For EMI ISN	0.22	PG#31	C1636 change to 100P	04/19	PR
15		For thermal team recommend	0.22	PG#19	Add R1816, R1817 reserve R1814, R1815	04/19	PR
16		For BRD ID	0.22	PG#32	Change R1606 to 215K.	04/19	PR
17		Reserve PX_EN signal	0.22	PG#32	Reserve PX_EN signal to EC pin74	04/19	PR
18		For JDIMM1 and JDIMM2 location definition	0.22	PG#11 PG#12	Swap JDIMM1 and JDIMM2 location	04/19	PR
19		Prevent the leakage from CRT monitor.	0.23	PG#27	Add R1644, R1645, Q2 and Del R17, R31.	04/22	PR
20		for EMI request	0.23	PG#31	H1 change to connect to GND	04/22	PR
21		Don't use for MP	0.23	PG#13	Unpop C1193	04/22	PR
22		For VGA Sequence.	0.23	PG#38	Change R1127 from 470 ohm to 33 ohm.	04/22	PR
23		for EMI request	1.0	PG#30	modify USB3.0 redriver schemaitc	04/25	PR
24		For de-emphasis USB3.0 signal	1.0	PG#30	reserve TEST and I2C_EN net	04/25	PR
25		For some HDMI device detect error	1.0	PG#28	Change R200, R201 to 3.9K ohm	04/25	PR
26		For WLAN module rising time specification	1.0	PG#35	Change R114 to 20K ohm C1663 change to 4700P	04/25	PR
27							

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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Compal Electronics, Inc.	
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				LA-7322P	0.22
Date: Friday, April 29, 2011				Sheet	51 of 51

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase																																																																																																																																																																																																																																																																																																																																				
1		Reduce the component count for MP.	1.0		Change below the footprints from 0 ohm to R short.	04/25	PR																																																																																																																																																																																																																																																																																																																																				
2					<table border="1"> <thead> <tr> <th>Reference</th> <th>Value</th> <th>Source Part</th> <th>Source Library</th> <th>Page</th> <th>Schematic</th> </tr> </thead> <tbody> <tr><td>R1800</td><td>0_0402_5%</td><td>R-SHORT</td><td>XACIS_SYM...</td><td>P06-FS1 P...</td><td>SCHEMAT...</td></tr> <tr><td>R1801</td><td>0_0402_5%</td><td>R-SHORT</td><td>XACIS_SYM...</td><td>P06-FS1 P...</td><td>SCHEMAT...</td></tr> <tr><td>R591</td><td>0_0402_5%</td><td>R-SHORT</td><td>XACIS_SYM...</td><td>P08-FS1 Di...</td><td>SCHEMAT...</td></tr> <tr><td>R598</td><td>0_0402_5%</td><td>R-SHORT</td><td>XACIS_SYM...</td><td>P08-FS1 Di...</td><td>SCHEMAT...</td></tr> <tr><td>R606</td><td>0_0402_5%</td><td>R-SHORT</td><td>XACIS_SYM...</td><td>P08-FS1 Di...</td><td>SCHEMAT...</td></tr> <tr><td>R608</td><td>0_0402_5%</td><td>R-SHORT</td><td>XACIS_SYM...</td><td>P08-FS1 Di...</td><td>SCHEMAT...</td></tr> <tr><td>R611</td><td>0_0402_5%</td><td>R-SHORT</td><td>XACIS_SYM...</td><td>P08-FS1 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P06-FS1 P...	SCHEMAT...	R1801	0_0402_5%	R-SHORT	XACIS_SYM...	P06-FS1 P...	SCHEMAT...	R591	0_0402_5%	R-SHORT	XACIS_SYM...	P08-FS1 Di...	SCHEMAT...	R598	0_0402_5%	R-SHORT	XACIS_SYM...	P08-FS1 Di...	SCHEMAT...	R606	0_0402_5%	R-SHORT	XACIS_SYM...	P08-FS1 Di...	SCHEMAT...	R608	0_0402_5%	R-SHORT	XACIS_SYM...	P08-FS1 Di...	SCHEMAT...	R611	0_0402_5%	R-SHORT	XACIS_SYM...	P08-FS1 Di...	SCHEMAT...	R162	0_0402_5%	R-SHORT	XACIS_SYM...	P13-HUDS...	SCHEMAT...	R163	0_0402_5%	R-SHORT	XACIS_SYM...	P13-HUDS...	SCHEMAT...	R565	0_0402_5%	R-SHORT	XACIS_SYM...	P13-HUDS...	SCHEMAT...	R566	0_0402_5%	R-SHORT	XACIS_SYM...	P13-HUDS...	SCHEMAT...	R568	0_0402_5%	R-SHORT	XACIS_SYM...	P13-HUDS...	SCHEMAT...	R570	0_0402_5%	R-SHORT	XACIS_SYM...	P13-HUDS...	SCHEMAT...	R607	0_0402_5%	R-SHORT	XACIS_SYM...	P13-HUDS...	SCHEMAT...	R612	0_0402_5%	R-SHORT	XACIS_SYM...	P13-HUDS...	SCHEMAT...	R81	0_0402_5%	R-SHORT	XACIS_SYM...	P14-HUDS...	SCHEMAT...	R912	0_0402_5%	R-SHORT	XACIS_SYM...	P16-HUDS...	SCHEMAT...	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Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/25	Deciphered Date	2012/04/25	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number QBL60 LA-7552P Date: Friday, April 29, 2011 Sheet 53 of 53