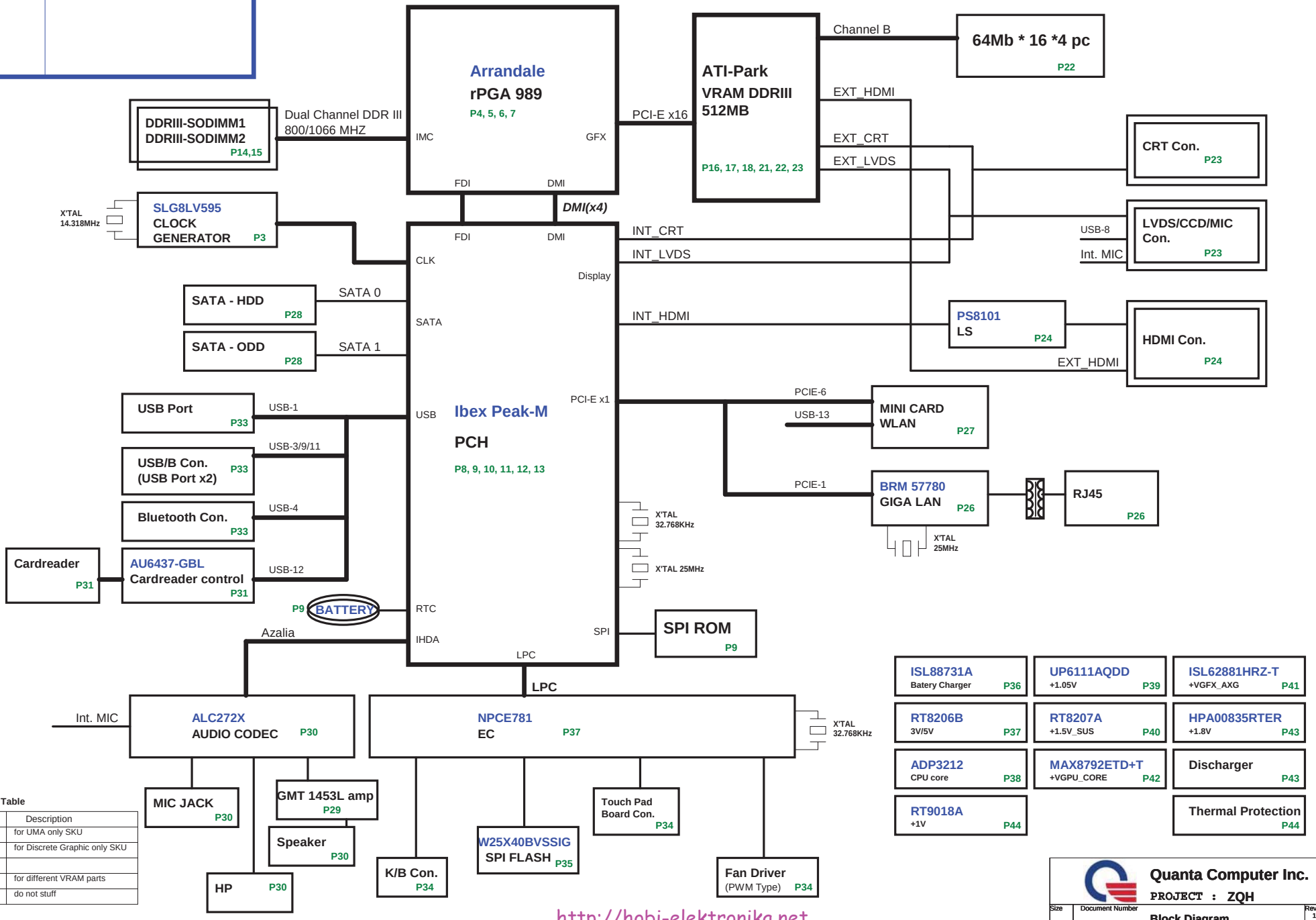
VER : 1A

BOM P/N	Description

ZQH SYSTEM BLOCK DIAGRAM



BOM Option Table

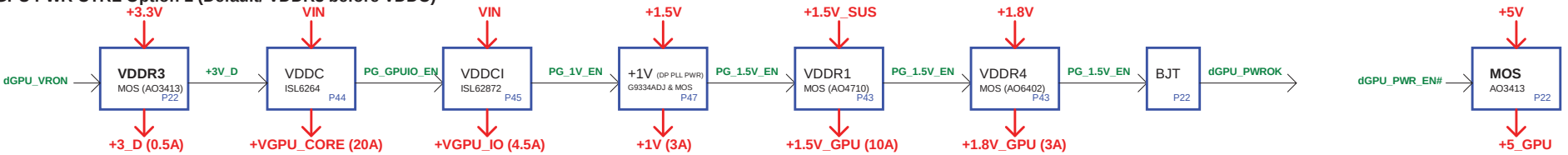
Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
VRAM@	for different VRAM parts
*	do not stuff

Quanta Computer Inc.
PROJECT : ZQH

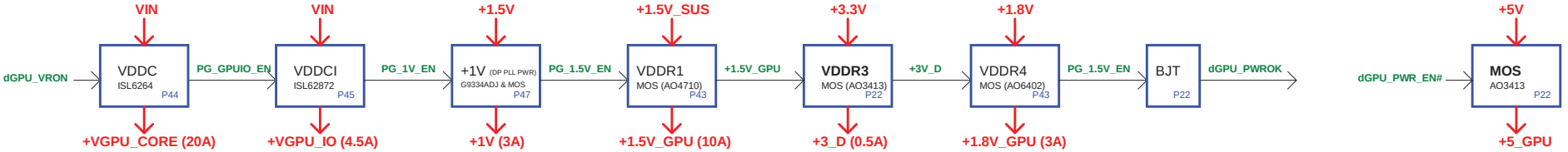
Size	Document Number	Rev
	Block Diagram	1A

Date: Monday, March 14, 2011 Sheet 1 of 35

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



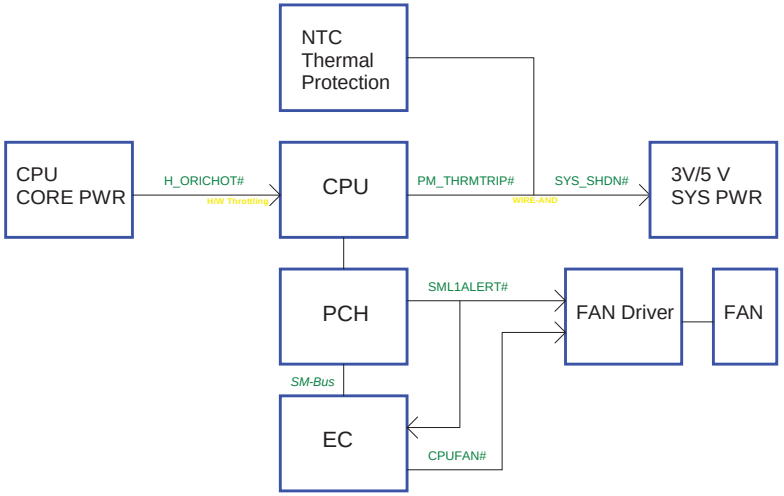
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



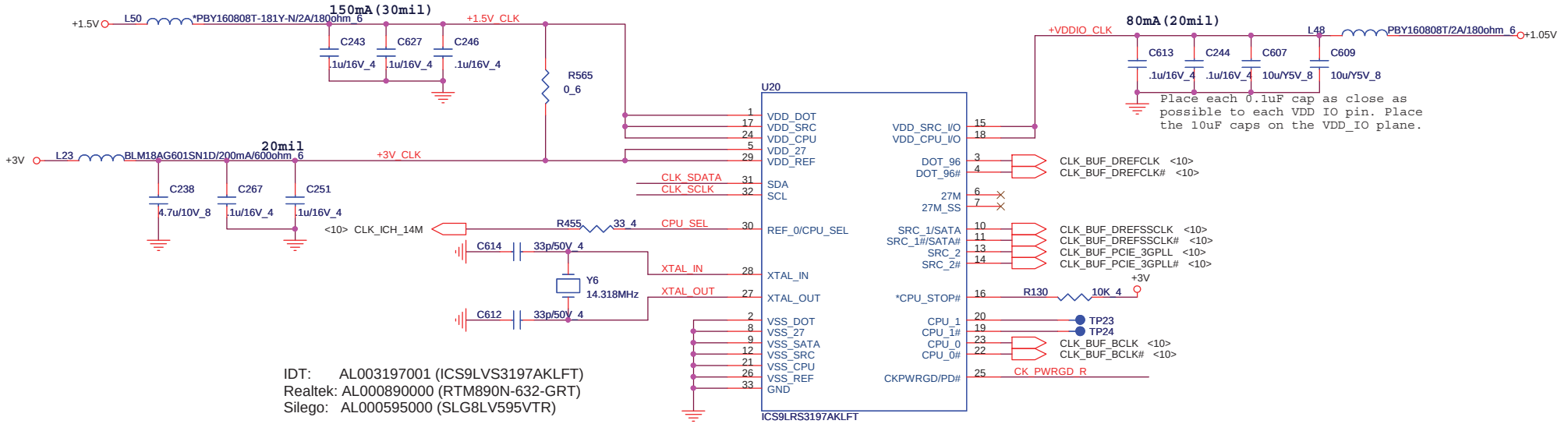
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart

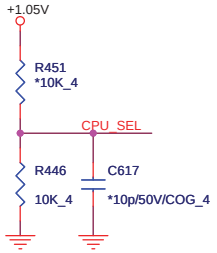


Quanta Computer Inc.
PROJECT : ZQH
Size | Document Number: PWR Status & GPU PWR CRL & THRM | Rev 1A
Date: Monday, March 14, 2011 | Sheet 2 of 45



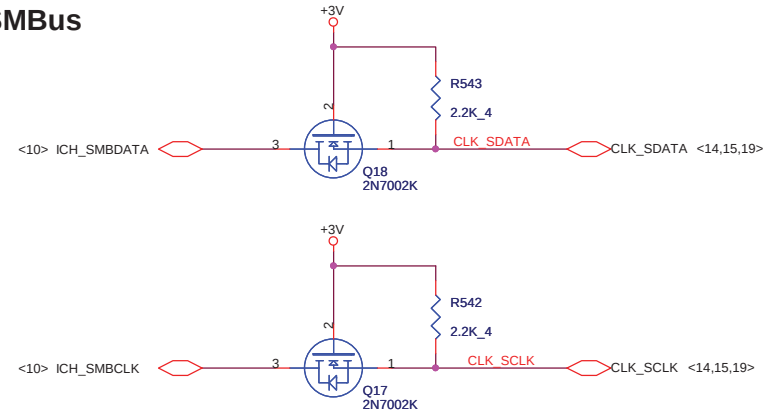
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select

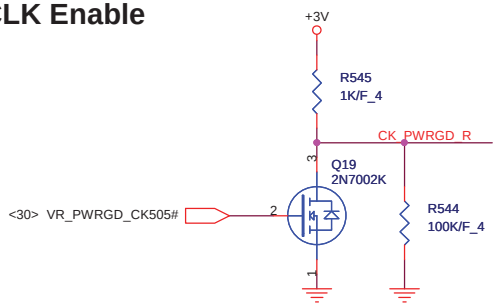


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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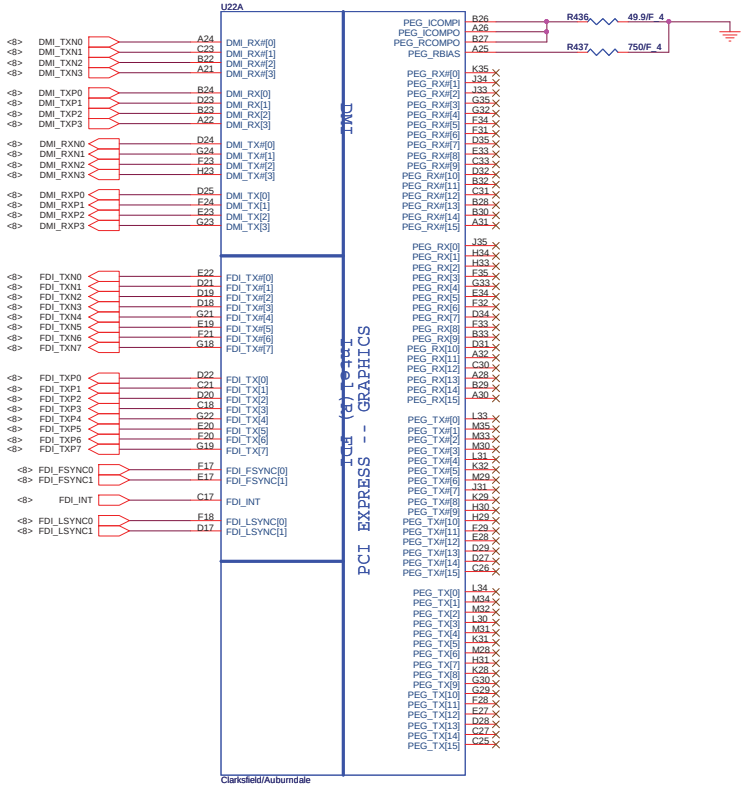
PROJECT : ZQH

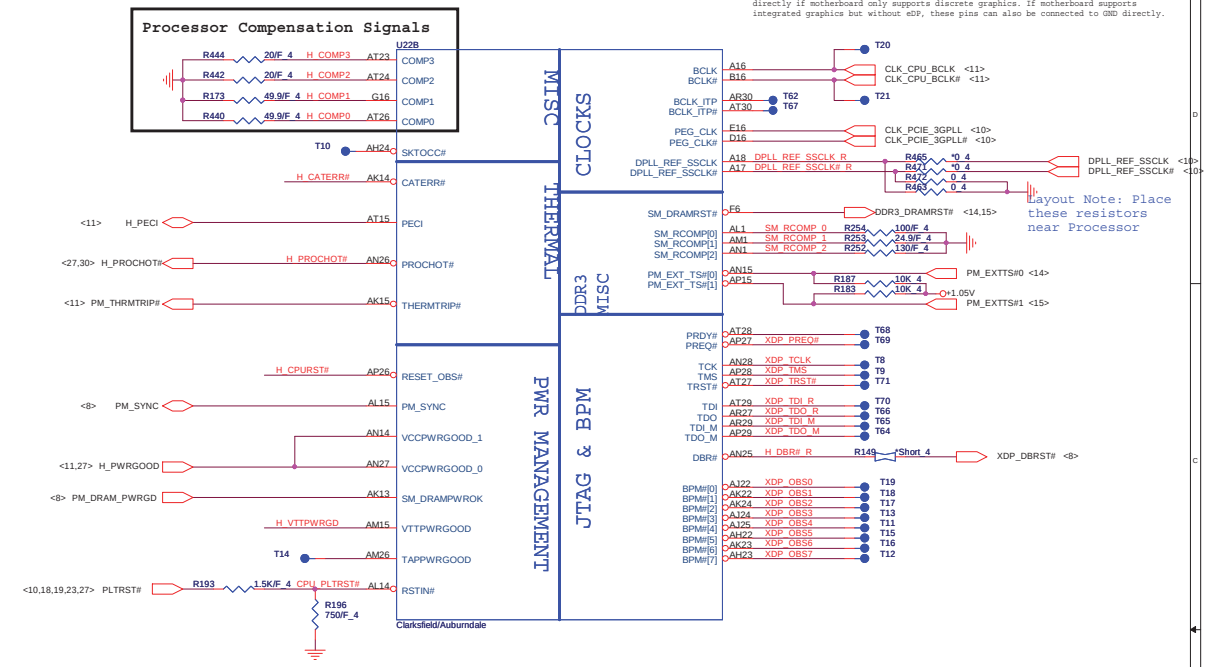
Size	Document Number	Rev
	Clock Generator	1A
Date: Monday, March 14, 2011	Sheet 3 of 45	

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



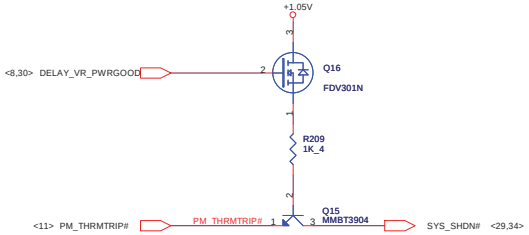
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Arrandale directly if motherboard only supports discrete graphics. If motherboard supports integrated graphics but without eDP, these pins can also be connected to GND directly.

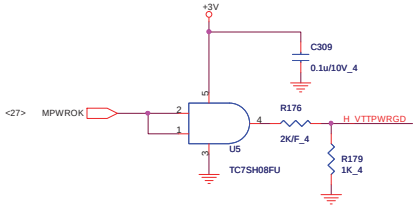


Layout Note: Place these resistors near Processor

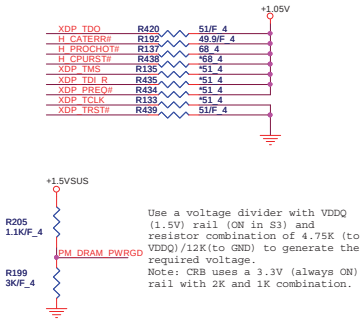
Thermaltrip protect



VTT PWR_Good

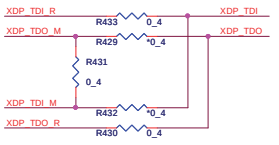


Processor pull-up



Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

JTAG MAPPING

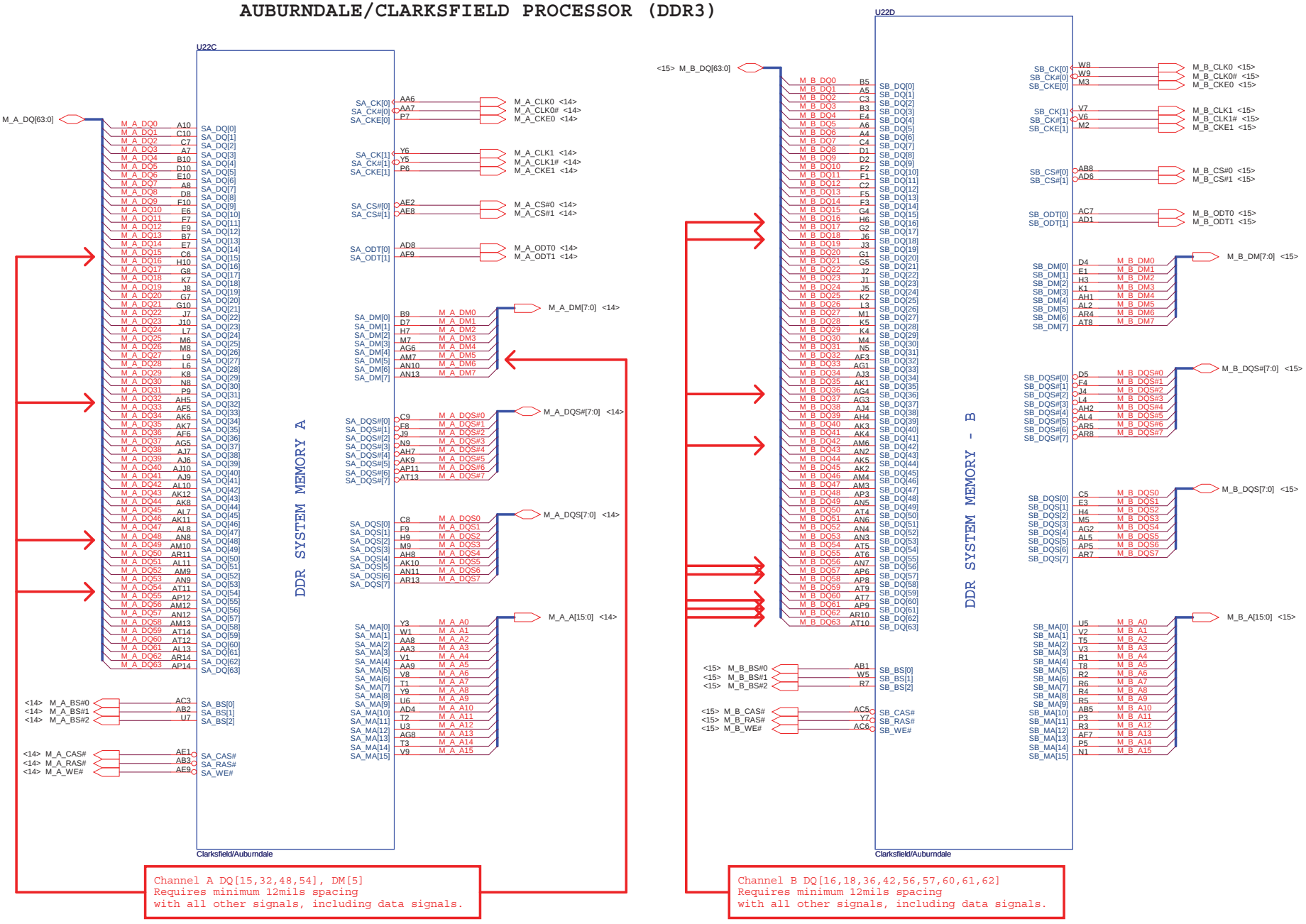


Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	AUBURNDA 1/4	1A
Date: Monday, March 14, 2011	Sheet 4 of 45	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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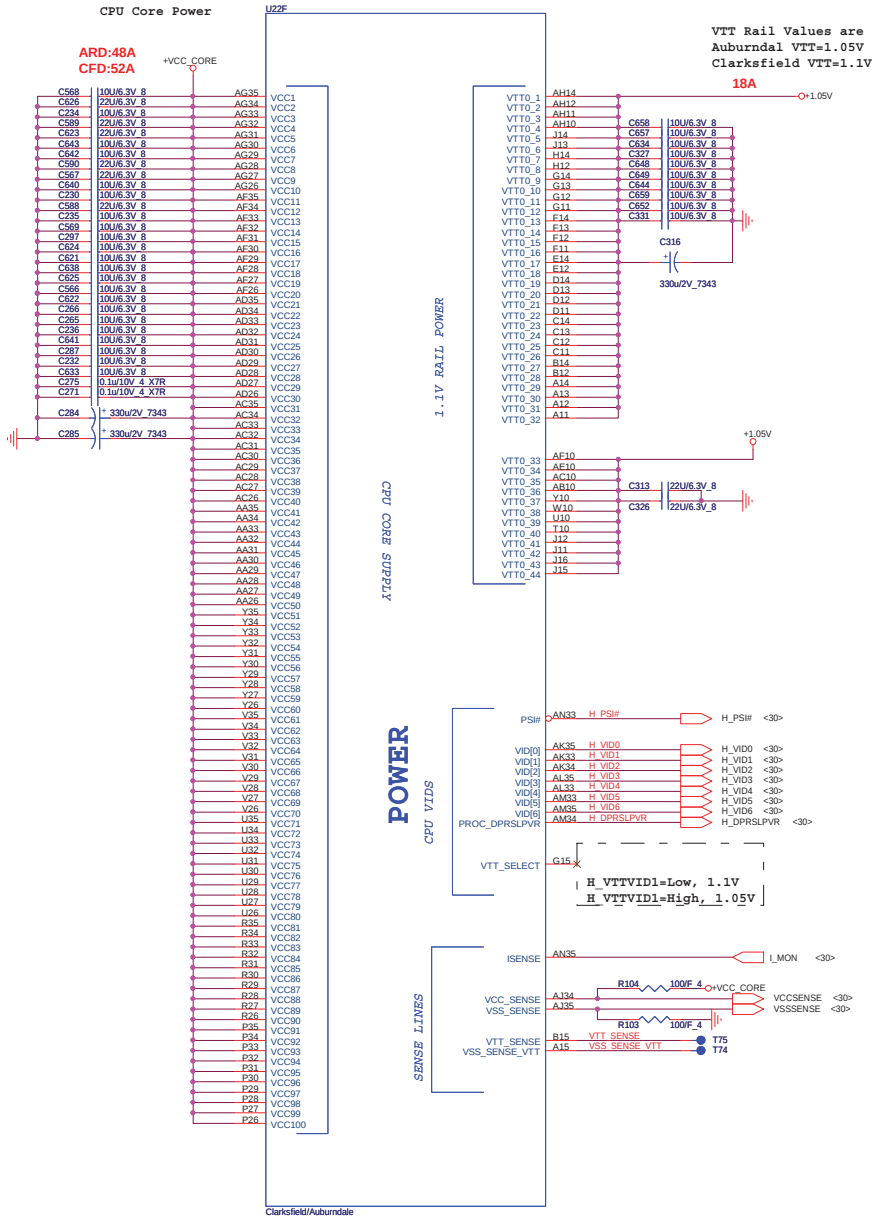
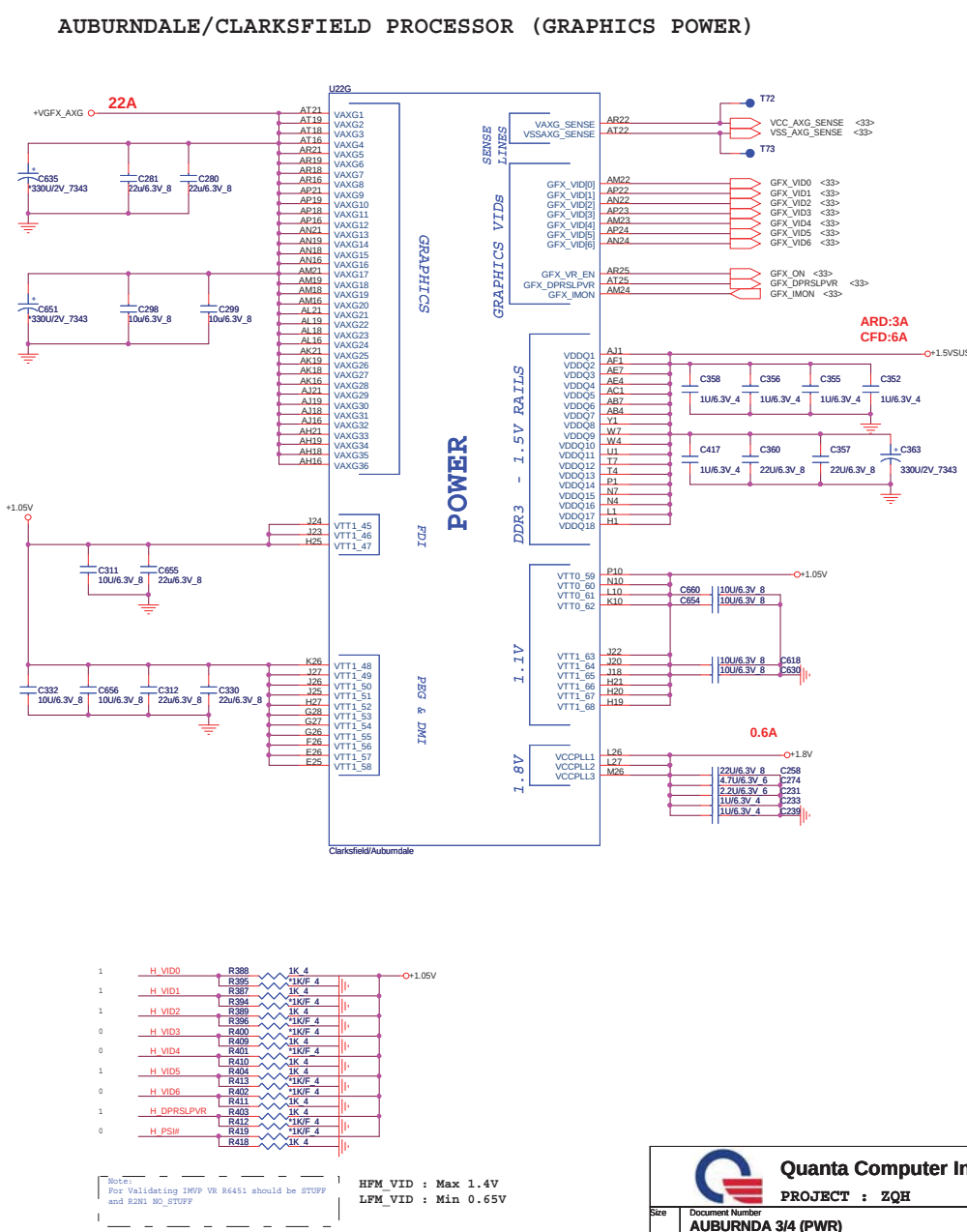
PROJECT : ZQH

Size	Document Number	Rev
	AUBURNDA 2/4	1A

Date: Monday, March 14, 2011 Sheet 5 of 45





AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

Note:
For Validating IMVP VR R6451 should be STUFF and R2N1 NO_STUFF

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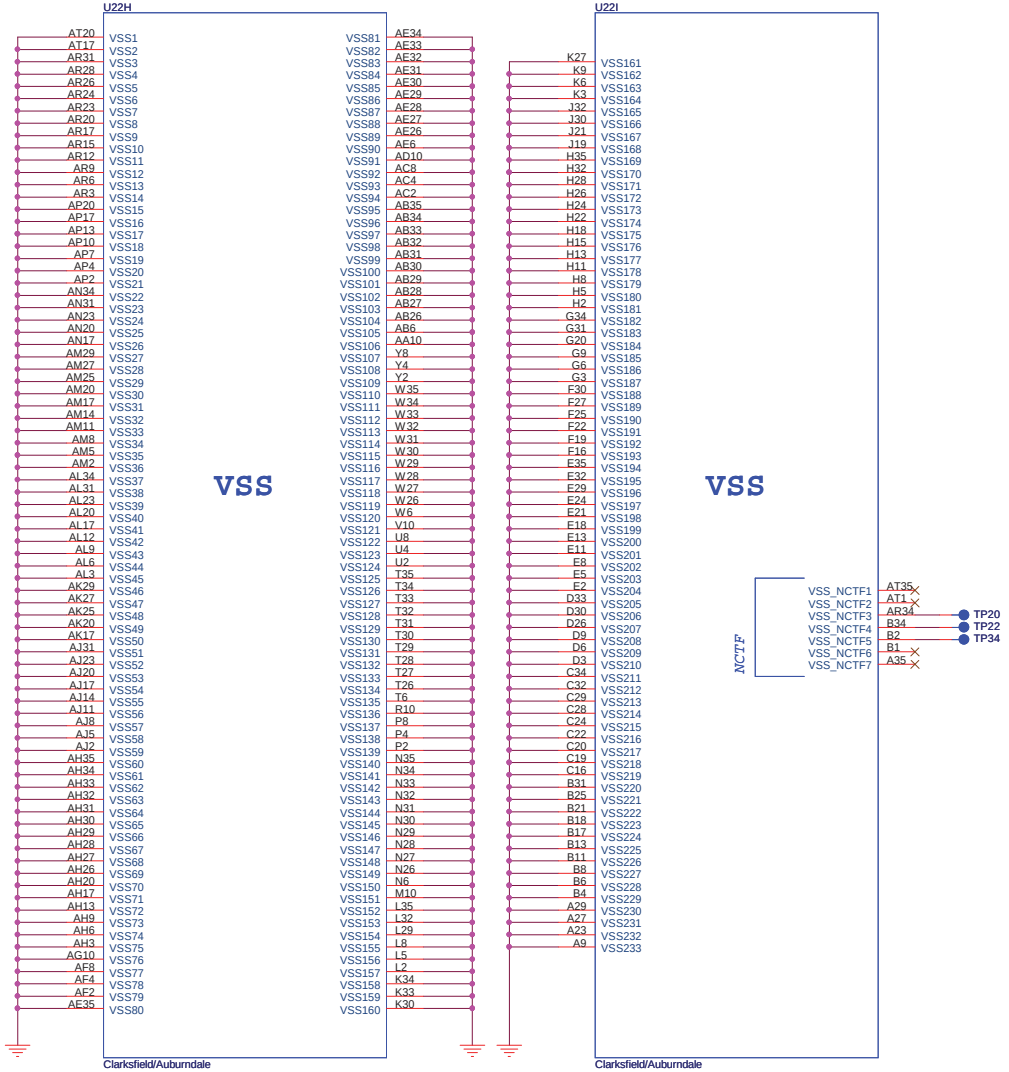
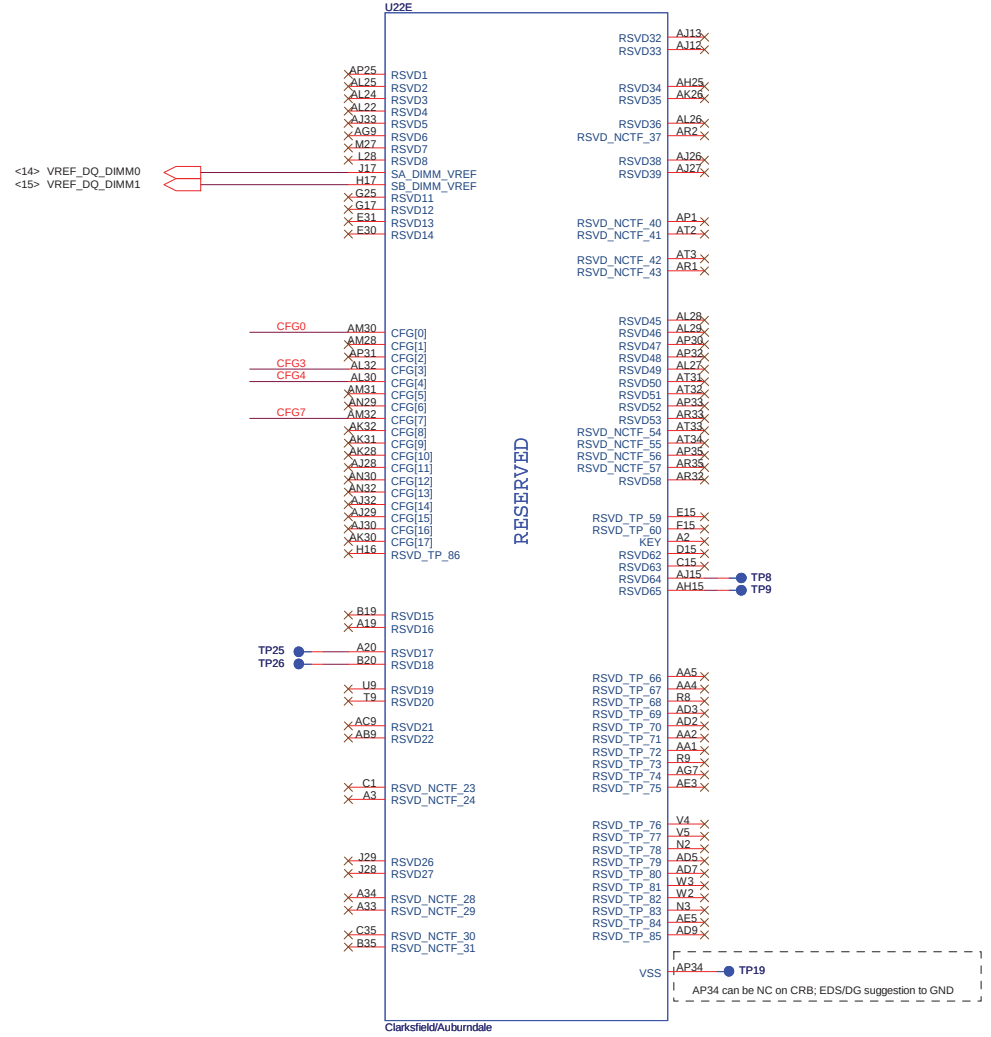
PROJECT : ZQH		
Size	Document Number: AUBURNDA 3/4 (PWR)	Rev: 1A
Date: Monday, March 14, 2011	Sheet 6 of 45	

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R128 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R125 3.01K/F_4
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R127 *3.01K
T				CFG7 R126 *3.01K/F_4

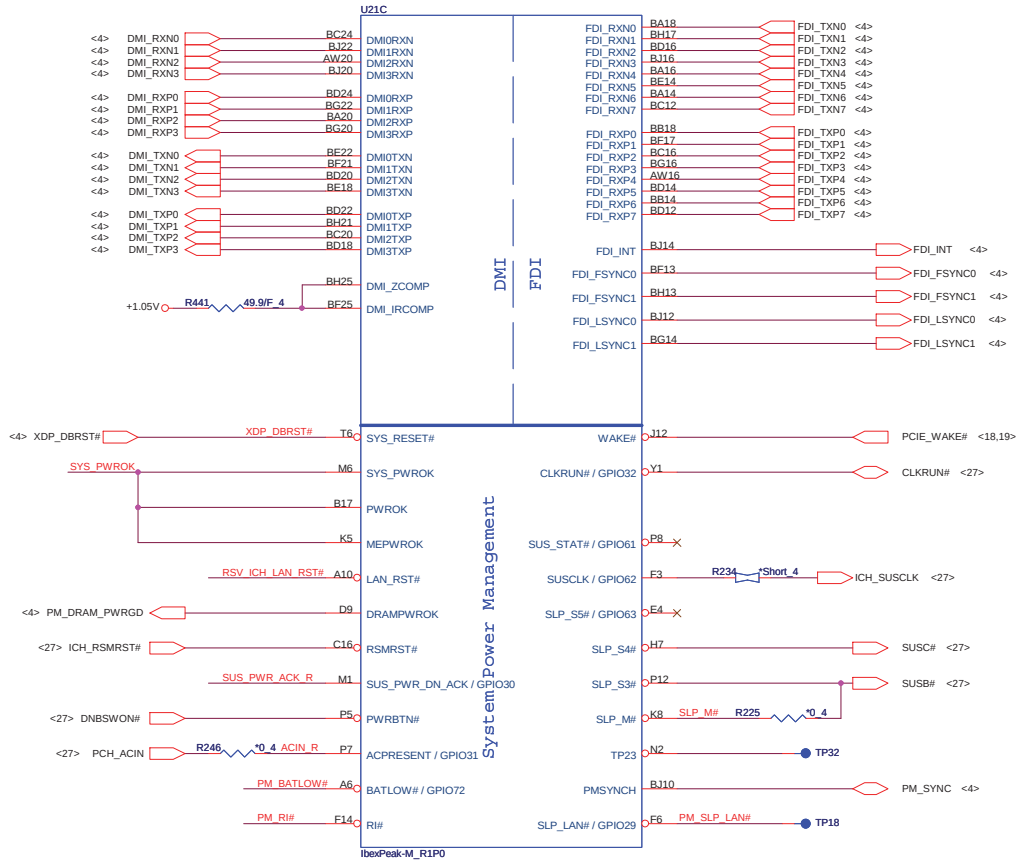
Quanta Computer Inc.

PROJECT : ZQH

Size	Document Number	Rev
	AUBURNDA 4/4	1A

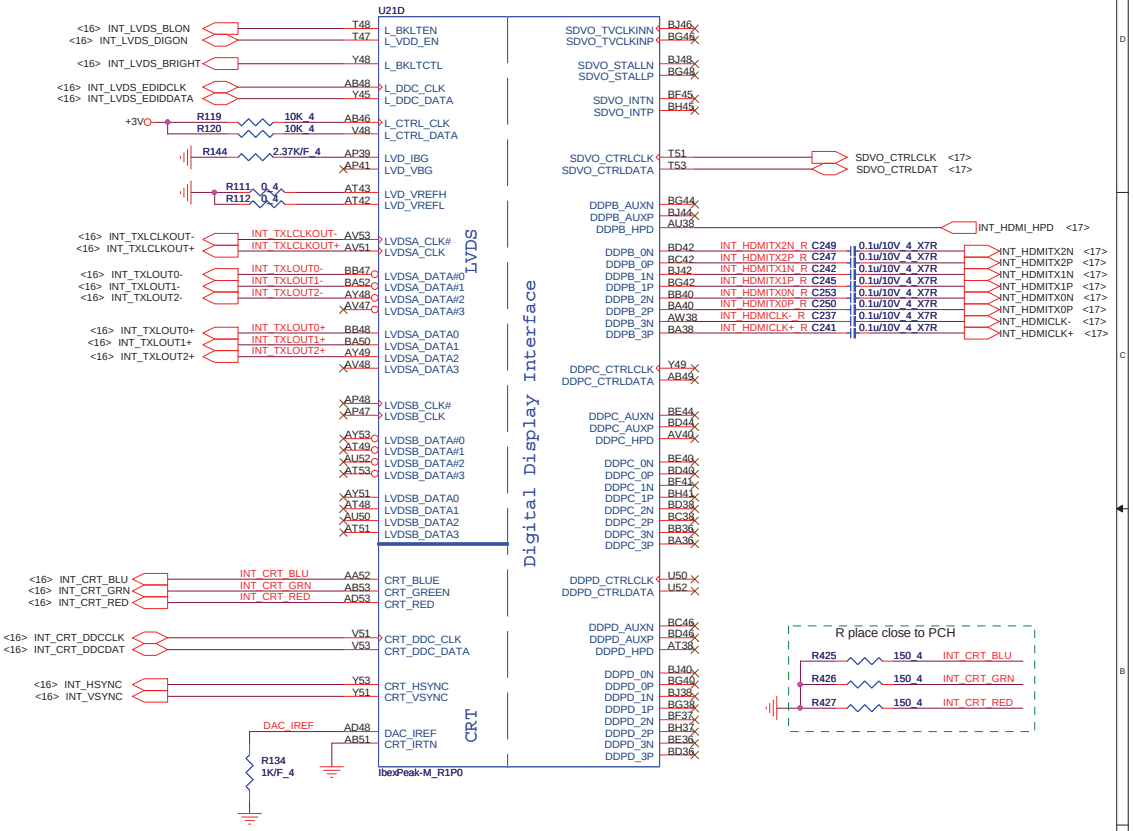
Date: Monday, March 14, 2011 Sheet 7 of 45

IBEX PEAK-M (DMI,FDI,GPIO)

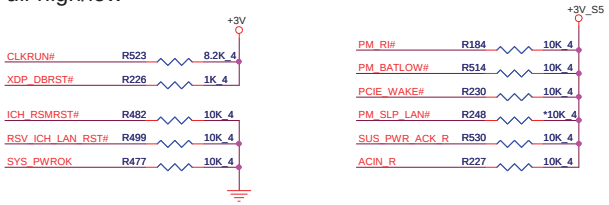


AC-coupling CAP place close to PCH

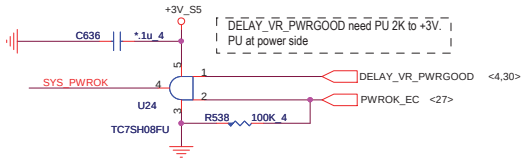
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low

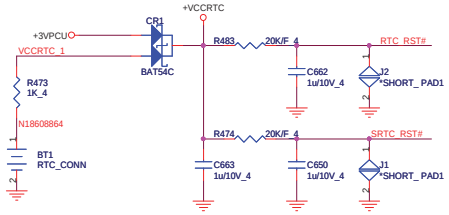


System PWR_OK

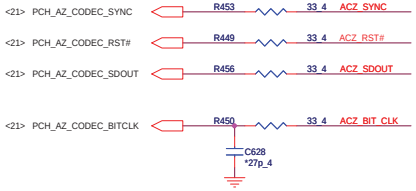


Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number	Rev
	IBEX PEAK-M 1/6	1A
Date: Monday, March 14, 2011	Sheet 8 of 45	

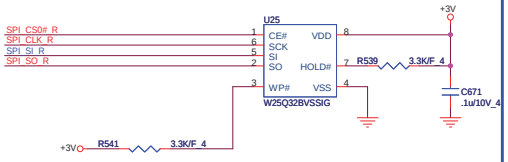
RTC Circuitry

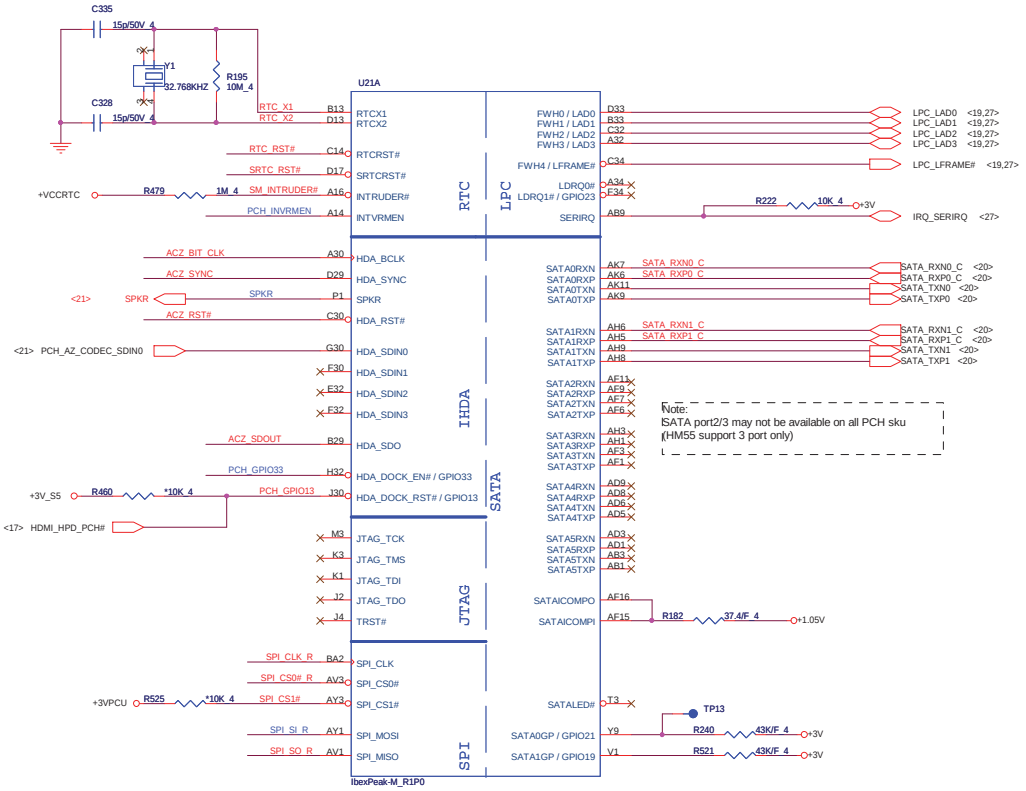


HDA Bus



PCH SPI





PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R164 *1K/F_4 R145 *10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K_4 R122 1K_4 R123 *1K_4 R131 *1K_4 +3V <10> PCI_GNT0# <10> PCI_GNT1#
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10> PWM_SELECT# R158 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<10> PCI_GNT3# R421 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R202 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R206 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	<11> RSV_GPIO8 R204 10K_4 +3V_S5 R203 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	<11> CR_WAKE# R244 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R221 *10K_4

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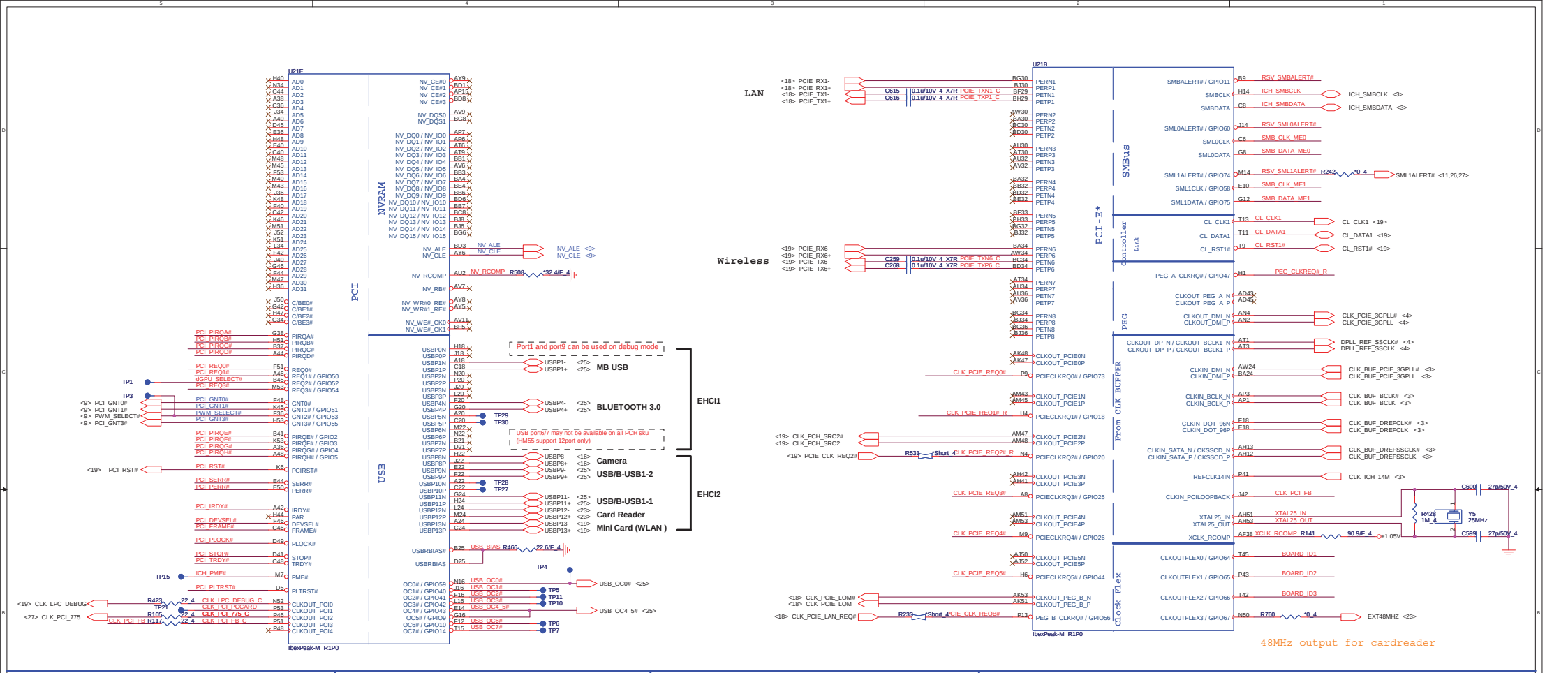
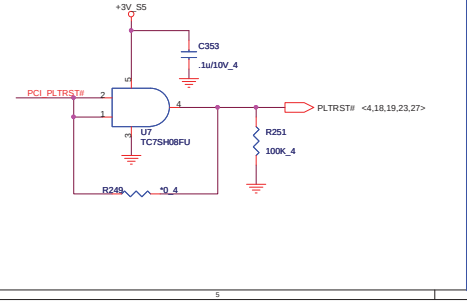
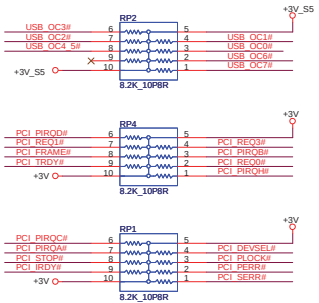
PROJECT : ZQH

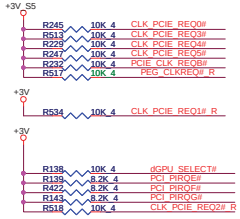
Size	Document Number	Rev
	IBEX PEAK-M 2/6	1A

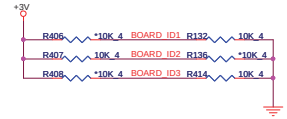
Date: Monday, March 14, 2011 Sheet 9 of 45



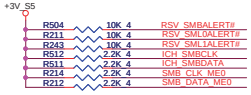


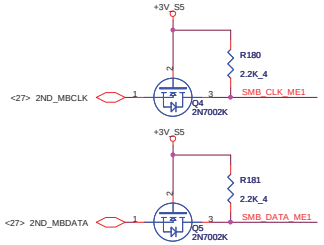






BOARD_ID1	Not Defined
BOARD_ID2	High = 80port output to LPC Low = 80port output to PCI
BOARD_ID3	High = Reserved Low = Reserved (Default)





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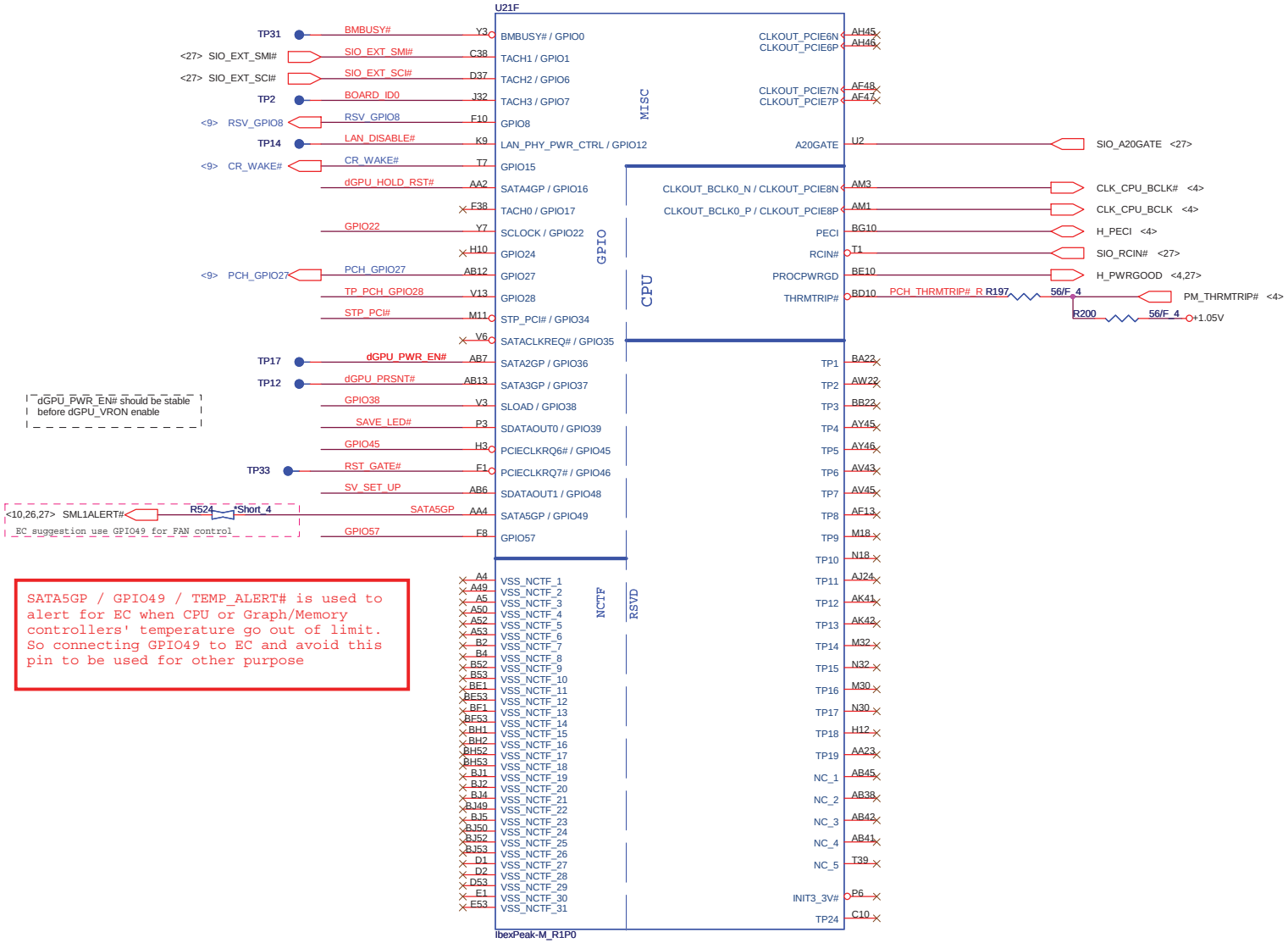
PROJECT : ZQH

Size	Document Number	Rev
	IBEX PEAK-M 3/6	1A

Date: Monday, March 14, 2011 Sheet 10 of 45

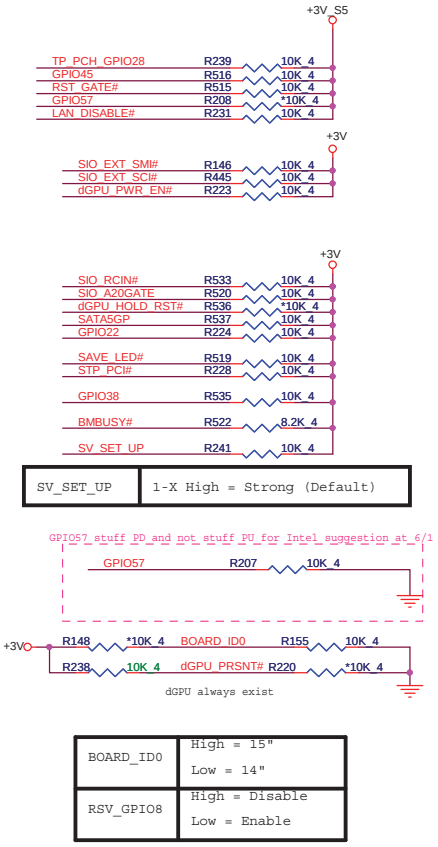
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#

GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

BOARD_ID0	High = 15" Low = 14"
RSV_GPIO8	High = Disable Low = Enable

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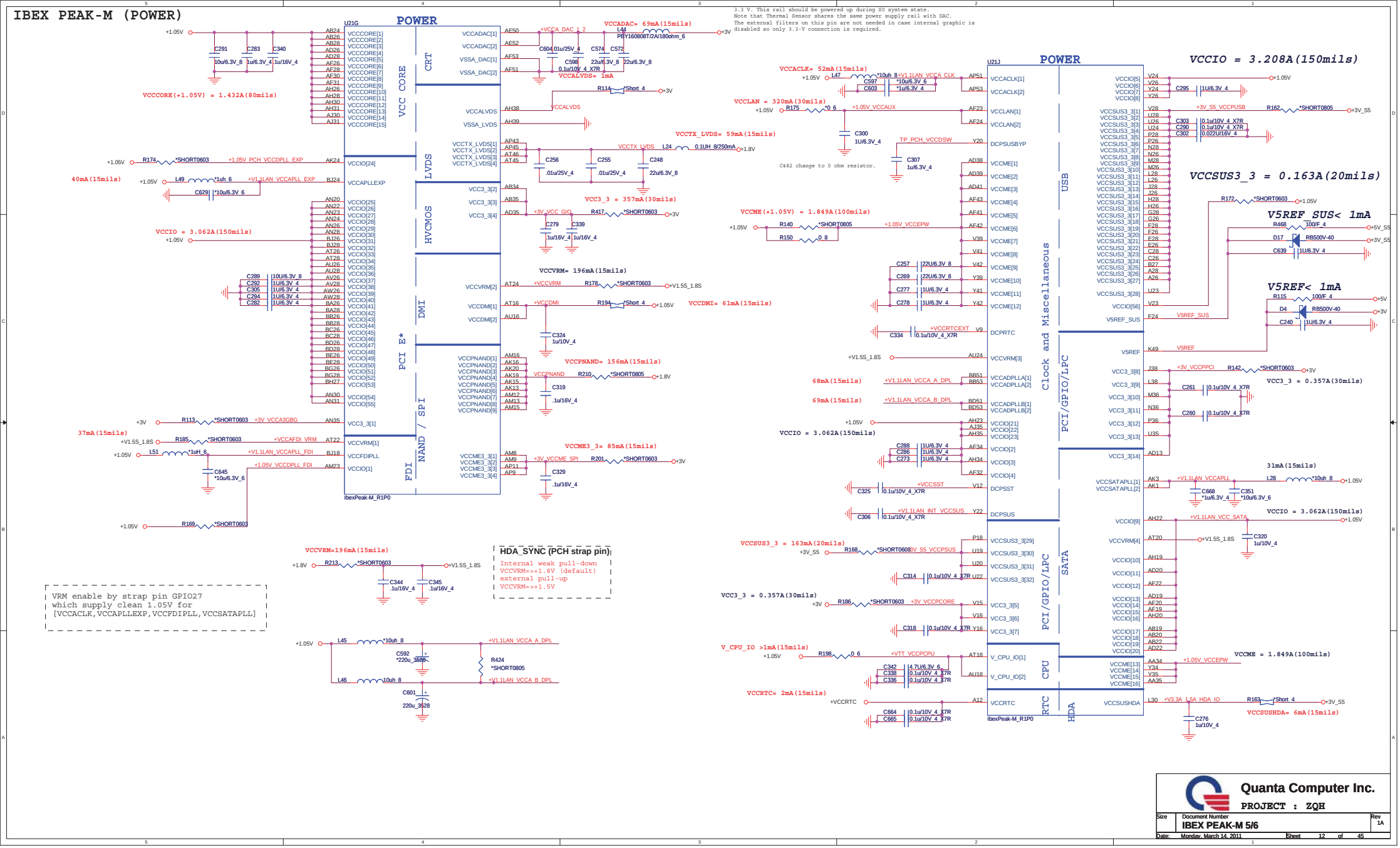
PROJECT : ZQH

Size	Document Number	Rev
	IBEX PEAK-M 4/6	1A

Date: Monday, March 14, 2011 Sheet 11 of 45

IBEX PEAK-M (POWER)

3.3 V. This rail should be powered up during S0 system state.
Note that Thermal Sensor shares the same power supply rail with DAC.
The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.



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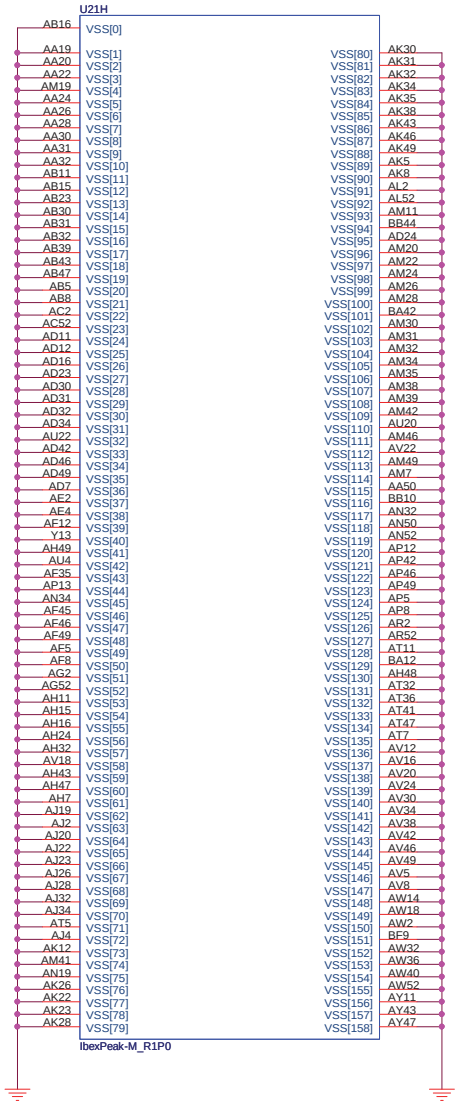
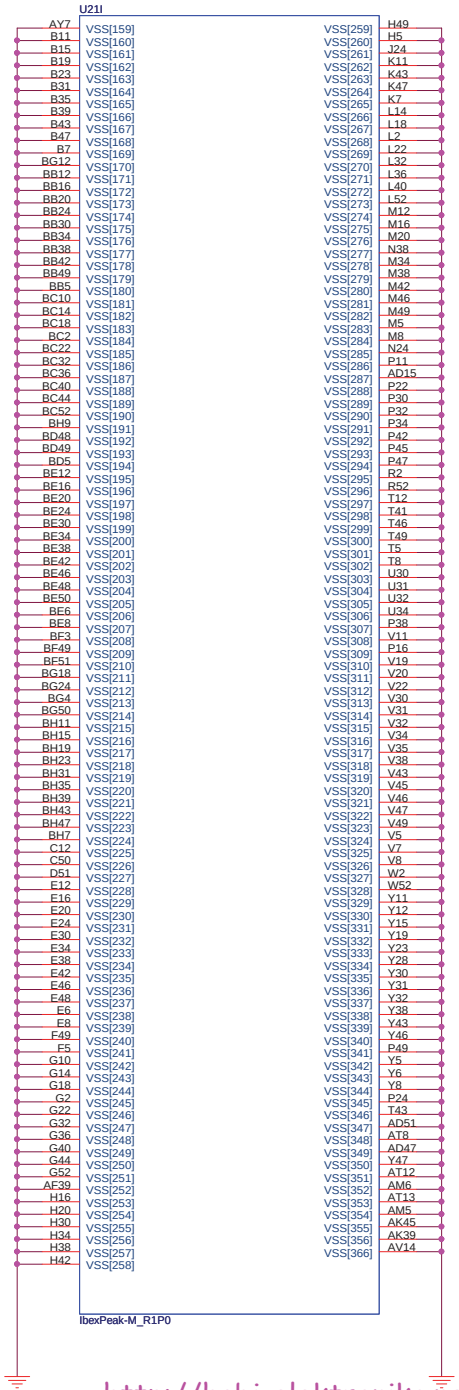
PROJECT : ZQH		
Size	Document Number: IBEX PEAK-M 5/6	Rev: 1A
Date: Monday, March 14, 2011	Sheet 12 of 45	

IBEX PEAK-M (GND)



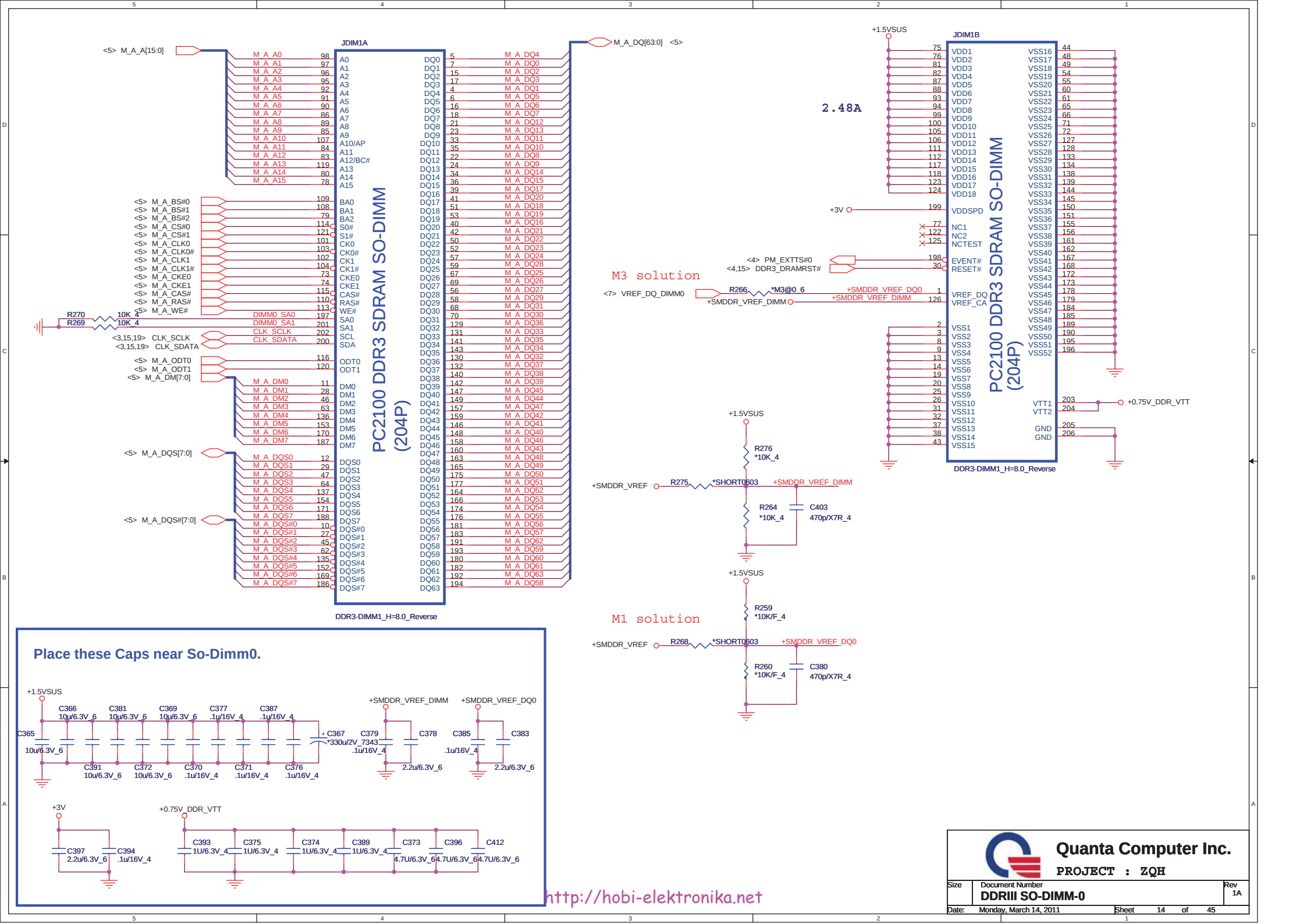


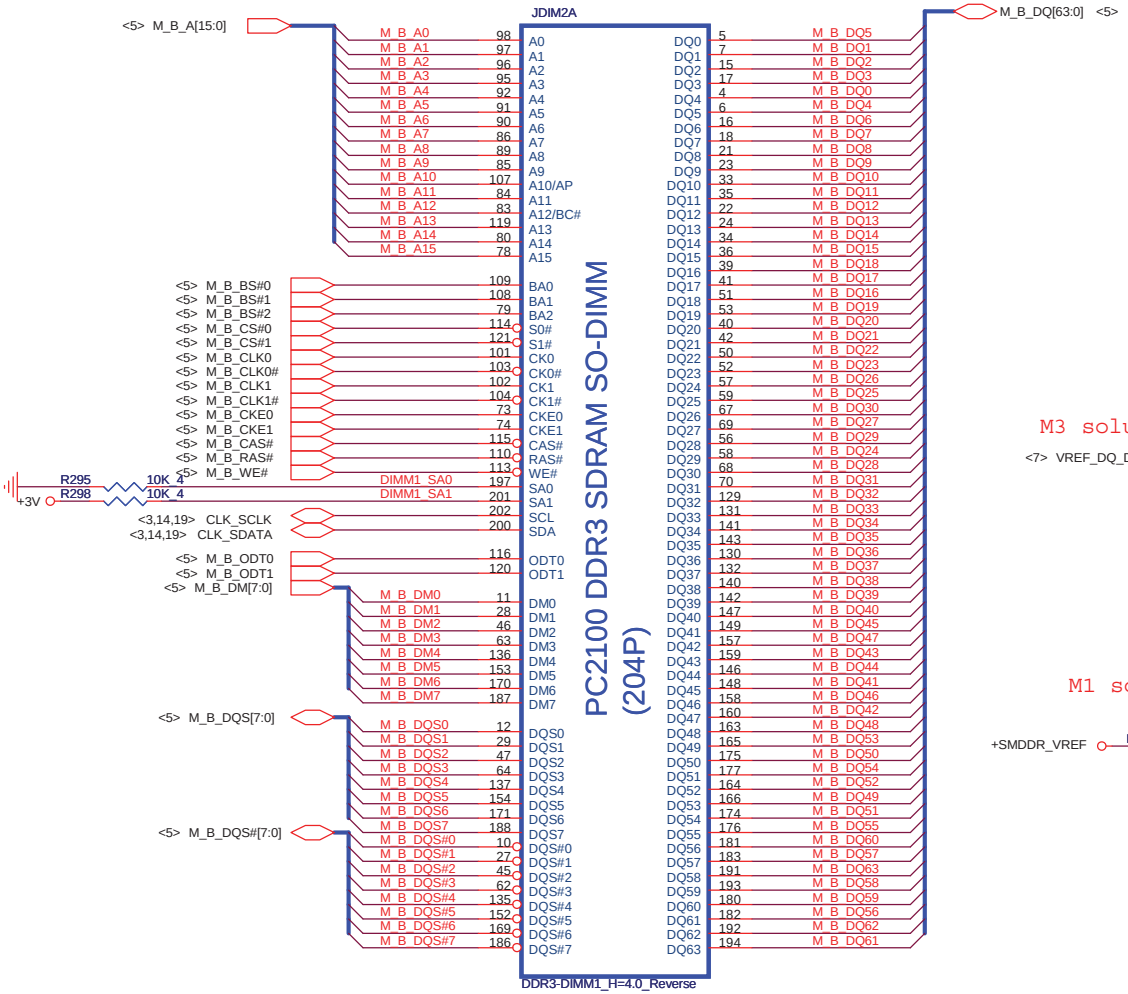
Quanta Computer Inc.

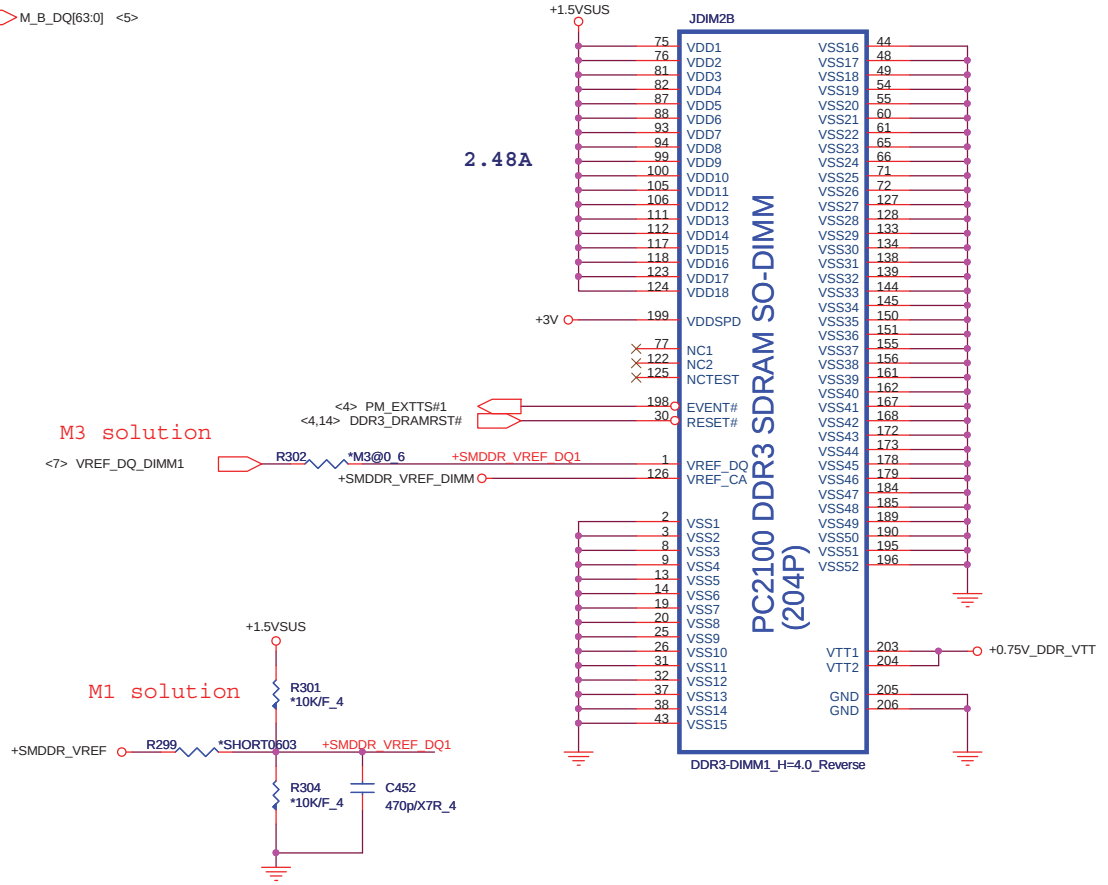
PROJECT : ZQH

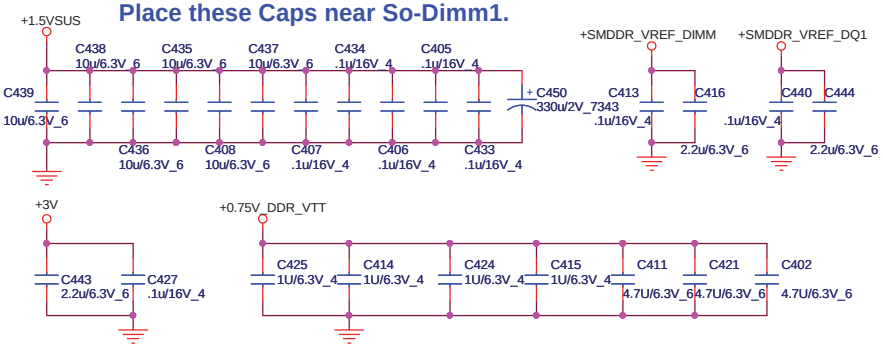
Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

Date: Monday, March 14, 2011 Sheet 13 of 45


JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=8.0_Reverse
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=8.0_Reverse
2.48A
M3 solution
M1 solution
Place these Caps near So-Dimm0.
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : ZQH
DDRIII SO-DIMM-0
Monday, March 14, 2011







Quanta Computer Inc.

PROJECT : ZQH

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Monday, March 14, 2011	Sheet 15 of 35	

CRT Switch

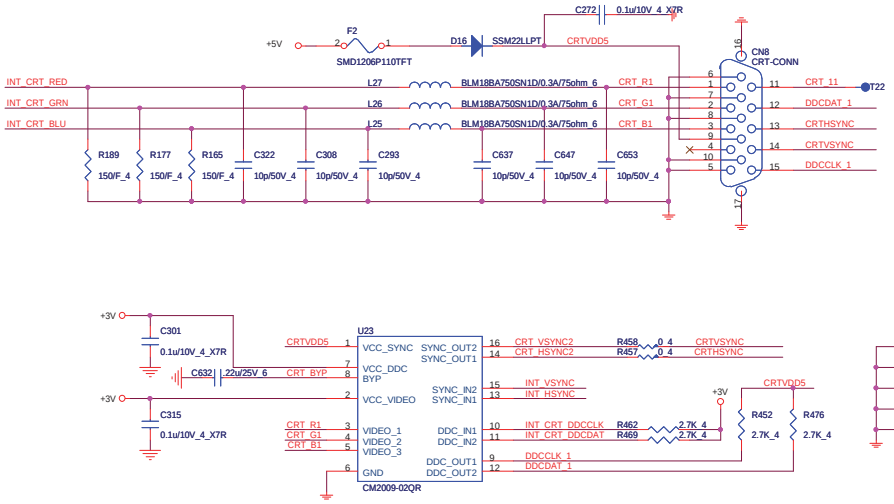
0_ohm Resistor place close to Joint-Point

<8> INT_CRT_RED — INT_CRT_RED
<8> INT_CRT_GRN — INT_CRT_GRN
<8> INT_CRT_BLU — INT_CRT_BLU

<8> INT_VSYNC — INT_VSYNC
<8> INT_HSYNC — INT_HSYNC

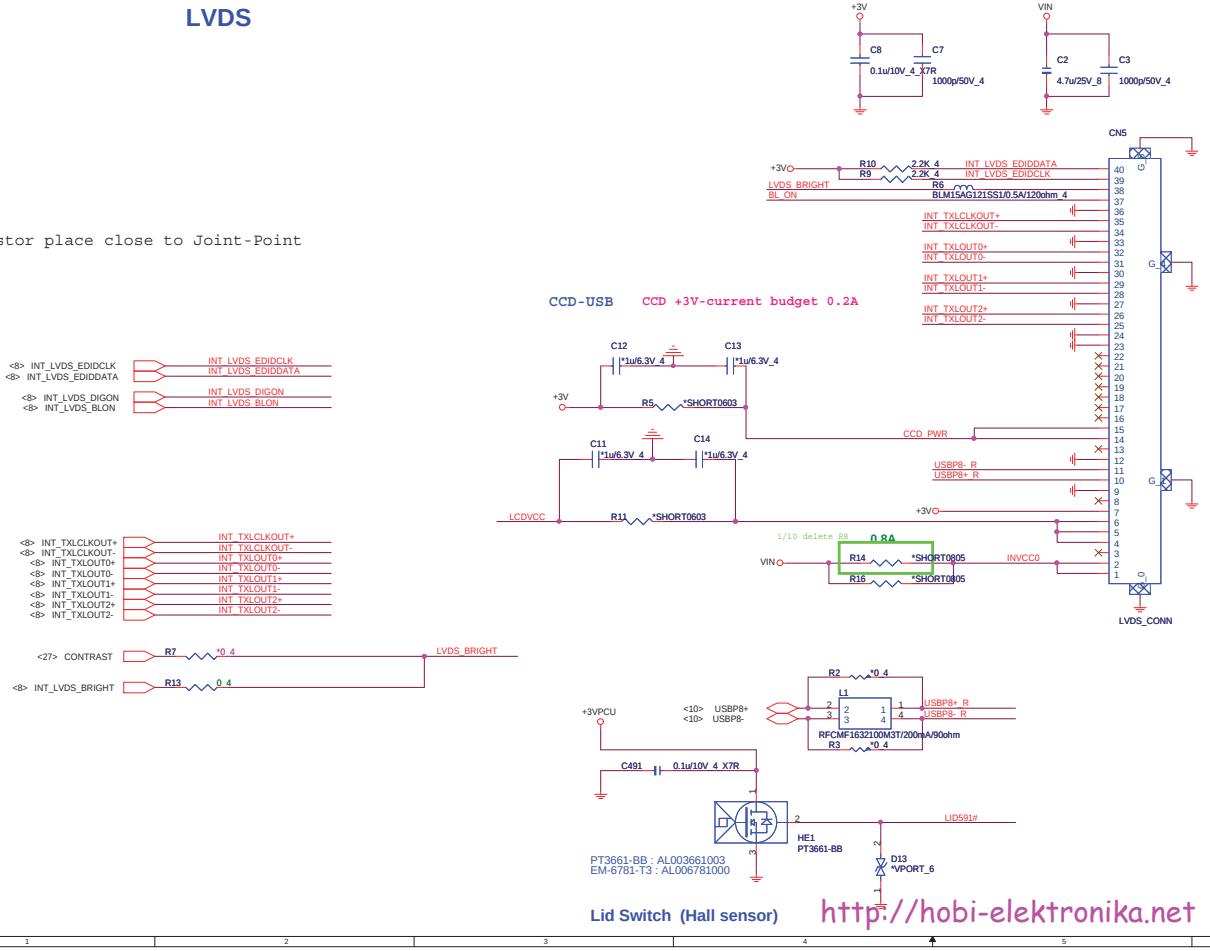
<8> INT_CRT_DDCDAT — INT_CRT_DDCDAT
<8> INT_CRT_DDCCLK — INT_CRT_DDCCLK

CRT

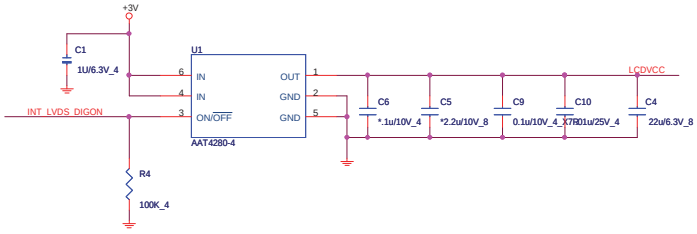


LVDS

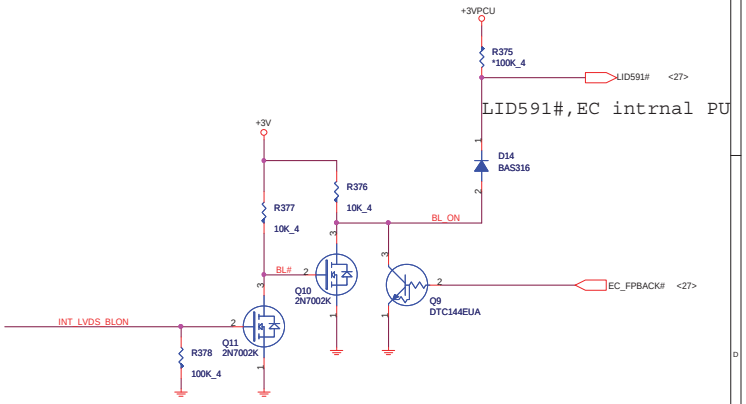
0_ohm Resistor place close to Joint-Point



LCD Power

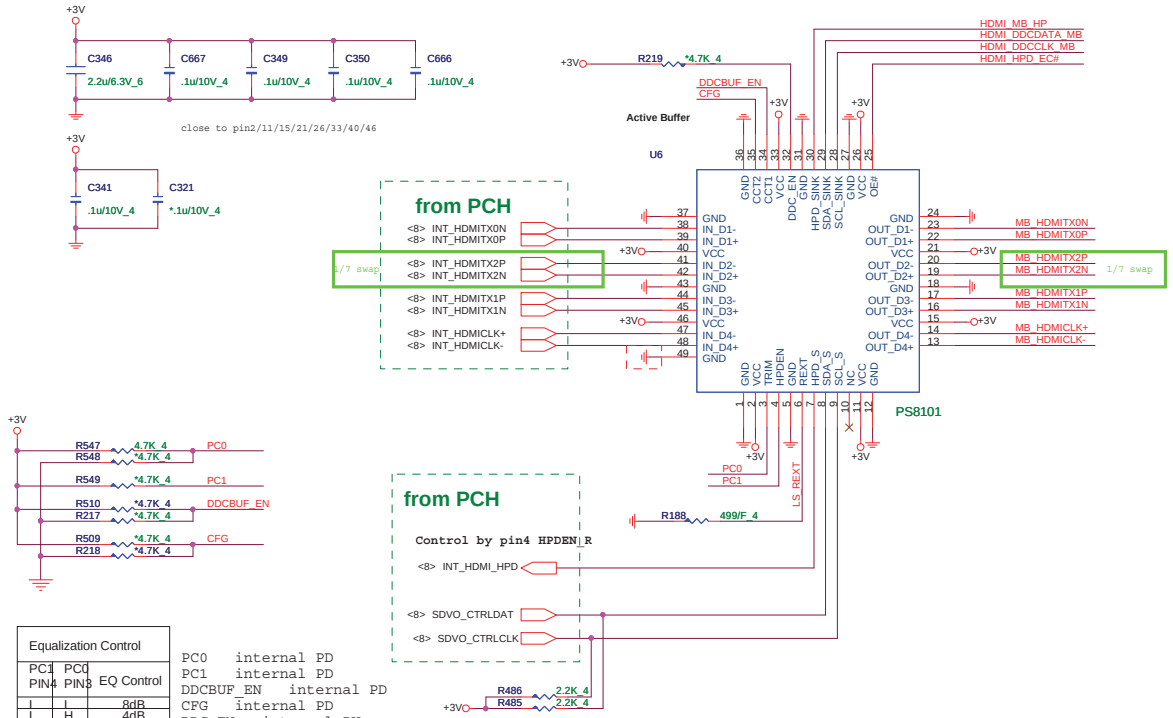


Backlight Control



Quanta Computer Inc.	PROJECT : ZQH	
Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A
Date: Monday, March 14, 2011	Sheet 16 of 35	

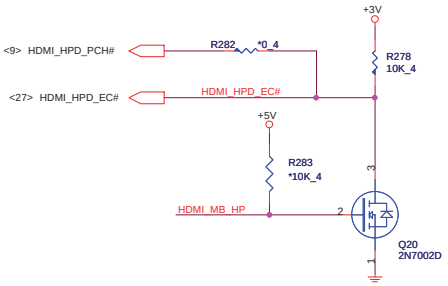
HDMI LEVEL SHIFTER



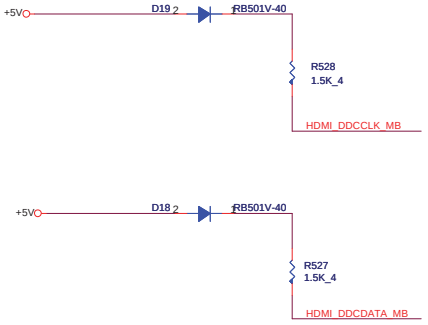
Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

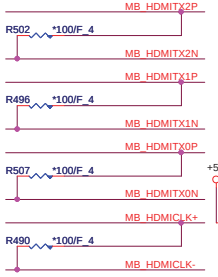
HDMI-detect



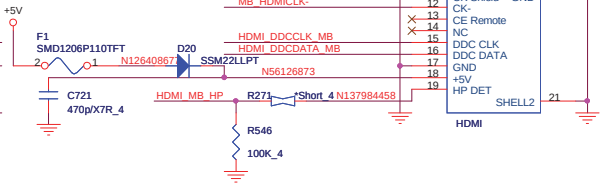
I2C



EMI



HDMI connector



Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	HDMI (PS8101)	1A
Date: Monday, March 14, 2011	Sheet 17 of 35	

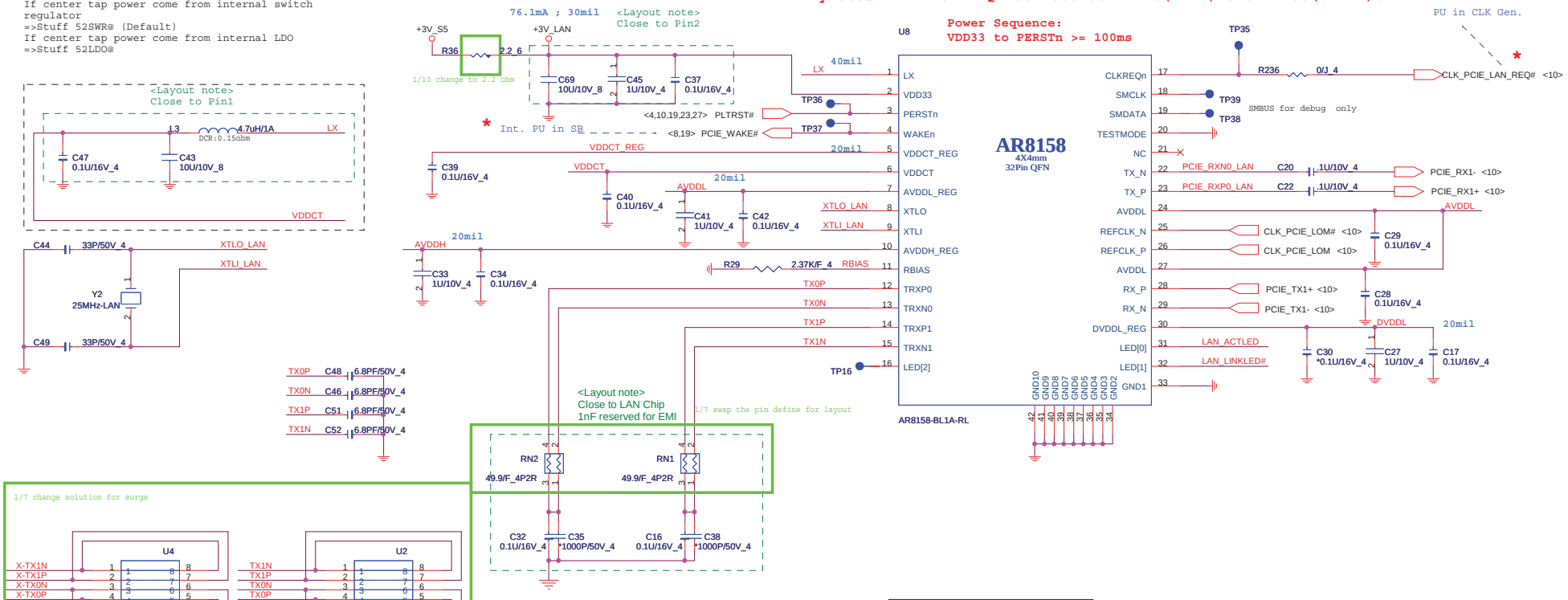
LAN (LAN)

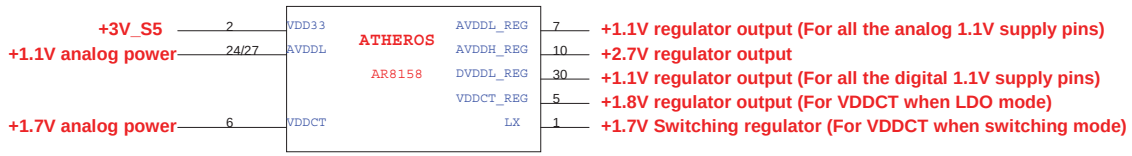
<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

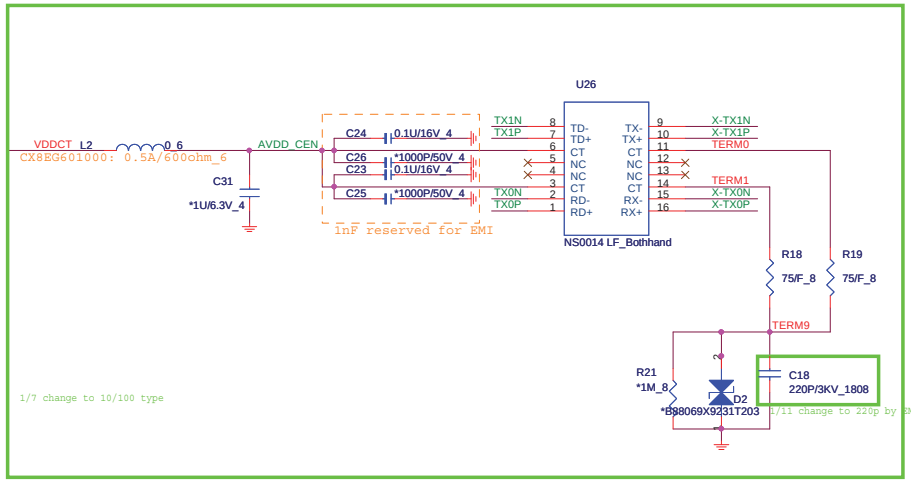
Power Sequence:
VDD33 to PERSTn >= 100ms

PU in CLK Gen.

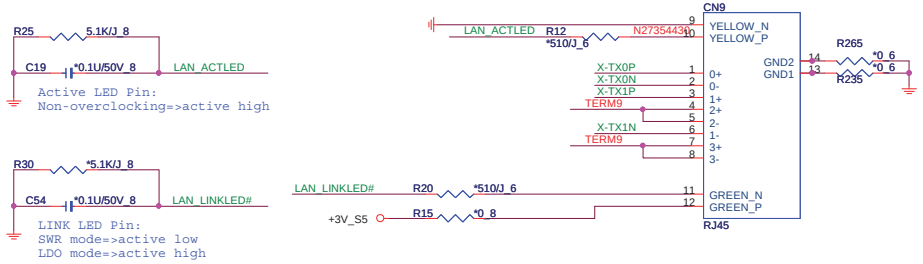




TRANSFORMER (LAN)



RJ45 Connector (LAN)



Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	LAN AR8158L	1A
Date: Monday, March 14, 2011	Sheet 18 of 35	

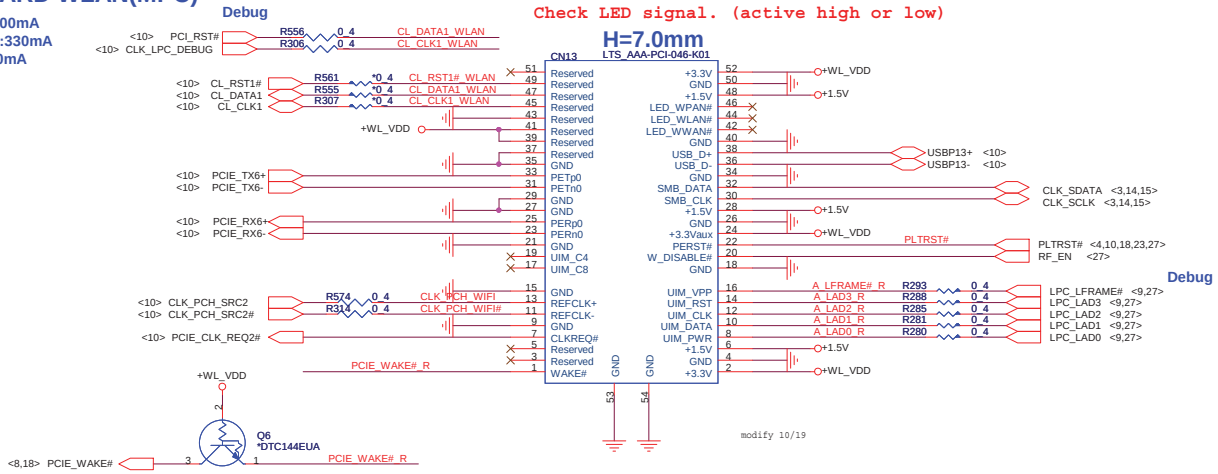
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Debug

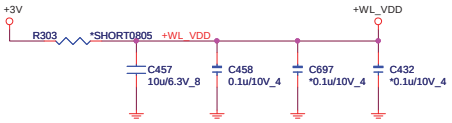
Check LED signal. (active high or low)

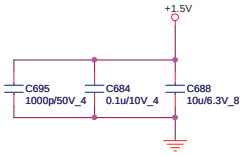
H=7.0mm



Debug

modify 10/19



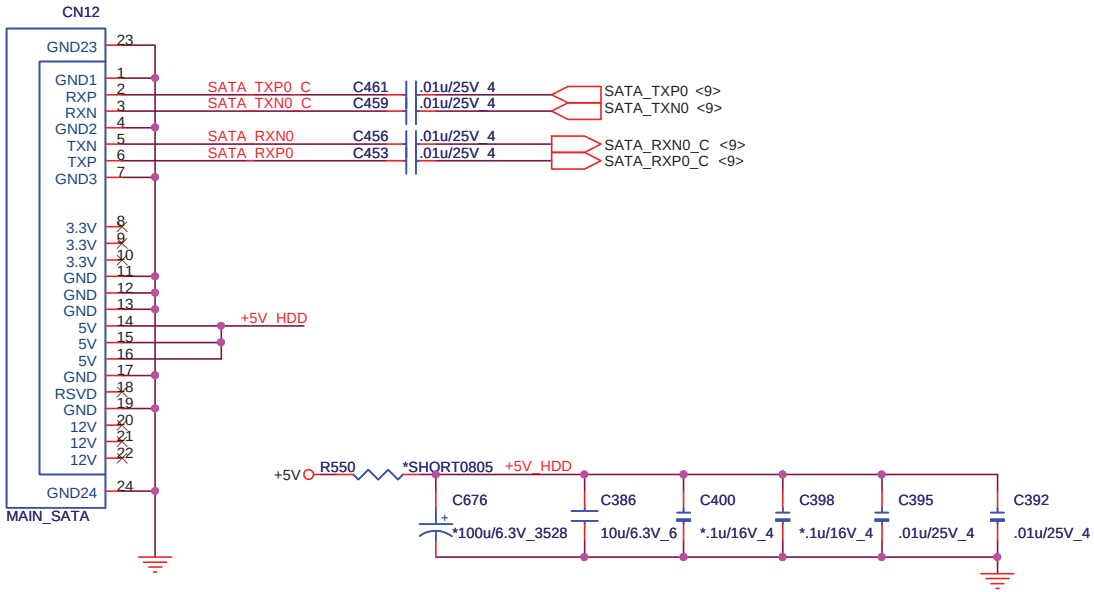


Quanta Computer Inc.
PROJECT : ZQH

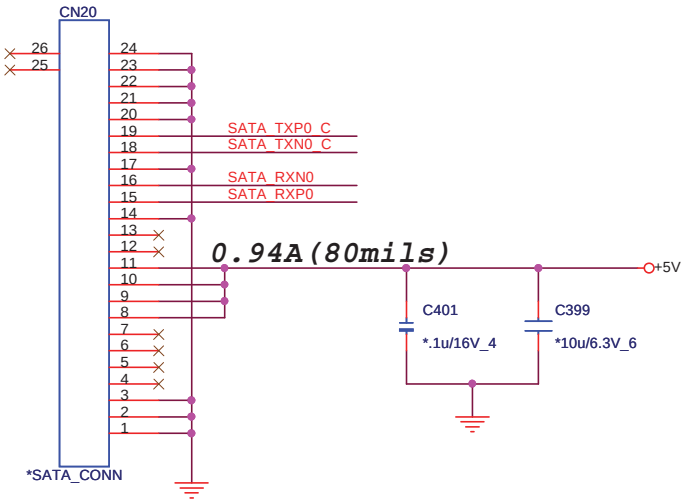
Size	Document Number	Rev
	MINI PCI-E card/TV	1A

Date: Monday, March 14, 2011 Sheet 19 of 45

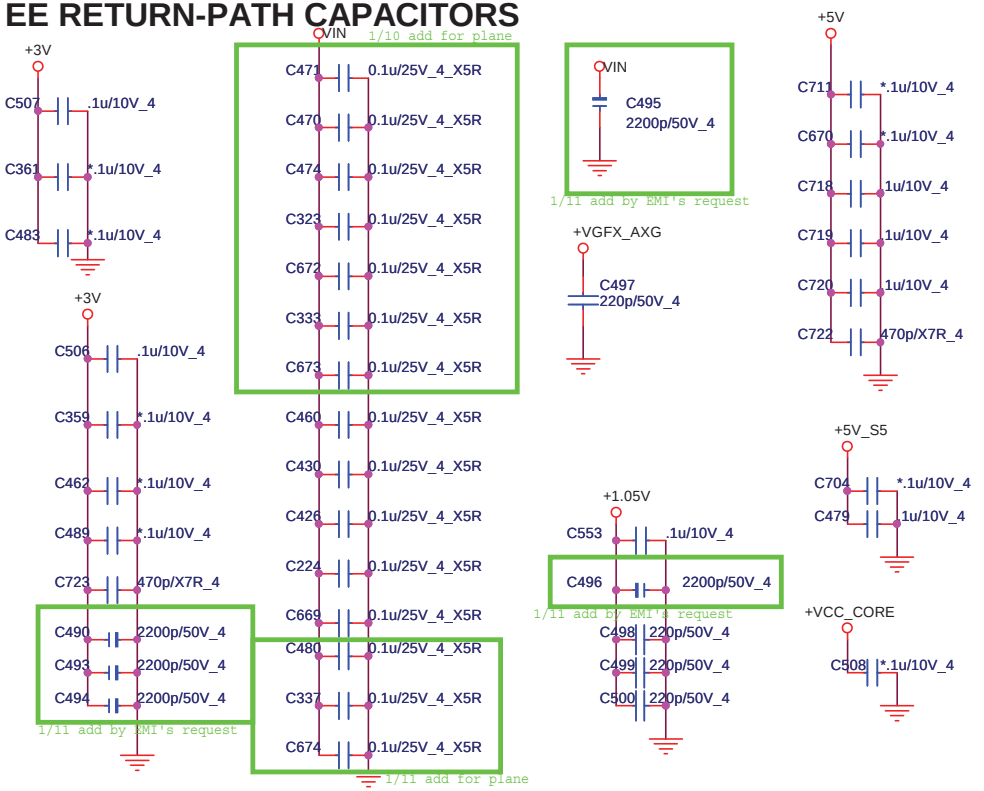
MAIN SATA HDD



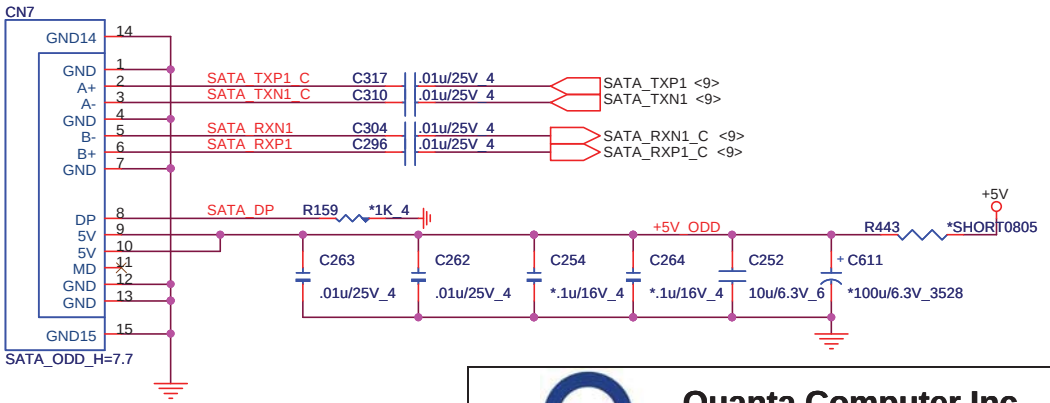
2.5" SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)

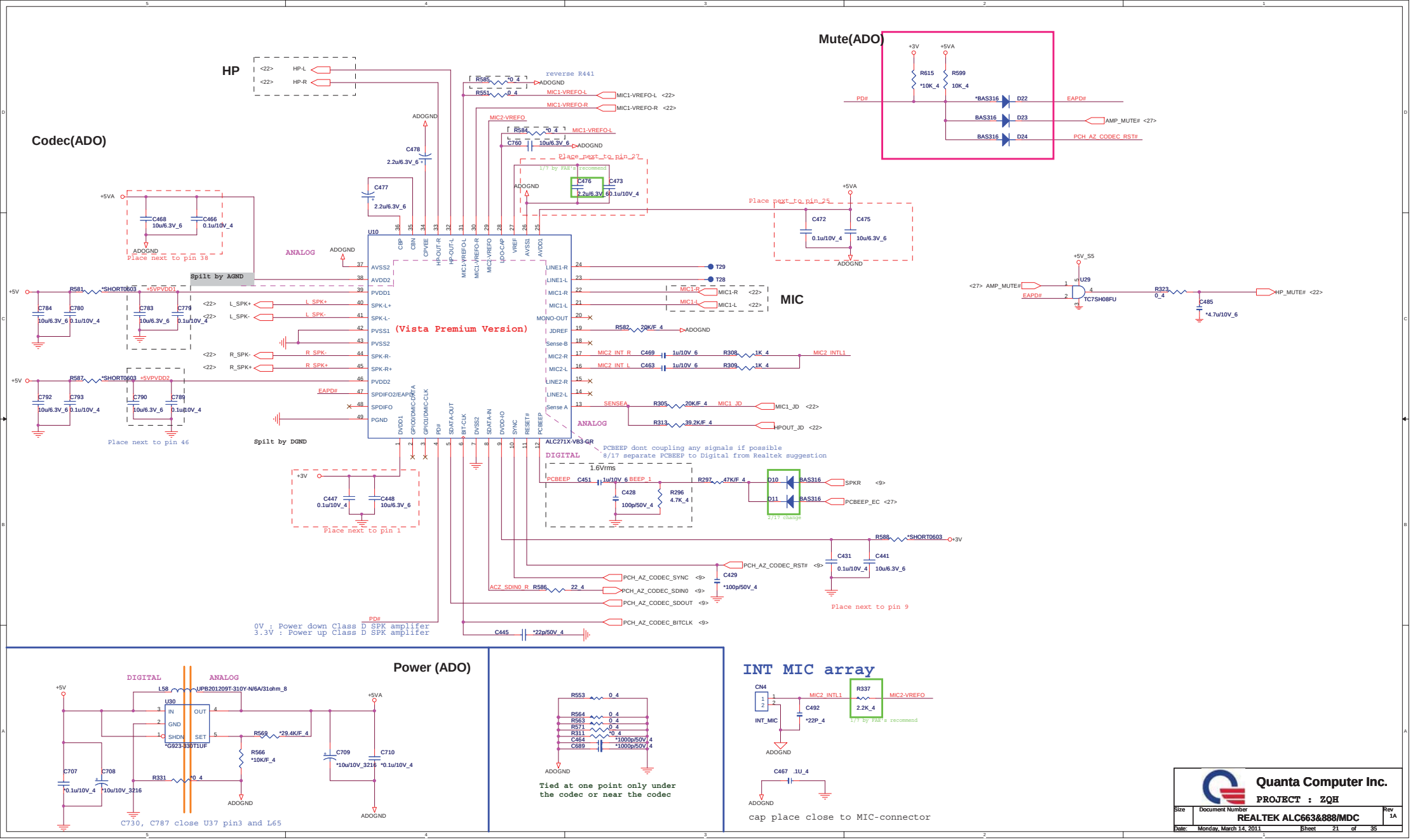


Quanta Computer Inc.

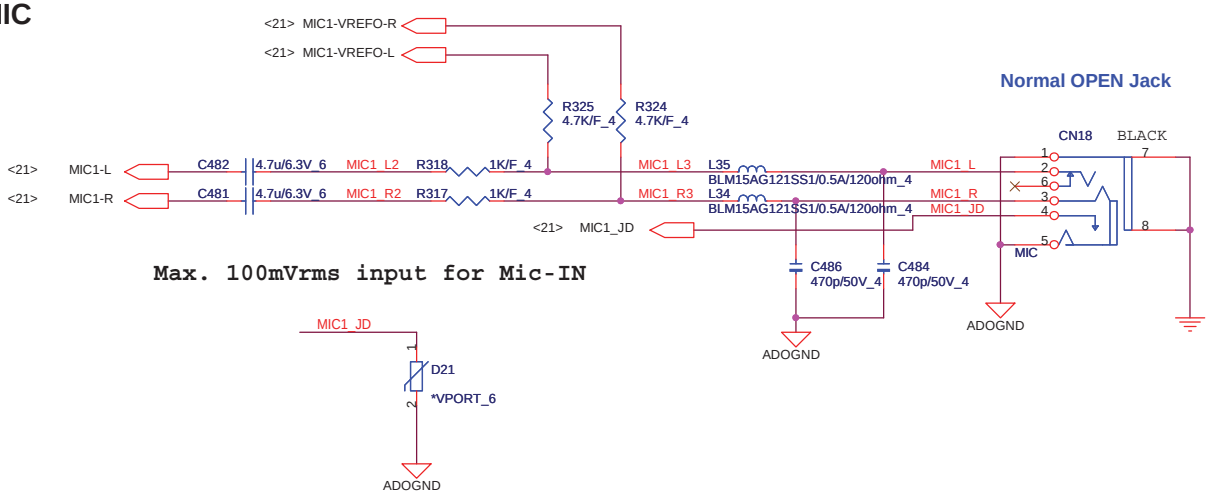
PROJECT : ZQH

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A

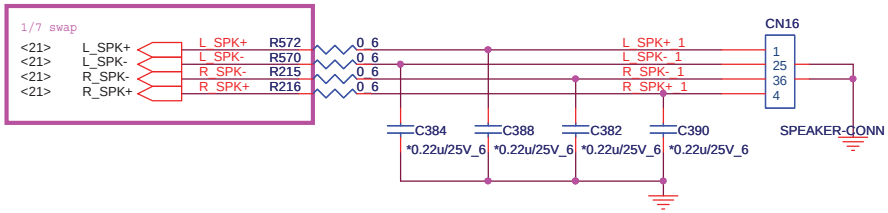
Date: Monday, March 14, 2011 Sheet 20 of 35



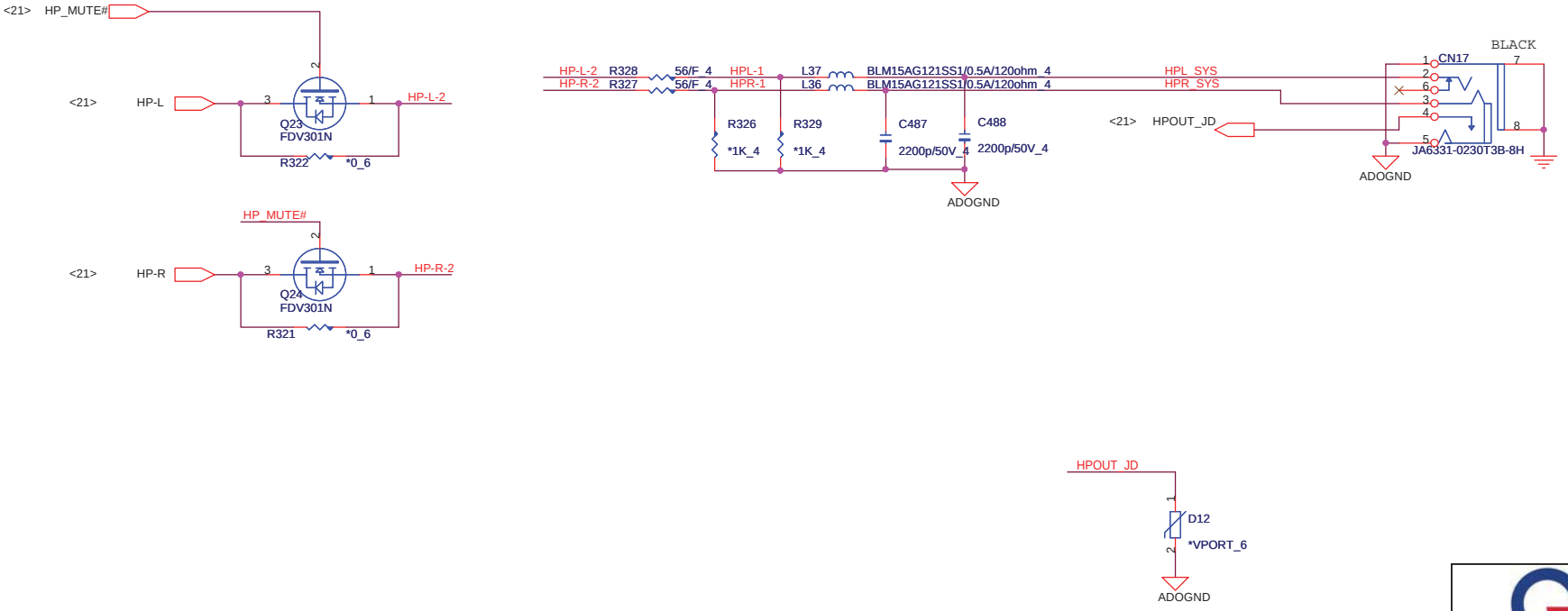
MIC



Internal Speaker



HP/SPDIF



Quanta Computer Inc.

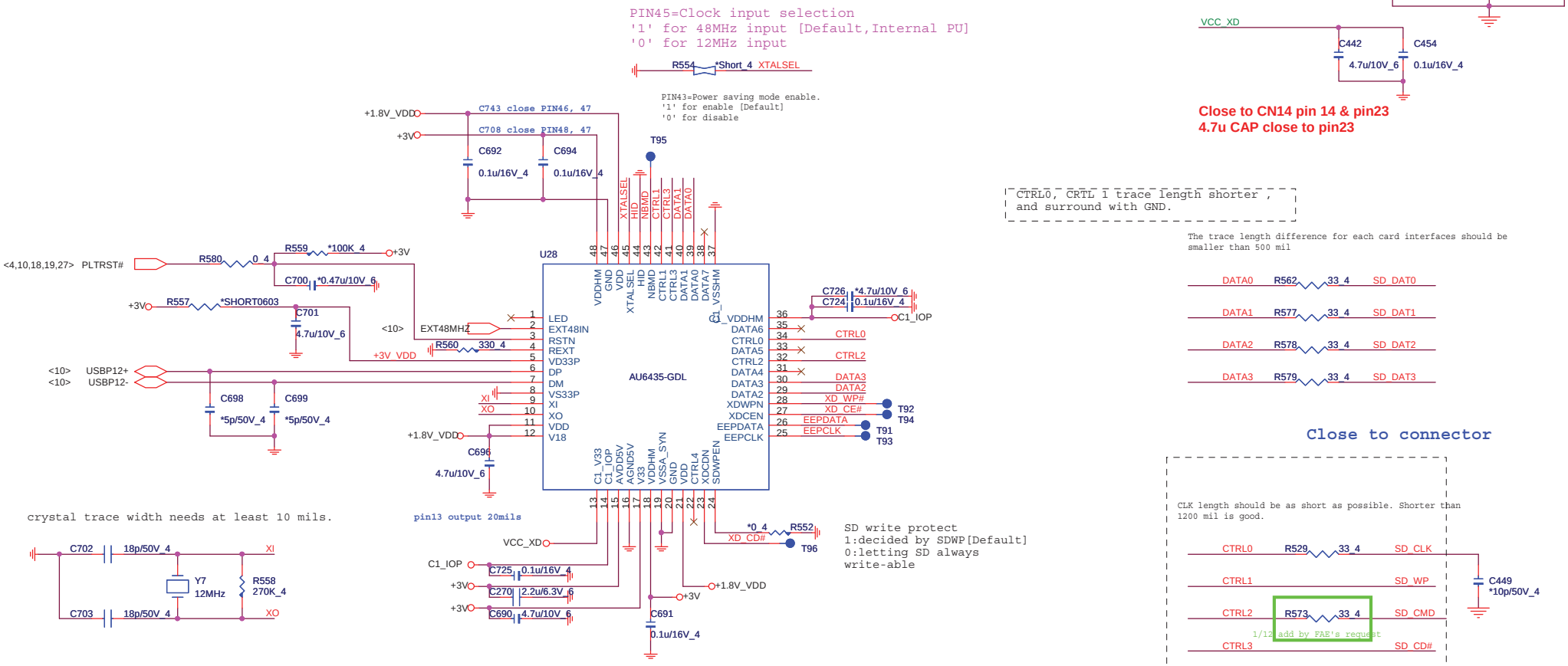
PROJECT : ZQH

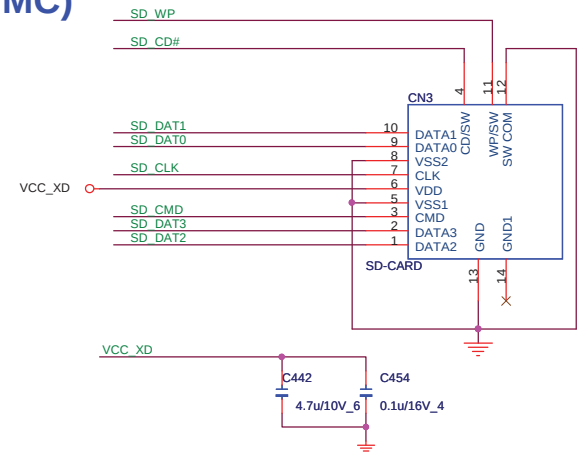
Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Monday, March 14, 2011	Sheet 22 of 35	

CARD READER Controller
AU6435-GDL

2 IN 1 CARD READER (SD/MMC)

Main	DFHS11FR011
Second	DFHS11FR033





Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

CTRL0, CRTL 1 trace length shorter , and surround with GND.

The trace length difference for each card interfaces should be smaller than 500 mil

Close to connector

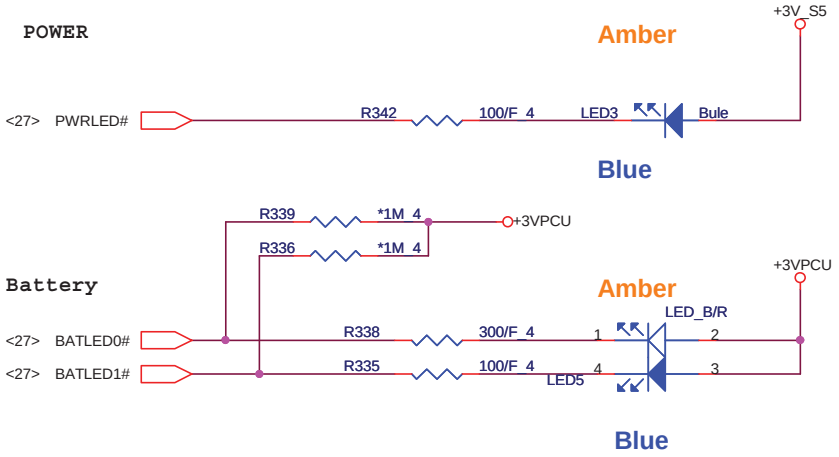
CLK length should be as short as possible. Shorter than 1200 mil is good.

http://hobi-elektronika.net

PROJECT : ZQ5
Quanta Computer Inc.

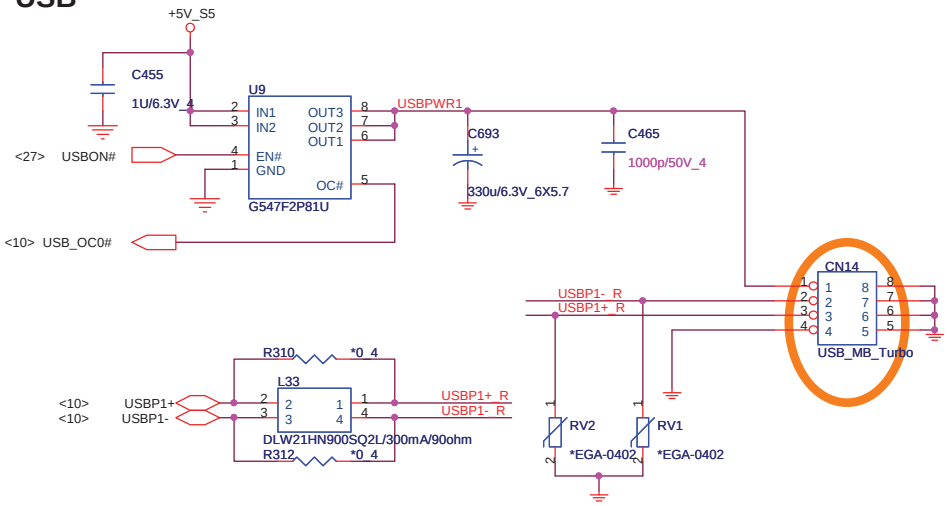
Size	Document Number	Rev
	AU6433 CardReader	1A
Date:	Monday, March 14, 2011	Sheet 23 of 43

LED

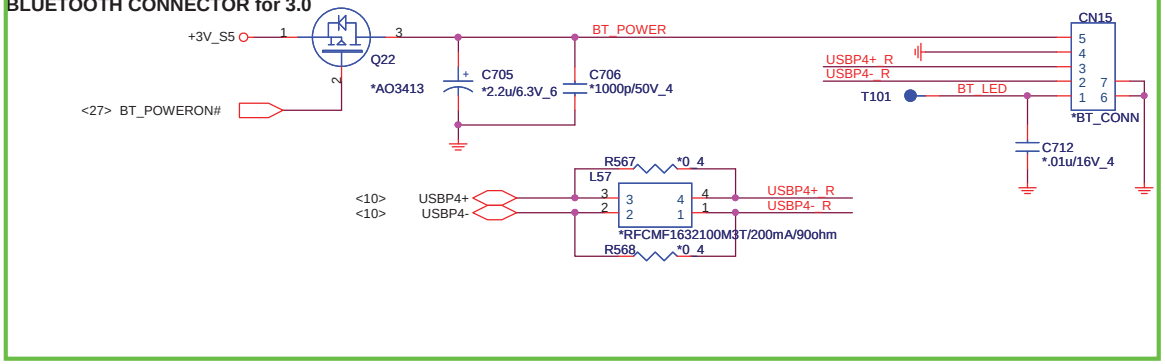


Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number: POWER/MMB/LAUNCH/LED	Rev: 1A
Date: Monday, March 14, 2011	Sheet 24 of 35	

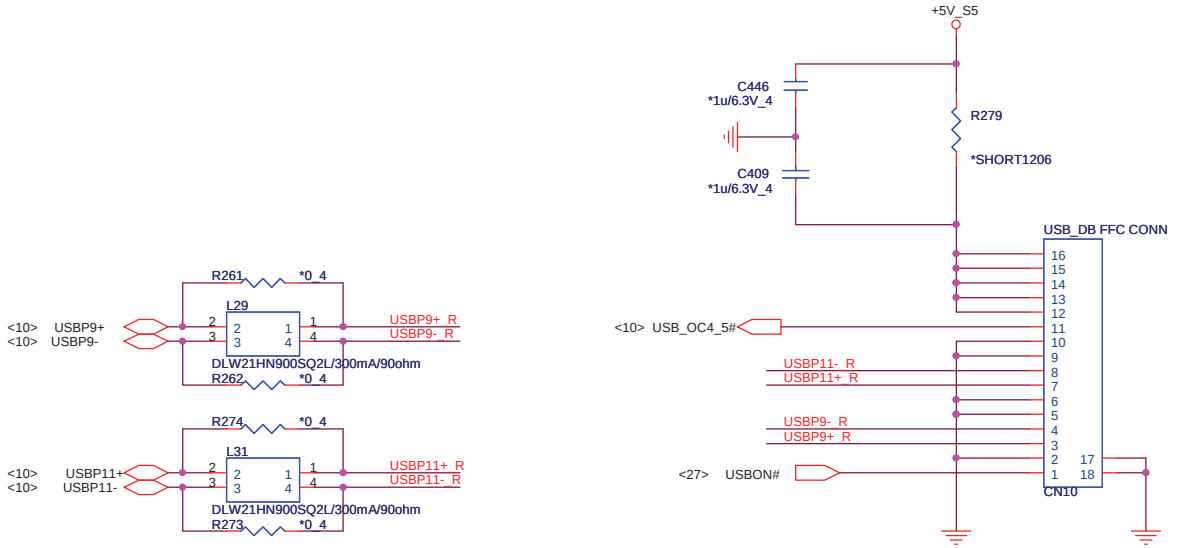
USB



BLUETOOTH CONNECTOR for 3.0



USB/B

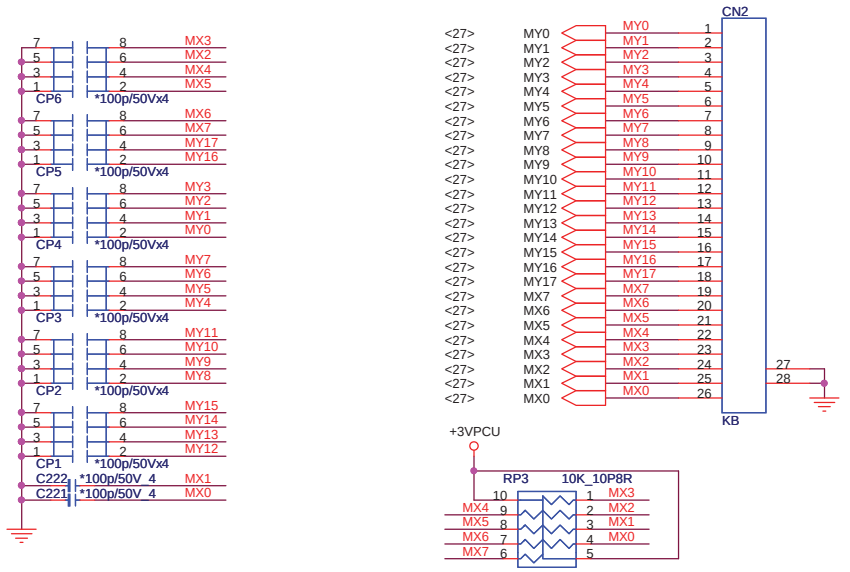


Quanta Computer Inc.

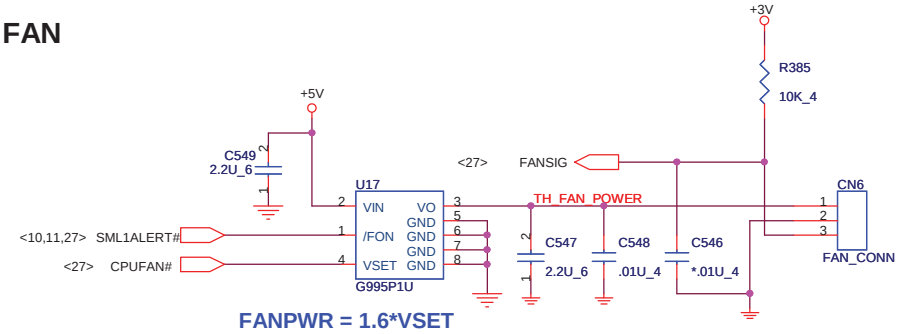
PROJECT : ZQH

Size	Document Number	Rev
	USB/ BT	1A
Date: Monday, March 14, 2011	Sheet 25 of 35	

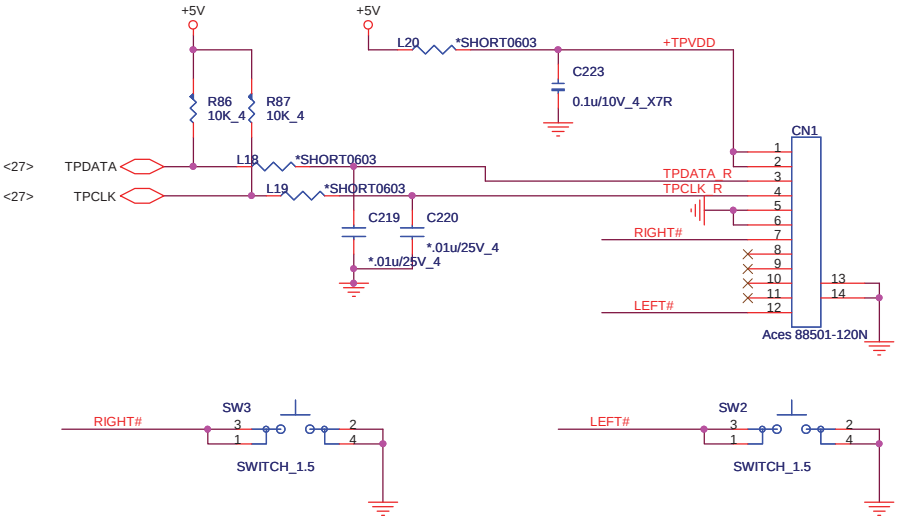
K/B



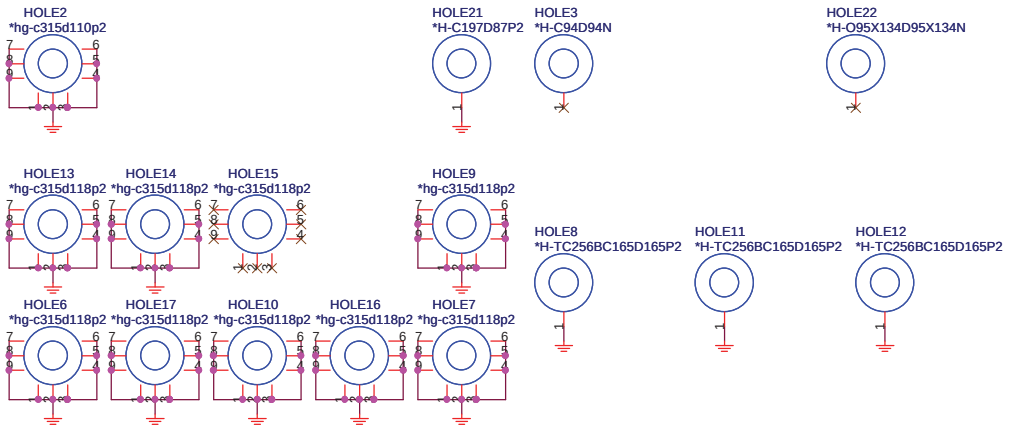
CPU FAN



TOUCHPAD & Switch CONN.



HOLE



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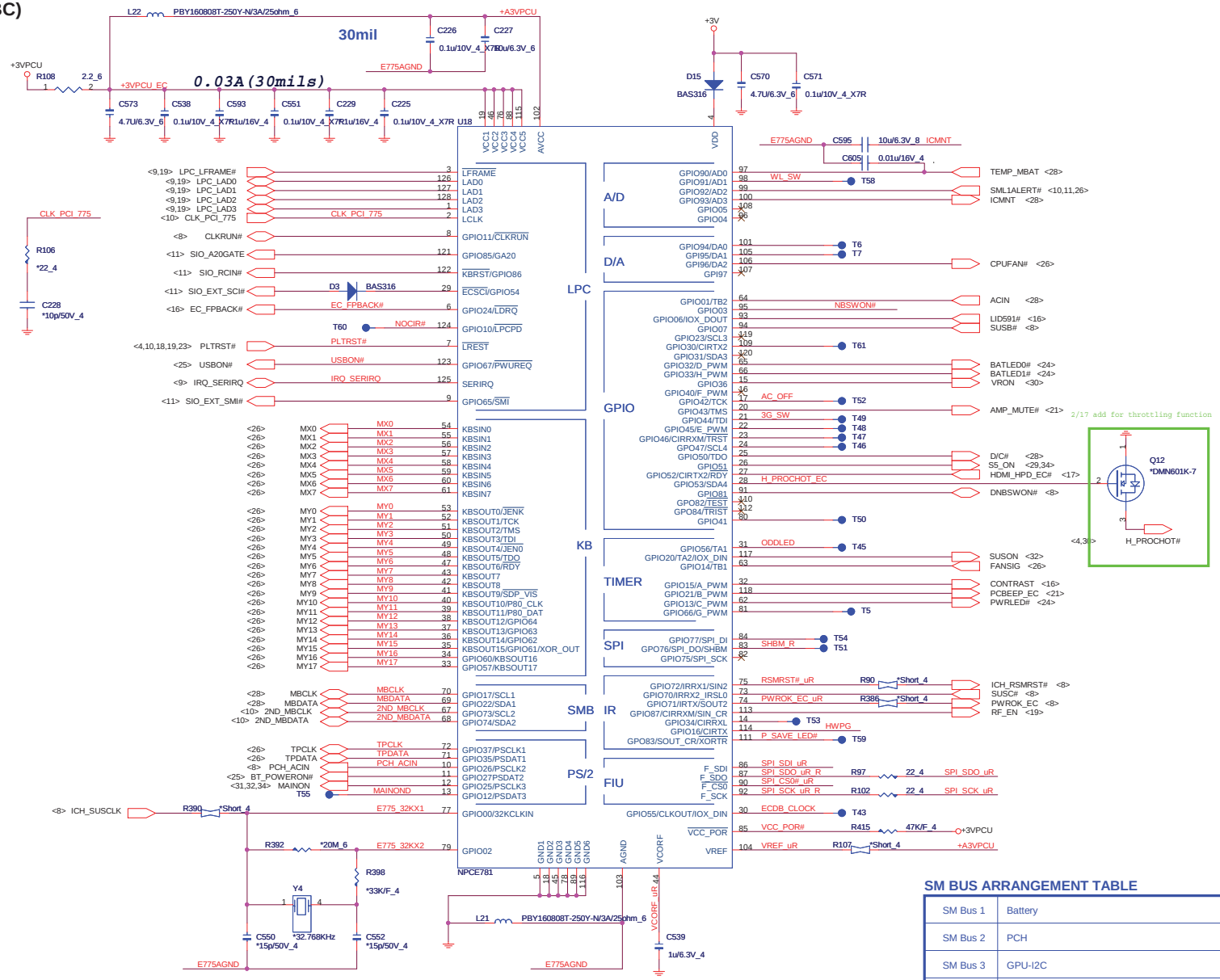
PROJECT : ZQH

Size	Document Number	Rev
	KB/FAN/TP+FP	1A
Date: Monday, March 14, 2011	Sheet 26 of 35	

EC(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

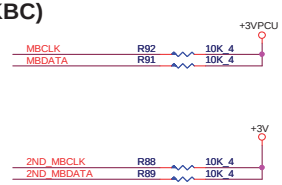
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

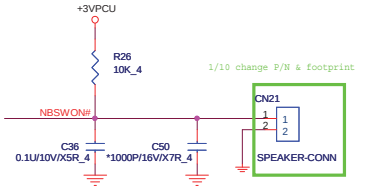
SHBM — SHBM_R — R405 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

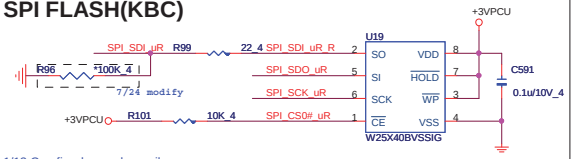
SM BUS PU(KBC)



PWR/B

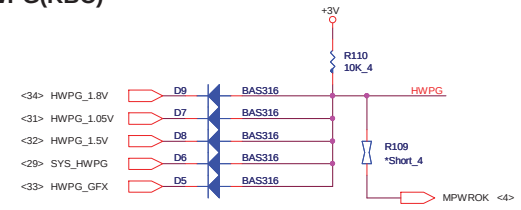


SPI FLASH(KBC)

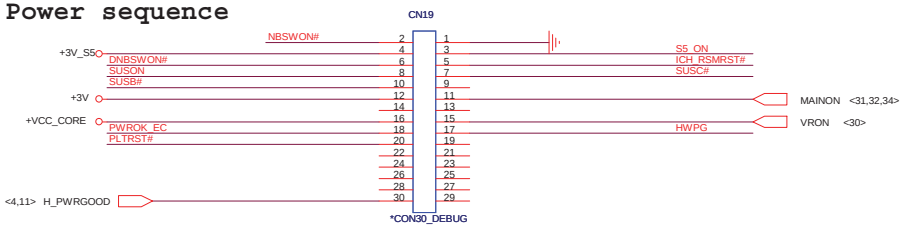


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

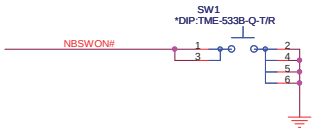
HWPG(KBC)



Power sequence

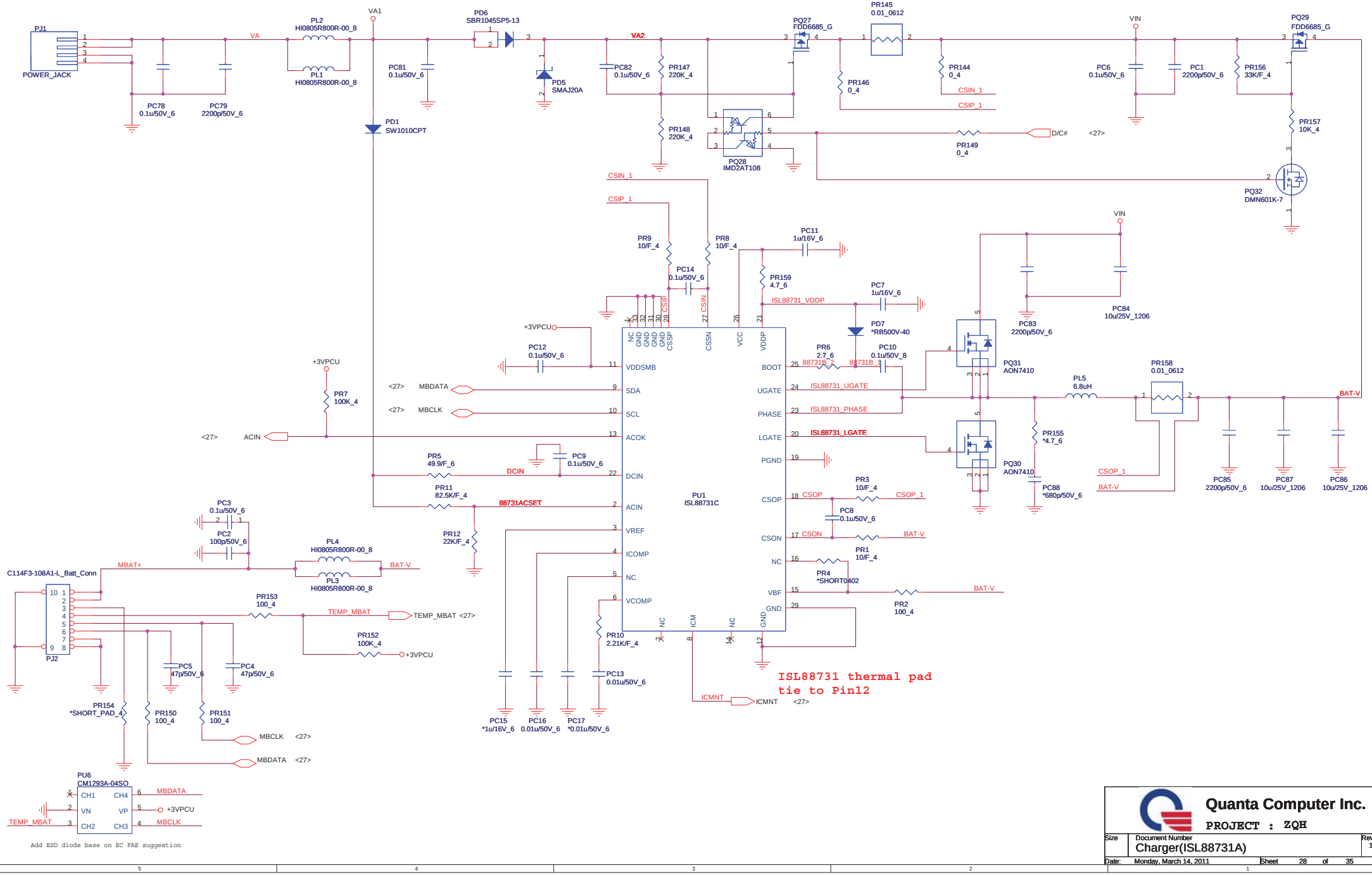


POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

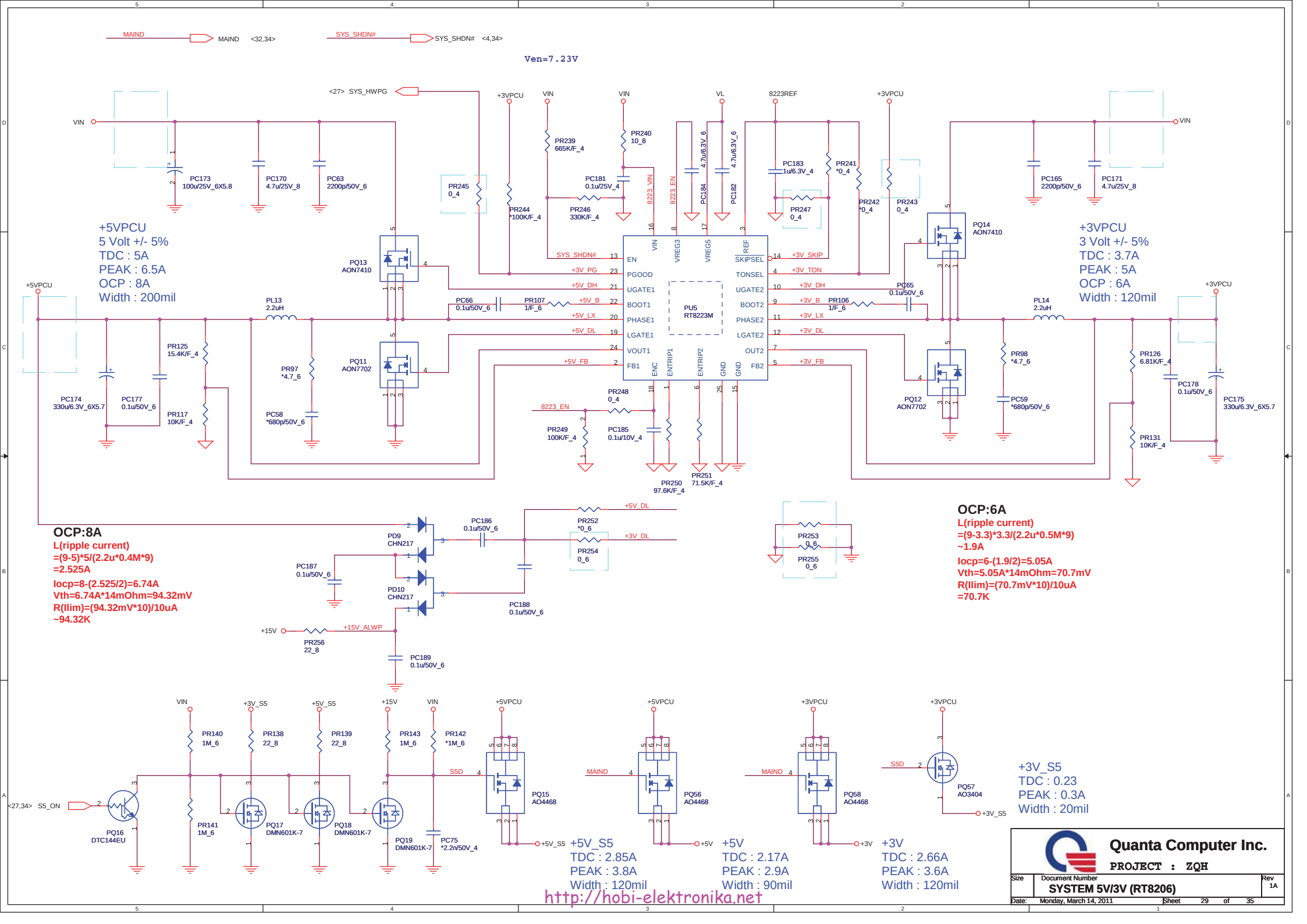
Quanta Computer Inc.			
PROJECT : ZQH			
Size	Document Number		Rev
	WPCE781 & FLASH		1A
Date: Monday, March 14, 2011		Sheet 27 of 35	

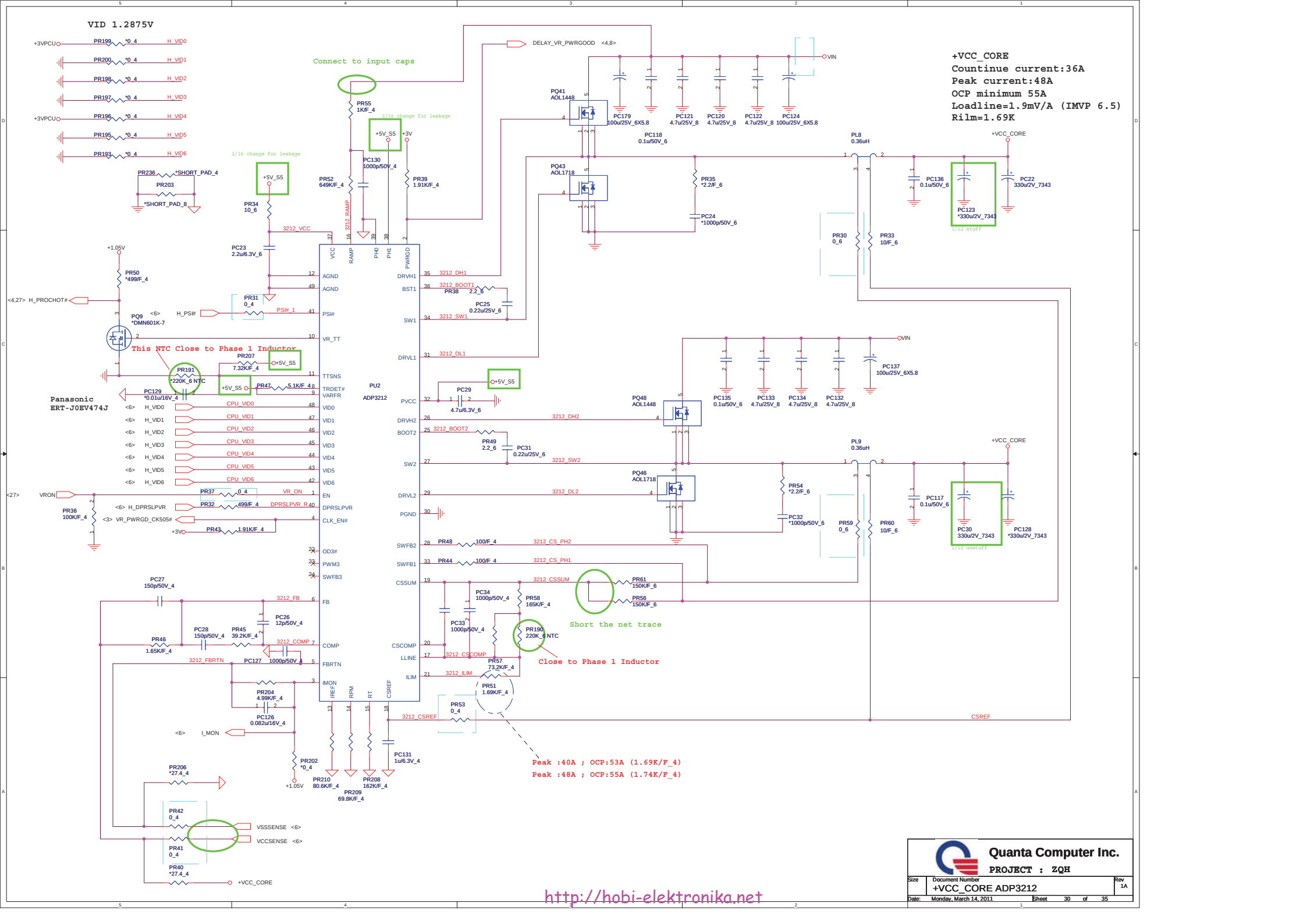


Quanta Computer Inc.

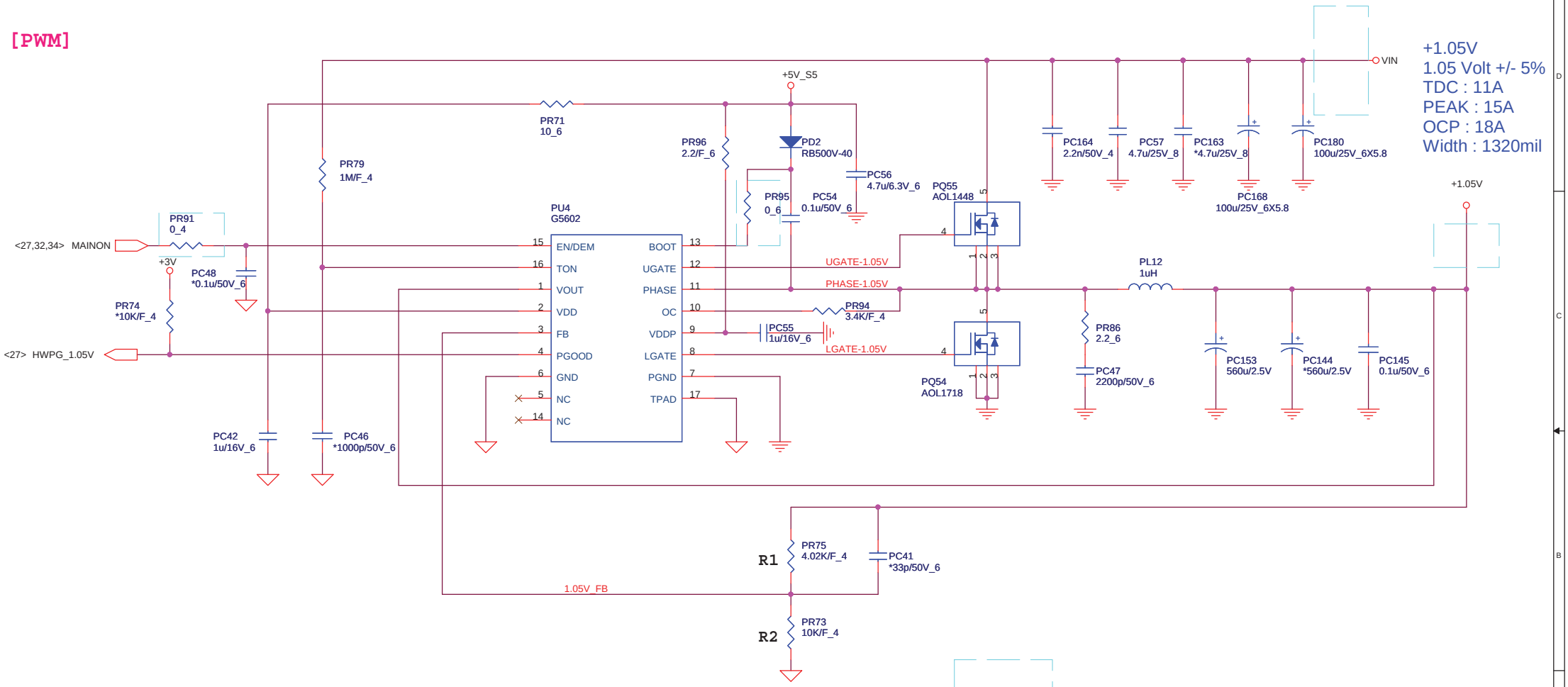
PROJECT : ZQH

Size	Document Number	Rev
	Charger(ISL88731A)	1A
Date: Monday, March 14, 2011	Sheet 28 of 35	


MAIND
MAIND <32,34>
SYS_SHDN#
SYS_SHDN# <4,34>
Ven=7.23V
<27> SYS_HWPG
+5VPCU
5 Volt +/- 5%
TDC : 5A
PEAK : 6.5A
OCP : 8A
Width : 200mil
+3VPCU
3 Volt +/- 5%
TDC : 3.7A
PEAK : 5A
OCP : 6A
Width : 120mil
PU5
RT8223M
PQ13 AON7410
PQ11 AON7702
PQ14 AON7410
PQ12 AON7702
PL13 2.2uH
PL14 2.2uH
OCP:8A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=8-(2.525/2)=6.74A
Vth=6.74A*14mOhm=94.32mV
R(Ilim)=(94.32mV*10)/10uA
~94.32K
OCP:6A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=6-(1.9/2)=5.05A
Vth=5.05A*14mOhm=70.7mV
R(Ilim)=(70.7mV*10)/10uA
=70.7K
PD9 CHN217
PD10 CHN217
PQ15 AO4468
PQ56 AO4468
PQ58 AO4468
PQ57 AO3404
PQ16 DTC144EU
PQ17 DMN601K-7
PQ18 DMN601K-7
PQ19 DMN601K-7
+3V_S5
TDC : 0.23
PEAK : 0.3A
Width : 20mil
+5V_S5
TDC : 2.85A
PEAK : 3.8A
Width : 120mil
+5V
TDC : 2.17A
PEAK : 2.9A
Width : 90mil
+3V
TDC : 2.66A
PEAK : 3.6A
Width : 120mil
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : ZQH
SYSTEM 5V/3V (RT8206)
Rev 1A
Monday, March 14, 2011
Sheet 29 of 35


VID 1.2875V
+VCC_CORE
Countinue current:36A
Peak current:48A
OCP minimum 55A
Loadline=1.9mV/A (IMVP 6.5)
Rilm=1.69K
Connect to input caps
DELAY_VR_PWRGOOD <4,8>
VIN
+3VPCU
PR199 *0_4 H_VID0
PR200 *0_4 H_VID1
PR198 *0_4 H_VID2
PR197 *0_4 H_VID3
PR196 *0_4 H_VID4
PR195 *0_4 H_VID5
PR193 *0_4 H_VID6
PR236 *SHORT_PAD_4
PR203 *SHORT_PAD_8
2/16 change for leakage
PR55 1K/F_4
PR52 649K/F_4
PC130 1000p/50V_4
PR39 1.91K/F_4
PR34 10_6
3212_VCC
3212_RAMP
PC23 2.2u/6.3V_6
+1.05V
PR50 *499/F_4
PR31 0_4
PSI# 1
PQ9 *DMN601K-7
<4,27> H_PROCHOT#
H_PSI#
This NTC Close to Phase 1 Inductor
PR207 7.32K/F_4
PR191 *220K_6 NTC
PR47 5.1K/F_4
PC129 *0.01u/16V_4
Panasonic
ERT-J0EV474J
PU2
ADP3212
VCC
RAMP
PHD
PH1
PWRGD
AGND
DRVH1
BST1
SW1
DRVL1
VR_TT
TTSNS
TRDET#
VARFR
VID0
VID1
VID2
VID3
VID4
VID5
VID6
EN
DPRSLPVR
CLK_EN#
PVCC
DRVH2
BOOT2
SW2
DRVL2
PGND
OD3#
PWM3
SWFB3
SWFB2
SWFB1
CSSUM
CSCOMP
LLINE
ILIM
FB
COMP
FBRTN
IMON
IREF
RPM
RT
CSREF
3212_DH1
3212_BOOT1
3212_SW1
3212_DL1
3212_DH2
3212_BOOT2
3212_SW2
3212_DL2
PR38 2.2_6
PC25 0.22u/25V_6
PR49 2.2_6
PC31 0.22u/25V_6
PC29 4.7u/6.3V_6
PR48 100/F_4
PR44 100/F_4
3212_CS_PH2
3212_CS_PH1
3212_CSSUM
3212_CSCOMP
3212_ILIM
3212_CSREF
PR58 165K/F_4
PC34 1000p/50V_4
PC33 1000p/50V_4
PR190 220K_4 NTC
PR57 73.2K/F_4
PR51 1.69K/F_4
PR53 0_4
Short the net trace
Close to Phase 1 Inductor
Peak :40A ; OCP:53A (1.69K/F_4)
Peak :48A ; OCP:55A (1.74K/F_4)
PR61 150K/F_6
PR56 150K/F_6
PC27 150p/50V_4
PC26 12p/50V_4
PR46 1.65K/F_4
PC28 150p/50V_4
PR45 39.2K/F_4
PC127 1000p/50V_4
PR204 4.99K/F_4
PC126 0.082u/16V_4
PR202 *0_4
PR206 *27.4_4
PR42 0_4
PR41 0_4
PR40 *27.4_4
PR210 80.6K/F_4
PR209 69.8K/F_4
PR208 162K/F_4
PC131 1u/6.3V_4
VSSSENSE <6>
VCCSENSE <6>
I_MON
PR36 100K/F_4
PR37 0_4
PR32 499/F_4
PR43 1.91K/F_4
VR_ON
DPRSLPVR_R
<27> VRON
<6> H_DPRSLPVR
<3> VR_PWRGD_CK505#
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPU_VID6
PQ41 AOL1448
PQ43 AOL1718
PQ48 AOL1448
PQ46 AOL1718
PC179 100u/25V_6X5.8
PC121 4.7u/25V_8
PC120 4.7u/25V_8
PC122 4.7u/25V_8
PC124 100u/25V_6X5.8
PC118 0.1u/50V_6
PR35 *2.2/F_6
PC24 *1000p/50V_6
PL8 0.36uH
PC136 0.1u/50V_6
PC123 *330u/2V_7343
PC22 330u/2V_7343
1/12 stuff
PR30 0_6
PR33 10/F_6
PC137 100u/25V_6X5.8
PC135 0.1u/50V_6
PC133 4.7u/25V_8
PC134 4.7u/25V_8
PC132 4.7u/25V_8
PR54 *2.2/F_6
PC32 *1000p/50V_6
PL9 0.36uH
PC117 0.1u/50V_6
PC30 330u/2V_7343
PC128 *330u/2V_7343
1/12 unstuff
PR59 0_6
PR60 10/F_6
CSREF
+VCC_CORE
Quanta Computer Inc.
PROJECT : ZQH
Document Number
+VCC_CORE ADP3212
Rev 1A
Date: Monday, March 14, 2011
Sheet 30 of 35
http://hobi-elektronika.net

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

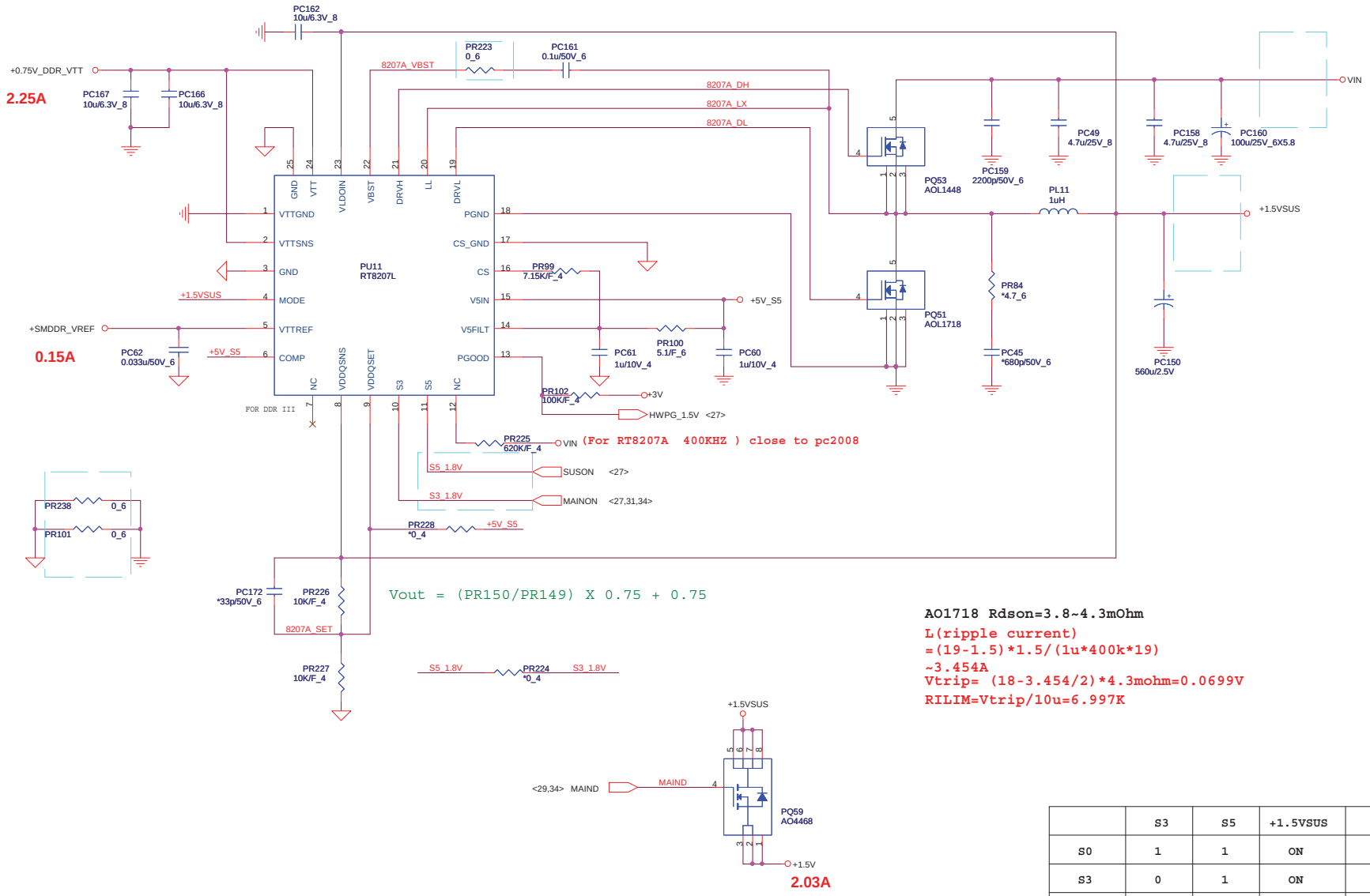
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.647A

RILIM=4.3mohm*18-1.823/20uA=3.477Kohm

I(choke)peak=21.647A

Quanta Computer Inc.		
PROJECT : ZQH		
Size	Document Number: +VTT (G5602R41U)	Rev: 1A
Date: Monday, March 14, 2011	Sheet 31 of 35	

[PWM]



+1.5V_SUS
1 Volt +/- 5%
TDC : 12A
PEAK : 16A
OCP : 18A
Width : 480mil

Vout = (PR150/PR149) X 0.75 + 0.75

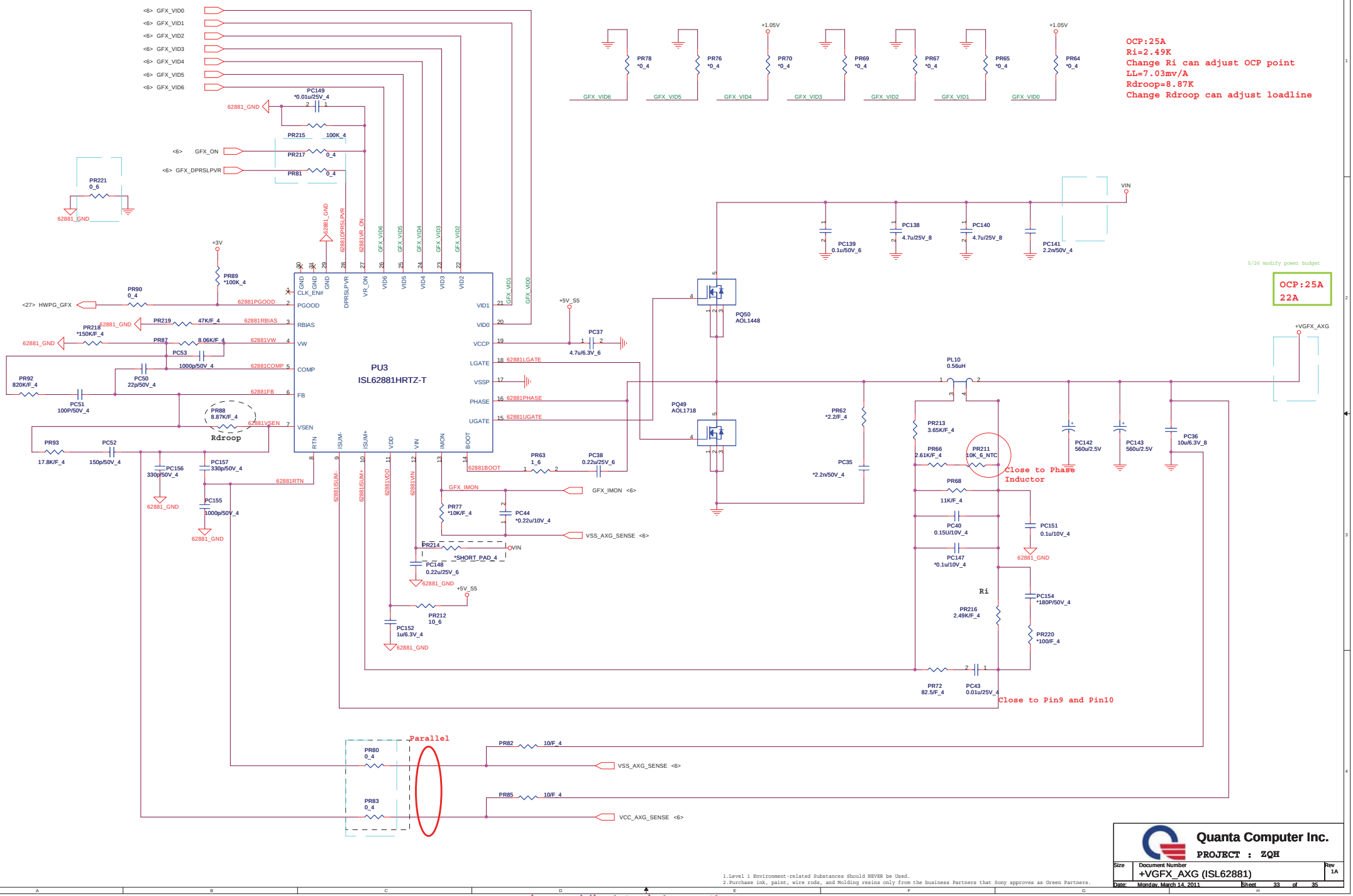
AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A
Vtrip= (18-3.454/2)*4.3mohm=0.0699V
RILIM=Vtrip/10u=6.997K

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQH

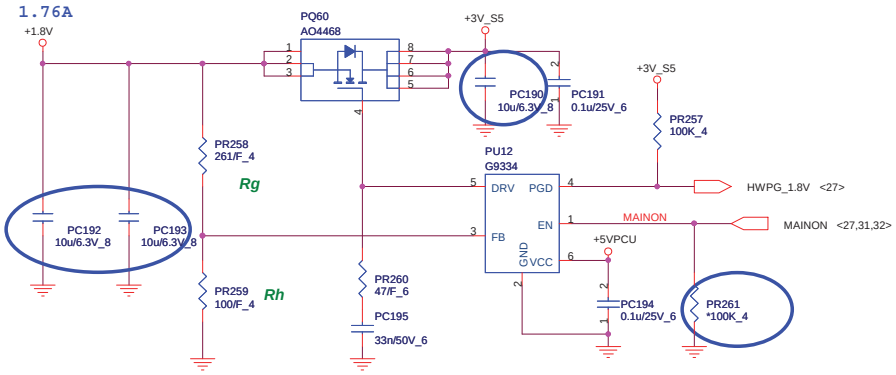
Size	Document Number	Rev
	DDR 1.5V(RT8207A)	1A
Date: Monday, March 14, 2011	Sheet 32 of 35	

Int_VGA [PWM]



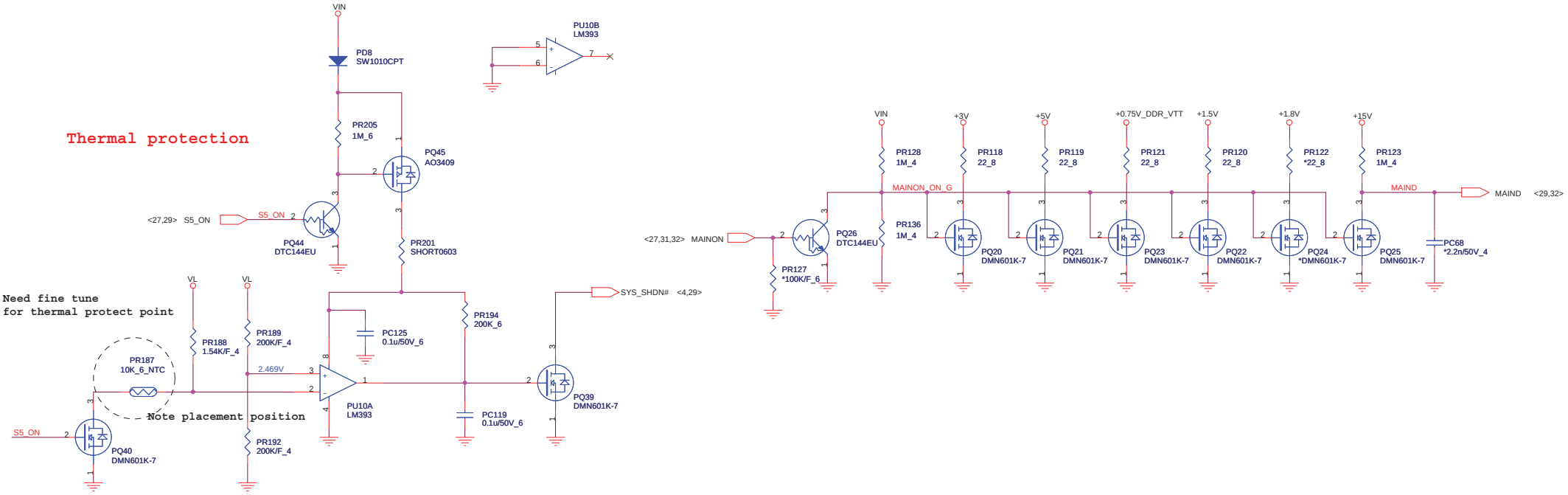
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

+1.8V
1.8 Volt +/- 5%
TDC : 0.76A
PEAK : 1.01A
Width : 40mil



*Vout1 = (1+Rg/Rh)*0.5*

For EC control thermal protection (output 3.3V)



Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	Discharge/1.8V)	1A
Date: Monday, March 14, 2011	Sheet 34 of 35	

1 7/7 modify

CHANGE LIST

Model	REV	CHANGE LIST
ZQH	1A	1/7 page.24 U6 HDMI pin 19,20 & pin 41,42 swap for layout page.30 CN16 speaker conn. pin1,2,3,4 swap for layout page.25 U26 transformer change to 10/100 type page.25 U2, U4 change type, add D2, R21 for surge solution. page.25 RN1, RN2 swap the pin define for layout page.29 R337 change to 2.2K, R476 change to 10u by FAE's recommend 1/10 page.16 delete R8 page.20 add C323, C333, C470, C471, C474, C672, C673 for Vin plane page.27 change CN21 PWR/B connector P/N & footprint page.18 change R36 to 2.2 ohm 1/11 page.20 add C480, C337, C674 for Vin plane page.34 delete +1V LDO power circuit page.20 add C490, C493, C494, C495, C496 by EMI's request page.18 change C18 to 220P by EMI's request 1/10 page.30 stuff PC123, unstuff PC30 page.23 add R573 for FAE's request
	2A	2/14 Test-Point change footprint. TP3075 change to TP2675 TP3050 change to TP2650 2/14 page.21 Add R574 & R575 page.21 R599 chane to 10K ohm resistor. 2/14 page.30 PC123 unstuff , PC30 stuff. page.27 unstuff SW1 & CN19 page.25 unstuff Bluetooth group. page.26 EMI CP1, CP2, CP3, CP4, CP5, CP6 stuff 100pF cap array page.20 EMI stuff C553 , ADD C361/C483/C507,C497,C498,C499,C500. page.16 EMI stuff C619/C620 2/14 page20 Reserve C508 2/14 page19 LED5 , PIN1 connect to<BATLED0#>& PIN4 connect to<BATLED1#> 2/14 page16 add R16 C671 & C40 change to TOP side. 2/14 FDI :: delete R152/R161/R157/R171/R167 , R454/R470/R481/R487/R464/R480/R500/R495/R459/R475/R478/R491/R461/R484/R498/R493 Change to 0402short :: R149/R234/R233/R531/R524/R114/R163/R194/R271/R554/R107/R109/R386/R390/R90 2/14 Change to 0603short :: R113/R142/R168/R186/R169/R172/R174/R178/R185/R201/R213/R417/R268/R275/R299/R5/R11/R581/R587/R588/R557/L18/L19/L20 2/14 page.18 Add C46/C48/C51/C52 2/15 POWER cahnge to shortpad 2/15 page12 delete R116 & R124. Add C574. C598 & C604 change to TOP Add C339 , C340 page16 stuff C661 2/16 page.30 change +5V_PCU power to +5V_S5 for leakage 2/17 page.21 remove R574, R575 & add D10, D11 2/17 page.27 add Q12 and use GPIO53 for throttling function for 40W adaptor 2/17 page.21 change U10 P/N 2/17 page.16 change R14, R16 to 0805 shortpad page.18 change R15 to 0805 shortpad page.12 change R140, R162, R210,R424 to 0805 shortpad page.19 change R303 to 0805 shortpad page.20 change R443, R550 to 0805 shortpad 2/17 page.25 change R279 to 1206 shortpad 2/17 page.18 unstuff C30
	3C	3/10 page.27 Unstuff Q12 3/14 page25. L33 exchange order for USB signal routing. 3/14 page.18 X12 & R20 unstuff , R15 change to 0805 resistor and unstuff. 3/10 page.19 Add R314 & R574 , 0 ohm or CAP depend on result. 3/10 page.32 delete shortpad , PR229 & PR230
	4A	

MODEL ZQ9

FROM	To
X	1A
X	1A
X	1A

Quanta Computer Inc.
PROJECT : ZQH
Change list2

DOC NO.	PROJECT MODEL :	ZQH	APPROVED BY:		DATE:
	PART NUMBER:		DRAWING BY:		REVISON: