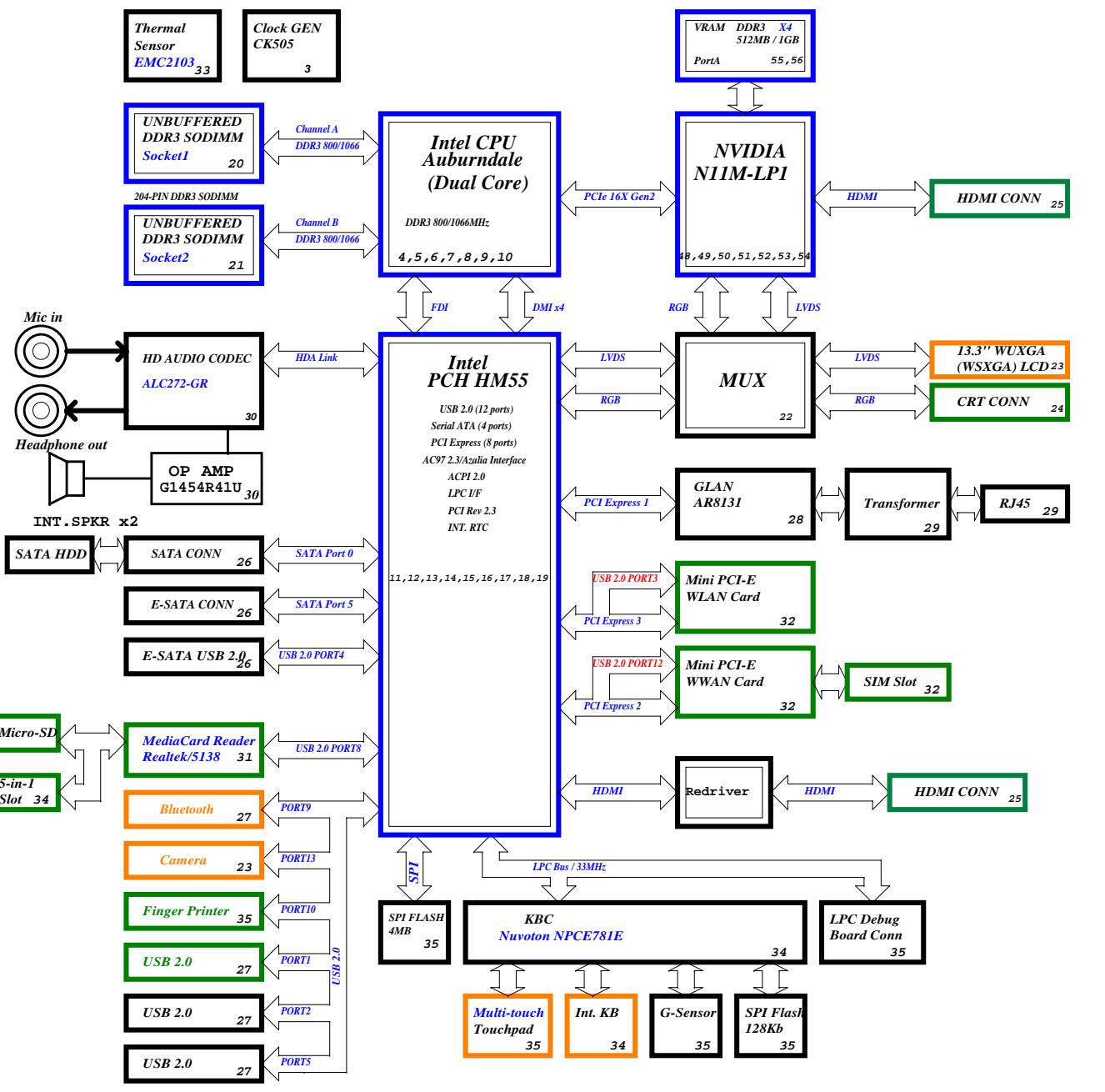


LA36 Switchable Graphics System Schematics

Project Code: 91.4JG01.001
PCB(Raw Card): 09939-1

PCB LAYER	
L1:	Top
L2:	VCC/GND
L3:	Signal
L4:	Signal
L5:	GND
L6:	Boot



- Finger Printer BD
- BT BD
- AV BD

CPU DC/DC	
ISL62882 40, 41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC	
RT8223BGQW 42	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC	
RT8209E 44	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC	
RT8209E 44	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC	
RT8209E 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO	
RT9025 46	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO	
RT9026 46	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC	
ISL62881 47	
INPUTS	OUTPUTS
DCBATOUT	VCC GFXCORE

SYSTEM DC/DC	
RT8208A 45	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

CHARGER	
BQ24745 43	
INPUTS	OUTPUTS
DCBATOUT	BT+

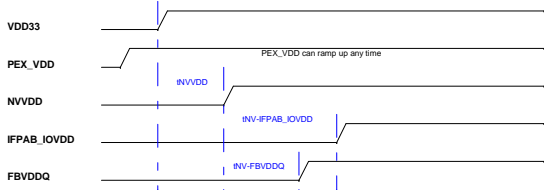
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarkfield samples.	Clarkfield (only for early samples pre-ESI) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

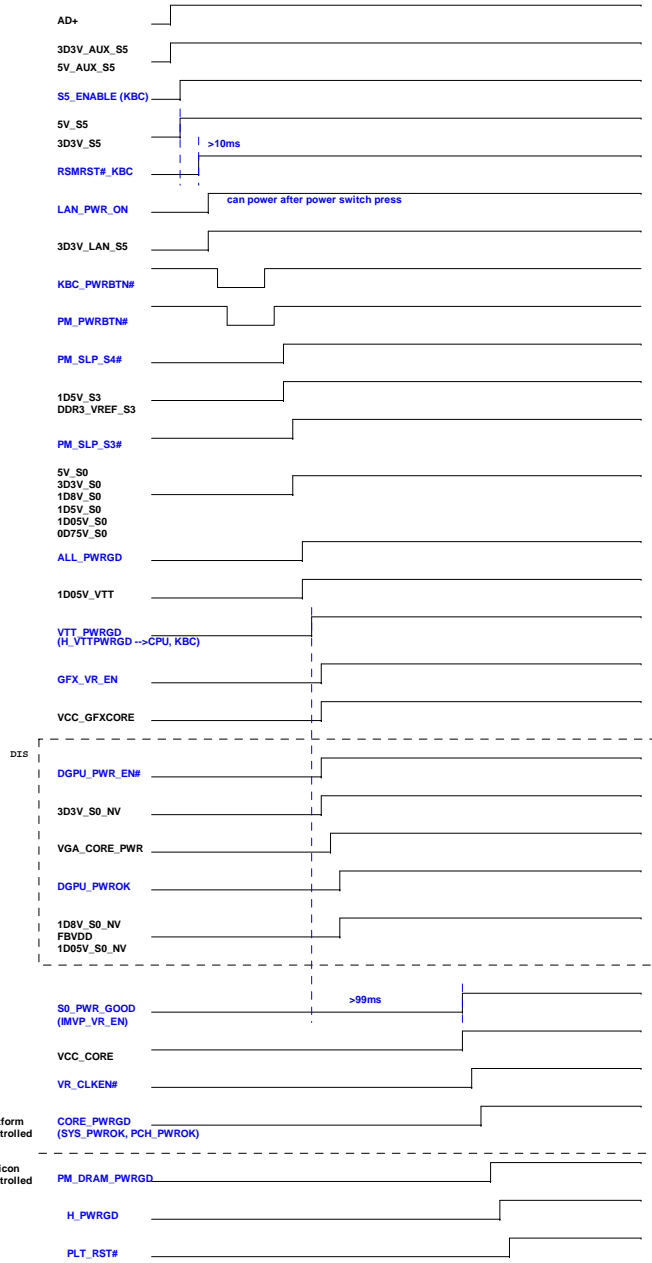
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1): Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

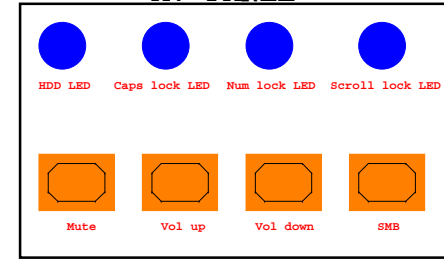
N11M-GE Power Sequence



Sequence AC

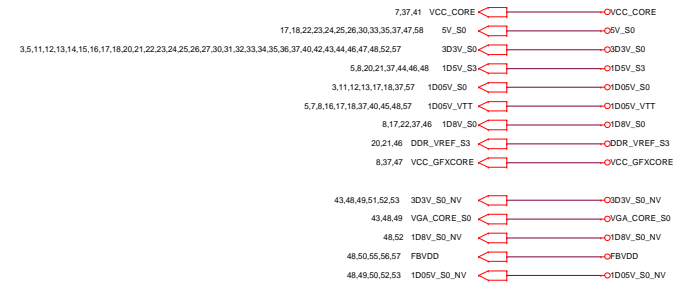


AV PANEL



PLANAR_ID[1..0]

KBC GPin	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0		
	0	0	LA36 - SA	SA
	0	1		SB
	1	0		SC
	1	1		-1



A

A

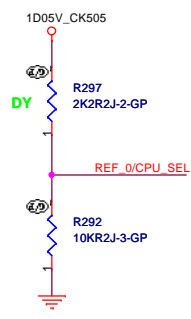
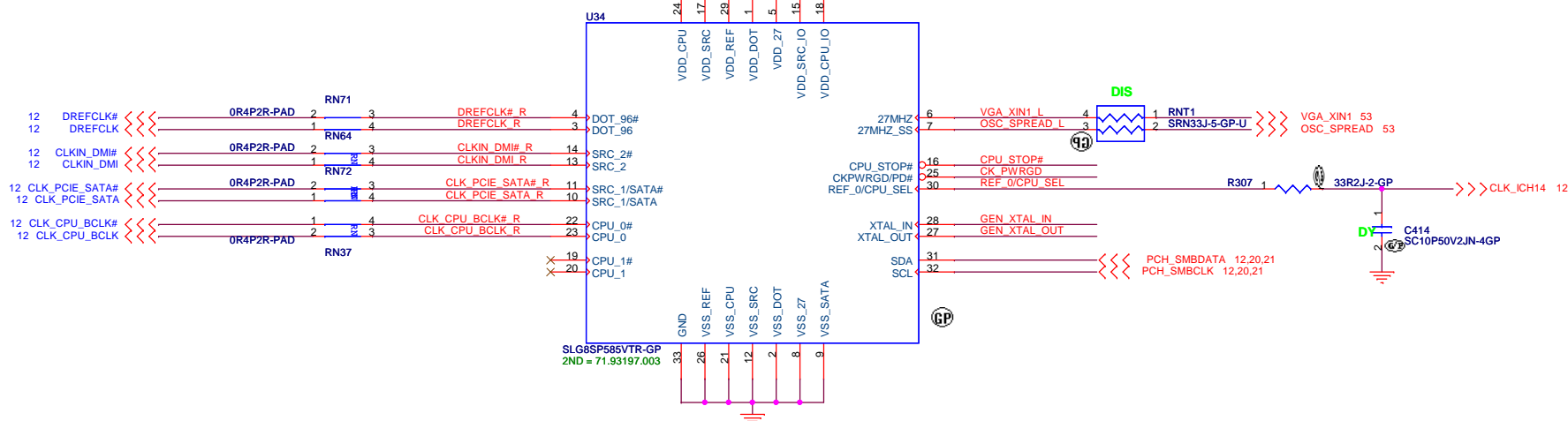
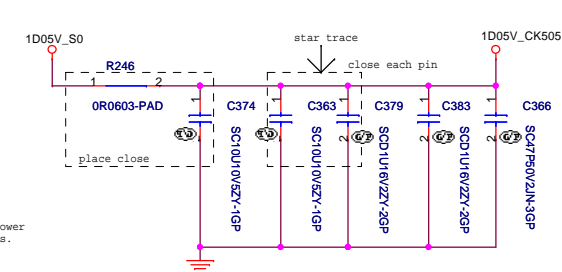
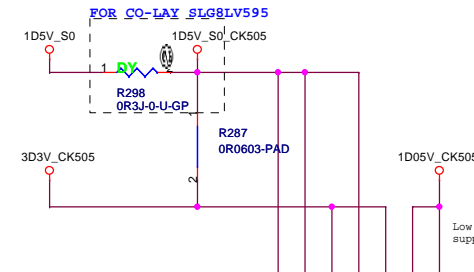
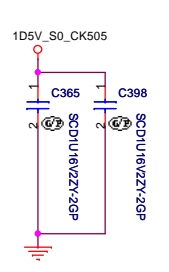
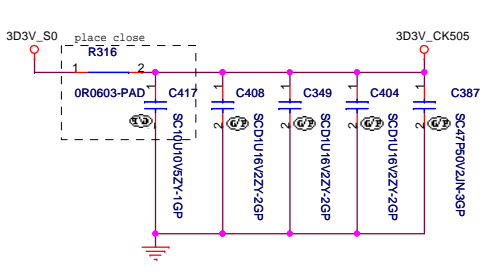
<Variant Name>

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 301, Taiwan, R.O.C.

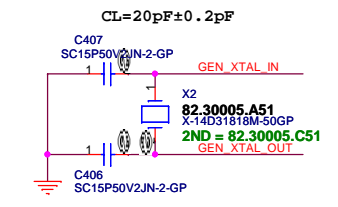
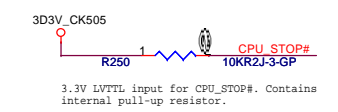
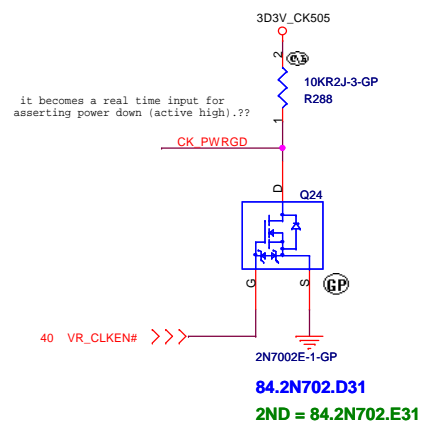
File **Reference**

Size A2 Document Number **LA36 MB DIS** Rev -1

Date: Monday, March 22, 2010 Sheet 2 of 58

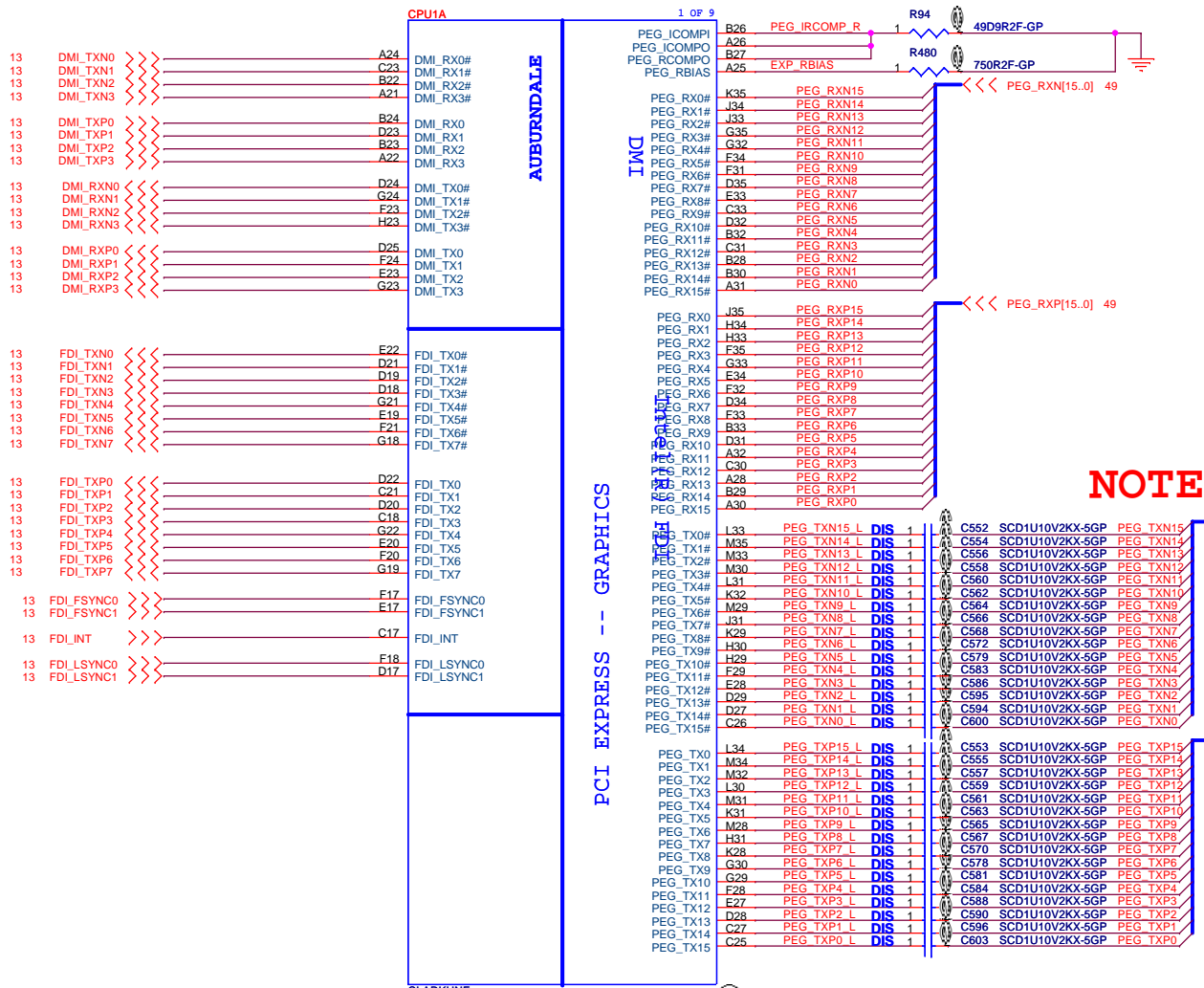


FSC	0	1
SPEED	133MHz (Default)	100MHz

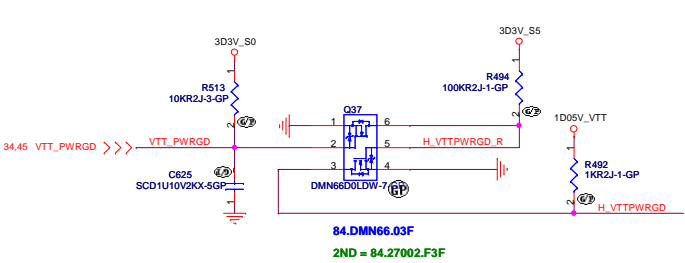
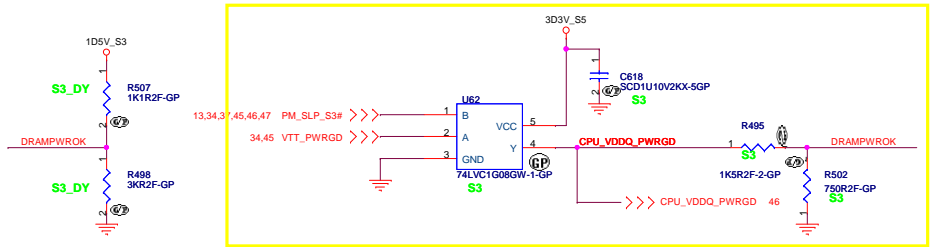
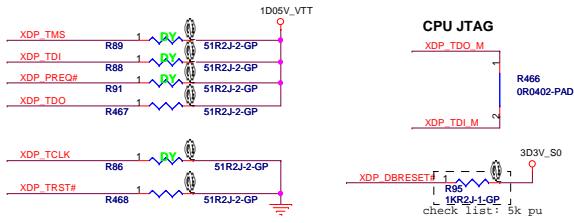
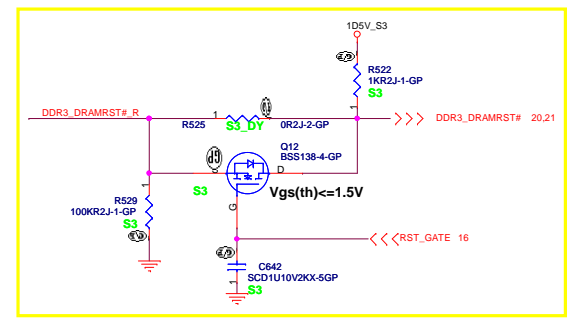
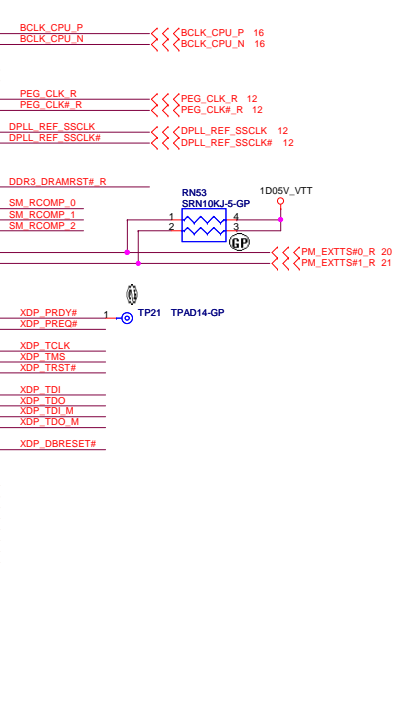
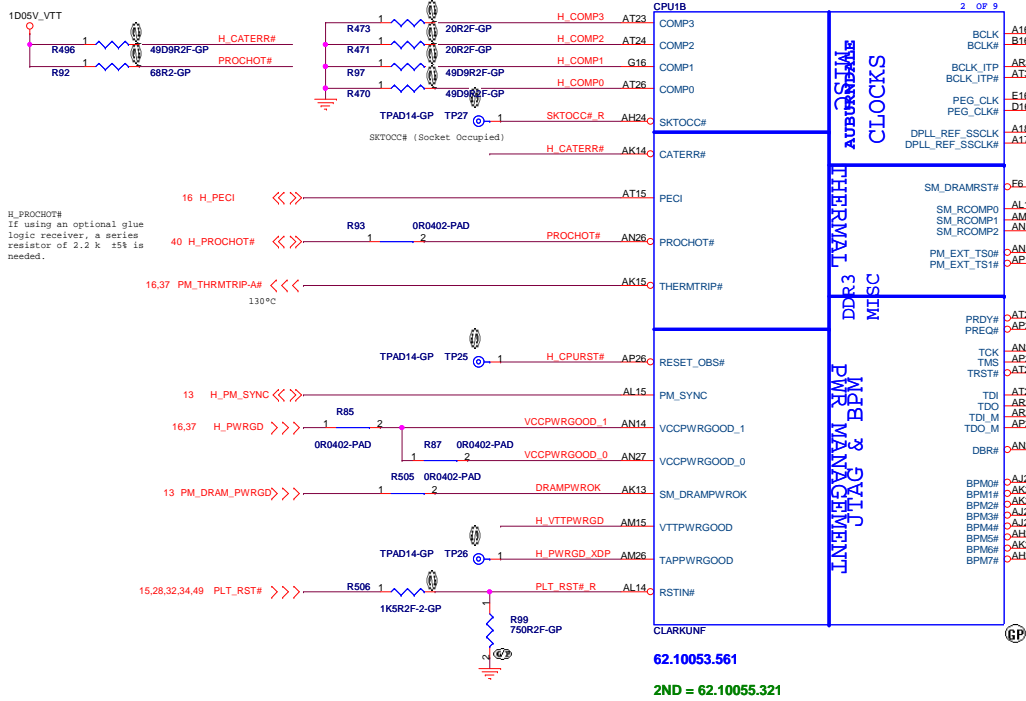


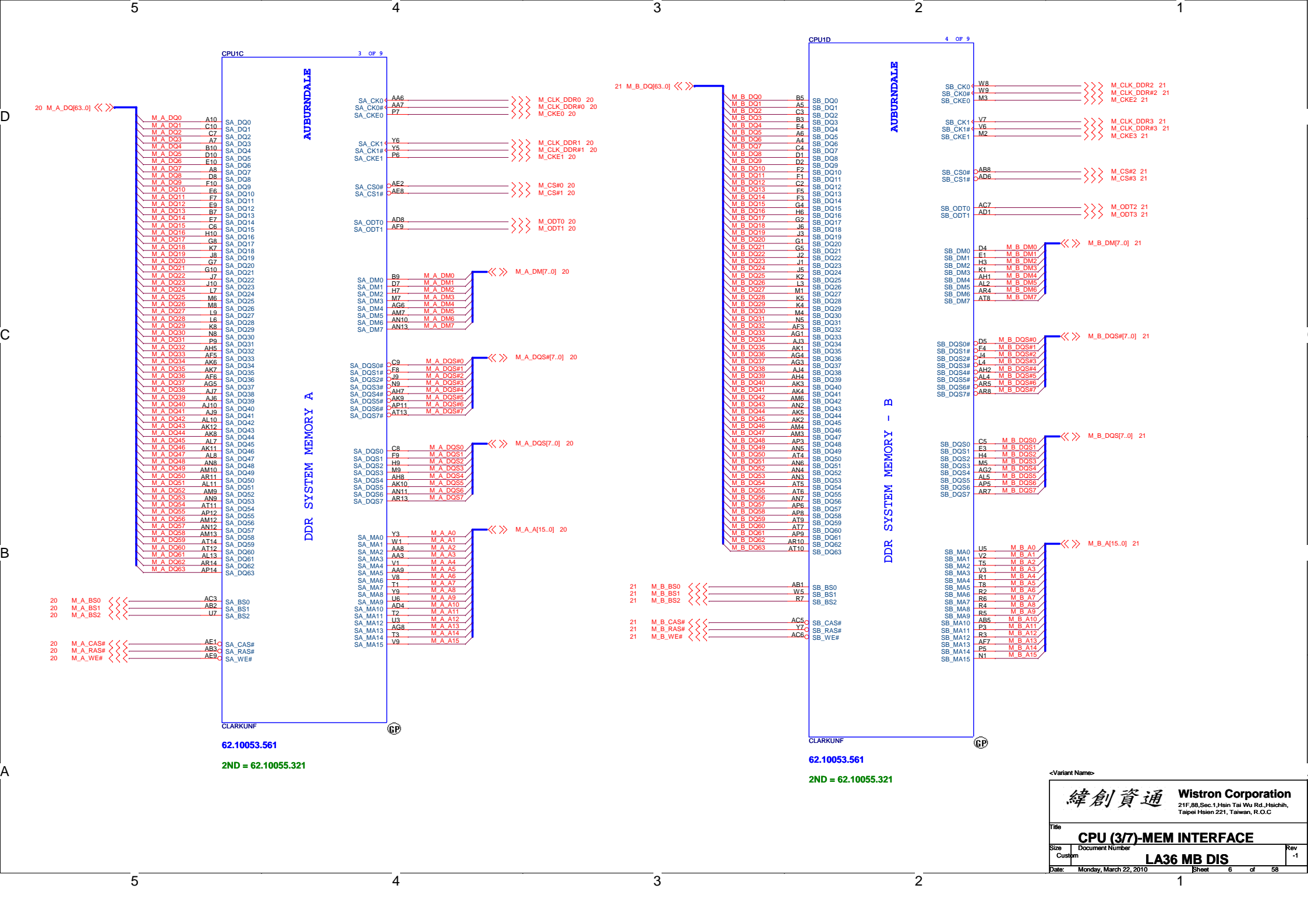
Layout Notes:

Make sure that the stubs to the test points (CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.



NOTE SWAP TX0~15





20 M_A_DQ[63..0] <<>

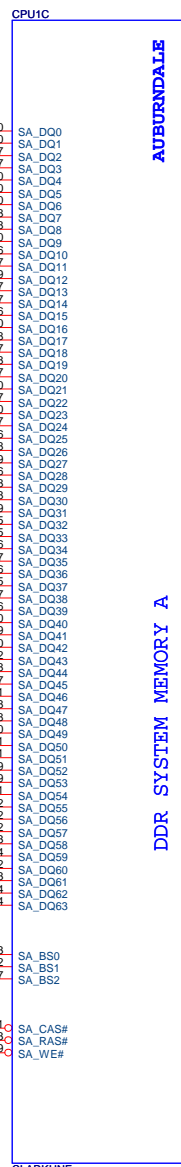
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20 M_A_BS1 <<>
20 M_A_BS2 <<>

20 M_A_CAS# <<>
20 M_A_RAS# <<>
20 M_A_WE# <<>

21 M_B_DQ[63..0] <<>

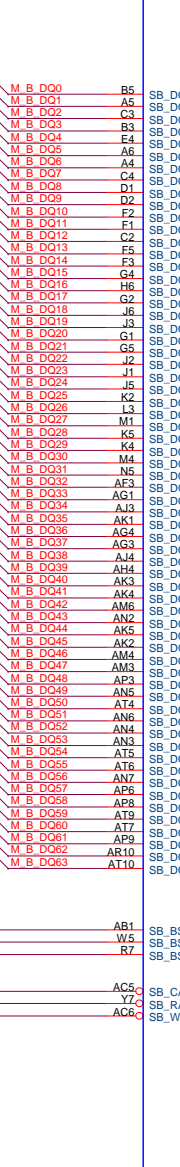
21 M_B_BS0 <<>
21 M_B_BS1 <<>
21 M_B_BS2 <<>

21 M_B_CAS# <<>
21 M_B_RAS# <<>
21 M_B_WE# <<>



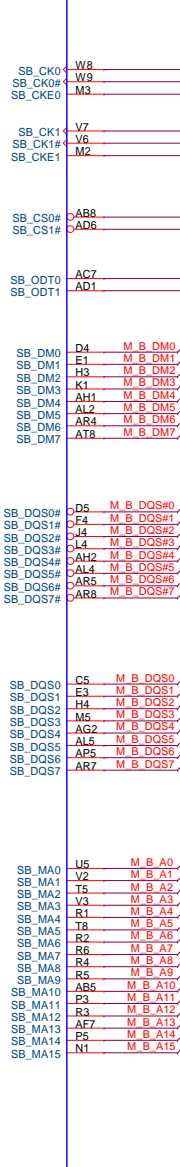
62.10053.561

2ND = 62.10055.321



62.10053.561

2ND = 62.10055.321

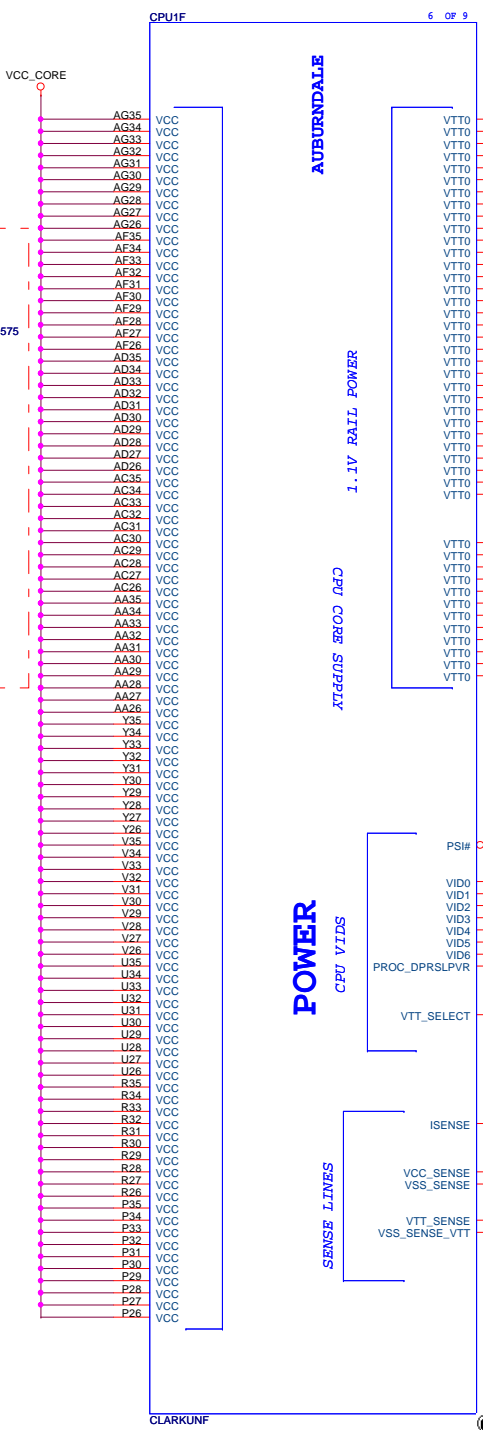
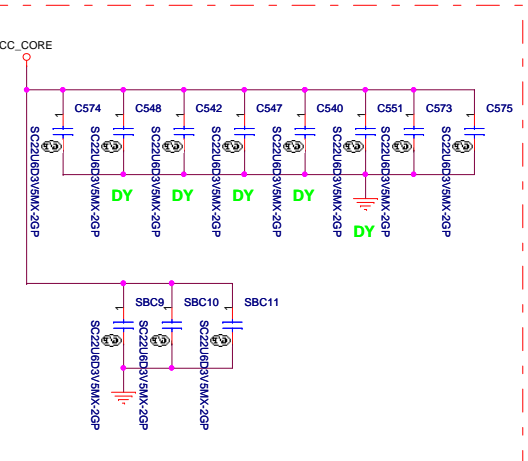


<Variant Name>



Title		CPU (37)-MEM INTERFACE	
Size	Document Number	Rev	
Custom	LA36 MB DIS	-1	
Date:	Monday, March 22, 2010	Sheet	6 of 58

PROCESSOR CORE POWER
48A -->Arrandale



AUBURNDALE

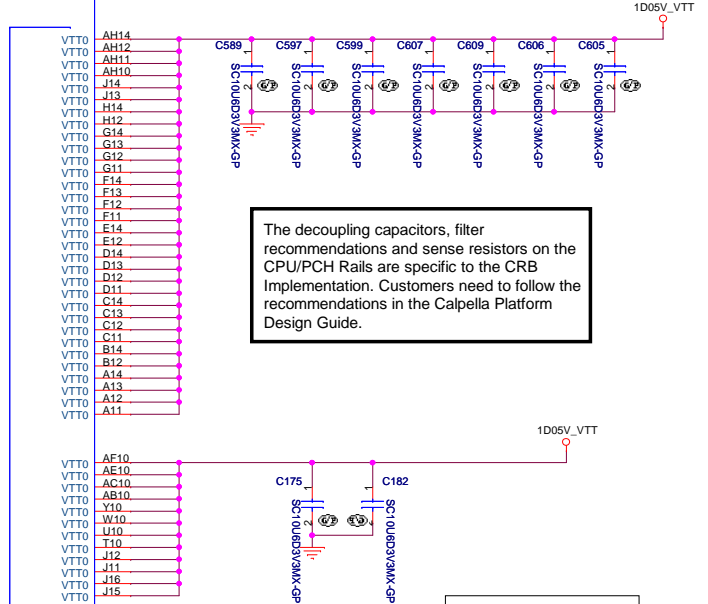
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

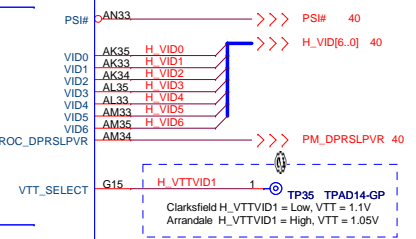
CPU VIDS

SENSE LINES

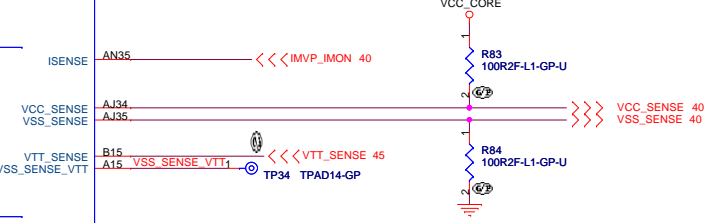


The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



H_VTTVID1 TP35 TPAD14-GP
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V



<Variant Name>

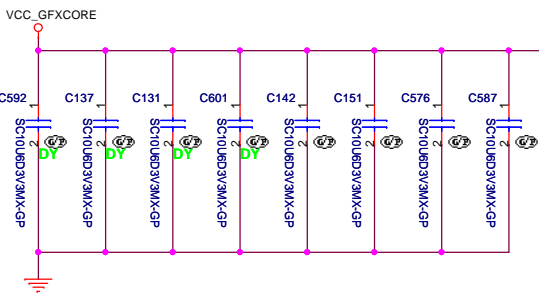
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title **CPU (47)-POWER**

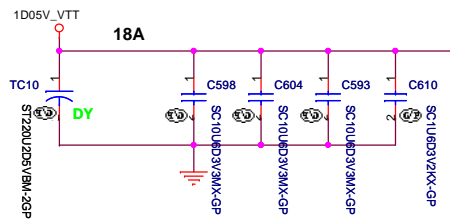
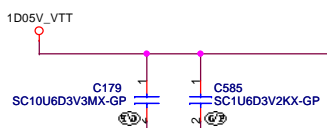
Size Custom Document Number **LA36 MB DIS** Rev -1

Date: Monday, March 22, 2010 Sheet 7 of 58

62.10053.561
2ND = 62.10055.321

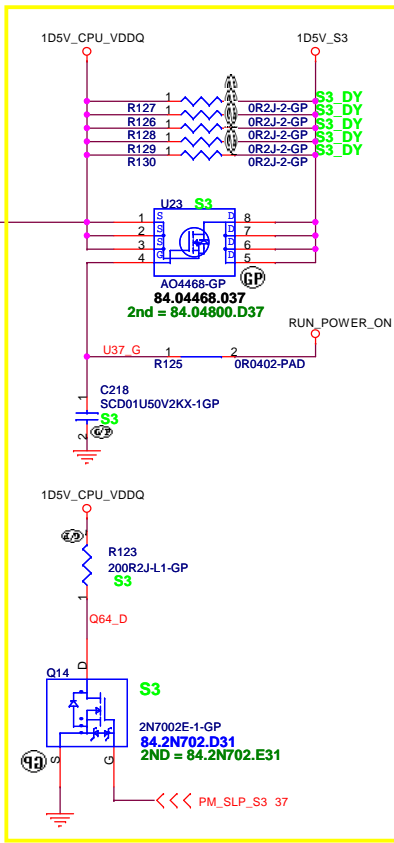
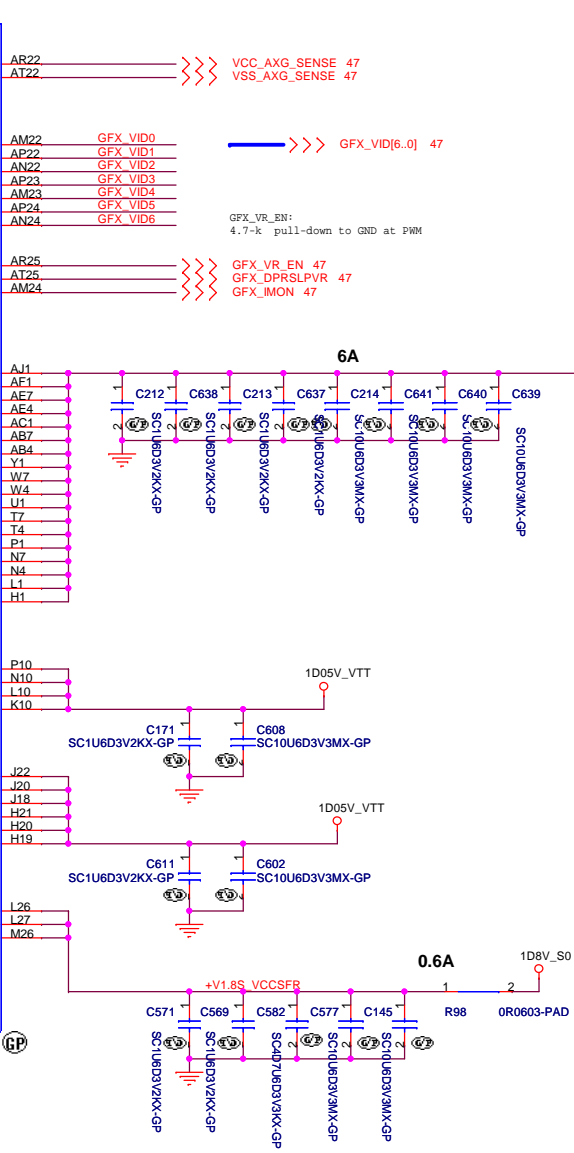


Please note that the VTT Rail Values are Aurburdale
VTT=1.05V; Clarksfield
VTT=1.1V



- CPU1G
- AT21 VAXG1
 - AT19 VAXG2
 - AT18 VAXG3
 - AR21 VAXG4
 - AR19 VAXG6
 - AR18 VAXG7
 - AP21 VAXG9
 - AP19 VAXG10
 - AP18 VAXG11
 - AN21 VAXG12
 - AN19 VAXG13
 - AN18 VAXG14
 - AM21 VAXG15
 - AM19 VAXG16
 - AM18 VAXG17
 - AM16 VAXG18
 - AM16 VAXG19
 - AL21 VAXG20
 - AL19 VAXG21
 - AL18 VAXG22
 - AL16 VAXG24
 - AK21 VAXG25
 - AK19 VAXG26
 - AK18 VAXG27
 - AJ21 VAXG28
 - AJ19 VAXG29
 - AJ18 VAXG30
 - Y16 VAXG31
 - AH21 VAXG32
 - AH19 VAXG33
 - AH18 VAXG34
 - AH16 VAXG35
 - VAXG36

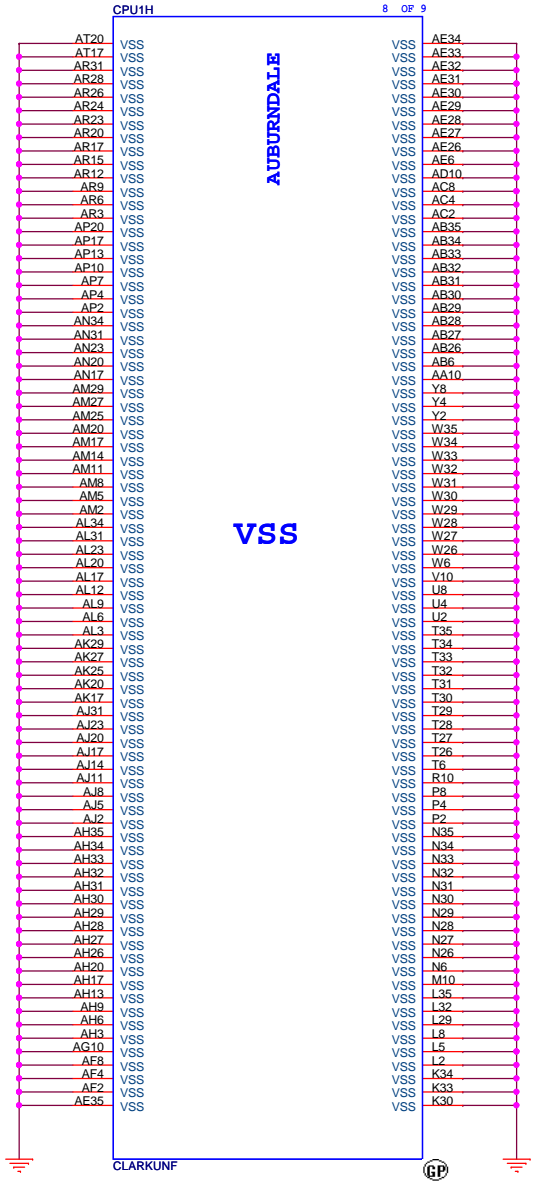
- AURBURDALE
- SENSE LINES
- GRAPHICS VIDS
- POWER
- DDR3 - 1.5V RAILS
- 1.1V
- 1.8V
- PEG & DMI
- CLARKUNF



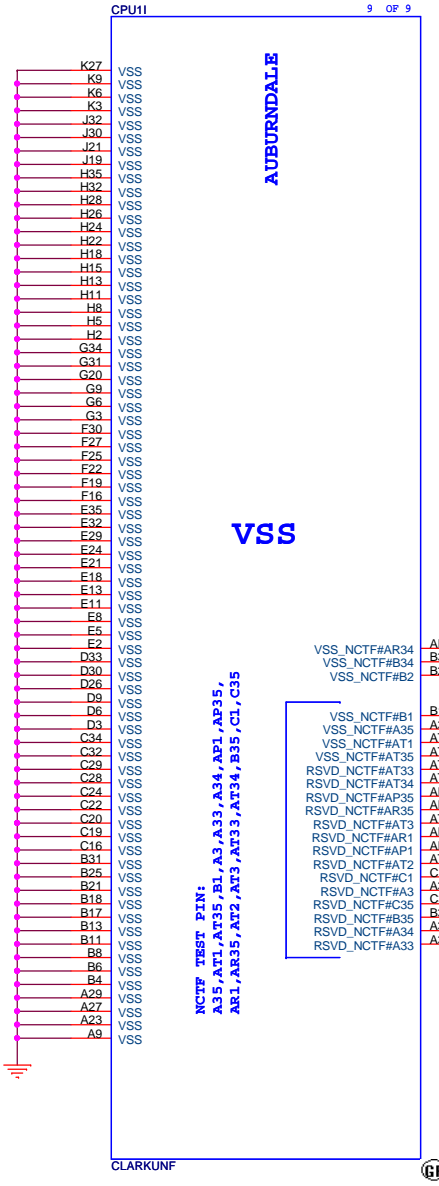
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File		
CPU (57)-Graphic PWR		
Size	Document Number	Rev
A3	LA36 MB DIS	-1
Date:	Monday, March 22, 2010	Sheet 8 of 58

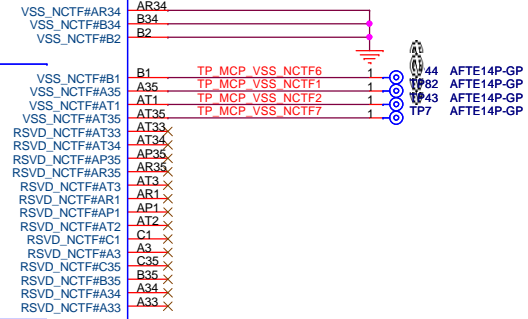


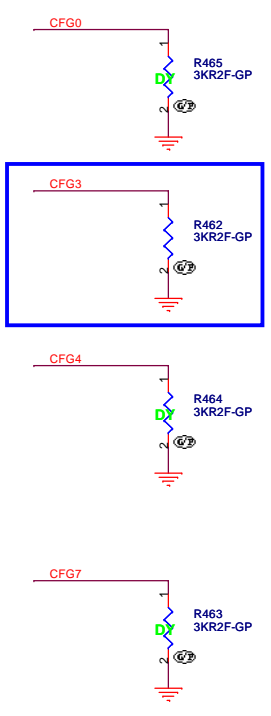
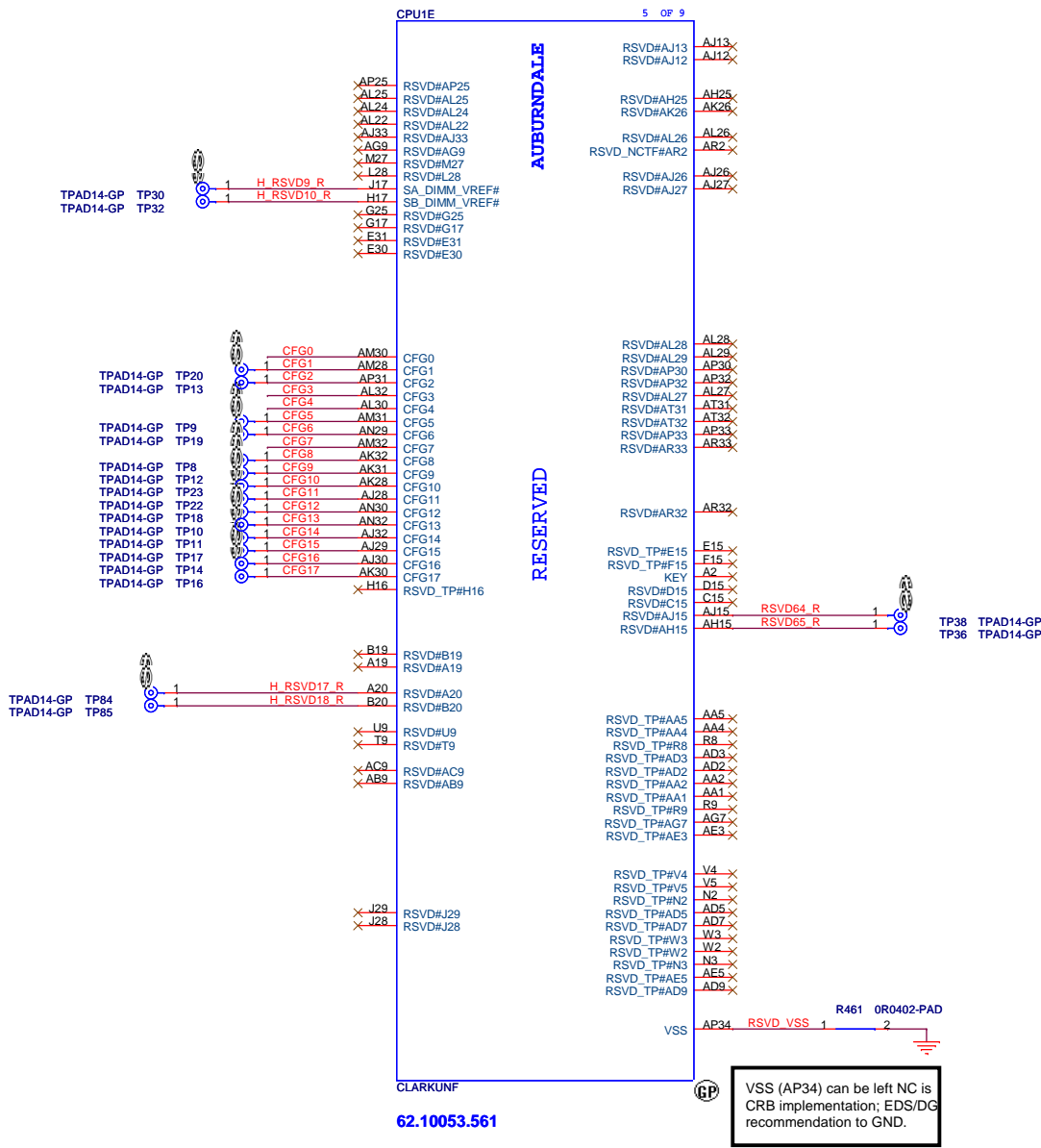
62.10053.561



62.10053.561

NCTF TEST PIN:
 A35,AT1,AT35,B1,A3,A33,A34,AP1,AP35,
 AR1,AR35,AT2,AT3,AT33,AT34,B35,CI,C35





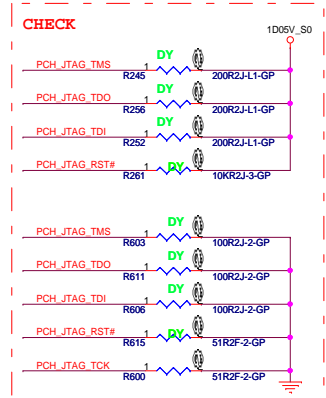
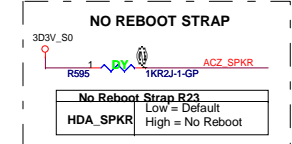
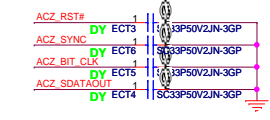
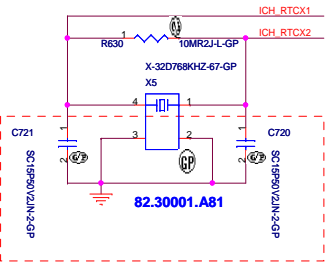
PCI-Express Configuration Select	
CFG0	1: Single PEG 0: Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

CLARKUNF
62.10053.561

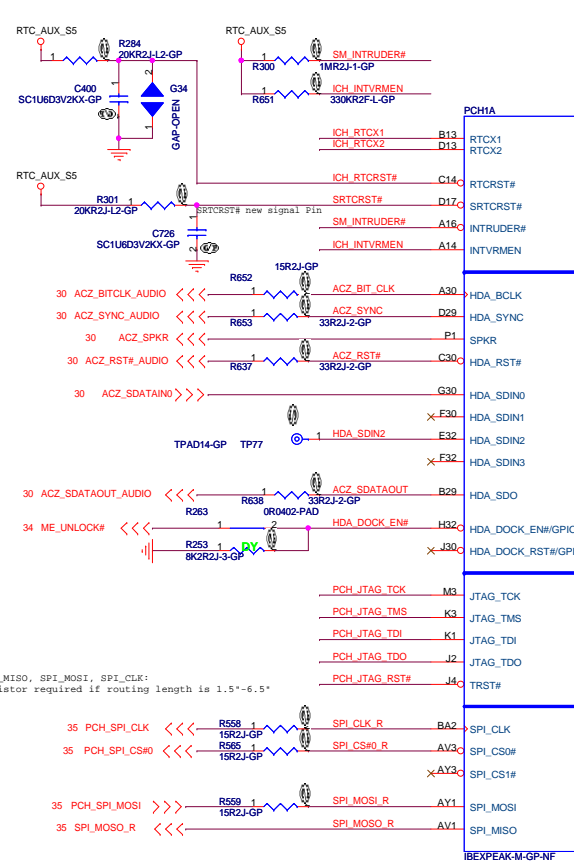


Place the resistors on RST, TCK, TMS, and TDI near PCH.

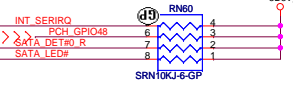
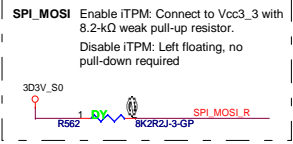
Place the resistors on TDO near XDP.

PCH Pin	PCH JTAG Enable		PCH JTAG Disable		Production	
	ES1	ES2	ES1	ES2	Enable	Disable
TDO	R-1	DY	200 Ohms	DY	DY	DY
	R-2	DY	100 Ohms	DY	DY	DY
	R-10	DY	DY	DY	51 Ohms	DY
TMS	R-3	200 Ohms	200 Ohms	DY	DY	DY
	R-4	100 Ohms	100 Ohms	DY	DY	DY
	R-11	DY	DY	DY	51 Ohms	DY
TDI	R-5	200 Ohms	200 Ohms	20K Ohms	DY	DY
	R-6	100 Ohms	100 Ohms	10K Ohms	DY	DY
	R-12	DY	DY	DY	51 Ohms	DY
TCK	R-7	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms
	R-8	20K Ohms	20K Ohms	DY	DY	DY
TRST#	R-9	10K Ohms	10K Ohms	DY	DY	DY
	R-13	DY	DY	DY	51 Ohms	DY

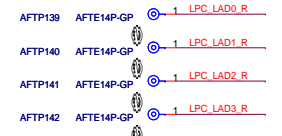
SPI_CS#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"



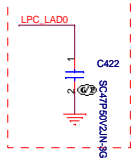
71.0HM55.A0U



Integrated VccSus1_05, VccSus1_5, VccCL1_5		
INTVTRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



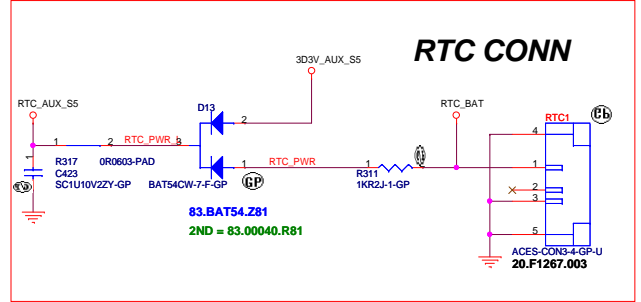
-1 version



HDD

E-SATA

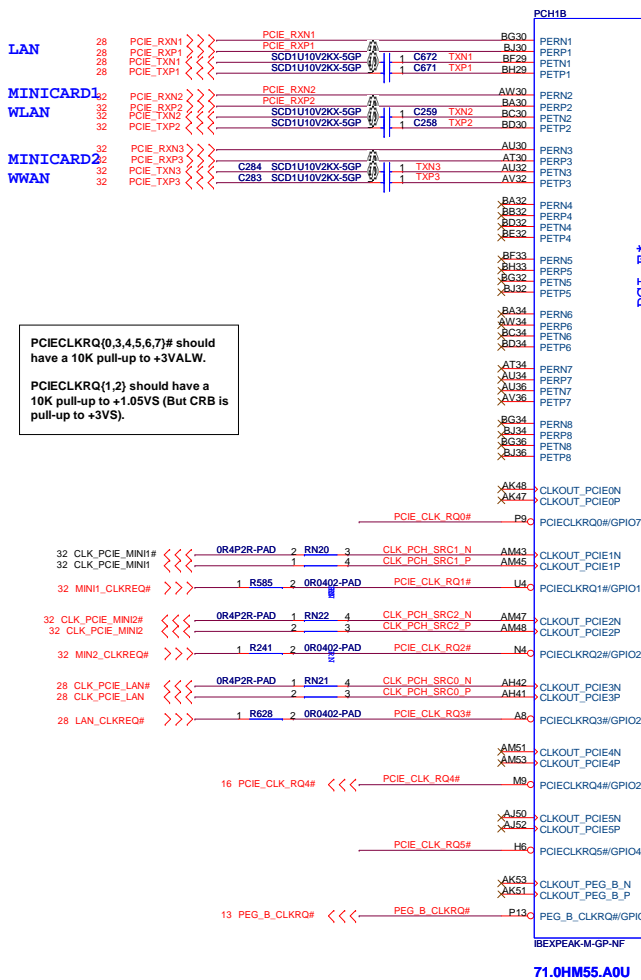
71.0HM55.A0U



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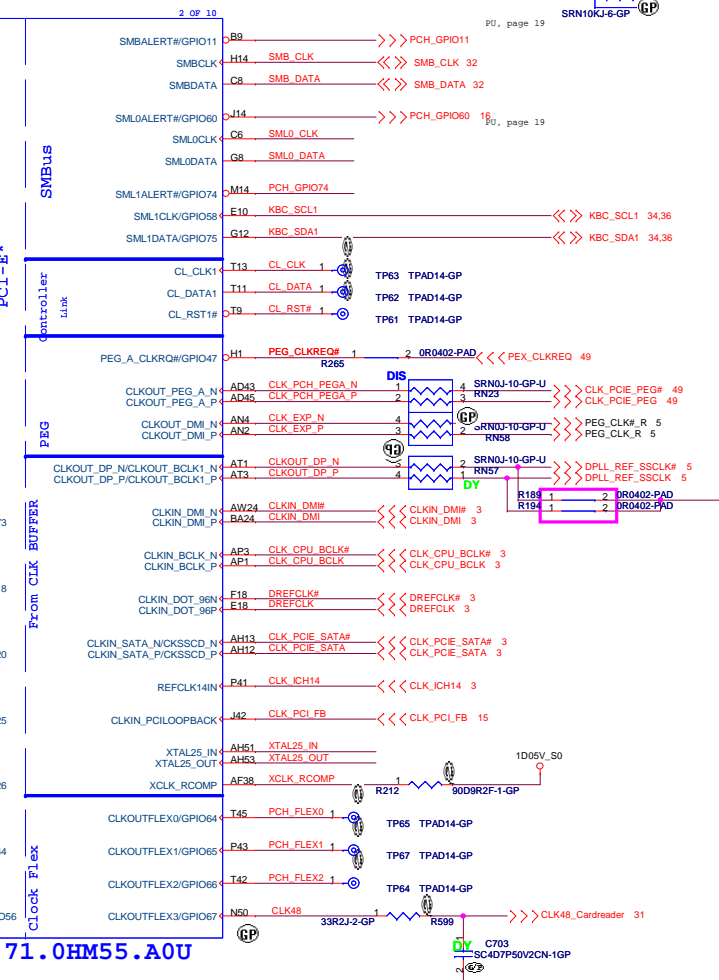
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Size: Custom
Customer: LA36 MB DIS
Date: Monday, March 22, 2010

Sheet 11 of 58

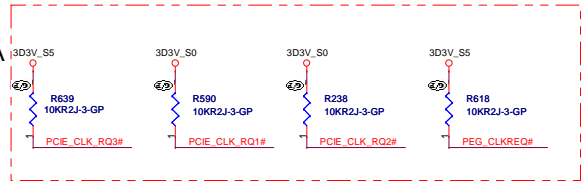
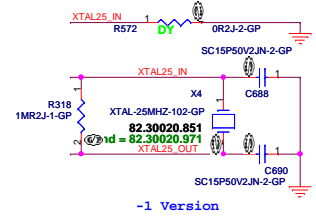
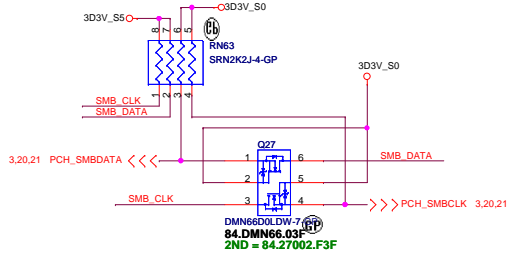
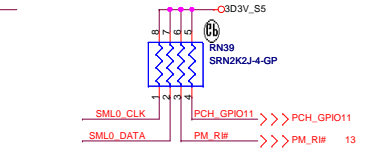
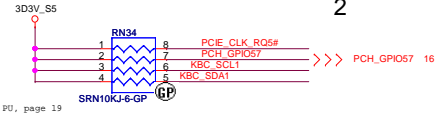


PCIECLKRQ(0,3,4,5,6,7)# should have a 10K pull-up to +3VALW.

PCIECLKRQ(1,2) should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).



71.0HM55.AOU



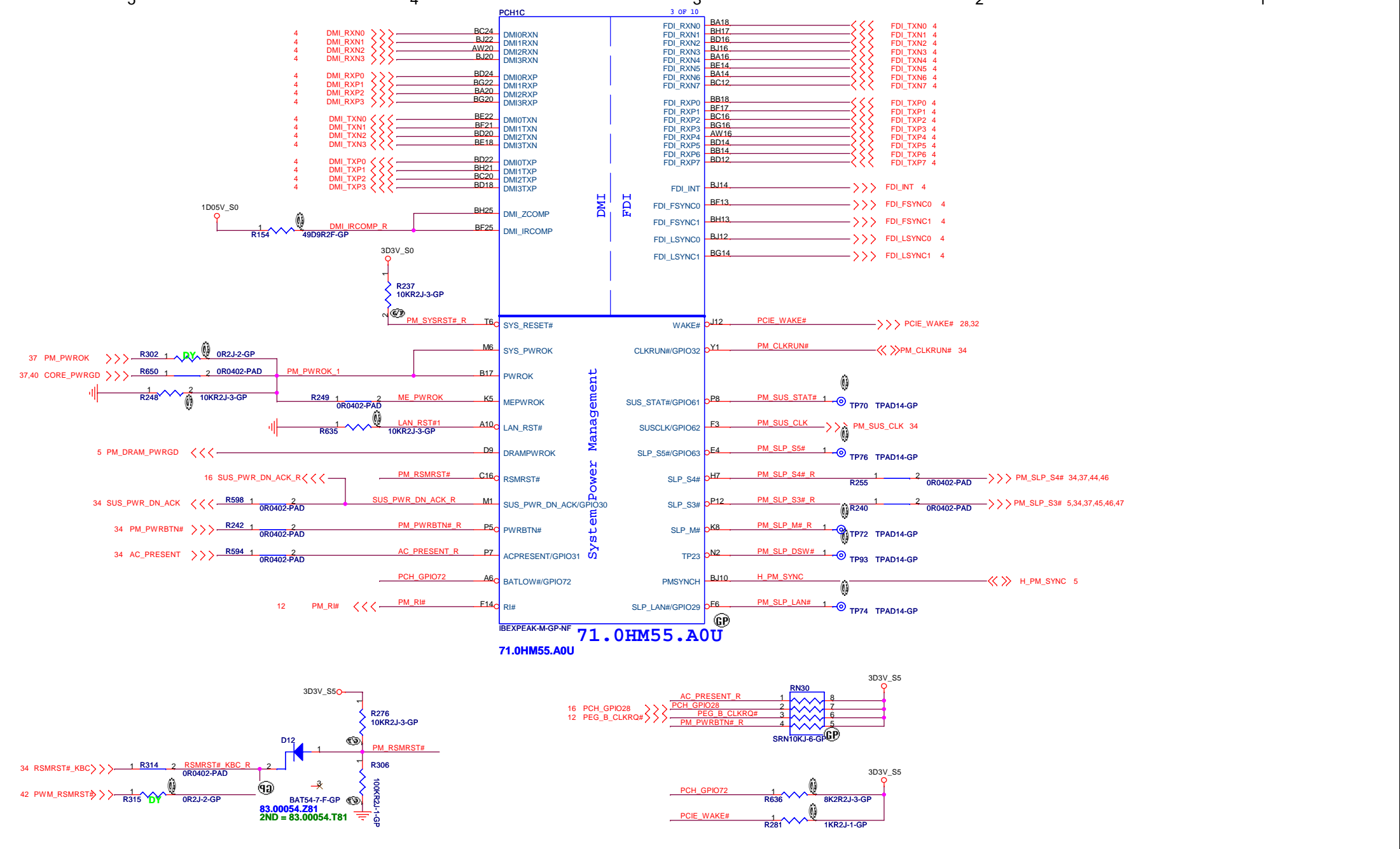
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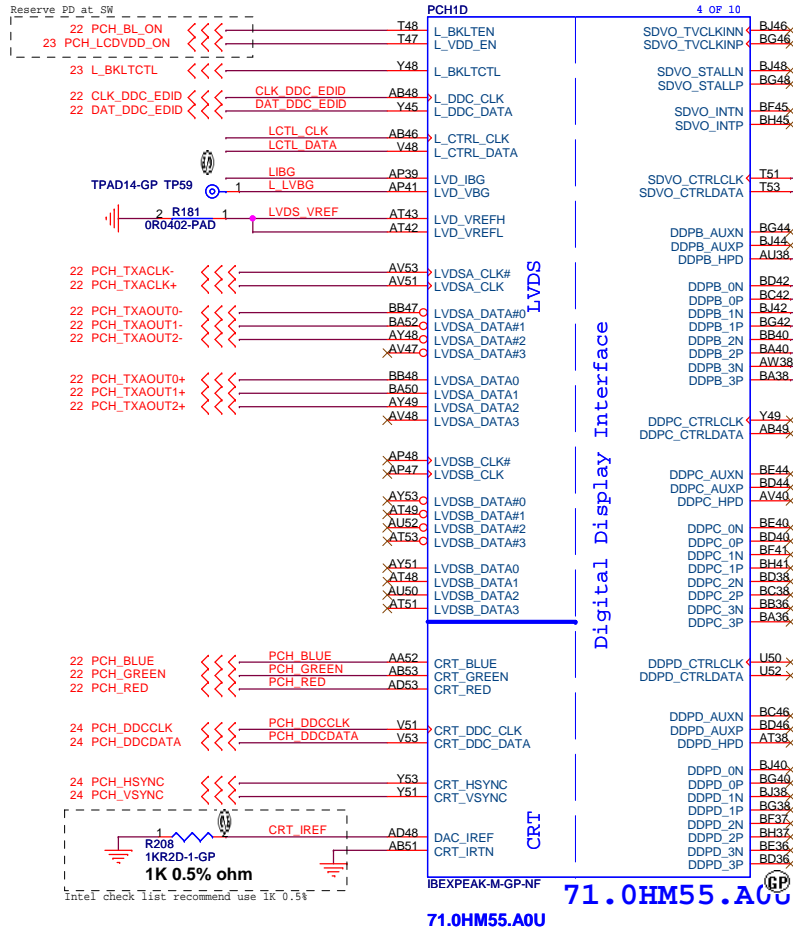
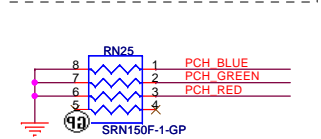
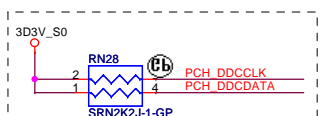
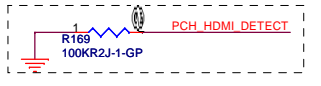
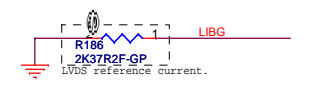
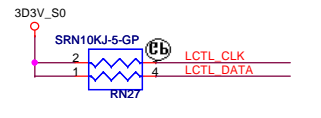
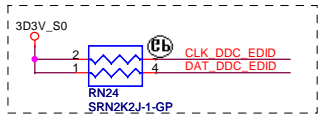
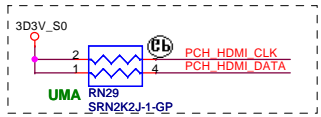
緯創資通 Wistron Corporation
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File: **PCH (2/9)-PCIE / SMBUS / CLK**

Size: **LA36 MB DIS**

Date: **Monday, March 22, 2010** Sheet **12** of **58**





Digital Display Interface

71.0HM55.A0U

Intel® check list recommend use 1K 0.5%

IBEXPEAK-M-GP-NF

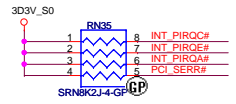
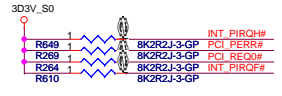
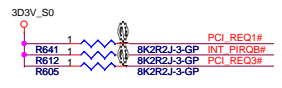
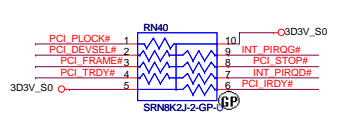
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File: **PCH (4/9)-LVDS / CRT**

Size: A3 Document Number: **LA36 MB DIS** Rev: -1

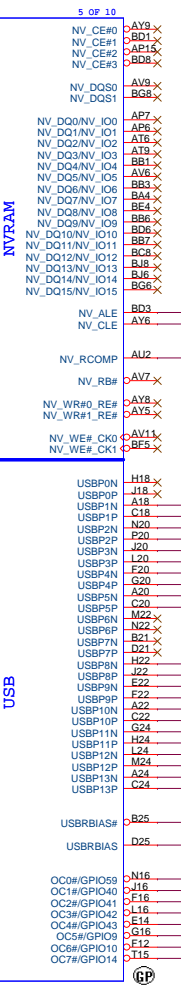
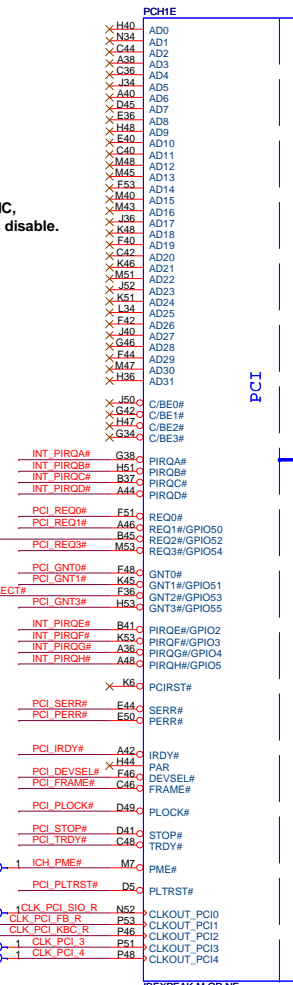
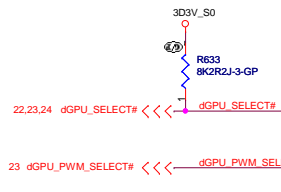
Date: Monday, March 22, 2010 Sheet 14 of 58



PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
0	1	PCI
1	1	SPI(Default)

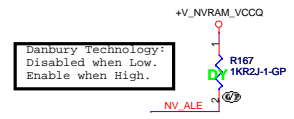
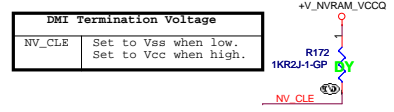
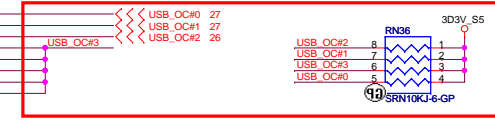
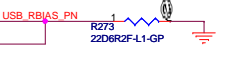
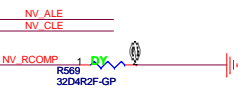
These pins are left as NC, because the function is disable.

CHECK

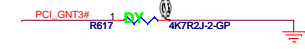
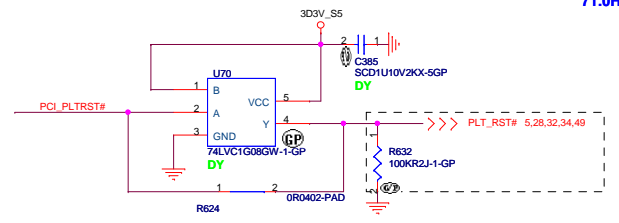


These pins are left as NC, because the function is disable.

CHECK



Pair	Device
0	NC
1	USB3
2	USB1
3	WLAN
4	E-SATA
5	USB2
6	Disable (HM55)
7	Disable (HM55)
8	Card Reader
9	Blue Tooth
10	Finger Print
11	Micro SD
12	WWAN
13	Camera



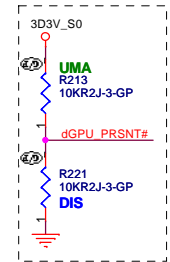
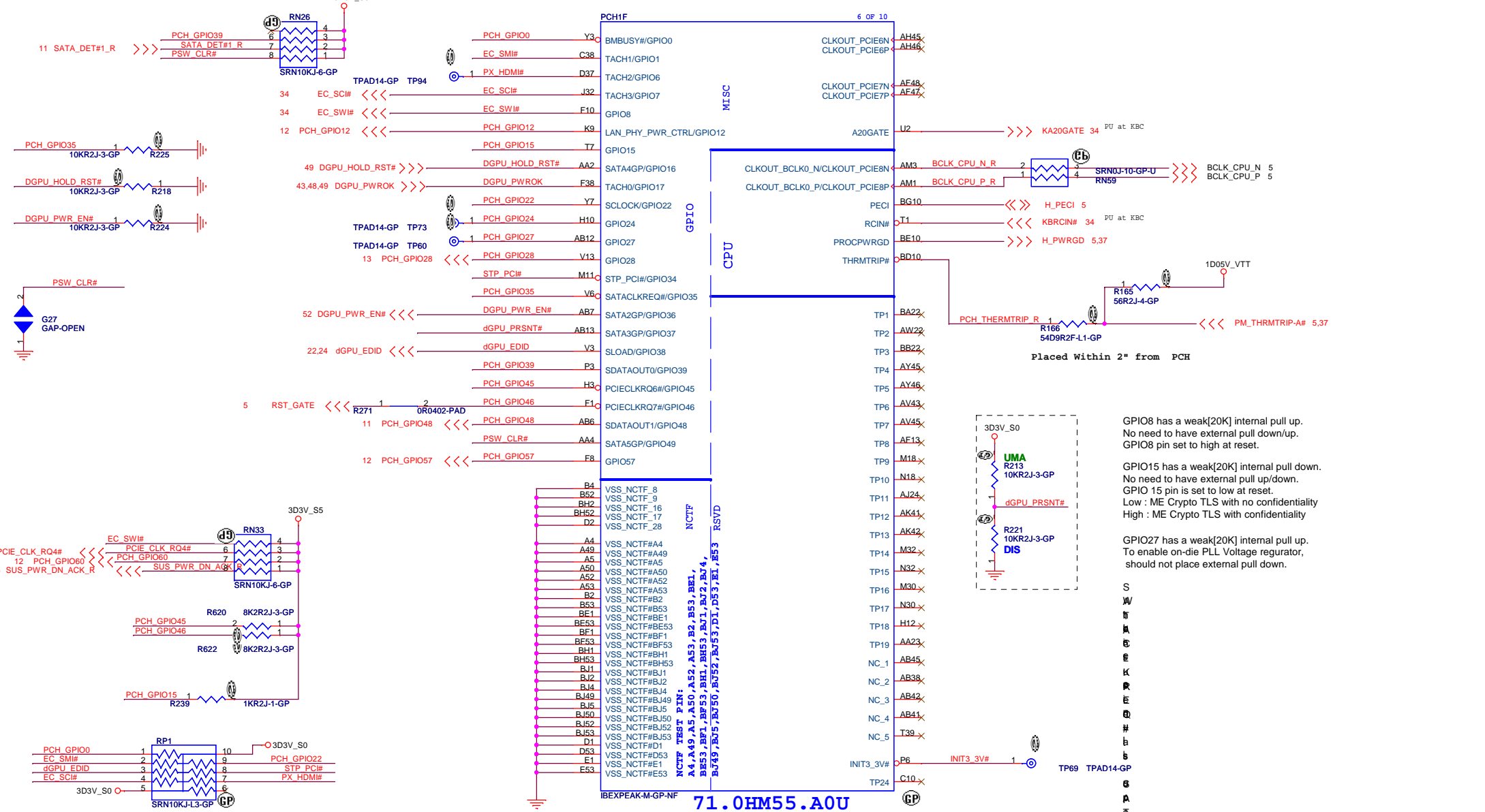
PCI_GNT#3
Low = A16 swap override/Top-Block Swap Override enabled
High = Default

OC#0	Port 0 & 1	EHCI 1
OC#1	Port 2 & 3	
OC#2	Port 4 & 5	
OC#3	Port 6 & 7	EHCI 2
OC#4	Port 8 & 9	
OC#5	Port 10 & 11	
OC#6	Port 12 & 13	
OC#7	Floater OC# (not used)	

<Variant Name>

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Title		
PCH (5/9)-PCI / USB		
Size	Document Number	Rev
Custom	LA36 MB DIS	-1
Date	Monday, March 22, 2010	Sheet 15 of 58



GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

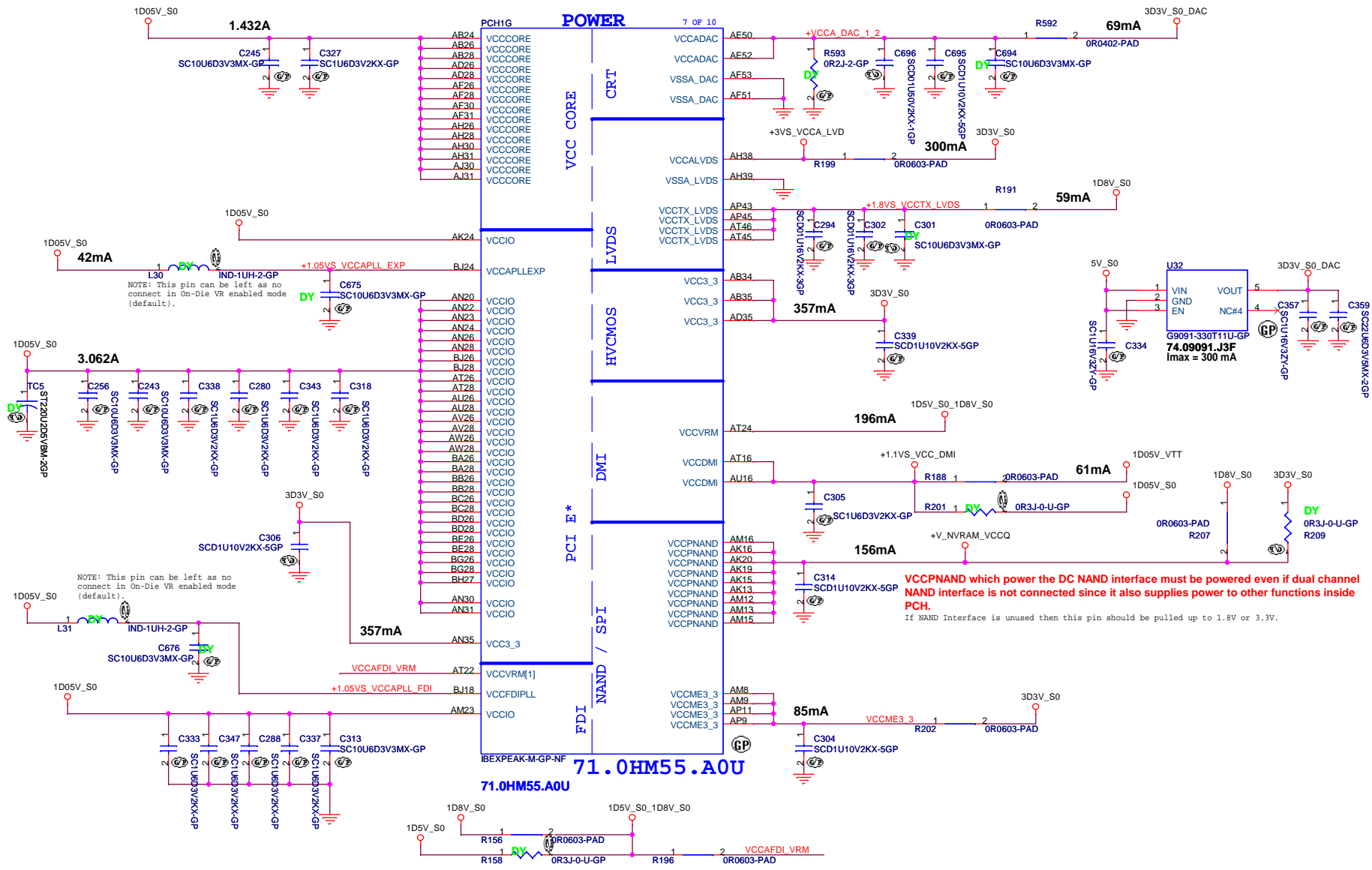
GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

S
W
T
B
E
E
K
R
E
Q

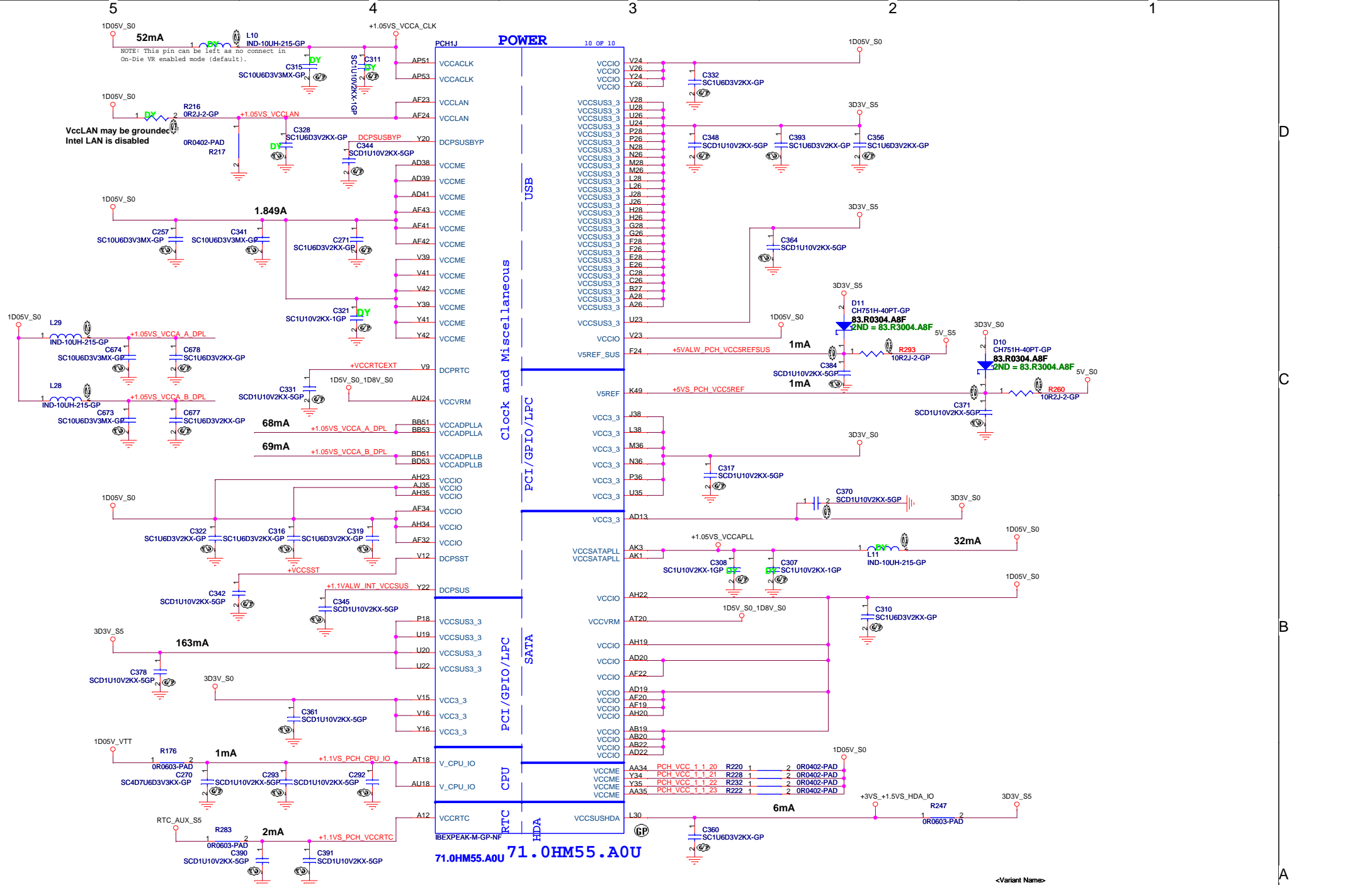
b
b
b
b
S
S
A
E
E
K
R
E
Q

p
a
n
d



<Variant Name>

緯創資通		Wistron Corporation	
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Title			
PCH (7/9)-PWR 1			
Size	Document Number		Rev
A3	LA36 MB DIS		-1
Date:	Monday, March 22, 2010	Sheet	17 of 58



PCH1 9 OF 10

AY7	VSS	H49
B11	VSS	H5
B15	VSS	J24
B19	VSS	K11
B23	VSS	K43
B31	VSS	K47
B35	VSS	K7
B39	VSS	L14
B43	VSS	L18
B47	VSS	L2
B7	VSS	L22
BG12	VSS	L32
BB12	VSS	L36
BB16	VSS	L40
BB20	VSS	L52
BB24	VSS	M12
BB30	VSS	M16
BB34	VSS	M20
BB38	VSS	N38
BB42	VSS	M34
BB49	VSS	M38
BB5	VSS	M42
BC10	VSS	M46
BC14	VSS	M49
BC18	VSS	M5
BC2	VSS	M5
BC22	VSS	M8
BC32	VSS	N24
BC36	VSS	P11
BC40	VSS	AD15
BC44	VSS	P22
BC52	VSS	P30
BH9	VSS	P32
BD48	VSS	P34
BD49	VSS	P42
BD5	VSS	P45
BE12	VSS	P47
BE16	VSS	R2
BE20	VSS	R52
BE24	VSS	T12
BE30	VSS	T41
BE34	VSS	T46
BE38	VSS	T49
BE42	VSS	T5
BE46	VSS	T5
BE48	VSS	U30
BE50	VSS	U31
BE6	VSS	U32
BE8	VSS	U34
BF3	VSS	P38
BF49	VSS	V11
BG18	VSS	P16
BG24	VSS	V19
BG4	VSS	V20
BH11	VSS	V22
BH15	VSS	V30
BH19	VSS	V31
BH23	VSS	V32
BH31	VSS	V34
BH35	VSS	V35
BH43	VSS	V38
BH47	VSS	V43
BH7	VSS	V45
C12	VSS	V46
C50	VSS	V47
D51	VSS	V49
E12	VSS	V5
E16	VSS	V7
E20	VSS	V8
E24	VSS	W2
E30	VSS	W52
E34	VSS	Y11
E38	VSS	Y12
E42	VSS	Y15
E46	VSS	Y19
E48	VSS	Y23
E6	VSS	Y28
E8	VSS	Y30
F8	VSS	Y31
F9	VSS	Y32
F5	VSS	Y38
F5	VSS	Y43
F9	VSS	Y46
G10	VSS	P49
G14	VSS	P49
G18	VSS	Y5
G2	VSS	Y6
G22	VSS	Y8
G32	VSS	P24
G38	VSS	T43
G40	VSS	AD51
G44	VSS	A19
GS2	VSS	AD47
AF39	VSS	Y47
H16	VSS	AT12
H20	VSS	AM6
H30	VSS	AT13
H34	VSS	AM5
H38	VSS	AK45
H42	VSS	AK33
	VSS	AV14

PCHH 8 OF 10

AA19	VSS	AK30
AA20	VSS	AK31
AA22	VSS	AK32
AA19	VSS	AK34
AA24	VSS	AK35
AA26	VSS	AK38
AA28	VSS	AK43
AA30	VSS	AK46
AA31	VSS	AK49
AA32	VSS	AK5
AB11	VSS	AK8
AB15	VSS	AL2
AB23	VSS	AM28
AB30	VSS	AM11
AB31	VSS	BB44
AB32	VSS	AD25
AB39	VSS	BC44
AB43	VSS	AM22
AB47	VSS	AM24
AB5	VSS	AM26
AB8	VSS	AM28
AC2	VSS	BA42
AC52	VSS	AM30
AD11	VSS	AM31
AD12	VSS	AM32
AD16	VSS	AM34
AD23	VSS	AM35
AD30	VSS	AM38
AD31	VSS	AM39
AD32	VSS	AM42
AD34	VSS	AU20
AU22	VSS	AM46
AD42	VSS	AV22
AD46	VSS	AM49
AD49	VSS	AM7
AD7	VSS	AA50
AE2	VSS	BF10
AE4	VSS	BF51
AF12	VSS	AN50
Y13	VSS	AN52
AH49	VSS	AP12
AL4	VSS	AP42
AF35	VSS	AP46
AP13	VSS	AP49
AN34	VSS	AP5
AF45	VSS	BH23
AF46	VSS	BH31
AF49	VSS	AR2
AF5	VSS	AR52
AF8	VSS	AT11
AG2	VSS	BA12
AG52	VSS	AH48
AH11	VSS	AT32
AH15	VSS	AT36
AH16	VSS	AT41
AH24	VSS	AT47
AH32	VSS	AT7
AV18	VSS	AV12
AH43	VSS	AV16
AH47	VSS	AV20
AH7	VSS	AV24
AJ19	VSS	AV30
AJ2	VSS	AV34
AJ20	VSS	AV38
AJ22	VSS	AV42
AJ23	VSS	E46
AJ26	VSS	E48
AJ28	VSS	E49
AJ32	VSS	E6
AJ34	VSS	AV5
AT5	VSS	AV8
AJ4	VSS	AW14
AK12	VSS	AW18
AM41	VSS	AW2
AK19	VSS	BF9
AK26	VSS	AW32
AK22	VSS	AW36
AK23	VSS	AW40
AK28	VSS	AW52
	VSS	AY11
	VSS	G40
	VSS	G44
	VSS	GS2
	VSS	AF39
	VSS	H16
	VSS	H20
	VSS	H30
	VSS	H34
	VSS	H38
	VSS	H42

IBEXPEAK-M-GP-NF 71.0HM55.A0U 71.0HM55.A0U

IBEXPEAK-M-GP-NF 71.0HM55.A0U

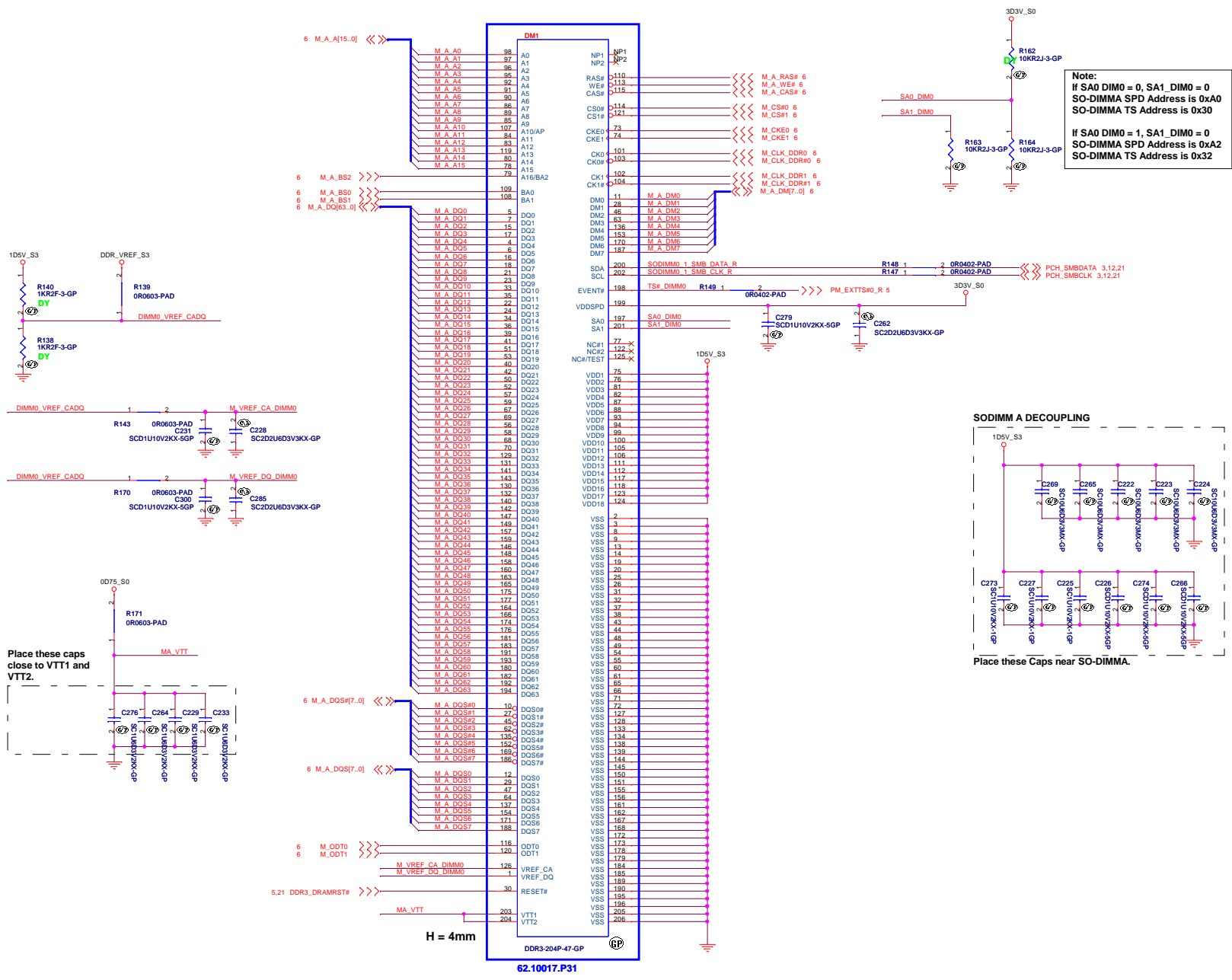
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Taipei Hsien 221, Taiwan, R.O.C

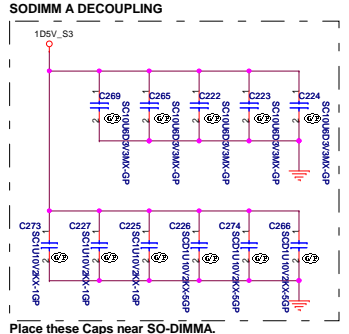
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Size: Custom Document Number: **LA36 MB DIS** Rev: -1

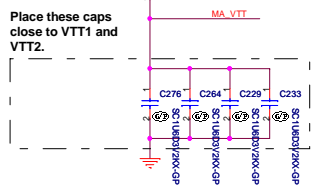
Date: Monday, March 22, 2010 Sheet 19 of 58



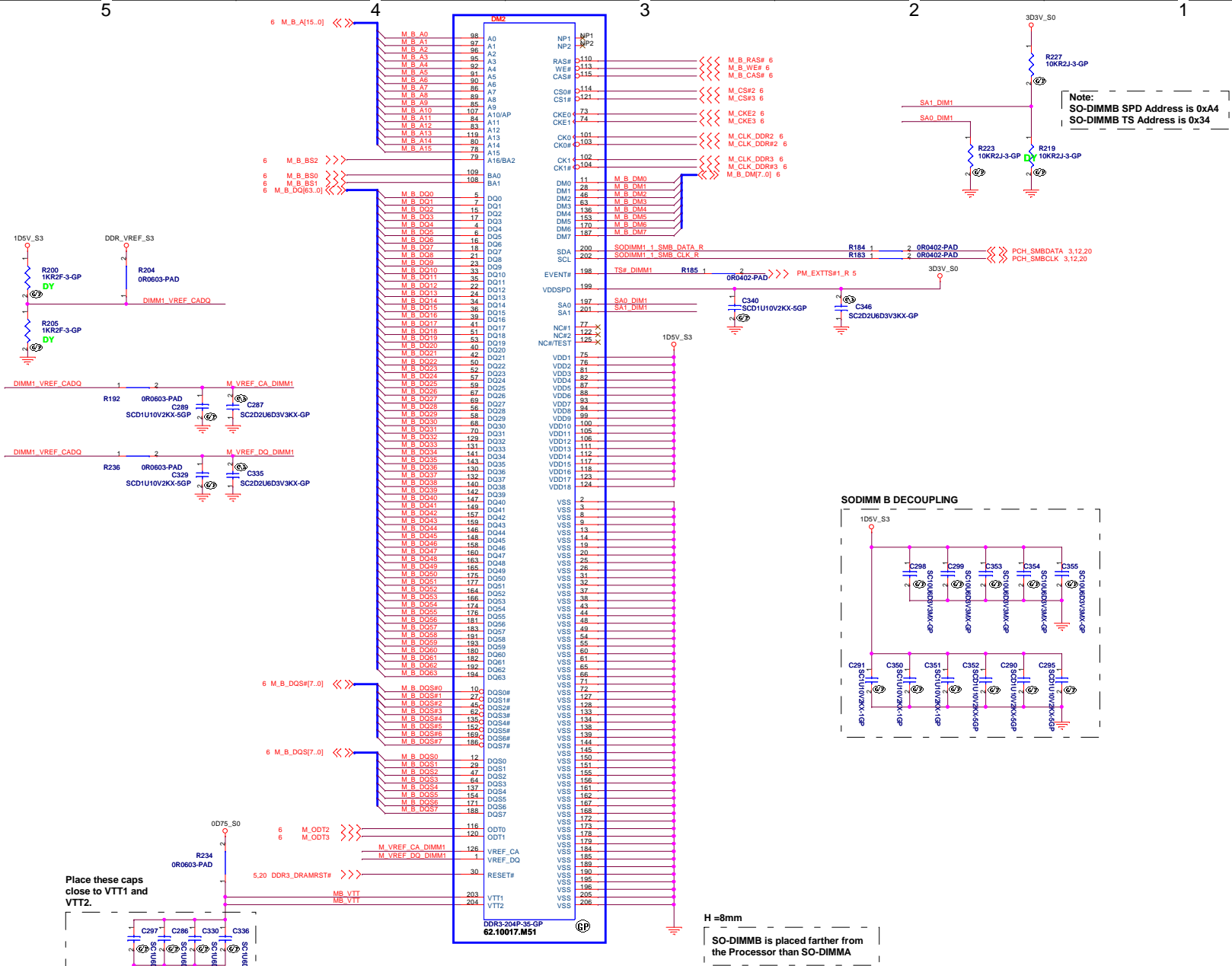
Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30
 If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32



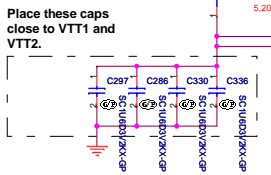
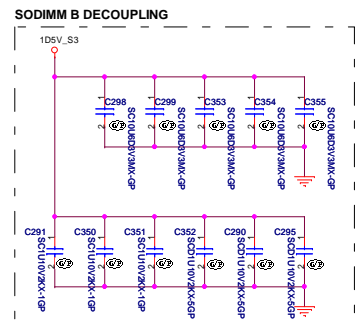
Place these Caps near SO-DIMMA.



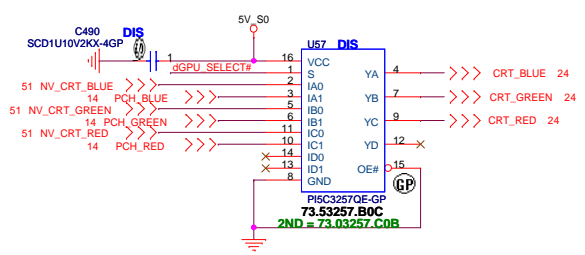
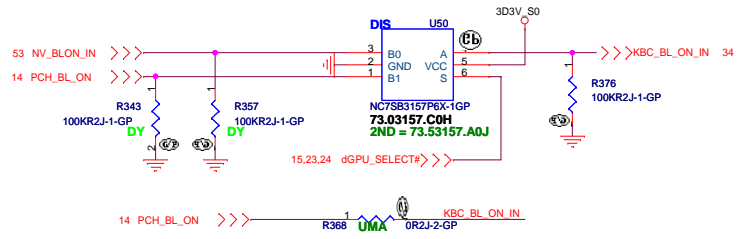
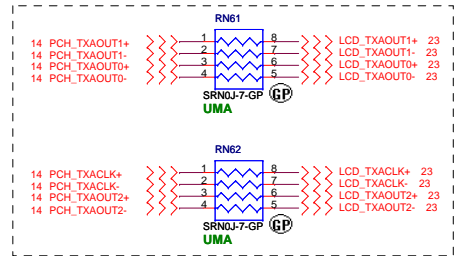
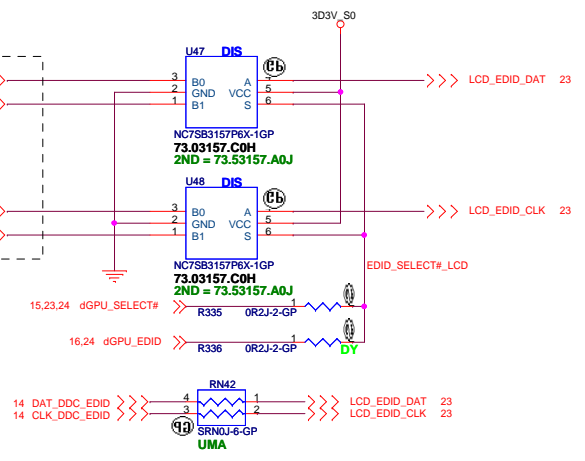
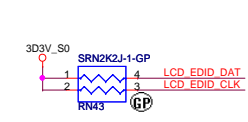
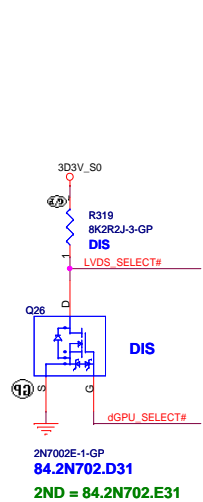
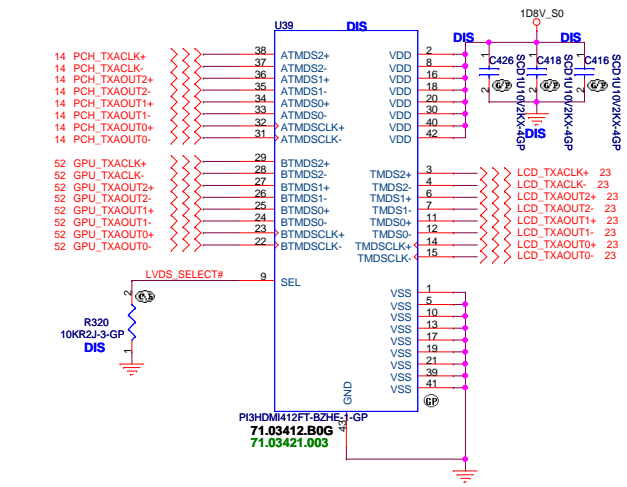
Place these caps close to VTT1 and VTT2.



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34



H=8mm
SO-DIMMB is placed farther from the Processor than SO-DIMMA



FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<-Variant Name>

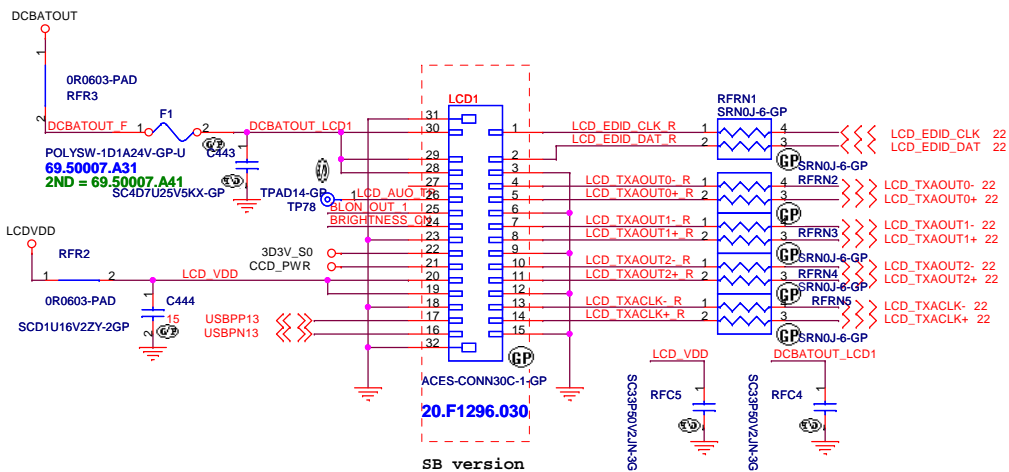
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 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsinchu, Taipei Hsein 221, Taiwan, R.O.C

Title: **Display MUX**

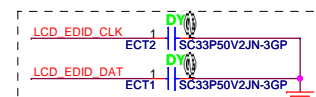
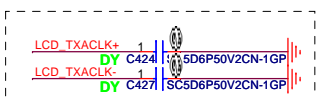
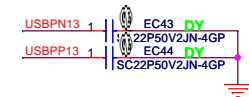
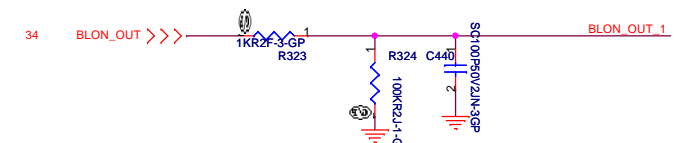
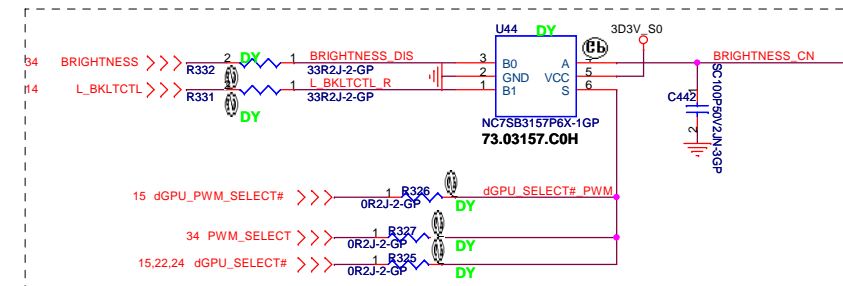
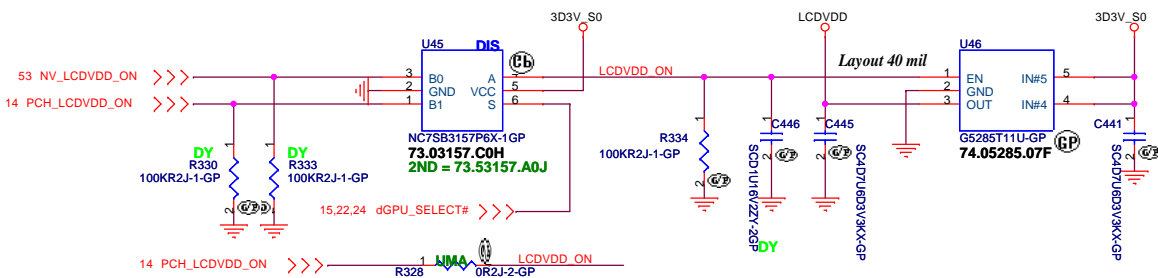
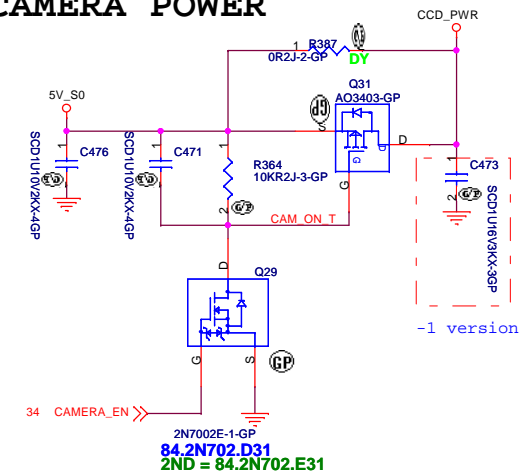
Size: Custom Document Number: **LA36 MB DIS** Rev: -1

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LCD/INVERTER/CCD CONN



CAMERA POWER



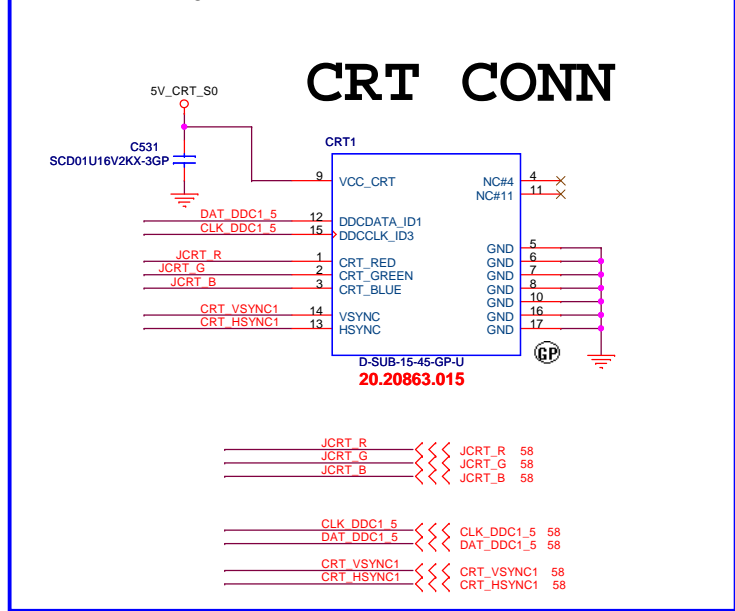
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緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C

File
LCD & CCD

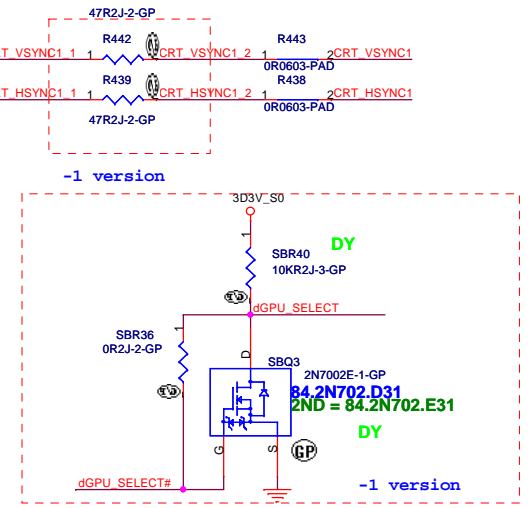
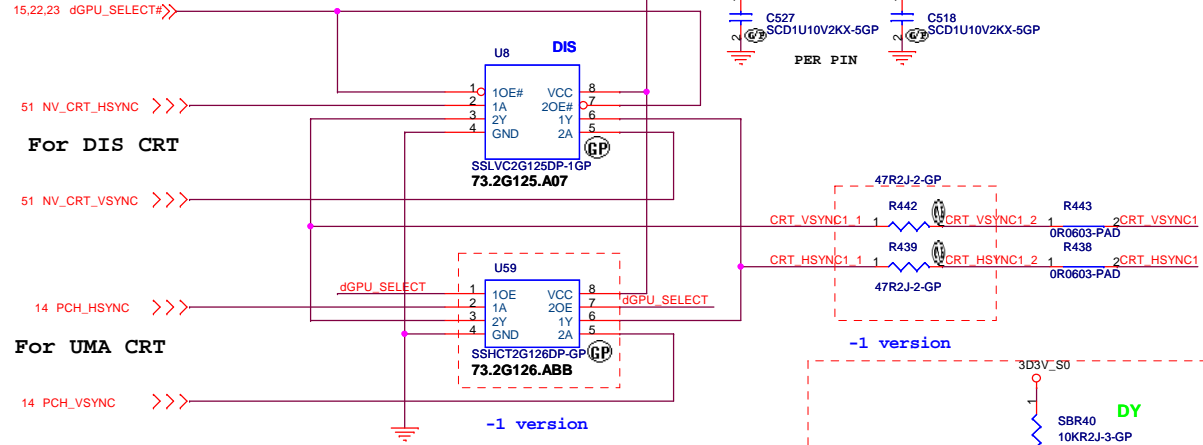
Size A3 Document Number
LA36 MB DIS

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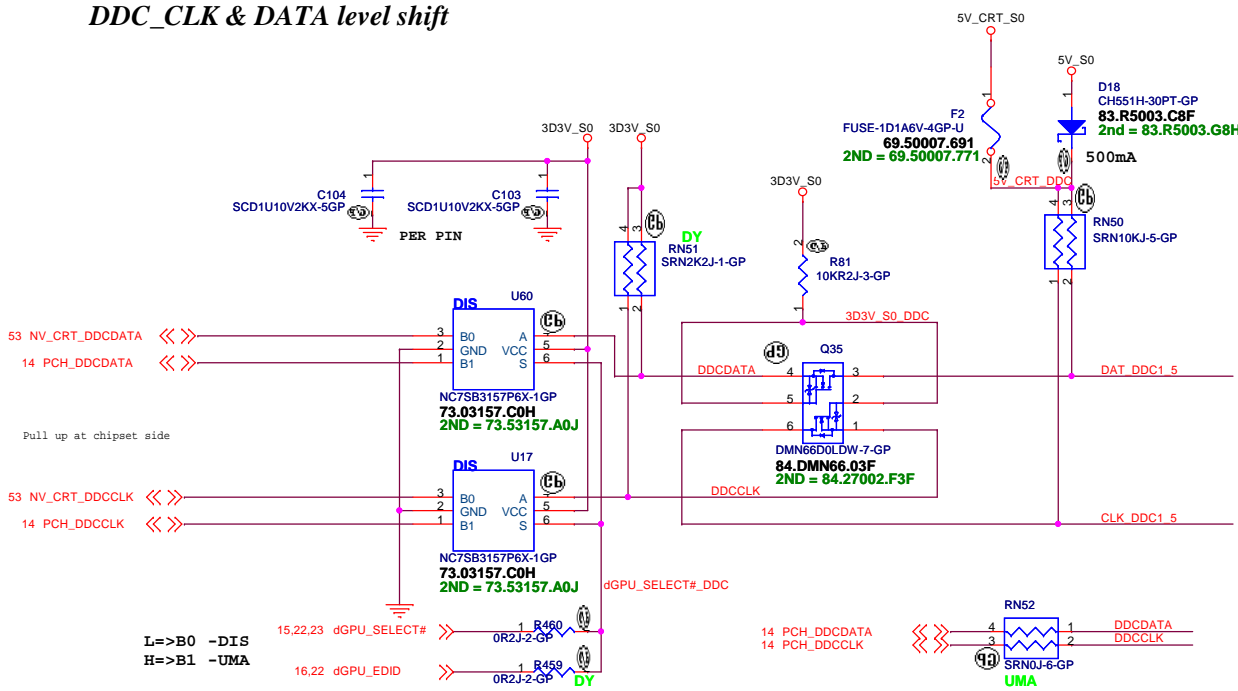


L=>B0 -DIS
H=>B1 -UMA

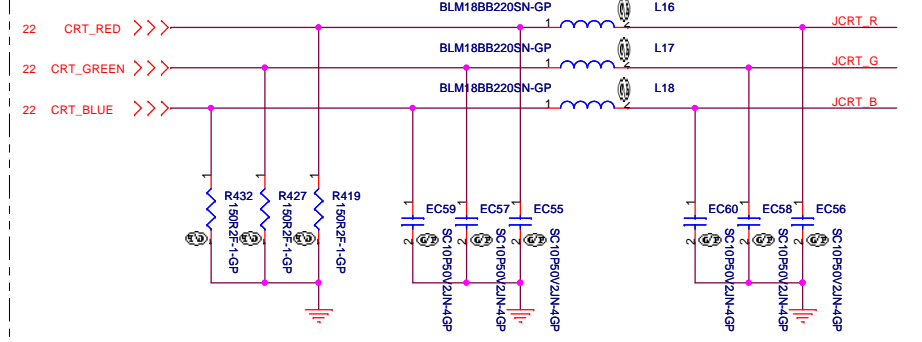
Hsync & Vsync level shift



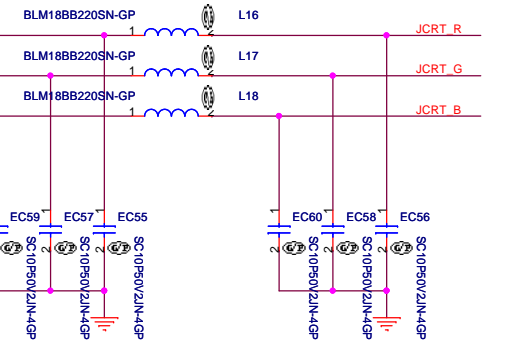
DDC_CLK & DATA level shift

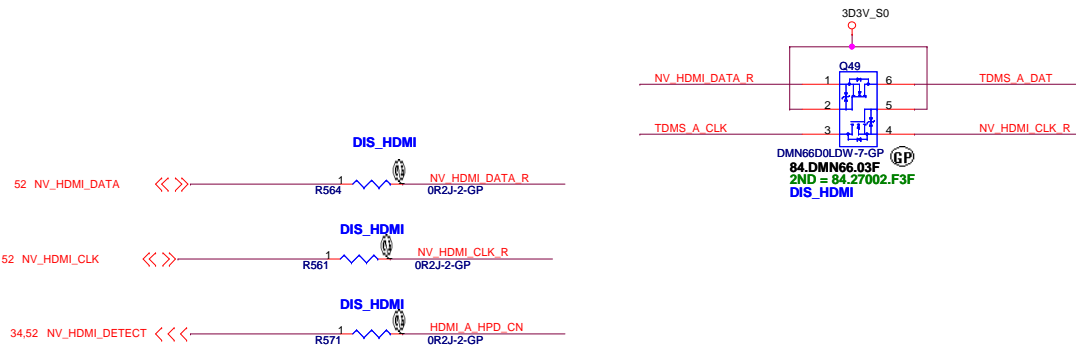
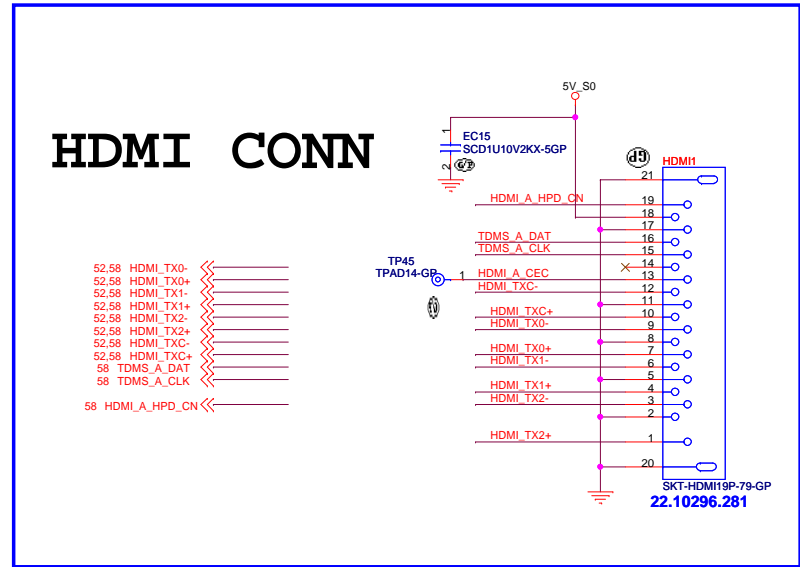
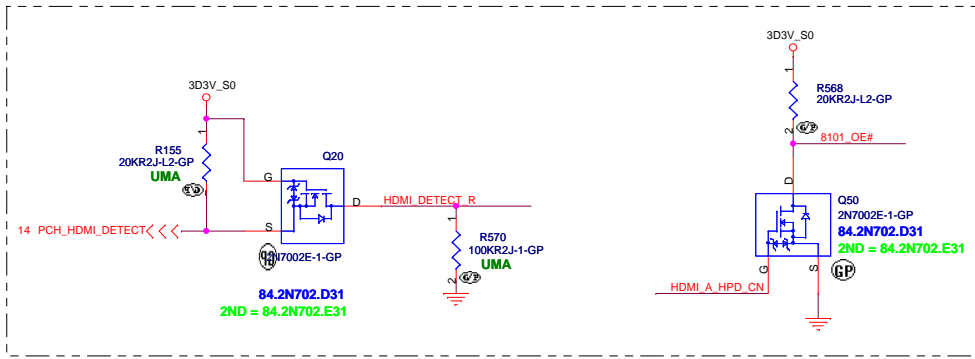
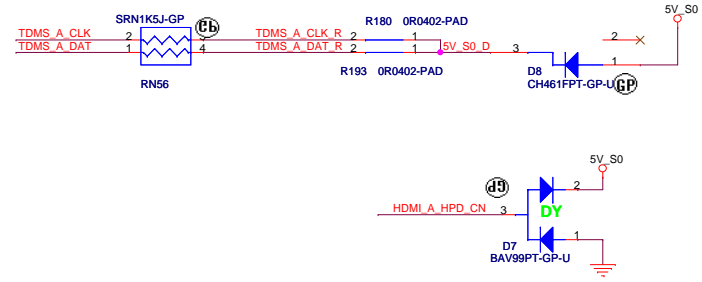
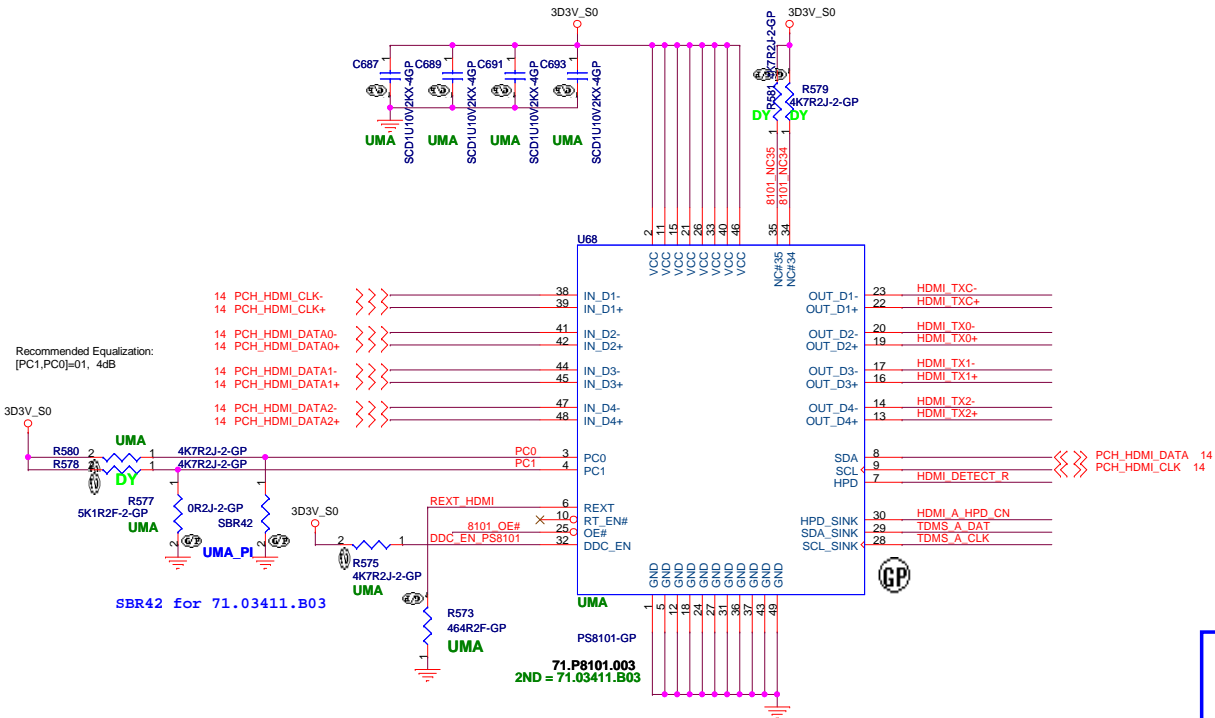


CRT Termination/EMI Filter

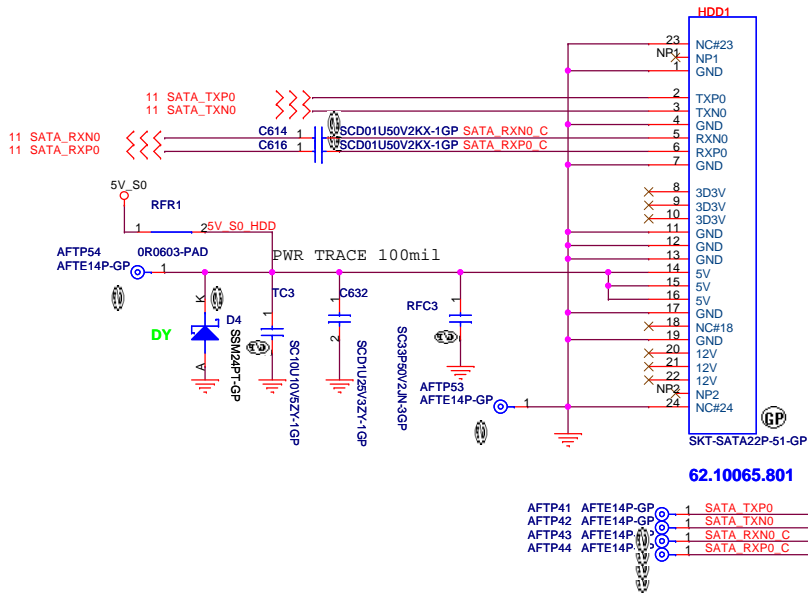


Place Close Connector

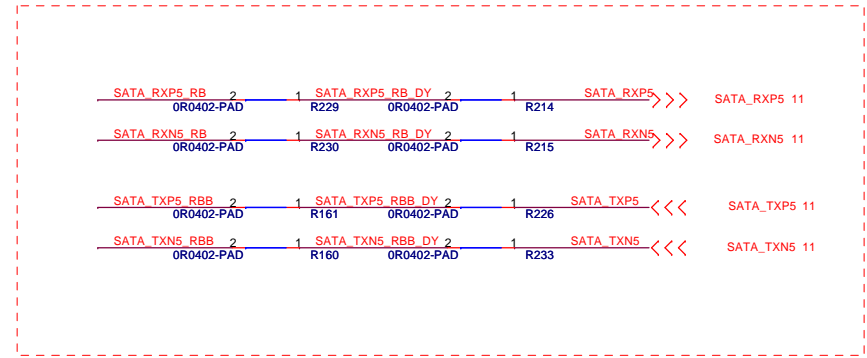
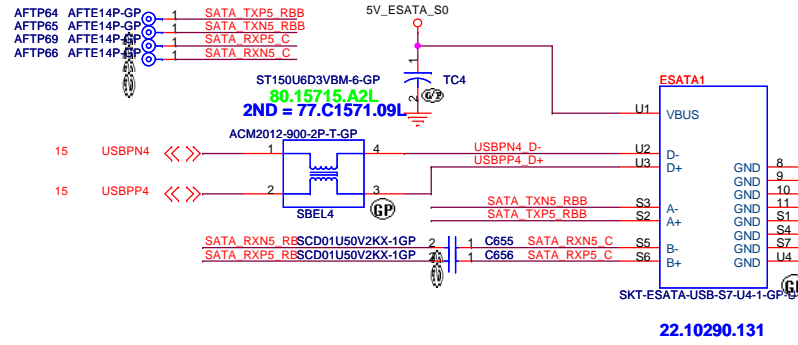




SATA Connector

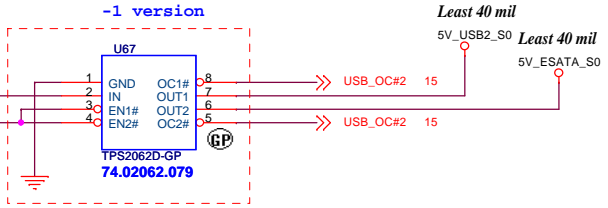
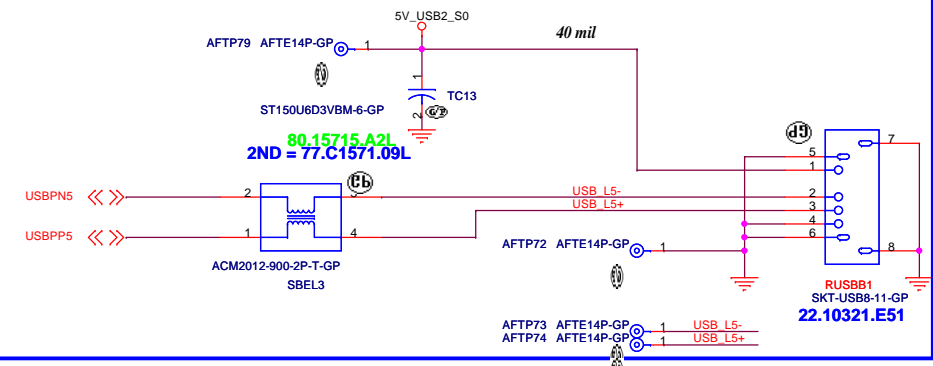


E-SATA Connector

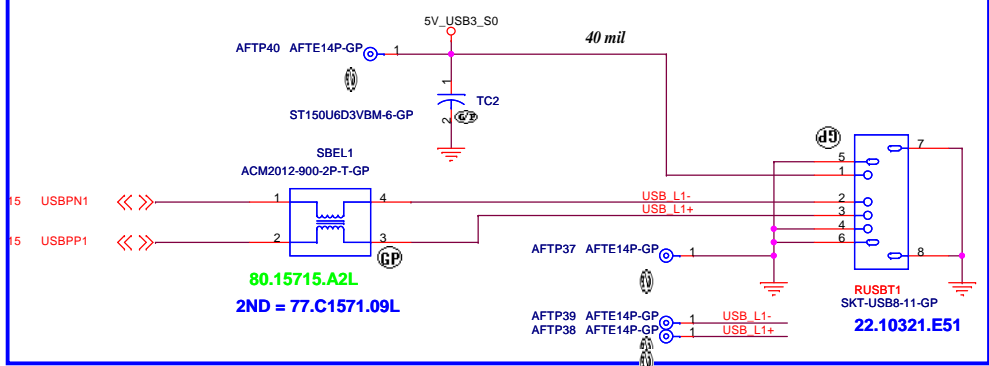


-1 Version

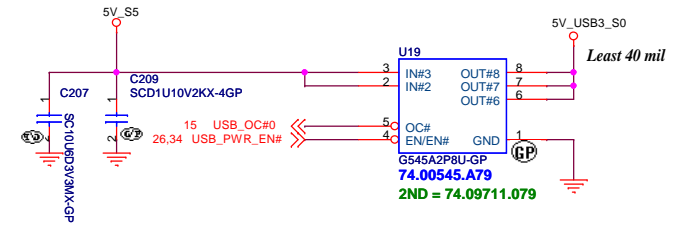
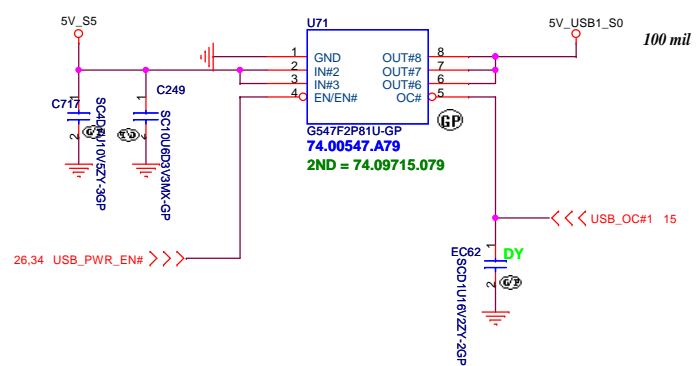
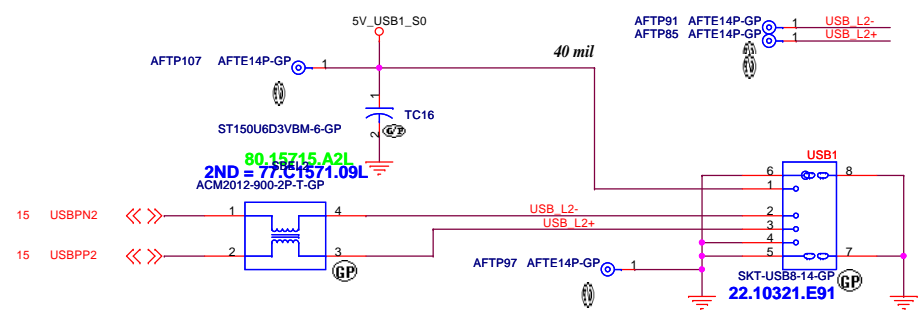
USB2



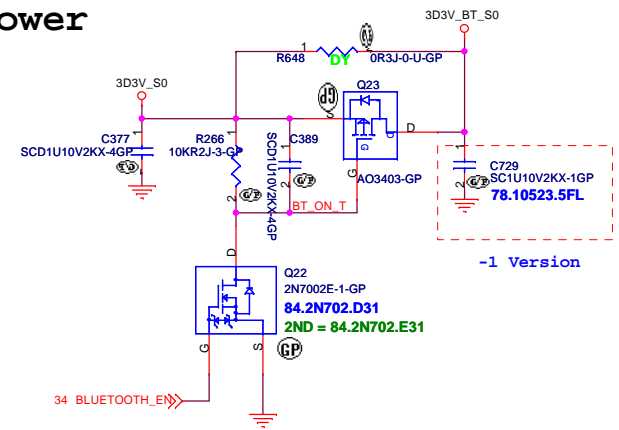
USB3



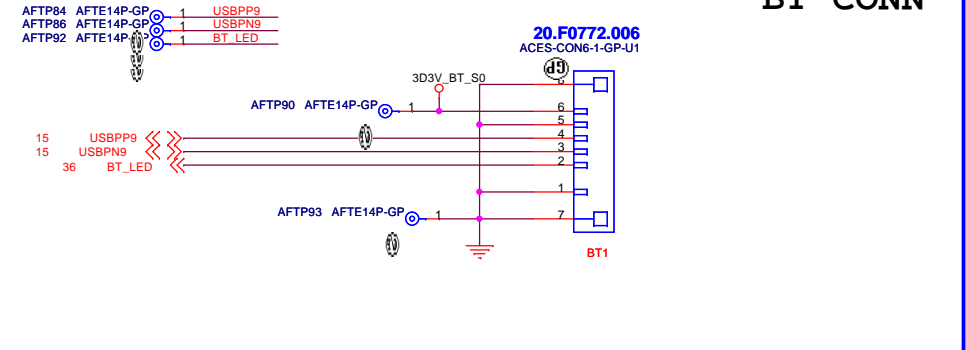
USB1

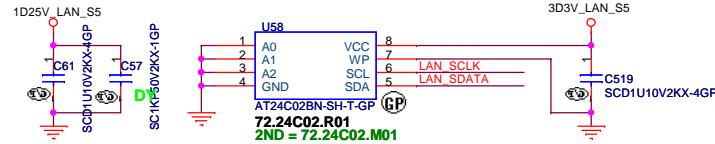
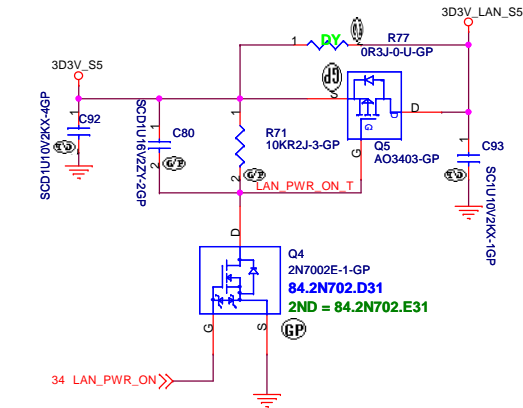
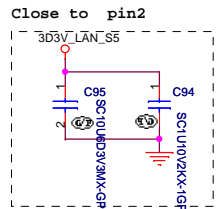
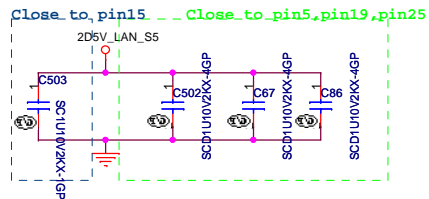
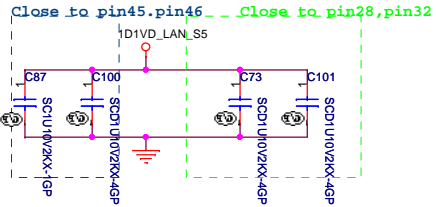
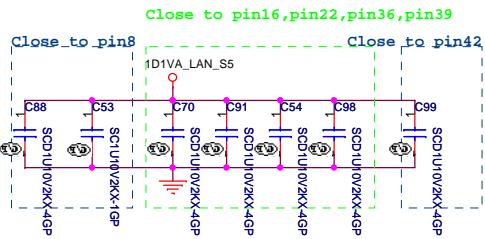


Bluetooth Power

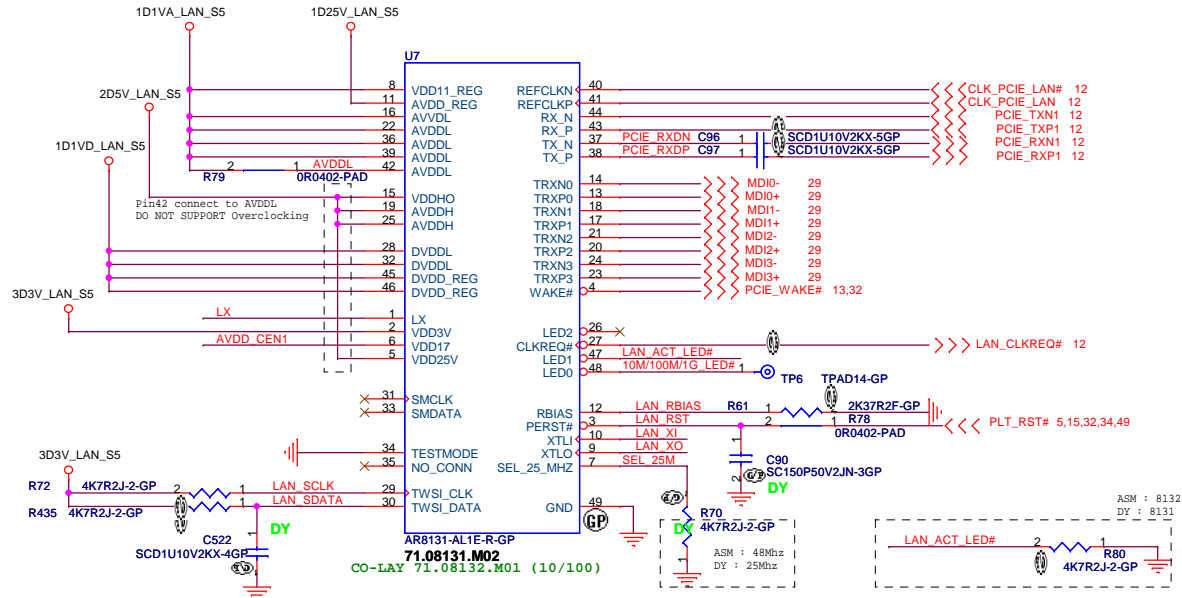
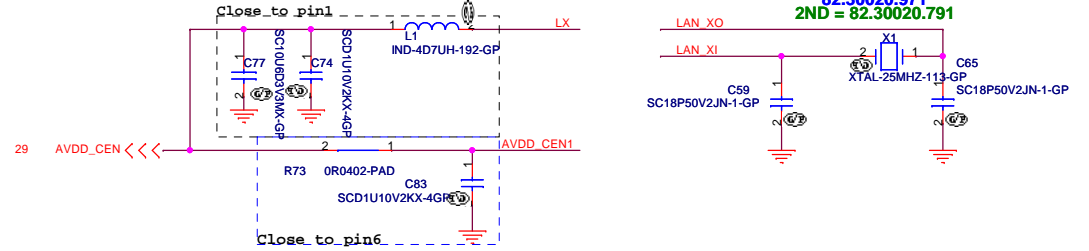
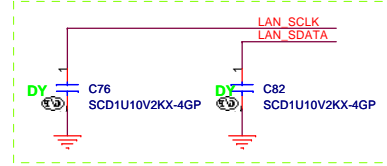


BT CONN





for AR8131M apply in the future

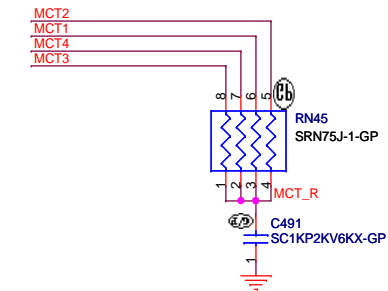
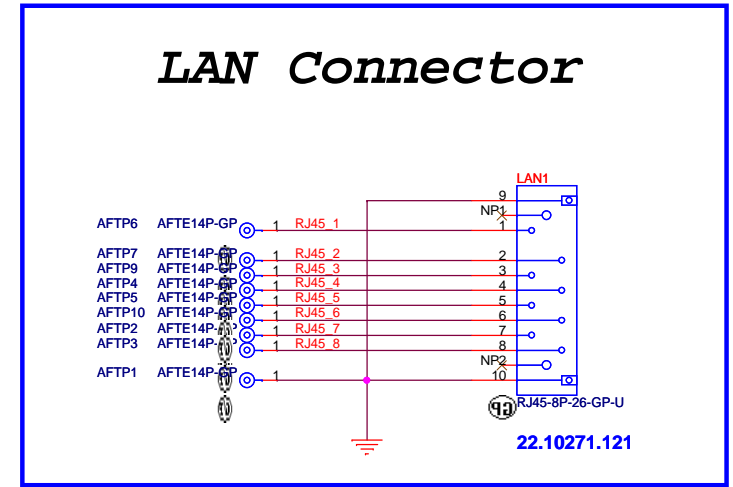
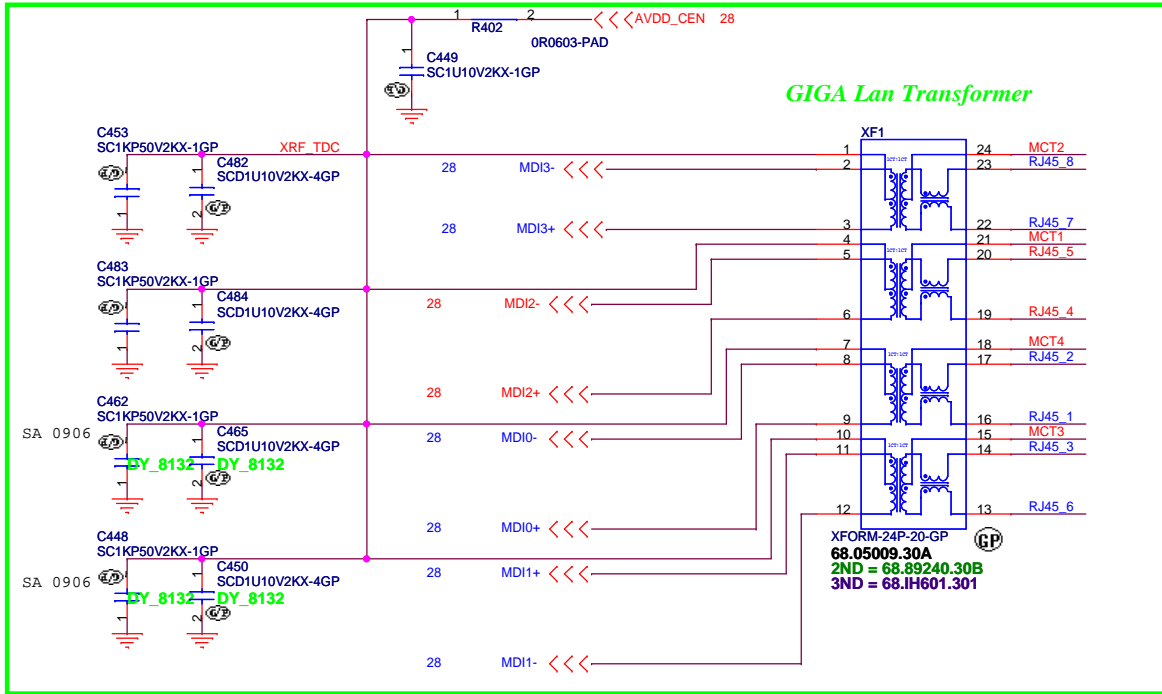


<Variant Name>

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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



<Variant Name>

緯創資通

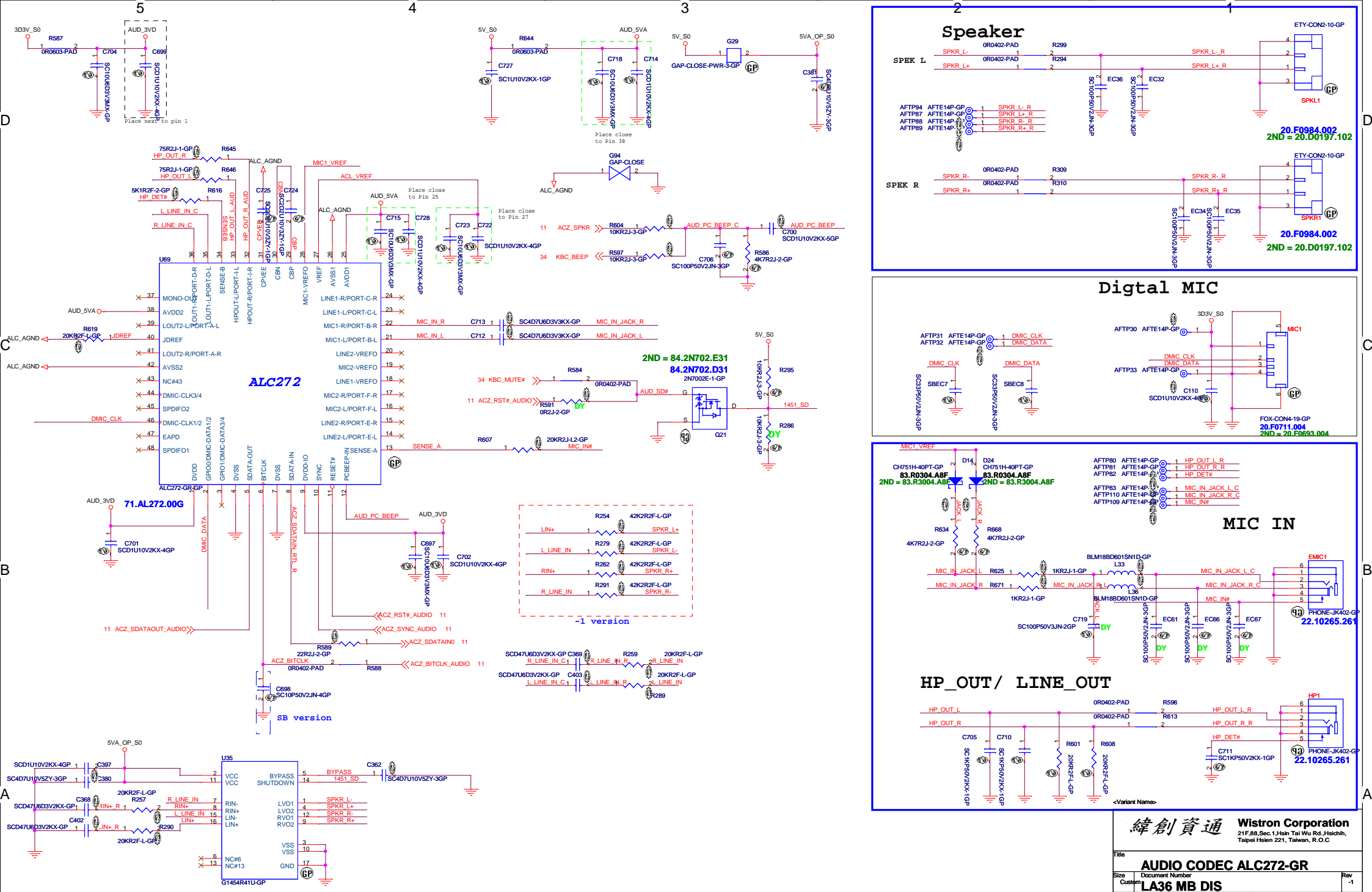
Wistron Corporation

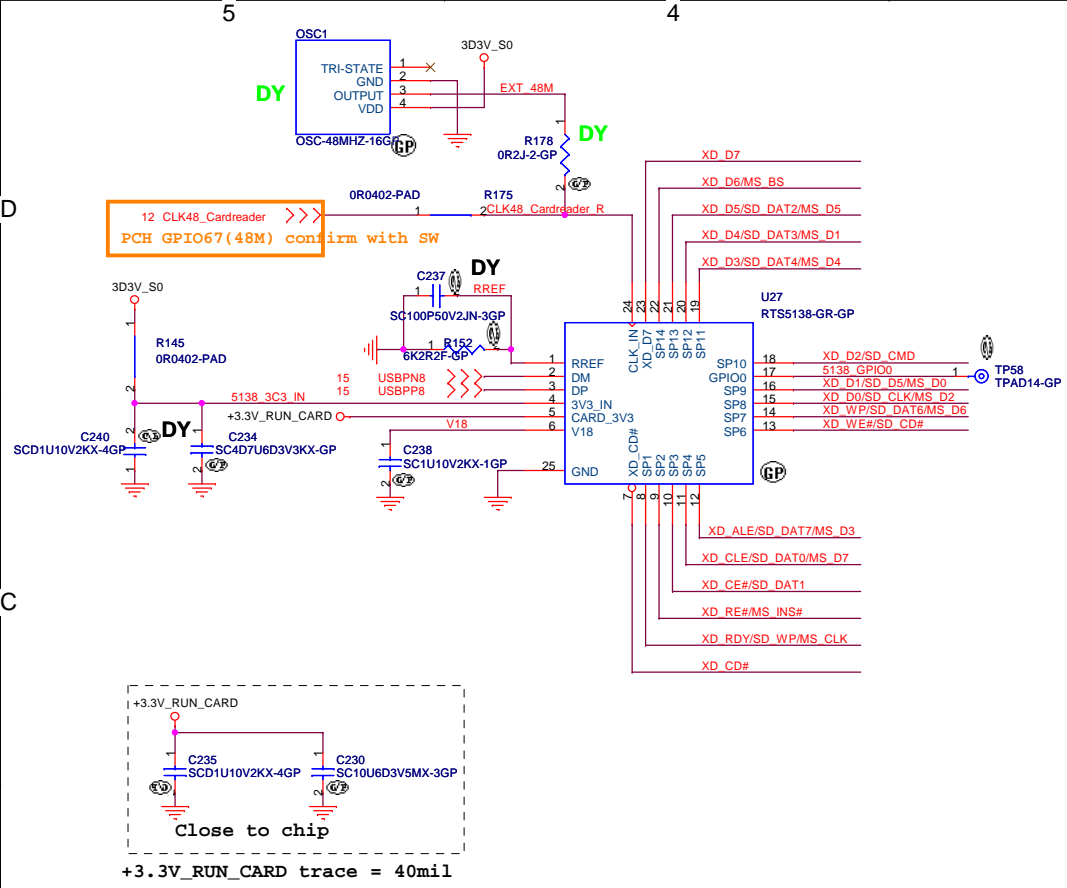
21F,66,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title
LAN CONN

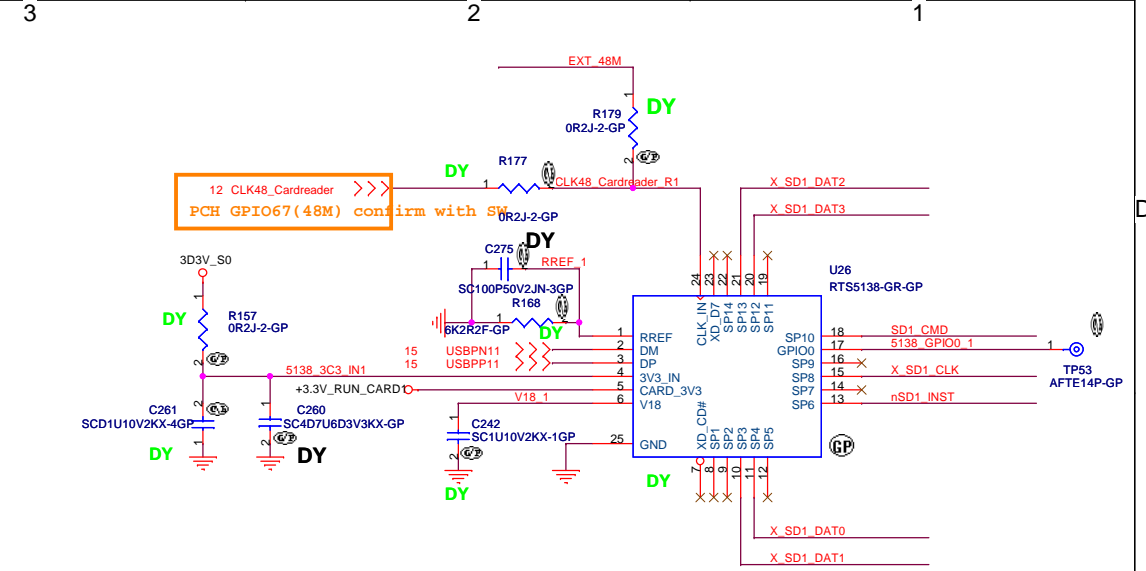
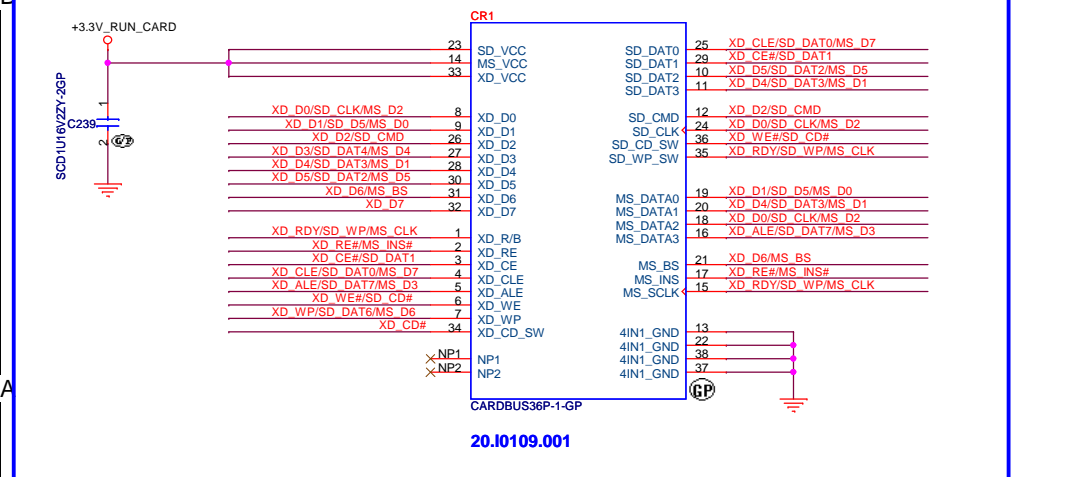
Size Document Number
Custom **LA36 MB DIS**

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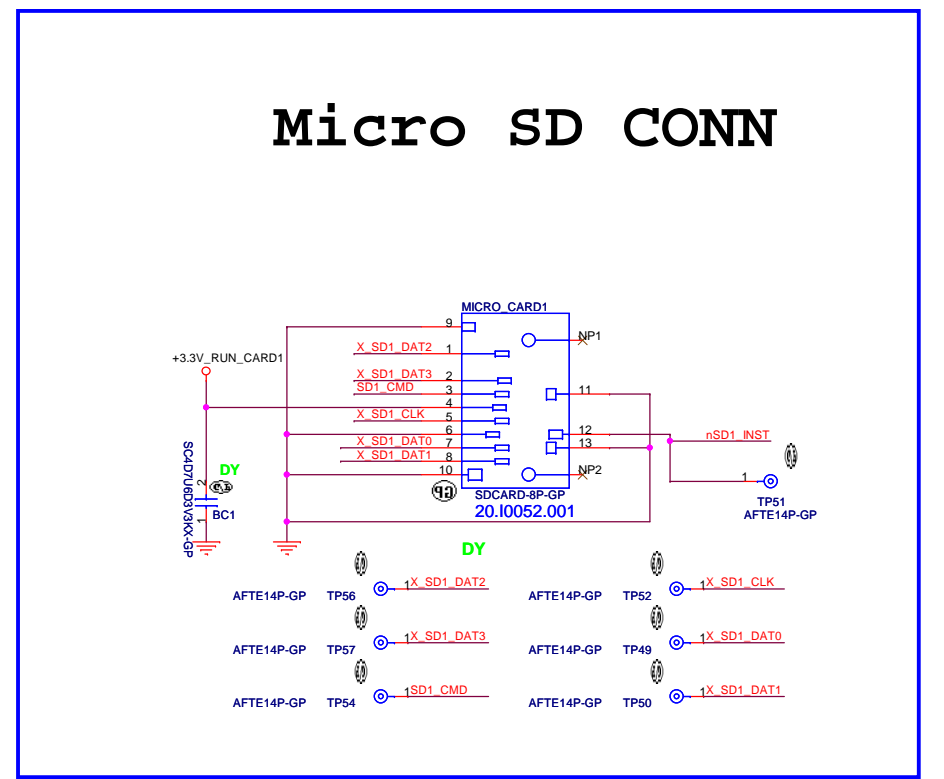




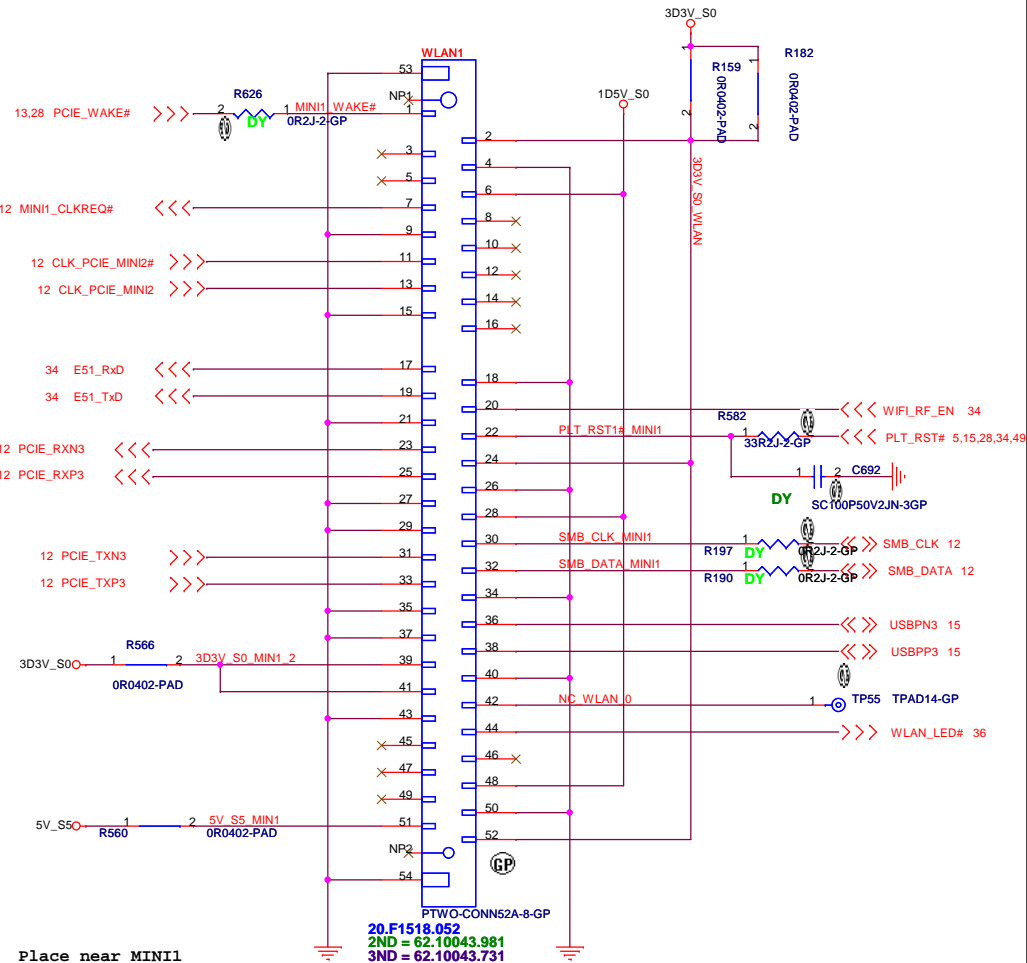
4 IN 1 CONN



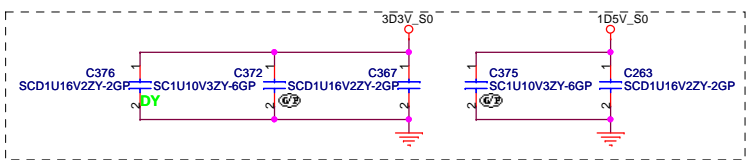
Micro SD CONN



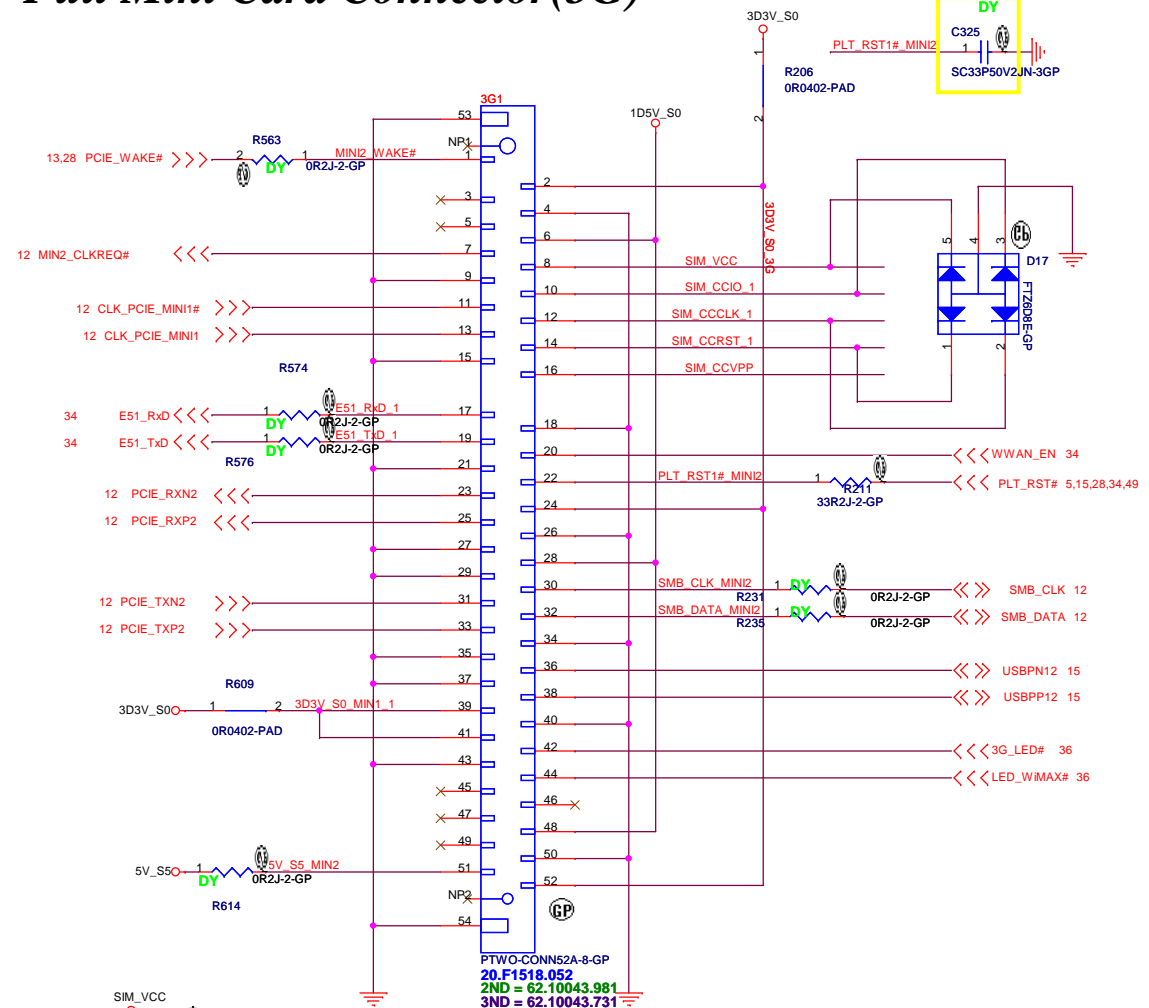
Half Mini Card Connector(WLAN)



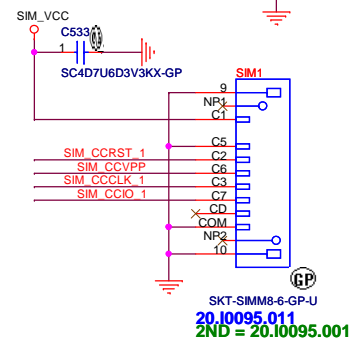
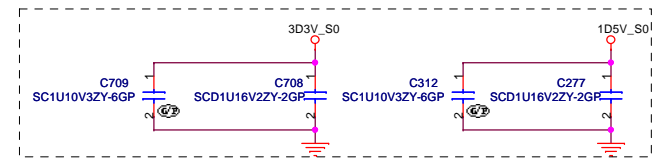
Place near MINI1
 20.F1518.052
 2ND = 62.10043.981
 3ND = 62.10043.731



Full Mini Card Connector(3G)



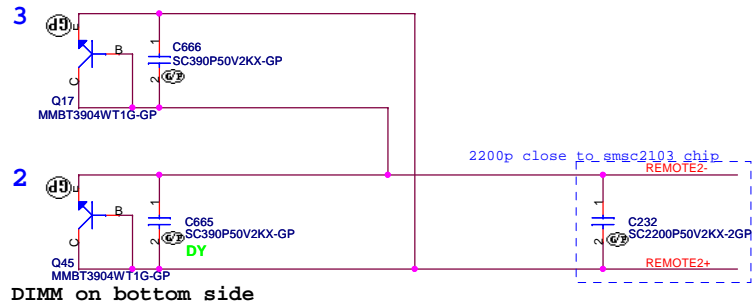
Place near MINIC2



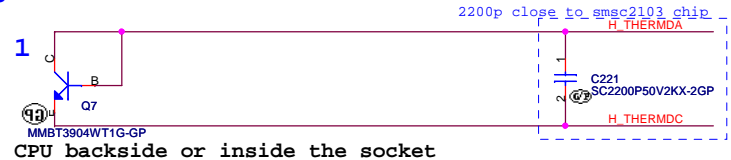
20.I0095.011
 2ND = 20.I0095.001

<Variant Name>	
緯創資通 Wistron Corporation	
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Close to PCH on top side.

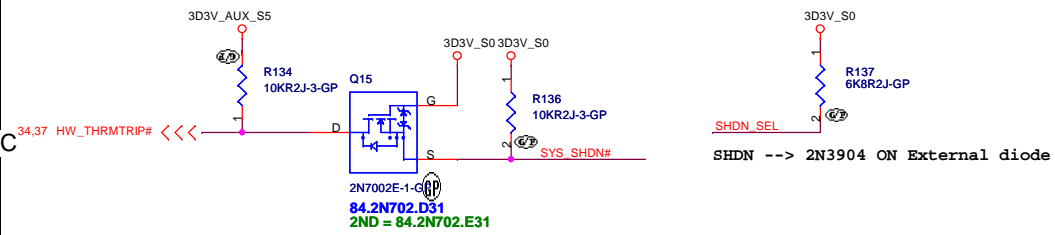


DIMM on bottom side

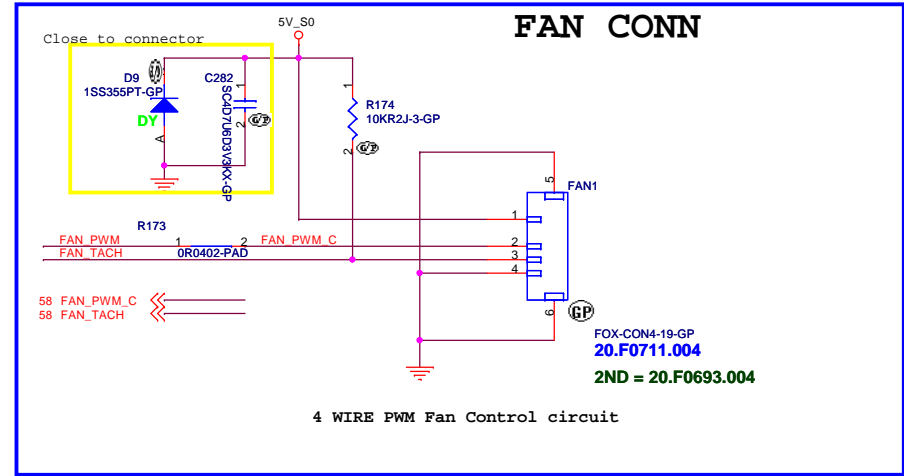


CPU backside or inside the socket

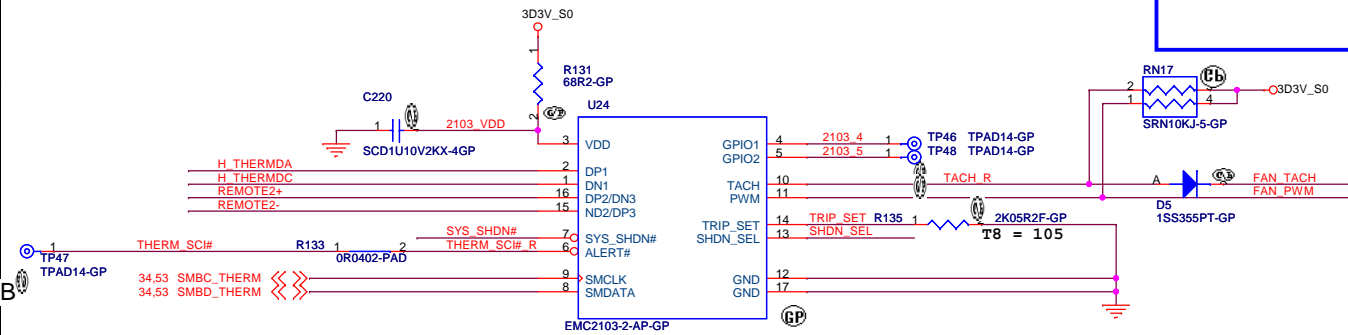
CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.



SHDN --> 2N3904 ON External diode



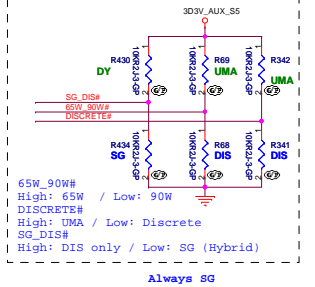
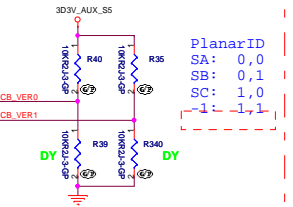
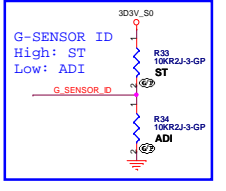
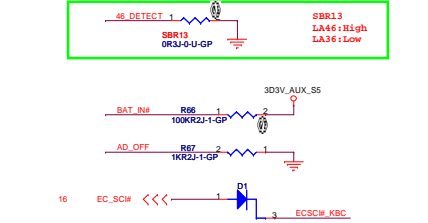
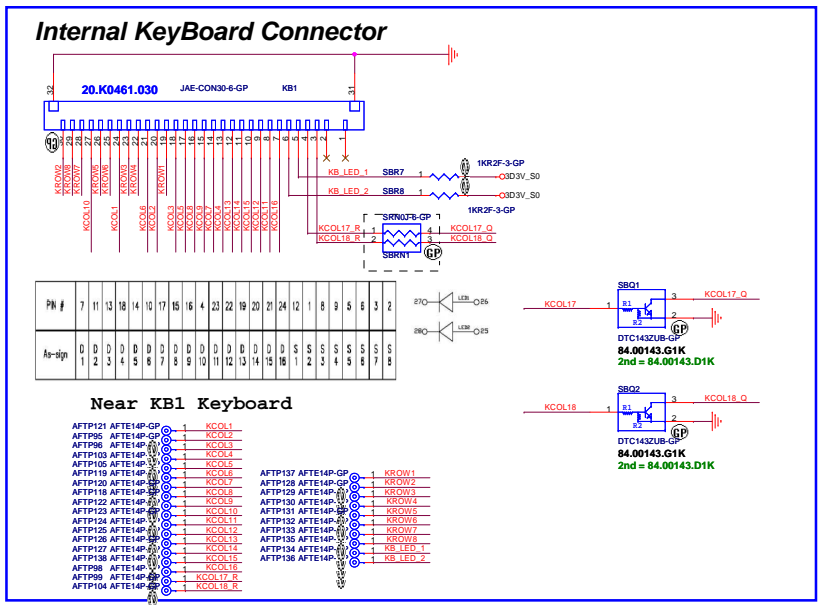
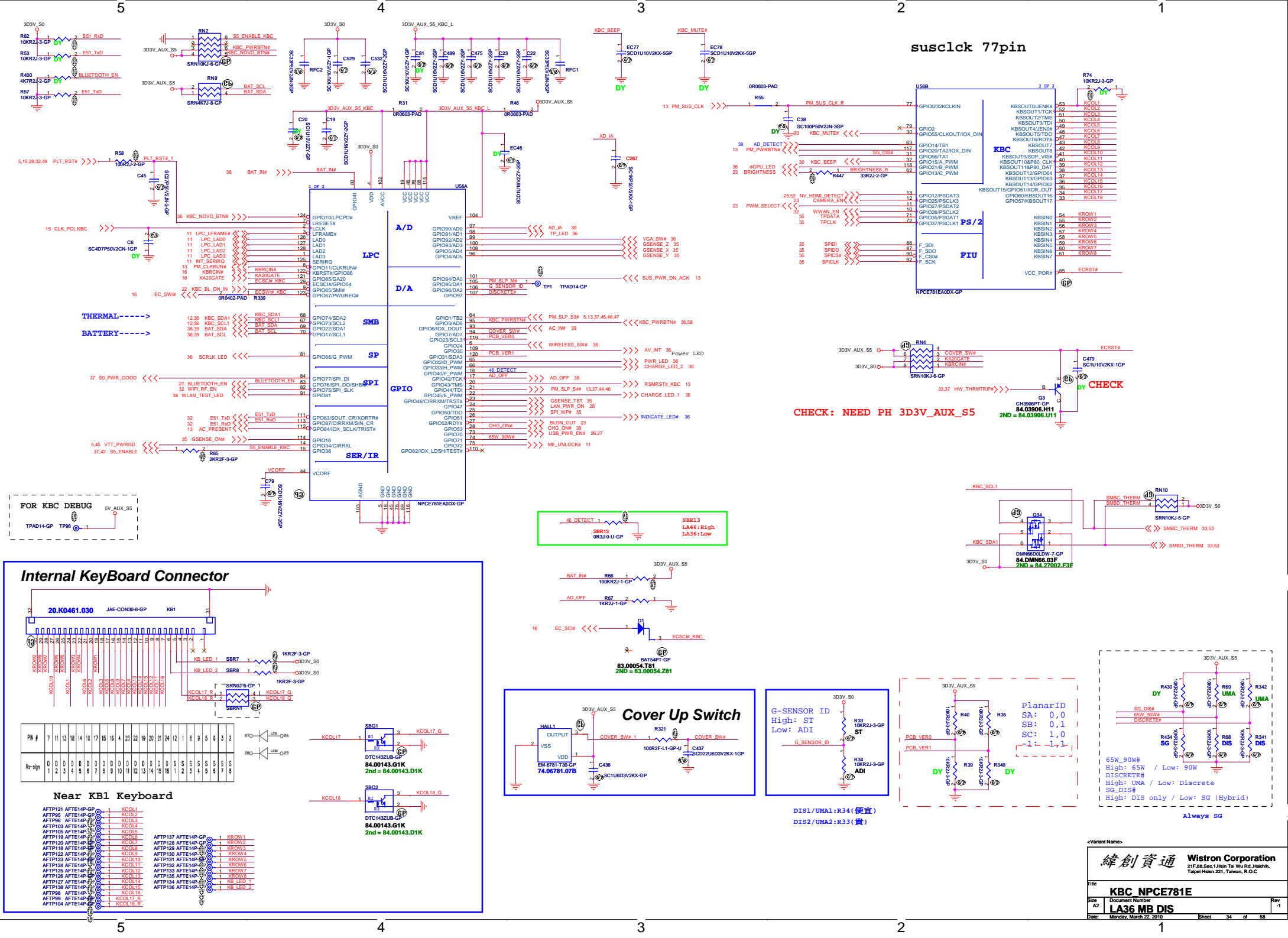
4 WIRE PWM Fan Control circuit



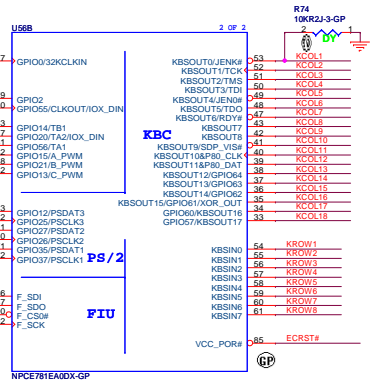
pin6, ALERT# OD
pin7, SYS_SHDN# OD

<Variant Name>

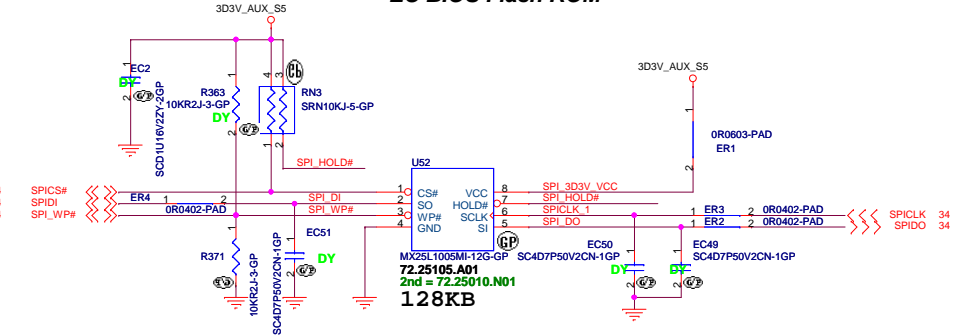
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
THERMAL SMSC2103		
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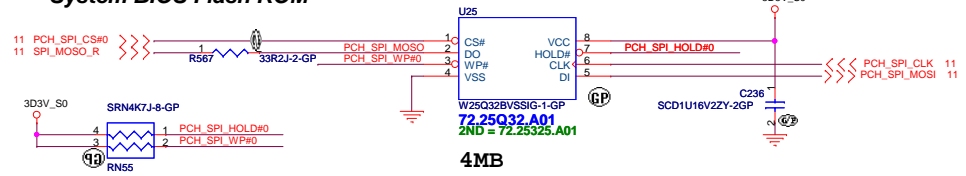
susclk 77pin



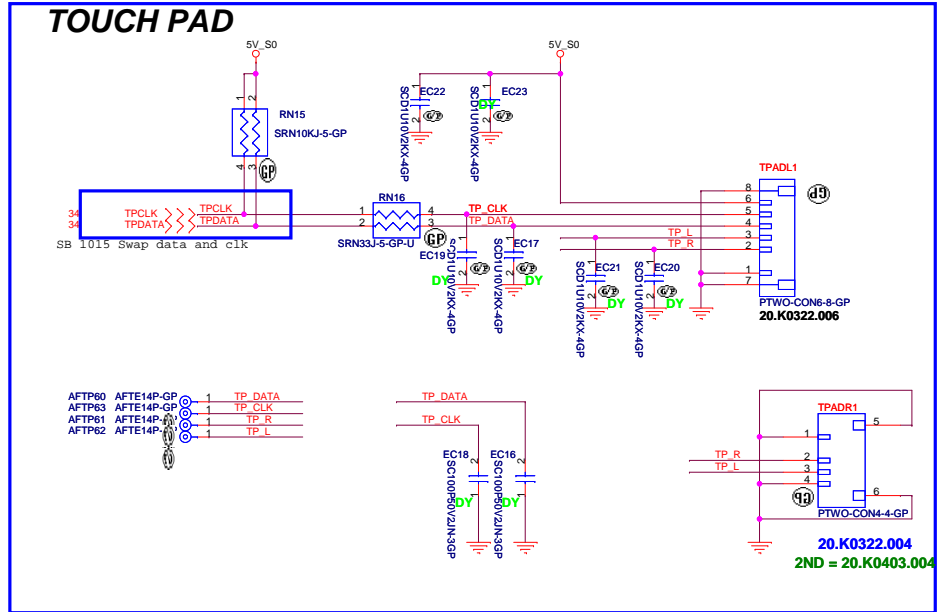
EC BIOS Flash ROM



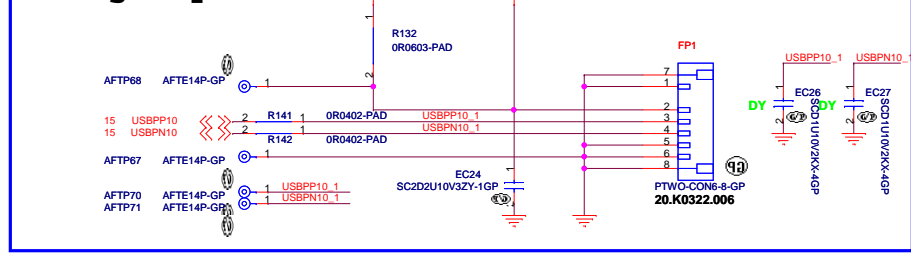
System BIOS Flash ROM



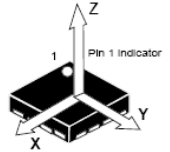
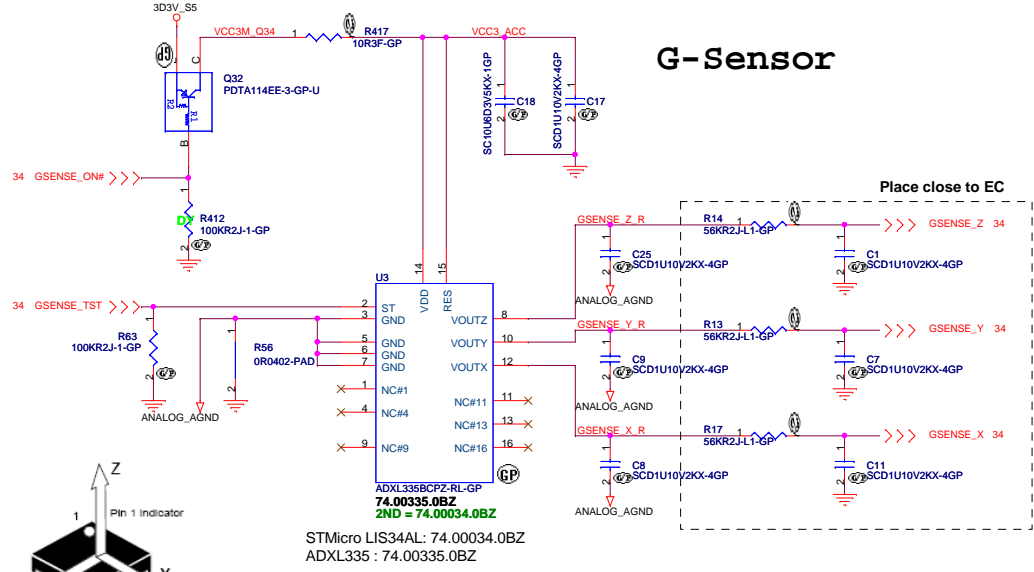
TOUCH PAD

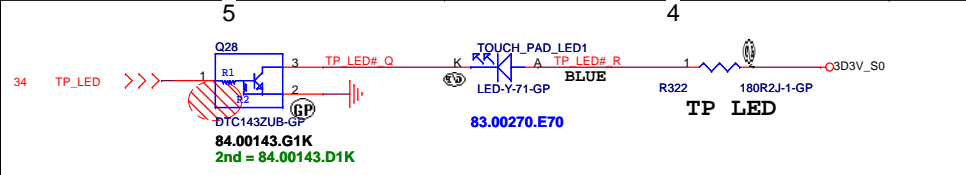


Finger printer

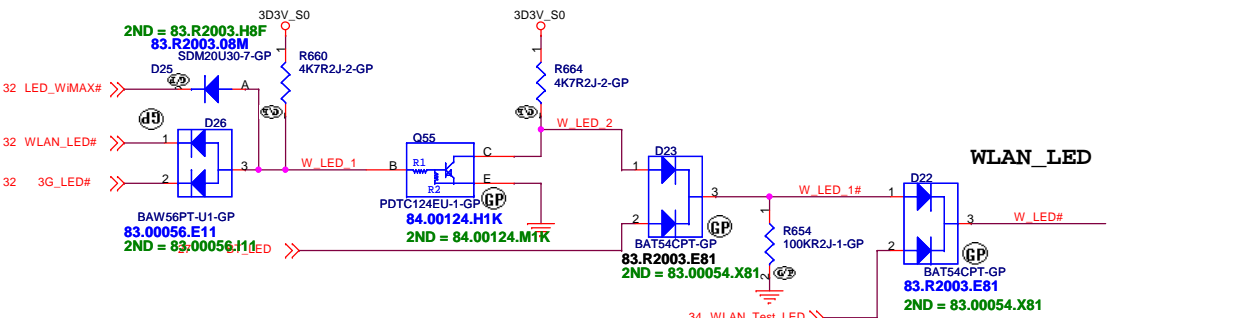
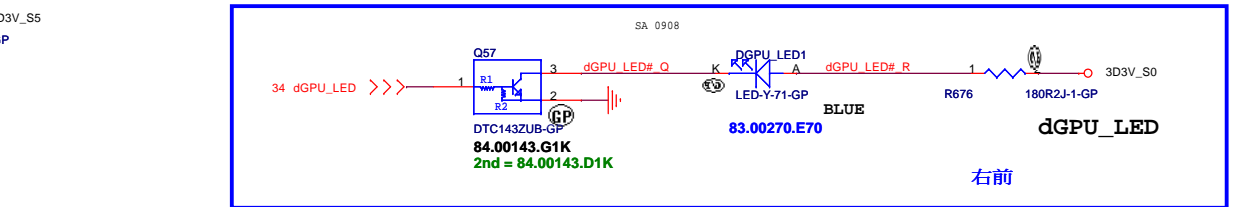
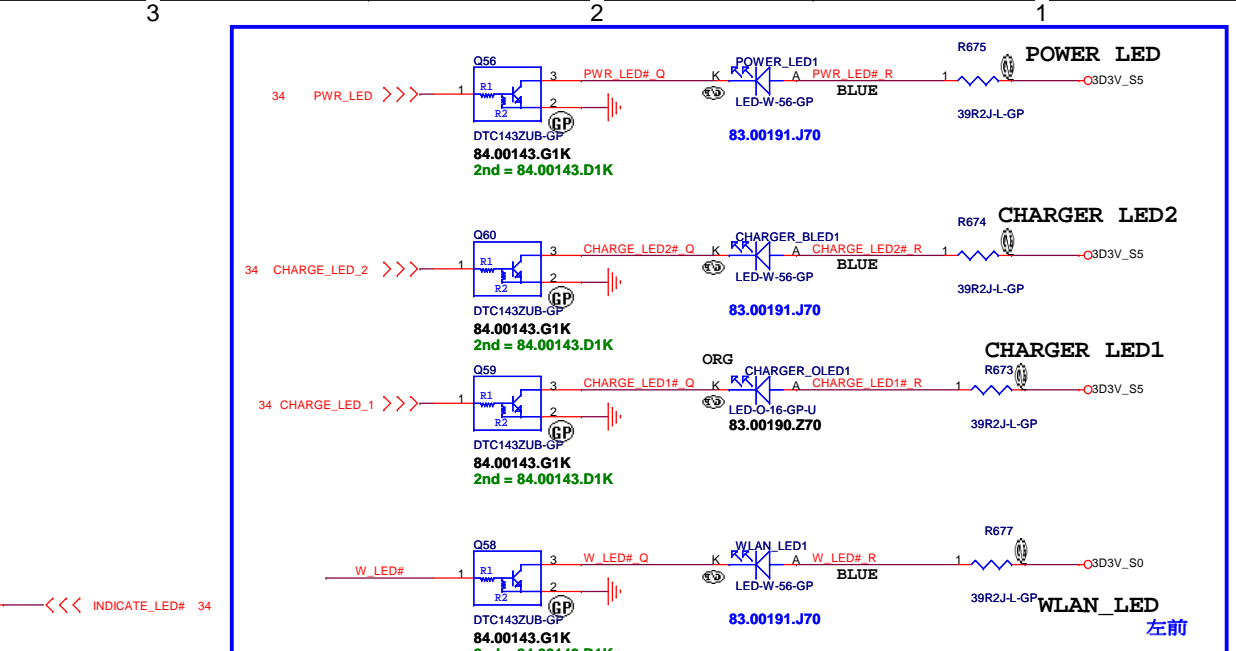
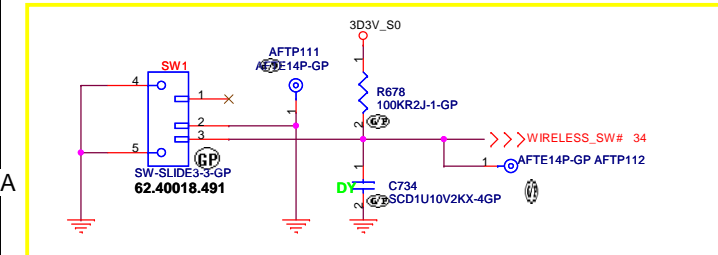
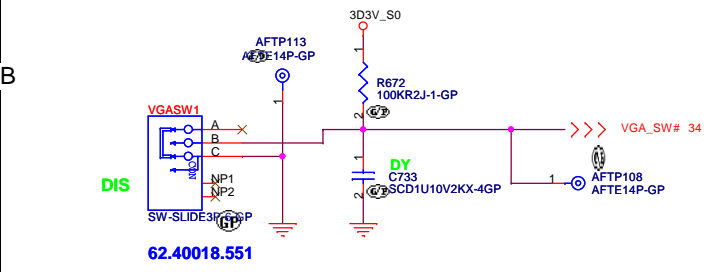
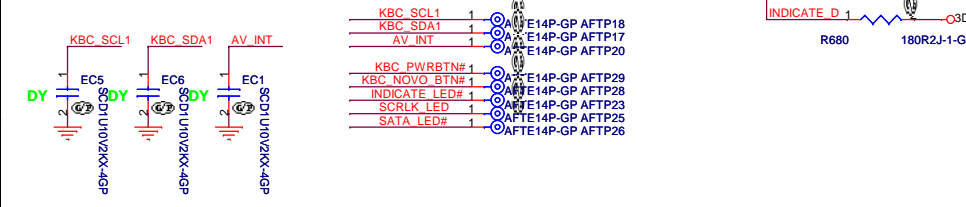
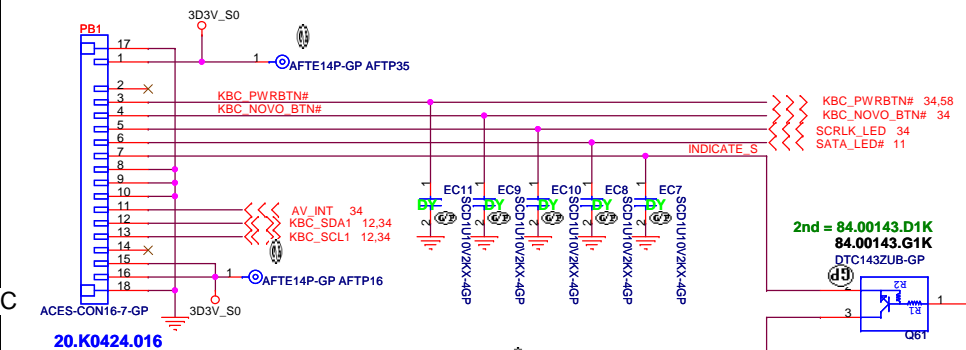


G-Sensor



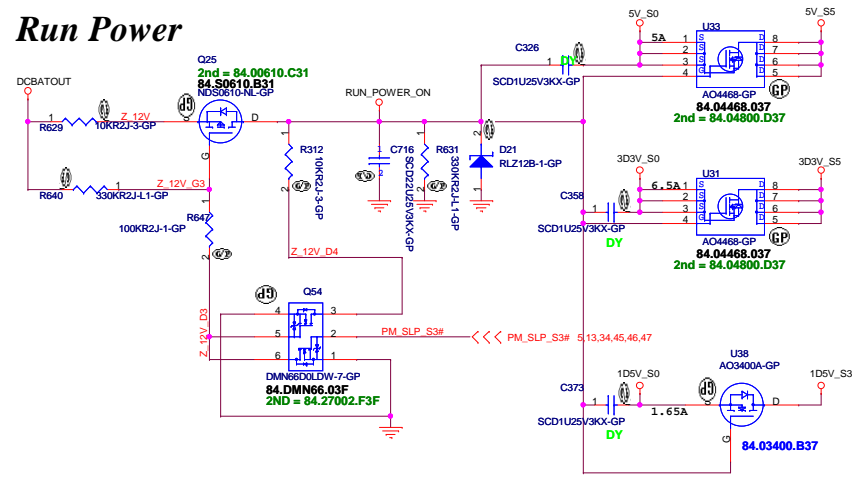


POWER BOARD CONN



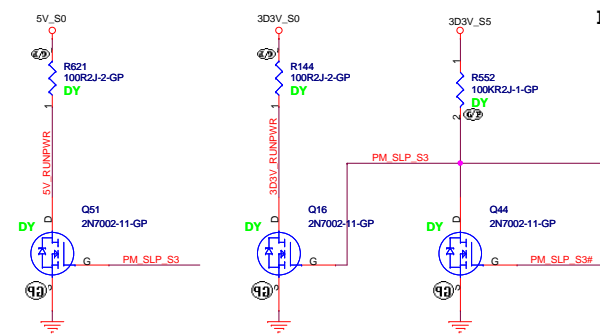
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Run Power

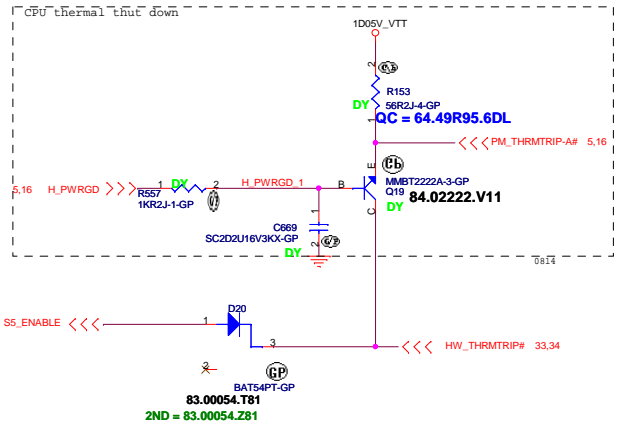
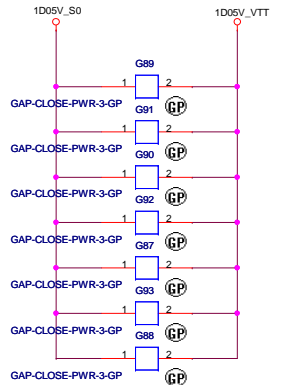


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For Discharge



For Discharge



A

B

C

D

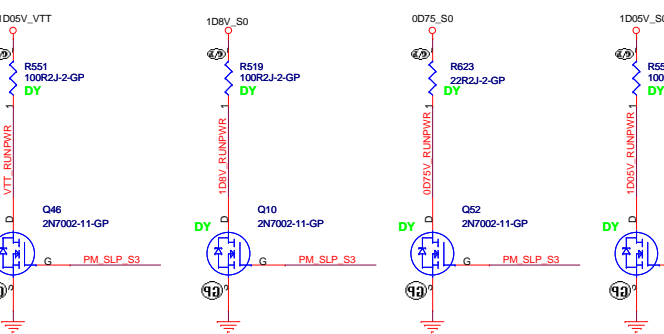
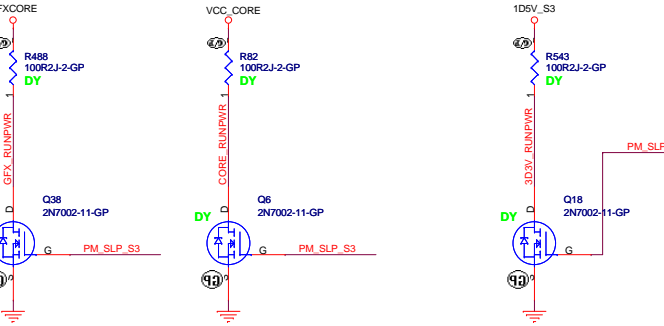
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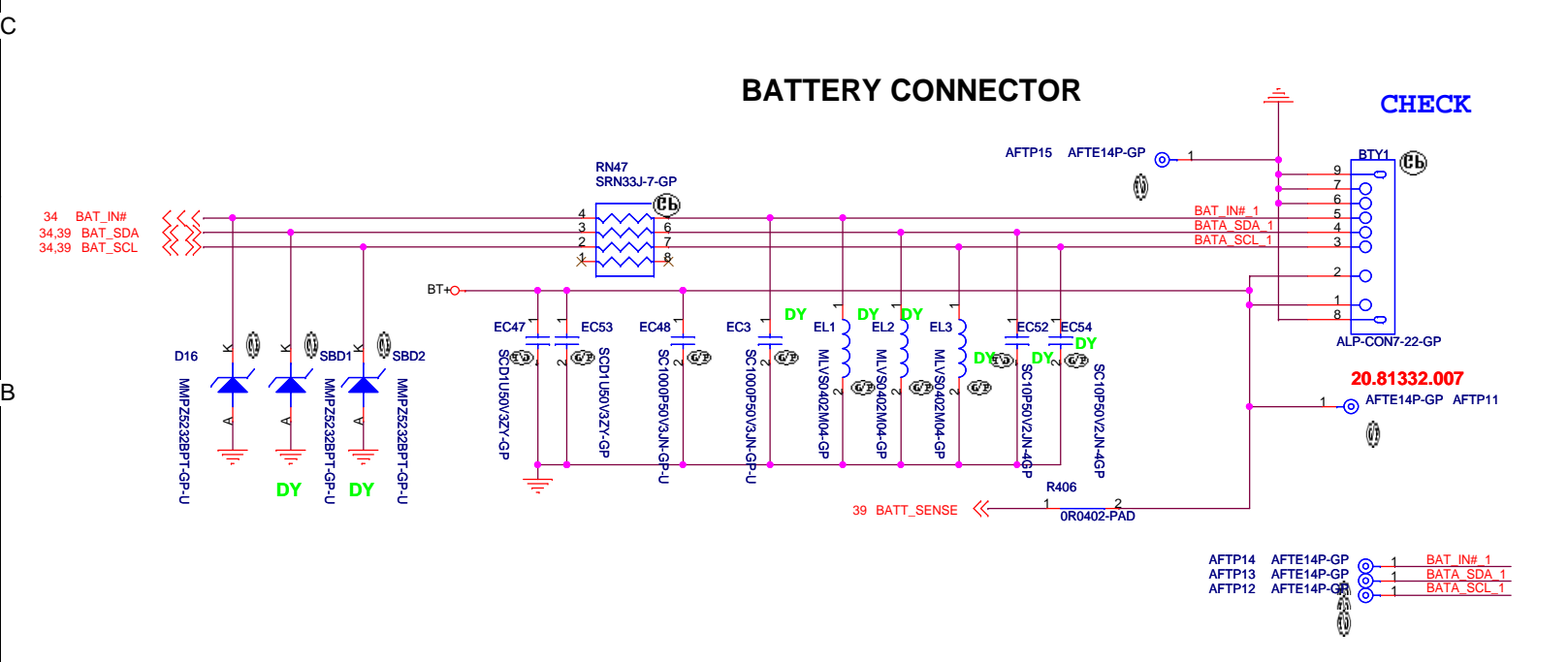
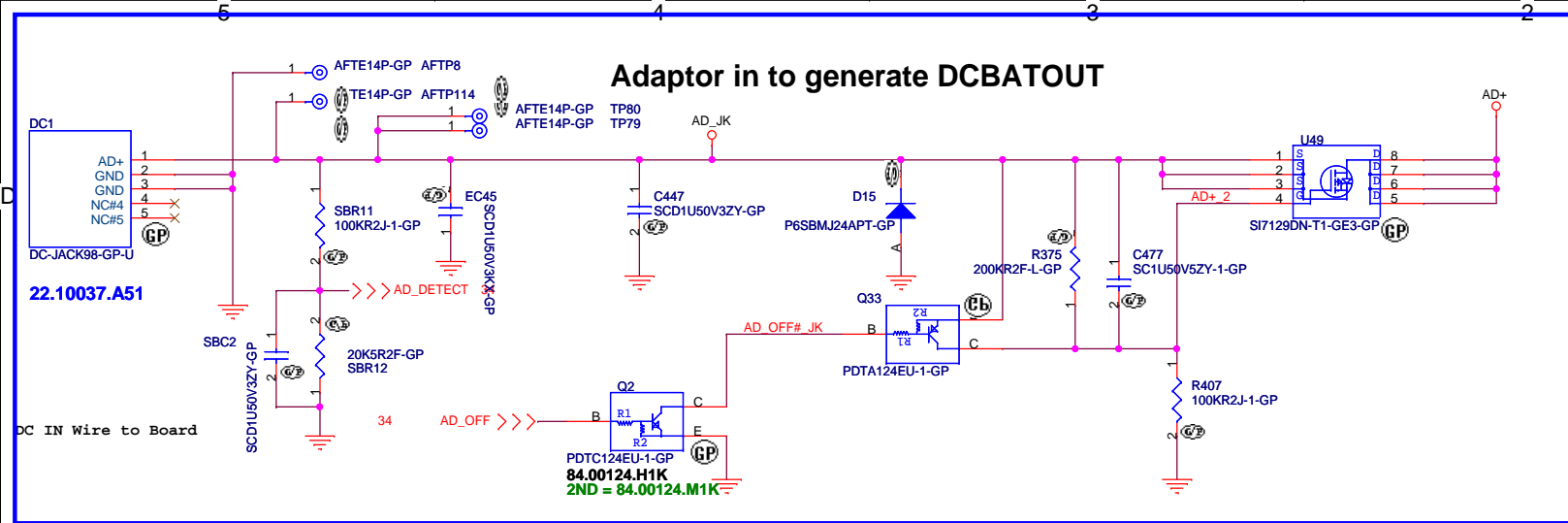
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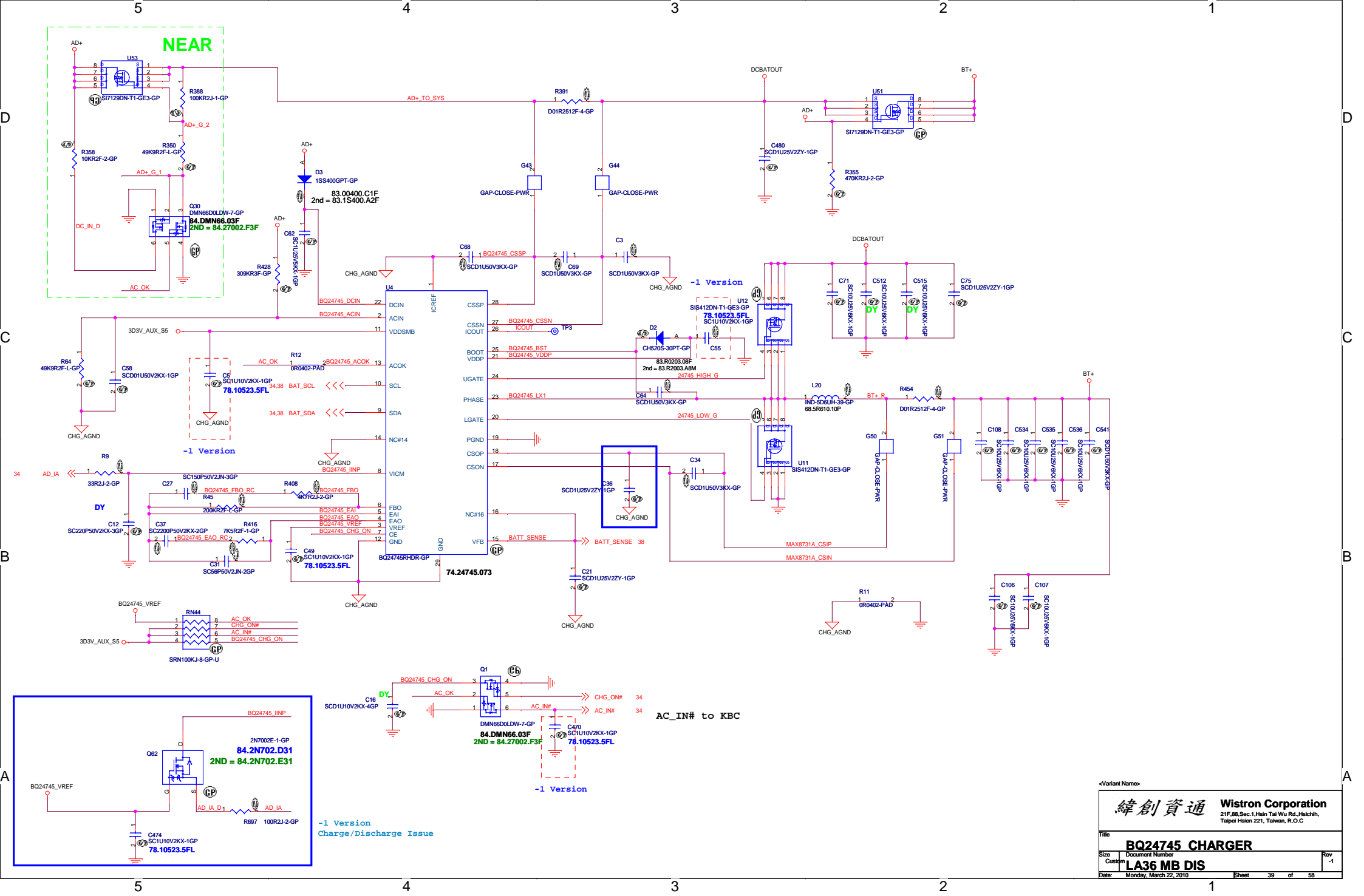
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2

1

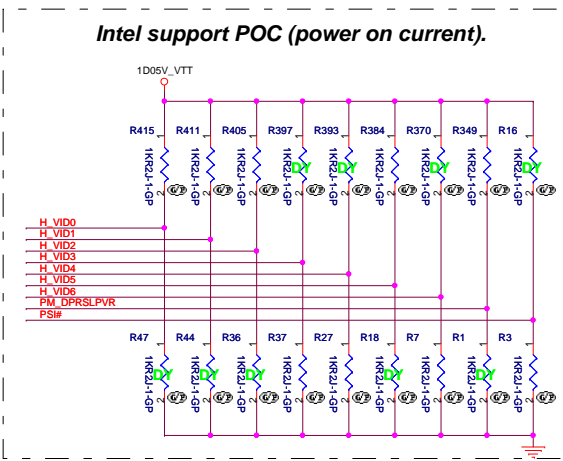
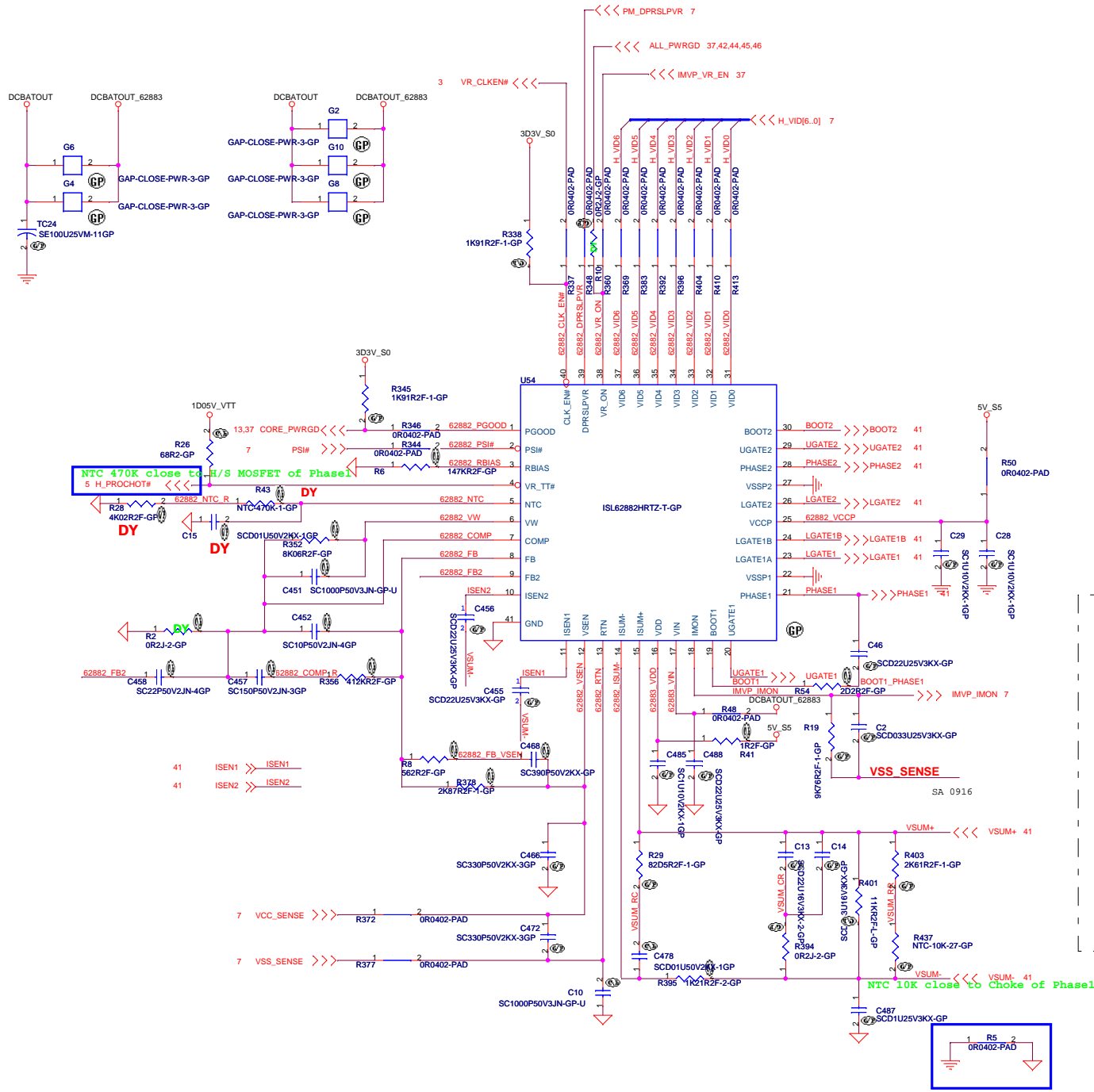


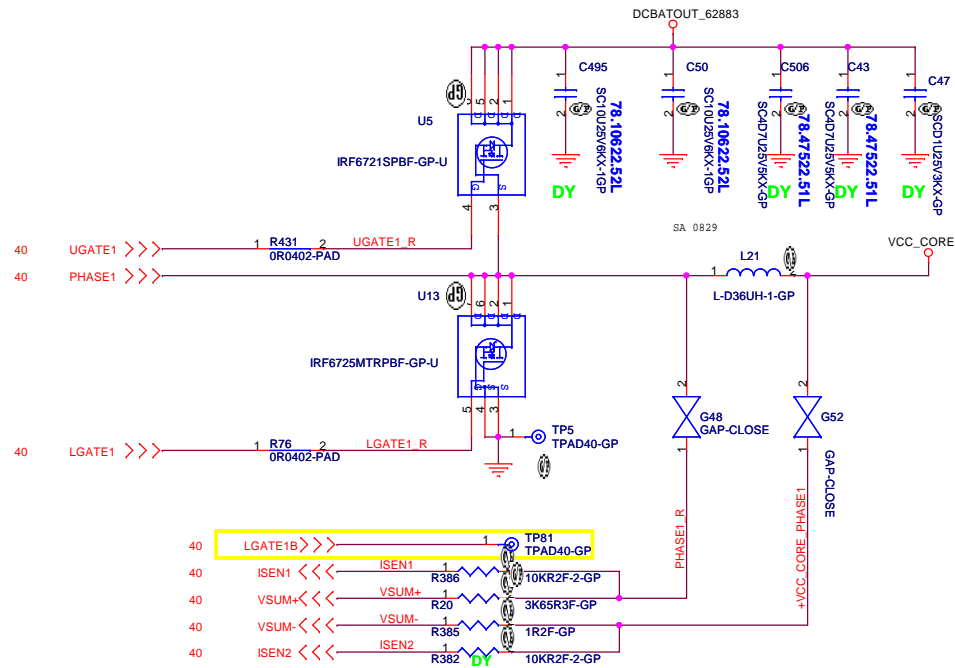
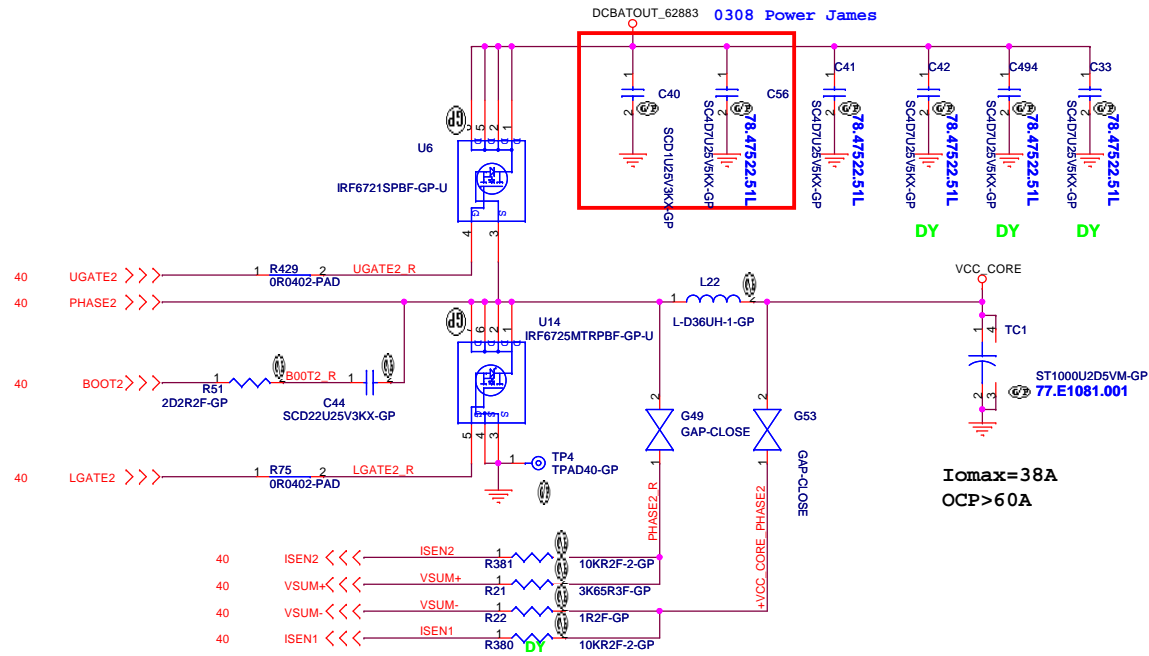




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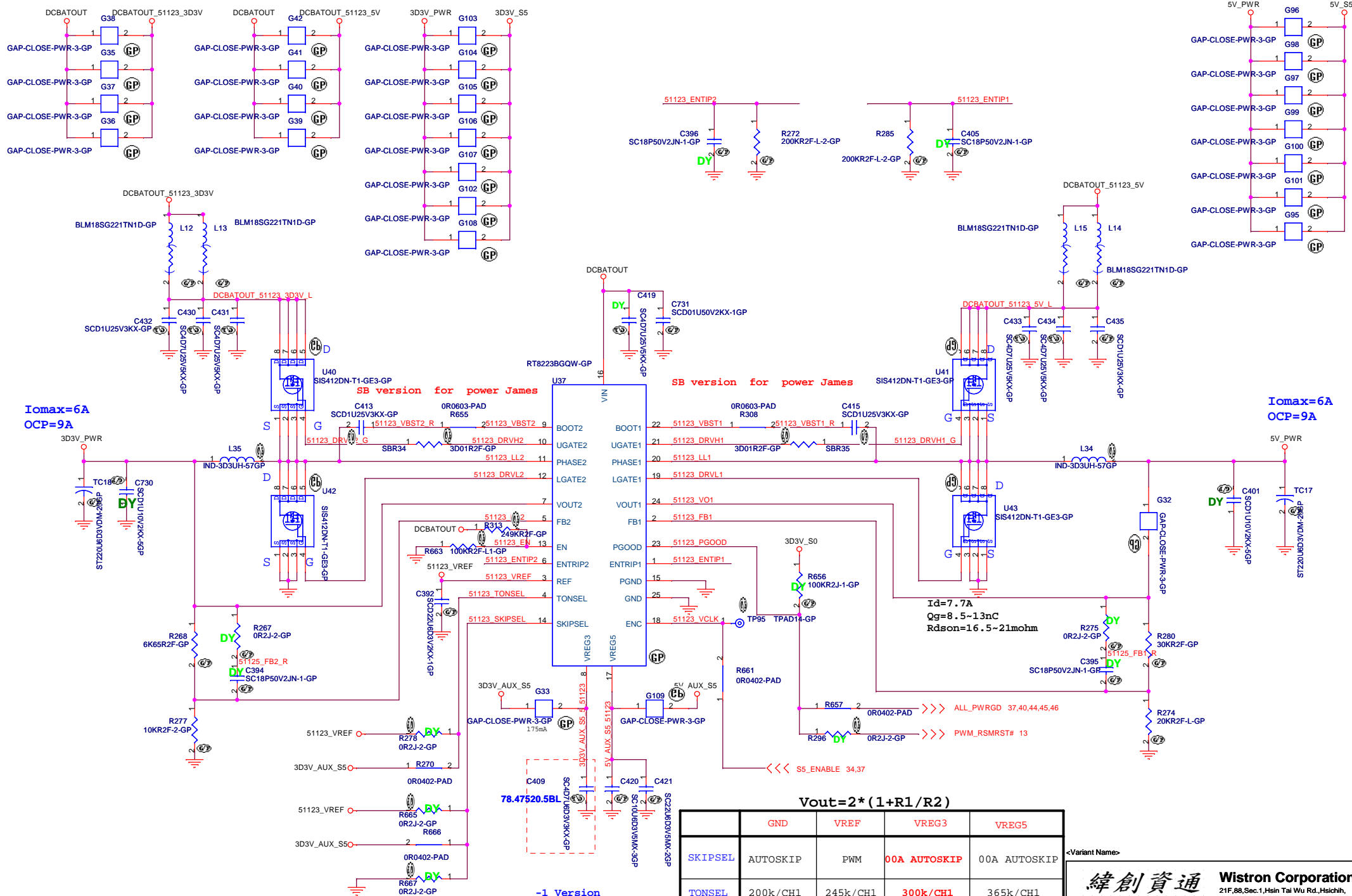
Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
BQ24745 CHARGER	
Title	Document Number
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緯創資通		Wistron Corporation	
		21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
File			
ISL62882 CPU CORE (2 of 2)			
Size			
LA36 MB DIS			
Date: Monday, March 22, 2010			
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Iomax=6A
OCP=9A

Iomax=6A
OCP=9A

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C

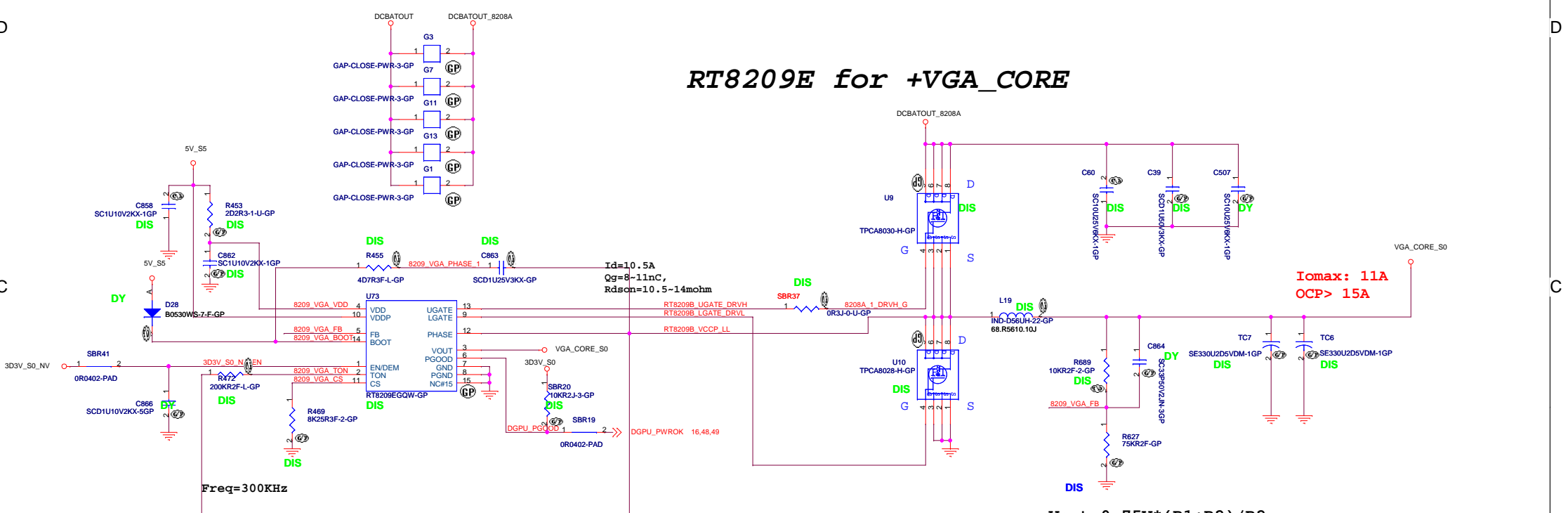
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Size: A3 Document Number: **LA36 MB DIS**

Date: Monday, March 22, 2010 Sheet: 42 of 58 Rev: -1

RT8209E for +VGA_CORE

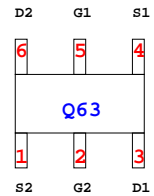
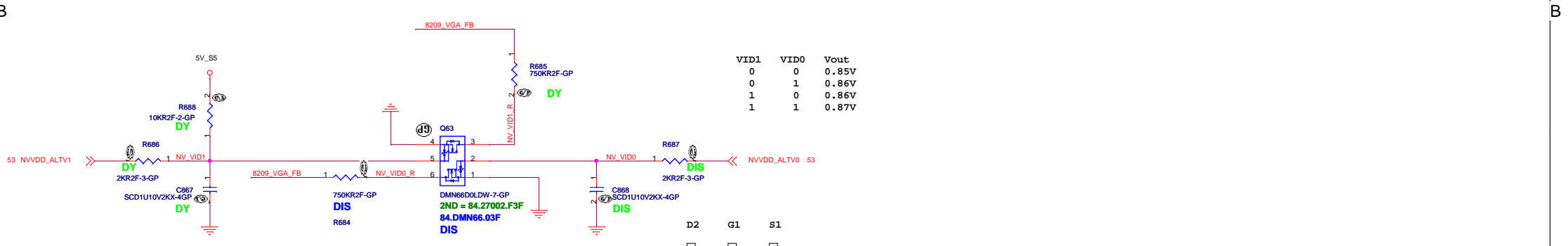
Freq=360KHz



Freq=300KHz

$$V_{out} = 0.75V * (R1 + R2) / R2$$

VID1	VID0	Vout
0	0	0.85V
0	1	0.86V
1	0	0.86V
1	1	0.87V



<Variant Name>

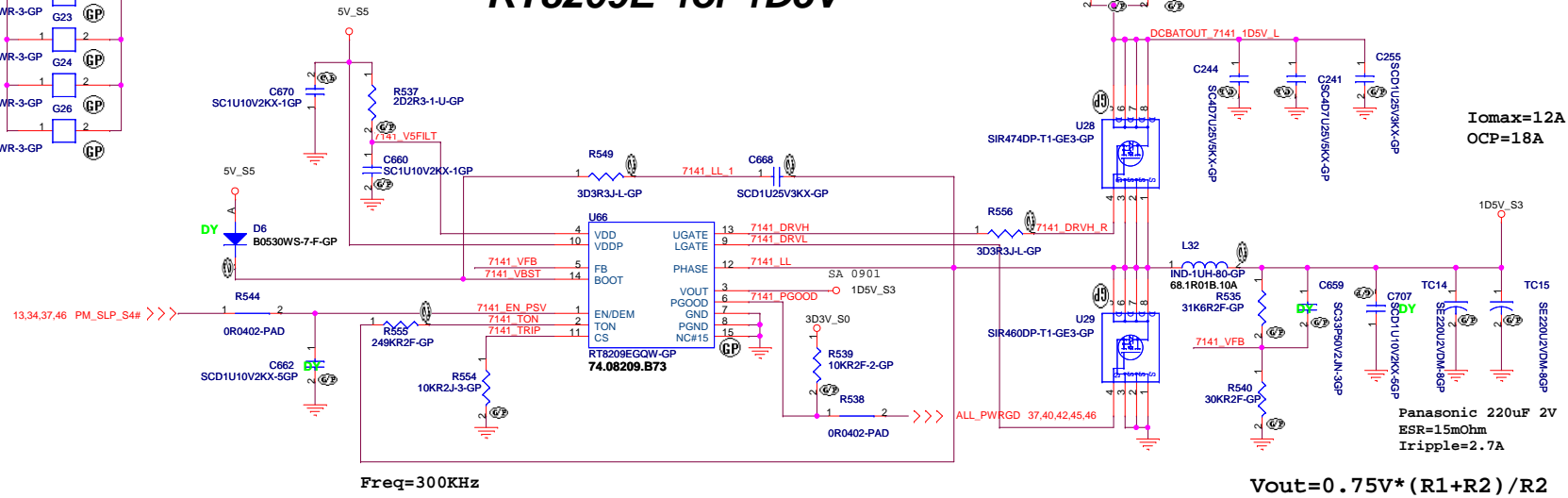
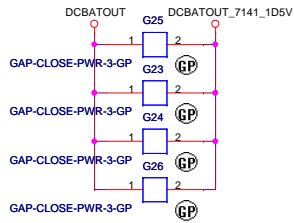
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C

Title: **RT8208A VGA CORE**

Size: Custom Document Number: **LA36 MB DIS** Rev: -1

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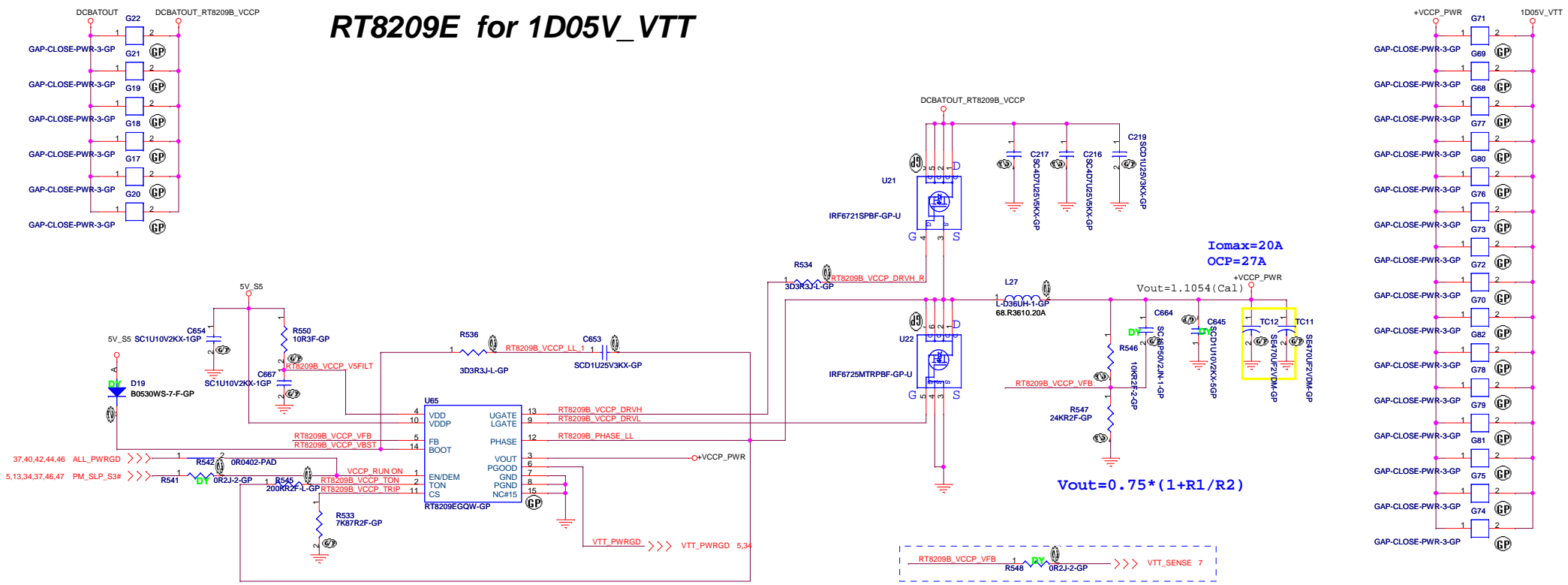
RT8209E for 1D5V



Title		RT8209E 1D5V / RT8209E 1D05V	
Size	Document Number	Customer	Rev
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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Heichih,
Taipei Hsien 221, Taiwan, R.O.C

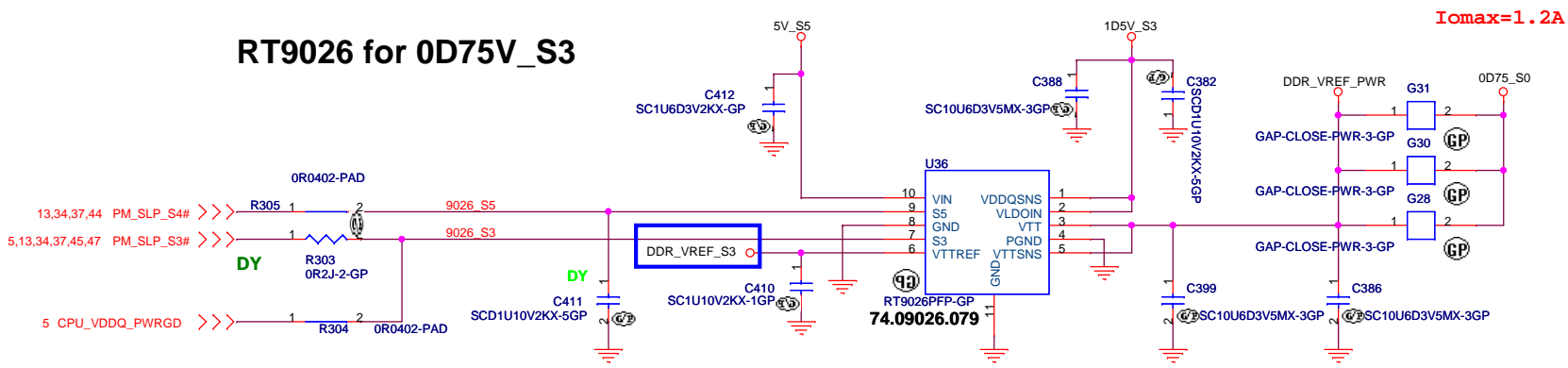
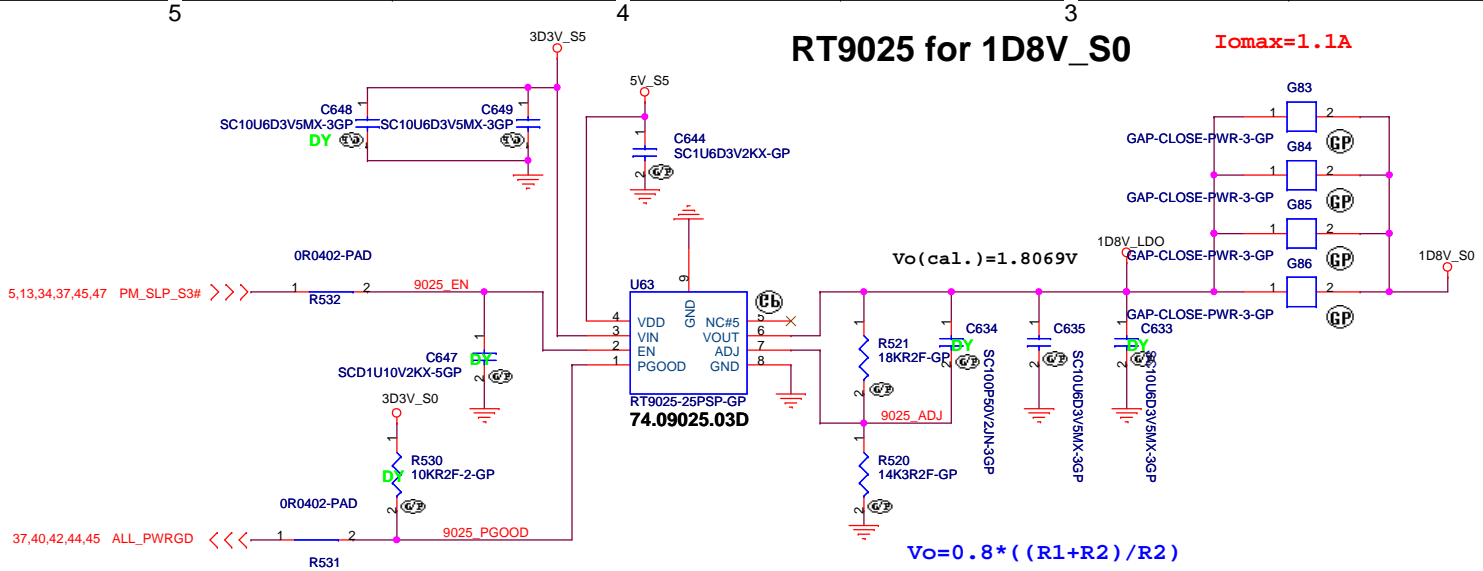
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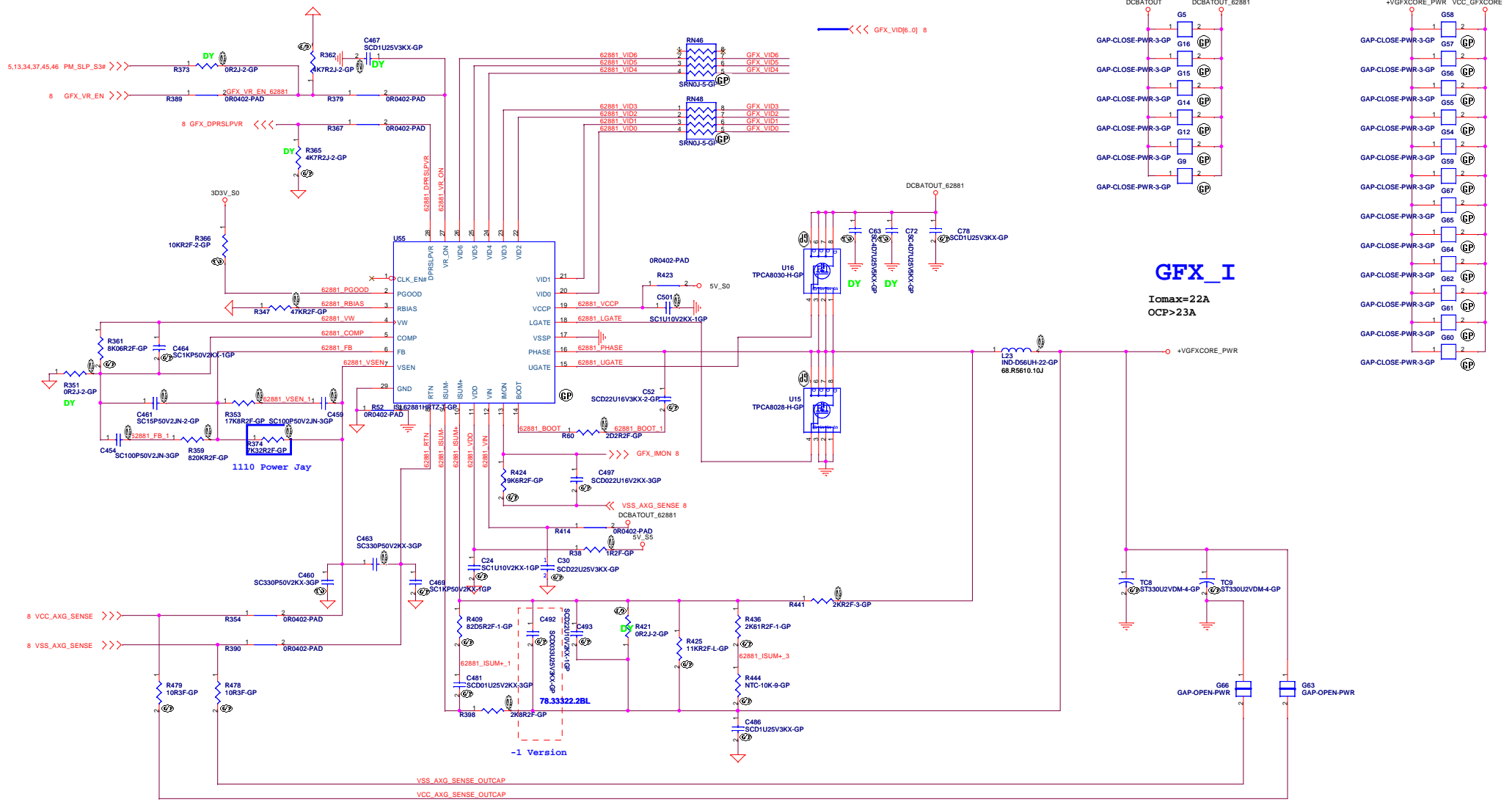
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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C

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Size	Document Number	Rev
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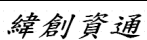


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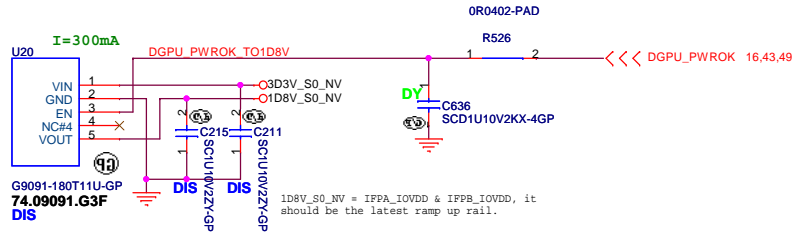
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21F.88.Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C			
RT9025 1D8V/ RT9026 0D75			
Size	Document Number	Rev	
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-<Variant Name->

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ISL62881 +VCC GFXCORE	
File	Document Number
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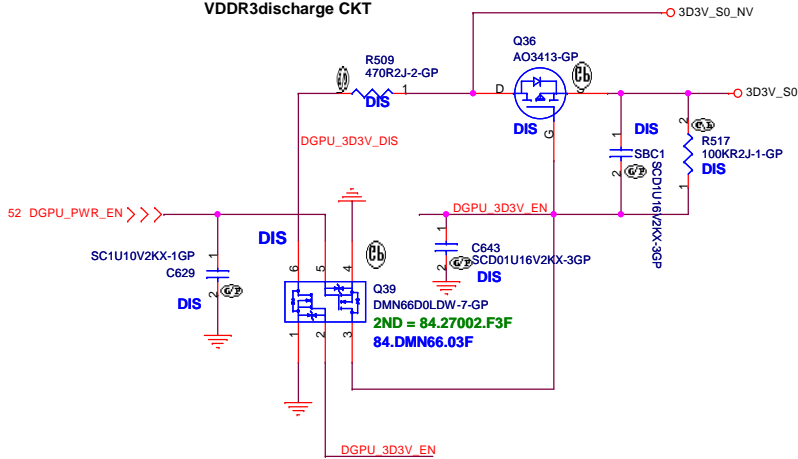
+3VS to 1.8V Transfer



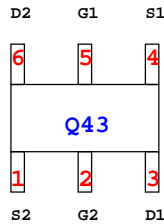
+3VS to 3.3V_DELAY Transfer

3.3v (580mA)

VDDR3discharge CKT

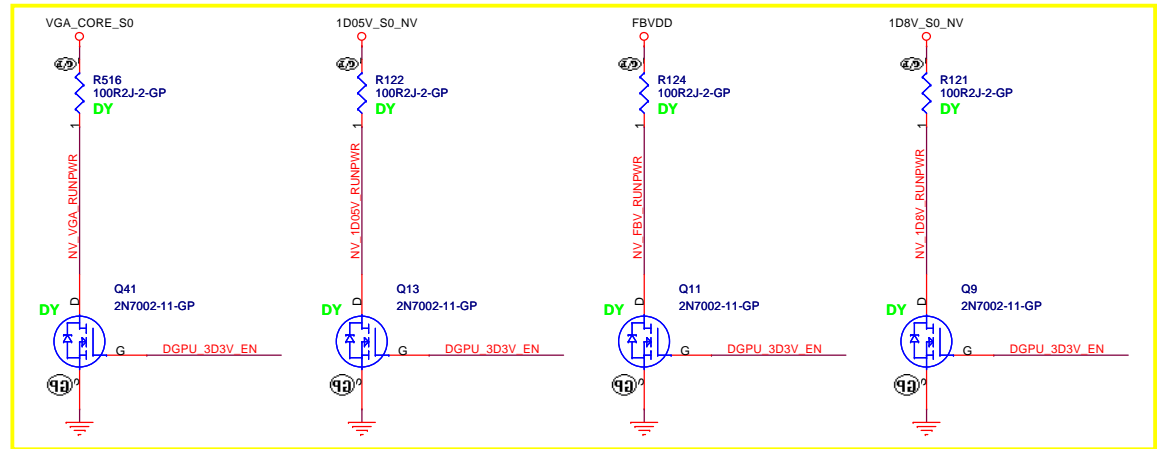
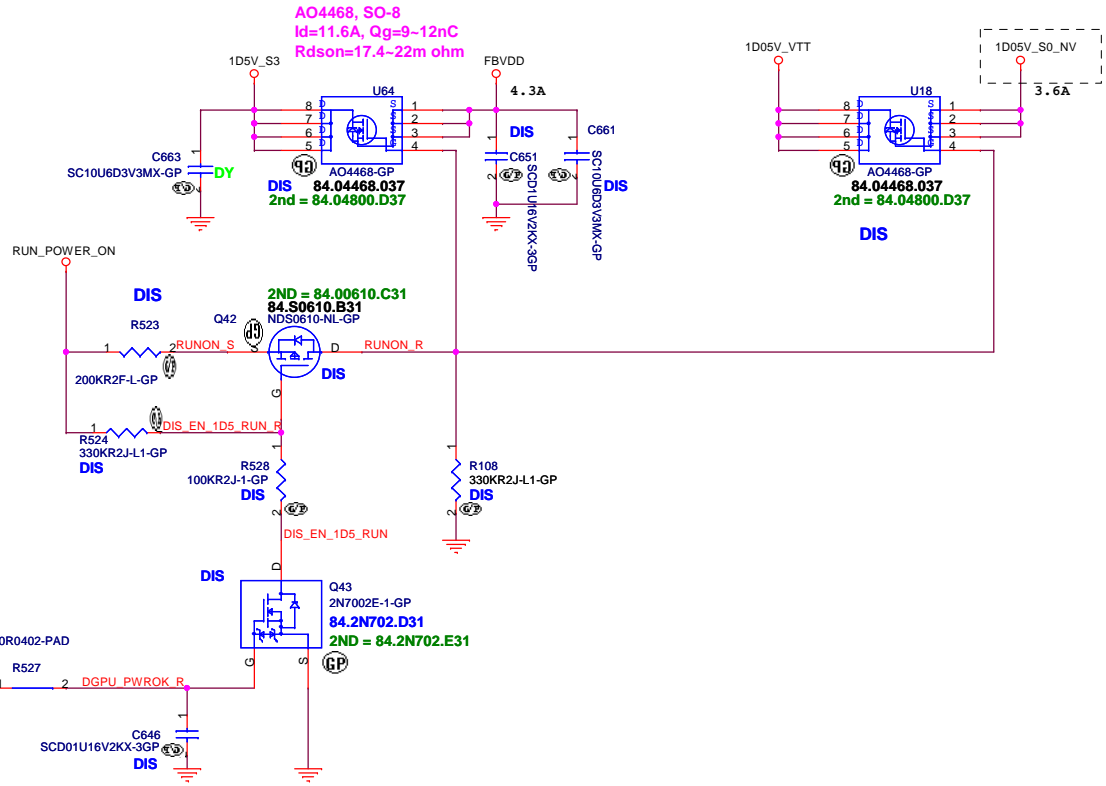


system turn on 3D3V_S0_NV --> VGA_CORE_S0
 DGPU_PWROK --> FBVDD, 1D05V_S0_NV, 1D8V_S0_NV



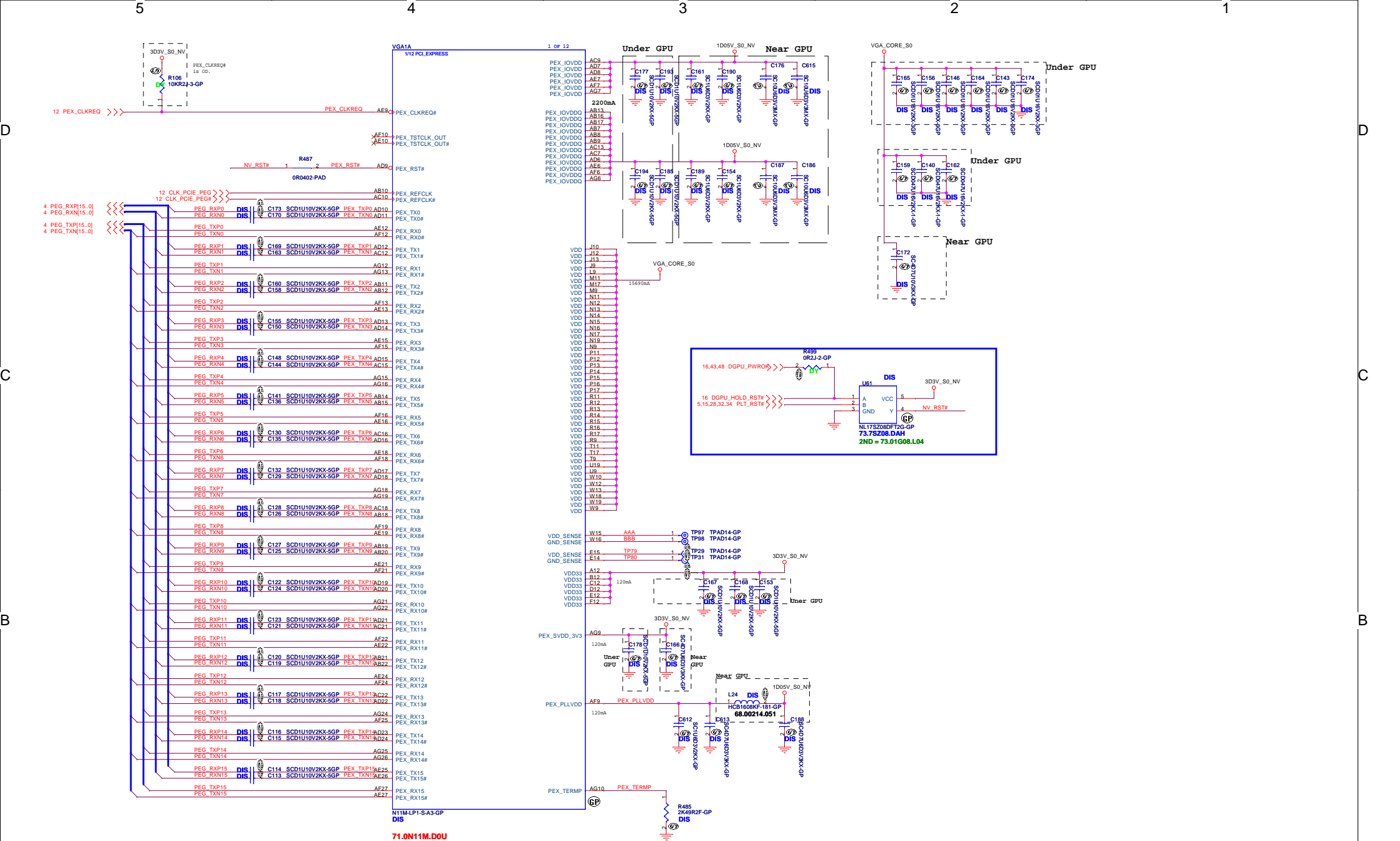
+1.5V to FBVDD Transfer

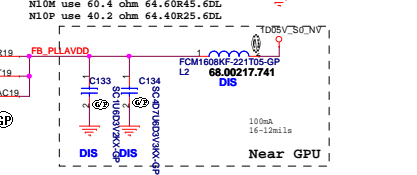
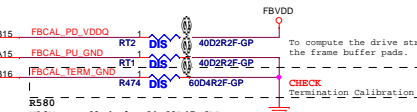
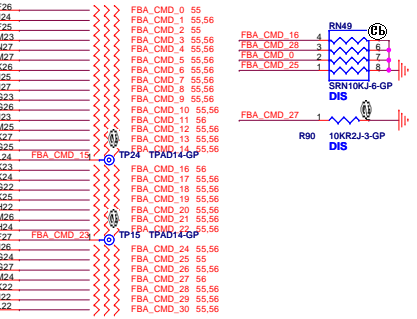
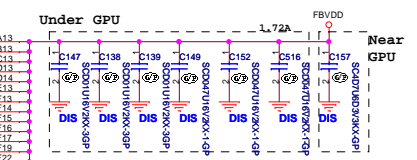
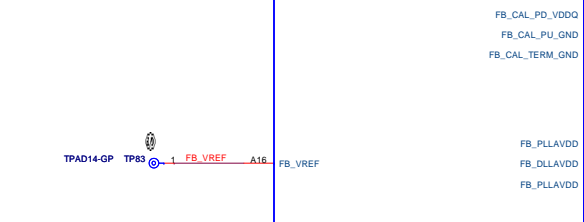
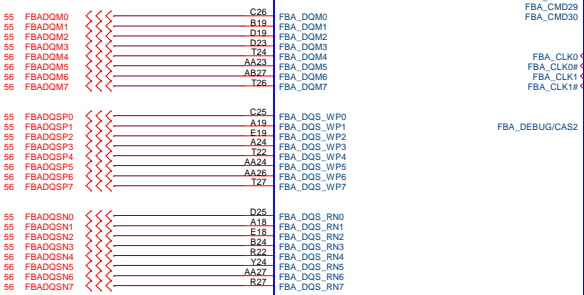
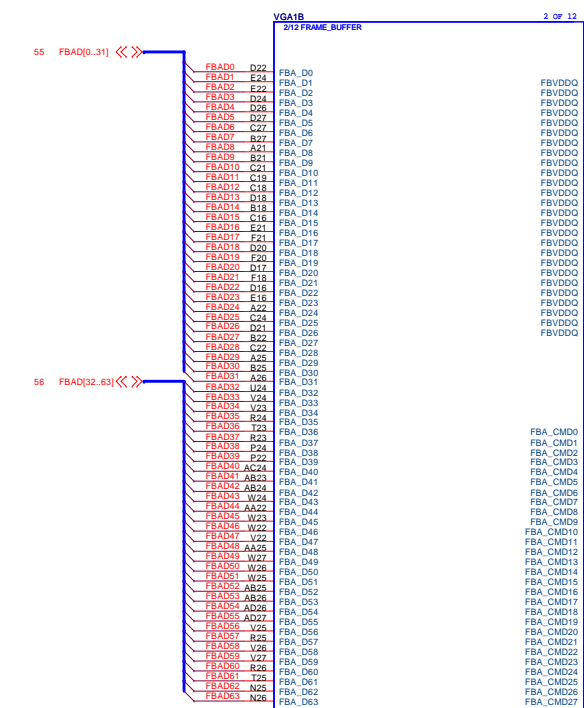
+1.05V to +1.05V_NV Transfer



<Variant Name>

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	
NV power	
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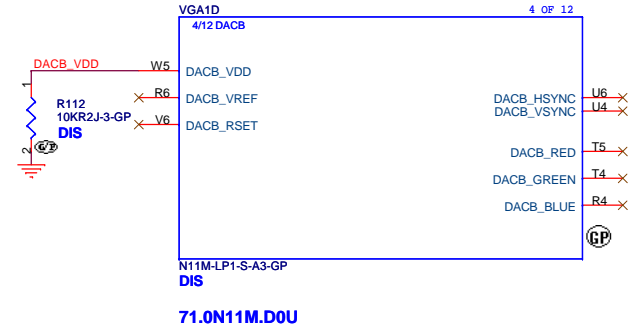
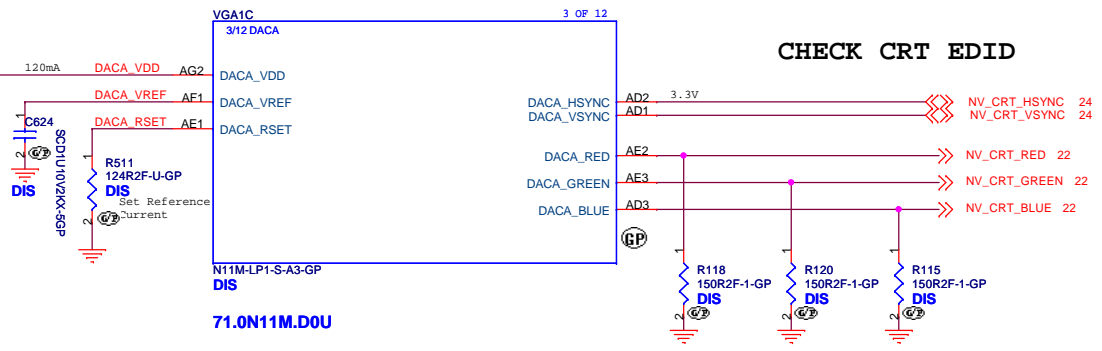
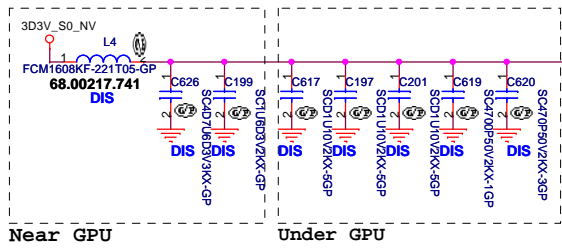


N11M-LP1-S-A3-GP
DIS

71.0N11M.D0U

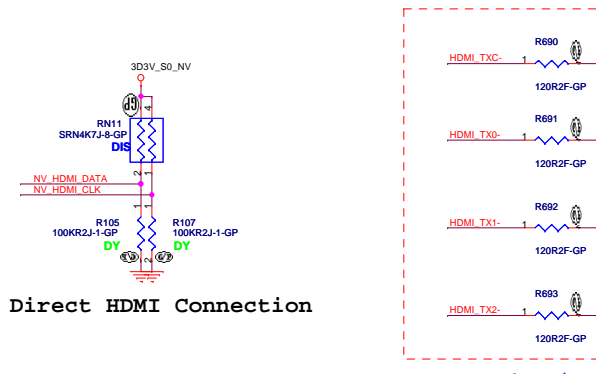
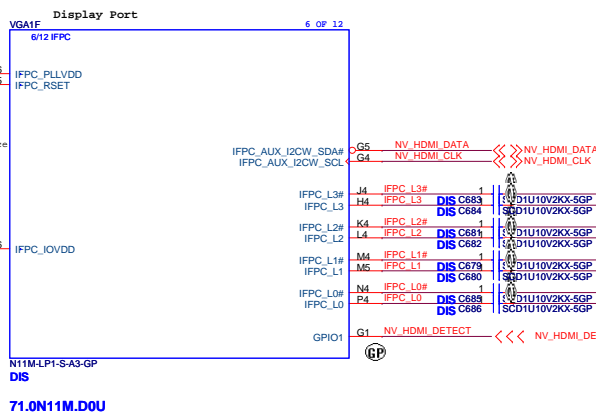
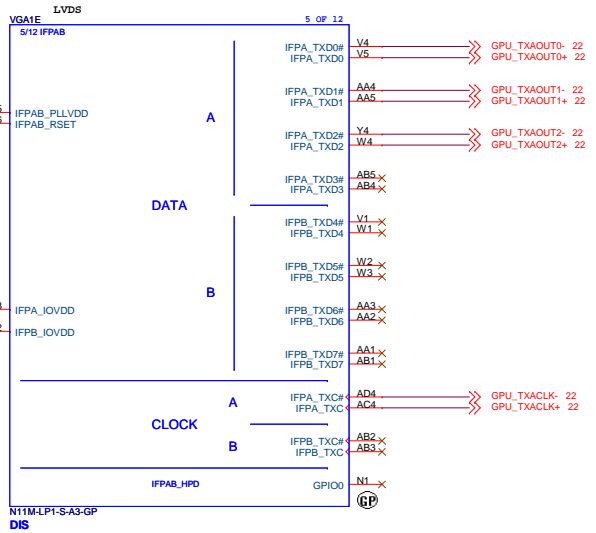
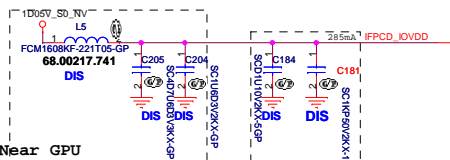
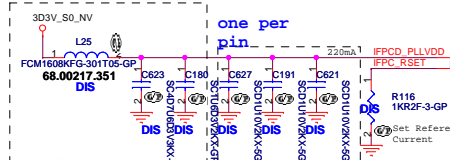
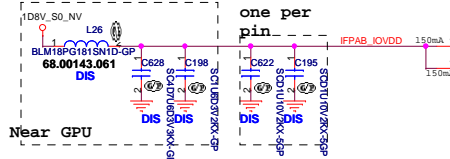
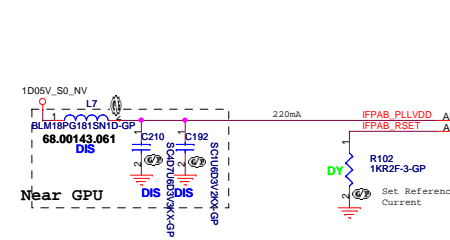
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsin 221, Taiwan, R.O.C.

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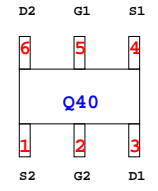
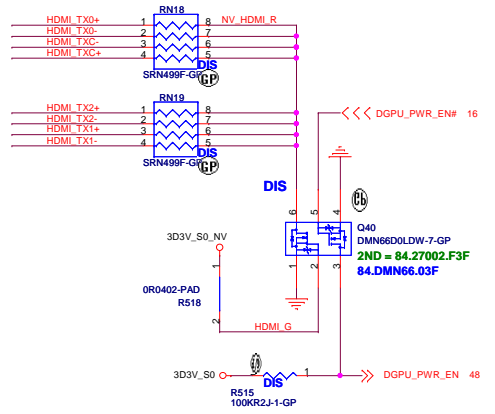
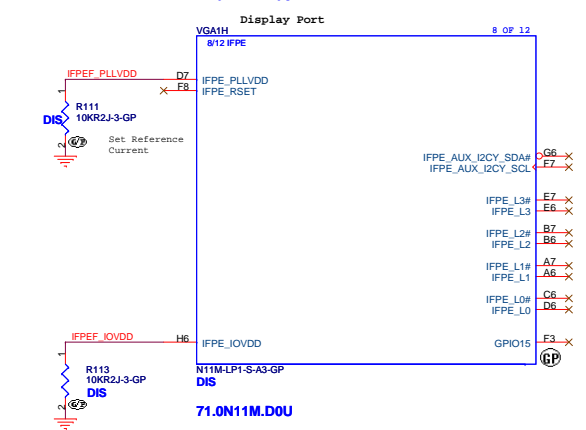
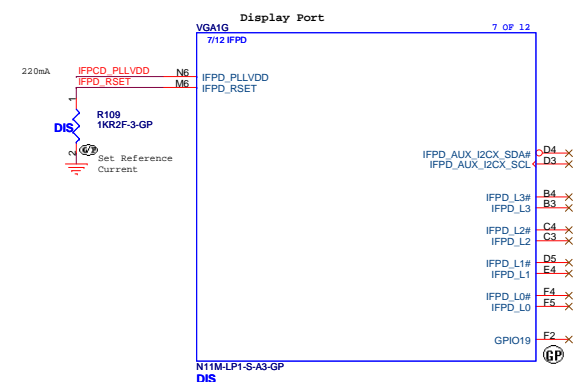
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Direct HDMI Connection

-1 version



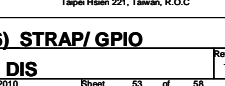
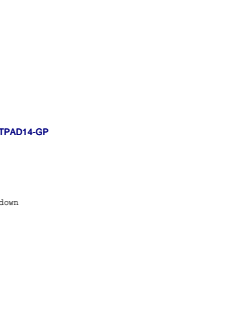
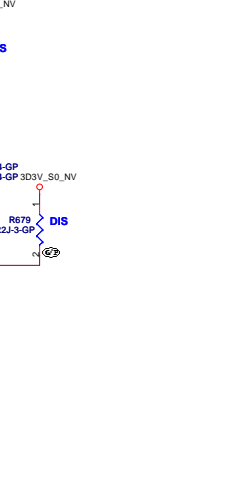
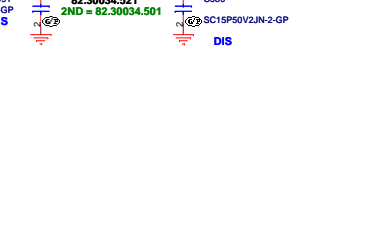
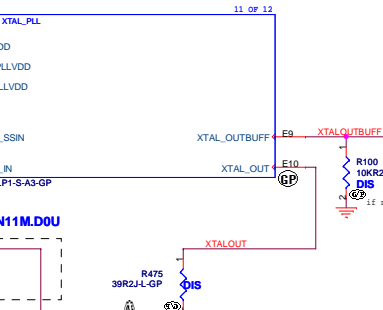
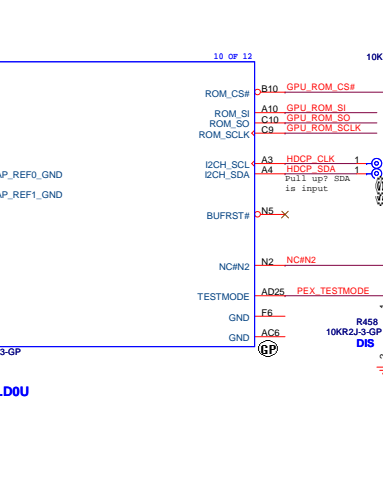
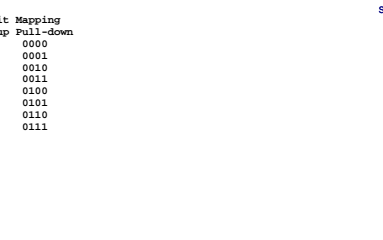
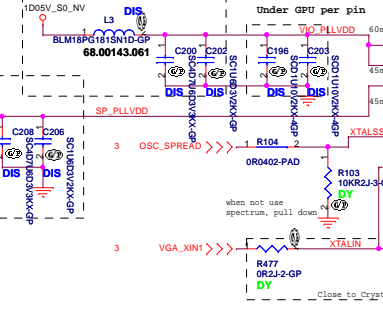
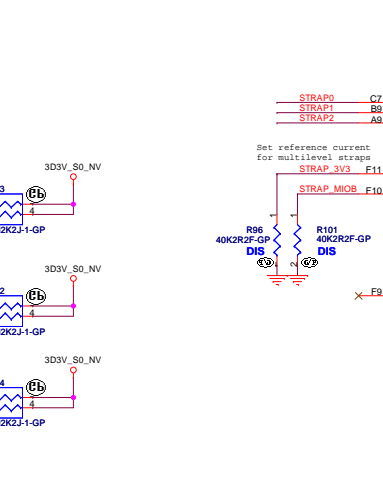
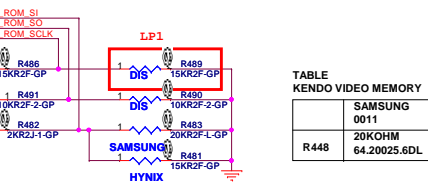
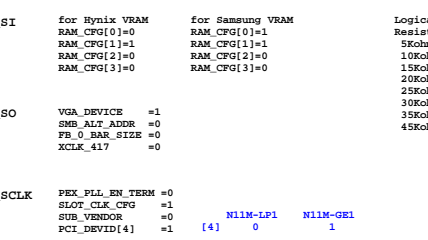
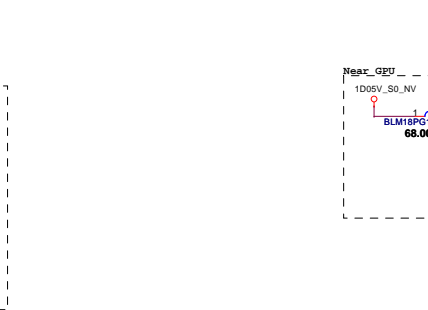
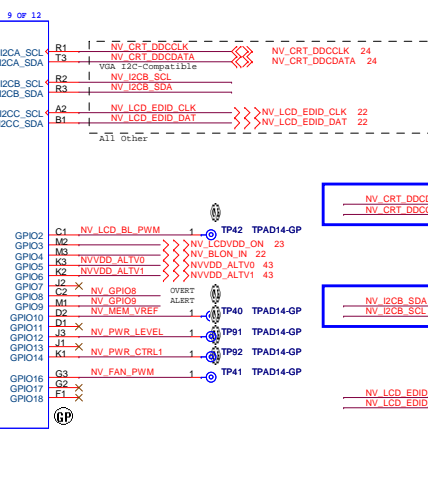
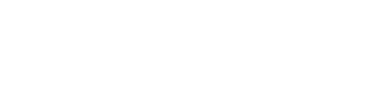
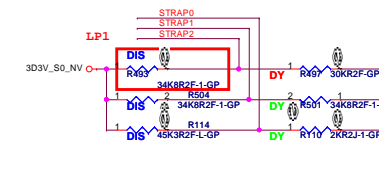
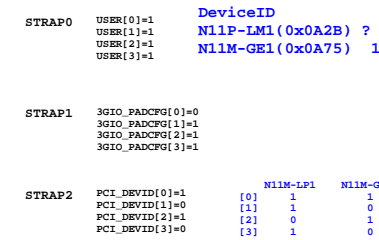
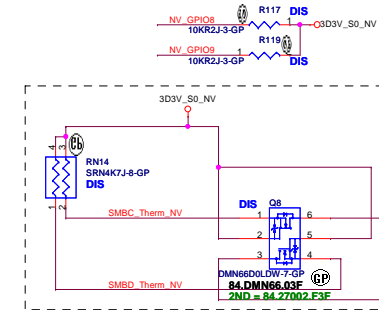
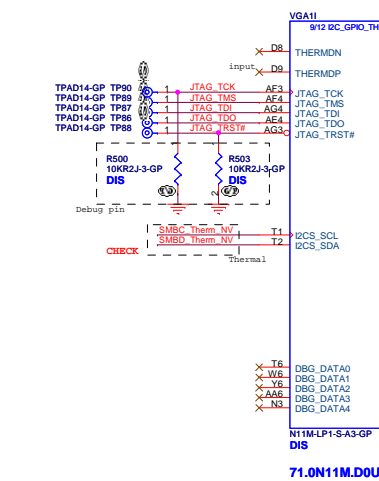
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C

File: **N11M(4/6) IFP**

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Customer: **LA36 MB DIS**

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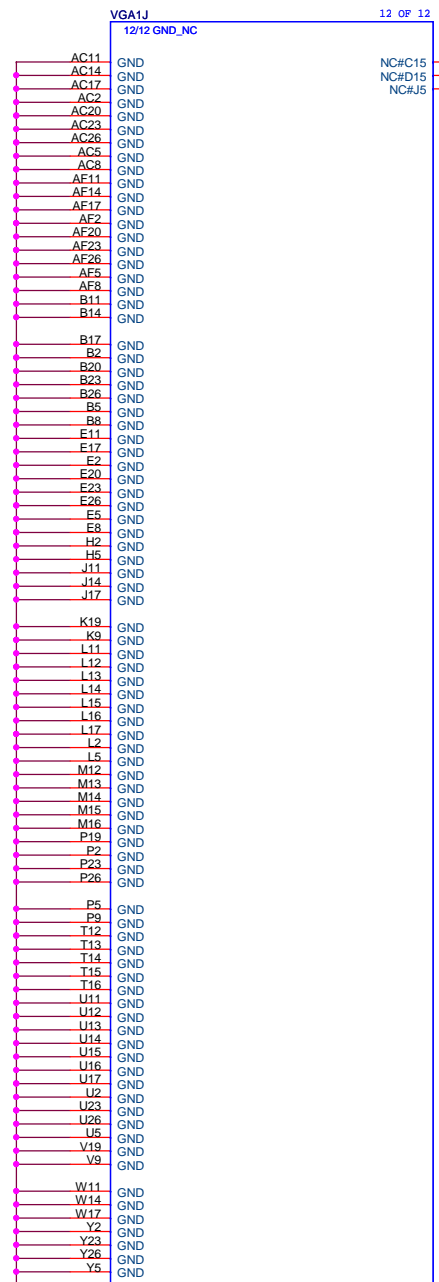
Strap	DeviceID	GPU_ROM_SI	GPU_ROM_SO	GPU_ROM_SCKL	GPU_ROM_CS#	Logical Strap Bit Mapping
STRAP0	USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1	for Hynix VRAM RAM_CFG[0]=0 RAM_CFG[1]=1 RAM_CFG[2]=0 RAM_CFG[3]=0	for Samsung VRAM RAM_CFG[0]=1 RAM_CFG[1]=1 RAM_CFG[2]=0 RAM_CFG[3]=0	VGA_DEVICE =1 SMB_ATT_ADDR =0 FB_0_BAR_SIZE =0 XCLK_417 =0	ROM_CS# A10 GPU_ROM_SI C10 GPU_ROM_SO C9 GPU_ROM_SCKL	Resistor Pull-up Pull-down 5Kohms 1000 0000 10Kohms 1001 0001 15Kohms 1010 0010 20Kohms 1011 0011 25Kohms 1100 0100 30Kohms 1101 0101 35Kohms 1110 0110 45Kohms 1111 0111
STRAP1	3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1					
STRAP2	PCI_DEVID[0]=1 PCI_DEVID[1]=0 PCI_DEVID[2]=1 PCI_DEVID[3]=0	N11M-LP1 [0] 1 1 [1] 1 0 [2] 0 1 [3] 1 0	N11M-GEL [0] 1 1 [1] 1 0 [2] 0 1 [3] 1 0	PEX_PLL_EN_TERM =0 SLOT_CLK_CFG =1 SUB_VENDOR =0 PCI_DEVID[4]=1		[4] 0 1

TABLE
KENDO VIDEO MEMORY

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64.20025.6DL	64.20025.6DL	64.15025.6DL

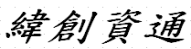
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: **N11M(5/6) STRAP/ GPIO**
Size: Document Number
Customer: **LA36 MB DIS**
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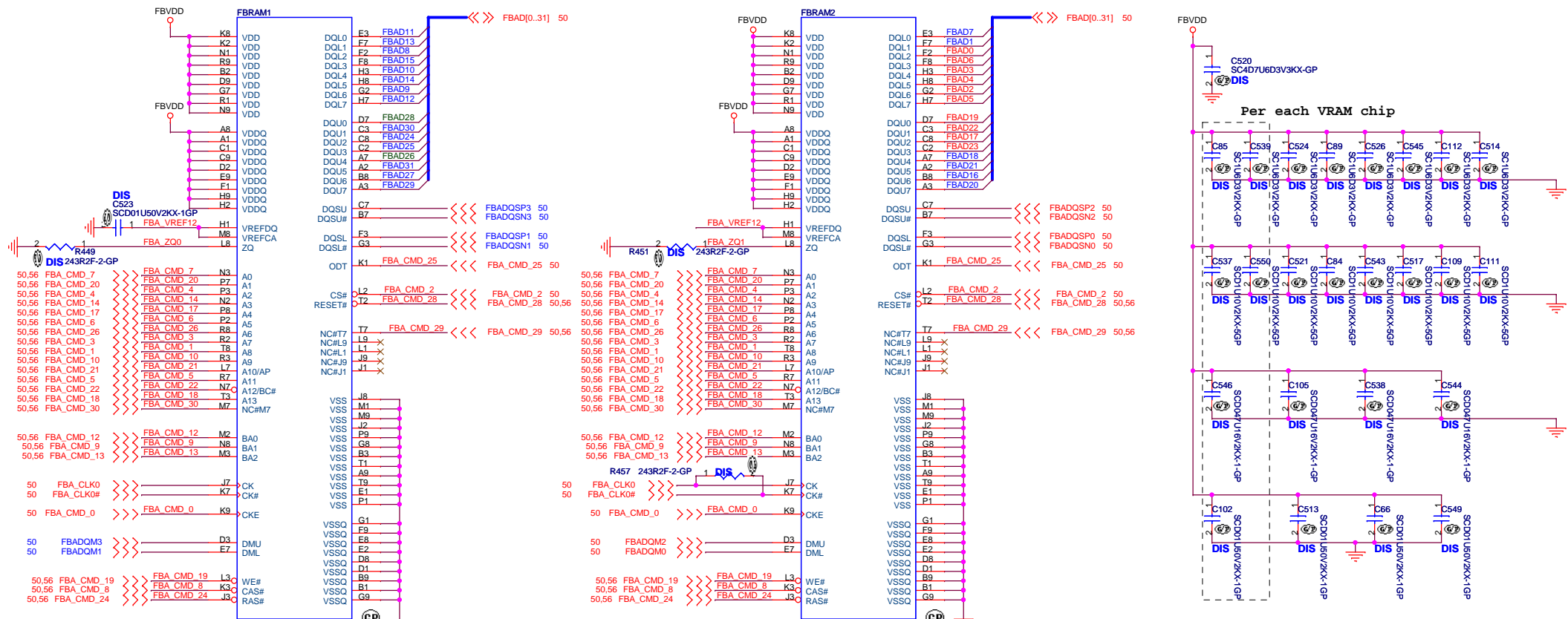


N11M-LP1-S-A3-GP
DIS
71.0N11M.D0U

<Variant Name>

 Wistron Corporation 21F, 88, Sec. 1, HeIn Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C	
File	
N11M(6/6) GND	
Size	Document Number
Customer	LA36 MB DIS
Date:	Monday, March 22, 2010
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Mode C Command Mapping



2nd: 72.51G63.C0U (IC SDRAM H5TQ1G63BFR-12C FBGA)

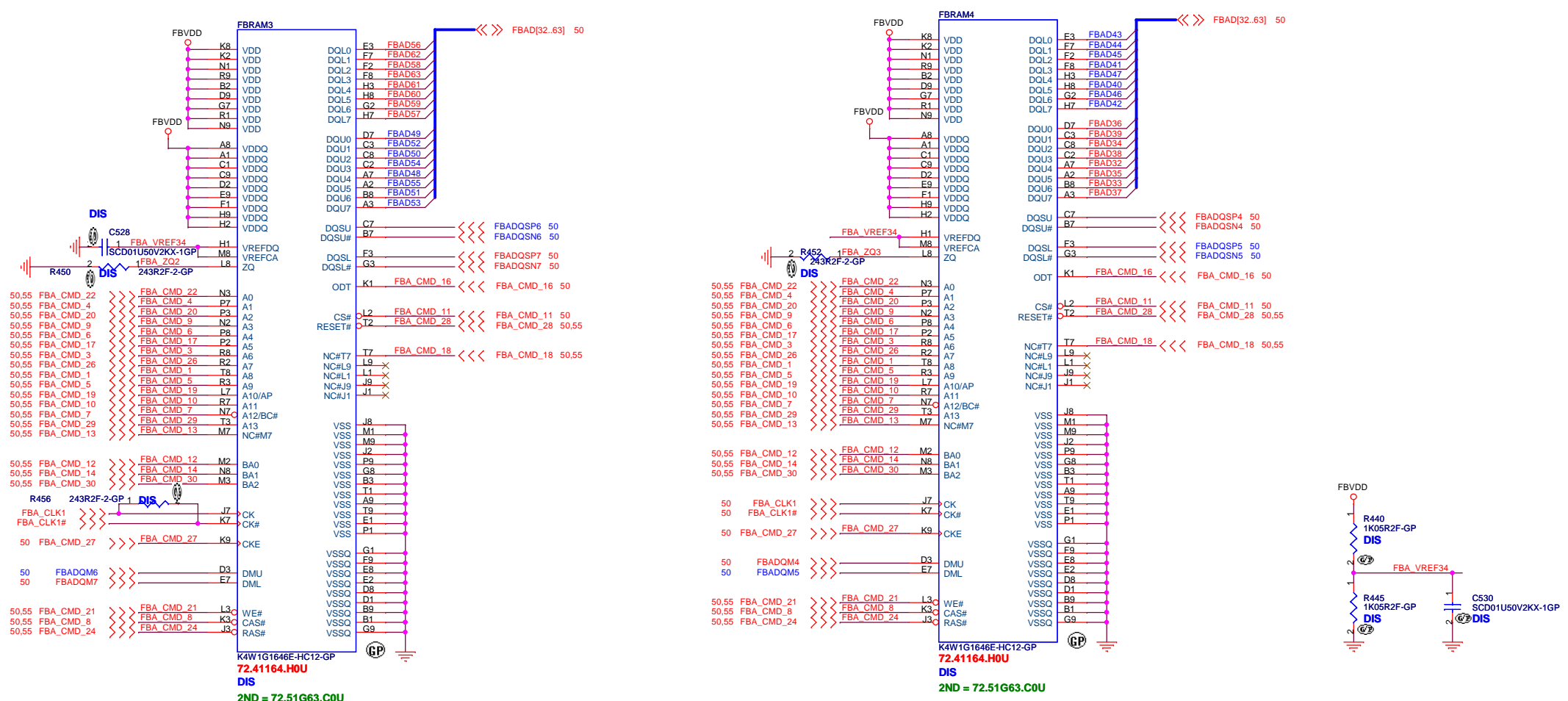
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C

Title: **VRAM(1/2)**

Size: Custom Document Number: **LA36 MB DIS** Rev: -1

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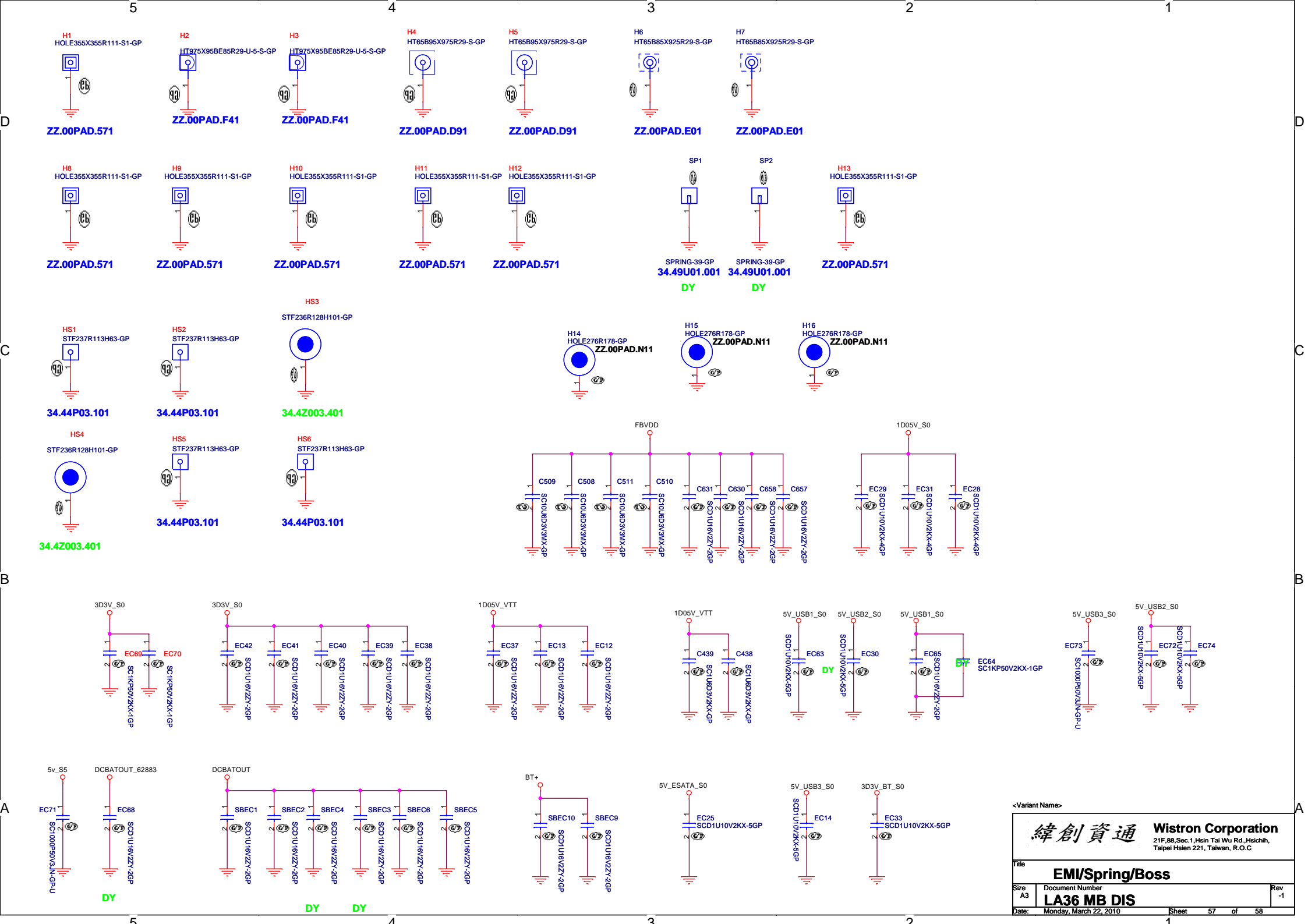
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緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

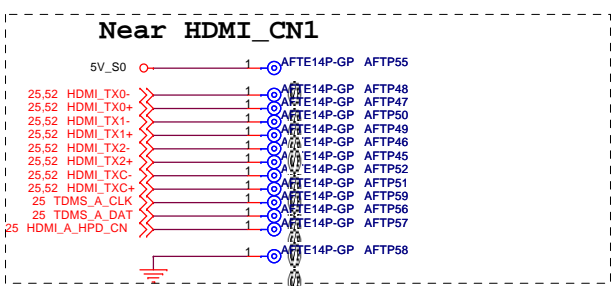
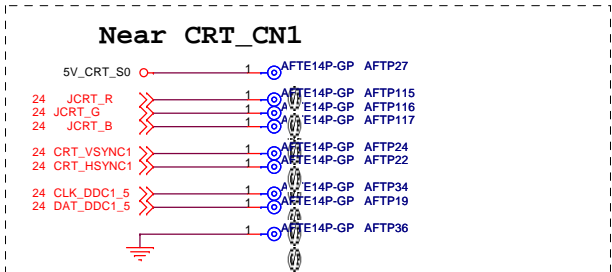
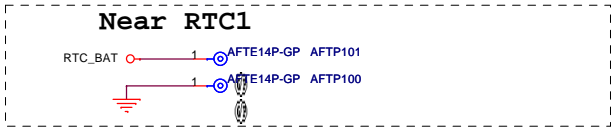
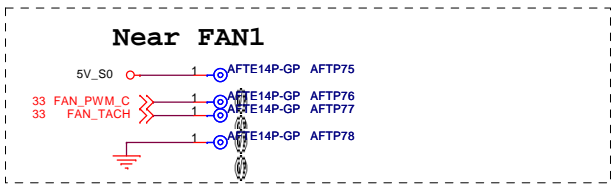
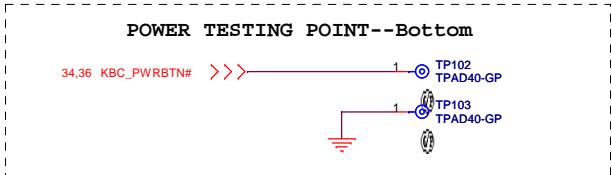
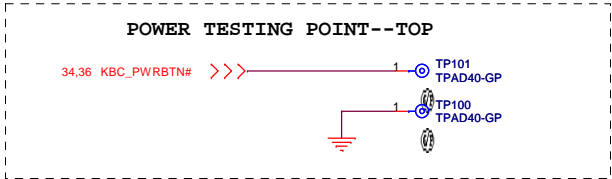
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