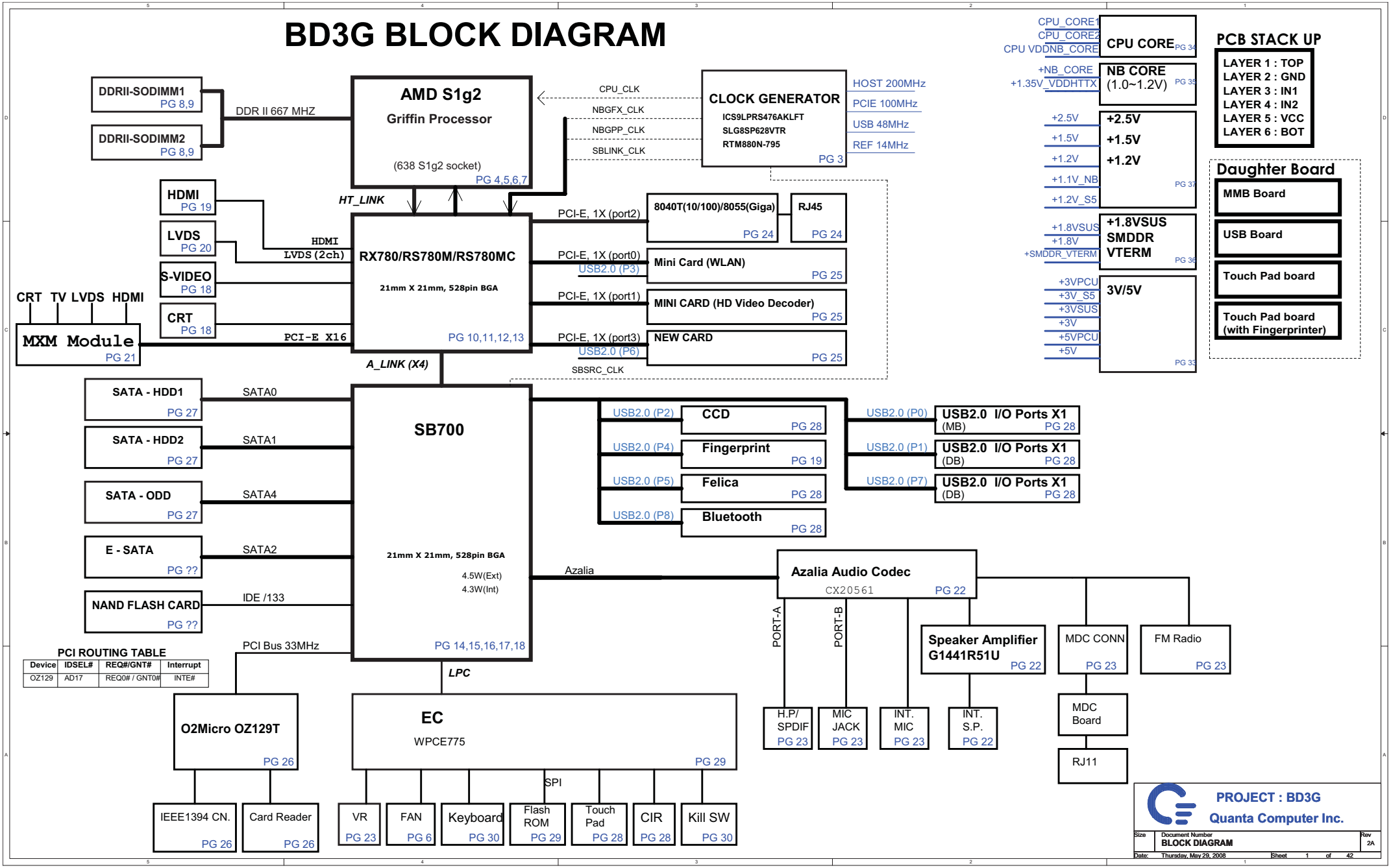
BD3G BLOCK DIAGRAM



PCI ROUTING TABLE

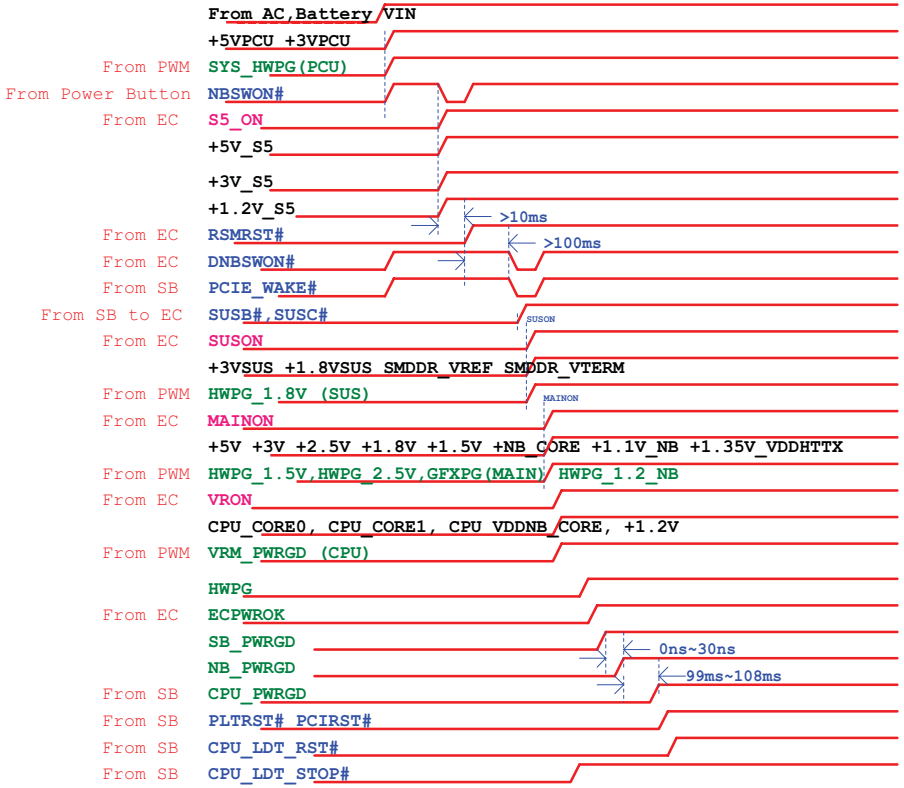
Device	IDSEL#	REQ#/GNT#	Interrupt
OZ129	AD17	REQ0# / GNT0#	INTE#

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	2A

Date: Thursday, May 29, 2008 Sheet 1 of 42

BD3G Power On Sequence



BOM naming rule

Items	Function	BTO	Name	Description
1	CIR	v	CIR@	
2	HDMI port	v	HDM@	
3	HDMI transmitter	v	SI@	Silicon image SiI 1392/1932
4	HDMI-CEC	v	CEC@	Renesas R8C/1B
5	Discrete VGA		EV@	External VGA stuff
6	UMA		IV@	Internal VGA stuff
7	New Card		NEW@	
8	RJ11	v	MD@	Modem
9	RJ45-10/100		40@	Marvell 8040T(10/100)
10	RJ45-1000		55@	Marvell 8055(Giga)
11	Option for RJ45-10/100 and RJ45-1000		40@55@	Option for 8040/8055
12	TV	v	TV@	
13	Cardbus		CB@	
14	FM transmitter	v	FM@	
15	Mainstream ID LED		MID@	
16	Low cost ID LED		LID@	
17	CCD	v	CCD@	
18	INT MIC	v	I_MIC@	
19	AMD Hyper Flash		HF@	Only for AMD platform
20	North bridge(690MC/RS780MC)		MC@	Only for AMD platform
21	North bridge(RX780)		RX@	Only for AMD platform
22	PowerXpress		PX@	Only for AMD platform
23	PowerXpress with UMA SKU		PX@IV@	Only for AMD platform
24	PowerXpress with Discrete VGA SKU		PX@EV@	Only for AMD platform
25	Power player/Power Shift		PP@	Only for AMD platform

*Note: EC will sampling SUSB# & SUSC# every 5ms.

AMD SB700 SMBUS Table

	CLK GEN	RAM	Mini Card (HD-Decoder)	Mini-card(WL)	New Card	HDMI
SB700 SDATA0/SCLK0(+3V)	V	V	V	V	V	
SB700 SDATA1/SCLK1(+3V_S5)						V
SB700 SDATA2/SCLK2(+3V_S5)						
Power	+3V	+3V	+3V	+3V (Atheros)	+3V	+3V_S5
Reserve MOS ckt	V	V	V	V	V	V

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM	VGA thermal Sensor	Touch Sensor	HDMI CEC
EC775 SDATA1/SCLK1(+3VPCU)	V					
EC775 SDATA2/SCLK2(+3VPCU)		V	V			
EC775 SDATA3/SCLK3(+3VPCU)				V	V	V
EC775 SDATA4/SCLK4(+3VPCU)						
Power	+3VPCU	+3V	+3VPCU	+3V	+3VPCU	+5VPCU
Reserve MOS ckt	X	V	X	V	X	V

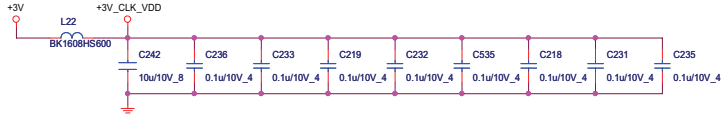
PROJECT : BD3G
Quanta Computer Inc.

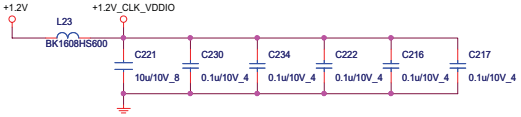
Size | Document Number: SYSTEM INFORMATION | Rev: 2A

Date: Thursday, May 29, 2008 | Sheet 2 of 42

CLK_GEN_SLG8SP628

03





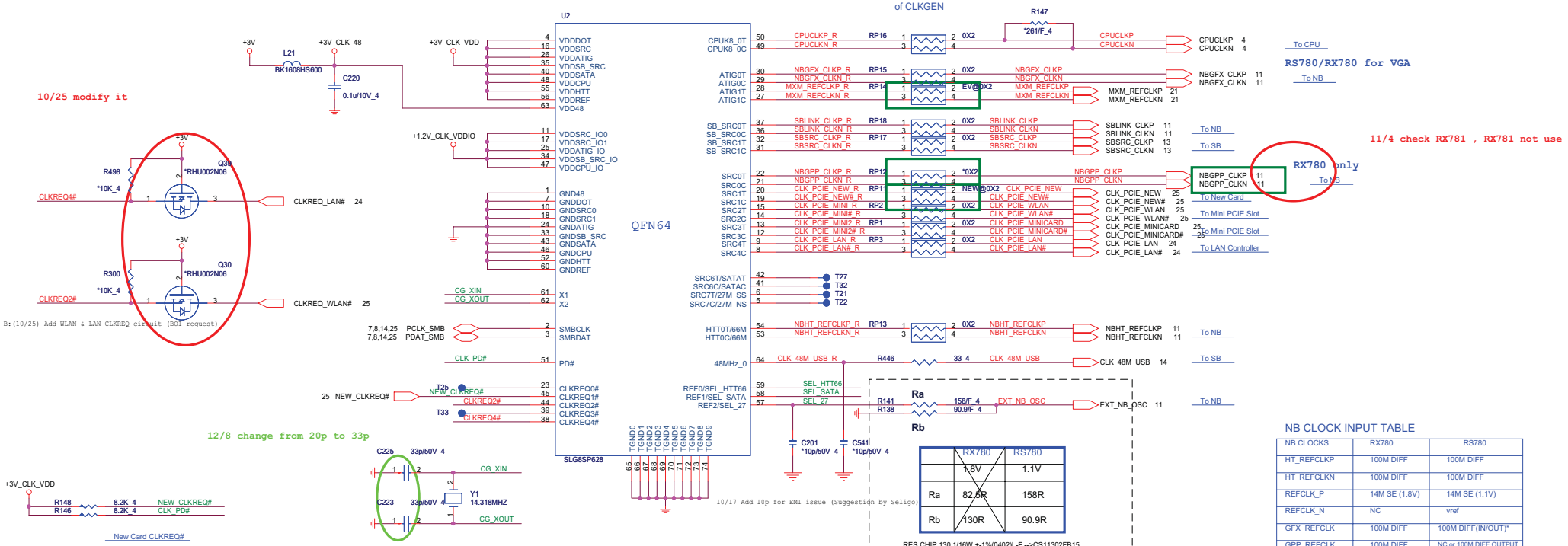
ICS9LPRS480 P/N : ALPRS480000

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN

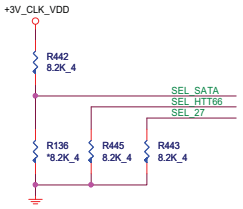


	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP1001 STUFF	RP1001 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP1005 STUFF	RP1005 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP1003 STUFF	RP1003 STUFF	to NB for AC-LINK reference clock



SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR_SLG8SP628	1A

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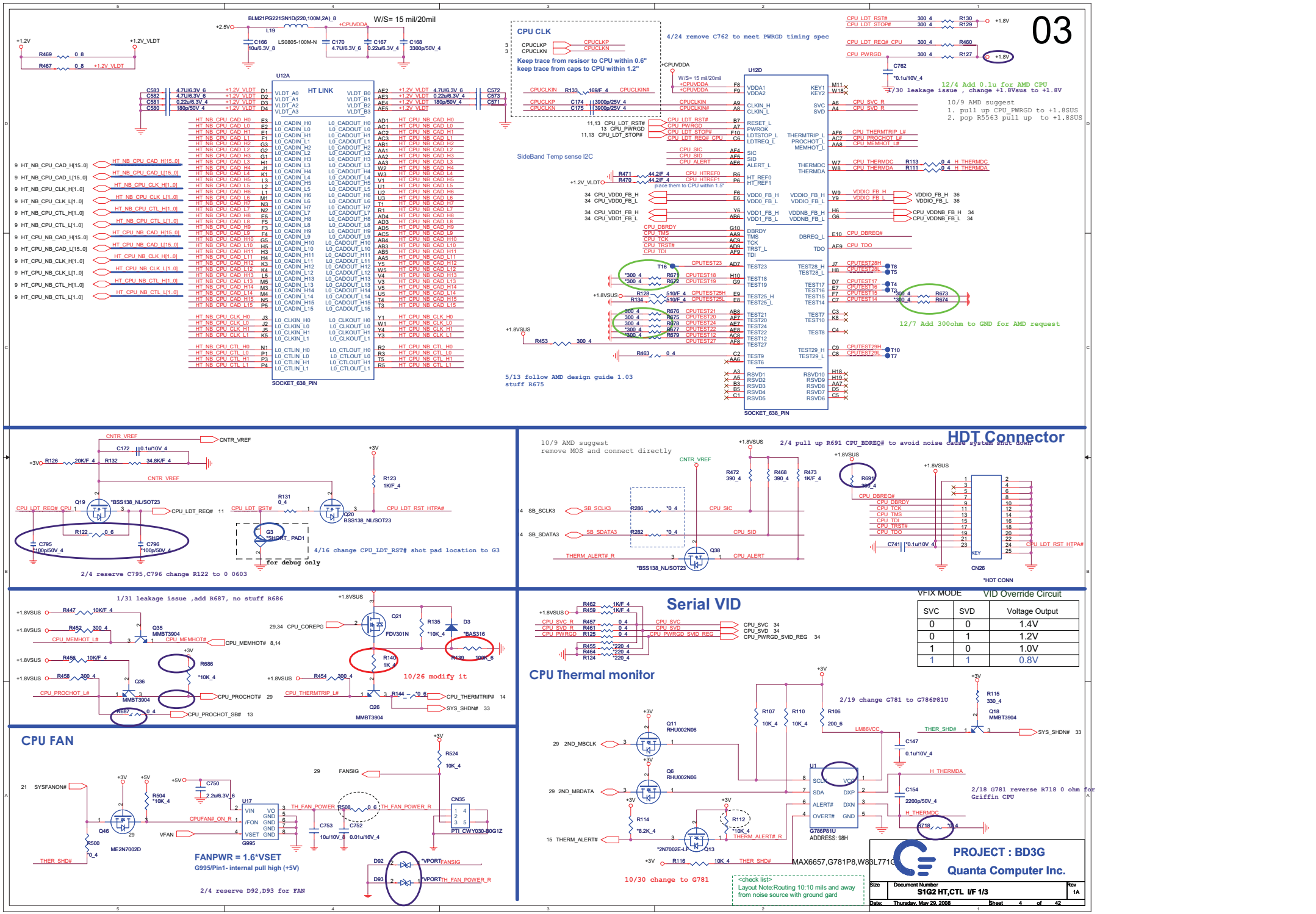

03
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
4/24 remove C762 to meet PWRGD timing spec
12/4 Add 0.1u for AMD CPU
1/30 leakage issue , change +1.8Vsus to +1.8V
10/9 AMD suggest
1. pull up CPU_PWRGD to +1.8SUS
2. pop R5563 pull up to +1.8SUS
SideBand Temp sense I2C
5/13 follow AMD design guide 1.03
stuff R675
12/7 Add 300ohm to GND for AMD request
HT HUB
SOCKET_638_PIN
HDT Connector
10/9 AMD suggest
remove MOS and connect directly
2/4 pull up R691 CPU_BDREQ# to avoid noise cause system shut down
2/4 reserve C795,C796 change R122 to 0 0603
4/16 change CPU_LDT_RST# shot pad location to G3
for debug only
1/31 leakage issue ,add R687, no stuff R686
10/26 modify it
Serial VID
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.4V
0 1 1.2V
1 0 1.0V
1 1 0.8V
CPU Thermal monitor
2/19 change G781 to G786P81U
2/18 G781 reverse R718 0 ohm for Griffin CPU
10/30 change to G781
MAX6657,G781P8,W83L771G
CPU FAN
FANPWR = 1.6*VSET
G995/Pin1- internal pull high (+5V)
2/4 reserve D92,D93 for FAN
PROJECT : BD3G
Quanta Computer Inc.
S1G2 HT,CTL I/F 1/3
Thursday, May 29, 2008
Sheet 4 of 42

Processor Memory Interface

04

PLACE THEM CLOSE TO CPU WITHIN 1"

750 mA

11/05 change to RC0402-C

Place close to socket

Close to CPU within 1500 mils

U12B

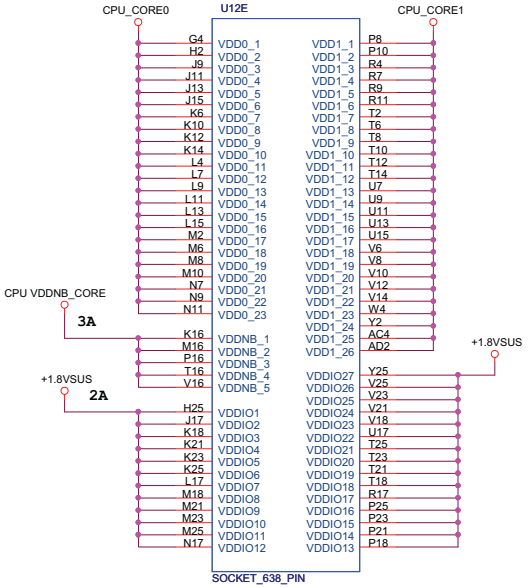
SOCKET_638_PIN

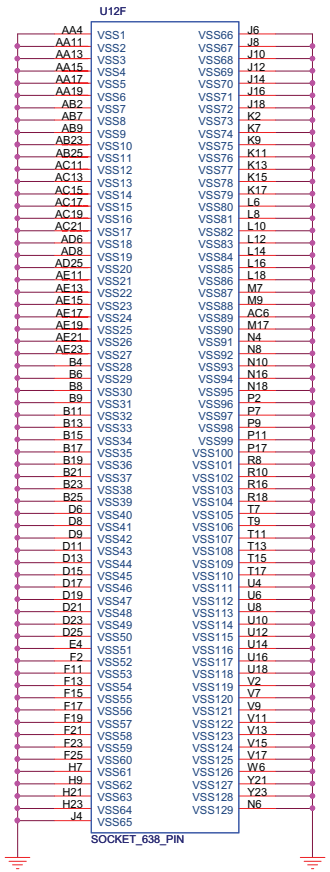
U12C

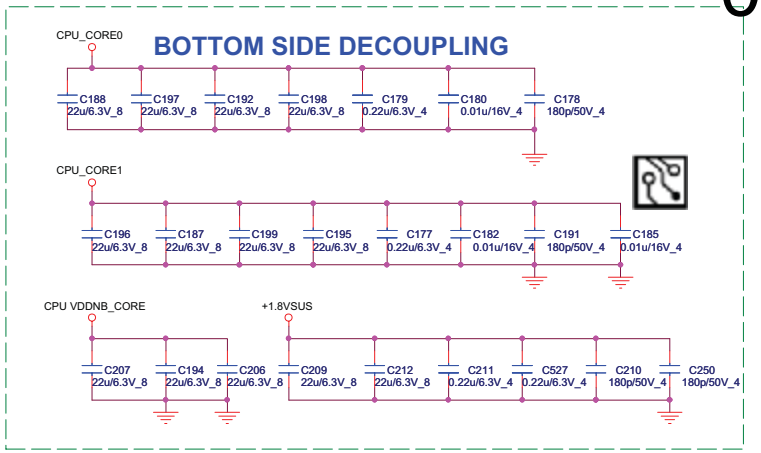
MEM:DATA

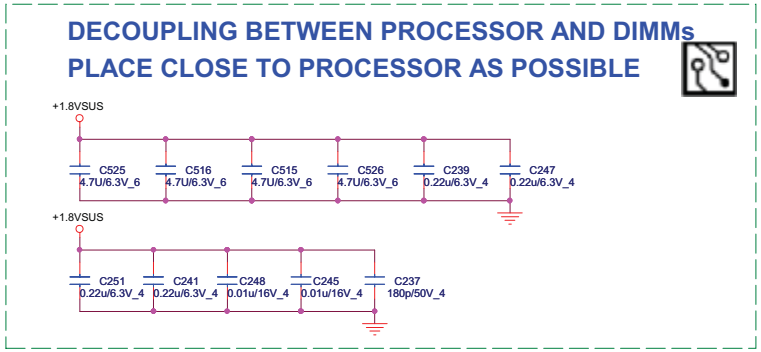
SOCKET_638_PIN

Project	PROJECT : BD3G
Company	Quanta Computer Inc.
Size	Document Number: S1G2 DDRII MEMORY I/F 2/3
Rev	1A
Date	Thursday, May 29, 2008
Sheet	5 of 42





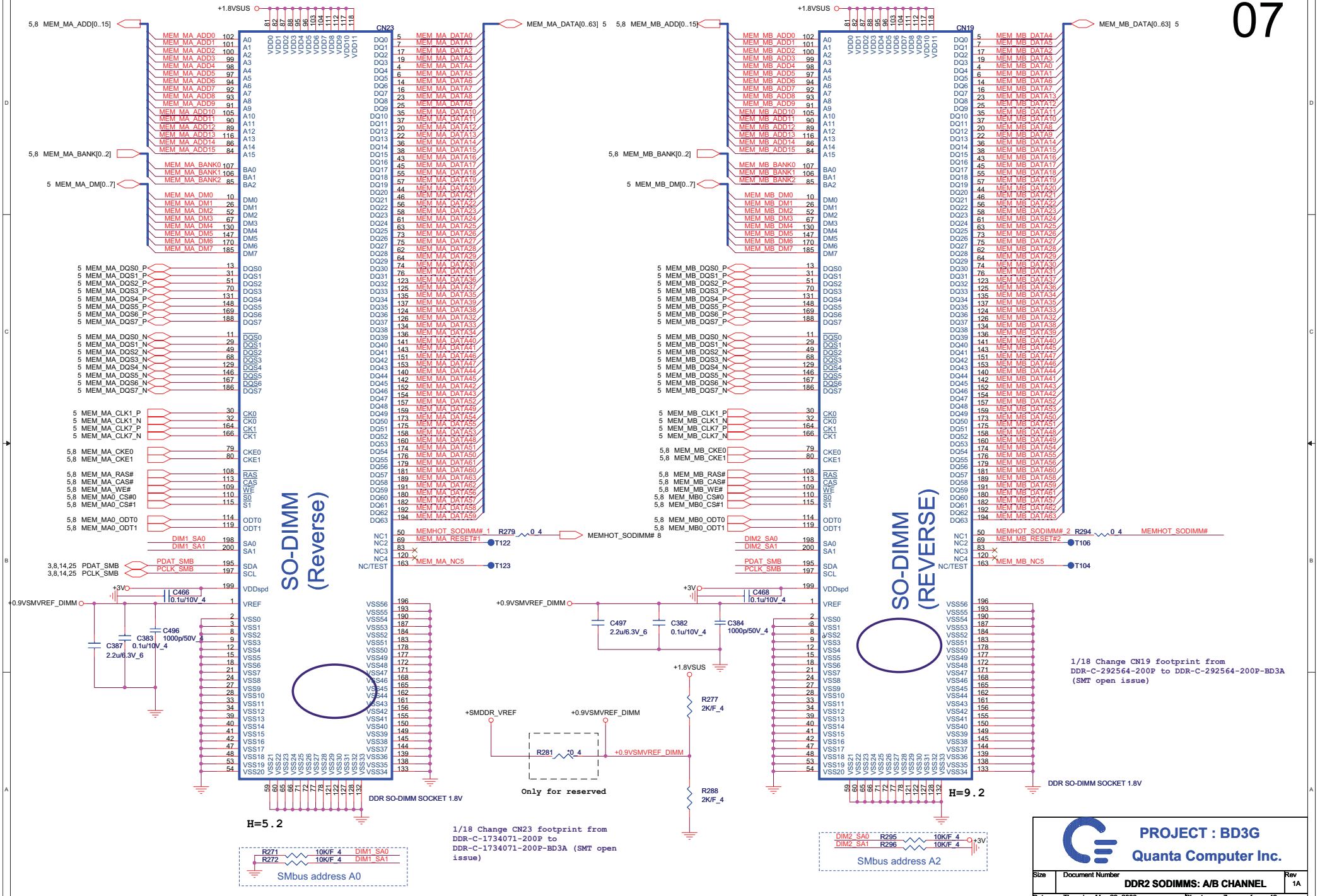




PROCESSOR POWER AND GROUND

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	S1G2 PWR & GND 3/3	1A
Date: Thursday, May 29, 2008	Sheet 6 of 42	

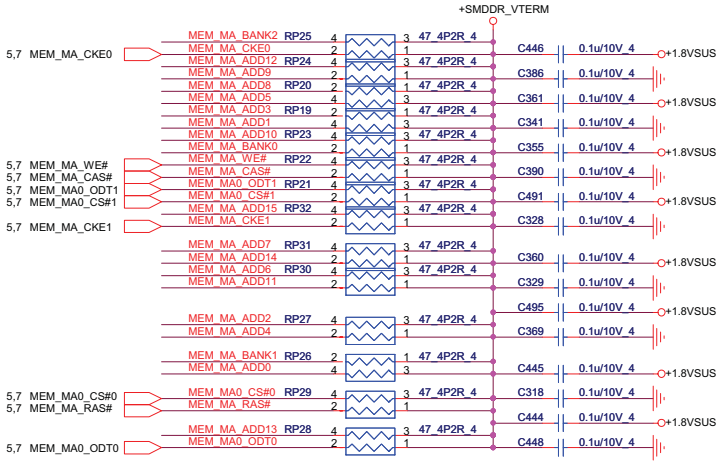


PROJECT : BD3G

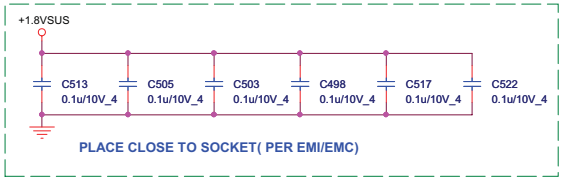
Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SODIMMS: A/B CHANNEL	1A
Date: Thursday, May 29, 2008	Sheet 7 of 42	

5,7 MEM_MA_ADD[0..15] MEM_MA_ADD[0..15]
5,7 MEM_MA_BANK[0..2] MEM_MA_BANK[0..2]

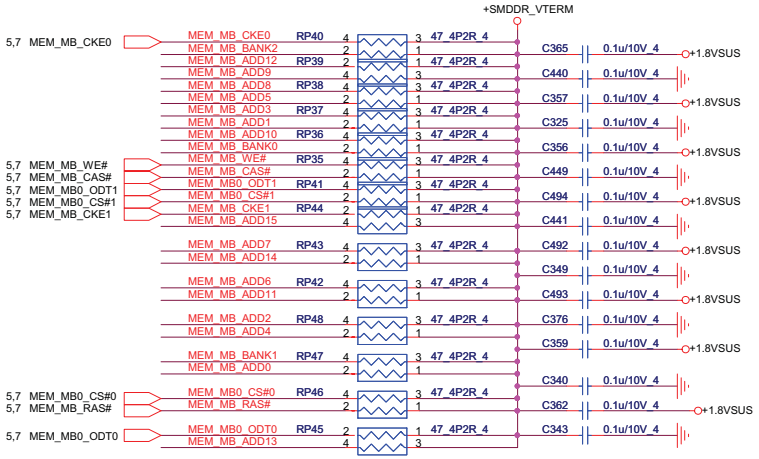


PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

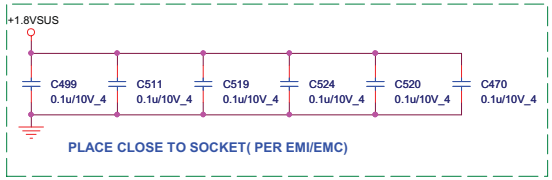


PLACE CLOSE TO SOCKET(PER EMI/EMC)

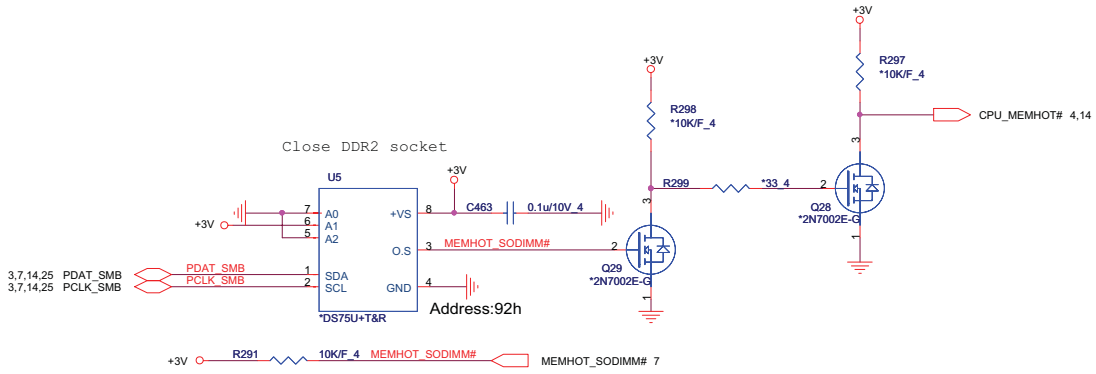
5,7 MEM_MB_ADD[0..15] MEM_MB_ADD[0..15]
5,7 MEM_MB_BANK[0..2] MEM_MB_BANK[0..2]



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

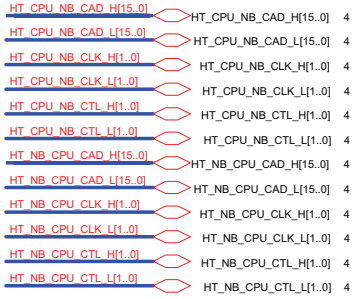


PLACE CLOSE TO SOCKET(PER EMI/EMC)



PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SODIMMS TERMINATIONS	1A
Date: Thursday, May 29, 2008	Sheet 8 of 42	



11/4 modify

signals	RS780	RX780
HT_TXCALP	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

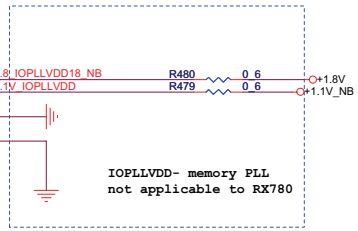
RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

A12 version
RS780M AJ067400T05 100-CK2612(216-0674008-00)
RS780MC AJ067400T06 100-CK2613(216-0674010-00)
RX781 AJ067400T10 100-CK2642(215-0674024)
SB700 AJA12FG0T18 100-CK2614(218S7EALA12FG)

A13 version
RS780M AJ067400T18 100-CK2699(216-0674022)
RS780MC AJ067400T20 100-CK2704(216-0674024)
RX781 AJ067400T21 100-CK2706(215-0674034)
A12 version
SB700 AJA12FG0T18

This block is for UMA RS780 only , RX780 can remove all component

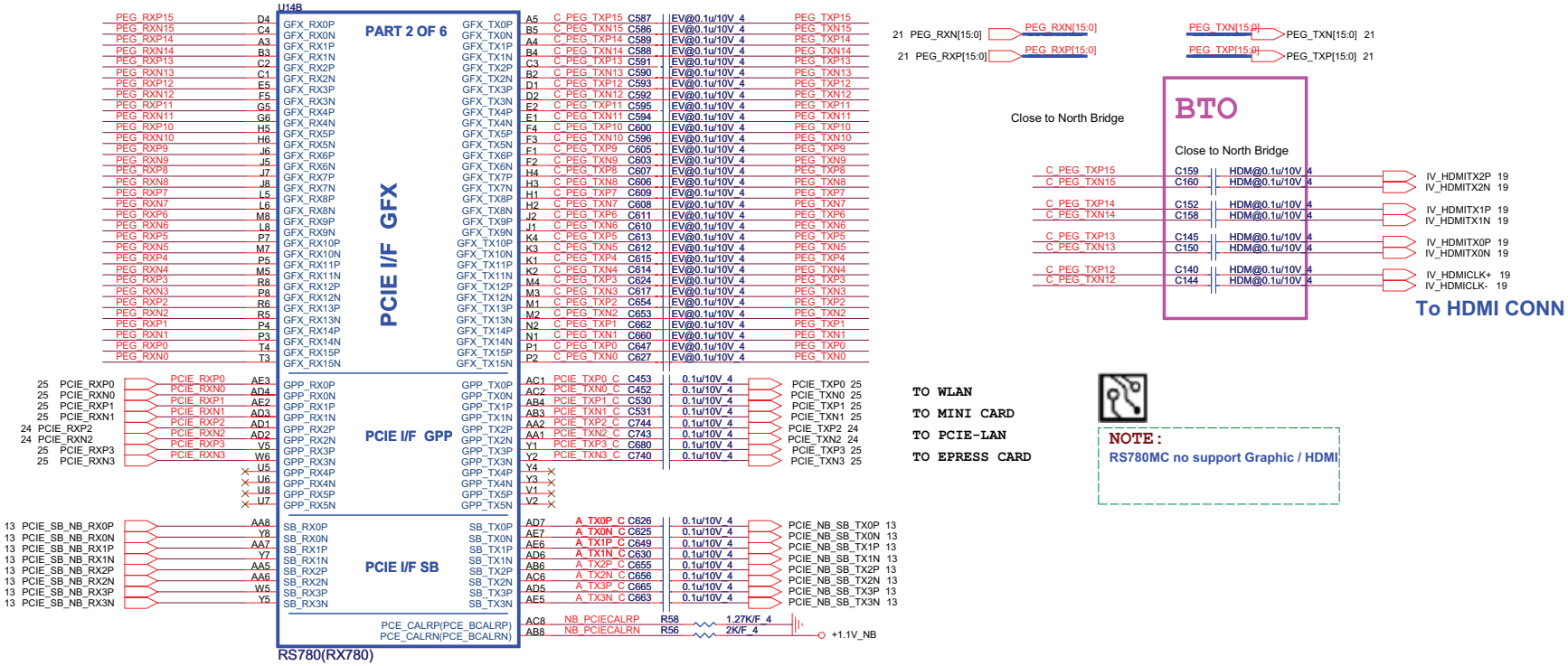


2/1 R480,R479 no stuff when RS780M without side port / RX781

4/24 stuff R480,R479

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-HT LINK I/F 1/5	1A
Date: Thursday, May 29, 2008	Sheet 9 of 42	



21 PEG_RXN[15:0] PEG_RXN[15:0]
21 PEG_RXP[15:0] PEG_RXP[15:0]
PEG_TXN[15:0] PEG_TXN[15:0] 21
PEG_TXP[15:0] PEG_TXP[15:0] 21

Close to North Bridge

BTO

Close to North Bridge

To HDMI CONN

TO WLAN
TO MINI CARD
TO PCIE-LAN
TO EPRESS CARD

NOTE :
RS780MC no support Graphic / HDMI

11/4 modify

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-PCIE I/F 2/5	1A
Date: Thursday, May 29, 2008	Sheet 10 of 42	

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

10/26 change to 4 pin S-video conn , no need TV_comp

2/1 follow A13 request change
R103 from 150 to 140 CS11402FB19

RX780
4,13 CPU_LDT_RST# — R30 *0_4 — NB_RST# IN
RS780
13 NB_PLTRST# — R31 0_4
North Bridge RESET

11/4 stuff R5160 for RS780M/MC/RX781

RX780
+1.1V_NB — R47 *2K/F_4 — INT_CRT_DDCDAT
R46 *2K/F_4 — INT_CRT_DDCCLK
10/9 add 2K pull up to DDCDAT /DDCCLK for RX780

11/4 no stuff for RS780M/MC/RX781

12/22 stuff R48 2.2K for power play

+NB_CORE_ON — R44 *10K/F_4 — +3V
R48 2.2K_4

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM
if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT

RX780
RS780_AUX_CAL — R491 *3K_4

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780

RX780
INT_TV_C/R — R96 *3K_4
Reserved only

12/22 stuff R65

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RS780 , Default
0 : Disable RS780
(RS780 use VSYNC#)

RS780
INT_VSYNC — R65 3K_4 — +3V
R66 *3K_4

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780
INT_HSYNC — R489 3K_4 — +3V
R490 *3K_4

10/19 RS780M Databook rev 1.01 define High disable

U14C — PART 3 OF 6 — RS780(RX780)

CRT/TVOUT
+3V_AVDD_NB — R95 IV@150/F_4 — INT_TV_C/R
R89 IV@150/F_4 — INT_TV_Y/G
R84 *150/F_4 — INT_TV_COMP
+1.8V_AVDDDI_NB
+1.8V_AVDDQ_NB
18 INT_TV_C/R
18 INT_TV_Y/G
18 INT_CRT_RED — R103 IV@140/F_4 — INT_CRT_RED
18 INT_CRT_GRN — R99 IV@150/F_4 — INT_CRT_GRN
18 INT_CRT_BLU — R102 IV@150/F_4 — INT_CRT_BLU
18 INT_HSYNC — INT_HSYNC
18 INT_VSYNC — INT_VSYNC
18 INT_CRT_DDCDAT — INT_CRT_DDCDAT
18 INT_CRT_DDCCLK — INT_CRT_DDCCLK
R79 IV@715/F_6 — DAC_RSET_NB

PLL PWR
+1.1V_PLLVDD
+1.8V_PLLVDD18
+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL

PM
17 NB_PWRGD_IN — NB_PWRGD_IN
NB_RST# IN
NB_LDT_STOP#
NB_ALLOW_LDTSTOP

CLOCKs
3 NBHT_REFCLKP — NBHT_REFCLKP
3 NBHT_REFCLKN — NBHT_REFCLKN
3 EXT_NB_OSC — R485 0_4 — NB_REFCLK_P
R53 0_4 — NB_REFCLK_N
+1.1V_NB — R50 4.7K_4 — RS780 — R51 4.7K_4
3 NBGFX_CLKP — NBGFX_CLKP
3 NBGFX_CLKN — NBGFX_CLKN
3 NBGPP_CLKP — NBGPP_CLKP
3 NBGPP_CLKN — NBGPP_CLKN
3 SBLINK_CLKP — SBLINK_CLKP
3 SBLINK_CLKN — SBLINK_CLKN

MIS.
20 INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA
20 INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK
19 IV_HDMI_DDCDATA — IV_HDMI_DDCDATA
19 IV_HDMI_DDCCLK — IV_HDMI_DDCCLK
T145 — RS740_DFT_GPIO1
T144
35 +NB_CORE_ON — R49 0_4 — STRP_DATA
T143 — RS780_AUX_CAL

TXOUT_L0P(NC) A22 — INT_TXLOUT0+ 20
TXOUT_L0N(NC) B22 — INT_TXLOUT0- 20
TXOUT_L1P(NC) A21 — INT_TXLOUT1+ 20
TXOUT_L1N(NC) B21 — INT_TXLOUT1- 20
TXOUT_L2P(NC) B20 — INT_TXLOUT2+ 20
TXOUT_L2N(DBG_GPIO0) A20 — INT_TXLOUT2- 20
TXOUT_L3P(NC) A19 — T139
TXOUT_L3N(DBG_GPIO2) B19 — T137
TXOUT_U0P(NC) B18 — INT_TXUOUT0+ 20
TXOUT_U0N(NC) A18 — INT_TXUOUT0- 20
TXOUT_U1P(PCIE_RESET_GPIO3) A17 — INT_TXUOUT1+ 20
TXOUT_U1N(PCIE_RESET_GPIO2) B17 — INT_TXUOUT1- 20
TXOUT_U2P(NC) D20 — INT_TXUOUT2+ 20
TXOUT_U2N(NC) D21 — INT_TXUOUT2- 20
TXOUT_U3P(PCIE_RESET_GPIO5) D18 — T140
TXOUT_U3N(NC) D19 — T138
TXCLK_LP(DBG_GPIO1) B16 — INT_TXLCLKOUT+ 20
TXCLK_LN(DBG_GPIO3) A16 — INT_TXLCLKOUT- 20
TXCLK_UP(PCIE_RESET_GPIO4) D16 — INT_TXUCLKOUT+ 20
TXCLK_UN(PCIE_RESET_GPIO1) D17 — INT_TXUCLKOUT- 20
VDDLT18P18(NC) A13 — +1.8V_VDDLTP18_NB
VSSLT18P18(NC) B13
VDDLT18_1(NC) A15 — +1.8V_VDDLT_18_NB
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14 — +3V_VDLT33_NB
VDDLT33_2(NC) B14
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

11/01 exchange LVDS_PWM /LVDS_BLON

LVDS_DIGON(PCE_TCALRP) E9 — INT_LVDS_DIGON 20
LVDS_BLON(PCE_RCALRP) F7 — INT_LVDS_PWM 20
LVDS_ENA_BL(PWM_GPIO2) G12 — INT_LVDS_BLON 20
R25 *1.27K/F_4
R11 *1.27K/F_4
For RX780 only

TMDS_HPD(NC) D9 — TMDS_HPD0 — R26 IV@0_4 — IV_HDMI_HPD 19
HPD(NC) D10 — TMDS_HPD1 — T2
TVCLKIN(PWM_GPIO5) D12 — SUS_STAT# NB — R71 0_4 — SUS_STAT# 14
THERMALDIODE_P AE8 — R_NB_THRMDA — T142
THERMALDIODE_N AD8 — R_NB_THRMDC — T141
TESTMODE D13 — TEST_EN
R75 1.82K/F_4

1/17 RX781 connect to GND
C104,C110,C646,C98,C136,C103,C118 change to CS00003J951

AVDD-DAC Analog not applicable to RX780
+3V — L2 BLM18PG221SN1D(220,1.4A)_6 — +3V_AVDD_NB — C104 2.2u/6.3V_6
+1.1V_NB — L53 BLM18PG221SN1D(220,1.4A)_6 — +1.1V_PLLVDD — C646 2.2u/6.3V_6

PLLVDD - Graphics PLL not applicable to RX780

PLLVDD18 - Graphics PLL not applicable to RX780
+1.8V — L12 BLM18PG221SN1D(220,1.4A)_6 — +1.8V_PLLVDD18 — C124 10u/6.3V_8 — C110 2.2u/6.3V_6

AVDDI-DAC Digital not applicable to RX780
+1.8V — R76 0_6 — +1.8V_AVDDI_NB — C98 2.2u/6.3V_6

AVDDQ-DAC Bandgap Reference not applicable to RX780
L17 BLM18PG221SN1D(220,1.4A)_6 — +1.8V_AVDDQ_NB — C136 2.2u/6.3V_6

VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780
+1.8V — L51 BLM18PG221SN1D(220,1.4A)_6 — +1.8V_VDDLTP18_NB — C103 2.2u/6.3V_6

L10 BLM21PG221SN1D(220,100M,2A)_8 — +1.8V_VDDLT_18_NB — C118 4.7u/6.3V_6 — C115 0.1u/10V_4

1/17 RX781 no stuff them
L2,L12,C124,L52,R76,L17,L51,L10,C115

VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

1/31 voltage leakage issue
remove Q5,Q3,R83,R80,R97
stuff R88,R77

VDDA18PCIEPLL -PCIE PLL
+1.8V — L1 BLM18PG221SN1D(220,1.4A)_6 — +1.8V_VDDA18PCIEPLL — C79 2.2u/6.3V_6
20mils width

VDDA18HTPLL -HT LINK PLL
L13 BLM18PG221SN1D(220,1.4A)_6 — +1.8V_VDDA18HTPLL — C131 2.2u/6.3V_6
20mils width

Q5 *BSS138_NL/SOT23
4,13 CPU_LDT_STOP# — R88 0_4 — NB_LDT_STOP#
+1.8V — R83 *4.7K_4 — +VDDG_NB
RS780

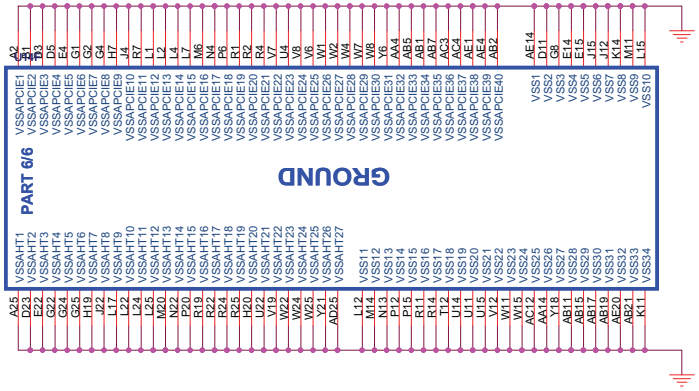
Q3 *BSS138_NL/SOT23
4 CPU_LDT_REQ# — R74 0_4 — NB_ALLOW_LDTSTOP
13 ALLOW_LDTSTOP — R77 0_4
+1.8V — R80 *4.7K_4 — +VDDG_NB
RS780

RX780
+1.8V — R106 *0_6 — +VDDG_NB
RS780
+3V — R97 *0_6

+3V — L9 *BLM21PG221SN1D(220,100M,2A)_8 — +3V_VDLT33_NB — C108 *2.2u/6.3V_6
VDDLT33 - LVDS or DVI/HDMI ANALOG RS740 only

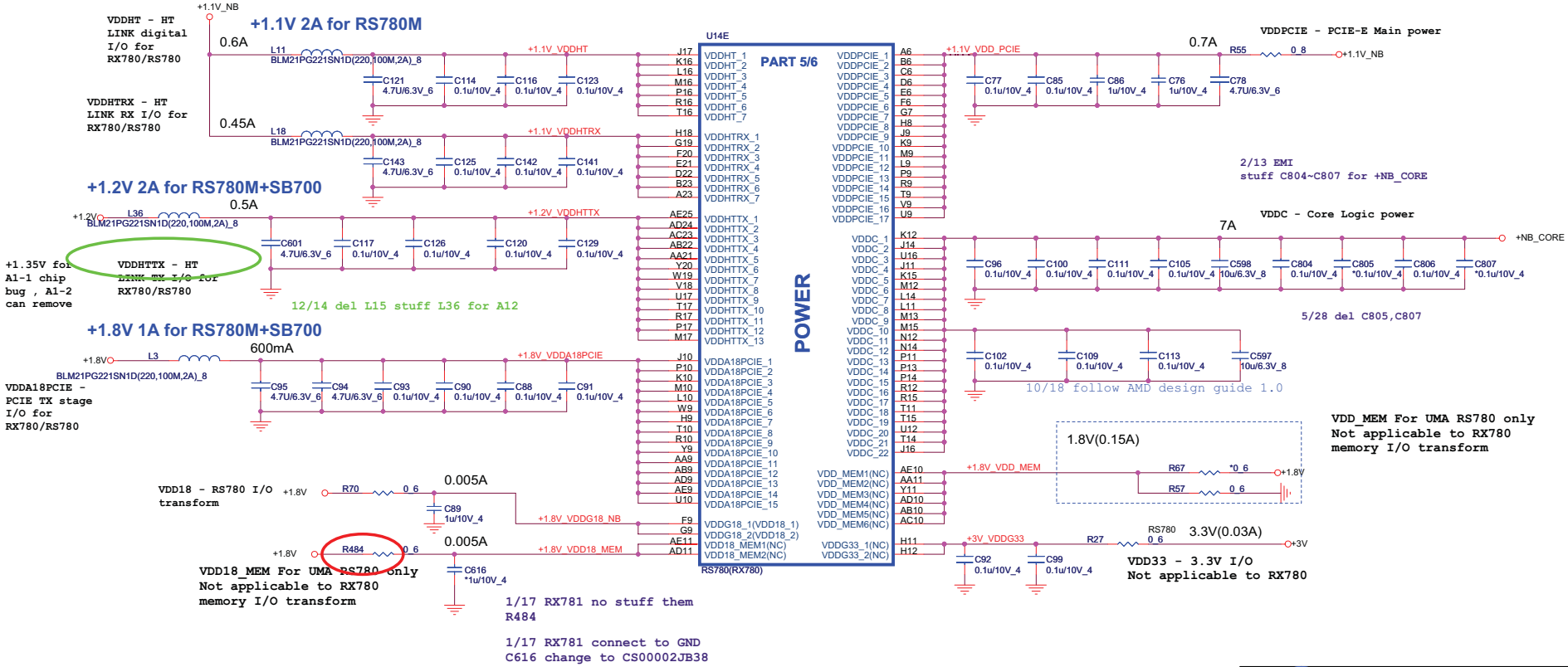
PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-SYSTEM I/F 3/5	1A
Date: Thursday, May 29, 2008	Sheet 11 of 42	



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



Size	Document Number		Rev
	RS740/RS780-POWER5/5		1A
Date: Thursday, May 29, 2008	Sheet 12 of 42		

PROJECT : BD3G
Quanta Computer Inc.

2/4 reserve C800 PLTRST#

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

PCIE_PVDD-- PCIE PLL POWER

SB700 Part 1 of 5

1/31 voltage leakage remove R349

1/17 R301,R302 change from 8.66k to 2k. R332 change from 4.7K to 6.8K

4/16 change RTC pad location to G1

All the PCI bus has build-in Pull-UP/Down resistors

Maybe can remove

A11 default PCICLK5
A12 default GPIO41

R571+R667 = (5V - 0.2V-2V)/0.2mA = 14k

10/18 AMD suggest to not connect to GND

100MHZ

40mA

SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	SB700-PCIE/PCI/CPU/LPC 1/4	1A
Date: Thursday, May 29, 2008	Sheet 13 of 42	

NC only ,Can't be install

11/01 chagne +3VSUS to +3V_S5

10/31 add newcard DET#

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it

Clock gen
/DDR2 /MINI CARD/NEW CARD

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

4/16 pull up USB_OC5# R719

10/26 modify it
11/06 check it

1/31 NEW_DET# change from GEVEN5# to GPM1#

12/7 add D57,D58 to avoid voltage leakage

HD audio
interface is
3.3V voltage

To Azalia

12/21EMI
change R241from 33 to BK1005HM121-T
stff C309 22p

High : Main Strem
Low : Low Cost

High : W/O FM
Low : W FM

10/25 modify it

1/31 voltage leakage
BOARD_ID4 change from GPIO66 to GPIO3

12/4 change PD from 10K to 1K

10/25 Board ID define MXM

MB ID

MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ MXM W/O MXM			H L		
W/ S-VIDEO W/O S-VIDEO		H L			
W/ HDMI W/O HDMI	H L				

SB700 Part 4 of 5

10/25 change M.B USB to port 6/7

3/3 del Mini card USB10,Felica USB5 , change BT to port5 ,
ESATA to port 10

10/18 USB swap for layout route

SPI/LPC define

for EMI

PROJECT : BD3G	
Quanta Computer Inc.	
Size	Document Number: SB700-ACPI/GPIO/USB 2/4 — Rev: 1A
Date: Thursday, May 29, 2008	Sheet 14 of 42

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

SATA PORT 0,1,2,3 can support AHCI mode

SATA1

SATA2

E-SATA

ODD

2/22 change SATA ODD from port3 to port4 (solve ODD post detect fail)

SATA PORT 4,5 are only support IDE mode

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

10/25 modify it

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

12/8 change from 10p to 27p

SB700
Part 2 of 5

SERIAL ATA

SATA PWR

ATA 66/100/133

SPI ROM

HW MONITOR

12/4 change BOARD ID3 from GEVENT7 to GPIO48

11/02 modify it

10/18 AMD suggest to connect to GND

AVDD--H/W monitor Analog power

5mA

2/13 EMI
stuff C375,C366 for SB HW MONITOR

77mA

1mA

Place near ball

PROJECT : BD3G
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Size	Document Number	Rev
	SB700-SATA/IDE/HWM/SPI 3/4	1A
Date: Thursday, May 29, 2008	Sheet 15 of 42	

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

12/14 del R234 stuff R235 for A2

23

VDDQ--3.3V I/O power

0.8A

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

10/18 change to +1.8V

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power

0.45A

4/24 IDE/FLASH not use
,remove
C287,C288,C297,C293,C294

VDD-- S/B CORE power

604mA

CKVDD_1.2V-- Internal
clock Generator I/O
power

286mA

4/24 internal clk not use
remove C332,C330,C327,C331
change L28 to 0 ohm

POWER

PCIE_VDDR--PCIE I/O power

844mA

S5_3.3--3.3v standby power

0.01A

Change to 0603

AVDD_SATA--SATA phy power

0.2A

S5_1.2V--1.2V standby power

0.22A

0.2A

For support USB wakeup-->3V_S5

AVDDTX--USB Phy
Analog I/O power

0.2A

V5_VREF--PCI 5V TOLERANCE

4mA

7mA

44mA

16mA

USB_PHY_1.2V--USB Phy
digital power

AVDDC--USB Analog PLL power

AVDDCK_1.2--USB Phy
digital power

AVDDCK_3.3--Analog
system PLL power

SB700
Part 3 of 5

SB700
Part 5 of 5

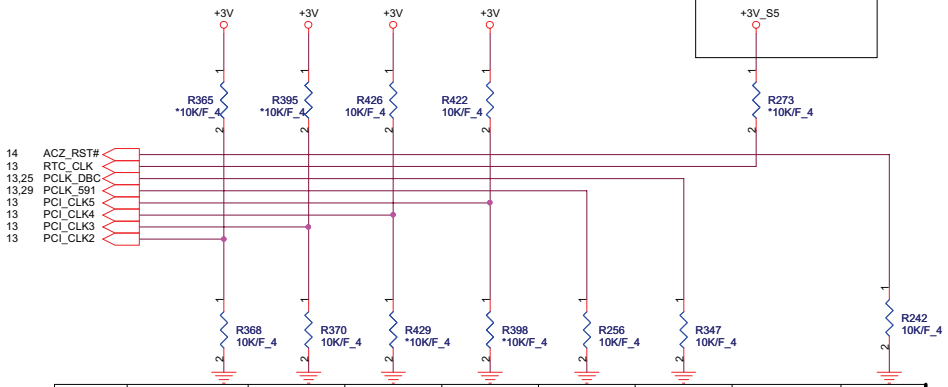
GROUND

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	SB700-PWR/DECOUPLING 4/4	1A
Date: Thursday, May 29, 2008	Sheet 16 of 42	

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

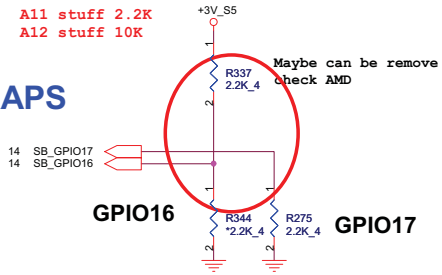
It must ready refore RSMRST#



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT
					EC ENABLED			ENABLE PCI MEM BOOT

REQUIRED STRAPS

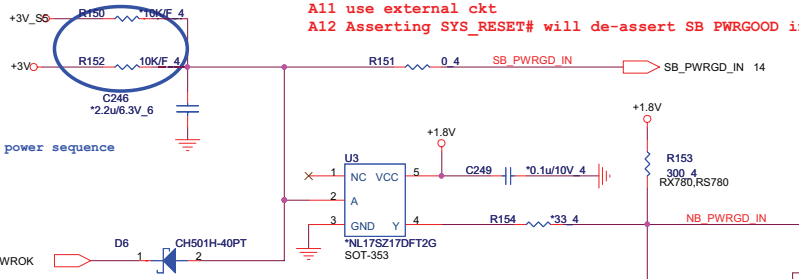
A11 stuff 2.2K
A12 stuff 10K



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

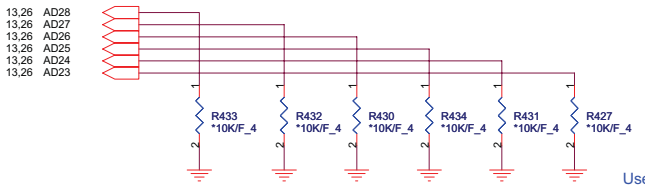
SB_PWRGD
A11 use external ckt
A12 Asserting SYS_RESET# will de-assert SB PWRGOOD internally



4/10 change R150 to R152 for power sequence

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB/SB POWER GOOD CIRCUIT

WD_PWRGD: Push/Pull when A11SB700, OD when A12SB700.

	U11	R230	R229	R245	R234
RX780 RS780M	V	V	V	X	X

12/18 add cap for NB_PWRGD signal

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

4/24 stuff C765 10nf to meet power sequence

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	SB700-STRAPS	1A
Date: Thursday, May 29, 2008	Sheet 17 of 42	

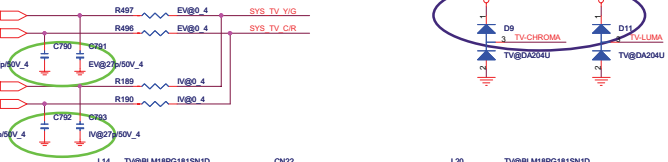
TVOUT BTO

5/8 stuff D9,D11 for S-VIDEO

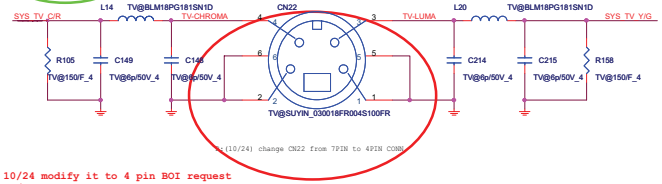
TVOUT

close to NB & VGA connector

12/21 EMI
add 27p for TV_Y/G , TV_C/R



BTO



10/24 modify it to 4 pin BOI request
10/30 modify footprint to SV-030018FR004S100FR-RVS-4P-H
12/12 update p/n to DFMD04FR006
4/16 update footprint to sv-030018fr004s100fr-4p-h-b15m

CRT PORT

2/1
RS780M A13 R8 ---> 140 CS11402FB19
MXM R8 ---> 150 CS11502FB21

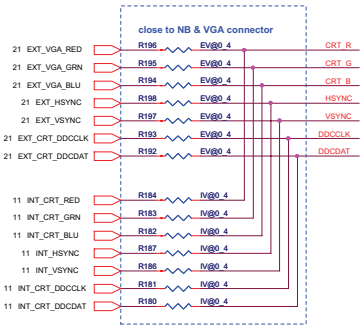
1/31 EMI Change L4,L5,L6 from CX0HM121008 to CX8BA470003

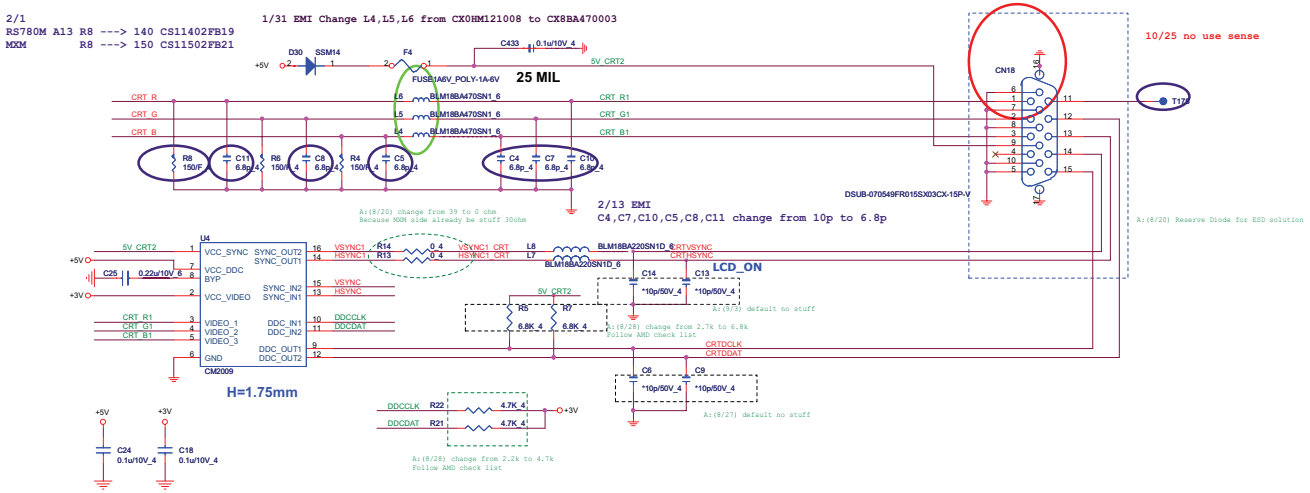
10/12 fix CRT connect error

2/10 DEL D4,D5 footprint and DEL CRT_SENSE# net

10/25 no use sense

close to NB & VGA connector

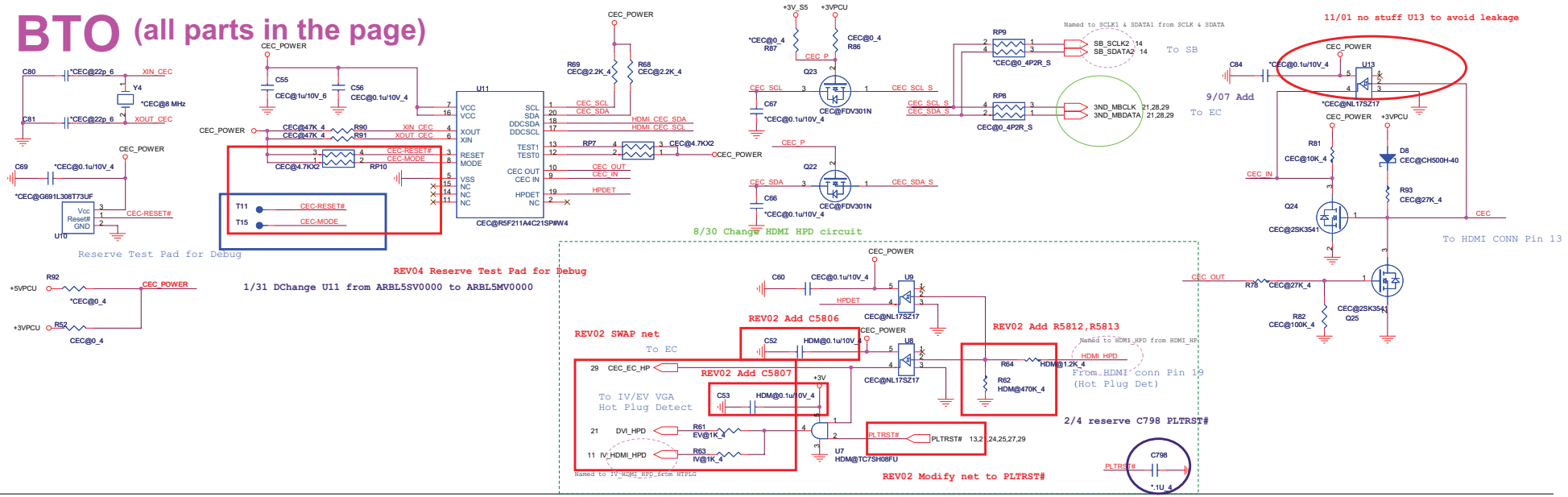




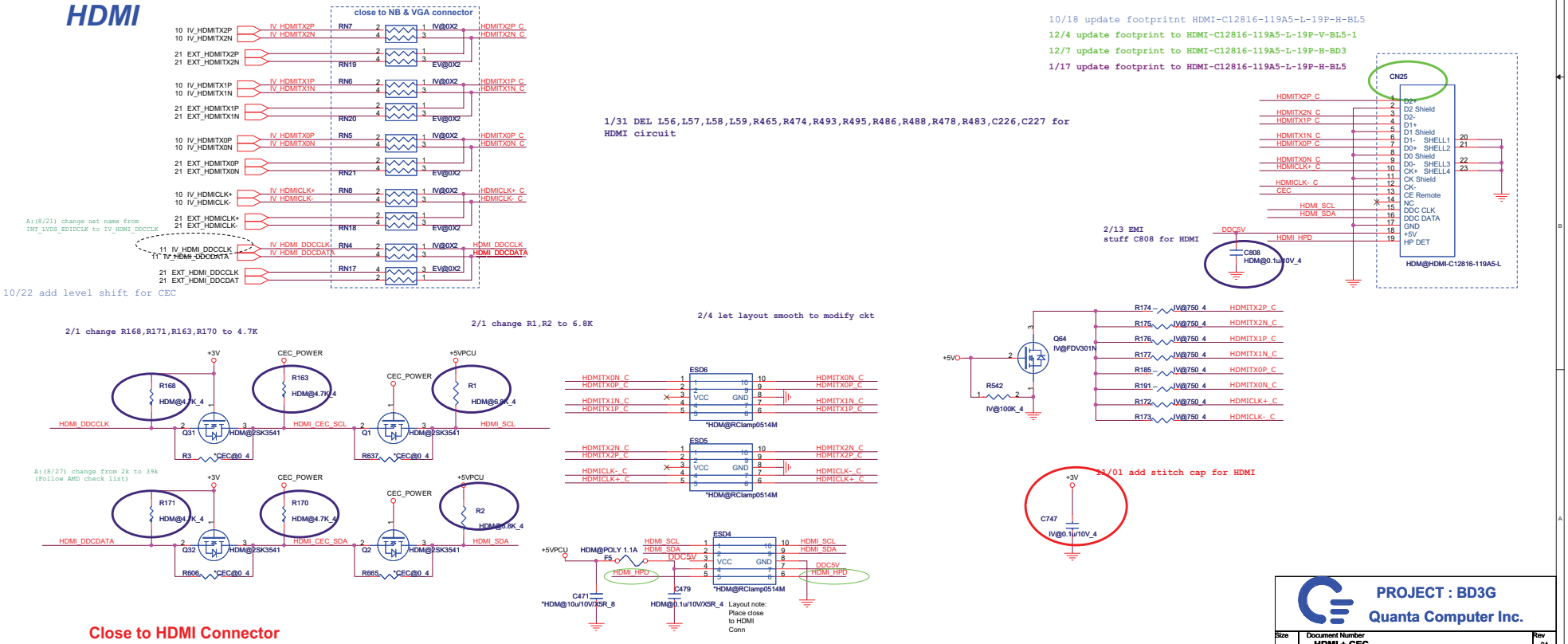
PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	SB600 STRAPS/TV/CRT	2A
Date: Thursday, May 29, 2008	Sheet 18 of 42	

BTO (all parts in the page)

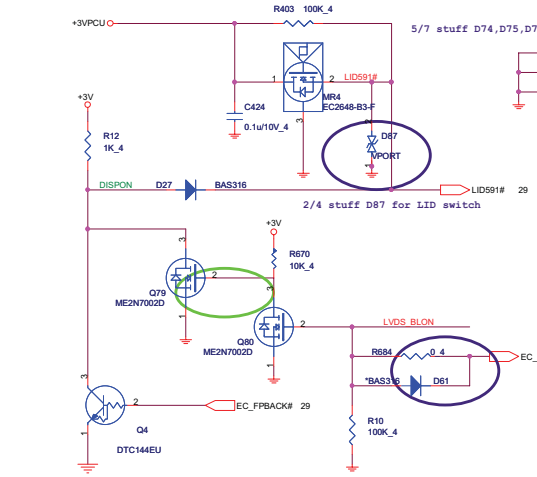


HDMI

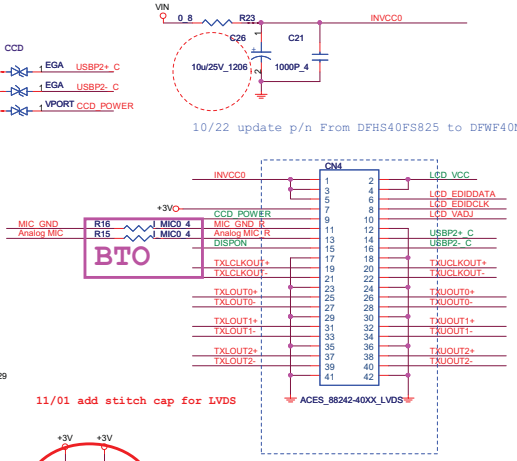


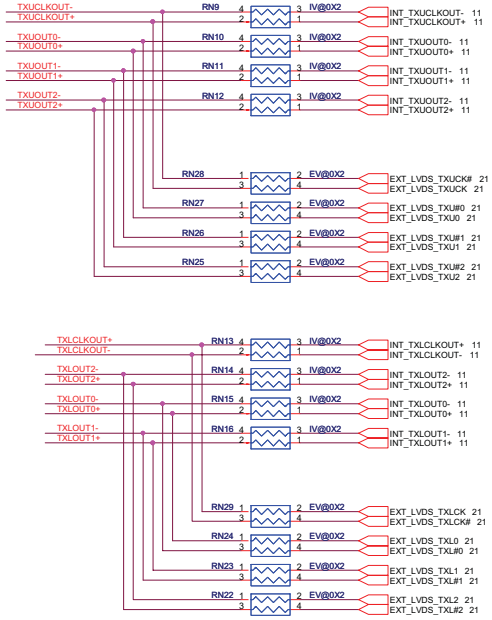
PROJECT : BD3G			
Quanta Computer Inc.			
Size	Document Number		Rev
	HDMI + CEC		2A
Date:	Thursday, May 29, 2008	Sheet 19 of 42	

HALL SENSOR

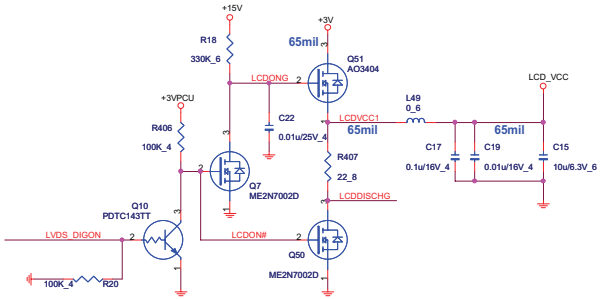


LCD TYPE CONNECTOR

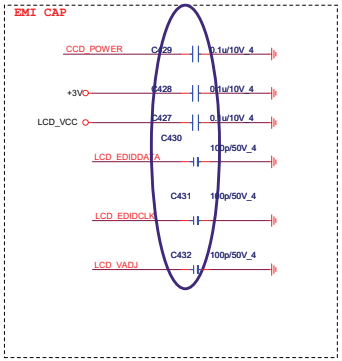


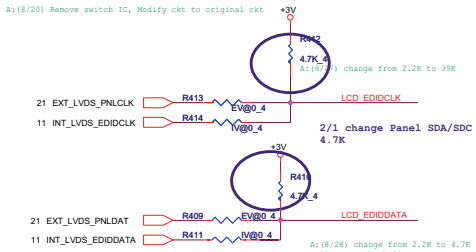


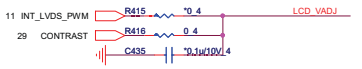
1/17 EnegryStar 4.0 Idle power issue
When BLON= High, Turn ON LCD then turn ON MMB
When BLON= Low, Turn OFF LCD then turn OFF MMB

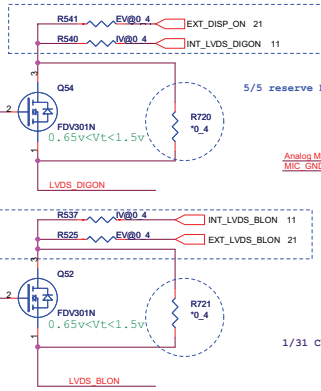


2/13 EMI
stuff C427~C432

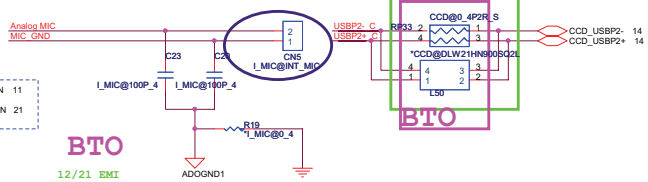






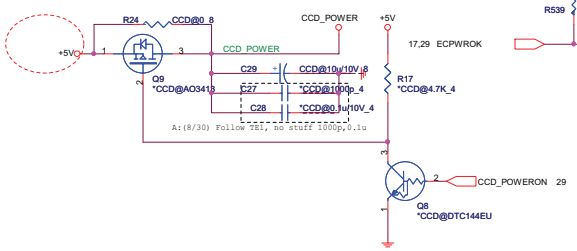


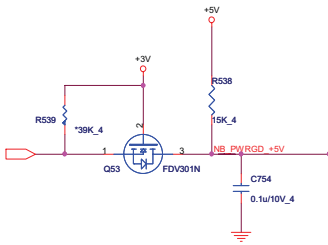
5/5 reserve R720,R721 for cost down



BTO

CAMERA MODULE





A:(8/27) Camera module power +5V or +3V?

A:(8/18) update VGA conn footprint base on Allan information
A:(8/23) update VGA conn pin-define (change pin 1 location)

CN27

EV@QT00200A-5120T-9F

2/4 reserve C797 PLTRST#

C797 *1U_4

A:(9/18) don't connect pin 161, 167, 171, 183, 187,188 to ground and reserve test point for A build.

A:(9/19) don't have enough space to put the test point, Remove it for A-test

0.5A

1.5A

A:(9/14) no stuff for A-stage

10/30 modify to +3V

A:(8/29) reserve 100u for VIN

4A

1/17 Remove R492,R517, Short CN27/Pin189,190 to VIN directly.

12/21 EMI
stuff C568,C548

R208 EV@4.7K_4
Q37 EV@RHU002N06
19,28,29 3ND_MBCLK
VGA_MBCLK

R203 EV@4.7K_4
Q34 EV@RHU002N06
19,28,29 3ND_MBDATA
VGA_MBDATA

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	MXM CONNECTOR / TV	2A
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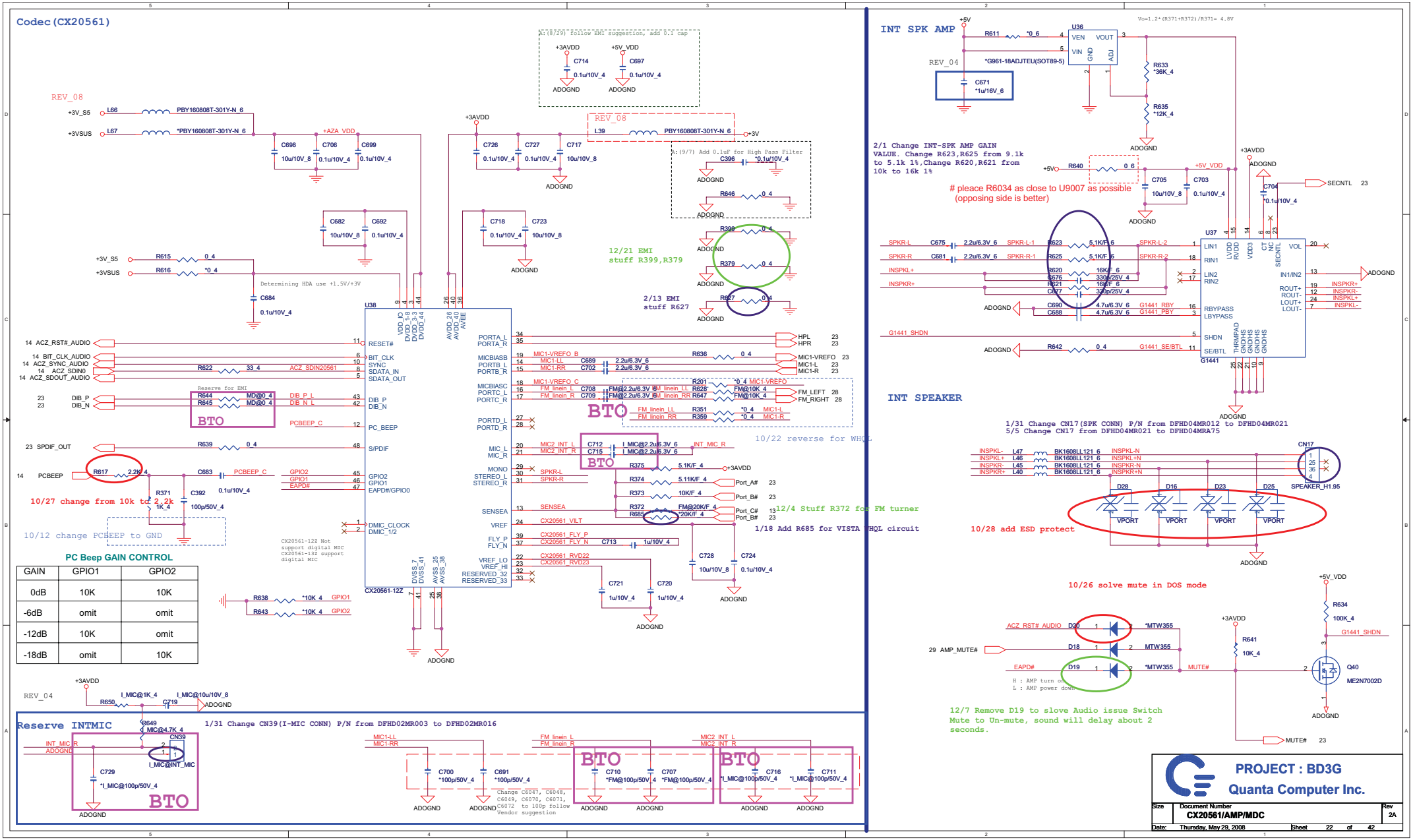
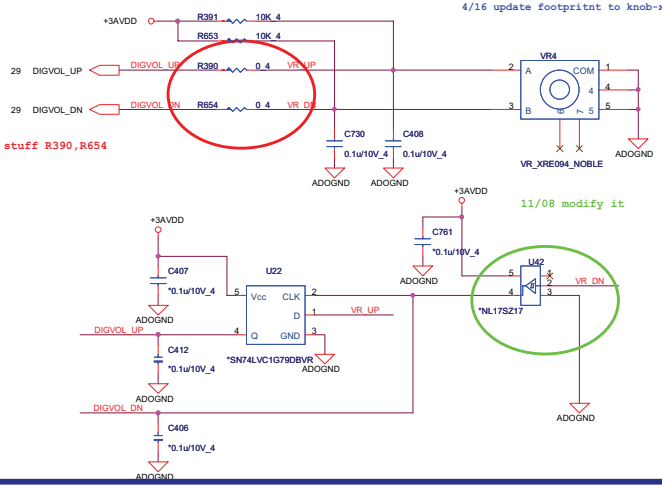
Codec (CX20561)



VR

4/16 update footpritnt to knob-xre094-3p-bl5m

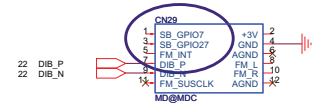


MDC

REV_04

1/18 Change CN43 footprint from MDC-1-179373-2-12P-RUV to MDC-1-179373-2-12P-RUV-BD3A (SMT open issue)

BTO



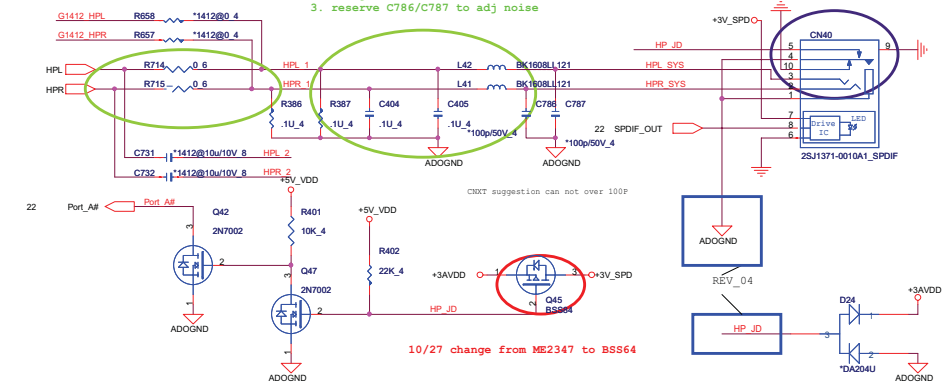
12/07 Slove Audio issue:When plug in-out headphone,headphone has bo sound.
1. Change R652&R651 to C763,C764(10U/6.3V 0603)

2/5 Change R714,R715 from 10uF to 0 ohm (Audio HP circuit)

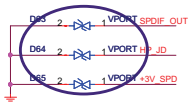
HP

12/20 solve GPRS noise
1. stuff R386/R387/C404/C405 to 0.1U
2. Change L44/41 to BK1608LL121
3. reserve C786/C787 to adj noise

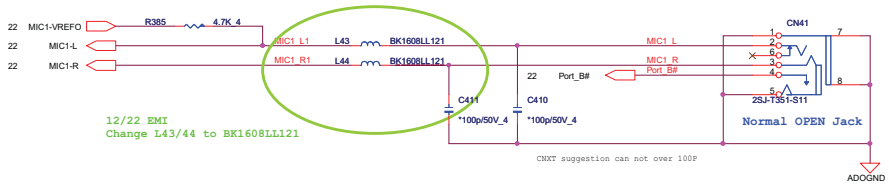
2/4 CN40 pin 9/10 connect to GND



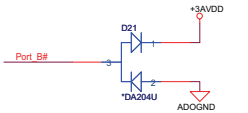
2/4 add Varistor D63,D64,D65 on SPDIF_OUT/HP_JD/+3V_SPD



SYSTEM MIC

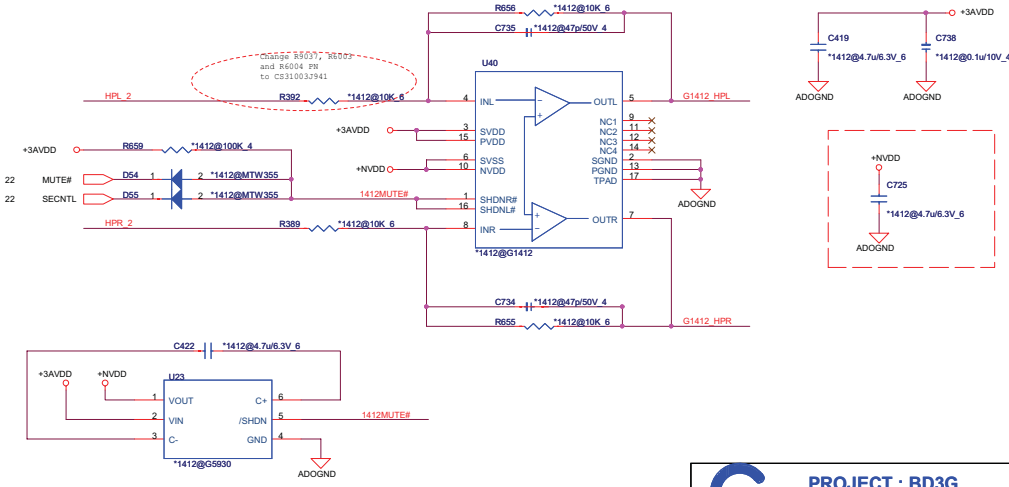


12/22 EMI
Change L43/44 to BK1608LL121



HP Amplifier

REV_05



PROJECT : BD3G		
Quanta Computer Inc.		
Size	Document Number: Audio JACK /VR/FM Tuner	Rev: 2A
Date: Thursday, May 29, 2008	Sheet 23 of 42	

LAN_MARVELL_88E8040/88E8055

10/100 : 88E8040T P/N : AL008040001
GIGA : 88E8072 P/N : AL008072000

U35

88E805X

10 PCIE_RXN2
10 PCIE_RXP2
10 PCIE_TXN2
10 PCIE_TXP2
C657 0.1u/10V_4
C650 0.1u/10V_4
PERN1
PERP1
TX_N
TX_P
RX_N
RX_P

3 CLK_PCIE_LAN#
3 CLK_PCIE_LAN
REFCLKN
REFCLKP

SPI_DI
SPI_DO
SPI_CLK
SPI_CS

+3V_S5
3 CLKREQ_LAN#
R594 40@4.7K_4
PU_VDDO_TTL
PU_VDDO_TTL
CLKREQn

To: SB PCIE wake up pin (Input)

VPD_DATA
VPD_CLK
Rev04 modify 2007/08/14

13,19,21,25,27,29 PLTRST#
R629 0_4
PERSTn/TSTPT

14,25 PCIE_WAKE#
WAKEn

R631 40@55@4.87K/F_4
LAN_RSET
RSET
Rev03 modify 2007/08/13
Rev05 modify 2007/08/16

TESTMODE

+3V
+3V_S5
VMAIN_AVLBL
VAUX_AVLBL

T171
SWITCH_VAUX
T170
SWITCH_VCC

+3V_S5
R630 4.7K_4
29 LOM_DISABLE#
D56 *BAS316
LOM_DISABLEn

LAN_XIN
LAN_XOUT
XTALI
XTALO

LAN_RSET
2K Ohm for 8040
4.87K Ohm for 8055

12/7 change R499 0ohm to D56 to avoid leakage

C395 27p/50V_4 LAN_XIN
Y8 25MHz
C394 27p/50V_4 LAN_XOUT

GND10
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9

VDDO_TTL
VDDO_TTL
VDDO_TTL
VDDO_TTL
+3V_S5

AVDDH
AVDD
AVDD
AVDD
AVDD
+2.5V_1.8V_LAN

AVDDL
AVDDL
NC
NC
VDD25
CTRL18

VDD
VDD
VDD
VDD
VDD
VDD
VDD
VDD
+1.2V_LAN

CTRL12
TSTPT T167
HSDACN T169
HSDACP T168

MDIN[3]
MDIP[3]
MDIN[2]
MDIP[2]
MDIN[1]
MDIP[1]
MDIN[0]
MDIP[0]

LED_ACTn
LED_LINK10/100n
LED_LINK1000n
LED_LINKn

100MBPS# R614 *0_4
1000MBPS# R618 *0_4
10_1000MBPS# R619 0_4
LAN_ACTLED#
LAN_LINKLED#

40@50@88E8040_55

DELTA 10/100 : LFE8696-R P/N : DB0MA8LAN00
H = 4mm GIGA : LFE9291-R P/N : DB0BD3LAN00

BOTHHAND 10/100 : P/N :
H = 4mm GIGA : GST5006 P/N : DB0BD3LAN01

HAN WEI 10/100 : HPL-9060 P/N : DBBL5MLAN00
H = 4mm GIGA : HPL-68 P/N : DB0Z03LAN00

12/21 EMI
add L74,C766,C767 for +2.5V_1.8V_LAN

+2.5V_1.8V_LAN
L74 BK1608HS600_6 +2.5V_1.8V_LAN_T
C766 0.1u/10V_4
C767 0.1u/10V_4

U16
TCT1 MCT1
TD1+ MX1+
TD1- MX1-
TCT2 MCT2
TD2+ MX2+
TD2- MX2-
TCT3 MCT3
TD3+ MX3+
TD3- MX3-
TCT4 MCT4
TD4+ MX4+
TD4- MX4-

+2.5V_1.8V_LAN_T
TX3P
TX3N
TX2P
TX2N
TX1P
TX1N
TX0P
TX0N

C789 55@0.1u/16V_4
C788 55@1000p/50V_4
C264 0.1u/16V_4
C263 1000p/50V_4

TERM4
TERM3
TERM2
TERM1

X-TX3P
X-TX3N
X-TX2P
X-TX2N
X-TX1P
X-TX1N
X-TX0P
X-TX0N

40@50@TRANSFORMER

R219 75/F_4
R224 75/F_4
R240 55@75/F_4
R252 55@75/F_4

C286 1000p/3KV_1808
TERM9
Check by Safety

TERMINATION PLANE

12/21
add C789,C788

Rev05 modify 2007/08/16

+3V_S5
C421 10u/6.3V_8
C673 0.1u/16V_4
C638 0.1u/16V_4
C640 0.1u/16V_4
C425 0.1u/16V_4
C693 0.1u/16V_4
L48 55@BK1608HS220_6_1A
AUX3V_S5

C420 55@4.7u/6.3V_6
C418 55@0.1u/16V_4
R397 55@4.7K_4
CTRL18
Q43 55@BCP69T1
25 mil Trace width

+2.5V_1.8V_LAN
C667 C659 C668 0.1u/16V_4
C674 C645 C678 C666 0.1u/16V_4
C417 55@4.7u/6.3V_6
Close to Q9001 Pin2/4

Close to U9001 Pin64
+2.5V_1.8V_LAN
C685 40@4.7u/6.3V_6
Rev05 modify 2007/08/16

12/21 EMI
add L73 for +1.2V_LAN

C415 55@4.7u/6.3V_6
C414 55@0.1u/16V_4
R393 55@4.7K_4
CTRL12
Q44 55@BCP69T1
25 mil Trace width

+1.2V_LAN
BK1608HS600_6 L73
C643 C639 C637 C694 0.1u/16V_4
C669 C696 C695 C642 0.1u/16V_4
C401 55@4.7u/6.3V_6
Close to Q9000 Pin2/4

Close to U9001 Pin39
+1.2V_LAN
C641 40@4.7u/6.3V_6
Rev05 modify 2007/08/16

10/30 88E8072 has included termination RC

TX3N
TX3P
TX2N
TX2P
TX1N
TX1P
TX0N
TX0P

RN33 *55@49.9/F_4P2R
RN32 *55@49.9/F_4P2R
RN31 *55@49.9/F_4P2R
RN30 *55@49.9/F_4P2R

LAN_N1 C679 *55@0.1u/16V_4
LAN_N2 C686 *55@1000p/50V_4 C670 *55@0.1u/16V_4
LAN_N3 C672 *55@1000p/50V_4 C661 *55@0.1u/16V_4
LAN_N4 C664 *55@1000p/50V_4 C648 *55@0.1u/16V_4 C652 *55@1000p/50V_4

12/22 cost down remove LAN eeprom
stuff R381
remove U21,R380,R378

+3V_S5
R380 *4.7K_4
R378 *4.7K_4
U21 *24LC08
SDA SCL A0 A1 A2 WP GND VCC
VPD_DATA
VPD_CLK
R381 0_4
+3V_S5

EEPROM No Use
VPD_DATA Pull Down

Foxconn JM36111-R2125-7F P/N : DFTJ12FR015

CN28
+3V_S5 R204 220_4 LAN_ACTLED# LAN_VCC3
C561 470p/50V_4 LAN_ACTLED#
C602 470p/50V_4 LAN_LINKLED#
C567 470p/50V_4 +3V_S5

X-TX3N
X-TX3P
X-TX1N
X-TX2N
X-TX2P
X-TX1P
X-TX0N
X-TX0P

NC4/3-
NC3/3+
RX-/1-
NC2/2-
NC1/2+
RX+/1+
TX-/0-
TX+/0+
GND
GND

R502 0_8
R554 0_8

+3V_S5 R552 220_4 LAN_LINKLED# LAN_VCC4
G-
G+
RJ45-CONN

1/17 Change CN28 (RJ45 CONN) from DFTJ12FR024 to DFTJ12FR035
1/18 Change RJ45 footprint from LAN-100073FR012G101ZL-12P to rj45-c100s7-10806-1-12P

Change CN9001 to BU1 LAN Connector

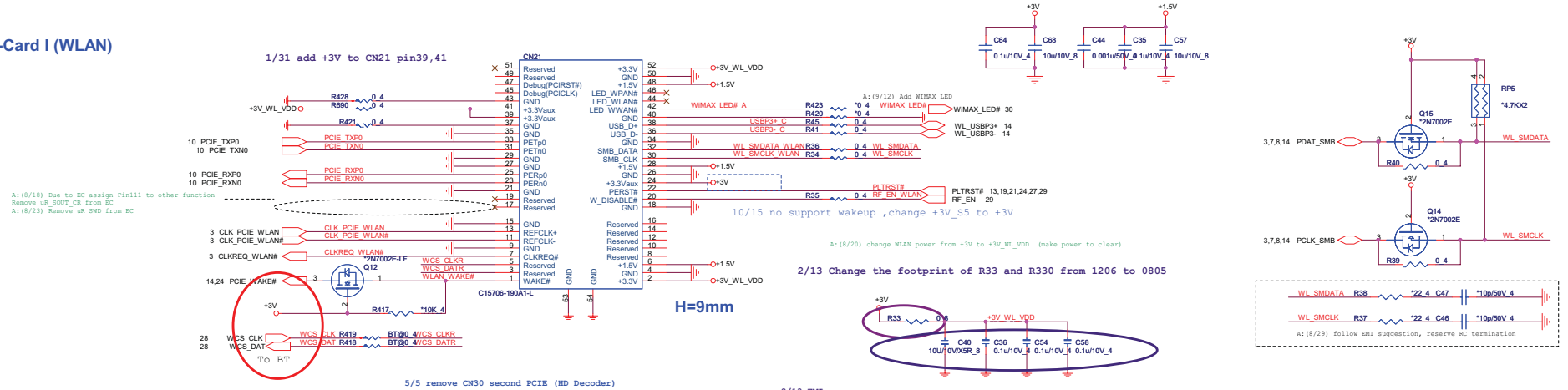
Rev05 modify 2007/08/16

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	LAN_Marvell_8040/8055	2A

Date: Thursday, May 29, 2008 Sheet 24 of 42

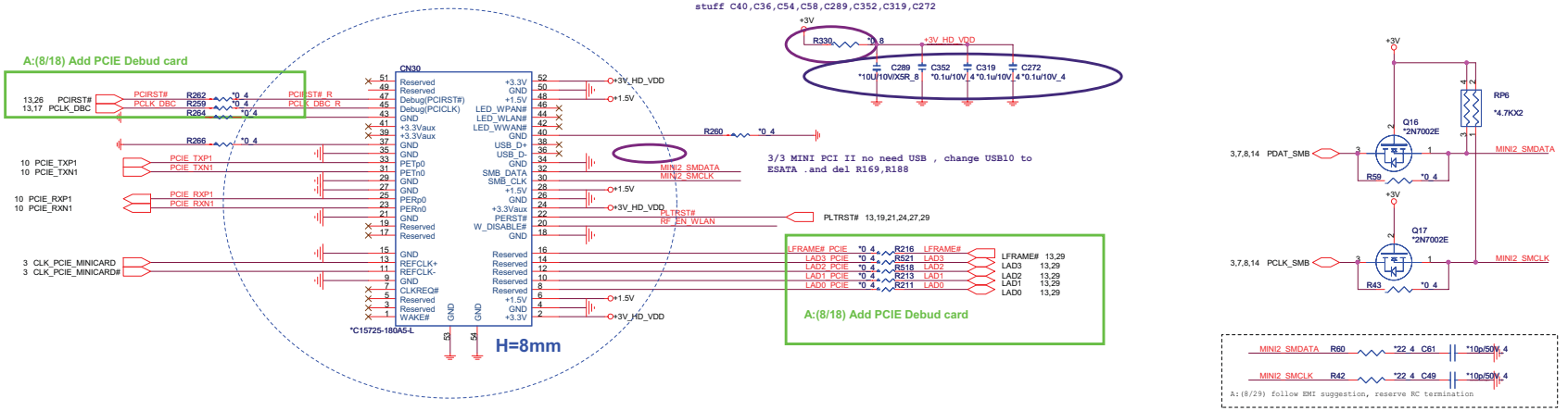
MINI-Card I (WLAN)



5/5 remove CN30 second PCIE (HD Decoder)

2/13 EMI
stuff C40,C36,C54,C58,C289,C352,C319,C272

MINI-Card II (HD Decoder)



A:(9/7) per TI FAE suggestion:
(1)Please keep all Input and Output capacitor value > 4.8uF (0.1uF +4.7uF)
(2)Please put these caps closed to IC
(3)R4101(pin 19,OC#) value should change to 2k ohm.

12/10 Change New card footprint to NCARD-13180151-T-26P-L-BL5F

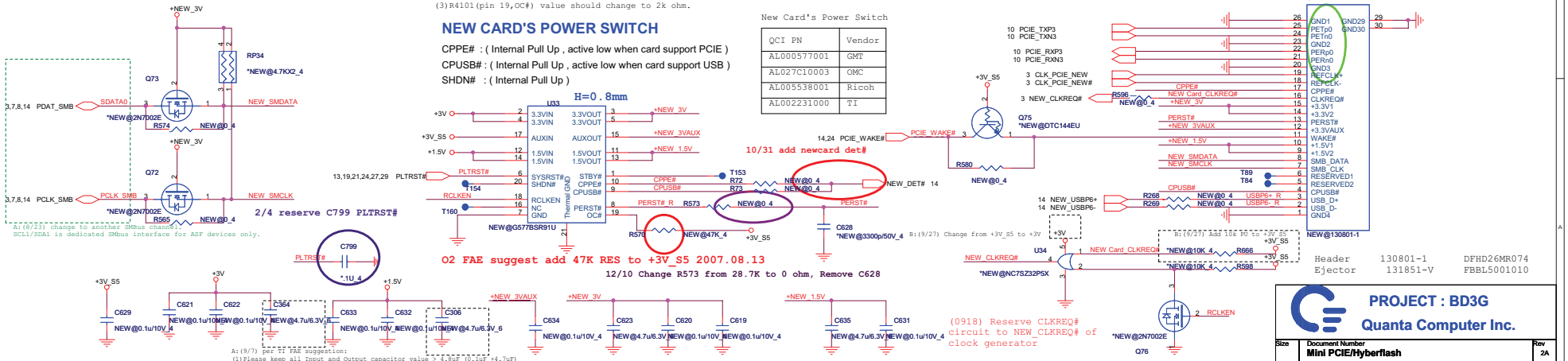
New card

NEW CARD'S POWER SWITCH

CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)

New Card's Power Switch

QCI PN	Vendor
AL000577001	GMT
AL027C10003	OMC
AL005538001	Ricoh
AL002231000	TI



PROJECT : BD3G			
Quanta Computer Inc.			
Size	Document Number: Mini PCIE/Hyberflash		Rev: 2A
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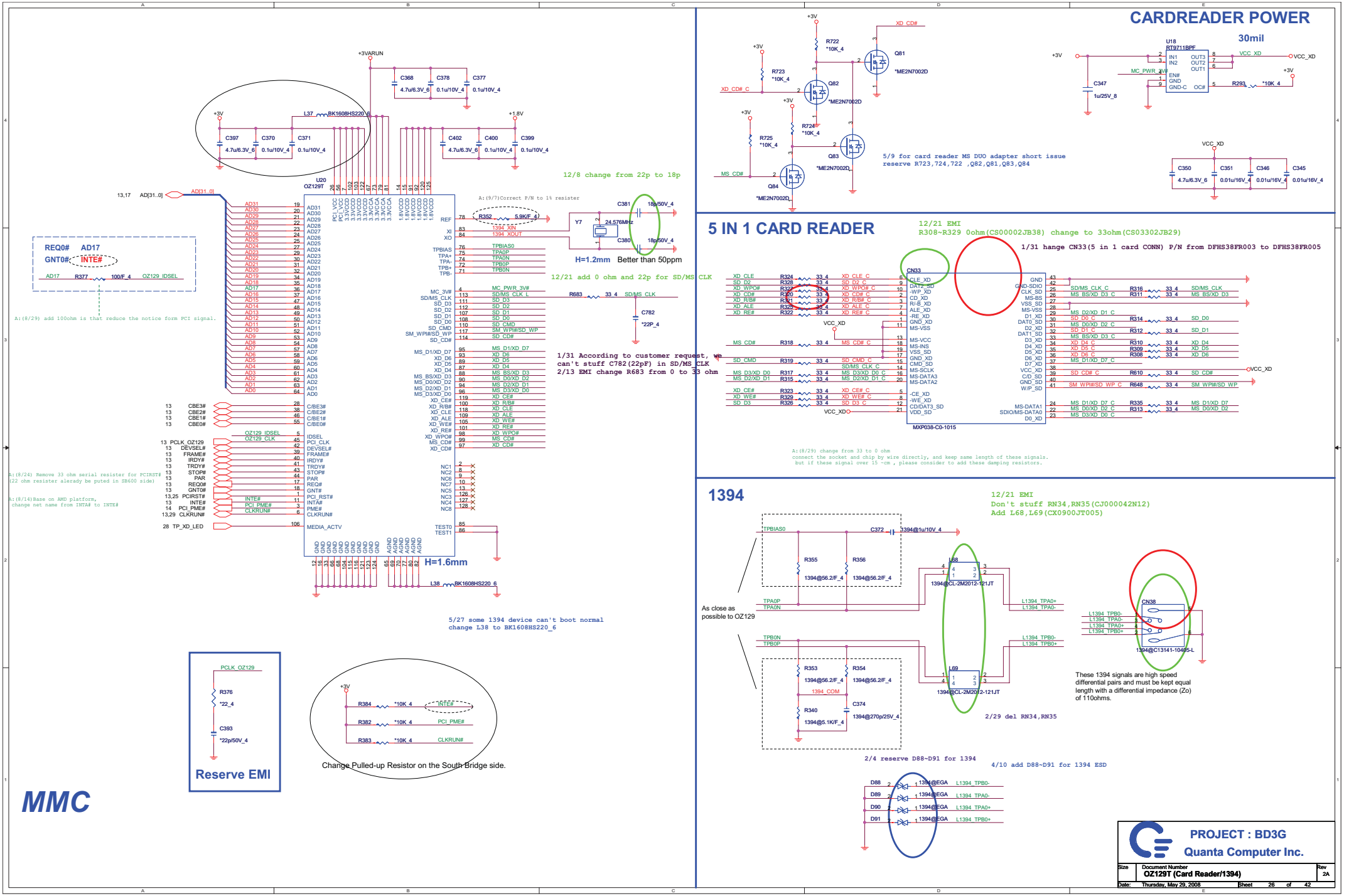
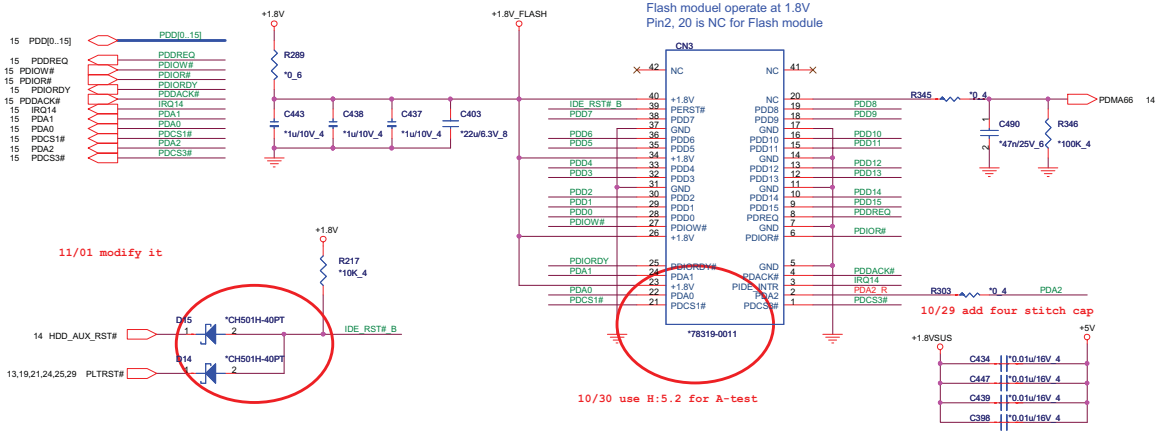

MMC
CARDREADER POWER
30mil
5 IN 1 CARD READER
1394
Reserve EMI
PROJECT : BD3G
Quanta Computer Inc.
OZ129T (Card Reader/1394)
Rev 2A
Date: Thursday, May 29, 2008
Sheet 26 of 42
5/9 for card reader MS DUO adapter short issue reserve R723,724,722 ,Q82,Q81,Q83,Q84
12/8 change from 22p to 18p
H=1.2mm Better than 50ppm
12/21 add 0 ohm and 22p for SD/MS CLK
1/31 According to customer request, we can't stuff C782(22pF) in SD/MS_CLK
2/13 EMI change R683 from 0 to 33 ohm
H=1.6mm
5/27 some 1394 device can't boot normal change L38 to BK1608HS220_6
Change Pulled-up Resistor on the South Bridge side.
12/21 EMI
R308~R329 0ohm(CS00002JB38) change to 33ohm(CS03302JB29)
1/31 hange CN33(5 in 1 card CONN) P/N from DFHS38FR003 to DFHS38FR005
12/21 EMI
Don't stuff RN34,RN35(CJ000042N12)
Add L68,L69(CX0900JT005)
As close as possible to OZ129
These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.
2/29 del RN34,RN35
2/4 reserve D88~D91 for 1394
4/10 add D88~D91 for 1394 ESD

FLASH

4/10 remove Flash card ckt

Flash moduel operate at 1.8V
Pin2, 20 is NC for Flash module



11/01 modify it

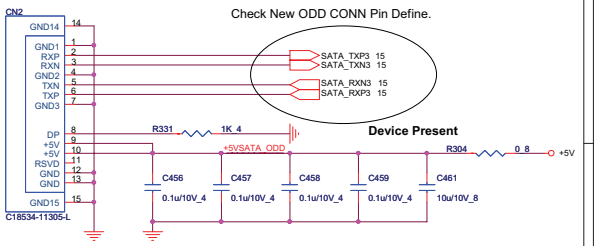
10/30 use H:5.2 for A-test

10/29 add four stitch cap

SATA ODD

9/28 change to SATA ODD conn to BD3G use

10/22 update footprint to SATA-C18534-11305-13P-R



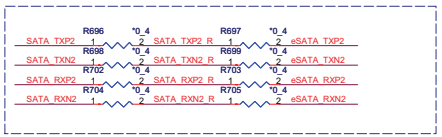
ESATA

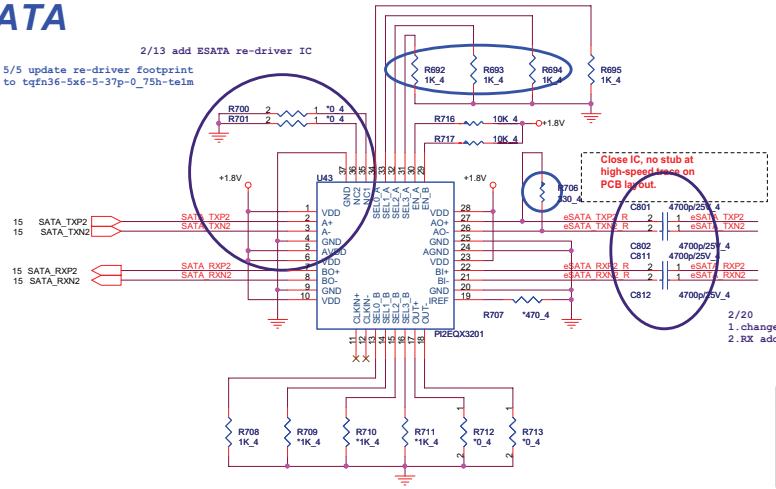
4/14 change R706 from 0 ohm to 330 , stuff R692,R693,R694

2/13 add ESATA re-driver IC

5/5 update re-driver footprint
to tqfn36-5x6-5-37p-0_75h-telm

Option SB to ESATA directly





2/20
1.change C801,C82 from 0.01u to 4.7n
2.RX add C811,C812 4.7n

SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				

Co-lay ESATA footprint

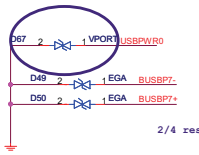
2/29 del R572,R569

2/26 change ESATA conn usb-2006109-11p
update p/n to DFHS11FR021

4/10 change ESATA conn usb-2006109-11p
update p/n to DFHS11FR023

4/10 add D67,D49,D50 for ESATA USB ESD

5/29 change ESATA conn p/n to DFHS11FR027

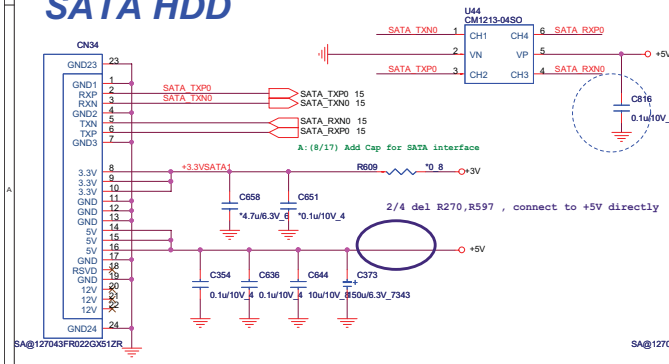


2/4 reserve D67 for CN31

4/17 remove D77~D81 for CN34 , change to U44 CM1213-04SO

5/5 add C816 0.01u to U44 +5V for ESD

SATA HDD



2/4 del R270,R597 , connect to +5V directly

2'nd SATA HDD

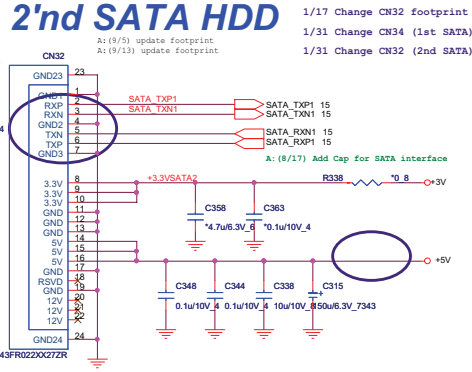
A:(9/5) update footprint
A:(9/13) update footprint

1/17 Change CN32(2nd SATA CONN) from DFHS22FR064 to DFHS22FR094

1/17 Change CN32 footprint from SATA-127043FR022XX27ZR-22P-L-H to SATA-127043FR022G285ZR-22P-L

1/31 Change CN34 (1st SATA) P/N from DFHS22FR063 to DFHS22FR082

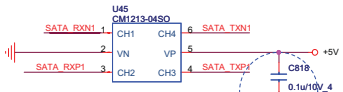
1/31 Change CN32 (2nd SATA) P/N from DFHS22FR094 to DFHS22FR083



2/4 reserve D82~D86 for CN32(2ND HDD)

4/17 remove D82~D86 for CN32 , change to U45 CM1213-04SO

5/5 add C818 0.01u to U45 +5V for ESD



PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	SATA / PATA	2A
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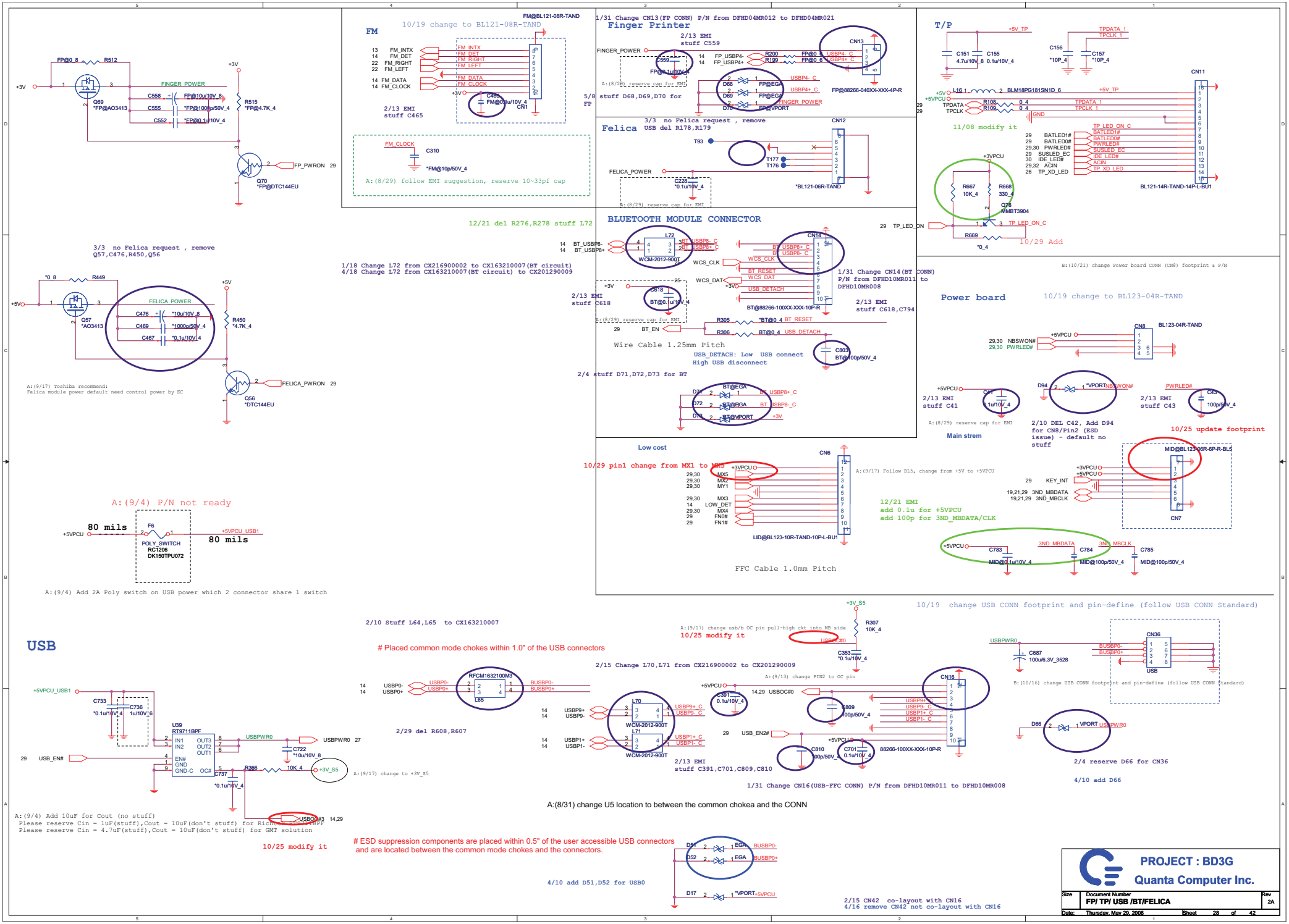
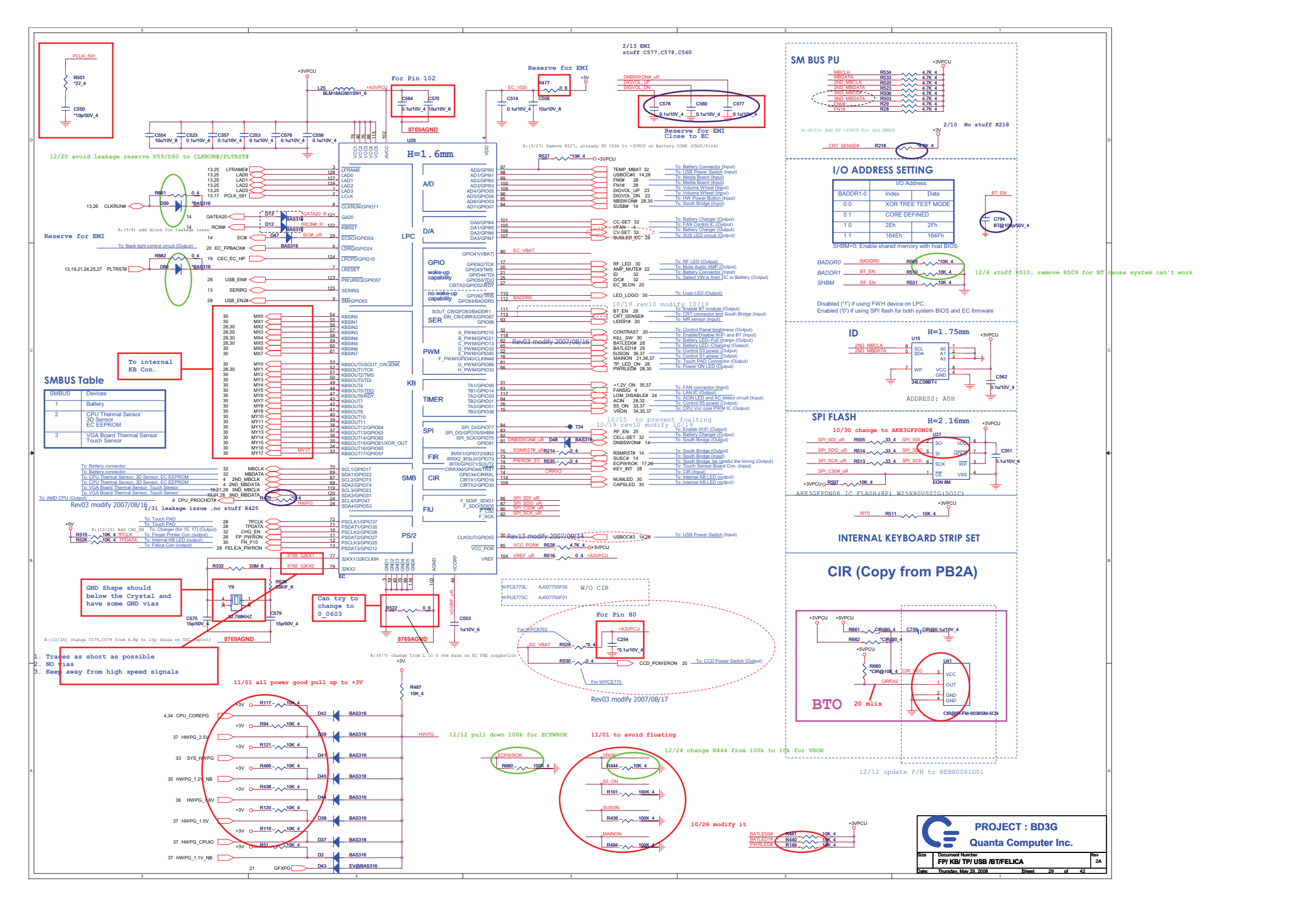
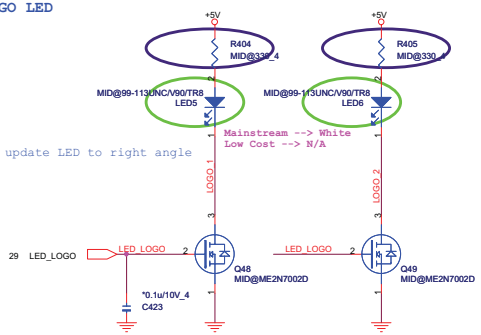

FM
10/19 change to BL121-08R-TAND
FM@BL121-08R-TAND
FM_INTX
FM_DET
FM_RIGHT
FM_LEFT
FM_DATA
FM_CLOCK
2/13 EMI stuff C465
FM_CLOCK
C310
*FM@10p/50V_4
A:(8/29) follow EMI suggestion, reserve 10~33pf cap
Finger Printer
1/31 Change CN13(FP CONN) P/N from DFHD04MR012 to DFHD04MR021
2/13 EMI stuff C559
FINGER_POWER
C559
FP@4.1u/10V_4
A:(8/29) reserve cap for EMI
FP_USBP4-
FP_USBP4+
R200
R199
FP@0_6
USBP4- C
USBP4+ C
CN13
D68
D69
D70
FP@EGA
FP@VPORT
5/8 stuff D68,D69,D70 for FP
FP@88266-040XX-XXX-4P-R
Felica
3/3 no Felica request , remove USB del R178,R179
T93
T177
T176
FELICA_POWER
C220
*0.1u/10V_4
CN12
*BL121-08R-TAND
A:(8/29) reserve cap for EMI
T/P
+5V_TP
C151
4.7u/10V_8
C155
0.1u/10V_4
C156
*10P_4
C157
*10P_4
TPDATA_1
TPCLK_1
L16
BLM18PG181SN1D_6
R108
R109
0_4
GND
11/08 modify it
TP_LED_ON_C
BATLED1#
BATLED0#
PWRLED#
SUSLED_EC
IDE_LED#
ACIN
TP_XD_LED
CN11
BL121-14R-TAND-14P-L-BU1
+3VPCU
R667
10K_4
R668
330_4
Q28
MMBT3904
R669
*0_4
10/29 Add
12/21 del R276,R278 stuff L72
BLUETOOTH MODULE CONNECTOR
L72
WCM-2012-900T
BT_USBP8-
BT_USBP8+
BT_USBP8- C
BT_USBP8+ C
CN14
WCS_CLK
WCS_DAT
BT_RESET
USB_DETACH
BT@88266-100XX-XXX-10P-R
1/31 Change CN14(BT CONN) P/N from DFHD10MR011 to DFHD10MR008
2/13 EMI stuff C618,C794
C618
BT@0.1u/10V_4
R305
*BT@0_4
R306
BT@0_4
BT_EN
C803
BT@100p/50V_4
Wire Cable 1.25mm Pitch
USB_DETACH: Low USB connect
High USB disconnect
2/4 stuff D71,D72,D73 for BT
D71
D72
D73
BT@EGA
BT@VPORT
3/3 no Felica request , remove Q57,C476,R450,Q56
R449
*0_8
Q57
*AO3413
FELICA_POWER
C476
*10u/10V_8
C469
*1000p/50V_4
C467
*0.1u/10V_4
R450
*4.7K_4
Q56
*DTC144EU
FELICA_PWRON
A:(9/17) Toshiba recommend:
Felica module power default need control power by EC
Power board
10/19 change to BL123-04R-TAND
B:(10/21) change Power board CONN (CN8) footprint & P/N
CN8
BL123-04R-TAND
NBSWON#
PWRLED#
2/13 EMI stuff C41
C41
0.1u/10V_4
D94
*VPORT
NBSWON#
2/13 EMI stuff C43
C43
100p/50V_4
A:(8/29) reserve cap for EMI
Main strem
2/10 DEL C42, Add D94 for CN8/Pin2 (ESD issue) - default no stuff
10/25 update footprint
MID@BL123-06R-6P-R-BL5
CN7
Low cost
10/29 pin1 change from MX1 to MX5
CN6
MX5
MX2
MX1
MX3
LOW_DET
MX4
FN0#
FN1#
LID@BL123-10R-TAND-10P-L-BU1
A:(9/17) Follow BL5, change from +5V to +5VPCU
12/21 EMI add 0.1u for +5VPCU add 100p for 3ND_MBDATA/CLK
KEY_INT
3ND_MBDATA
3ND_MBCLK
C783
C784
C785
MID@0.1u/10V_4
MID@100p/50V_4
FFC Cable 1.0mm Pitch
A:(9/4) P/N not ready
80 mils
F6
POLY_SWITCH
RC1206
DK150TPU072
+5VPCU_USB1
A:(9/4) Add 2A Poly switch on USB power which 2 connector share 1 switch
USB
2/10 Stuff L64,L65 to CX163210007
Placed common mode chokes within 1.0" of the USB connectors
2/29 del R608,R607
RFCM1632100M3
L65
USBP0-
USBP0+
BUSBP0-
BUSBP0+
2/15 Change L70,L71 from CX216900002 to CX201290009
L70
L71
WCM-2012-900T
USBP9+ C
USBP9- C
USBP1+ C
USBP1- C
2/13 EMI stuff C391,C701,C809,C810
C391
0.1u/10V_4
C809
100p/50V_4
C810
C701
88266-100XX-XXX-10P-R
1/31 Change CN16(USB-FFC CONN) P/N from DFHD10MR011 to DFHD10MR008
CN16
USBOC#0
USB_EN2#
A:(9/13) change PIN2 to OC pin
10/19 change USB CONN footprint and pin-define (follow USB CONN Standard)
CN36
USB
USBPWR0
C687
100u/6.3V_3528
B:(10/16) change USB CONN footprint and pin-define (follow USB CONN Standard)
D66
VPORT
2/4 reserve D66 for CN36
4/10 add D66
A:(9/17) change usb/b OC pin pull-high ckt into MB side
10/25 modify it
R307
10K_4
C353
*0.1u/10V_4
U39
RT9711BPF
IN1
IN2
EN#
GND
GND-C
OC#
OUT3
OUT2
OUT1
C733
*0.1u/10V_4
C736
1u/10V_6
C722
*10u/10V_8
R366
10K_4
C737
*0.1u/10V_4
USBOC#3
A:(9/17) change to +3V_S5
A:(9/4) Add 10uF for Cout (no stuff)
Please reserve Cin = 1uF(stuff),Cout = 10uF(don't stuff) for Richtek RT9711BPF
Please reserve Cin = 4.7uF(stuff),Cout = 10uF(don't stuff) for GMT solution
10/25 modify it
A:(8/31) change U5 location to between the common chokea and the CONN
ESD suppression components are placed within 0.5" of the user accessible USB connectors and are located between the common mode chokes and the connectors.
4/10 add D51,D52 for USB0
D51
D52
D17
EGA
VPORT
2/15 CN42 co-layout with CN16
4/16 remove CN42 not co-layout with CN16
PROJECT : BD3G
Quanta Computer Inc.
Size
Document Number
FP/ TP/ USB /BT/FELICA
Rev
2A
Date: Thursday, May 29, 2008
Sheet 28 of 42


SMBUS Table
SMBUS | Devices
1 | Battery
2 | CPU Thermal Sensor 3D Sensor EC EEPROM
3 | VGA Board Thermal Sensor Touch Sensor
To internal KB Con.
H=1.6mm
LPC
A/D
D/A
GPIO
SER
PWM
KB
TIMER
SPI
FIR
CIR
SMB
FIU
PS/2
EC
Reserve for EMI
For Pin 102
8769AGND
12/20 avoid leakage reserve D59/D60 to CLKRUN#/PLTRST#
Rev03 modify 2007/08/16
1/31 leakage issue ,no stuff R425
GND Shape should below the Crystal and have some GND vias
Can try to change to 0_0603
1. Traces as short as possible
2. NO vias
3. Keep away from high speed signals
11/01 all power good pull up to +3V
12/12 pull down 100k for ECPWROK
11/01 to avoid floating
12/24 change R444 from 100k to 10k for VRON
10/26 modify it
2/13 EMI stuff C577,C578,C560
Reserve for EMI Close to EC
SM BUS PU
2/10 No stuff R218
I/O ADDRESS SETTING
SHBM=0: Enable shared memory with host BIOS
12/4 stuff R510, remove R509 for BT cause system can't work
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
ID
H=1.75mm
ADDRESS: A0H
SPI FLASH
H=2.16mm
10/30 change to AKE3GFP0N08
AKE3GFP0N08 IC FLASH(8P) W25X80VSSIG(SOIC)
INTERNAL KEYBOARD STRIP SET
CIR (Copy from PB2A)
BTO
20 mils
12/12 update P/N to BEBK0081D01
WPCE775L: AJ007750F00 W/O CIR
WPCE775C: AJ007750F01
PROJECT : BD3G
Quanta Computer Inc.
Size | Document Number | Rev
FP/ KB/ TP/ USB /BT/FELICA | 2A
Date: Thursday, May 29, 2008 | Sheet 29 of 42

2/1 Change R404,R405 from CS13902JB14 (390 ohm) to CS13302JB21(330 ohm)

LOGO LED

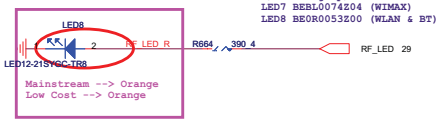


10/16 update LED to right angle

W-LAN&BT

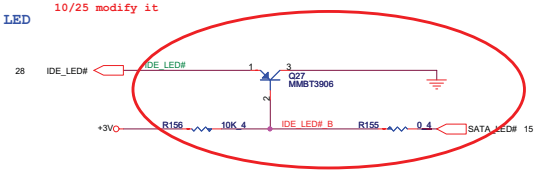
1/18 LED7,8 change footprint from LED12-21SYGC-TR8 to LED27-21-BHC-ZL1M2TY-3C

1/18 change p/n
LED7 BEBL0074Z04 (WIMAX)
LED8 BE0R0053Z00 (WLAN & BT)

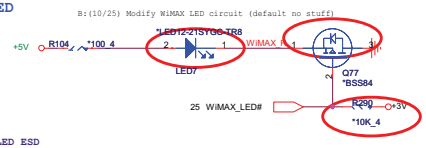


IDE LED

10/25 modify it



WiMAX LED



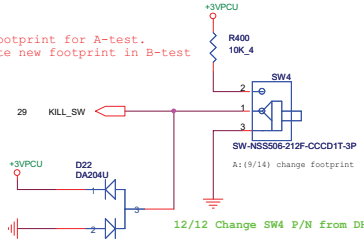
5/8 stuff D53 for RF_LED ESD

12/7 change LED5,LED6 footprint and p/n

Kill SW

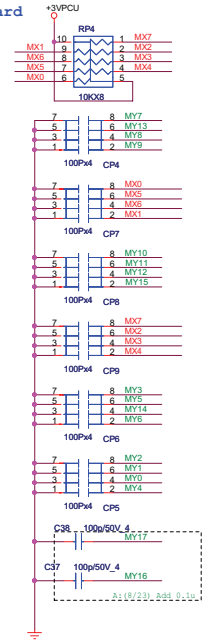
1/18 Change SW4 footprint from SW-NSS506-212F-CCCD1T-3P to SW-NSS506-212F-CCCD1T-3P-BD3A (SMT open issue)

Use old footprint for A-test.
Must update new footprint in B-test



12/12 Change SW4 P/N from DHL00212F05 to DHL00212F07

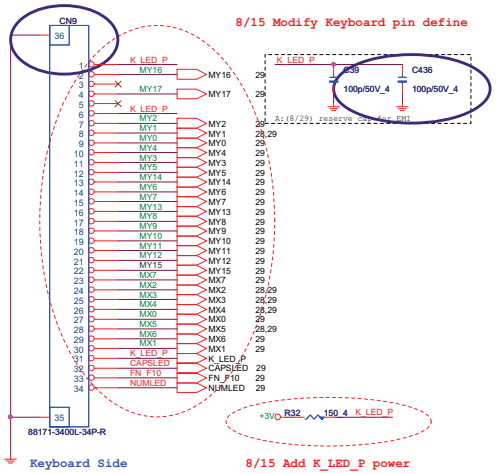
Keyboard



1/18 change footprint from 88171-3400L-34P-L to 91504-340N-34P-L

8/15 Modify Keyboard pin define

2/13 EMI
stuff C39,C436

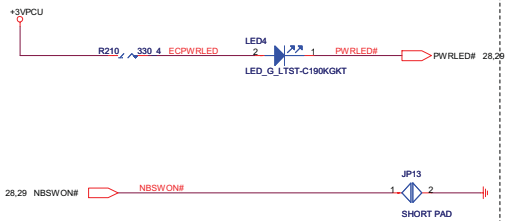


Keyboard Side

8/15 Add K_LED_P power

1/17 Remove CN10 (Keyboard CONN)

Jumper & LED (debug use)



A:(8/27) Confirm with EC FAE,
MY no need External PU resister

	15"	17"
CAPSLED K_LED_P (Pin 31)	V	V
FN_F10 K_LED_P (Pin 6)	V	
NUMLED K_LED_P (Pin 1)	V	V

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	SW/LED/KEYBOARD	2A
Date: Thursday, May 29, 2008	Sheet 30 of 42	

HOLE

Take care NUT P/N base on IV/EV sku

1/18 HOLE 17,18.23 FBBL5004010
change to FBBL5002010

VGA NUT

(BOT)

HOLE15 H-TC315BC236D146P2
HOLE24 H-C236D146P2
HOLE25 H-C236D146P2

10/31 EMI request

2/18 HOLE 15,24.25 FBBD3017010
change to FBBD3021010

MDC NUT

(BOT)

HOLE32 MD@H-C236D146P2

CPU NUT

(BOT)

HOLE17 H-C236D146P2
HOLE18 H-C236D146P2
HOLE23 H-C236D146P2

Mini-PCI-B NUT

(BOT)

HOLE13 H-C236D146P2
HOLE14 H-C236D146P2

2/18 HOLE 13,14 FBBL5008010
change to FBBL5051010

Mini-PCI-A NUT

(BOT)

HOLE28 *H-C236D126P2
HOLE35 *H-C236D126P2

B:(10/17) update footprint

2/18 HOLE 28.35 FBBL5007010
change to FBBL5050010

5/5 remove HOLE28,35 (HD Decoder)

B:(10/17) update footprint

KB NUT

(TOP)

HOLE5 H-C236D146P2
HOLE6 H-C236D146P2

E-SATA NUT

(BOT)

4/21 remove Hole31,37

HOLE30 *H-C236D91P2
HOLE38 *H-C236D91P2
HOLE8 *H-C216D91P2
HOLE9 *H-C216D91P2
HOLE22 *H-C216D91P2
HOLE34 *H-C216D91P2
HOLE39 *H-C216D91P2
HOLE16 *H-CT315

A:(9/17) Base ON EMI mail(9/13) Item5

HOLE33 *h-sped110p2
HOLE26 *H-C216D91P2
HOLE40 *H-SPED118P2

A:(9/12) Base ON EMI mail(9/13) Item1

10/24 update footprint

B:(10/17) update footprint

HOLE44 *H-TS315BC295D118P2-8
HOLE43 *H-TS8C315D118P2-8

HOLE42 *H-C276D118P2-8
HOLE41 *H-C335D118P2-8
HOLE19 *H-C335D118P2-8
HOLE4 *H-C335D118P2-8
HOLE7 *H-C335D146P2-8
HOLE12 *H-C335D118P2-8
HOLE10 *H-C335D118P2-8
HOLE11 *H-C315D118P2-8

B:(10/17) update footprint

HOLE36 *H-C335D118P2-8
HOLE27 *H-C335I248D118P2-8
HOLE29 *H-C335D118P2-8
HOLE21 *H-C335D118P2-8
HOLE20 *H-C335D118P2-8

R85 0_8

10/31 EMI request

RAMP:(1/16) Follow BL5, update Hole footprint (13pcs)

NUT P/N Control Table

	UMA sku	EV sku
HOLE15	FBBL5002010	FBBD3021010
HOLE24	FBBL5002010	FBBD3021010
HOLE25	FBBL5002010	FBBD3021010

Stitch CAP

CPU_CORE0

C134 0.01u/16V_4
C133 0.01u/16V_4
C130 0.01u/16V_4
C135 0.01u/16V_4

For fix HyperTransport nets across plane splits

4/17 update HOLE13,14 footprint to H-C236D146P2

VIN

C768 C769 C770 C771 C772 C773 C774 C775 C776 C777 C778 C779 C780 C781
0.1u/10V_4

EMI CAP.

VIN

C746 C63 0.1u/10V_4
C87 C137 C106 C97 C119 0.1u/10V_4
C169 0.1u/10V_4

VIN

C529 C270 C472 C758 C755 C756 C31 C30 C74
0.1u/10V_4

+3V

C244 C243 C204 C202 C162 C138 C749 C112 C742
0.1u/10V_4

+3V

C12 C85 C2 C416 C451 C1 C71 C72 C50 C62
0.1u/10V_4

+3V

C450 C454 C224 C480 C409 C460 C455
0.1u/10V_4

+3VPCU

C240 C549
0.1u/10V_4

+3VSUS

C229 C518 C128
*0.1u/10V_4

+5VPCU

C83 C161 C132 C165 C760 C205
0.1u/10V_4

3/3 EMI request add C813,C814

+5V

C464 C745 C51 C3 C759 C59
0.1u/10V_4

+1.5V

C813 C814
0.1u/10V_4

+3VPCU

C164 C547 C122 C748 C32 C33 C75 C34 C70
0.1u/10V_4

+1.8V

C273 C213 C574 C107 C146
0.1u/10V_4

+1.2V

C528 C163 C127 C585 C584
0.1u/10V_4

+5V

C139 C271 C462 C442 C171
0.1u/10V_4

+5VPCU

C16 C757 C45
0.1u/10V_4

+1.8V

C599 C385 C283 C203 C189 C176 C173 C153
0.1u/10V_4

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	HOLE/EMI CAP/ESD PAD	2A
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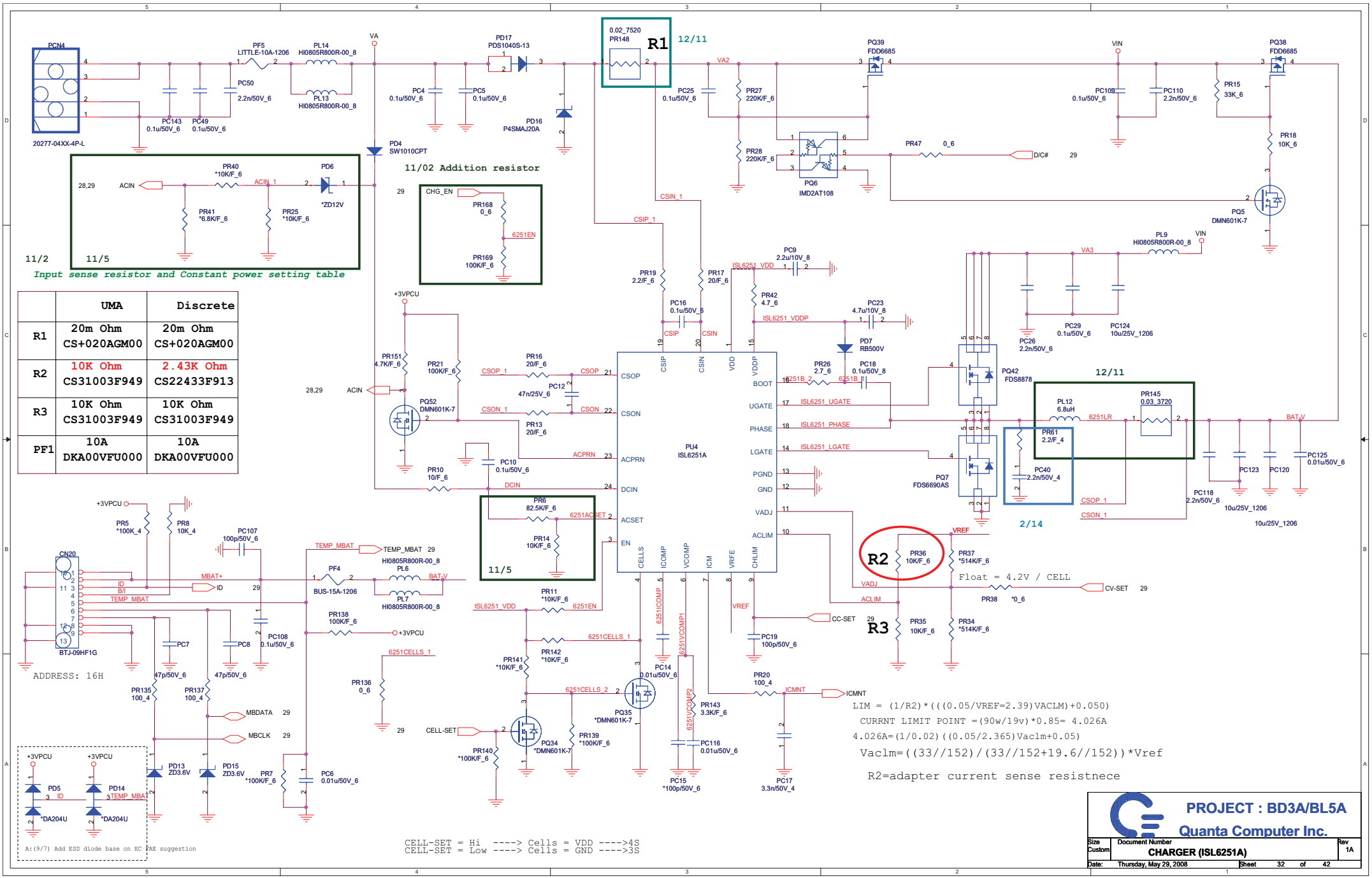

	UMA	Discrete
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	10K Ohm CS31003F949	2.43K Ohm CS22433F913
R3	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000

PROJECT : BD3A/BL5A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER (ISL6251A)	1A
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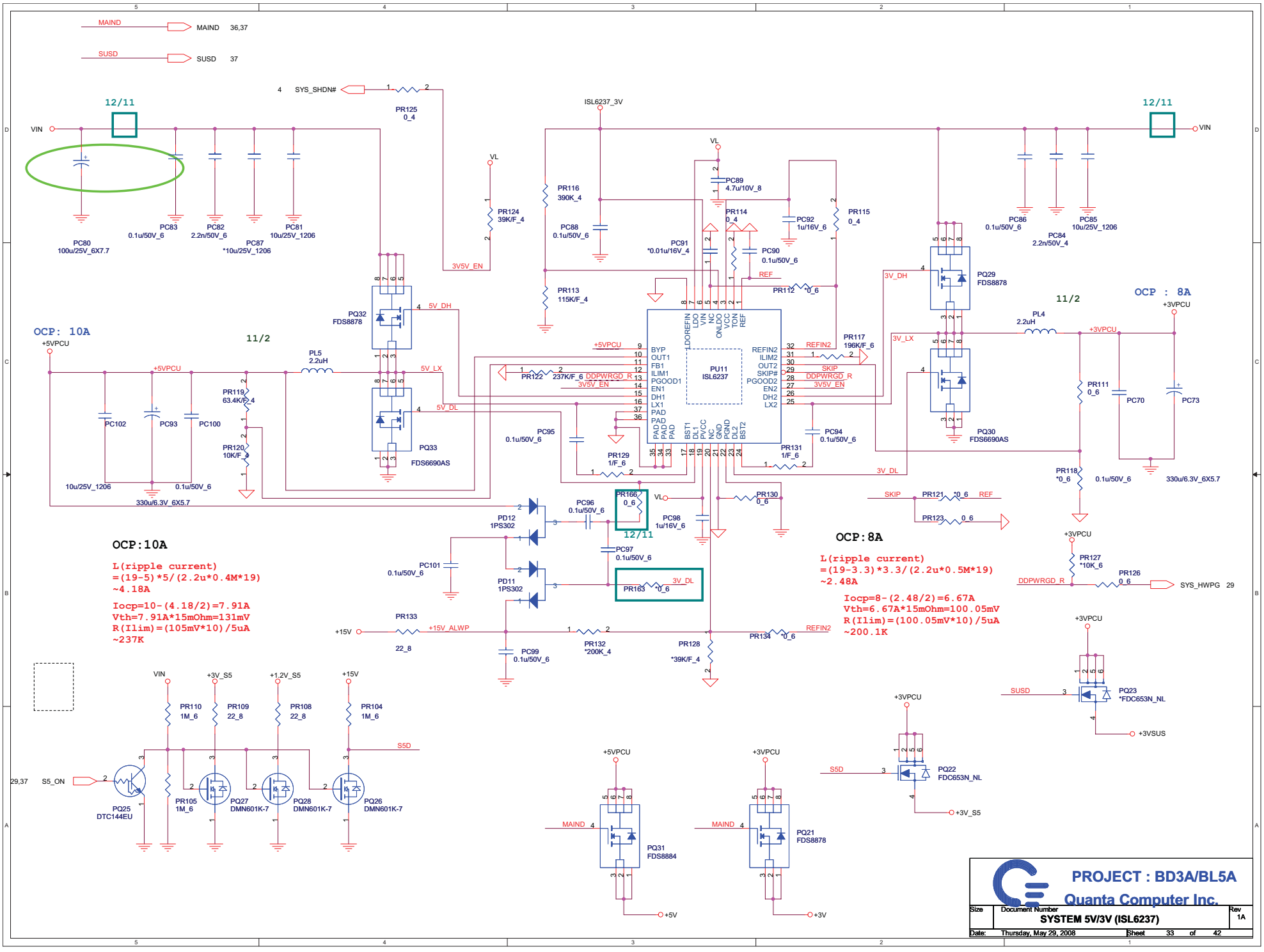
MAIND
MAIND 36,37
SUSD
SUSD 37
4 SYS_SHDN#
PR125 0_4
12/11
VIN
PC80 100u/25V_6X7.7
PC83 0.1u/50V_6
PC82 2.2n/50V_6
PC87 *10u/25V_1206
PC81 10u/25V_1206
VL
PR124 39K/F_4
3V5V_EN
ISL6237_3V
PR116 390K_4
PC88 0.1u/50V_6
PC89 4.7u/10V_8
PR114 0_4
PC92 1u/16V_6
PR115 0_4
PC91 *0.01u/16V_4
PC90 0.1u/50V_6
REF
PR112 *0_6
PR113 115K/F_4
PC86 0.1u/50V_6
PC84 2.2n/50V_4
PC85 10u/25V_1206
12/11
VIN
OCP: 10A
11/2
+5VPCU
PL5 2.2uH
5V_LX
5V_DH
5V_DL
PQ32 FDS8878
PQ33 FDS6690AS
PR119 63.4K/F_4
PR120 10K/F
PC102
PC93
PC100
10u/25V_1206
0.1u/50V_6
330u/6.3V_6X5.7
PC95 0.1u/50V_6
PR122 237K/F_6 DDPWRGD_R
3V5V_EN
PU11 ISL6237
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND DL2 BST2
PR117 196K/F_6
PR129 1/F_6
PR131 1/F_6
PC94 0.1u/50V_6
3V_DH
3V_LX
3V_DL
PQ29 FDS8878
PQ30 FDS6690AS
OCP : 8A
11/2
+3VPCU
PL4 2.2uH
PR111 0_6
PC70
PC73
330u/6.3V_6X5.7
PR118 *0_6
0.1u/50V_6
SKIP
PR121 *0_6 REF
PR123 0_6
PR166 0_6
PC96 0.1u/50V_6
PC98 1u/16V_6
PR130 0_6
PD12 1PS302
PD11 1PS302
PC97 0.1u/50V_6
PC101 0.1u/50V_6
12/11
PR163 *0_6
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*15mOhm=131mV
R(Ilim)=(105mV*10)/5uA
~237K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA
~200.1K
PR127 *10K_6
PR126 0_6
DDPWRGD_R
SYS_HWPG 29
+15V
+15V_ALWP
PR133 22_8
PC99 0.1u/50V_6
PR132 *200K_4
PR128 *39K/F_4
PR134 *0_6
REFIN2
VIN
+3V_S5
+1.2V_S5
+15V
PR110 1M_6
PR109 22_8
PR108 22_8
PR104 1M_6
S5D
29,37 S5_ON
PQ25 DTC144EU
PR105 1M_6
PQ27 DMN601K-7
PQ28 DMN601K-7
PQ26 DMN601K-7
+5VPCU
MAIND
PQ31 FDS8884
+5V
+3VPCU
MAIND
PQ21 FDS8878
+3V
+3VPCU
S5D
PQ22 FDC653N_NL
+3V_S5
+3VPCU
SUSD
PQ23 *FDC653N_NL
+3VSUS
PROJECT : BD3A/BL5A
Quanta Computer Inc.
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev 1A
Date: Thursday, May 29, 2008
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

3A

CPU VDDNB_CORE

PL11 2.5uH

4 CPU_VDDNB_FB_H

4 CPU_VDDNB_FB_L

PR219 10/F_6

PR158 10/F_6

PC194 330u_2V_7343

PC103 10u/25V_1206

PR208 10/F_6

+5VPCU

PC134 1u/25V_8

PR214 0_8

PR198 10/F_6

VIN

PC166 0.1u/50V_6

PR211 22.1K/F_4

PC159 1000p/50V_6

PC163 33p/50V_4

PC114 1200p/50V_4

PR176 44.2K/F_4

PR209 0_4

PR179 0_4

2/14

PR217 11.3K/F_4

LGATE_NB

PHASE_NB

UGATE_NB

PC126 0.1u/50V_6

PR206 1/F_6

12/11

VIN

LGATE_NB

PQ48 SI4914

UGATE_NB

PC171 10u/25V_1206

PC140 10u/25V_1206

PC167 0.1u/50V_6

12/11

VIN

PC130 10u/25V_1206

PC160 10u/25V_1206

PC162 0.1u/50V_6

20A

11/2 TOKIN

PQ46 AOL1414

UGATE_0

PL17 0.36uH

CPU_CORE0

PR237 2.2/F_4

PC189 2.2n/50V_4

PR199 0_6

PR189 0_6

PC161 330u_2V_7343

PC105 330u_2V_7343

PQ43 AOL1412

ISP_0

ISN_0

2/14

PR162 1/F_6

PC113 0.1u/50V_6

PC141 2.2u/10V_6

+5VPCU

VIN

PC112 10u/25V_1206

PC147 10u/25V_1206

PC157 0.1u/50V_6

20A

11/2 TOKIN

PQ37 AOL1414

UGATE_1

PL16 0.36uH

CPU_CORE1

PR238 2.2/F_4

PC190 2.2n/50V_4

PR203 0_6

PR201 0_6

PC135 330u_2V_7343

PC165 330u_2V_7343

PQ41 AOL1412

LGATE_1

2/14

PR202 1/F_6

PC164 0.1u/50V_6

12/11

+5VPCU

+3V

PR181 0_4

PR182 *0_4

PR192 *10K/F_4

PR188 0_4

4,29 CPU_COREPG

+1.8V

+3V

PQ51 DTC144EU

PR234 10K_6

4 CPU_PWRGD_SVID_REG

PR235 *0_4

4 CPU_SVD

4 CPU_SVC

29,35,37 VRON

PR190 0_4

PR195 0_4

PR191 0_4

PR185 0_4

PR218 107K/F_4

PR157 10K/F_4

5/5

PR196 255/F_4

PC158 4700p/25V_4

PR210 1K/F_4

PR200 54.9K/F_4

PC111 1200p/50V_4

PC106 180p/50V_4

PR177 6.81K/F_4

PC122 1000p/50V_6

Pin 49 is GND Pin

PU3 ISL6265

Pin	Name	Pin	Name
49	GND	36	BOOT_NB
48	VIN	35	BOOT_0
47	VCC	34	UGATE_0
46	FB_NB	33	PHASE_0
45	COMP_NB	32	PGND_0
44	FSET_NB	31	LGATE_0
43	VSEN_NB	30	PVCC
42	RTN_NB	29	LGATE_1
41	OCSET_NB	28	PGND_1
40	PGND_NB	27	PHASE_1
39	LGATE_NB	26	UGATE_1
38	PHASE_NB	25	BOOT_1
37	UGATE_NB		
1	OFS/VFIXEN		
2	PGOOD		
3	PWROK		
4	SVD		
5	SVC		
6	ENABLE		
7	RBIAS		
8	OCSET		
9	VDIFF_0		
10	FB_0		
11	COMP_0		
12	VW_0		
13	ISP_0	24	ISN_1
14	ISN_0	23	ISP_1
15	VSEN_0	22	VW_1
16	RTN_0	21	COMP_1
17	RTN_1	20	FB_1
18	VSEN_1	19	VDIFF_1

Close to CPU socket

5/27

ISP_0

ISN_0

PR160 3.92K/F_4

PR213 18.2K/F_4

PC172 0.1u/50V_6

PR178 0_4

PR207 0_4

PR187 0_4

PR186 0_4

CPU_CORE0

PR212 10/F_6

4 CPU_VDD0_FB_H

4 CPU_VDD0_FB_L

PR194 10/F_6

Parallel

PC173 0.1u/50V_6

PR205 6.81K/F_4

PC104 1000p/50V_6

ISN_1

ISP_1

PR215 18.2K/F_4

PR216 3.92K/F_4

5/27

Close to CPU socket

PR184 10/F_6

4 CPU_VDD1_FB_L

4 CPU_VDD1_FB_H

CPU_CORE1

PR183 10/F_6

PC142 4.7n/25V_4

PR204 255/F_4

PR197 1K/F_4

PC170 1200p/50V_4

PC168 180p/50V_4

PR180 54.9K/F_4

12/18

CPU_CORE1

CPU_CORE0

CPU VDDNB_CORE

PC191 330u_2V_7343

PC193 330u_2V_7343

PC169 *330u_2V_7343

2/14

4/10 add PC191,PC193

PROJECT : BD3A/BL5A

Quanta Computer Inc.

Size	Document Number	Rev
C	OZ826 CPU	1A

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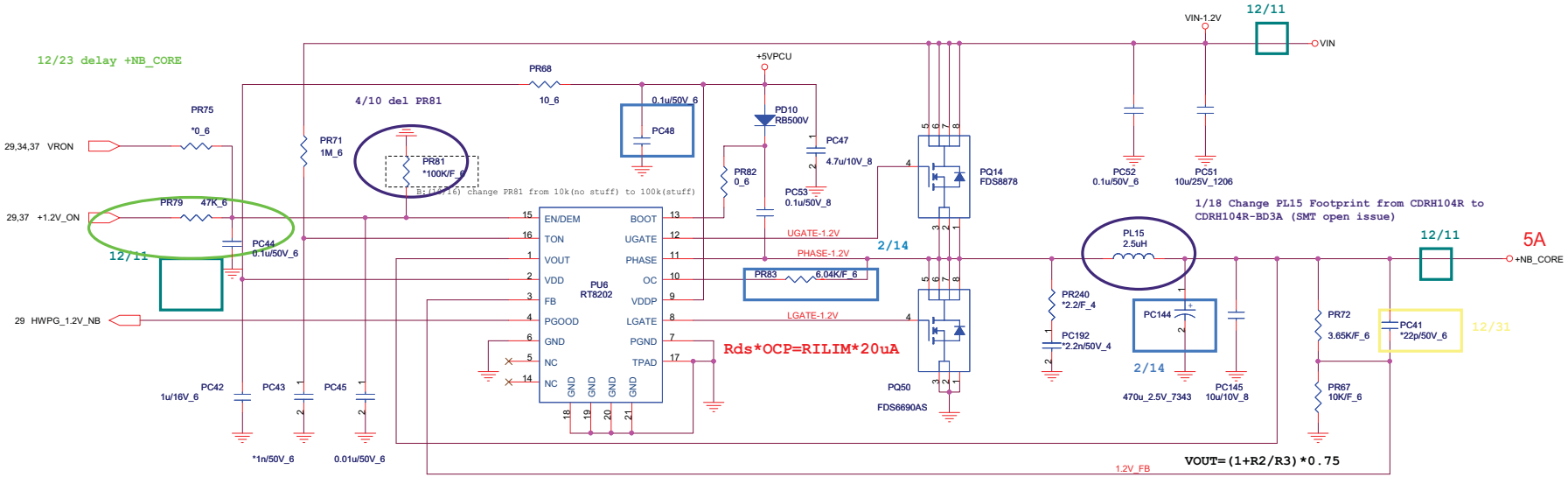
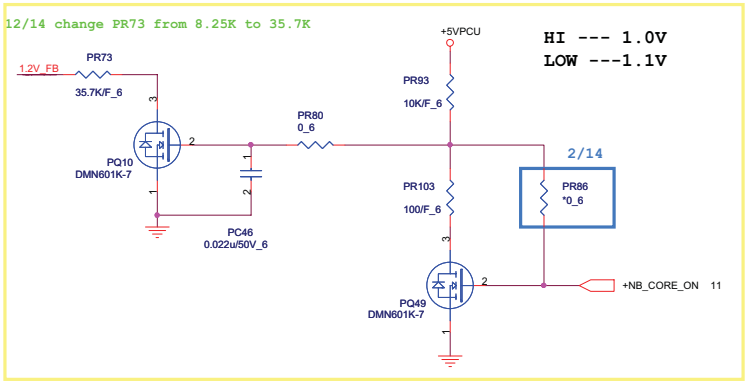


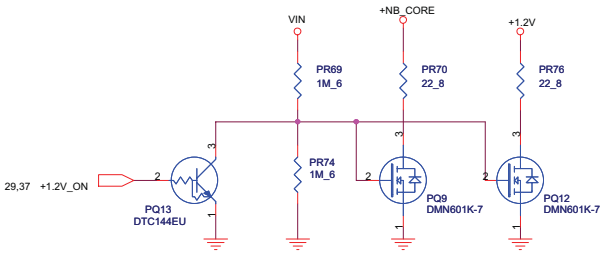
TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

6A OCP --- OC=4.53K
FDS6690AS Rds=15mOhm

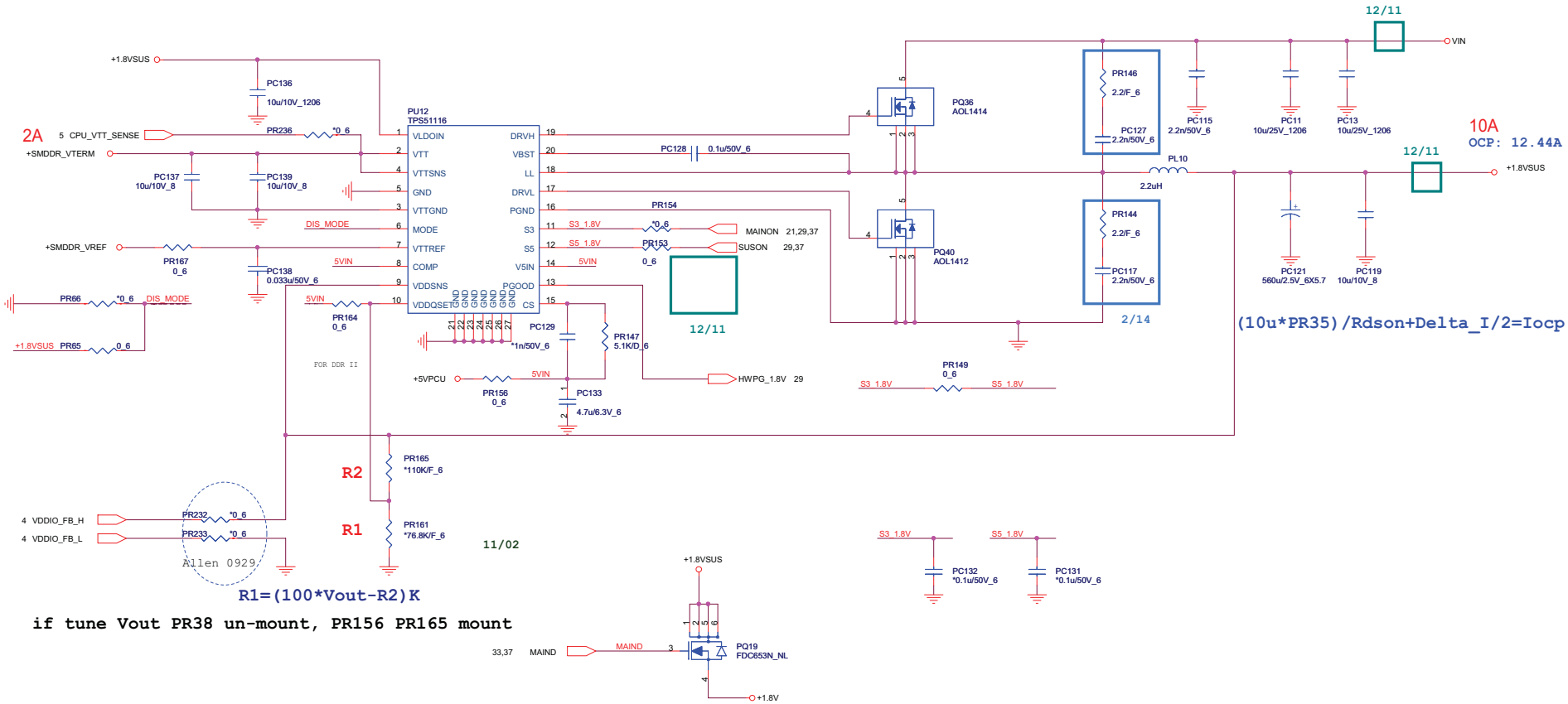


12/14 del +1.35V_VDDHTTX
PU15
PC180,PC182,PC179
PR227,PR226,PR225



PROJECT : BD3A/BL5A
Quanta Computer Inc.

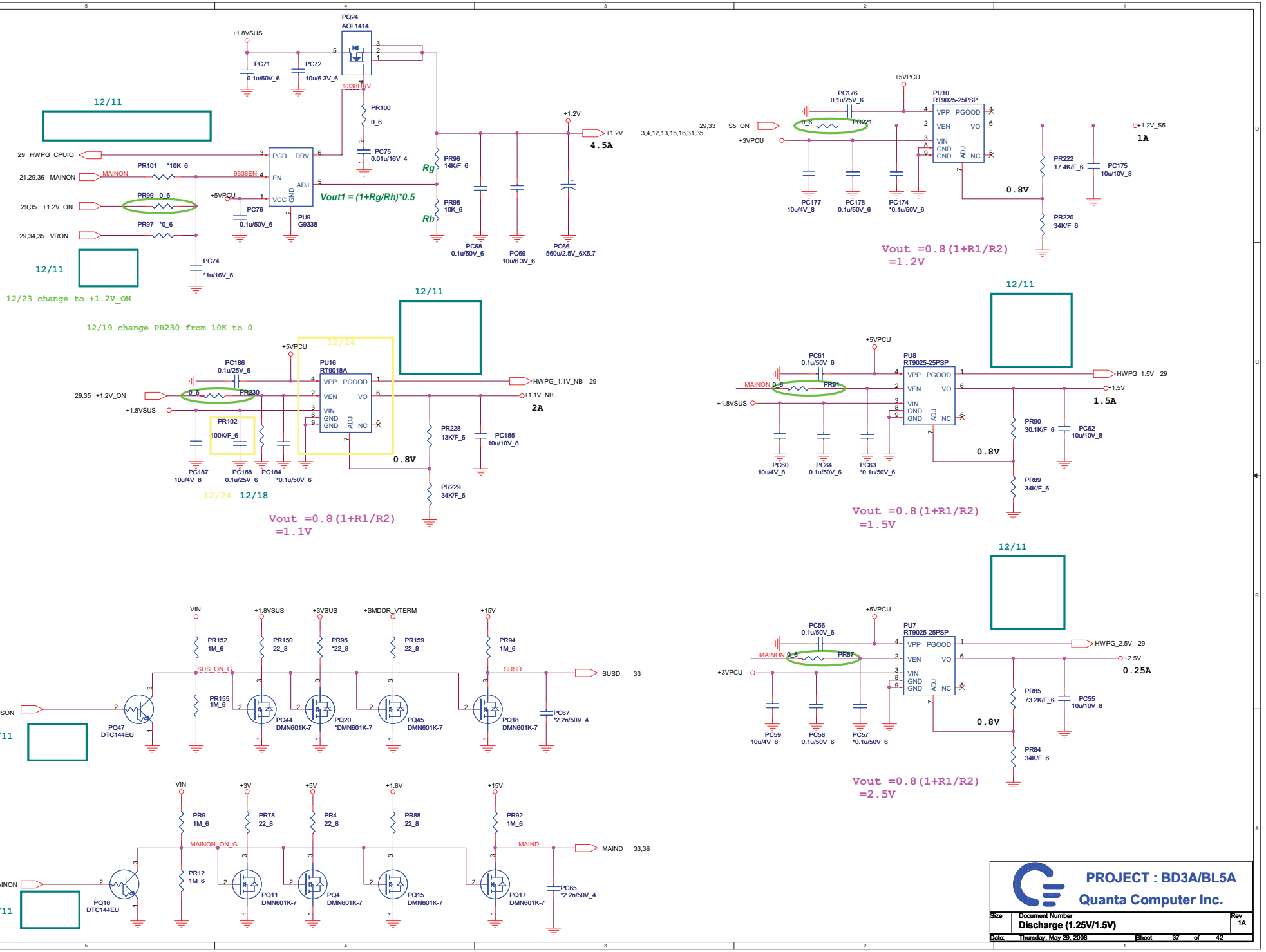
Size	Document Number	Rev
	NB_VCC (RT8202)	1A
Date: Thursday, May 29, 2008	Sheet 35 of 42	



PROJECT : BD3A/BL5A

Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A
Date: Thursday, May 29, 2008	Sheet 36 of 42	


PQ24
AOL1414
+1.8VSUS
PC71
0.1u/50V_6
PC72
10u/6.3V_6
9338B_5V
PR100
0_6
PC75
0.01u/16V_4
12/11
29 HWPG_CPUIO
PR101 *10K_6
21,29,36 MAINON
MAINON
9338EN
PR99 0_6
29,35 +1.2V_ON
PR97 *0_6
29,34,35 VRON
+5VPCU
PC76
0.1u/50V_6
PU9
G9338
PGD DRV
EN ADJ
VCC GND
Vout1 = (1+Rg/Rh)*0.5
Rg
Rh
PR96
14K/F_6
PR98
10K_6
+1.2V
+1.2V
4.5A
PC68
0.1u/50V_6
PC69
10u/6.3V_6
PC66
560u/2.5V_6X5.7
PC74
*1u/16V_6
12/11
12/23 change to +1.2V_ON
12/19 change PR230 from 10K to 0
12/24
12/11
PC186
0.1u/25V_6
PU16
RT9018A
VPP PGOOD
VEN VO
VIN
GND GND ADJ NC
+5VPCU
29,35 +1.2V_ON
0_6
PR230
+1.8VSUS
PR102
100K/F_6
HWPG_1.1V_NB 29
+1.1V_NB
2A
PR228
13K/F_6
PC185
10u/10V_8
0.8V
PR229
34K/F_6
PC187
10u/4V_8
PC188
0.1u/25V_6
PC184
*0.1u/50V_6
12/24 12/18
Vout =0.8(1+R1/R2)
=1.1V
29,33 S5_ON
3,4,12,13,15,16,31,35
+3VPCU
PC176
0.1u/25V_6
PU10
RT9025-25PSP
PR221
+1.2V_S5
1A
PR222
17.4K/F_6
PC175
10u/10V_8
PC177
10u/4V_8
PC178
0.1u/50V_6
PC174
*0.1u/50V_6
0.8V
PR220
34K/F_6
Vout =0.8(1+R1/R2)
=1.2V
12/11
PC61
0.1u/50V_6
PU8
RT9025-25PSP
MAINON 0_6
PR91
+1.8VSUS
HWPG_1.5V 29
+1.5V
1.5A
PR90
30.1K/F_6
PC62
10u/10V_8
PC60
10u/4V_8
PC64
0.1u/50V_6
PC63
*0.1u/50V_6
0.8V
PR89
34K/F_6
Vout =0.8(1+R1/R2)
=1.5V
12/11
VIN
+1.8VSUS
+3VSUS
+SMDDR_VTERM
+15V
PR152
1M_6
PR150
22_8
PR95
*22_8
PR159
22_8
PR94
1M_6
SUS_ON_G
SUSD
SUSD 33
29,36 SUSON
PR155
1M_6
PQ47
DTC144EU
PQ44
DMN601K-7
PQ20
*DMN601K-7
PQ45
DMN601K-7
PQ18
DMN601K-7
PC67
*2.2n/50V_4
12/11
PC56
0.1u/50V_6
PU7
RT9025-25PSP
MAINON 0_6
PR87
+3VPCU
HWPG_2.5V 29
+2.5V
0.25A
PR85
73.2K/F_6
PC55
10u/10V_8
PC59
10u/4V_8
PC58
0.1u/50V_6
PC57
*0.1u/50V_6
0.8V
PR84
34K/F_6
Vout =0.8(1+R1/R2)
=2.5V
VIN
+3V
+5V
+1.8V
+15V
PR9
1M_6
PR78
22_8
PR4
22_8
PR88
22_8
PR92
1M_6
MAINON_ON_G
MAIND
MAIND 33,36
21,29,36 MAINON
PR12
1M_6
PQ16
DTC144EU
PQ11
DMN601K-7
PQ4
DMN601K-7
PQ15
DMN601K-7
PQ17
DMN601K-7
PC65
*2.2n/50V_4
12/11
PROJECT : BD3A/BL5A
Quanta Computer Inc.
Size
Document Number
Discharge (1.25V/1.5V)
Rev
1A
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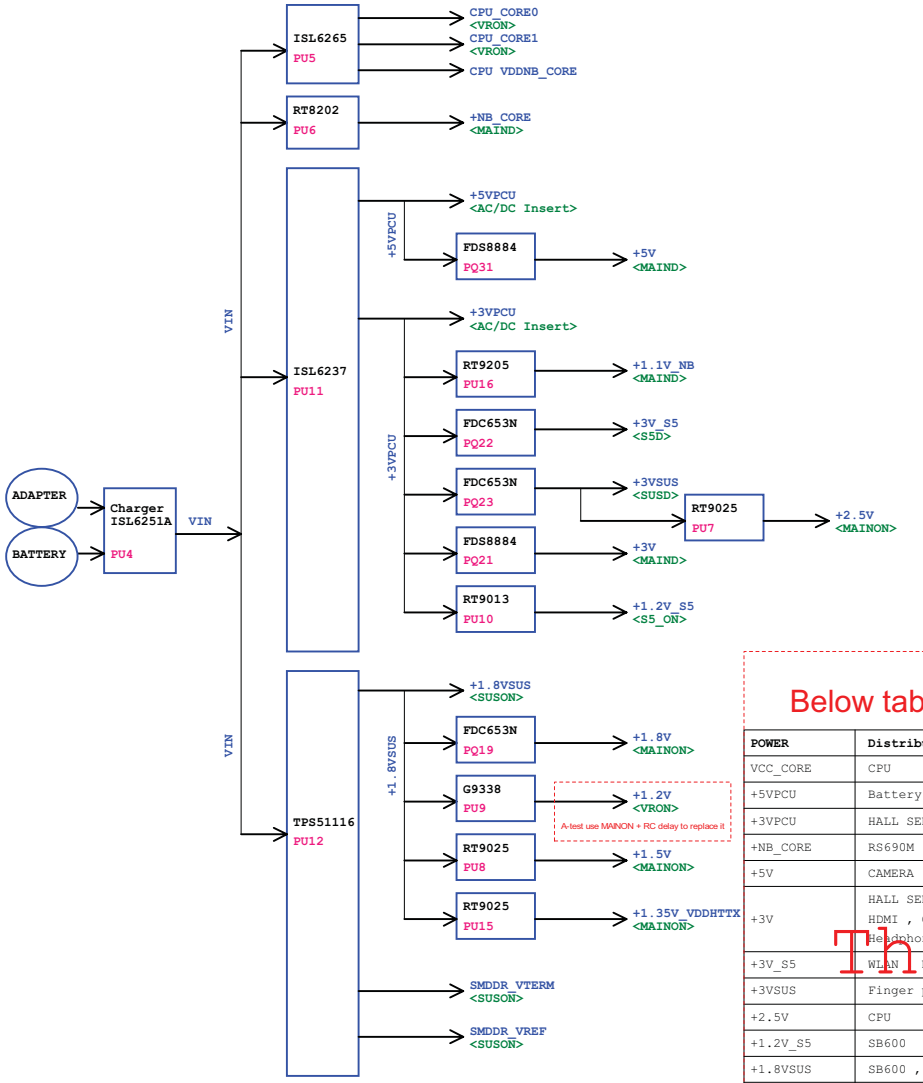
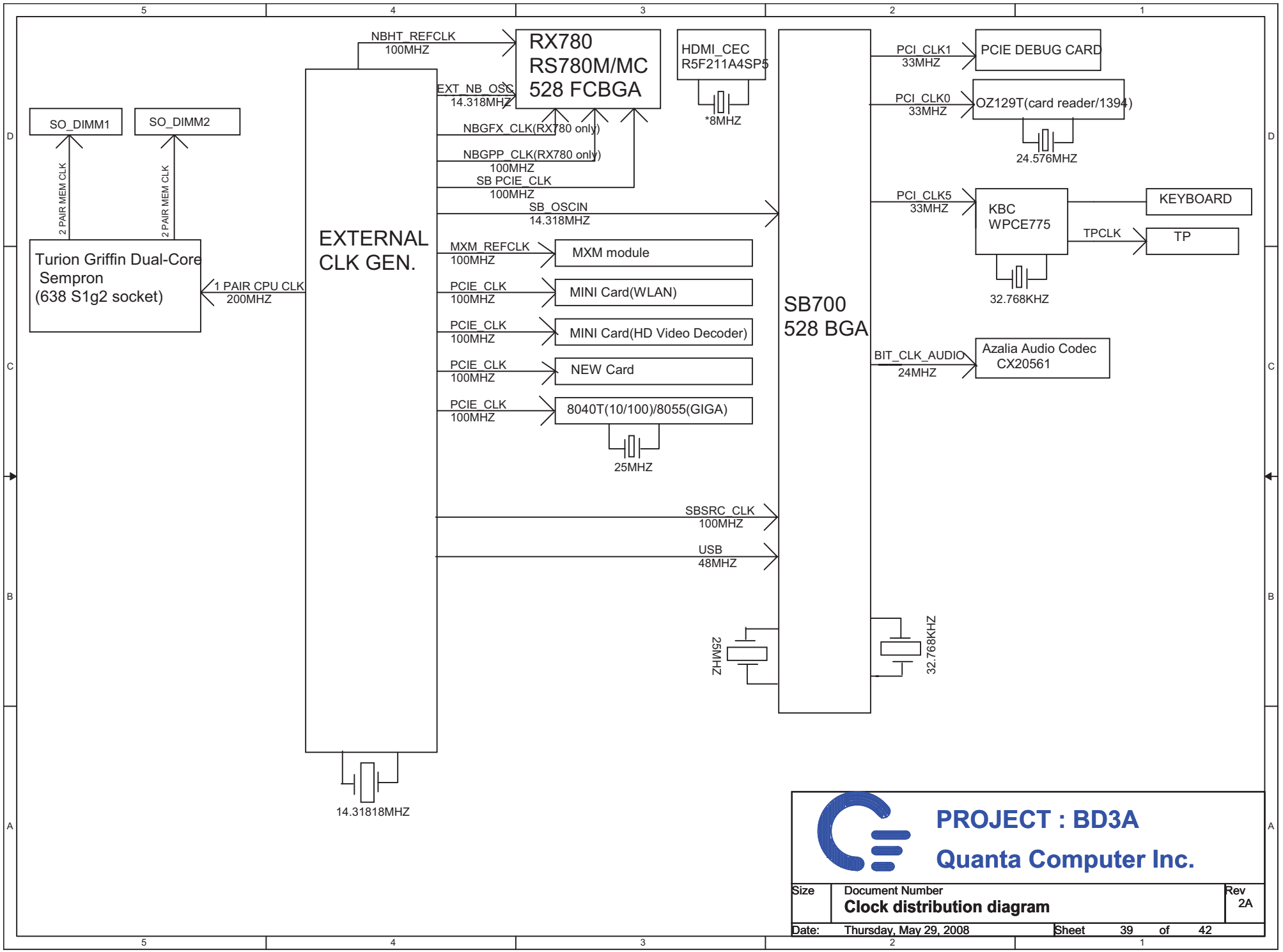


Below table need be modify (waiting other schematic ready)

POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_CORE	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	

The Table NOT READY

PROJECT : BD3A
Quanta Computer Inc.
Size | Document Number: Power Tree | Rev: 3A
Date: Thursday, May 29, 2008 | Sheet 38 of 42



PROJECT : BD3A

Quanta Computer Inc.

Size	Document Number	Rev
	Clock distribution diagram	2A
Date: Thursday, May 29, 2008	Sheet 39 of 42	

Model	REV	DATE	CHANGE LIST	NOTE
BD3G	A1A	2007	FIRST RELEASED : Import BOM ECN	ECN Release
	B2A	20071008	PAGE23:Reverse U42,C761 for VR	Circuit modify
		20071008	PAGE28:Add R667,R668,Q78 for TP_LED	Circuit modify
		20071204	PAGE04:Reverse C762 for AMD engineer CPU use	Circuit modify
		20071204	PAGE19:update CN25 HDMI footprint to HDMI-C12816-119A5-L-19P-V-BL5-1	Circuit modify
		20071204	PAGE15:change BOARD ID3 from GEVENT7 to GPIO48	Circuit modify
		20071204	PAGE14:change BOARD ID PD value from 10K to 1K(R227,R228,R229,R248,R343,R236)	Circuit modify
		20071204	PAGE29:Stuff R510, no-stuff R509 (slove BT module can't bring up issue)	Circuit modify
		20071204	PAGE20: modify display on ckt to avoid flash when into S3/S4/S5 (add Q78,Q80,R670,del Q41,R388)	Circuit modify
		20071207	PAGE19:update CN25 HDMI footprint to HDMI-C12816-119A5-L-19P-H-BD3	Circuit modify
		20071207	PAGE32:update ACIN design	Circuit modify
		20071207	PAGE24:Change R449(0 ohm) to D56(Diode) for leakage issue (3VPCU to 3V_S5)	Circuit modify
		20071207	PAGE23: Slove Audio issue:When plug in-out headphone, headphone has bo sound. 1. Change R652&R651 to C763,C764(10U/6.3V 0603)	Circuit modify Circuit modify Circuit modify
		20071207	PAGE22: Remove D19 to slove Audio issue Switch Mute to Un-mute, sound will delay about 2 seconds.	Circuit modify
		20071207	PAGE14: add D57,D58 to avoid voltage leakage	Circuit modify
		20071207	PAGE30:update LED5,LED6 footprint and PN	Circuit modify
		20071207	PAGE04:add R671~R679 for AMD request	Circuit modify
		20071208	PAGE03:change C223 C225 from 10p to 33p PAGE15:change C257 C258 from 10p to 27p PAGE26:change C380 C381 from 22p to 18p	
		20071210	PAGE25:Change New card footprint to NCARD-13180151-T-26P-L-BL5S	
		20071210	PAGE22:stuff R372 for FM	
		20071211	update power	
		20071212	PAGE29: Change U41(CIR) from BEBK0081D00 to BEBK0081D01	
		20071212	PAGE18: Change CN22(S-Video) from DFMD04FR296(Yellow Color) to DFMD04FR006(Black Color)	
		20071212	PAGE30: Change SW4 P/N from DHL00212F05 to DHL00212F07	
		20071212	PAGE31: Update Hole43 H-TSBC315D118P2, Hole 44 H-TS315BC295D118P2	
		20071212	PAGE29: pull down 100k R680 for ECPWROK	
		20071212	A11 to A12 implemen PAGE12: Del L15 stuff L36 PAGE16: Del R234 stuff R235 PAGE35: Del PU15,PC180,PC182,PC179PR227,PR226,PR225, Change PR73 from 8.25K to 35.7K	
		20071220	PAGE23: Slove GPRS noise 1. stuff R386/R387/C404/C405 to 0.1U 2. Change L44/41 to BK1608LL121	
		20071220	PAGE29: avoid leakage reserve D59/D60 to CLKRUN#/PLTRST#	
		20071221 EMI	PAGE18:add 27p(C790~C793) for TV_Y/G , TV_C/R PAGE21:stuff C568,C548 PAGE22:stuff R399,R379 PAGE23:Change L43/44 to BK1608LL121 PAGE24:add L74,C766,C767,C789,C788 for +2.5V_1.8V_LAN,add L73 for +1.2V_LAN PAGE26:add 0 ohm and 22p for SD/MS CLK , R308~R329 0ohm(CS00002JB38) change to 33ohm(CS03302JB29), remove RN34,RN35, stuff L68,L69 for 1394 PAGE28:del R276,R278 stuff L72 , del R613,R612,R624,R626 stuff L70,L71 , add 0.1u for +5VPCU add 100p for 3ND_MBDATA/CLK PAGE31:stuff all 0.1 cap	
		20071221	update power	
		20071222	PAGE11: stuff R48 2.2K for power play	
		20071222	PAGE24: Per cost down remove LAN eeprom,stuff R381,remove U21,R380,R378	
	C3A	20080102	PAGE14: NEW_DET# change from Geven3# to GPM1#	
		20080117	Update RX781	
		20080117	PAGE13:Modify RTC circuit. R301,R302 change from 8.66k to 2k. R332 change from 4.7K to 6.8K	
		20080117	PAGE13:Change RTC Battery from VARTA (AHL03001441) to MATSUSHITA (AHL03002005)	
		20080117	PAGE19:Change back HDMI connector(CN25) footprint from HDMI-C12816-119A5-L-19P-H-BD3 to HDMI-C12816-119A5-L-19P-H-BL5(SMT open issue)	
		20080117	PAGE20:for engery star add R684 connect to EC pin27	
		20080117	PAGE24:Change CN28 (RJ45 CONN) from DFTJ12FR024 to DFTJ12FR035	
		20080117	PAGE27:Change CN32(2nd SATA CONN) from DFHS22FR064 to DFHS22FR094	
		20080117	PAGE27:Change CN32 footprint from SATA-127043FR022XX27ZR-22P-L-H to SATA-127043FR022G285ZR-22P-L	
		20080117	PAGE30:Remove CN10 (Keyboard CONN)	
		20080117	PAGE21:Remove R492,R517, Short CN27/Pin189,190 to VIN directly.	
		20080118	PAGE28:Change L72 from CX216900002 to CX163210007(BT circuit)	
		20080118	PAGE08:Change CN19 footprint from DDR-C-292564-200P to DDR-C-292564-200P-BD3A (SMT open issue)	
		20080118	PAGE08:Change CN23 footprint from DDR-C-1734071-200P to DDR-C-1734071-200P-BD3A (SMT open issue)	
		20080118	PAGE30:Change SW4 footprint from SW-NSS506-212F-CCCD1T-3P to SW-NSS506-212F-CCCD1T-3P-BD3A (SMT open issue)	
		20080118	PAGE23:Change CN43 footprint from MDC-1-179373-2-12P-RUV to MDC-1-179373-2-12P-RUV-BD3A (SMT open issue)	
		20080118	PAGE35:Change PL15 Footprint from CDRH104R to CDRH104R-BD3A (SMT open issue)	
		20080118	PAGE22:Add R685 for VISTA WHQL circuit	
		20080118	PAGE24: Change RJ45 footprint from LAN-100073FR012G101ZL-12P to rj45-c100s7-10806-l-12P	
		20080118	PAGE31:HOLE 17,18.23 FBBL5004010 change to FBBL5002010	

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	Change list	2A

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Model	REV	DATE	CHANGE LIST	NOTE
BD3G	C3A	20080118	PAGE30:change footprint from 88171-3400L-34P-L to 91504-340N-34P-L	Circuit modify
		20080118	PAGE30:LED7,8 change footprint from LED12-21SYGC-TR8 to LED27-21-BHC-ZL1M2TY-3C	Circuit modify
		20080118	PAGE30:change p/n LED7 BEBL0074Z04 (WIMAX),LED8 BE0R0053Z00 (WLAN & BT)	Circuit modify
		20080131	PAGE31:update HOLE42,41,19,4,7,12,10,11,36,27,29,21,20,43,44	Circuit modify
		20080131	voltage leakage issue	Circuit modify
			PAGE04:modify CPU_PROCHOT# ckt (add R687, no stuff R686,R425), CPU_LDT_REQ#_CPU ,CPU_PWRGD connect to +1.8V	Circuit modify
			PAGE11:remove Q5,Q3,R83,R80,R97,stuff R88,R77	Circuit modify
			PAGE14:BOARD_ID4 change from GPIO66 to GPIO3	Circuit modify
		20080131	PAGE14:NEW CARD hot plug issue ,NEW_DET# change from GEVEN5# to GPM1# (SB700 A12 Errata)	Circuit modify
		20080131	PAGE19: DEL L56,L57,L58,L59,R465,R474,R493,R495,R486,R488,R478,R483,C226,C227 for HDMI circuit	Circuit modify
		20080131	PAGE25: add +3V to CN21 pin39,41	Circuit modify
		20080131	PAGE18: Change L4,L5,L6 to CX8BA470003 to meet CRT spec	Circuit modify
		20080131	PAGE19: Change U11 from ARBL5SV0000 to ARBL5MV0000	Circuit modify
		20080131	PAGE26:According to customer request, we can't stuff C782 (22pF) in SD/MS_CLK.	Circuit modify
		20080131	PAGE25: Change R573 from 28.7K to 0 ohm, Remove C628 for NEW card some device can't work normal	Circuit modify
		20080131	PAGE14: Change R350 from 1K to 0 ohm (Slove VCCRTC can't reach 0V when clear CMOS.)	Circuit modify
		20080131	PAGE26: Change CN33(5 in 1 card CONN) P/N from DFHS38FR003 to DFHS38FR005	Circuit modify
		20080131	PAGE27: Change CN34 (1st SATA) P/N from DFHS22FR063 to DFHS22FR082	Circuit modify
		20080131	PAGE27: Change CN32 (2nd SATA) P/N from DFHS22FR094 to DFHS22FR083	Circuit modify
		20080131	PAGE20: Change CN5 (I-MIC)P/N from DFHD02MR003 to DFHD02MR016	Circuit modify
		20080131	PAGE22: Change CN39(I-MIC CONN) P/N from DFHD02MR003 to DFHD02MR016	Circuit modify
		20080131	PAGE22: Change CN17(SPK CONN) P/N from DFHD04MR012 to DFHD04MR021	Circuit modify
		20080131	PAGE28: Change CN16(USB-FFC CONN) P/N from DFHD10MR011 to DFHD10MR008	Circuit modify
		20080131	PAGE28: Change CN13(FP CONN) P/N from DFHD04MR012 to DFHD04MR021	Circuit modify
		20080131	PAGE28: Change CN14(BT CONN) P/N from DFHD10MR011 to DFHD10MR008	Circuit modify
		20080201	PAGE22: Change INT-SPK AMP GAIN VALUE. Change R623,R625 from 9.1k to 5.1k 1%,Change R620,R621 from 10k to 16k 1%	Circuit modify
		20080201	PAGE30: Change R404,R405 from CS13902JB14 (390 ohm) to CS13302JB21(330 ohm)	Circuit modify
		20080201	RS780M A13 Errata	Circuit modify
			PAGE11:change R103 from 150 to 140 CS11402FB01	Circuit modify
			PAGE18:RS780M A13 R8 ---> 140 CS11402FB19,MXM R8 ---> 150 CS11502FB21	Circuit modify
		20080201	PAGE19: change HDMI SCL/SDA pull res R168,R171,R163,R170 to 4.7K ,change R1,R2 to 6.8K	Circuit modify
		20080201	PAGE20: change Panel SDA/SDC pull res R412,R410 from 39K to 4.7K	Circuit modify
		20080204	ESD solution	Circuit modify
			PAGE23: add Varistor D63,D64,D65 on SPDIF_OUT/HP_JD/+3V_SPD	Circuit modify
			PAGE28: reserve D66 for CN36 , reserve D68,D69,D70 for FP , stuff D71,D72,D73 for BT	Circuit modify
			PAGE20:reserve D74,D75,D76 for CCD ,stuff D87 for LID switch	Circuit modify
			PAGE27:del R270,R597 , connect to +5V directly ,reserve D77~D81 for CN34(1ND HDD) ,reserve D82~D86 for CN32(2ND HDD) ,reserve D67 for CN31	Circuit modify
			PAGE26:reserve D88~D91 for 1394	Circuit modify
			PAGE04:reserve D92,D93 for FAN , reserve C795,C796 change R122 to 0 0603	Circuit modify
			PAGE13,19,21,25:reserve C797~800 for PLTRST#	Circuit modify
		20080204	PAGE04: pull up R691 CPU_BDREQ# to avoid noise cause system shut down	Circuit modify
		20080205	PAGE23:Change R714,R715 from 10uF to 0 ohm (Audio HP circuit)	Circuit modify
		20080210	PAGE18,29: DEL D4,D5 footprint and DEL CRT_SENSE# net, No stuff R218	Circuit modify
		20080210	PAGE28: DEL C42, Add D94 for CN8/Pin2 (ESD issue) - default no stuff	Circuit modify
		20080210	PAGE28: Change L70,L71 from CX216900002 to CX163210007	Circuit modify
		20080210	PAGE28: Stuff L64,L65 to CX163210007	Circuit modify
		20080213	PAGE27: Add ESATA re-driver IC	Circuit modify
		20080213	PAGE25: Change the footprint of R33 and R330 from 1206 to 0805	Circuit modify
		20080213	EMI solution	Circuit modify
			PAGE18: C4,C7,C10,C5,C8,C11 change from 10p to 6.8p	Circuit modify
			PAGE28: stuff C391,C701, C559 ,C228,C465,C618,C41,C43, C618,C794,C809,C810	Circuit modify
			PAGE20: stuff C427~C432	Circuit modify
			PAGE30: stuff C39,C346	Circuit modify
			PAGE29: stuff C577,C578,C560	Circuit modify
			PAGE12: stuff C804~C807 for +NB_CORE	Circuit modify
			PAGE25: stuff C40,C36,C54,C58,C289,C352,C319,C272 for WL	Circuit modify
			PAGE19: stuff C808 for HDMI	Circuit modify
			PAGE15: stuff C375,C366 for SB HW MONITOR	Circuit modify
			PAGE22: stuff R627	Circuit modify
			PAGE26: change R683 from 0 to 33 ohm	Circuit modify
		20080214	UPDATE POWER	Circuit modify
		20080215	PAGE28: CN42 co-layout with CN16	Circuit modify
		20080215	PAGE31: Remove R98,R145,R118 Hole15,17,18	Circuit modify
		20080215	PAGE28: Change L70,L71 from CX216900002 to CX201290009	Circuit modify
		20080218	PAGE31: HOLE 15,24.25 FBBD3017010 change to FBBD3021010	Circuit modify
		20080218	PAGE31: HOLE 28.35 FBBL5007010 change to FBBL5050010 , HOLE 13,14 FBBL5008010 change to FBBL5051010	

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BD3G	C3A	20080218	PAGE04: G781 reverse R718 0 ohm for Griffin CPU	Circuit modify
		20080219	PAGE04: change G781 to G786P81U	Circuit modify
		20080220	PAGE27:1.change C801,C82 from 0.01u to 4.7n, 2.RX add C811,C812 4.7n	Circuit modify
		20080222	PAGE15:change SATA ODD from port3 to port4 (solve ODD post detect fail)	Circuit modify
		20080226	PAGE27:change ESATA conn usb-2006109-11p,update p/n to DFHS11FR021	Circuit modify
		20080227	update power include EMI	Circuit modify
		20080229	del co-layout parts	Circuit modify
			RN34,RN35,R608,R607,R572,R569	Circuit modify
		20080303	PAGE14: del Mini card USB10,Felica USB5 , change BT to port5 , ESATA to port 10	Circuit modify
		20080303	PAGE25: MINI PCI II no need USB , change USB10 to ESATA .and del R169,R188	Circuit modify
		20080303	PAGE28: no Felica request , remove USB del R178,R179,remove Q57,C476,R450,Q56	Circuit modify
		20080303	PAGE31: EMI request add C813,C814	Circuit modify
		20080410	PAGE17: change R150 to R152 for power sequence	Circuit modify
		20080410	PAGE26: add D88~D91 for 1394 ESD	Circuit modify
		20080410	PAGE27: change ESATA conn usb-2006109-11p update p/n to DFHS11FR023	Circuit modify
		20080410	PAGE27: add D67,D49,D50 for ESATA USB ESD	Circuit modify
		20080410	PAGE28: add D51,D52, D66 for USB0	Circuit modify
		20080410	PAGE34: add PC191,PC193 for CPU core	Circuit modify
		20080410	PAGE35: del PR81	Circuit modify
		20080410	PAGE27: remove Flash card ckt	Circuit modify
		20080416	PAGE13: change RTC pad location to G1	Circuit modify
		20080416	PAGE14: pull up USB_OC5# R719	Circuit modify
		20080416	PAGE18: update footprint to sv-030018fr004s100fr-4p-h-bl5m	Circuit modify
		20080416	PAGE23: update footpritnt to knob-xre094-3p-bl5m	Circuit modify
		20080416	PAGE28: remove CN42 not co-layout with CN16	Circuit modify
		20080416	PAGE31: update HOLE13,14 footprint to H-C236D146P2	Circuit modify
		20080417	PAGE27: remove D77~D81 for CN34 , change to U44 CM1213-04SO(AL001213001) ,remove D82~D86 for CN32 , change to U45 CM1213-04SO	Circuit modify
		20080418	PAGE28: Change L72 from CX163210007(BT circuit) to CX201290009	Circuit modify
		20080421	PAGE31: remove Hole31,37	Circuit modify
		20080421	no stuff +3VSUS component	Circuit modify
			PAGE31: no stuff C229,C518,C128	Circuit modify
			PAGE33: no stuff PQ23	Circuit modify
			PAGE37: no stuff PR95,PQ20	Circuit modify
		20080424	PAGE16: IDE/FLASH not use ,remove C287,C288,C297,C293,C294	Circuit modify
		20080424	PAGE16: internal clk not use ,remove C332,C330,C327,C331, change L28 to 0 ohm	Circuit modify
		20080424	To meet ESATA SI	Circuit modify
			PAGE27: change R706 from 0 ohm to 330 , stuff R692,R693,R694	Circuit modify
				Circuit modify
		20080424	PAGE16: remove C762 to meet PWRGD timing spec	Circuit modify
		20080424	PAGE9: stuff R480,R479 to meet AMD spec	Circuit modify
		20080424	PAGE17: stuff C765 10nf to meet power sequence	Circuit modify
		20080505	PAGE34: intersil recommand to set OCP to 30A	Circuit modify
			Change PR218 from CS32052FB21 to CS41072FB11,Change PR157 from CS41002FB28 to CS31002FB26,Change PR160 PR216 from	Circuit modify
			CS31622FB27 to CS23652FB08	Circuit modify
		20080505	PAGE22: Change CN17 from DFHD04MR021 to DFHD04MRA75	Circuit modify
		20080505	PAGE27: update re-driver footprint to tqfn36-5x6-5-37p-0_75h-te1m	Circuit modify
		20080505	PAGE20: reserve R720,R721 for cost down	Circuit modify
		20080505	PAGE27: add C816 0.1u to U44 +5V for ESD , add C818 0.1u to U45 +5V for ESD	Circuit modify
		20080505	PAGE25: remove CN30 second PCIE (HD Decoder)	Circuit modify
		20080505	PAGE31: remove HOLE28,35 (HD Decoder)	Circuit modify
		20080507	PAGE20: stuff D74,D75,D76 for CCD	Circuit modify
		20080508	PAGE20: reserve CM1293 U46,C819 for CCD ESD protect	Circuit modify
		20080508	PAGE28: stuff D68,D69,D70 for FP	Circuit modify
		20080508	PAGE30: stuff D53 for RF_LED ESD	Circuit modify
		20080509	PAGE26: 5/9 for card reader MS DUO adapter short issue	Circuit modify
			reserve R723,724,722 ,Q82,Q81,Q83,Q84	Circuit modify
		20080513	PAGE4: follow AMD design guide 1.03 stuff R675	Circuit modify
		20080527	PAGE26: some 1394 device can't boot normal	Circuit modify
			change L38 to BK1608HS220_6	Circuit modify
		20080527	PAGE34: CPU core adj	Circuit modify
			1.PR160,PR216 change to 3.92K/F_4	Circuit modify
			2.PR213,PR215 change to 18.2K/F_4	Circuit modify
		20080527	PAGE33: solve system hang up , when plug adp quickly	Circuit modify
			change PR113 from 150K_4 to 115K/F_4	Circuit modify
		20080527	PAGE33: avoid right side USB voltage drop	Circuit modify
			change PR119 to 63.4K , PR120 to 10K	Circuit modify
		20080528	PAGE12: del C805,C807	
		20080529	PAGE27: change ESATA conn p/n to DFHS11FR027	

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