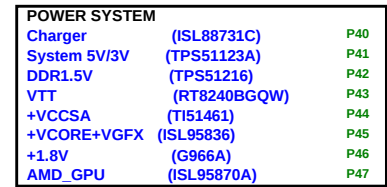
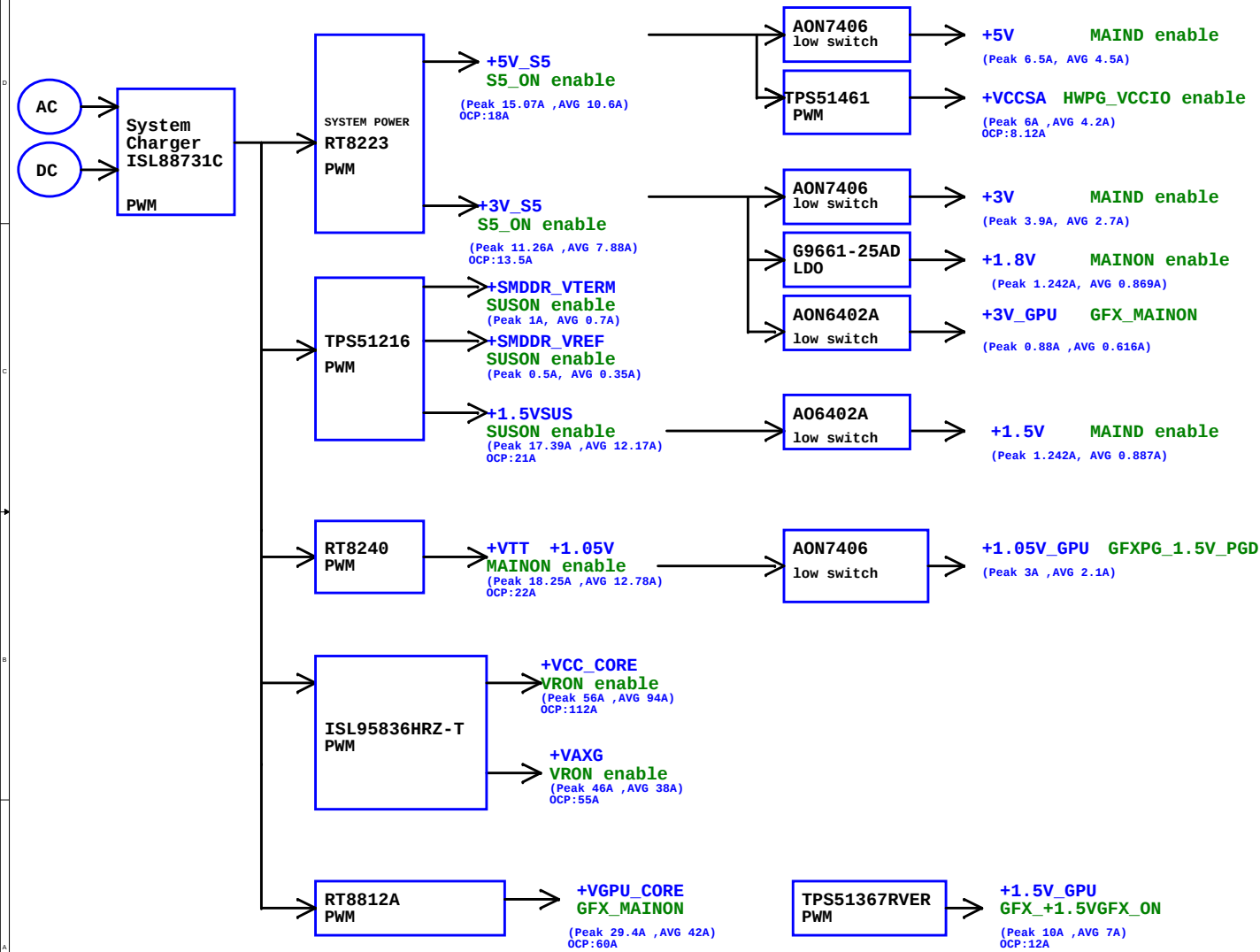
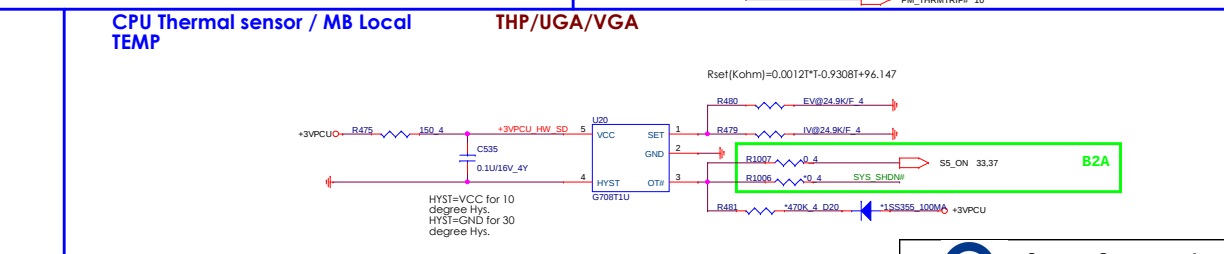
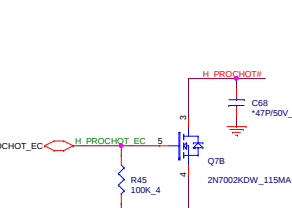


01



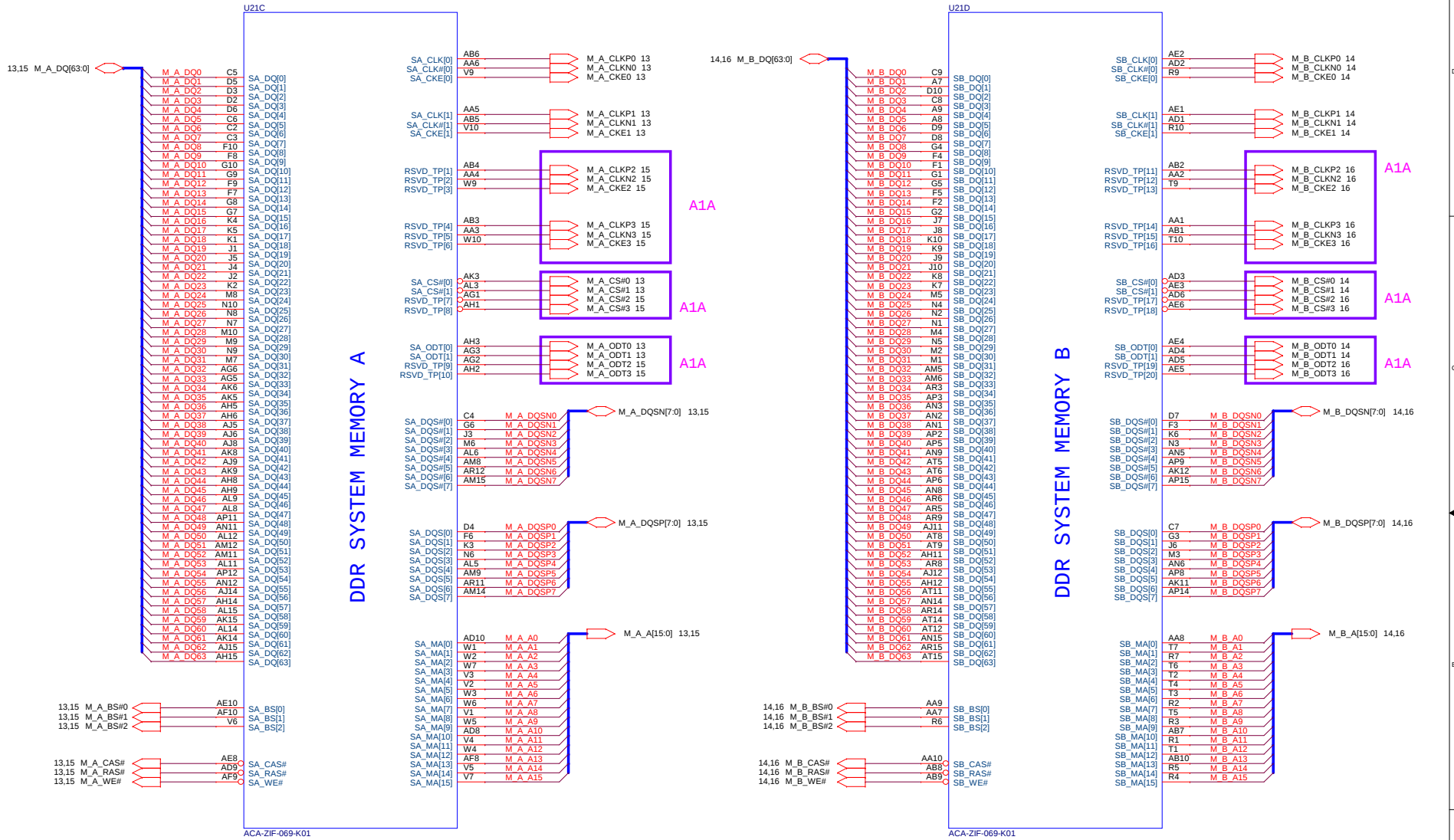


POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

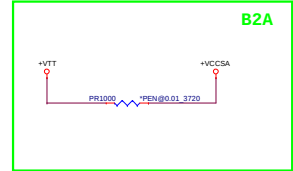


Ivy Bridge Processor (DDR3)CPU

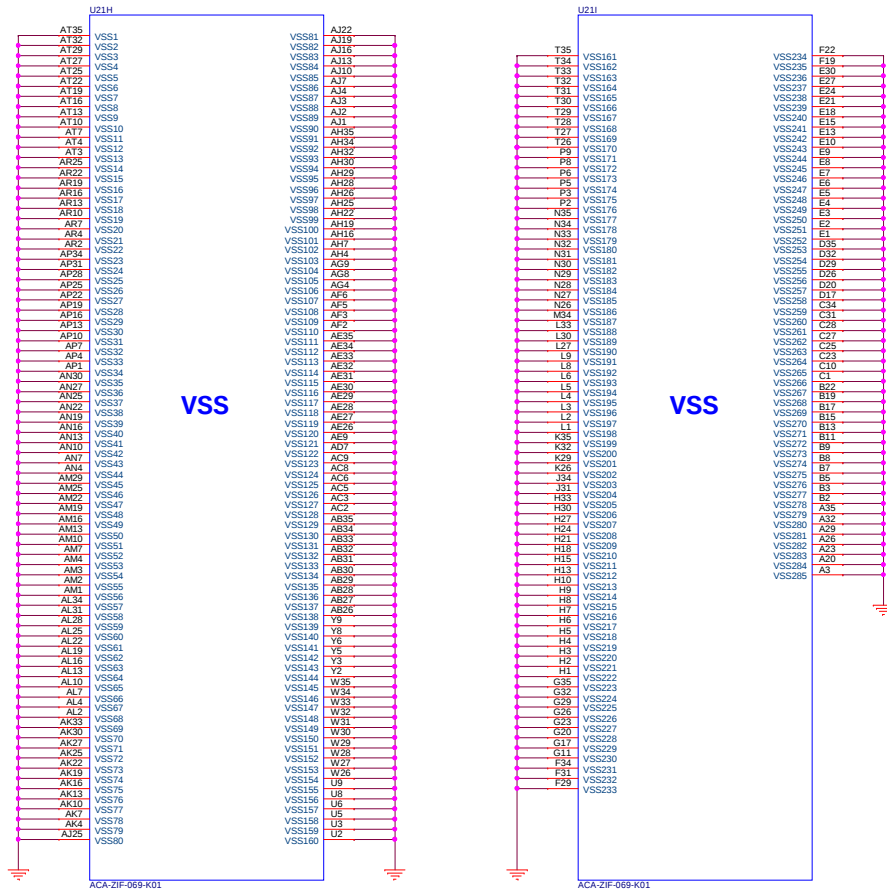
04



POWER

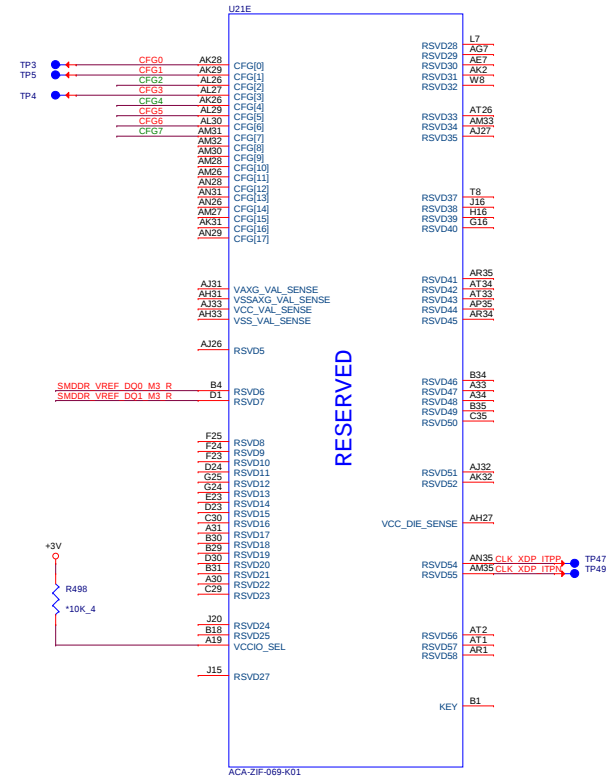


Ivy Bridge Processor (GND) CPU



Ivy Bridge Processor (RESERVED, CFG) CPU

06

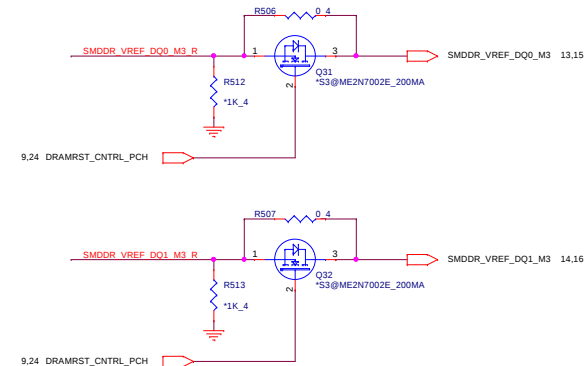


Processor Strapping CPU/VGA

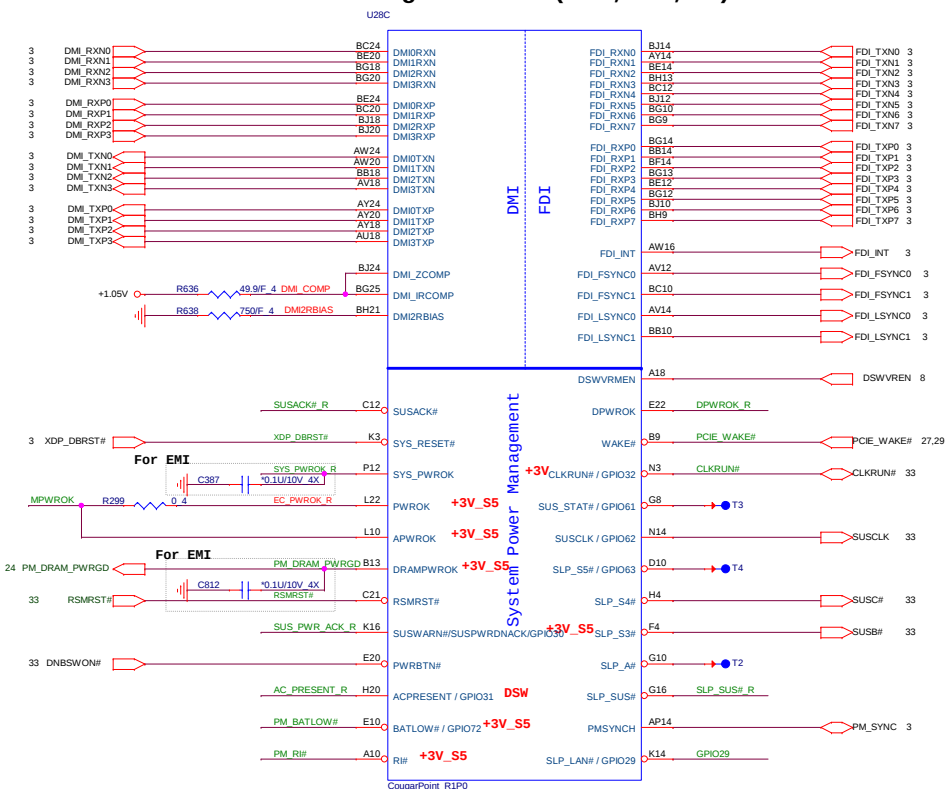
The CFG signals have a default value of '1' if not terminated on the board.

Pin Name	Configuration	
CFG2 (PEG Static Lane Reversal --> 16 Lane)	1=Normal Operation 0=Lane Reversed	
CFG3 (Reserved)		
CFG4 (DP Presence Strap)	1=Disable; No physical DP attached to eDP 0=Enable; An ext DP device is connected to eDP	
CFG5 CFG6 (PCIe Bifurcation)	00=x8,x4,x4 - Device 1 function 1 and 2 enable 01=Reserved - (Device 1 function 1 disable ; function 2 enable) 10=x8,x8 -Device 1 function 1 enable ; function 2 enable 11=(Default) x16 -Device 1 function 1 and 2 disable	
CFG7 (PEG Defer Training)	1=PEG train immediately following xoRESETB de assertion 0=PEG wait for BIOS training	

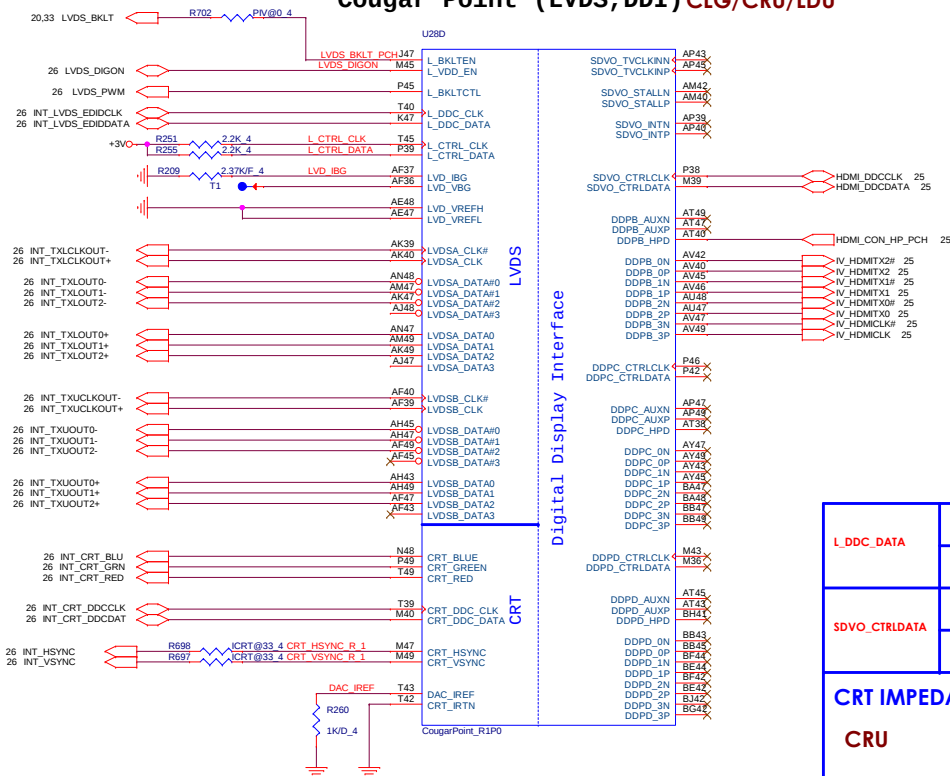
DDR3 VREF DQ (M3) S3P



Cougar Point (DMI, FDI, PM) **CLG**



Cougar Point (LVDS, DDI) CLG/CRU/LDU



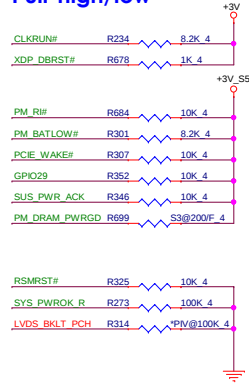
I_DDC_DATA	1 -- LVDS ENABLE
	0 -- LVDS DISABLE
SDVO_CTRLDATA	1 -- PORT B Detected
	0 -- PORT B Disable

CRT IMPEDANCE MATCHING

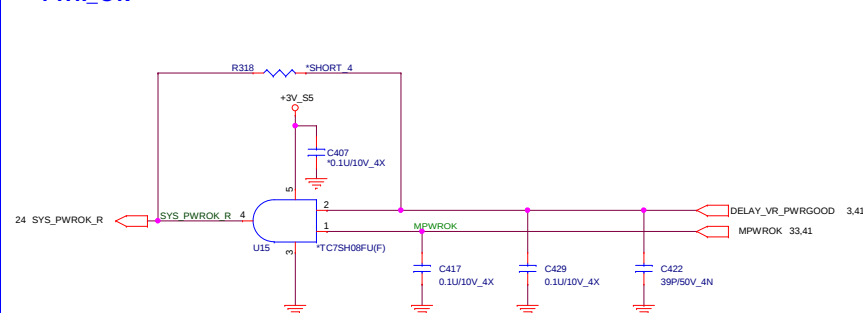
CRU



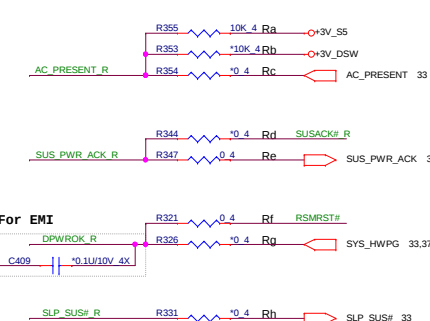
PCH Pull-high/low CLG/PIV/S3P



System PWR OK CLG

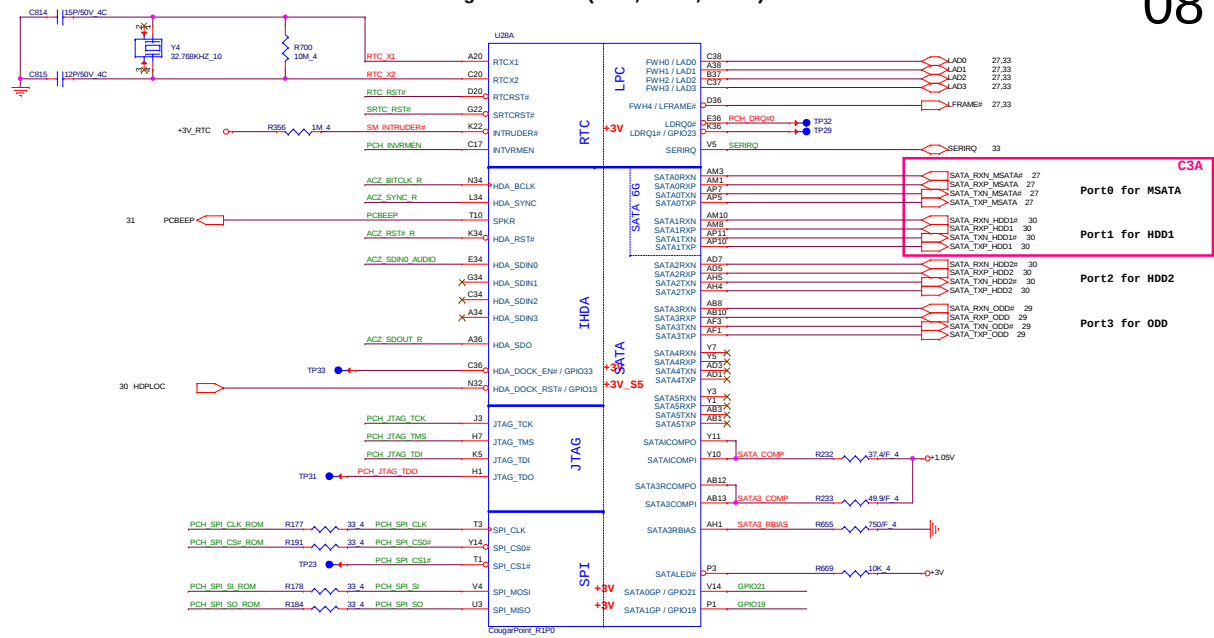


Deep Sx CLG



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

Cougar Point (HDA, JTAG, SATA) CLG/GCK

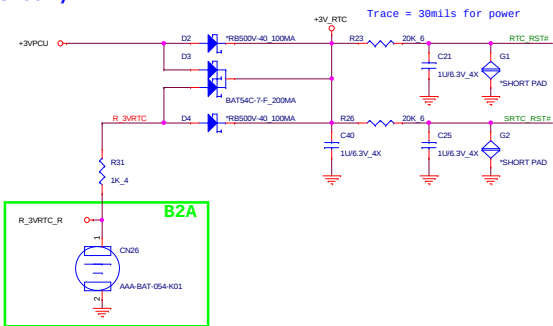


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V ₀ R222 1K 4 PCBEEP									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R313 1K 4 PCH_GNT3# 9									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R330 300K 4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GPIO19</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GPIO19	Boot Location	1	1	SPI *	0	0	LPC	R712 1K 4 GNT1# 9 R670 1K 4 GPIO19
GNT1#	GPIO19	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R708 1K 4 ACZ_SDOOUT_R 3									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R634 2.2K 4 DF_TVS 10 R635 1K 4 HDA_SMB_VBtr 3									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3V_S5 R227 10K 4 PLL_ODVR_EN 10 R242 1K 4									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R365 3K 4 ACZ_SYNC_R									
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low, leave as No Connect									
GNT2# / GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile									
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 R680 1K 4 GPIO15 10									
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0 = NC									
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0 = NC									
SATA3GPI / GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
SATA2GPI / GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	+3V_RTC R340 300K 4 DSWVRMEN 7 R339 330K 4									

RTC Circuitry

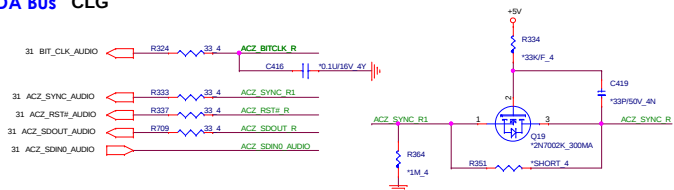
RTC



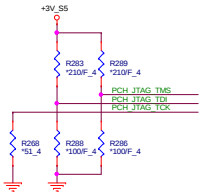
PU & Password Clear CLG



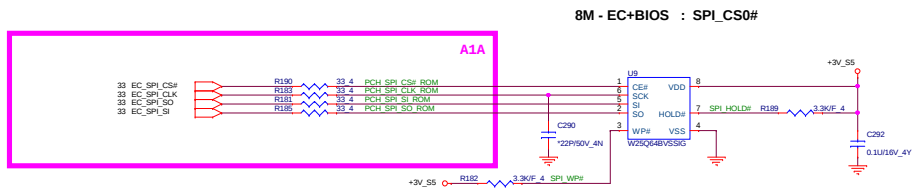
HDA Bus CLG



PCH JTAG Debug DEG

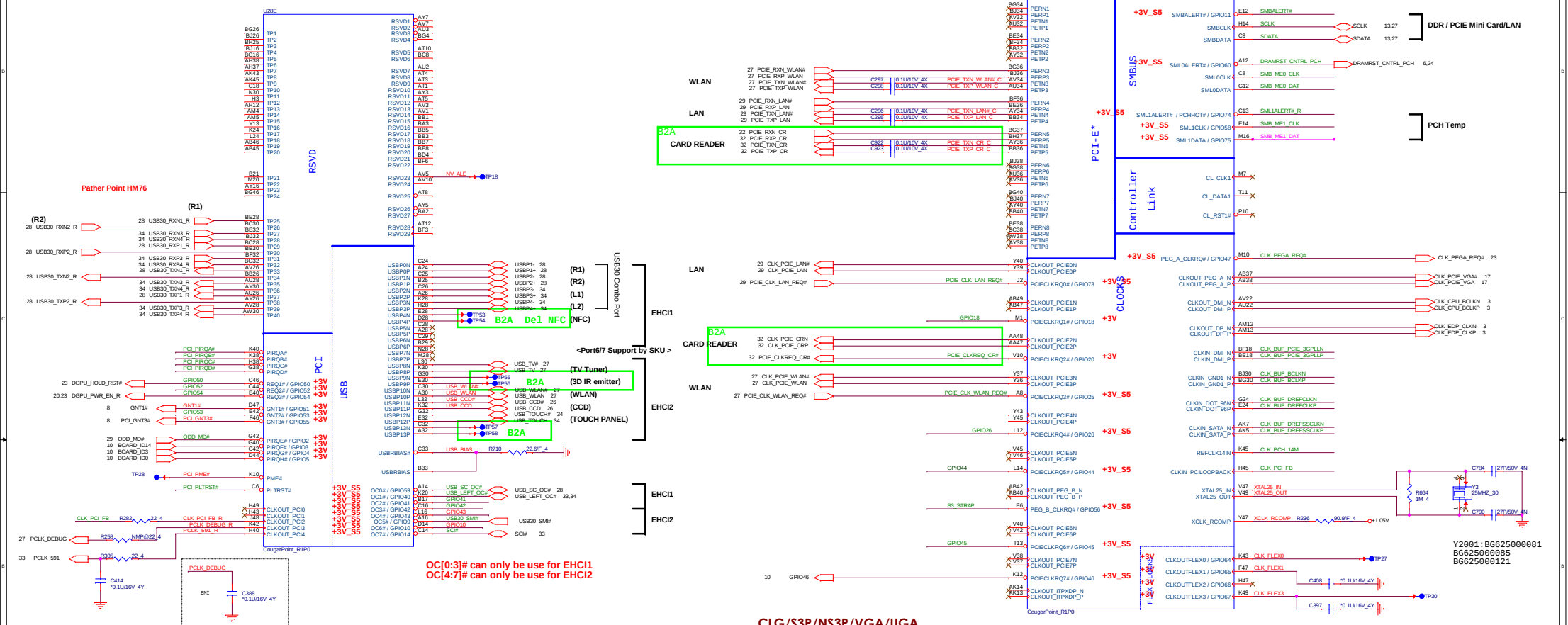


PCH Dual SPI CLG

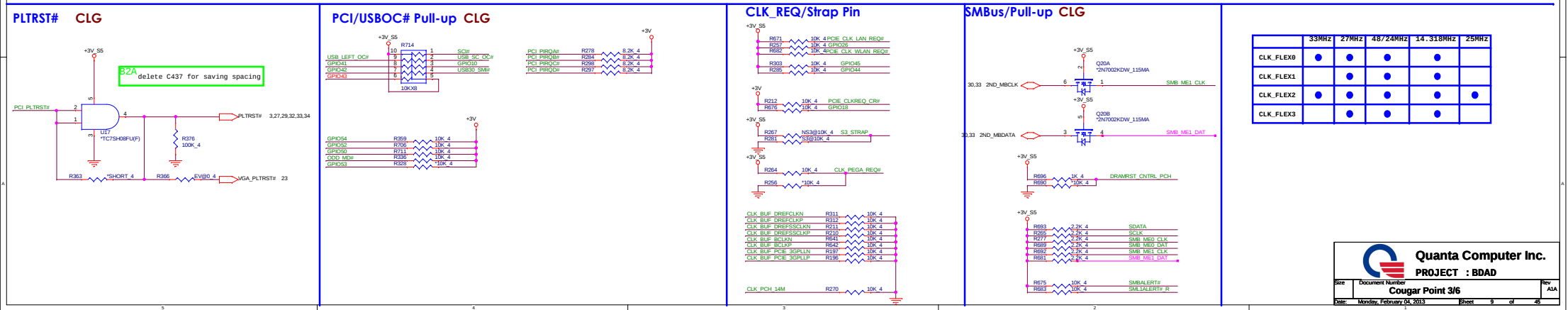


8M - EC+BIOS : SPI_CS0#

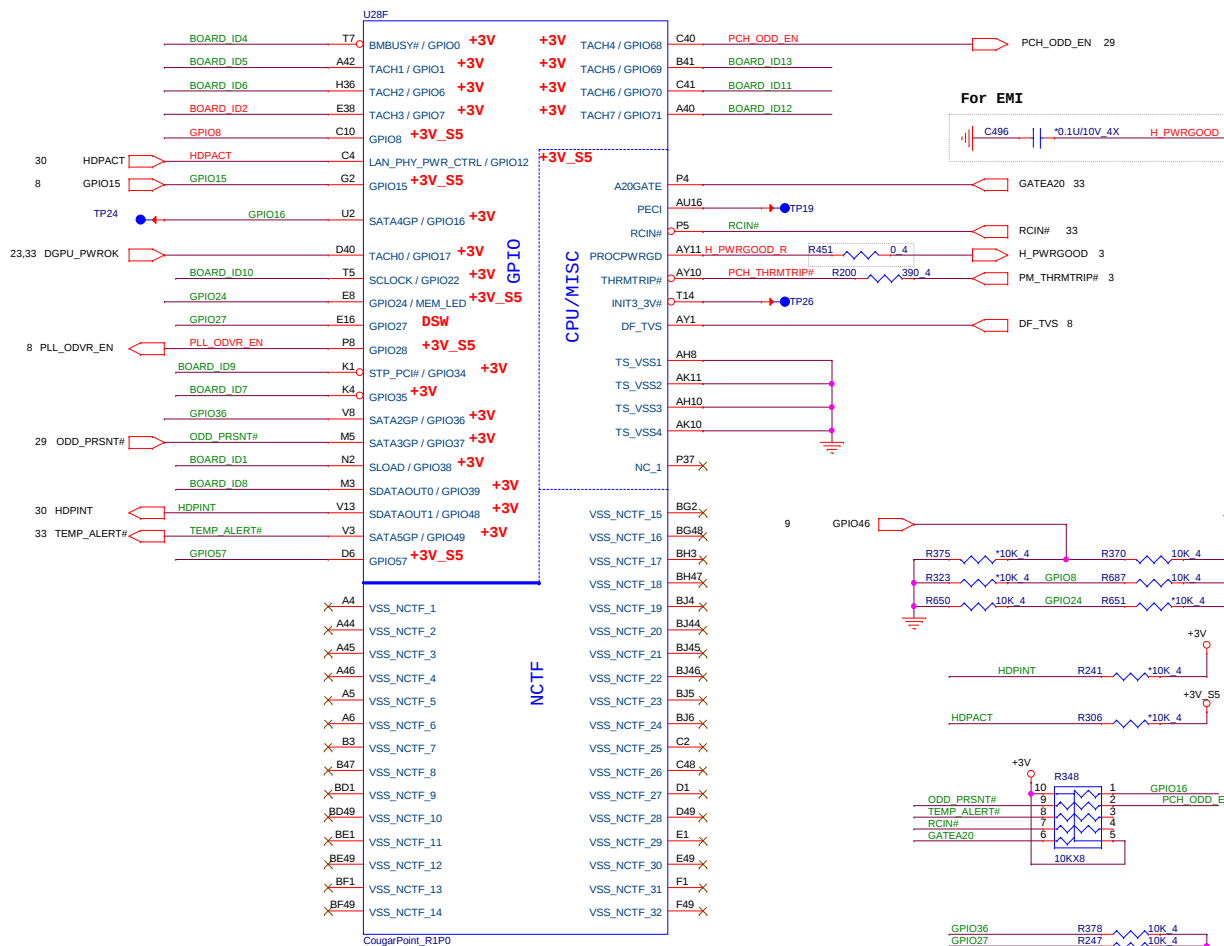
Cougar Point-M (PCI,USB,NVRAM) CLG/DEG



CLG/S3P/NS3P/VGA/UGA

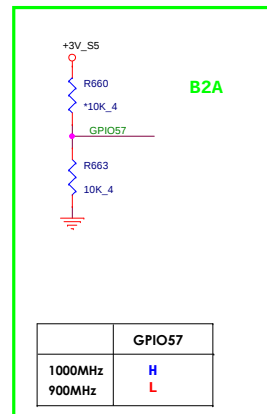
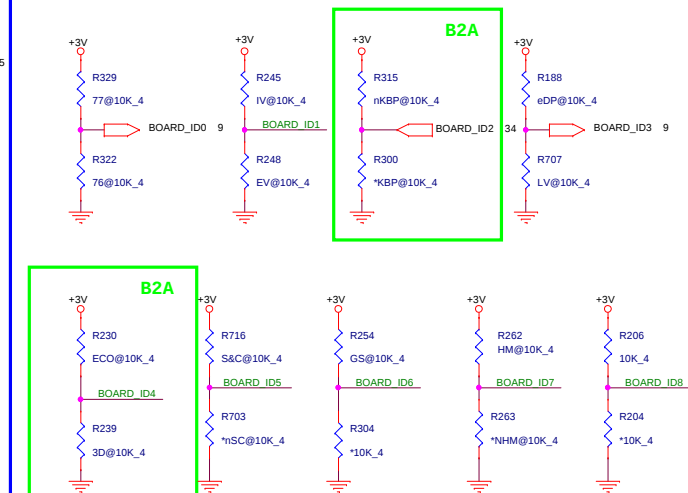


Cougar Point (GPIO, VSS_NCTF, RSVD) CLG

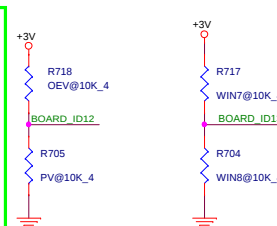


BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

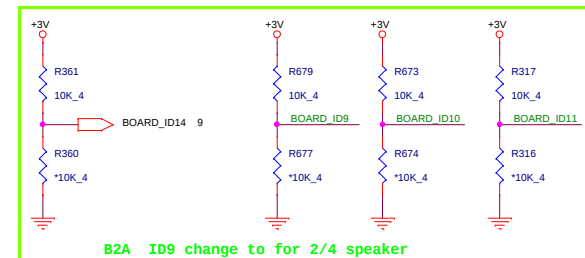
Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID12	ID13	ID14
HM77 HM76	H L											
UMA SKU VGA SKU		H L										
W/O LED KB W/ LED KB			H L									
eDP LVDS				H L								
ECO Mode 3D Mode				H L								
S&C Non S&C					H L							
W/ 6-sensor W/O 6-sensor						H L						
W/ HDMI W/O HDMI							H L					
Premium Gaming								H L				
Only VGA Optimus mode									H L			
WIN7 WIN8										H L		
W/O TV W/ TV											H L	



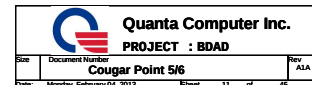
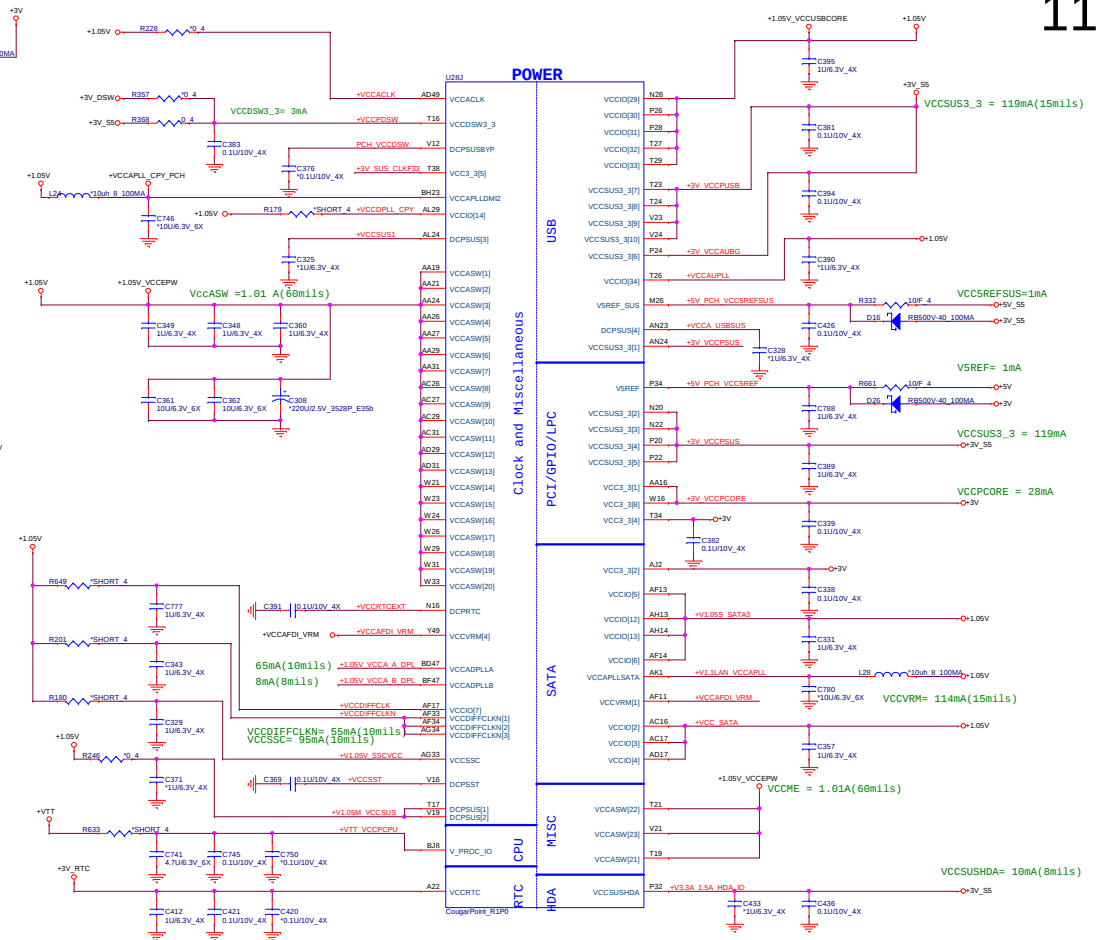
	GPIO57
1000MHz	H
900MHz	L



Board ID	ID9	ID10	ID11
4 Speaker 2 Speaker	H L		
W/O CIR W/ CIR		H L	
W/O TouchSCN W/ TouchSCN			H L



B2A ID9 change to for 2/4 speaker



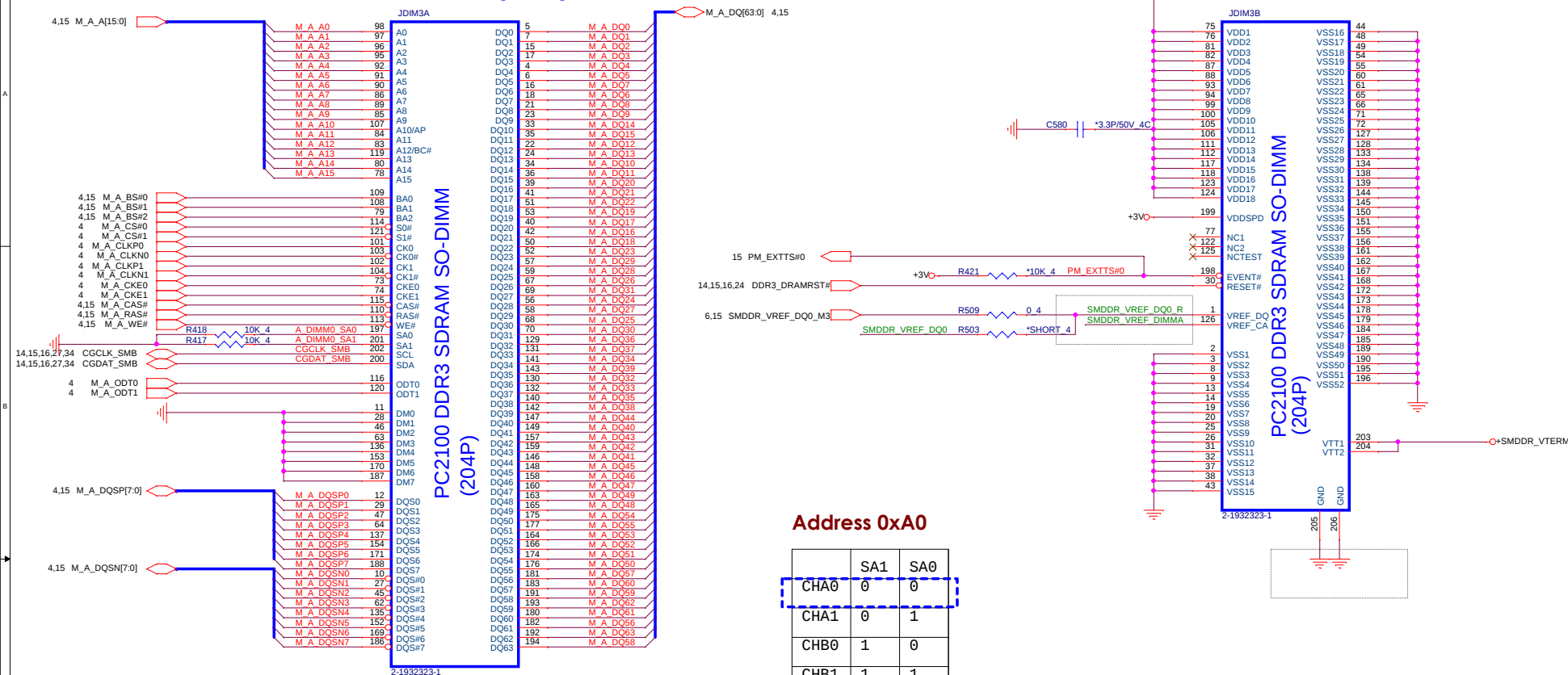


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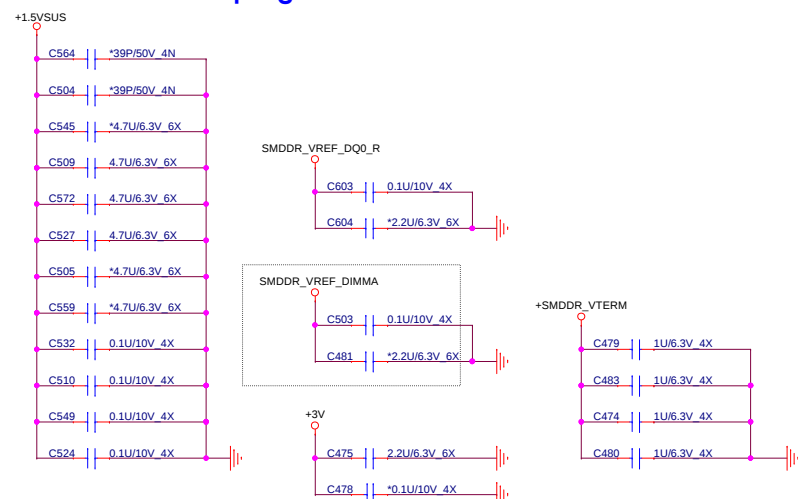
DDR

BOT side close to CPU

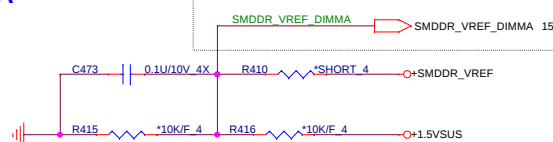
H=8 (Rev)



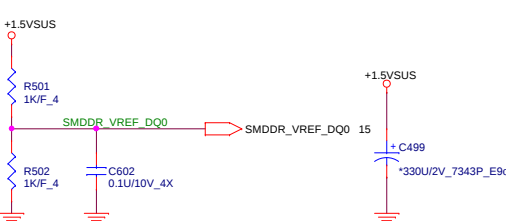
DDR Power Decoupling DDR



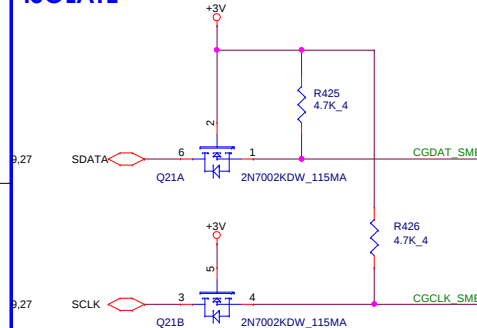
DDR3 VREF DDR CA



DDR3 VREF DQ (M1) DDR

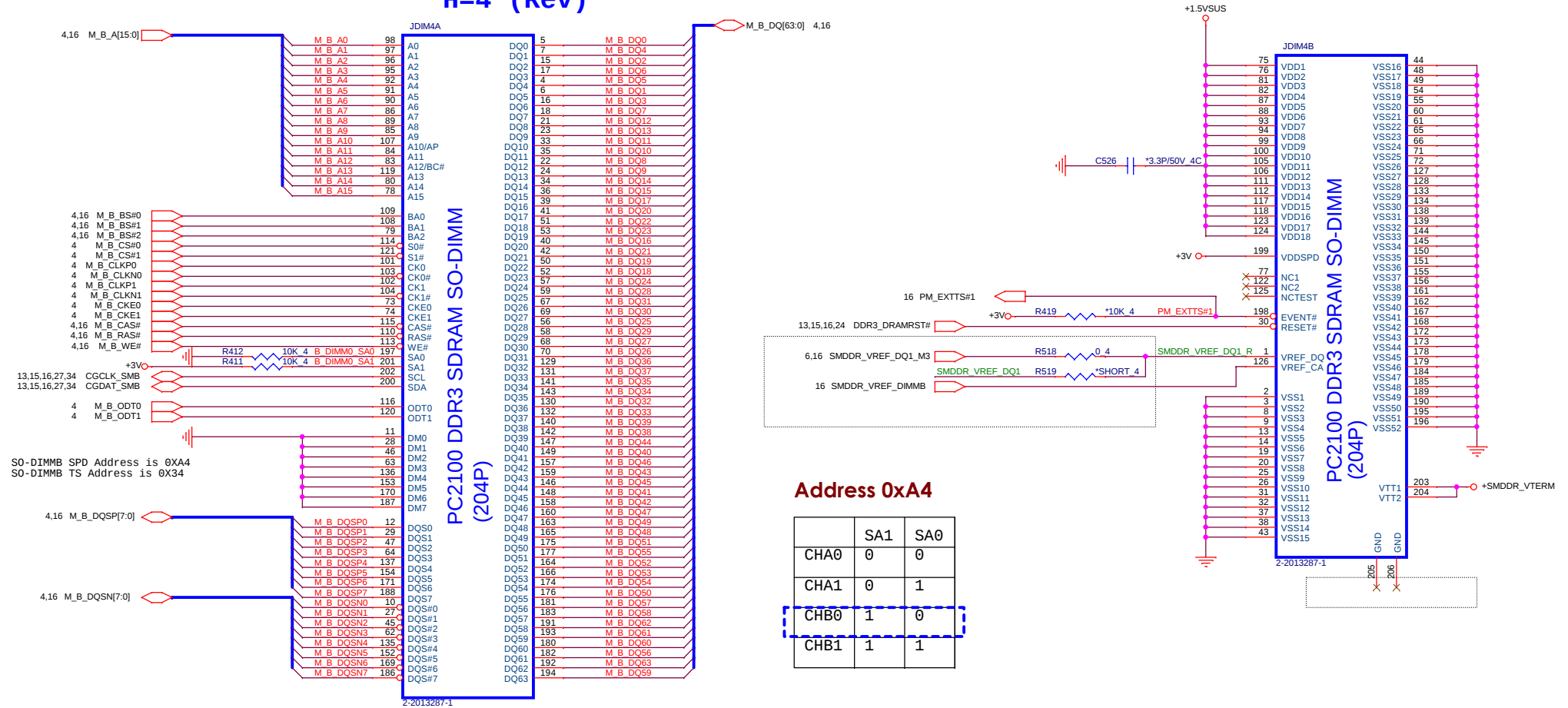


SMBUS ISOLATE

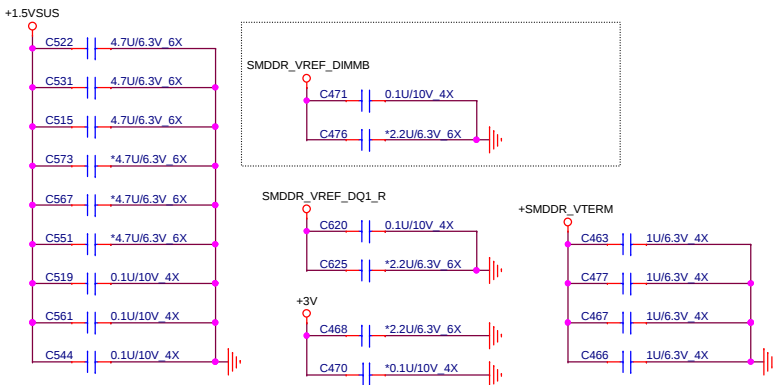


BOT Side Far Away CPU

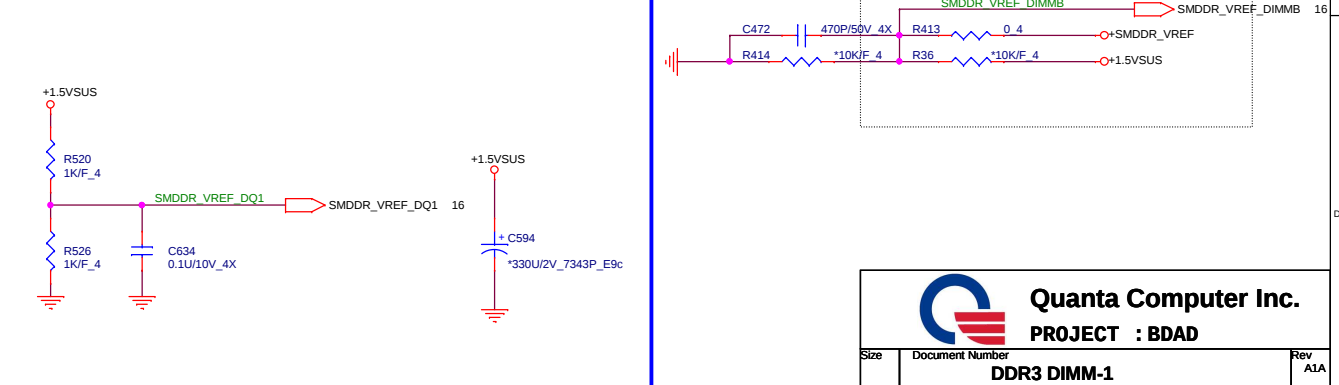
H=4 (Rev)



DDR Power Decoupling DDR



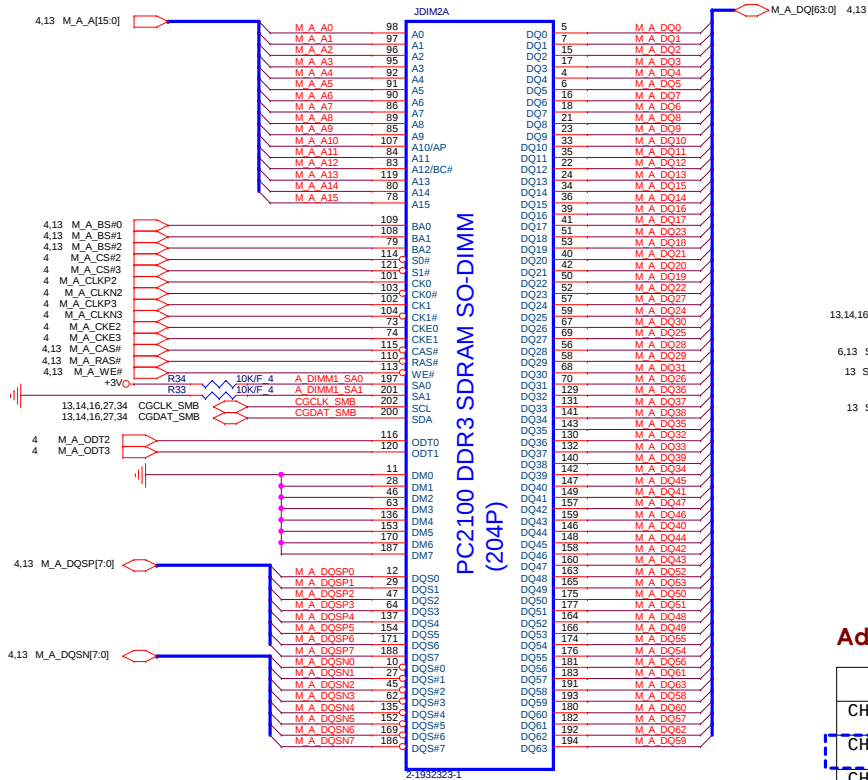
DDR3 VREF DQ (M1) DDR



TOP side Face to CPU

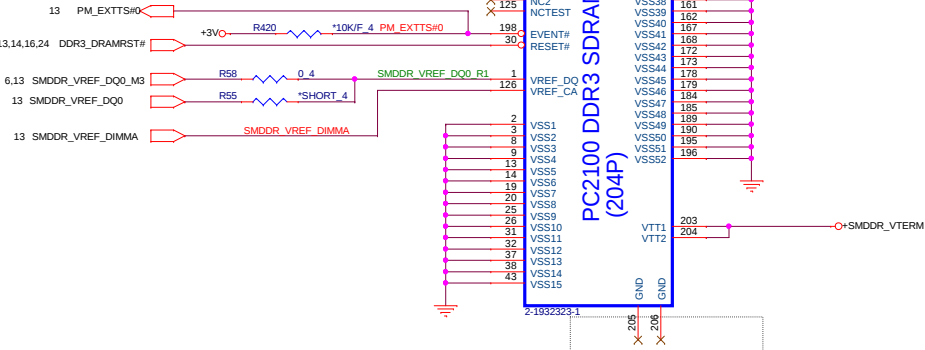
H=4

H=4

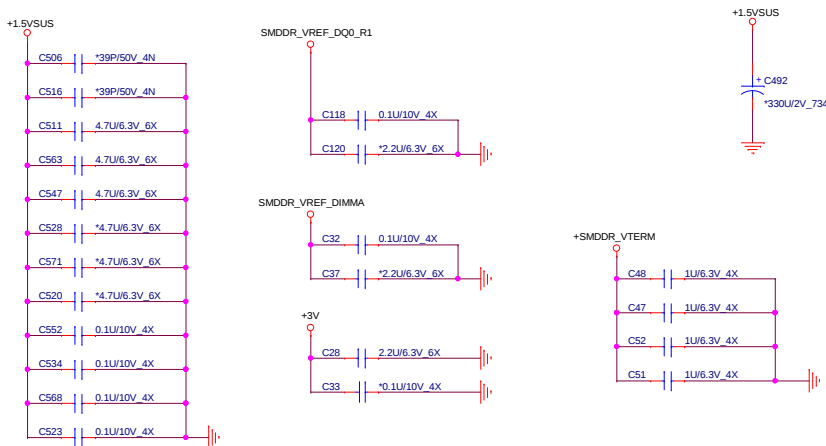


Address 0xA2

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Place these Caps near Memory Down-1

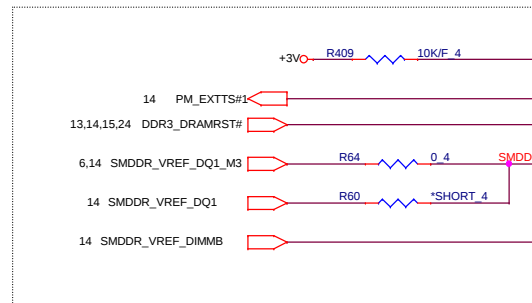
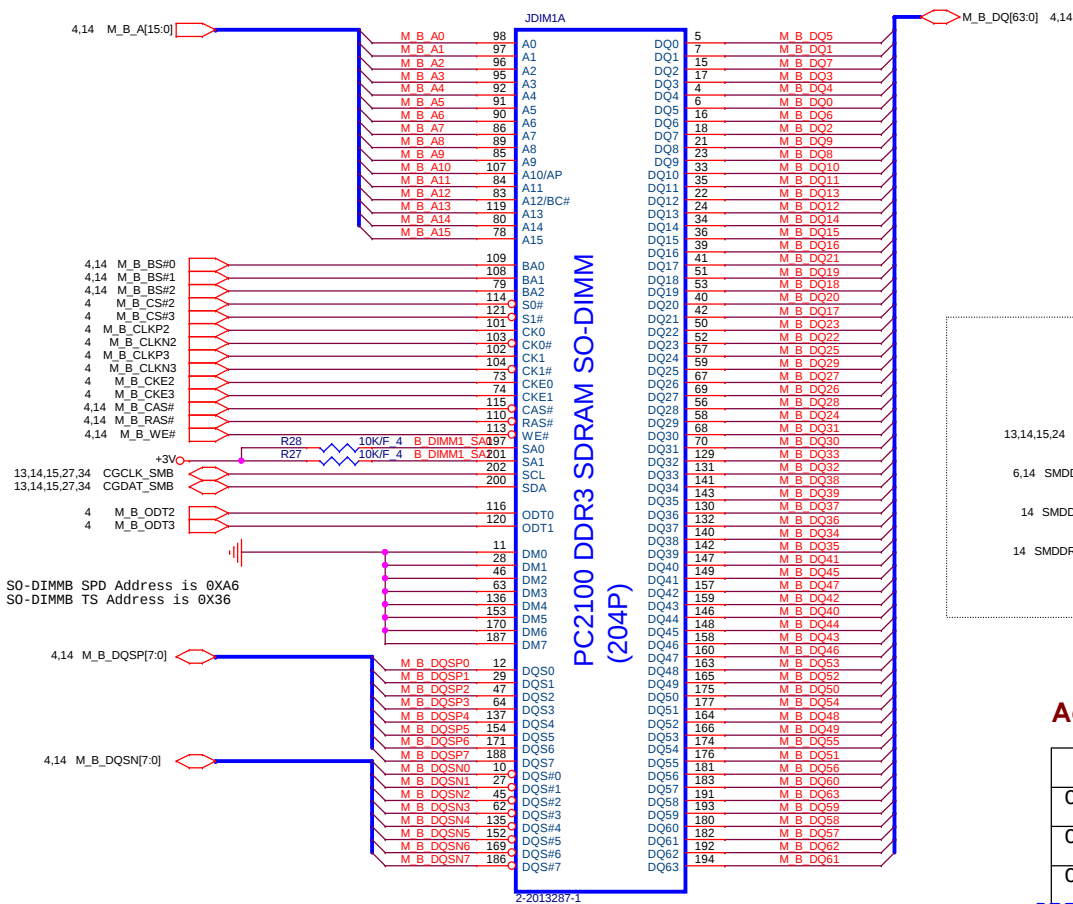


<DDR>

TOP Side Far Away CPU

H=4

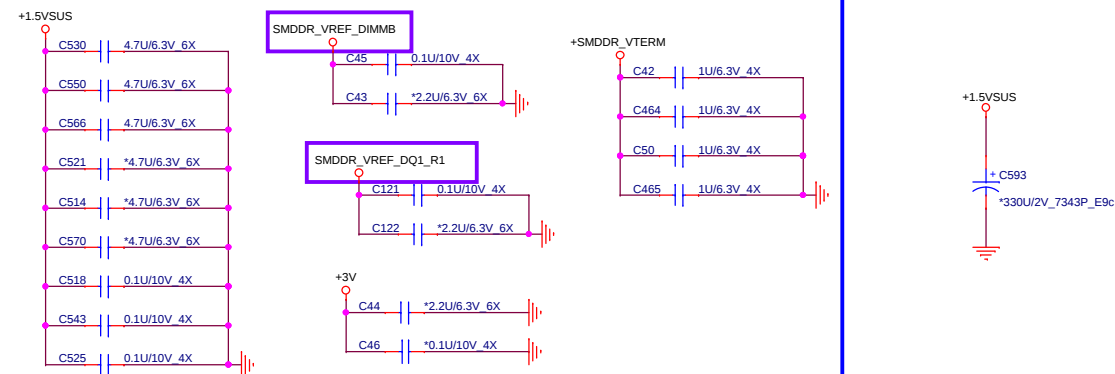
H=4

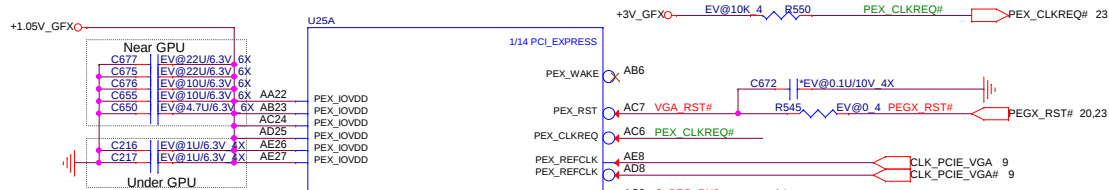
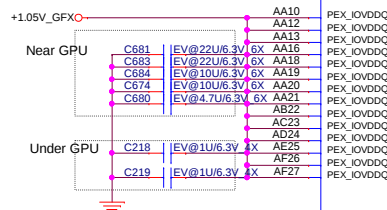


Address 0xA6

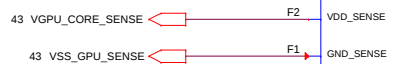
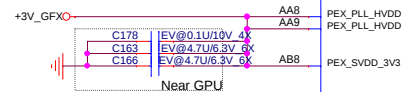
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Place these Caps near So-Dimm1.

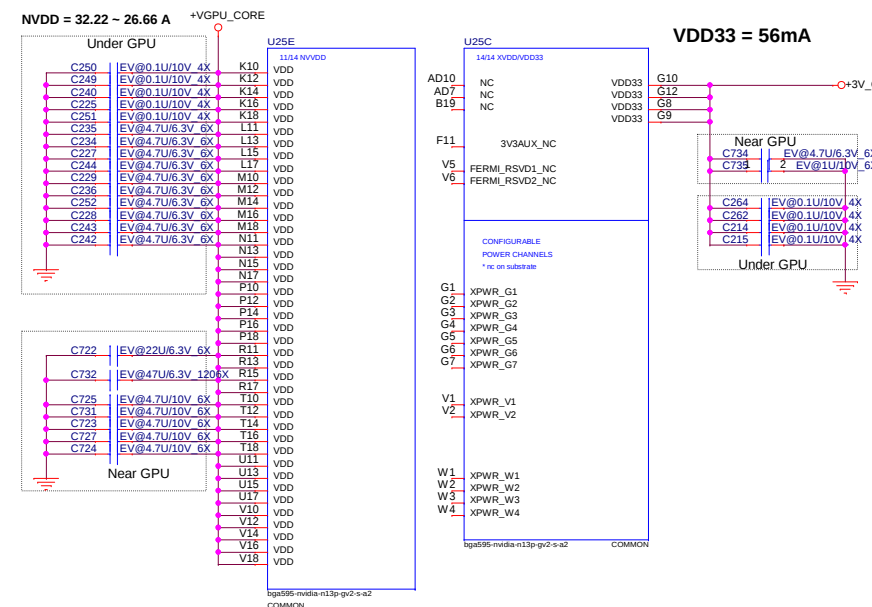
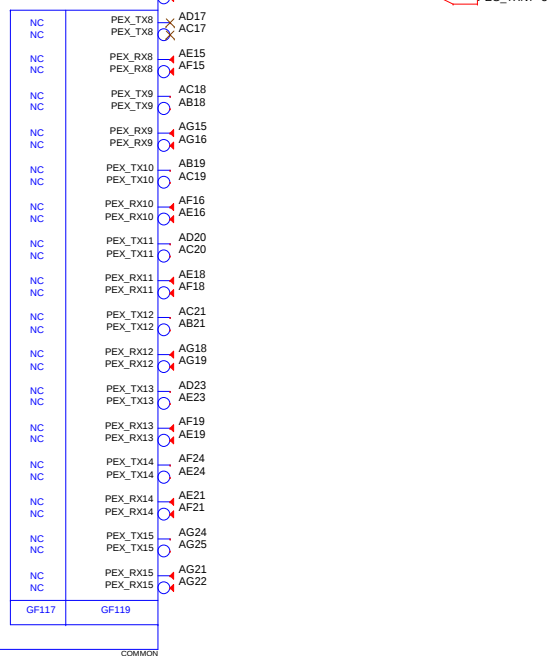
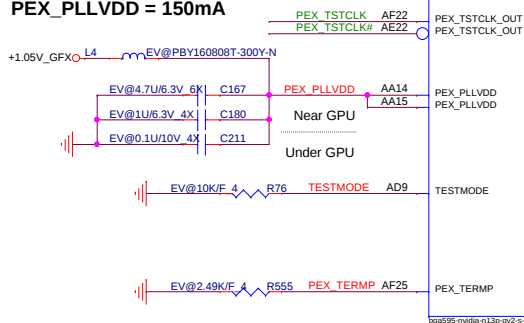



$$\text{PEX_IOVDD} + \text{PEX_IOVDDQ} = 3.5\text{A}$$


PEX_PLL_HVDD +
PEX_SVDD 3V3 = 210mA



PEX_PLLVDD = 150mA



Power up sequence

VDD33
+3V_GFX

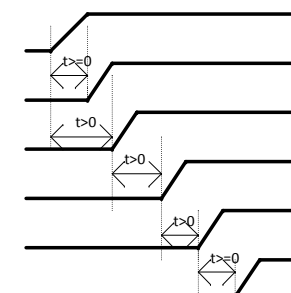
IFPx_IOVDD
+3V_GFX

NVVD
+VGPU_CORE

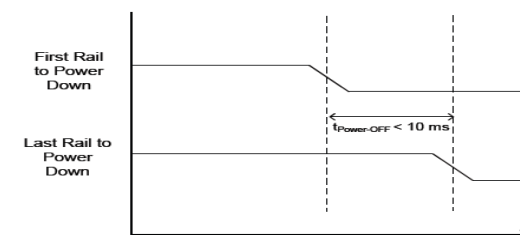
FBVDDQ
+1.5V_GFX

PEX_VDD
+1.05V_GFX

IFPy_IOVDD
+1.05V_GFX

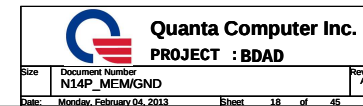


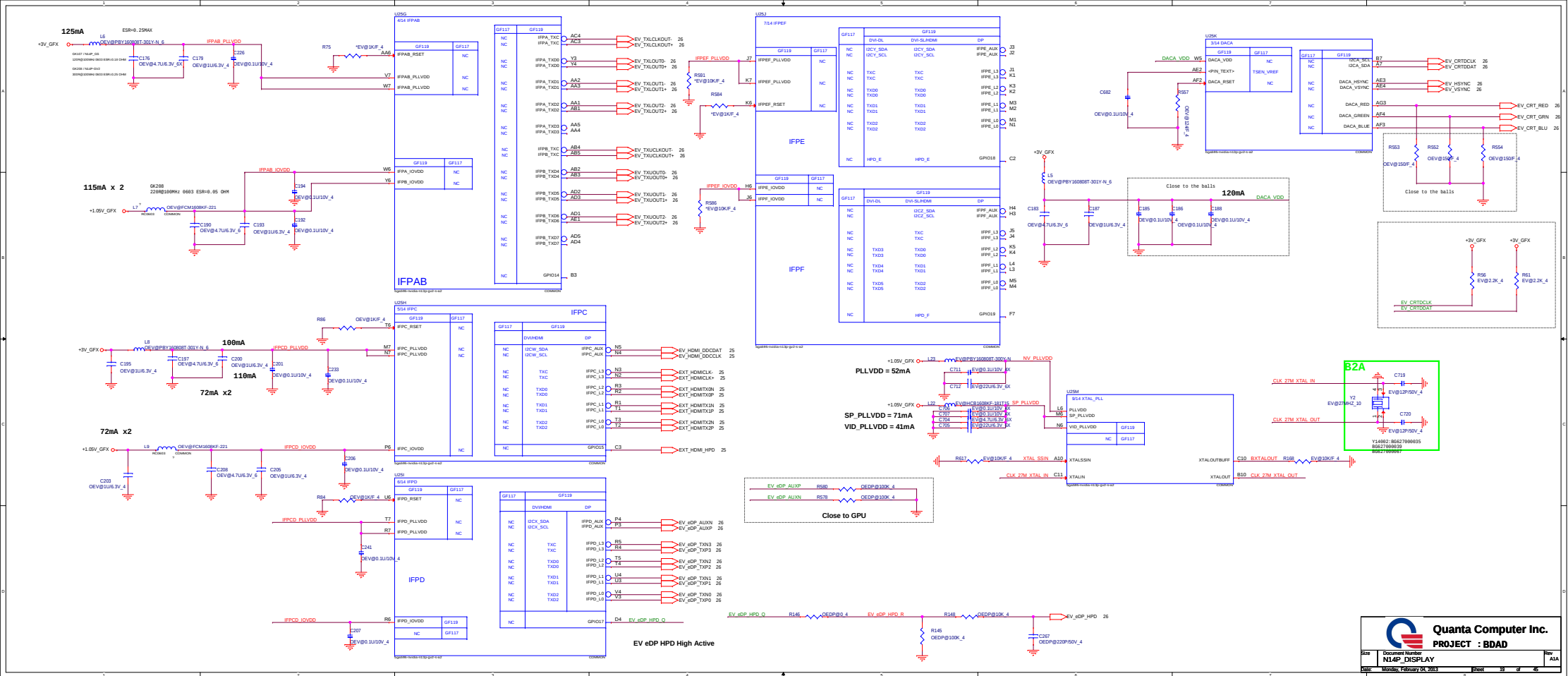
Power down sequence



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Size	Document Number N14P_PEG/NVDD	Rev A1
Date:	Monday, February 04, 2013	Sheet 17 of 45





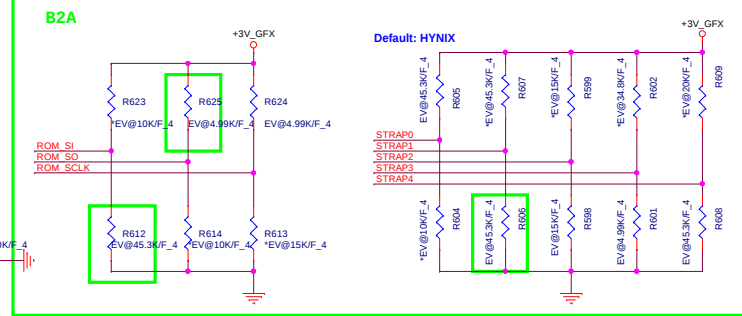
DDR3 Memory TYPE

Vendor	Vendor P/N	QCI P/N	Size	Max Speed CLK	ROM_SI
Samsung	K4W2G1646E-BC1A (128M*16)	0x7	2GB	1000MHZ	PD 45K
	K4W2G1646E-BC11 (128M*16)	0x7	2GB	900MHZ	PD 45K
	K4W4G1646B-HC11 (256M*16)	0x3	4GB	900MHZ	PD 20K
Micron	MT41J128M16JT-093G:K (128M*16)	0x5	2GB	1000MHZ	PD 30K
	MT41J128M16JT-107G:K (128M*16)	0x5	2GB	900MHZ	PD 30K
	MT41K256M16HA-107G:E (256M*16)	0x1	4GB	900MHZ	PD 10K
Hynix	H5TQ2G63DFR-N0C (128M*16)	0x6	2GB	1000MHZ	PD 35K
	H5TQ2G63DFR-11C (128M*16)	0x6	2GB	900MHZ	PD 35K

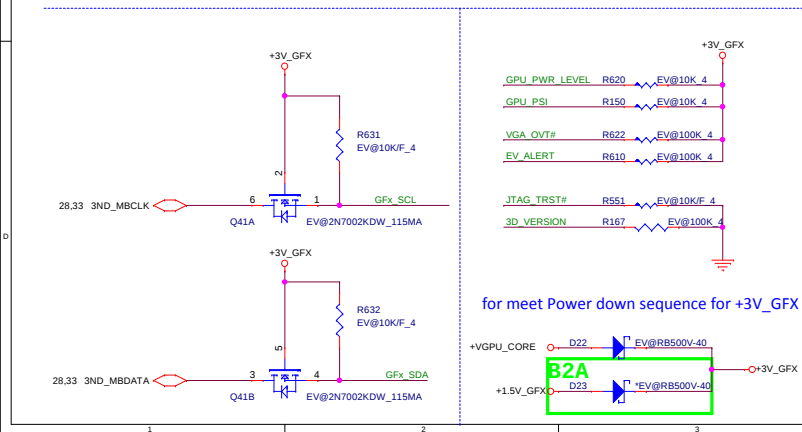
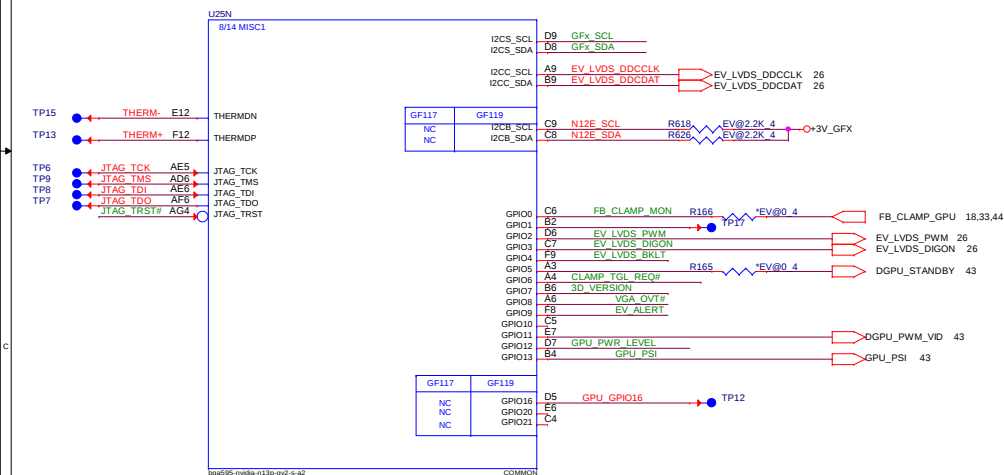
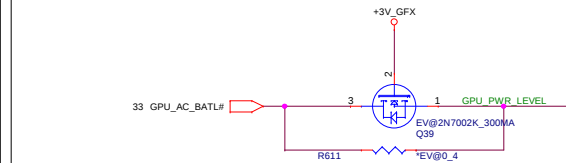
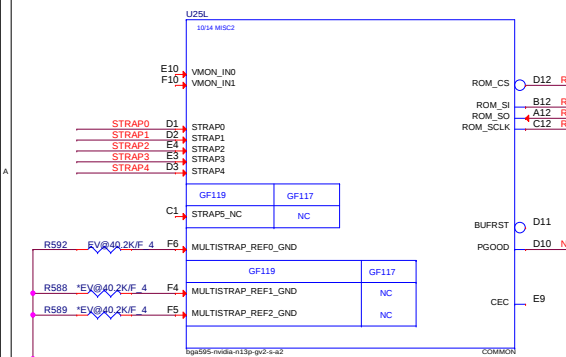
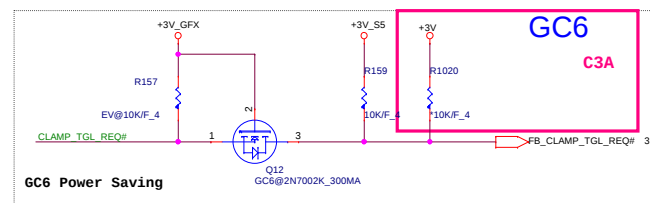
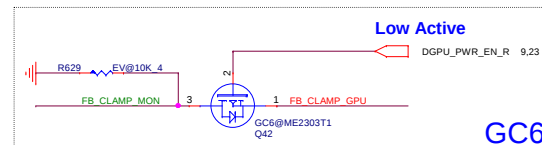
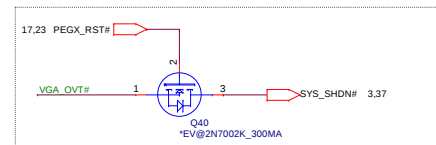
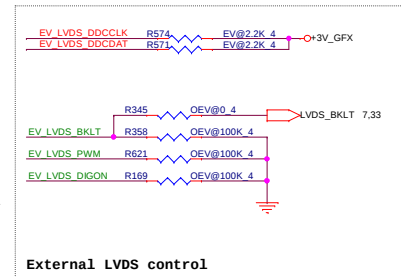
4.99K/F 4: CS24992FB26 RES CHIP 1/16W +1% (0402)
 10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
 15K/F 4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
 20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)
 30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)
 34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)
 45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

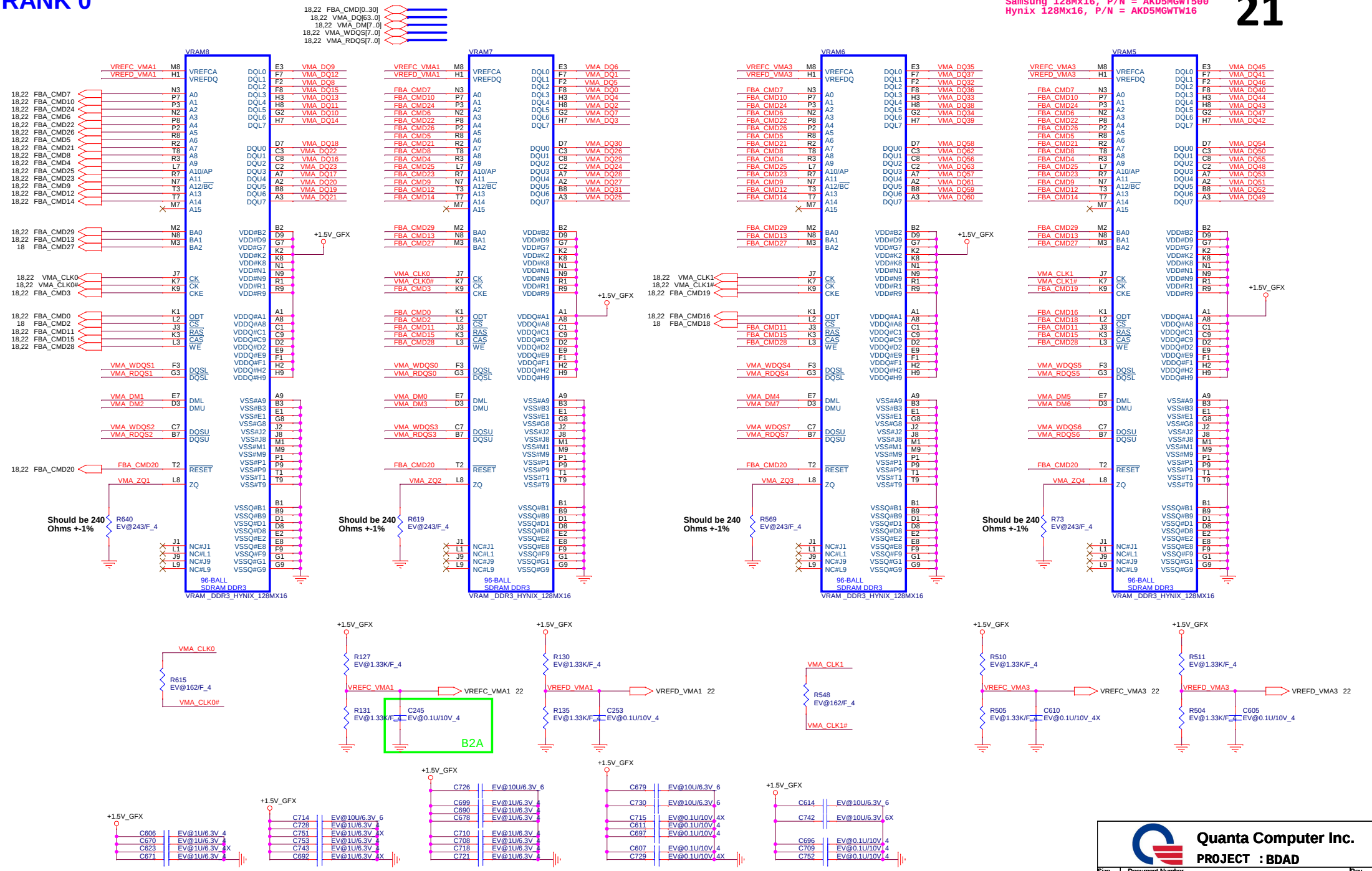
GPIO ASSIGNMENTS

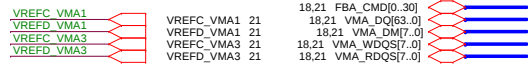
GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect , HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	



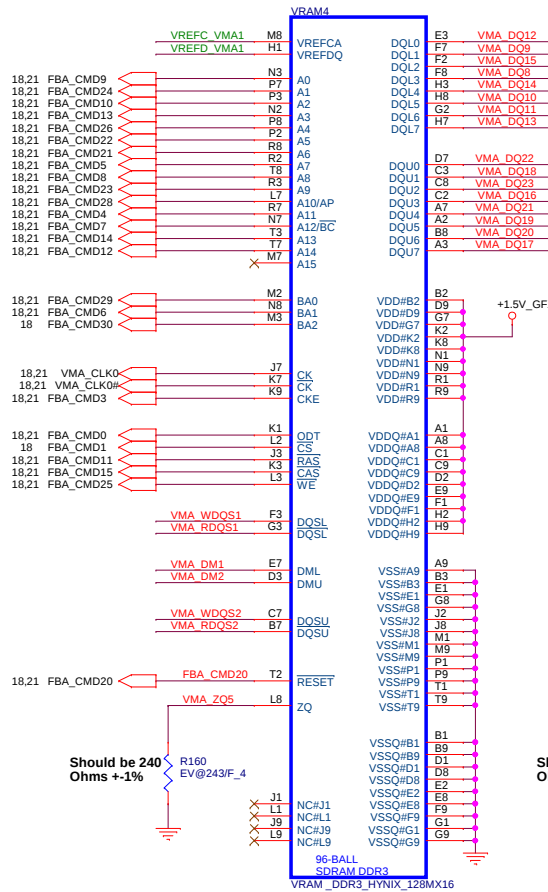
Netname	N14P-GV2	
ROM_S0	10K PU	5kohm PU for Optimus, 10K PU for Discrete
ROM_SCLK	5K PU	0x1000, 0x8, 4.99kohm pull up
STRAP0	45K PU	user strap, 0xF, 45kohm pull up
STRAP1	5K PD	5K PD for QS, 45K PD for after QS
STRAP2	15K PD	Device_ID, 0x0010_15K pull down
STRAP3	5K PD	0x0 for optimus, 5k PD. 0010 for Discrete, 15K PD
STRAP4	45K PD	0x111, 45kohm pull down



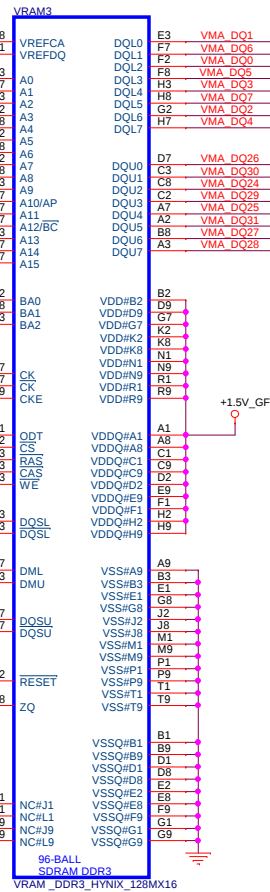
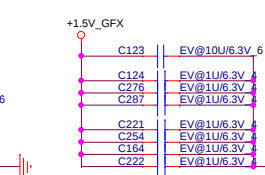




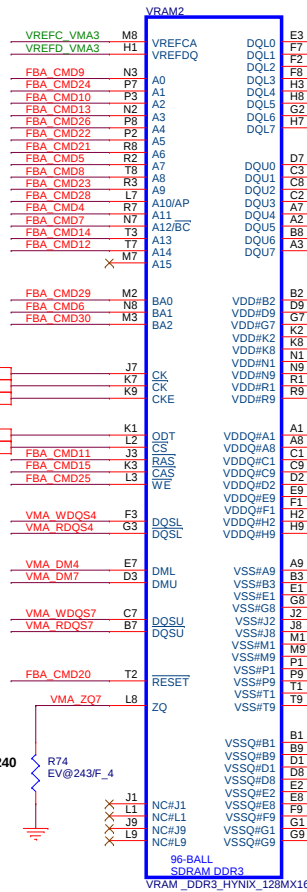
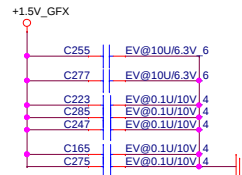
18.21 FBA_CMD0[30]
18.21 VMA_DQ[63,0]
18.21 VMA_DM[7,0]
18.21 VMA_WDQS[7,0]
18.21 VMA_RDQS[7,0]



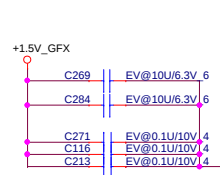
Should be 240 Ohms +1%



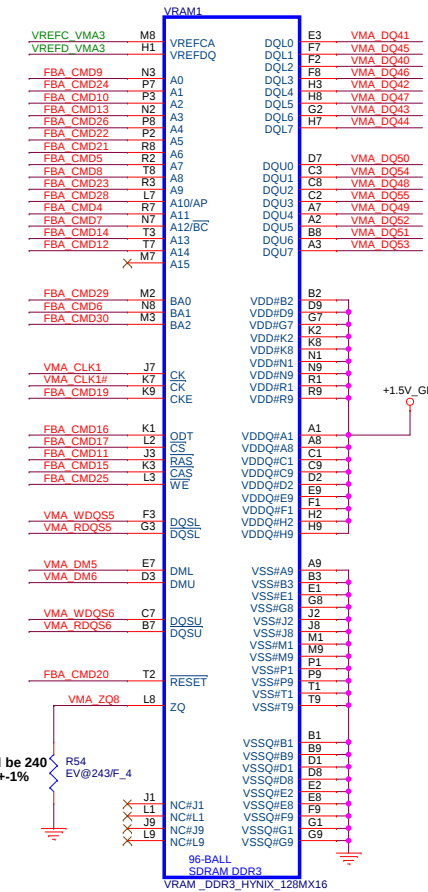
Should be 240 Ohms +1%



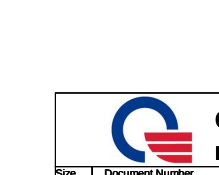
Should be 240 Ohms +1%



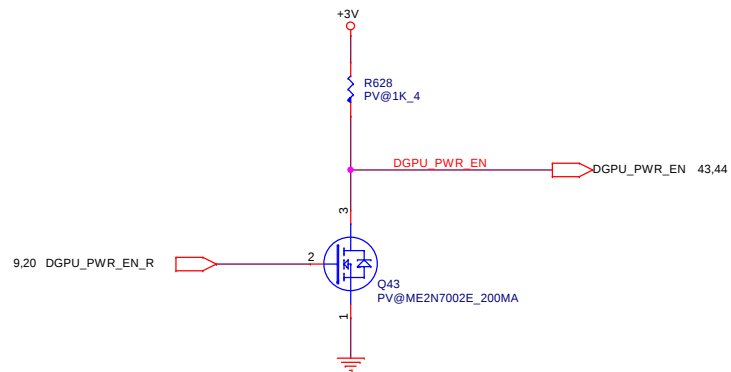
900MHz VRAM size:
Samsung 128Mx16, P/N = AKD5MGWT509
Hynix 128Mx16, P/N = AKD5MGWTW16



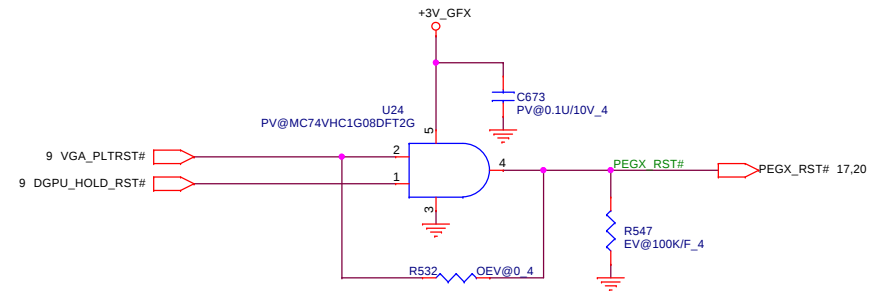
Should be 240 Ohms +1%



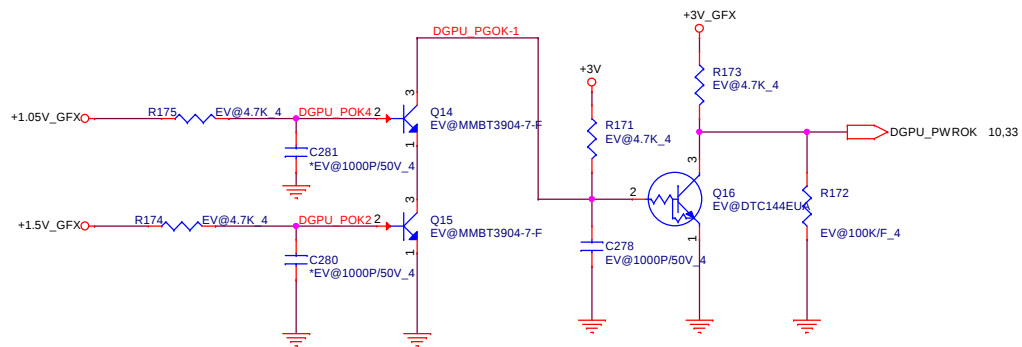
VGA Power Enable Reverse (Intel --> Low Active)



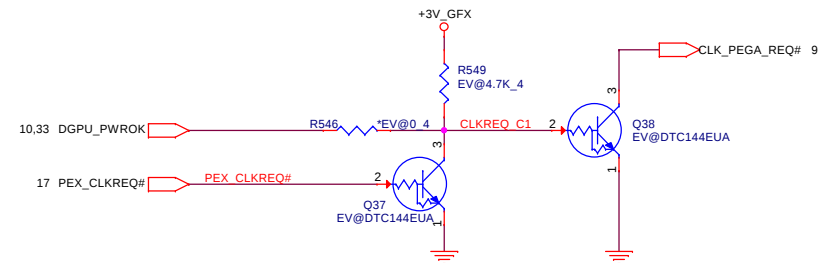
Platform Reset



GPU Power Good



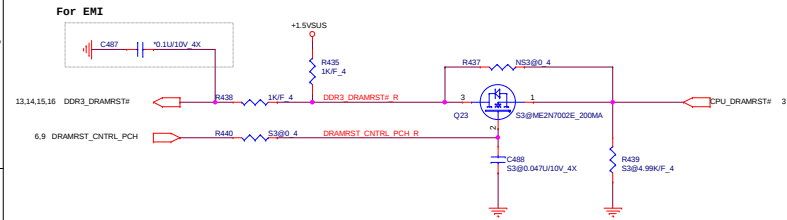
GPU CLOCK REQ



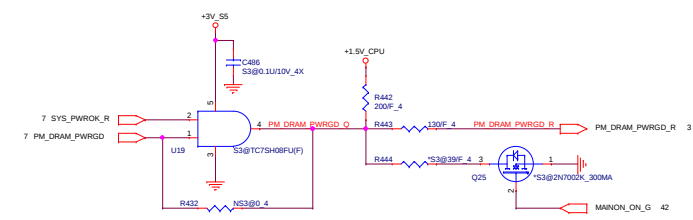
Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	Blank	A1A
Date:	Monday, February 04, 2013	Sheet 23 of 45

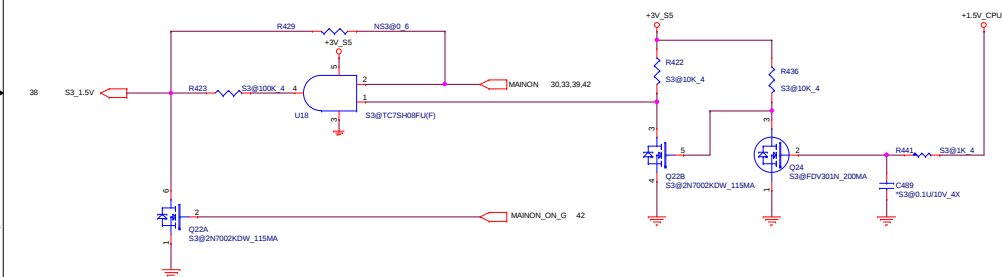
S3 power Reduction (SM_DRAMRST#) S3P/NS3P/CPU



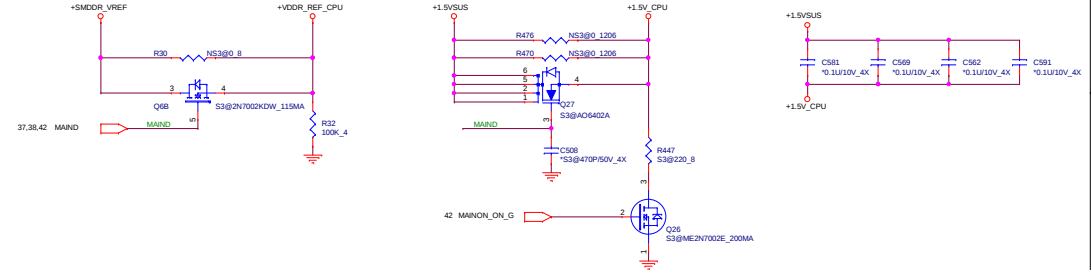
S3 power Reduction (SM_DRAMPWR0K) S3P/NS3P/CPU



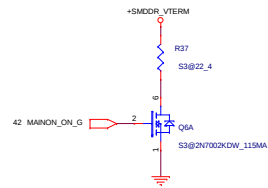
For S3 power Reduction Sequence S3P/NS3P/CPU

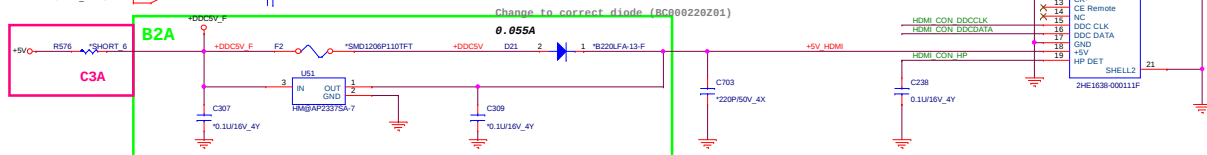


S3 power Reduction (CPU Power) S3P/NS3P/CPU

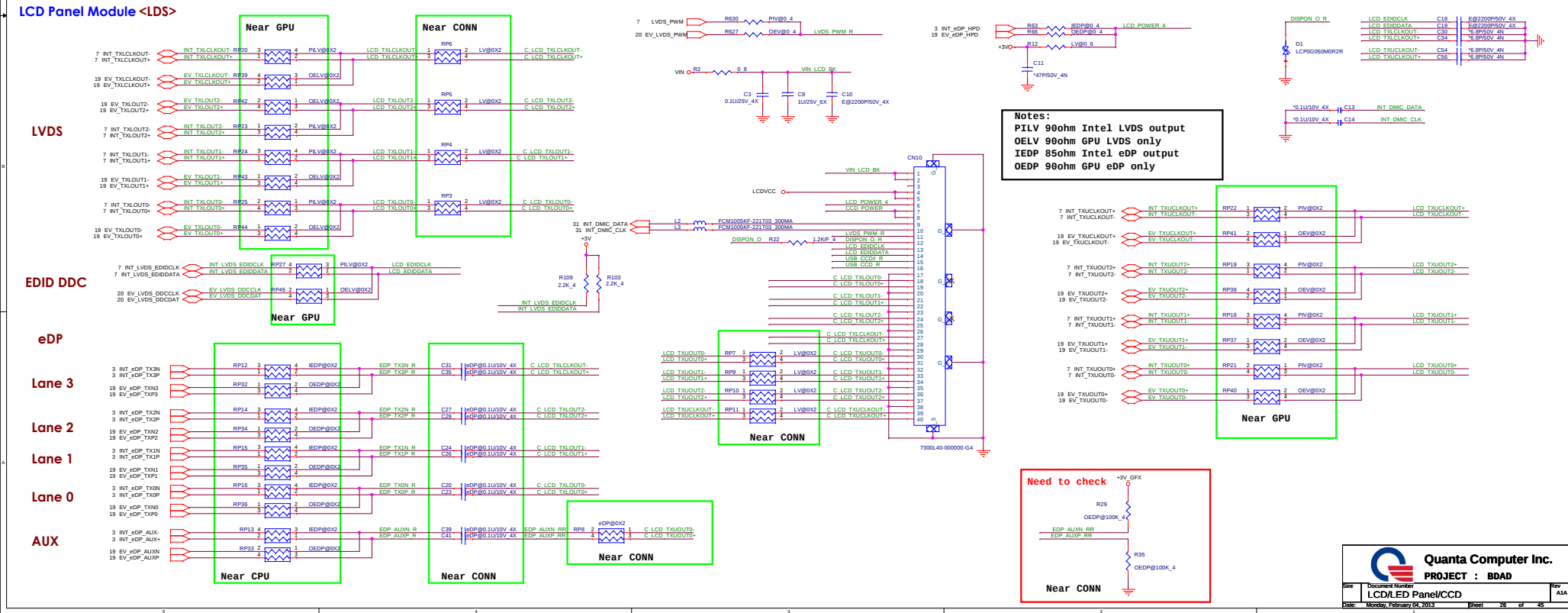
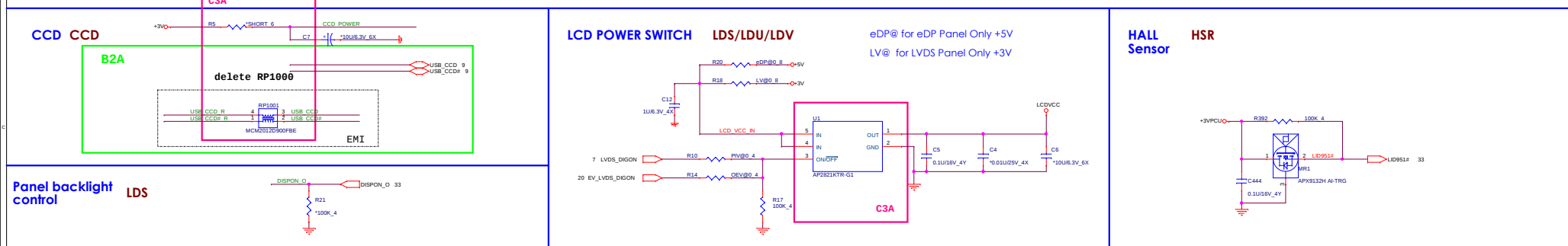
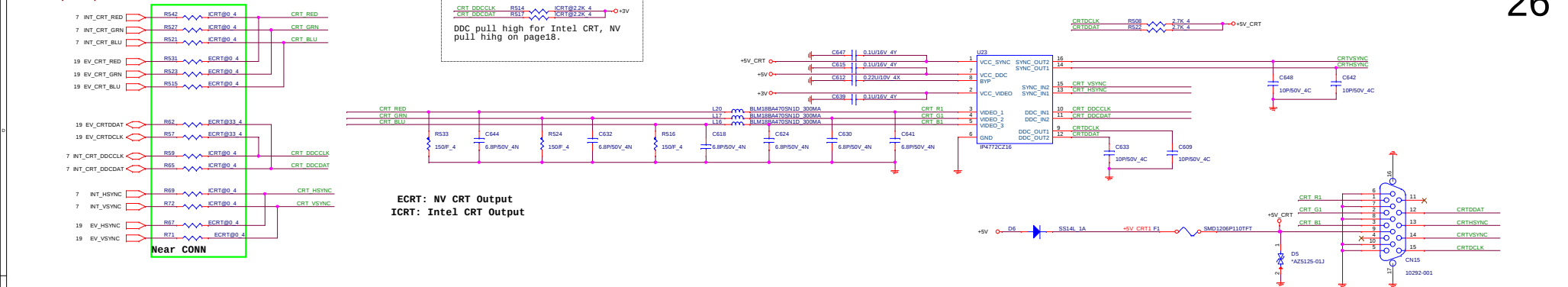


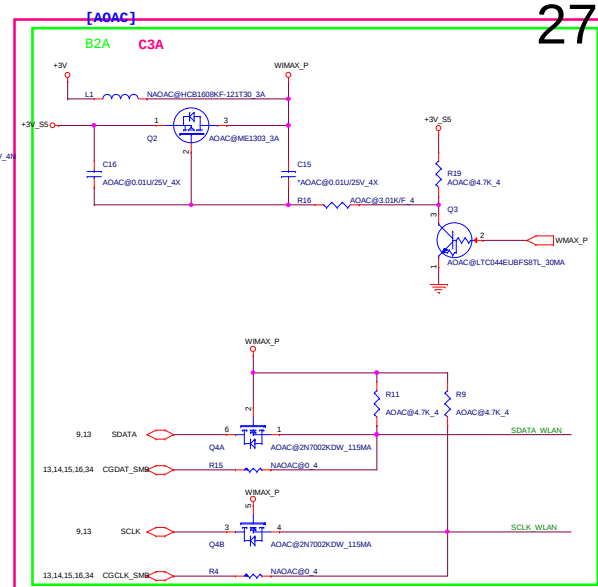
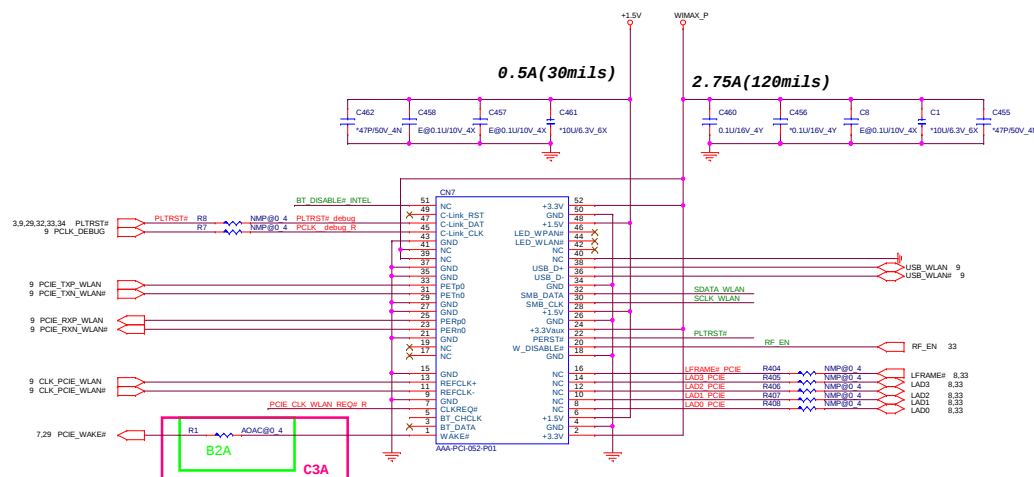
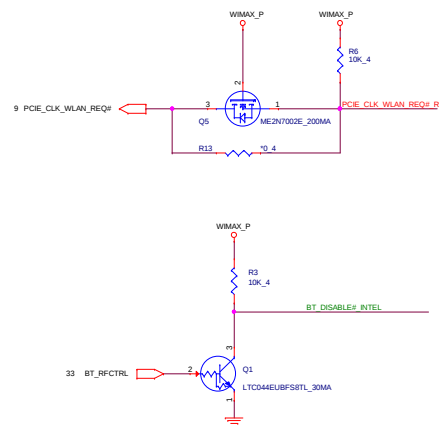
For S3 power Reduction VTT discharge S3P/NS3P/CPU



[illegible][illegible]

The schematic diagram illustrates the HDMI input section, divided into two channels: B2A and B2B. Channel B2A (left) features a 7-pin HDMI connector (HDMI_DDCCLK) and a 19-pin EV_HDMI connector (EV_HDMI_DDCCLK). The B2A channel includes a power supply section with +3V_HDMI and +3V_GFX inputs, a +3V_HDMI output, and a +DDCSV_F input. The B2B channel (right) features a 7-pin HDMI connector (HDMI_DDCDATA) and a 19-pin EV_HDMI connector (EV_HDMI_DDCDATA). The B2B channel includes a power supply section with +3V_HDMI and +DDCSV_F inputs. Both channels include a 7-pin HDMI connector (HDMI_DDCCLK) and a 19-pin EV_HDMI connector (EV_HDMI_DDCCLK). The B2A channel includes a power supply section with +3V_HDMI and +3V_GFX inputs, a +3V_HDMI output, and a +DDCSV_F input. The B2B channel includes a power supply section with +3V_HDMI and +DDCSV_F inputs. Both channels include a 7-pin HDMI connector (HDMI_DDCCLK) and a 19-pin EV_HDMI connector (EV_HDMI_DDCCLK).

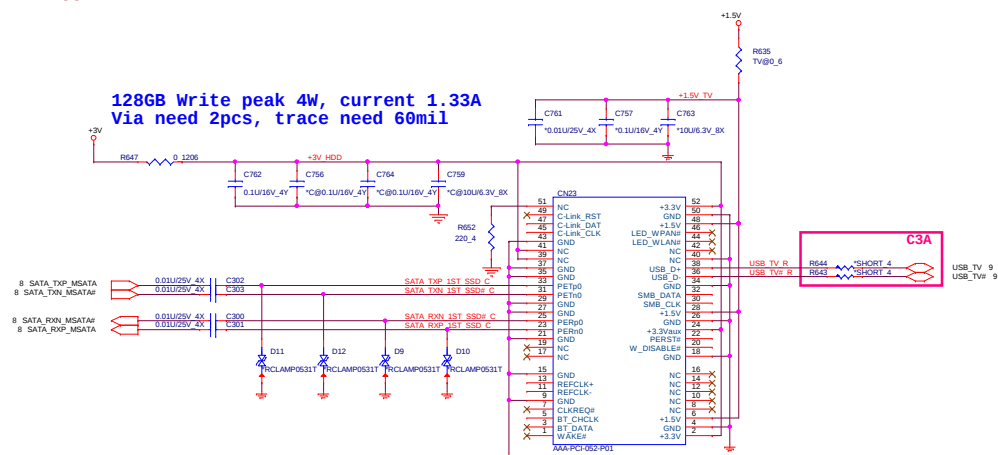




TV Tuner / MSATA

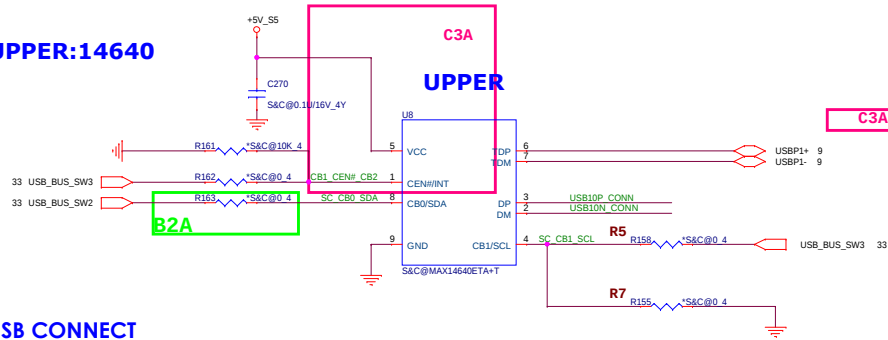
<SSD>

TV Tuner: 1.5V@240mA 3.3V@470mA



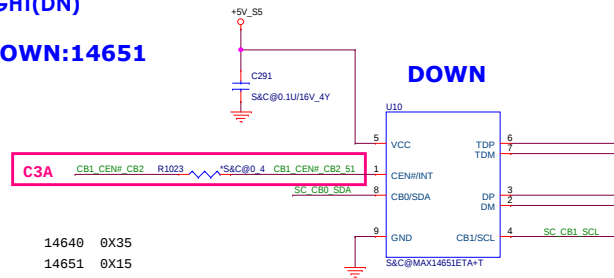
USB CONNECT <U3B/USB> RIGHT(UR)

UPPER:14640



USB CONNECT RIGHT(DN)

DOWN:14651

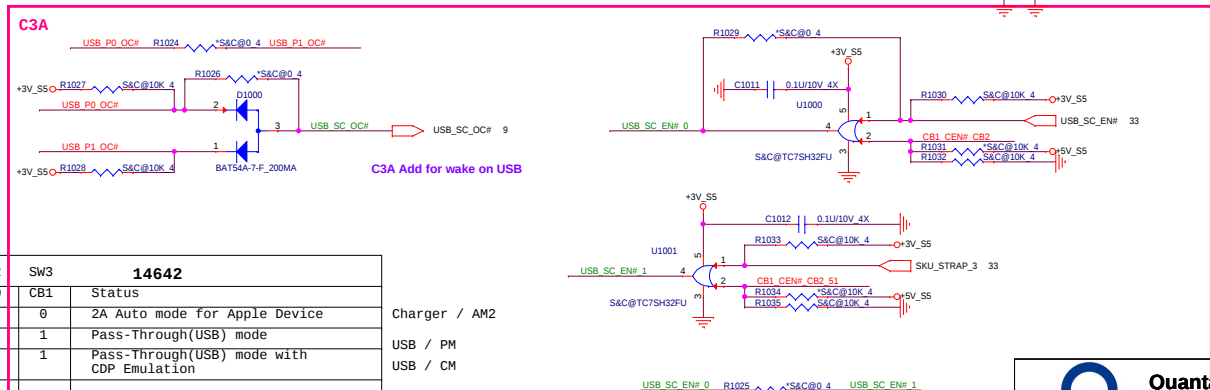


	R1	R2	R3	Q5018	R5	Q5018	R7	R8
14566		V	V		V		V	
14600		V	V		V		V	
14617(with CB2)	V		V		V			V
14617(no CB2)			V		V			
14641/42/44			V		V			
14640			V		V			

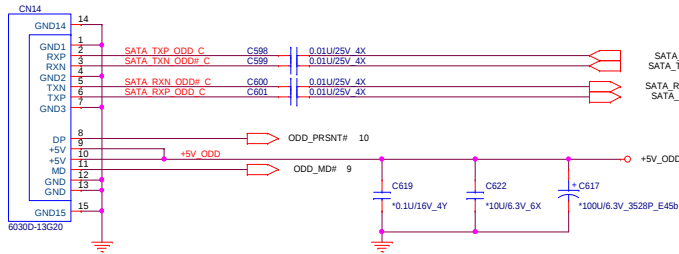
I2C Control				14640/14651	
2	1	0	Status		
0	0	0	2A Auto mode for Apple Device	Charger / AM2	
0	0	1	Pass-Through(USB) mode	USB / PM	
0	1	0	Force dedicated charger mode	Charger / FM	
0	1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM	
1	0	0	1A Auto mode for Apple Device	Charger / AM1	
1	0	1	1A Forced mode for Apple Device	Charger / AP1	
1	1	0	2A Forced mode for Apple Device	Charger / AP2	
1	1	1	2A Forced mode for Samsung Device	Charger / SS	

SW2	SW3	14644	
CB0	CB1	Status	
0	0	2A Auto mode for Apple Device	Charger / AM2
1	0	Force dedicated charger mode	Charger / FM
0	1	Pass-Through(USB) mode	USB / PM
1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM

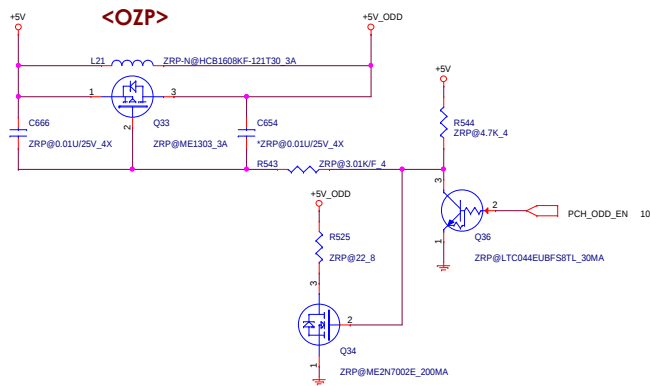
SW2	SW3	14642	
CB0	CB1	Status	
X	0	2A Auto mode for Apple Device	Charger / AM2
0	1	Pass-Through(USB) mode	USB / PM
1	1	Pass-Through(USB) mode with CDP Emulation	USB / CM



SATA ODD <ODD>

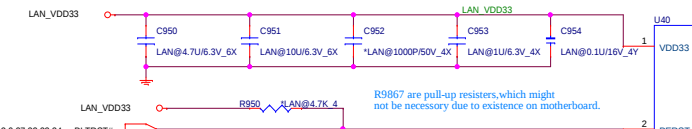


ODD Zero power . (Only for Intel)



AR8161-BL3A-RL = AL008161003

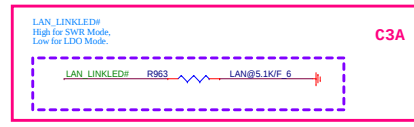
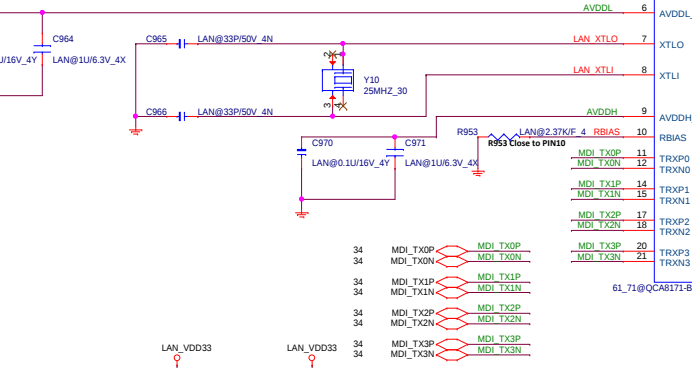
277mA(30mils)



Atheros

AR8161/AR8162

QCA8171/QCA8172

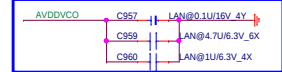


pin38, pin39 & pin23
(LED0, LED1 & LED2) has internal pull up.

The pin 38 "LED0" doesn't pull down
to choose low core voltage. (It's internal pull up)
by FAE's command.20120914

AR8161/8162 Pin 23 for LAN LED, No use NC.

AVDDVCO add C957,C959,C960 by FAE's command.20120914

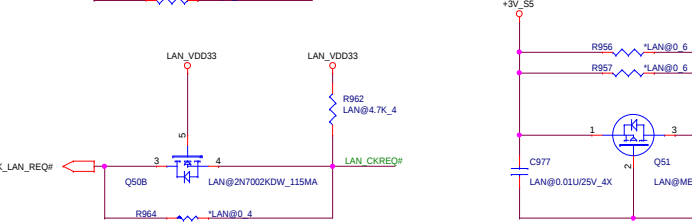


If AVDDL/DVDDL comes from internal SWR:
mount L5036.
But,if comes from internal LDO, no mount.

If AVDDL/DVDDL comes from internal SWR:
mount L5035, C5467, C5468, C5469.
But,if comes from internal LDO, no mount.



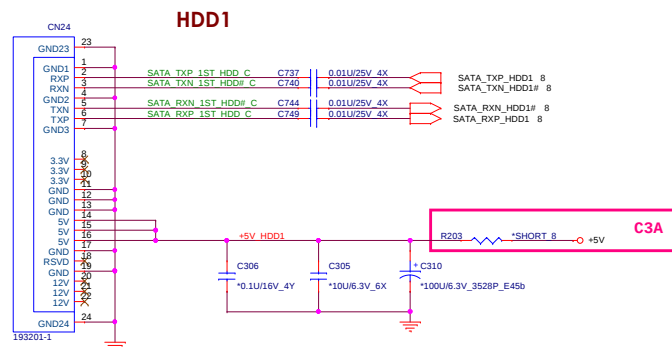
LAN-Wake up Power Control Circuit



LED0 = LAN_ACTLED	1	High core voltage. (default = 1)
	0	Low core voltage.
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select
	0	LDO linear regulator select (default = 0)
LED2 = EXTCLK Use Xta1=>NC	1	25MHz External clock input
	0	48MHz External clock input

SATA HDD1

HDD1

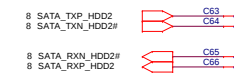


2nd HDD SATA Re-driver

Layout Note: Closed to IC

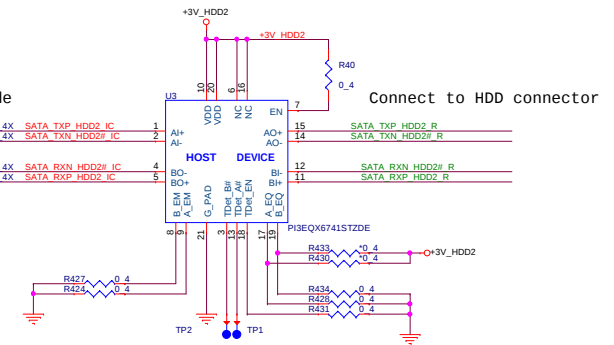


Connect to PCH side



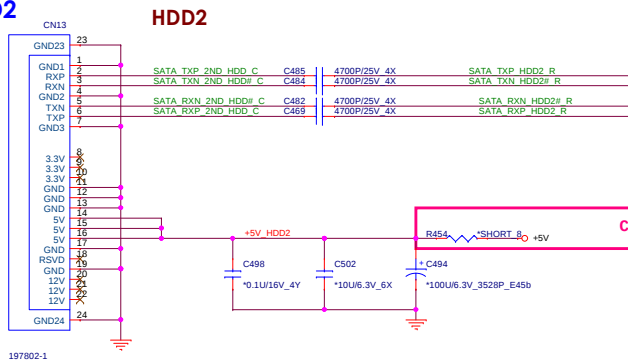
A_EQ	B_EQ	1.5 Gb/s	3 Gb/s	6 Gb/s
0	0	1 bB	2.5 bB	3 bB
1	1	4 bB	7.5 bB	9 bB
floating		2.5 bB	5 bB	6 bB

A_EM	B_EM	3 Gb/s	6 Gb/s
0	0	550mV pp	650mV pp
1	1	550mV pp+3dB Pre-emphasis	650mV pp+1.5dB Pre-emphasis

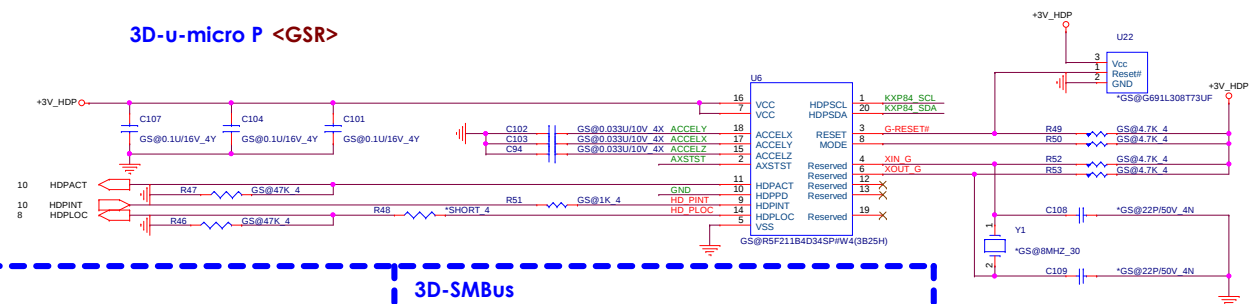


SATA HDD2

HDD2



3D-u-micro P <GSR>

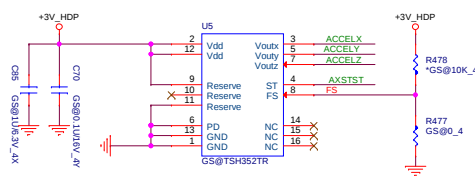
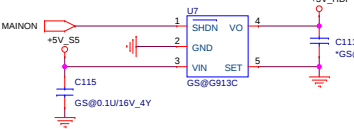


3D-Sensor IC

<GSR>

3D-LDO Power <GSR>

0.3A



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

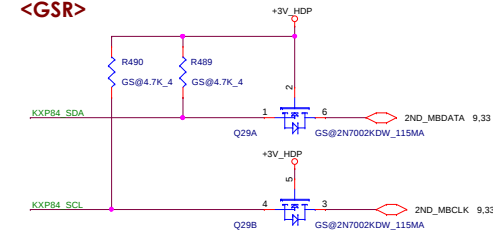
PD	0	1
	Normal Mode	Power-down mode

HDDPD selection

HDDPD	0	1
	Normal Mode	Power-down mode

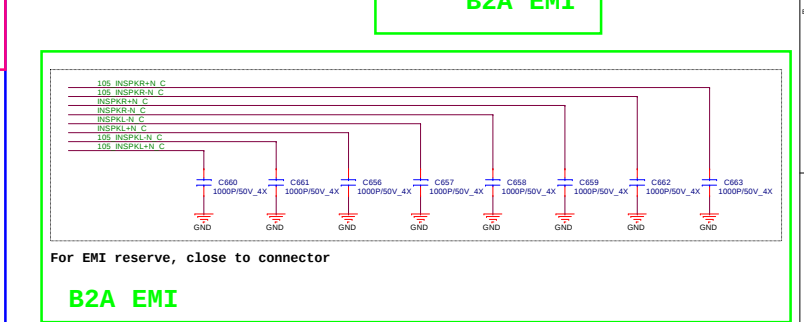
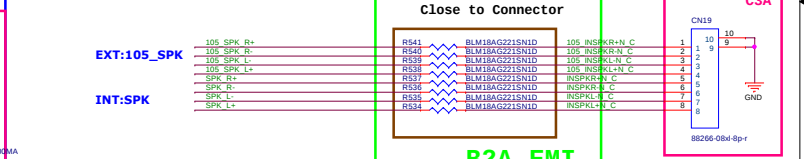
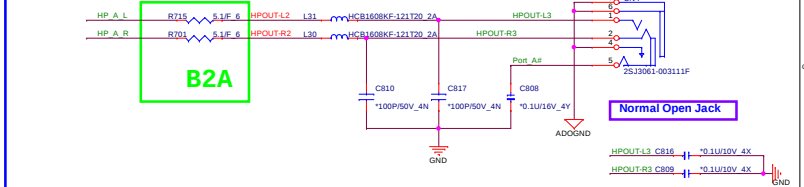
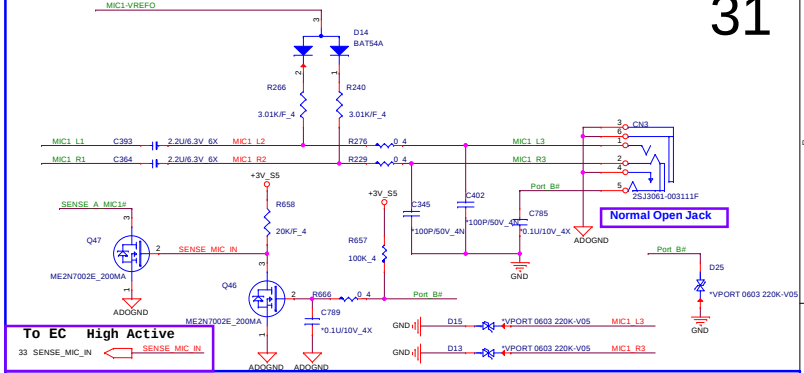
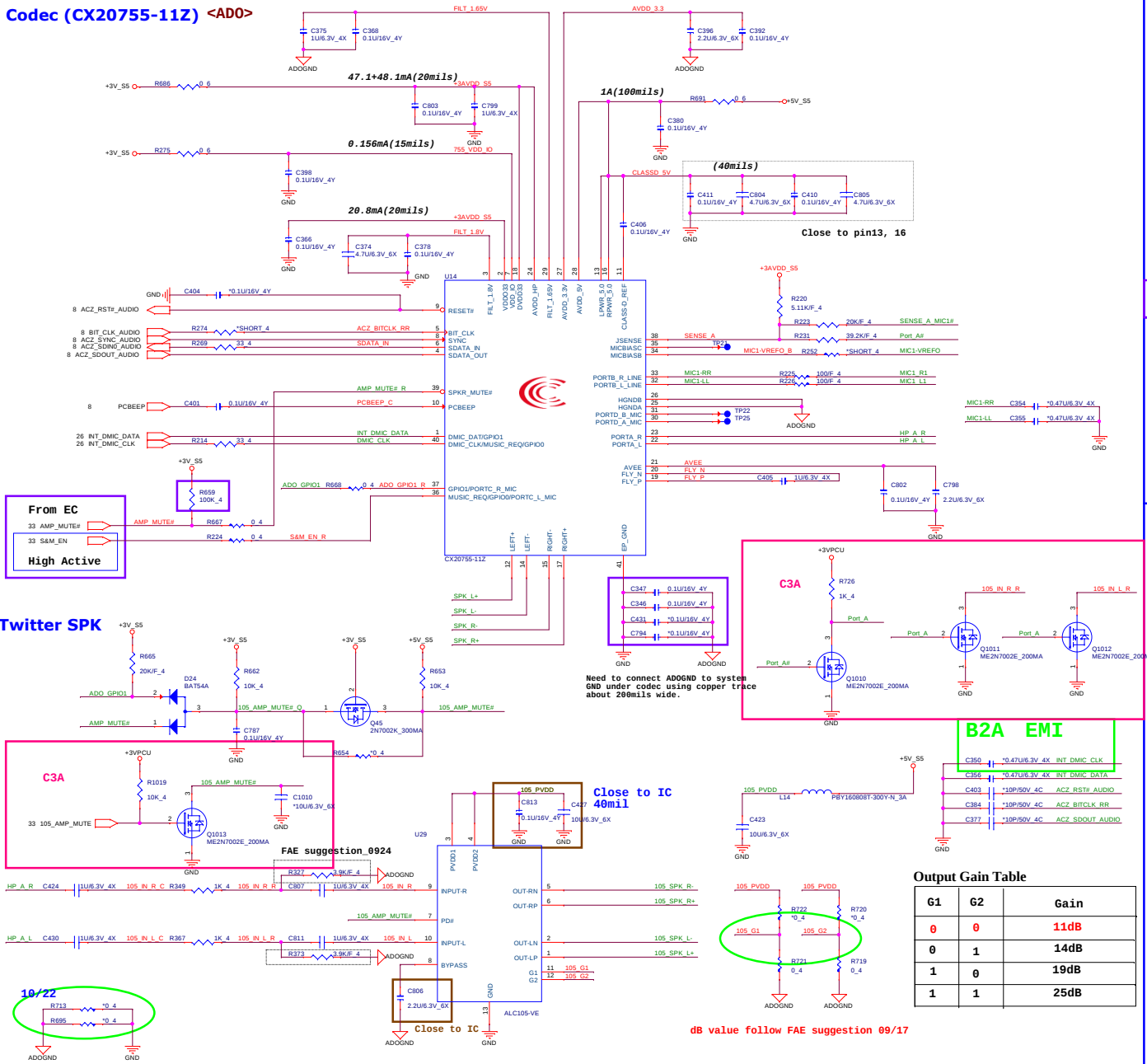
3D-SMBus

<GSR>

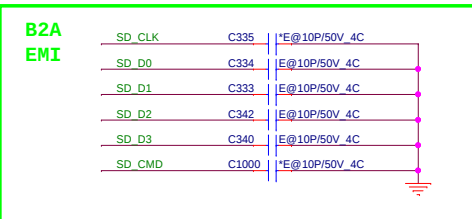


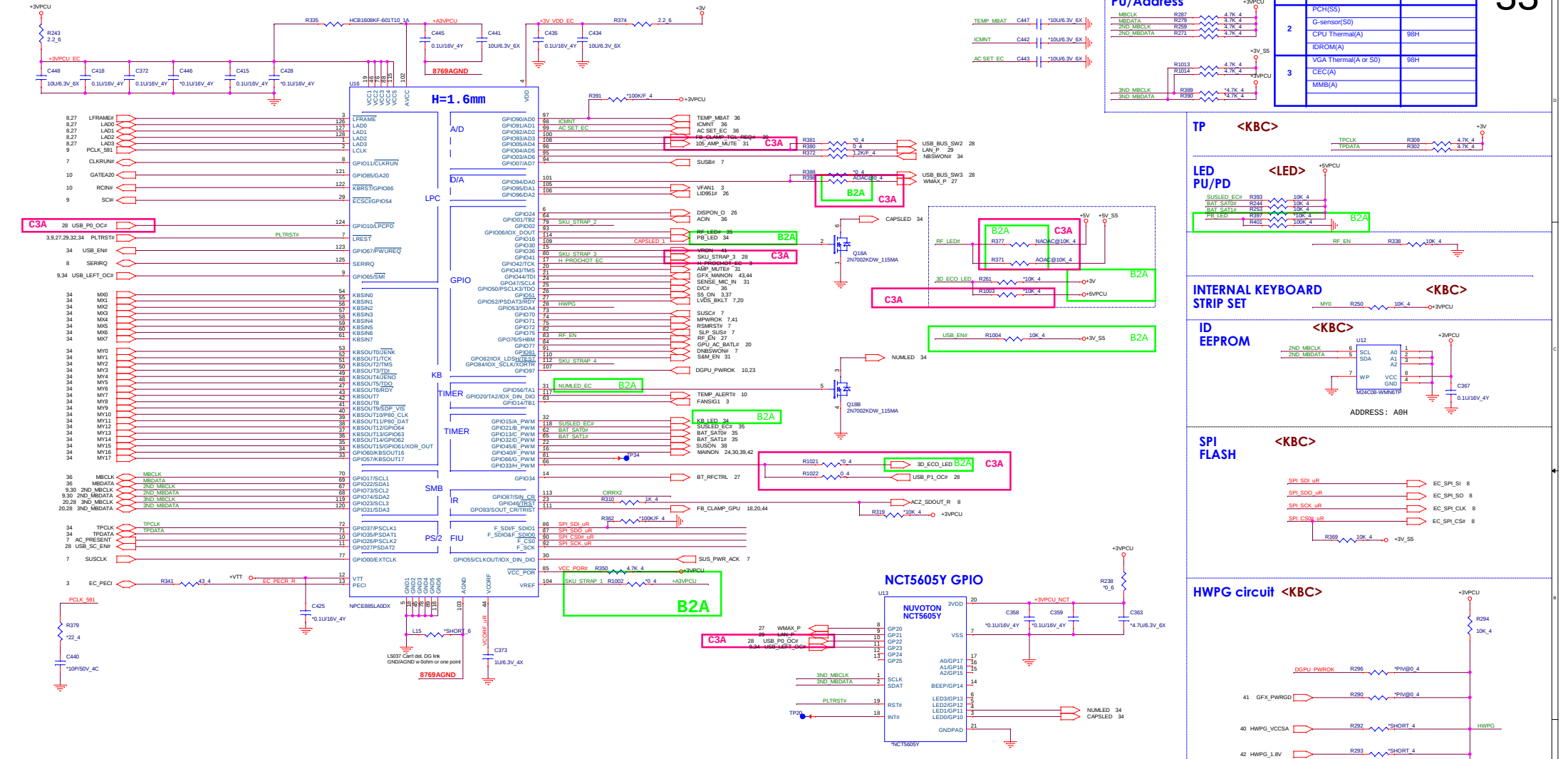
Size Document Number
HDD/ODD/G-Sensor

Date: Monday, February 04, 2013 Sheet 30 of 45

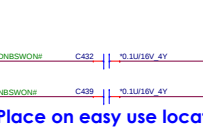


G1	G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB





Power Button <KBC>



Place on easy use location

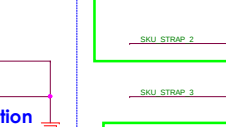


Power Button <KBC>



Power Button <KBC>

Power Button <KBC>



Place on easy use location



Power Button <KBC>



Power Button <KBC>

Power Button <KBC>



Place on easy use location



Power Button <KBC>



Power Button <KBC>

Power Button <KBC>



Place on easy use location

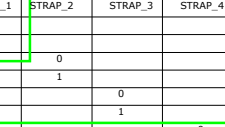


Power Button <KBC>



Power Button <KBC>

Power Button <KBC>



Place on easy use location

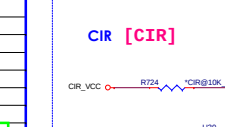


Power Button <KBC>



Power Button <KBC>

Power Button <KBC>



Place on easy use location

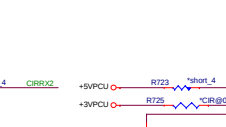


Power Button <KBC>



Power Button <KBC>

Power Button <KBC>



Place on easy use location



Power Button <KBC>



Power Button <KBC>

Power Button <KBC>



Place on easy use location



Power Button <KBC>



Power Button <KBC>

Power Button <KBC>



Place on easy use location



Power Button <KBC>

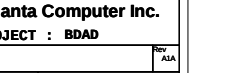


Power Button <KBC>

Power Button <KBC>



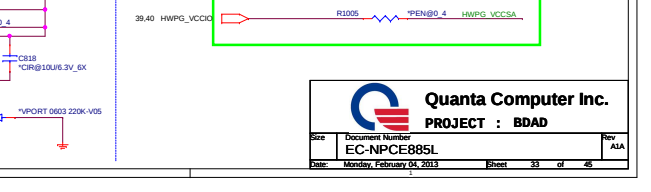
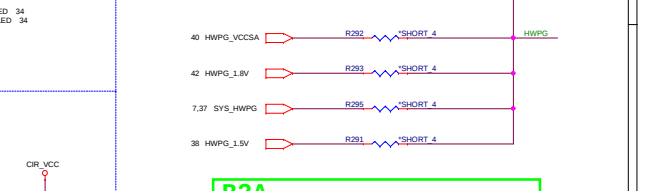
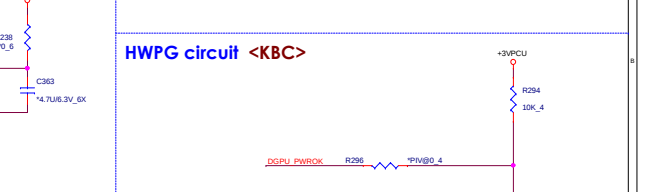
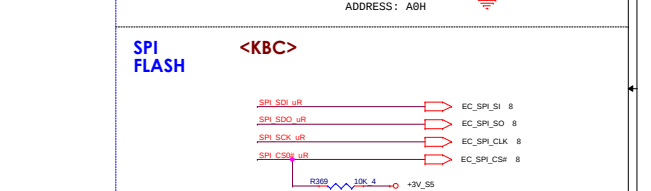
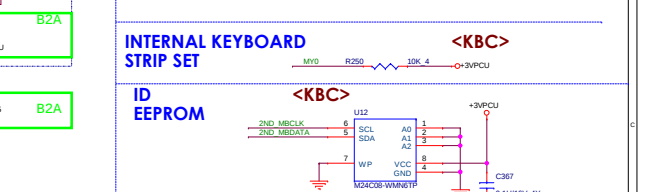
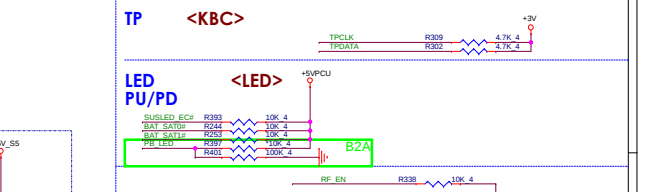
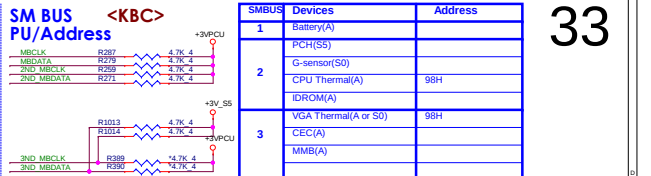
Place on easy use location



Power Button <KBC>



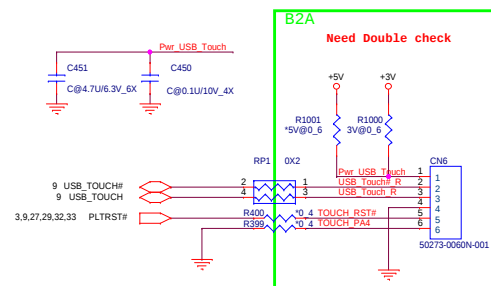
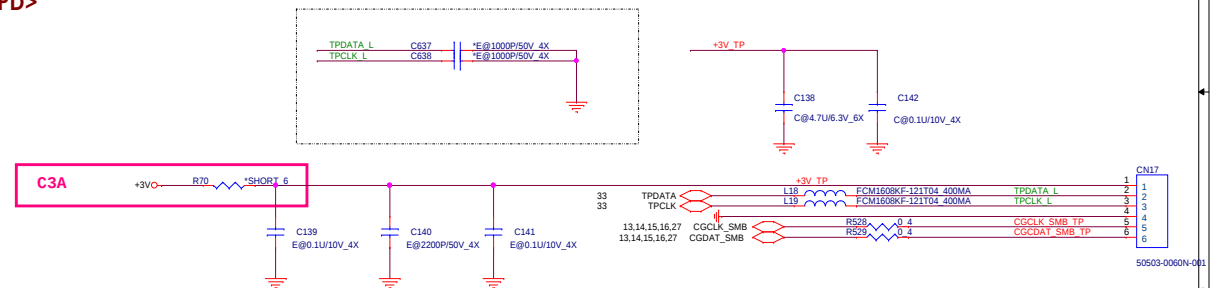
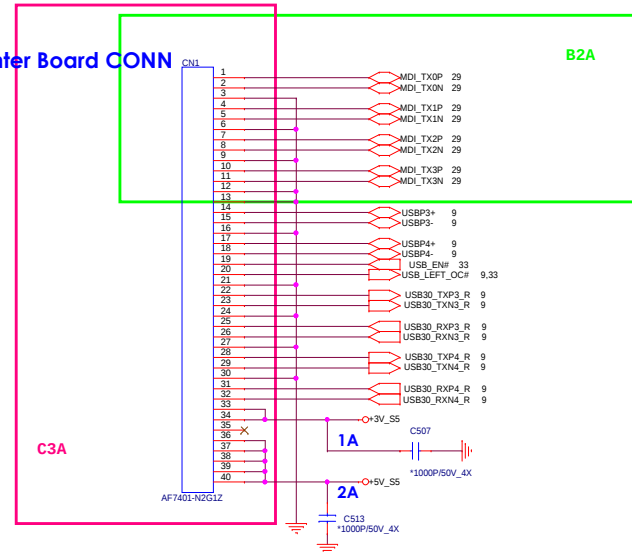
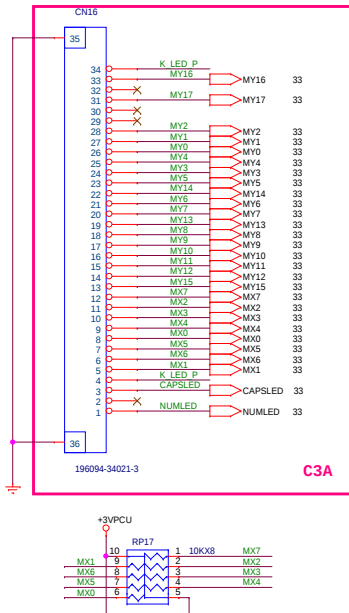
Power Button <KBC>



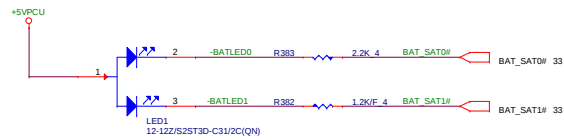
MS Strap	STRAP_1	STRAP_2	STRAP_3	STRAP_4
17" P	0			
17" G	1			
Chief River		0		
Shark Bay		1		
W/ 3D			0	
W/O 3D			1	
UMA				0
Discrete(Optimus)				1



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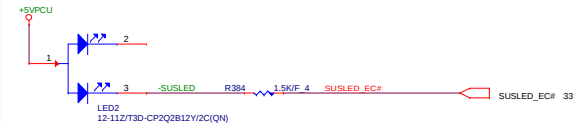
BEW00011ZA0



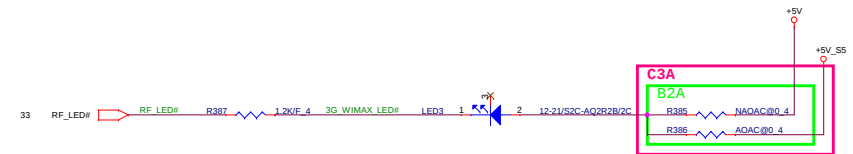
BEWH0139Z00

```
S0 Mode = White ON
S3 Mode = White BLINK
```

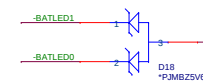
S3 Mode = White BLINK



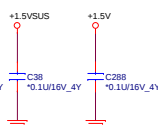
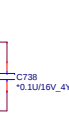
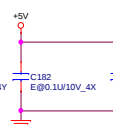
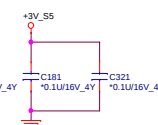
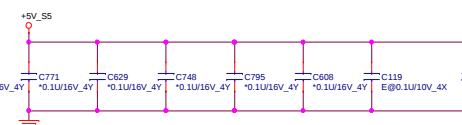
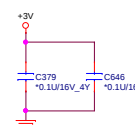
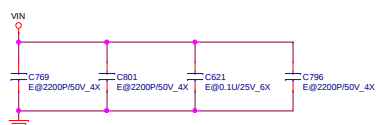
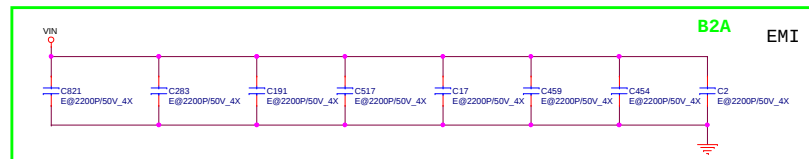
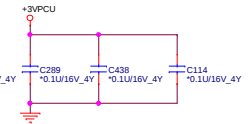
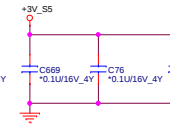
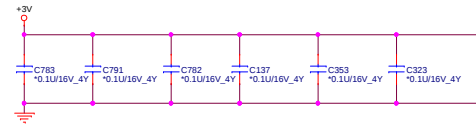
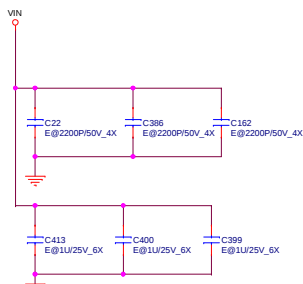
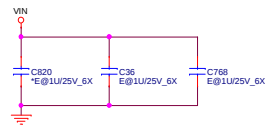
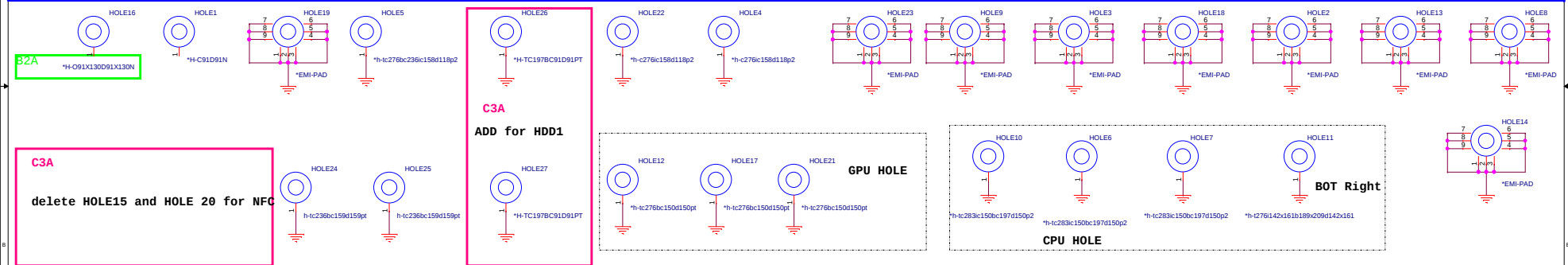
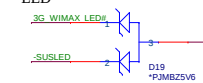
ESD Protect LED



FOR BATTERY LED



FOR W-LAN&POWER
LED



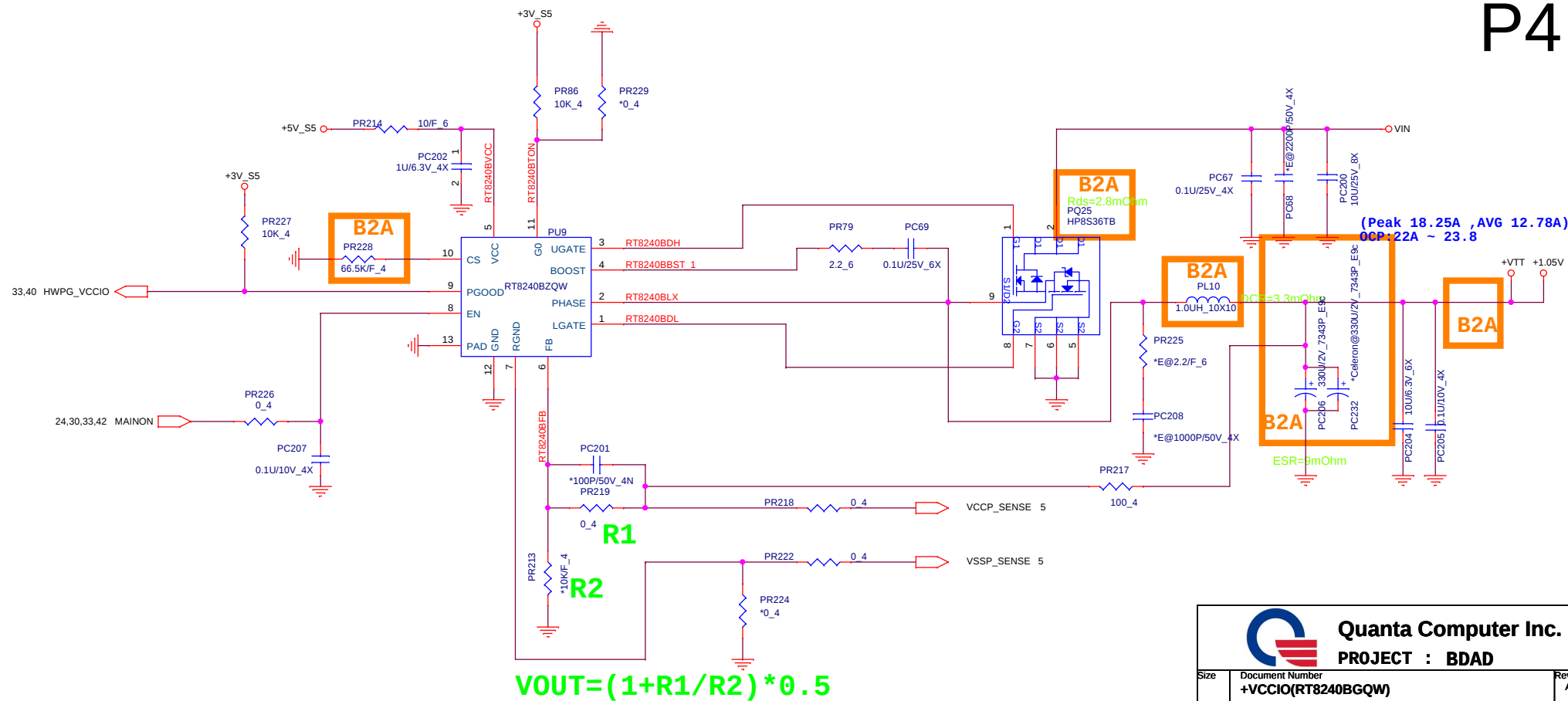
A vertical number line with four points labeled A, B, C, and D from bottom to top. An arrow points to point C.

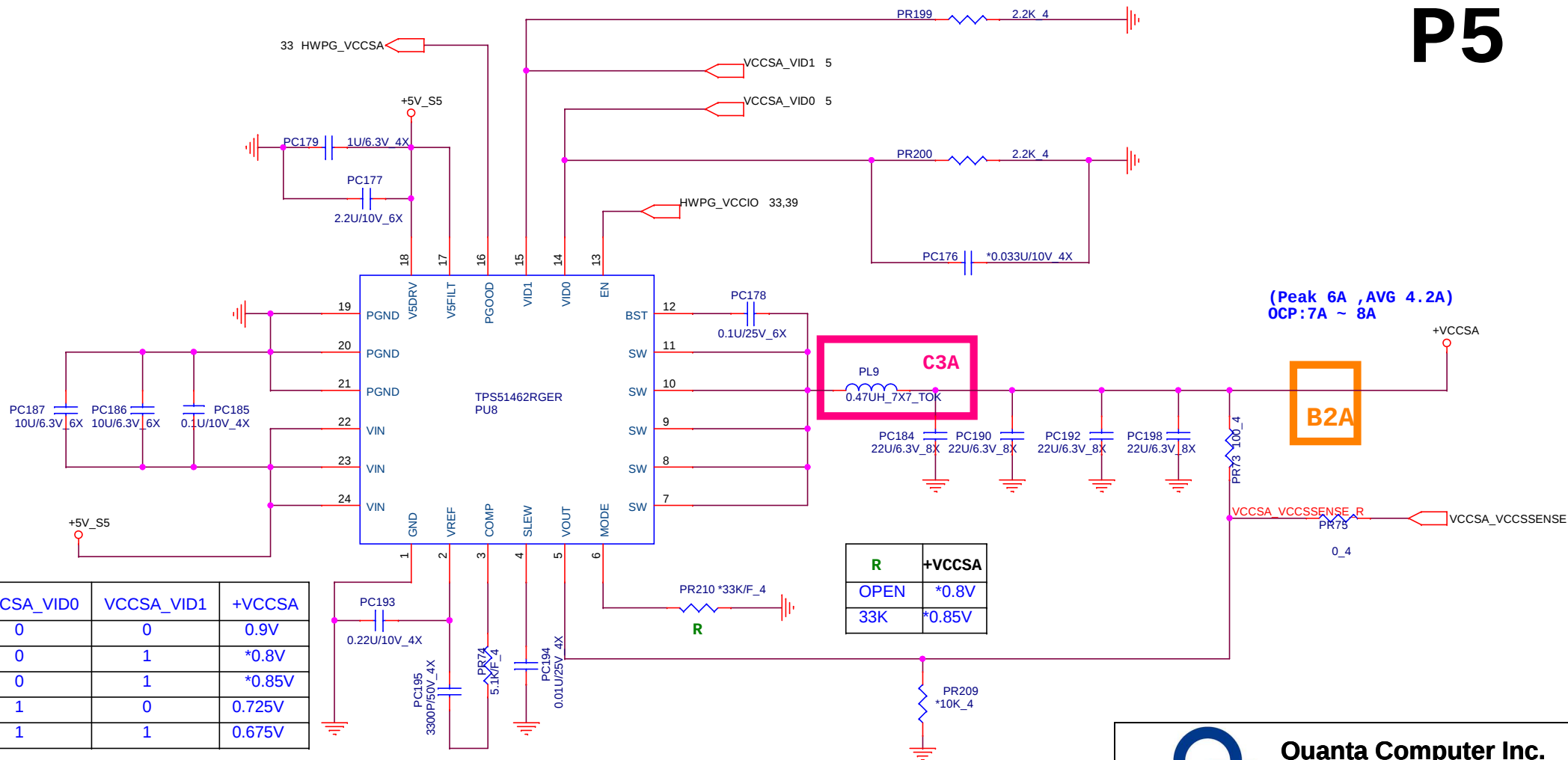




A







VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	*0.8V
0	1	*0.85V
1	0	0.725V
1	1	0.675V

*0.8V FOR SV TYPE
 *0.85V FOR LV/ULV TYPE

R	+VCCSA
OPEN	*0.8V
33K	*0.85V

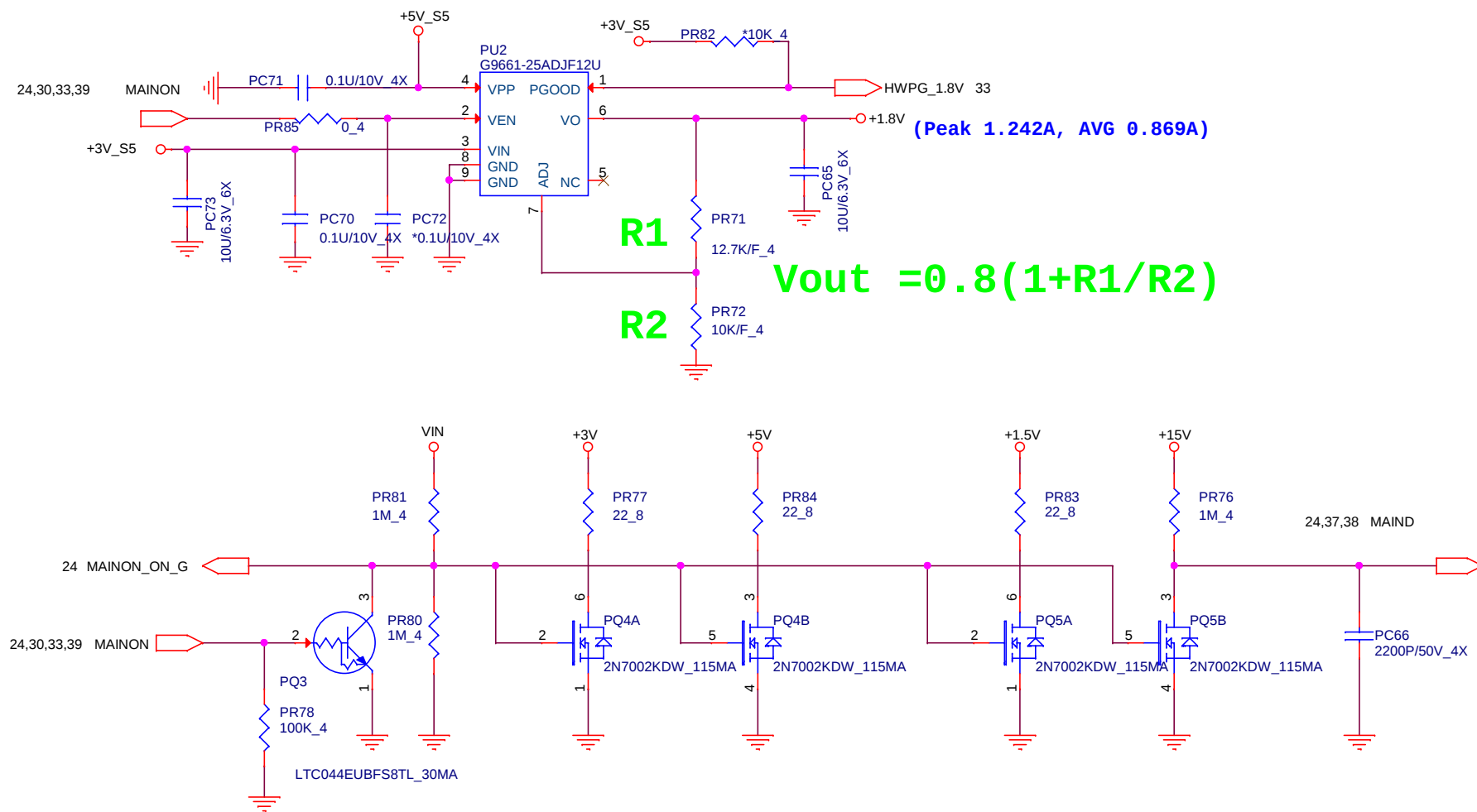


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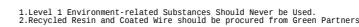
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	+VCCSA(TI51462)	A1A
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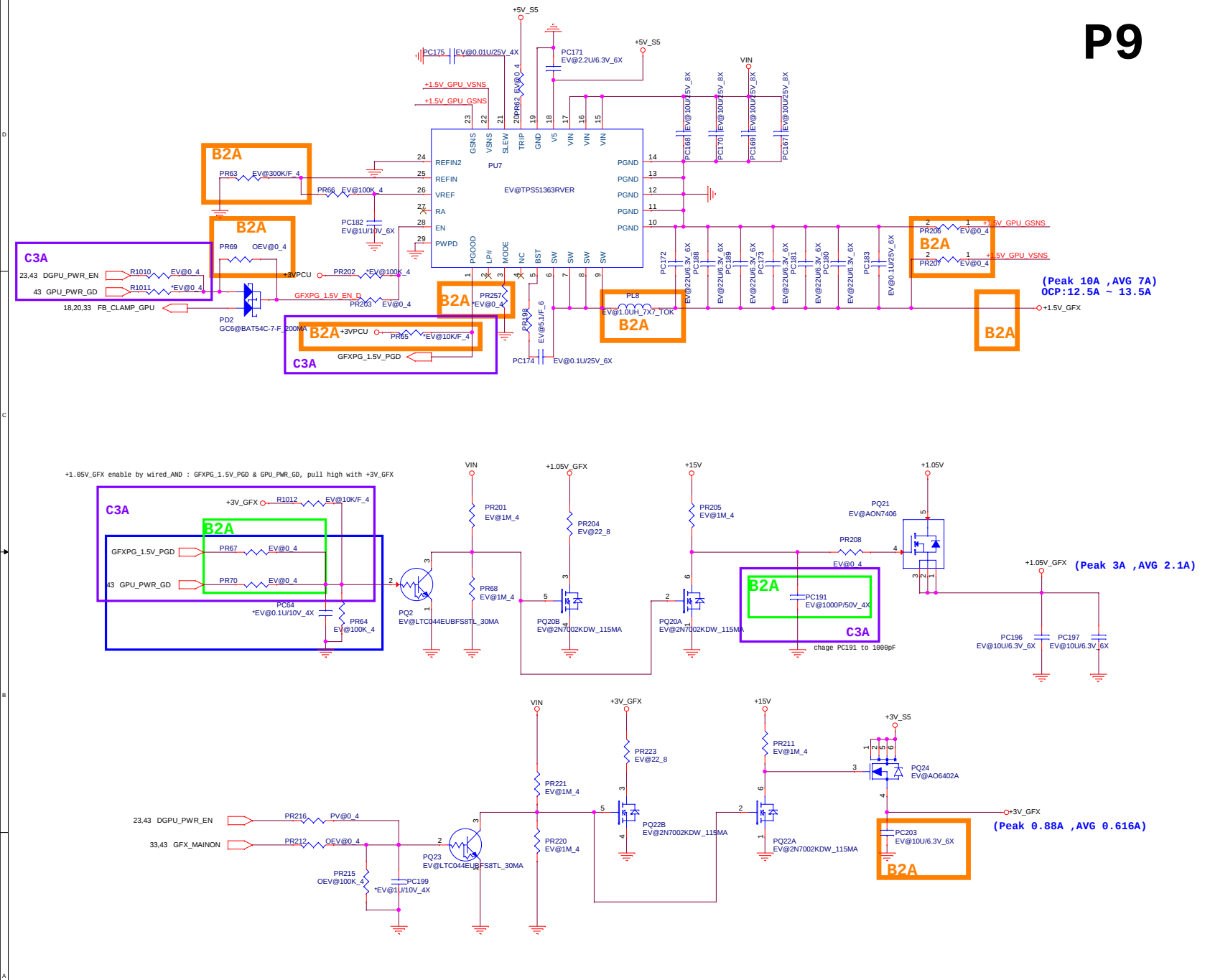




$$V_{out} = 0.8(1 + R1/R2)$$



P9



- GPU Power On Sequence**
1. DGPU_PWR_EN_R(delay) Enable +3V_GFX from +3V_S5
 2. DGPU_PWR_EN Enable +VGPU_CORE
 3. GPU_PWR_GD Enable +1.5V_GFX
 4. GPU_PWR_GD Enable(Delay) +1.05V_GFX

Model		REV		CHANGE LIST	

MODEL		BDAD	
PAGE	FROM	To	
1	1A		
2	1A		
3	1A		
4	1A		
5	1A		
6	1A		
7	1A		
8	1A		
9	1A		
10	1A		
11	1A		
12	1A		
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24	1A		
25	1A		
26	1A		
27	1A		
28	1A		
29	1A		
30	1A		

DOC NO. 204	PROJECT MODEL :	BY3E,BY4E	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISION:	



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Size

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Rev

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