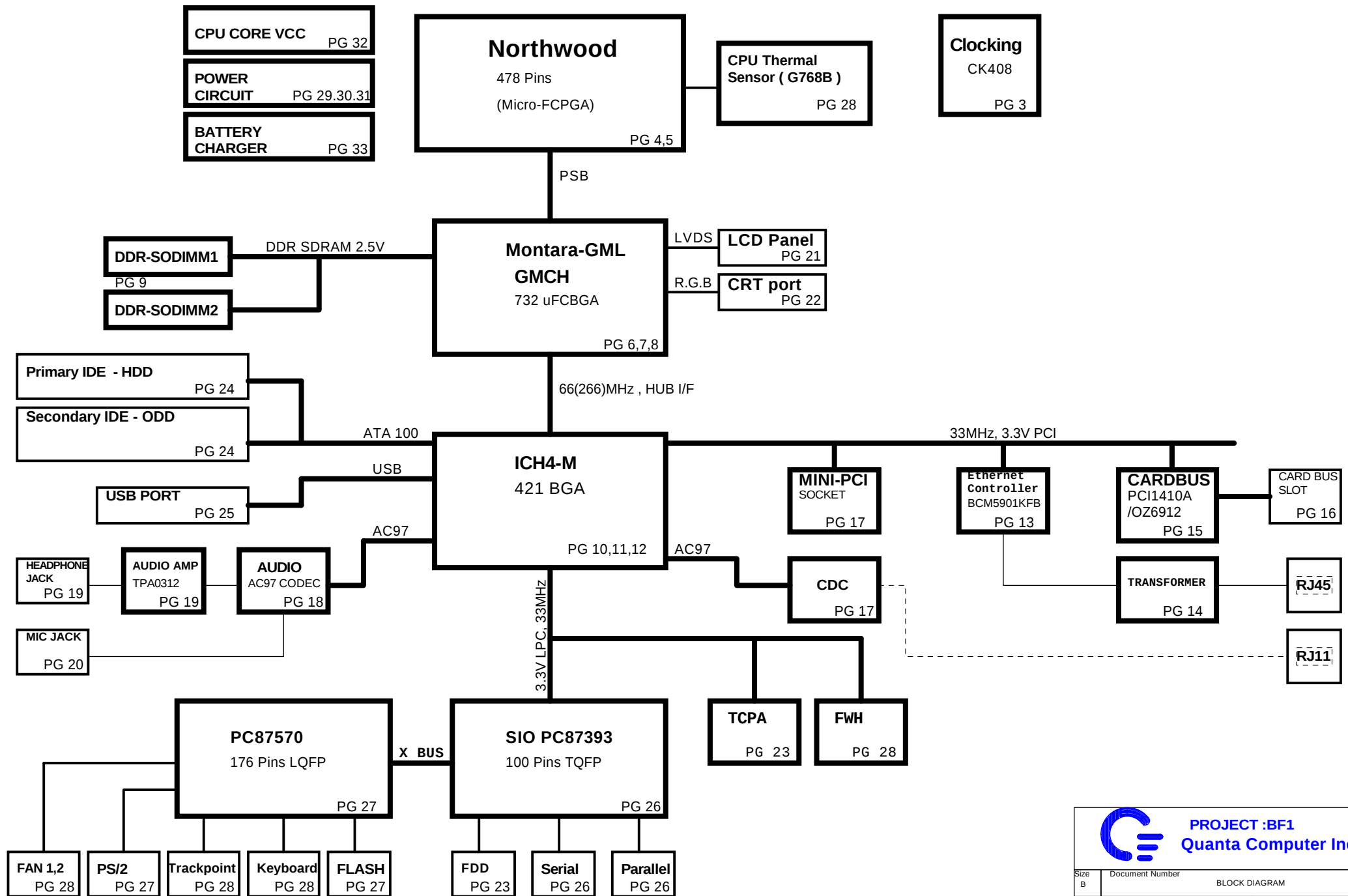


BF1 BLOCK DIAGRAM

NORTHWOOD / MONTARA-GML

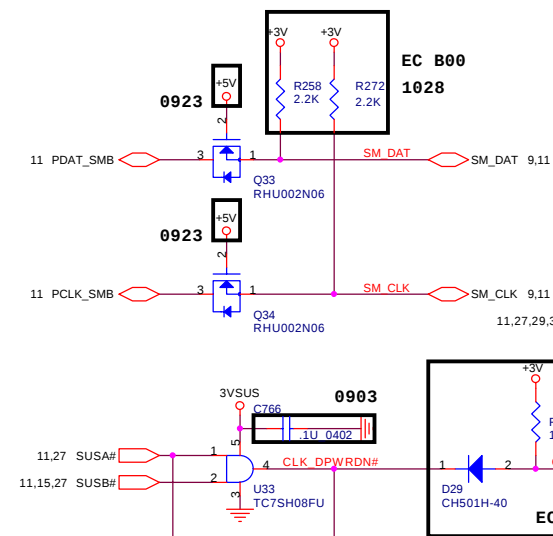
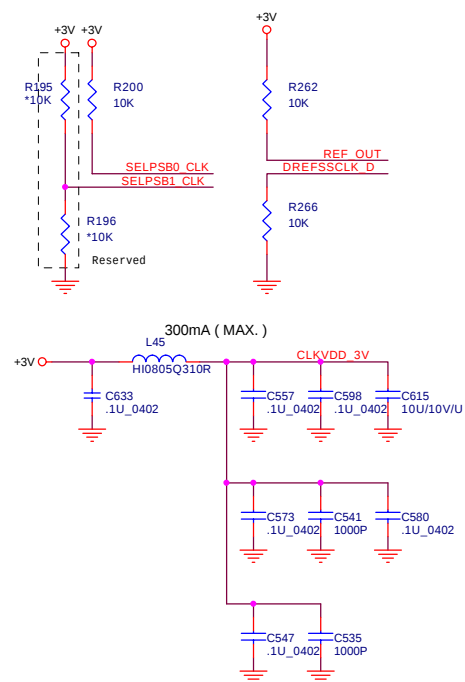


PROJECT :BF1
Quanta Computer Inc.

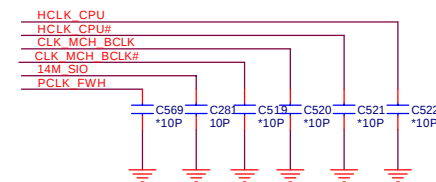
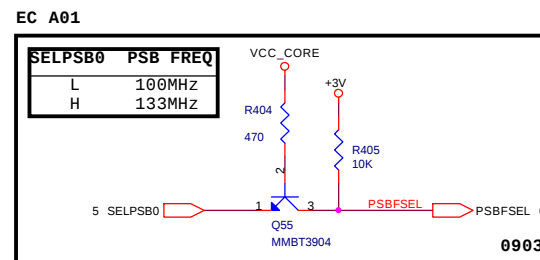
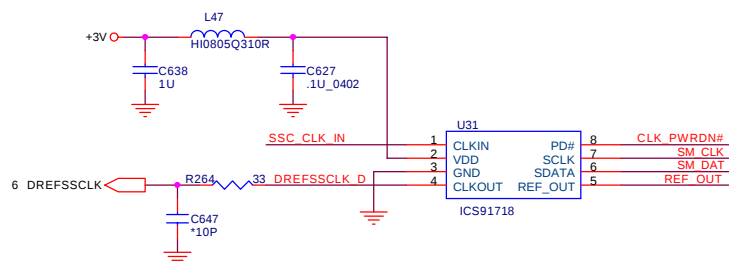
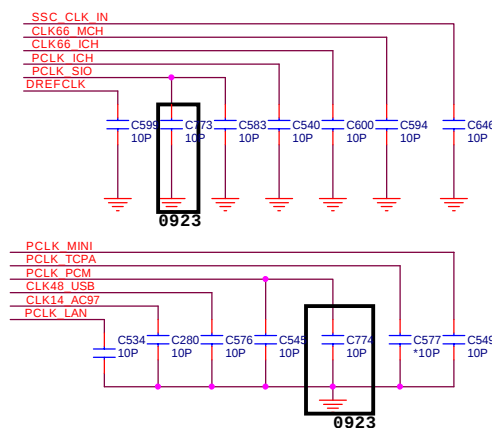
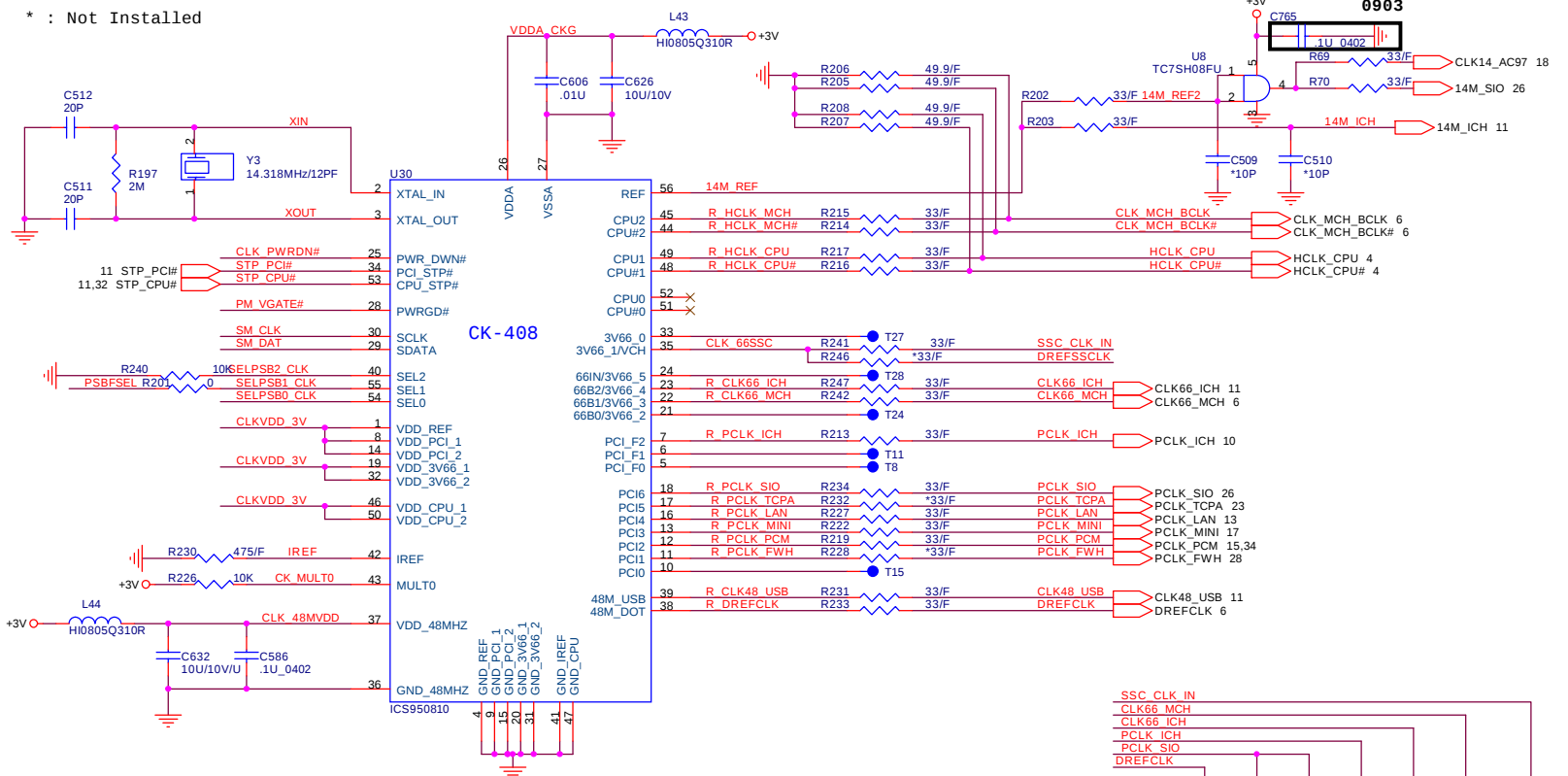
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P02: TABLE OF CONTENTS	P20: AUDIO JACKS & H/W THROTTLING
P03: CLOCK GENERATOR	P21: LCD CONNECTOR
P04: NORTHWOOD (HOST BUS)	P22: CRT CONNECTOR
P05: NORTHWOOD (POWER/GND)	P23: FDD , PC BEEP & TCPA
P06: GMCH-GML (HOST, HUB, LVDS)	P24: HDD & ODD
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P13: BCM5901KFB LAN CONTROLLER	P31: 1.2V & 1.5V
P14: LAN TRANSFORMER & CONN.	P32: CPU VCC CORE POWER
P15: PCI1410A/OZ6912 CARDBUS CONTROLLER	P33: BATTERY CHARGER
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P17: MINI PCI & CDC I/F	P35: REMARK
P18: AC97 AUDIO CODEC	P36~: REVISION HISTORY

S2	S1	S0	CPU	AGP	PCI
0	0	0	166	66	33
0	0	1	100	66	33
0	1	0	200	66	33
0	1	1	133	66	33



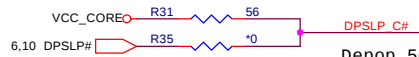
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Size	Document Number	Rev
Custom	Clock Generator	3F
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EC C05 1228

Depop 56ohm for Mobile
Depop 0ohm for DesktopNorthWood
1 OF 3REQUEST
PHASE
SIGNALSDATA
PHASE
SIGNALSERROR
SIGNALSARBITRATION
PHASE
SIGNALSSNOOP PHASE
SIGNALSRESPONSE
PHASE
SIGNALS

ITP

PC COMPATIBILITY
SIGNALSEXECUTION
CONTROL
SIGNALS

THERMAL DIODE

UPGA478P

DBI0# HDBI0# 6
DBI1# HDBI1# 6
DBI2# HDBI2# 6
DBI3# HDBI3# 6DSTBN0# HDSTBN0# HDSTBN0# 6
DSTBP0# HDSTBP0# HDSTBP0# 6
DSTBN1# HDSTBN1# HDSTBN1# 6
DSTBP1# HDSTBP1# HDSTBP1# 6
DSTBN2# HDSTBN2# HDSTBN2# 6
DSTBP2# HDSTBP2# HDSTBP2# 6
DSTBN3# HDSTBN3# HDSTBN3# 6
DSTBP3# HDSTBP3# HDSTBP3# 6DBSY# DBSY# 6
DRDY# DRDY# 6DP0# K26#
DP1# K26#
DP2# L25#
DP3#

MCERR# V6#

RESET# AB25# CPURST# 6

BCLK1# AF23# HCLK_CPU# 3

BCLK0# AF22# HCLK_CPU# 3

E21 HDBI0#
G25 HDBI1#
P26 HDBI2#
V21 HDBI3#E22 HDSTBN0#
E21 HDSTBP0#
K22 HDSTBN1#
J23 HDSTBP1#
R22 HDSTBN2#
P23 HDSTBP2#
W22 HDSTBN3#
W23 HDSTBP3#H5 DBSY#
H2 DRDY#J26 K26#
K25#
L25#

V6#

AB25# CPURST# 6

AF23# HCLK_CPU# 3

AF22# HCLK_CPU# 3

E21 HDBI0#
G25 HDBI1#
P26 HDBI2#
V21 HDBI3#E22 HDSTBN0#
E21 HDSTBP0#
K22 HDSTBN1#
J23 HDSTBP1#
R22 HDSTBN2#
P23 HDSTBP2#
W22 HDSTBN3#
W23 HDSTBP3#H5 DBSY#
H2 DRDY#J26 K26#
K25#
L25#

V6#

AB25# CPURST# 6

AF23# HCLK_CPU# 3

AF22# HCLK_CPU# 3

E21 HDBI0#
G25 HDBI1#
P26 HDBI2#
V21 HDBI3#E22 HDSTBN0#
E21 HDSTBP0#
K22 HDSTBN1#
J23 HDSTBP1#
R22 HDSTBN2#
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H2 DRDY#J26 K26#
K25#
L25#

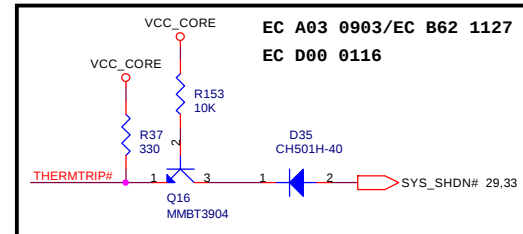
V6#

AB25# CPURST# 6

AF23# HCLK_CPU# 3

AF22# HCLK_CPU# 3

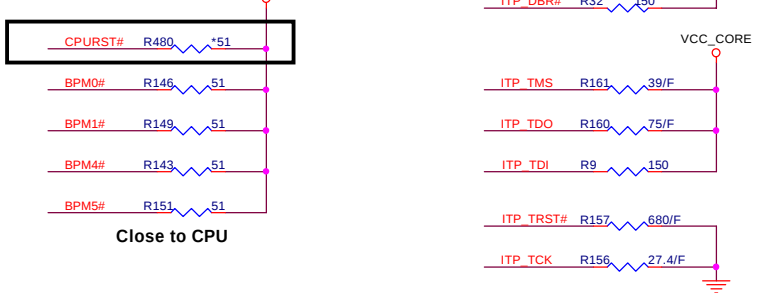
EC B59 1127

Del U21, R139, R136, R134, R137,
R145, C366, C370

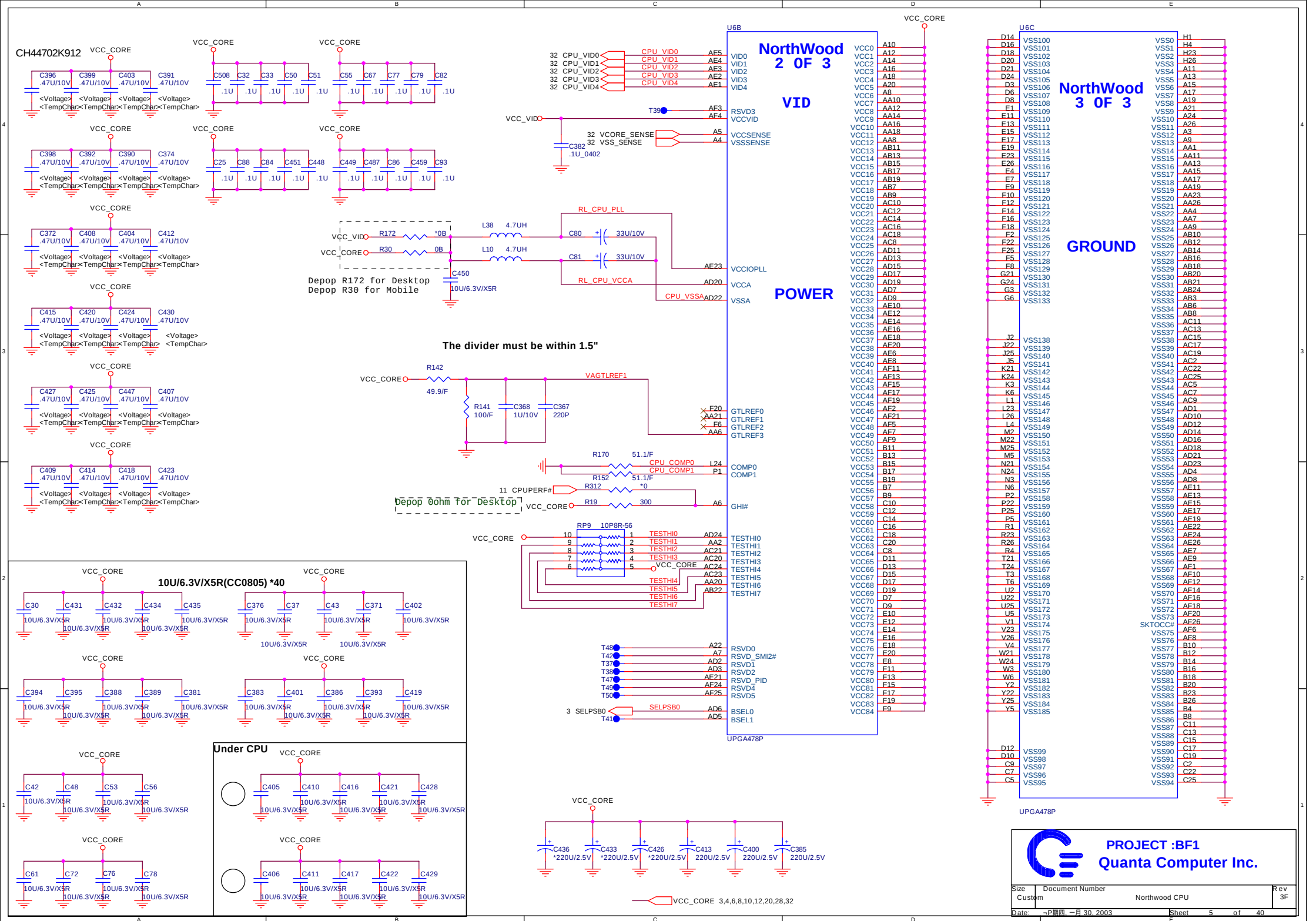
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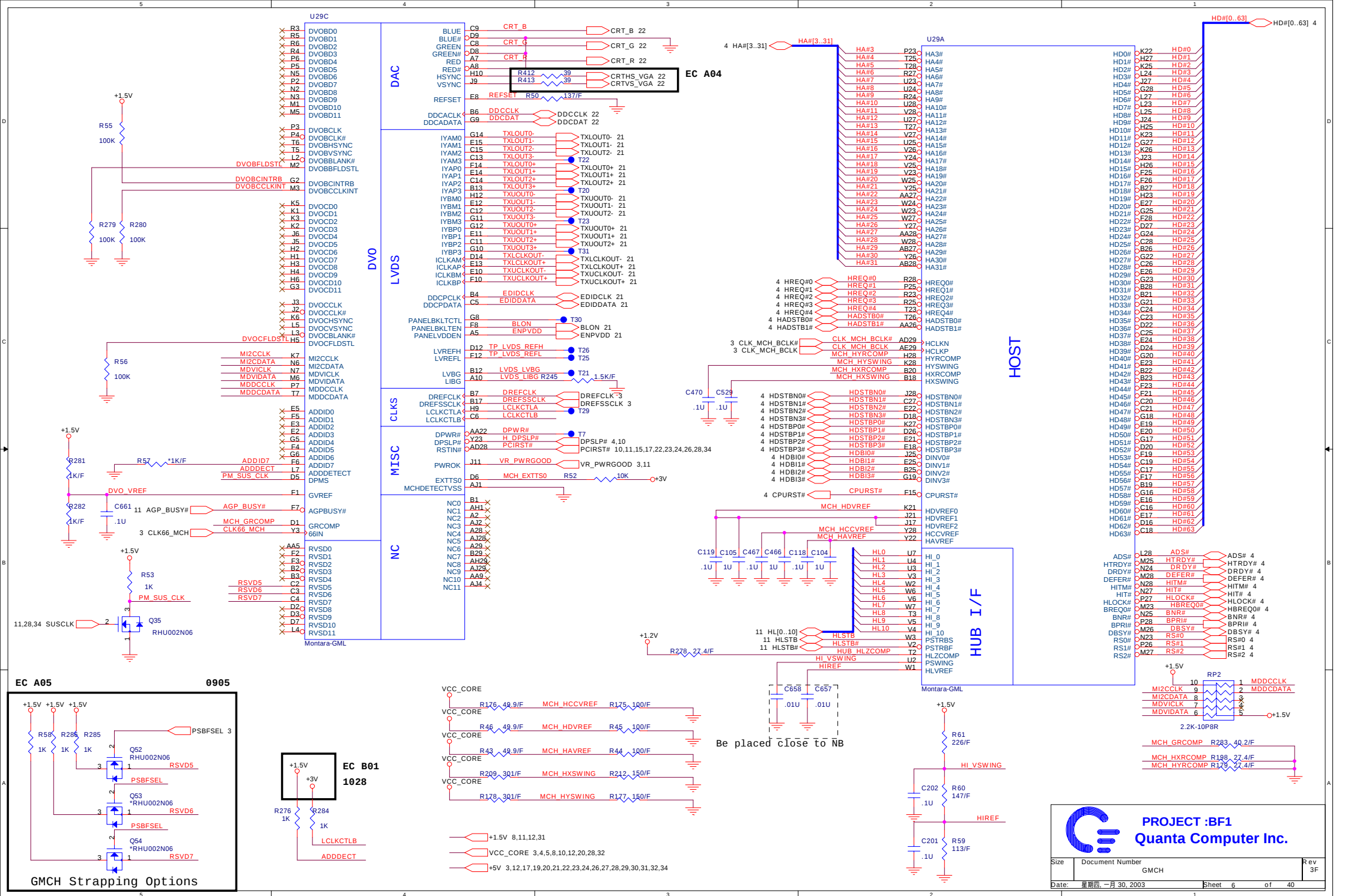
Del R36, Q2; move R38 to page29.

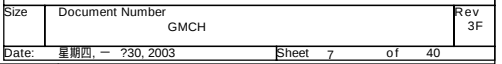
EC D00 0116

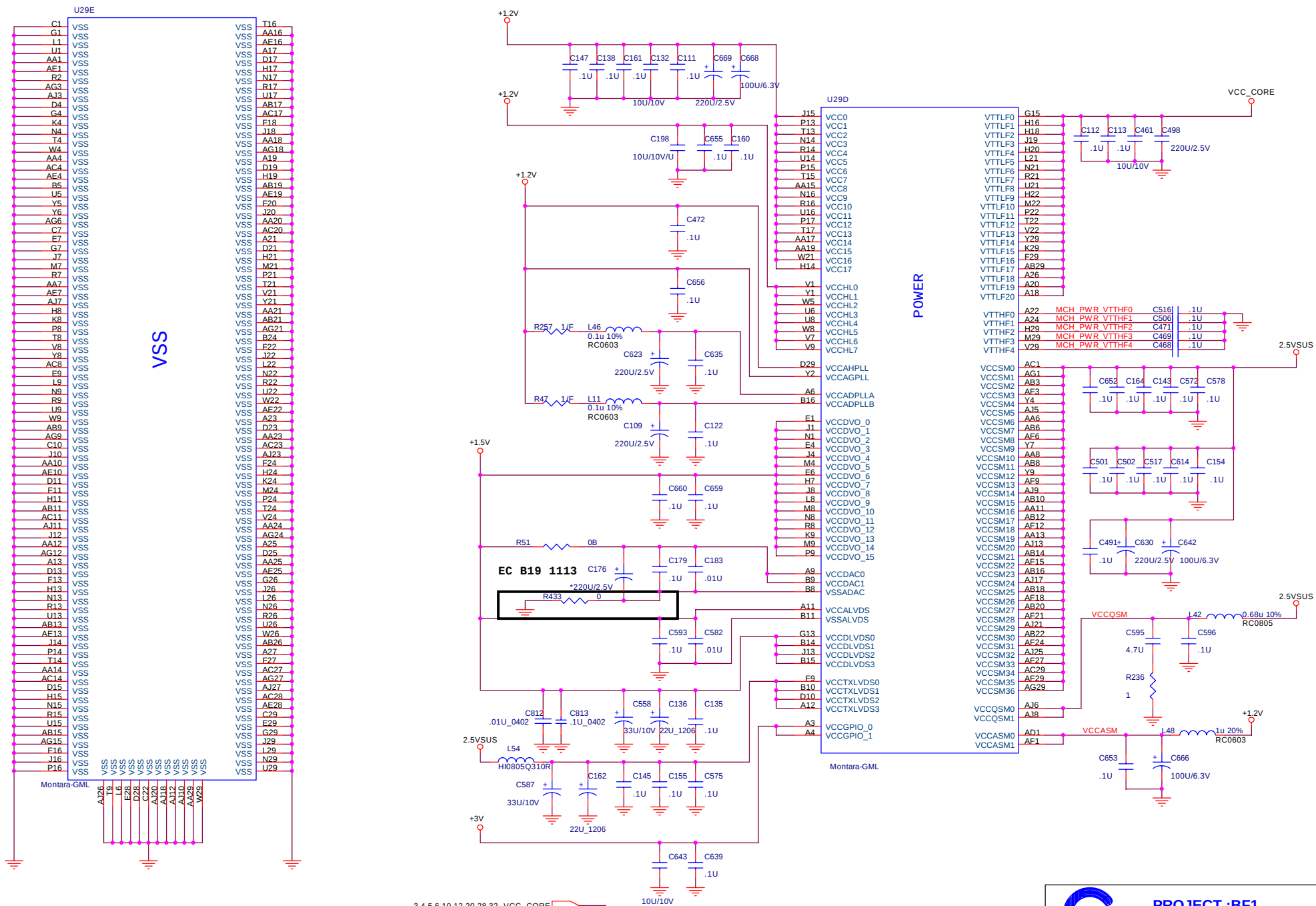
PROJECT :BF1
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Size B	Document Number	Northwood CPU	Rev 3F
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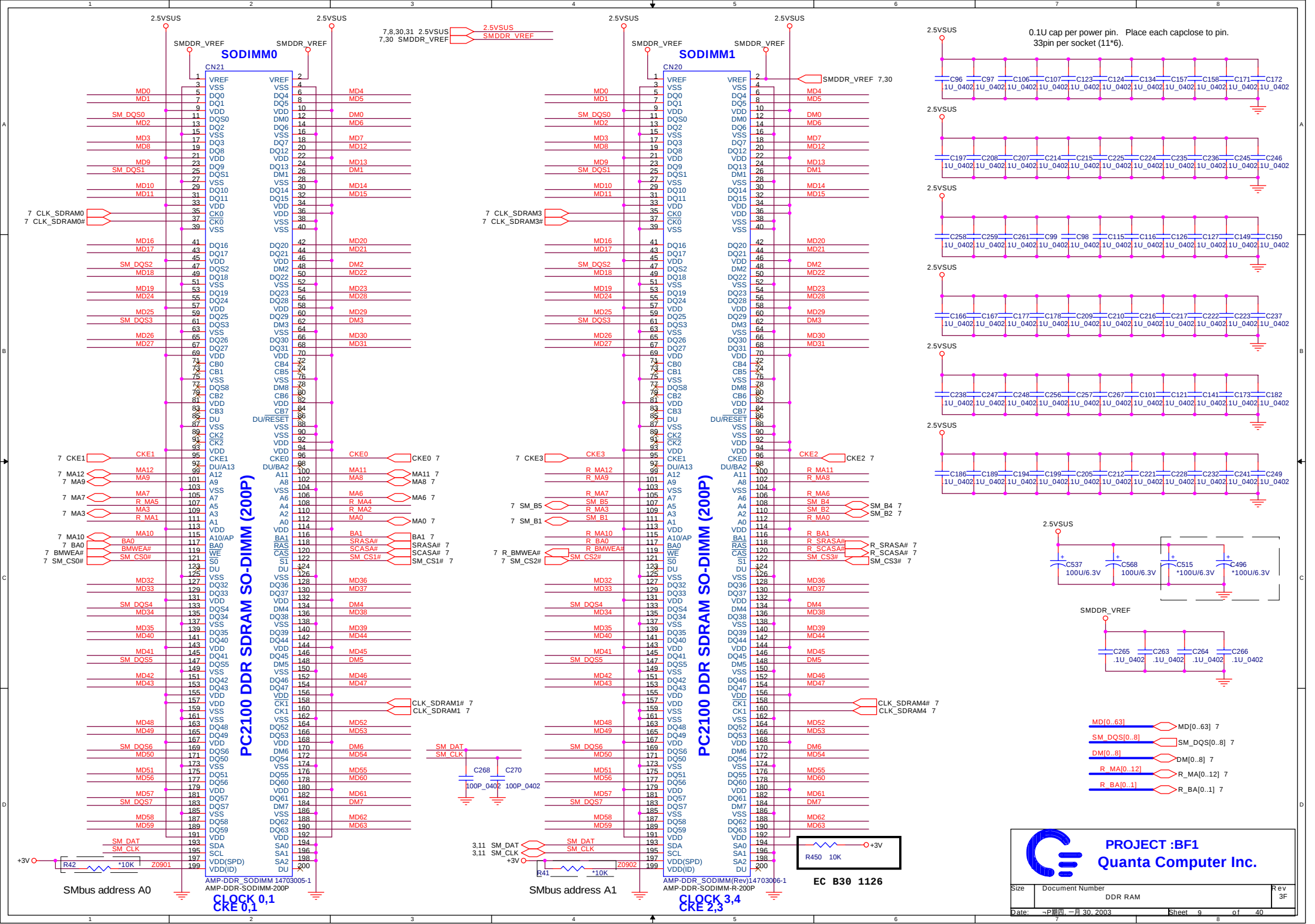


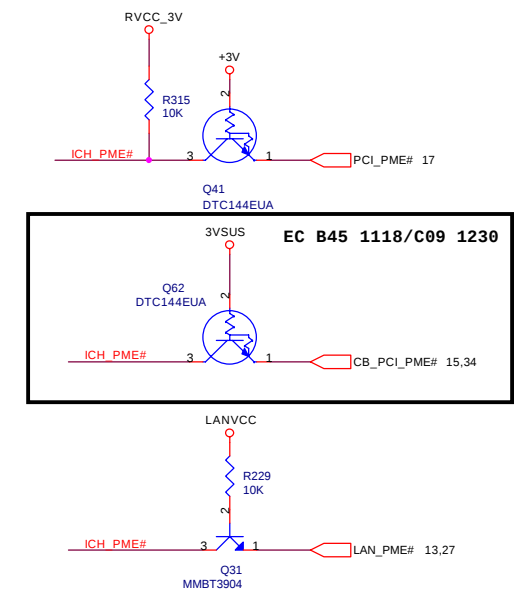
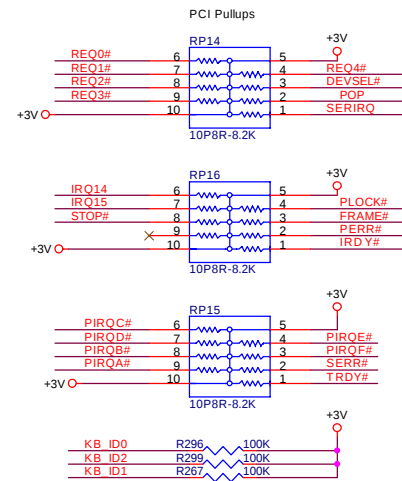
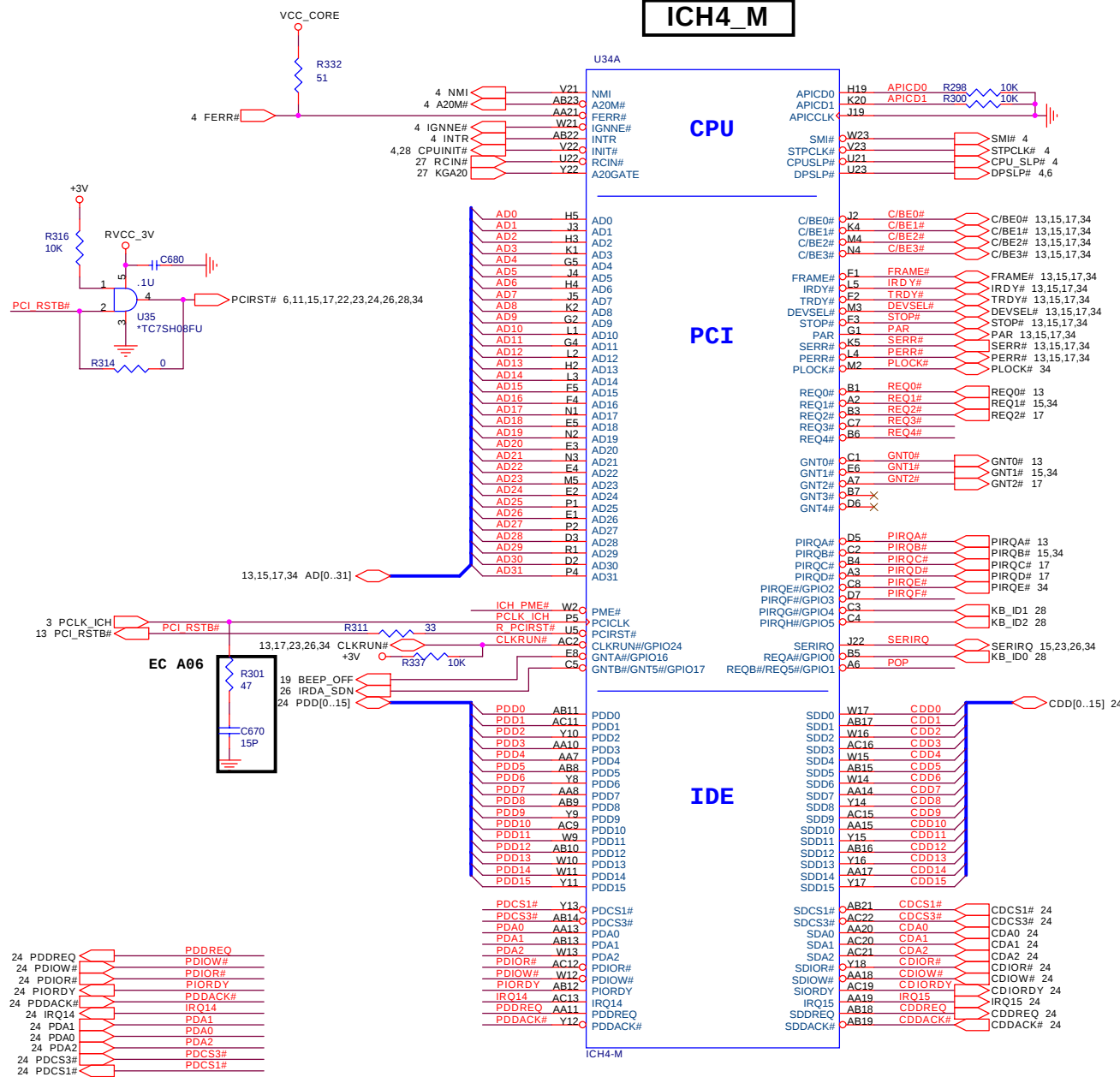


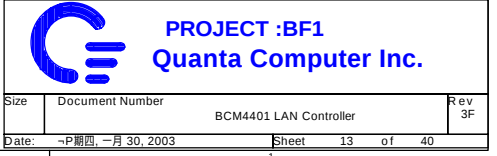


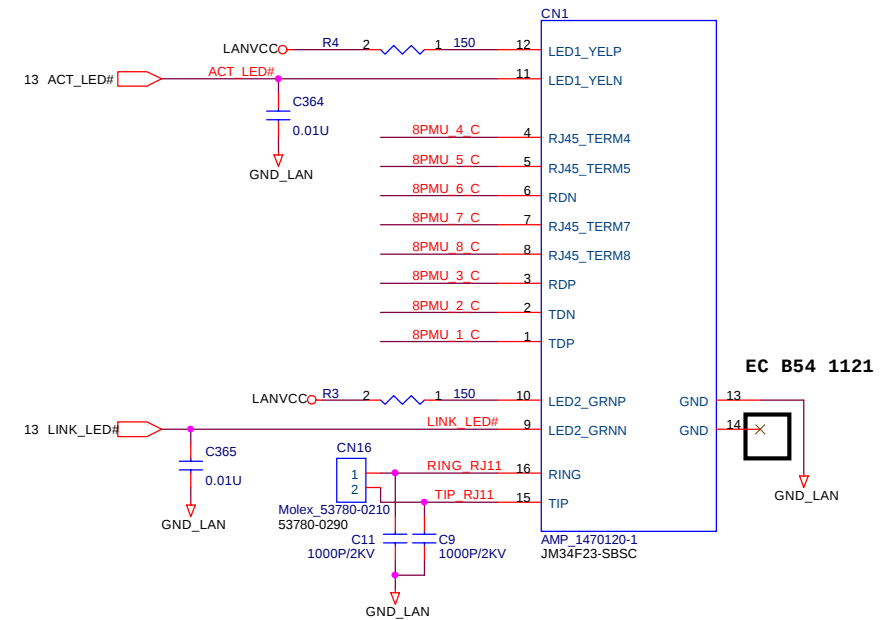
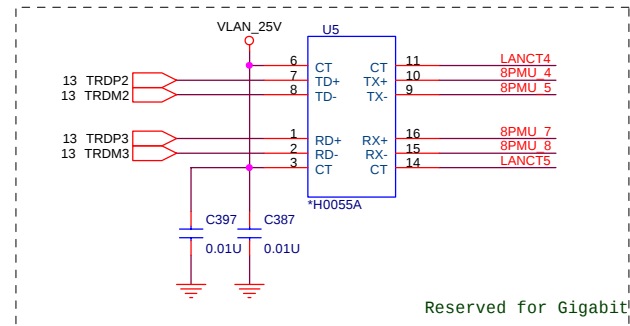
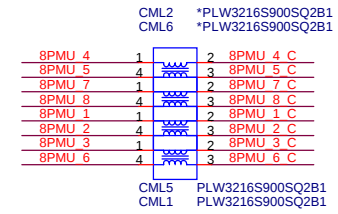
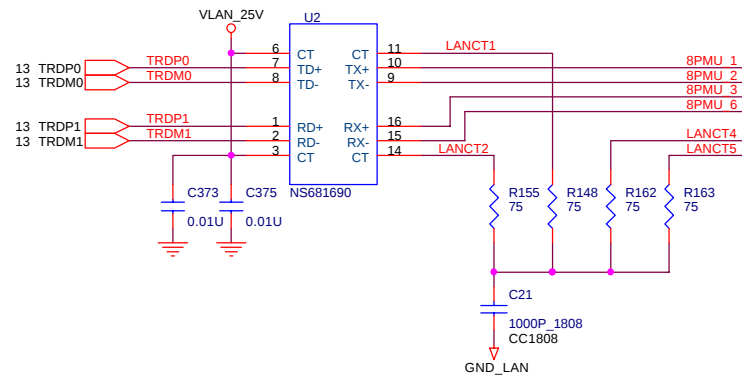


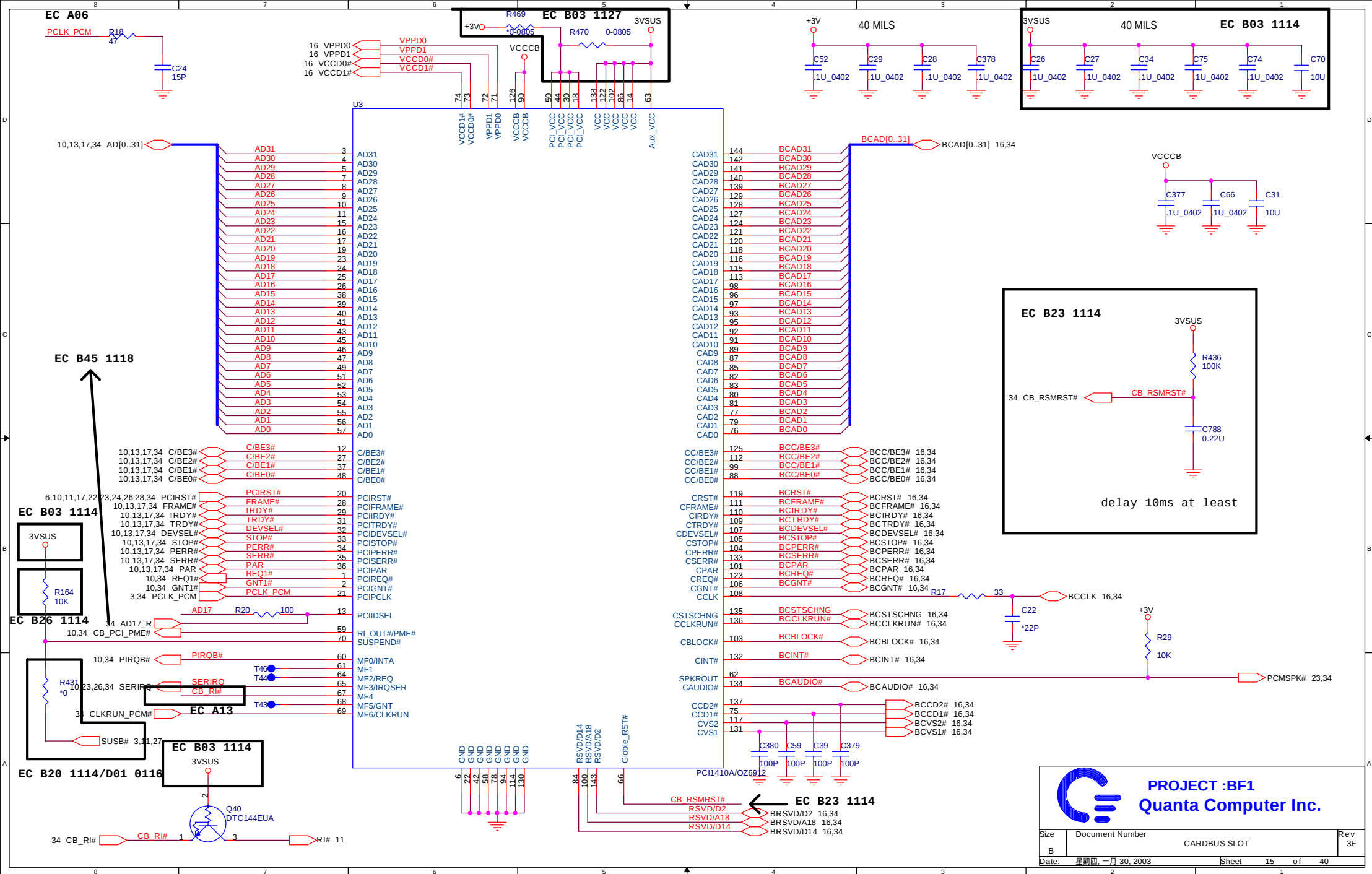
PROJECT :BF1
Quanta Computer Inc.

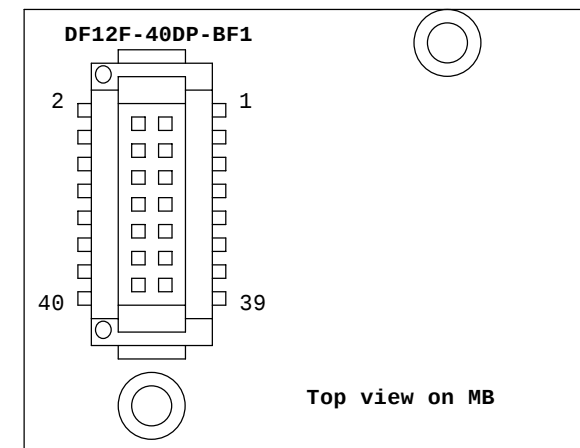
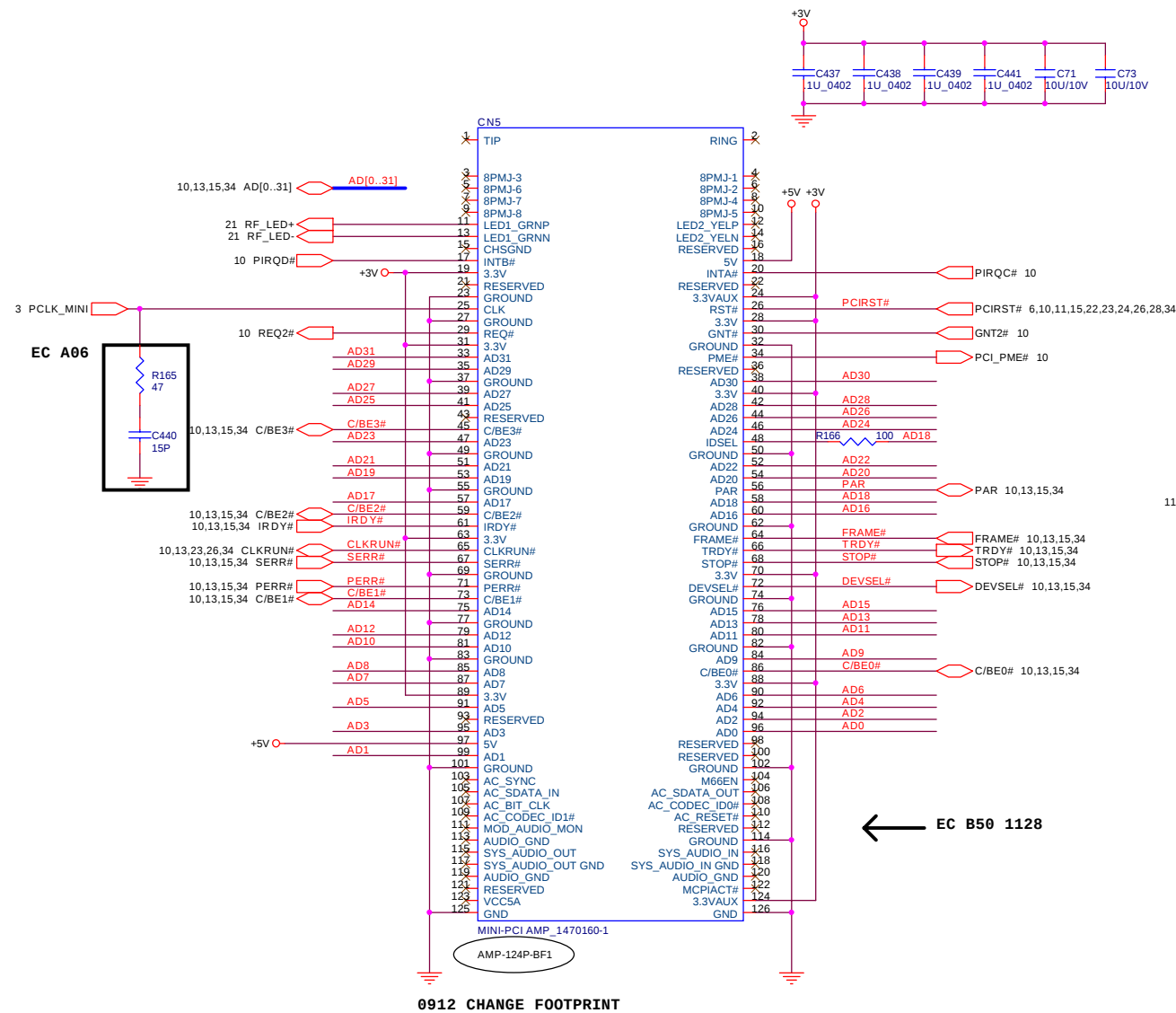




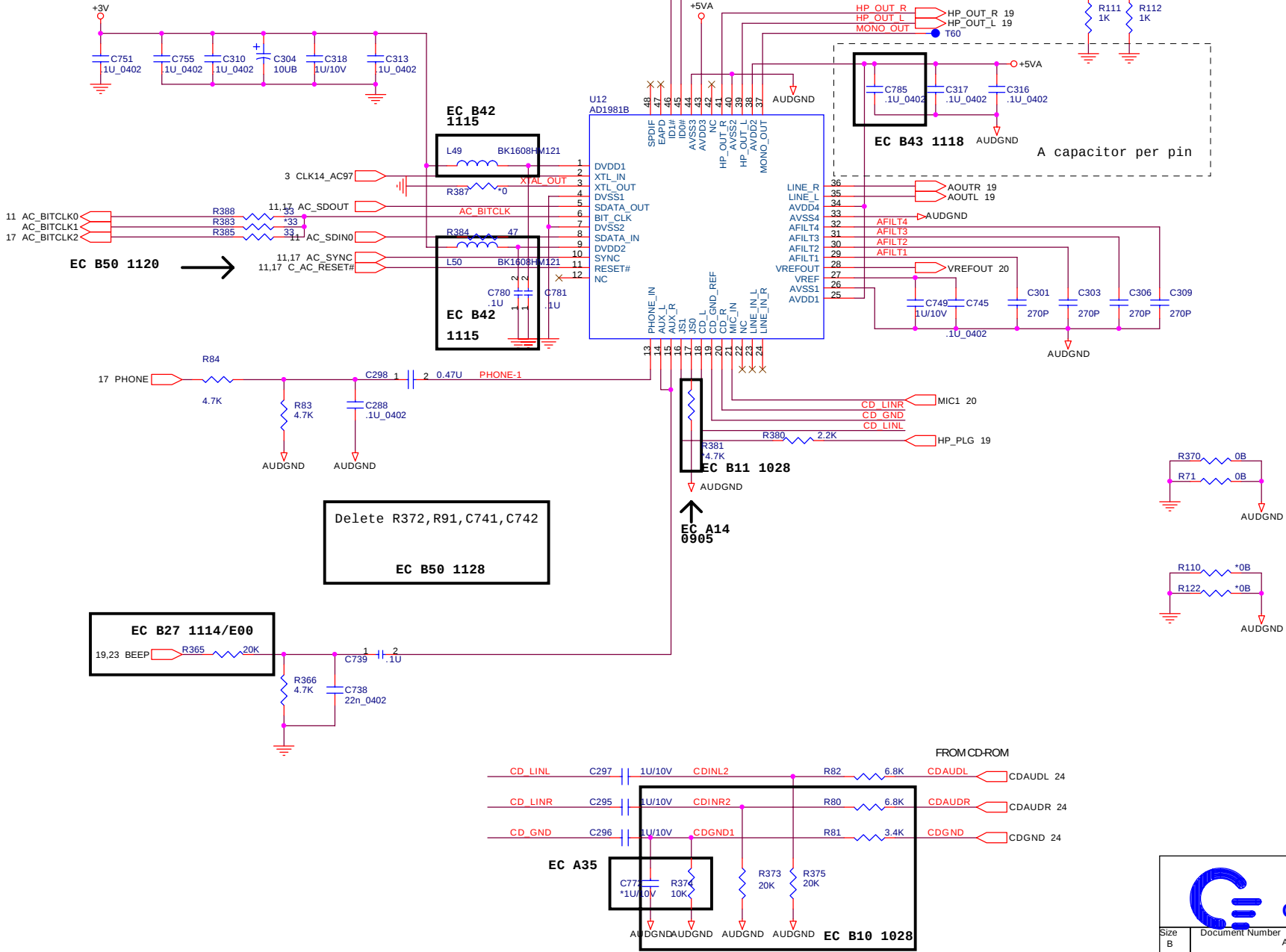
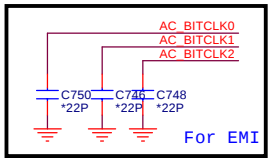




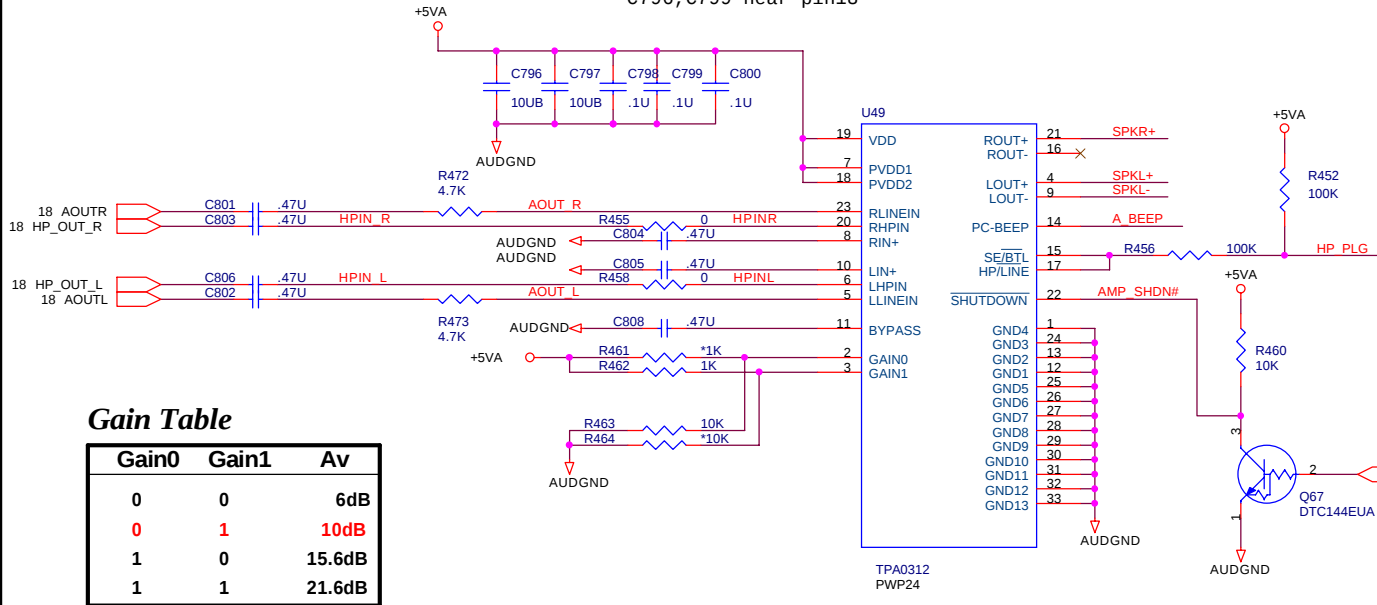




External Clock	ID1#	ID0#	XTAL_OUT
14.318MHz	1K	1K	X
48MHz	1K	Open	X



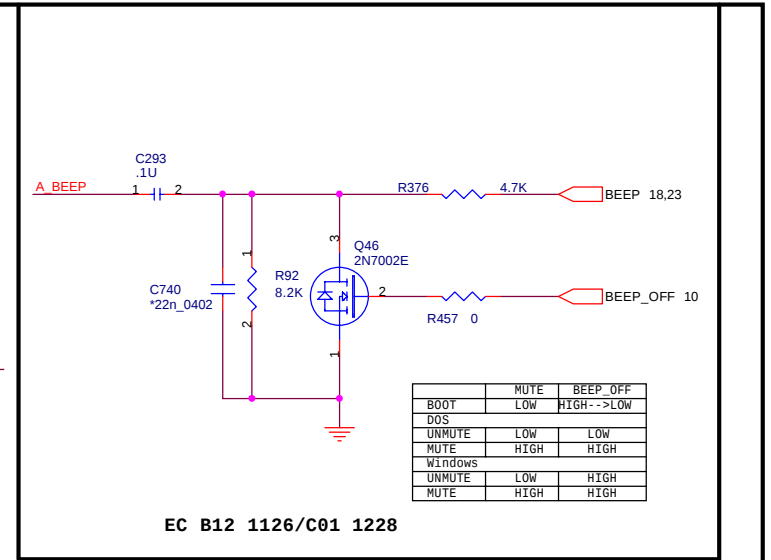
Need place C800 near pin19
C797,C798 near pin 7
C796,C799 near pin18



Gain Table

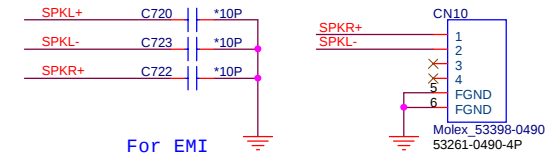
Gain0	Gain1	Av
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

EC B13 1126/C08 0113

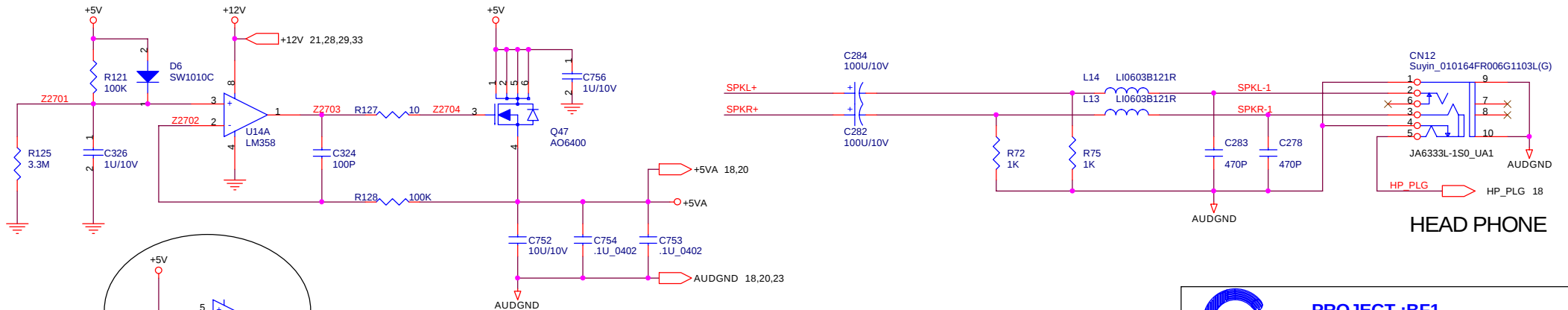


	MUTE	BEEP OFF
BOOT	LOW	HIGH->LOW
DOS		
UNMUTE	LOW	LOW
MUTE	HIGH	HIGH
Windows		
UNMUTE	LOW	HIGH
MUTE	HIGH	HIGH

EC B12 1126/C01 1228



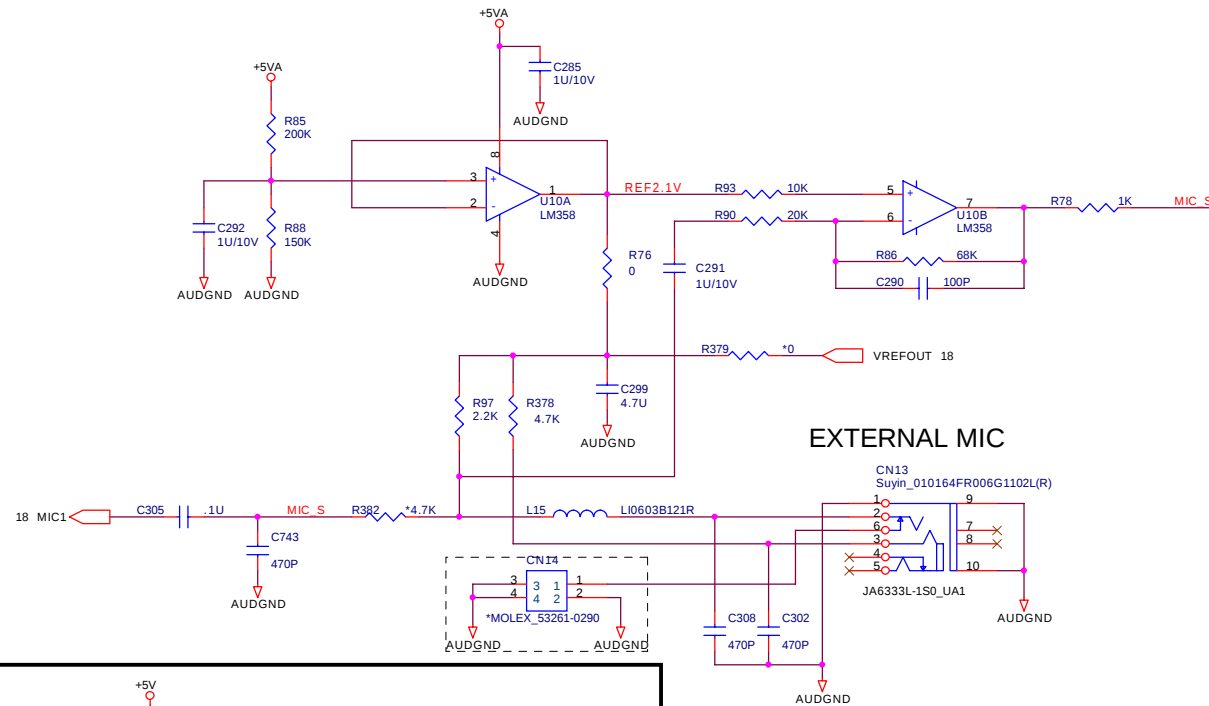
For EMI



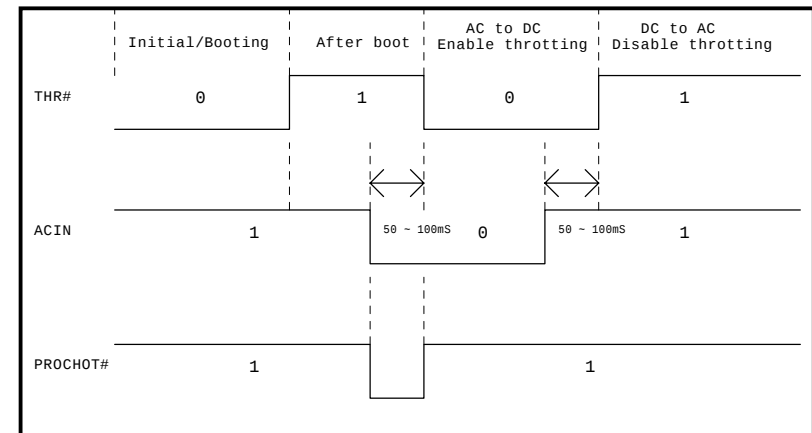
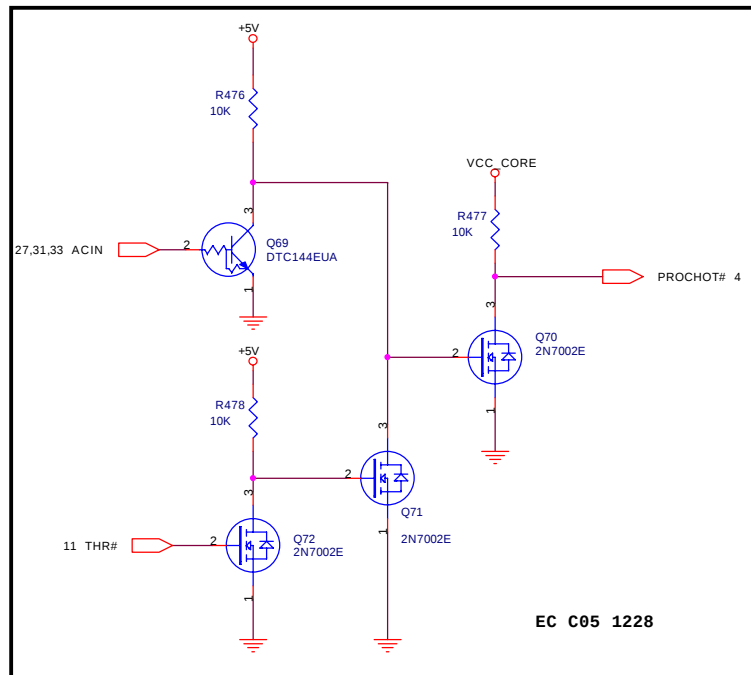
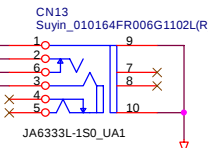
HEAD PHONE

PROJECT :BF1
Quanta Computer Inc.

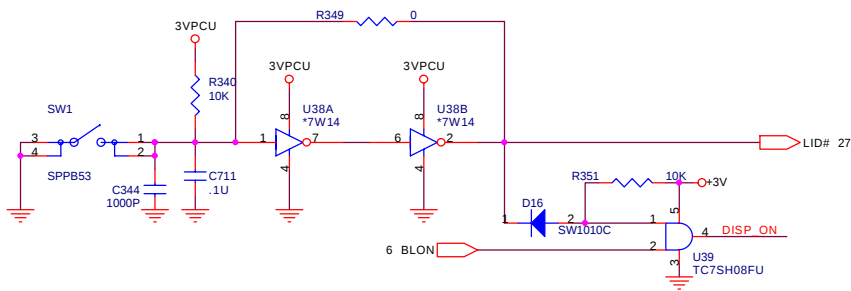
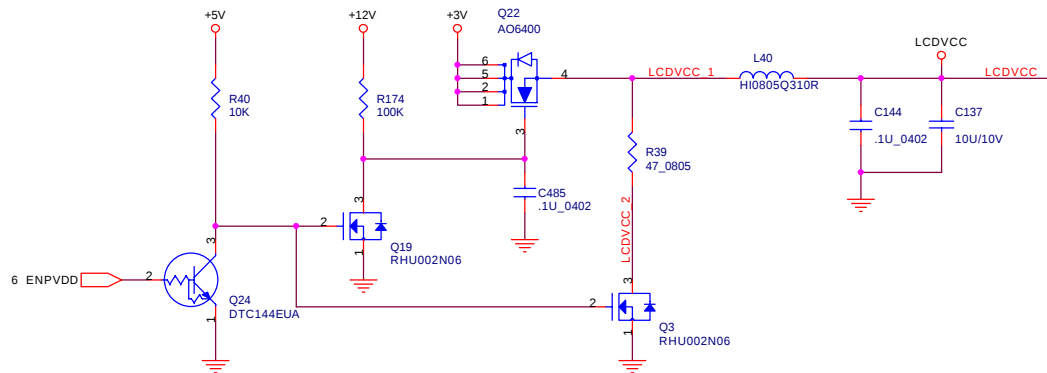
Size B	Document Number	AUDIO AMP. & Speaker	Rev 3F
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EXTERNAL MIC

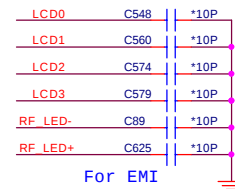
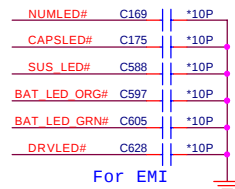
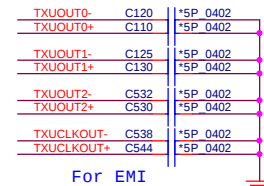
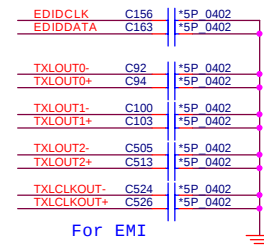
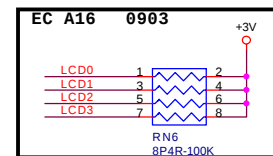
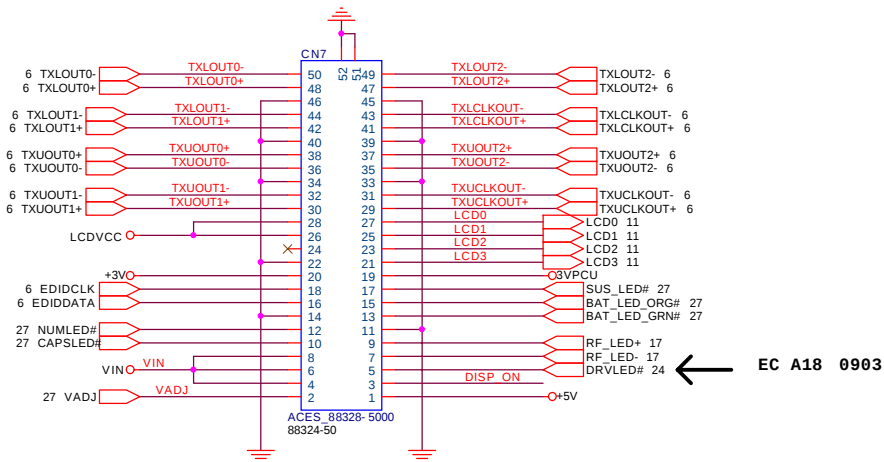
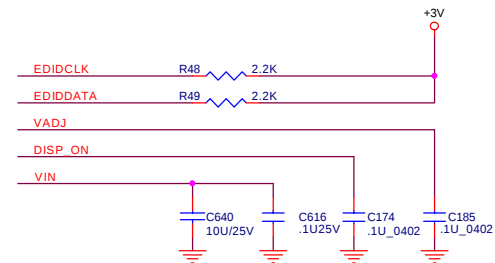


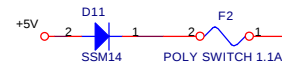
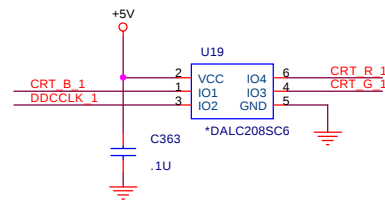
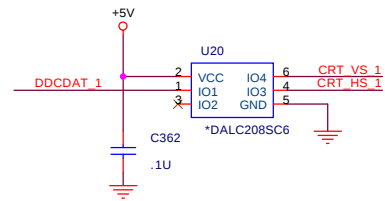
PROJECT :BF1
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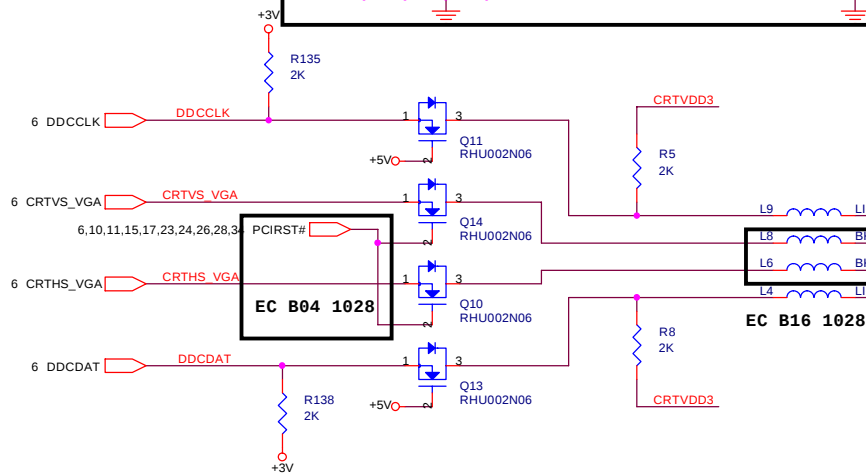
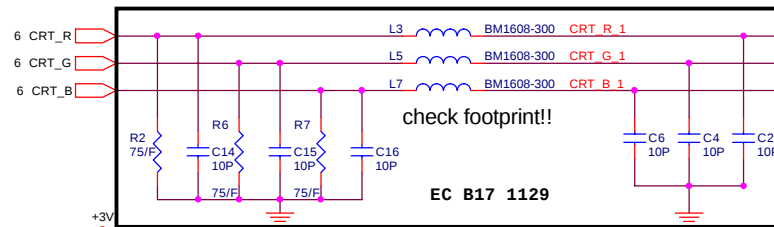
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+5V 3,12,17,19,20,22,23,24,26,27,28,29,30,31,32,34
+3V 3,4,6,8,9,10,11,12,13,15,17,18,22,23,24,26,27,28,29,31,32,34
+12V 19,28,29,33

			LCD3	LCD2	LCD1	LCD0
Hydis	14.1" XGA	HT14X19-100	1	1	1	0
IDT	14.1" XGA	IAVG15S/F8915S	1	1	1	1
LG	15" XGA	LP150X2-B2	1	1	0	1
Hitachi	15" XGA	TX38D81VC1CAD	1	0	1	1
Hitachi	15" SXGA+	TX38D91VC1CAD	1	1	0	0
Samsung	15" SXGA+	LTN150P4-L01	0	1	1	1

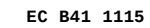
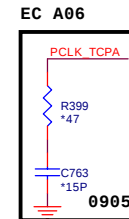
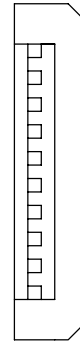




CRT PORT

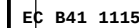
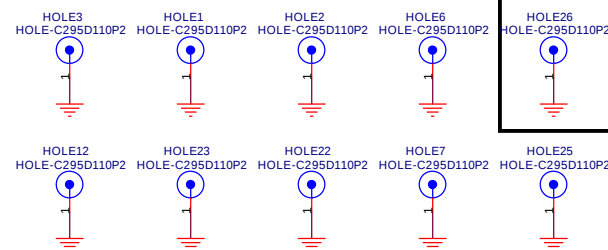
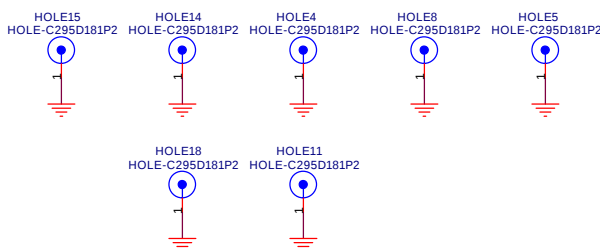
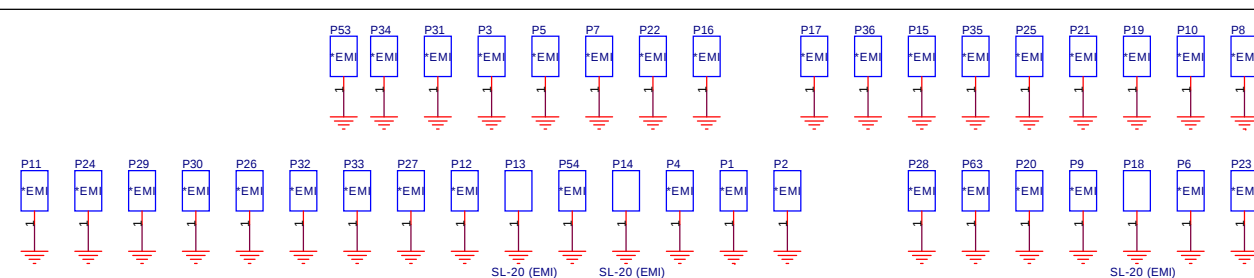
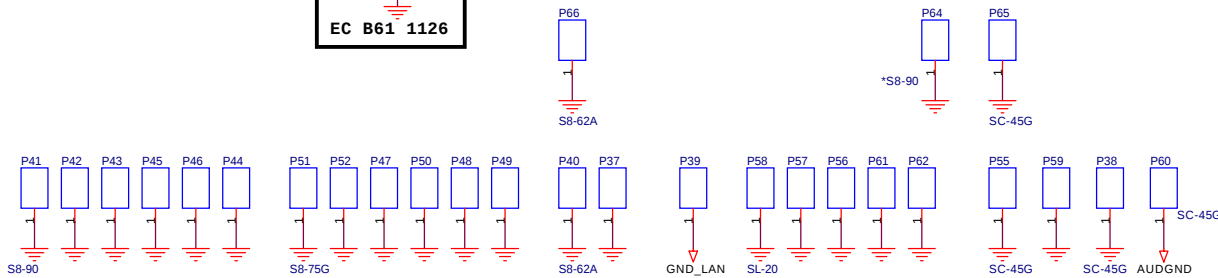


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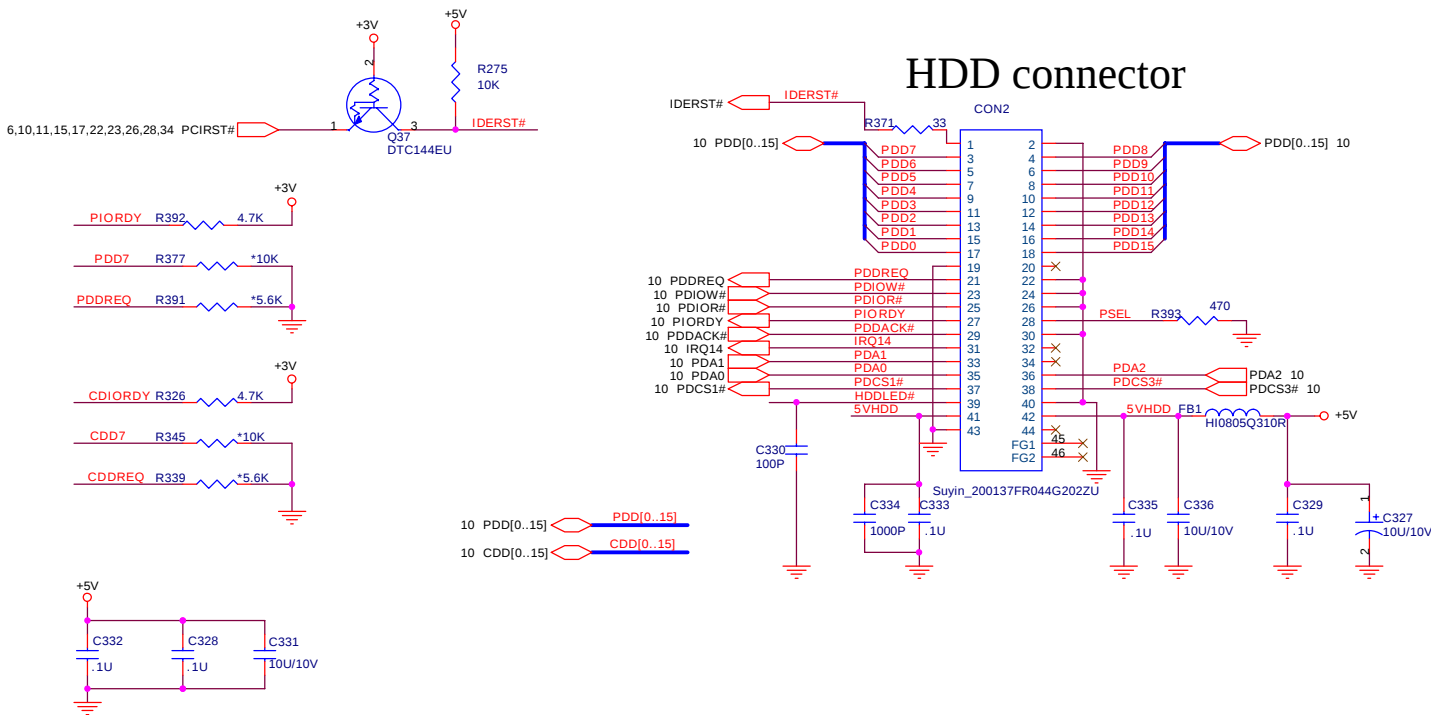


PROJECT :BF1
Quanta Computer Inc.

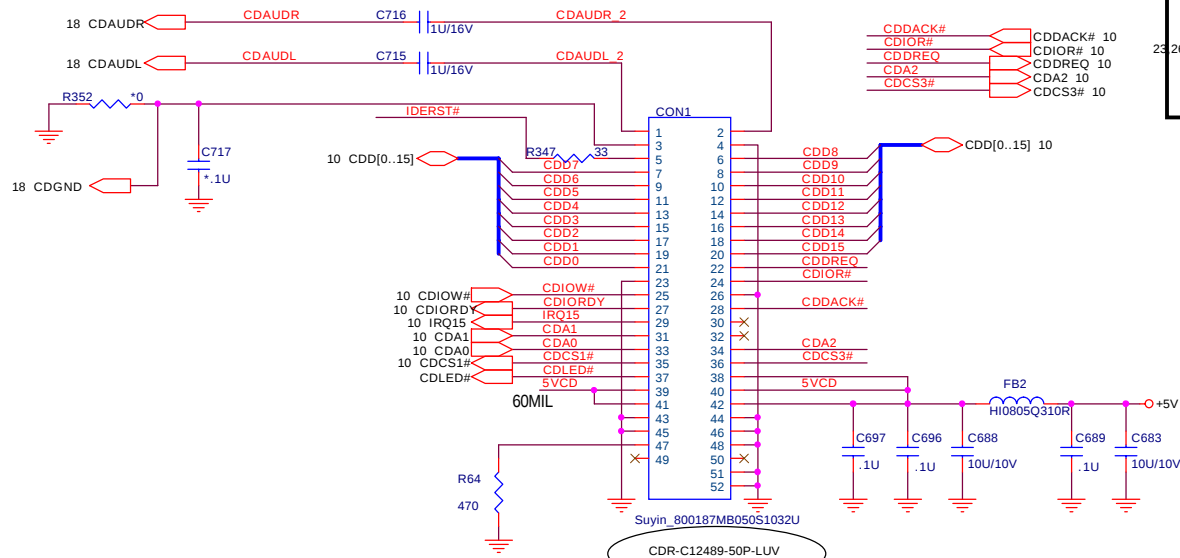
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HDD connector

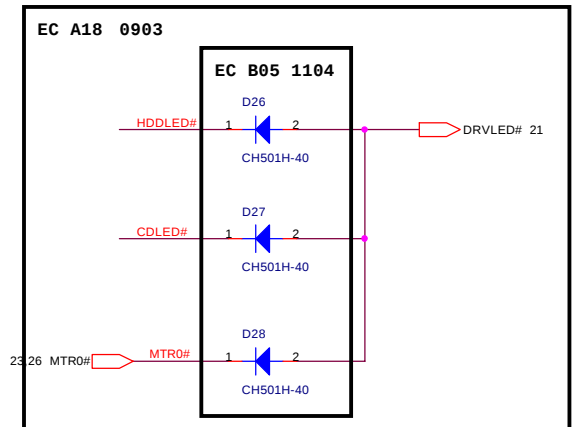


ODD connector



CDR-C12489-50P-LUV

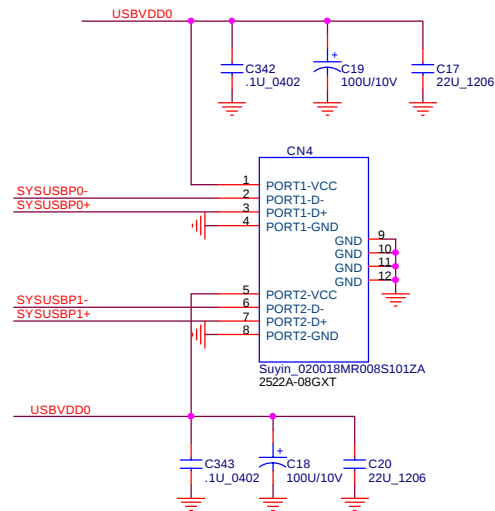
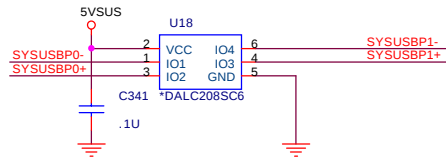
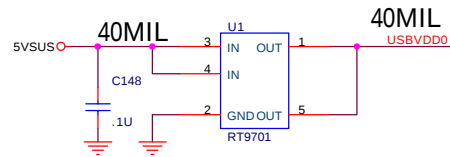
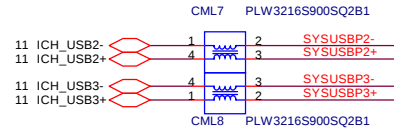
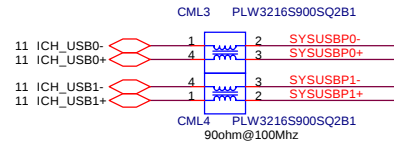
0912 Change footprint



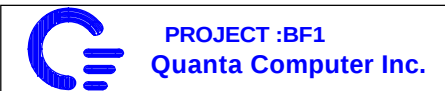
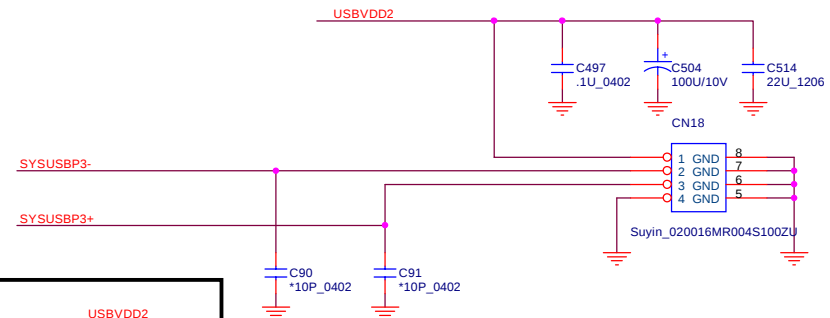
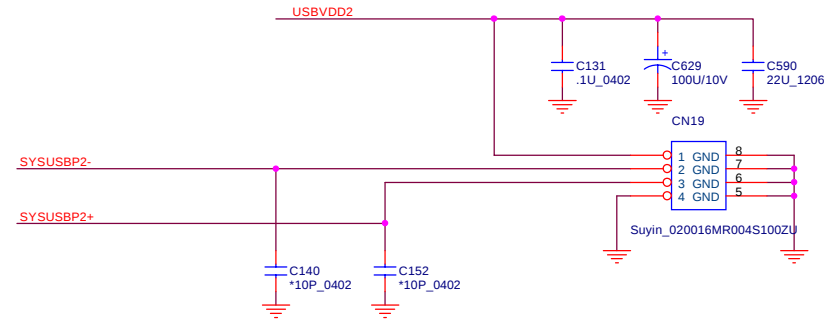
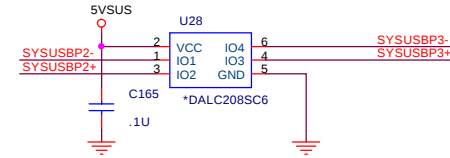
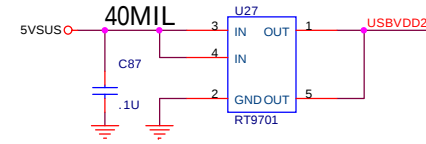
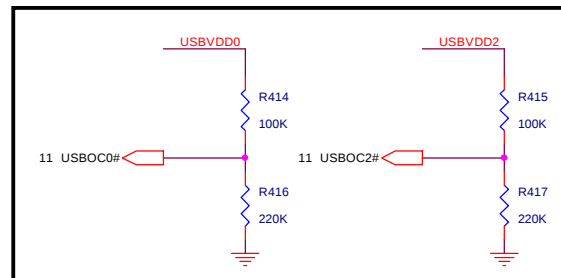
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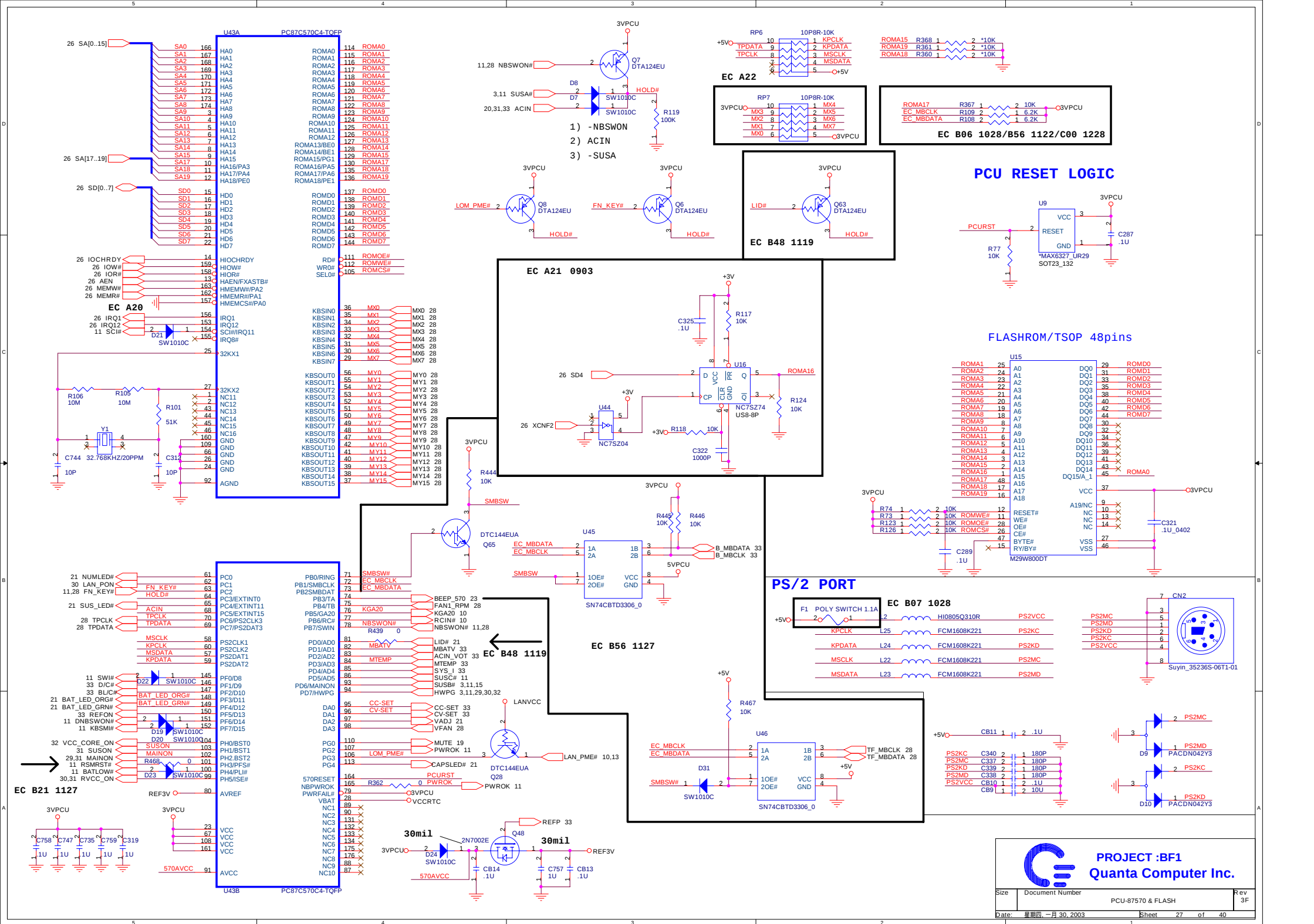
+5V 3,12,17,19,20,21,22,23,24,26,27,28,29,30,31,32,34

5VSUS 12,16,29,30,31,34

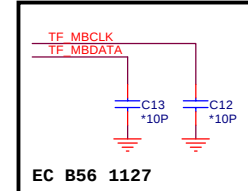
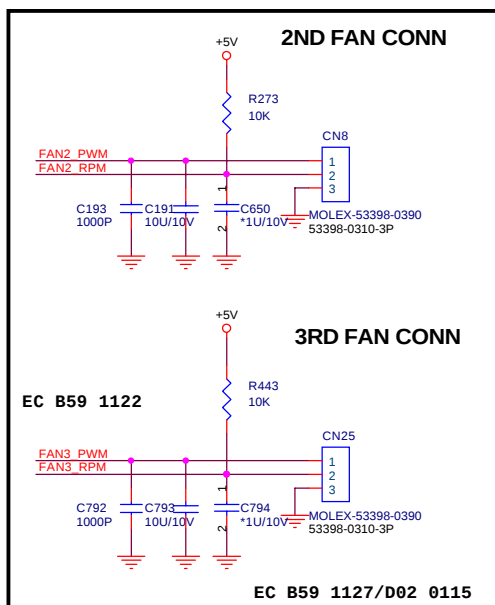
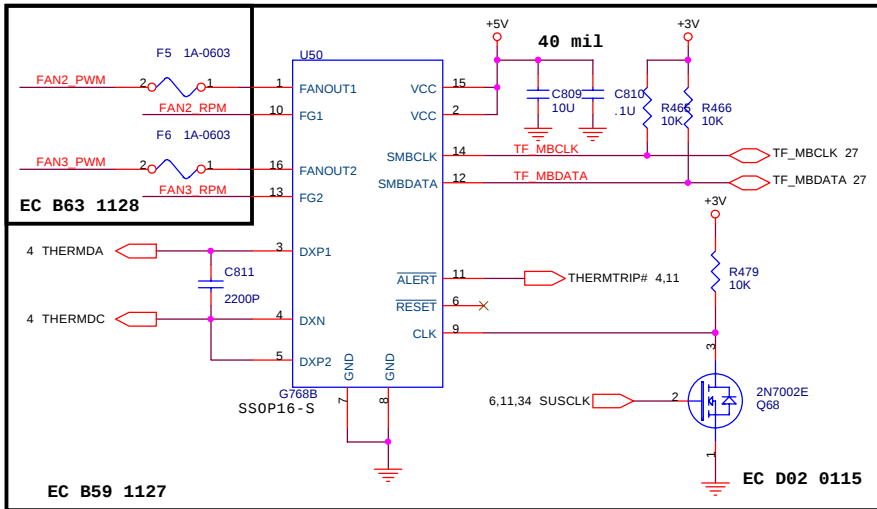
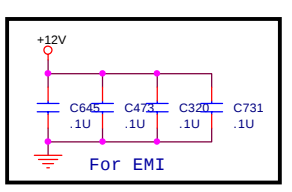
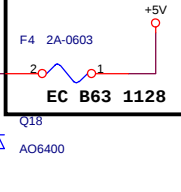
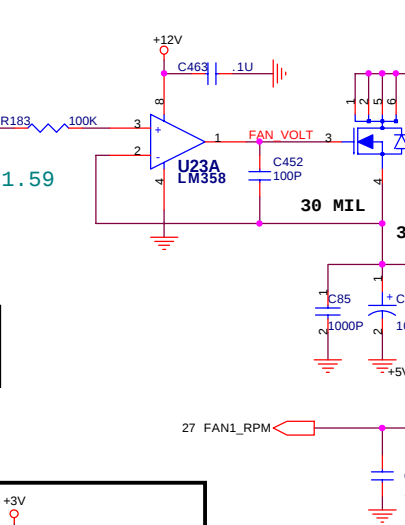
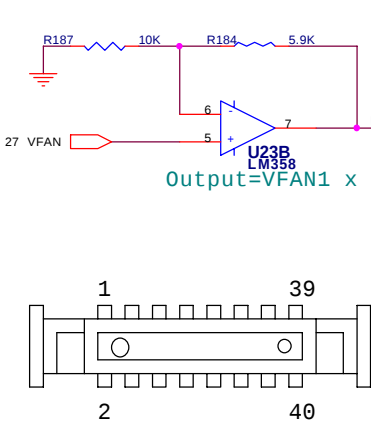
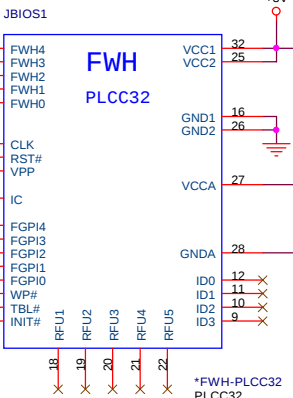
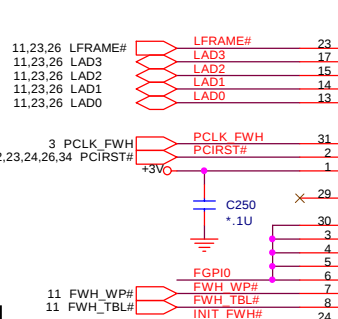
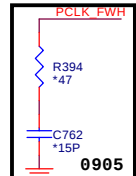
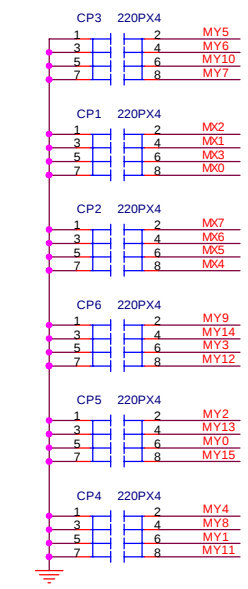
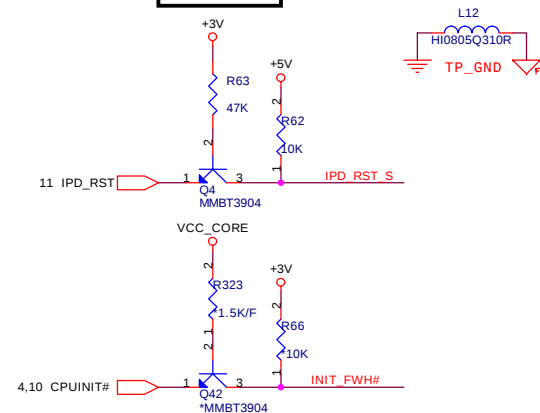
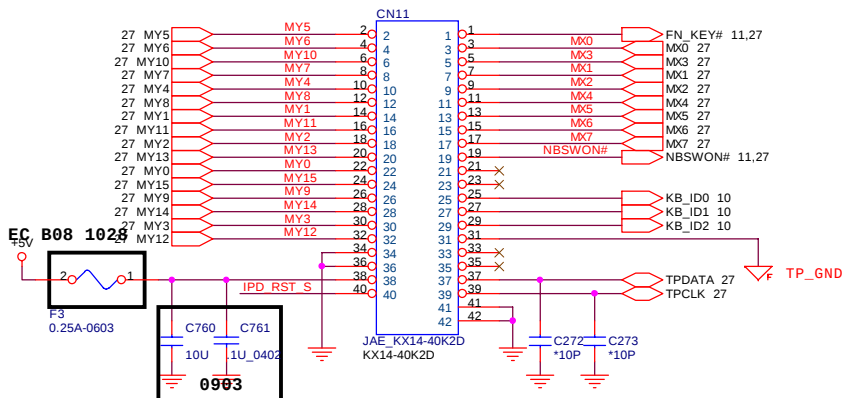


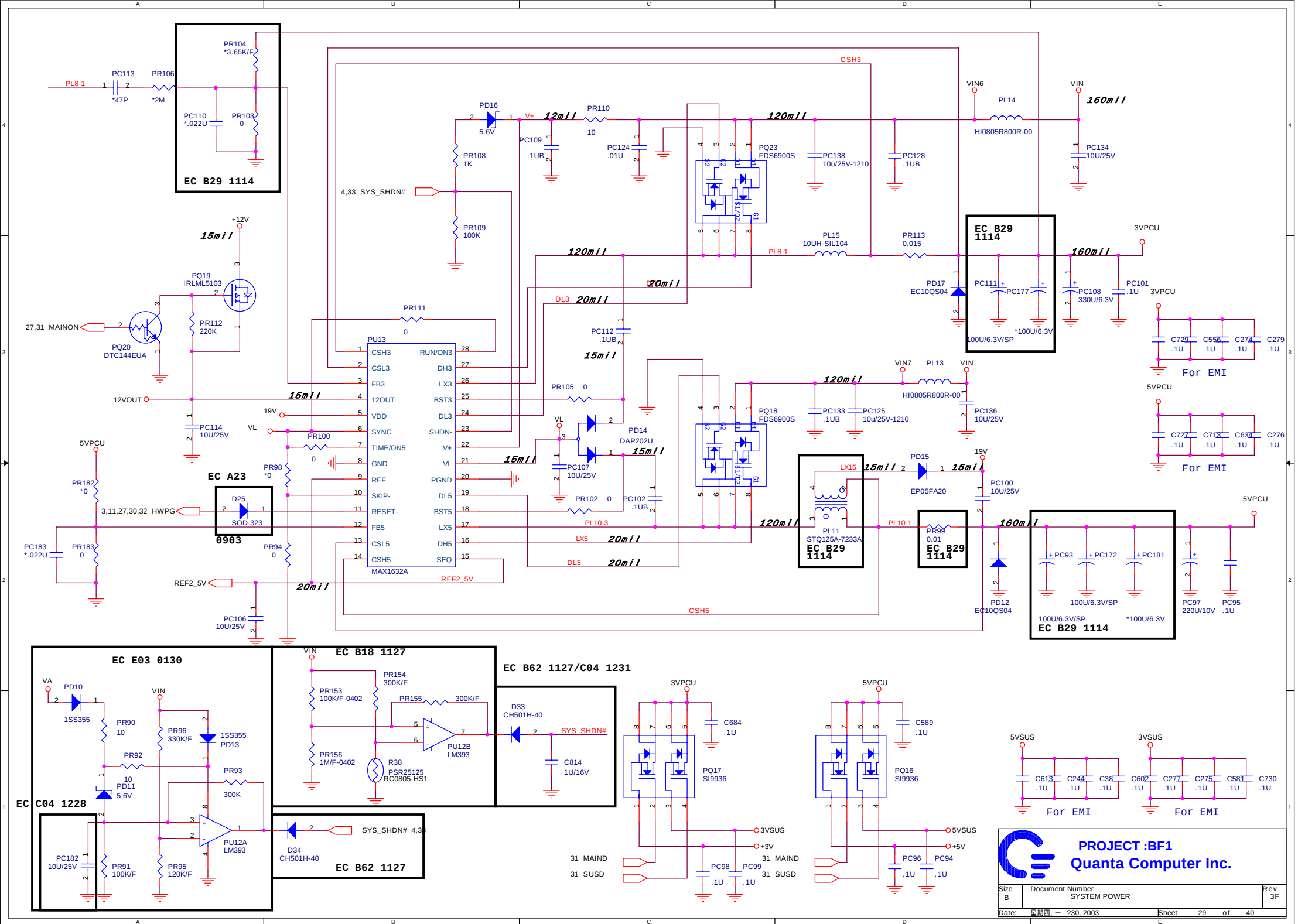
EC A36

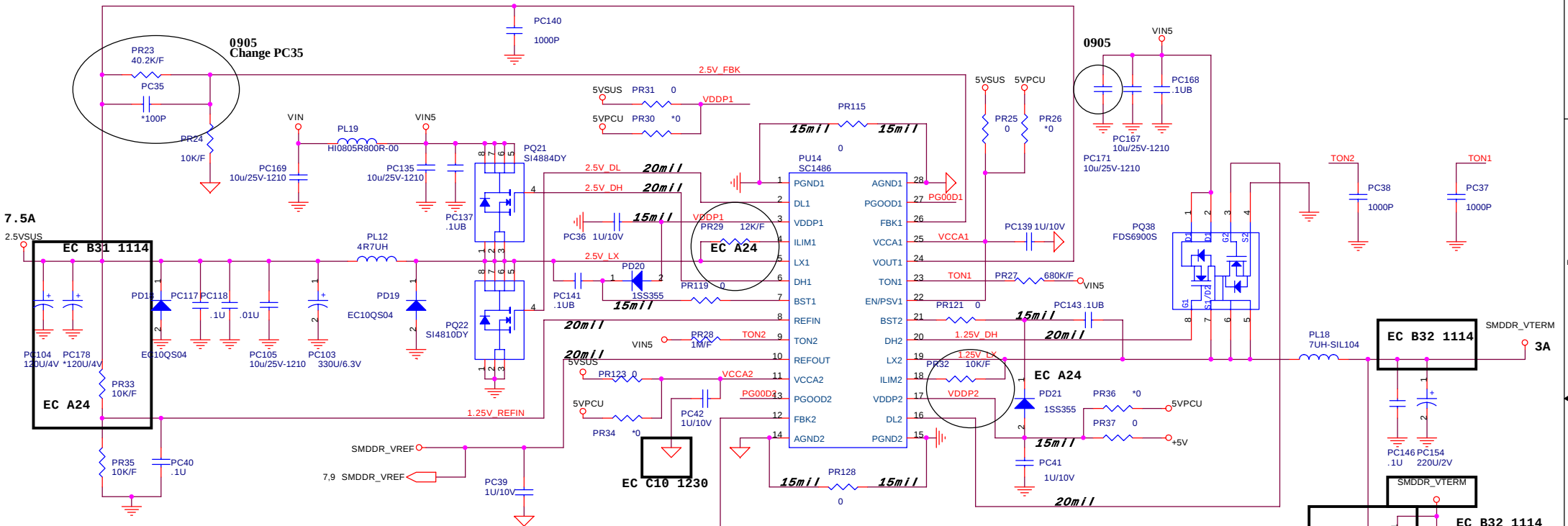




KEYBOARD/TRACK POINT







0905

PC104 47U/6.3V Change to 120U/4V

PC105 47U/6.3V Change to 10U/25V X6S

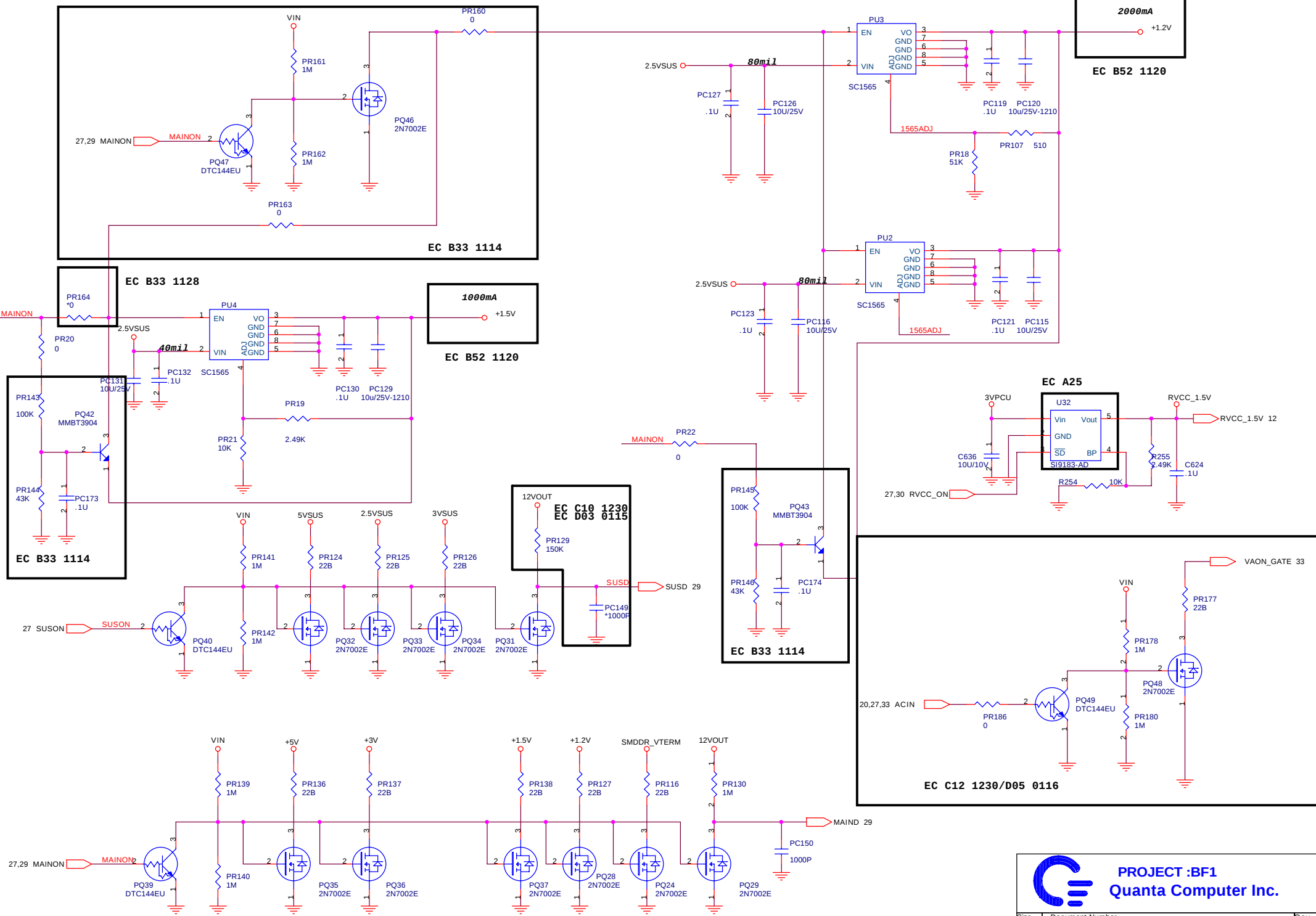
3,11,27,29,32 HWPG PG00D1

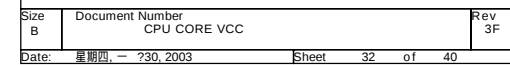
3,11,27,29,32 HWPG PG00D2

MODE	LAN_PON
AC S1-S5	HIGH
DC	
S3 WOL ENABLE	HIGH
S3 WOL DISABLE	LOW
S4	LOW
S5	LOW

10,13,14,27 LANVCC

10,11,12 RVCC_3V

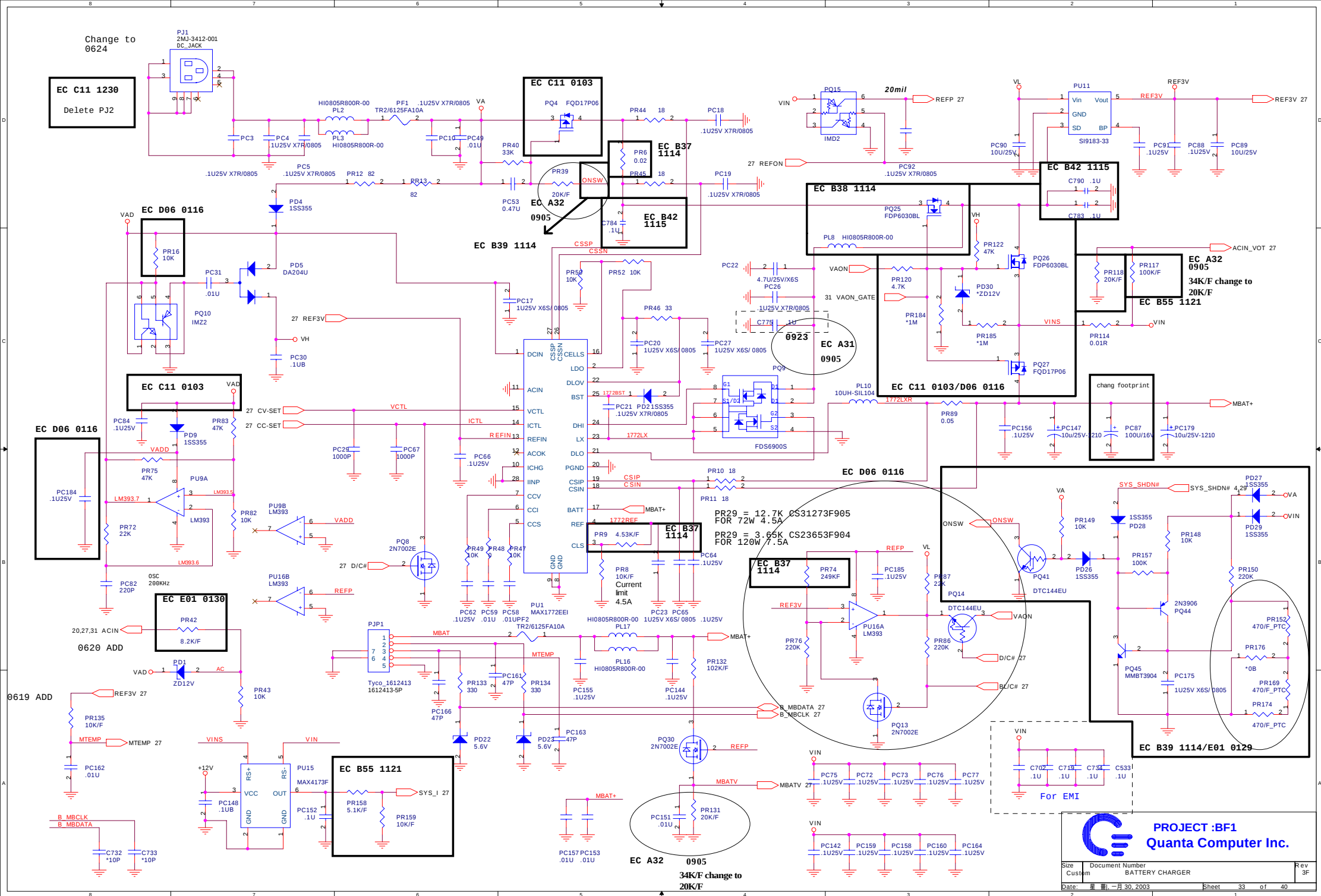


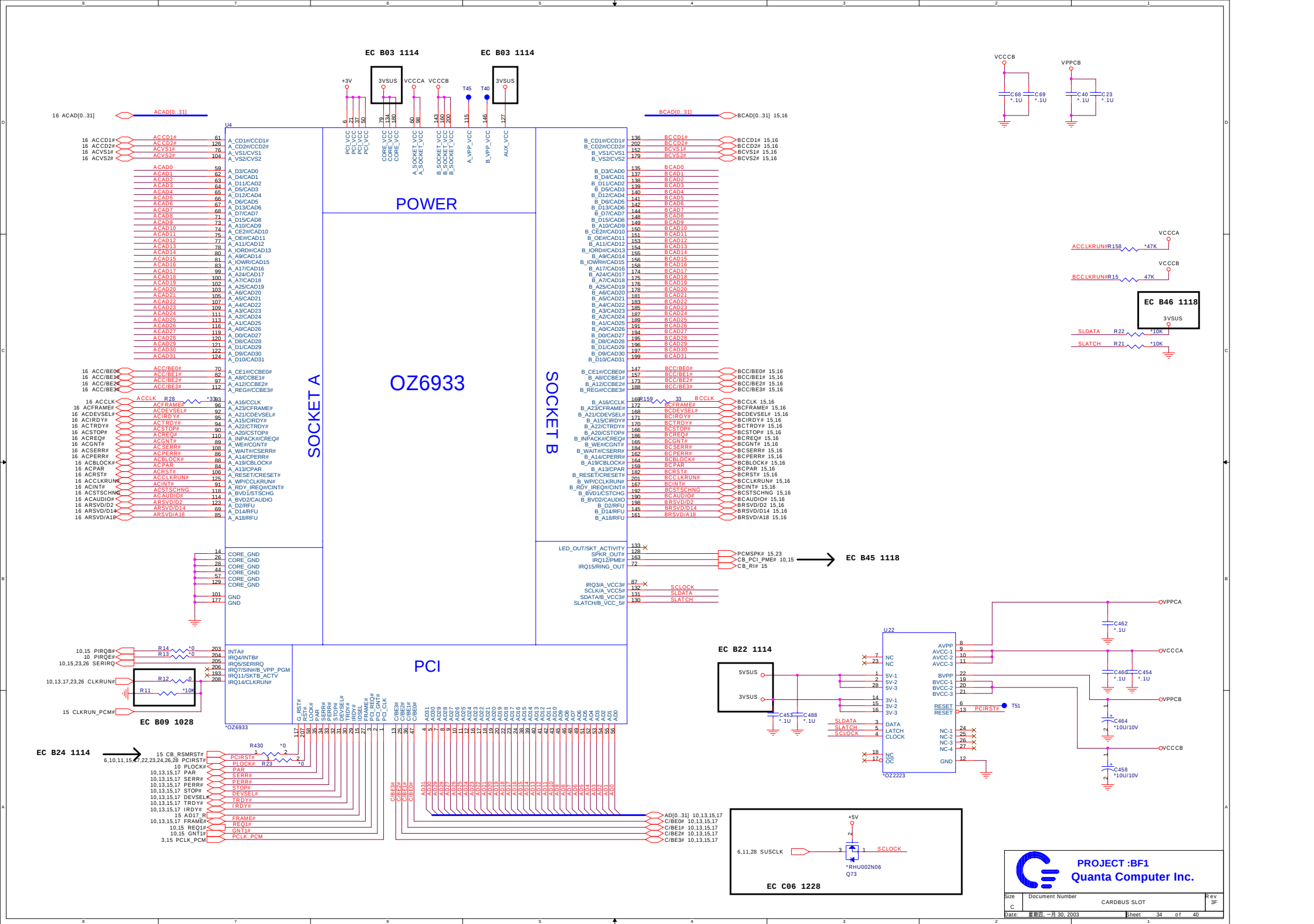


Change to 0624

EC C11 1230

Delete PJ2





PCI Device

DEVICE	IDSEL#	REQ#/GNT#	IRQ
ETHERNET	AD16	0	A
CARDBUS	AD17	1	B
MINI PCI	AD18	2	C,D

Power State

SIGNAL	SLP_S1# (SUSA#)	SLP_S3# (SUSB#)	SLP_S4# (TBD)	SLP_S5# (SUSC#)	CLKs	3/5VPCU	+*V	+*VSUS	RVCC_*V
STATE									
S0(Full ON)	H	H	H	H	ON	ON	ON	ON	ON
S1(POS)	L	H	H	H	STATIC	ON	ON	ON	ON
S3(S2R)	L	L	H	H	OFF	ON	OFF	ON	ON
S4(S2D)	L	L	L	H	OFF	ON	OFF	OFF	ON(AC_MODE) OFF(BATT_MODE)
S5(Soft OFF)	L	L	L	L	OFF	ON	OFF	OFF	ON(AC_MODE) OFF(BATT_MODE)

Voltage Rails

VOLTAGE	Power Plane	Active State	Control Signal
1.2V	VCC_CORE	S0-S1	VCC_CORE_ON
	VCC_VID	S0-S1	VCC_CORE_ON
	+1.2V	S0-S1	MAINON
1.25V	SMDDR_VTERM	S0-S3	SUSON
1.5V	+1.5V	S0-S1	MAINON
	RVCC_1.5V	(NOTE)	RVCC_ON
2.5V	2.5VSUS	S0-S3	SUSON
3.3V	3VPCU	S0-S5	(Always ON)
	+3V	S0-S1	MAINON
	3VSUS	S0-S3	SUSON
5V	RVCC_3V	(NOTE)	RVCC_ON
	VCCRTC	S0-S5	(Always ON)
	5VPCU	S0-S5	(Always ON)
	+5V	S0-S1	MAINON
	5VSUS	S0-S3	SUSON
3.3V,5V	VCCCB	S0-S1	
	VPPCB	S0-S1	
12V	+12V	S0-S1	MAINON

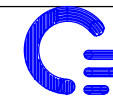
I2C / SMBUS ADDRESSING

DEVICE		ADDRESS
ICH4	DDR SO-DIMM 0	A0H
	DDR SO-DIMM 1	A2H
	CLOCK GEN (CY28346)	D2H/D3H
	SSC (ICS91718)	D4H/D5H
	EEPROM (24RF08C)	A8H-AFH
87570	GAS GAUGE CHIP	4EH
	G768B (THERMAL MONITOR	
	FAN PWM Controller	A7H
	2nd and 3rd FAN)	A8H

NOTE: REFER TO THE ABOVE "POWER STATE" TABLE

Revision History

Rev .	Date	Phase	Change List
1A	08/02 2002	DV	Initial release
2A	10/02 2002	SIV	See page 37
3A	12/04 2002	SIT	See page 38,39
3D	12/28 2002	SIT2	See page 40
3E	01/16 2003	SITR	See page 40
3F	01/29 2003	SVT	See page 40



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EC #/Page/Description/Part Affected/CMVC #

EC A003Change Q23 from NMBT3904 to DTC144EUAQ232069
EC A013Add level shifter on SELPSB0/PSBFSEL0Q552070
3Add EMC cap C766 0.1uF on U33 pin 5C766
3Add EMC cap C765 0.1uF on U8 pin 5C765
EC A024Remove CPURST# pull-upR332071
EC A034Update SYS_SHDN# circuitR38, Q2, Q161905
EC A046Add serial damping on CRTHS_VGA and CRTVS_VGAR412, R4132072
EC A056Add optional FET switch on M-GML strapping pinQ52, Q53, Q542073
EC A0610,13,15,17,23,26,28Add RC parallel terminator on all PCI clocks. R is 47 ohm and C is 15pF.R301/C670, R400/C764,
R18/C24, R165/C440, R399/C763, R94/C300, R394/C7622074
EC A0710Assign GPIO1 for "Power-On-Password Erase". Add PAD G2PAD G22004
EC A0811Connect ICH4 pin W20 to THERMTRIP# and R329 removed.R3291905
EC A0911Change BOARD_ID0 strapingR274, R288
EC A1013Change BCM5901 pin connection. Pin P7 and M11 are changed to NC and R186 is changed to a bead.L41, R224, R1861914
EC A1113Change U26 from Atmel AT24C64 to Fairchild FM24C64FLM8XU262075
EC A1213Remove Q29 and Q30Q29, Q302076
EC A1315Change CB_RI# from U3 pin 68 to 672077
EC A1418Change HP_PLG from U12 pin 18 to 17.R381 de-poped R3812078
EC A1519Change U13 from LM4871 to LM4890 and related circuit and partsU13, Q5, Q56, etc.1930
EC A1621Add 100K pull-up on LCD[0..3]RN61948
EC A1723Modify CN19 connection to support IBM-type FDD. FDDSENS# is moved to pin 36.R406, R407, R4081904
EC A1821, 24Modify HDDLED# circuit to include HDD/FDD/ODDQ49, Q50, Q511912
EC A1925Modify USB0C0# and USB0C2# circuitD2, D12, R414~4172079
EC A2026, 27Change U11 pin 73 to NC and U43 pin 157 to GND1908
EC A2127Modify flash ROM ROMA16 circuitU16, Q9, U441909
EC A2227Mount 10K on RP7 footprintRP71988
EC A2329Change PR101 to a diode SOD-323PR101, D252080
EC A2430Change part value:PC104, PC105, PR29, PR32, PC1652093
PC104 47U/6.3V change to 120U/4V
PC105 47U/6.3V change to 10U/25V X6S
PR29 7.5K/F change to 12K/F (for 2.5VSUS limIt)
PR32 7.5K/F change to 10K/F (for SMDDR_VTERM limit)
PC165 47U/6.3V change to 10U/25V X6S
EC A2531Change U32 from SI9183 to SI9183-ADU322094
EC A2632Change CPU_VID[0..4] connection to PU81910
Add serial diode between PR77, PR78, PR79, PR80, PR81 and 3.3VD?
EC A2732Change PR17, PR7 and PR4 from 1.5K/F PTC to 3.9K/F PTC (for VCC_CORE limIt)PR17, PR7, PR4
EC A2832Remove PR63 88.7K/FPR632095
EC A2932Add PR54 130K/FPR542096
EC A3032Change PU8 footprint from ssop28 to tssop28PU82097
EC A3133PD3 removedPD32098
EC A3233Change part value:2099
PR39 33K change to 20K (add PQ4 Vgs)PR39
PR118 and PR131 34K/F change to 20K/F (down reference voltage for 570 read)PR118, PR131
EC A348,9,19,25Change capacitor type to non-TAN typeC18, C19, C307, C537, C568, C642, C666, C668,
C504, C6292081
EC A35 4 Change thermal chip to MAX6648 U21
EC A36 11,25 Modify USB OC# circuit RN3, R414~417

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EC B00/3/Change R258 and R272 from 4.7K to 2.2K for rising time/R258,R272/2299
EC B01/6/Change R276 pull-up to +1.5V,and R284 pull-up to +3V/R276,R284
EC B02/11/Delete RN3 and add R423 and R424 pull-up to RVCC_3V for USB0C4# and USB0C#5/R423,R424
EC B03/15,34/Change Cardbus power plane from +3V to 3VSUS and add R469,R470 to support Ti & O2/U3,R164,Q40,C26,C27,C34,C75,C74,C70,U4,R469,R470
EC B04/22/Change gate control signals of Q10 and Q14 to PCIRST# in order to avoid the system into test mode/Q10,Q14/2323
EC B05/24/Del Q49,Q50,Q51 and add D26,D27,D28 to isolate DSAP# per channel/Q49,Q50,Q51,D26,D27,D28
EC B06/27/Change R108 and R109 from 4.7K to 1.5K for rising time/R108,R109/2299
EC B07/27/Change PS/2 fuse(F1) to poly-switch /F1/2411
EC B08/28/Add serial fuse(F3 Stech 39194 1608FF-250MA 0.25A / 0603) to VCC on KB/TP (CN11 pin38)/CN11,F3
EC B09/34/Mount R12 and R11 is un-populated/R12,R11
EC B10/18/Change R80,R373 from 2.7K to 4.7K,the R81,R374 are changed from 47K to 2.7K,and C772 is un-populated/R80,R81,R373,R374,C772
EC B11/18/Change R381 to be un-populated/R381
EC B12/19/Add BEEP control circuit Q46,Q66,R92,R376,R453,R457,C293,C740/Q46,Q66,R92,R376,R453,R457,C293,C740
EC B13/19/Change Audio amp from LM4890 to TAP0312/See page 19
EC B14/11/Populate AC'97 pull-down/R237,R238,R249,R252
EC B15/17/Change R359 from 47 Ohm to 33 Ohm/R359
EC B16/22/Change Bead of HSYNC/VSYNC/L6,L8
EC B17/22/Change Bead&Cap&Res of the pie-filter of RGB/L3,L5,L7,C2,C4,C5,C6,C7,C14,C15,C16,R2,R6,R7
EC B18/4,29/Delete R36,Q2 and add PR153,PR154,PR155,PR156 to modify thermal shutdown circuit/PR153,PR154,PR155,PR156,R38,PU12
EC B19/8/Reserve R433 to GND for CRT ripple/R433
EC B20/15/Add R431 connect to U3.70 SUSPEND# and SUSB#/R431,U3
EC B21/11,27/Add R468 for RSMRST# change to 570 control and un-populated R269,R271,C648/R468,R269,R271,C648
EC B22/16,34/Change +5V to 5VSUS and +3V to 3VSUS/U7,C41,C58,C45,C65,C453,C488
EC B23/15/Change U3.66 Globle_RST# from PCIRST# to 3VSUS RC circuit R436,R437,C788 CB_RSMRST#/U3,R436,R437,C788
EC B24/34/U4.117 through add R430 connect to CB_RSMRST#/U4,R430
EC B25/11/Change R343 pull up from RVCC_3V to 3VSUS for wakeup FN_key/R343
EC B26/15/un-populated R164 for CB suspend/R164
EC B27/18/Change R365 from 4.7K to 47K adjust PC-BEEP sound/R365
EC B28/19/Change R102 from 20K to 200K adjust gain/R102
EC B29/29/Change PR103 from 10KF to 0,PC111,PC93,PC172 from 47U/6.3V to 100U/6.3V,PR99 from 0.015 to 0.01,PL11 from STQ124-1022 to STQ125A-7233A
un-populated PR104,PC110/PR103,PR104,PC110,PC111,PC93,PC172,PR99,PL11
EC B30/3,9/Add R451,D29 to CLK_PERDN# to prevent leakage,add R450 pull up SA0 /R450,R451,D29
EC B31/30/Del JP7,8,11 2.5VS short to 2.5VSUS power plane,Del 2.5VS net ,PC104,PC105 connect to 2.5VSUS/JP7,JP8,JP11,PC104,PC105
EC B32/30/Del JP14,15 VDDR short to SMDDR_VTERM power plane,Del VDDR net ,PC165,PD24 connect to SMDDR_VTERM/JP14,JP15,PC165,PD24
EC B33/31/Add new circuit PR143,PR144,PR145,PR146,PR160-PR164,PC173,PC174,PQ42,PQ43,PQ46,PQ47/PR143,PR144,PR145,PR146,PR160-PR164,PC173,PC174,
PQ42,PQ43,PQ46,PQ47
EC B34/32/Change PR62 from 0 to 56,PR54 from 130KF to 680KF,PR64 from 1.6KF to 2.4KF,PR4,7,17 from 3.9K/PTC to 2.7K/PTC/PR62,PR54,PR64,PR4,PR7,
PR14



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EC B35/32/Mount PC79,PR56,PD6,PD7,PD8,Add PR147,Change PQ1,5,6 from FDP7030BL to FDB7045L,PR1,3,14 from 0 to 2 ,add PR175/PC79,PR56,PD6,PD7,PD8,PR147,PR175PQ1,PQ5,PQ6,PR1,PR3,PR14

EC B36/32/Del JP2,JP3,JP5 and short/JP2,JP3,JP5

EC B37/33/Change PR9 from 3.65KF to 4.87KF,PR74 from 258KF to 249KF,and change PR6 footprint/PR9,PR74,PR6

EC B38/33/Modify PL8 connect to PQ25 pin5,6,7,8/PL8,PQ25

EC B39/33/Add new circuit PQ44,PQ45,PQ41,PR148,PR149,PR150,PR152,PR169,PR174,PR176,PC175,PD26/PQ44,PQ45,PQ41,PR148,PR149,PR150,PR151,PR152,PR169,PR174,PR176,PC175,PD26,PD27,PD28,PD29

EC B40/11/Add R435 to GND for USBRBIAS and unpopulated R435/R435

EC B41/23/Add a new HOLE26, and change HOLE21 footprint to HOLE-C295D110P2

EC B42/13,18,33/Add L49,L50,L51,L52,L53,C780,C781,C782,C783,C784,C786,C787,C790 For EMI solution/L49,L50,L51,L52,L53,C780,C781,C782,C783,C784,C790,C786,C787

EC B43/18/Add a C785 TO U12 AVDD power plane/C785

EC B44/11/Change MB ID form ID1 to ID 2, populated R270,R288, un-populated R268,R274/R268,R274,R270,R288

EC B45/10,15,34/Change U3.59 and U4.163 net from PCI_PME# to CB_PCI_PME# and Add Q62,R438 to protect CB_PCI_PME# leakage/U3,U4,Q62,R438

EC B46/34/Change R22 power plane from +3V to 3VSUS, and Q1 from +5V to 5VSUS/R22,Q1

EC B47/32/Change PR69 from 10K to 1K Strong Pull high/PR69

EC B48/27/Add Q63,R439 support DC mode LID switch S3 resume, and LID# change to U43 pin 81/Q63,R439

EC B49/12/Add R448 to 5VPCU and D30 to RVCC_3V and D32 to 5VSUS for USB OC[5:0]# 5V tolerance/R448,D30,D32

EC B50/11,17,18/Add R441 for AC_RESET# and del minPCI AC LINK signal/R441,R167,R168,R169,R171,C446,L37,C444,R91,R372,C741,C742

EC B51/12/Add C789 between +1.5V and +3V/C789

EC B52/31/Delete JP12,JP13 and short to +1.5V,delete JP9,JP10 and short to +1.2V/JP12,JP13,JP9,JP10

EC B53/13/Add R194,T62,T63,T64 support ATE test/R194,T62,T63,T64

EC B54/14/CN1 pin 14 change to no connect/CN1

EC B55/33/Change PR117 from 102K/F to 100K/F and add PR158,PR159 to PU15 pin6 output/PR117,PR158,PR159

EC B56/27,28/Add U45,U46,R444,R445,R446,Q65,D31,R467, delete Q12,Q15 for separate SMBus/U45,U46,R444,R445,R446,Q65,Q12,Q15,D31,R467

EC B57/13/U25 pin A4 IDSEL add R447/R447

EC B58/27/Delete C47 and U7 pin 9 floating don't suporrt 12Vcard/C47

EC B59/4,28/Delete Max6648 thermal sense change to G768B and FAN2/3 control/U21,R139,R136,R134,R137,R145,C366,C370,U50,Q68,R465,R466,C809,C810,C811Q36,C649,Q64,C791

EC B60/11/Add R471 Pull-up ICH4 THRM# to +3V/R471

EC B61/23/Add FDD INDEX# signal damper R449 and cap C795/R449,C795

EC B62/4,29/Add D33,D34,D35 to prevent leakage/D33,D34,D35

EC B63/28/Add F4,F5,F6 Fan fuse/F4,F5,F6

BF1 / F2-Note Schematic EC Tracking Record (SIT-SIT2)Dec 28, 2002

EC #/ Page/ Description/ Part Affected/ SIT --> SIT2

EC C00/27/Change R108,R109 from 1.5K to 6.2K for SMBus/R108,R109

EC C01/19/Change R92 from 47K to 8.2K for Beep sound level/R92

EC C02/11/Change R441 from 100hm to 470hm for AC_RESET# overshoot, Add C815 1u to thermtrip#/R441,C815

EC C03/30/Populated PD24/PD24

EC C04/29/Add a PC182 10uF/25V parallel to PR91 and a C814 between SYS_SHDN# and GND to absorb Vin Voltage drop/PC182,C814

EC C05/4,11,20/Add H/W throttling circuit Q69-Q72,R476,R477/Q69,Q70,Q71,Q72,R476,R477

EC C06/34/Add a Q73 for SCLCK/Q73

EC C07/11/Change board ID to REV:D "0011" populated R274 unpopulated R288/R274,R288

EC C08/19/Change gain to 10dB R462,R463 populated,R461,R464 un-populated and change R472,R473 to 4.7K/R461,R462,R463,R464
R472,R473

EC C09/10/Change Q62 to DTC144EUA, and delete R438 for CB_PCI_PME#/Q62,R438

EC C10/30,31/Change R253,R199 to 1M,PR129 to 150K,un-populated PC149 for 5VSUS knee,change PC42 from DGND to AGND/R253,R199,
PR129,PC149,PC42

EC C11/33/Delete PJ2 foot-print,change PQ4,PQ27 from SI4425DY to FQD17P06,PQ25,PQ26 from SI4884 to FDP6676 ,change PR120 from
4.7K to 1KF,REFP change to VAD/PJ2,PQ27,PR120

EC C12/31/Add PQ48,PQ49,PR177-PR181 for decrease leakage current circuit/PQ48,PQ49,PR177-PR181

BF1 / F2-Note Schematic EC Tracking Record (SIT2-SITR)Jan 16, 2003

EC #/ Page/ Description/ Part Affected/ SIT2 --> SITR

EC D00/4/Change R37 from 56 to 330 for SYS_SHDN#,Reserve R480 51 Ohm pull-up to vcore for CPURST#

EC D01/15/Mount R164 10K and unpopulated R431 for CardBus suspend

EC D02/28/Change Q68 circuit for leakage, unpopulated C650,C794

EC D03/31/Change PR129 from 100K to 150K

EC D04/11/Change board ID to REV:E "0100" populated R260,R268,R288 10K unpopulated R263,R274,R270/R274,R270,R260,R288,R268,R263

EC D05/31/Change discharge circuit,delete PR179,PR181/PR179,PR181

EC D06/33/Change PR16 5.1K to 10K, change power circuit PU9,PU16,add bypass capacitor PC184,PC185, and reserve PD30,PR185,PR184(un-populated)

EC D07/32/Add 3 input capacitor PC186,PC187,PC188

BF1 / F2-Note Schematic EC Tracking Record (SITR-SVT)Jan 30, 2003

EC #/ Page/ Description/ Part Affected/ SITR --> SVT

EC E00/18/Change R365 from 47K to 20K for modem card tone sound loudly /R365

EC E01/33/Change PR152,PR169,PR174 footprint to 0603 size,and change PR42 from 10K to 8.2KF/PR152,PR169,PR174,PR42

EC E02/11/Change board ID to REV:F "0101" populated R274 10K unpopulated R288/R274,R288

EC E03/29/Change PR96 to 330KF,PR95 to 120KF,PR91 to 100KF/PR91,PR95,PR96

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		Quanta Computer Inc.	
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