BL1

CPU CORE
SENTECH
SC451
Page:25
→ VCC_CORE

+3VPCU
+3V_S5/+3VSUS
+3V
+5VSUS/+5V
10V/15V
+1.8V_S5
MAXIM
MAX8744ETJ+ Page:26
→ +3VPCU, +3V_S5, +3VSUS, +3V, +5VSUS, +5V, 10V/15V, +1.8V_S5

+1.8VSUS/+1.8V
+1.2V
MAXIM
MAX8743EEI Page:27
→ +1.8VSUS, +1.8V, +1.2V

+1.05V
SENTECH
SC4215*2 Page:29
→ +1.05V

+0.9VSUS
+0.9V
GMT
G2996 Page:26,29
→ +0.9VSUS, +0.9V

BATTERY CHARGER
MAXIM
MAX8724 Page:28

CLOCK GEN
RTM865-300
+3V Page:4

CELERON-M/PENTIUM-M
INTEL Mobile_479 CPU
Page:2, 3

HOST BUS 400MHZ

NB
RC410MB/RC410MD
ATI
Page: 5, 6 , 7, 8

DDR-II SODIMM1 Page: 9
DDR-II SODIMM2 Page: 9
DDR-II

RGB → **CRT (option)** Page: 10
LVDS → **LVDS** Page: 10

2X PCIE

SB
ATi SB450
Page: 11, 12, 13, 14

SATA HDD Page: 18 — SATA
IDE-ODD Page: 18 — ATA 66/100
HD AUDIO

PCI BUS 33MHZ
USB 2.0
LPC 33MHZ

ENE PCMCIA
CB1410 (option)
AD17
REQ3# / GNT3#
INTE#
Page: 16
→ **TYPE II SLOT** Page: 16

MINI-PCI
Wireless LAN
AD20
REQ1# / GNT1#
INTG# , INTH#
Page: 17

REALTEK
RTL8100CL
AD18
REQ0# / GNT0#
INTF#
Page: 15
→ **BOTHHAND TRANSFORMER NS0013** Page: 15
→ **RJ45** Page: 15

AUDIO CODEC
REALTEK
ALC861
Page: 19

GMT
G1432+G1410
Page: 20

MODEM
AGERE
DELPHI-MOM
Page: 21,22

KBC
NS
PC97541V
Page: 23

SYSTEM
USB PORT *2
USB2,3 Page: 17

MIC IN Page: 20
SPEAKER Page: 20
LINE OUT Page: 20
RJ11
Touchpad Page: 24
Keyboard Page: 24
FLASH Page: 24
FAN Page: 24

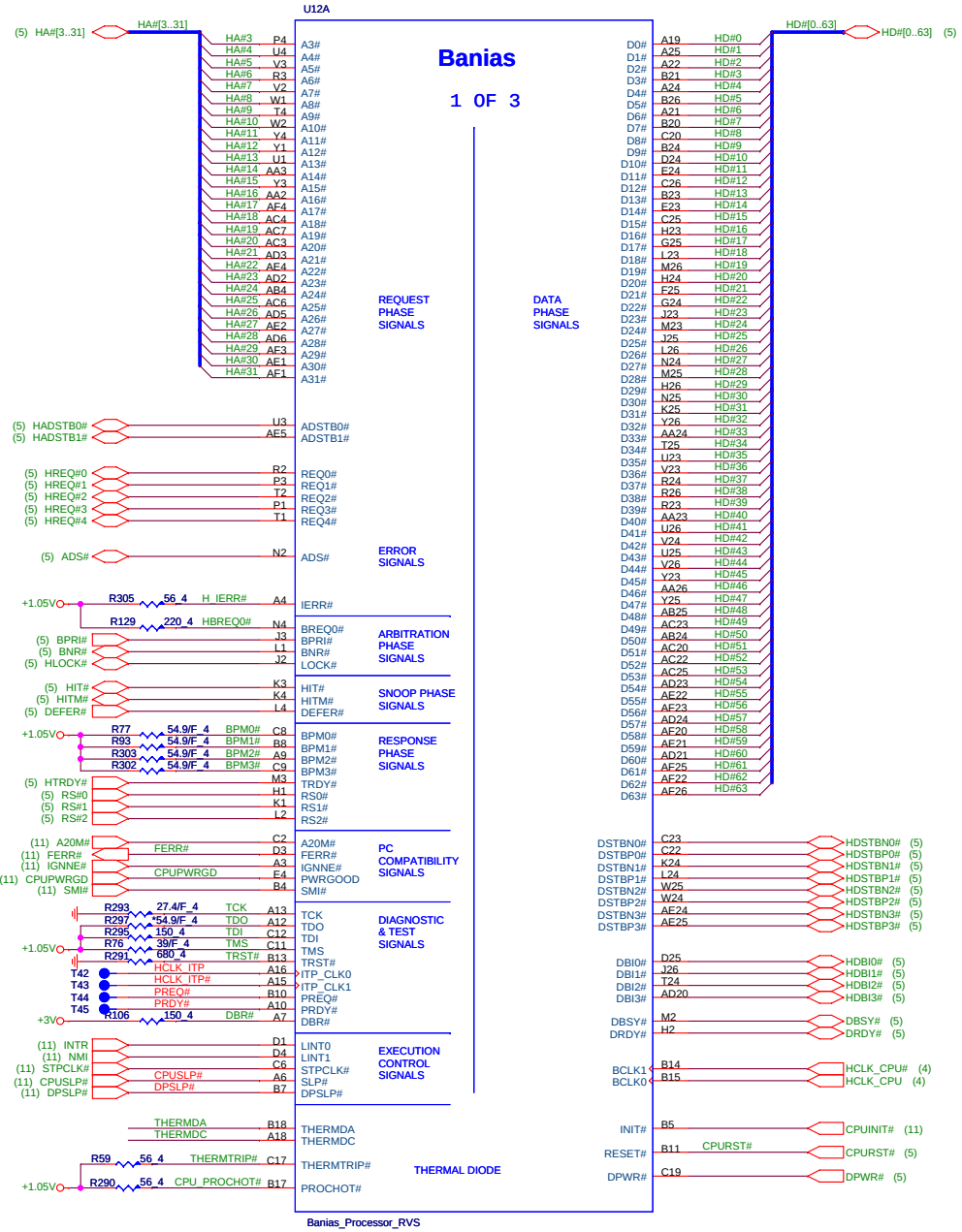
Power State Table

Power Name	Control Signal	Power State	Power Source
VCC_CORE	VRON	S0	VIN
+3VPCU	N/A	ALWAYS	VIN
+3V_S5	S5_ON	S0-S5	+3VPCU
+3VSUS	SUSON	S0-S3	+3VPCU
+3V	MAINON	S0	+3VPCU
+5VPCU	N/A	ALWAYS	VIN
+5V_S5	S5_ON	S0-S5	+5VPCU
+5VSUS	SUSON	S0-S3	+5VPCU
+5V	MAINON	S0	+5VPCU
15V/10V	N/A	S0	+5VPCU
+1.2V	MAINON	S0	VIN
+1.05V	MAINON	S0	+1.8VSUS
+0.9V	MAINON	S0	+1.8VSUS
+1.8V_S5	S5_ON	S0-S5	+3VPCU
+1.8VSUS	SUSON	S0-S3	VIN
+1.8V	MAINON	S0	+1.8VSUS

PROJECT : BL1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

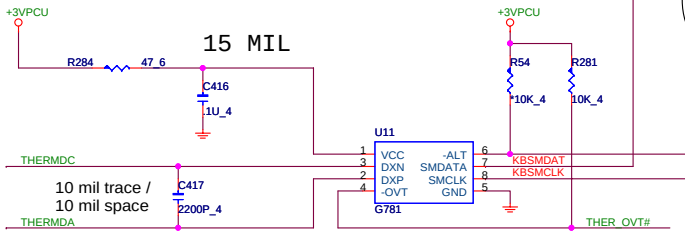
Date: Monday, April 03, 2006 Sheet 1 of 30

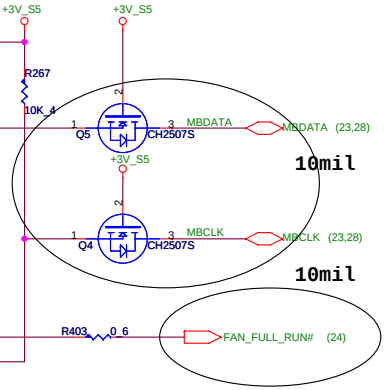


CPU

H/W MONITOR

SMB setting : thermal Alert temp is 85
thermal over temp is 127

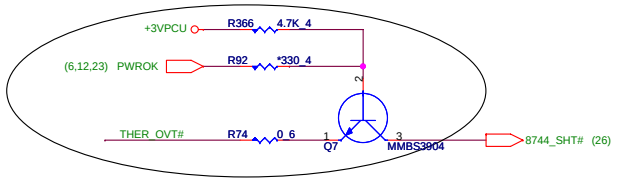


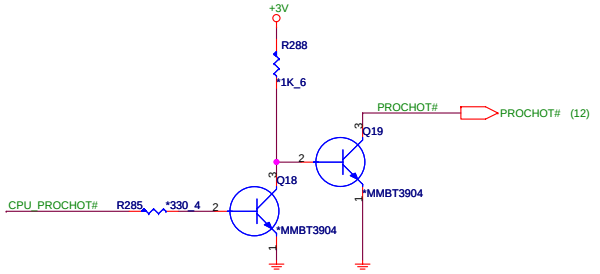


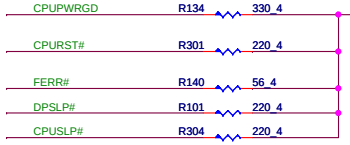
03/22 Change the power supply into Always.

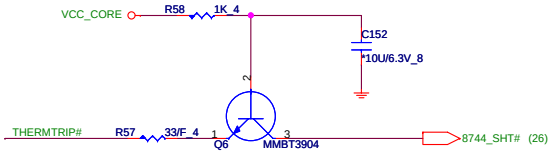
SMBus SLAVE ADDRESS: 98

	-OVT	-ALT
CPU	127	
Ambient		85







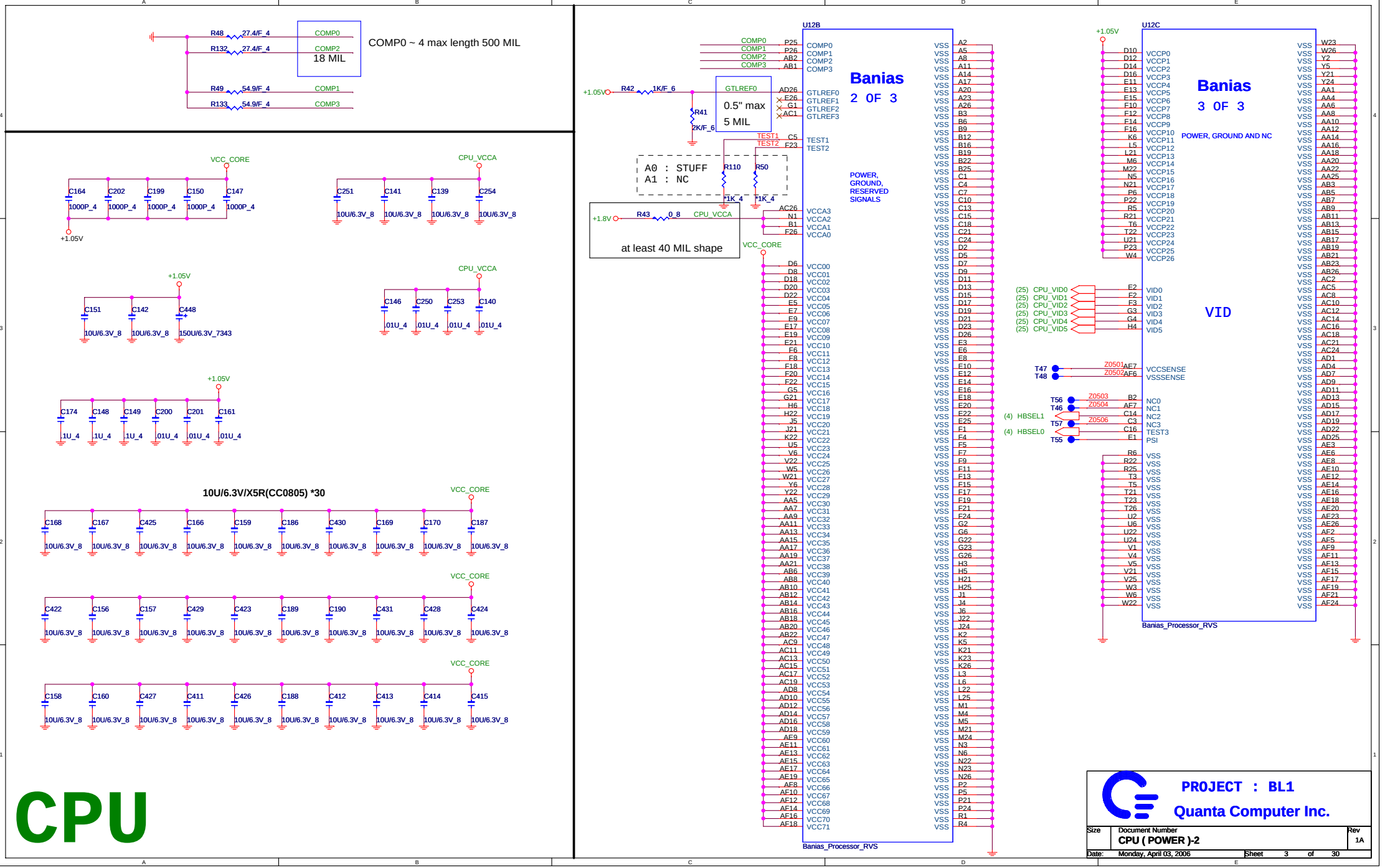


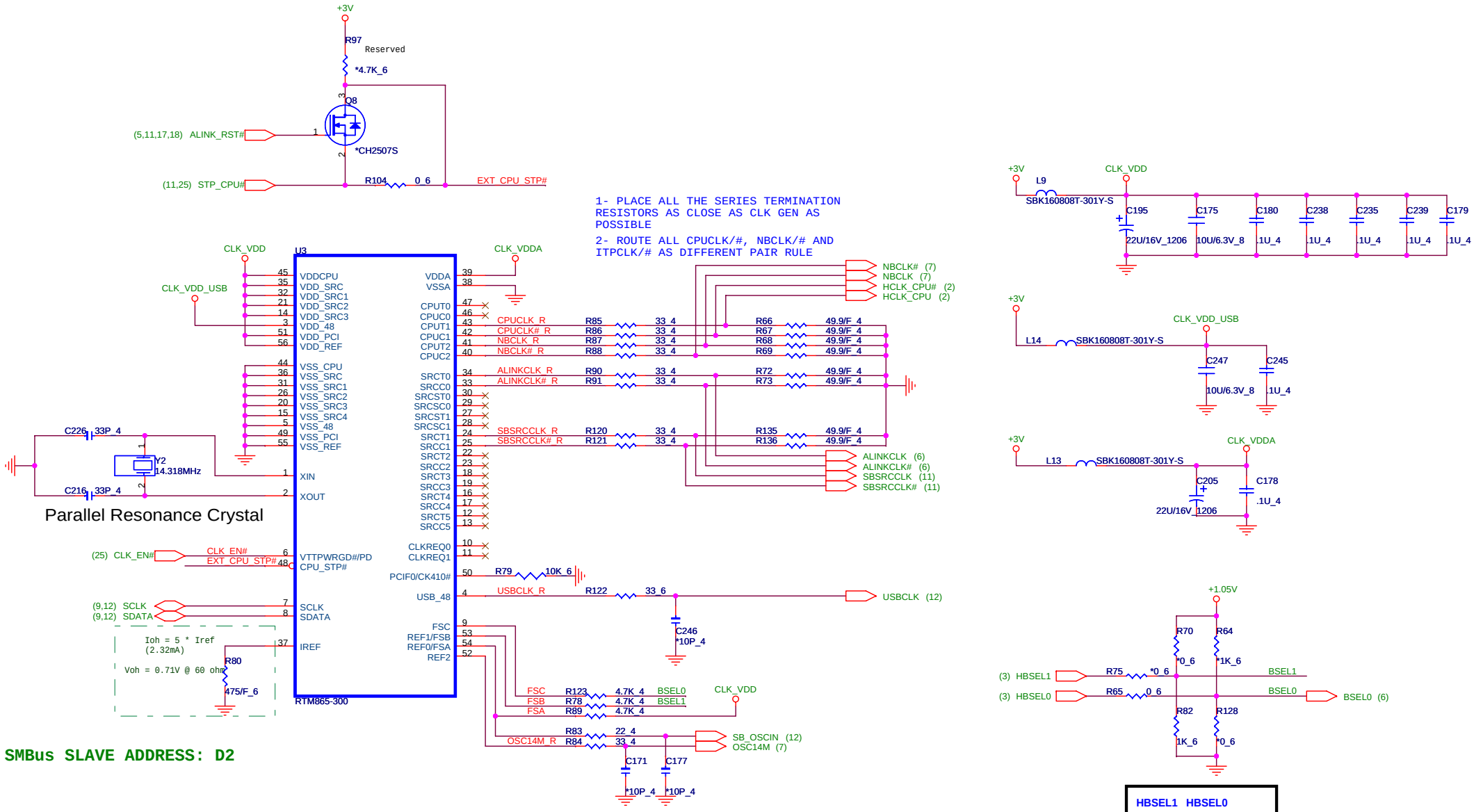
PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	CPU (HOST BUS)-1	2A

Date: Monday, April 03, 2006 Sheet 2 of 30


R48 27.4/F_4
R132 27.4/F_4
R49 54.9/F_4
R133 54.9/F_4
COMP0
COMP2
18 MIL
COMP1
COMP3
COMP0 ~ 4 max length 500 MIL
VCC_CORE
C164 C202 C199 C150 C147
1000P_4
+1.05V
CPU_VCCA
C251 C141 C139 C254
10U/6.3V_8
C151 C142 C448
10U/6.3V_8 150U/6.3V_7343
C146 C250 C253 C140
.01U_4
C174 C148 C149 C200 C201 C161
1U_4 .01U_4
10U/6.3V/X5R(CC0805) *30
C168 C167 C425 C166 C159 C186 C430 C169 C170 C187
C422 C156 C157 C429 C423 C189 C190 C431 C428 C424
C158 C160 C427 C411 C426 C188 C412 C413 C414 C415
CPU
U12B
Banias
2 OF 3
COMP0 COMP1 COMP2 COMP3
P25 P26 AB2 AB1
GTLREF0 GTLREF1 GTLREF2 GTLREF3
AD26 E26 G1 AC1
R42 1K/F_6
R41 2K/F_6
0.5" max
5 MIL
TEST1 TEST2
C5 F23
A0 : STUFF
A1 : NC
R110 R50
1K_4
R43 0_8
CPU_VCCA
at least 40 MIL shape
AC26 N1 B1 F26
VCCA3 VCCA2 VCCA1 VCCA0
POWER, GROUND, RESERVED SIGNALS
D6 D8 D18 D20 D22 E5 E7 E9 E17 E19 E21 F6 F8 F18 F20 F22 G5 G21 H6 H22 J5 J21 K22 U5 V6 V22 W5 W21 Y6 Y22 AA5 AA7 AA9 AA11 AA13 AA15 AA17 AA19 AA21 AB6 AB8 AB10 AB12 AB14 AB16 AB18 AB20 AB22 AC9 AC11 AC13 AC15 AC17 AC19 AD8 AD10 AD12 AD14 AD16 AD18 AE9 AE11 AE13 AE15 AE17 AE19 AF8 AF10 AF12 AF14 AF16 AF18
VCC00 VCC01 VCC02 VCC03 VCC04 VCC05 VCC06 VCC07 VCC08 VCC09 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71
VSS A2 A5 A8 A11 A14 A17 A20 A23 A26 B3 B6 B9 B12 B16 B19 B22 B25 C1 C4 C7 C10 C13 C15 C18 C21 C24 D2 D5 D7 D9 D11 D13 D15 D17 D19 D21 D23 D26 E3 E6 E8 E10 E12 E14 E16 E18 E20 E22 E25 F1 F4 F5 F7 F9 F11 F13 F15 F17 F19 F21 F24 G2 G6 G22 G23 G26 H3 H5 H21 H25 J1 J4 J6 J22 J24 K2 K5 K21 K23 K26 L3 L6 L22 L25 M1 M4 M5 M21 M24 N3 N6 N22 N23 N26 P2 P5 P21 P24 R1 R4
Banias_Processor_RVS
U12C
Banias
3 OF 3
POWER, GROUND AND NC
D10 D12 D14 D16 E11 E13 E15 F10 F12 F14 F16 K6 L5 L21 M6 M22 N5 N21 P6 P22 R5 R21 T6 T22 U21 P23 W4
VCCP0 VCCP1 VCCP2 VCCP3 VCCP4 VCCP5 VCCP6 VCCP7 VCCP8 VCCP9 VCCP10 VCCP11 VCCP12 VCCP13 VCCP14 VCCP15 VCCP16 VCCP17 VCCP18 VCCP19 VCCP20 VCCP21 VCCP22 VCCP23 VCCP24 VCCP25 VCCP26
VSS W23 W26 Y2 Y5 Y21 Y24 AA1 AA4 AA6 AA8 AA10 AA12 AA14 AA16 AA18 AA20 AA22 AA25 AB3 AB5 AB7 AB9 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB26 AC2 AC5 AC8 AC10 AC12 AC14 AC16 AC18 AC21 AC24 AD1 AD4 AD7 AD9 AD11 AD13 AD15 AD17 AD19 AD22 AD25 AE3 AE6 AE8 AE10 AE12 AE14 AE16 AE18 AE20 AE23 AE26 AF2 AF5 AF9 AE11 AE13 AE15 AE17 AF19 AF21 AF24
(25) CPU_VID0 (25) CPU_VID1 (25) CPU_VID2 (25) CPU_VID3 (25) CPU_VID4 (25) CPU_VID5
F2 F2 F3 G3 G4 H4
VID0 VID1 VID2 VID3 VID4 VID5
VID
T47 T48
Z0501 Z0502
AE7 AF6
VCCSENSE VSSSENSE
T56 T46 T57 T55
Z0503 Z0504 Z0506
(4) HBSEL1 (4) HBSEL0
B2 AF7 C14 C3 C16 E1
NC0 NC1 NC2 NC3 TEST3 PSI
R6 R22 R25 T3 T5 T21 T23 T26 U2 U6 U22 U24 V1 V4 V5 V21 V25 W3 W6 W22
Banias_Processor_RVS
PROJECT : BL1
Quanta Computer Inc.
Size
Document Number
CPU (POWER)-2
Rev
1A
Date: Monday, April 03, 2006
Sheet 3 of 30



SMBus SLAVE ADDRESS: D2

HBSEL1	HBSEL0	
0	0	133 MHz
0	1	100 MHz

CK410 FREQUENCY SELECT TABLE(MHZ)

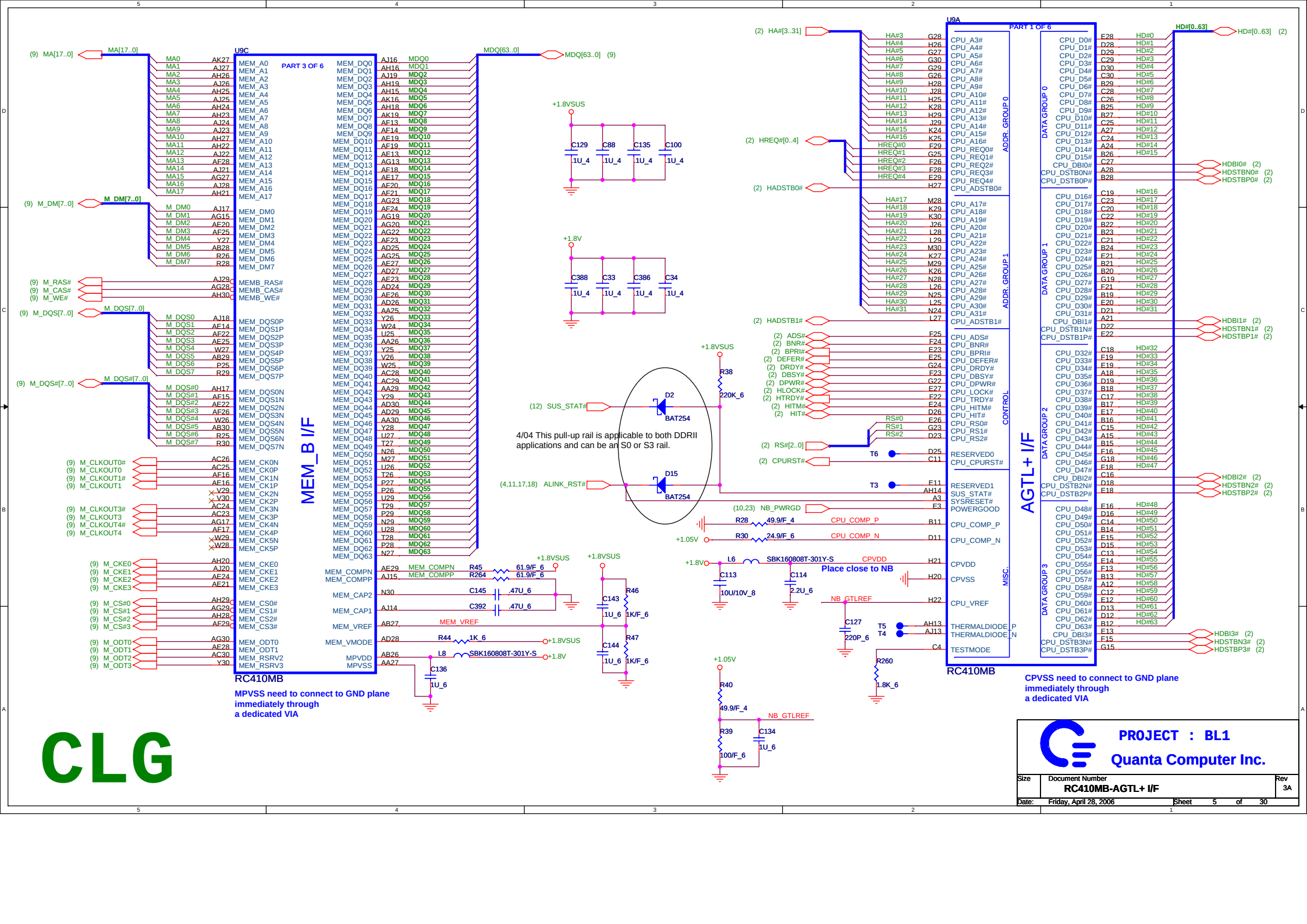
FSC BSEL0	FSB BSEL1	FSA	CPU MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Rsvd

CLK

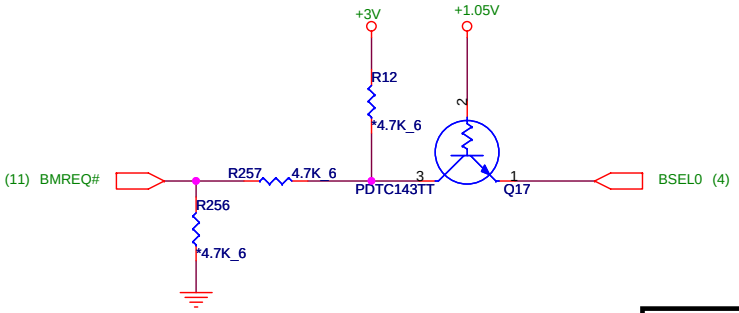
PROJECT : BL1

Quanta Computer Inc.

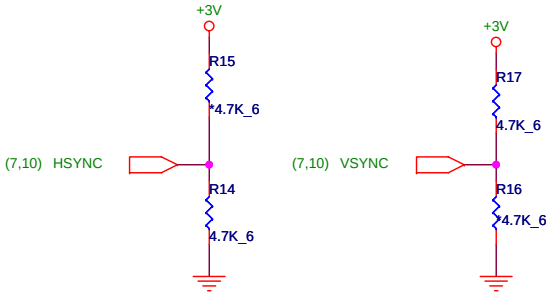
Size	Document Number	Rev
	EXTERNAL CLKGEN	1A
Date: Monday, May 08, 2006	Sheet 4 of 30	


U9C
PART 3 OF 6
MEM_B I/F
RC410MB
MPVSS need to connect to GND plane immediately through a dedicated VIA
4/04 This pull-up rail is applicable to both DDRII applications and can be an S0 or S3 rail.
U9A
PART 1 OF 6
AGTL+ I/F
ADDR. GROUP 0
ADDR. GROUP 1
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
CONTROL
MISC.
RC410MB
Place close to NB
CPVSS need to connect to GND plane immediately through a dedicated VIA
CLG
PROJECT : BL1
Quanta Computer Inc.
RC410MB-AGTL+ I/F
Friday, April 28, 2006
Sheet 5 of 30

NB strapping



BSEL1	BSEL0	
0	0	133 MHz
0	1	100 MHz

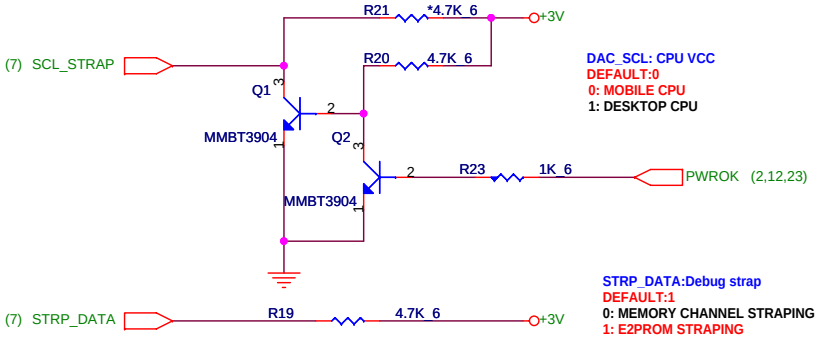


BMREQ#&HSYNC&VSYNC: FSB CLK SPEED

DEFAULT: 101

101: 100 MHZ RC420MB

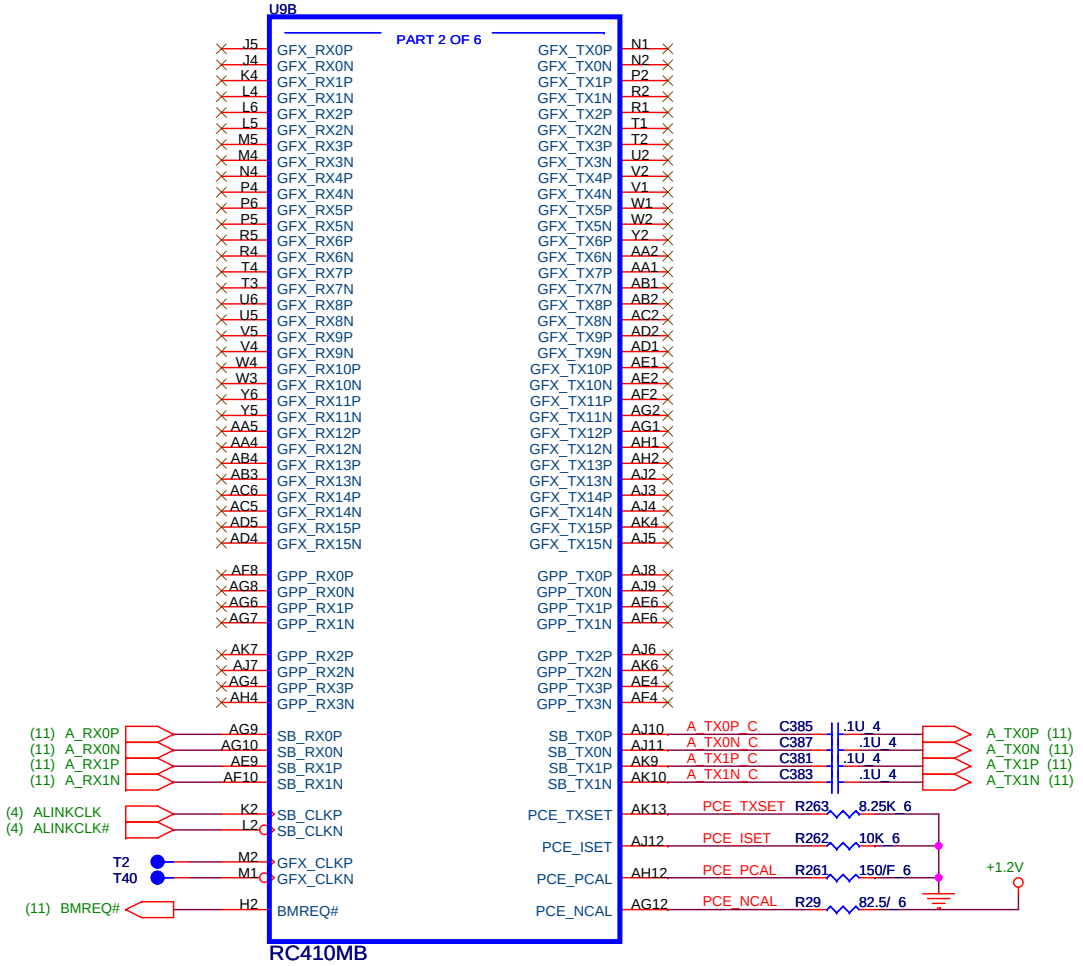
001: 133 MHZ RC420MD



DAC_SCL: CPU VCC
DEFAULT:0
0: MOBILE CPU
1: DESKTOP CPU

STRP_DATA:Debug strap
DEFAULT:1
0: MEMORY CHANNEL STRAPING
1: E2PROM STRAPING

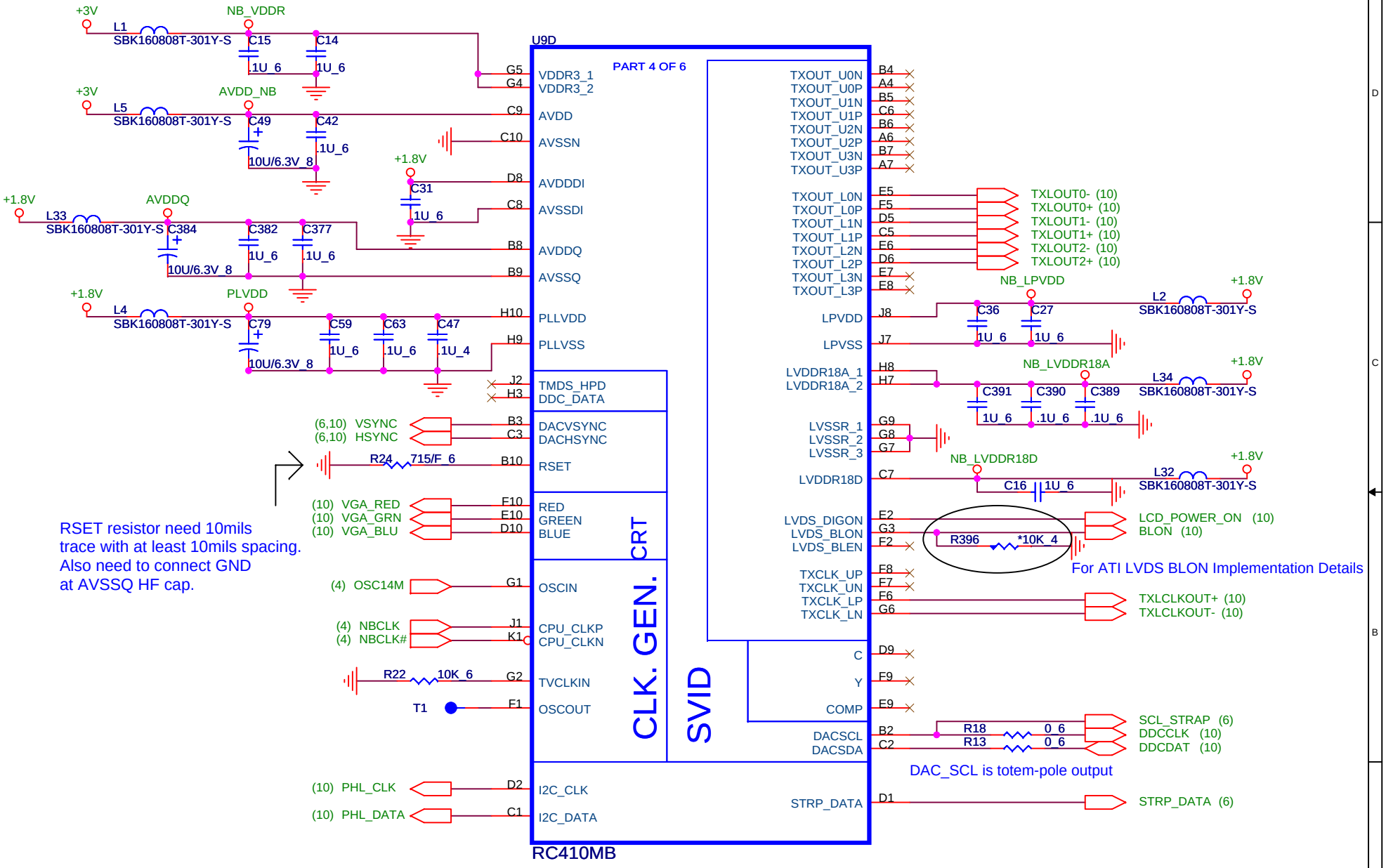
CLG



PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-PCIE LINK I/F	1A
Date: Friday, April 28, 2006	Sheet 6 of 30	

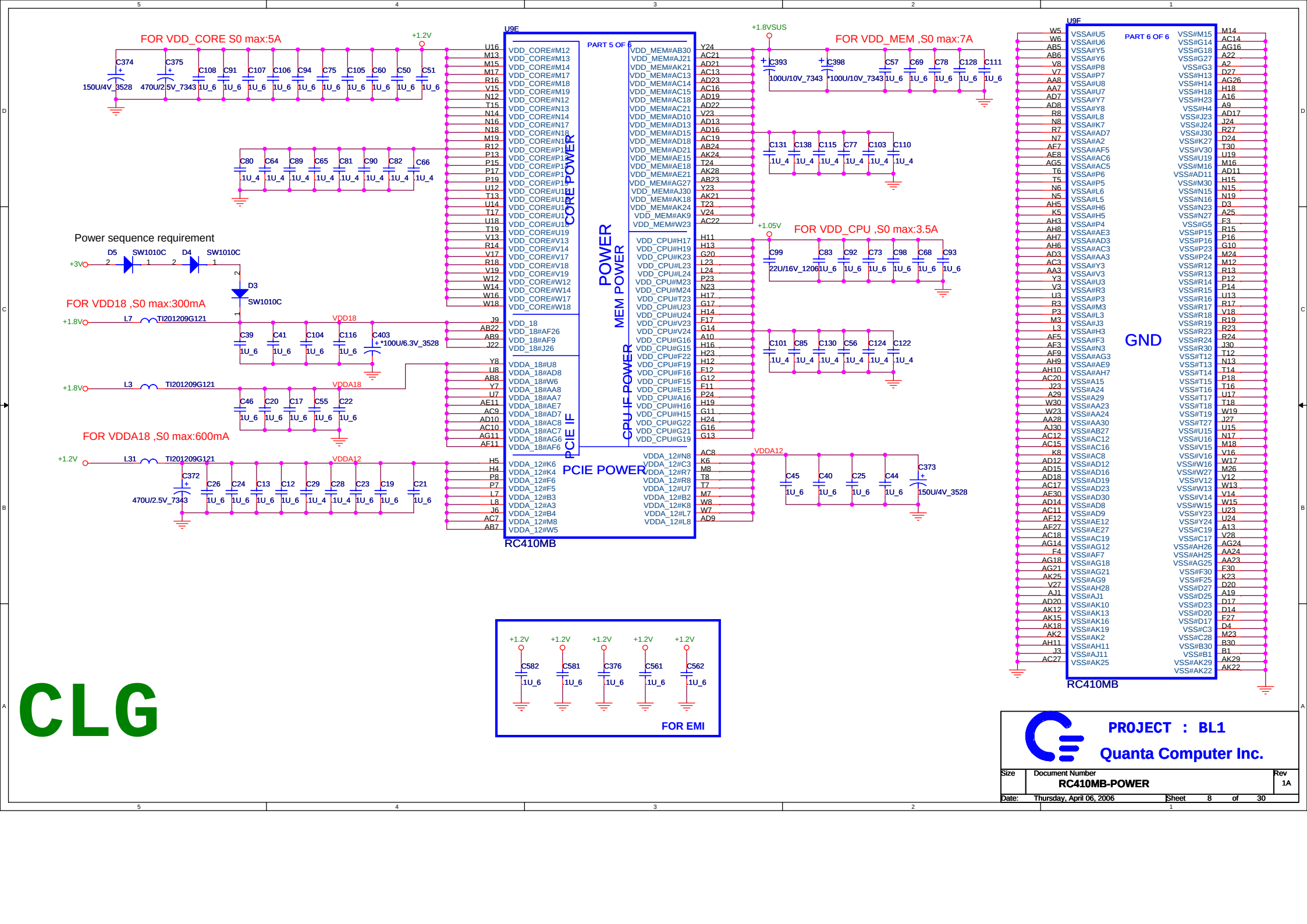


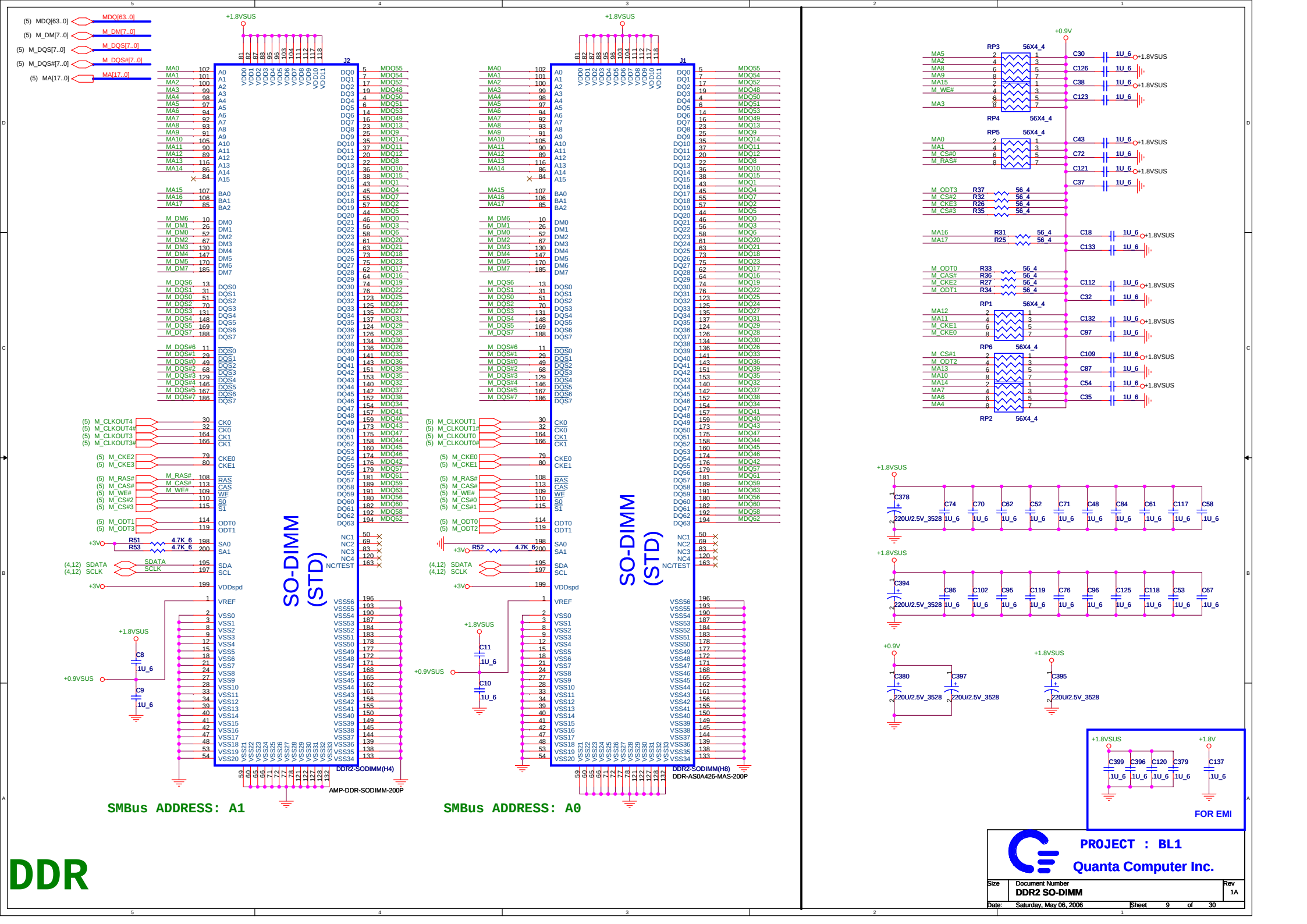
CLG

PROJECT : BL1

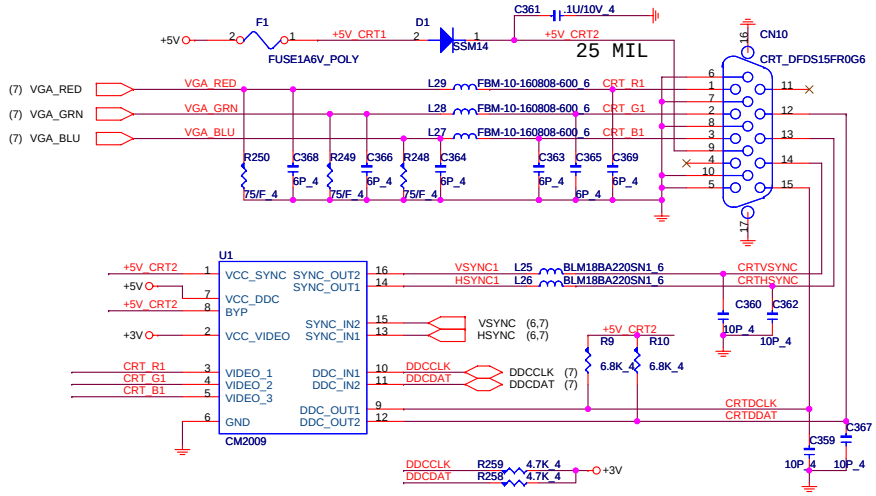
Quanta Computer Inc.

Size	Document Number	Rev
	RC410MB-VIDEO & CLKGEN	2A
Date: Friday, May 05, 2006	Sheet 7 of 30	

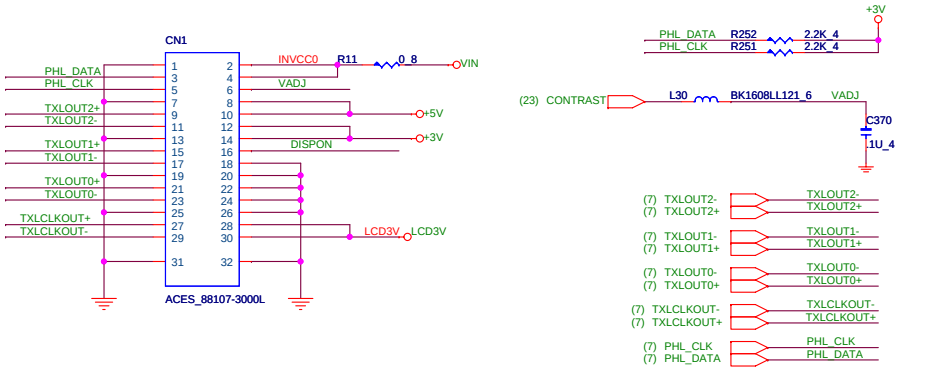

FOR VDD_CORE S0 max:5A
+1.2V
C374 150U/4V_3528
C375 470U/2.5V_7343
C108 C91 C107 C106 C94 C75 C105 C60 C50 C51 1U_6
C80 C64 C89 C65 C81 C90 C82 C66 1U_4
U9E
PART 5 OF 6
CORE POWER
VDD_CORE#M12 VDD_CORE#M13 VDD_CORE#M14 VDD_CORE#M17 VDD_CORE#M18 VDD_CORE#M19 VDD_CORE#N12 VDD_CORE#N13 VDD_CORE#N14 VDD_CORE#N17 VDD_CORE#N18 VDD_CORE#P11 VDD_CORE#P12 VDD_CORE#P13 VDD_CORE#P14 VDD_CORE#U11 VDD_CORE#U12 VDD_CORE#U13 VDD_CORE#U14 VDD_CORE#U17 VDD_CORE#U18 VDD_CORE#U19 VDD_CORE#V13 VDD_CORE#V14 VDD_CORE#V17 VDD_CORE#V18 VDD_CORE#V19 VDD_CORE#W12 VDD_CORE#W14 VDD_CORE#W17 VDD_CORE#W18
U16 M13 M15 M17 R16 V15 N12 T15 N14 N16 N18 M19 R12 P13 P15 P17 P19 U12 T13 U14 T17 U18 T19 V13 R14 V17 R18 V19 W12 W14 W16 W18
POWER
MEM POWER
VDD_MEM#AB30 VDD_MEM#AJ21 VDD_MEM#AK21 VDD_MEM#AC13 VDD_MEM#AC14 VDD_MEM#AC15 VDD_MEM#AC18 VDD_MEM#AC21 VDD_MEM#AD10 VDD_MEM#AD13 VDD_MEM#AD15 VDD_MEM#AD18 VDD_MEM#AD21 VDD_MEM#AE15 VDD_MEM#AE18 VDD_MEM#AE21 VDD_MEM#AG27 VDD_MEM#AJ30 VDD_MEM#AK18 VDD_MEM#AK24 VDD_MEM#AK9 VDD_MEM#W23
Y24 AC21 AD21 AC13 AD23 AC16 AD19 AD22 V23 AD13 AD16 AC19 AB24 AK24 T24 AK28 AB23 Y23 AK21 T23 V24 AC22
+1.8VSUS
FOR VDD_MEM ,S0 max:7A
C393 100U/10V_7343
C398 *100U/10V_7343
C57 C69 C78 C128 C111 1U_6
C131 C138 C115 C77 C103 C110 1U_4
+1.05V
FOR VDD_CPU ,S0 max:3.5A
C99 22U/16V_1206
C83 C92 C73 C98 C68 C93 1U_6
CPU IF POWER
VDD_CPU#H17 VDD_CPU#H19 VDD_CPU#K23 VDD_CPU#L23 VDD_CPU#L24 VDD_CPU#M23 VDD_CPU#M24 VDD_CPU#T23 VDD_CPU#U23 VDD_CPU#U24 VDD_CPU#V23 VDD_CPU#V24 VDD_CPU#G16 VDD_CPU#G15 VDD_CPU#F22 VDD_CPU#F19 VDD_CPU#F16 VDD_CPU#F15 VDD_CPU#E15 VDD_CPU#A16 VDD_CPU#H16 VDD_CPU#H15 VDD_CPU#G22 VDD_CPU#G21 VDD_CPU#G19
H11 H13 G20 L23 L24 P23 N23 H17 G17 H14 F17 G14 A10 H16 H23 H12 F12 G12 F11 P24 H19 G11 H24 G16 G13
C101 C85 C130 C56 C124 C122 1U_4
Power sequence requirement
+3V
D5 SW1010C D4 SW1010C
D3 SW1010C
FOR VDD18 ,S0 max:300mA
+1.8V
L7 TI201209G121
VDD18
C39 C41 C104 C116 C403 1U_6
*100U/6.3V_3528
VDD_18 VDD_18#AF26 VDD_18#AF9 VDD_18#J26
J9 AB22 AB9 J22
FOR VDDA18 ,S0 max:600mA
L3 TI201209G121
VDDA18
C46 C20 C17 C55 C22 1U_6
VDDA_18#U8 VDDA_18#AD8 VDDA_18#W6 VDDA_18#AA8 VDDA_18#AA7 VDDA_18#AE7 VDDA_18#AD7 VDDA_18#AC8 VDDA_18#AC7 VDDA_18#AG6 VDDA_18#AF6
Y8 U8 AB8 Y7 U7 AE11 AC9 AD10 AC10 AG11 AF11
+1.2V
L31 TI201209G121
VDDA12
C372 470U/2.5V_7343
C26 C24 C13 C12 C29 C28 C23 C19 C21 1U_6
VDDA_12#K6 VDDA_12#K4 VDDA_12#F6 VDDA_12#F5 VDDA_12#B3 VDDA_12#A3 VDDA_12#B4 VDDA_12#M8 VDDA_12#W5
H5 H4 P8 P7 L7 L8 J6 AC7 AB7
PCIE IF
PCIE POWER
VDDA_12#N8 VDDA_12#C3 VDDA_12#R7 VDDA_12#R8 VDDA_12#U7 VDDA_12#B2 VDDA_12#K8 VDDA_12#L7 VDDA_12#L8
AC8 K6 M8 T8 T7 M7 W8 W7 AD9
VDDA12
C45 C40 C25 C44 C373 1U_6
150U/4V_3528
+1.2V
C582 C581 C376 C561 C562 1U_6
FOR EMI
U9F
PART 6 OF 6
GND
VSSA#U5 VSSA#U6 VSSA#Y5 VSSA#Y6 VSSA#P8 VSSA#P7 VSSA#U8 VSSA#U7 VSSA#Y7 VSSA#Y8 VSSA#L8 VSSA#K7 VSSA#AD7 VSSA#A2 VSSA#AF5 VSSA#AC6 VSSA#AC5 VSSA#P6 VSSA#P5 VSSA#L6 VSSA#L5 VSSA#H6 VSSA#H5 VSSA#P4 VSSA#AE3 VSSA#AD3 VSSA#AC3 VSSA#AA3 VSSA#Y3 VSSA#V3 VSSA#U3 VSSA#R3 VSSA#P3 VSSA#M3 VSSA#L3 VSSA#J3 VSSA#H3 VSSA#F3 VSSA#N3 VSSA#AG3 VSSA#AE9 VSSA#AH7 VSS#A15 VSS#A24 VSS#A29 VSS#AA23 VSS#AA24 VSS#AA30 VSS#AB27 VSS#AC12 VSS#AC16 VSS#AC8 VSS#AD12 VSS#AD16 VSS#AD19 VSS#AD23 VSS#AD30 VSS#AD8 VSS#AD9 VSS#AE12 VSS#AE27 VSS#AC19 VSS#AG12 VSS#AF7 VSS#AG18 VSS#AG21 VSS#AG9 VSS#AH28 VSS#AJ1 VSS#AK10 VSS#AK13 VSS#AK16 VSS#AK19 VSS#AK2 VSS#AH11 VSS#AJ11 VSS#AK25
W5 W6 AB5 AB6 V8 V7 AA8 AA7 AD7 AD8 R8 N8 R7 N7 AF7 AE8 AG5 T6 T5 N6 N5 AH5 K5 AH3 AH8 AH7 AH6 AD3 AC3 AA3 Y3 V3 U3 R3 P3 M3 L3 AF5 AF3 AF9 AH9 AH10 AC20 J23 A29 W30 W23 AA28 AJ30 AC12 AC15 K8 AD12 AD15 AD18 AC17 AE30 AD14 AC11 AF12 AF27 AC18 AG14 F4 AG18 AG21 AK25 V27 AJ1 AD20 AK12 AK15 AK18 AK2 AH11 J3 AC27
VSS#M15 VSS#G14 VSS#G18 VSS#G27 VSS#G3 VSS#H13 VSS#H14 VSS#H18 VSS#H23 VSS#H4 VSS#J23 VSS#J24 VSS#J30 VSS#K27 VSS#V30 VSS#U19 VSS#M16 VSS#AD11 VSS#M30 VSS#N15 VSS#N16 VSS#N23 VSS#N27 VSS#G5 VSS#P15 VSS#P16 VSS#P23 VSS#P24 VSS#R12 VSS#R13 VSS#R14 VSS#R15 VSS#R16 VSS#R17 VSS#R18 VSS#R19 VSS#R23 VSS#R24 VSS#R30 VSS#T12 VSS#T13 VSS#T14 VSS#T15 VSS#T16 VSS#T17 VSS#T18 VSS#T19 VSS#T27 VSS#U15 VSS#U16 VSS#V15 VSS#V16 VSS#W16 VSS#W27 VSS#V12 VSS#W13 VSS#V14 VSS#W15 VSS#U23 VSS#U24 VSS#Y23 VSS#Y24 VSS#C19 VSS#C17 VSS#AH26 VSS#AH25 VSS#AG25 VSS#F30 VSS#F25 VSS#D27 VSS#D25 VSS#D23 VSS#D20 VSS#D17 VSS#C3 VSS#C28 VSS#B30 VSS#B1 VSS#AK29 VSS#AK22
M14 AC14 AG16 A22 A2 D27 AG26 H18 A16 A9 AD17 J24 R27 D24 T30 U19 M16 AD11 H15 N15 N19 D3 A25 E3 R15 P16 G10 M24 M12 R13 P12 P14 U13 R17 V18 R19 R23 R24 J30 T12 N13 T14 P18 T16 U17 T18 W19 J27 U15 N17 M18 V16 W17 M26 V12 W13 V14 W15 U23 U24 A13 V28 AG24 AA24 AA23 E30 K23 D20 A19 D17 D14 F27 D4 M23 B30 B1 AK29 AK22
RC410MB
RC410MB
CLG
PROJECT : BL1
Quanta Computer Inc.
Size
Document Number
RC410MB-POWER
Rev
1A
Date: Thursday, April 06, 2006
Sheet 8 of 30

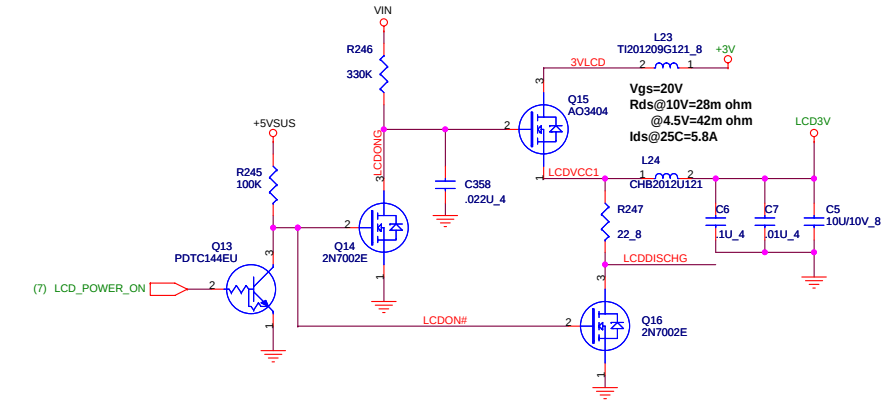

(5) MDQ[63..0]
(5) M_DM[7..0]
(5) M_DQS[7..0]
(5) M_DQS#[7..0]
(5) MA[17..0]
MDQ[63..0]
M_DM[7..0]
M_DQS[7..0]
M_DQS#[7..0]
MA[17..0]
+1.8VSUS
J2
SO-DIMM (STD)
DDR2-SODIMM(H4)
AMP-DDR-SODIMM-200P
SMBus ADDRESS: A1
J1
SO-DIMM (STD)
DDR2-SODIMM(H8)
DDR-AS0A426-MAS-200P
SMBus ADDRESS: A0
+0.9V
RP3 56X4_4
RP4 56X4_4
RP5 56X4_4
RP1 56X4_4
RP6 56X4_4
RP2 56X4_4
+3V
+0.9VSUS
+1.8V
FOR EMI
DDR
PROJECT : BL1
Quanta Computer Inc.
Size
Document Number
DDR2 SO-DIMM
Rev
1A
Date: Saturday, May 06, 2006
Sheet 9 of 30

CRT PORT



LCD Connector



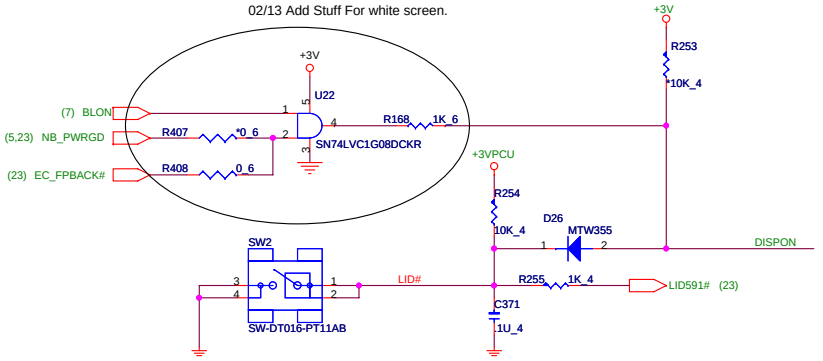


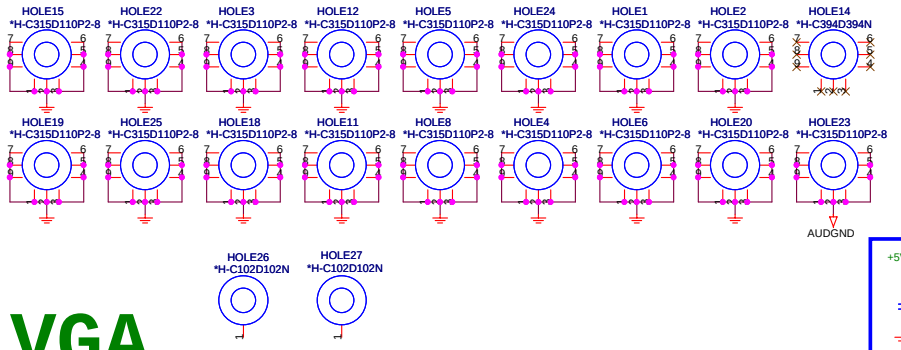
Lid Switch

05/05 Add Resistor 1Kohm on Buffer output.

04/28 The Solve Boot up white line on LG LCD issue.

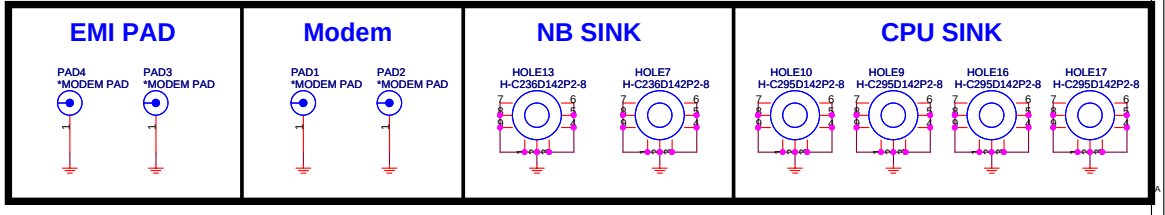
02/13 Add Stuff For white screen.

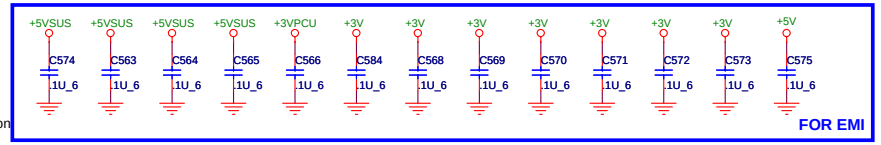




VGA

3/31 Add EMI Solution



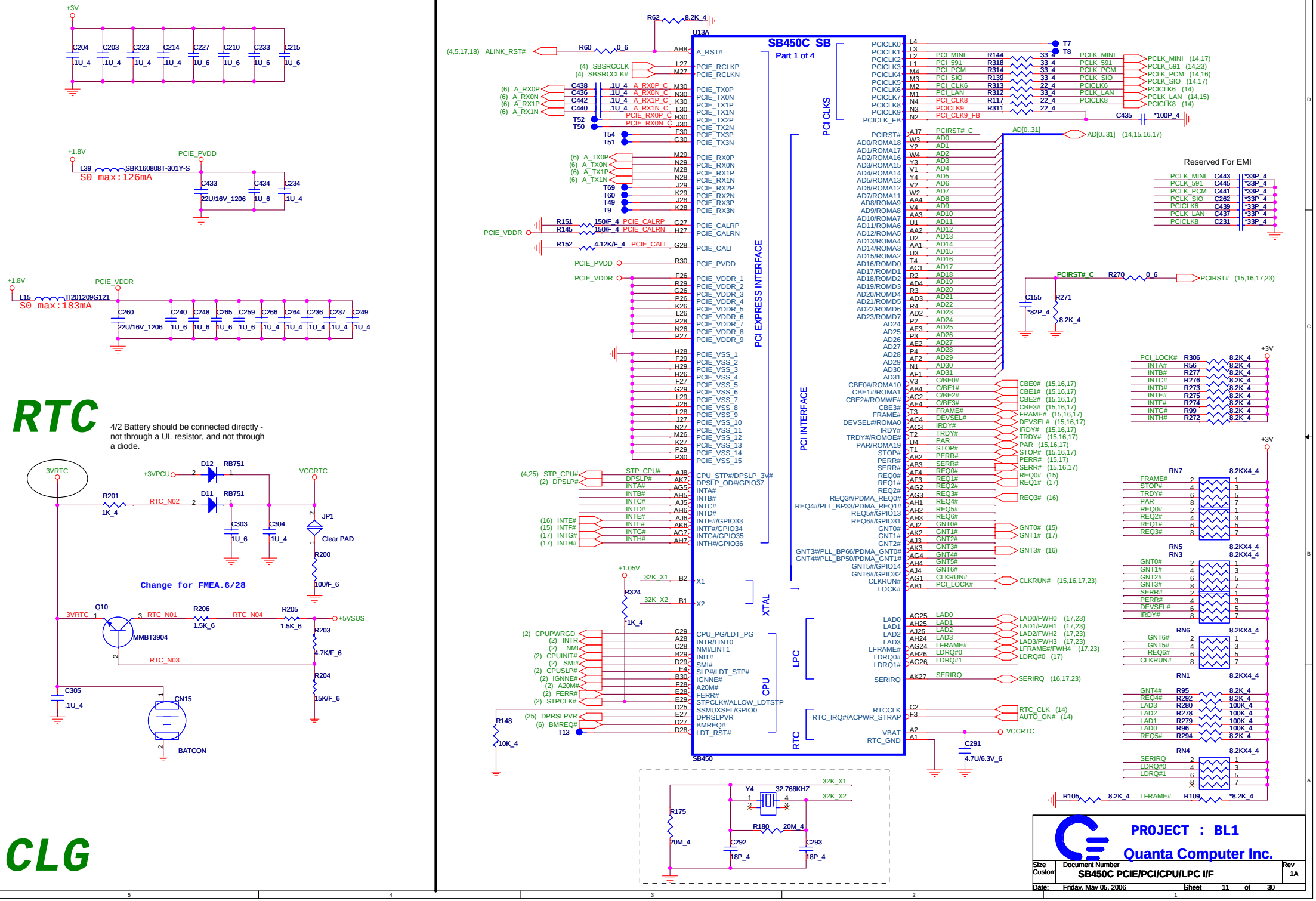


PROJECT : BL1

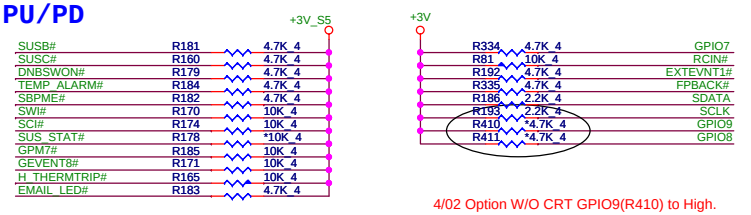
Quanta Computer Inc.

Size	Document Number	Rev
	VGA Ports, LID, & HOLES	3B

Date: Wednesday, May 10, 2006 Sheet 10 of 30

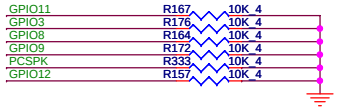

+3V
C204 C203 C223 C214 C227 C210 C233 C215
.1U_4 .1U_4 .1U_4 .1U_4 1U_6 1U_6 1U_6 1U_6
+1.8V
PCIE_PVDD
L39 SBK160808T-301Y-S
S0 max:126mA
C433 C434 C234
22U/16V_1206 1U_6 .1U_4
+1.8V
PCIE_VDDR
L15 TI201209G121
S0 max:183mA
C260 C240 C248 C265 C259 C266 C264 C236 C237 C249
22U/16V_1206 1U_6 1U_6 1U_6 1U_6 1U_4 1U_4 1U_4 1U_4 1U_4 1U_4
RTC
4/2 Battery should be connected directly - not through a UL resistor, and not through a diode.
3VRTC
D12 RB751
D11 RB751
+3VPCU
VCCRTC
R201 1K_4
RTC_N02
C303 1U_6
C304 1U_4
JP1
Clear PAD
R200 100/F_6
Change for FMEA.6/28
Q10 MMBT3904
3VRTC
RTC_N01
R206 1.5K_6
RTC_N04
R205 1.5K_6
+5VSUS
R203 4.7K/F_6
RTC_N03
R204 15K/F_6
C305 .1U_4
CN15
BATCON
R62 8.2K_4
U13A
SB450C SB
Part 1 of 4
(4,5,17,18) ALINK_RST#
R60 0_6
A_RST#
(4) SBSRCCLK
(4) SBSRCCLK#
PCIE_RCLKP
PCIE_RCLKN
(6) A_RX0P
(6) A_RX0N
(6) A_RX1P
(6) A_RX1N
C438 C436 C442 C440
.1U_4 A_RX0P_C
.1U_4 A_RX0N_C
.1U_4 A_RX1P_C
.1U_4 A_RX1N_C
PCIE_RX0P_C
PCIE_RX0N_C
T52 T50 T54 T51
PCIE_TX0P PCIE_TX0N PCIE_TX1P PCIE_TX1N PCIE_TX2P PCIE_TX2N PCIE_TX3P PCIE_TX3N
(6) A_TX0P
(6) A_TX0N
(6) A_TX1P
(6) A_TX1N
T69 T60 T49 T9
PCIE_RX0P PCIE_RX0N PCIE_RX1P PCIE_RX1N PCIE_RX2P PCIE_RX2N PCIE_RX3P PCIE_RX3N
R151 150/F_4 PCIE_CALRP
R145 150/F_4 PCIE_CALRN
PCIE_VDDR
R152 4.12K/F_4 PCIE_CALI
PCIE_CALRP PCIE_CALRN PCIE_CALI
PCIE_PVDD
PCIE_VDDR_1 PCIE_VDDR_2 PCIE_VDDR_3 PCIE_VDDR_4 PCIE_VDDR_5 PCIE_VDDR_6 PCIE_VDDR_7 PCIE_VDDR_8 PCIE_VDDR_9
PCIE_VSS_1 PCIE_VSS_2 PCIE_VSS_3 PCIE_VSS_4 PCIE_VSS_5 PCIE_VSS_6 PCIE_VSS_7 PCIE_VSS_8 PCIE_VSS_9 PCIE_VSS_10 PCIE_VSS_11 PCIE_VSS_12 PCIE_VSS_13 PCIE_VSS_14 PCIE_VSS_15
PCI EXPRESS INTERFACE
(4,25) STP_CPU#
(2) DPSLP#
STP_CPU#
DPSLP#
INTA# INTB# INTC# INTD# INTE# INTF# INTG# INTH#
(16) INTE#
(15) INTF#
(17) INTG#
(17) INTH#
CPU_STP#/DPSLP_3V#
DPSLP_OD#/GPIO37
INTA# INTB# INTC# INTD# INTE#/GPIO33 INTF#/GPIO34 INTG#/GPIO35 INTH#/GPIO36
+1.05V
32K_X1
32K_X2
R324 1K_4
X1
X2
XTAL
(2) CPUPWRGD
(2) INTR
(2) NMI
(2) CPUINIT#
(2) SMI#
(2) CPUSLP#
(2) IGNNE#
(2) A20M#
(2) FERR#
(2) STPCLK#
CPU_PG/LDT_PG
INTR/LINT0
NMI/LINT1
INIT#
SMI#
SLP#/LDT_STP#
IGNNE#
A20M#
FERR#
STPCLK#/ALLOW_LDTSTP
SSMUXSEL/GPIO0
DPRSLPVR
BMREQ#
LDT_RST#
CPU
(25) DPRSLPVR
(6) BMREQ#
T13
R148 10K_4
SB450
PCI CLKS
PCICLK0 PCICLK1 PCICLK2 PCICLK3 PCICLK4 PCICLK5 PCICLK6 PCICLK7 PCICLK8 PCICLK9 PCICLK_FB
T7 T8
PCI_MINI R144 33_4 PCLK_MINI
PCI_591 R318 33_4 PCLK_591
PCI_PCM R314 33_4 PCLK_PCM
PCI_SIO R139 33_4 PCLK_SIO
PCI_CLK6 R313 22_4 PCICLK6
PCI_LAN R312 33_4 PCLK_LAN
PCI_CLK8 R117 22_4 PCICLK8
PCICLK9 R311 22_4
PCI_CLK9_FB
C435 *100P_4
PCLK_MINI (14,17)
PCLK_591 (14,23)
PCLK_PCM (14,16)
PCLK_SIO (14,17)
PCICLK6 (14)
PCLK_LAN (14,15)
PCICLK8 (14)
PCI INTERFACE
PCIRST# AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
AD0/ROMA18 AD1/ROMA17 AD2/ROMA16 AD3/ROMA15 AD4/ROMA14 AD5/ROMA13 AD6/ROMA12 AD7/ROMA11 AD8/ROMA9 AD9/ROMA8 AD10/ROMA7 AD11/ROMA6 AD12/ROMA5 AD13/ROMA4 AD14/ROMA3 AD15/ROMA2 AD16/ROMD0 AD17/ROMD1 AD18/ROMD2 AD19/ROMD3 AD20/ROMD4 AD21/ROMD5 AD22/ROMD6 AD23/ROMD7
AD[0..31]
AD[0..31] (14,15,16,17)
C/BE0# C/BE1# C/BE2# C/BE3#
CBE0#/ROMA10 CBE1#/ROMA1 CBE2#/ROMWE# CBE3#
FRAME# DEVSEL#/ROMA0 IRDY# TRDY#/ROMOE# PAR/ROMA19 STOP# PERR# SERR# REQ0# REQ1# REQ2# REQ3#/PDMA_REQ0# REQ4#/PLL_BP33/PDMA_REQ1# REQ5#/GPIO13 REQ6#/GPIO31 GNT0# GNT1# GNT2# GNT3#/PLL_BP66/PDMA_GNT0# GNT4#/PLL_BP50/PDMA_GNT1# GNT5#/GPIO14 GNT6#/GPIO32 CLKRUN# LOCK#
CBE0# (15,16,17)
CBE1# (15,16,17)
CBE2# (15,16,17)
CBE3# (15,16,17)
FRAME# (15,16,17)
DEVSEL# (15,16,17)
IRDY# (15,16,17)
TRDY# (15,16,17)
PAR (15,16,17)
STOP# (15,16,17)
PERR# (15,17)
SERR# (15,16,17)
REQ0# (15)
REQ1# (17)
REQ3# (16)
GNT0# (15)
GNT1# (17)
GNT3# (16)
CLKRUN# (15,16,17,23)
PCI_LOCK#
CLKRUN#
PCIRST# C
R270 0_6
PCIRST# (15,16,17,23)
C155 *82P_4
R271 8.2K_4
Reserved For EMI
PCLK_MINI C443 *33P_4
PCLK_591 C445 *33P_4
PCLK_PCM C441 *33P_4
PCLK_SIO C262 *33P_4
PCICLK6 C439 *33P_4
PCLK_LAN C437 *33P_4
PCICLK8 C231 *33P_4
+3V
PCI_LOCK# R306 8.2K_4
INTA# R56 8.2K_4
INTB# R277 8.2K_4
INTC# R276 8.2K_4
INTD# R273 8.2K_4
INTE# R275 8.2K_4
INTF# R274 8.2K_4
INTG# R99 8.2K_4
INTH# R272 8.2K_4
LPC
LAD0 LAD1 LAD2 LAD3 LFRAME# LDRQ0# LDRQ1#
LAD0/FWH0 (17,23)
LAD1/FWH1 (17,23)
LAD2/FWH2 (17,23)
LAD3/FWH3 (17,23)
LFRAME#/FWH4 (17,23)
LDRQ#0 (17)
LDRQ#1
SERIRQ
SERIRQ (16,17,23)
RTC
RTCCLK
RTC_IRQ#/ACPWR_STRAP
RTC_CLK (14)
AUTO_ON# (14)
VBAT
RTC_GND
VCCRTC
C291 4.7U/6.3V_6
RN7 8.2KX4_4
FRAME# STOP# TRDY# PAR REQ0# REQ2# REQ1# REQ3#
RN5 8.2KX4_4
RN3 8.2KX4_4
GNT0# GNT1# GNT2# GNT3# SERR# PERR# DEVSEL# IRDY#
RN6 8.2KX4_4
GNT6# GNT5# REQ6# CLKRUN#
RN1 8.2KX4_4
GNT4# 8.2K_4
REQ4# R292 8.2K_4
LAD3 R280 100K_4
LAD2 R278 100K_4
LAD1 R279 100K_4
LAD0 R96 100K_4
REQ5# R294 8.2K_4
RN4 8.2KX4_4
SERIRQ
LDRQ#0
LDRQ#1
R105 8.2K_4 LFRAME#
R109 *8.2K_4
Y4 32.768KHZ
32K_X1
32K_X2
R175 20M_4
R180 20M_4
C292 18P_4
C293 18P_4
PROJECT : BL1
Quanta Computer Inc.
Size Custom
Document Number SB450C PCIE/PCI/CPU/LPC I/F
Rev 1A
Date: Friday, May 05, 2006
Sheet 11 of 30
CLG

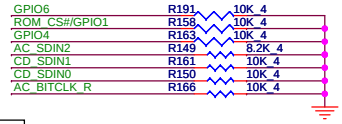
PU/PD



4/02 Option W/O CRT GPIO9(R410) to High.

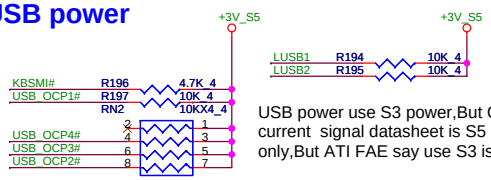
4/02 Option(Normal) CRT GPIO9(R172) to Low.



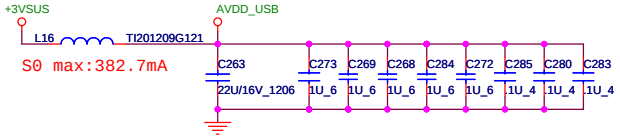


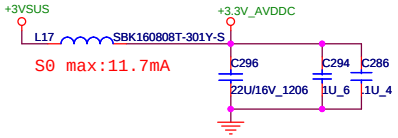
	GPIO9 PIN	GPIO8 PIN
CRT	LOW	
W/O CRT	HIGH	
Modem		LOW
W/O Modem		HIGH

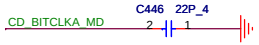
USB power



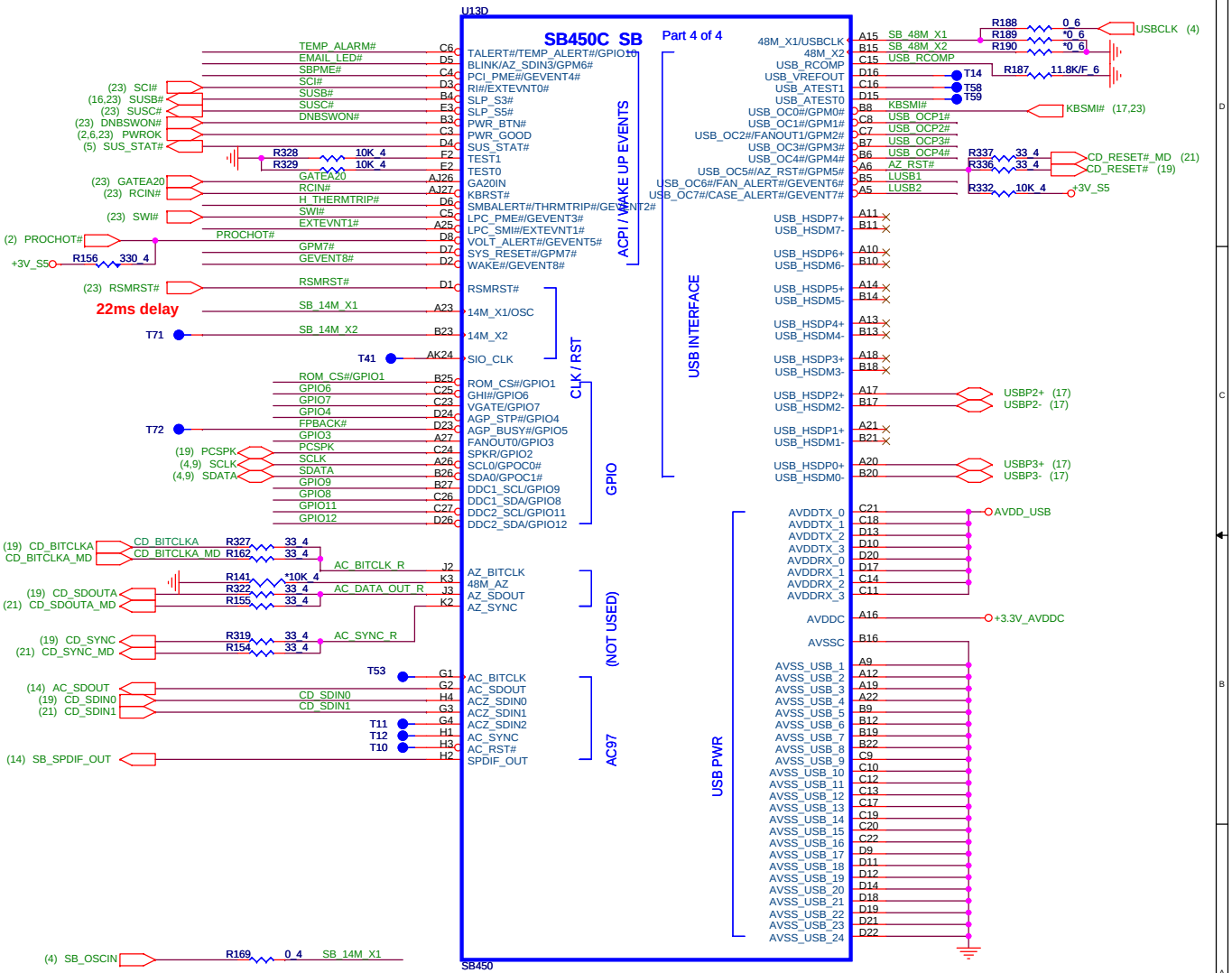
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok

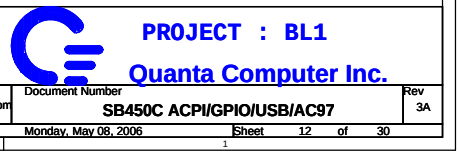


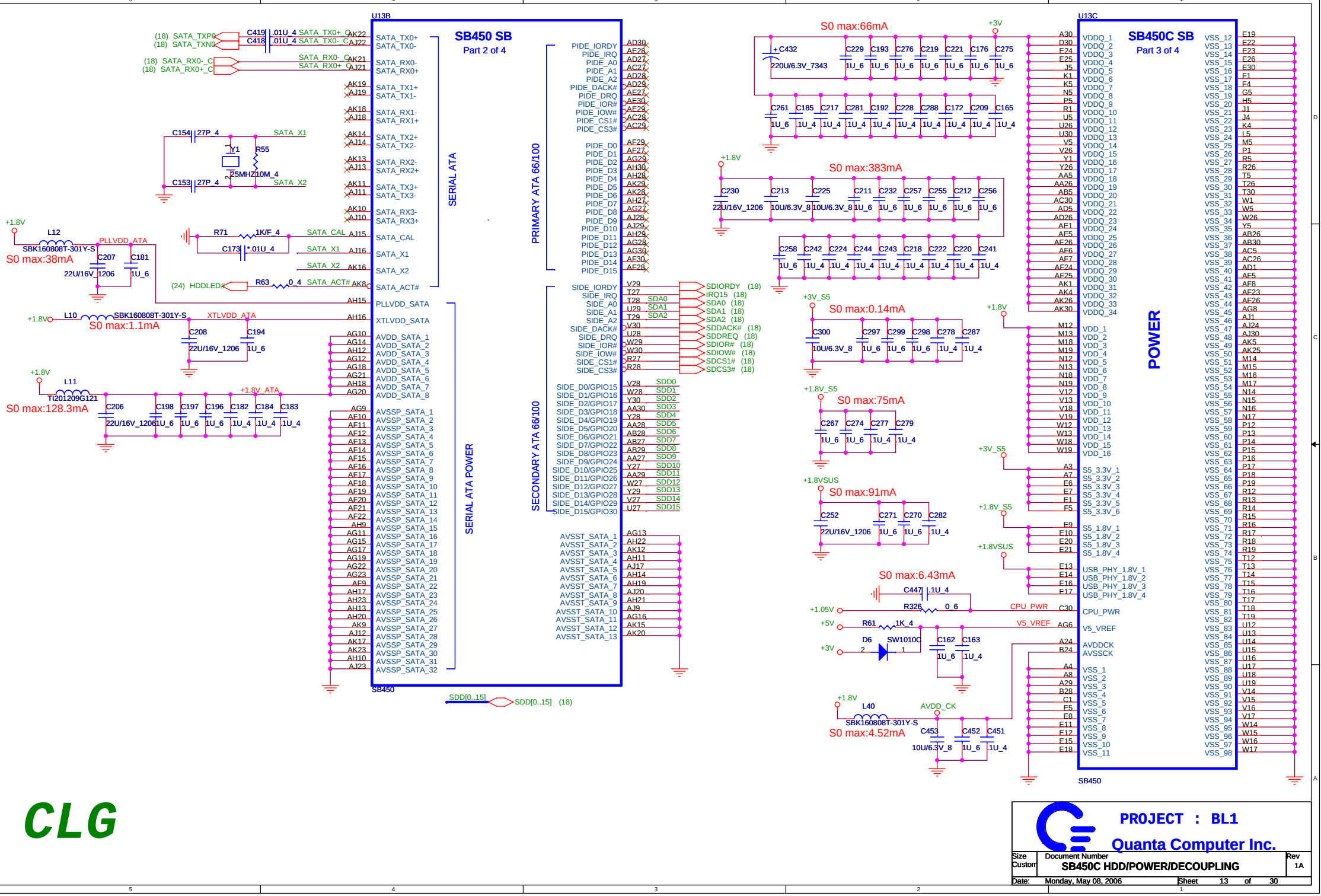


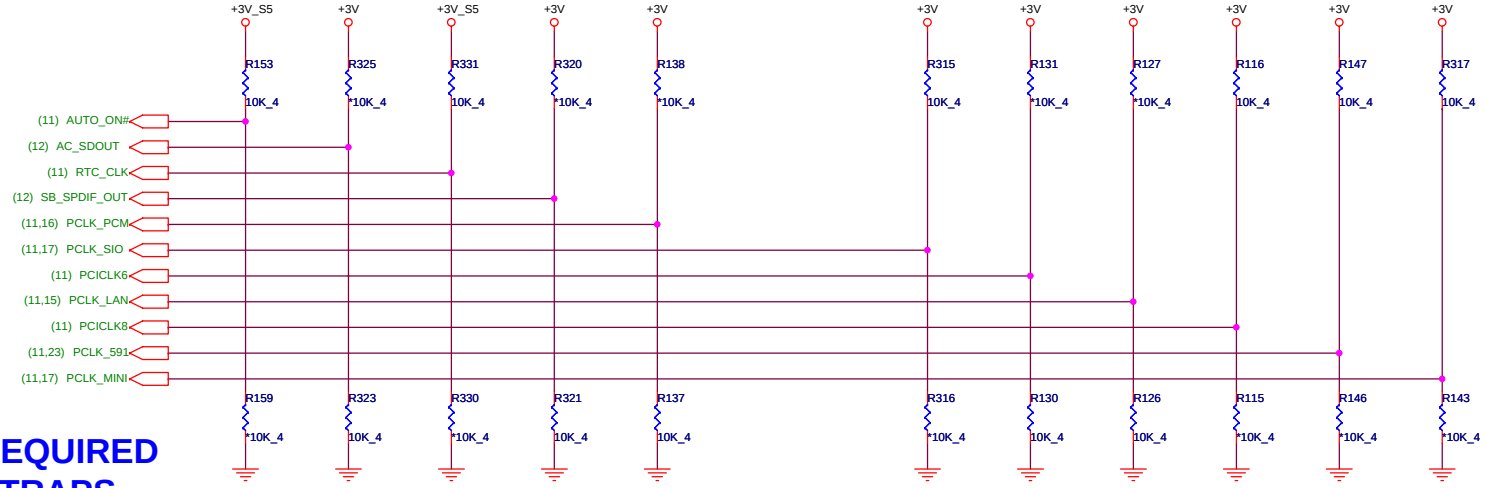


CLG





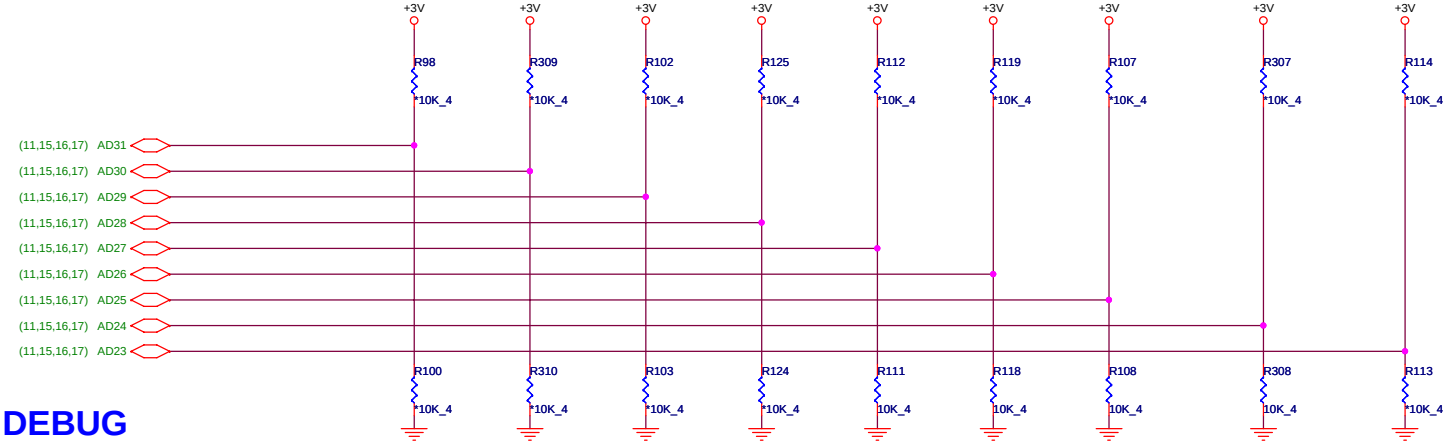

U13B
SB450 SB
Part 2 of 4
SERIAL ATA
PRIMARY ATA 66/100
SECONDARY ATA 66/100
SERIAL ATA POWER
SB450
U13C
SB450C SB
Part 3 of 4
POWER
SB450
S0 max:38mA
S0 max:1.1mA
S0 max:128.3mA
S0 max:66mA
S0 max:383mA
S0 max:0.14mA
S0 max:75mA
S0 max:91mA
S0 max:6.43mA
S0 max:4.52mA
CLG
PROJECT : BL1
Quanta Computer Inc.
SB450C HDD/POWER/DECOUPLING
Monday, May 08, 2006
Sheet 13 of 30



REQUIRED STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK4 PCLK_PCM	PCI_CLK5 PCLK_SIO	PCI_CLK6 PCI_CLK6	PCI_CLK7 PCLK_LAN	PCI_CLK8 PCI_CLK8	PCI_CLK3 PCLK_591	PCI_CLK2 PCLK_MINI*
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz use Internal PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8	H,H = PCI(X BUS) ROM H,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space)		USB PHY PWRDOWN DISABLE DEFAULT	48MHz Crystal Pad DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz use External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT	L,H = LPC ROM II DEFAULT (addresses mapped to below 1M) L,L = FWH ROM		USB PHY PWRDOWN ENABLE	48MHz OSC/Clock Buffer

*This strap is only required if the strap on PCICLK4 is configured for External Clock.



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

CLG

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB450C STRAPS	1A

Date: Monday, April 03, 2006 Sheet 14 of 30

ID Select : AD18
Interrupt Pin : INTF#
Request Indicate : REQ0#
Grant Indicate : GNT0#

LAN

RTL8110SBL/8100CL

U15

RTL8110SBL

VDD33---+3.3V DIGITAL
AVDDH------+3.3V ANALOG
AVDDL-----+2.5V ANALOG
DVDD-----+1.2V DIGITAL
DVDD_A----+1.2V ANALOG

RTL8100CL

VDD33---+3.3V DIGITAL
AVDDL-----+3.3V ANALOG
DVDD-----+2.5V DIGITAL
AVDDH-----+2.5V ANALOG

Near Lan chipset

Near transformer.

U18 93C46-3GR

U8 NS681687

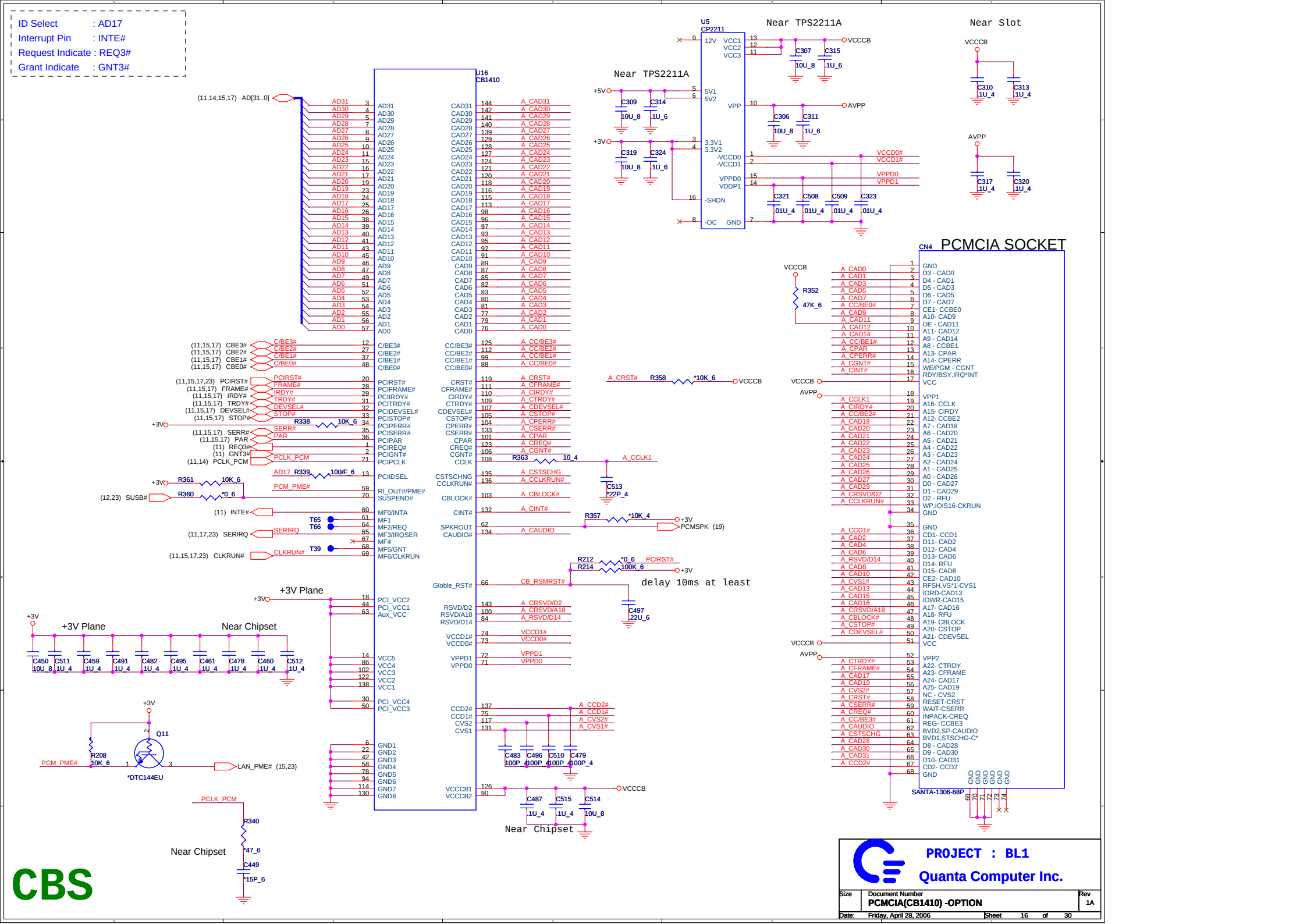
CN9 RJ45-C100F8-100B-8P-L

Size	Document Number	Rev
	LAN RTL8110SBL/8100CL	1A

PROJECT : BL1
Quanta Computer Inc.

Date: Saturday, May 06, 2006 Sheet 15 of 30

ID Select	: AD17
Interrupt Pin	: INTE#
Request Indicate	: REQ3#
Grant Indicate	: GNT3#



CBS

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	PCMCIA(CB1410) -OPTION	1A
Date: Friday, April 28, 2006	Sheet 16 of 30	

ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ1#
Grant Indicate : GNT1#

MINI-PCI

03/22 Add Diode to avoid EC keep RF_EN Low.

CN18
FOX_MINIPCI_H7.95

D32 MTW355
D21 MTW355

(23,24) WIRELESS_SW#
(23) RF_EN
(11) INTH#

(11,14) PCLK_MINI — PCLK_MINI
(11) REQ1#
(11,14,15,16) AD31
(11,14,15,16) AD29
(11,14,15,16) AD27
(11,14,15,16) AD25
(11,15,16) CBE3#
(11,14,15,16) AD23
(11,15,16) AD21
(11,15,16) AD19
(11,15,16) AD17
(11,15,16) CBE2#
(11,15,16) IRDY#
(11,15,16,23) CLKRUN#
(11,15,16) SERR#
(11,15) PERR#
(11,15,16) CBE1#
(11,15,16) AD14
(11,15,16) AD12
(11,15,16) AD10
(11,15,16) AD8
(11,15,16) AD7
(11,15,16) AD5
(11,15,16) AD3
(11,15,16) AD1

RP10 *0X4_4
(11,23) LAD0/FWH0 — RLAD0
(11,23) LAD1/FWH1 — RLAD1
(11,23) LAD2/FWH2 — RLAD2
(11,23) LAD3/FWH3 — RLAD3
(11,23) LFRAME#/FWH4 — R234 *0-4 RLFRAME#
(4,5,11,18) ALINK_RST# — R233 *0-4 RLRESET#

+3V
+5V
+3VSUS
GND

TIP LAN1 LAN3 LAN5 LAN7 LED_GP LED_GN NC1 -INTB +3V R(IRQ3) GND PCICLK GND -REQ +3V AD31 AD29 GND AD27 AD25 (V) -CBE3 AD23 GND AD21 AD19 GND AD17 -CBE2 -IRDY +3V -CLKRUN -SERR GND -PERR -CBE1 AD14 GND AD12 AD10 GND AD8 AD7 +3V AD5 (V) AD3 +5V AD1 GND SYNC SDIN0 BITCLK -AC_PRIMARY BEEP AGND +MIC -MIC AGND -RI +5VA

RING LAN2 LAN4 LAN6 LAN8 LED_YP LED_YN NC2 +5V -INTA R(IRQ4) +3VAUX -RST +3V -GNT GND -PME (V) AD30 +3V AD28 AD26 AD24 IDSEL GND AD22 AD20 PAR AD18 AD16 GND -FRAME -TRDY -STOP +3V -DEVSEL GND AD15 AD13 AD11 GND AD9 -CBE0 +3V AD6 AD4 AD2 AD0 (V) SERIRQ GND M66EN SDOUT SDIN1 -RESET -MPCICACK AGND +SPK -SPK AGND NC4 +3VAUX

+5V — INTG# (11)
+3VSUS — PCIRST# (11,15,16,23)
GNT1# (11)
PME#
AD30 (11,14,15,16)
AD28 (11,14,15,16)
AD26 (11,14,15,16)
AD24 (11,14,15,16)
R228 150_4 AD20
AD20
AD22 (11,15,16)
AD20 (11,15,16)
PAR (11,15,16)
AD18 (11,15,16)
AD16 (11,15,16)
FRAME# (11,15,16)
TRDY# (11,15,16)
STOP# (11,15,16)
DEVSEL# (11,15,16)
AD15 (11,15,16)
AD13 (11,15,16)
AD11 (11,15,16)
AD9 (11,15,16)
CBE0# (11,15,16)
AD6 (11,15,16)
AD4 (11,15,16)
AD2 (11,15,16)
AD0 (11,15,16)
SERIRQ (11,16,23)
RLDRQ# R226 *0-4 LDRQ#0 (11)
SDIN1_MINI
RKBSMI# R224 *0-4 KBSMI# (12,23)
RRPCLK_SIO R223 *0-4 PCLK_SIO (11,14)
+3VSUS

+3V: C334 .1U_4, C341 .1U_4, C343 .1U_4, C332 .1U_4
+5V: C333 .1U_4, C342 .1U_4

+3VSUS: C580 .1U_6, C583 .1U_6
FOR EMI

+3VSUS: R225 4.7K_4 — SDIN1_MINI; R227 4.7K_4 — PME#

PCLK_MINI R229 *22_4 C335 *10P_4
PCLK_SIO R222 *22_4 C331 *10P_4

MPC

USB

U2
G545B2RD1U
+5VSUS — IN1, IN2
USB_LEFT — EN#
GND, GND-C
OUT3, OUT2, OUT1
OC#
USBPWR0
R94 *6.34K/F_6

(23) USB_LEFT

CN13
USBPWR0
C191 100U/6.3V-3528
BUSBP2-
BUSBP2+
USB_DFHD04MR671

02/24 Add 0ohm jumper

R401 *0_4
L38
(12) USBP2-
(12) USBP2+
RFCM1632100M3
R402 *0_4
BUSBP2-
BUSBP2+

U14
G545B2RD1U
+5VSUS — IN1, IN2
EN#, GND, GND-C
OUT3, OUT2, OUT1
OC#
USBPWR1
R142 *6.34K/F_6

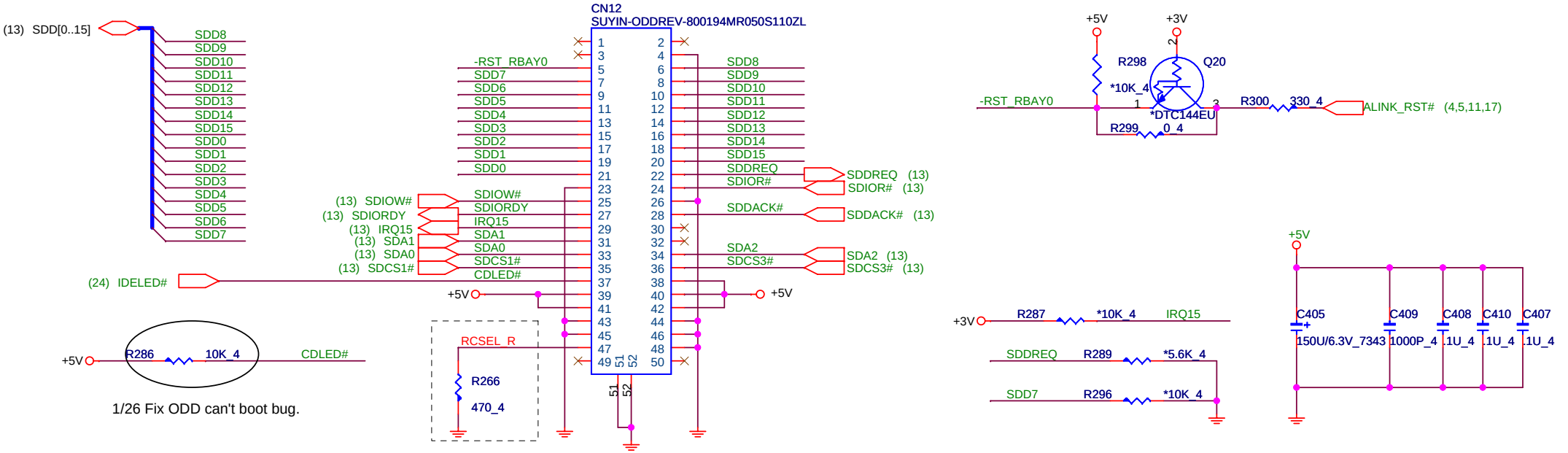
CN14
100U/6.3V-3528
C444
USBPWR1
R376 0_6 USB_P3-
R400 0_6 USB_P3+
(12) USBP3-
(12) USBP3+
4Pin connector

04/28 Del Reserved the Second USB Port.

PROJECT : BL1
Quanta Computer Inc.

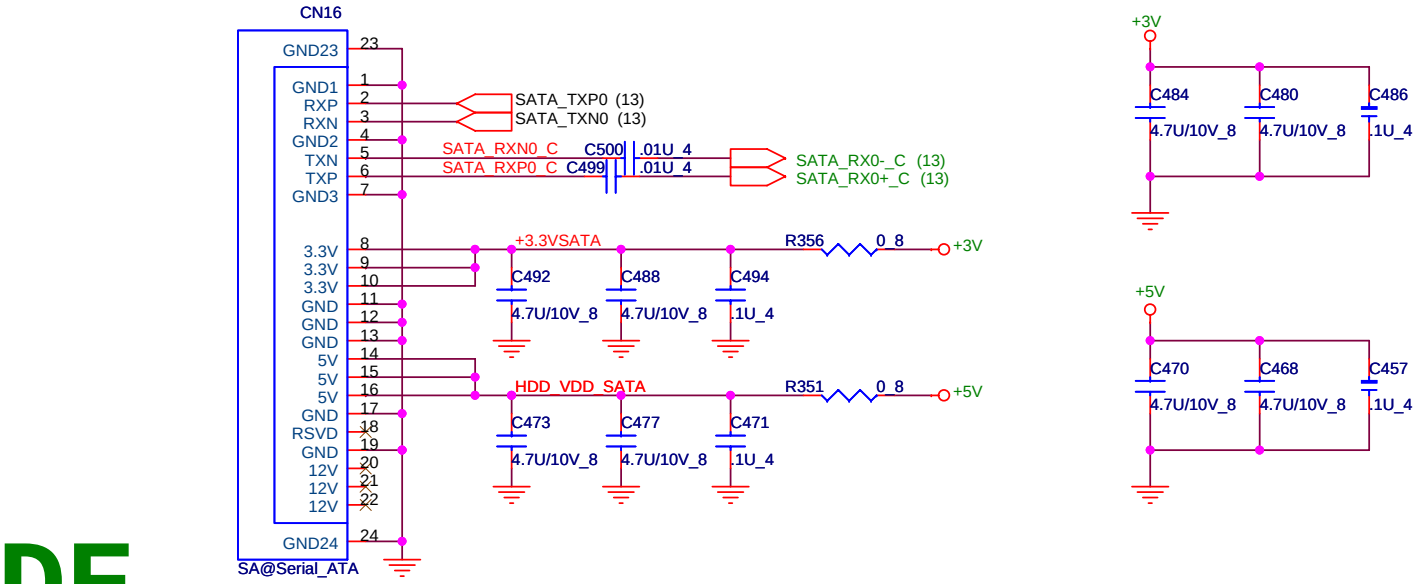
Size	Document Number	Rev
	MINI PCI,USB	3B
Date: Tuesday, May 09, 2006	Sheet 17 of 30	

ODD CONN



1/26 Fix ODD can't boot bug.

SATA HDD CONN

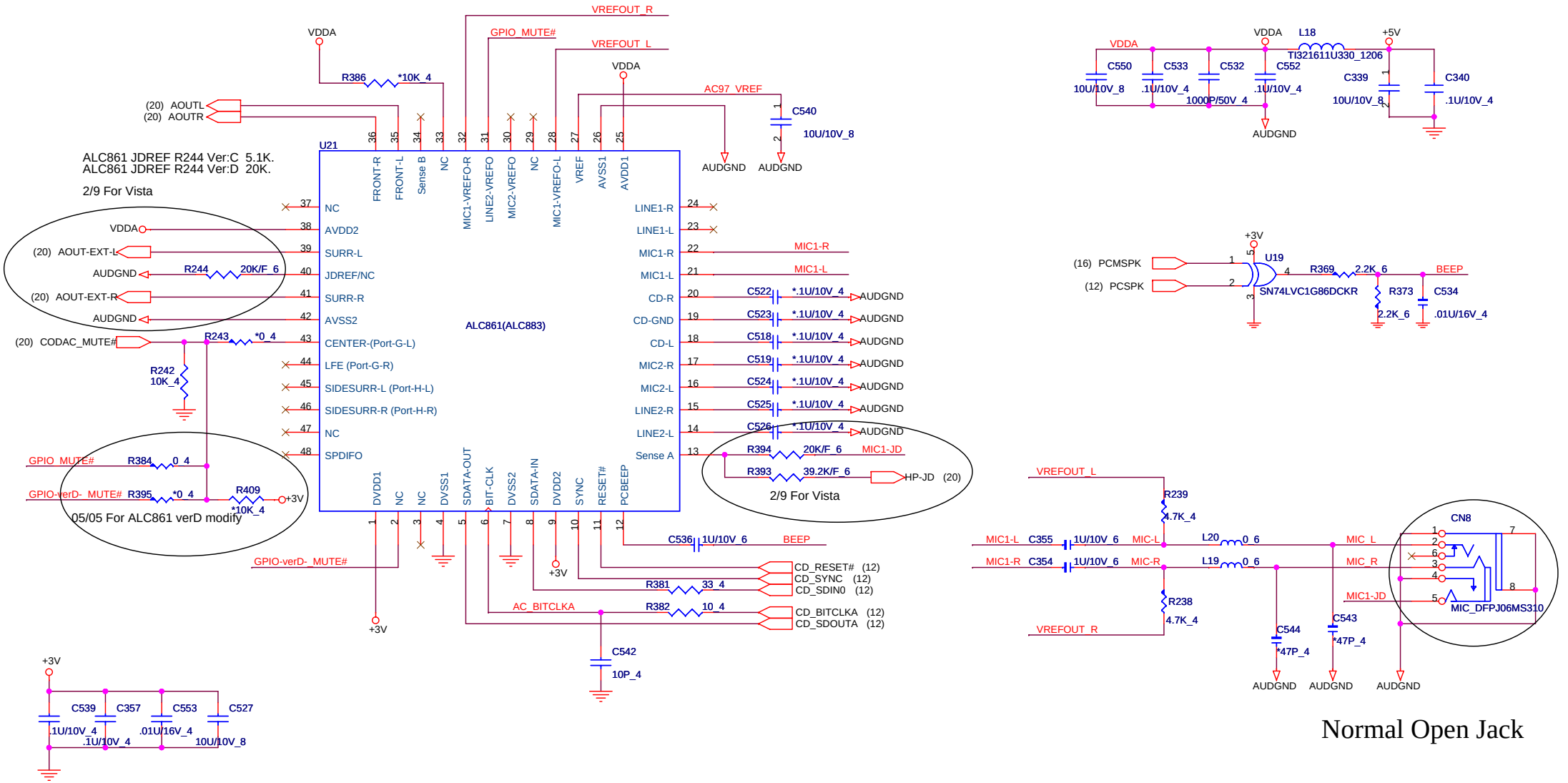


IDE

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM	2A
Date: Monday, May 08, 2006	Sheet 18 of 30	



Normal Open Jack

ADO

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	REALTEK ALC861	2A
Date: Friday, May 05, 2006	Sheet 19 of 30	

2/5 Modify RVDD & GND Circuit

3/29 Reserved circuir for new AMP G1441.

EMI

SPEAKER CON

HEADPHONE

04/28 Add Gate circuit For "PoPo" Sound issue.

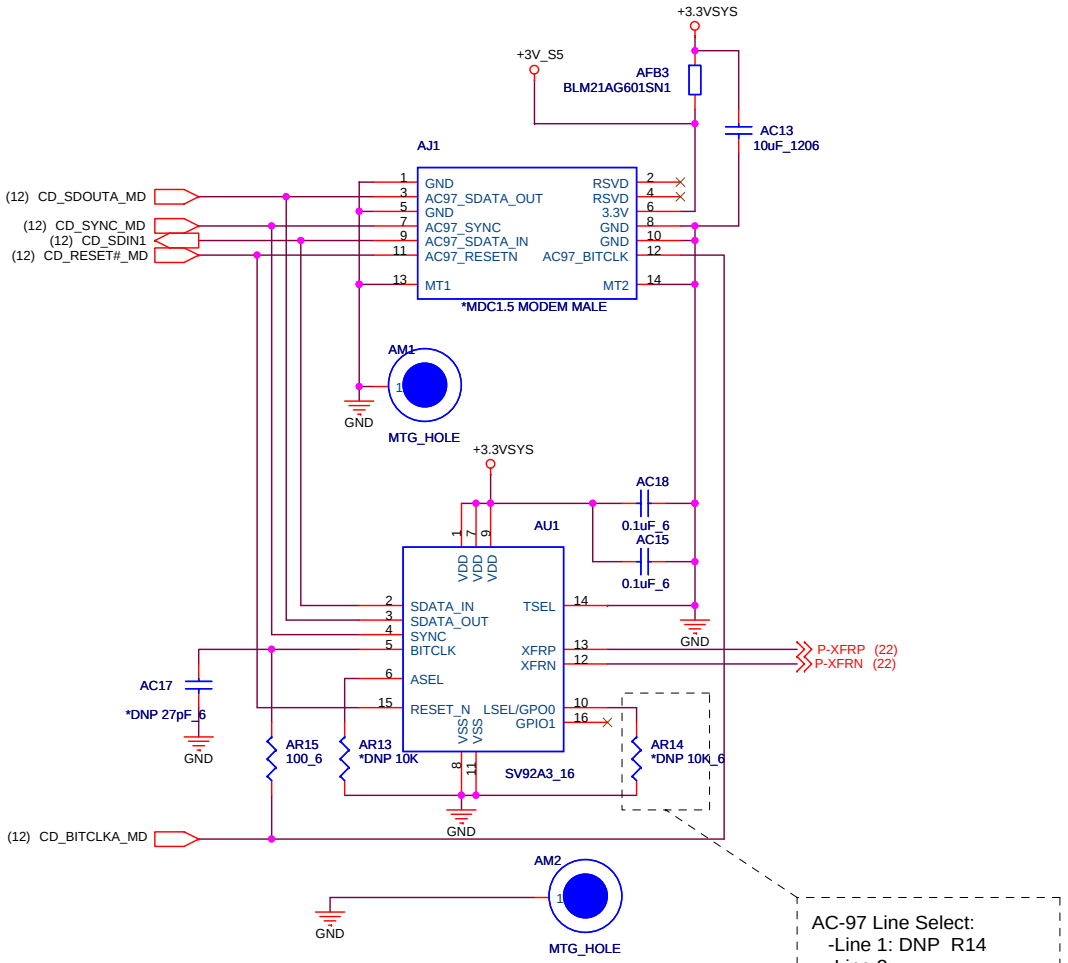
2/9 For Vista

Normal Open Jack

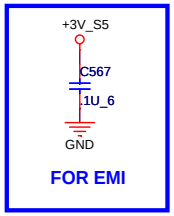
04/28 Add Gate circuit For "PoPo" Sound issue.

ADO

PROJECT : BL1		
Quanta Computer Inc.		
Size	Document Number: AUDIO AMP(G1432 / G1410)	Rev: 3B
Date: Wednesday, May 10, 2006	Sheet 20 of 30	



MDM



Pb

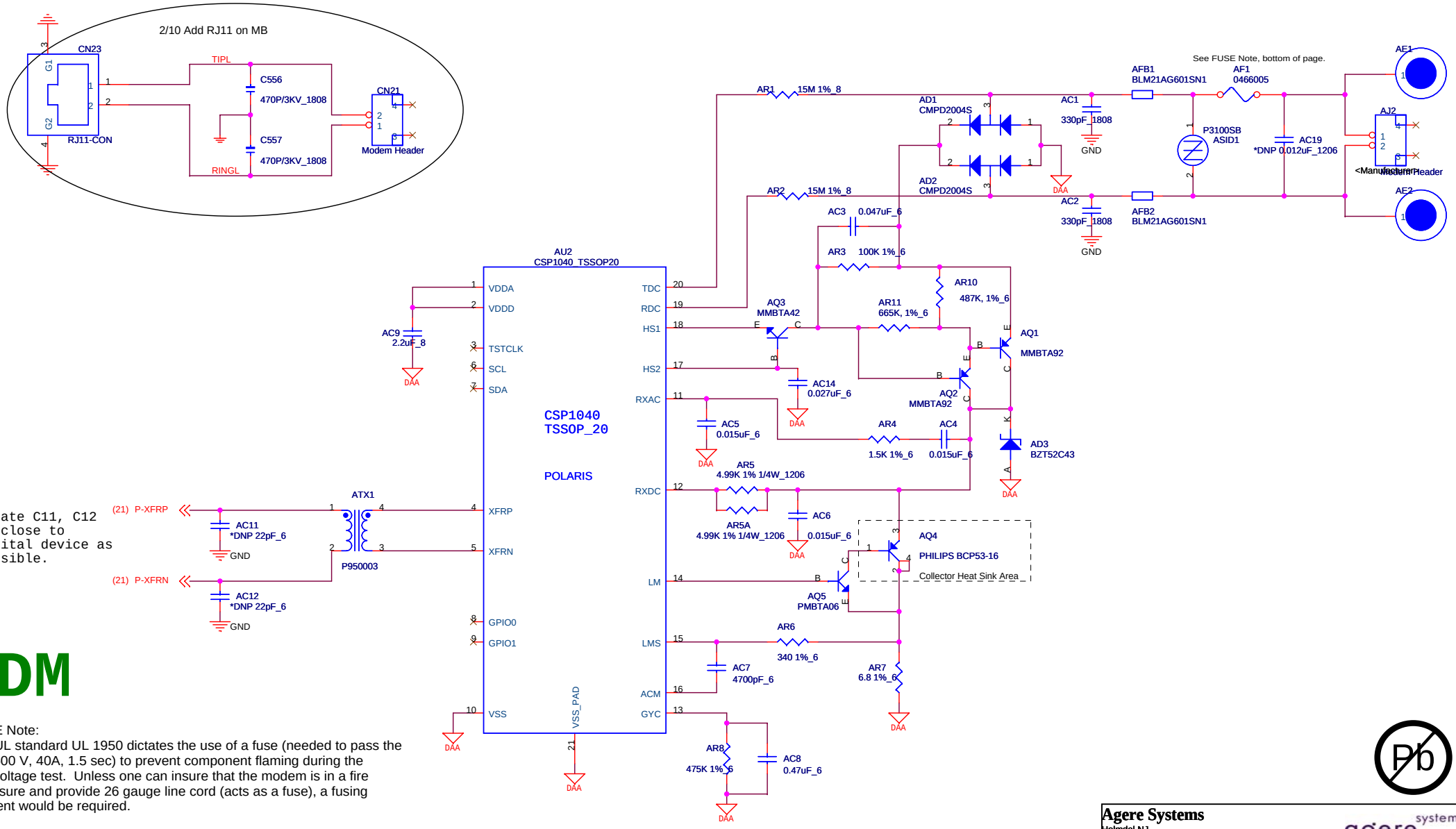
Agere Systems
Holmdel NJ
agere systems

Design Engineer: C. Russo

Title
DELPHI SV92A3 MDC 1.5 Reference Design

Size	Document Number	Rev
B	**DIGITAL INTERFACE**	1A

Date: Friday, April 28, 2006 Sheet 21 of 30

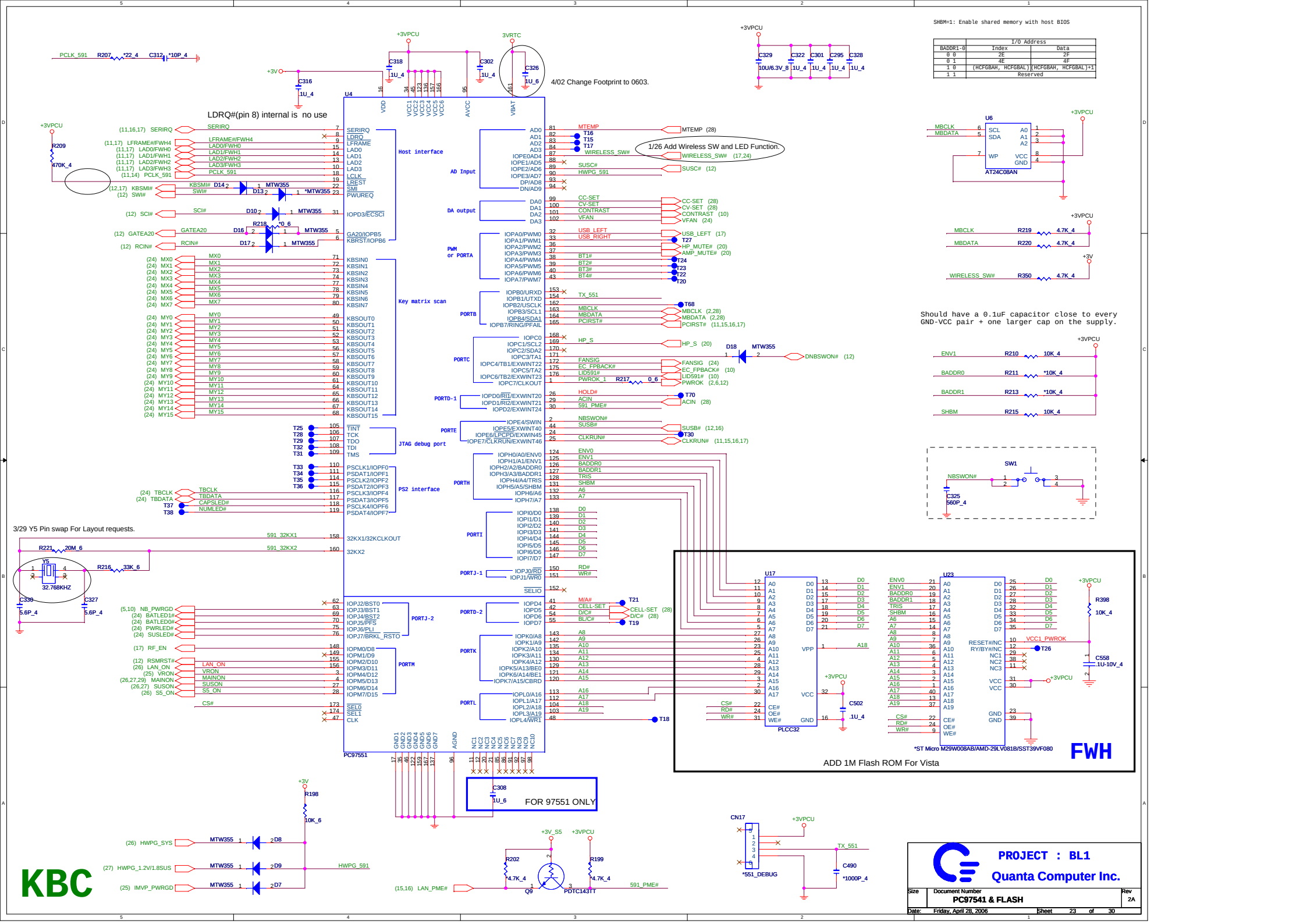


MDM

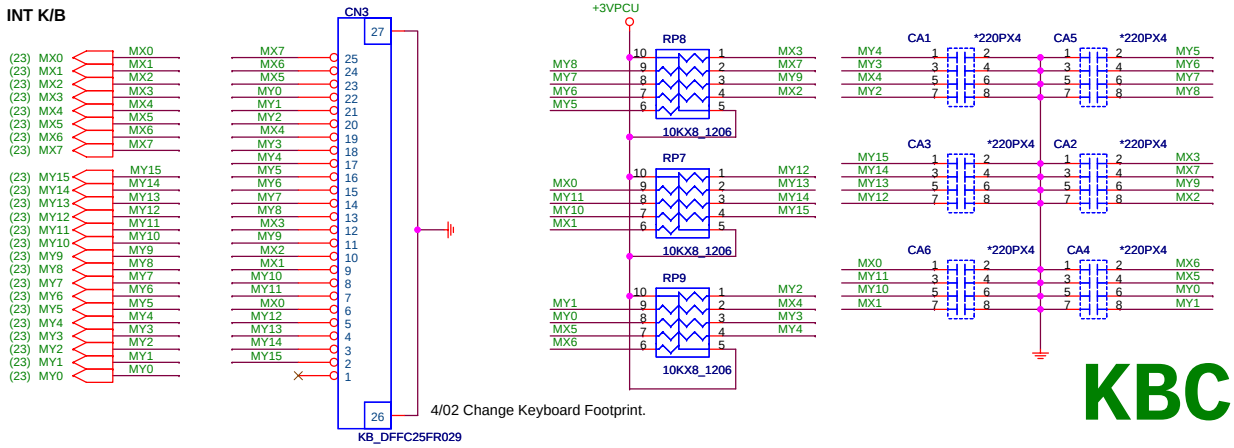
FUSE Note:
The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.

Agere Systems
Holmdel NJ
Design Engineer: R. Trevino
Title
DELPHI SV92A3 MDC 1.5 Reference Design
Size B | Document Number CSP1040 DAA | Rev 2A
Date: Saturday, May 06, 2006 | Sheet 22 of 30

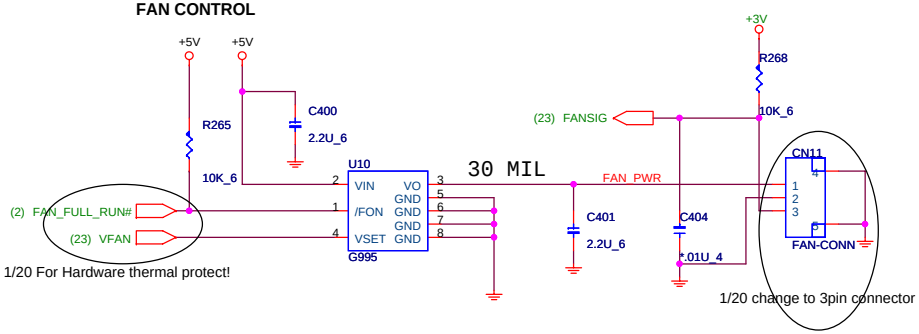

SHBM=1: Enable shared memory with host BIOS
I/O Address
BADDR1-0 | Index | Data
0 0 | 2E | 2F
0 1 | 4E | 4F
1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1
1 1 | Reserved
4/02 Change Footprint to 0603.
LDRQ#(pin 8) internal is no use
1/26 Add Wireless SW and LED Function.
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
3/29 Y5 Pin swap For Layout requests.
ADD 1M Flash ROM For Vista
*ST Micro M29W008AB/AMD-29LV081B/SST39VF080
FWH
FOR 97551 ONLY
*551_DEBUG
PROJECT : BL1
Quanta Computer Inc.
PC97541 & FLASH
Rev 2A
Date: Friday, April 28, 2006
Sheet 23 of 30
KBC

INT K/B



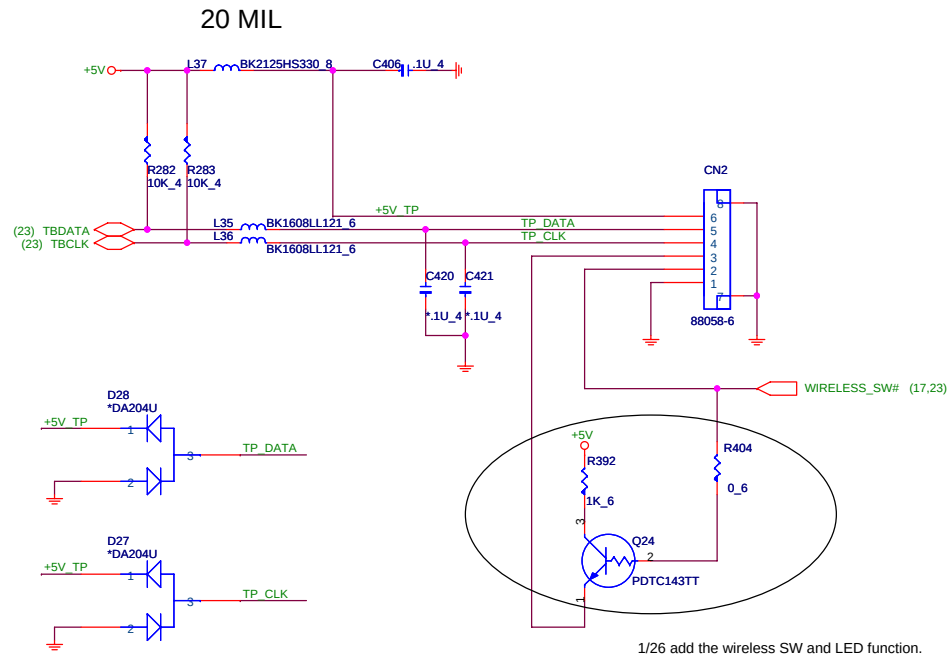
KBC

FAN CONTROL



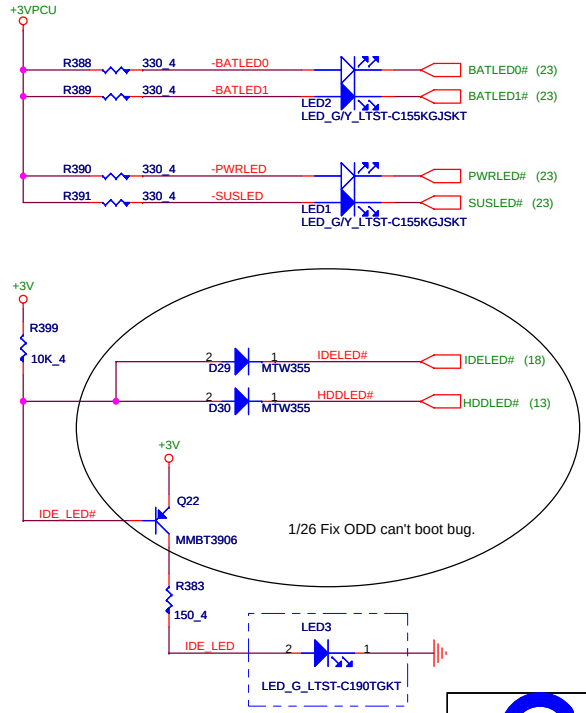
THM

TOUCH PAD



TPD

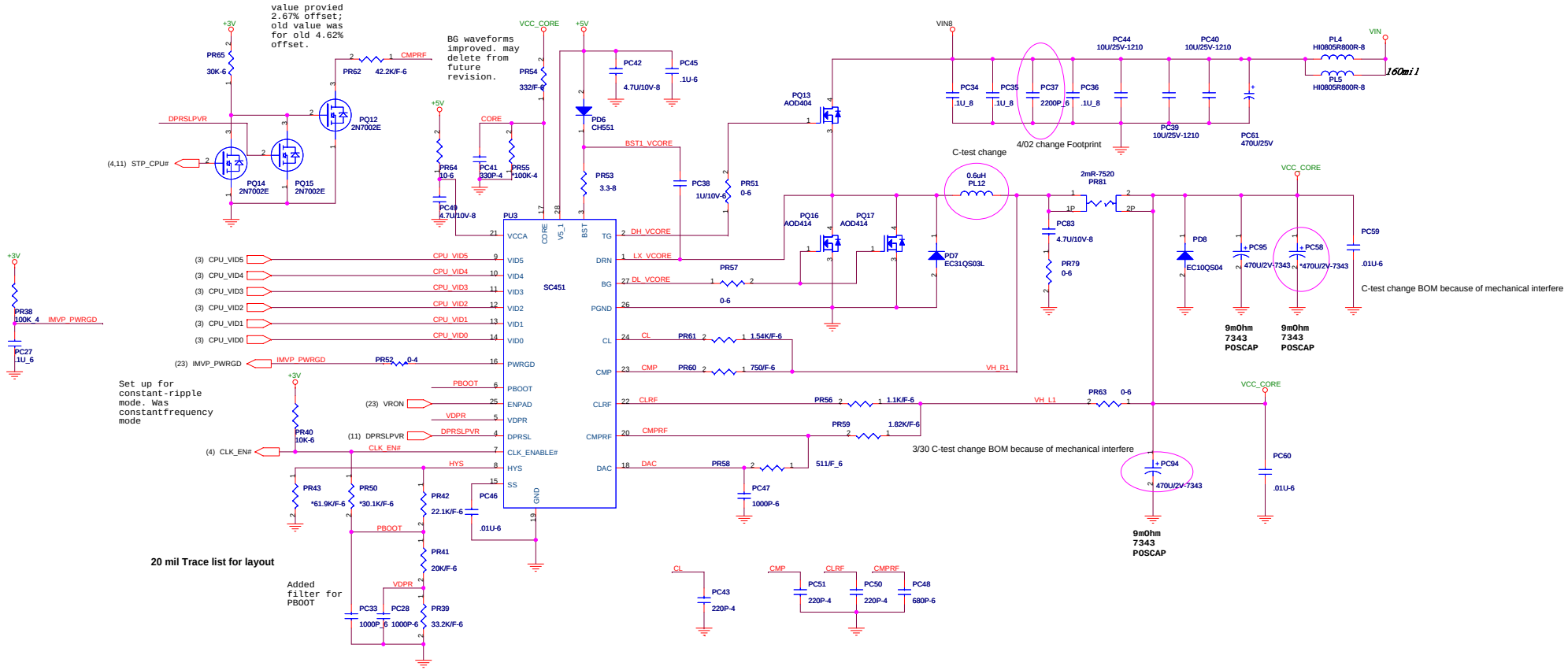
ON BOARD LED



PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	T/P,FAN,SWITCH,LED,K/B	3A
Date: Friday, May 05, 2006	Sheet 24 of 30	



V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

DCD

PROJECT : BL1
Quanta Computer Inc.

Size	Document Number	Rev
	SC451(VCORE)	1A
Date: Friday, April 28, 2006	Sheet 25 of 30	

4/27 Change capacitor tolerance for worst environment.

3/30 C-test change to solve 8744 error UVP issue

3/30 C-test change to solve 8744 error UVP issue

3/30 C-test change to solve S3 fail

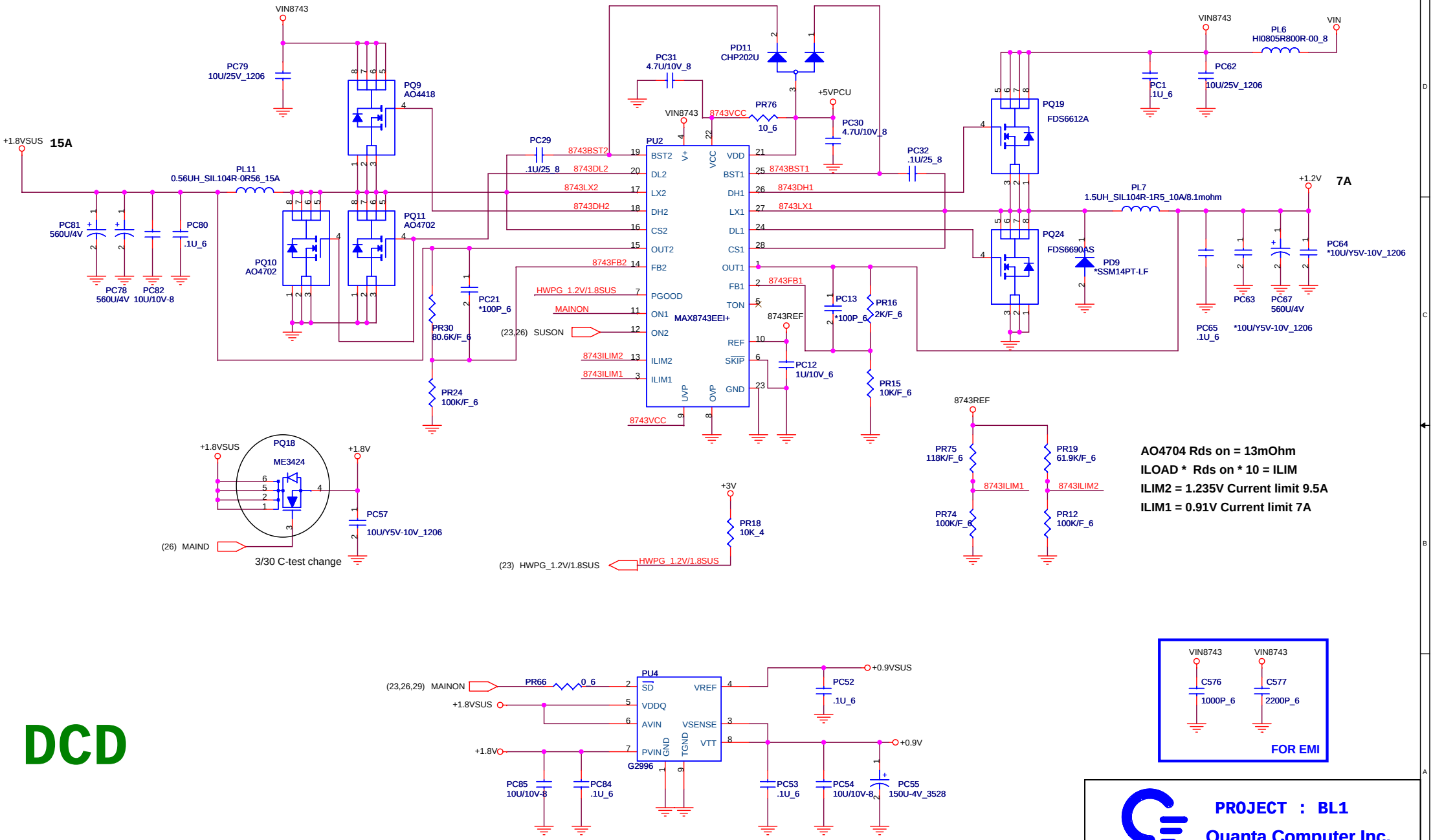
3/30 C-test change

3/30 C-test change

3/30 C-test change to speed up +3V discharge time

DCD

PROJECT :	BL1
Quanta Computer Inc.	
Size	Document Number: 5V/3.3V (MAX8744) — Rev: 3A
Date: Tuesday, May 09, 2006	Sheet 26 of 30



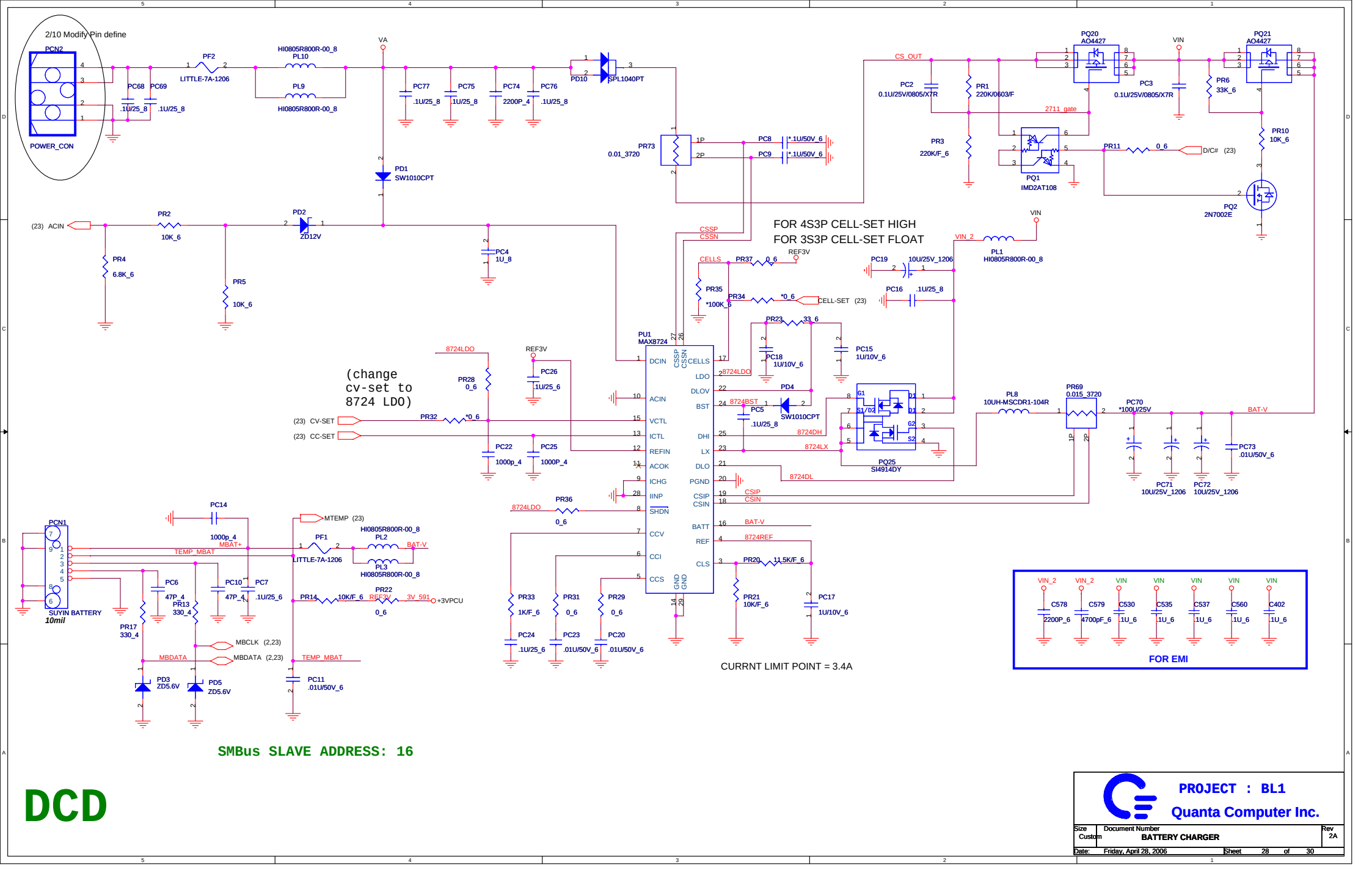
DCD

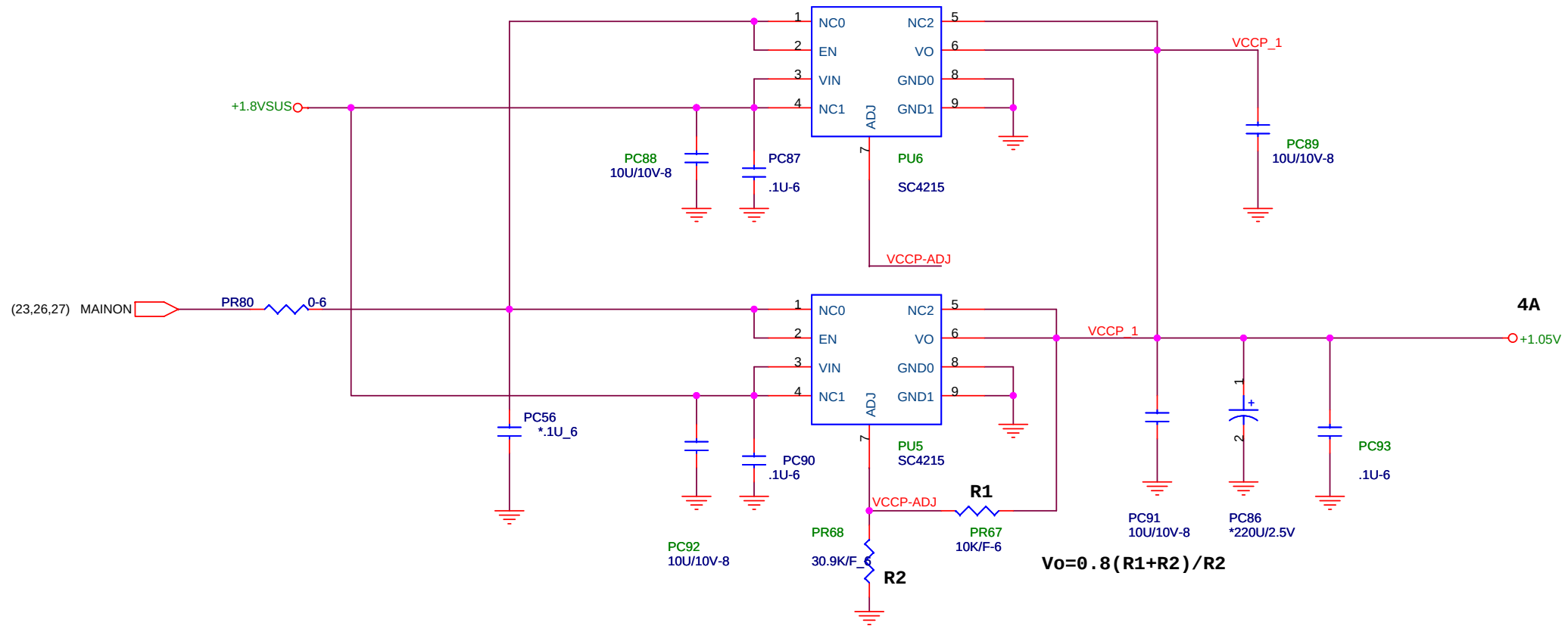
PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	+1.8/1.2V / VTT	1A

Date: Friday, April 28, 2006 Sheet 27 of 30


2/10 Modify Pin define
PCN2
POWER_CON
PF2
LITTLE-7A-1206
HI0805R800R-00_8
PL10
PL9
HI0805R800R-00_8
VA
PC68
PC69
.1U/25_8
.1U/25_8
PC77
.1U/25_8
PC75
.1U/25_8
PC74
2200P_4
PC76
.1U/25_8
PD10
SPL1040PT
PD1
SW1010CPT
PR73
0.01_3720
1P
2P
PC8
*.1U/50V_6
PC9
*.1U/50V_6
CS_OUT
PC2
0.1U/25V/0805/X7R
PR1
220K/0603/F
PQ20
AO4427
VIN
PC3
0.1U/25V/0805/X7R
PQ21
AO4427
PR6
33K_6
2711_gate
PR3
220K/F_6
PQ1
IMD2AT108
PR11
0_6
D/C#
(23)
PR10
10K_6
PQ2
2N7002E
(23) ACIN
PR2
10K_6
PD2
ZD12V
PR4
6.8K_6
PR5
10K_6
PC4
1U_8
CSSP
CSSN
FOR 4S3P CELL-SET HIGH
FOR 3S3P CELL-SET FLOAT
VIN
VIN_2
PL1
HI0805R800R-00_8
CELLS
PR37
0_6
REF3V
PC19
10U/25V_1206
PC16
.1U/25_8
PR35
*100K_6
PR34
*0_6
CELL-SET
(23)
PR23
33_6
PC18
1U/10V_6
PC15
1U/10V_6
PU1
MAX8724
DCIN
CSSP
CSSN
CELLS
LDO
DLOV
BST
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
REF
CLS
ACIN
VCTL
ICTL
REFIN
ACOK
ICHG
IINP
SHDN
CCV
CCI
CCS
GND
8724LDO
PD4
SW1010CPT
PC5
.1U/25_8
8724BST
8724DH
8724LX
8724DL
PQ25
SI4914DY
PL8
10UH-MSCDR1-104R
PR69
0.015_3720
PC70
*100U/25V
BAT-V
PC71
10U/25V_1206
PC72
10U/25V_1206
PC73
.01U/50V_6
8724LDO
REF3V
PR28
0_6
PC26
.1U/25_6
(23) CV-SET
(23) CC-SET
PR32
*0_6
PC22
1000p_4
PC25
1000P_4
(change
cv-set to
8724 LDO)
PR36
0_6
8724LDO
PR33
1K/F_6
PC24
.1U/25_6
PR31
0_6
PC23
.01U/50V_6
PR29
0_6
PC20
.01U/50V_6
PR21
10K/F_6
PR20
11.5K/F_6
8724REF
PC17
1U/10V_6
CURRNT LIMIT POINT = 3.4A
PC14
1000p_4
PCN1
SUYIN BATTERY
10mil
MBAT+
TEMP_MBAT
PF1
LITTLE-7A-1206
HI0805R800R-00_8
PL2
PL3
HI0805R800R-00_8
BAT-V
PC6
47P_4
PC10
47P_4
PC7
.1U/25_6
PR13
330_4
PR17
330_4
PR14
10K/F_6
REF3V
PR22
0_6
3V_591
+3VPCU
MTEMP (23)
MBCLK (2,23)
MBDATA
MBDATA (2,23)
TEMP_MBAT
PD3
ZD5.6V
PD5
ZD5.6V
PC11
.01U/50V_6
VIN_2
VIN_2
VIN
VIN
VIN
VIN
VIN
C578
2200P_6
C579
4700pF_6
C530
.1U_6
C535
.1U_6
C537
.1U_6
C560
.1U_6
C402
.1U_6
FOR EMI
SMBus SLAVE ADDRESS: 16
DCD
PROJECT : BL1
Quanta Computer Inc.
Size
Custom
Document Number
BATTERY CHARGER
Rev
2A
Date: Friday, April 28, 2006
Sheet 28 of 30



DCD

PROJECT : BL1

Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V	1A
Date: Friday, April 28, 2006	Sheet 29 of 30	