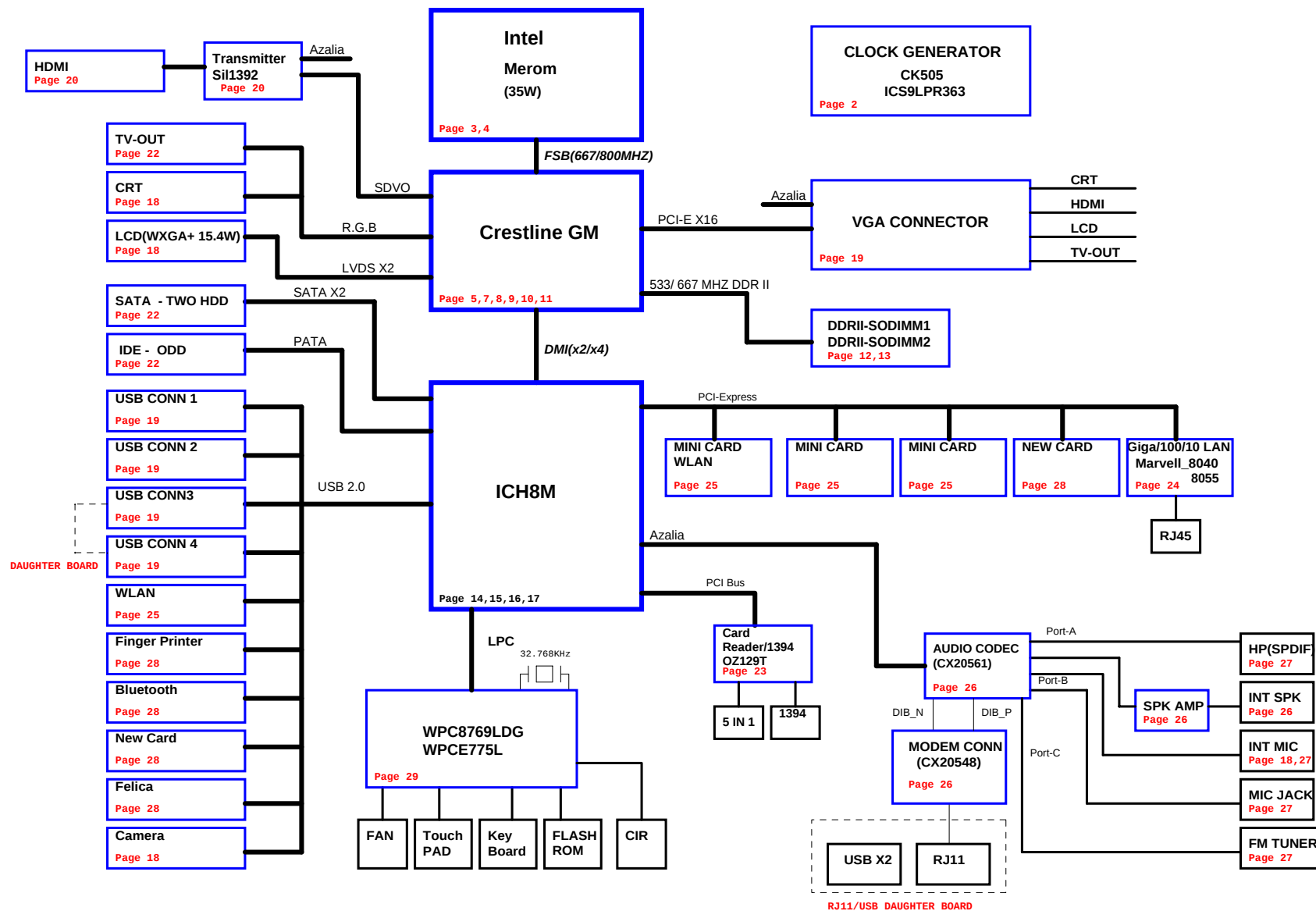


LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

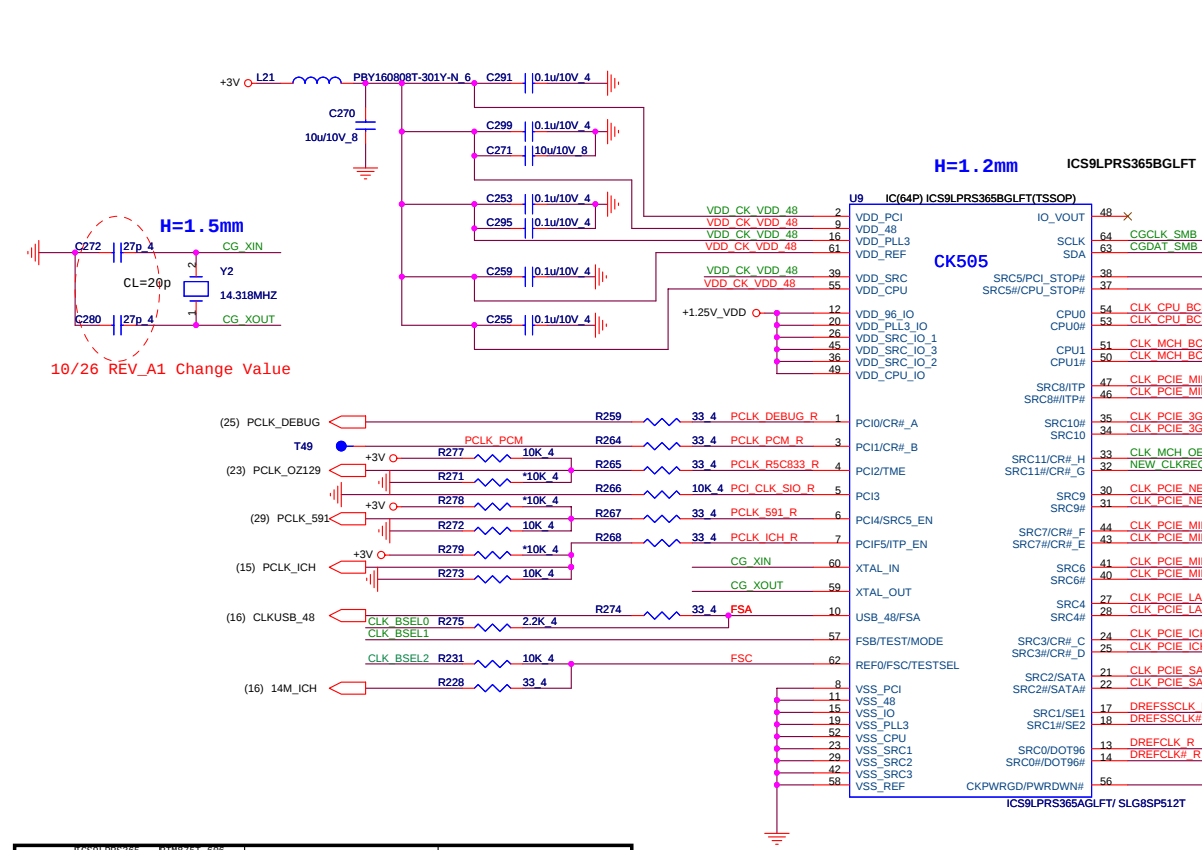
+1.8VSUS

+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V_S5
+5V
SMDDR_VTERM
SMDDR_VREF

**Intel
Merom
(35W)**



Clock Generator

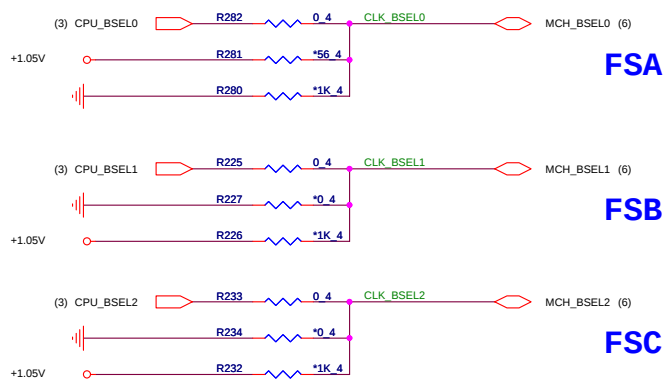


	ICS9LPRS365 (ALPRS365K13)	RT8751-666 (AL090875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME Internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5 EN Internal PD	PIN37/38 IS SRC5	PIN37/38 IS SRC5 (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL Internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN Internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRCB (default)

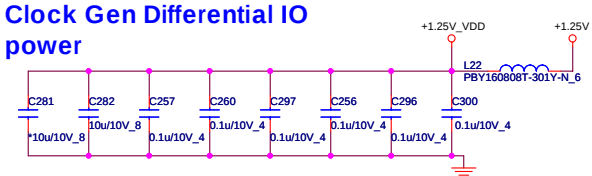
CPU Clock select

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

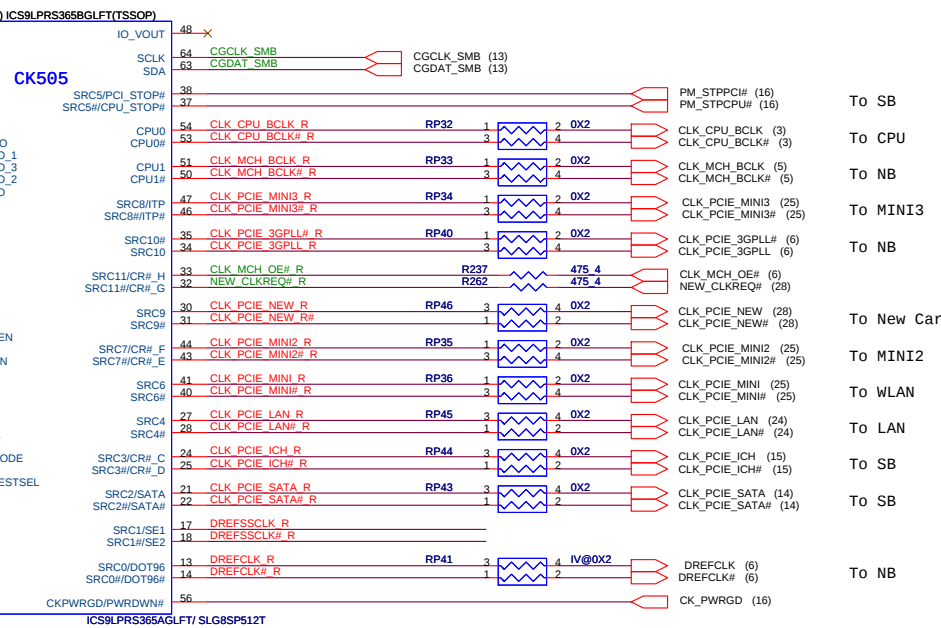


Clock Gen Differential IO power

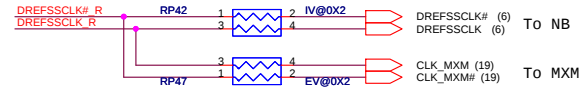
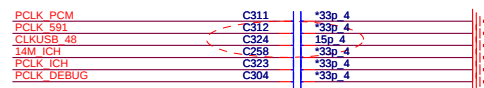


H=1.2mm ICS9LPRS365BGLFT

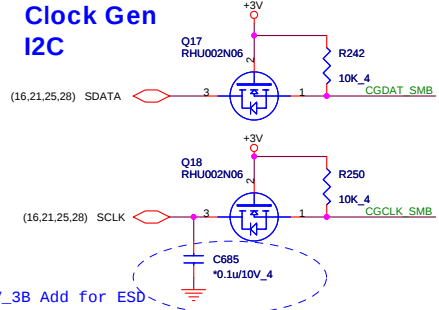
CK505



10/31 REV_A1 Change Value



Clock Gen I2C



01/21 REV_3B Add for ESD



Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

CLK_GEN./ CK505

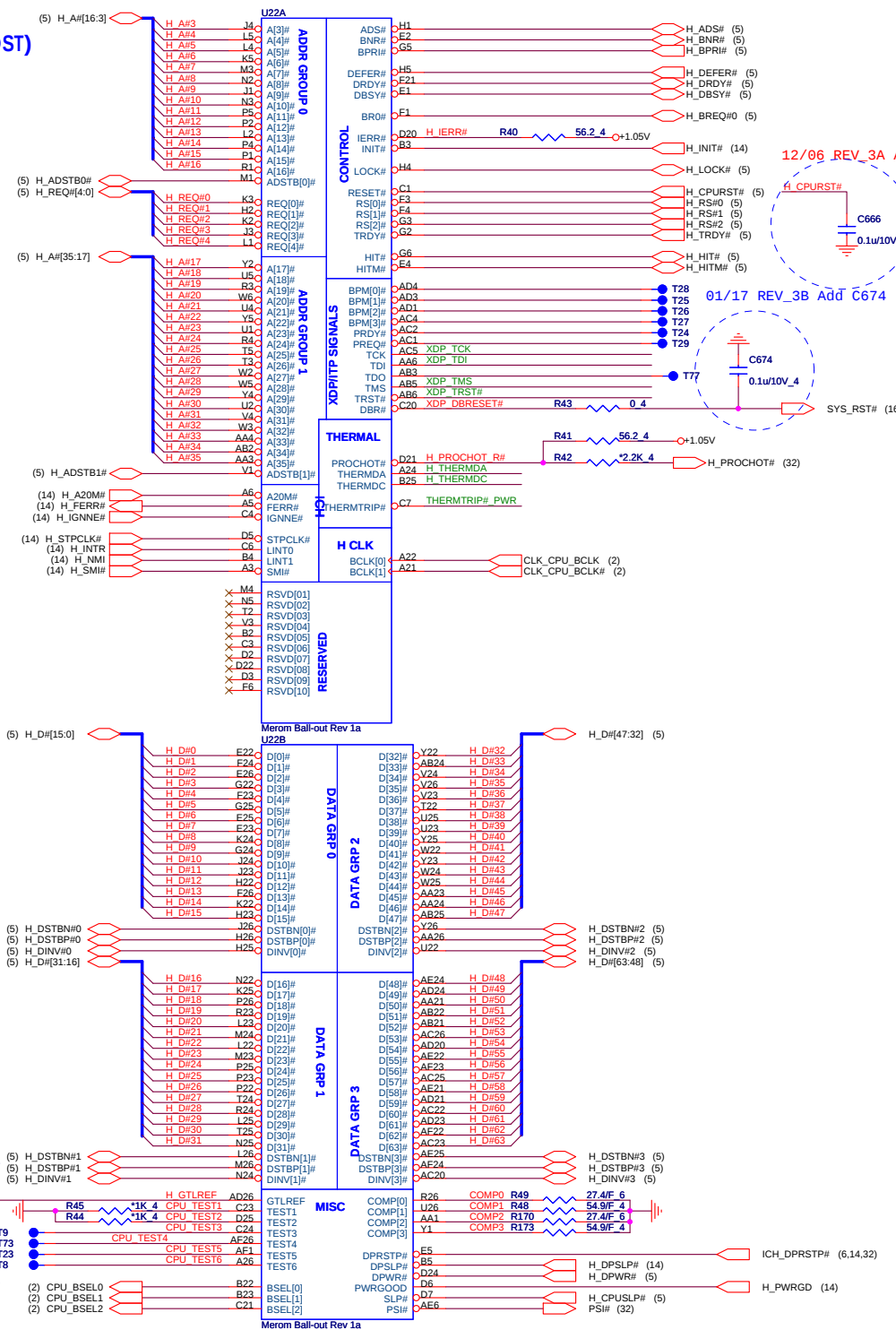
Size Document Number

Date: Tuesday, January 22, 2008

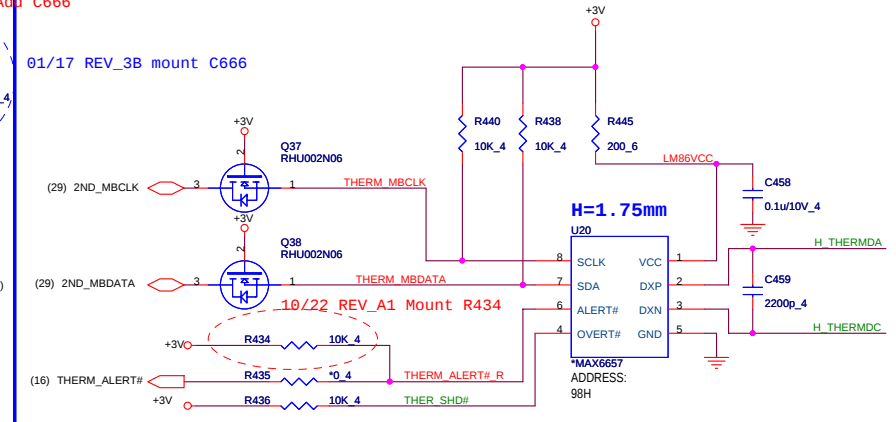
Rev 1A

Sheet 2 of 37

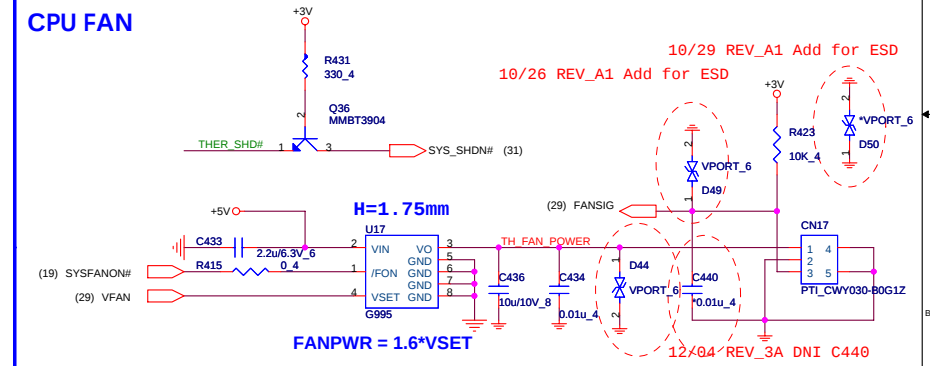
CPU(HOST)



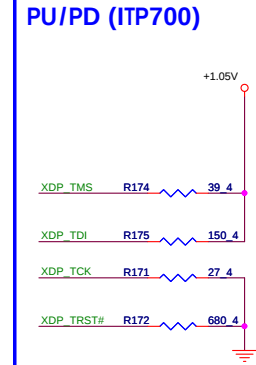
CPU Thermal monitor



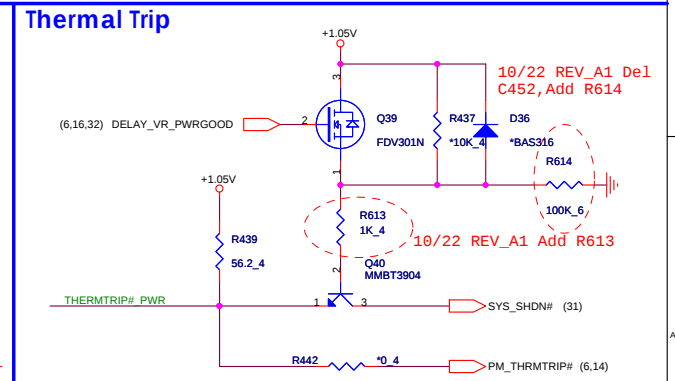
CPU FAN



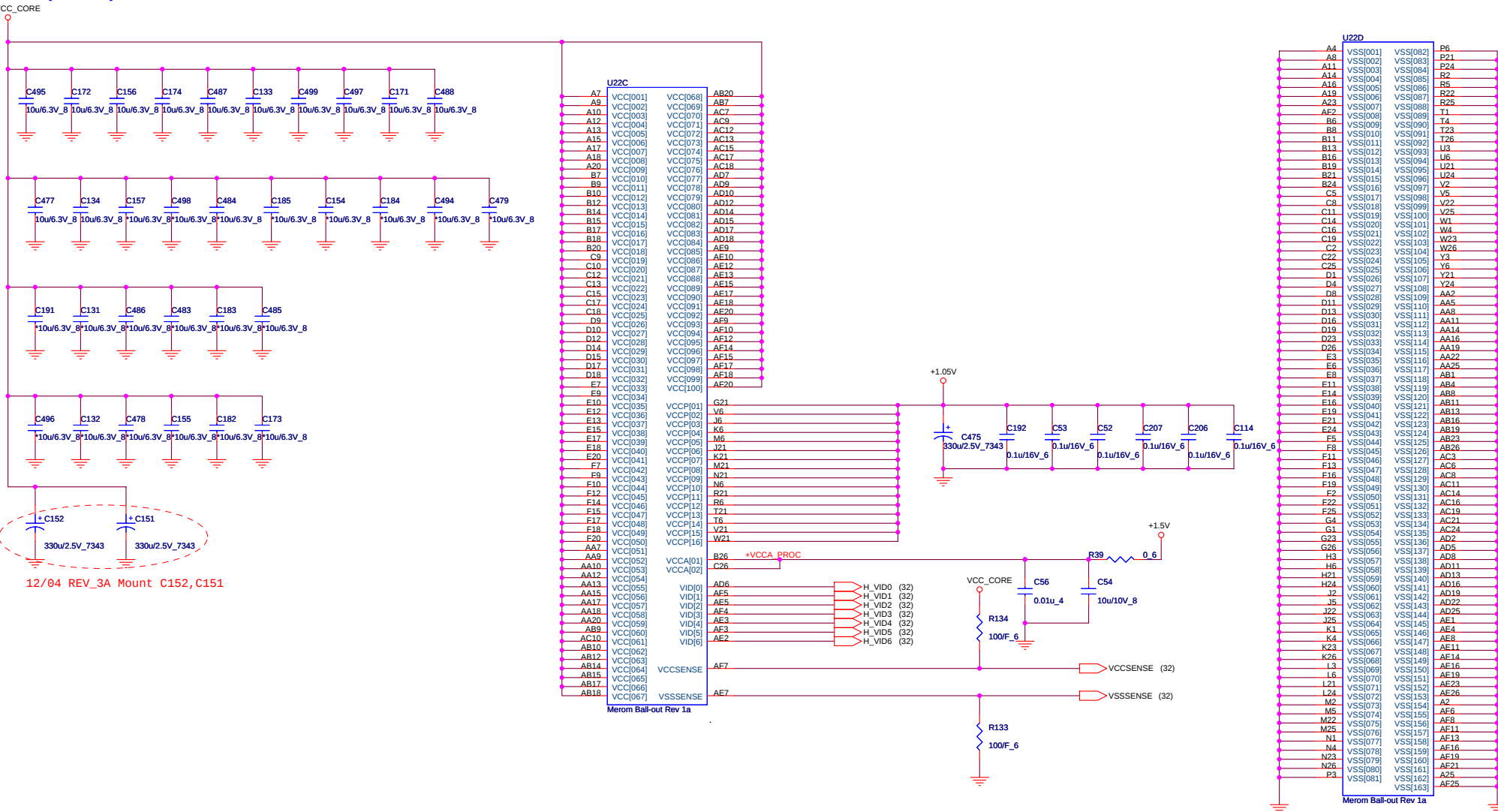
PU/PD (ITP700)



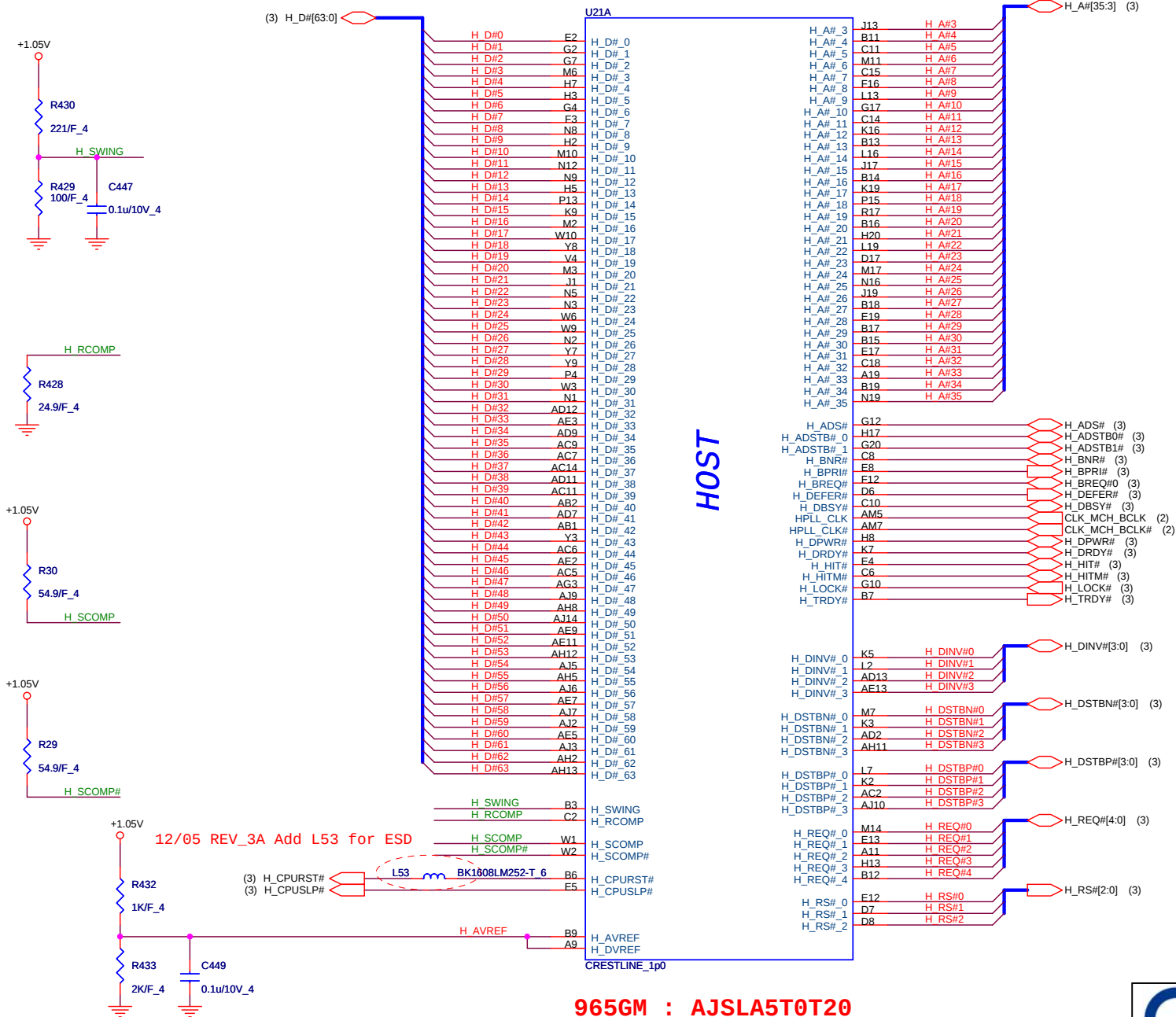
Thermal Trip



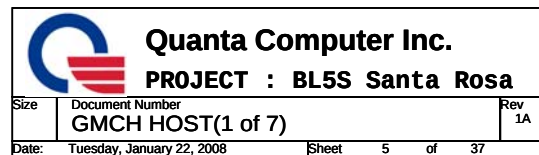
CPU(Power)

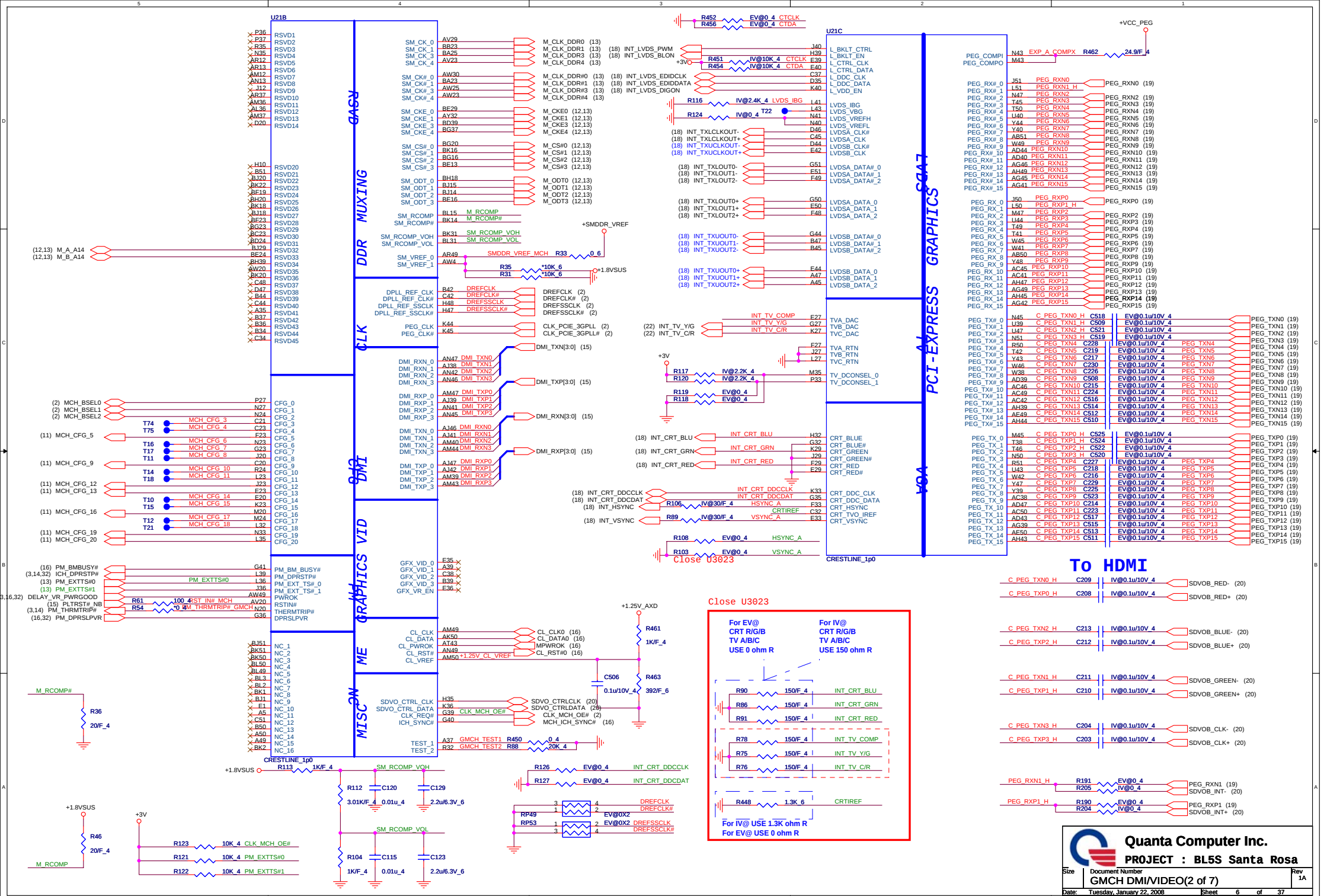


NB(HOST)

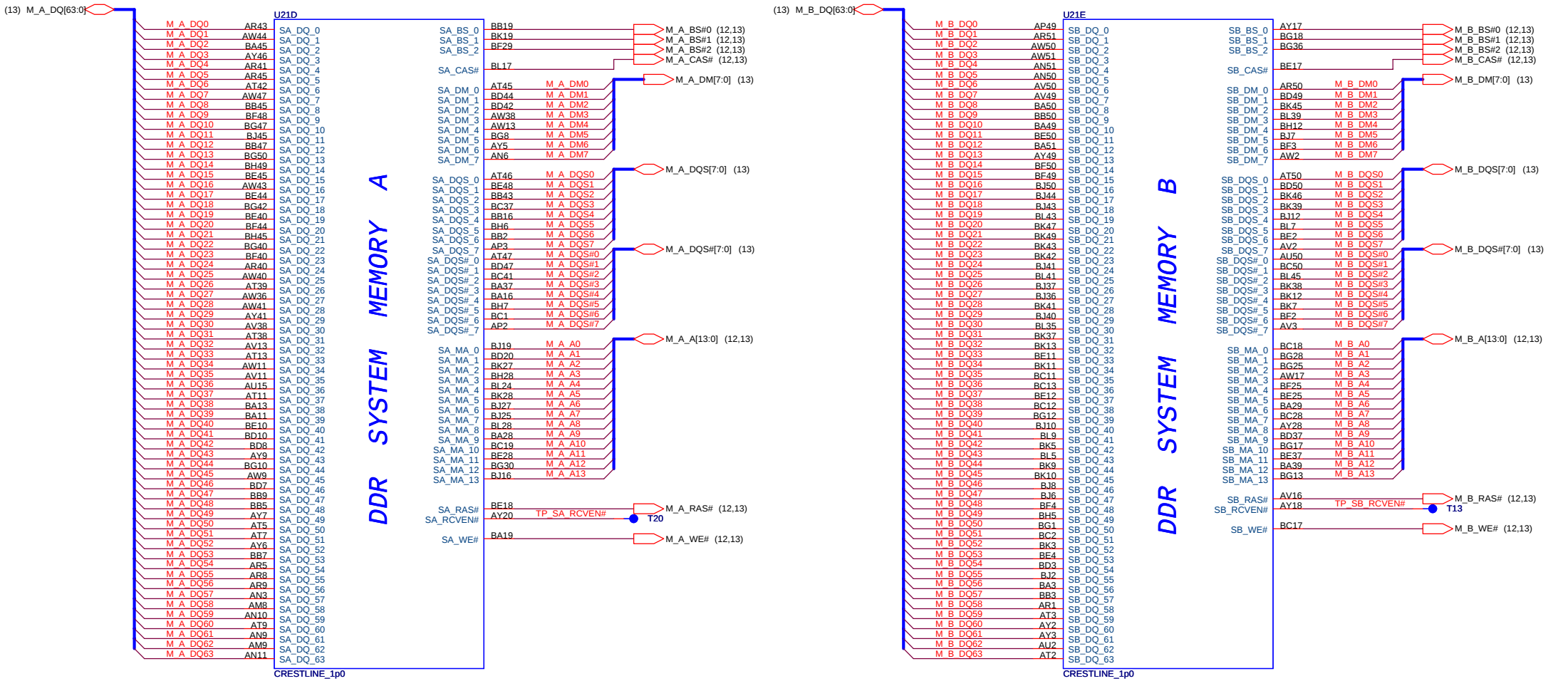


965GM : AJSLA5T0T20
965PM : AJSLA5U0T25
960GL : AJSLA5V0T09

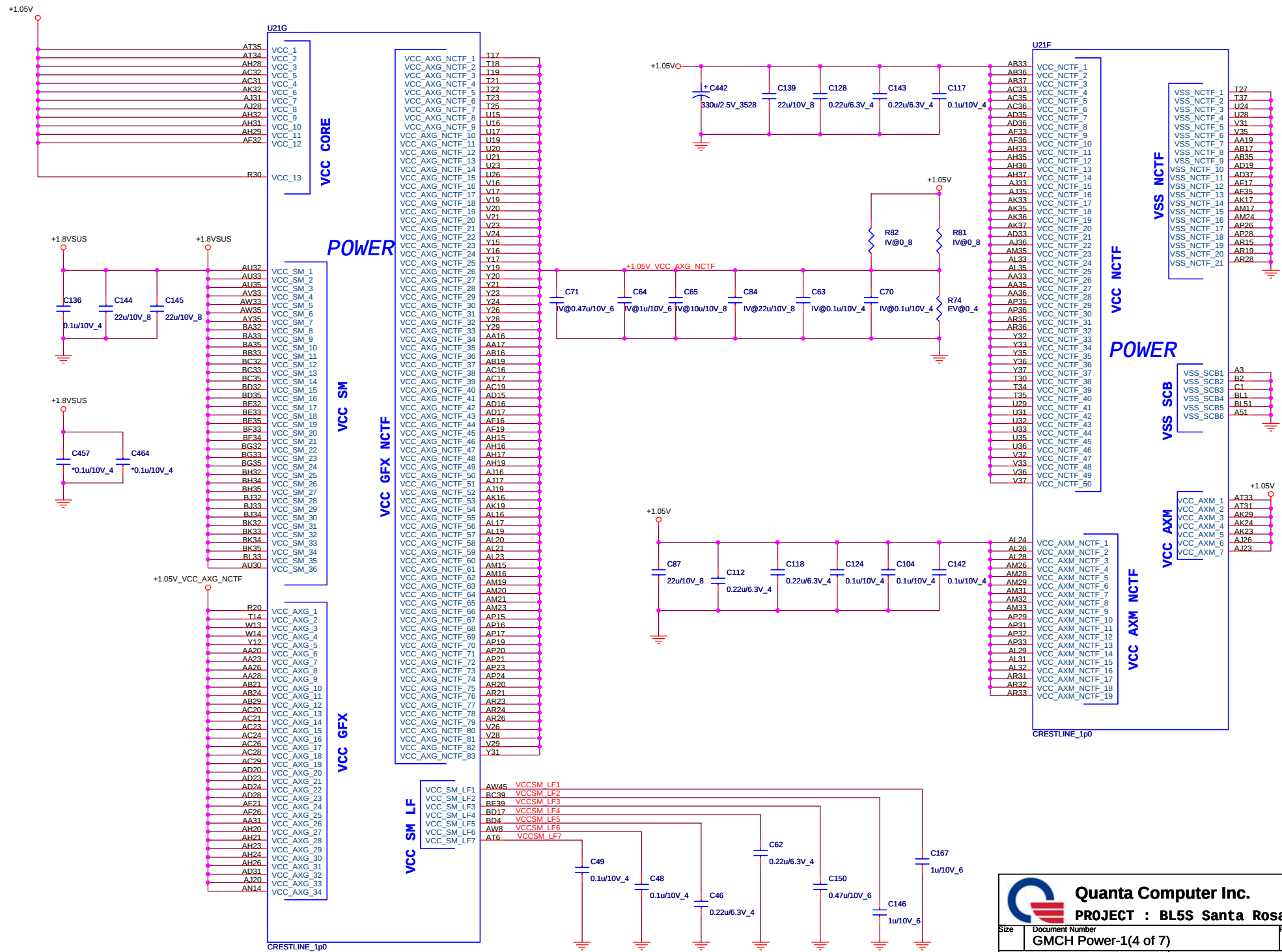




NB(Memory controller)



NB(Power-1)



NB(Power-2)

IV&EV Dis/Enable setting

CRT/TV Disable/Enable guideline

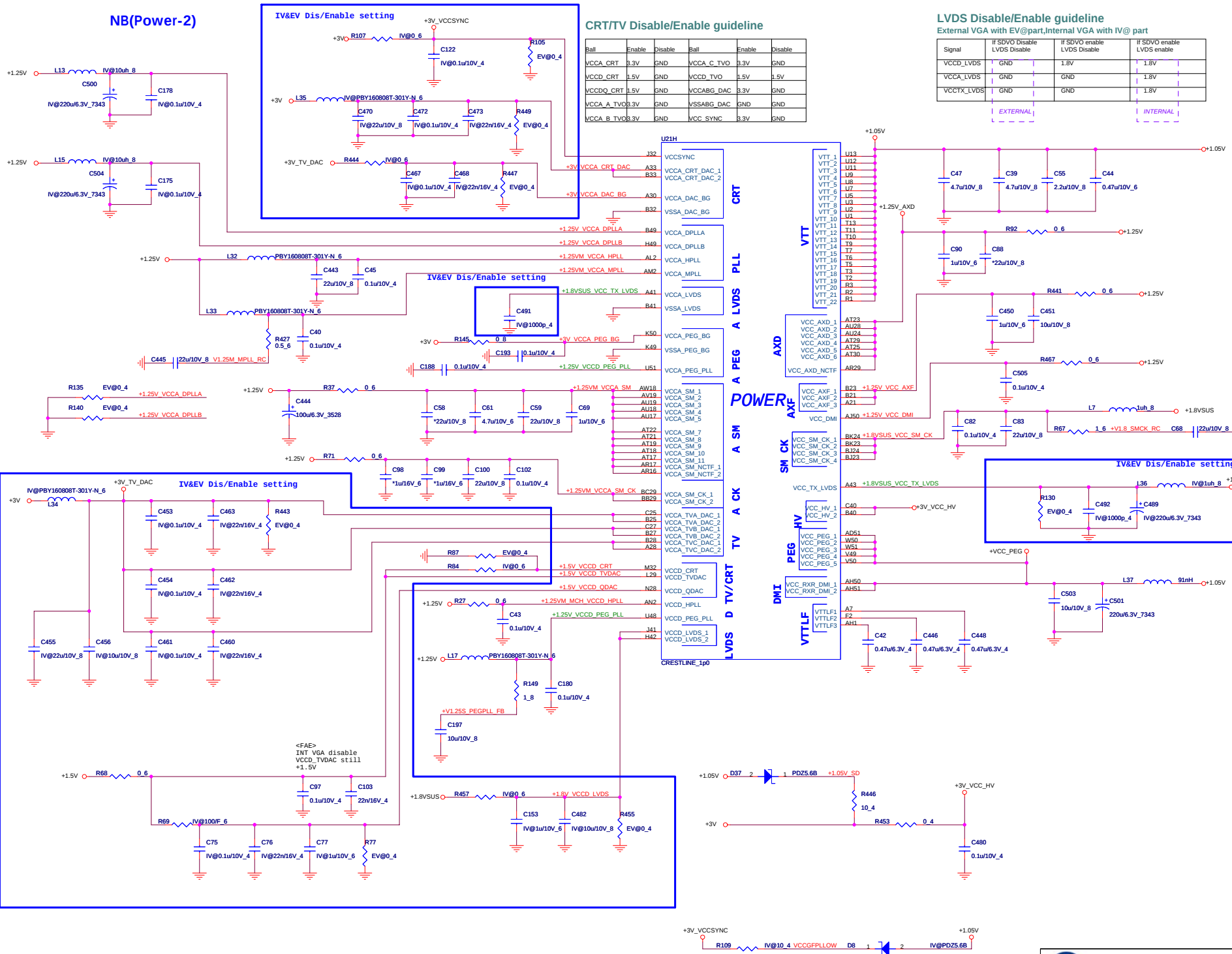
LVDS Disable/Enable guideline

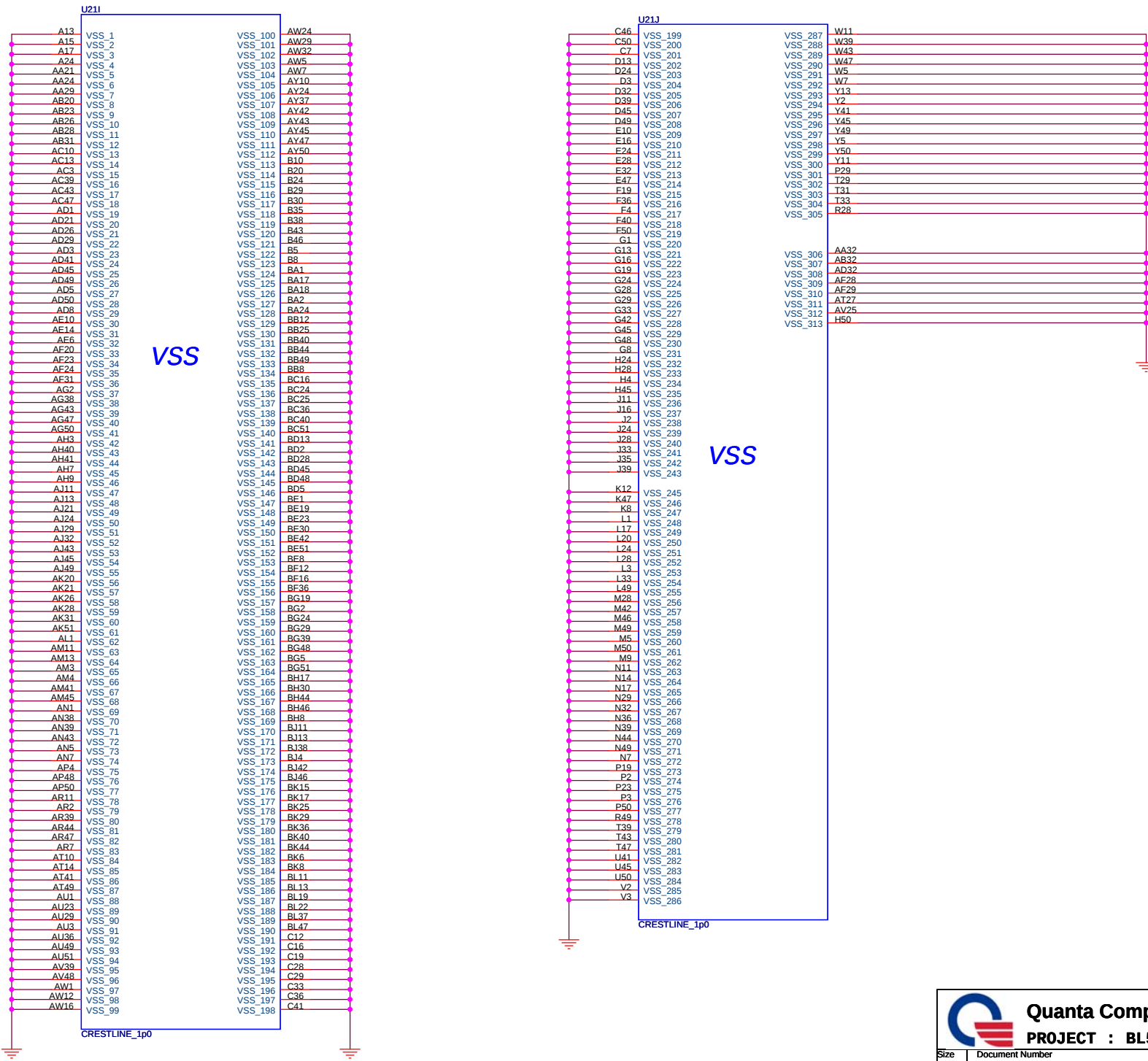
External VGA with EV@part, Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCC1X_LVDS	GND	GND	1.8V

EXTERNAL

INTERNAL





Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMI X4(Default)
-----------	--



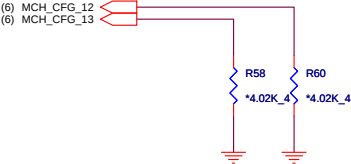
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--



XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

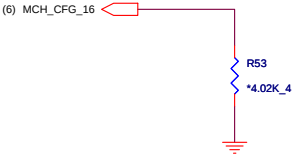


SDVO Present

Strap define at External DVI control page

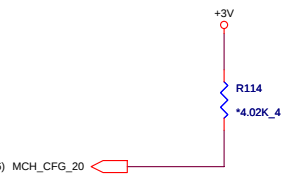
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---

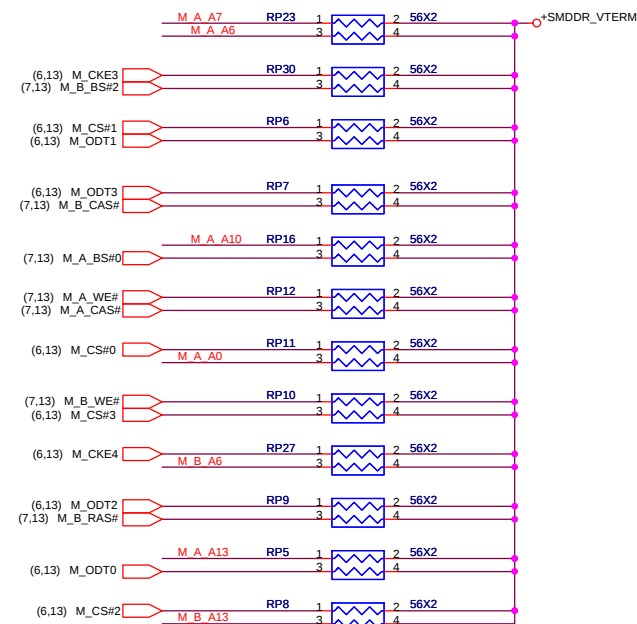
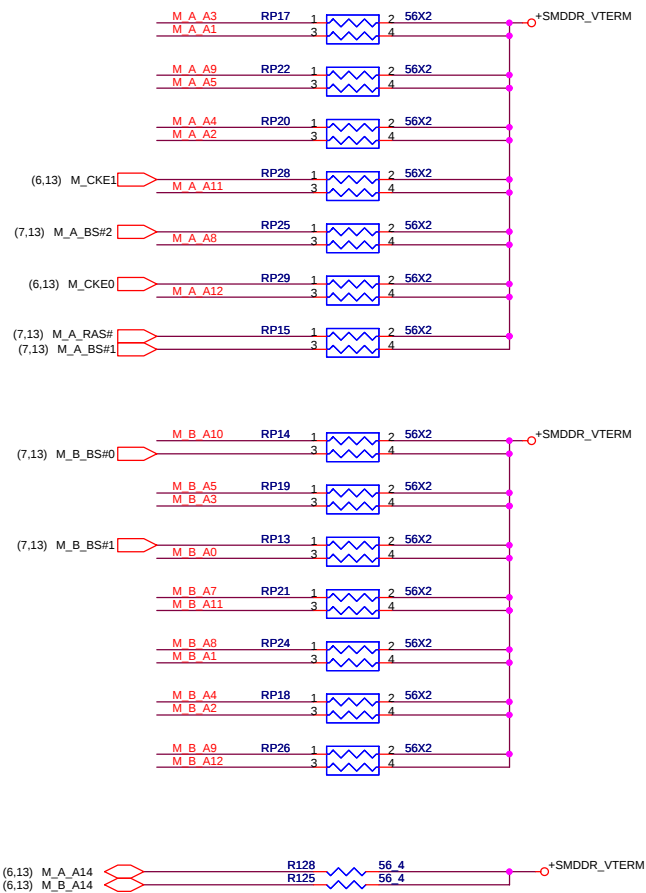


SDVO/PCIE Concurrent operation

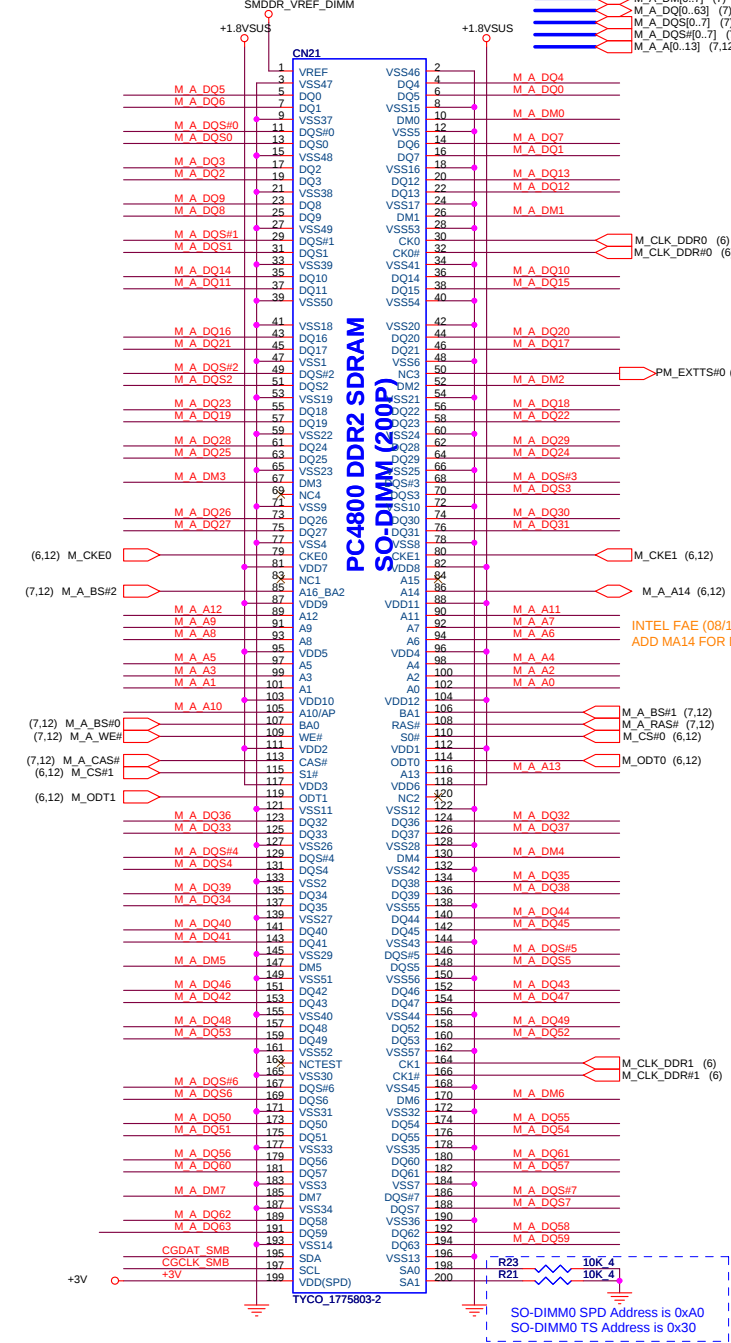
MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
------------	---



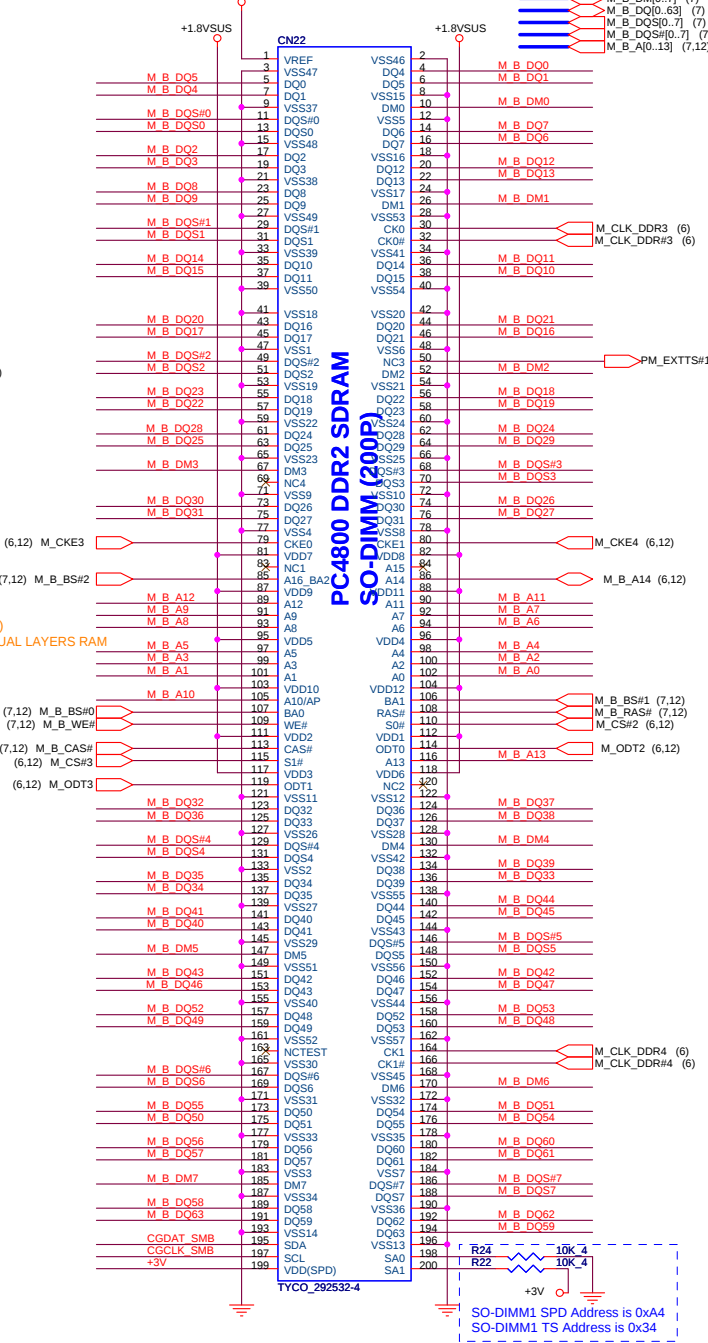
DDR2 Dual channel A/B PU



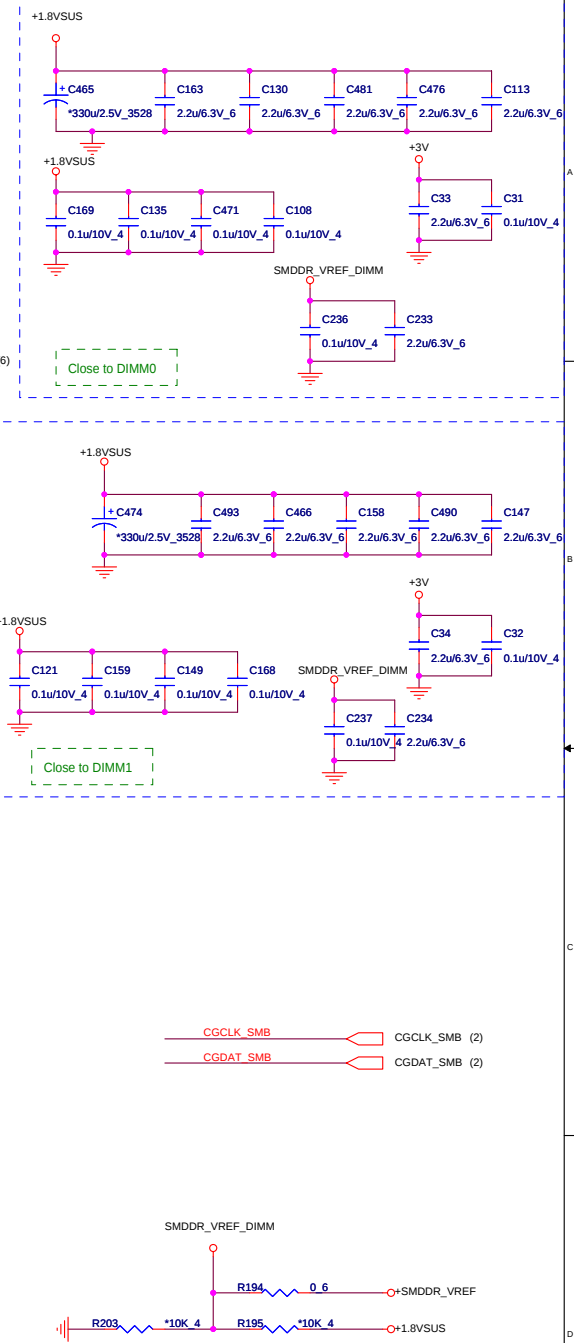
DDR2 Dual channel A/B CONN



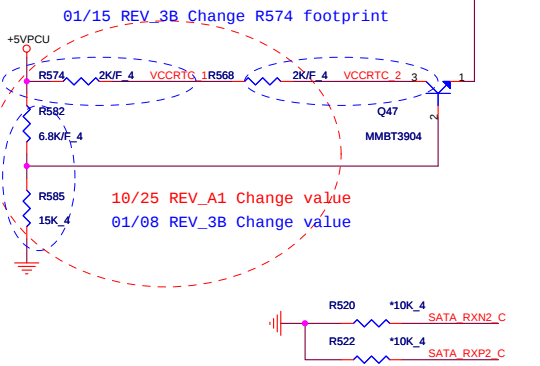
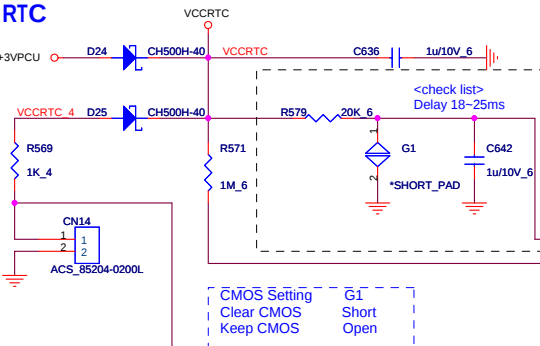
Standard Type H: 6.5mm
CLOCK 0,1
CKE 0,1



Standard Type H: 11mm
CLOCK 3,4
CKE 2,3



RTC



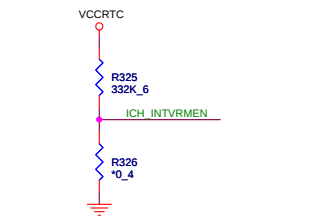
SATA Disable

- 1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
- 2.NC: SATA[2:0]TXp/n , SATALED#
- 3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
- 4.BIOS disable

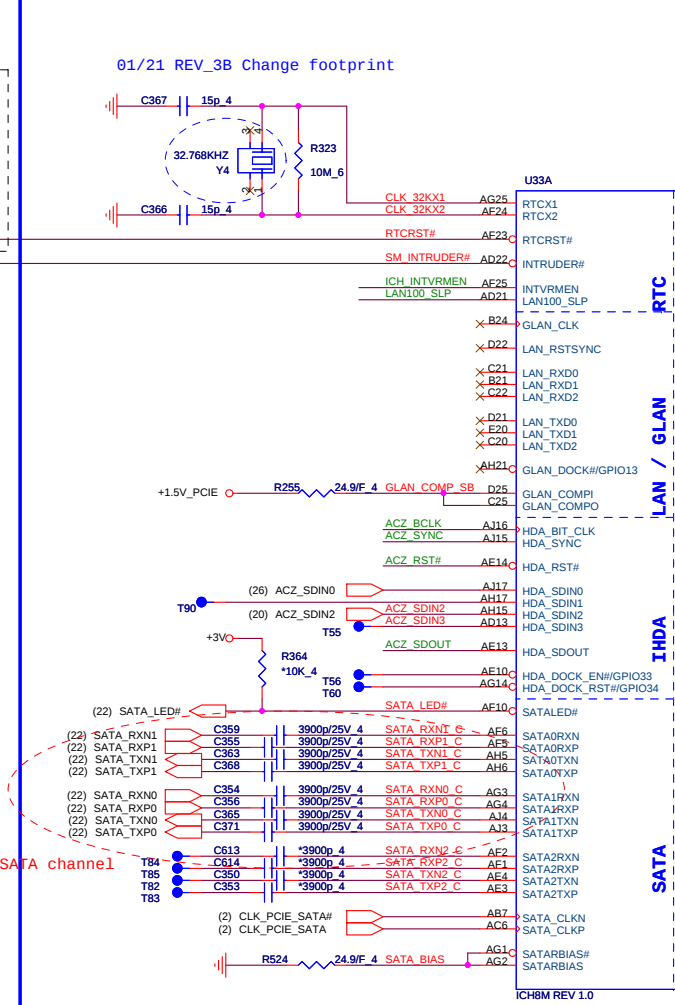
SB Strap

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

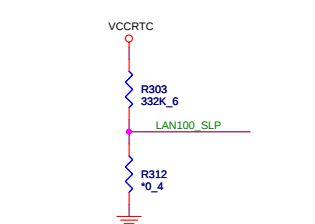


01/21 REV_3B Change footprint



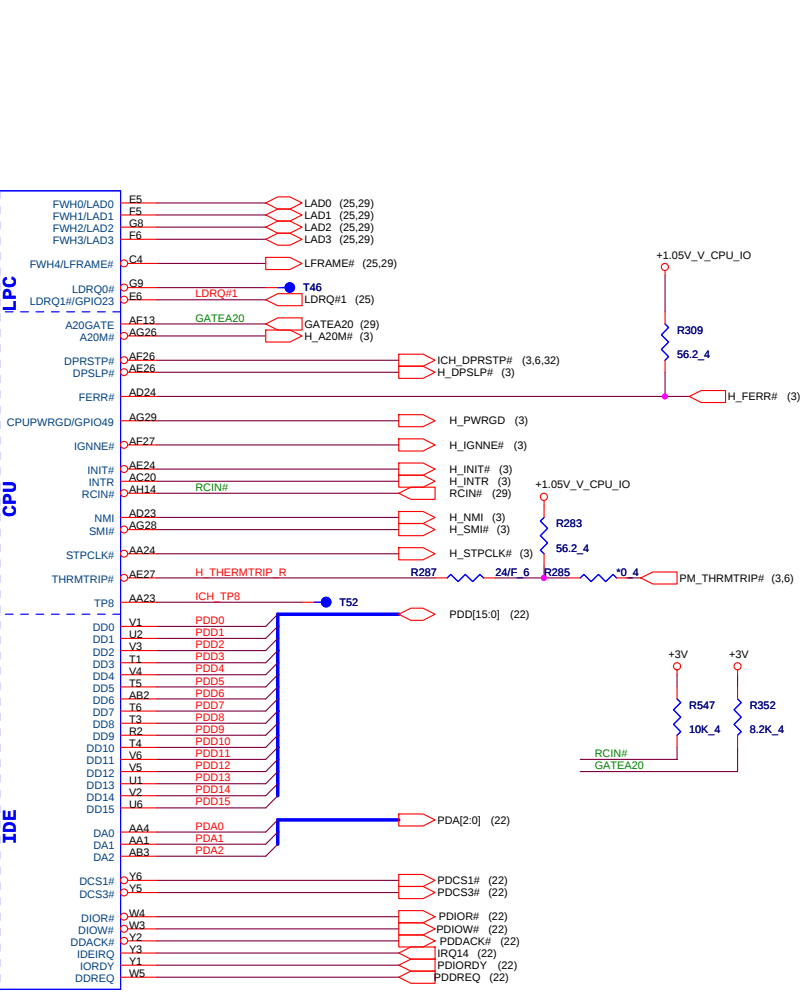
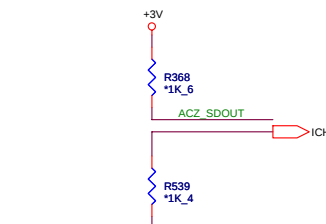
ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

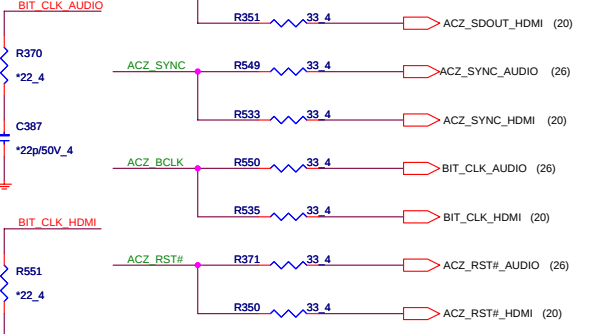


XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1



HDA





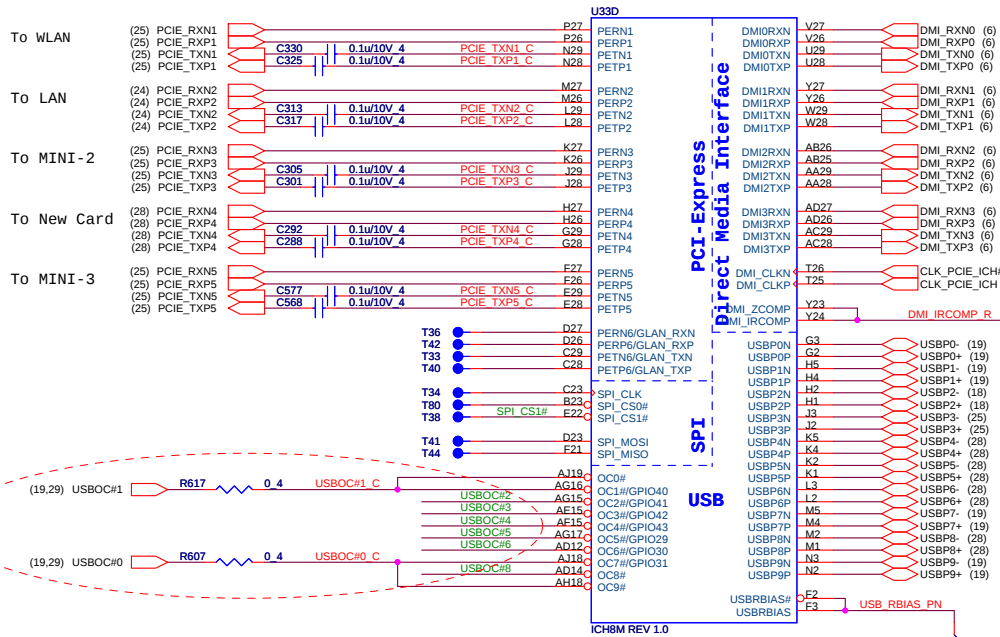
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size Document Number
ICH8M HOST(1 of 4)

Date: Tuesday, January 22, 2008 Sheet 14 of 37

Rev 1A

SB-PCIE/USB/DMI



PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---



ICH8 Boot BIOS select

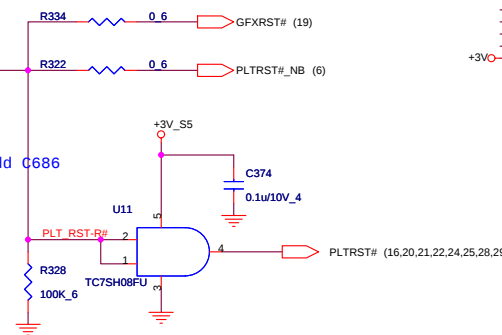
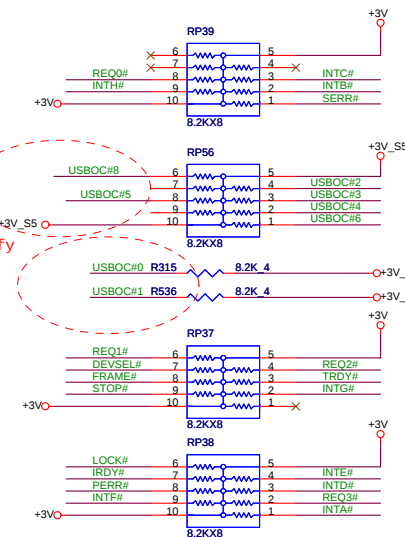
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC



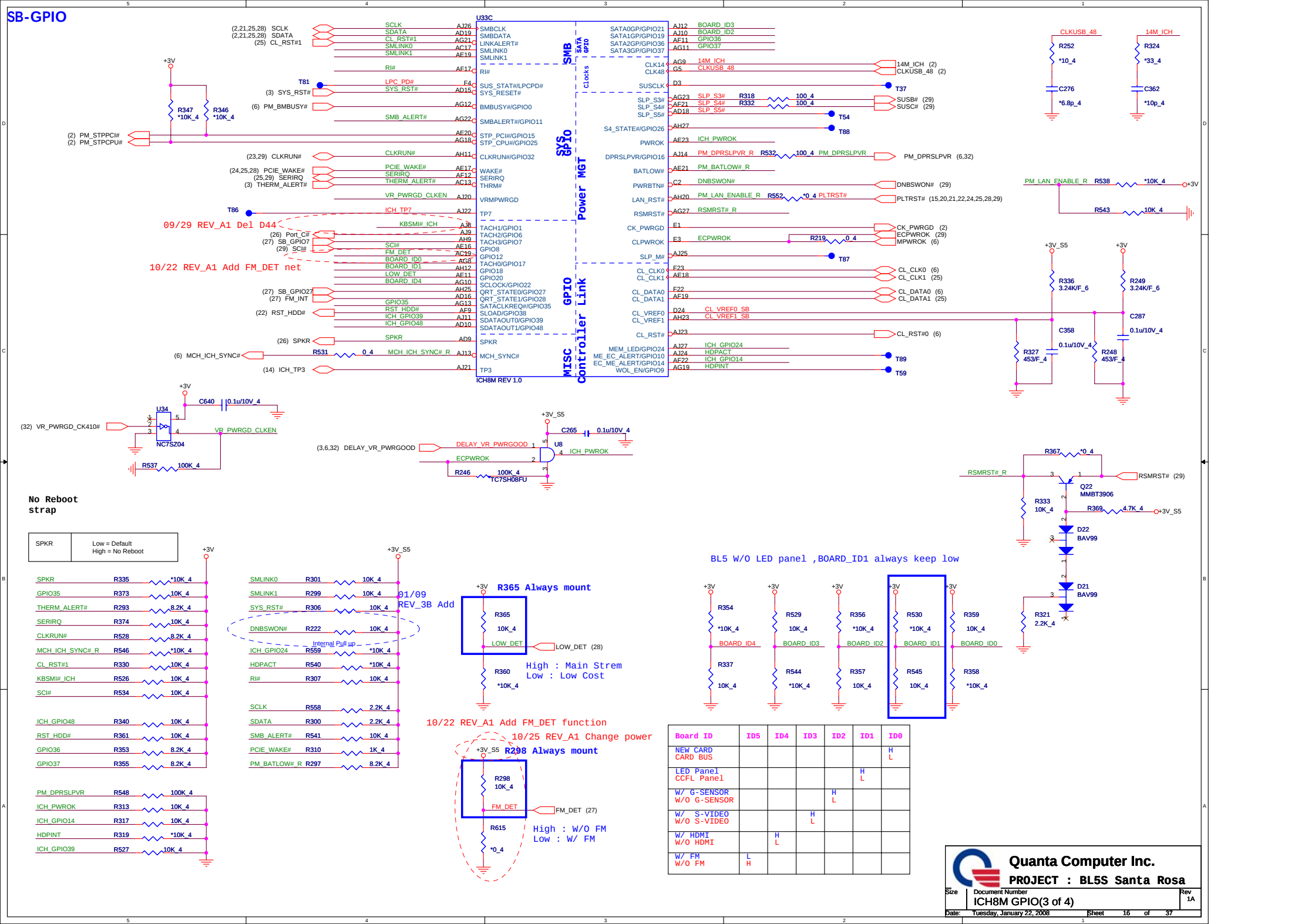
- To USB BOARD
- To USB BOARD
- To Camera
- To WLAN
- To Finger Printer
- To Bluetooth
- To New Card
- To eSATA
- To Felica
- To M/B USB

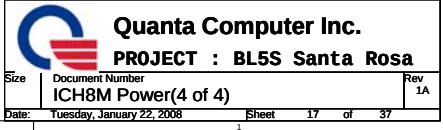
10/26 REV_A1 Modify

09/20 REV_A1 Modify

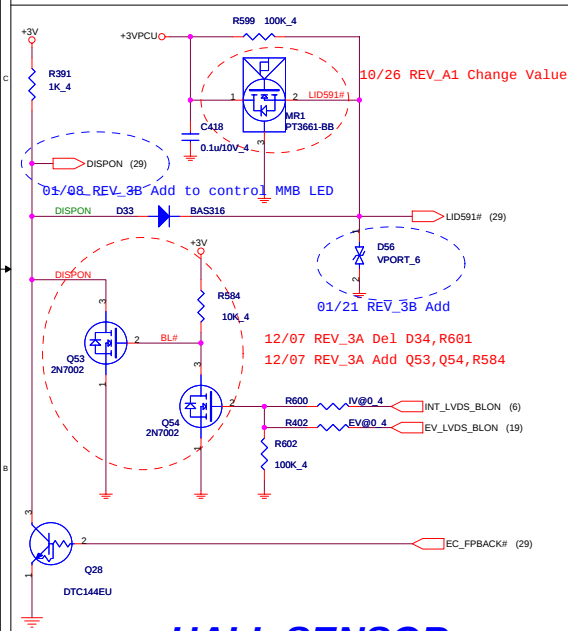
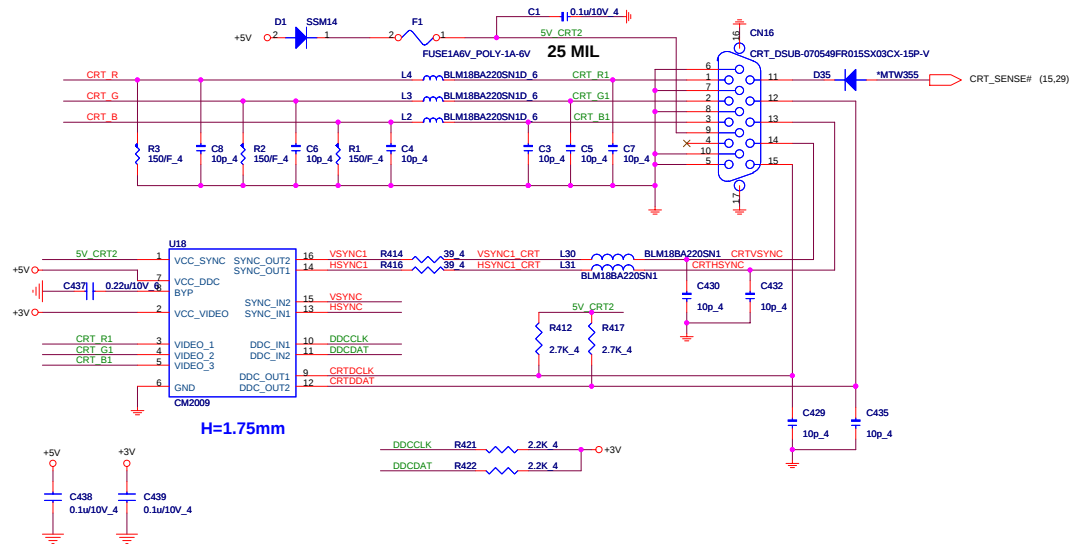
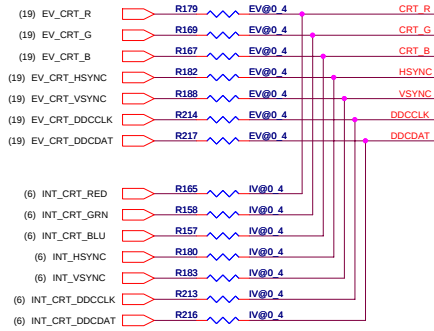


SB-GPIO



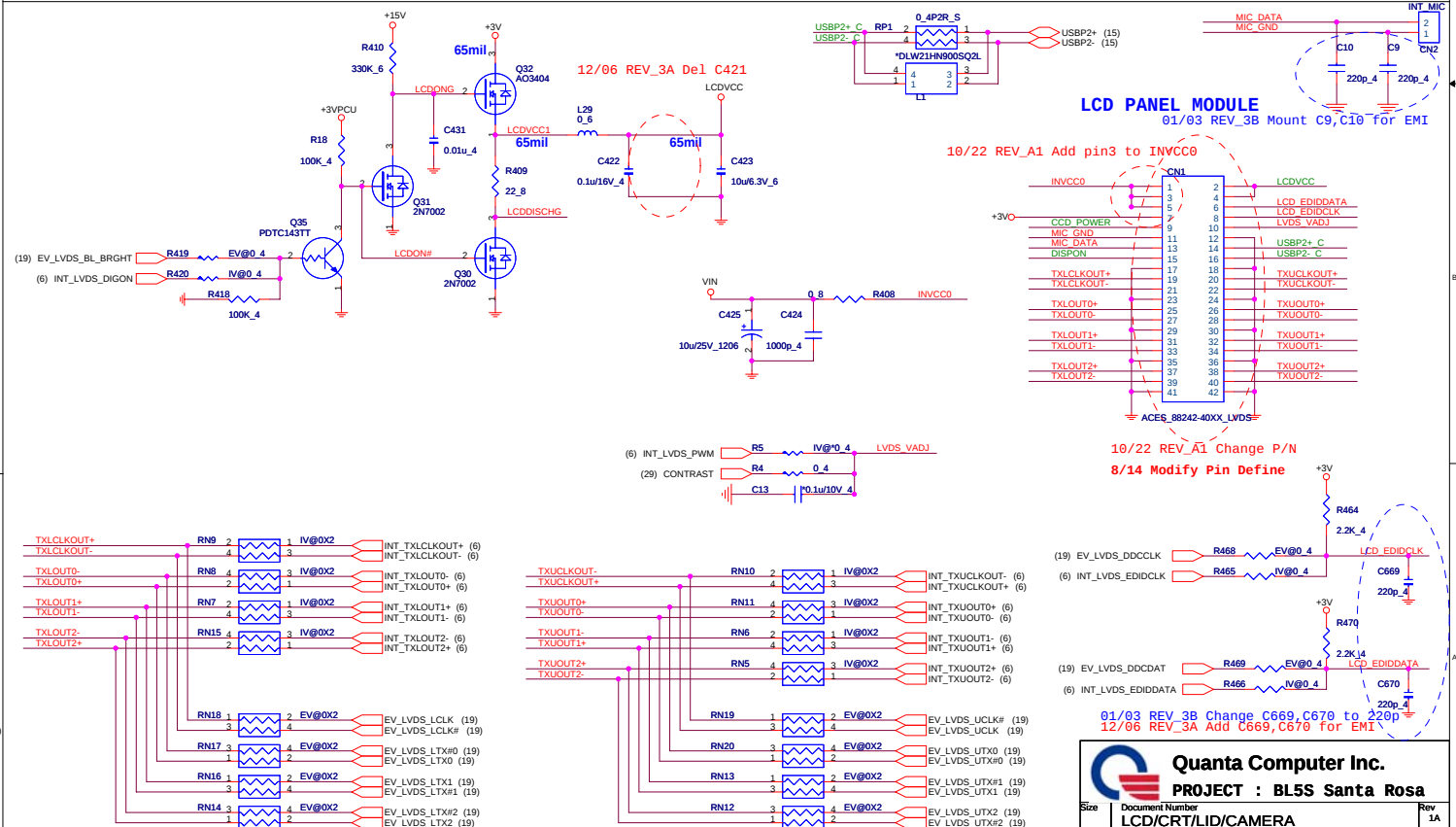
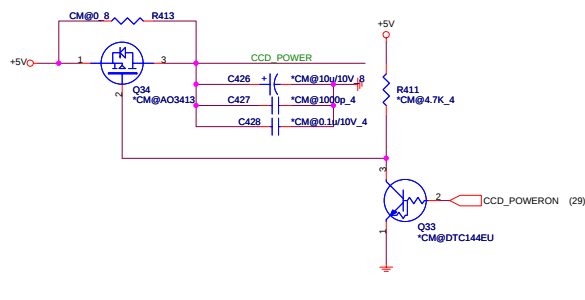


CRT PORT

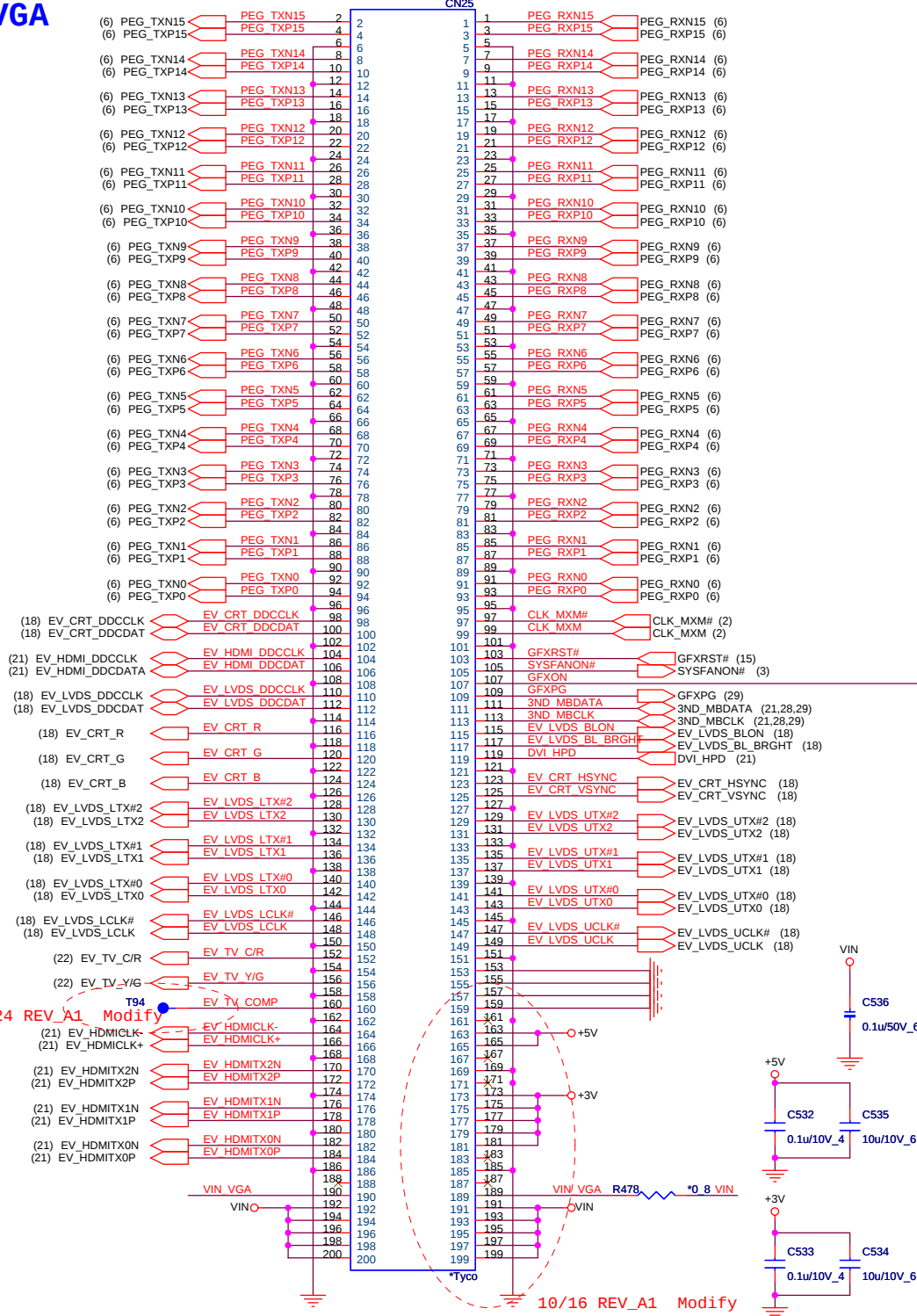


HALL SENSOR

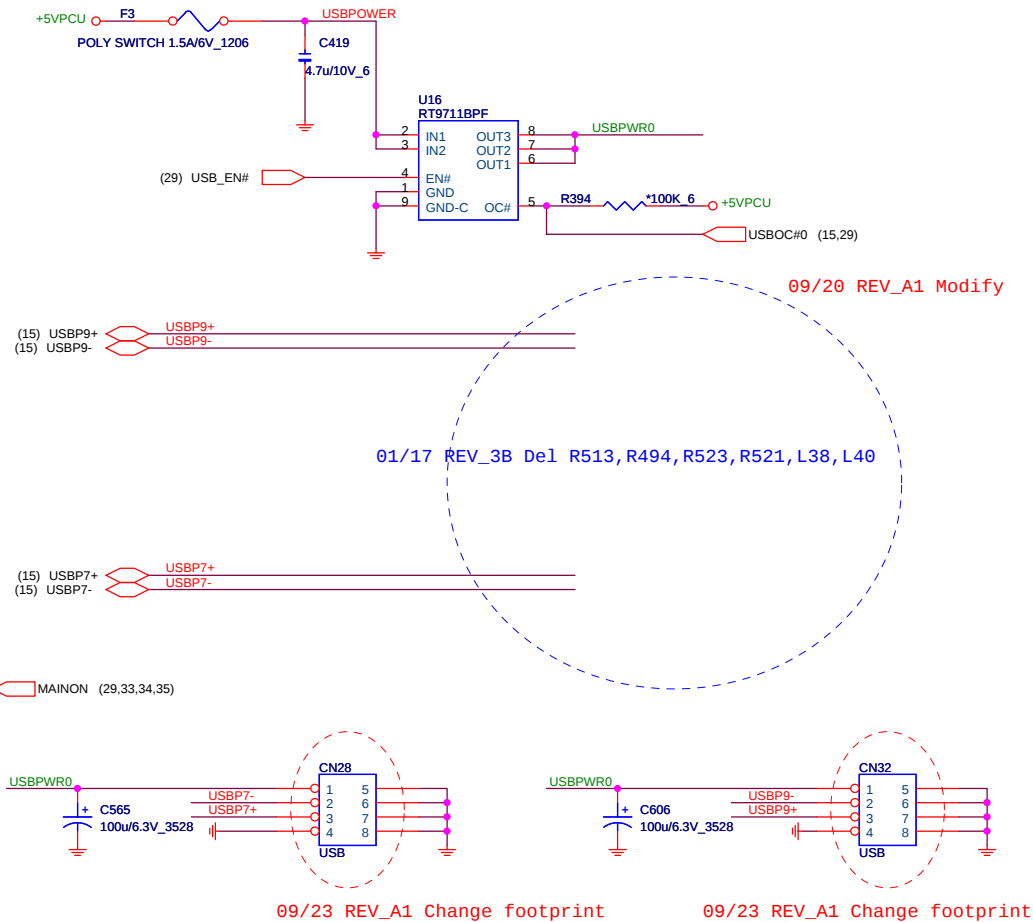
CAMERA MODULE



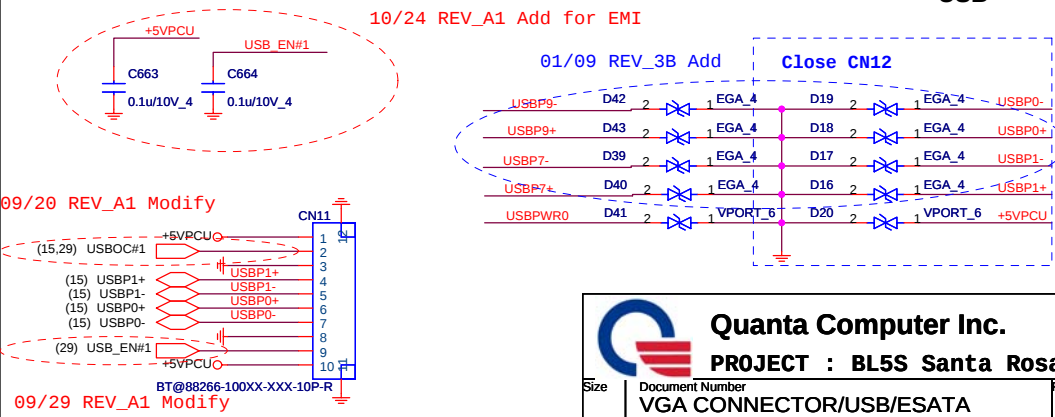
VGA



USB



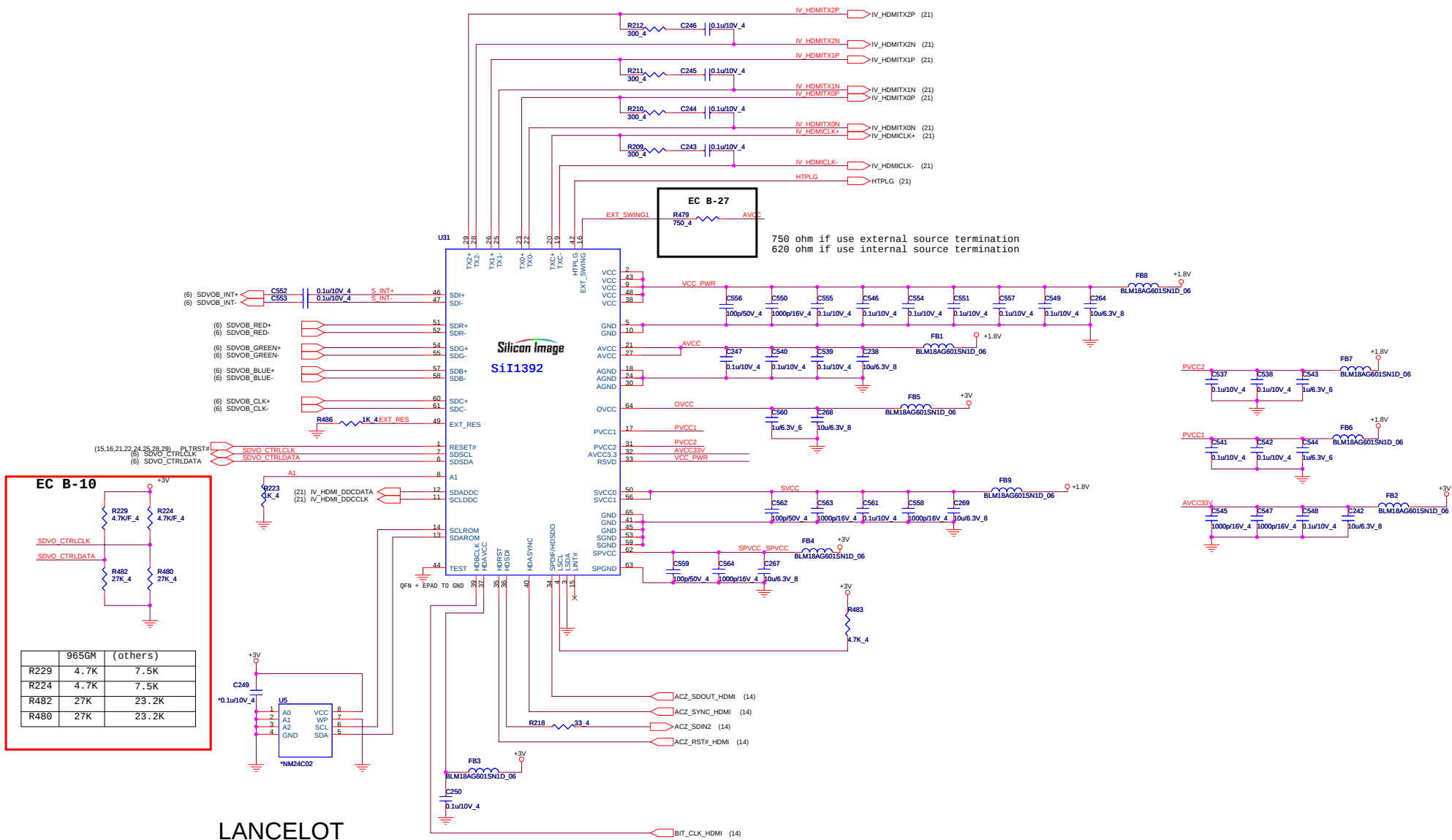
USB board connector



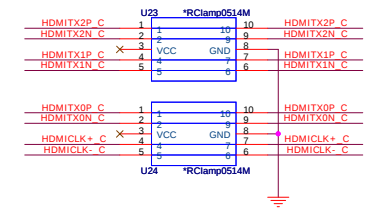
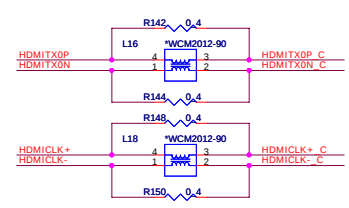
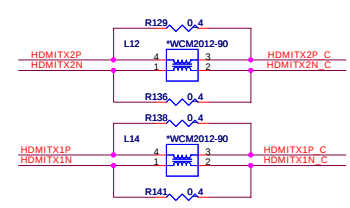
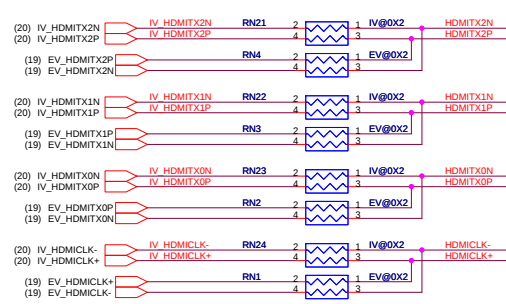
SiI1392 HDMI TX

LAYOUT RULES:

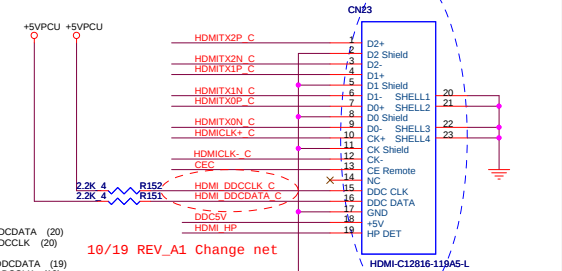
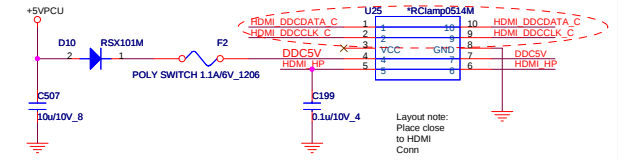
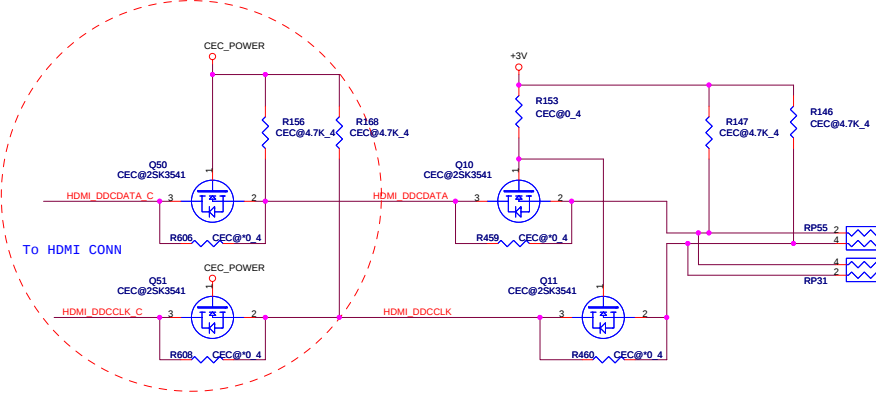
Route traces with 100 Ohm Differential Impedance
Avoid placing GND Copper or traces adjacent to TMDS Trace
Put these 4 resistors and 4 capacitors as close as possible
to the TMDS output pins of the Sil392



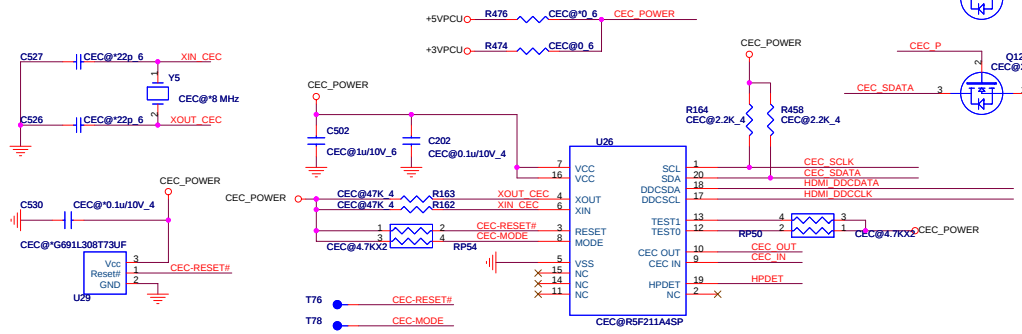
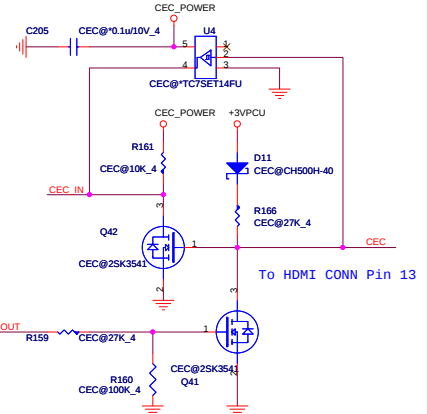
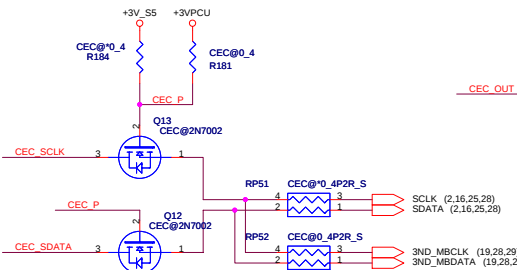
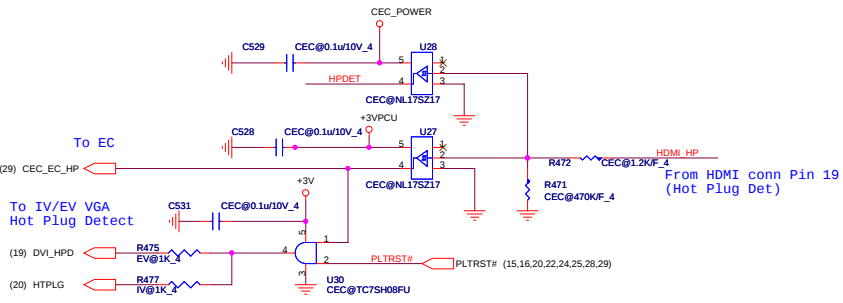
LANCELOT



10/19 REV_A1 Add Q50, Q51, R156, R168, R606, R608

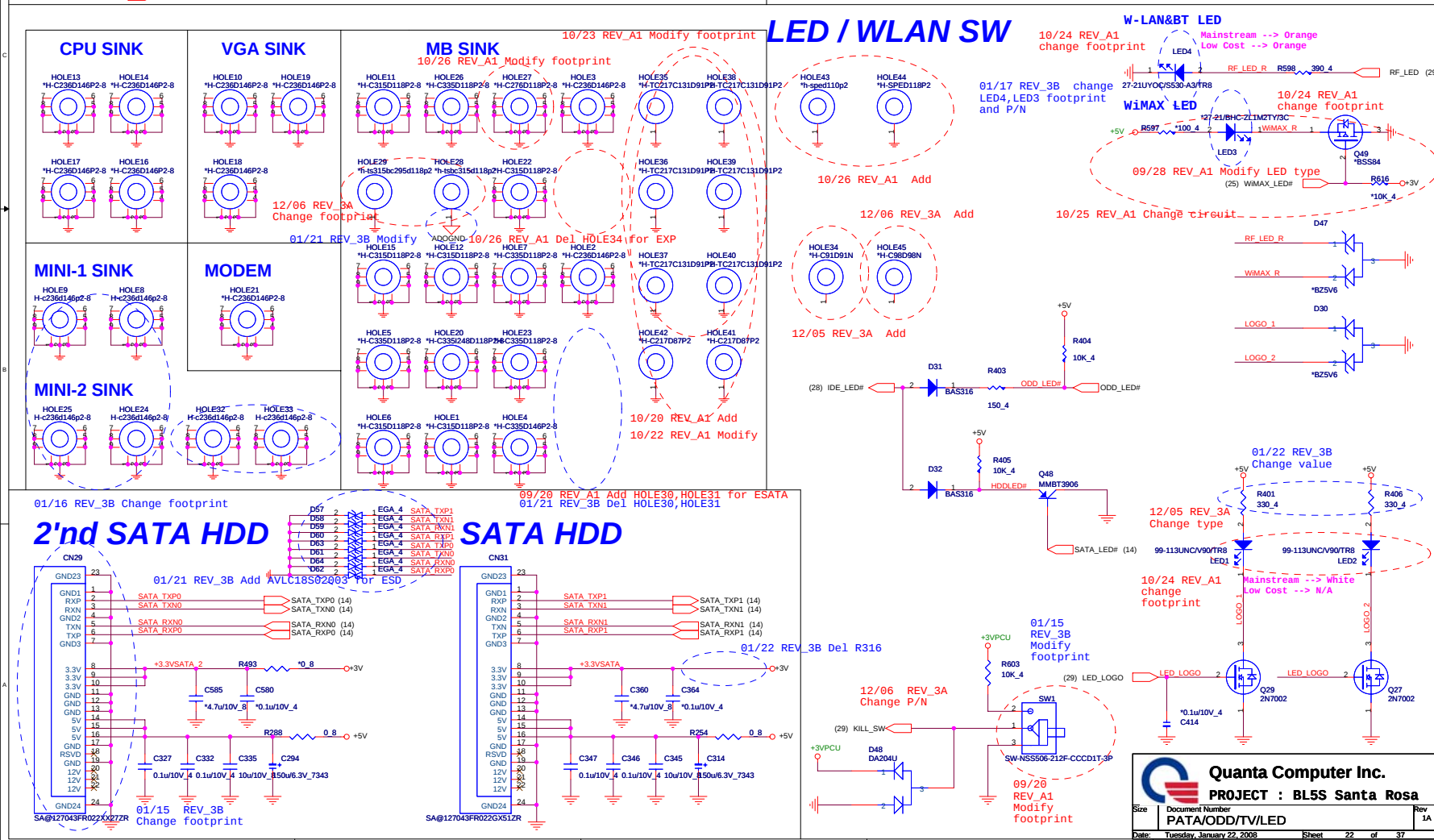
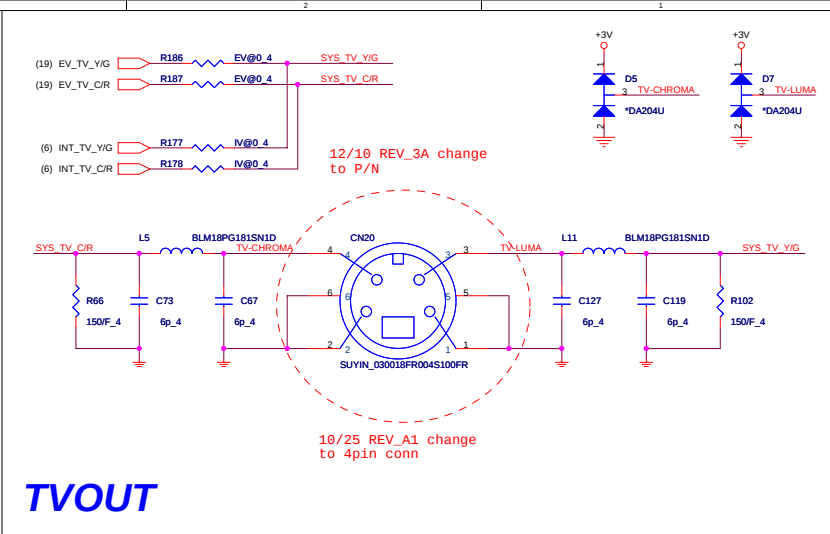
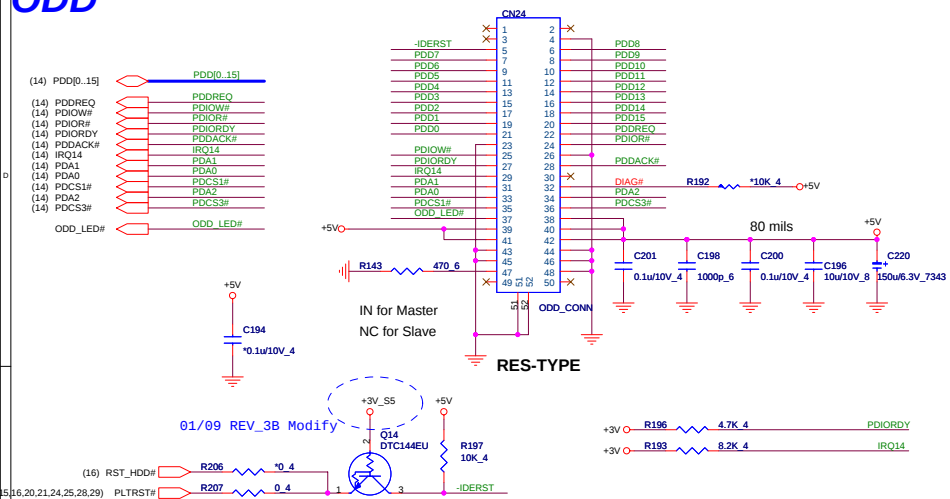


10/19 REV_A1 Change net
01/09 REV_3B Change footprint
10/19 REV_A1 Change footprint
12/07 REV_3A Change footprint



To SB
To EC

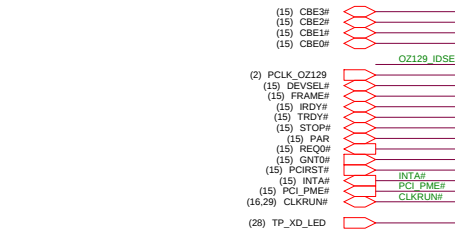
ODD



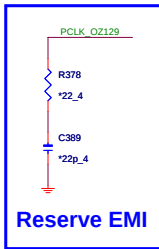
MMC



The 100ohm is that reduce the notice form PCI signal

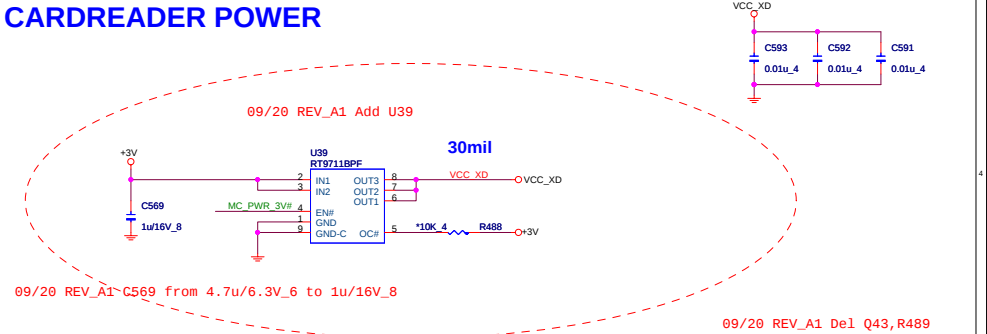


MEDIA_LED: 1=Enable MEDIA_LED activity(Default)

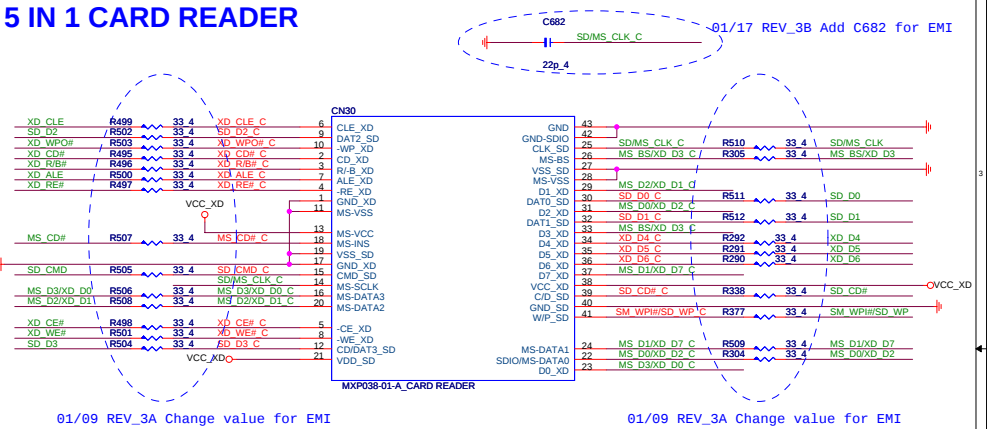


A B C D E

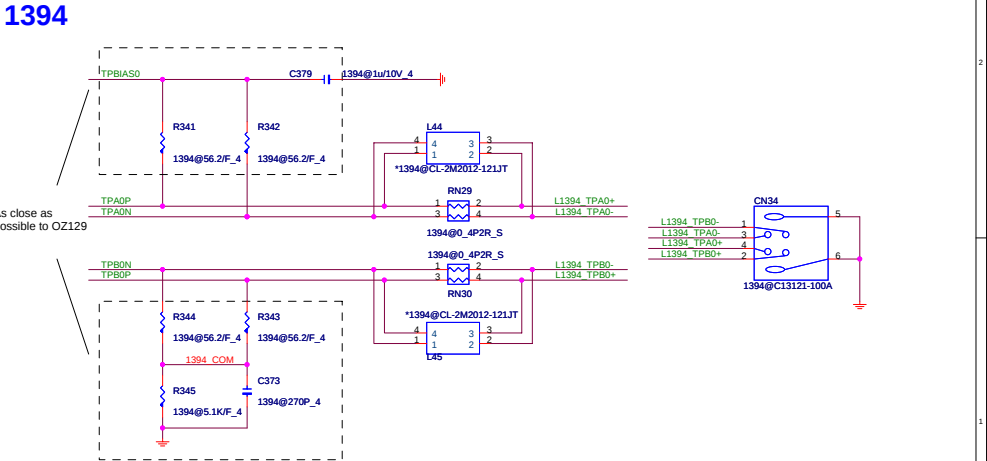
CARDREADER POWER



5 IN 1 CARD READER

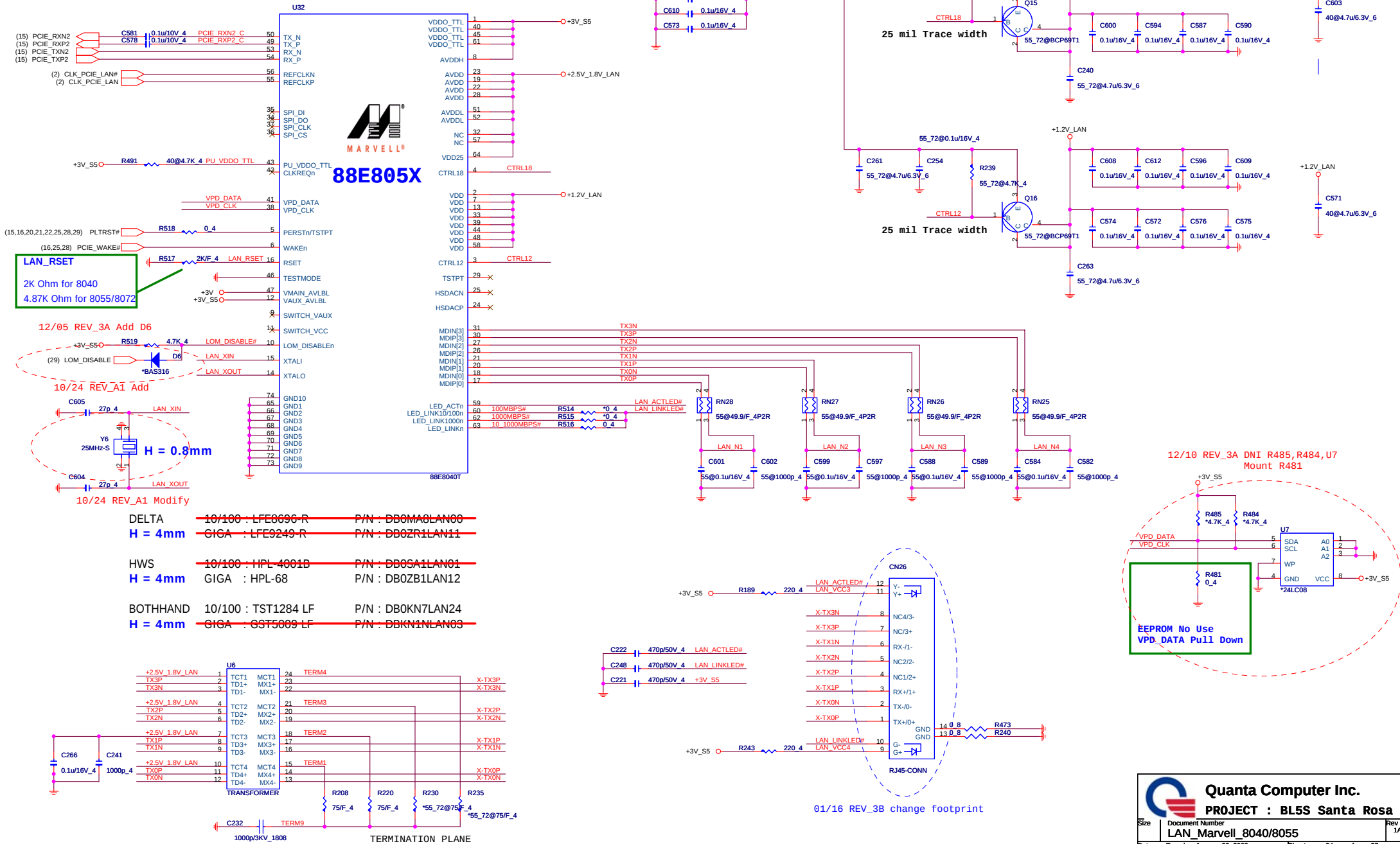


1394



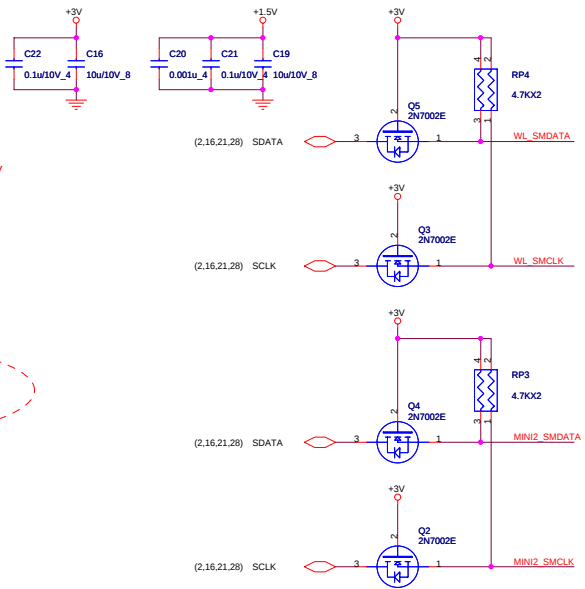
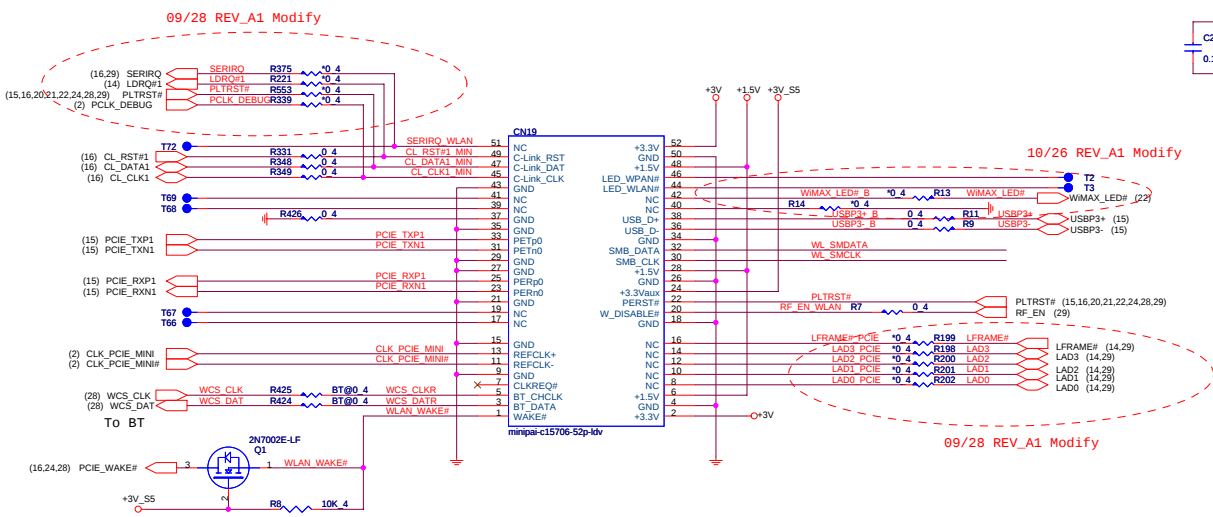
LAN_MARVELL_88E8040/88E8055/88E8072

10/100 : 88E8040	P/N : AL008040001
GIGA : 88E8055	P/N : AJ080550000
GIGA : 88E8072	P/N : AL008072000

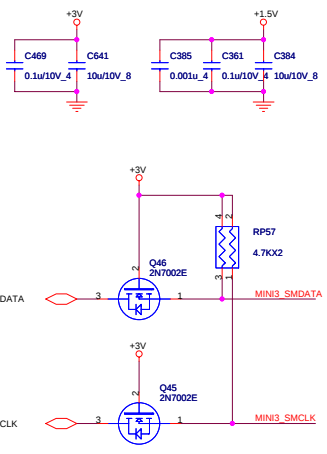
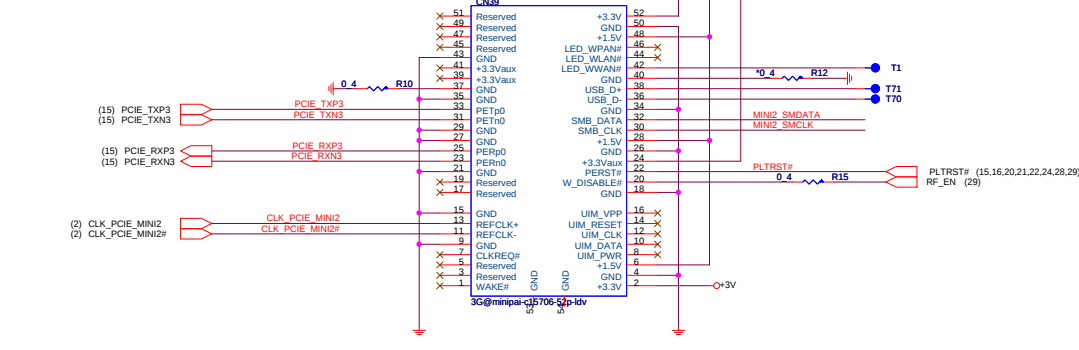
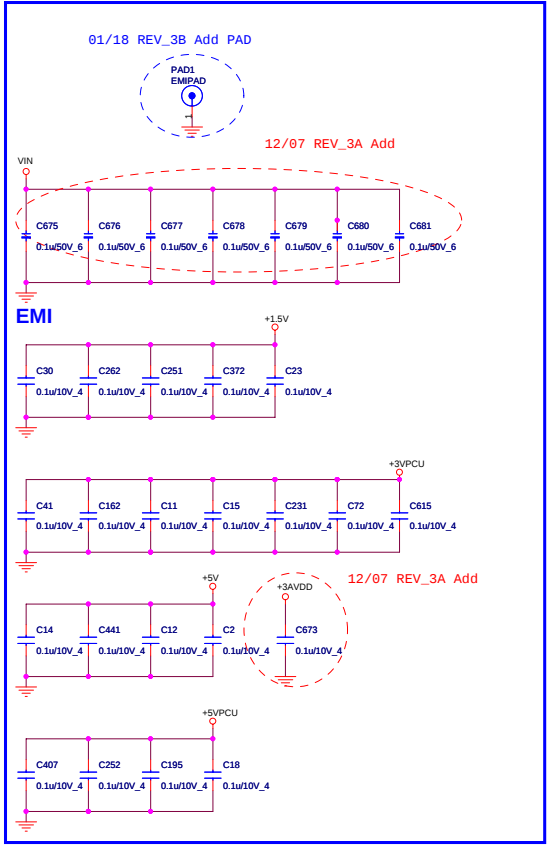


Mini PCI-E Card WLAN

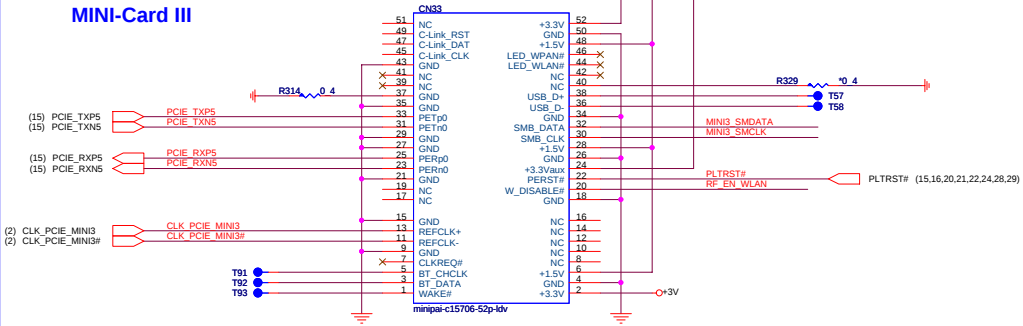
MINI-Card I



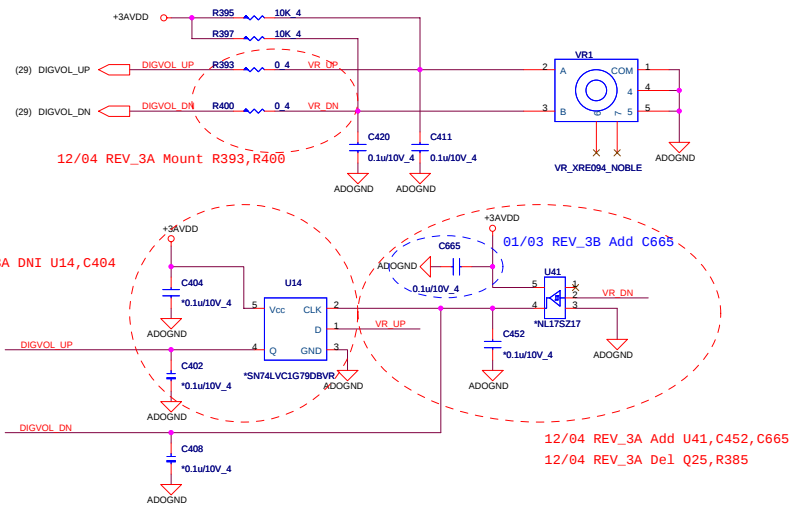
MINI-Card II



MINI-Card III

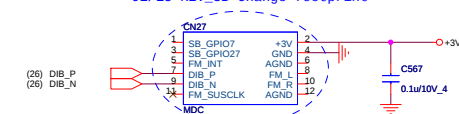


VR

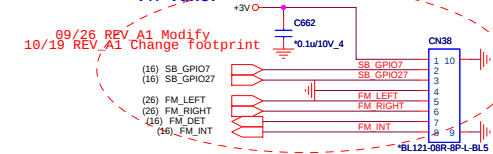


MDC

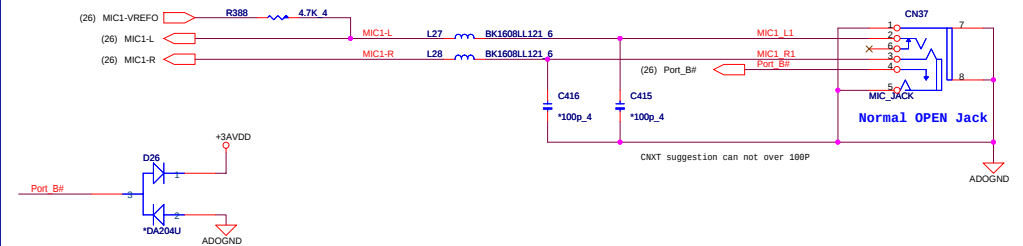
01/15 REV_3B Change footprint



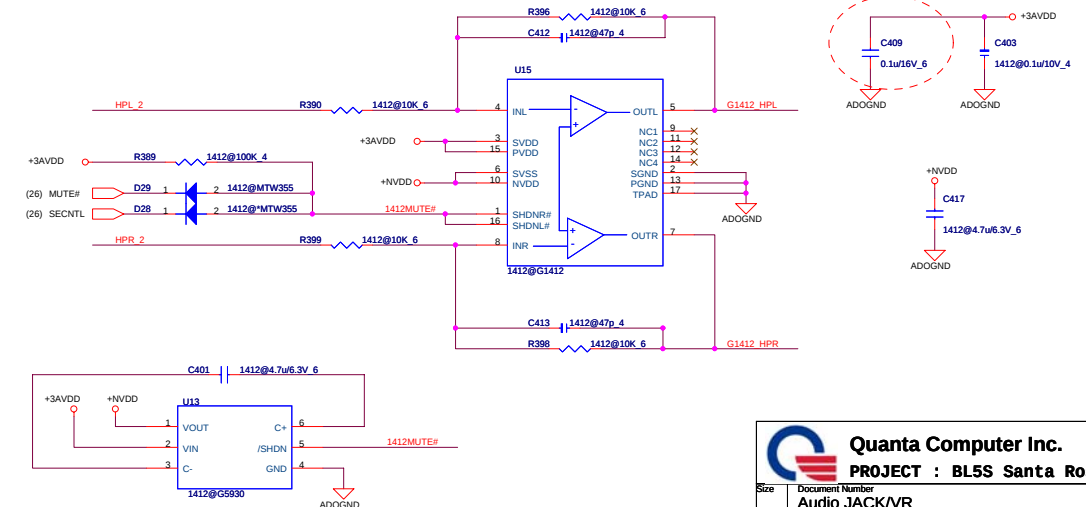
FM Tuner

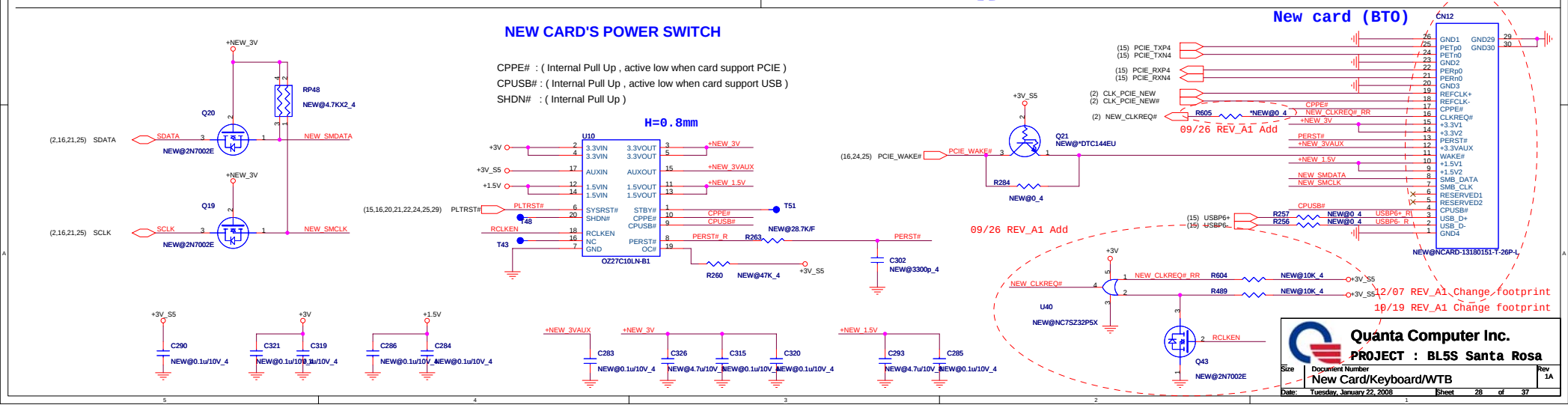
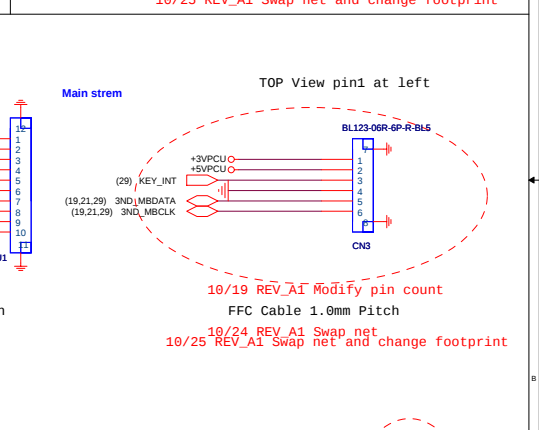
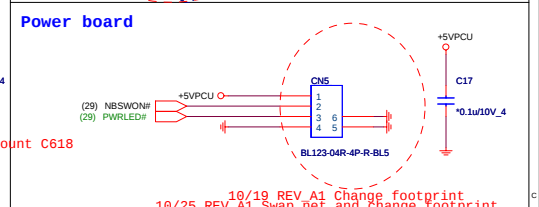
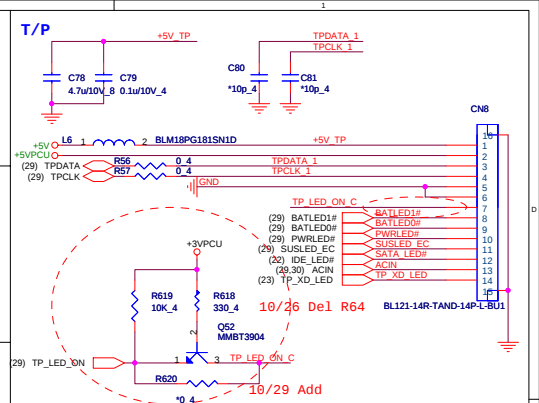


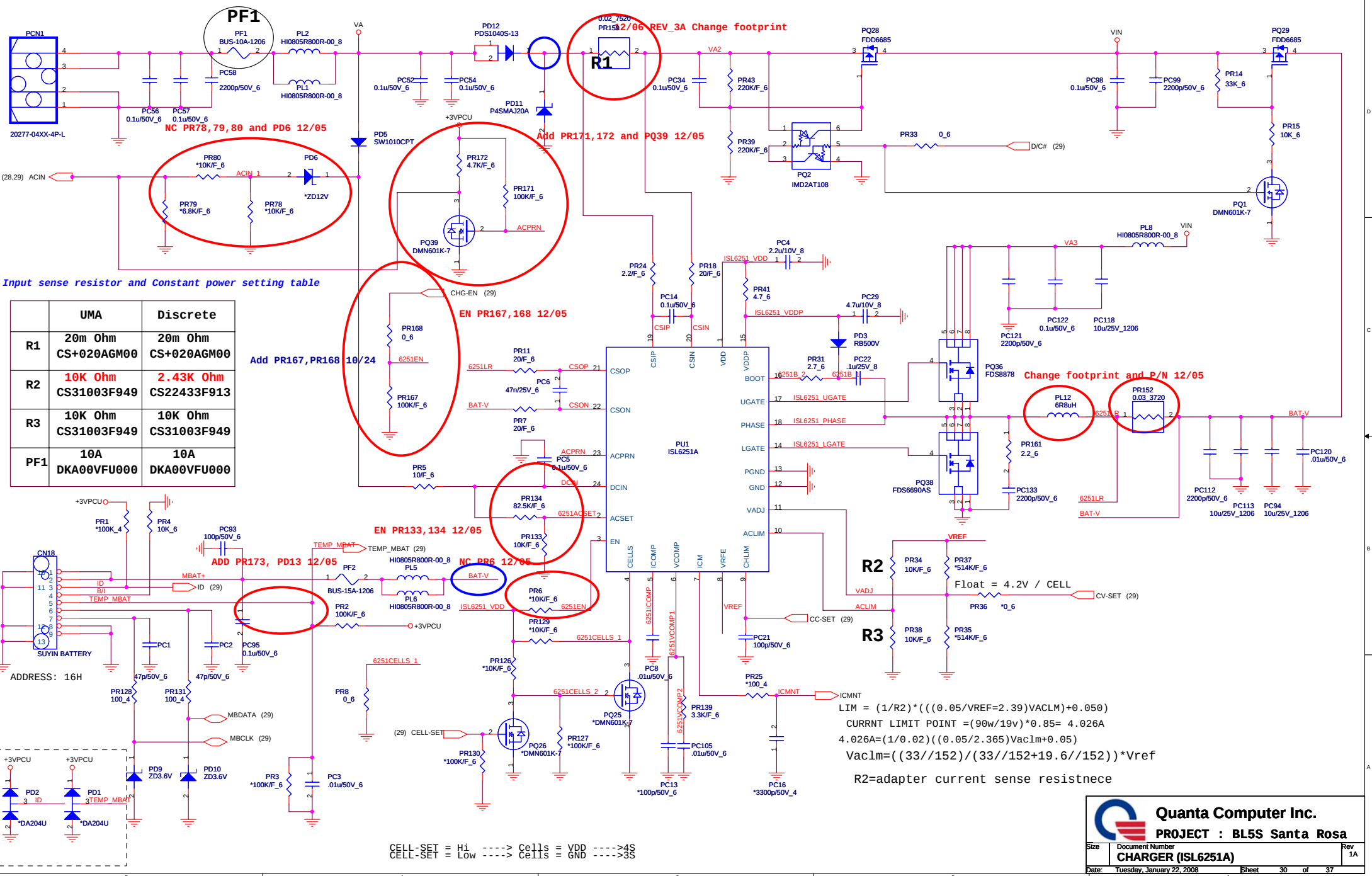
SYSTEM MIC

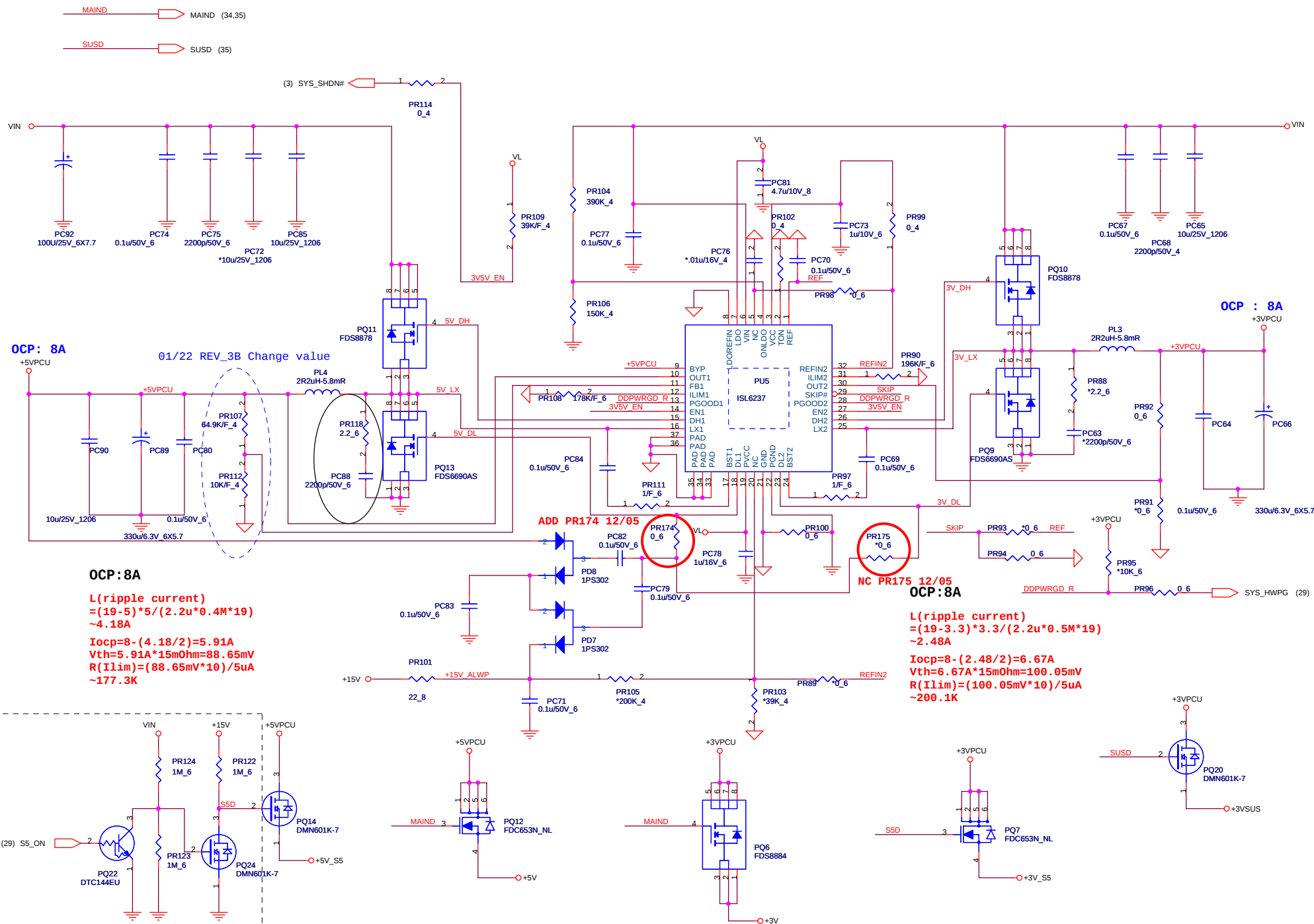


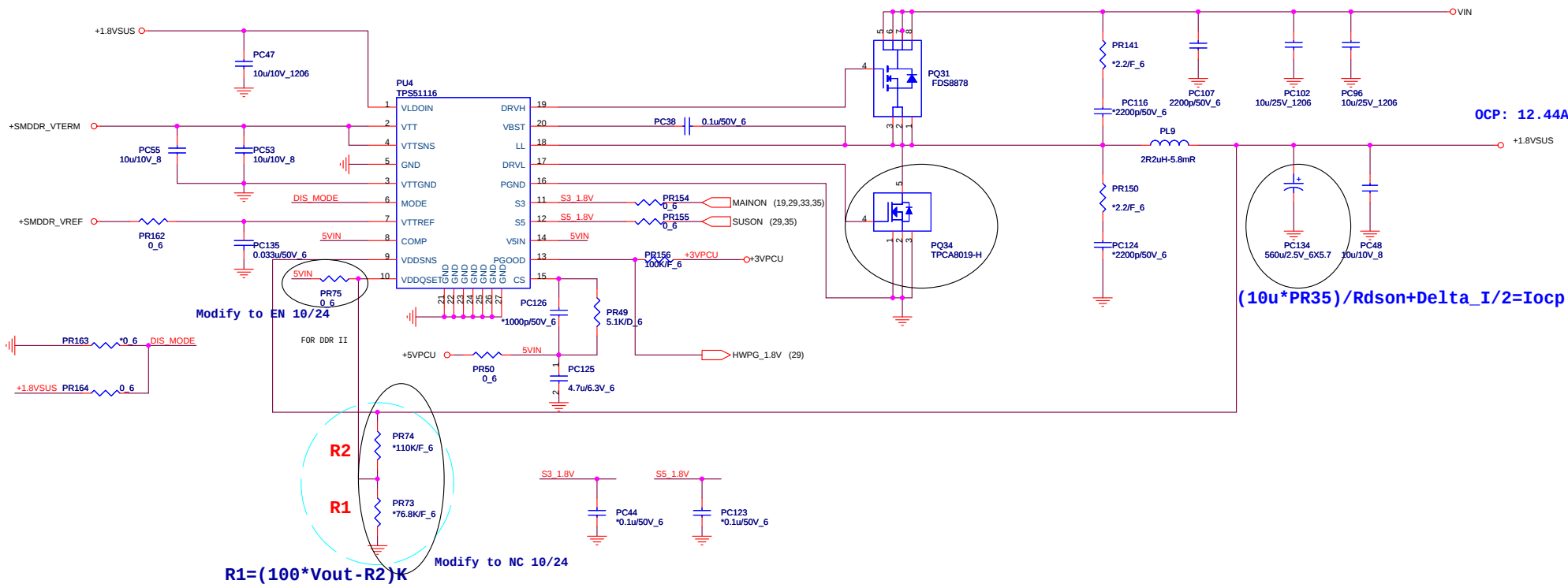
HP Amplifier



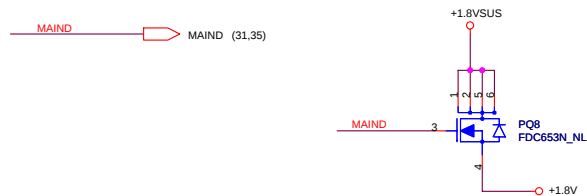


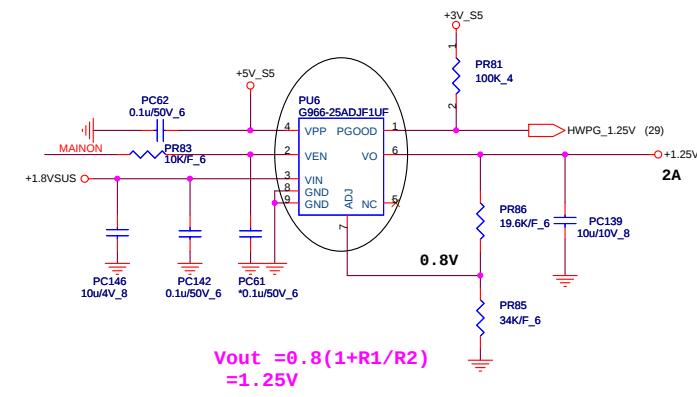
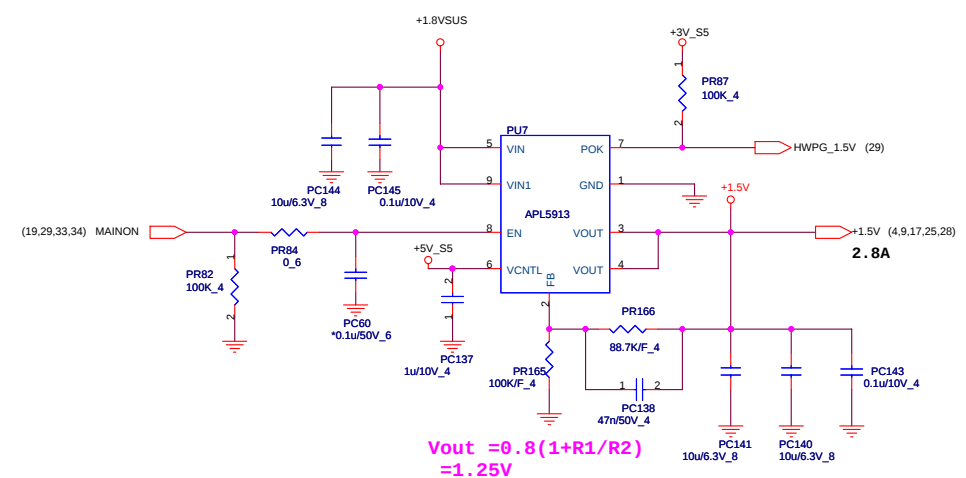
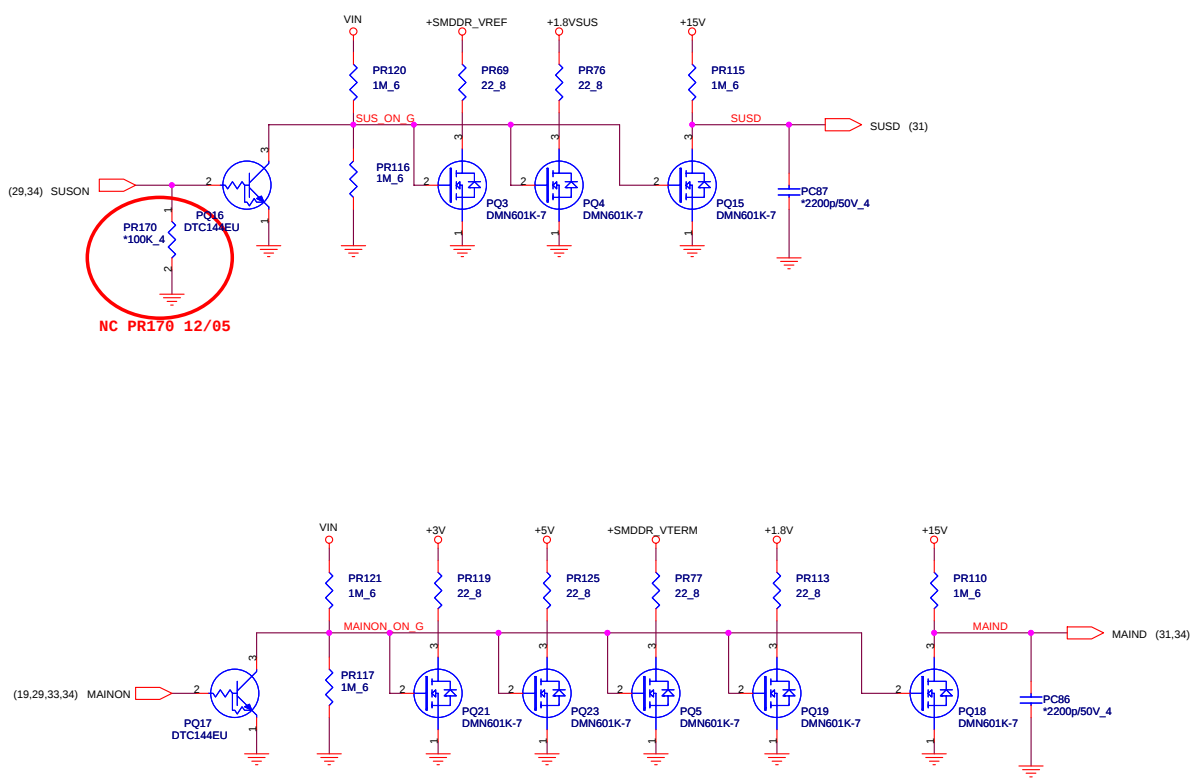


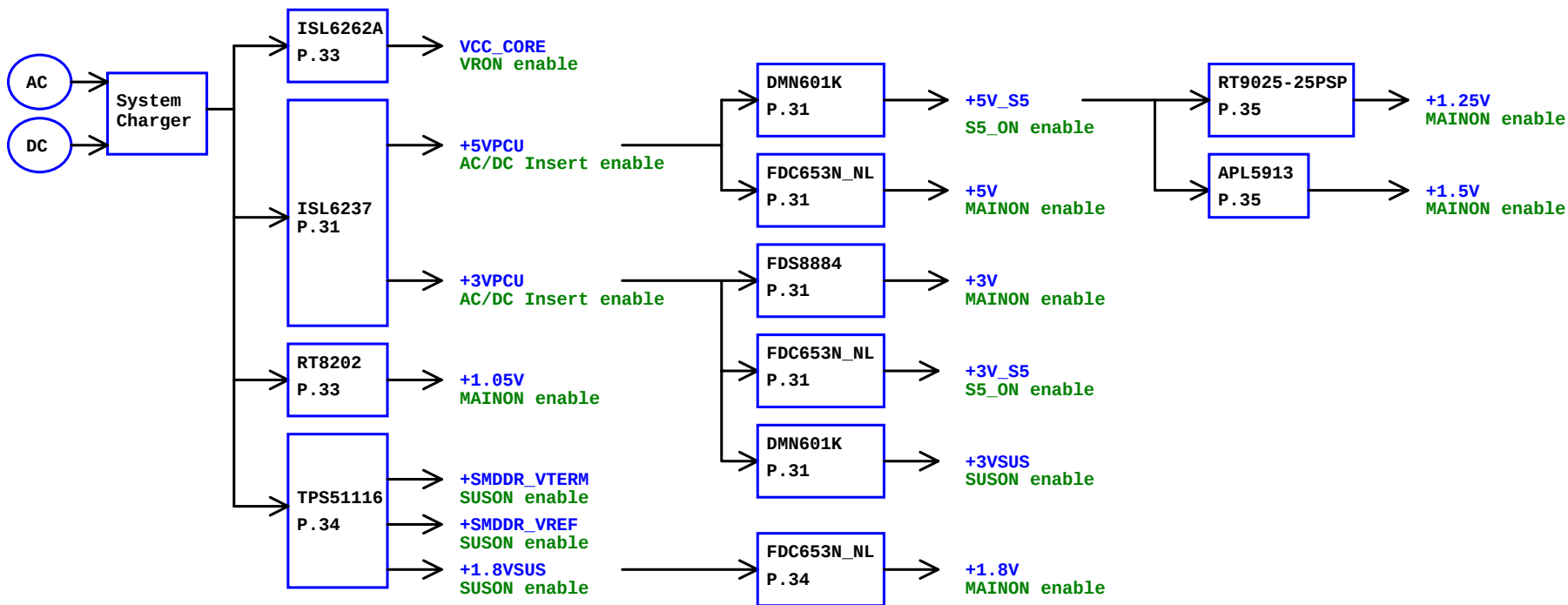




if tune Vout PR38 un-mount, PR156 PR165 mount







Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M