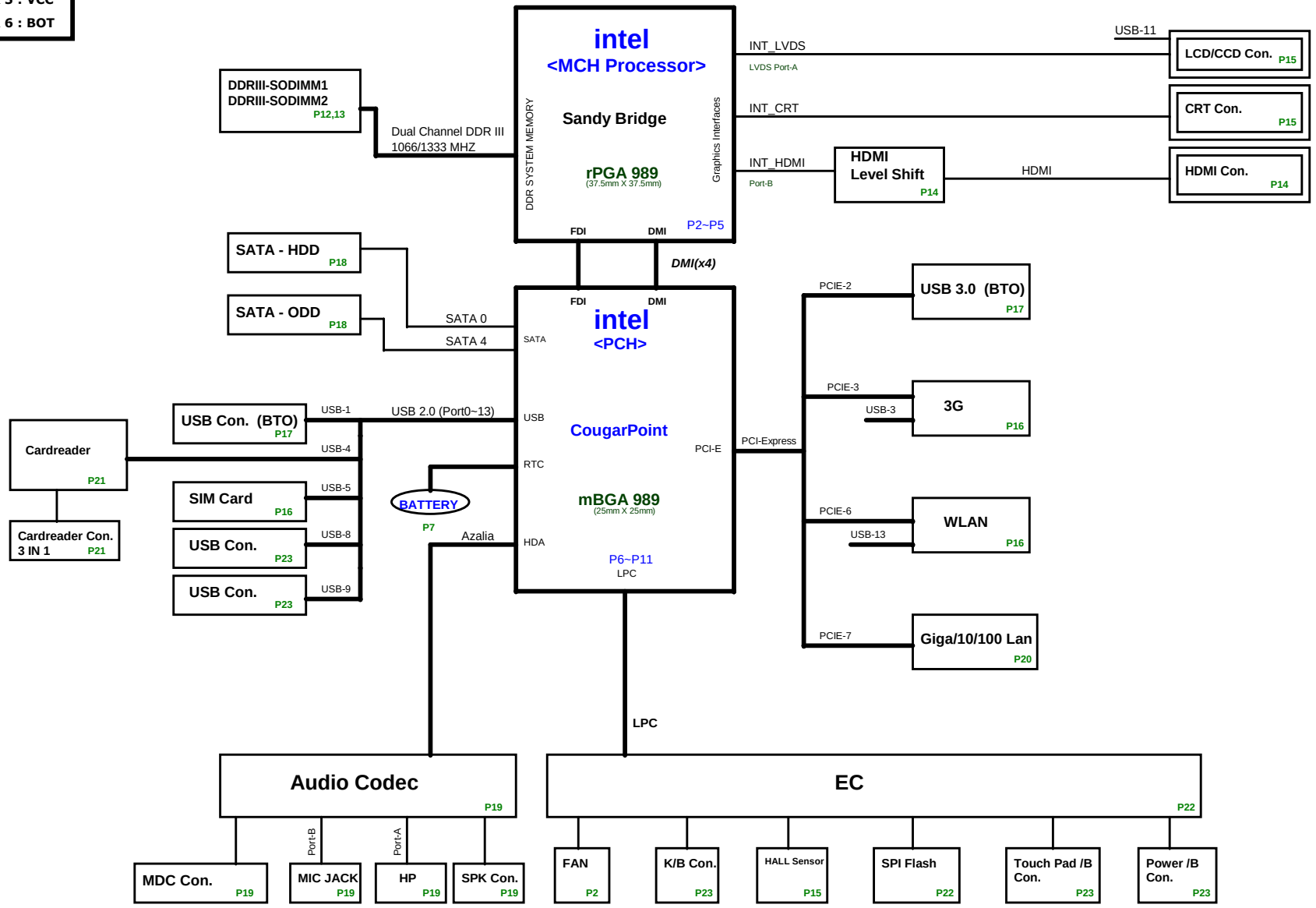
BLB Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



POWER SYSTEM

ISL88731CHRTZ-T	P.25
ISL95835HRTZ-T	P.30
RT8207LGQW	P.27
RT8240BGQW	P.28
G9661-25ADJF12U	P.31
PM6686TR	P.26
ISL95870AHRUZ-T	P.29

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF
+VGPU_CORE
+VAXG
+VCCSA

Quanta Computer Inc.
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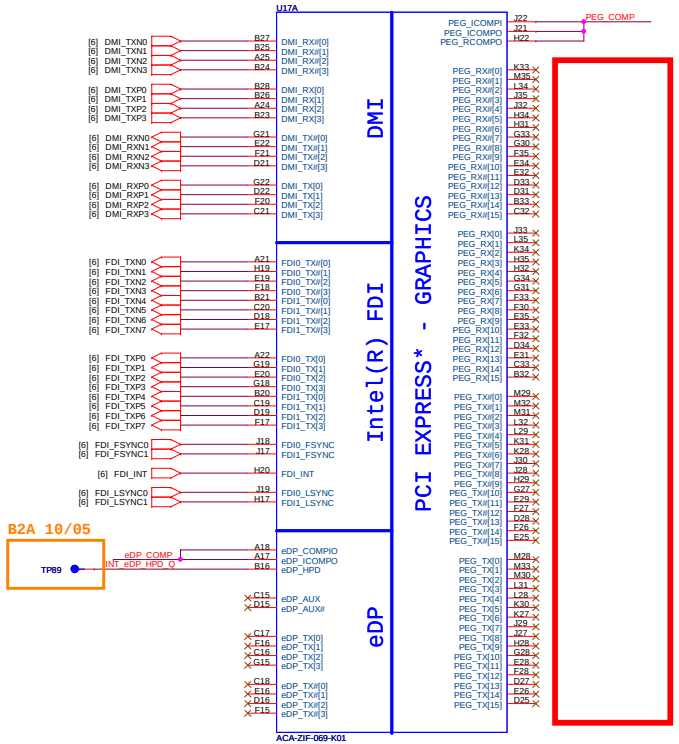
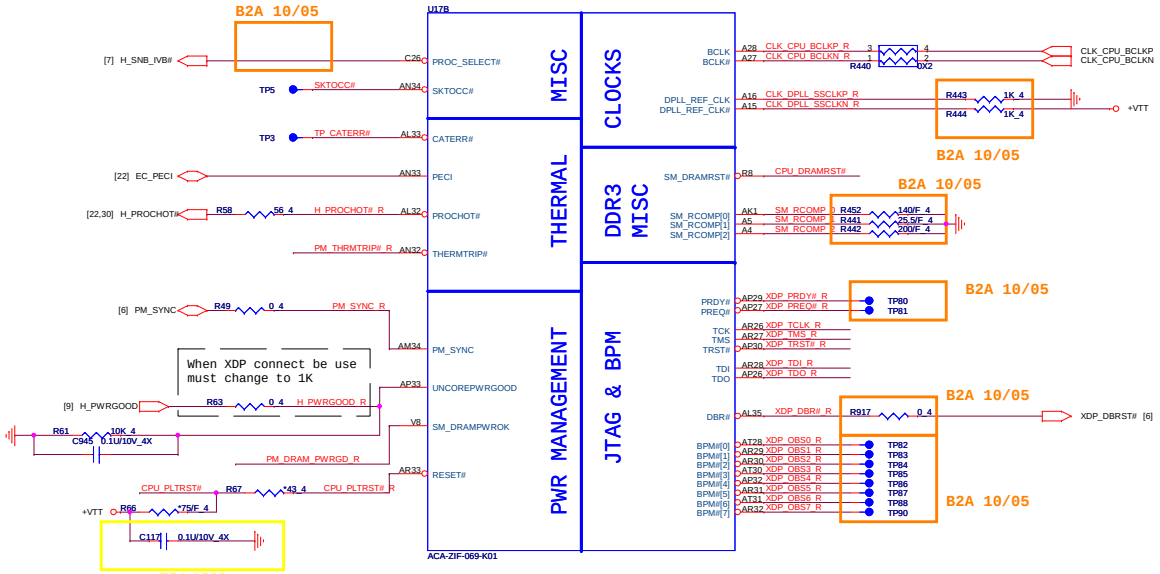
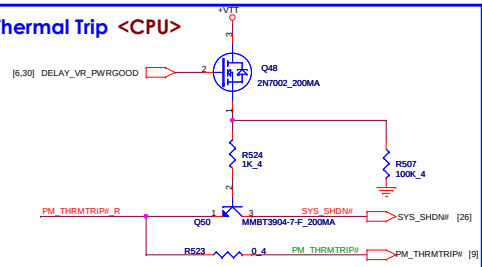
Sandy Bridge Processor (DMI,PEG,FDI) <CPU>



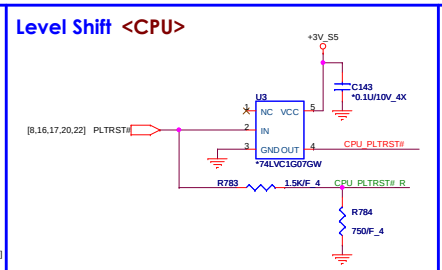
Sandy Bridge Processor (CLK,MISC,JTAG) <CPU>



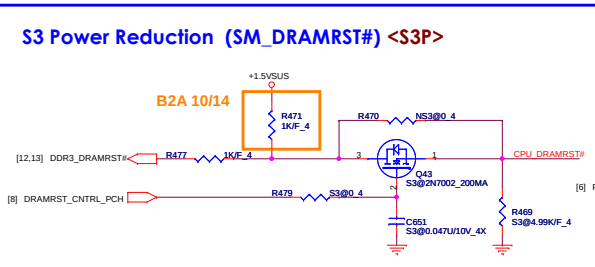
Thermal Trip <CPU>



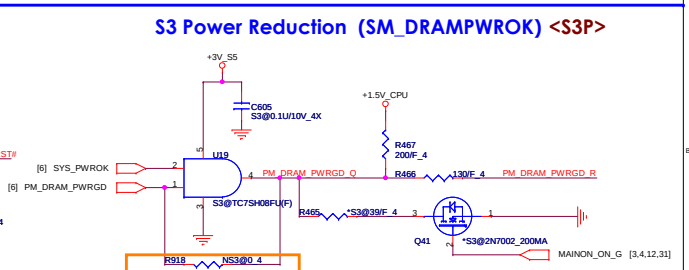
Level Shift <CPU>



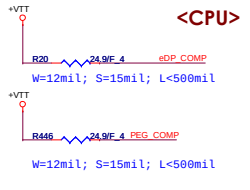
S3 Power Reduction (SM_DRAMRST#) <S3P>



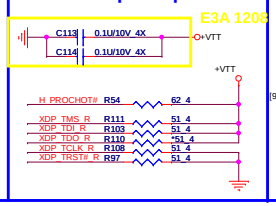
S3 Power Reduction (SM_DRAMPWROK) <S3P>



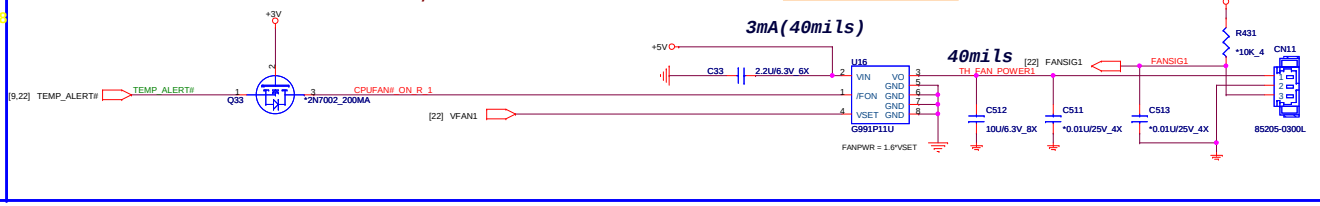
DP & PEG Compensation <CPU>



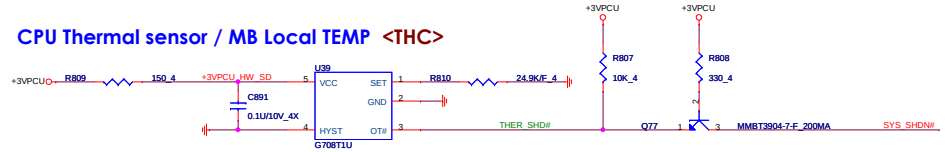
Processor pull-up <CPU>



FAN Control-->For one FAN solution <THC/THV>



CPU Thermal sensor / MB Local TEMP <THC>



Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 86dgree
Hysteresis is 30C

Quanta Computer Inc.			
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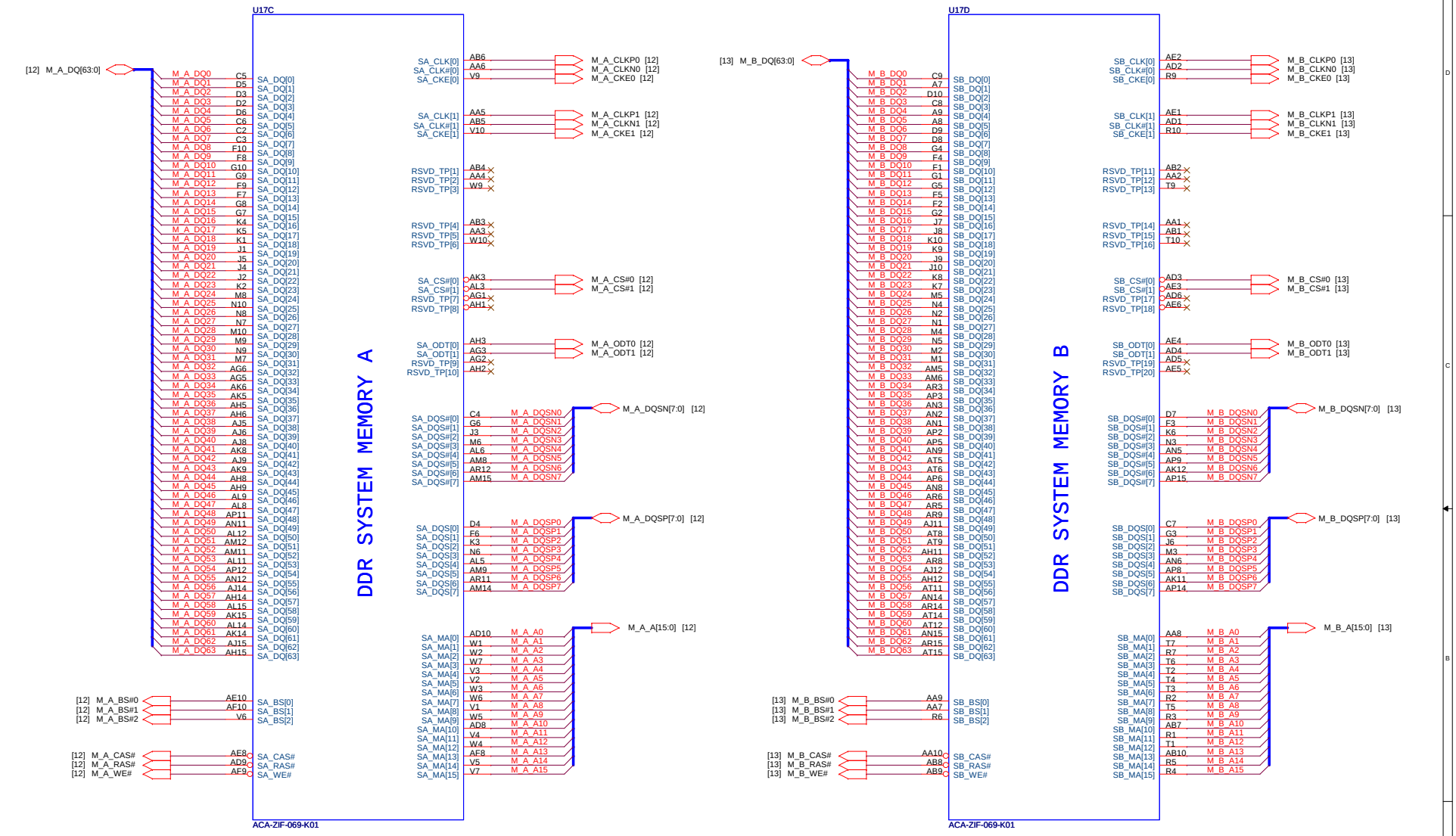
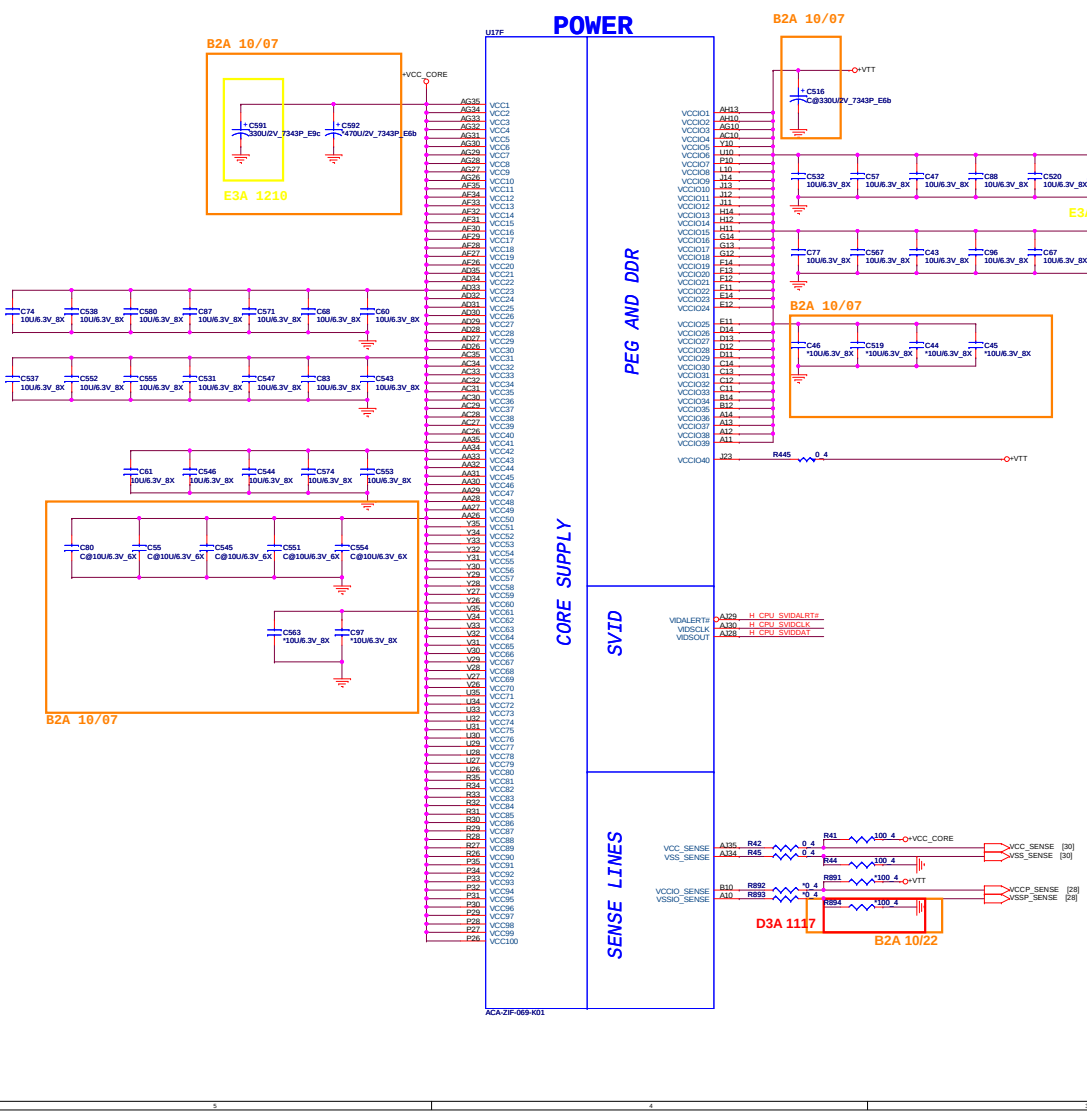
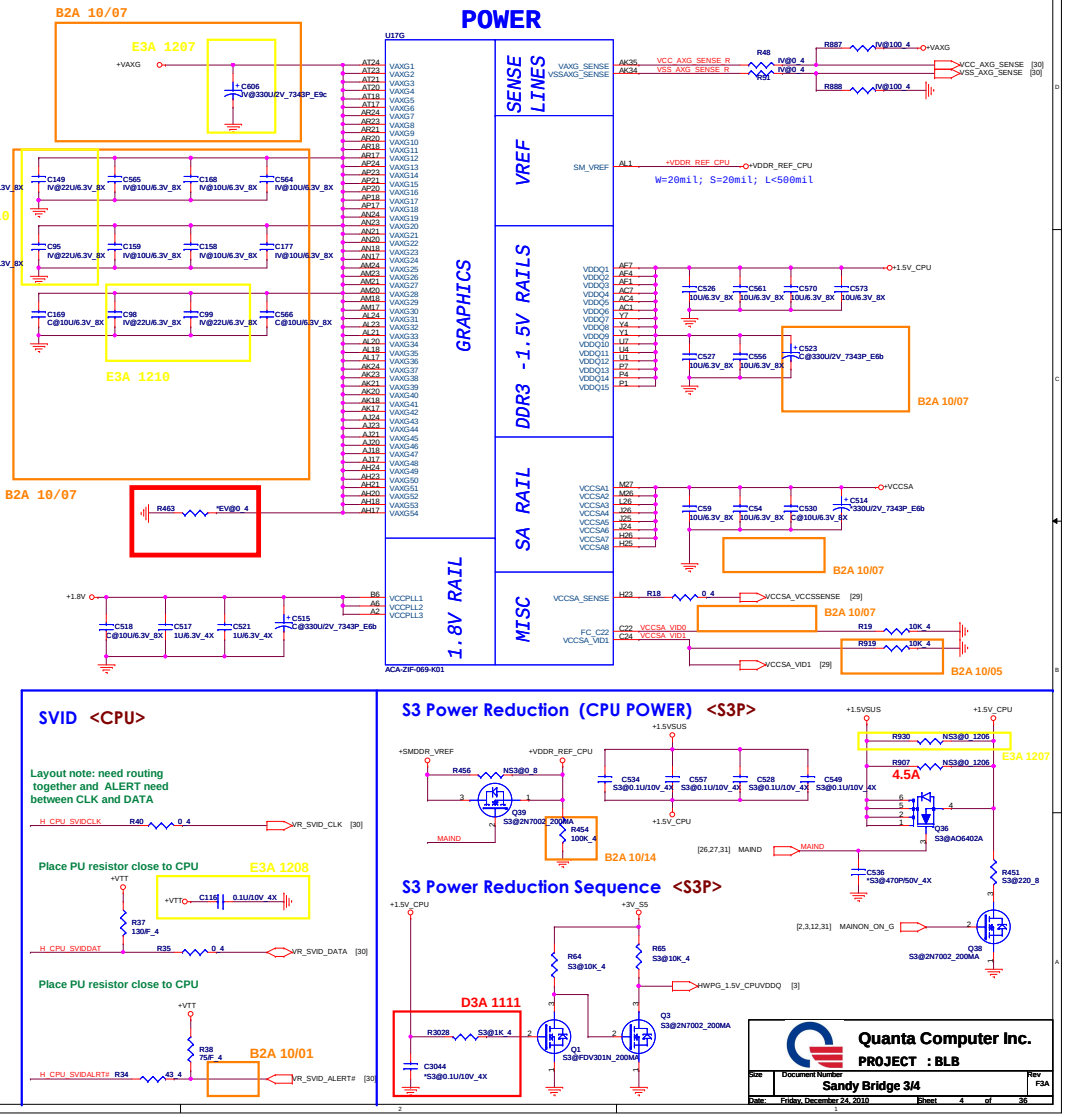
Sandy Bridge Processor (DDR3) <CPU>



Sandy Bridge Processor (POWER) <CPU>



Sandy Bridge Processor (GRAPHIC POWER) <CPU>



SVID <CPU>

S3 Power Reduction (CPU POWER) <S3P>

S3 Power Reduction Sequence <S3P>

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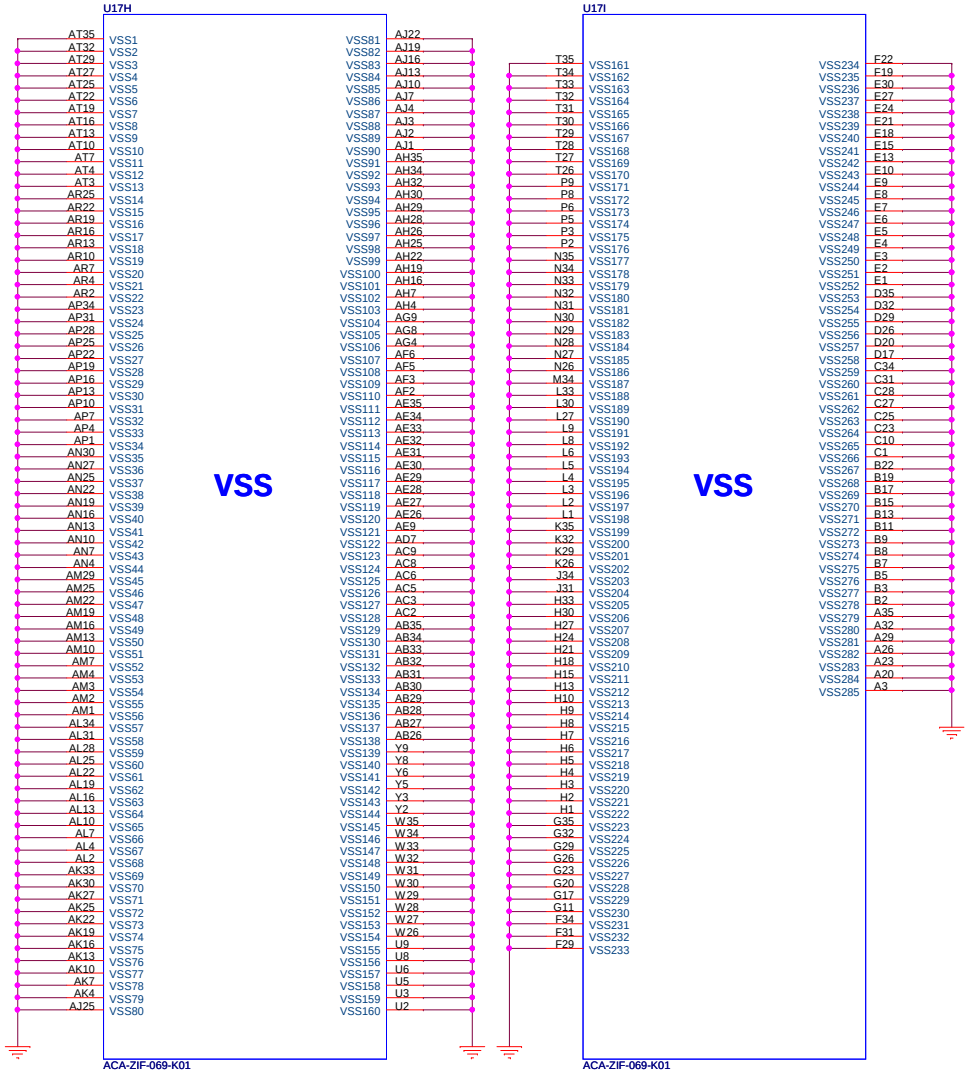
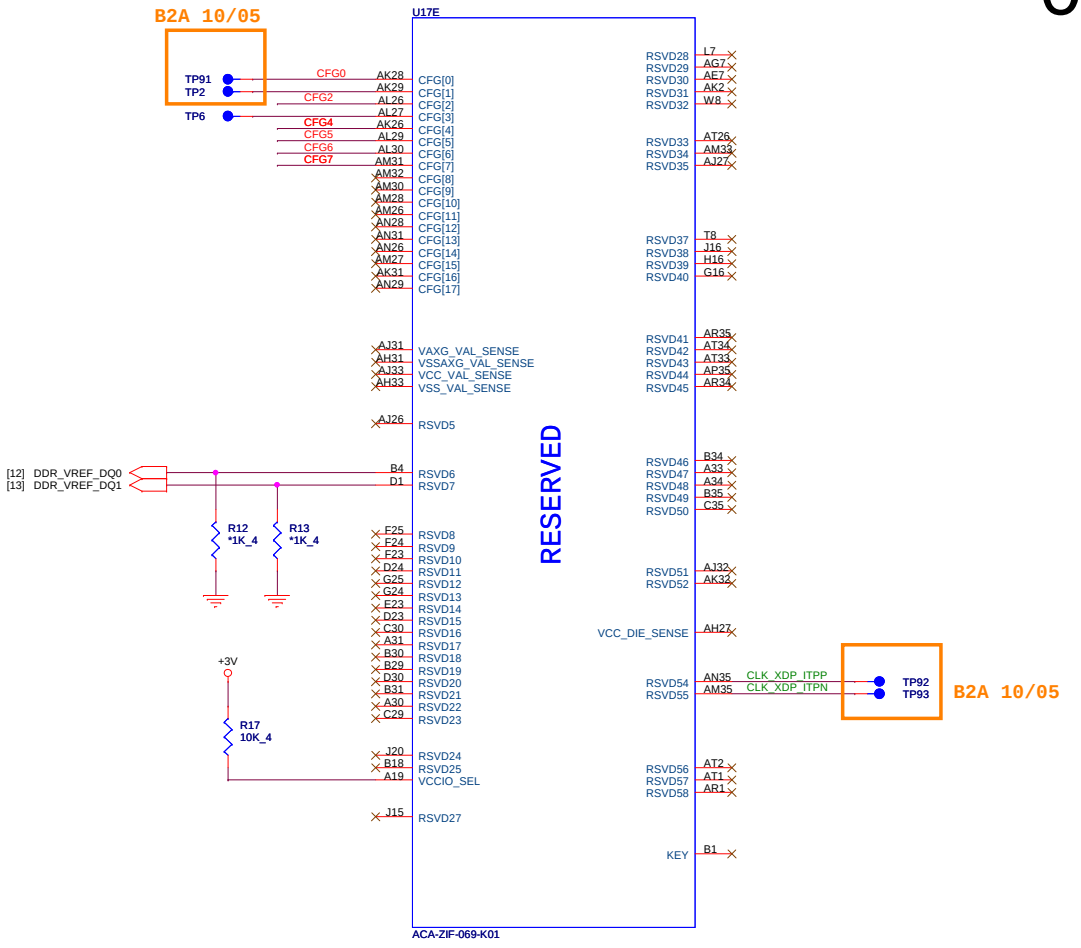
Sandy Bridge Processor (GND) <CPU>



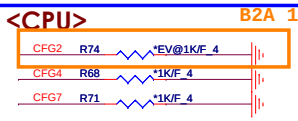
Sandy Bridge Processor (RESERVED, CFG) <CPU>

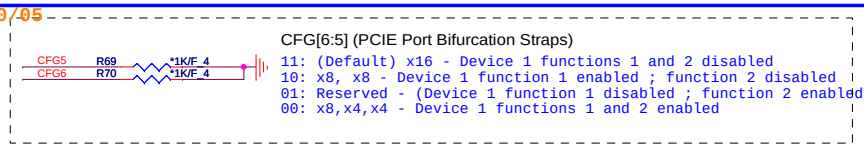


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	**Normal Operation**	Lane Reversed
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





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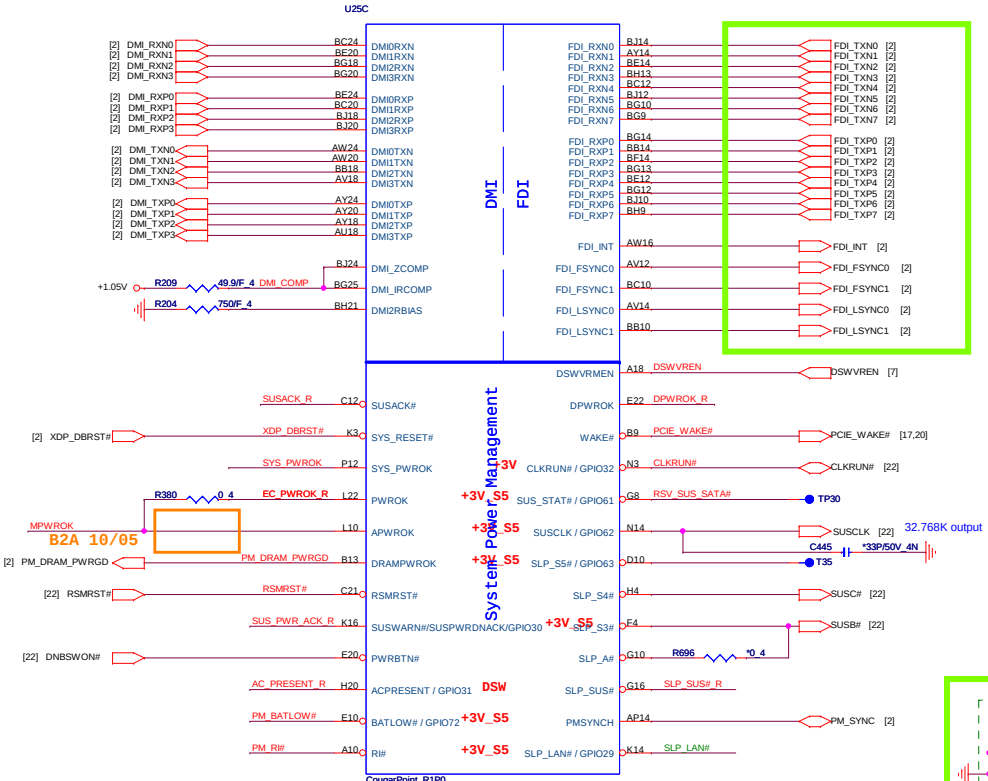
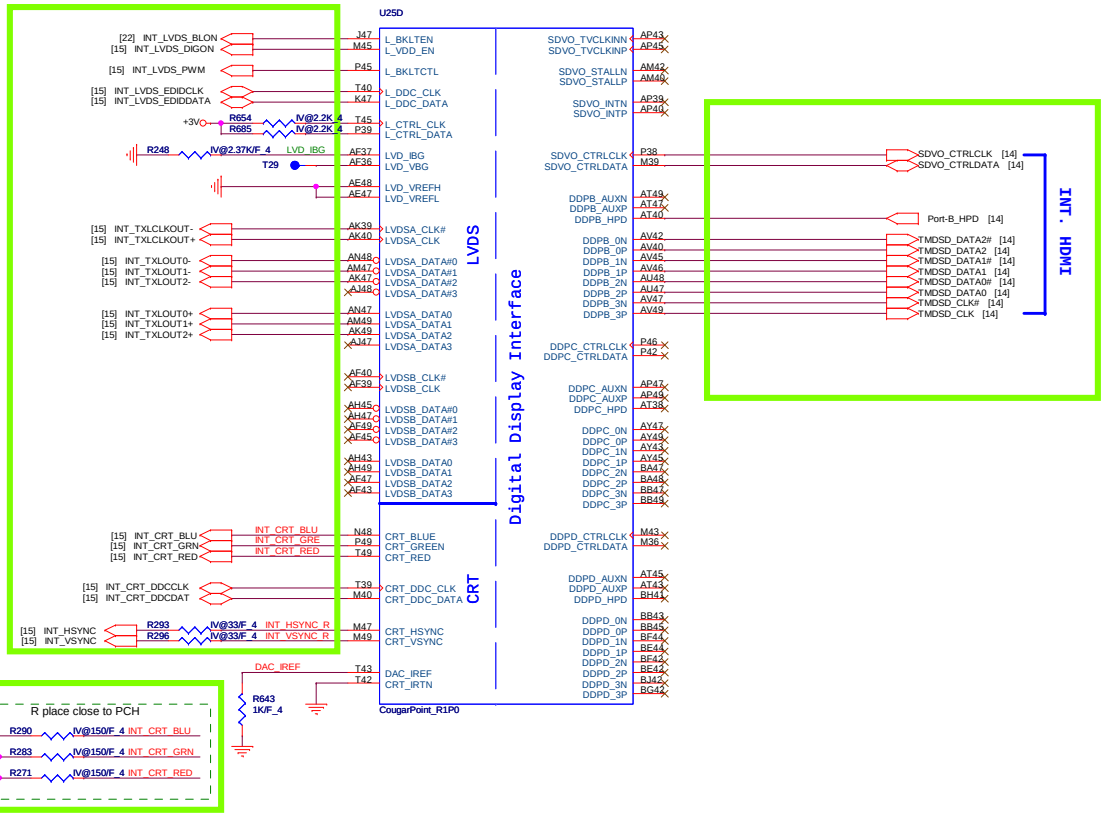
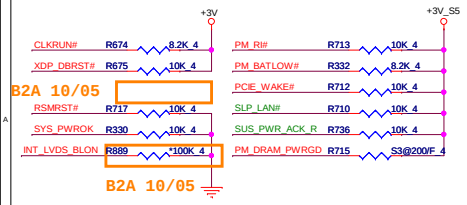
Cougar Point (DMI,FDI,PM) <CLG>



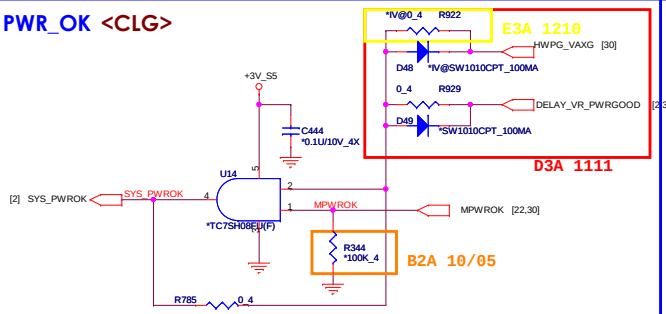
Cougar Point (LVDS,DDI) <CLG/UGA>



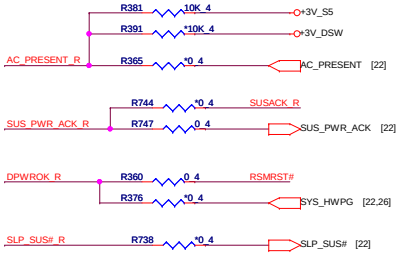
PCH Pull-high/low <CLG>



System PWR_OK <CLG>



Deep Sx <CLG>



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	R391,R365 stuff	R381 stuff
SUS_PWR_ACK	R744 stuff	R747 stuff
DPWROK	R376 stuff	R360 stuff
SLP_SUS	R738 stuff	R738 No stuff

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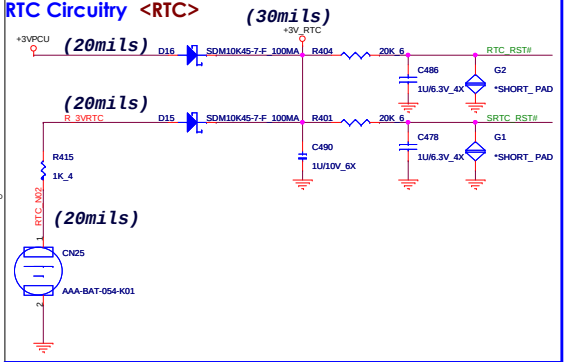
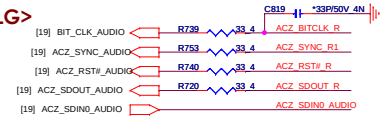
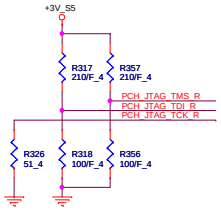
RTC Circuitry <RTC>



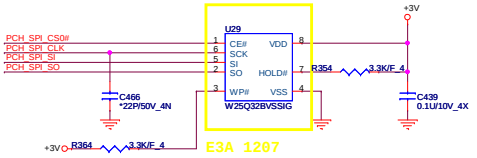
HDA Bus <CLG>



PCH JTAG Debug <CLG>

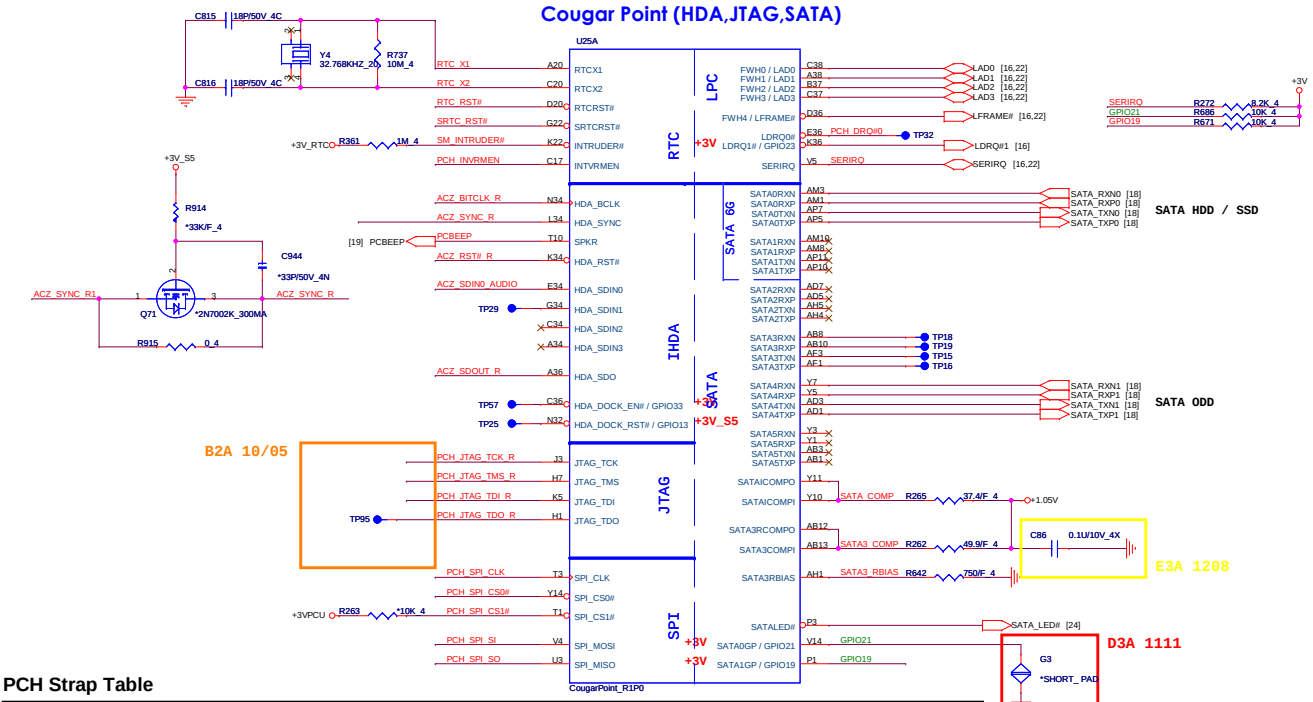


PCH Dual SPI <CLG>



PCH2 <CLG>

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R292 *1K_4 PCBEEP
INIT3_3V#	**Reserved**	PWROK	1 = Default (weak pull-up 20K)	**Should not pull low. leave as No Connect**
GNT3#/ GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R705 *1K_4 PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R716 330K_4 PCH_INVRMEN
GNT1#/ GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1, GNT0# 1 → Boot Location SPI *	R702 *1K_4 GNT1 [8]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	GNT1# 0, GNT0# 0 → Boot Location LPC	R672 *1K_4 GPIO19
GNT2#/ GPIO53	**ESI Strap (Server Only)**	PWROK	1 = Default. Should not be pulled low for desktop and mobile	**Should not pull low for desktop and mobile**
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Default (weak pull-up 20K) 1 = Override	+3V R719 *1K_4 ACZ_SDOUT_R ACZ_SDOUT_R [22]
DF_TVS	**DMI/FDI Termination voltage**	**PWROK**	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**	R581 2.2K_4, R582 1K_4 +1.8V DF_TVS [9] H_SNB_IVB# [2]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R298 *1K_4 PLL_ODVR_EN [9]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Default. Support by 1.8V 1 = Support by 1.5V	+3V_S5 R752 1K_4 ACZ_SYNC_R
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 R694 1K_4 GPIO15 GPIO15 [9]
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	+3V_RTC R711 330K_4 R729 *330K_4 DSWVREN [6]
SATA2GP/ GPIO36	**Reserved**	PWROK	0 = Default	**Should not be pulled hight when strap is sampled**
SATA3GP/ GPIO37	**Reserved**	PWROK	0 = Default	**Should not be pulled hight when strap is sampled**

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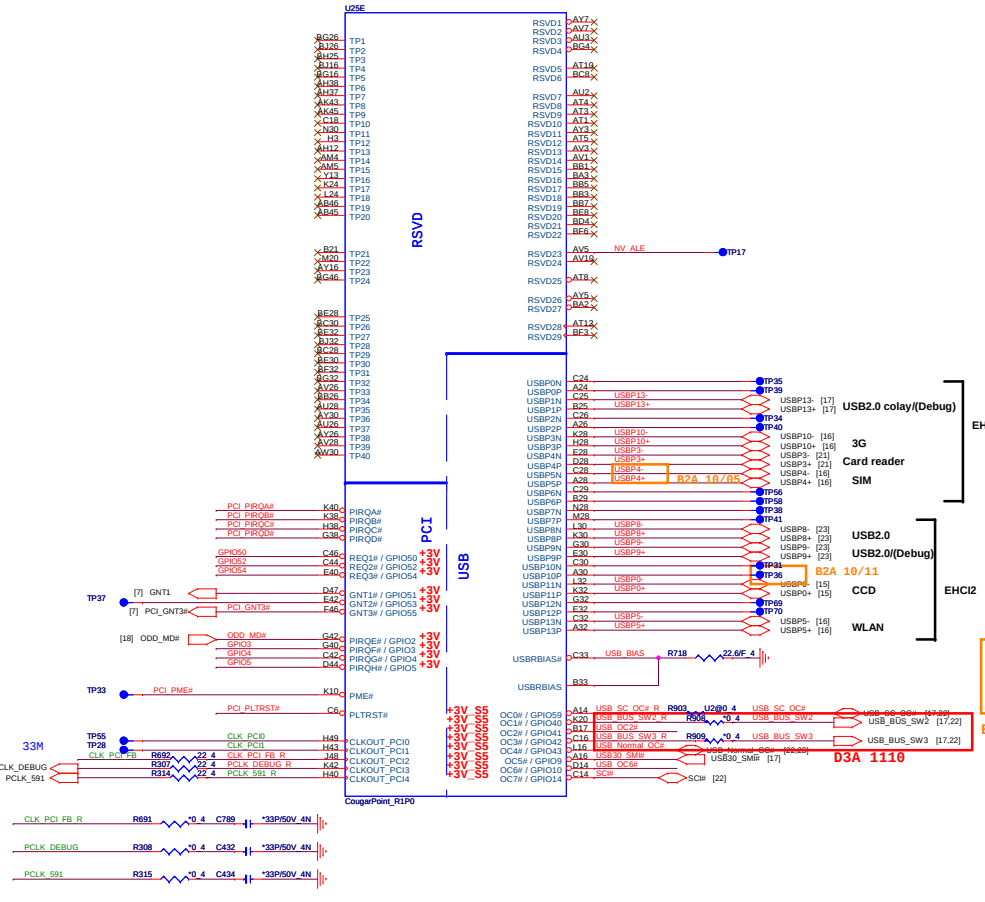
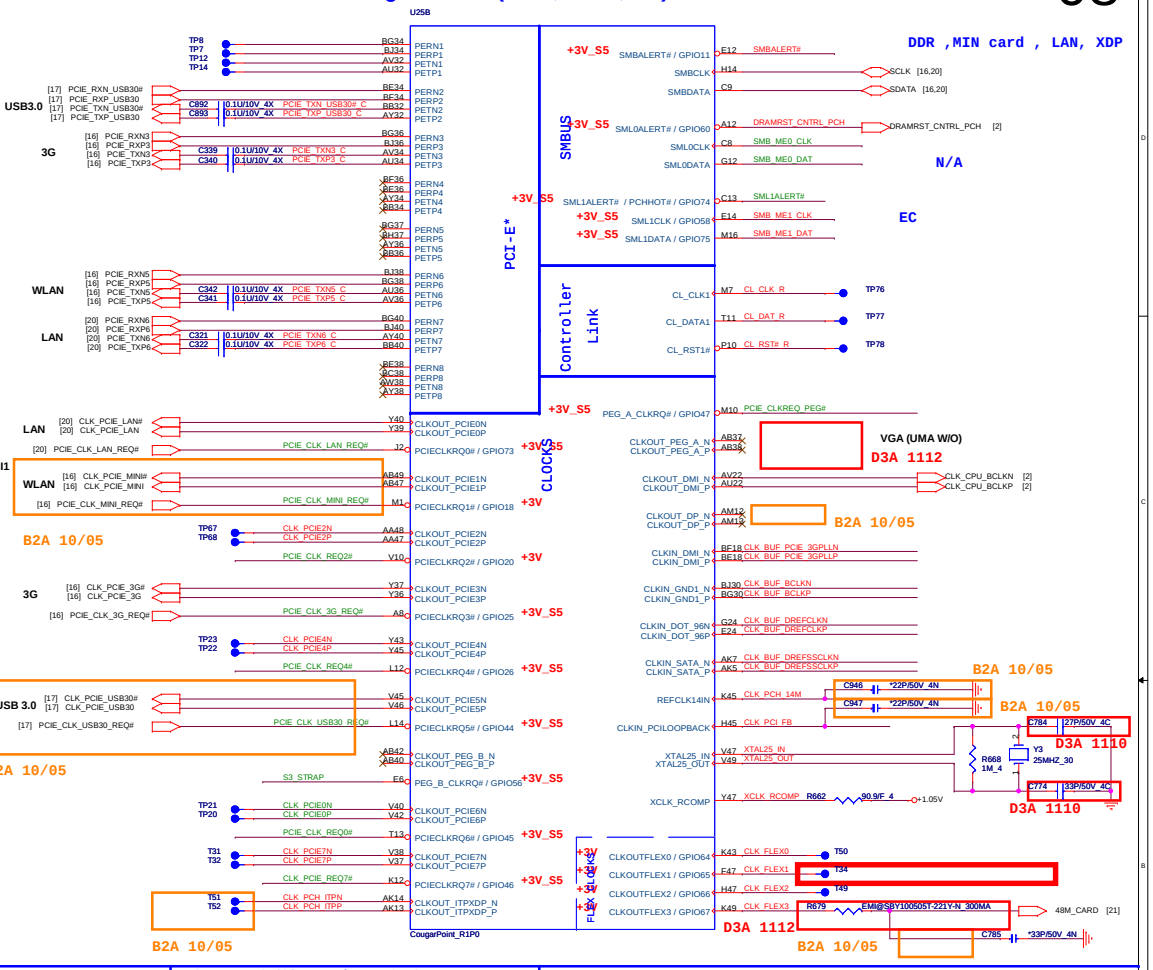
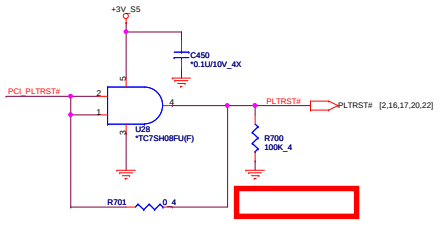
Cougar Point-M (PCI,USB,NVRAM) <CLG>



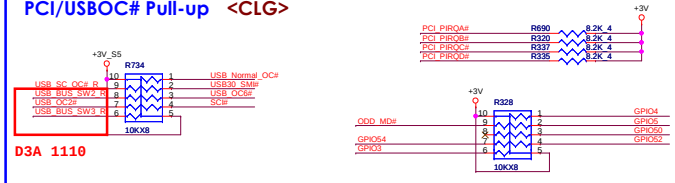
Cougar Point-M (PCI-E,SMBUS,CLK) <CLG>



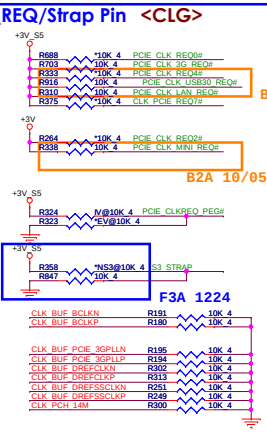
PLTRST# <CLG>



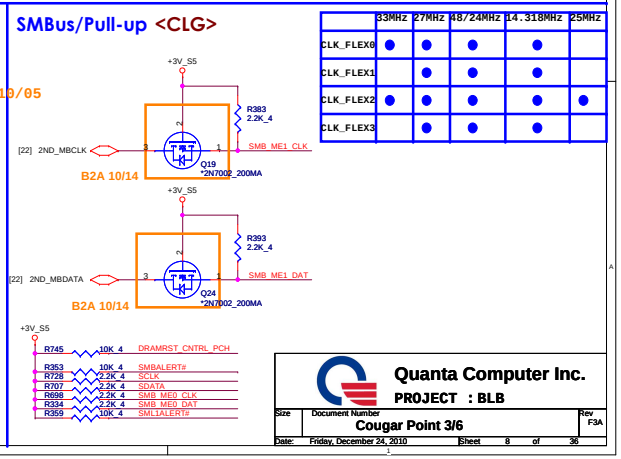
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap Pin <CLG>



SMBus/Pull-up <CLG>



Quanta Computer Inc.
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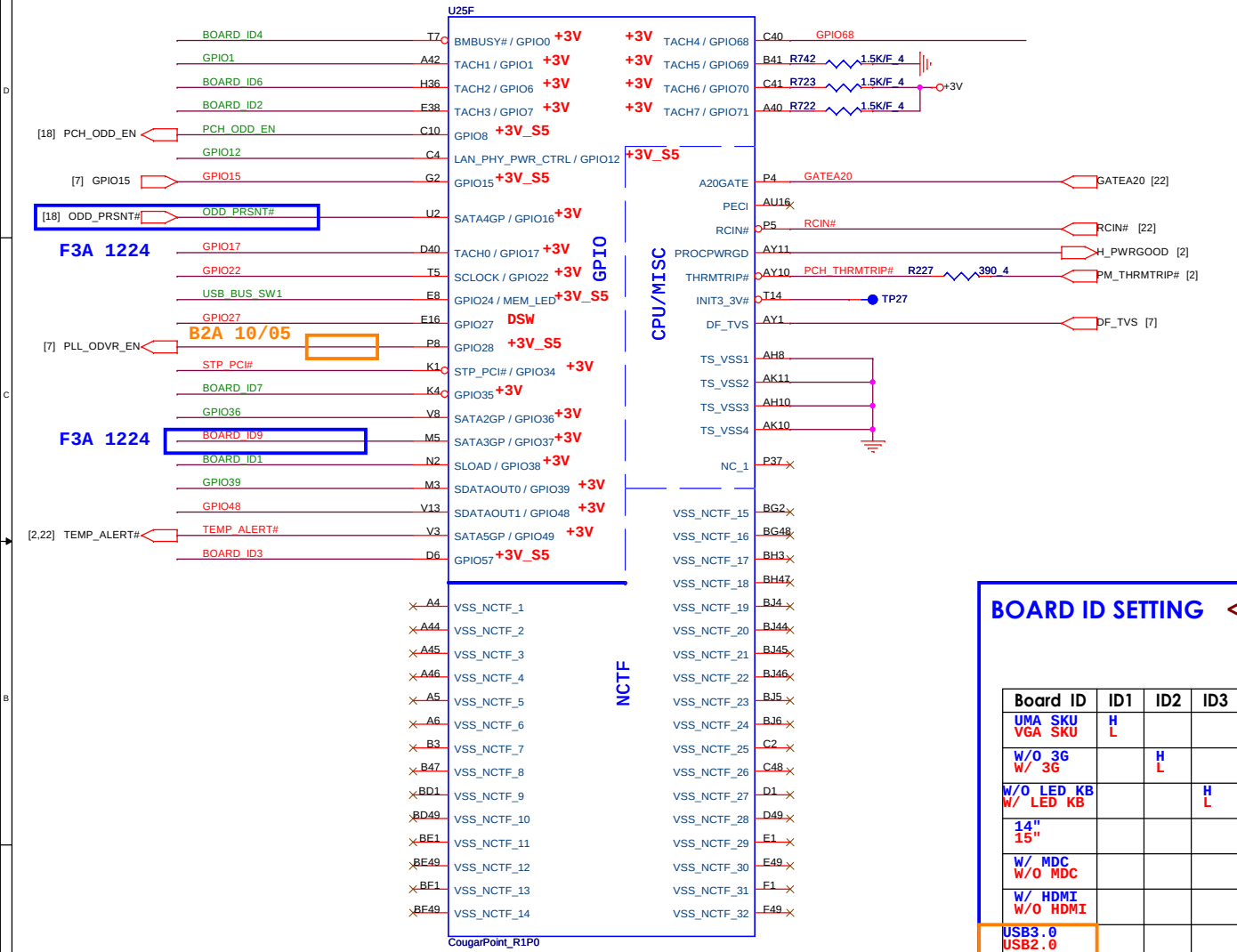
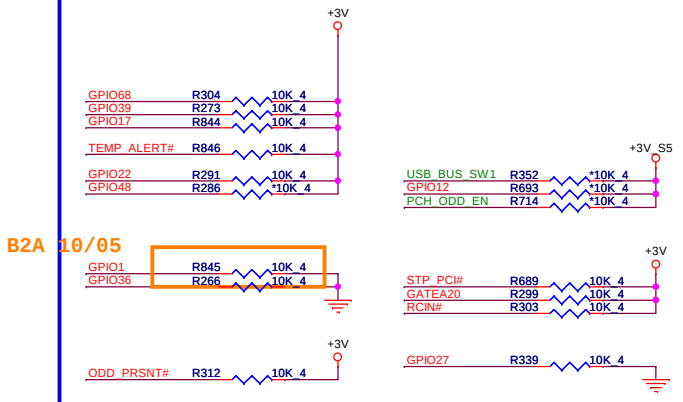
Cougar Point (GPIO,VSS_NCTF,RSVD) <CLG>



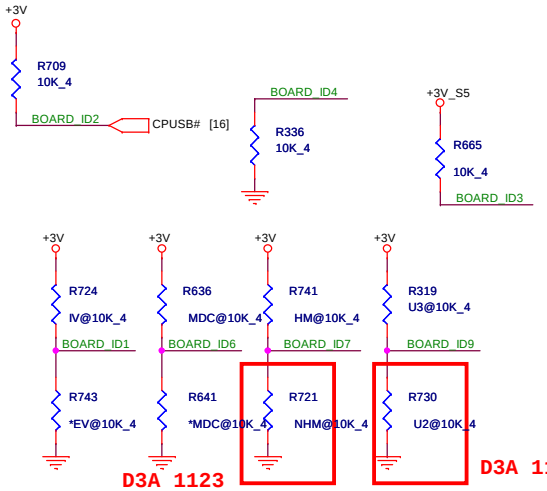
GPIO Pull-up/Pull-down <CLG>



BOARD ID SETTING <CLG>

Board ID	ID1	ID2	ID3	ID4	ID6	ID7	ID9
UMA SKU VGA SKU	H L						
W/O 3G W/ 3G		H L					
W/O LED KB W/ LED KB			H L				
14" 15"				H L			
W/ MDC W/O MDC					H L		
W/ HDMI W/O HDMI						H L	
USB3.0 USB2.0							H L

B2A 10/05



D3A 1123

D3A 1123

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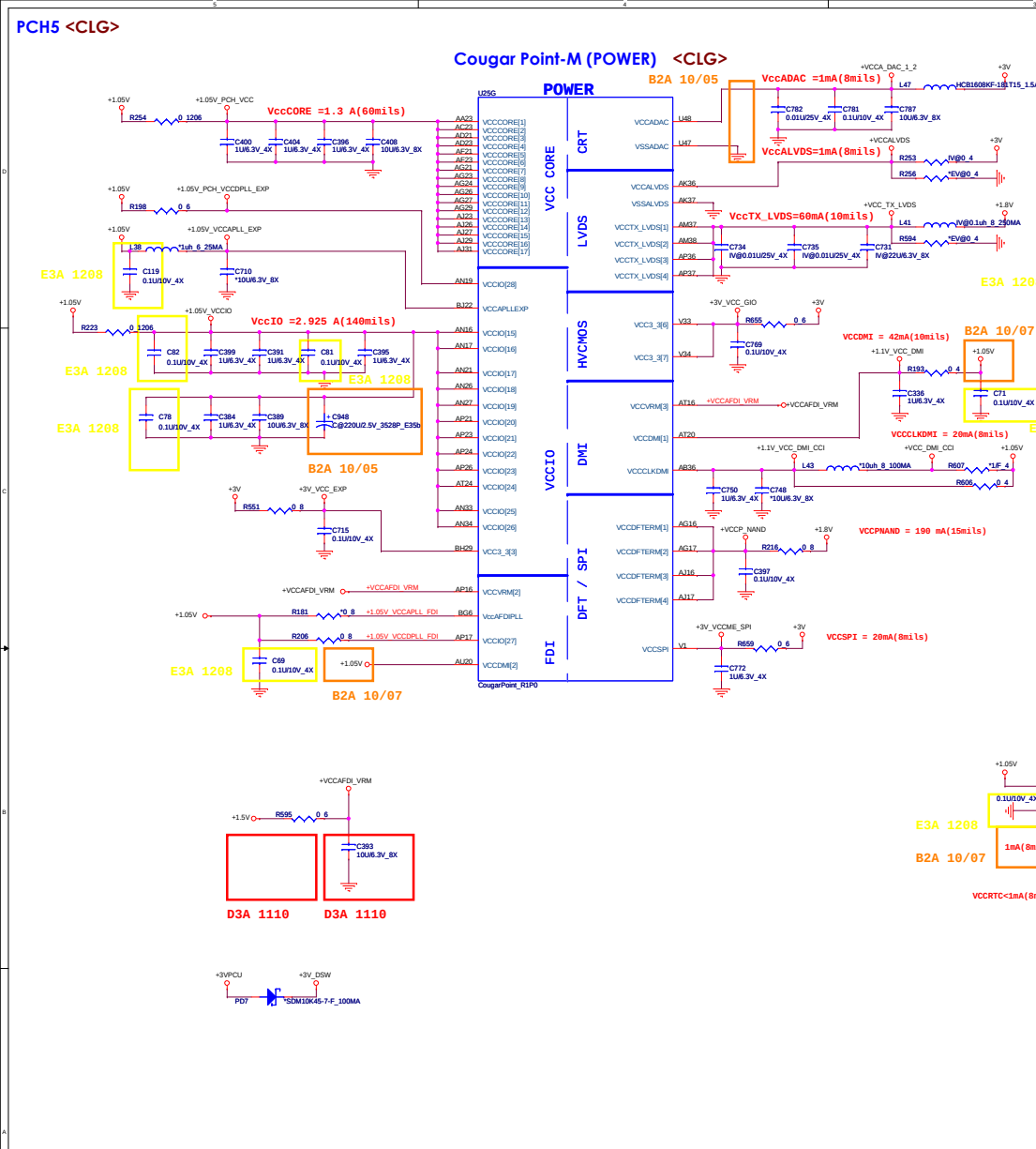
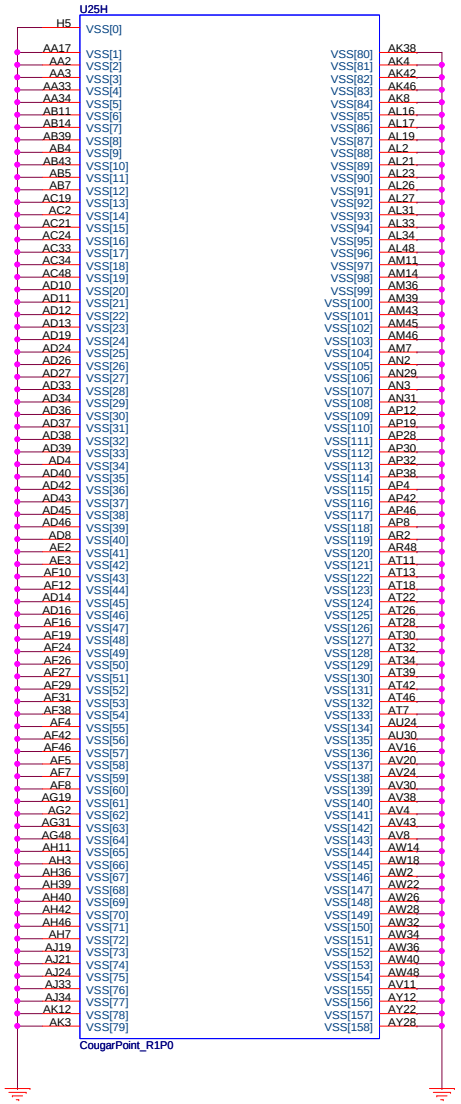
Cougar Point-M (POWER) <CLG>

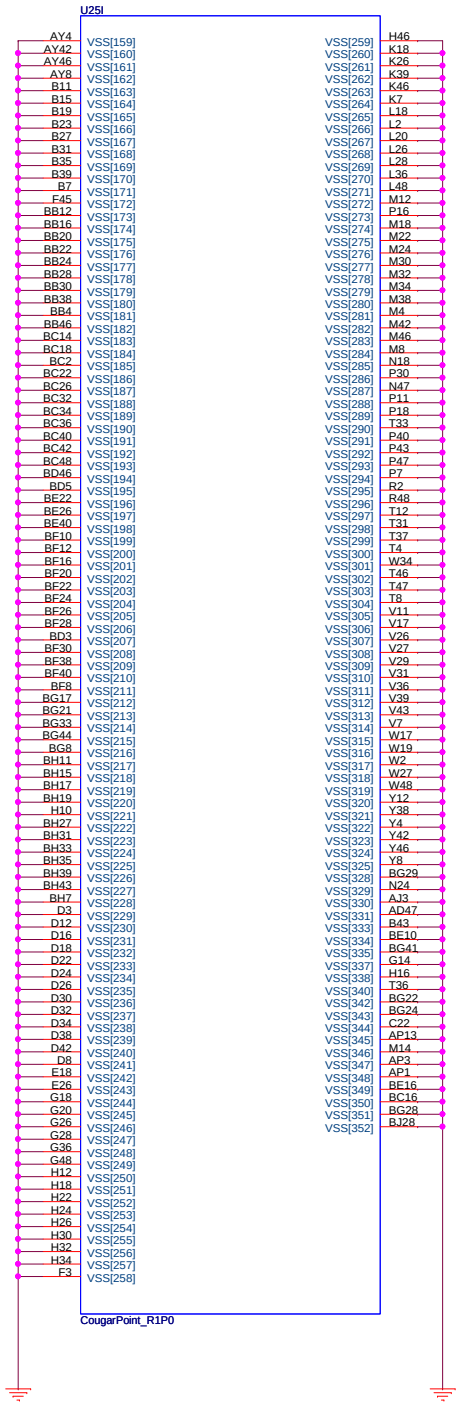


Cougar Point-M (POWER) <CLG>

Cougar Point (GND)



Cougar Point (GND)



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<DDR>

B2A 10/22

H=8

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

[3] M_A_A[15:0]

M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15

[3] M_A_BS#0
[3] M_A_BS#1
[3] M_A_BS#2
[3] M_A_CS#0
[3] M_A_CS#1
[3] M_A_CLKP0
[3] M_A_CLKN0
[3] M_A_CLKP1
[3] M_A_CLKN1
[3] M_A_CKE0
[3] M_A_CKE1
[3] M_A_CAS#
[3] M_A_RAS#
[3] M_A_WE#

R88 10K/F_4 DIMM0_SA0
R91 10K/F_4 DIMM0_SA1

[13,16] CGCLK_SMB
[13,16] CGDAT_SMB

[3] M_A_ODT0
[3] M_A_ODT1

[3] M_A_DQSP[7:0]

M_A_DQSP0 M_A_DQSP1 M_A_DQSP2 M_A_DQSP3 M_A_DQSP4 M_A_DQSP5 M_A_DQSP6 M_A_DQSP7

[3] M_A_DQSN[7:0]

M_A_DQSN0 M_A_DQSN1 M_A_DQSN2 M_A_DQSN3 M_A_DQSN4 M_A_DQSN5 M_A_DQSN6 M_A_DQSN7

M_A_DQ[63:0] [3]

M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7 M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15 M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31 M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63

[5] DDR_VREF_DQ0

R8 *0_6

SMDDR_VREF_DQ0
SMDDR_VREF_DIMM

VREF_DQ/(M3)

+1.5VSUS

B2A 10/22

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

+3V

R464 *10K_4 PM_EXTTS#0

[2,13] DDR3_DRAMRST#

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18

VDDSPD

NC1 NC2 NCTEST

EVENT# RESET#

VREF_DQ VREF_CA

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15

VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52

VTT1 VTT2

+SMDDR_VTERM

GND GND

B2A 10/07

+1.5V_CPU

C3038 0.1U/10V_4X
C3039 0.1U/10V_4X
C3040 0.1U/10V_4X
C3041 0.1U/10V_4X

SMDDR_VREF_DIMM [13]

C91 470P/50V_4X R30 0_4 +SMDDR_VREF

R32 *10K/F_4 R29 *10K/F_4 +1.5VSUS

Place these Caps near So-Dimm0. <DDR>

+1.5VSUS

C48 4.7U/6.3V_6X
C64 4.7U/6.3V_6X
C49 C@4.7U/6.3V_6X
C62 4.7U/6.3V_6X
C76 C@4.7U/6.3V_6X
C84 4.7U/6.3V_6X
C56 0.1U/10V_4X
C75 0.1U/10V_4X
C58 0.1U/10V_4X
C63 0.1U/10V_4X
C73 *0.1U/10V_4X
C52 *0.047U/10V_4X
C65 *0.047U/10V_4X

SMDDR_VREF_DQ0

C40 0.1U/10V_4X
C37 2.2U/6.3V_6X

SMDDR_VREF_DIMM

C93 0.1U/10V_4X
C100 2.2U/6.3V_6X
C101 *0.047U/10V_4X

+3V

C161 2.2U/6.3V_6X
C154 *0.1U/10V_4X
C145 *0.047U/10V_4X

+SMDDR_VTERM

C165 1U/6.3V_4X
C174 1U/6.3V_4X
C162 1U/6.3V_4X
C166 1U/6.3V_4X
C163 *10U/6.3V_8X
C171 *10U/6.3V_8X
C172 *4.7U/6.3V_6X
C173 *0.047U/10V_4X
C157 *0.047U/10V_4X

VREF_DQ/(M1) <DDR>

+1.5VSUS

R7 1K/F_4

SMDDR_VREF_DQ0

R6 1K/F_4 C39 0.1U/10V_4X C34 *0.047U/10V_4X

+1.5VSUS

+ C572 C@330U/2.5V_7343P_E9a

For S3 Power Reduction VTT discharge <S3P>

+SMDDR_VTERM

R82 S3@22_4

[2,3,4,31] MAINON_ON_G

Q2 S3@2N7002_200MA

Quanta Computer Inc.

PROJECT : BLB

Size	Document Number	Rev
	DDR3 DIMM-0	F3A
Date: Friday, December 24, 2010	Sheet 12 of 36	

<DDR>

B2A 10/22 H=4

JDIM2A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

[3] M_B_A[15:0]

M_B_A0 98, M_B_A1 97, M_B_A2 96, M_B_A3 95, M_B_A4 92, M_B_A5 91, M_B_A6 90, M_B_A7 86, M_B_A8 89, M_B_A9 85, M_B_A10 107, M_B_A11 84, M_B_A12 83, M_B_A13 119, M_B_A14 80, M_B_A15 78

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15

M_B_DQ[63:0] [3]

M_B_DQ0 5, M_B_DQ1 7, M_B_DQ2 15, M_B_DQ3 17, M_B_DQ4 4, M_B_DQ5 6, M_B_DQ6 16, M_B_DQ7 18, M_B_DQ8 21, M_B_DQ9 23, M_B_DQ10 33, M_B_DQ11 35, M_B_DQ12 22, M_B_DQ13 24, M_B_DQ14 34, M_B_DQ15 36, M_B_DQ16 39, M_B_DQ17 41, M_B_DQ18 51, M_B_DQ19 53, M_B_DQ20 40, M_B_DQ21 42, M_B_DQ22 50, M_B_DQ23 52, M_B_DQ24 57, M_B_DQ25 59, M_B_DQ26 67, M_B_DQ27 69, M_B_DQ28 56, M_B_DQ29 58, M_B_DQ30 68, M_B_DQ31 70, M_B_DQ32 129, M_B_DQ33 131, M_B_DQ34 141, M_B_DQ35 143, M_B_DQ36 130, M_B_DQ37 132, M_B_DQ38 140, M_B_DQ39 142, M_B_DQ40 147, M_B_DQ41 149, M_B_DQ42 157, M_B_DQ43 159, M_B_DQ44 146, M_B_DQ45 148, M_B_DQ46 158, M_B_DQ47 160, M_B_DQ48 163, M_B_DQ49 165, M_B_DQ50 175, M_B_DQ51 177, M_B_DQ52 164, M_B_DQ53 166, M_B_DQ54 174, M_B_DQ55 176, M_B_DQ56 181, M_B_DQ57 183, M_B_DQ58 191, M_B_DQ59 193, M_B_DQ60 180, M_B_DQ61 182, M_B_DQ62 192, M_B_DQ63 194

[3] M_B_BS#0 108
[3] M_B_BS#1 79
[3] M_B_BS#2 114
[3] M_B_CS#0 121
[3] M_B_CS#1 101
[3] M_B_CLKP0 103
[3] M_B_CLKN0 102
[3] M_B_CLKP1 104
[3] M_B_CLKN1 73
[3] M_B_CKE0 74
[3] M_B_CKE1 115
[3] M_B_CAS# 110
[3] M_B_RAS# 113
[3] M_B_WE# 109

BA0 BA1 BA2 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#

+3V
R62 10K/F_4 DIMM1_SA0 197
R59 10K/F_4 DIMM1_SA1 201
SA0 SA1

[12,16] CGCLK_SMB 202
[12,16] CGDAT_SMB 200
SCL SDA

[3] M_B_ODT0 116
[3] M_B_ODT1 120
ODT0 ODT1

DM0 11, DM1 28, DM2 46, DM3 63, DM4 136, DM5 153, DM6 170, DM7 187

[3] M_B_DQSP[7:0]

M_B_DQSP0 12, M_B_DQSP1 29, M_B_DQSP2 47, M_B_DQSP3 64, M_B_DQSP4 137, M_B_DQSP5 154, M_B_DQSP6 171, M_B_DQSP7 188

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

[3] M_B_DQSN[7:0]

M_B_DQSN0 10, M_B_DQSN1 27, M_B_DQSN2 45, M_B_DQSN3 62, M_B_DQSN4 135, M_B_DQSN5 152, M_B_DQSN6 169, M_B_DQSN7 186

DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

[5] DDR_VREF_DQ1
R10 *0_6
SMDDR_VREF_DQ1
[12] SMDDR_VREF_DIMM

VREF_DQ/(M3)

H=4 B2A 10/22

+1.5VSUS

JDIM2B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

VDD1 75, VDD2 76, VDD3 81, VDD4 82, VDD5 87, VDD6 88, VDD7 93, VDD8 94, VDD9 99, VDD10 100, VDD11 105, VDD12 106, VDD13 111, VDD14 112, VDD15 117, VDD16 118, VDD17 123, VDD18 124

+3V VDDSPD 199

NC1 77, NC2 122, NCTEST 125

+3V R105 *10K_4 PM_EXTTS#1 198
[2,12] DDR3_DRAMRST# EVENT# 30
RESET#

VREF_DQ 1, VREF_CA 126

VSS1 2, VSS2 3, VSS3 8, VSS4 9, VSS5 13, VSS6 14, VSS7 19, VSS8 20, VSS9 25, VSS10 26, VSS11 31, VSS12 32, VSS13 37, VSS14 38, VSS15 43

VSS16 44, VSS17 48, VSS18 49, VSS19 54, VSS20 55, VSS21 60, VSS22 61, VSS23 65, VSS24 66, VSS25 71, VSS26 72, VSS27 127, VSS28 128, VSS29 133, VSS30 134, VSS31 138, VSS32 139, VSS33 144, VSS34 145, VSS35 150, VSS36 151, VSS37 155, VSS38 156, VSS39 161, VSS40 162, VSS41 167, VSS42 168, VSS43 172, VSS44 173, VSS45 178, VSS46 179, VSS47 184, VSS48 185, VSS49 189, VSS50 190, VSS51 195, VSS52 196

VTT1 203, VTT2 204 +SMDDR_VTERM

GND 205, GND 206

Place these Caps near So-Dimm1. <DDR>

+1.5VSUS
C548 4.7U/6.3V_6X
C51 4.7U/6.3V_6X
C524 C@4.7U/6.3V_6X
C529 4.7U/6.3V_6X
C85 C@4.7U/6.3V_6X
C542 4.7U/6.3V_6X
C53 0.1U/10V_4X
C66 0.1U/10V_4X
C50 0.1U/10V_4X
C70 0.1U/10V_4X
C525 *0.1U/10V_4X
C550 *0.047U/10V_4X
C540 *0.047U/10V_4X

SMDDR_VREF_DIMM
C562 0.1U/10V_4X
C569 2.2U/6.3V_6X
C559 *0.047U/10V_4X

SMDDR_VREF_DQ1
C35 0.1U/10V_4X
C41 2.2U/6.3V_6X

+3V
C155 2.2U/6.3V_6X
C164 *0.1U/10V_4X
C156 *0.047U/10V_4X

+SMDDR_VTERM
C613 1U/6.3V_4X
C178 1U/6.3V_4X
C630 1U/6.3V_4X
C179 1U/6.3V_4X
C181 *10U/6.3V_8X
C176 *4.7U/6.3V_6X
C650 *4.7U/6.3V_6X
C611 *0.047U/10V_4X
C634 *0.047U/10V_4X

VREF_DQ/(M1) <DDR>

+1.5VSUS
R11 1K/F_4
SMDDR_VREF_DQ1
R9 1K/F_4
C38 0.1U/10V_4X
C36 *0.047U/10V_4X

+1.5VSUS
C522 C@330U/2.5V_7343P_E9a

Quanta Computer Inc.
PROJECT : BLB

Size	Document Number	Rev
	DDR3 DIMM-1	F3A

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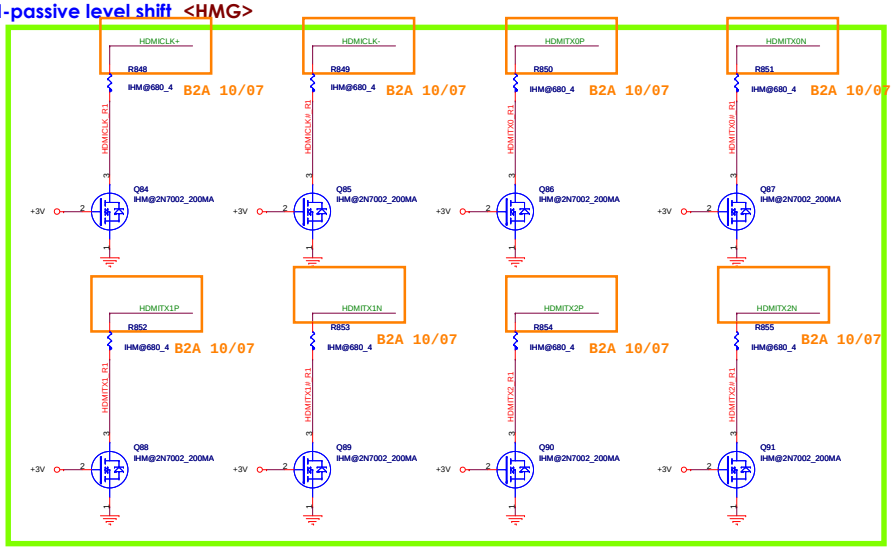
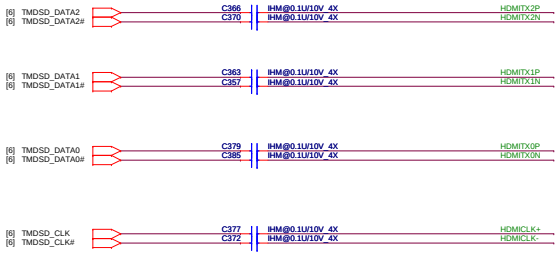
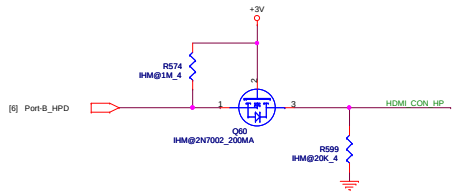
HDMI-passive level shift <HMG>



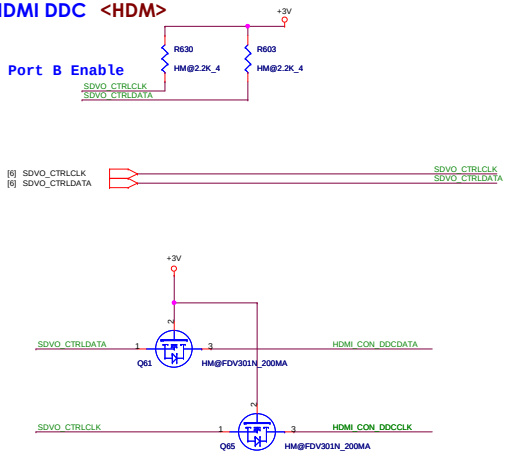
UMA HDMI <HMG>



HDMI HPD <HMP/HMG>

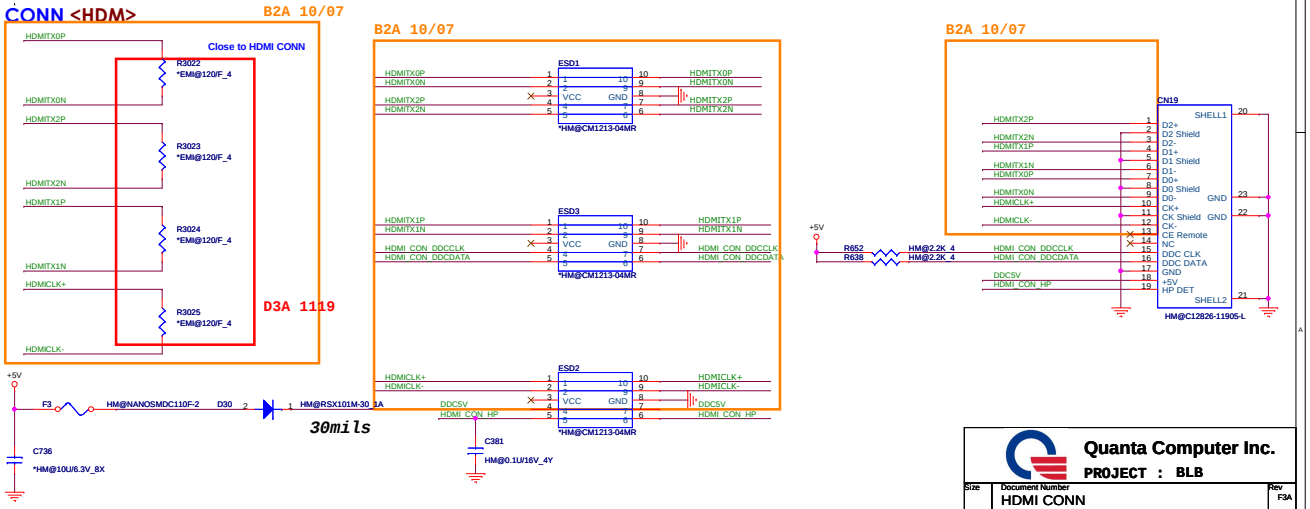


HDMI DDC <HDM>



HDMI CONN <HDM>

B2A 10/07



B2A 10/07

B2A 10/07

Quanta Computer Inc.
PROJECT : BLB

Size	Document Number	Rev
	HDMI CONN	F3A
Date:	Friday, December 24, 2010	Sheet 14 of 36

Panel backlight control <LDS>

B2A 10/05

DISPON_O

DISPON_O [22]

R857 *100K_4

CCD <CCD>

D3A 11/10 EMI

USBP0+ LCD

USBP0- LCD

L20 EMI@DLP11SN900HL2L

USBP0+ [8]

USBP0- [8]

E3A 1209

0.2A(20mils)

+3V R430 0_8 CCD_POWER

C510 10U/6.3V_8X

HALL SENSOR <HSR>

+3VPCU R764 100K_4

MR1 AH5249NTR-G1

LID591# [22]

C839 0.1U/16V_4Y

E3A 1207

15

LCD Panel Module <LDS>

0.3A (20mils)

VIN R858 0_8 LCD_BK_POWER

C504 C@10U/25V_1206X

C505 *1000P/50V_4X

C506 *0.1U/25V_6X

D47 *EGA10402V05AH DISPON_O

B2A 10/05

+3V R83 2.2K_4 INT_LVDS_EDIDCLK

R76 2.2K_4 INT_LVDS_EDIDDATA

[6] INT_LVDS_PWM R419 IV@0_4 LVDS_VADJ

C499 *0.1U/16V_4Y

LCDVCC

[6] INT_LVDS_EDIDCLK

[6] INT_LVDS_EDIDDATA

[6] INT_TXLOUT0-

[6] INT_TXLOUT0+

[6] INT_TXLOUT1-

[6] INT_TXLOUT1+

[6] INT_TXLOUT2-

[6] INT_TXLOUT2+

[6] INT_TXLCLKOUT-

[6] INT_TXLCLKOUT+

LVDS_VADJ

DISPON_O

LCD_BK_POWER

CCD_POWER

USBP0- LCD

USBP0+ LCD

[19] INT_DMIC_CLK

[19] INT_DMIC_DATA

R416 SBY100505T-221Y-N_300MA

R417 SBY100505T-221Y-N_300MA

C894 *22P/50V_4N

C895 *22P/50V_4N

CN1 50373-03001-001

B2A 10/07

LCD POWER SWITCH <LDS>

[6] INT_LVDS_DIGON

+15V R423 330K_6

+3VPCU R425 100K_4

R426 100K_4

Q29 DTC143TKA146_100MA

Q28 2N7002_200MA

Q26 ME2306_4A

Q27 2N7002_200MA

LCDONG

LCDON#

LCDISCHG

C507 0.01U/25V_4X

R424 22_8

1.5A(65mils)

+3V

LCDVCC1

L25 *SHORT_6

LCDVCC

C502 C@0.1U/16V_4Y

C500 C@0.01U/25V_4X

C501 C@10U/6.3V_8X

CRT <CRT>

[6] INT_CRT_RED

[6] INT_CRT_GRN

[6] INT_CRT_BLU

INT_CRT_RED

INT_CRT_GRN

INT_CRT_BLU

L26 BLM18BA470SN1D_300MA

L27 BLM18BA470SN1D_300MA

L28 BLM18BA470SN1D_300MA

CRT_R1

CRT_G1

CRT_B1

R458 150/F_4

C593 6.8P/50V_4N

R461 150/F_4

C602 6.8P/50V_4N

R472 150/F_4

C610 6.8P/50V_4N

C607 6.8P/50V_4N

C601 6.8P/50V_4N

C590 6.8P/50V_4N

[6] INT_CRT_DDCCLK

[6] INT_CRT_DDCDAT

[6] INT_HSYNC

[6] INT_VSYNC

+5V D23 B130L-13-F_1A F1 SMD1206P100TF

(30mils)

C183 0.1U/16V_4Y

5V_CRT2

B2A 9/30

CRT_R1

CRT_G1

CRT_B1

CRTDDAT

CRTHSYNC

CRTVSYNC

CRTDCLK

CN14 DHR41-15K1201

D3A 1119

+3V R95 2.2K_4 INT_CRT_DDCCLK

R94 2.2K_4 INT_CRT_DDCDAT

+5V C144 C@0.1U/16V_4Y

+3V C167 C@0.1U/16V_4Y

0.01mA(15mils)

2.05mA(20mils)

0.01mA(15mils)

C600 0.22U/6.3V_4X

U2 CM2009-02QR

VCC_SYNC SYNC_OUT2

SYNC_OUT1

VCC_DDC

BYP

VCC_VIDEO

SYNC_IN2

SYNC_IN1

VIDEO_1

VIDEO_2

VIDEO_3

GND

DDC_IN1

DDC_IN2

DDC_OUT1

DDC_OUT2

VSYNC1

HSYNC1

INT_VSYNC

INT_HSYNC

INT_CRT_DDCCLK

INT_CRT_DDCDAT

CRTDCLK

CRTDDAT

R478 0_4

R476 0_4

CRTVSYNC

CRTHSYNC

C652 10P/50V_4C

C632 10P/50V_4C

R73 2.7K_4

R81 2.7K_4

C142 10P/50V_4C

C153 10P/50V_4C

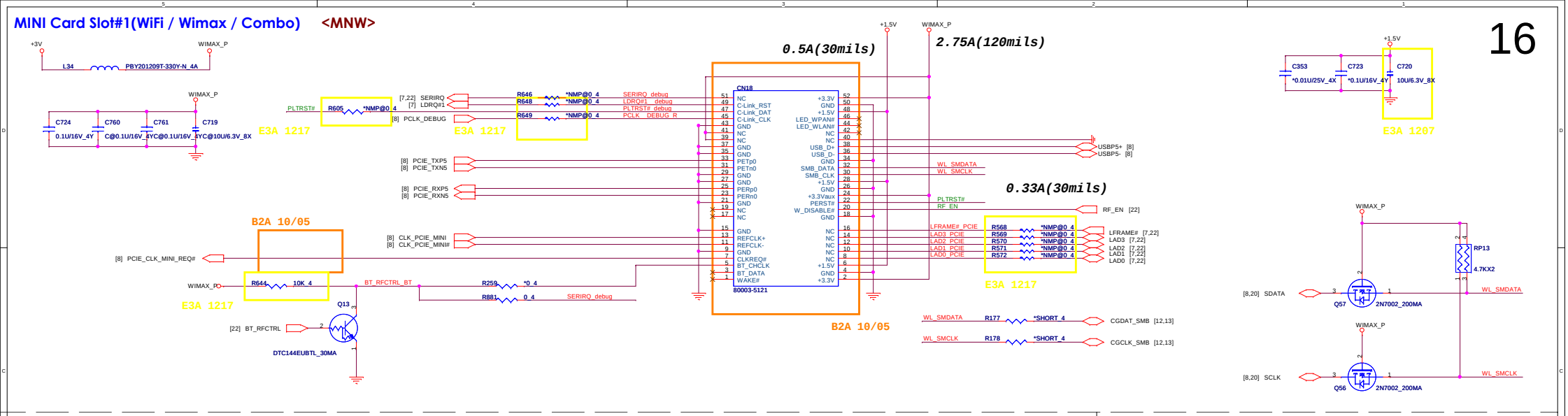
Quanta Computer Inc.

PROJECT : BLB

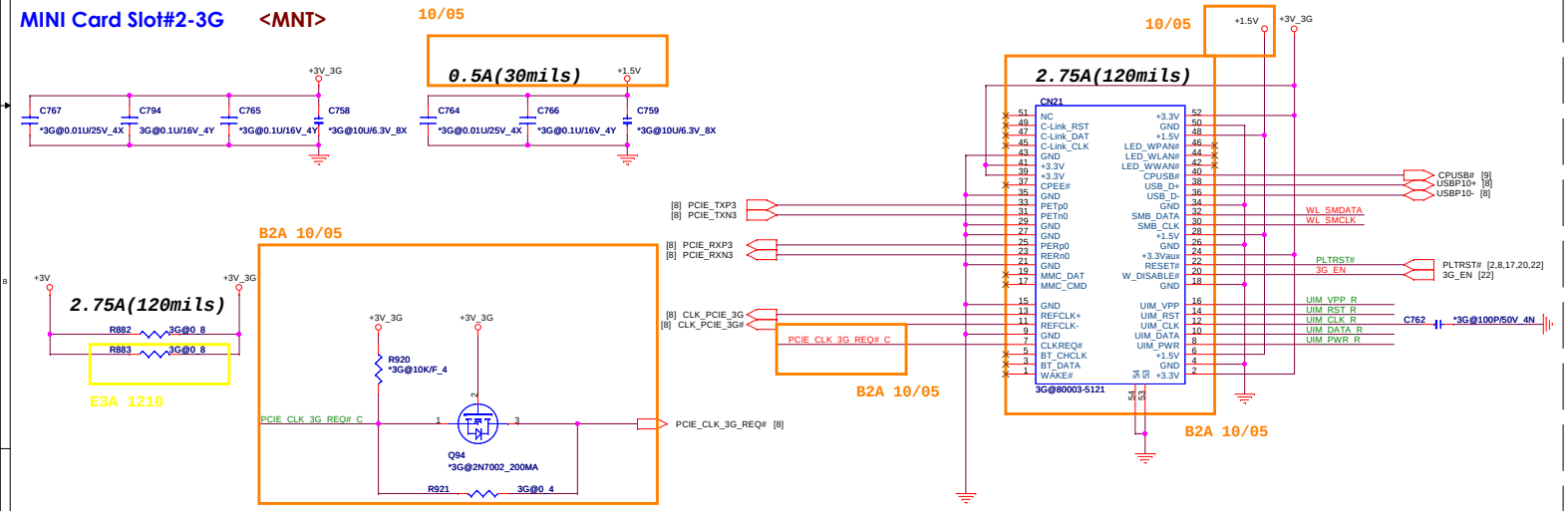
Size | Document Number: LCD/LED Panel/CCD | Rev: F3A

Date: Friday, December 24, 2010 | Sheet 15 of 36

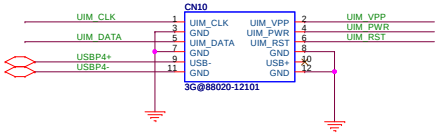
MINI Card Slot#1(WiFi / Wimax / Combo) <MNW>



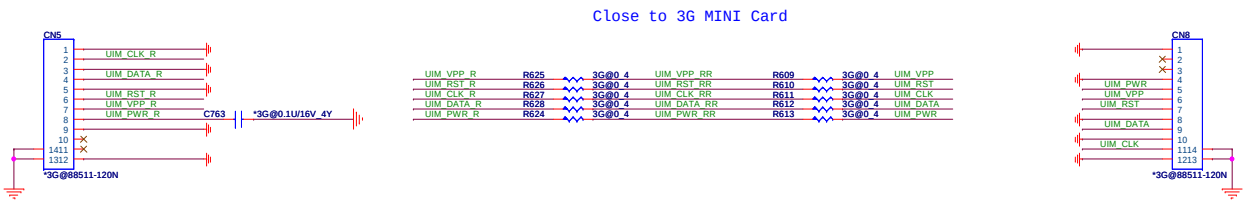
MINI Card Slot#2-3G <MNT>



SIM CARD board to board



3G CONN



Quanta Computer Inc.	
PROJECT : BLB	
Size	Document Number: MINI CARD(WLAN/3G/SIM Card) — Rev: F3A
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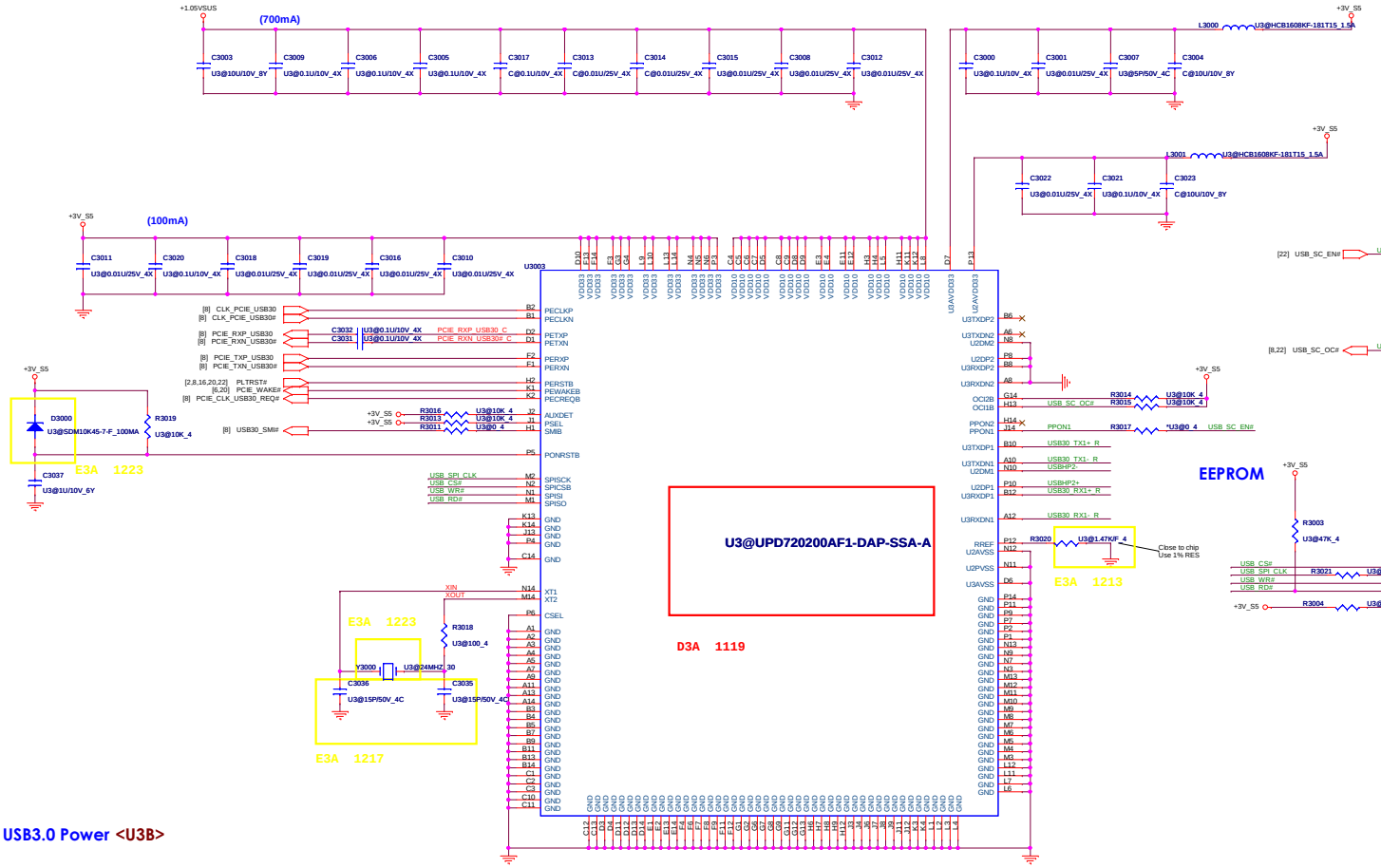
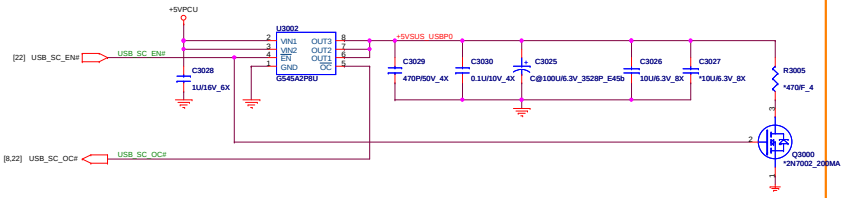
USB 3.0 Controller <U3B>

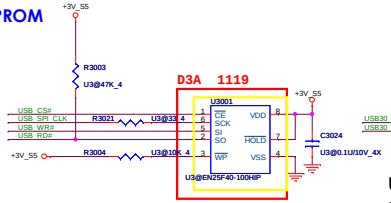
B2A 10/6



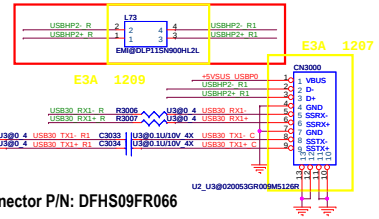
USB 3.0 Power switch <USB>



EEPROM



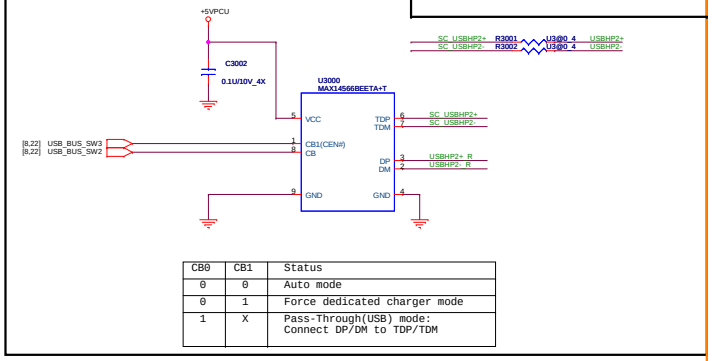
USB 3.0 CONN



USB 3.0 connector P/N: DFHS09FR066

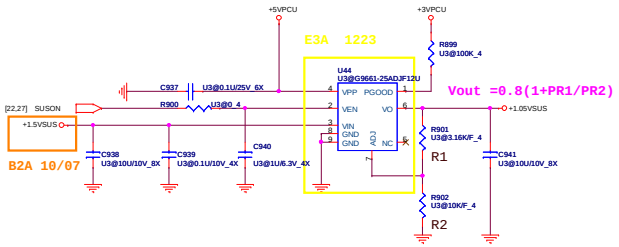
USB 2.0 connector P/N: DFHS04FR461

USB w S&C MAXIM solution <SLC>



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

USB3.0 Power <U3B>



Quanta Computer Inc.

PROJECT : BLB

USB 3.0

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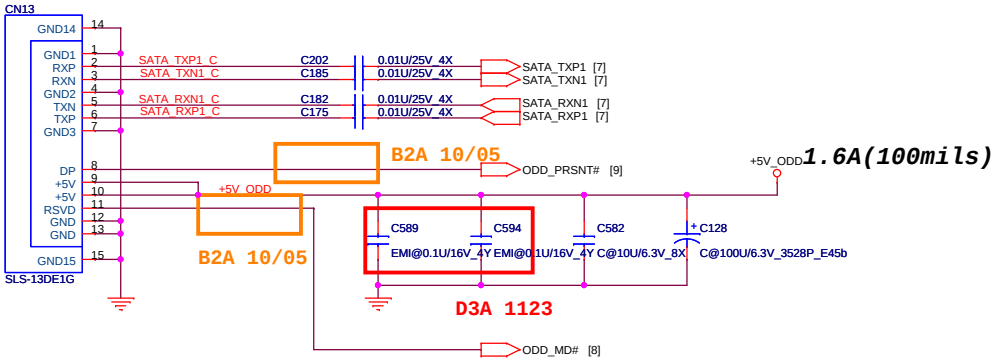
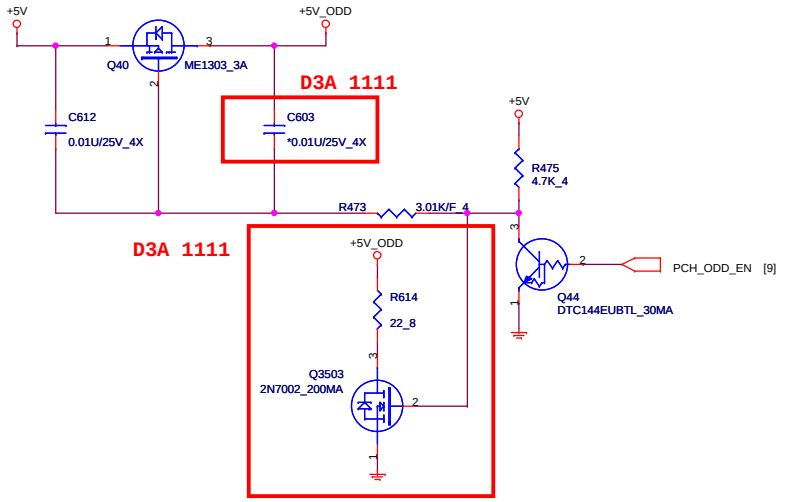
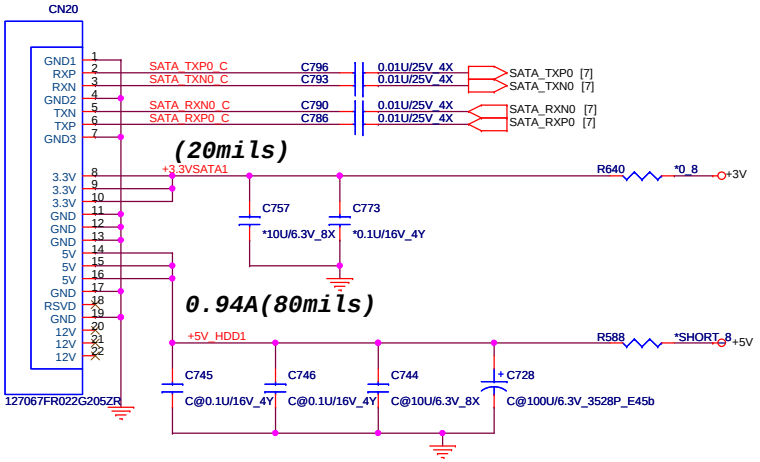
SATA ODD <ODD>



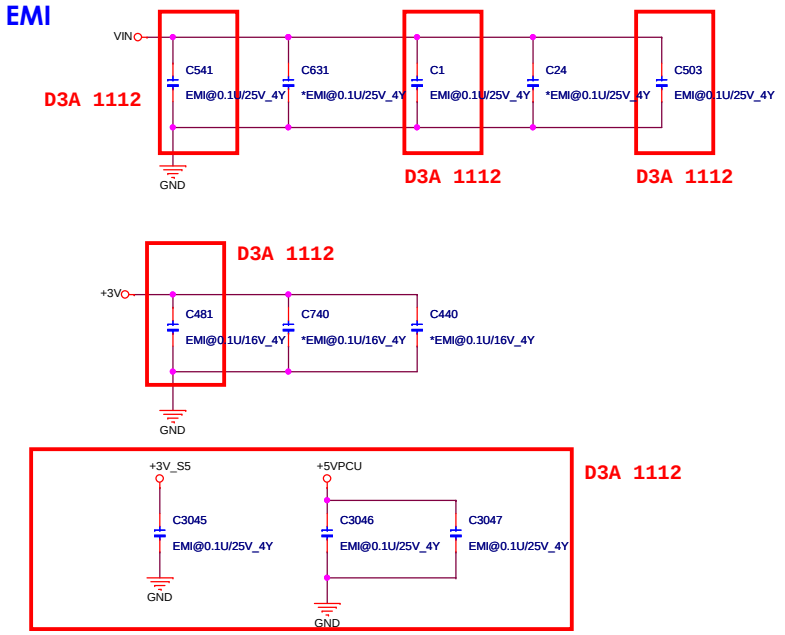
ODD Zero power . (Only for Intel) <OZP>



SATA HDD <HDD>



EMI



Quanta Computer Inc.		
PROJECT : BLB		
Size	Document Number: HDD/ODD/EMI	Rev: F3A
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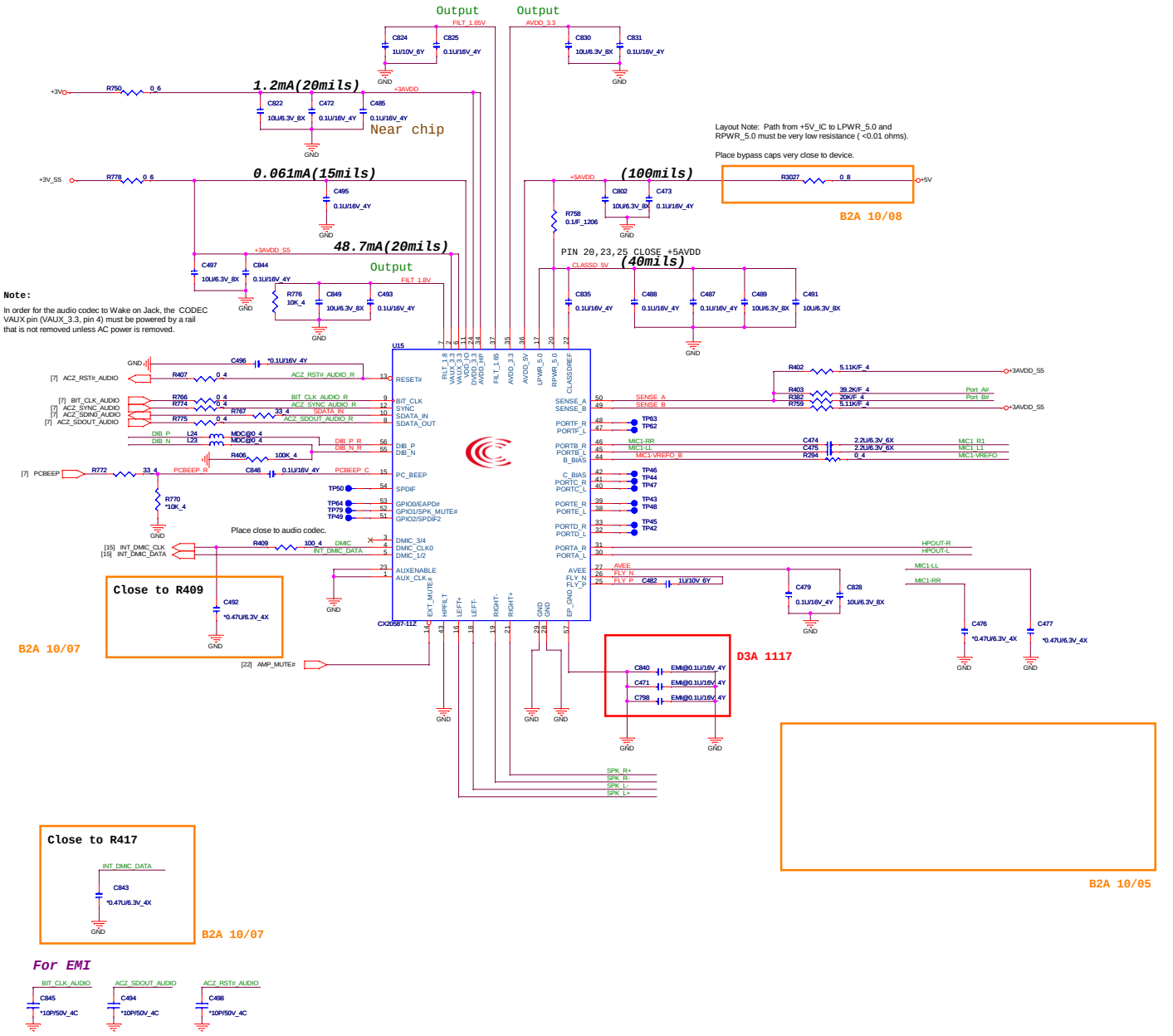
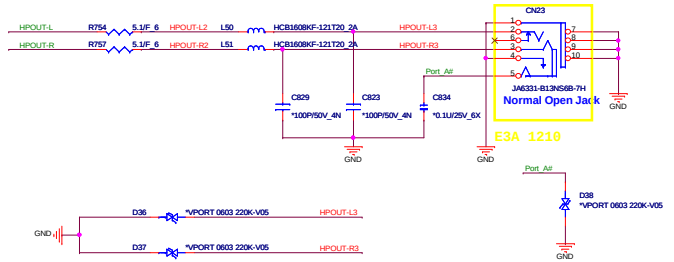
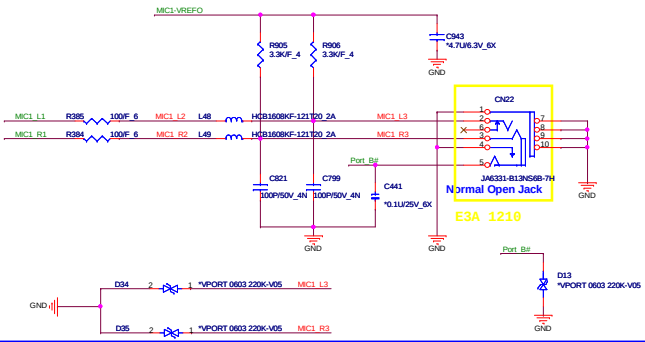


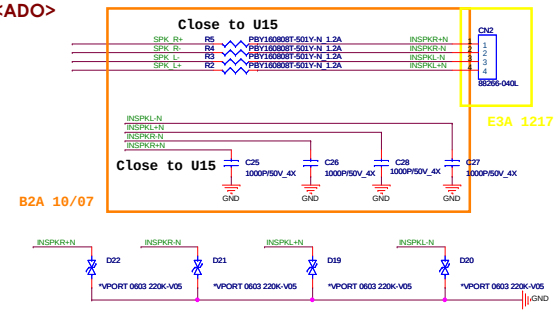
EXT H.P / Beats <ADO>



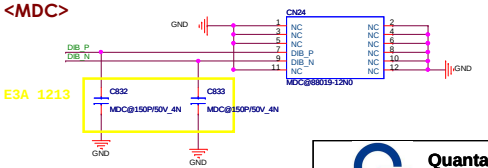
EXT MIC <ADO>



INT SPK <ADO>



MDC <MDC>



Quanta Computer Inc.
PROJECT : BLB

Size	Document Number	Rev
	Audio Codec (CX20587)	F3A
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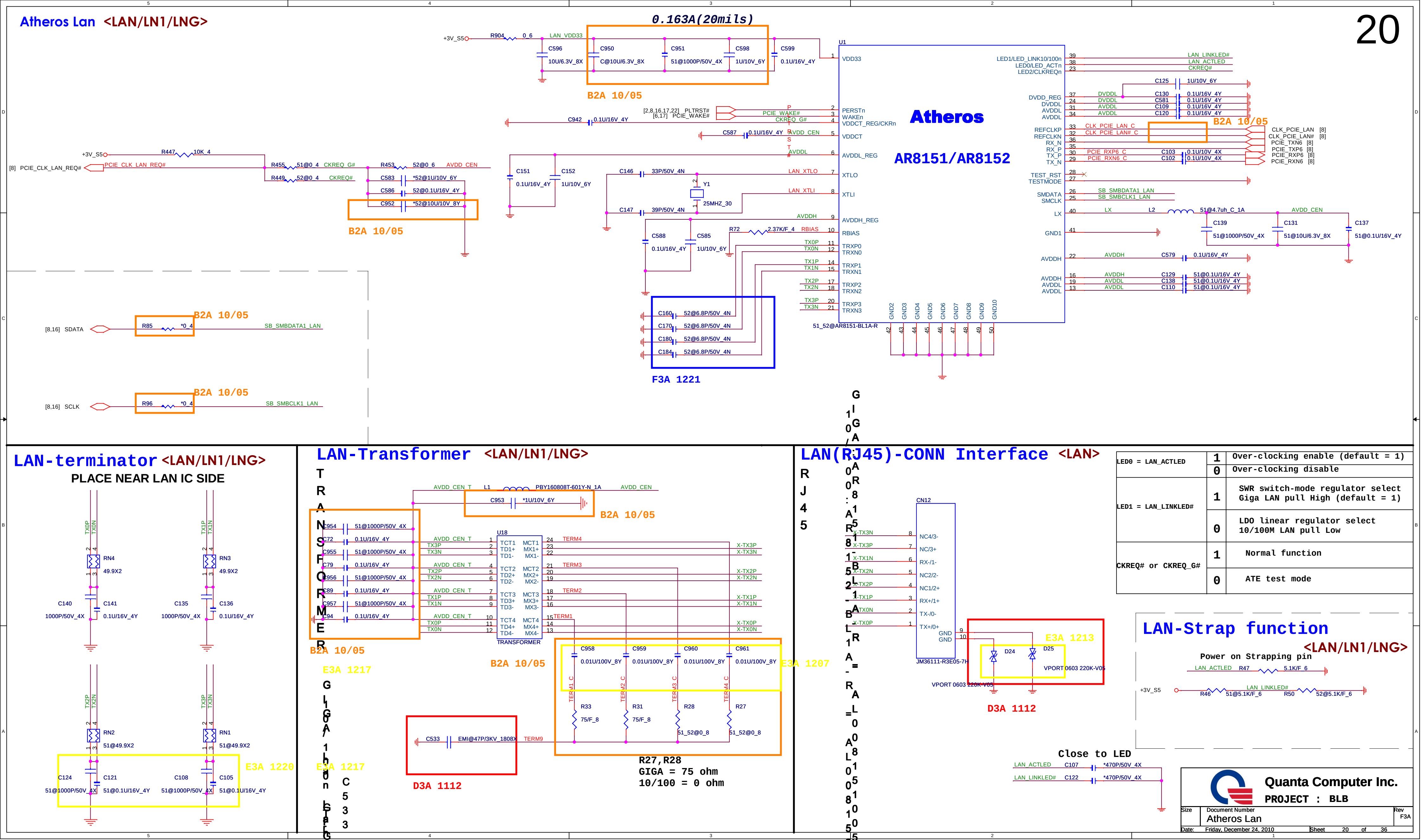
Atheros Lan <LAN/LN1/LNG>
20
0.163A(20mils)
B2A 10/05
Atheros
AR8151/AR8152
51_52@AR8151-BL1A-R
F3A 1221
LAN-terminator <LAN/LN1/LNG>
PLACE NEAR LAN IC SIDE
LAN-Transformer <LAN/LN1/LNG>
TRANSFORMER
LAN(RJ45)-CONN Interface <LAN>
JM36111-R3E05-7H
E3A 1220
E3A 1217
E3A 1207
E3A 1213
D3A 1112
R27,R28
GIGA = 75 ohm
10/100 = 0 ohm
LED0 = LAN_ACTLED | 1 | Over-clocking enable (default = 1)
| 0 | Over-clocking disable
LED1 = LAN_LINKLED# | 1 | SWR switch-mode regulator select Giga LAN pull High (default = 1)
| 0 | LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G# | 1 | Normal function
| 0 | ATE test mode
LAN-Strap function
<LAN/LN1/LNG>
Power on Strapping pin
Close to LED
Quanta Computer Inc.
PROJECT : BLB
Document Number
Atheros Lan
Rev F3A
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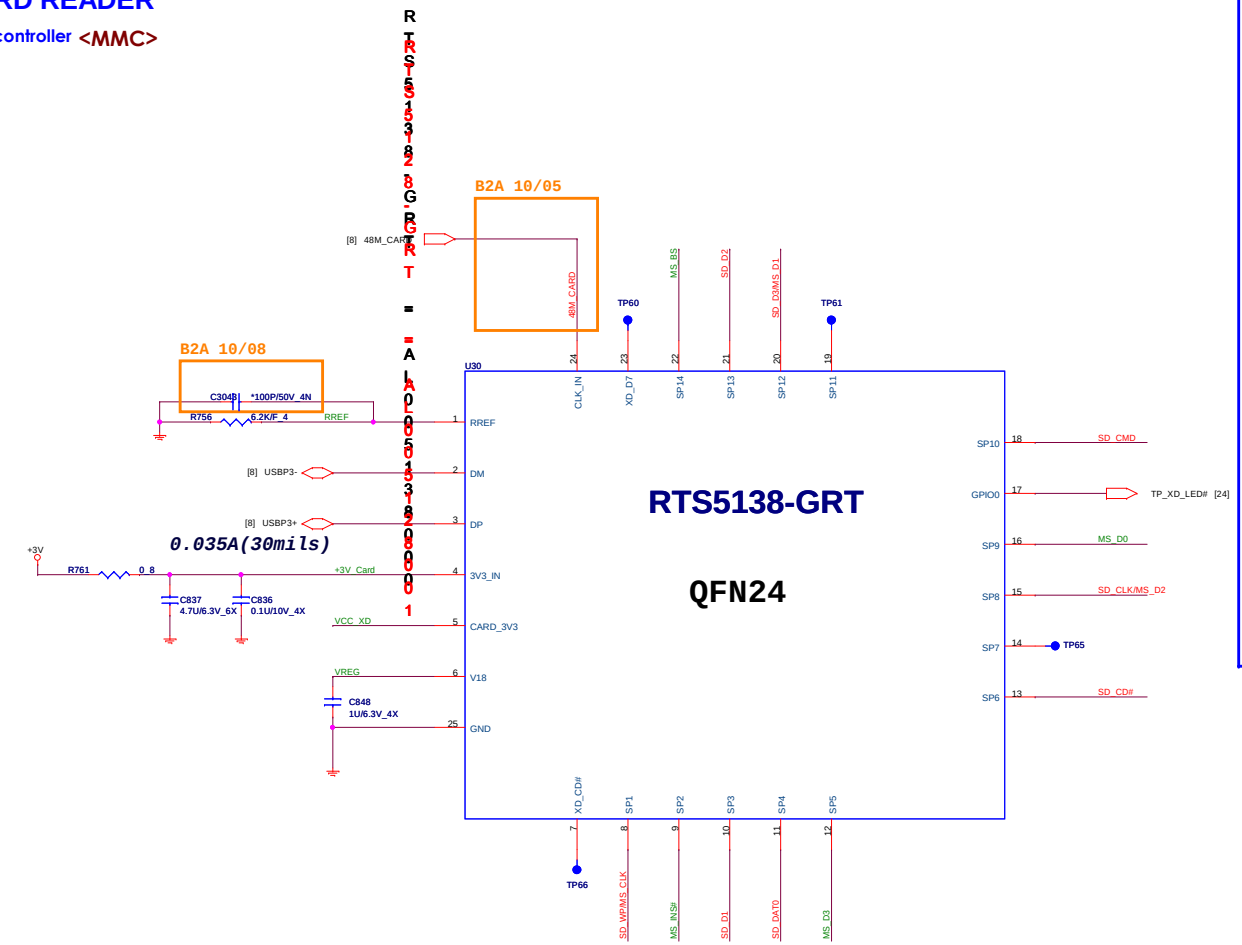
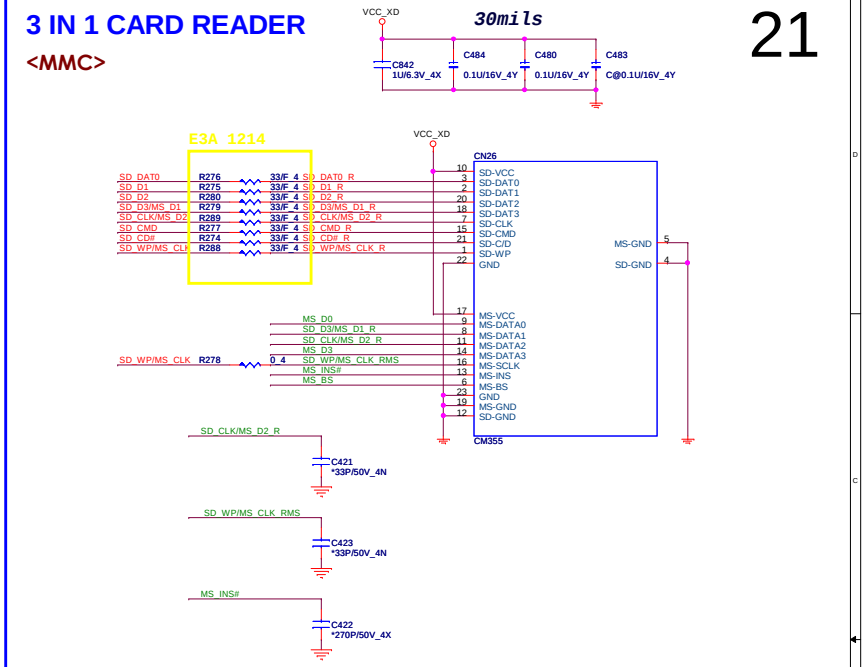
3 IN 1 CARD READER

Card reader controller <MMC>



3 IN 1 CARD READER

<MMC>



21

Quanta Computer Inc.

PROJECT : BLB

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	RTS5159 (Card Reader)	F3A

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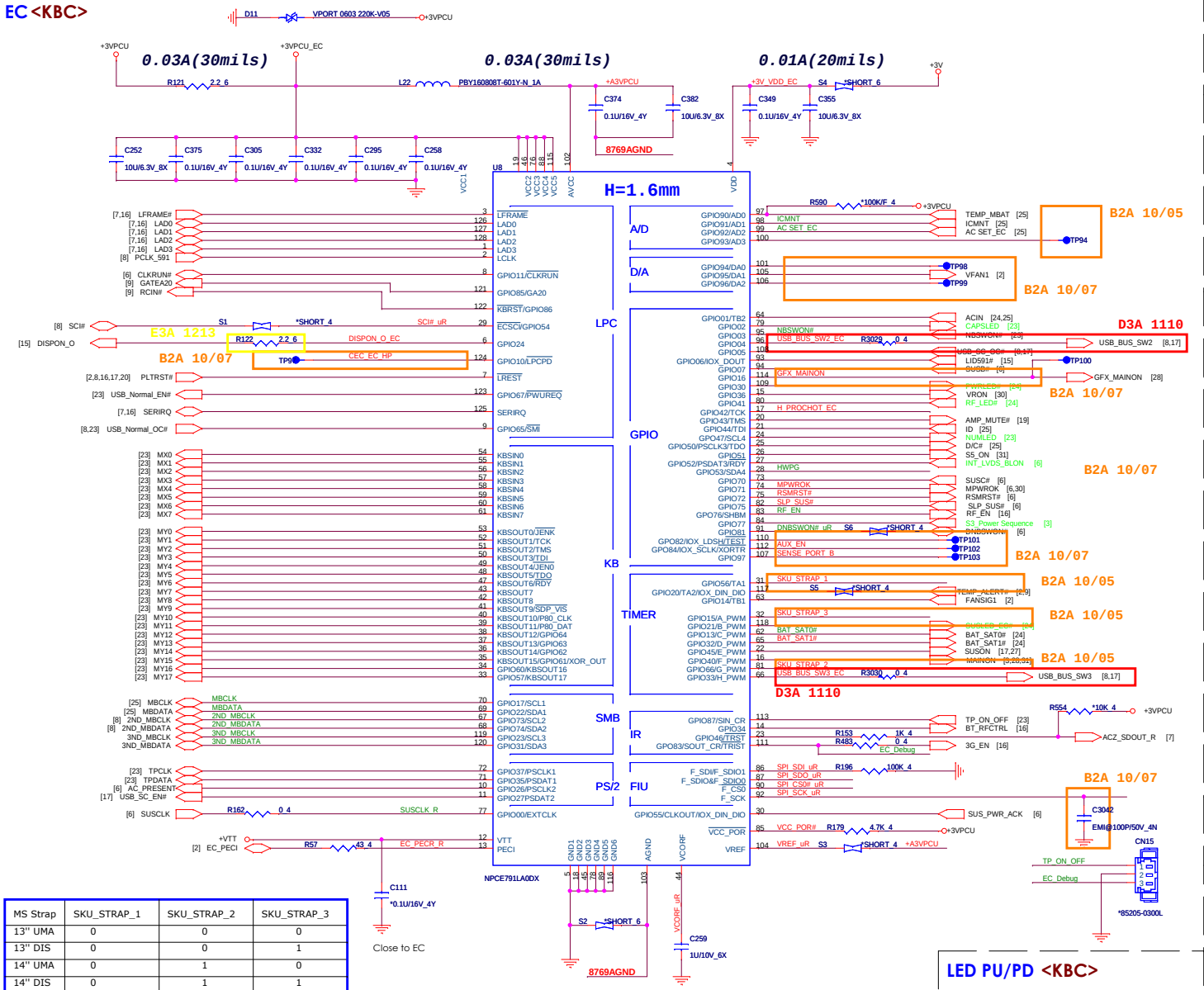
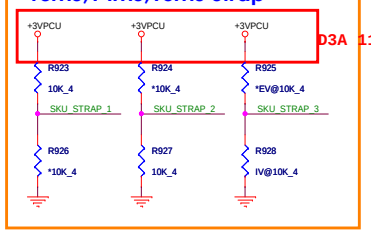
EC <KBC>



MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3
13" UMA	0	0	0
13" DIS	0	0	1
14" UMA	0	1	0
14" DIS	0	1	1
15" UMA	1	0	0
15" DIS	1	0	1

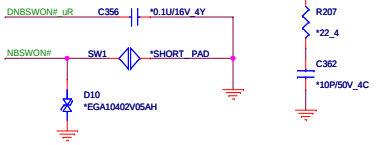
13MS,14MS,15MS Strap

B2A 10/07

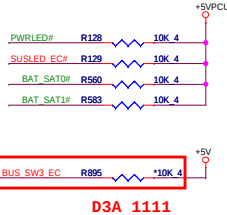


TP <KBC>

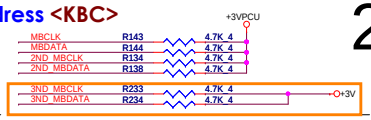
Close to U8



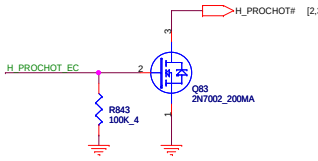
LED PU/PD <KBC>



SM BUS PU/Address <KBC>



Intel Turbo mode only <CPU>

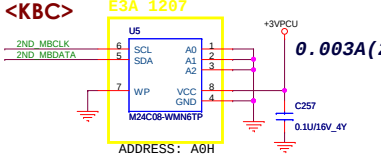


Strap <KBC>

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

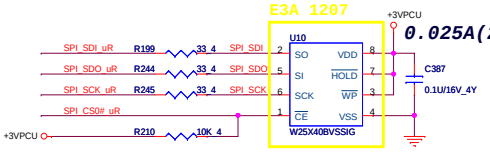
ID EEPROM <KBC>

E3A 1207



SPI FLASH <KBC>

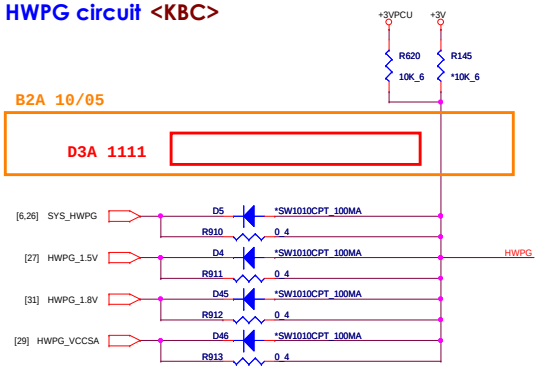
E3A 1207



Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

INTERNAL KEYBOARD STRIP SET <KBC>

HWPG circuit <KBC>



Quanta Computer Inc.
PROJECT : BLB

Size	Document Number	Rev
	EC-WPC8763LDG/WPC8769L(O)	F3A

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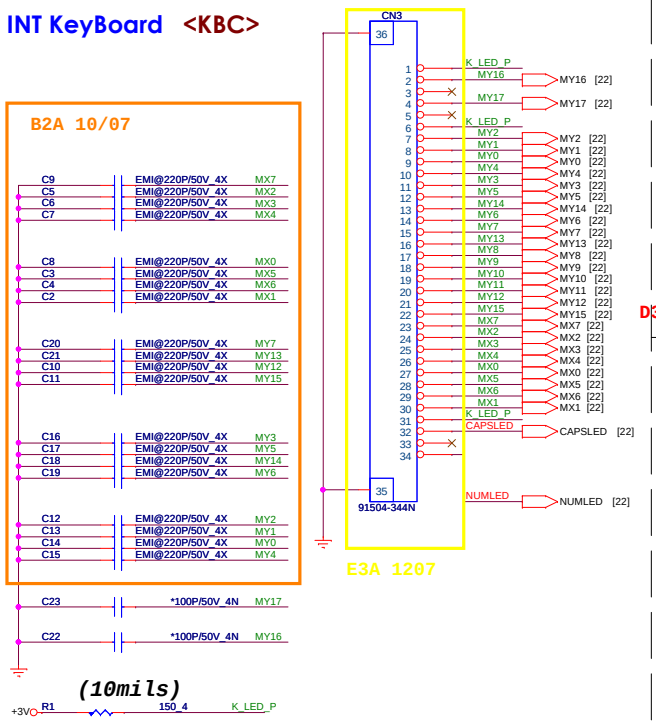
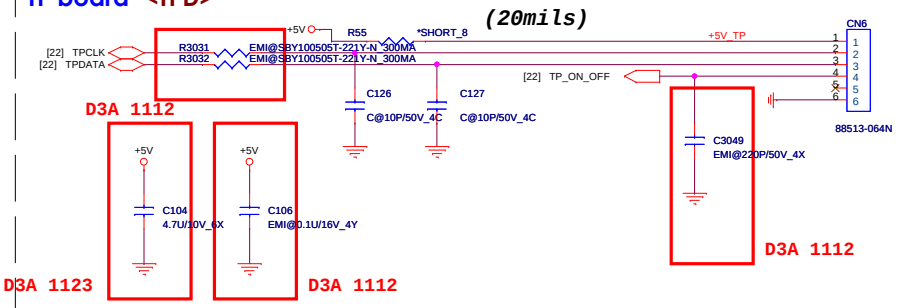
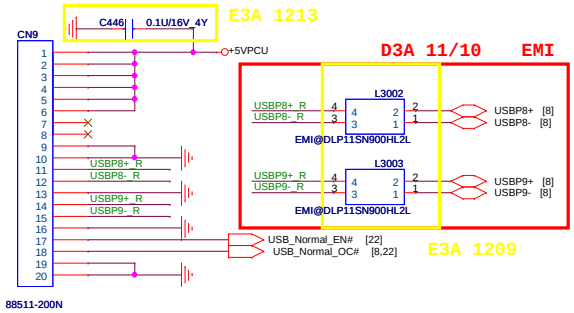
INT KeyBoard <KBC>



TP board <TPD>

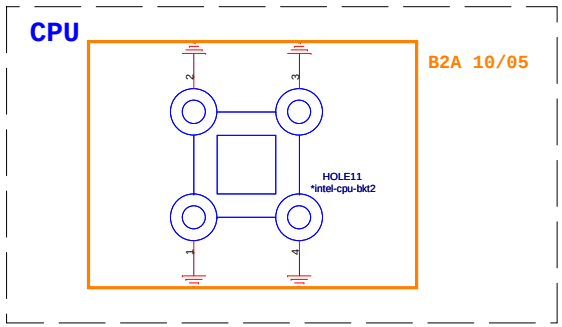


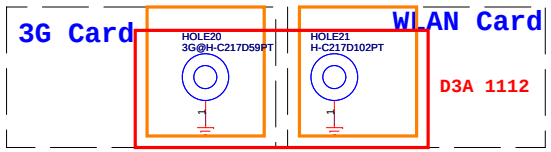
USB board <USB>

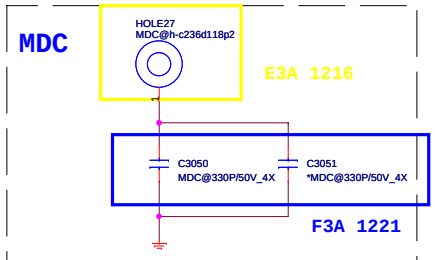


Power board <PSW>

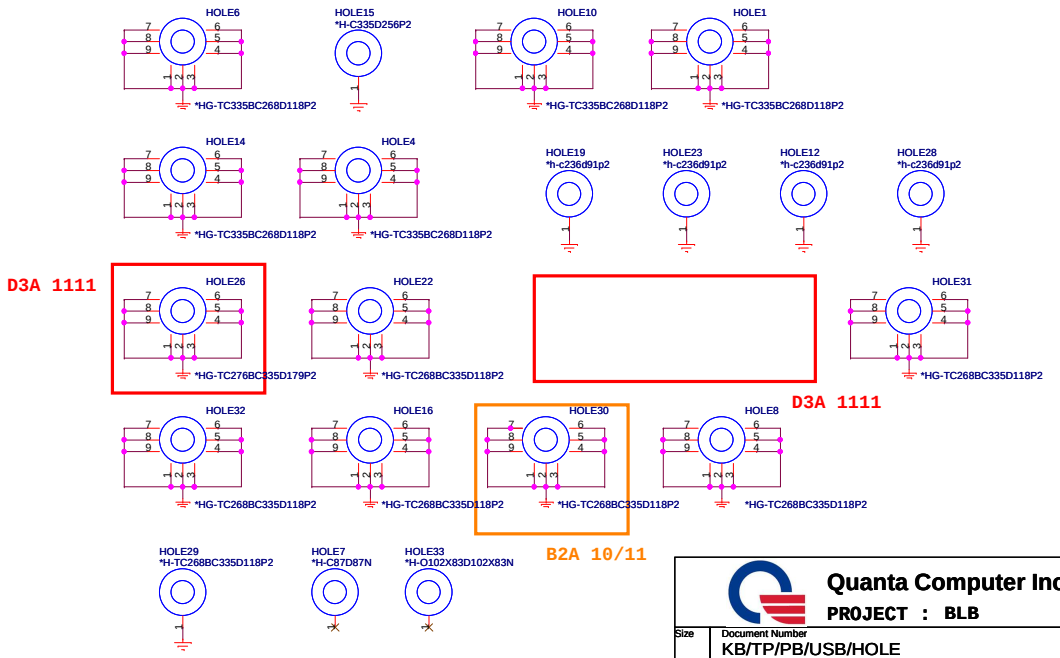
NUT







HOLE



Quanta Computer Inc.
PROJECT : BLB

Size	Document Number	Rev
	KB/TP/PB/USB/HOLE	F3A
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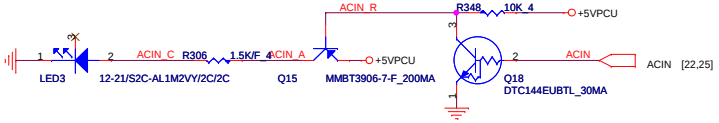
LED <LED>

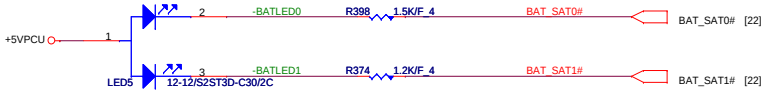
AC-IN



BATERRY

Full Charge = White

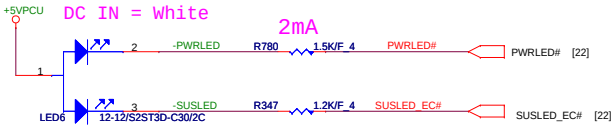
2mA



Charging = Orange

2mA

POWER

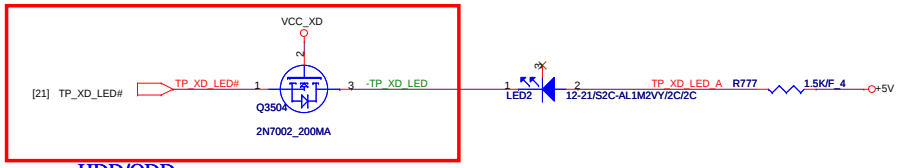


S3 Mode = Orange

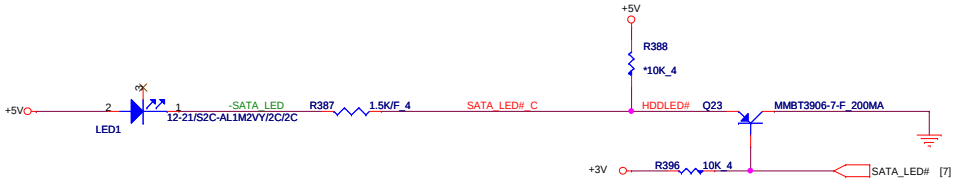
2mA

CARDREADER

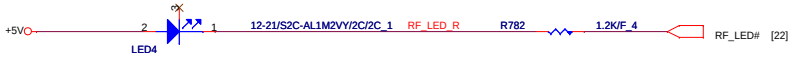
D3A 1110



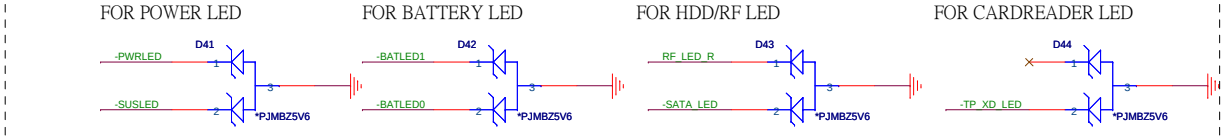
HDD/ODD



RF LED



ESD Protect



Quanta Computer Inc.

PROJECT : BLB

Size	Document Number	Rev
	LED	F3A

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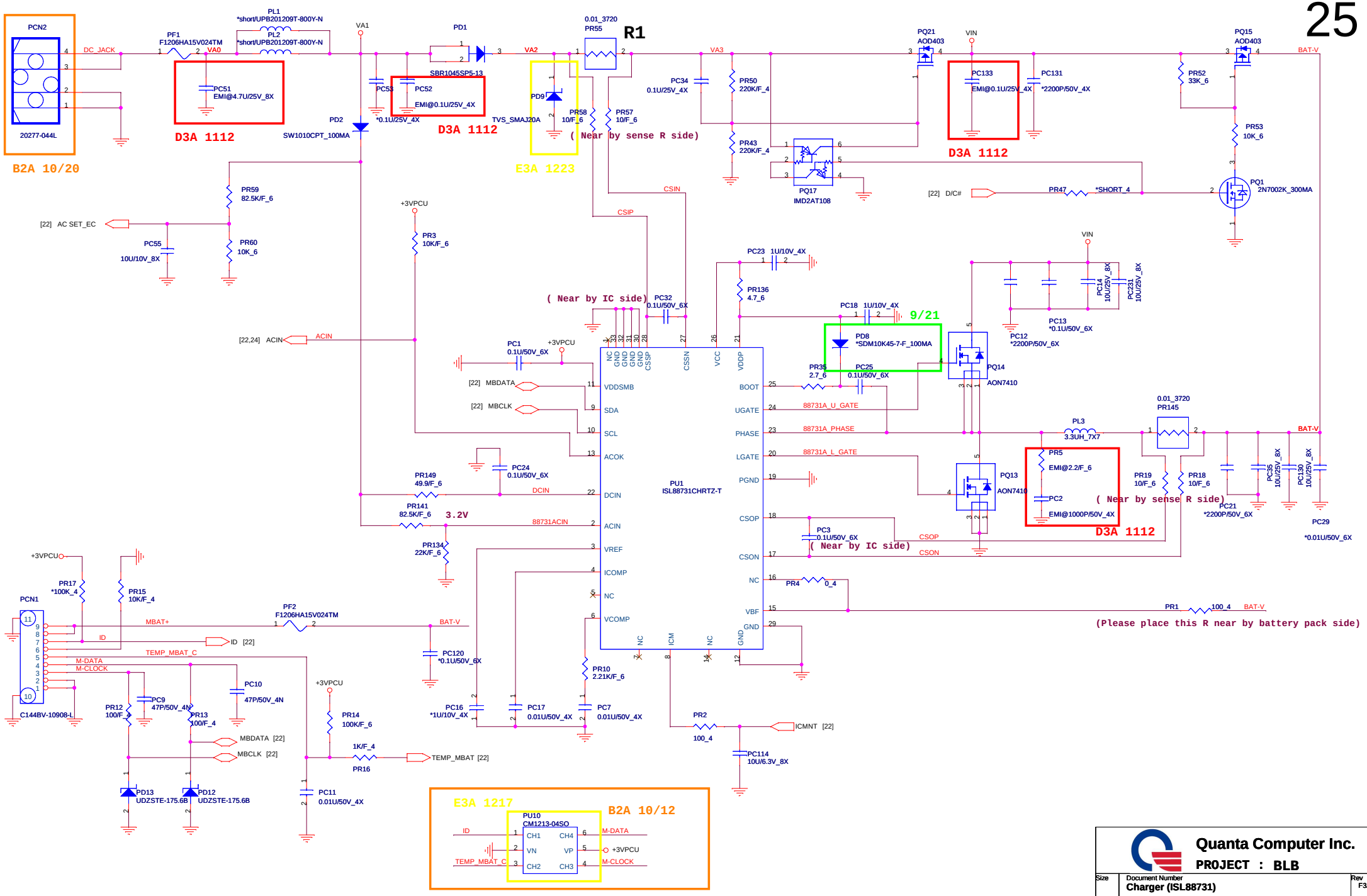
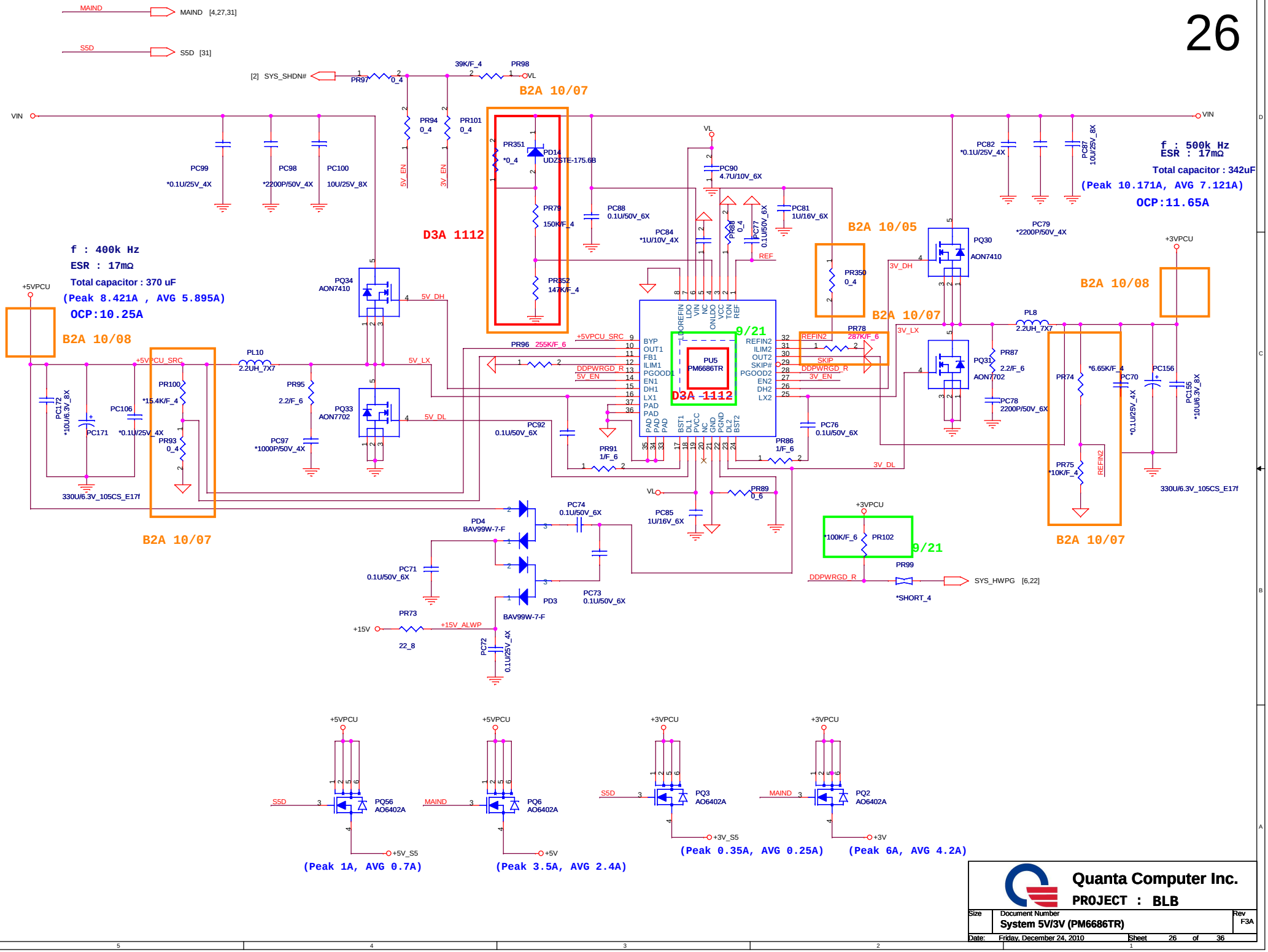
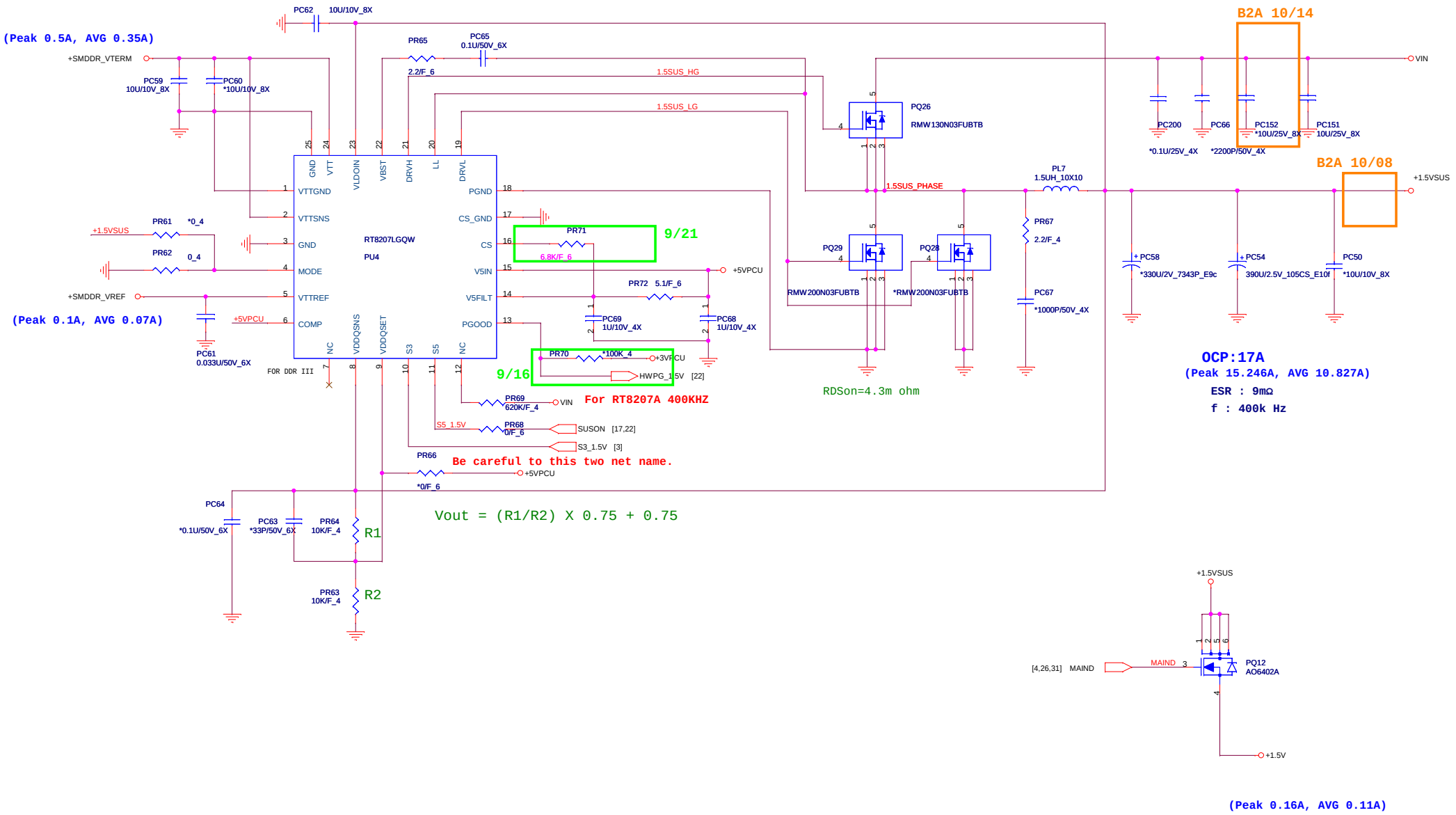


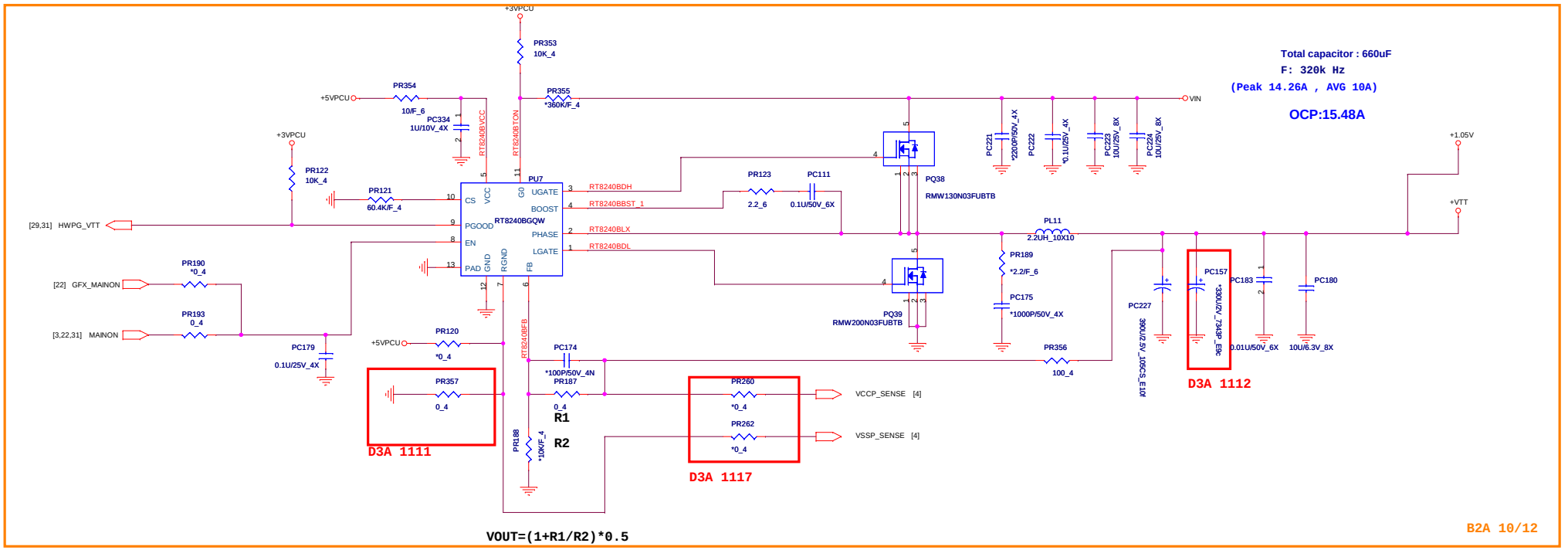
Quanta Computer Inc.			
PROJECT : BLB			
Size	Document Number: Charger (ISL88731)		Rev: F3A
Date: Friday, December 24, 2010		Sheet 25 of 36	



Quanta Computer Inc.		
PROJECT : BLB		
Size	Document Number: System 5V/3V (PM6686TR)	Rev: F3A
Date: Friday, December 24, 2010	Sheet 26 of 36	



Quanta Computer Inc.		
PROJECT : BLB		
Size	Document Number: DDR 1.5V(UP6163)	Rev: F3A
Date: Friday, December 24, 2010	Sheet 27 of 36	



Quanta Computer Inc.		
PROJECT : BLB		
Size	Document Number: +VTT /+1.05V(RT8240BGQW)	Rev: F3A
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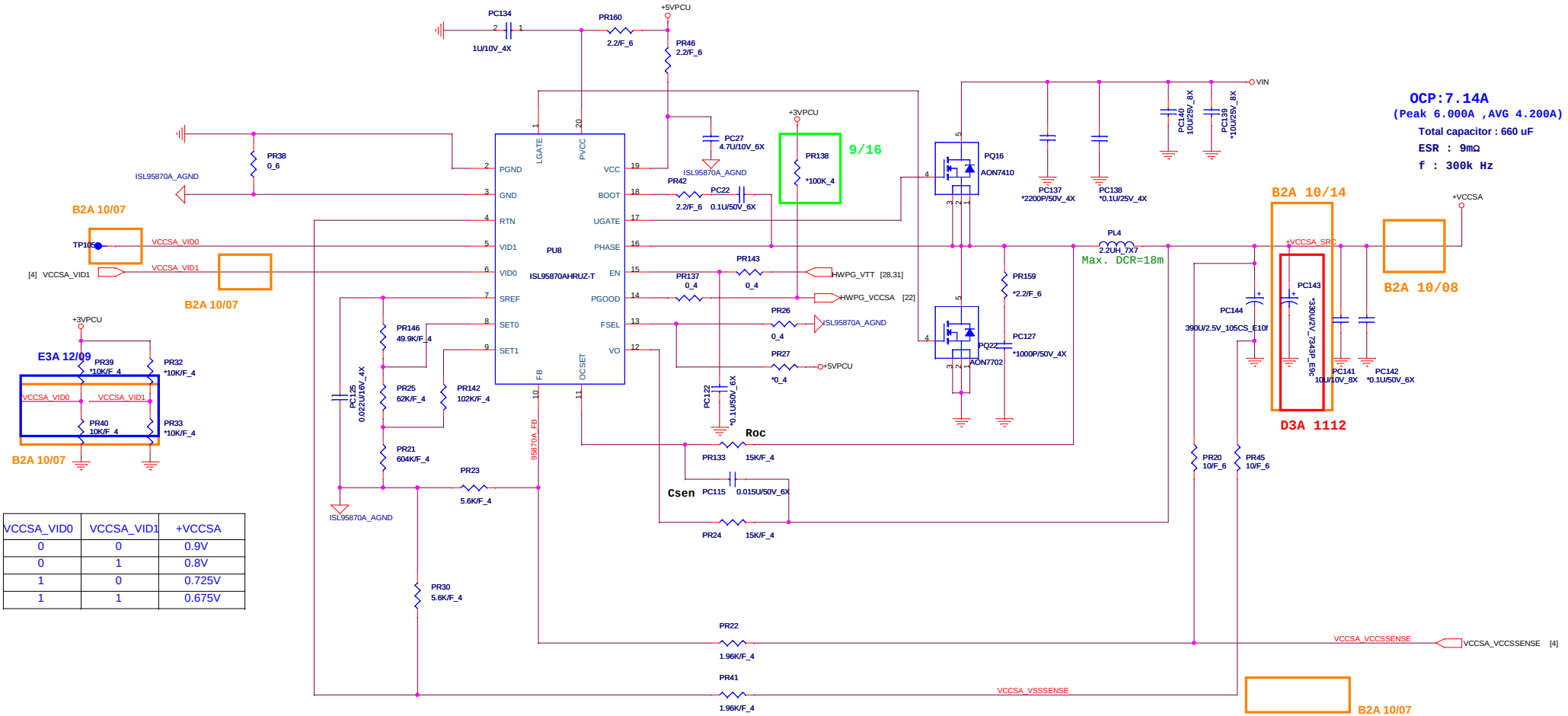

VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

Quanta Computer Inc.
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	+VCCSA ISL95870A)	F3A
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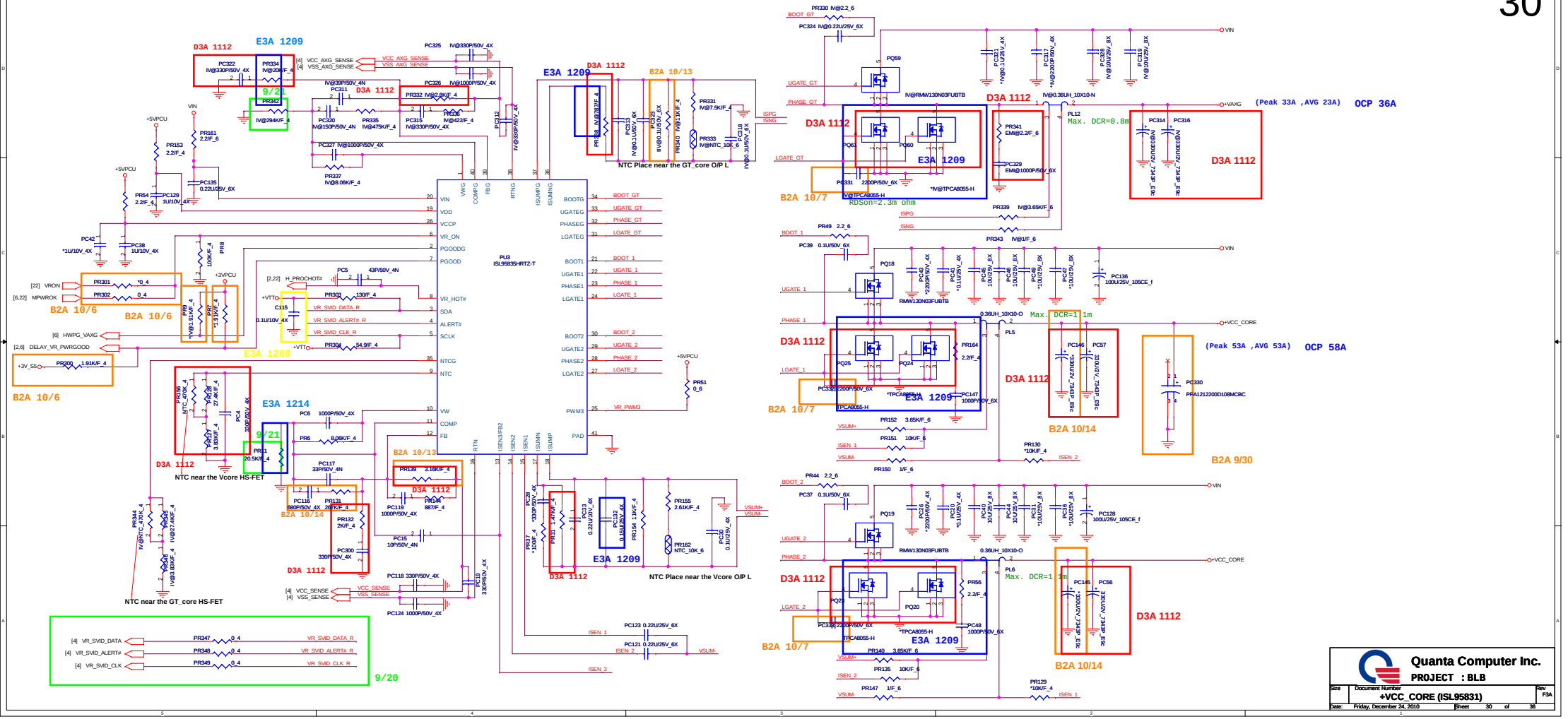

Quanta Computer Inc.			
PROJECT : BLB			
Size	Document Number		Rev
	+VCC_CORE (ISL95831)		F3A
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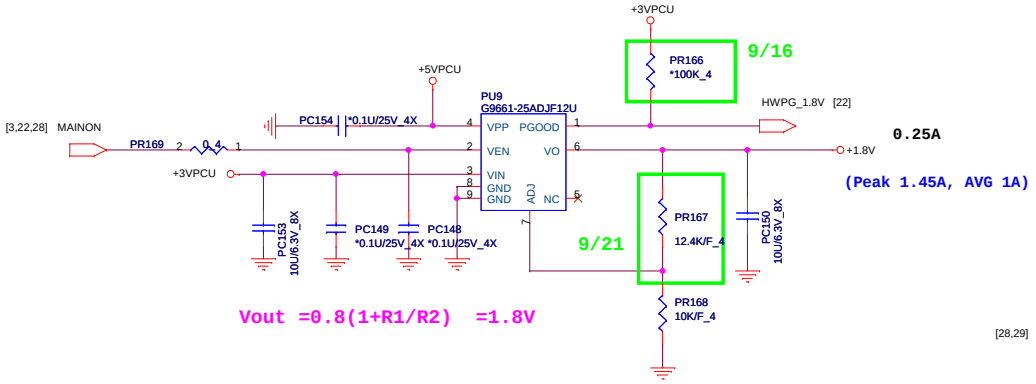

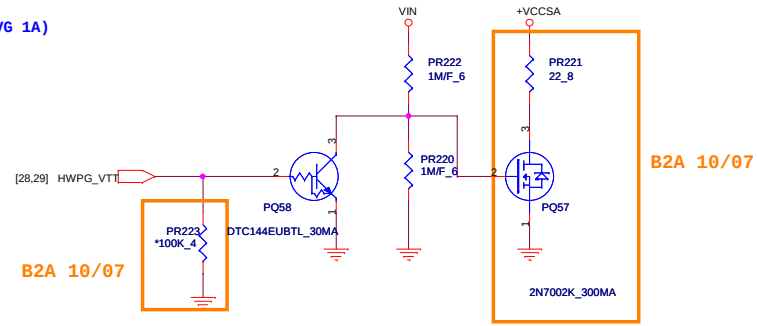

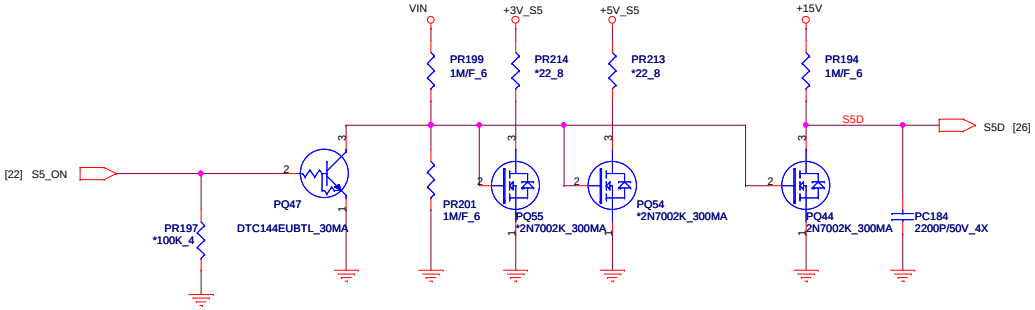

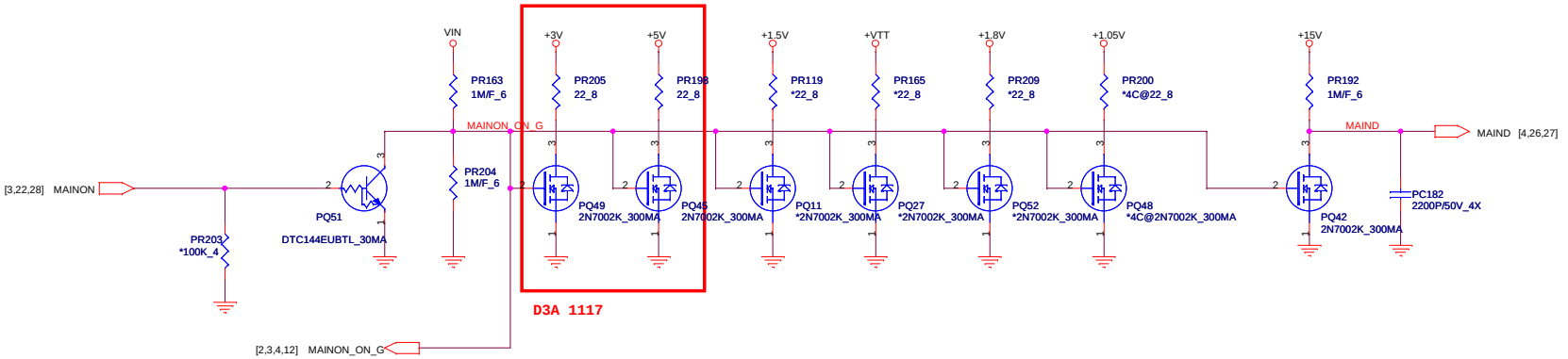

Quanta Computer Inc.

PROJECT : BLB

Size	Document Number	Rev
	Discharge (1.5V_S5/1.8V)	F3A

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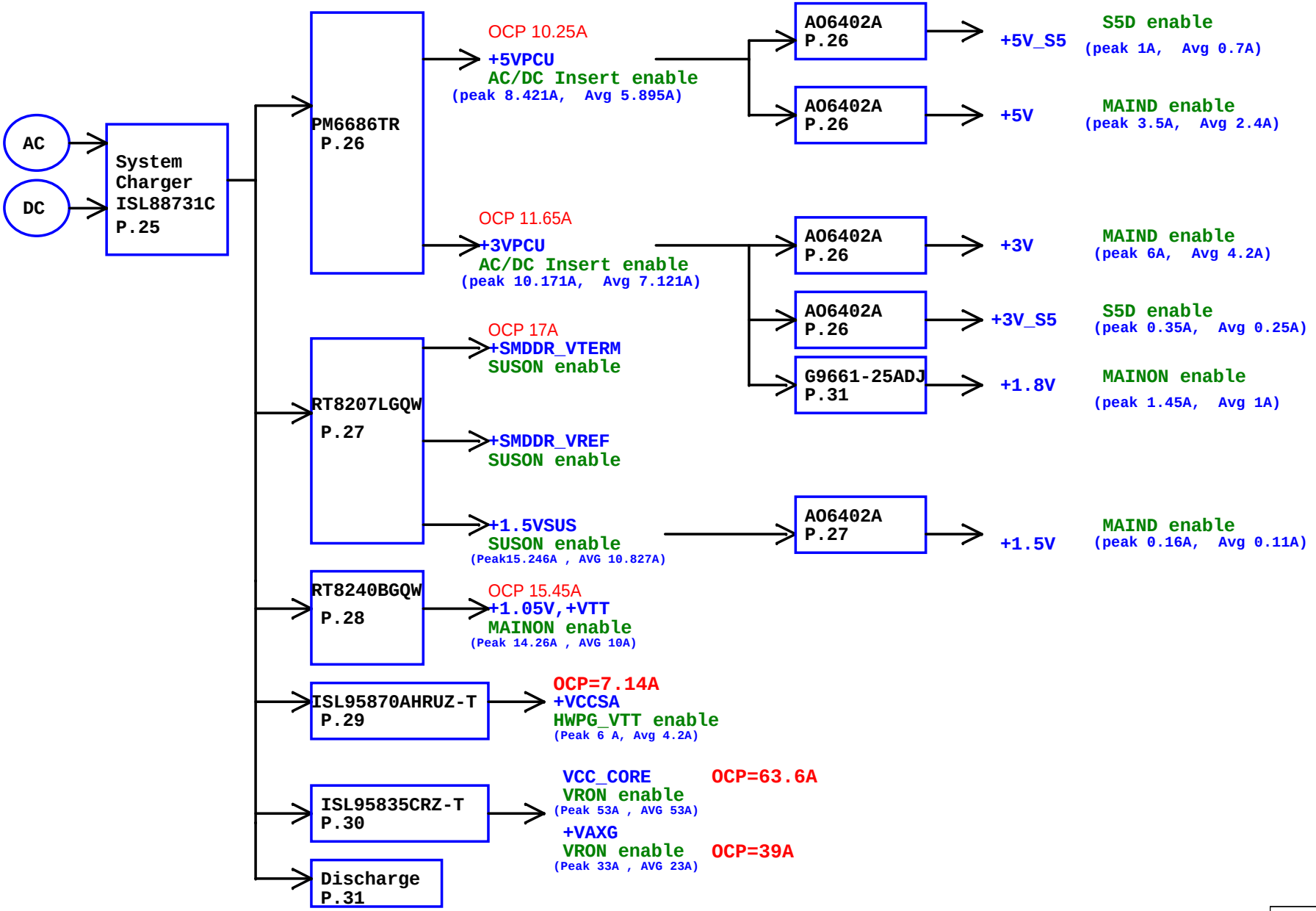

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Size	Document Number	Rev
	POWER TREE TABLE	F3A

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Model	REV	CHANGE LIST
BLB MB	B2A	PAGE 2 : Remove R14 and add TP89
		PAGE 2 : Remove R15
		PAGE 2 : Remove R439
		PAGE 2 : R441 change to 25.5 ohm 1% 0402
		PAGE 2 : Remove XDP; R106,R107,R102,R109,R98,R87,R78,R84
		PAGE 2 : Add R917 and Remove TP80,TP81,TP82,TP83,TP84,TP85,TP86,TP87,TP88,TP90
		PAGE 2 : Remove S3@ of R471
		PAGE 2 : Add R918 for non-S3 power reduction
		PAGE 3 : R550 change to 0 ohm 0402 for S3 power reduction sequence.
		PAGE 4 : Remove C71,C90 for cost down and C591,C592 add " * "no stuff.
		PAGE 4 : C563, C97 change to 10U/6.3V 0805 no stuff.
		PAGE 4 : Remove C649 for cost down
		PAGE 4 : C46, C519, C44, C45 change to 10U/6.3V 0805 no stuff.
		PAGE 4 : R894 stuff 100 ohm 0402 for power issue <Cann't power on>.
		PAGE 4 : Remove C633, C150,C160,C148,C170 for cost down
		PAGE 4 : C565, C168, C564, C159, C158, C177, C98, C99 change to 10U/6.3V 0805 no stuff.
		PAGE 4 : R463 add " * "no stuff.
		PAGE 4 : Remove R39
		PAGE 4 : Remove C576, C535 for cost down
		PAGE 4 : Remove R890 for VCCSA SENSE.
		PAGE 4 : Remove R890 and NET name "VCCSA_VID0" and R919 for VCCSA VID.
		PAGE 4 : Remove S3@ of R454
		PAGE 5 : Add TP91
		PAGE 5 : Remove R60, R56 and add TP92,TP93
		PAGE 5 : R74 add " * " no stuff.
		PAGE 6 : Remove R340, R682.
		PAGE 6 : R889, R344 add " * " no stuff.
		PAGE 7 : Remve R342, R325 and add TP95
		PAGE 8 : Remve R748, R749
		PAGE 8 : Change TP36 footprint to TP3050
		PAGE 8 : WLAN PCIE clock <CLK_PCIE_MINI# , CLK_PCIE_MINI, PCIE_CLK_MINI_REQ#> change to PCIE clock port1.
		PAGE 8 : USB 3.0 PCIE clock <CLK_PCIE_USB30# , CLK_PCIE_USB30, PCIE_CLK_USB30_REQ#> change to PCIE clock port5.
		PAGE 8 : Remove R247 and add T51,T52
		PAGE 8 : Remove C946,C947,R680
		PAGE 8 : R916 change PU to +3V_S5 for USB3.0 PCIE CLK
		PAGE 8 : R338 change PU to +3V for WLAN PCIE CLK
		PAGE 8 : Q19 and Q18 add " * " no stuff.
		PAGE 9 : Remove R305
		PAGE 9 : R845 change PD to GND for PCH GPIO1
		PAGE 9 : Change BOARD ID for USB3.0 and USB 2.0
		PAGE 10 : Reserve C948, C949 no stuff.
		PAGE 10 : Remove R673
		PAGE 10 :Change power source to +1.05V of V_PROC_IO, VCCDMI[2], VCCDMI[1]
		PAGE 10 : Add R3026 and L36, C714, C 700 add " * " no stuff for cost down.
		PAGE 12 : JDIM1 Change Main source P/N: DGMK4000087; 2nd source P/N: DGMK4000178
		PAGE 12 : Add C3038, C3039, C3040, C3041 for SI
		PAGE 13 : JDIM2 Change Main source P/N: DGMK4000005; 2nd source P/N: DGMK0000120
		PAGE 14 : Remove RN6,RN5,RN8,RN9 and add R3022, R3023, R3024,R3025 for EMI
		PAGE 15 : Remove R856
		PAGE 15 : Reserve D47 for ESD
		PAGE 15 : CN1 LVDS connector change footprint and PN:DFHS30FR015
		PAGE 15 : CN14 CRT connector change PN:DFDS15FR158
		PAGE 16 : Remove R205
		PAGE 16 : CN18 WLAN connector change PN:DFHD52MR016
		PAGE 16 : CN21 3G connector change PN:DFHD52MR032
		PAGE 16 : CN21 3G connector pin48, pin28,pin6 change power source +1.5V
		PAGE 16 : Add R921 and Reserve R920,Q94 for leakage
		PAGE 17 : USB3.0 change NEC solution
		PAGE 17 : Change power source +1.5VSUS for VIN of USB3.0 LDO
		PAGE 18 : Remove R77, R53 for cost down
		PAGE 19 : C492 close to R409; C843 close to R417; R2,R3,R4,R5,C25,C26,C27,C28 close to U15
		PAGE 19 : Remove L52 and Add R3027 for conexant suggest.
		PAGE 19 : Remove C29,C30,C31,C32 for conexant suggest.
		PAGE 20 : Add C950,C951,C952,C954,C955,C956,C957,C953 for Atheros suggest.

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PART NUMBER:	31BLBMB0IG0	DRAWING BY:		REVISON:	F3A

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Model	REV	CHANGE LIST
BLB MB	B2A	PAGE 20 : R85, R96 add " * "no stuff.
		PAGE 20 : Remove R450, R448 for cost down.
		PAGE 20 : Add C958,C959,C960,C961 for Atheros suggest.
		PAGE 21 : Remove R755 for cost down.
		PAGE 21 : Add C3043 for Realtek suggest.
		PAGE 22 : Remove R615,R614 and add TP97,TP94,TP98,TP99,TP96,TP100,TP101,TP102,TP103,TP104
		PAGE 22 : Add C3042 for EMI
		PAGE 22 : Add R923,R926,R924,R927,R925,R928 for SKU strap of EC code
		PAGE 22 : EC GPIO56 change to SKU_STRAP_1
		PAGE 22 : EC GPIO15 change to SKU_STRAP_3
		PAGE 22 : EC GPIO66 change to SKU_STRAP_2
		PAGE 22 : 3ND_MBCLK and 3ND_MBDATA change PU 4.7K to 3V
		PAGE 22 : Add D48, R922 for HWPG_VAXG
		PAGE 23 : C9,C5,C6,C7,C8,C3,C4,C2,C20,C21,C10,C11,C16,C17,C18,C19,C12,C13,C14,C15 remove " * " stuff for EMI.
		PAGE 23 : Hole11 change footprint: intel-cpu-bkt2
		PAGE 23 : Hole20 change PN to MBZK6002010
		PAGE 23 : Hole21 change PN to MBIM3001010
		PAGE 23 : Hole30 change footprint: HG-TC268BC335D118P2
		PAGE 25 : PCN2 change PN: DFHD04MS988
		PAGE 25 : Add PU10 for ESD
		PAGE 26 : Remove PJP6, PJP5 short pad
		PAGE 26 : PR100 add " * "no stuff and PR93 change to 0 ohm
		PAGE 26 : Add PD14 and PR352 no stuff and Add PR35
		PAGE 26 : Add PR350
		PAGE 26 : PR278 change to 287Kohm
		PAGE 26 : PR74, PR75 add " * "no stuff
		PAGE 27 : Remove PJP1
		PAGE 27 : PC152 add " * "no stuff
		PAGE 28 : +VTT/+1.05V change to RT8240BGQW solution.
		PAGE 29 : Remove PJP4
		PAGE 29 : PC143 add " * "no stuff
		PAGE 29 : Remove net :VCCSA_VSSSENSE
		PAGE 29 : Remove PR34,PR28 and add TP105
		PAGE 29 : PR40 add " * "no stuff
		PAGE 30 : PR301,PR9,PR7add " * "no stuff
		PAGE 30 : PR302,PR300,PC232remove " * " stuff
		PAGE 30 : PR139 change to 3.09K 1% 0402
		PAGE 30 : PR131 change to 267K 1% 0402
		PAGE 30 : PC116 change to 680P 50V 0402
		PAGE 30 : PC323 remove " * " stuff
		PAGE 30 : Add PC332,PC333,PC331,PC330
		PAGE 30 : PC145,PC146 add " * "no stuff
		PAGE 31 : PR223 add " * "no stuff
		PAGE 31 : PR221,PQ57 remove " * " stuff
	D3A	PAGE 3: R550 change to 100k and connect to U23 pin4.
		PAGE 4: Add R3028 and C3044 for S3 power reduction sequence.
		PAGE 4: R894 add " * "no stuff
		PAGE 4: Add R922, D48, R929, D49 power sequence.
		PAGE 7: Add G3.
		PAGE 8: Add R908, R909 for USB Sleep and Charge.
		PAGE 8: C784 change to 27pF.
		PAGE 8: C774 change to 33pF.
		PAGE 8: Net name change to USB_BUS_SW2_R abd USB_BUS_SW3_R.
		PAGE 8: R679 change to SBY100505T-221Y-N_300MA for EMI
		PAGE 8: Remove discrete VGA PCIE CLK " CLK_PCIE_VGA ; CLK_PCIE_VGA#"
		PAGE 9: R730 remove " * " for USB2.0 SKU Board_ID9 PD.
		PAGE 9: R721 remove " * " for no HDMI SKU
		PAGE 10: Remove R598.
		PAGE 10: Add C393 for LCD flicker.
		PAGE 14: R3022, R3023, R3024, R3025 add " * "no stuff .
		PAGE 15: Add L20 for EMI.
		PAGE 15: CN14 P/N change to DFDS15FR252.
		PAGE 17 :USB3.0 EEPROM U3001 Change Main source P/N: AKE37ZN0Q01; 2nd source P/N: AKE37FN0N01
		PAGE 17 :USB3.0 Chip U3003 Change to MP P/N: AJ202000T03

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PART NUMBER:	31BLBMB0IG0	DRAWING BY:		REVISON:	F3A

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Model	REV	CHANGE LIST
BLB MB		
	D3A	PAGE 17 : Add L73 for EMI.
		PAGE 18 : C603 add " * " no stuff for ODD zero power.
		PAGE 18 : Add R614, Q3503 for ODD zero power.
		PAGE 18 : C541, C1, C503, C481remove " * " stuff for EMI.
		PAGE 18 : Add C3045, C3046, C3047, C589, C594 for EMI.
		PAGE 19 : C840, C471, C798 remove " * " stuff for EMI.
		PAGE 20 : C533 change to 47p for EMI.
		PAGE 20 : Add C30458 for EMI.
		PAGE 22: Add R3029, R3030 for USB Sleep and Charge.
		PAGE 22: R923, R924, R925 change to PU to +3VPCU.
		PAGE 22: R895 add " * " no stuff
		PAGE 22: R536,R535 change to 4.7K
		PAGE 23 : Add L3002,L3003, C3049, R3031, R3032 , C106 for EMI.
		PAGE 23 : C104 remove " * " stuff
		PAGE 23 : HOLE20, HOLE21, HOLE26 change footprint.
		PAGE 23 : Remove Hole5, Hole9
		PAGE 24 : Remove Q22 and add Q3504 for card reader LED.
		PAGE 25 : PC51, PC52, PC133, PR5, PC2 stuff for EMI.
		PAGE 26 : PD14 remove " * " stuff.
		PAGE 26 : PR351 add " * " no stuff.
		PAGE 26 : PR79 change to 150K ohm 1%
		PAGE 26 : PR352 change to 147K ohm 1%
		PAGE 26 : PU5 Change Main source P/N: AL006686000; 2nd source P/N: AL006188000
		PAGE 28 : Add PR357, PC157.
		PAGE 28 : PR260, PR262 add " * " no stuff.
		PAGE 29 : PC143 change to 330U/2V_7343P_E9c.
		PAGE 30 : PR338 change to 750 ohm 1%
		PAGE 30 : PR332 change to 2.8K ohm 1%
		PAGE 30 : PR322 change to 330p 50V
		PAGE 30 : PR334 change to 2K ohm 1%
		PAGE 30 : PR31 change to 1.47K ohm 1%
		PAGE 30 : PR139 change to 3.16K ohm 1%
		PAGE 30 : PR132 remove " * " stuff.
		PAGE 30 : PC300 remove " * " stuff.
		PAGE 30 : PR156, PR127, PR128, PC4 remove " * " stuff.
		PAGE 30 : PQ23, PQ20, PQ24, PQ25, PQ60, PQ61 Change Main source P/N: BAM02000000 ; 2nd source P/N: BAM14120000
		PAGE 30 : PC145, PC56, PC146, PC57, PC314, PC316 change to 330U/2V_7343P_E9c.
		PAGE 30 : PR341, PC329 stuff for EMI.
		PAGE 31 : Add PR205, PQ49, PR198, PQ45.
	E3A	PAGE 2 : Add C113,C114,C117 for ESD
		PAGE 4 : Add R930
		PAGE 4 : C606 remove " * " stuff.
		PAGE 4 : Change the C591 to 330uF .
		PAGE 4 : Add C116 for ESD
		PAGE 6 : R922 remove " * " stuff.
		PAGE 6, 7, 8, 9, 10, 11 : PCH U25 change to AJSLH9D0T06
		PAGE 7: U29 change to AKE391P0N00
		PAGE 7 : Add C86 for ESD
		PAGE 10: Add C69, C71,C78,C81,C82,C90,C92,C112,C118,C119,C123,C132,C133,C134 for ESD
		PAGE 15: MR1 remove 2ND soucre AL002618001, add 2ND soucre AL003661003
		PAGE 15: L20 change footprint.
		PAGE 16 : C720 remove " * " stuff.
		PAGE 16 : Add R883
		PAGE 16 : R644 remove " * " stuff
		PAGE 16 : R605,R648,R649,R568,R569,R570,R571,R572 add " * " no stuff
		PAGE 17 : CN3000 change footprint to usb-020053gr009m5176r-9p-smt
		PAGE 17: U3001 change to AKE37ZN0Q01
		PAGE 17: L73 change footprint.
		PAGE 17 : R3020 change to 1.47k.
		PAGE 17 : C3036, C3035 change to 15pf
		PAGE 19 : CN2 change P/N to DFHD04MR752
		PAGE 19 : CN22,CN23 change footprint.
		PAGE 19 : C832 and C833 change to 150p for EMI
		PAGE 20 : C958,C959,C960,C961 change to 0.01U/100V 0805

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	PART NUMBER:	31BLBMB0IG0	DRAWING BY:		REVISON:	F3A

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Model	REV	CHANGE LIST
BLB MB	E3A	PAGE 20 : Remove C3048 and add D24,D25 for ESD
		PAGE 21 : R276,R275,R280,R279,R289,R277,R274,R288 change to 33ohm for EMI.
		PAGE 22: U10 change to AKE37FN0N01
		PAGE 22: U5 remove 2ND soucre AKE3K8B0Y17
		PAGE 22 : Add R122 for ESD
		PAGE 23: CN3 remove 2ND soucre DFFC34R002
		PAGE 23: HOLE2, HOLE3 ,Hole27 change footprint and P/N.
		PAGE 23: L3002, L3003 change footprint.
		PAGE 23 : C446 remove " * " stuff for EMI.
		PAGE 30 : Add C115 for ESD
		PAGE 30 : Change the PC132 to 0.15uF from 0.1uF.
		PAGE 30 : Change the PR338 to 787Ohm from 750Ohm
		PAGE 30 : Change the PR334 to 20kOhm from NC.
		PAGE 04 : Change the C95,C149 to 22uF from 10uF.
		PAGE 04 : Change the C98,C99 to 22uF from NC.
		PAGE 29 : PR40 *10K/F_4 Change the 10K/F_4
		PAGE 30 : PR11 change to 20.5k
		PAGE 25 : Add PU10 for ESD
		PAGE 20 : C124,C121,C108,C105 add "51@" for Giga LAN
		PAGE 17 : D3000 ,Y3000,U44 remove 2ND source.
		PAGE 25 : PD9 remove 2ND source.
	F3A	PAGE 9 : NET: ODD_PRSNT# change to PCH pin U2 <SATA4GP/GPIO16>
		PAGE 9 : NET: BOARD_ID9 change to PCH pin M5 <SATA3GP/GPIO37>
		PAGE 8 : R358 add "*" no stuff.
		PAGE 8 : R847 remove "S3@" and stuff.
		PAGE 23 : Add C3050, C3051 for EMI
		PAGE 20 : Add C160,C170,C180,C184 for EMI

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