BU1 Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

- VCC_CORE
- +1.5V
- +1.05V
- +1.25V
- +1.8VSUS
- +3VPCU
  +3V_S5
  +3VSUS
  +3V
  +5VPCU
  +5V_S5
  +5V
  SMDDR_VTERM
  SMDDR_VREF

Intel
Merom
(35W)
Page 3,4

FSB(667/800MHZ)

CLOCK GENERATOR
CK505
ICS9LPR363
Page 2

Crestline GM
Page 5,7,8,9,10,11

R.G.B
LVDS X1
533/ 667 MHZ DDR II

DDRII-SODIMM1
DDRII-SODIMM2
Page 12,13

CRT
Page 18

LCD(WXGA 13W)
Page 18

SATA
PATA

SATA - HDD
Page 19
G SENSOR

IDE - ODD
Page 19

DMI(x2/x4)

ICH8M
Page 14,15,16,17

PCI-Express

MINI CARD
WLAN
Page 23

MINI CARD
Page 23 (BOT)

NEW CARD
Page 24 (BOT)

100/10 LAN
RTL8101E
Page 20

Connector

RJ11/RJ45/USB DAUGHTER BOARD

RJ45 **RJ11** **USB**

USB 2.0

DAUGHTER BORD

- System 0 — Page 24 — USB PORT 0
- System 1 — Page 24 — USB PORT 1
- System 2 — Page 24 — USB PORT 2
- WLAN — Page 23 — USB PORT 3
- Finger Printer (BOT) — Page 24 — USB PORT 4
- Bluetooth (BOT) — Page 24 — USB PORT 5
- New Card (BOT) — Page 24 — USB PORT 6
- Reserved (BOT) — Page 23 — USB PORT 7
- Camera (BOT) — Page 18 — USB PORT 8

Azalia

PCI Bus

LPC

32.768KHz

PCMCIA Controller (CB 1410)
Page 21 (BOT)

Card Reader/1394 (R5C833)
Page 22

PCMCIA
(BOT)

5 IN 1

1394
(BOT)

WPC8763LDG
Page 26

FAN **Touch PAD** **Key Board** **FLASH ROM**

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#,INTB#	R5C832
REQ1# / GNT1#	AD20	INTC#	CB1410

AUDIO/FM/USB DAUGHTER BOARD

HP **INT SPK** **USB**

HP AMP **SPK AMP**

AUDIO CODEC (ALC262)

MDC 1.5
Page 25

Connector

RJ11

BTO BOM OPTION

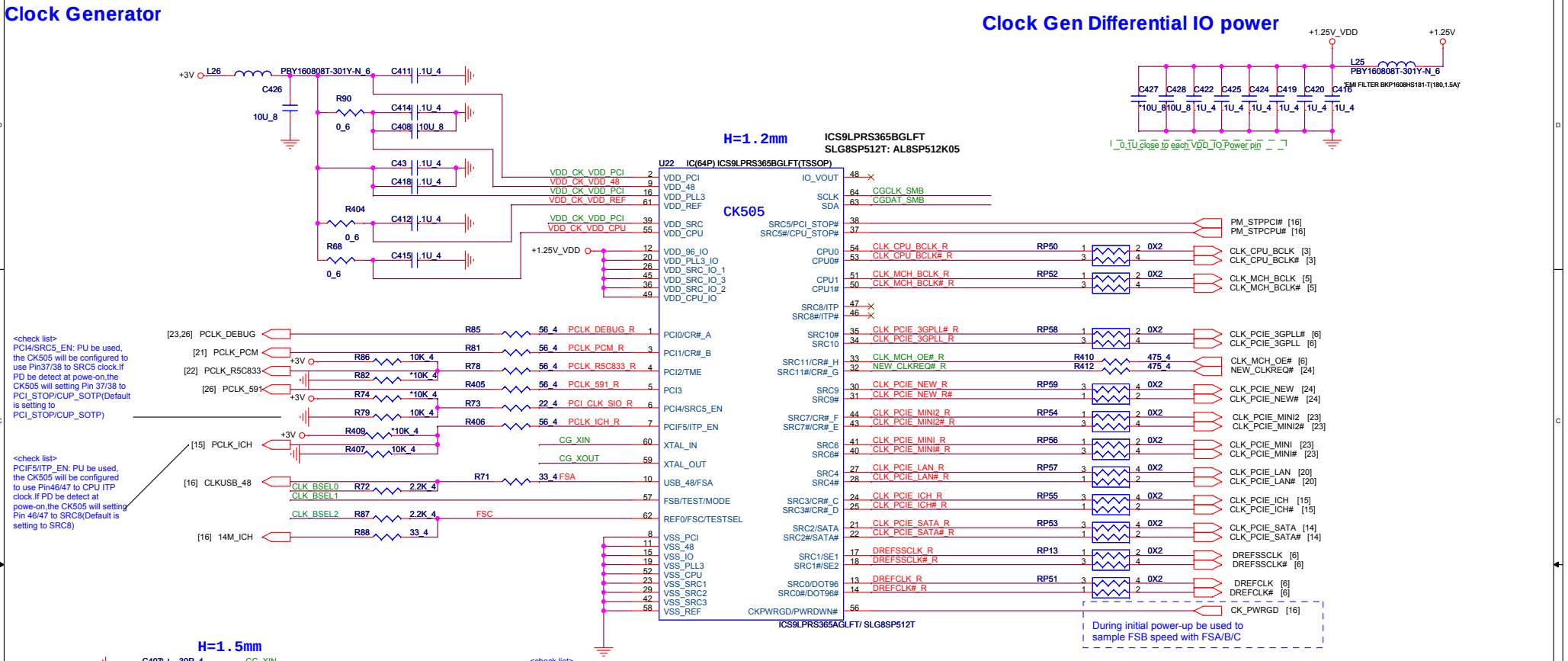
```
CB@ : CARD BUS
FP@ : FINGER PRINTER
BT@ : BLUETOOTH
CM@ : CAMERA
GS@ : G-SENSOR
NEW@ : NEW CARD
LCD@ : LCD TYPE PANEL
LED@ : LED TYPE PANEL
1394@ : 1394
```

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	Block Diagram	1A

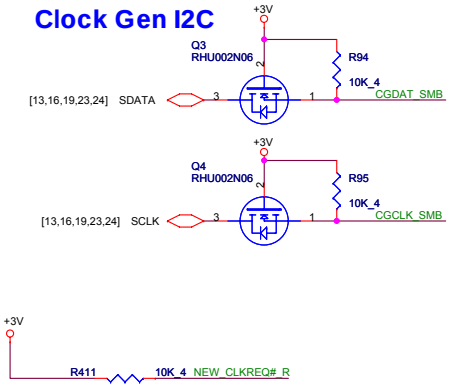
Date: Monday, March 26, 2007 Sheet 1 of 33

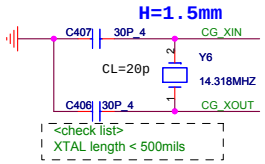
Clock Generator



Clock Gen Differential IO power

Clock Gen I2C





<check list>
(1)PCI2/TME: PU be used, the CK505 cannot over clock any of the clock for Trust Mode security purposes.

(2)PCI4/SRC5_EN: PU be used, the CK505 will be configured to use Pin37/38 to SRC5 clock.
If PD be detect at powe-on,the CK505 will setting Pin 37/38 to PCI_STOP/CUP_SOTP
(Default is setting to PCI_STOP/CUP_SOTP)

(3)PCIF5/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock.
If PD be detect at powe-on,the CK505 will setting Pin 46/47 to SRC8
(Default is setting to SRC8)

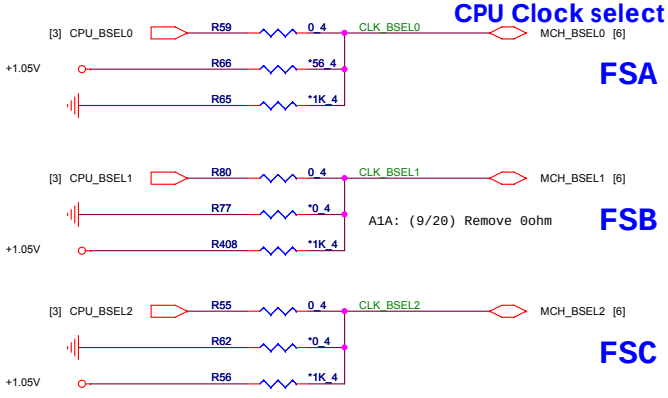
(4)SLG8SP512 Pin 6 select Pin 17, 18 output is LCDCLK or 27 M, PD is LCDCLK, PU is 27 M ,
Pin 37, 38 will fixed be use CPU_Stop and PCI_Stop.

(5)SLG505YC64 CK505 Standar parts follow standar setting

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

CPU Clock select



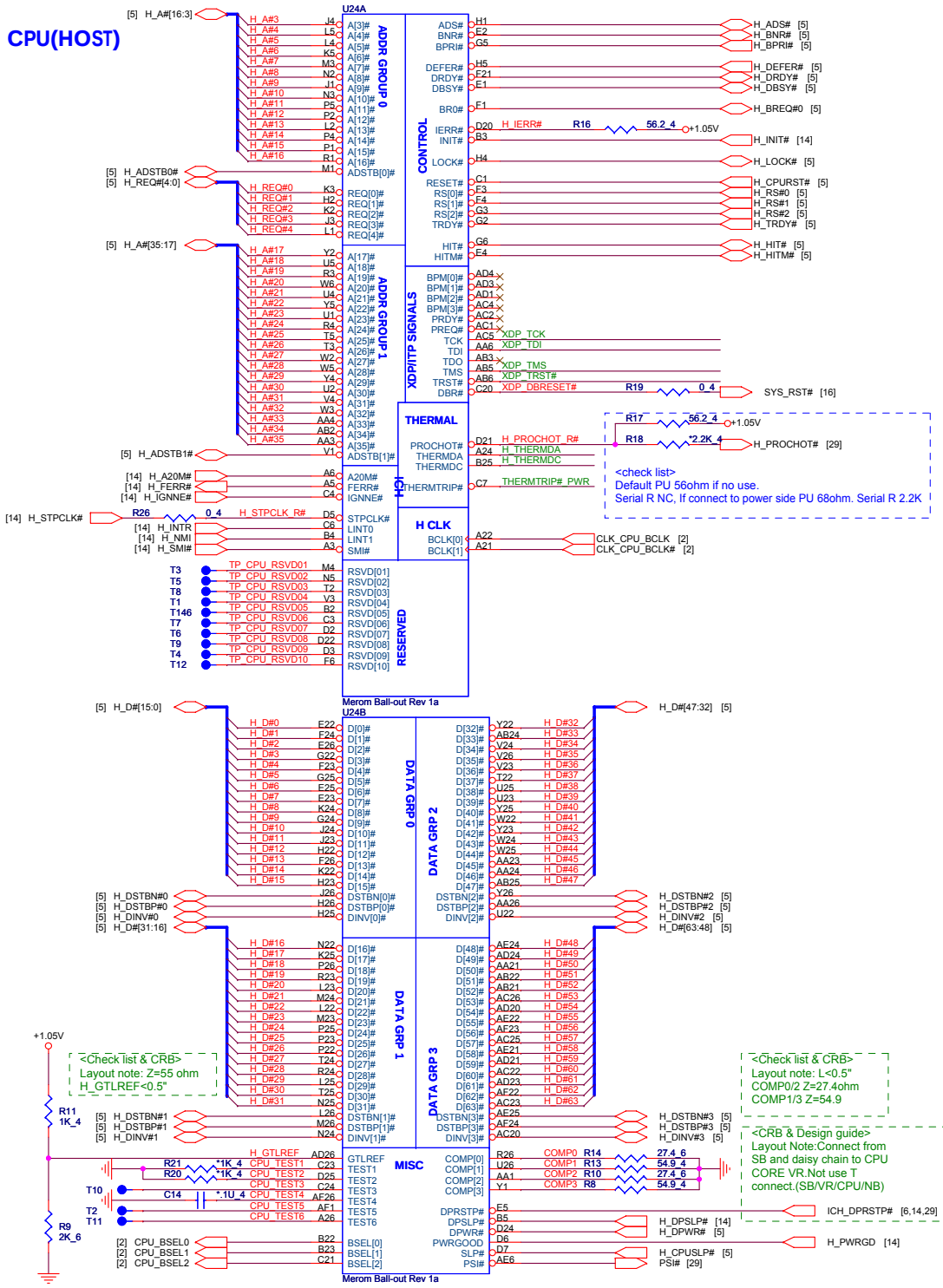
Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

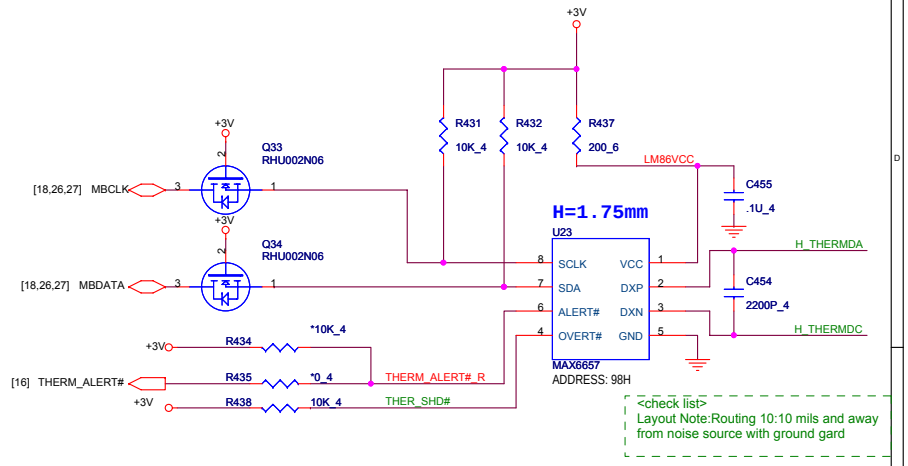
Size	Document Number	Rev
	CLK. GEN./ CK505	1A

Date: Monday, March 26, 2007 Sheet 2 of 33

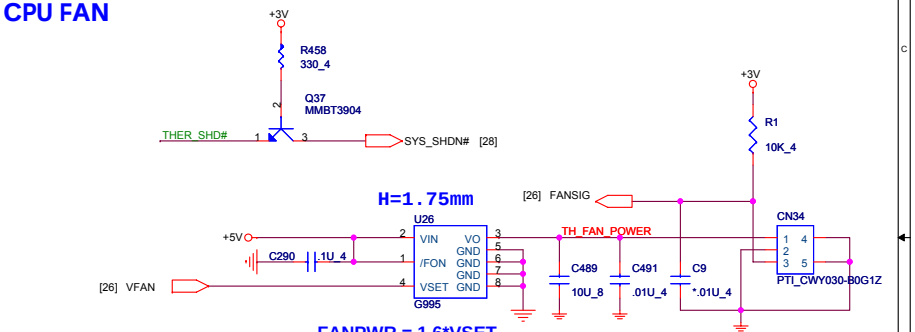
CPU(HOST)



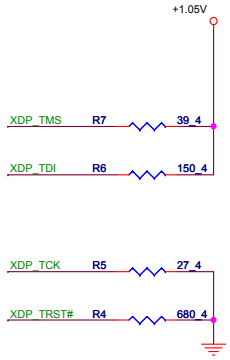
CPU Thermal monitor



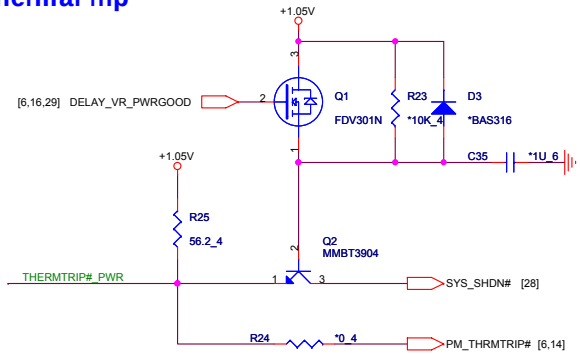
CPU FAN



PU/PD (ITP700)



Thermal Trip



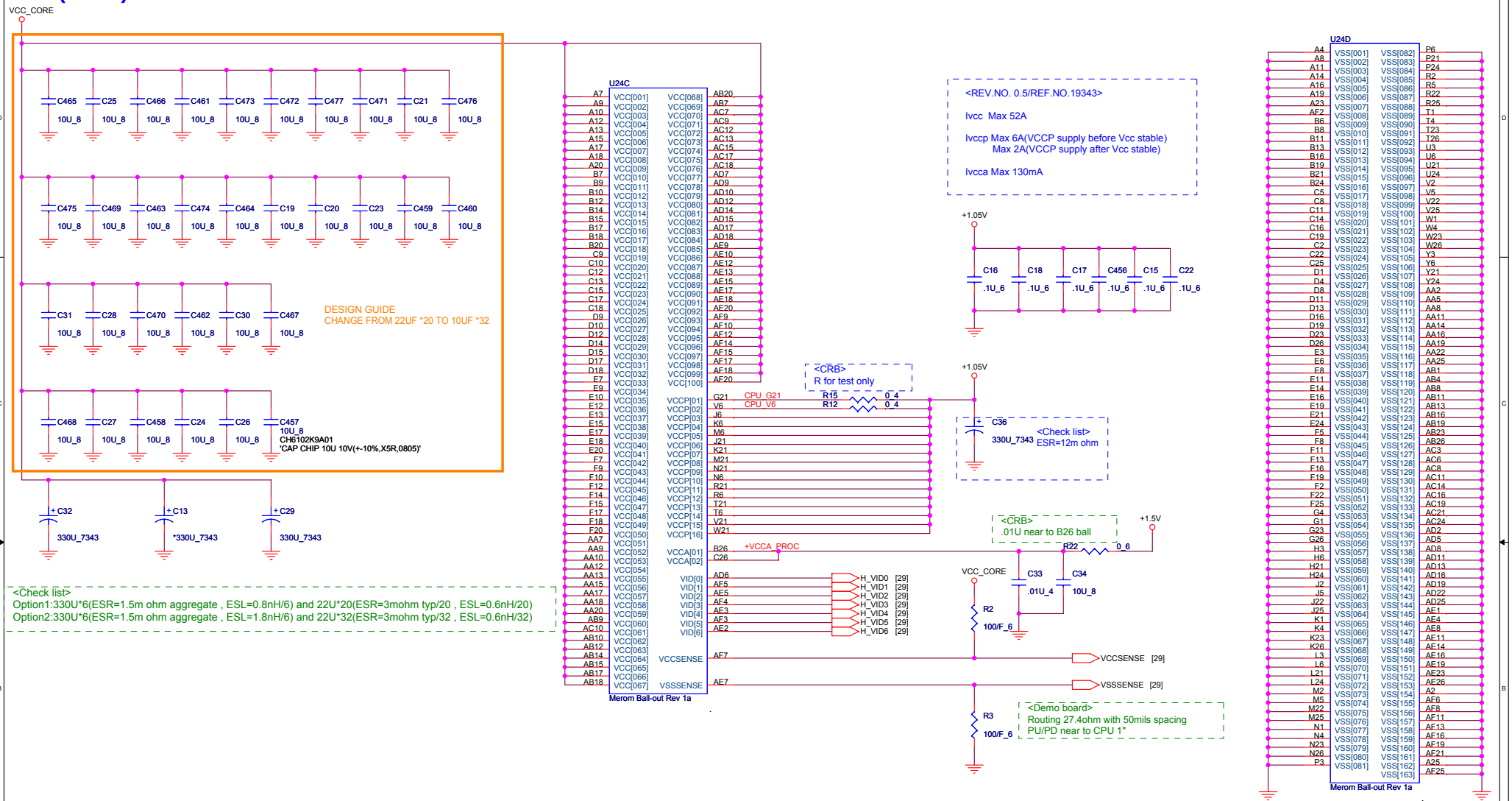
Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	CPU(1 of 2)/FAN/Thermal	3A

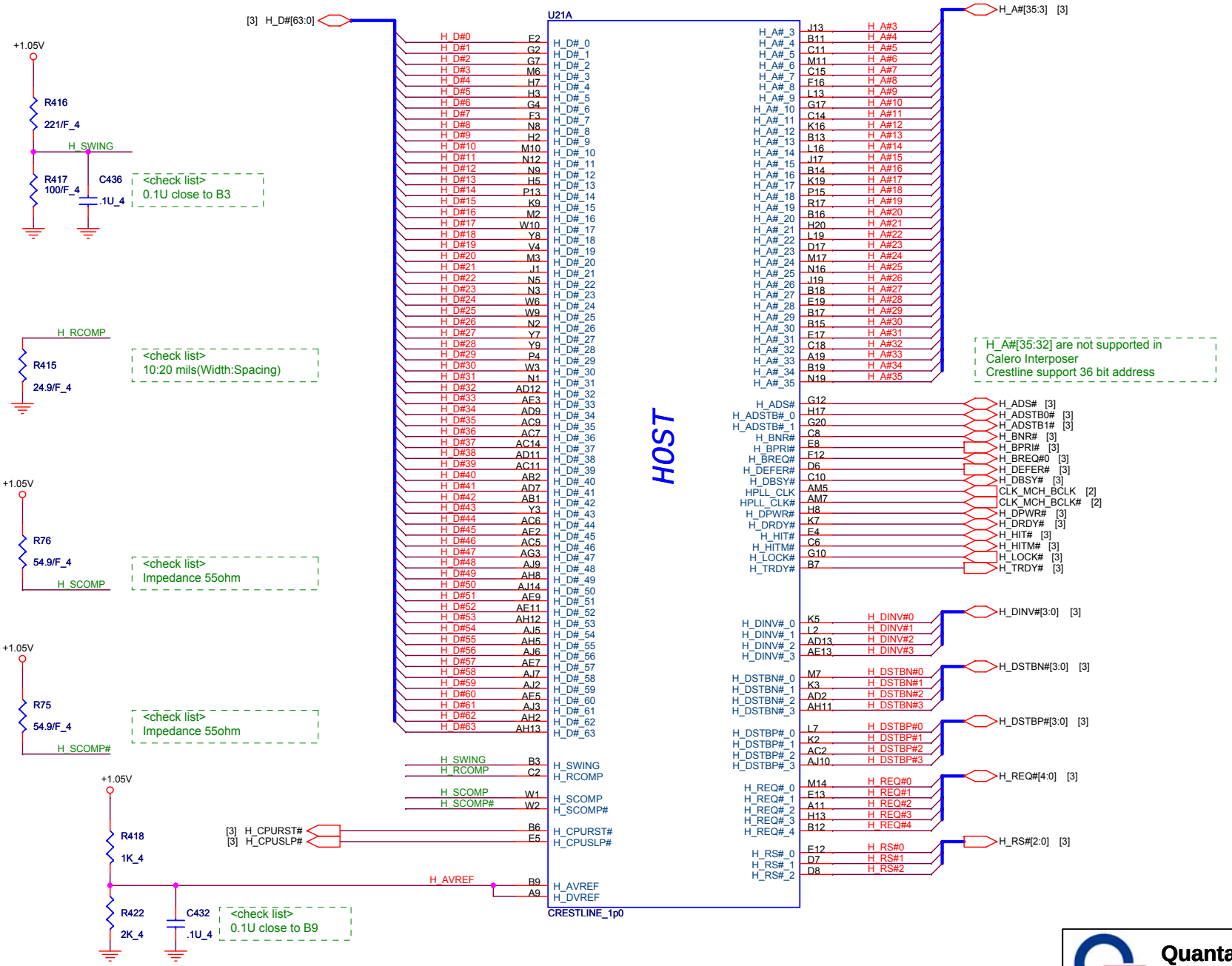
Date: Monday, March 26, 2007 Sheet 3 of 33

CPU(Power)

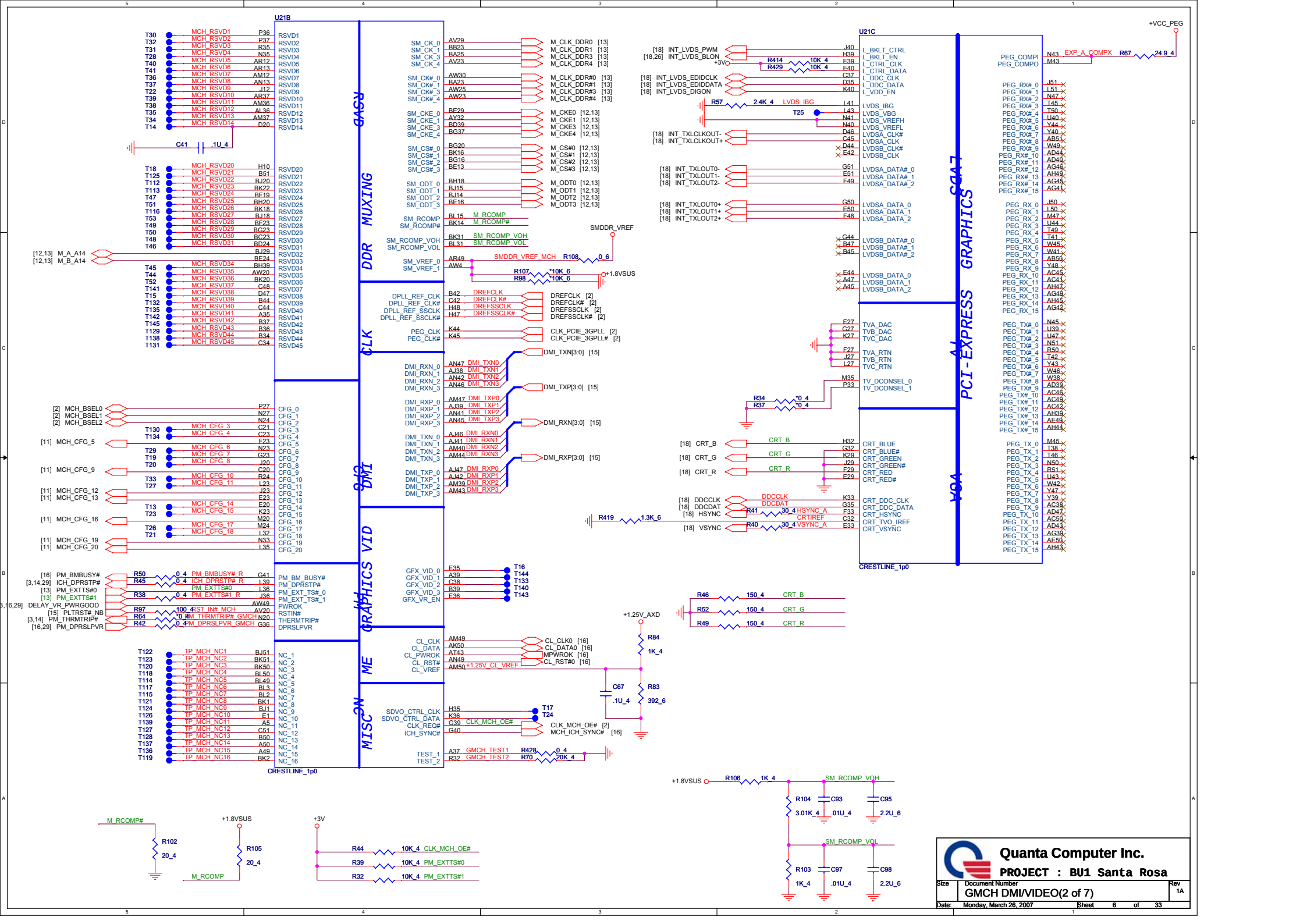


Quanta Computer Inc.			
PROJECT : BU1 Santa Rosa			
Size	Document Number		Rev
	CPU(2 of 2)		1A
Date: Monday, March 26, 2007	Sheet 4 of 33		

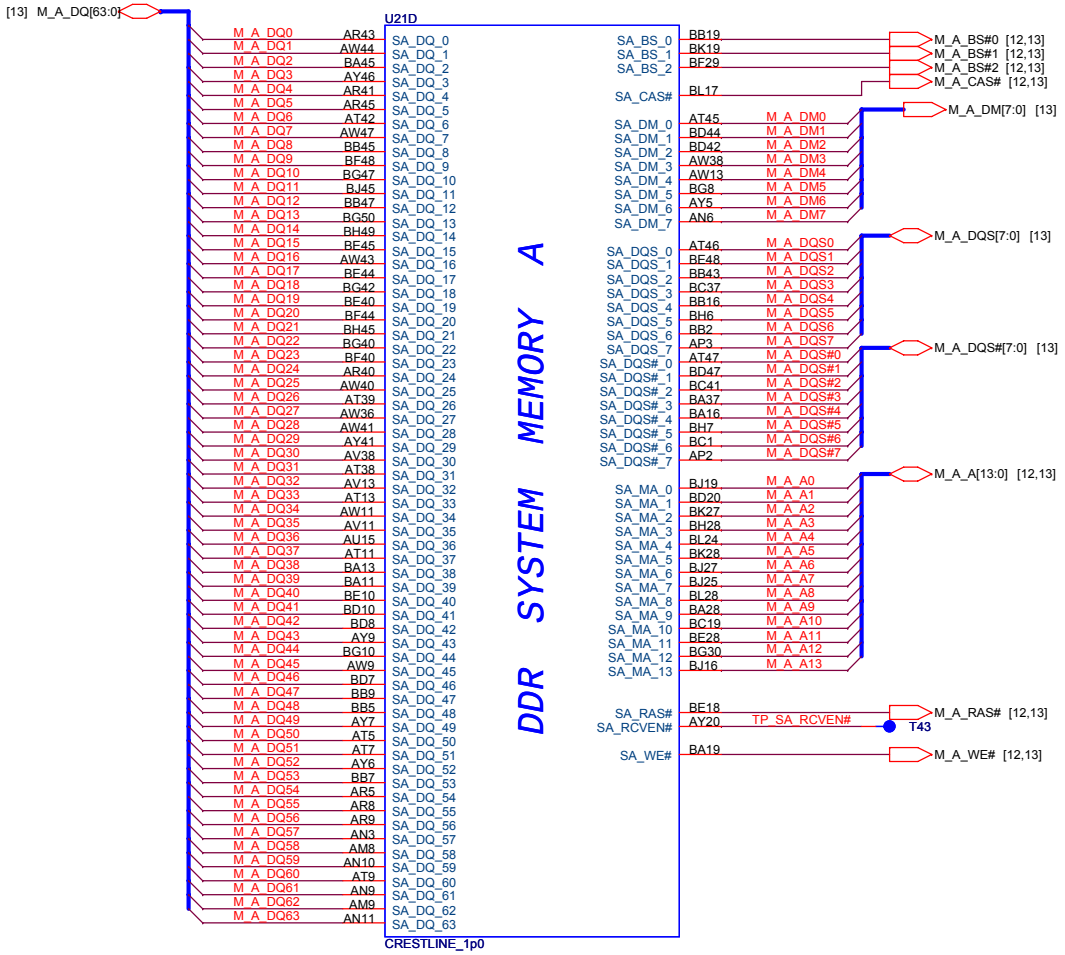
NB(HOST)

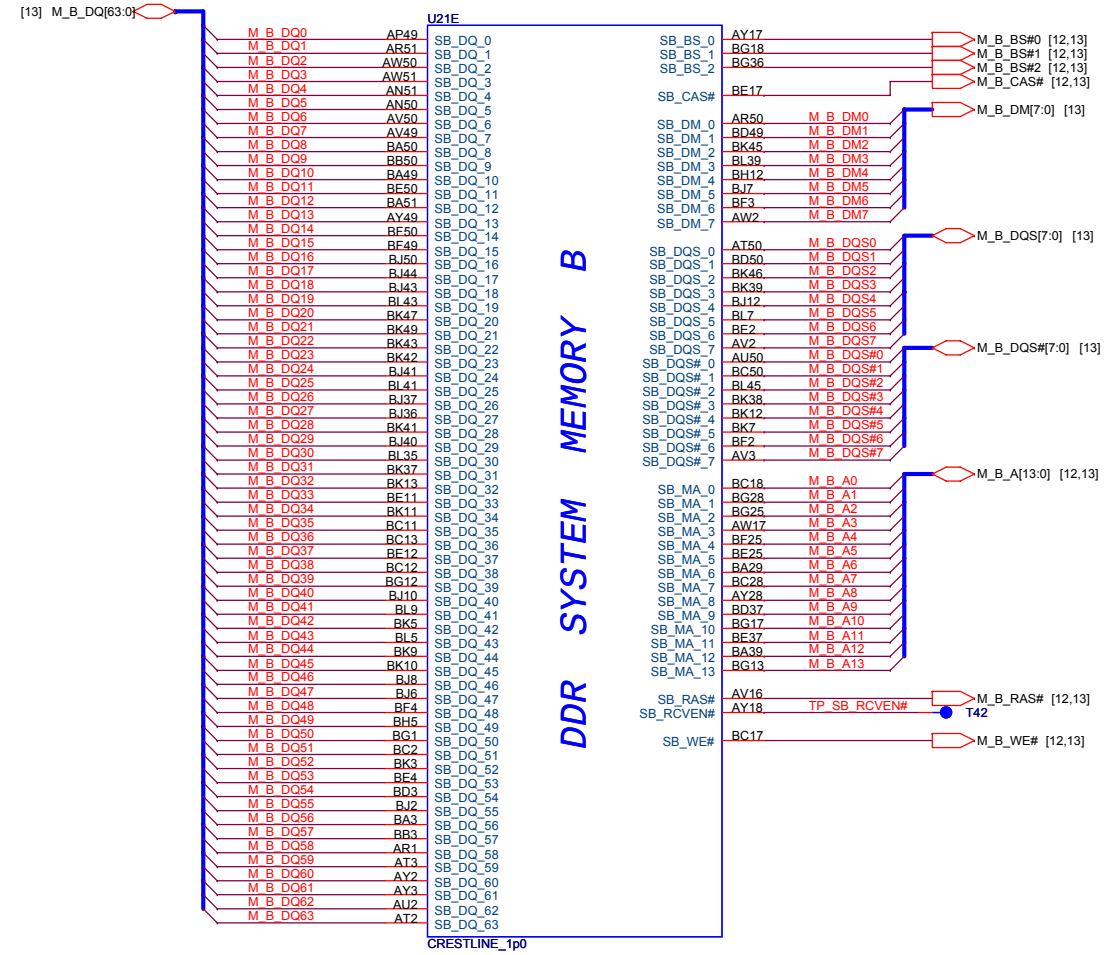


Quanta Computer Inc.		
PROJECT : BU1 Santa Rosa		
Size	Document Number: GMCH HOST(1 of 7)	Rev: 1A
Date: Monday, March 26, 2007	Sheet 5 of 33	


U21B
U21C
CRESTLINE_1p0
CRESTLINE_1p0
DMI
DDR MUXING
CLK
GRAPHICS VID
MISC
PCI-EXPRESS GRAPHICS
PCI-EXPRESS A
VGA
+VCC_PEG
+1.25V_AXD
+1.8VSUS
+3V
SMDDR_VREF
M_RCOMP#
M_RCOMP
Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
Size
Document Number
GMCH DMI/VIDEO(2 of 7)
Rev
1A
Date: Monday, March 26, 2007
Sheet 6 of 33

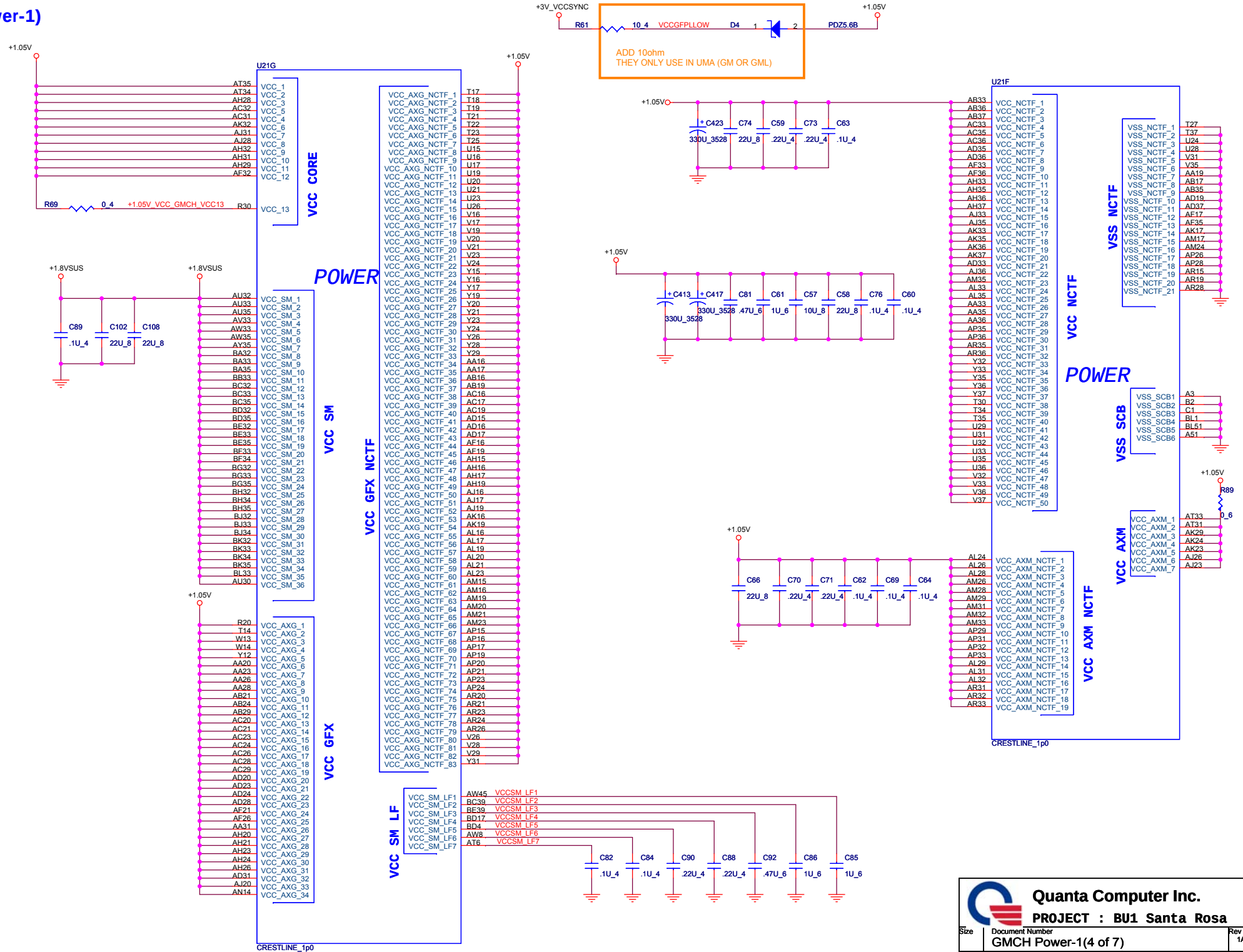
NB(Memory controller)





Quanta Computer Inc.		
PROJECT : BU1 Santa Rosa		
Size	Document Number: MCH DDR(3 of 7)	Rev: 1A
Date: Monday, March 26, 2007	Sheet 7 of 33	

NB(Power-1)



Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	GMCH Power-1(4 of 7)	1A
Date: Thursday, February 01, 2007	Sheet 8 of 33	

NB(Power-2)

CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL / INTERNAL

'IND CHIP 10UH(20%,100MA,LB2012T100MR)'

'EMI FILTER BKP1608HS181-T(180,1.5A)'

<FAE>
INT VGA disable
VCCSYNC connect to GND

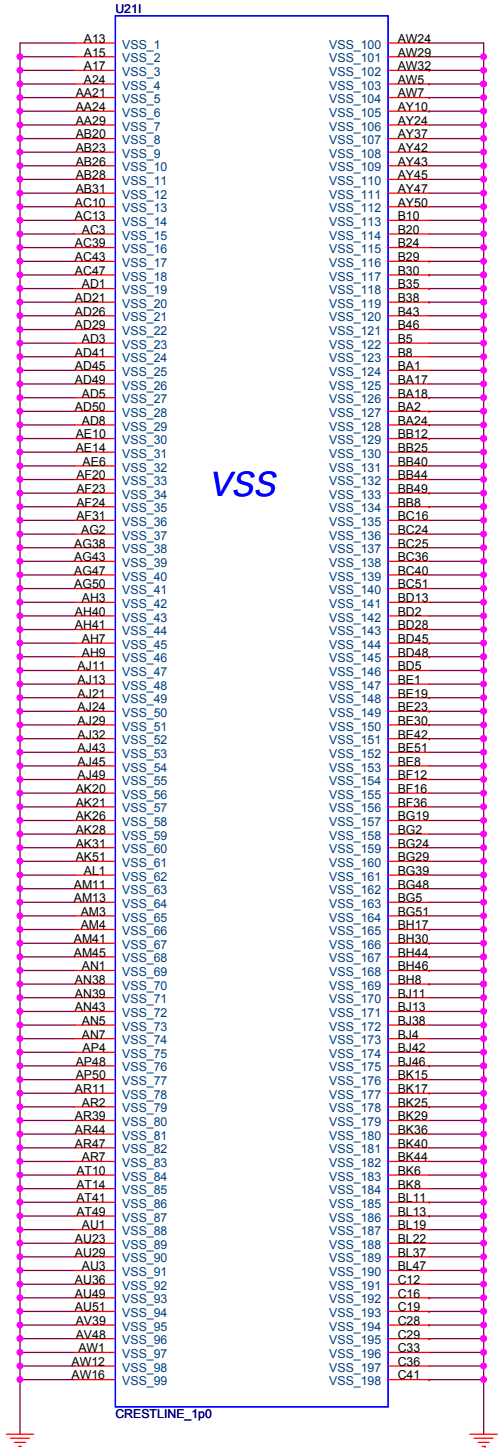
<FAE>
VCC_RXR_DMI and VCC_PEG
connect to+1.05V

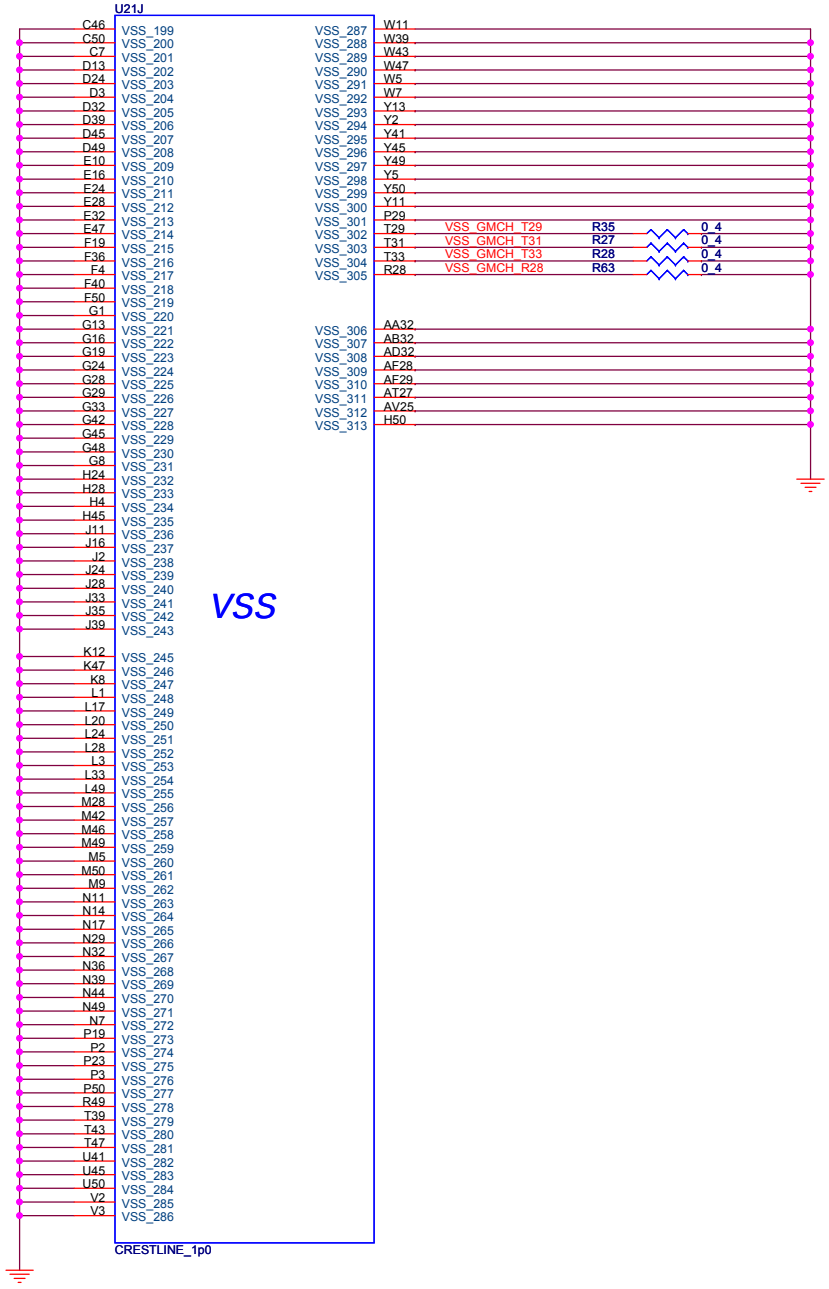
<CRB>
+1.25V AND +1.25M shall be
+1.5V for Calero Interposer

CRESTLINE_1p0

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
Size | Document Number: GMCH Power-2(5 of 7) | Rev 1A
Date: Tuesday, February 06, 2007 | Sheet 9 of 33

NB(Power-3)





Quanta Computer Inc.		
PROJECT : BU1 Santa Rosa		
Size	Document Number: GMCH Power-3(6 of 7)	Rev: 1A
Date: Thursday, February 01, 2007	Sheet 10 of 33	

Strap table

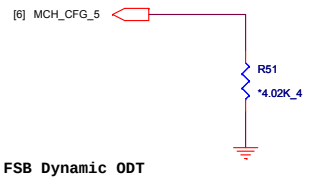
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

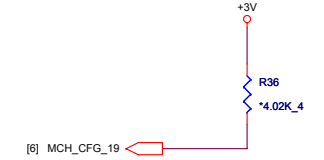
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

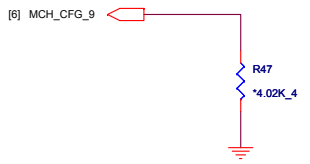


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

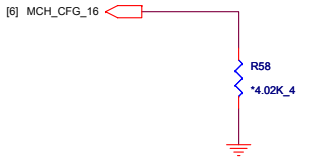


SDVO Present

Strap define at External DVI control page

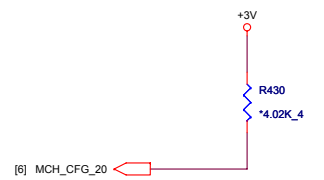
FSB Dynamic ODT

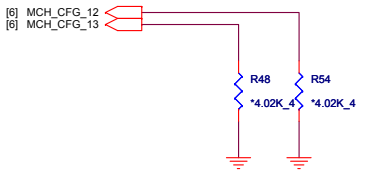
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	GMCH Strap(7 of 7)	1A

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DDR2 Dual channel A/B PU

M_A_A[13..0] → M_A_A[13..0] [7,13]

M_B_A[13..0] → M_B_A[13..0] [7,13]

DDRII A CHANNEL

SMDDR_VTERM

C176 .1U_4, C145 .1U_4, C143 .1U_4, C148 .1U_4, C195 .1U_4, C146 .1U_4, C230 .1U_4, C201 .1U_4, C228 .1U_4, C227 .1U_4, C142 .1U_4, C173 .1U_4, C200 .1U_4

DDRII B CHANNEL

SMDDR_VTERM

C174 .1U_4, C172 .1U_4, C177 .1U_4, C175 .1U_4, C231 .1U_4, C196 .1U_4, C197 .1U_4, C199 .1U_4, C171 .1U_4, C144 .1U_4, C226 .1U_4, C147 .1U_4, C225 .1U_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

M_A_A3 / M_A_A1	RP16	56X2	SMDDR_VTERM
M_A_A9 / M_A_A5	RP18	56X2	SMDDR_VTERM
M_A_A2 / M_A_A4	RP21	56X2	SMDDR_VTERM
M_A_A11 / [6,13] M_CKE1	RP23	56X2	SMDDR_VTERM
[6,13] M_CKE0 / M_A_A8	RP19	56X2	SMDDR_VTERM
M_A_A12 / [7,13] M_A_BS#2	RP20	56X2	SMDDR_VTERM
[7,13] M_A_BS#1 / M_A_A0	RP25	56X2	SMDDR_VTERM

M_B_A10 / [7,13] M_B_WE#	RP30	56X2	SMDDR_VTERM
M_B_A3 / M_B_A1	RP31	56X2	SMDDR_VTERM
[7,13] M_B_BS#1 / M_B_A0	RP38	56X2	SMDDR_VTERM
M_B_A7 / M_B_A11	RP35	56X2	SMDDR_VTERM
M_B_A8 / M_B_A5	RP27	56X2	SMDDR_VTERM
M_B_A2 / M_B_A4	RP34	56X2	SMDDR_VTERM
M_B_A9 / M_B_A12	RP28	56X2	SMDDR_VTERM

M_A_A7 / M_A_A6	RP22	56X2	SMDDR_VTERM
[6,13] M_CKE3 / [7,13] M_B_BS#2	RP32	56X2	SMDDR_VTERM
[6,13] M_ODT1 / [6,13] M_CS#1	RP14	56X2	SMDDR_VTERM
[6,13] M_ODT3 / [7,13] M_B_BS#0	RP33	56X2	SMDDR_VTERM
M_A_A10 / [7,13] M_A_BS#0	RP17	56X2	SMDDR_VTERM
[7,13] M_A_CAS# / [7,13] M_A_WE#	RP15	56X2	SMDDR_VTERM
[6,13] M_CS#0 / [7,13] M_A_RAS#	RP26	56X2	SMDDR_VTERM
[7,13] M_B_CAS# / [6,13] M_CS#3	RP29	56X2	SMDDR_VTERM
M_B_A6 / [6,13] M_CKE4	RP39	56X2	SMDDR_VTERM
[6,13] M_ODT2 / [7,13] M_B_RAS#	RP37	56X2	SMDDR_VTERM
[6,13] M_ODT0 / M_A_A13	RP24	56X2	SMDDR_VTERM
M_B_A13 / [6,13] M_CS#2	RP36	56X2	SMDDR_VTERM

INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

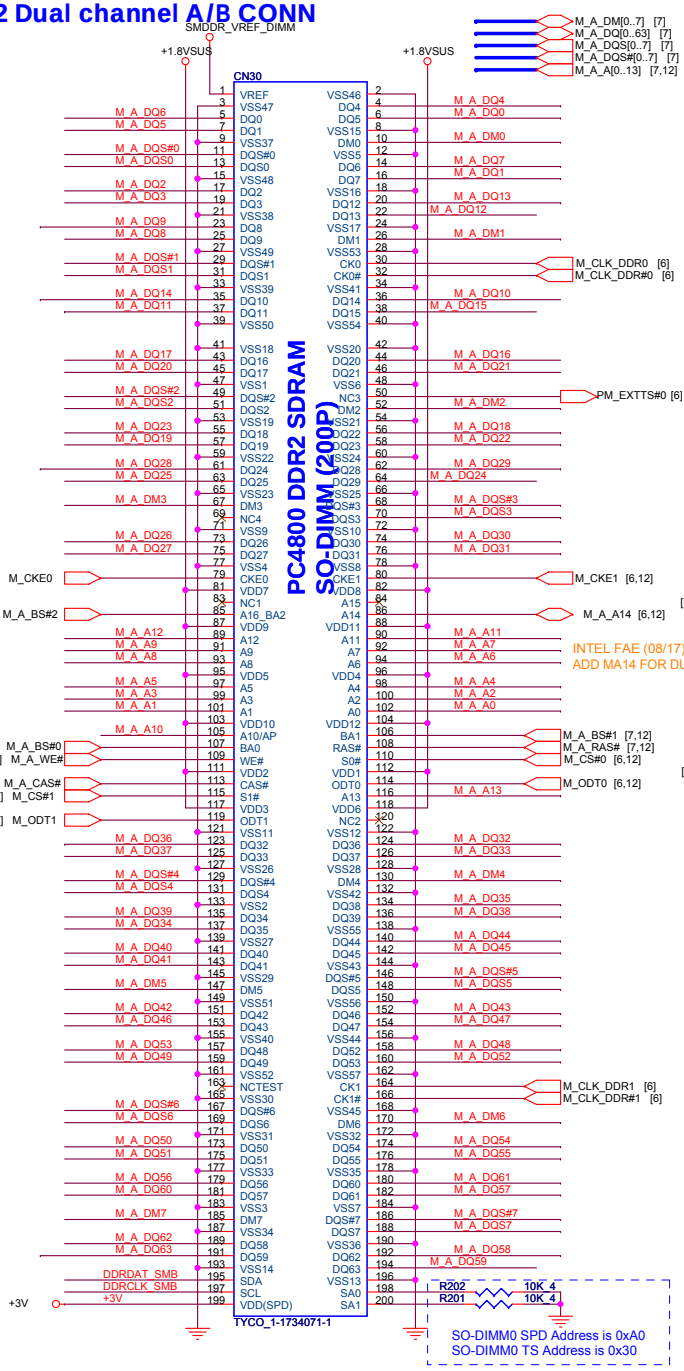
[6,13] M_A_A14 / [6,13] M_B_A14 → R199 56_4 / R219 56_4 → SMDDR_VTERM

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	DDR RES. ARRAY	1A

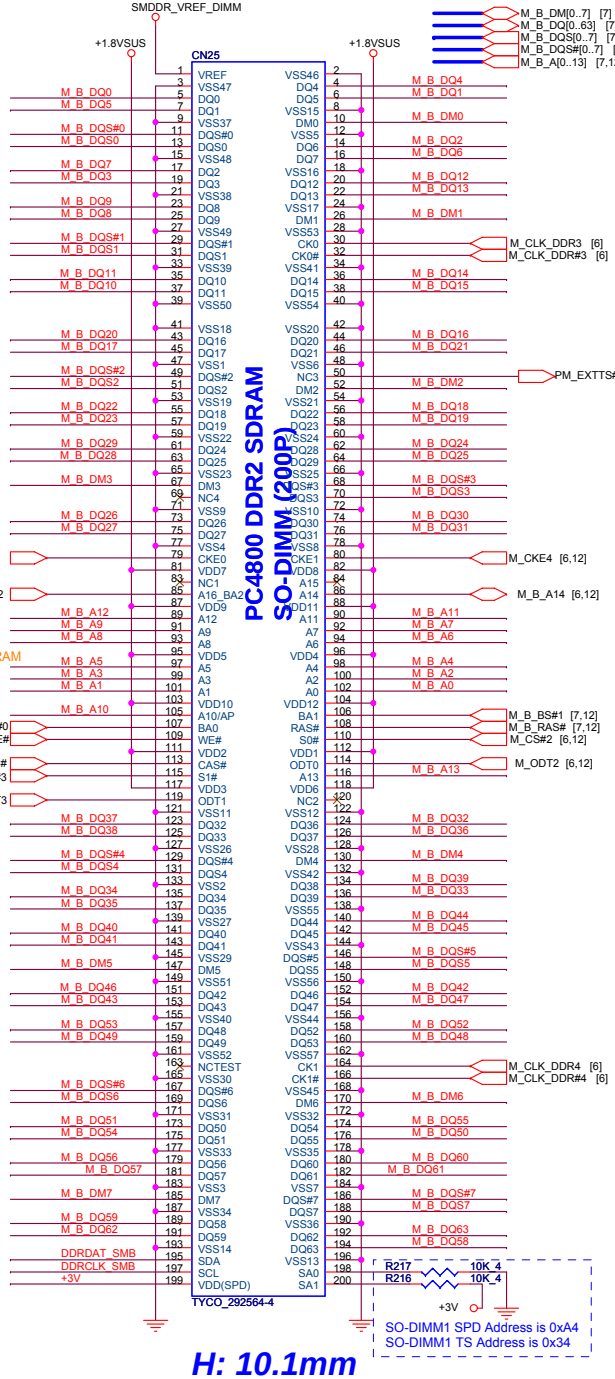
Date: Monday, March 26, 2007 Sheet 12 of 33

DDR2 Dual channel A/B CONN



H: 5.6mm

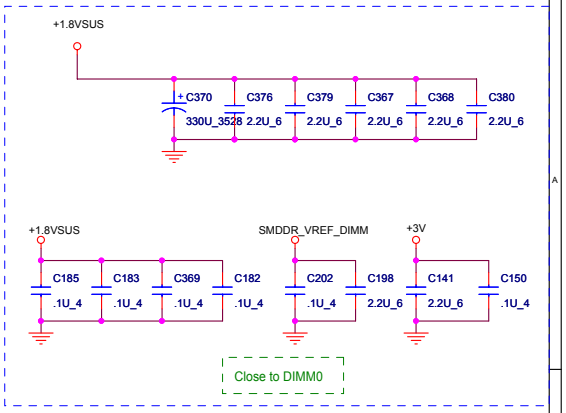
CLOCK 0,1
CKE 0,1

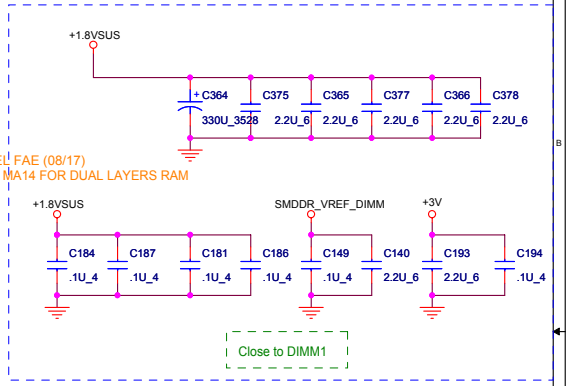


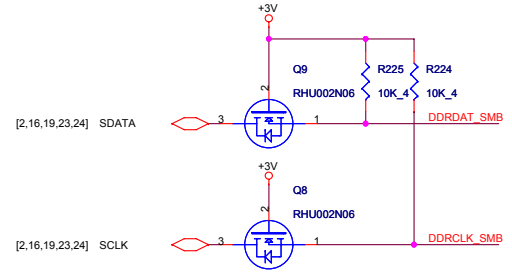
H: 10.1mm

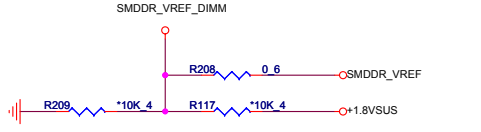
CLOCK 3,4
CKE 2,3

INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

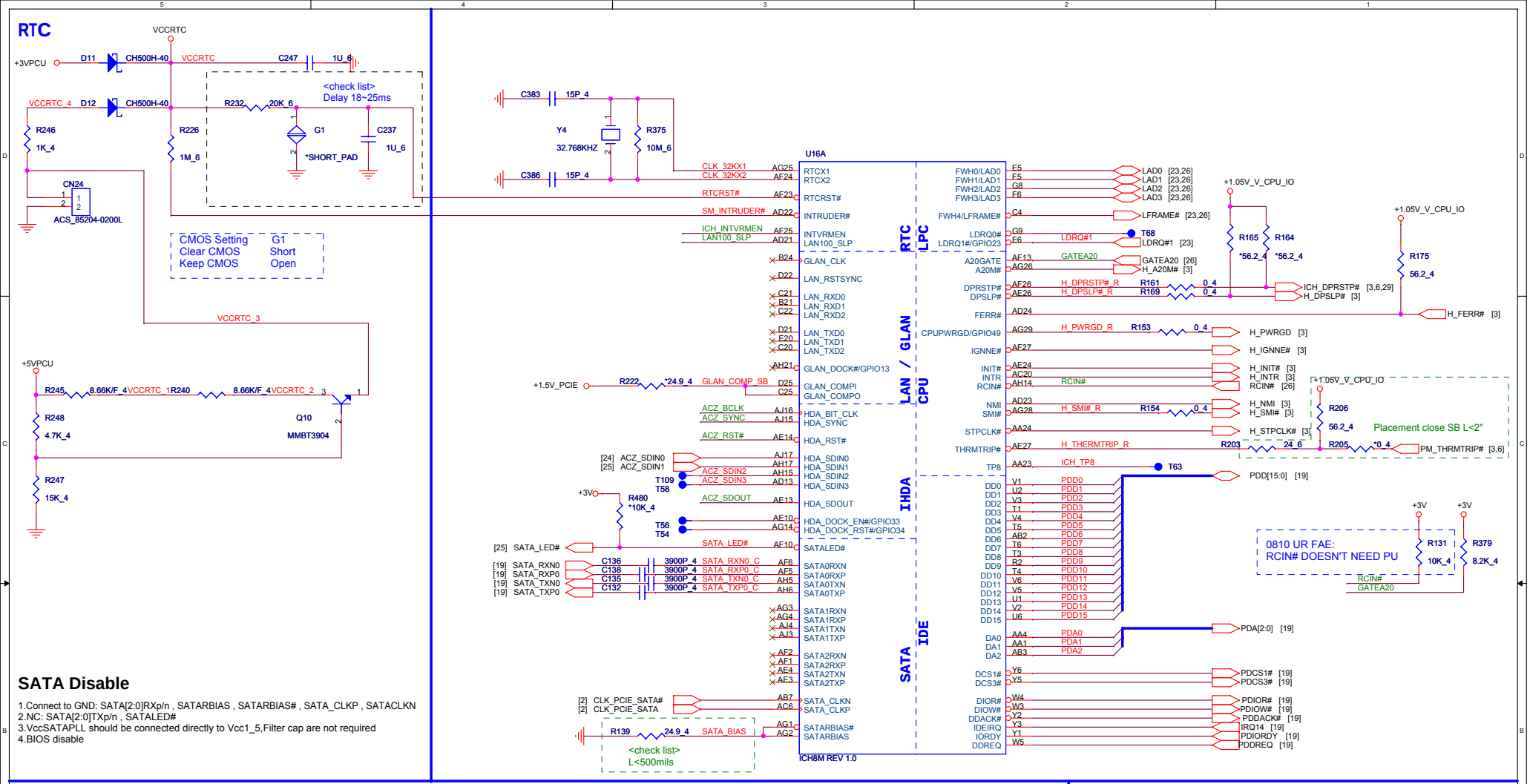








Quanta Computer Inc.		
PROJECT : BU1 Santa Rosa		
Size	Document Number: DDR SO-DIMM(200P)	Rev: 3A
Date: Monday, March 26, 2007	Sheet 13 of 33	



SATA Disable

1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
2.NC: SATA[2:0]TXp/n , SATALED#
3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
4.BIOS disable

SB Strap

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

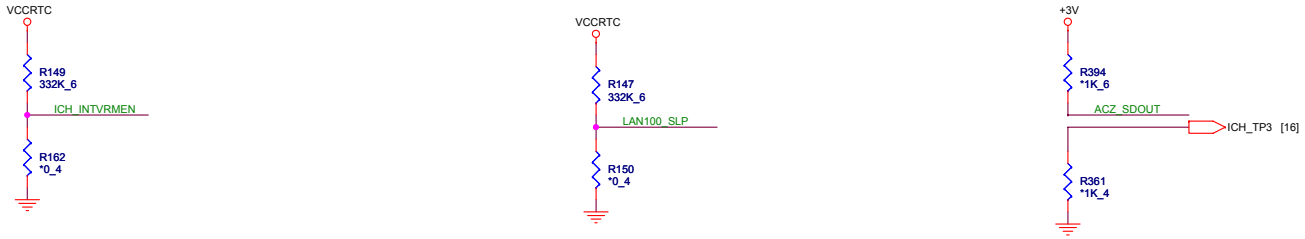
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

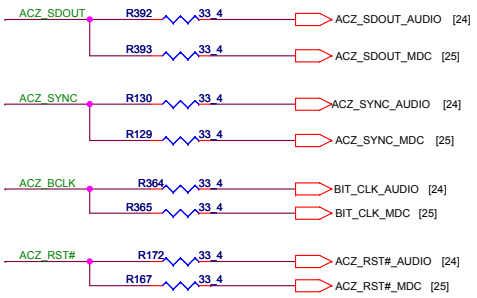
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



HDA



Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	ICH8M HOST(1 of 4)	2A

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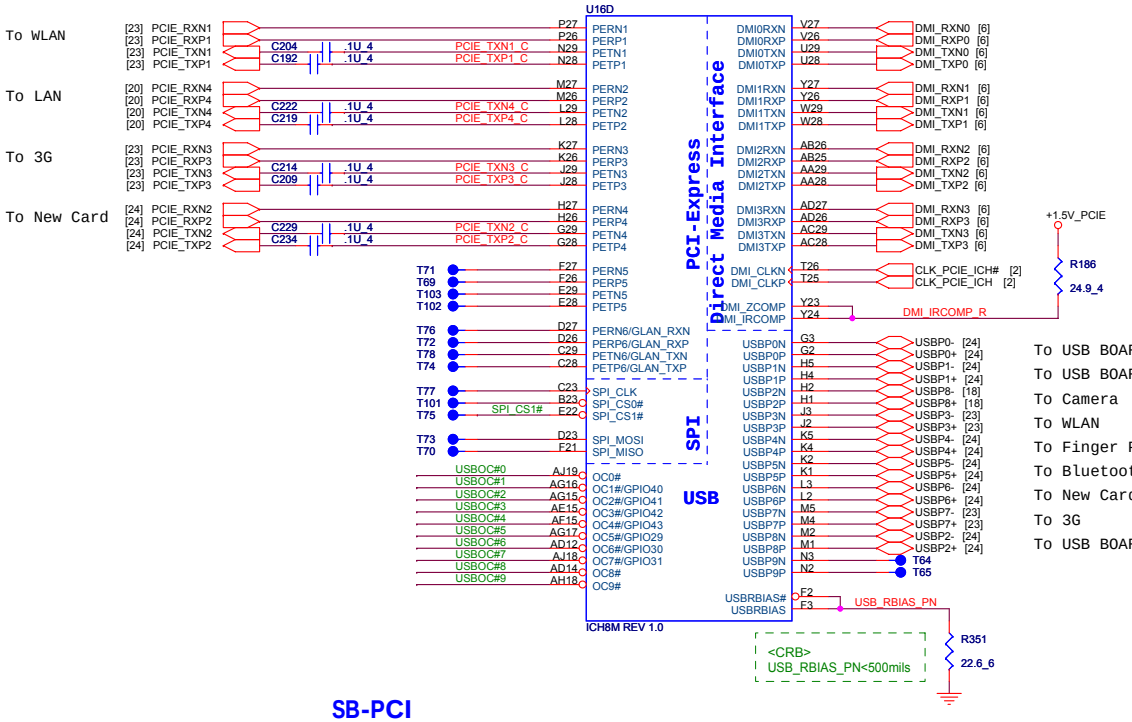
SB-PCIE/USB/DMI



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

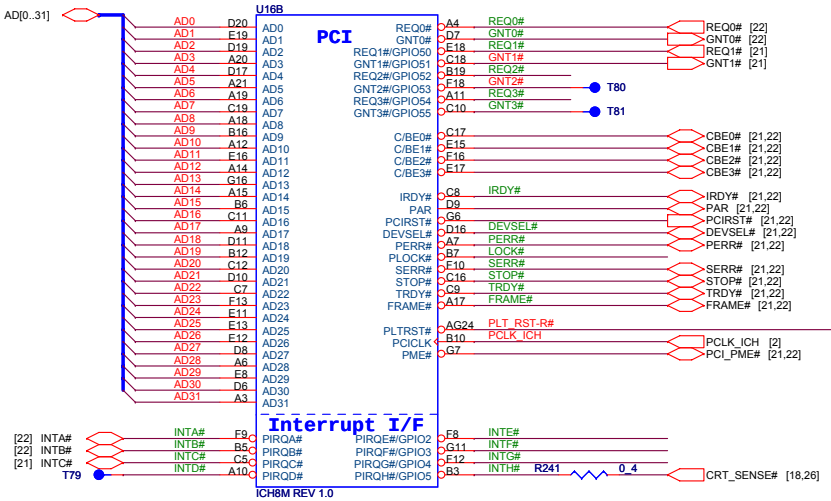
GNT3# R227 *1K_4

ICH8 Boot BIOS select

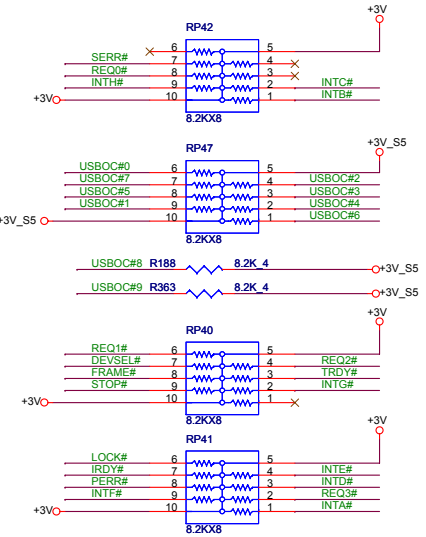
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R220 *1K_4
GNT0# R223 *1K_4

SB-PCI



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#,INTB#	R5C833
REQ1# / GNT1#	AD20	INTC#	CB1410



Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	ICH8M PCIE(2 of 4)/ BIOS	1A

Date: Monday, March 26, 2007 Sheet 15 of 33

SB-GPIO

U16C

ICH8M REV 1.0

SMB | SATA GPIO | CLOCKS | SYS GPIO | Power MGT | GPIO | Controller Link | MISC

SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1, RI#, SUS_STAT#/LPCPD#, SYS_RESET#, BMBUSY#/GPIO0, SMBALERT#/GPIO11, STP_PCI#/GPIO15, STP_CPU#/GPIO25, CLKRUN#/GPIO32, WAKE#, SERIRQ, THRM#, VRMPWRGD, TP7, TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, GPIO12, TACH0/GPIO17, GPIO18, GPIO20, SCLOCK/GPIO22, QRT_STATE0/GPIO27, QRT_STATE1/GPIO28, SATACLKREQ#/GPIO35, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SPKR, MCH_SYNC#, TP3

SATA0GP/GPIO21, SATA1GP/GPIO19, SATA2GP/GPIO36, SATA3GP/GPIO37, CLK14, CLK48, SUSCLK, SLP_S3#, SLP_S4#, SLP_S5#, S4_STATE#/GPIO26, PWROK, DPRSLPVR/GPIO16, BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, CK_PWRGD, CLPWROK, SLP_M#, CL_CLK0, CL_CLK1, CL_DATA0, CL_DATA1, CL_VREF0, CL_VREF1, CL_RST#, MEM_LED/GPIO24, ME_EC_ALERT/GPIO10, EC_ME_ALERT/GPIO14, WOL_EN/GPIO9

SMB

[2,13,19,23,24] SCLK → AJ26 SMBCLK
[2,13,19,23,24] SDATA → AD19 SMBDATA
[23] CL_RST#1 → AG21 LINKALERT#
T60 → AC17 SMLINK0
T59 → AE19 SMLINK1
RI# → AF17 RI#

SYS GPIO

[22] LPC_PD# → F4
[3] SYS_RST# → AD15 SYS_RST#
[6] PM_BMBUSY# → AG12 BMBUSY#/GPIO0
SMB_ALERT# → AG22 SMBALERT#/GPIO11
[2] PM_STPPCI# → R125 0_4 → PM_STPPCI_ICH# → AE20 STP_PCI#/GPIO15
[2] PM_STPCPU# → R126 0_4 → PM_STPCPU_ICH# → AG18 STP_CPU#/GPIO25
[22,26] CLKRUN# → AH11 CLKRUN#/GPIO32
[20,23,24] PCIE_WAKE# → AE17 WAKE#
[21,22,23,26] SERIRQ → AF12 SERIRQ
[3] THERM_ALERT# → AC13 THRM#
VR_PWRGD_CLKEN → AJ20 VRMPWRGD
T106 → ICH_TP7 → AJ22 TP7

R127 *10K_4 (+3V)
R124 *10K_4

<FAE>
CRB STP_PCI# PU is no stuff.
CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
(CLK_MCH_BCLK/# must keep alive to make ME work)
I think there will be update for this design, I suggest you to keep PU and 0Ω isolation resistors for this signal.

Power MGT

[26] KBSMI# → D25 BAS316 KBSMI#_ICH → AJ8
T107 → AJ9
T108 → AH9
[26] SCI# → SCI# AE16
GPIO12 AC19
BOARD_ID0 AG8
BOARD_ID1 AH12
BOARD_ID3 AE11
ICH_GPIO22 AG10
T111 → ICH_GPIO27 AH25
T149 → ICH_GPIO28 AD16
GPIO35 AG13
[19] RST_HDD# → RST_HDD# AF9
ICH_GPIO39 AJ11
ICH_GPIO48 AD10
[24] SPKR → SPKR AD9
[6] MCH_ICH_SYNC# → R369 0_4 → MCH_ICH_SYNC#_R → AJ13 MCH_SYNC#
[14] ICH_TP3 → AJ21 TP3

SATA0GP/GPIO21 AJ12 BOARD_ID4
SATA1GP/GPIO19 AJ10 BOARD_ID2
SATA2GP/GPIO36 AF11 GPIO36
SATA3GP/GPIO37 AG11 GPIO37

CLOCKS

CLK14 AG9 14M_ICH → 14M_ICH [2]
CLK48 G5 CLKUSB_48 → CLKUSB_48 [2]
SUSCLK D3 → T94

CLKUSB_48 → R211 *10_4 → C208 *10P_4
14M_ICH → R160 *33_4 → C128 *10P_4

Power MGT

SLP_S3# AG23 → R168 100_4 → SUSB# [26]
SLP_S4# AF21 → R385 100_4 → SUSC# [26]
SLP_S5# AD18 → T61
S4_STATE#/GPIO26 AH27 → T104
PWROK AE23 ICH_PWROK
DPRSLPVR/GPIO16 AJ14 PM_DPRSLPVR_R → R367 100_4 → PM_DPRSLPVR [6,29]

<FAE>
Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSLPVR to IMVP6 is correct

BATLOW# AE21 PM_BATLOW#_R
PWRBTN# C2 DNBSWON# → DNBSWON# [26]
LAN_RST# AH20 PM_LAN_ENABLE_R → R123 *0_4 → PLTRST# [15,19,20,23,24,26]
RSMRST# AG27 RSMRST#_R

If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

GPIO

CK_PWRGD E1 → CK_PWRGD [2], ECPWROK [26], MPWROK [6]
CLPWROK E3 ECPWROK → R221 0_4
SLP_M# AJ25 → T105

Controller Link

CL_CLK0 F23 → CL_CLK0 [6]
CL_CLK1 AE18 → CL_CLK1 [23]
CL_DATA0 F22 → CL_DATA0 [6]
CL_DATA1 AF19 → CL_DATA1 [23]
CL_VREF0 D24 CL_VREF0_SB
CL_VREF1 AH23 CL_VREF1_SB
CL_RST# AJ23 → CL_RST#0 [6]

+3V_S5: R378 3.24K_6 (CL_VREF0_SB), C134 .1U_4, R377 453_4
+3V: R229 3.24K_6 (CL_VREF1_SB), C235 .1U_4, R230 453_4

Controller Link 1 VREF for IAMT support only

MISC

MEM_LED/GPIO24 AJ27 ICH_GPIO24
ME_EC_ALERT/GPIO10 AJ24 HDPACT → HDPACT [19,26]
EC_ME_ALERT/GPIO14 AF22 ICH_GPIO14
WOL_EN/GPIO9 AG19 HDPINT → HDPINT [19,26]

+3VSUS

[3,6,29] DELAY_VR_PWRGOOD → DELAY_VR_PWRGOOD 1
ECPWROK 2
R233 100K_4 TC7SH08FU
U5 4 ICH_PWROK
C250 .1U_4

U17

[29] VR_PWRGD_CK410# → 2
C130 .1U_4
U17 NC7SZ04
3 → 4 VR_PWRGD_CLKEN
R362 100K_4

No Reboot strap

SPKR	Low = Default High = No Reboot

BIOS/ ERIC: UNSTUFF

SPKR	R178	*10K_4
GPIO35	R380	10K_4
THERM_ALERT#	R187	8.2K_4
SERIRQ	R157	10K_4
CLKRUN#	R371	8.2K_4
MCH_ICH_SYNC#_R	R381	*10K_4
CL_RST#1	R151	10K_4
KBSMI#_ICH	R390	10K_4
SCI#	R366	10K_4
ICH_GPIO22	R134	10K_4
ICH_GPIO48	R138	10K_4
RST_HDD#	R137	10K_4
GPIO36	R133	8.2K_4
GPIO37	R132	8.2K_4
PM_DPRSLPVR	R368	100K_4
ICH_PWROK	R170	10K_4
ICH_GPIO14	R166	10K_4
HDPINT	R468	*10K_4

+3V_S5

SMLINK0	R185	10K_4
SMLINK1	R184	10K_4
SYS_RST#	R179	10K_4
DNBSWON#	R239	*10K_4
ICH_GPIO24	R358	*10K_4 (Internal Pull up)
HDPACT	R140	*10K_4
RI#	R145	10K_4
SCLK	R359	2.2K_4
SDATA	R128	2.2K_4
SMB_ALERT#	R360	10K_4
PCIE_WAKE#	R146	1K_4
PM_BATLOW#_R	R158	8.2K_4
GPIO12	R183	10K_4

INTEL CRB NEED THOSE PU & PD.

+3V
PM_LAN_ENABLE_R R122 10K_4
INTEL CRB SHOW IT

ICH_GPIO39 R372 10K_4
INTEL CRB SHOW IT

PM_LAN_ENABLE_R R121 *0_4
DISABLE LAN: STUFF

INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"

Q5 MMBT3906
RSMRST#_R *TO ICH8*
RSMRST# [26] *FROM uR(EC)*
R155 10K_4
R200 4.7K_4 +3VSUS
D8 BAV99
D9 BAV99
R210 2.2K_4

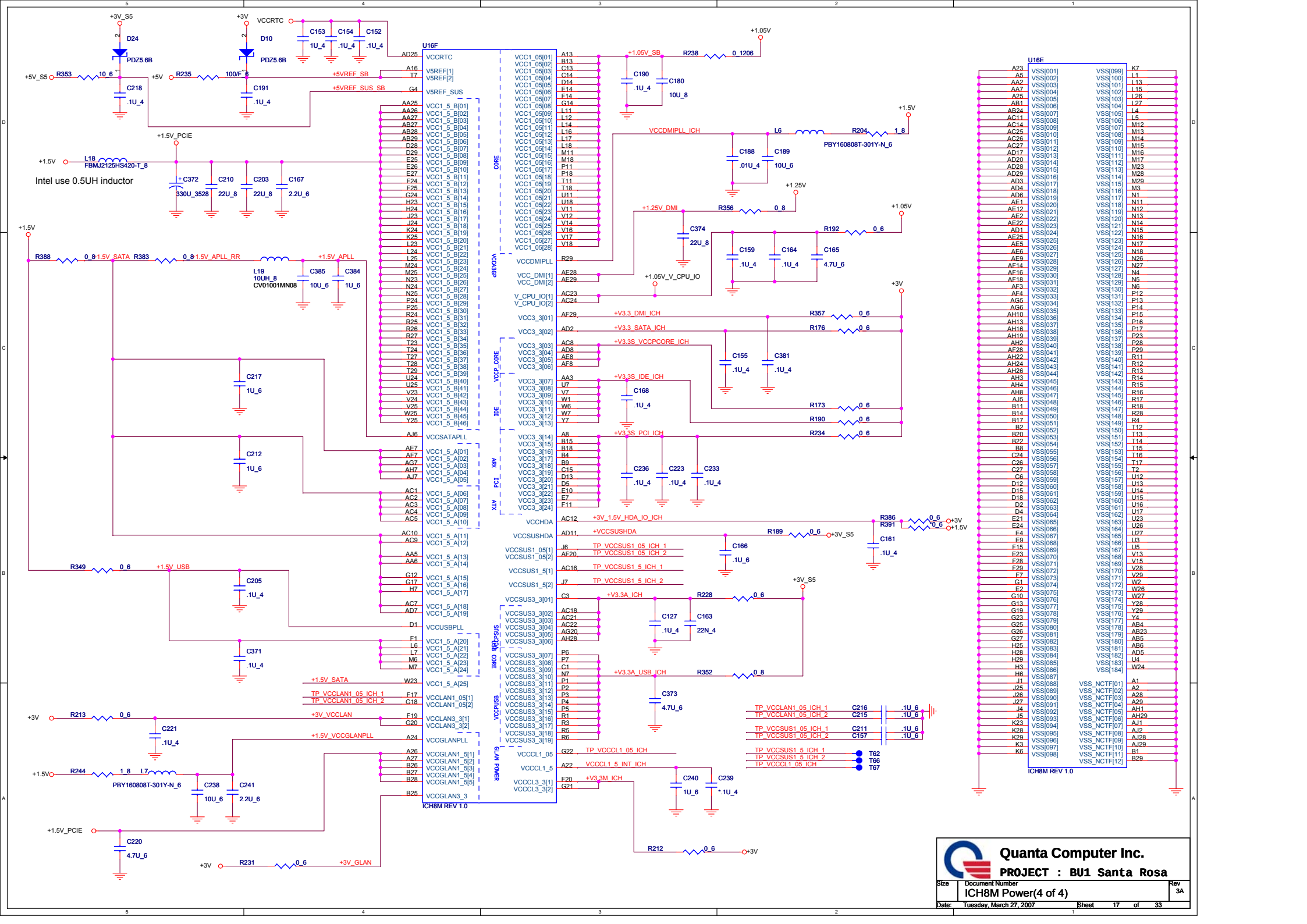
Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD	0	0	0	0	1
CARD BUS	0	0	0	1	0
G-SENSOR	0	0	1	0	0
CCD	0	1	0	0	0
ROBSON	1	0	0	0	0

+3V
R290 *10K_4 BOARD_ID4 R269 10K_4
R120 *10K_4 BOARD_ID3 R141 10K_4
R136 *10K_4 BOARD_ID2 R135 10K_4
R382 *10K_4 BOARD_ID1 R370 10K_4
R373 *10K_4 BOARD_ID0 R374 10K_4

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	ICH8M GPIO(3 of 4)	2A

Date: Monday, March 26, 2007 Sheet 16 of 33


U16F
ICH8M REV 1.0
U16E
ICH8M REV 1.0
Intel use 0.5UH inductor
L18 FBMJ2125HS420-T_8
L19 10UH_8 CV01001MN08
L6 PBY160808T-301Y-N_6
L7 PBY160808T-301Y-N_6
D24 PDZ5.6B
D10 PDZ5.6B
Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
Size
Document Number
ICH8M Power(4 of 4)
Rev 3A
Date: Tuesday, March 27, 2007
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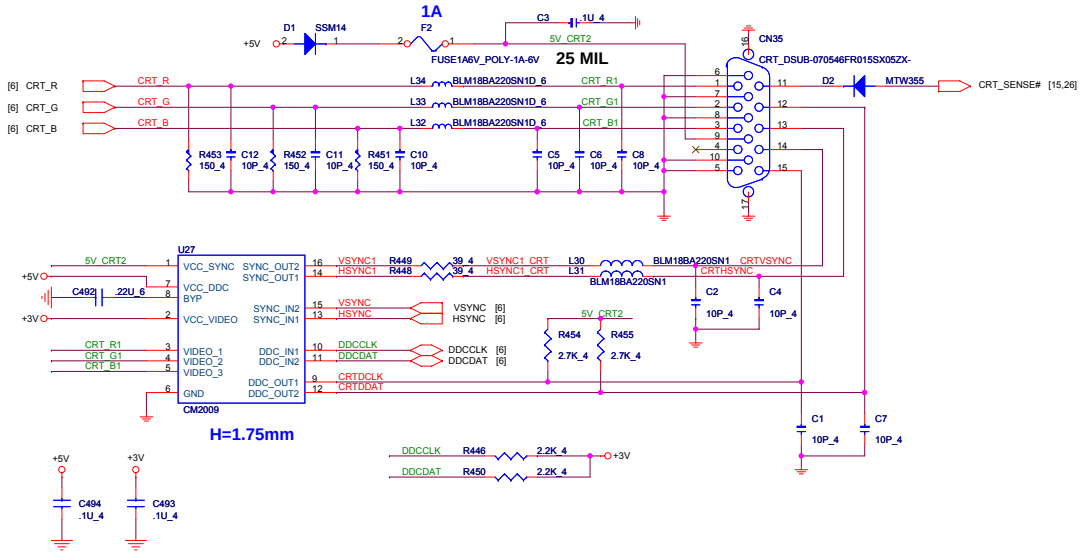
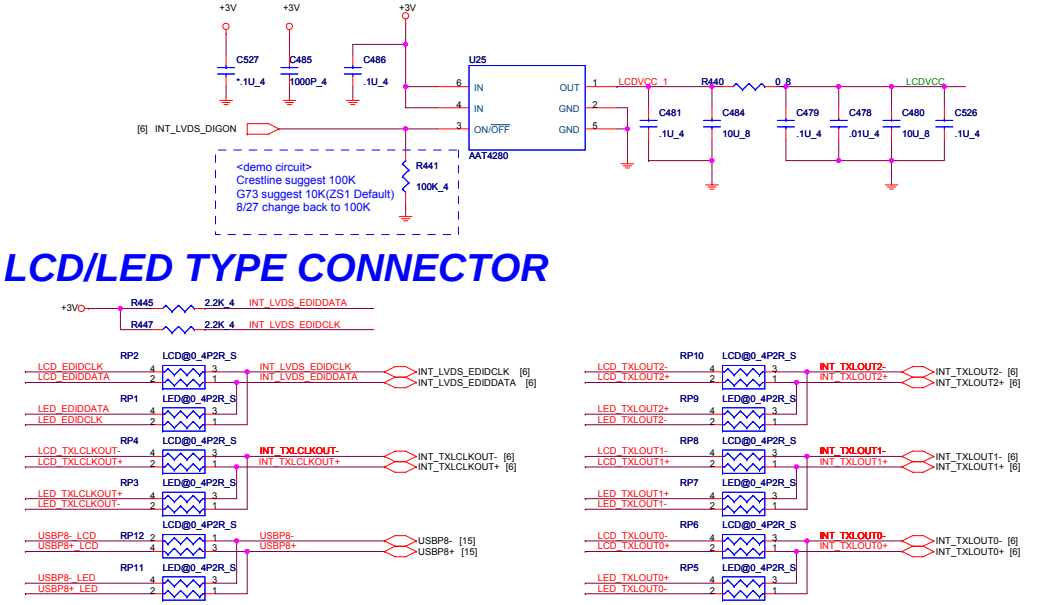
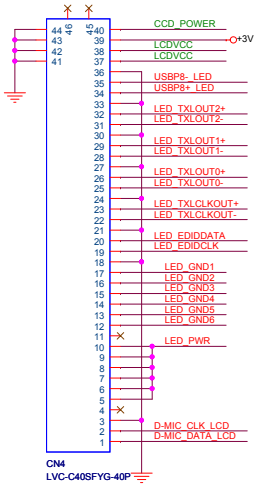
CRT PORT



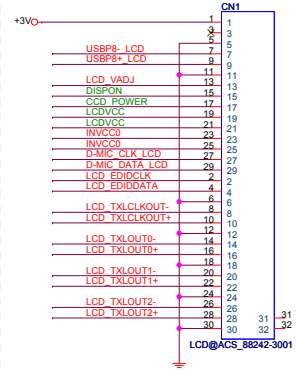
LCD/LED TYPE CONNECTOR



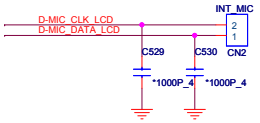
TOSHIBA LED PANEL MODULE



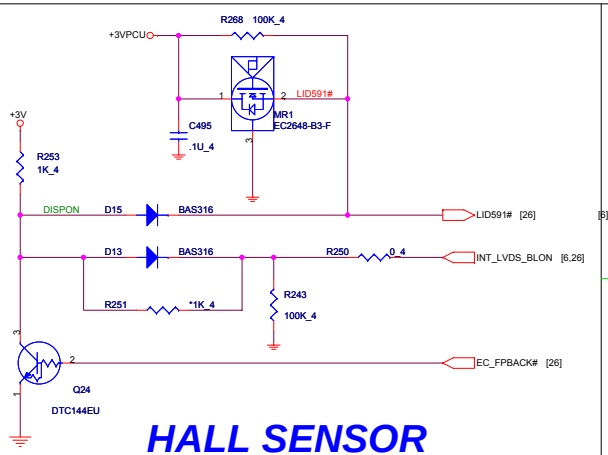
CHI MEI LED PANEL MODULE

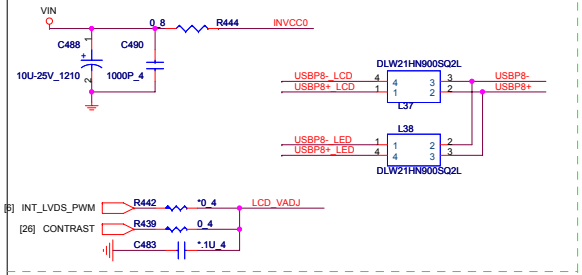


LCD PANEL MODULE

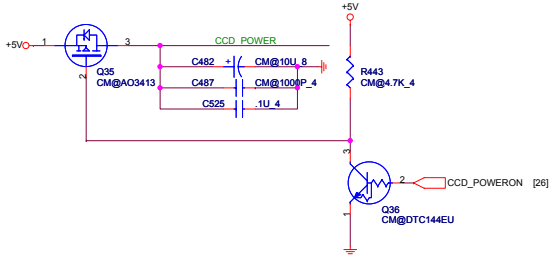


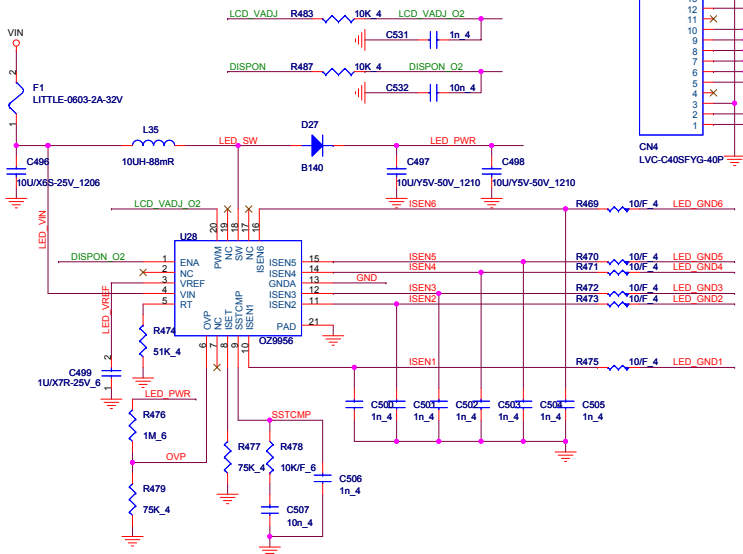
HALL SENSOR





CAMERA MODULE





Quanta Computer Inc.		
PROJECT : BU1 Santa Rosa		
Size	Document Number: LCD/CRT/LID/CAMERA	Rev: 3A
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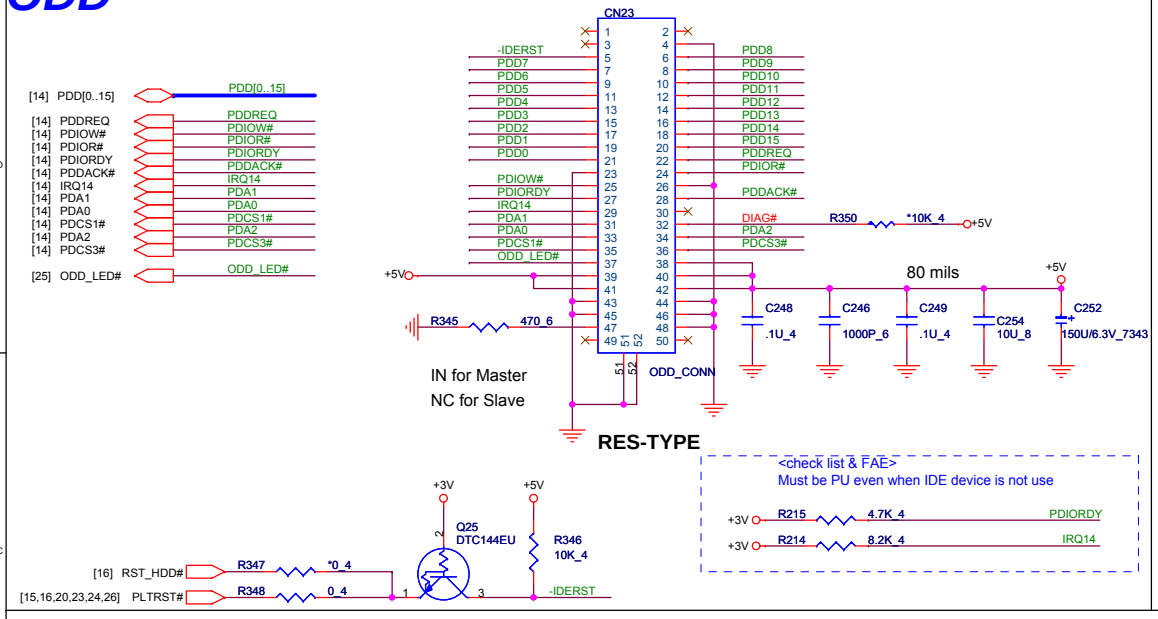
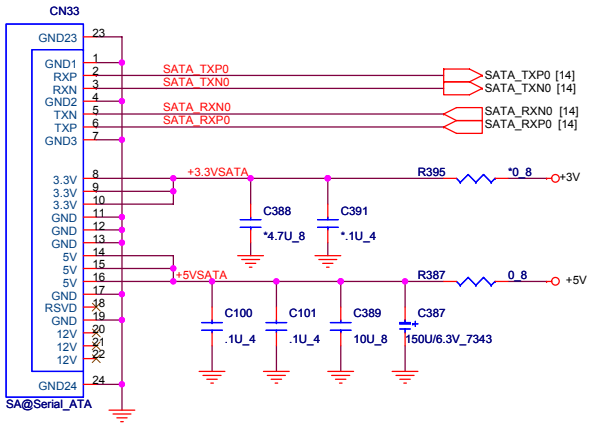
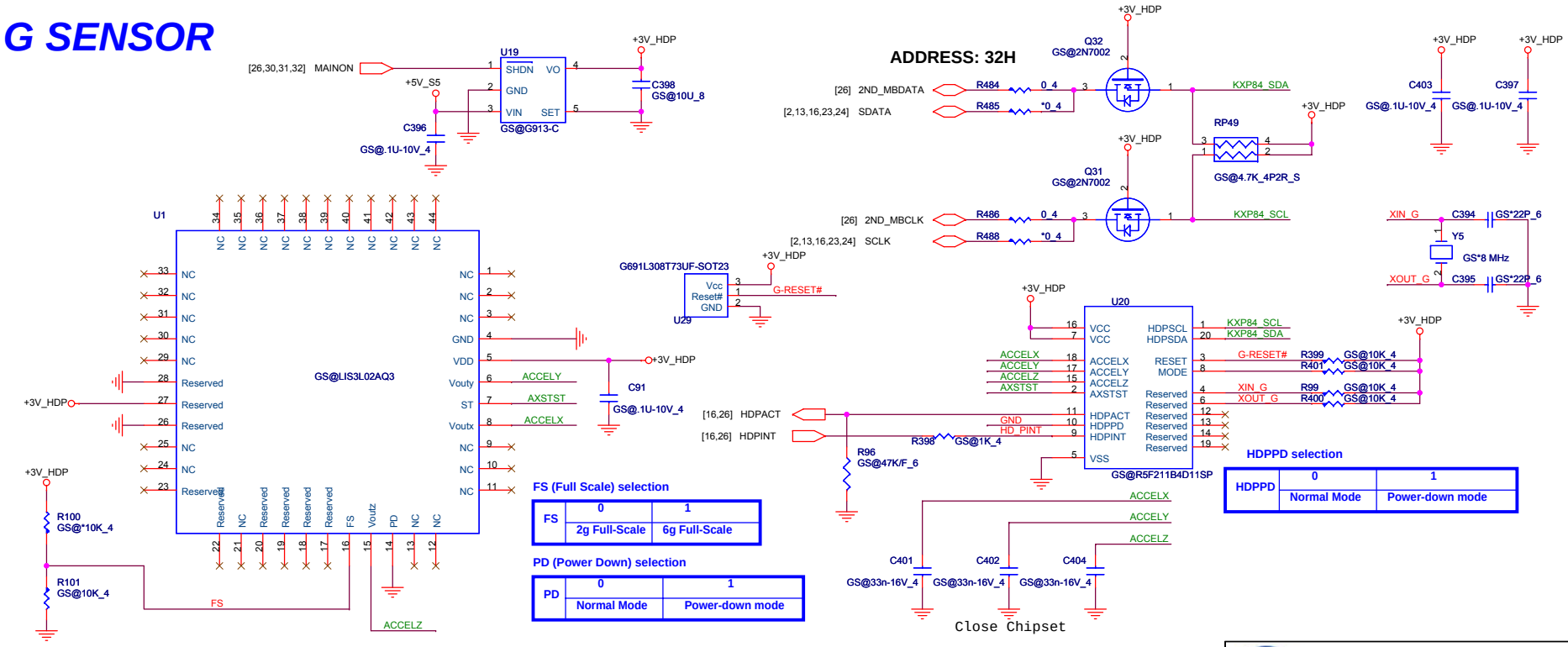
ODD



SATA HDD



G SENSOR



Close Chipset

Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	PATA/ODD/G SENSOR	2A

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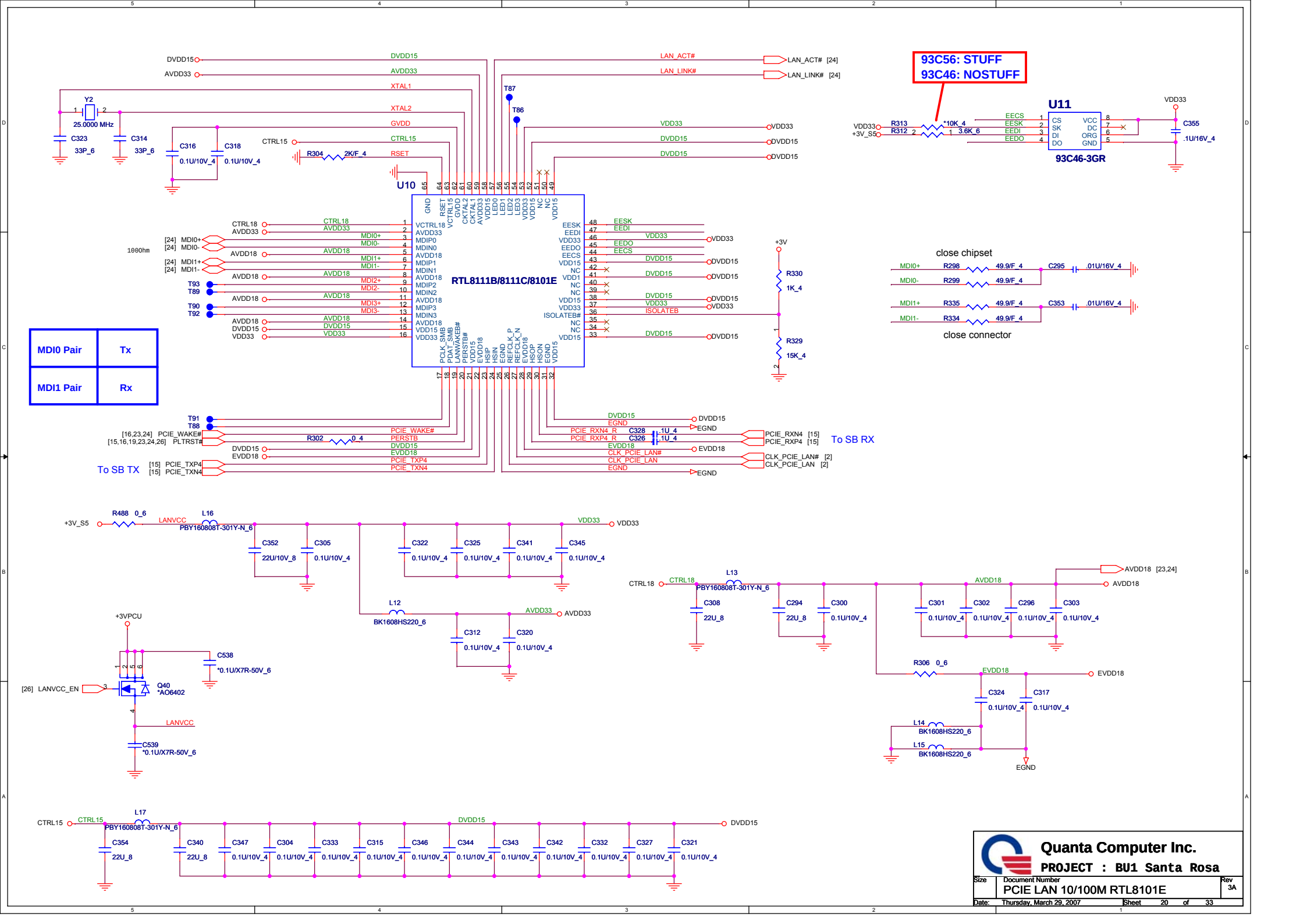
93C56: STUFF
93C46: NOSTUFF
U11
93C46-3GR
U10
RTL8111B/8111C/8101E
MDI0 Pair
Tx
MDI1 Pair
Rx
close chipset
close connector
To SB TX
To SB RX
Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
PCIE LAN 10/100M RTL8101E
Rev 3A
Thursday, March 29, 2007
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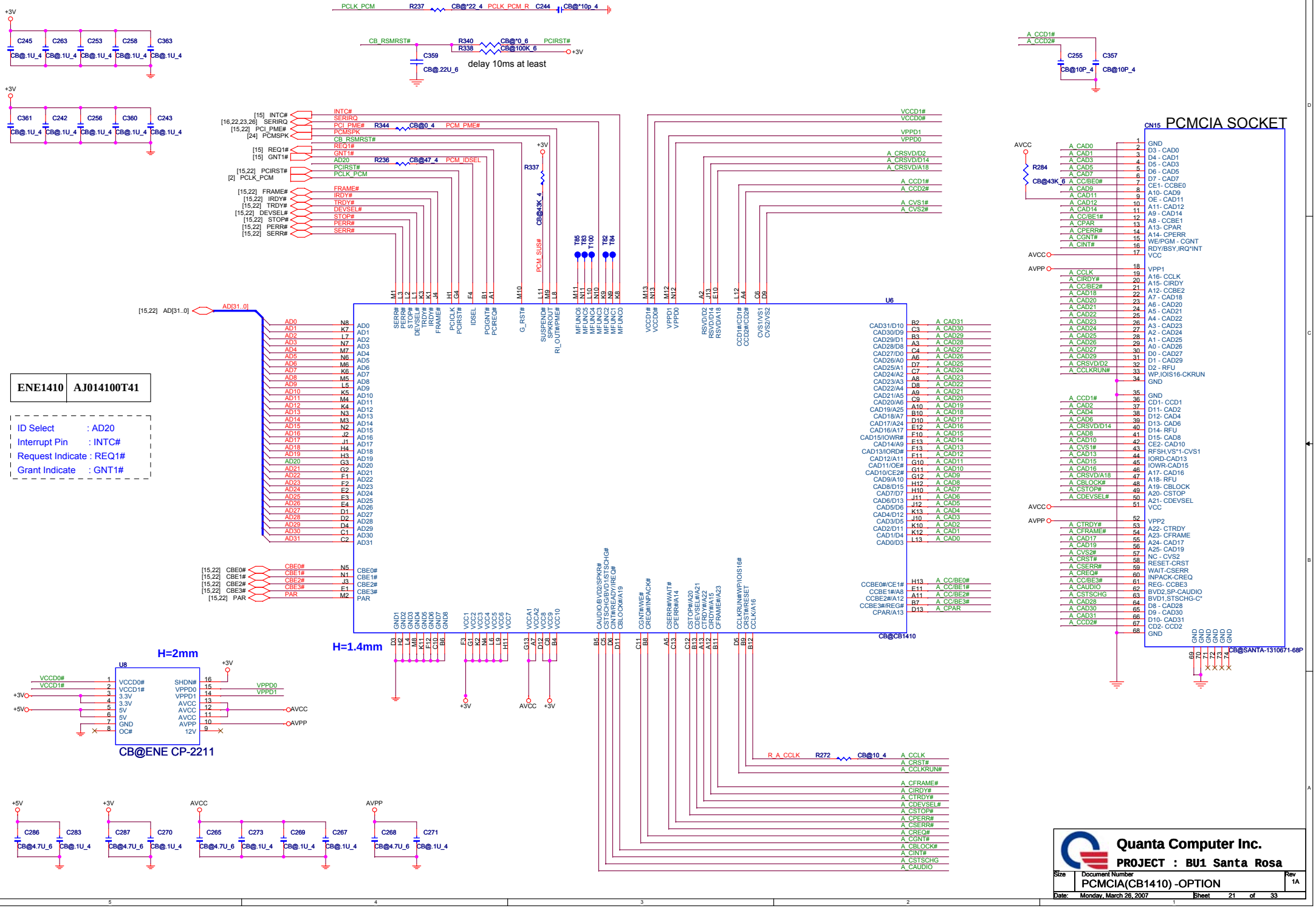
PCLK_PCM R237 CB@*22_4 PCLK_PCM_R C244 CB@*10p_4
CB_RSMRST# R340 CB@*0_6 PCIRST# R338 CB@100K_6 +3V
C359 CB@.22U_6
delay 10ms at least
+3V
C245 C263 C253 C258 C363
CB@.1U_4
C361 C242 C256 C360 C243
A_CCD1# A_CCD2#
C255 C357
CB@10P_4 CB@10P_4
PCMCIA SOCKET
CN15
CB@SANTA-1310671-68P
INTC# SERIRQ PCI_PME# PCMSPK CB_RSMRST# REQ1# GNT1# AD20 PCIRST# PCLK_PCM FRAME# IRDY# TRDY# DEVSEL# STOP# PERR# SERR#
R344 CB@0_4 PCM_PME#
R236 CB@47_4 PCM_IDSEL
R337 CB@43K_4 PCM_SUS#
R284 CB@43K_6
U6
AD[31..0]
CBE0# CBE1# CBE2# CBE3# PAR
VCCD1# VCCD0# VPPD1 VPPD0
A_CRSVD/D2 A_CRSVD/D14 A_CRSVD/A18
A_CCD1# A_CCD2#
A_CVS1# A_CVS2#
CB@CB1410
ENE1410 AJ014100T41
ID Select : AD20
Interrupt Pin : INTC#
Request Indicate : REQ1#
Grant Indicate : GNT1#
H=2mm
H=1.4mm
U8
CB@ENE CP-2211
R_A_CCLK R272 CB@10_4
C286 C283 C287 C270 C265 C273 C269 C267 C268 C271
CB@4.7U_6 CB@.1U_4
Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
PCMCIA(CB1410) -OPTION
Size Document Number Rev 1A
Date: Monday, March 26, 2007 Sheet 21 of 33

5 IN 1 CARD READER

R5C832 : AJ5C8320H26
R5C833 : AJ5C8330H05

U2B

VCC_PCI1 VCC_PCI2 VCC_PCI3 VCC_PCI4 VCC_PCI5 VCC_PCI6 VCC_RIN
VCC_ROUT1 VCC_ROUT2 VCC_ROUT3 VCC_ROUT4 VCC_ROUT5
VCC_3V VCC_MD
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10
AGND1 AGND2 AGND3 AGND4 AGND5

If VCC_3V tied to +3V, PME# function is not supported

When HWSPND# is controlled by system, the pull-up resistor(R4059) dose not need to apply.

PCI / OTHER

AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

PAR C/BE3# C/BE2# C/BE1# C/BE0# IDSEL
REQ# GNT# FRAME# IRDY# TRDY# DEVSEL# STOP# PERR# SERR#
GBRST# PCIRST# PCICLK PME# CLKRUN#
HWSPND# 832_SUS# D7 *BAS316 LPC_PD# [16]
MSEN XDEN UDIO5 UDIO3 UDIO4 UDIO2 UDIO1 UDIO0/SRIRQ#
SCL_CARD SDA_CARD
SERIRQ [16,21,23,26]
INTA# INTB# TEST

INTA# [15] Default setting:
INTB# [15] INTA# is assert to 1394
INTB# is assert to Cardreader

REQ0# AD17
GNT0# INTA#,B#

PowerOnReset for Vcc

When GRESET# is controlled by system, the pull-up resistor and capacitor do not need to apply.

U2A

XI XO FIL0 REXT VREF RSV
AVCC_PHY1 AVCC_PHY2 AVCC_PHY3 AVCC_PHY4
TPBIAS0 TPBN0 TPBP0 TPAN0 TPAP0
MDIO17 MDIO16 MDIO15 MDIO14 MDIO13 MDIO12 MDIO11 MDIO10
MDIO05 MDIO08 MDIO19 MDIO18 MDIO02 MDIO03 MDIO00 MDIO01 MDIO09 MDIO04 MDIO06 MDIO07

IEEE1394/SD

AS CLOSE AS POSSIBLE TO R5C833 and GUARD GND

24.576MHz Y1 better than 50ppm
R5C832 stuff only

H=1.2mm
H=1.4mm

22ohm/1A

XD_RE#/CLK should shield GND.
Close to CONN.

SD can't recognize issue in ES1 sample

Close to CONN.
Reduced external noise by FAE confirm

> 1 ms >60 ms >100 ms
VCC
GRST#
PRST#
PCLK(33MHz)

CARDREADER POWER

Q6 2N7002 Q7 AO3403
MC_PWR_CTRL_0# MC_PWR_CTRL_0
R207 10K_4 R218 150K_4 C224 2.2U_6
30mil
VCC_XD
C125 .01U_4 C120 .01U_4 C117 .01U_4
U4 *G5241T1U C206 *1U_4 C232 *4.7U_6

CN28 *CARD_READER_PROCONN-MXP038-A0-4010

Reserve MS DUO card issue (For A-test only)

Q28 Q27 Q26 *2N7002E
R376 0_4 R355 *10K_4 R354 0_4

EEPROM

* NOT Use EEPROM :
==>UDIO5 need pull-high.
* Use EEPROM :
==>UDIO5 need pull-down.

R193 10K_4 R194 10K_4
SDA_CARD SCL_CARD

1394

C114 .01U_4 C112 .33U_6 C99 .01U_4
R114 R113 1394@56.2/F_4
1394@CL-2M2012-121JT
L20 L21
1394@0_4P2R_S RN1 RN2
TPA0P TPA0N TPB0P TPB0N
L1394_TPA0+ L1394_TPA0- L1394_TPB0+ L1394_TPB0-
R112 R111 1394_COM R389 1394@5.1K/F_4 C392 1394@270P_4
AS CLOSE AS POSSIBLE TO R5C833

CN32 1394@1394-C13118-102-4P-V

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	R5C832/833(5IN1/1394)	3A

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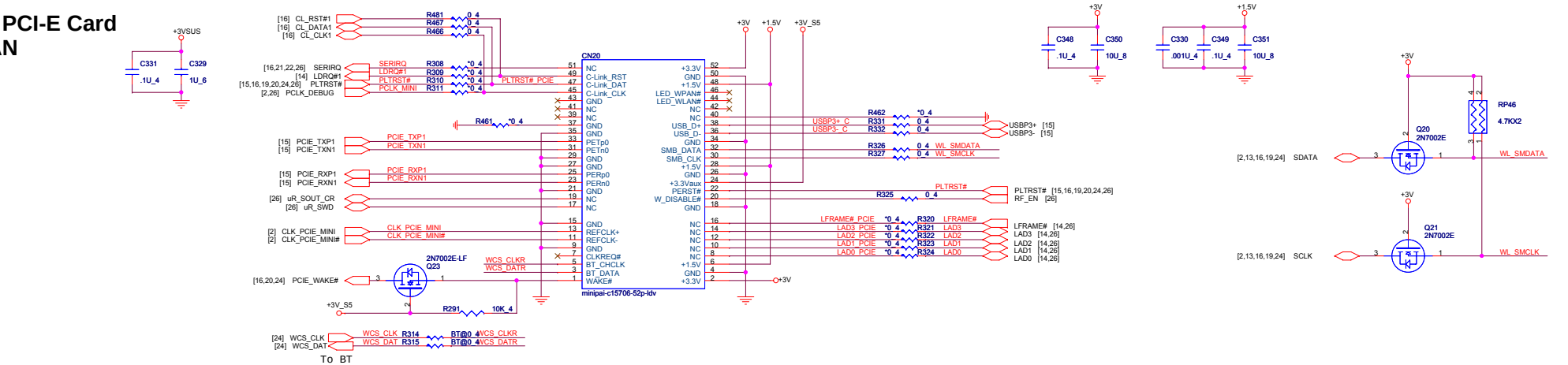
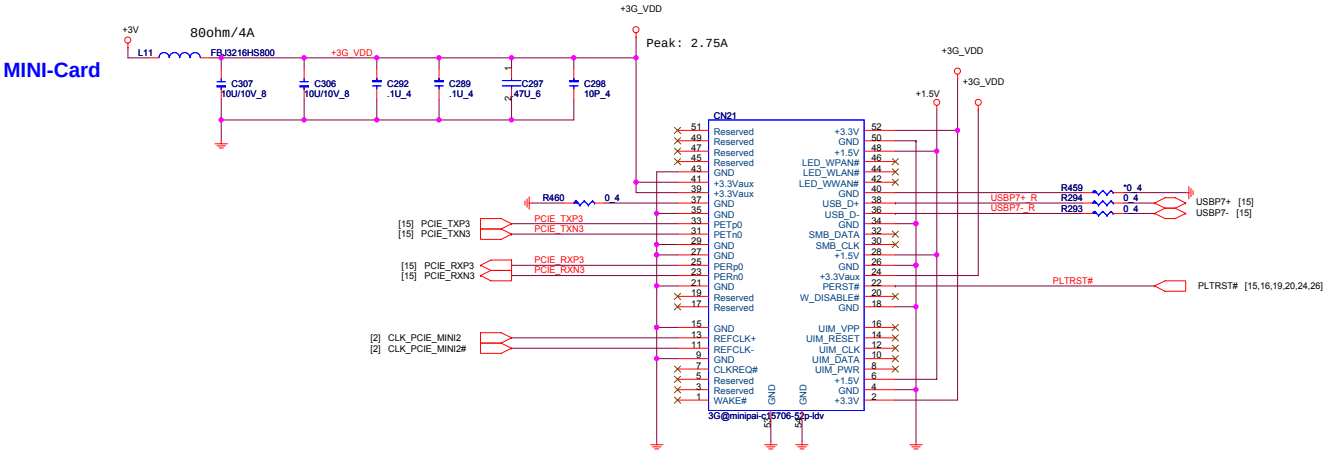
Mini PCI-E Card
WLAN



MINI-Card



NB SINK

HOLE8 H-C165D122P2-8
HOLE9 H-C165D122P2-8

CPU SINK

HOLE3 H-C165D122P2-8
HOLE5 H-C165D122P2-8
HOLE4 H-C165D122P2-8
HOLE6 H-C165D122P2-8

MINI CARD SINK

HOLE13 H-C197D122P2-8
HOLE14 H-C197D122P2-8

MB SINK

HOLE7 *H-C236D94P2-8
HOLE1 *H-C236D106P2-8
HOLE20 *H-C236D94P2-8
HOLE21 *H-C236D94P2-8
HOLE12 *H-TC295BC236D94P2-8
HOLE16 *H-C315D94P2-8
HOLE10 *H-C236D94P2-8
HOLE2 *H-C236D106P2-8
HOLE19 *H-C189D189N
HOLE15 *H-C197D94P2-8

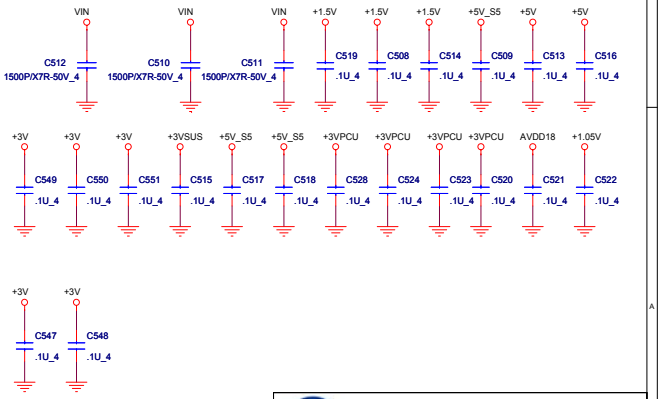
PCMCIA SINK

HOLE17 *H-C177D138P2-8
HOLE18 *H-C177D138P2-8

MDC PCMCIA SINK

HOLE11 H-C165D122P2-8
HOLE22 *H-C177D138P2-8

EMI



Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	MINI PCIE/HOLE	3A
Date: Thursday, March 29, 2007	Sheet 23 of 33	

INT KeyBoard

RP43 10KX8

CP1 100Px4 · CP2 100Px4 · CP3 100Px4 · CP5 100Px4 · CP6 100Px4

CN8 → BL121-28R-TAND-28P-L-BU1

CN37 → 196130-34020T-34P-R

CN5 → 8817-3400L-34P-R

CN6 → BL121-28R-TAND-28P-L-BU1

Keyboard Side

Audio Board

CN12 → BT@88266-100XX-XXX-10P-R

Wire Cable 1.25mm Pitch

U18 SN74LVC1G86DCKR

CN7 → BL121-14R-TAND-14P-L-BU1-BU1

FFC Cable 0.5mm Pitch

PAD1 EMIPAD134X71

T/P

CN11 → *88058-6

CN10 → BL123-06R-6P-L

FFC Cable 1.0mm Pitch

Finger Printer

CN14 → FP@88266-040XX-XXX-4P-R

Wire Cable 1.25mm Pitch

BLUETOOTH MODULE CONNECTOR

CN9 → BT@88266-100XX-XXX-10P-R

Wire Cable 1.25mm Pitch

USB_DETACH: Low USB connect
High USB disconnect

RJ45/USB

U12 G545B2RD1U

CN19 → BL123-12R-12P-L-BU1

Wire Cable 1.25mm Pitch

BUTTONS ON KB COVER

CN13 → BL123-10R-TAND-10P-L-BU1

SW1

FFC Cable 1.0mm Pitch

D32 CHN217 · D33 CHN217

U30 TC7SH08FU

NEW CARD'S POWER SWITCH

Q15 NEW@2N7002E · Q14 NEW@2N7002E

RP44 NEW@4.7KX2_4

U9 NEW@TPS2231PWG4

H=1.2mm

Q13 NEW@*DTC144EU

CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)

New card (BTO)

CN16 → NEW@13160171-1

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	New Card/Keyboard/WTB	3A

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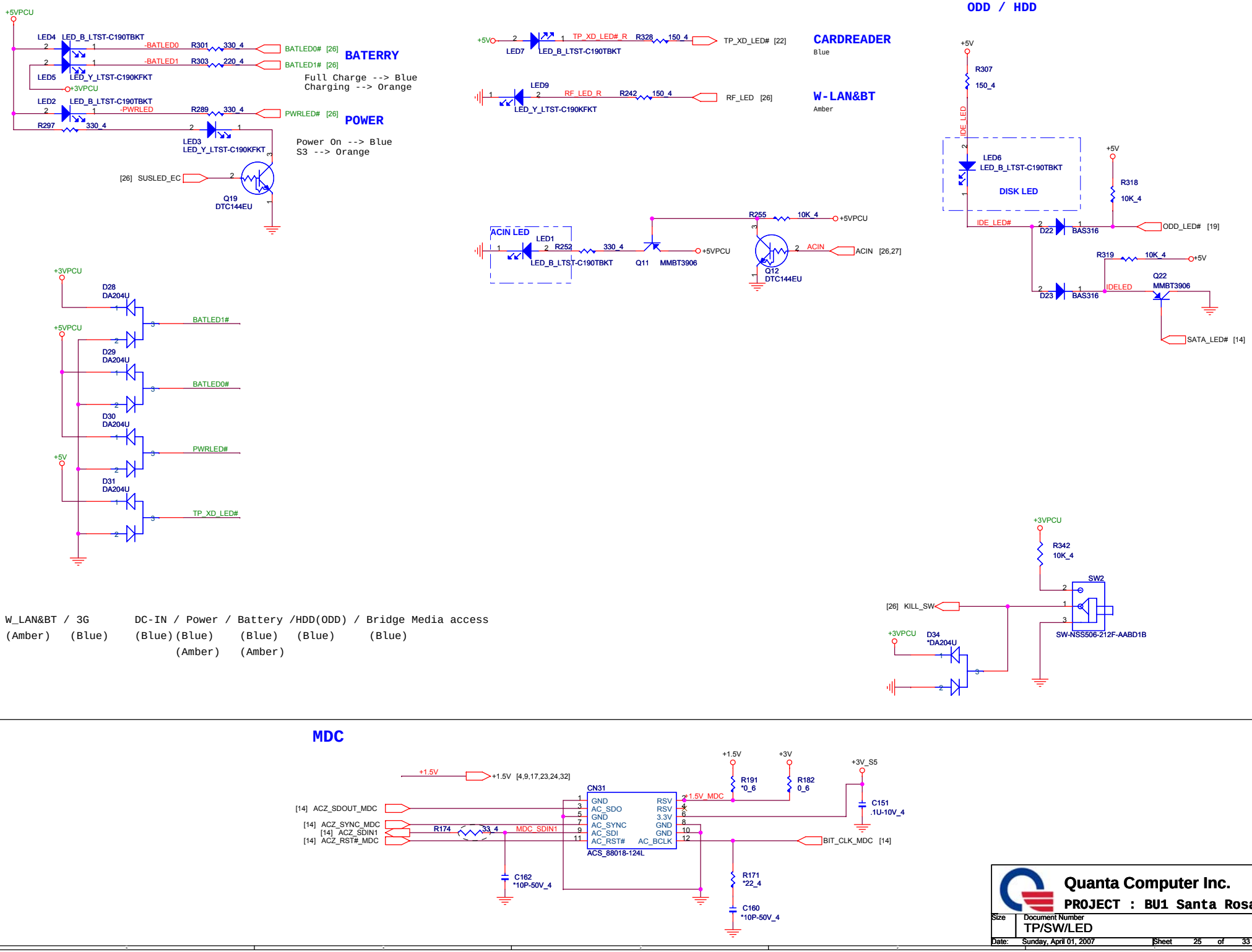
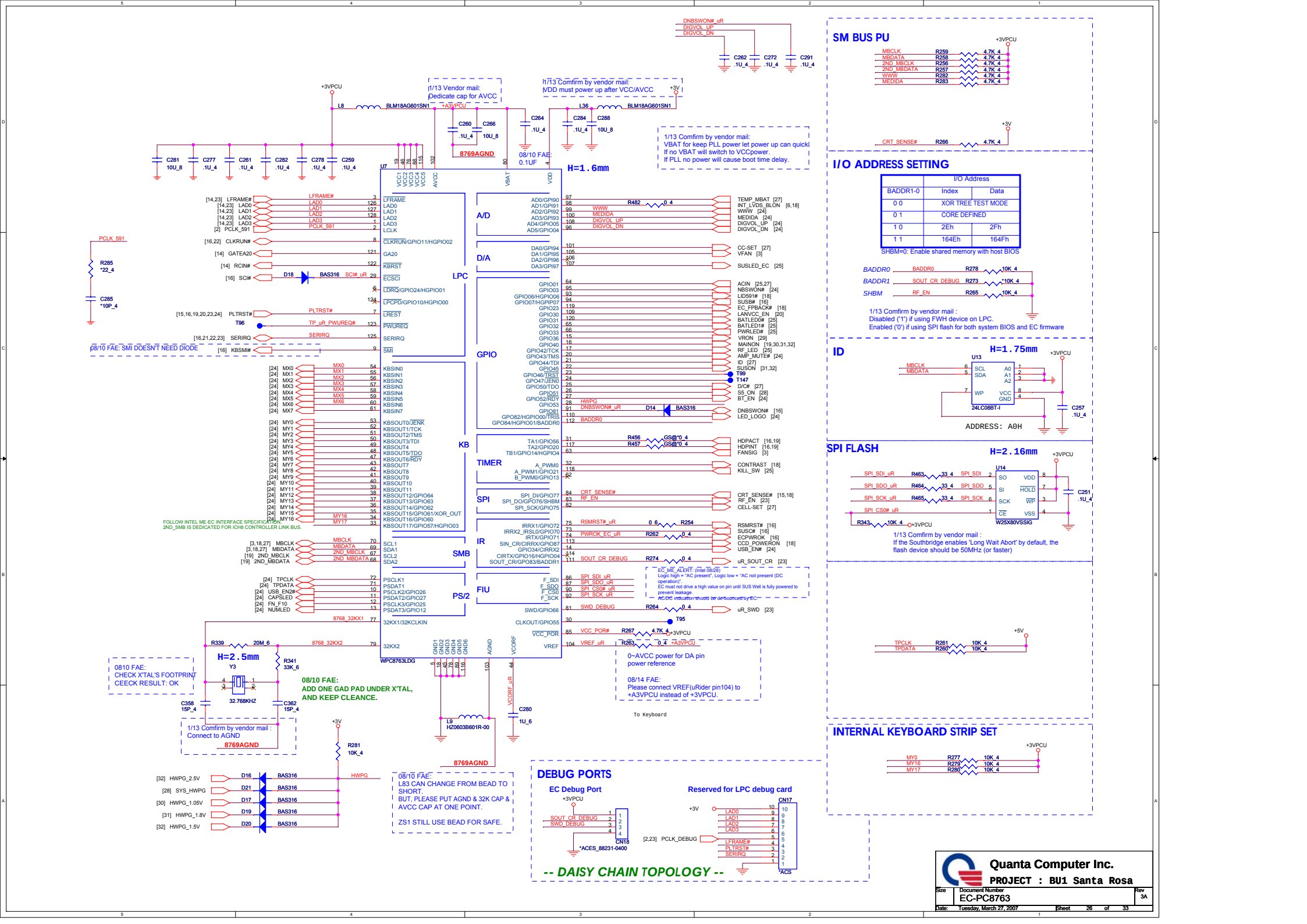


Quanta Computer Inc.		
PROJECT : BU1 Santa Rosa		
Size	Document Number: TP/SW/LED	Rev: 3A
Date: Sunday, April 01, 2007	Sheet 25 of 33	


SM BUS PU
I/O ADDRESS SETTING
I/O Address
BADDR1-0
Index
Data
0 0
XOR TREE TEST MODE
0 1
CORE DEFINED
1 0
2Eh
2Fh
1 1
164Eh
164Fh
SHBM=0: Enable shared memory with host BIOS
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
ID
H=1.75mm
ADDRESS: A0H
SPI FLASH
H=2.16mm
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)
INTERNAL KEYBOARD STRIP SET
DEBUG PORTS
EC Debug Port
Reserved for LPC debug card
-- DAISY CHAIN TOPOLOGY --
1/13 Vendor mail:
Dedicate cap for AVCC
1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC
1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick!
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.
08/10 FAE: SMI DOESN'T NEED DIODE
FOLLOW INTEL ME-EC INTERFACE SPECIFICATION.
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.
0810 FAE:
CHECK X'TAL'S FOOTPRINT
CEECK RESULT: OK
08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.
1/13 Comfirm by vendor mail :
Connect to AGND
0~AVCC power for DA pin
power reference
08/14 FAE:
Please connect VREF(uRider pin104) to
+A3VPCU instead of +3VPCU.
08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
To Keyboard
Quanta Computer Inc.
PROJECT : BU1 Santa Rosa
Size
Document Number
EC-PC8763
Rev
3A
Date: Tuesday, March 27, 2007
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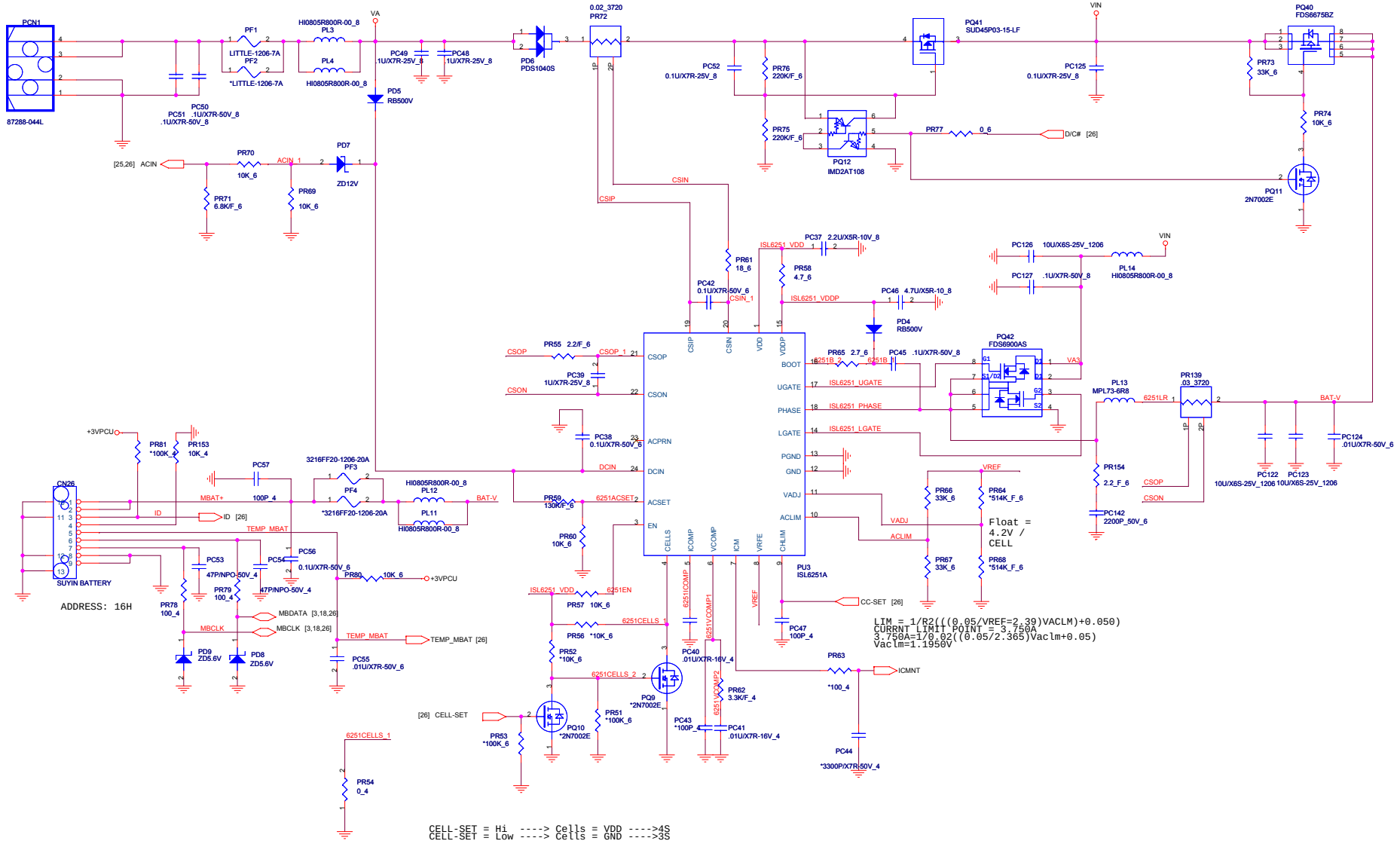

Quanta Computer Inc.

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Size	Document Number	Rev
	ISL6251	3A

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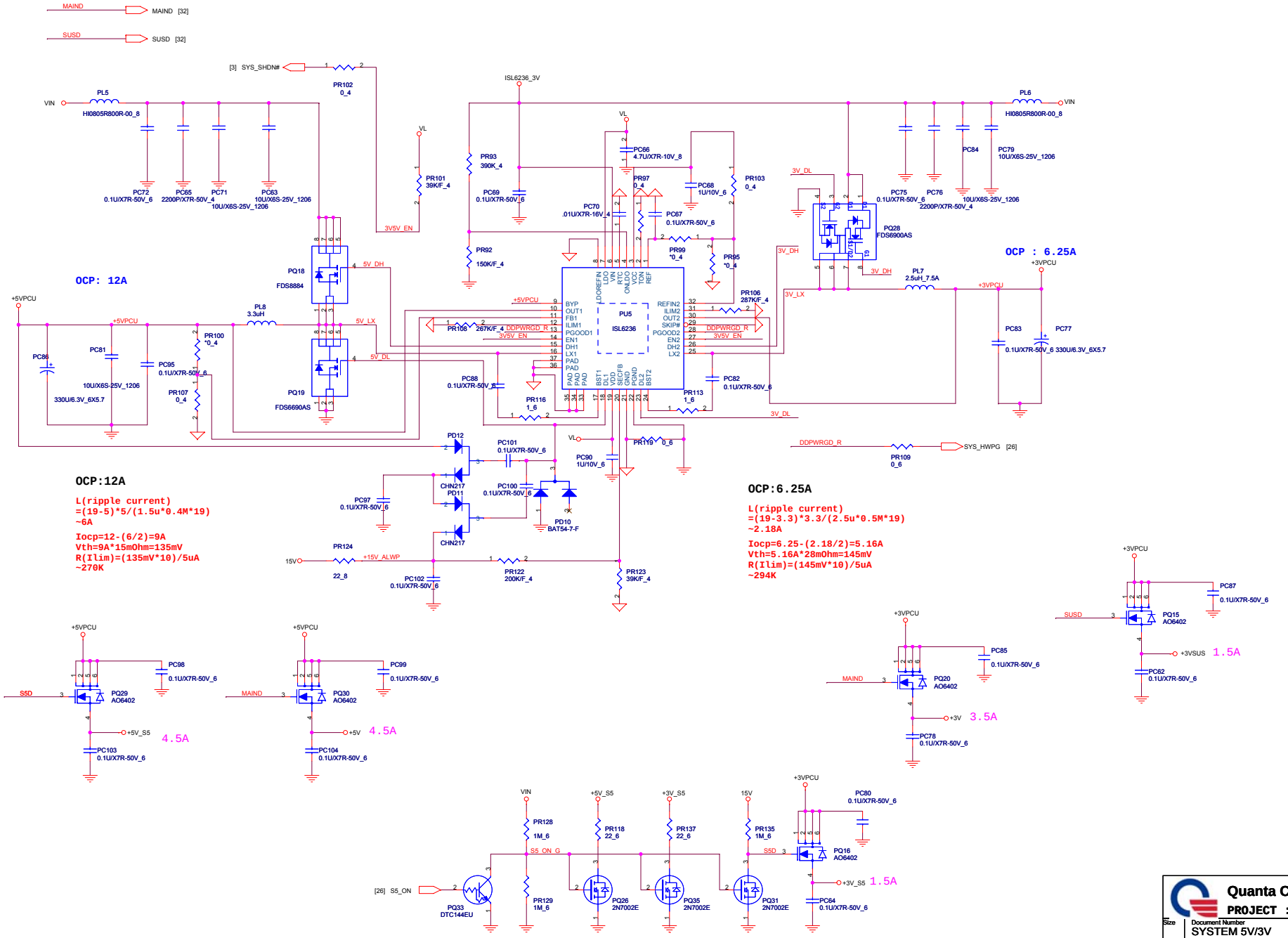
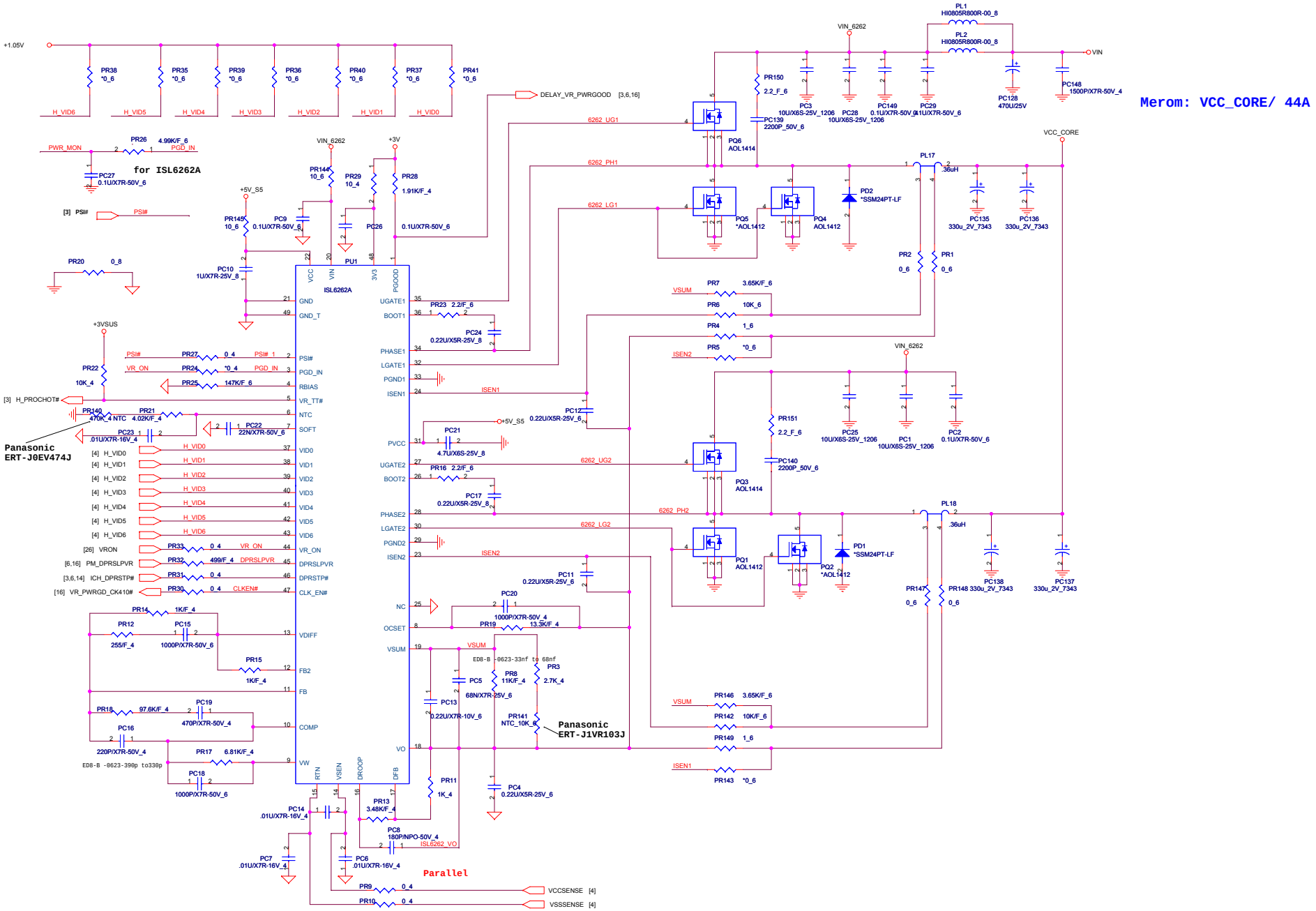


Quanta Computer Inc.

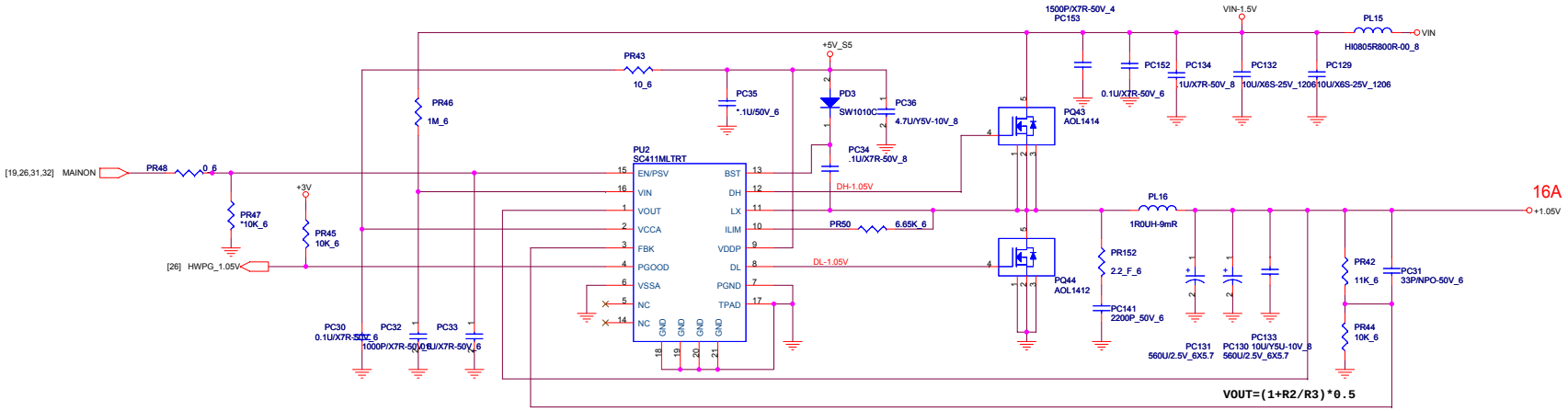
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	SYSTEM 5V/3V	1A

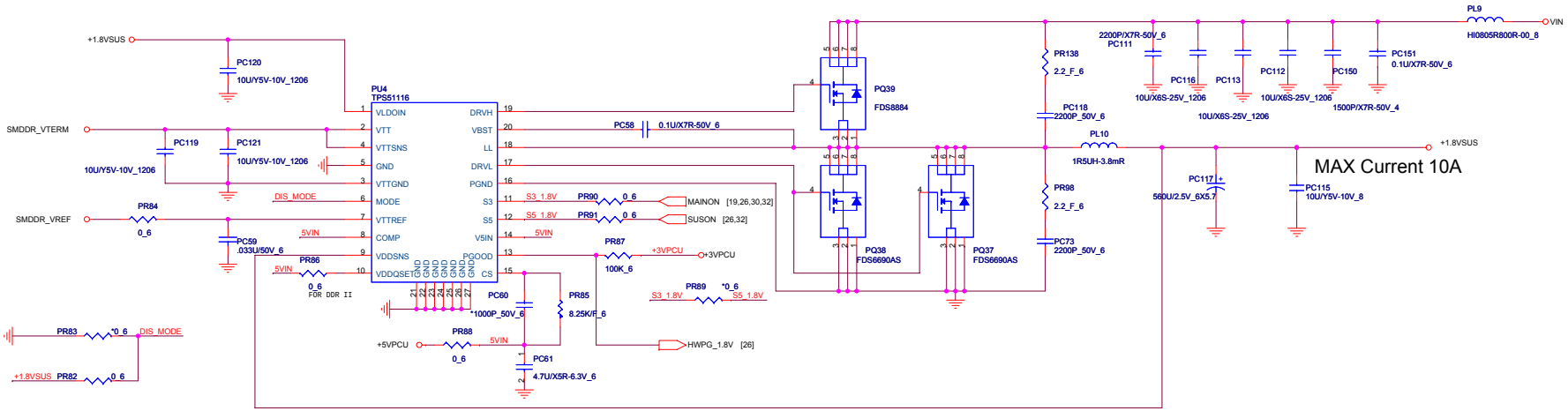
Date: Monday, March 26, 2007 Sheet 28 of 33



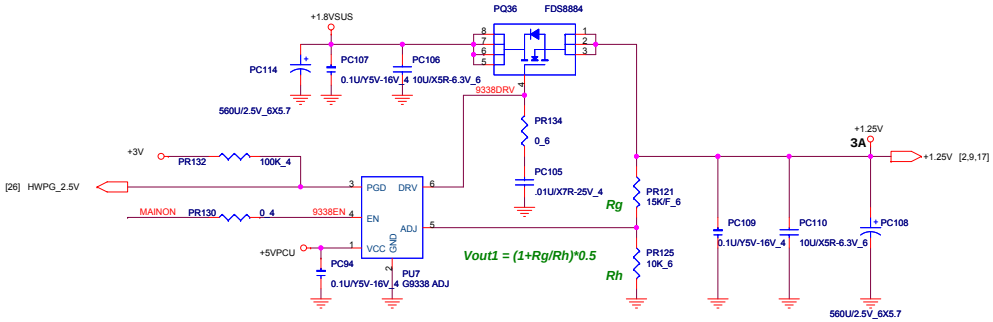
Quanta Computer Inc.	
PROJECT : BU1 Santa Rosa	
Size	Document Number: CPU CAORE (6262A) — Rev: 2A
Date: Thursday, March 29, 2007	Sheet 29 of 33

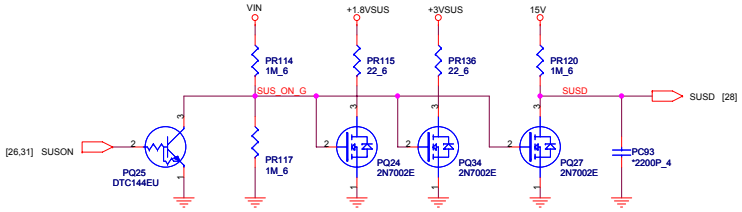


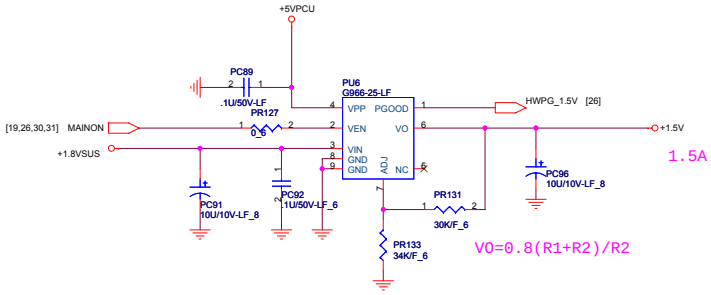
Quanta Computer Inc.		
PROJECT : BU1 Santa Rosa		
Size	Document Number: VTT 1.05V (SC11)	Rev: 2A
Date: Thursday, March 29, 2007	Sheet 30 of 33	

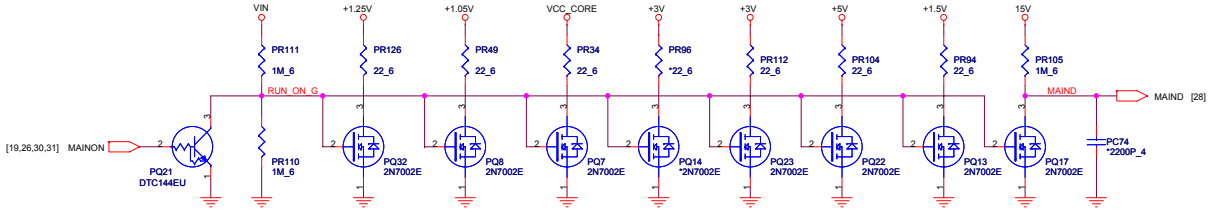


Quanta Computer Inc.		
PROJECT : BU1 Santa Rosa		
Size	Document Number: DDR2 1.8V(TP1116)	Rev: 3A
Date: Sunday, April 01, 2007	Sheet 31 of 33	









Quanta Computer Inc.

PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	DISCHARGE/1.5V/VCC1.25	1A

Date: Monday, March 26, 2007 Sheet 32 of 33

Model	REV	DATE	CHANGE LIST	NOTE
BU1	00	20061218	**FIRST RELEASED : 20061218**	
	01	20061225	Page02: Change CLK GEN. low power outs from +1.05V to +1.25V.Because VDD_IO will drop out when high loading	Circuit modify
			Page02: REV_01 Remove CLK_MCH_OE#_R had pull up resistor,because had be pull up at NB side	Circuit modify
			Page03: Del R382,R383,Q60,D39	Circuit modify
			Page04: Del R176 for FBS signals batter return path under +1.05V plane	Circuit modify
			Page08: Change Crestline VCC_AXM to 1.25V, reference to SR ww48 MoW. reserved 0 ohm resister	Circuit modify
			Page16: Add D43 to avoid leakage from EC to SB,Del R242	Circuit modify
			Page18: REV_01 Reserved LCD/LED type panel module and Digital/analogy MIC	Circuit modify
			Page19: Modify G-Sensor circuit	Circuit modify
			Page22: Reserved LPC_PD# control signal from SB to R5C833	Circuit modify
			Page23: Increase HOLE	Circuit modify
			Page24: Add 0.1u CAP. C810 from +5VPCU to GND	Circuit modify
			Page25: Modify IDE LED circuit	Circuit modify
			Page26: Reserved R756,R766 for EC control G-Sensor	Circuit modify
			Page27: Add 3 cell Battery always setting circuit	Circuit modify
			Page28: Add +3V_S5 discharge circuit	Circuit modify
			Page30: Reserved PD resistor to avoid leakage voltage	Circuit modify
			Page32: Reserve +3V discharge circuit	Circuit modify
	1A	20061227	**A TEST (PCB REV_1A) RELEASED : 20061227**	
	2A	20070201	Page03: Modify thermal protect circuit and FAN control	Circuit modify
			Page14: Modify RTC charge current / SB strip setting / Reserved PU resistor on SATALED# signal / Change XTAL capacitor value	BOM/Circuit modify
			Page16: Reserver Pull down resistor on HDPINT signal / Reserved C-Link to WLAN / Delete FM function / Add Board ID	Circuit modify
			Page18: Change panel backlight signal pull up resistor / Change camera power source / Add LED type panel circuit / Add fuse on CRT power	BOM/Circuit modify
			/ Reserved EMI choke on USB signals and add EMI solution / Add RC circuit on LED panel driver IC	Circuit modify
			Page19: Modify LDO power source / Add Microprocessor reset IC / Reserved G-sensor SMBUS to SB chipset	Circuit modify
			Page22: Reserved Cardreader external EEPROM	Circuit modify
			Page23: Separate RF enable/disable pin from WLAN and 3G card / Add EMI solution and Reserved C-Link circuit / Delete 3G card function	Circuit modify
			/ Add HOLE for card Bus connector	Circuit modify
			Page24: Increase CN7 pin for control illumination logo and enable/disable USB port power / Add capacitor on keyboard signals for EMI	Circuit modify
			/ Change LAN/B cable connector / Delete FM function	Circuit modify
			Page25: Modify battery LED and RF SW power source / Delete 3G card LED	Circuit modify
			Page26: Modify EC control circuit / Add EMI solution / Change XTAL capacitor value	BOM/Circuit modify
			Page27: Change fuse rating and switch MOS	Circuit modify
			Page29: Add EMI solution	Circuit modify
			Page30: Add EMI solution	Circuit modify
			Page31: Add EMI solution	Circuit modify
			Page32: Add EMI solution	Circuit modify
	3A	20070326	Page03: Add CAP to GND for FAN controller IC U12 power pin decoupling	Circuit modify
			Page13: Change DDR socket height	Circuit modify
			Page18: Exchange Dioid and Fuse placement	Circuit modify
			Page20: Add control LAN power circuit to enable/disable LAN	Circuit modify
			Page22: Change 1394 connector type and delete card reader connector 2nd source	Circuit modify
			Page23: Change mini-card 3V power source from +3VSUS to +3V_S5 for support wake on WLAN from S3/S4 / Change HOLE pad size	Circuit modify
			Page24: Reserve EMI capacitor / add solve insert PCMCIA Card speaker has bo sound circuit	Circuit modify
			Page25: Add ESD protect circuit	Circuit modify
			Page27: Change MOS footprint	Circuit modify
		20070327	Page14: Modify RTC short pad footprint	Circuit modify
			Page17: Modify inductance type	Circuit modify
			Page23: Add capacitors for EMI	Circuit modify
			Page24: Modify FFC connector footprint	Circuit modify
			Page26: Add capacitor for EMI	Circuit modify
			Page27: Reserve EMI circuit	Circuit modify
		20070328	Page22: Delete card reader external EEPROM	Circuit modify
			Page23: Add pull up resistor on PCIE_WAKE# signal	Circuit modify
		20070329	Page18: Delete CMO LED type connector	Circuit modify
			Page25: Reserve ESD protect on kill-switch	Circuit modify
			Page31: Stuff R/C Snubber for EMI	BOM modify

Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

Size	Document Number	Rev
	Change List	3A

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