

14" BY6/BY6D Comal Block Diagram

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

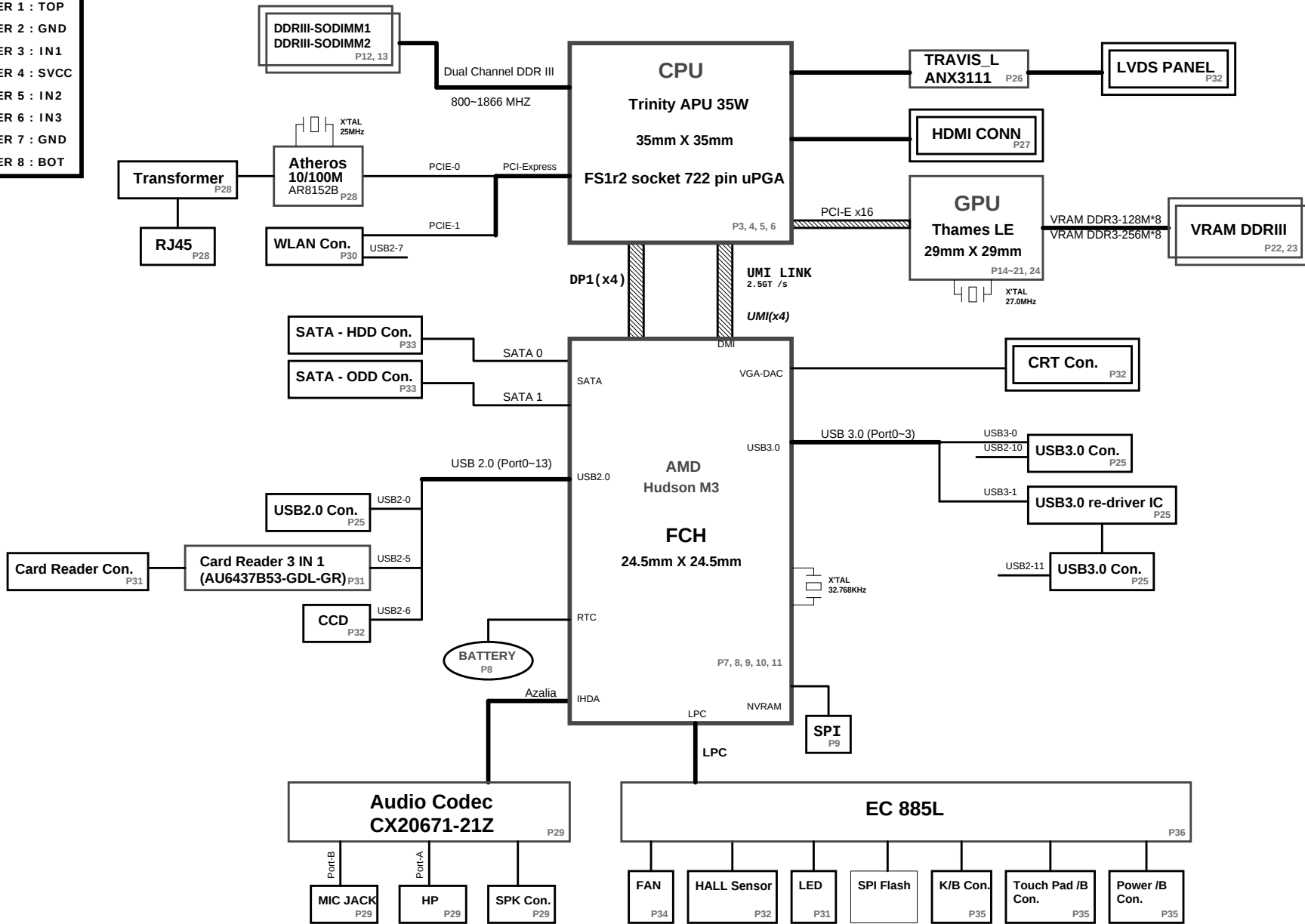


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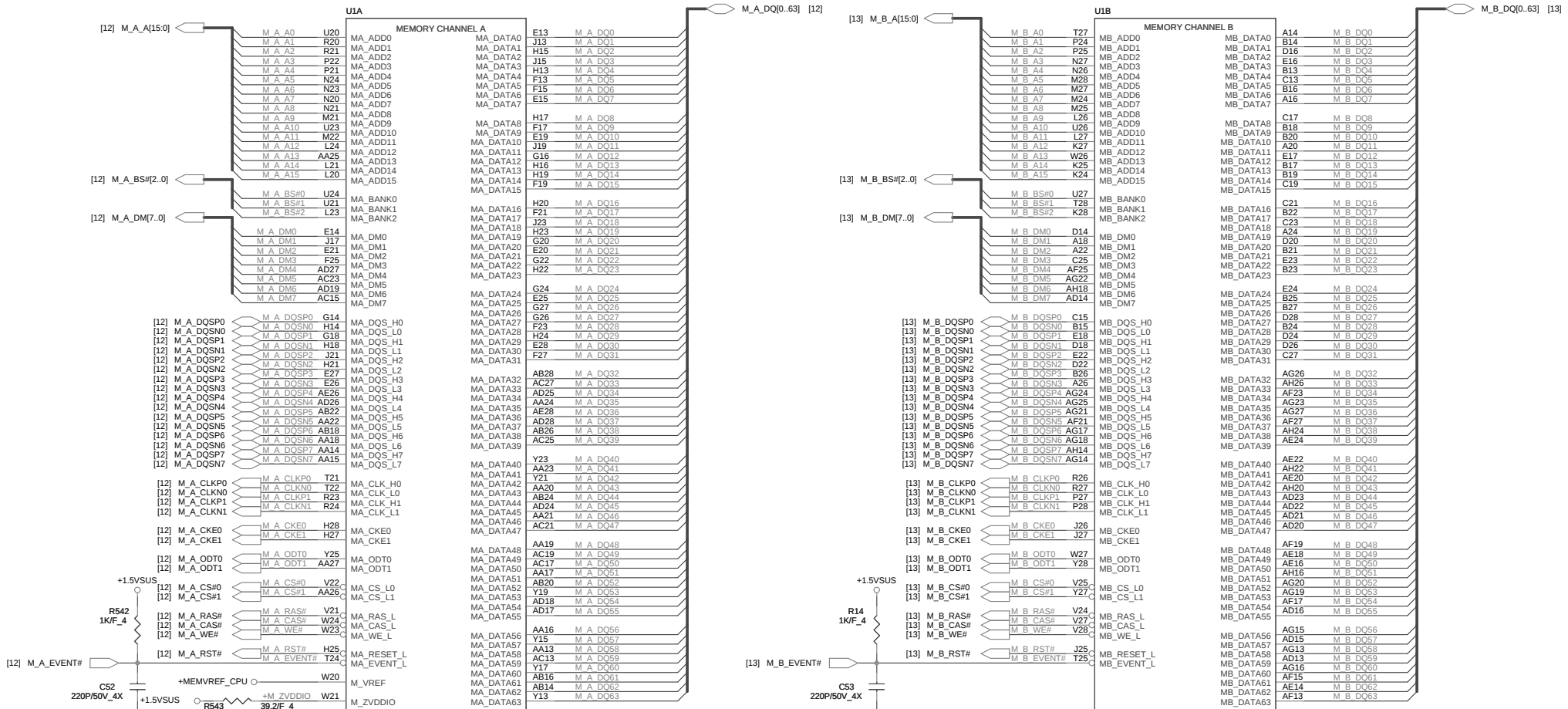
PAGE	DESCRIPTION	BOI -FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3 - 6	Processor	CPU
7 - 11	FCH	CLG
8	RTC	RTC
12 - 13	DDRIII SO-DIMM	DDR
14 - 21	Thames/Seymour(M2)	VGA
22 - 23	VRAM - DDR3	VGA
24	PX	VGA
25	USB Connector	USB
	USB 3.0 Redriver	U3B
	USB Sleep Charger	SLC
26	TRAVIS Decoder	LDS
27	HDMI comm part	HDM
	CEC	CEC
28	Atheros LAN	LAN
29	Codec (CX20671-21Z)	ADO
30	MINI Card (Wi-Fi & WIMAX)	MNW
31	Card reader	MMC
	LED	LED
32	VGA Connector	VGA
	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
33	HDD	HDD
	ODD	ODD
34	Thermal	THC
	FAN	THC
35	KeyBoard	KBC
	TP&FP board	TPD,FPD
	Power SW	PSW
36	EC NPCE885LA0DX	KBC
37	Charger (ISL88731CHRTZ-T)	PWM
38	System 5V/3V	PWM
39	DDR 1.5V	PWM
40	+1.2V_VDDPR	PWM
41	+1.1V_DUAL	PWM
42	+VCC_CORE 2+1	PWM
43	Discharge	PWM
44	GPU_CORE	PWM
45	Power Sequence	
46	Change List	

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3VPCU	+3.3V	AC/DC Insert enable	S0-S5
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P	S0
+1.5VSUS	+1.5V	S5_ON	S0-S3
+1.5V	+1.5V	MAIN_ON	S0
+1.2V_VDDPR	+1.2V	VDDA_PWRGD	S0
+1.1V_DUAL	+1.1V	+1.1V_DUAL_EN	S0-S5
+1.1V	+1.1V	MAIN_ON	S0
+VDD_CORE	~	VDDA_PWRGD	S0
+VDDNB_CORE	~	VDDA_PWRGD	S0
+VGPU_CORE		PX_MODE	S0
+1.8V_GPU	+1.8V	PE_GPIO1	S0
+1V_GPU	+1V	DGPU_PWREN	S0
+3V_GPU	+3.3V	PE_GPIO1	S0
+1.5V_GPU	+1.5V	PX_MODE_D	S0
+2.5V_VDDA	+2.5V	MAIN_ON	S0

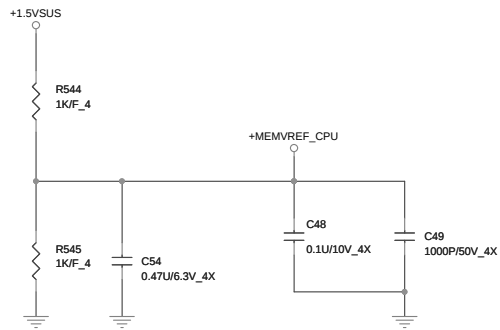
GND PLANE	PAGE
 GND_SIGNAL	32
 8769GND	36
 GND	28
 GND	ALL
 ADOGND	29

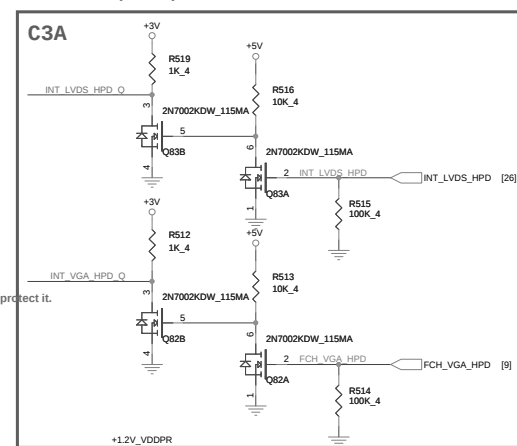
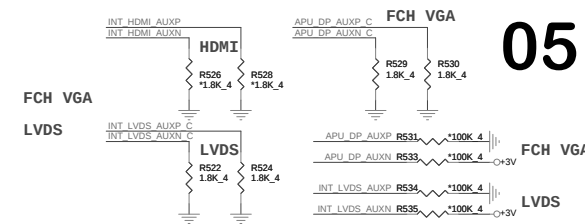
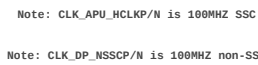
ITEM	Value Code	FUNCTIONS
1	CEC@	CEC
2	Debug@	HDT+ Debug
3	EV@	DISCRETE
4	IV@	UMA
5	U3@	Internal USB 3.0
6	1G4@	VRAM 1Gb*4
7	1G8@	VRAM 1Gb*8
8	2G@	VRAM 2Gb
9	AMD@	AMD VRAM
10	DIS@	DISCRETE
11	M2@	M2 FCH
12	M3@	M3 FCH
13	NMP@	LPC Debug Card
14	PX4@	PX4 Mode
15	PX5@	PX5 Mode
16	Sam@	Samsung VRAM
17	U2@	USB 2.0 (colay W USB 3.0)



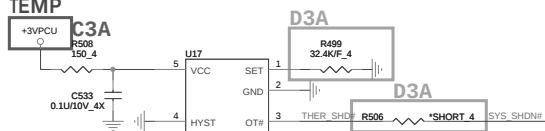
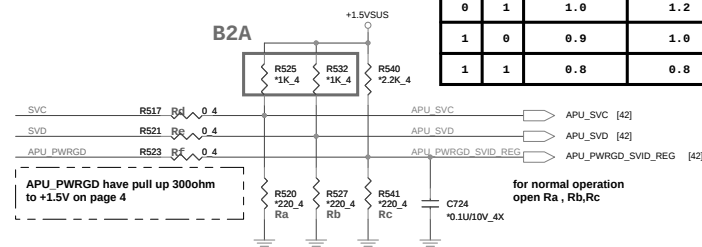
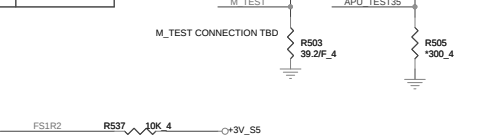
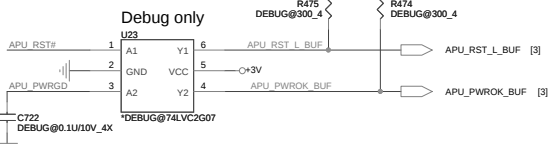


Trinity APU Soldermask openings for all bottom side vias/TTPs under FS1

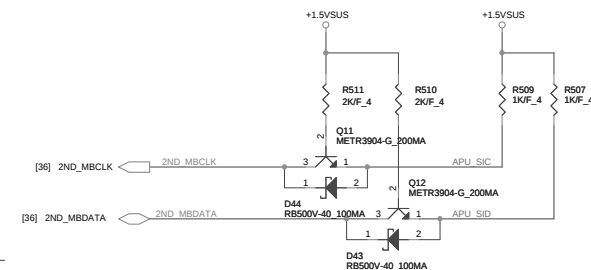


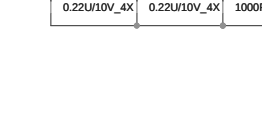
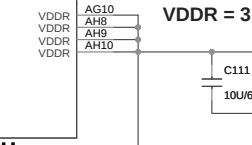
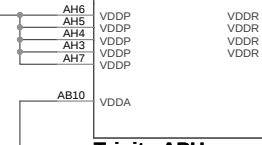
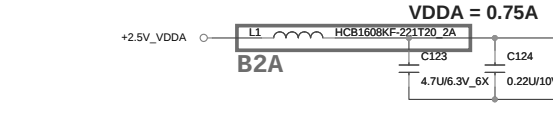


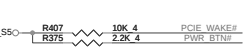
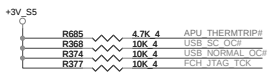
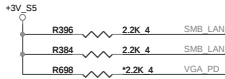
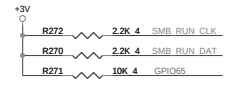
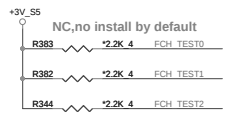
		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



Rset(Kohm)=0.0012T*T-0.9308T+96.147, Shut down on 76dgree
Hysteresis is 30C

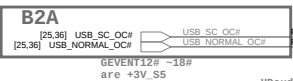




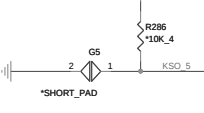
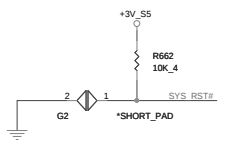
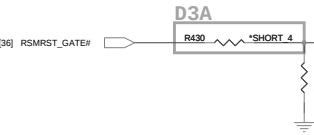


For Dimm

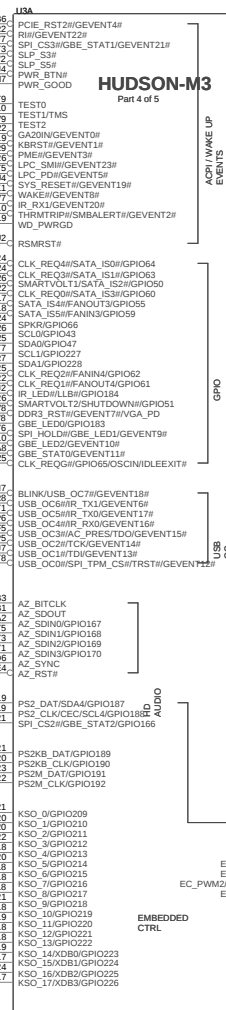
For Lan&WiFI



Note:LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported

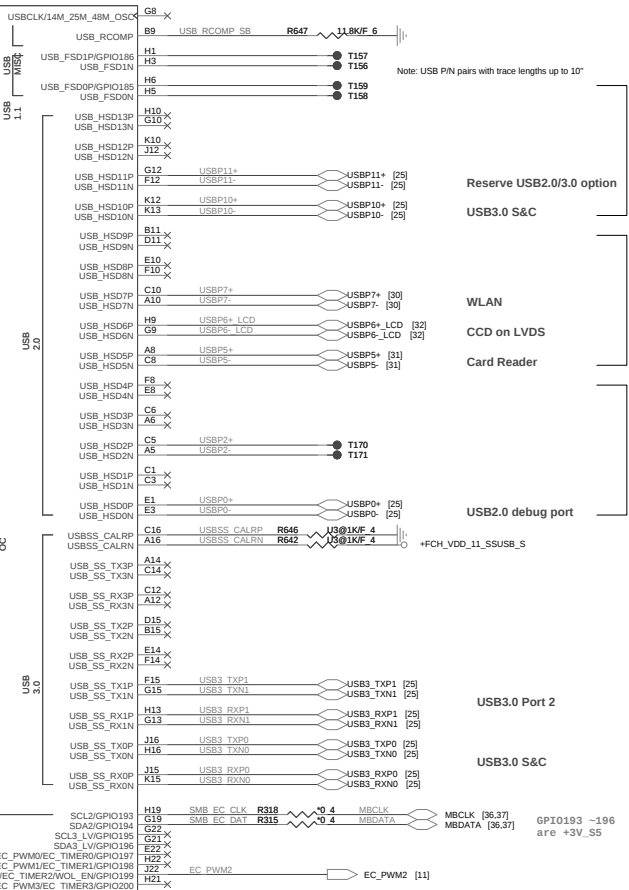
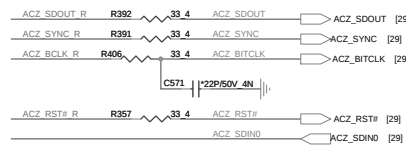


Provided test points from checklist



Hudson-M3

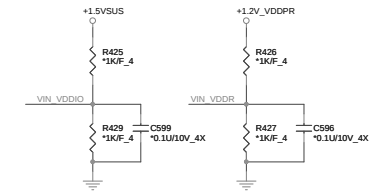
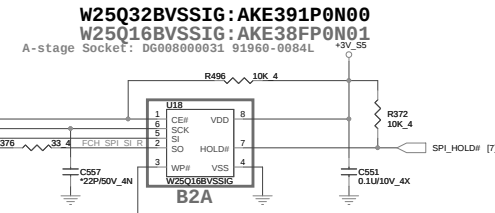
To Azalia



EC	FCH	Device	I2C_Device(S)
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery
I2Ce_2(M)		EEPROM	APU
I2Ce_3(M)		VGA Thermal	
	I2Cf_3(M)		APU
	I2Cf_1(M)	Lan	wLan
	I2Cf_0(M)	Dimm	Clk Gen

EC will Conflict with FCH, did not mount R315&R318

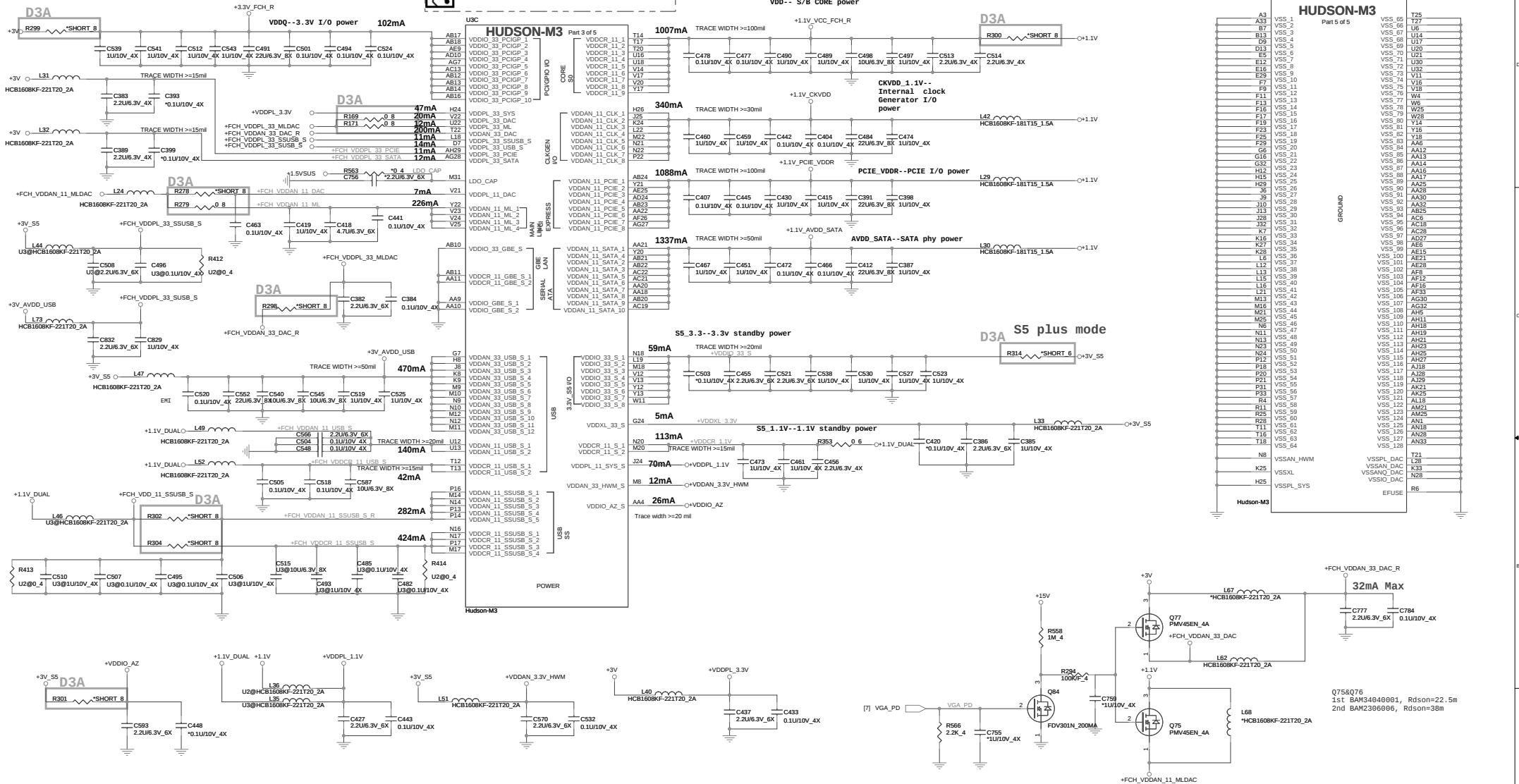




[7] BOARD_ID8
[7] BOARD_ID9
[7,35] BOARD_ID10



PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



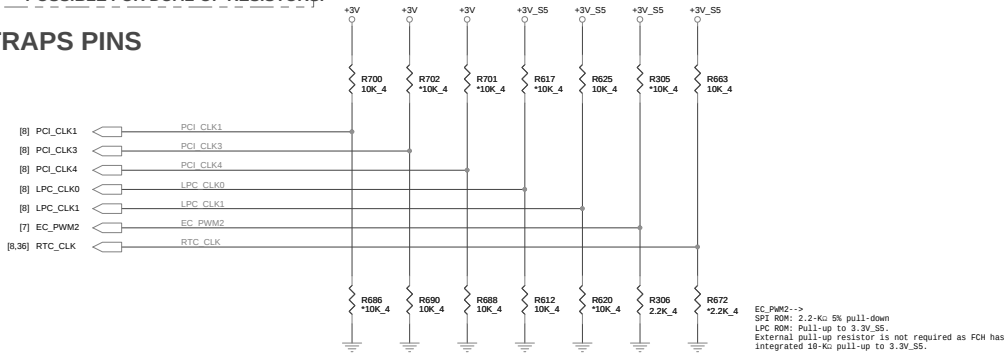
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Size	Document Number FCH 4/5(POWER)	Rev 1A
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OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

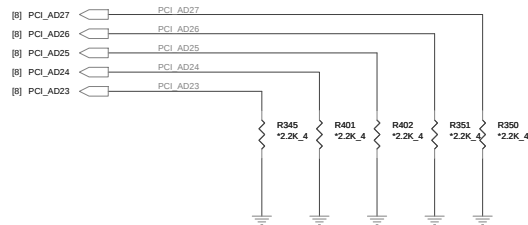


REQUIRED STRAPS

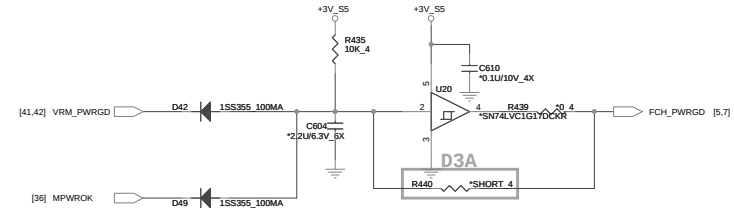
	-----	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIe Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIe Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT



FCH PWRGD CKT

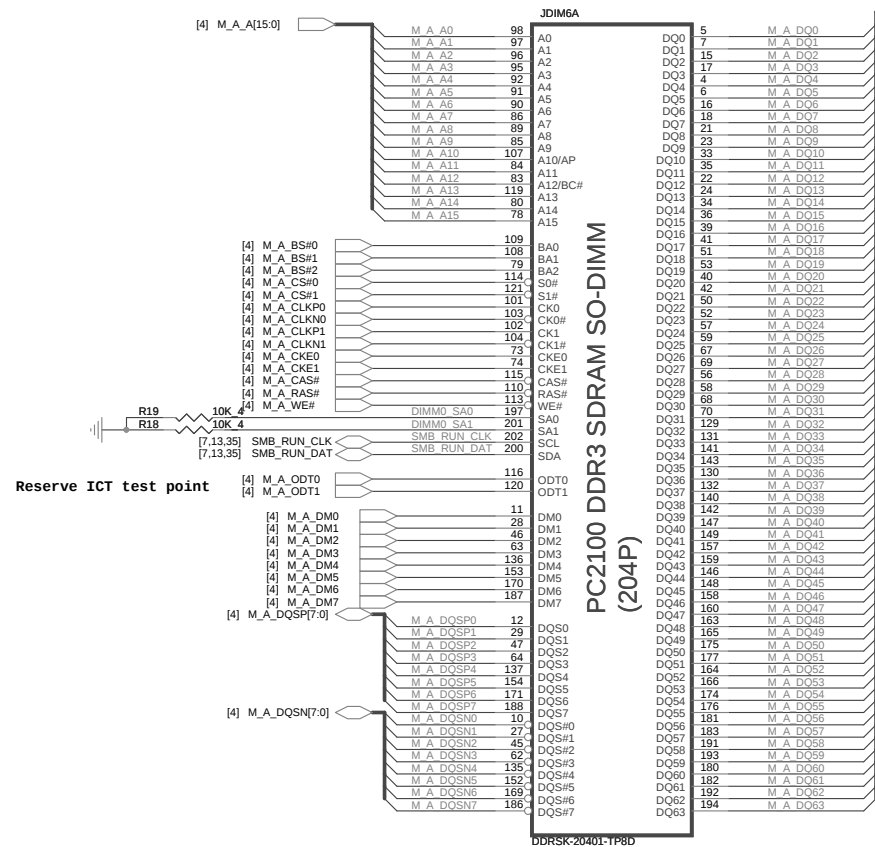


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PROJECT : BY6/BY6D

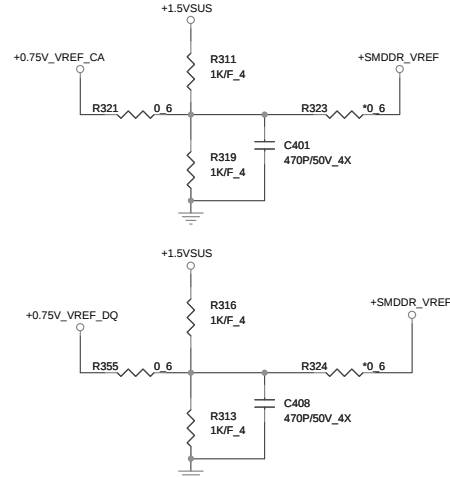
Size	Document Number	Rev
	FCH 5/5(STRAP & PWRGD)	1A
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DDR_STD(DDR)

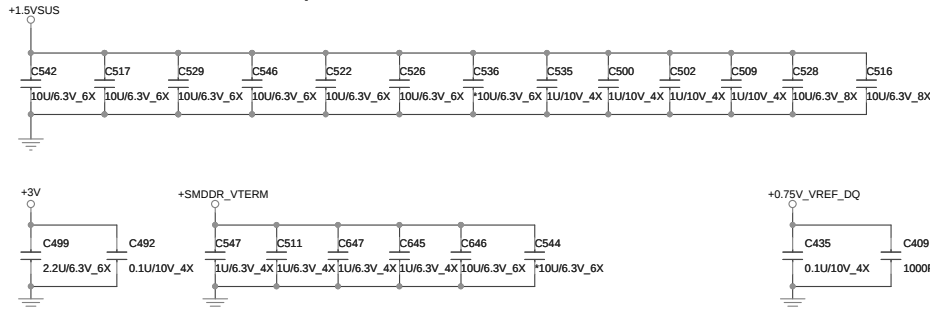
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Reserve ICT test point

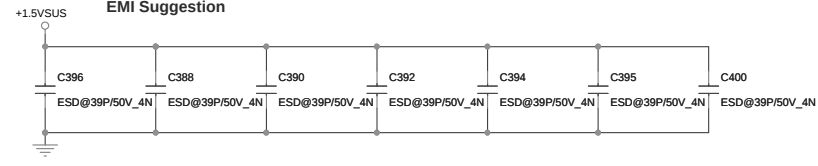


Place these Caps near So-Dimm0.

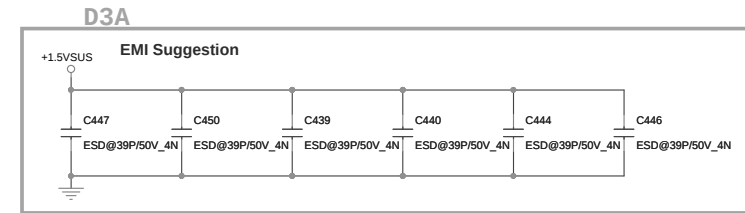
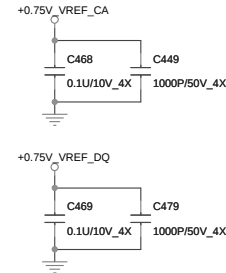
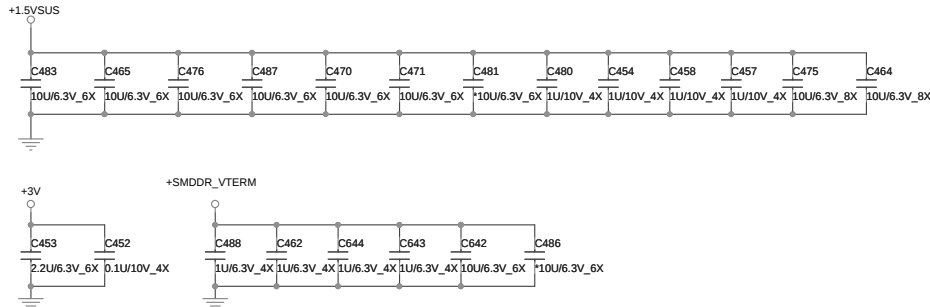
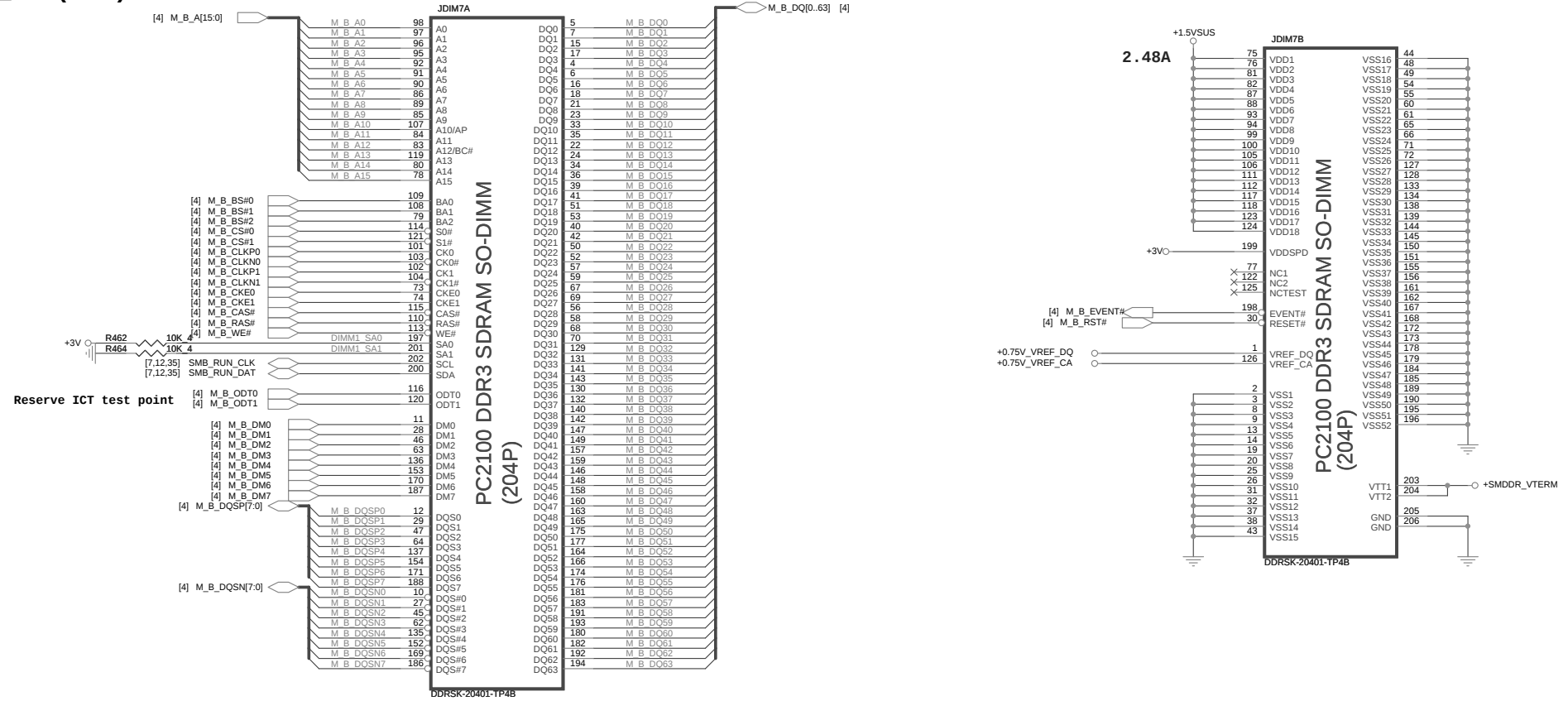


D3A

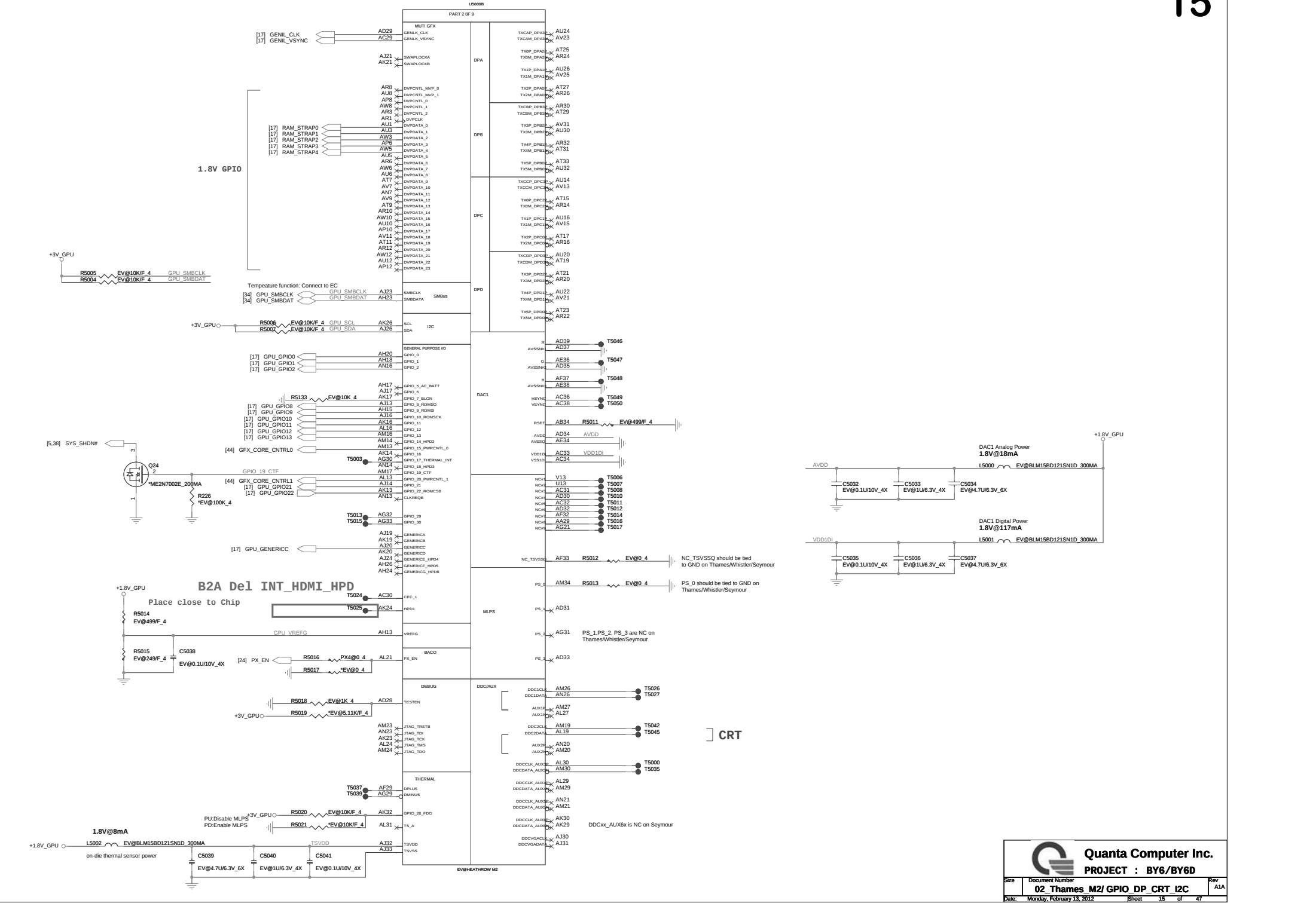
EMI Suggestion

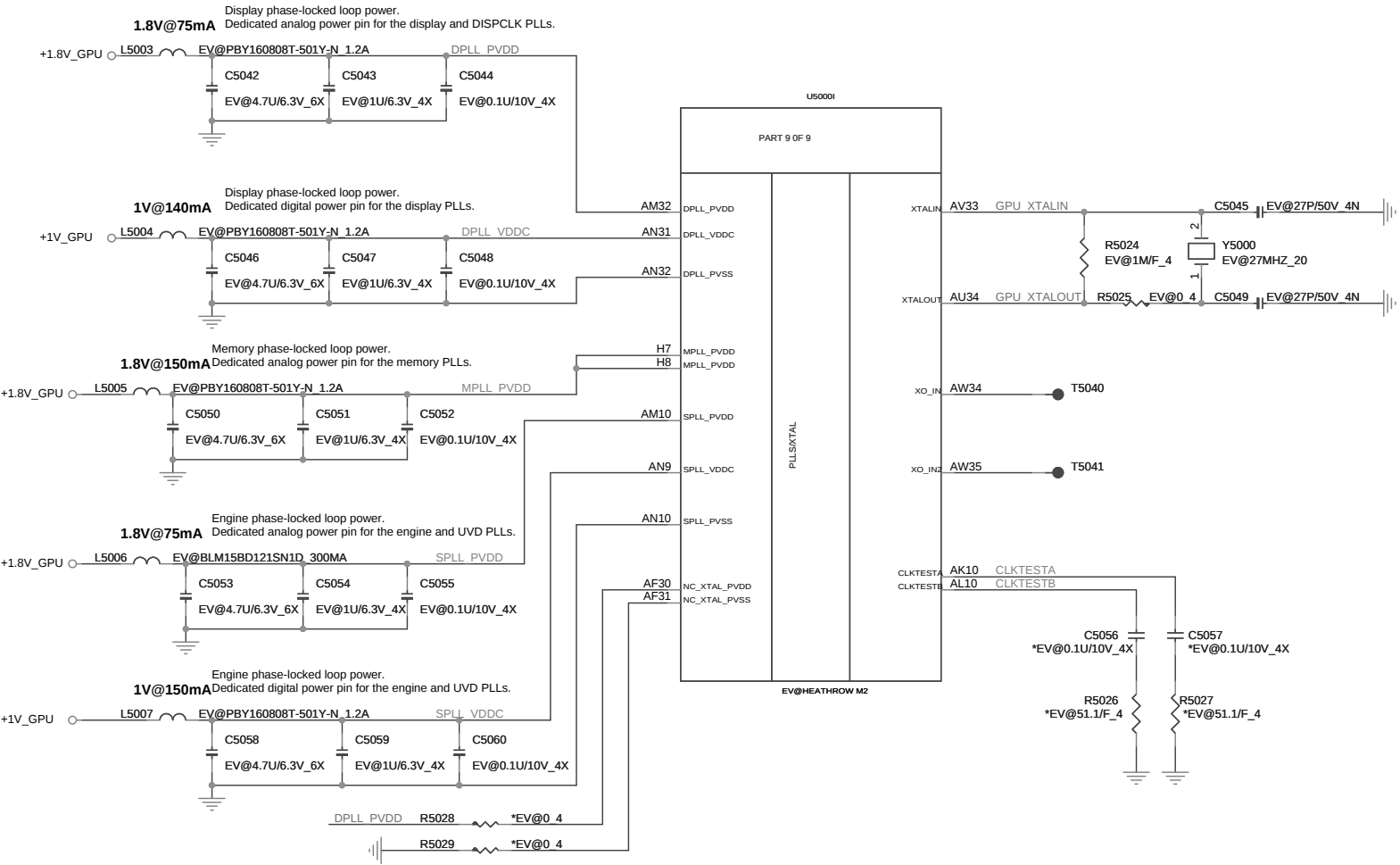


DDR_RVS(DDR)

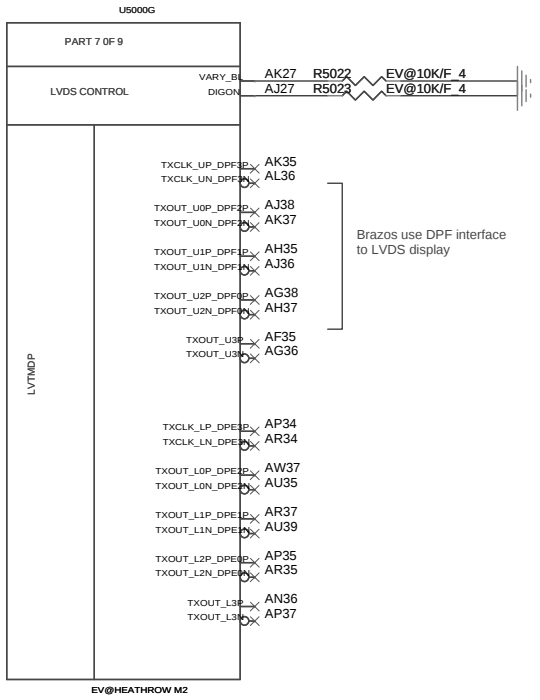








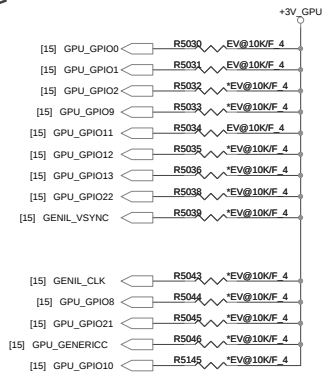
DPE/DPF/LVDS



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	Thames M2/ XTAL_LVDS	A1A
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<VGA>



DDR3 Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP4 DVPDATA_4	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63DFR-11C (64M*16)	AKD5LZWTW02 * 4	512MB	0	0	0	0	0
		AKD5LZWTW02 * 8	1GB	0	0	1	0	0
	H5TQ2G63BFR-11C (128M*16)	AKD5MGWTW00 * 4	1GB	0	1	0	0	0
		AKD5MGWTW00 * 8	2GB	0	1	1	0	0
	H5TQ4G***** (256M*16)	AK***** * 8	4GB	1	0	0	0	0
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 4	512MB	0	0	0	0	1
		AKD5EGGT500 * 8	1GB	0	0	1	0	1
	K4W2G1646C-HC11 (128M*16)	AKD5MGWT500 * 4	1GB	0	1	0	0	1
		AKD5MGWT500 * 8	2GB	0	1	1	0	1
	K4W4G***** (256M*16)	AK***** * 8	4GB	1	0	0	0	1
AMD	23EY2387MC11 (64M*16)	AKD5EZWT700 * 4	512MB	0	0	0	1	0
		AKD5EZWT700 * 8	1GB	0	0	1	1	0
	23EY4187MC11 (128M*16)	AKD5DZWT700 * 4	1GB	0	1	0	1	0
		AKD5DZWT700 * 8	2GB	0	1	1	1	0
	23EY***** (256M*16)	AK***** * 4	4GB	1	0	0	1	0

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CONFIGURATION STRAPS – SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

System Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1

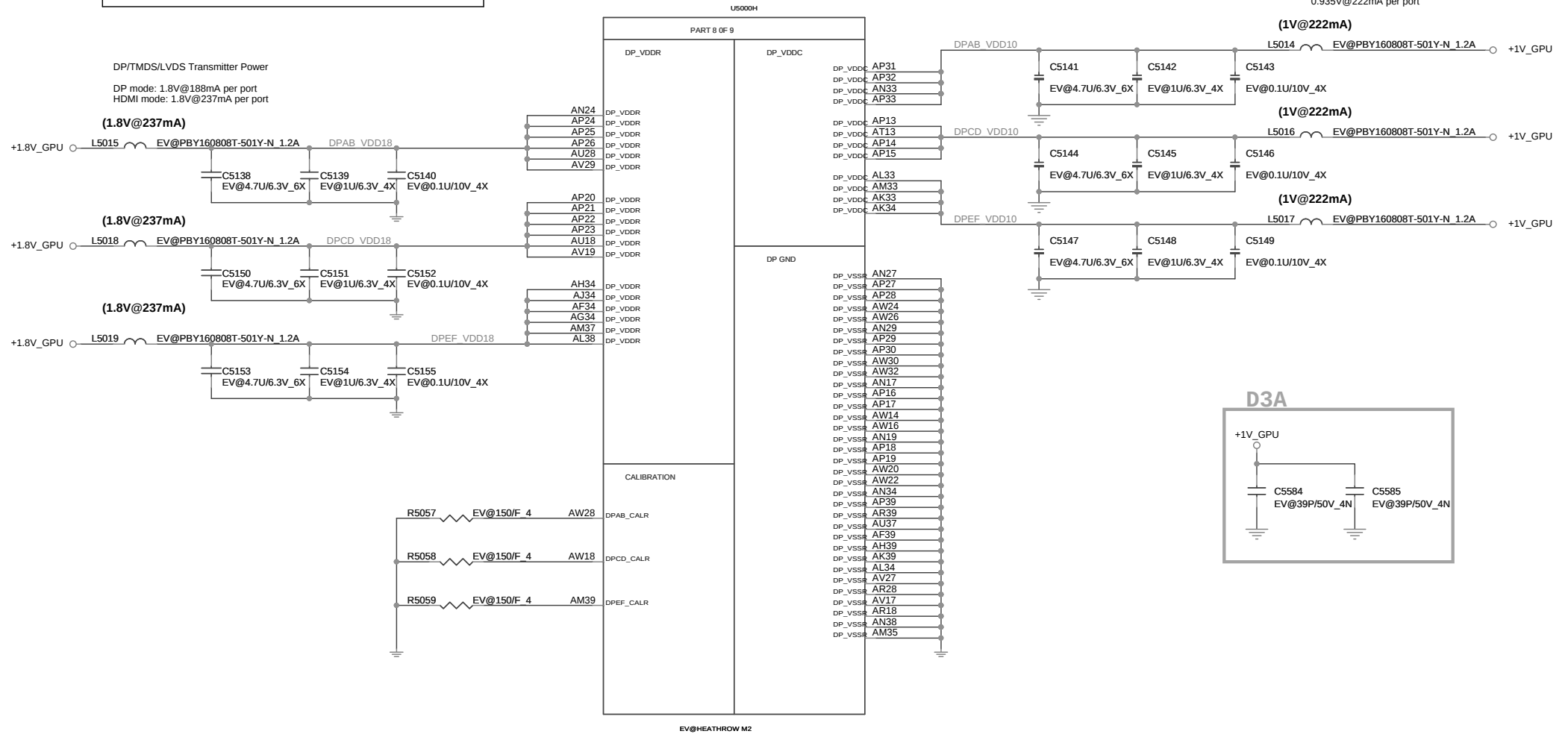
EEPROM

<VGA>

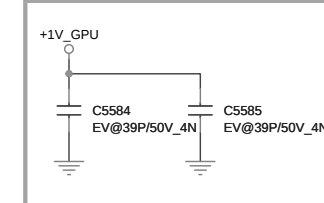
For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

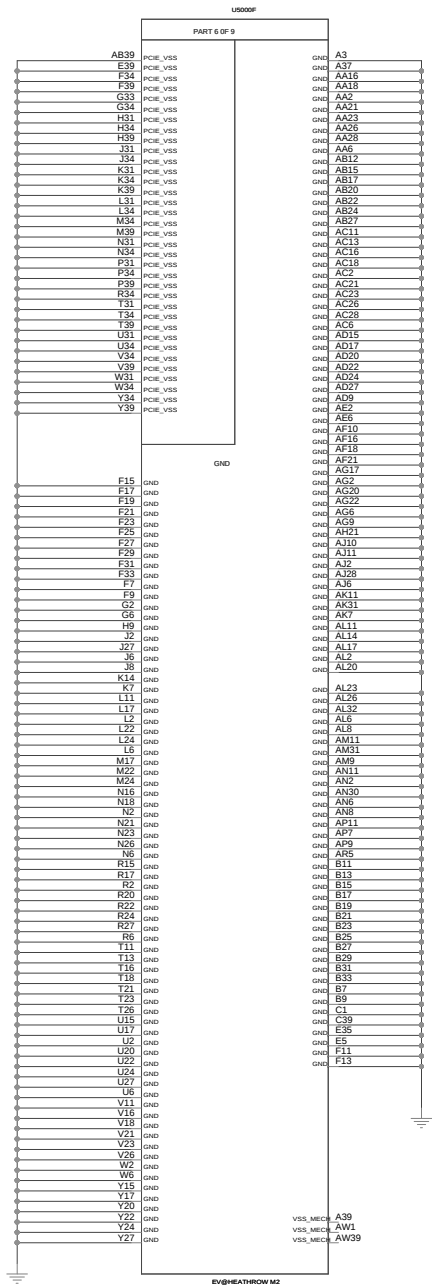


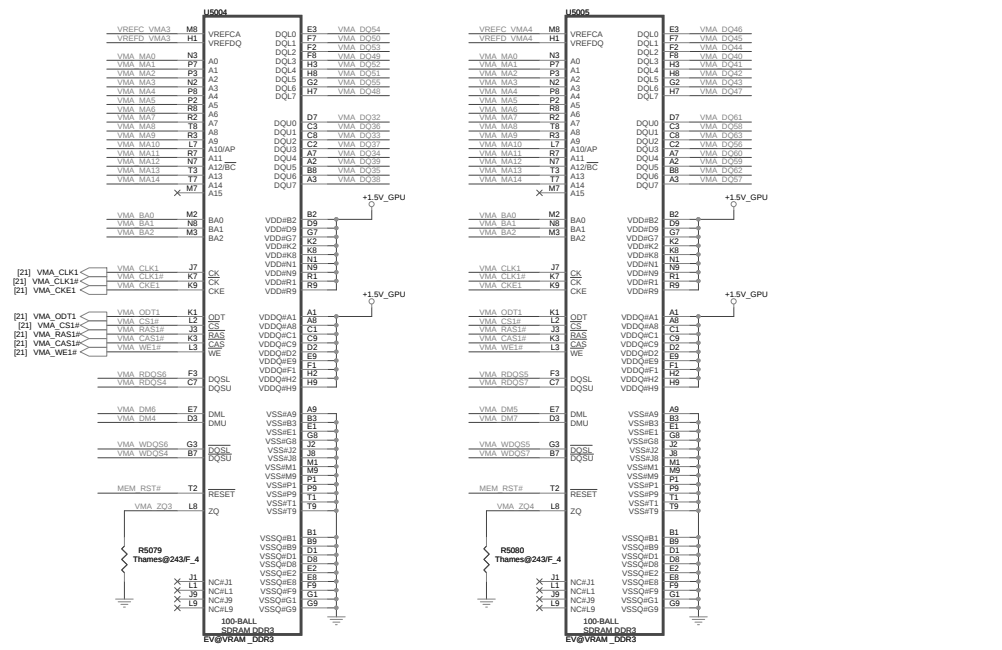
D3A



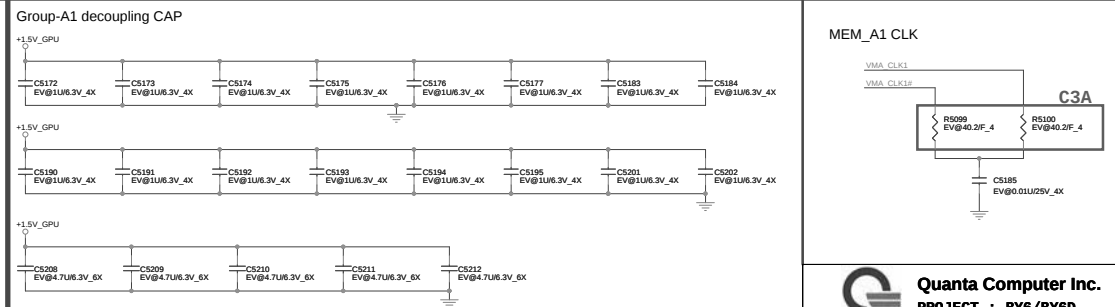
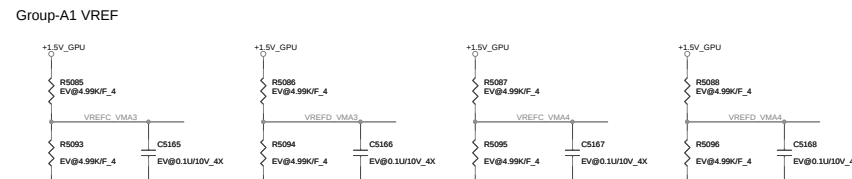
Quanta Computer Inc.
PROJECT : BY6/BY6D

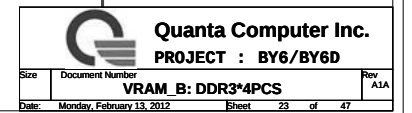
Size	Document Number	Rev
	Thames M2/ DP_Powers	A1A
Date:	Monday, February 13, 2012	Sheet 19 of 47

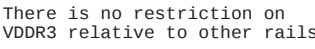




TOP Right

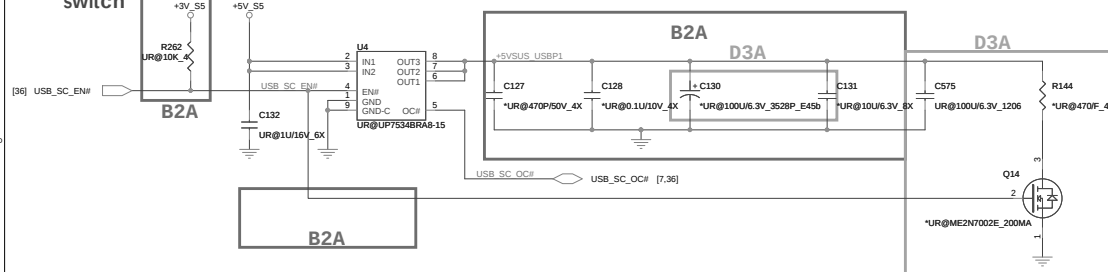




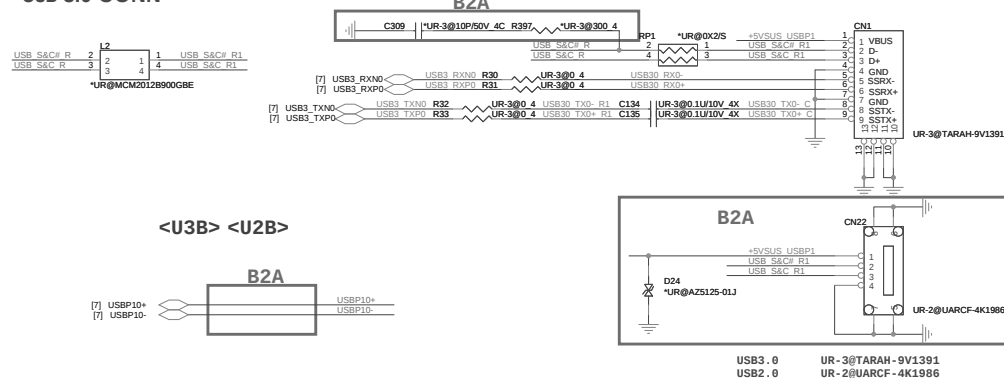


USB 3.0 Power switch

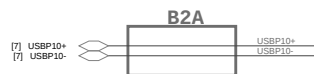
<USB> <U3B>



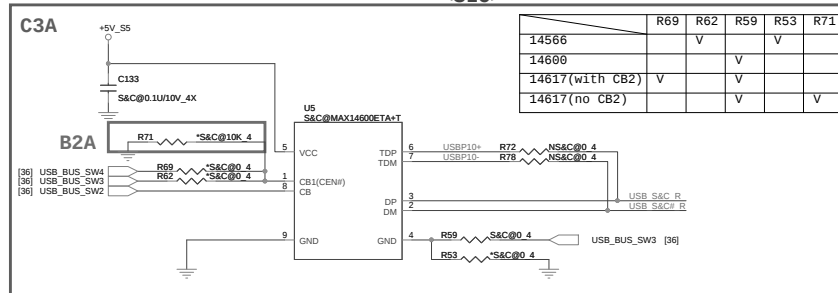
USB 3.0 CONN <U3B> <USB> <EMI>



<U3B> <U2B>

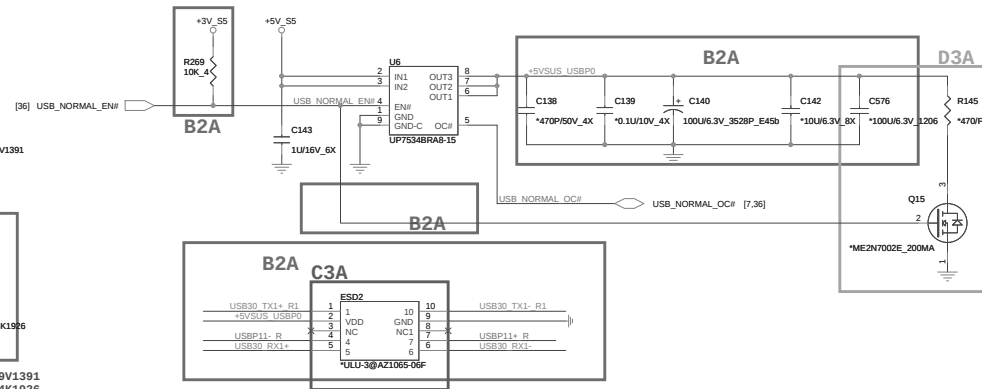
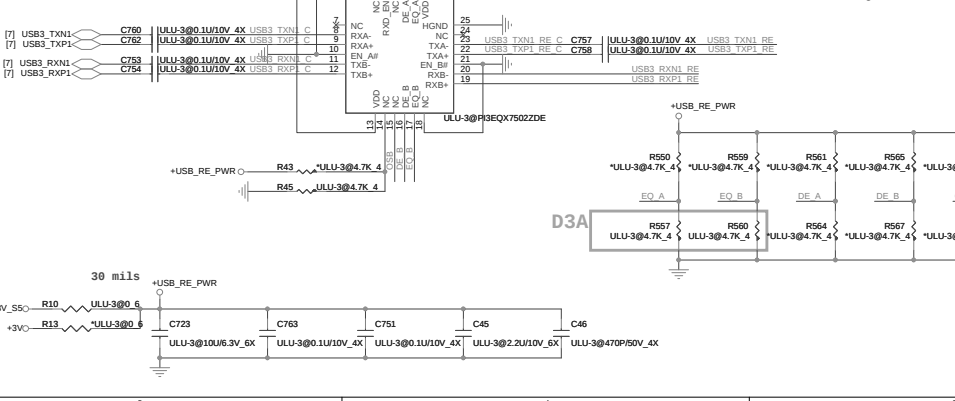
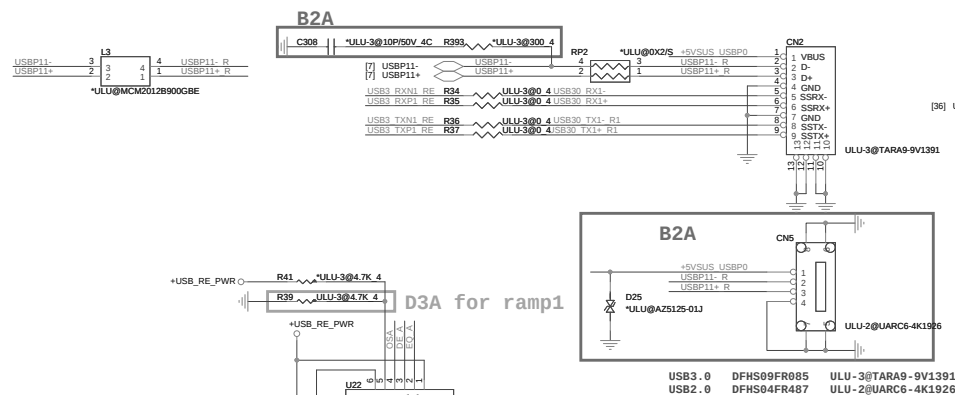


USB w S&C MAXIM solution<SLC>

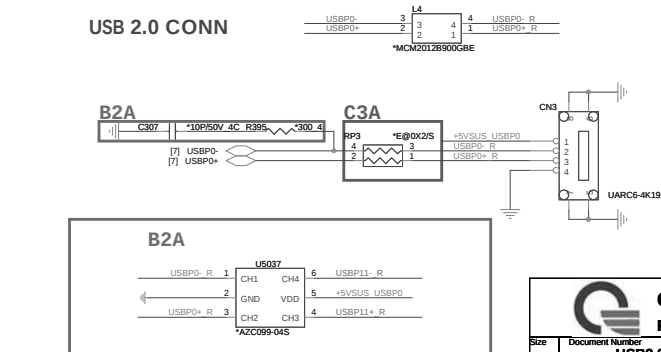


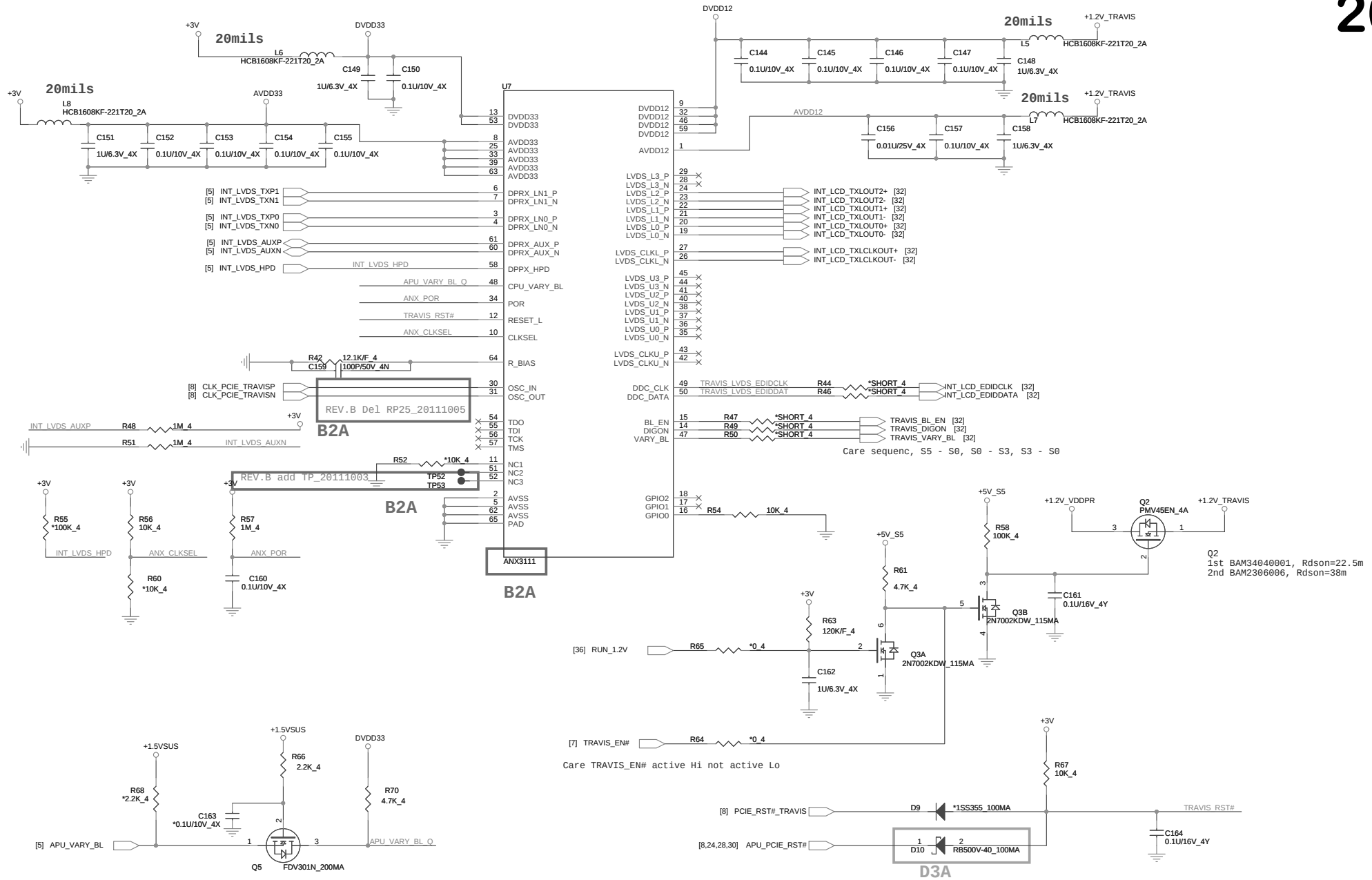
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

CB0	CB1	CB2	Status
X	X	1	Force Apple 2A Charger Mode
0	0	0	Autodetection charger mode
0	1	0	Force-Dedicated Charger Mode
1	0	0	USB Pass-Through Mode Connect DP/DM to TDP/TDM
1	1	0	USB Pass-Through Mode with CDP Emulation.Auto connect DP/DM to TDP/TDM depending on CDP status



USB 2.0 CONN



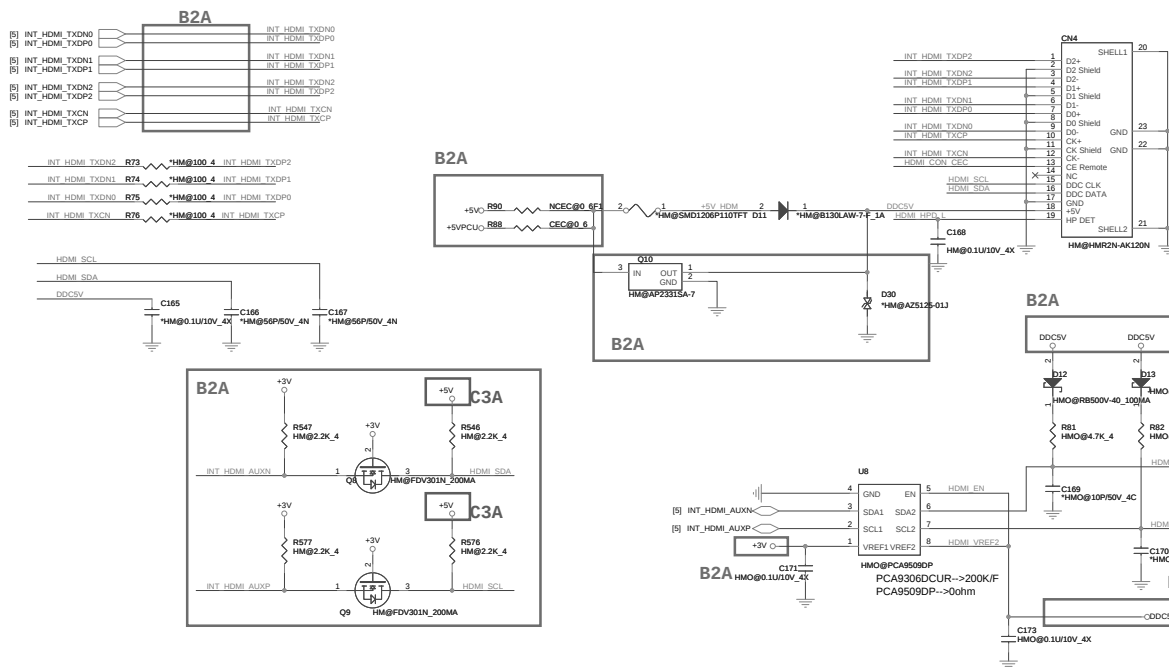


Quanta Computer Inc.
PROJECT : BY6/BY6D

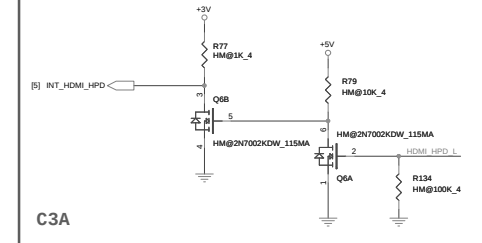
Size	Document Number	Rev
	TRAVIS ANX3110	1A

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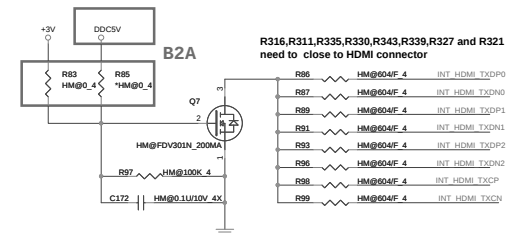
HDMI



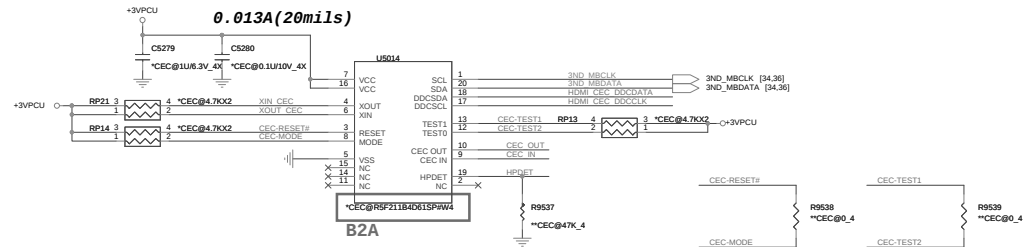
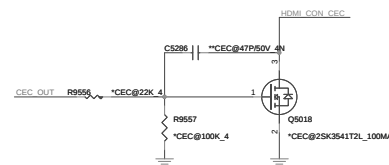
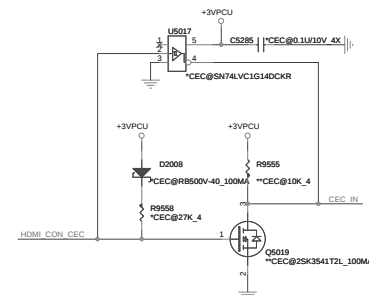
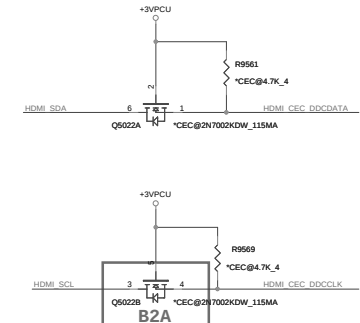
HDMI Hot-plug



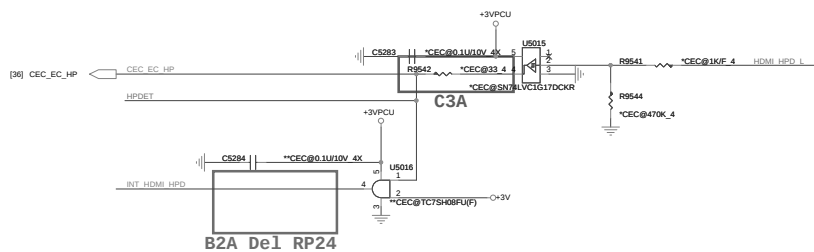
C3A

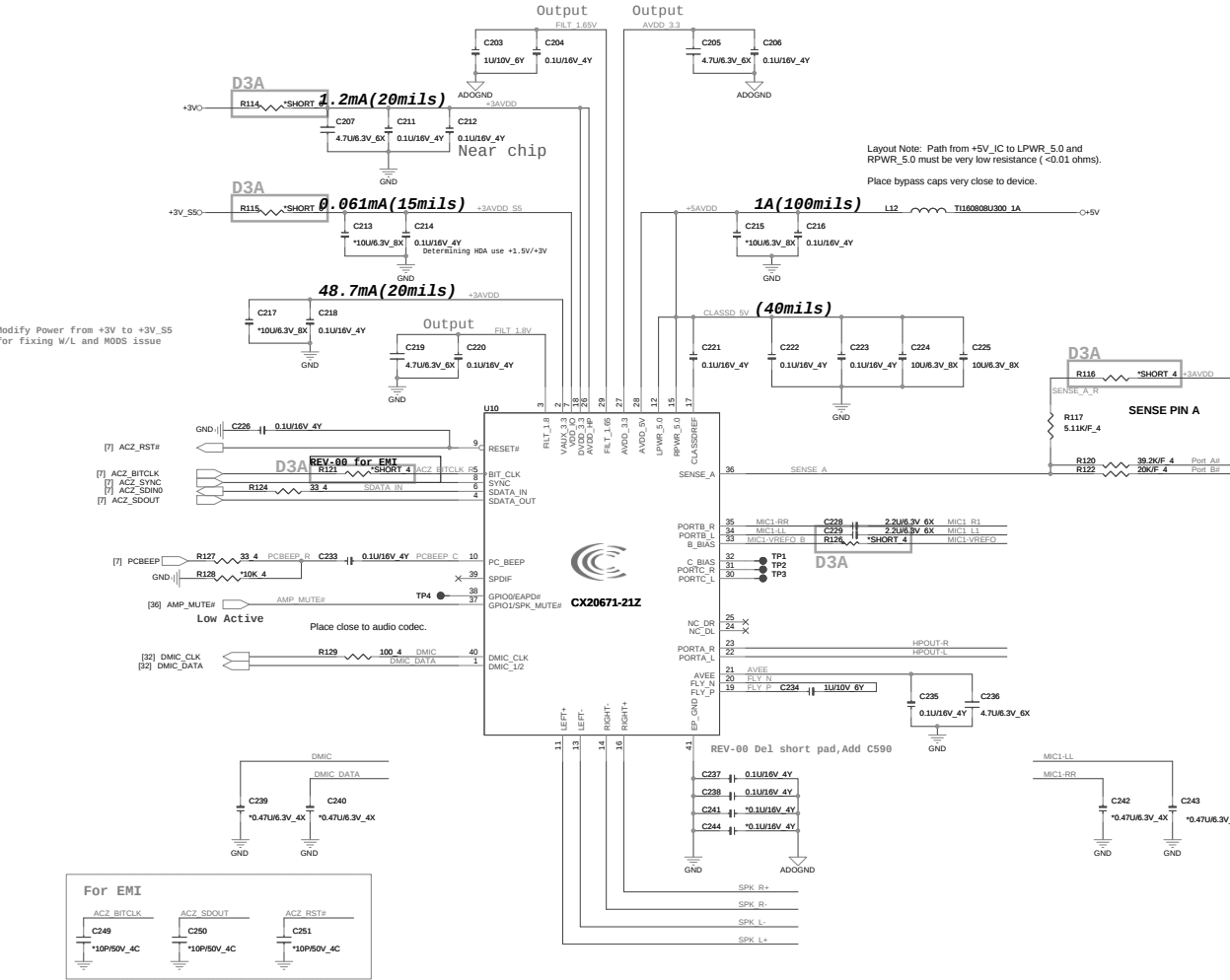


HDMI CEC <CEC>

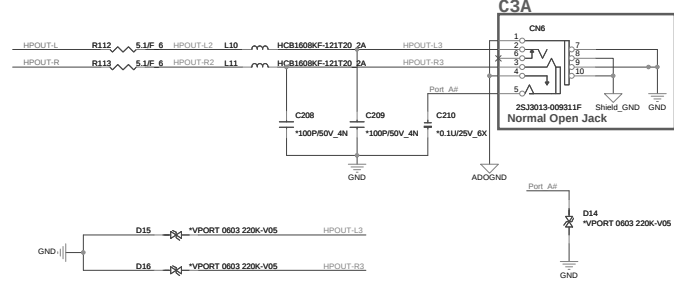
CEC Output <CEC>
(To Connect)CEC Input <CEC>
(To CECC)CEC SMBus Level
(To CECC) <CEC>

CEC HotPlug <CEC>

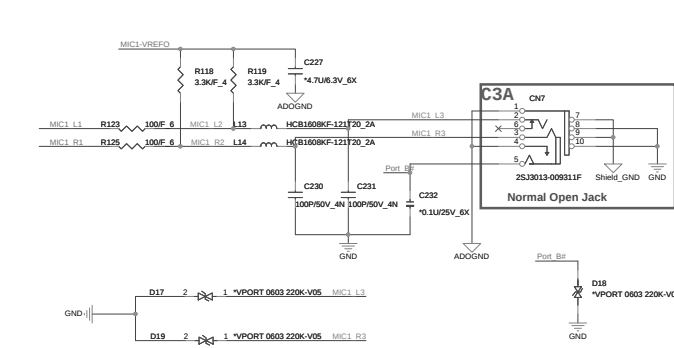




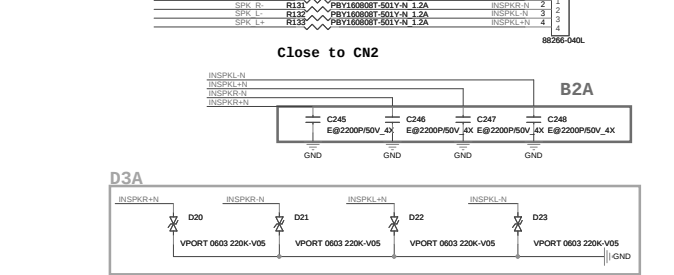
HP <ADO> <EMC>



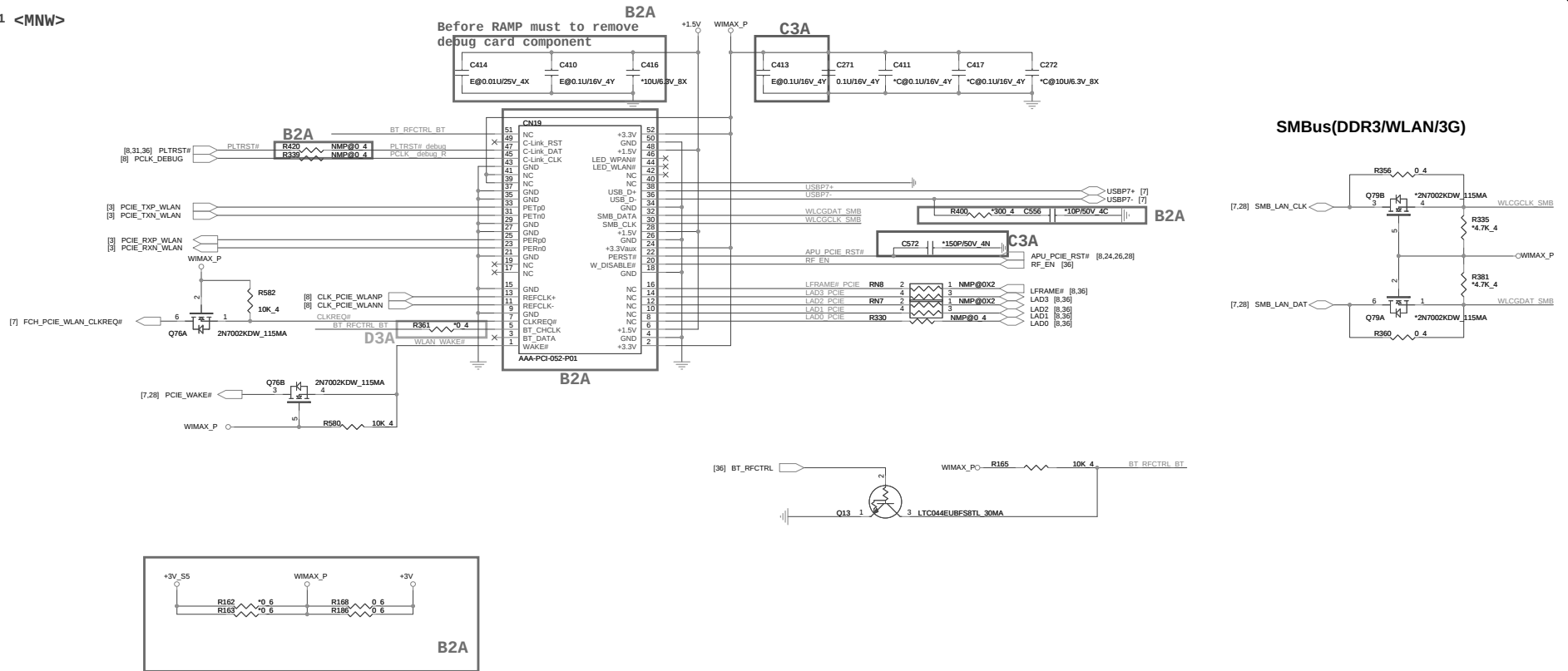
External MIC <ADO> <EMC>



Internal Speaker <ADO> <EMC>

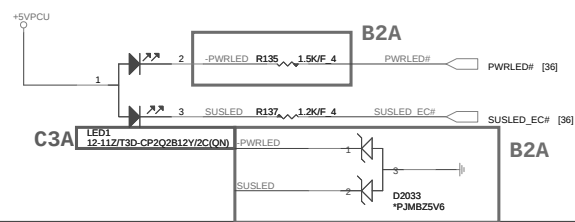


MINI Card Slot#1 <MNW>
(WiFi)



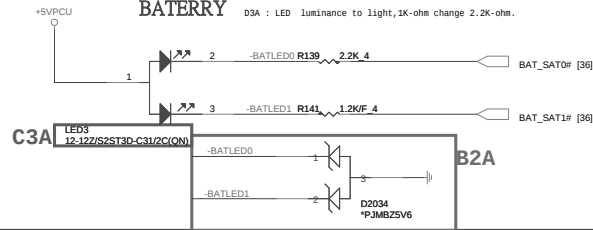
LED POWER

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

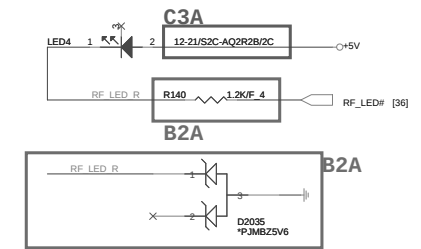


BATTERY

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

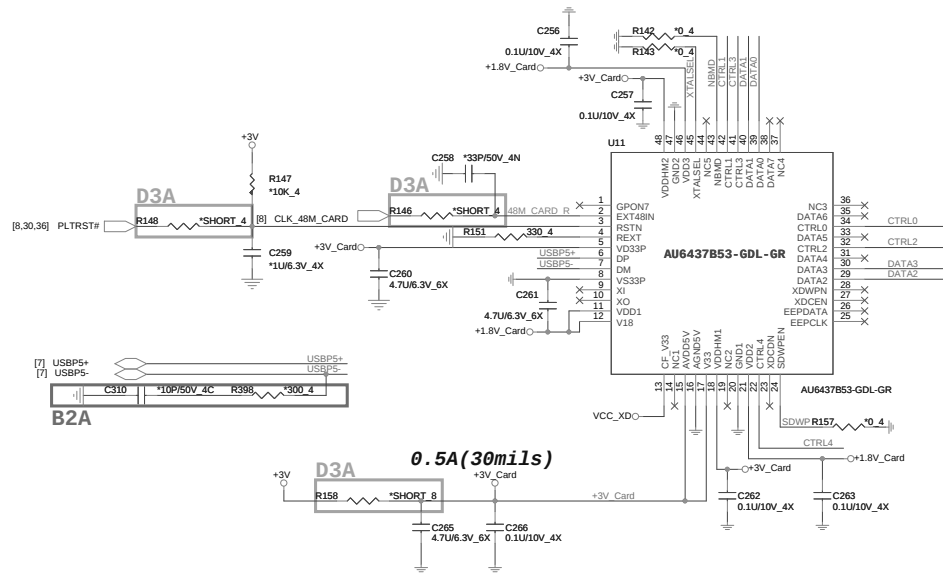


RF LED



3 IN 1 CARD READER (Type: MS/MMC/SD) <MMC>

Card Reader (AU6437B53-GDL-GR)



Clock input selection
1 : 48MHz input (default)
0 : 12MHz input

NBMD Power saving mode enable
1 : enable (default)
0 : disable

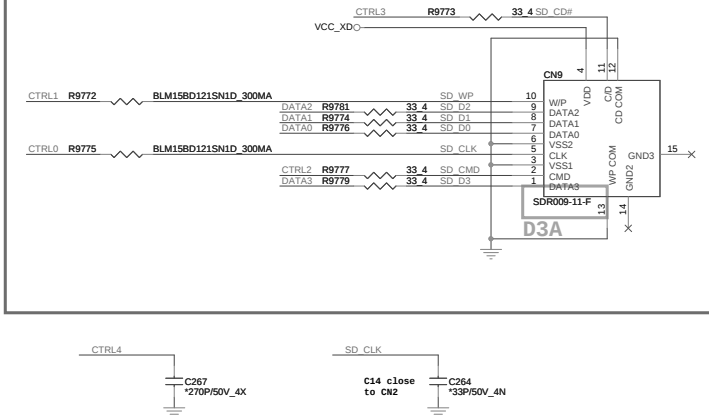
CTRL0 trace surround with GND

	SD	XD	MS
CTRL0	SDCLK	XDALE	MSBS
CTRL1	SDWP	XDCLE	MSCLK
CTRL2	SDCMD	XDRBD	
CTRL3	SDCDN	XDWRN	
CTRL4		XDRDN	MSINS

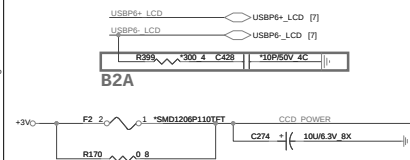
SD write protect enable
1 : decided by SDWP(default)
0 : SD always write-able

B2A

REV.B 20111023 change connector pin define

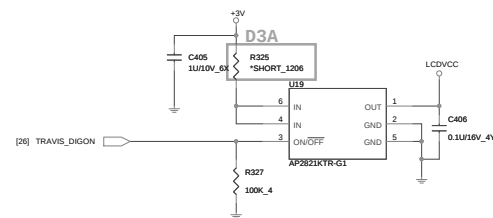


CCD [CCD]



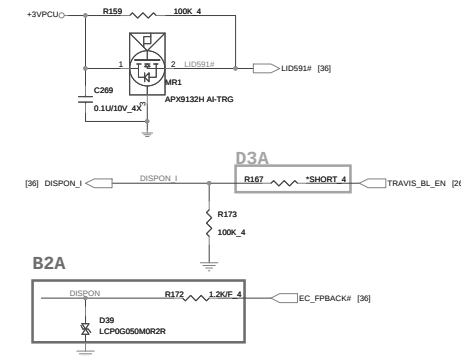
LCD POWER
SWITCH

<LDS>

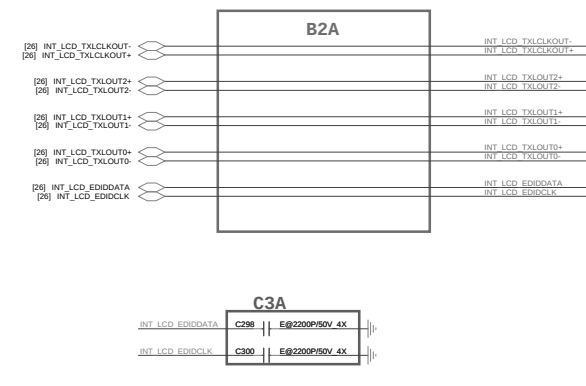
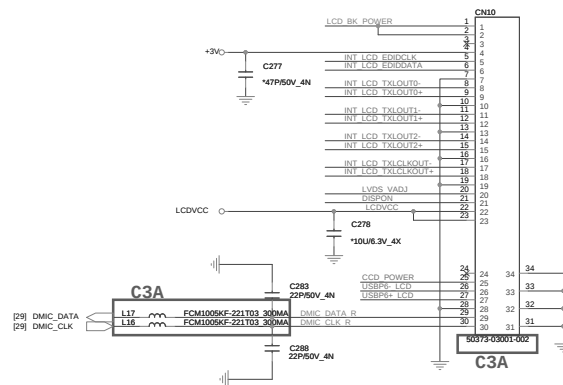
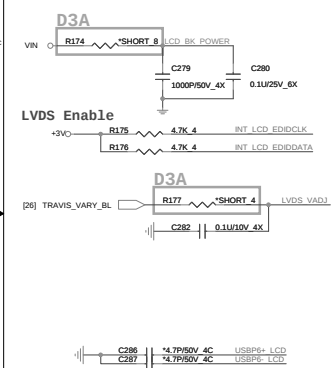


HALL SENSOR&BACK LIGHT
SWITCH

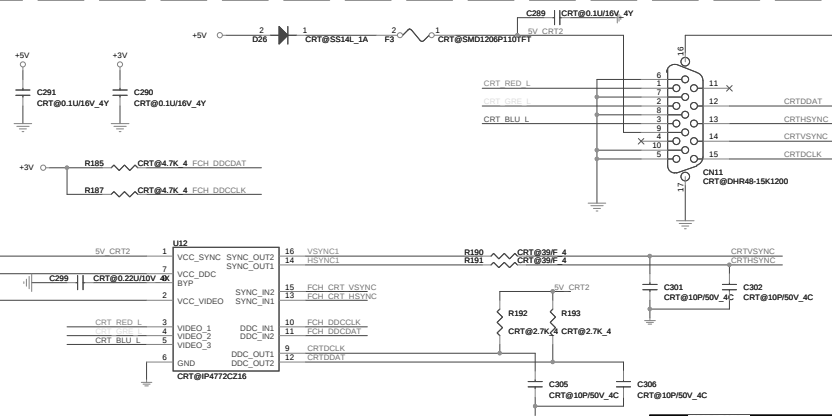
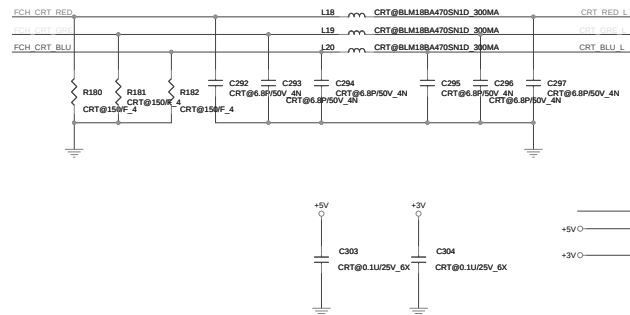
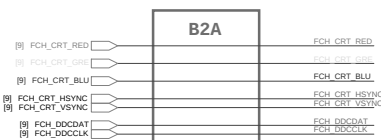
<HSR>



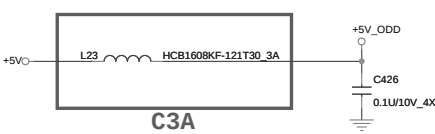
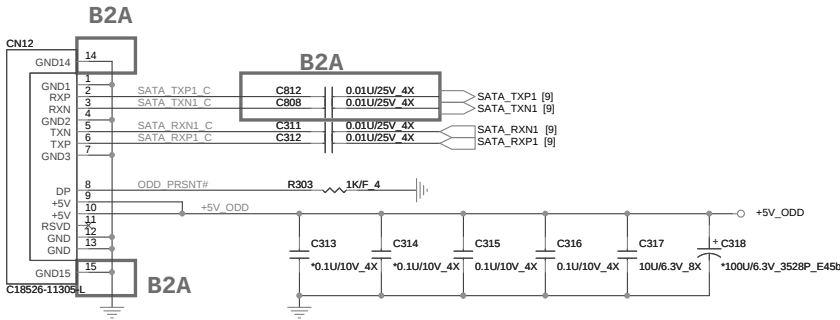
LCD Panel Module [LDS]



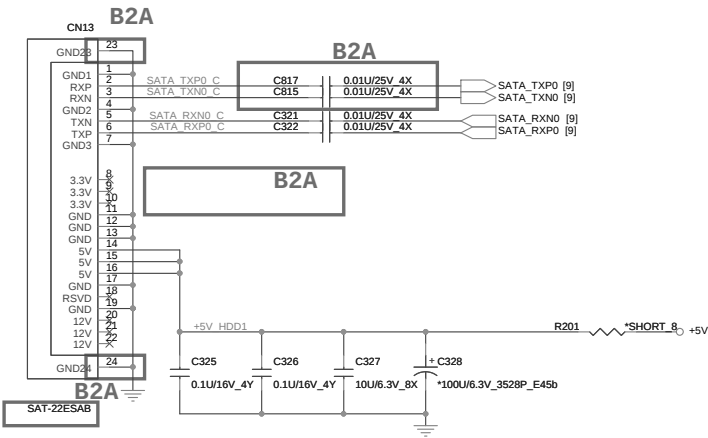
CRT [CRT]



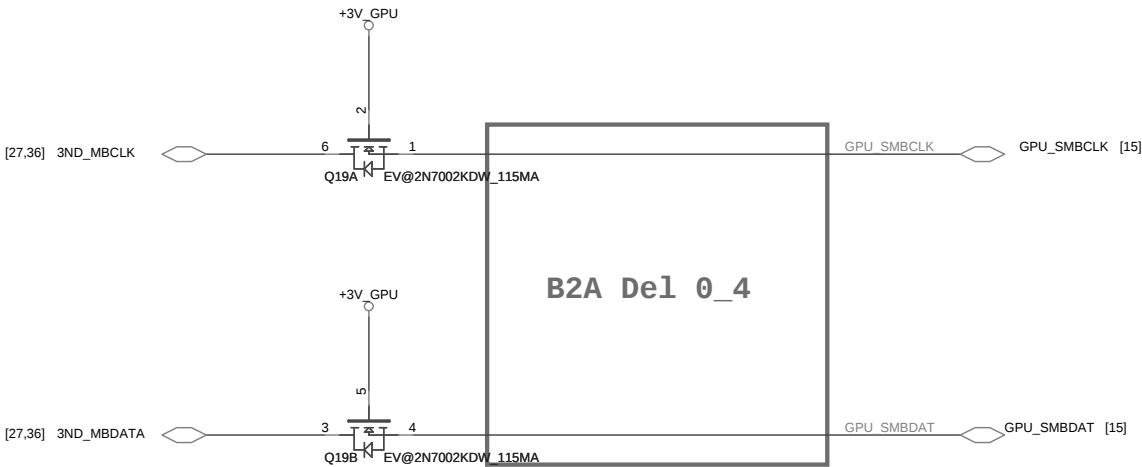
SATA ODD [ODD]



SATA HDD [HDD]

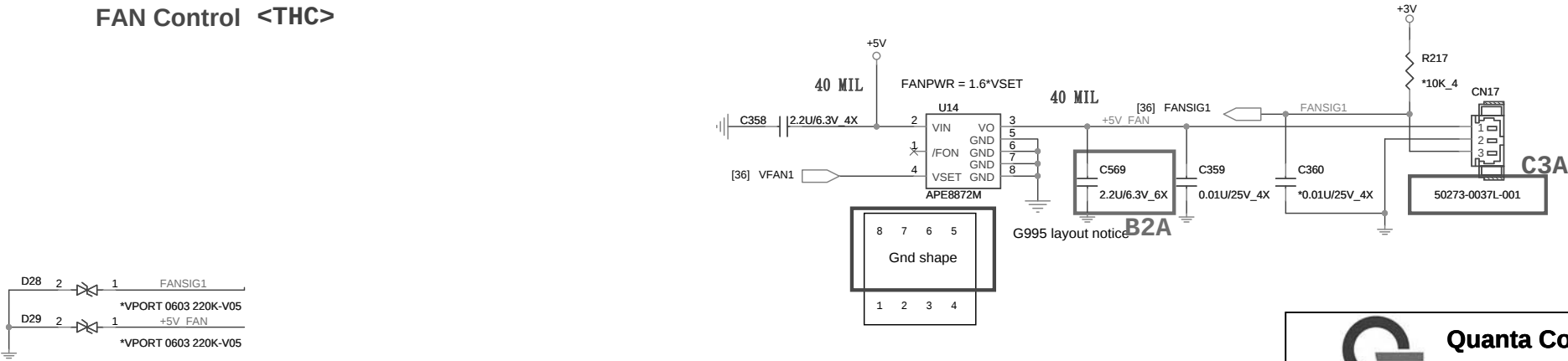


Thermal Sensor <THC>



Thermal	Ext Thermal	dGPU Int Thermal
EC(M) 3ND_SMB	U13	
EC(M) 3ND_SMB		dGPU int SMBUS
dGPU(M) SMB	U13	dGPU int SMBUS

FAN Control <THC>



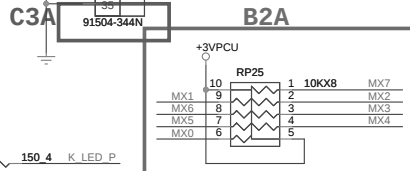
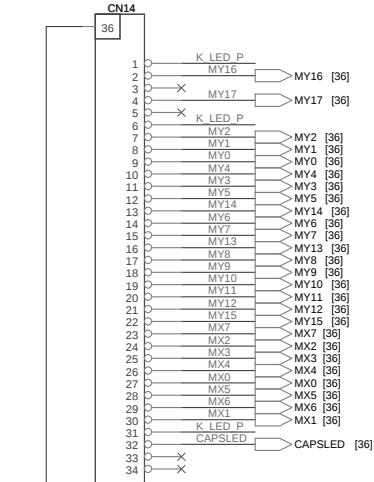
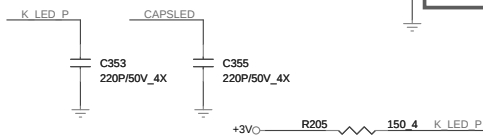
KEY BOARD Connector <KBC> <EMI>

INT KeyBoard

D3A

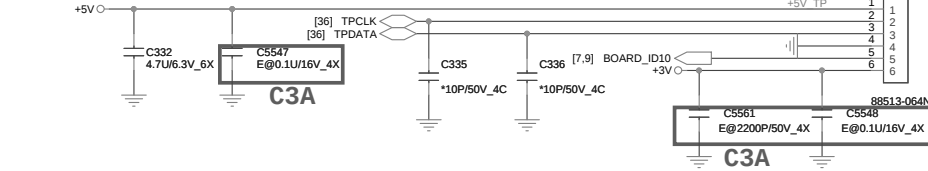
C329	ESD@39P/50V_4N	MX7
C330	ESD@39P/50V_4N	MX2
C331	ESD@39P/50V_4N	MX3
C333	ESD@39P/50V_4N	MX4
C337	ESD@39P/50V_4N	MX0
C338	ESD@39P/50V_4N	MX5
C339	ESD@39P/50V_4N	MX6
C340	ESD@39P/50V_4N	MX1
C341	ESD@39P/50V_4N	MY7
C342	ESD@39P/50V_4N	MY13
C343	ESD@39P/50V_4N	MY12
C344	ESD@39P/50V_4N	MY15
C345	ESD@39P/50V_4N	MY3
C346	ESD@39P/50V_4N	MY5
C347	ESD@39P/50V_4N	MY14
C348	ESD@39P/50V_4N	MY6
C349	ESD@39P/50V_4N	MY2
C350	ESD@39P/50V_4N	MY1
C351	ESD@39P/50V_4N	MY0
C352	ESD@39P/50V_4N	MY4
C357	ESD@39P/50V_4N	MY16
C373	ESD@39P/50V_4N	MY17

ESD Issue



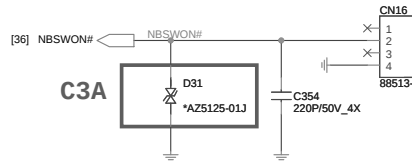
TOUCH PAD BOARD <TPD> <EMI>

35

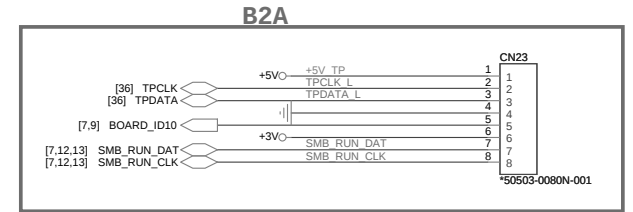


ID_Detect	default
Metal/IMR	H
TEXTURE	L

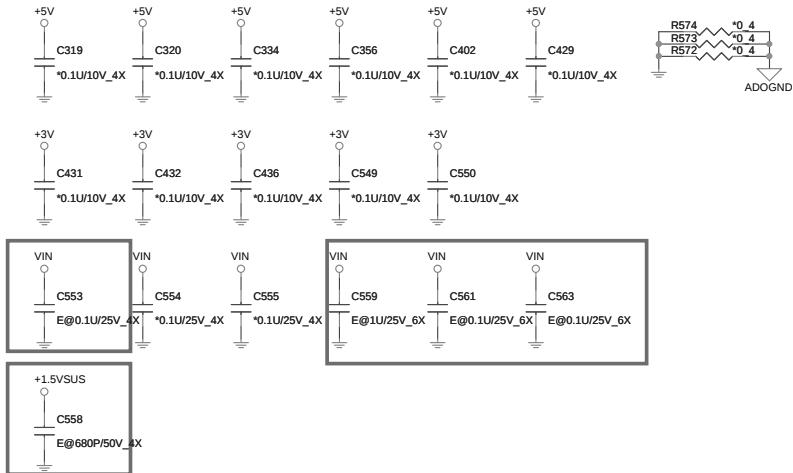
Power Board (UIF) <PSW>



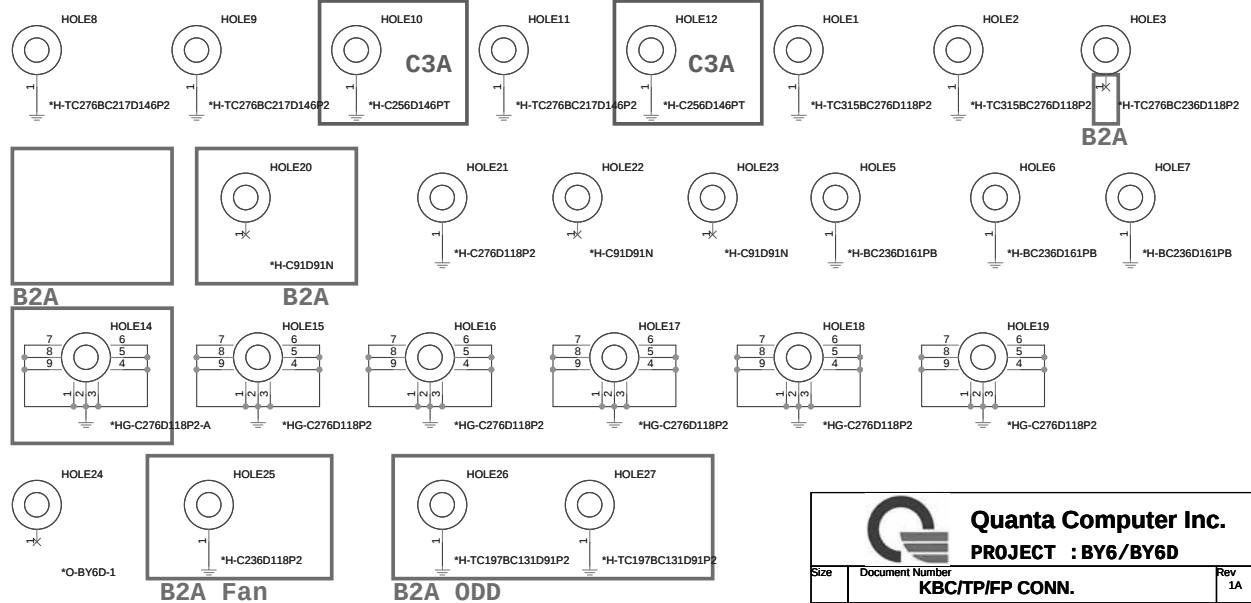
TP board <TPD>



EMI PAD <EMI>



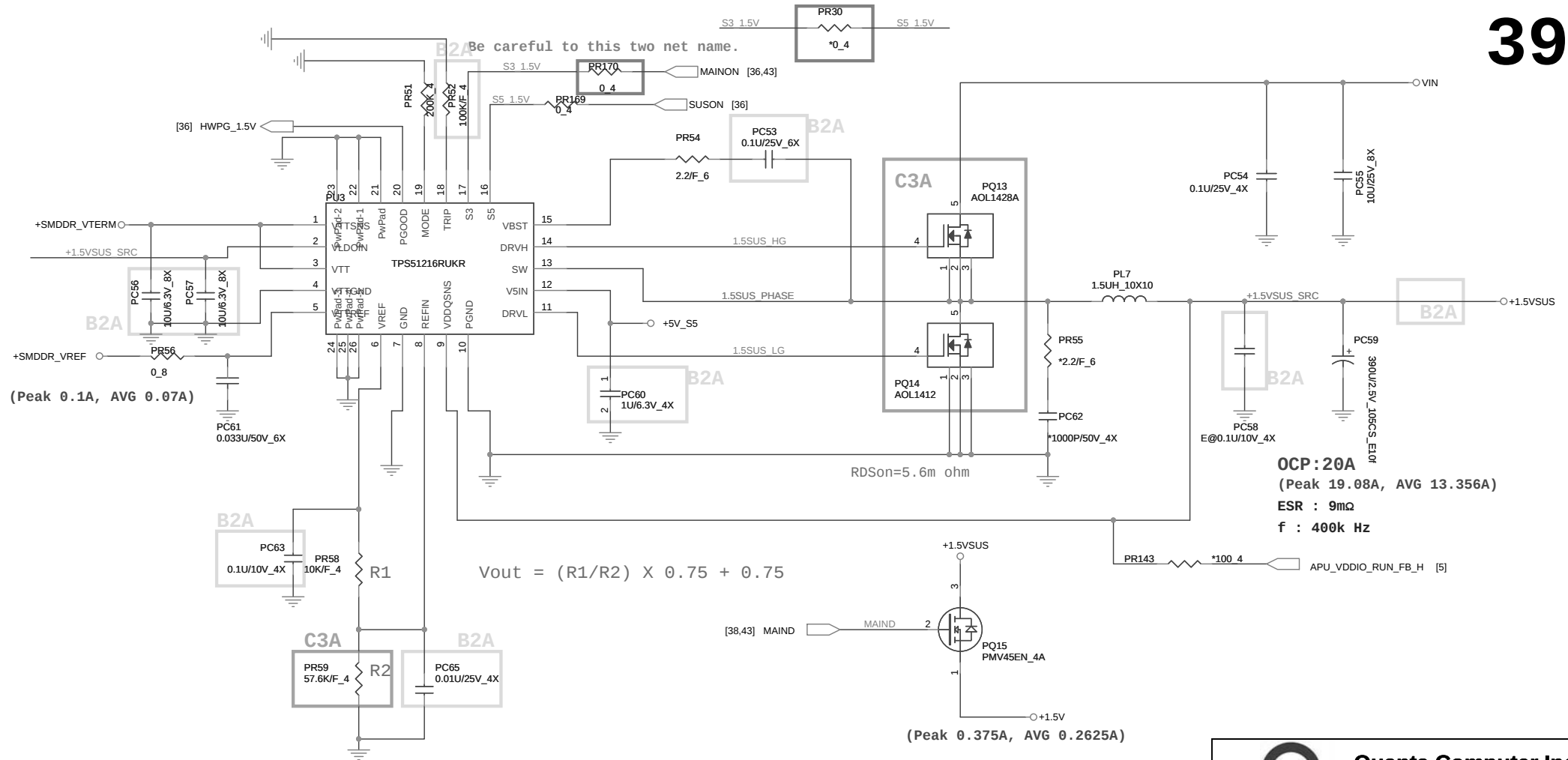
HOLE <OTH>



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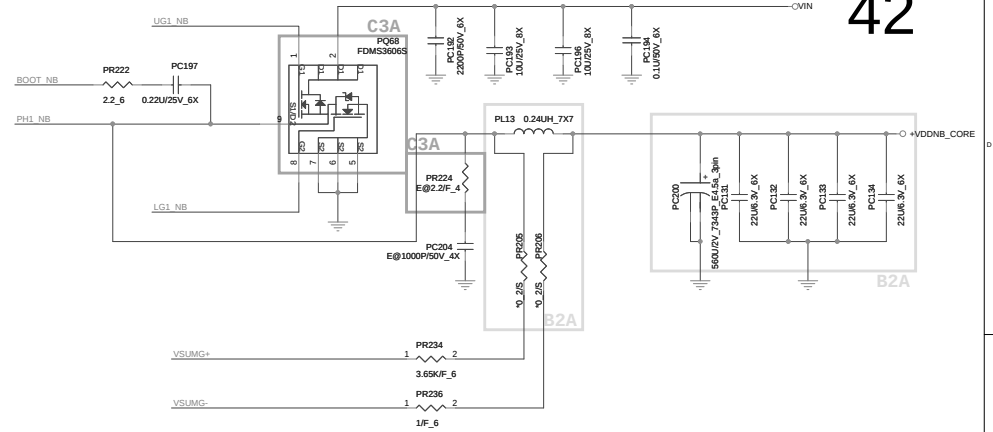


Quanta Computer Inc.
PROJECT : BY6/BY6D

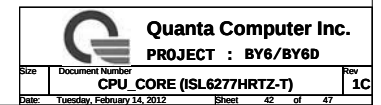
Size	Document Number	Rev
	+1.5VSUS (TPS51216RUKR)	1A
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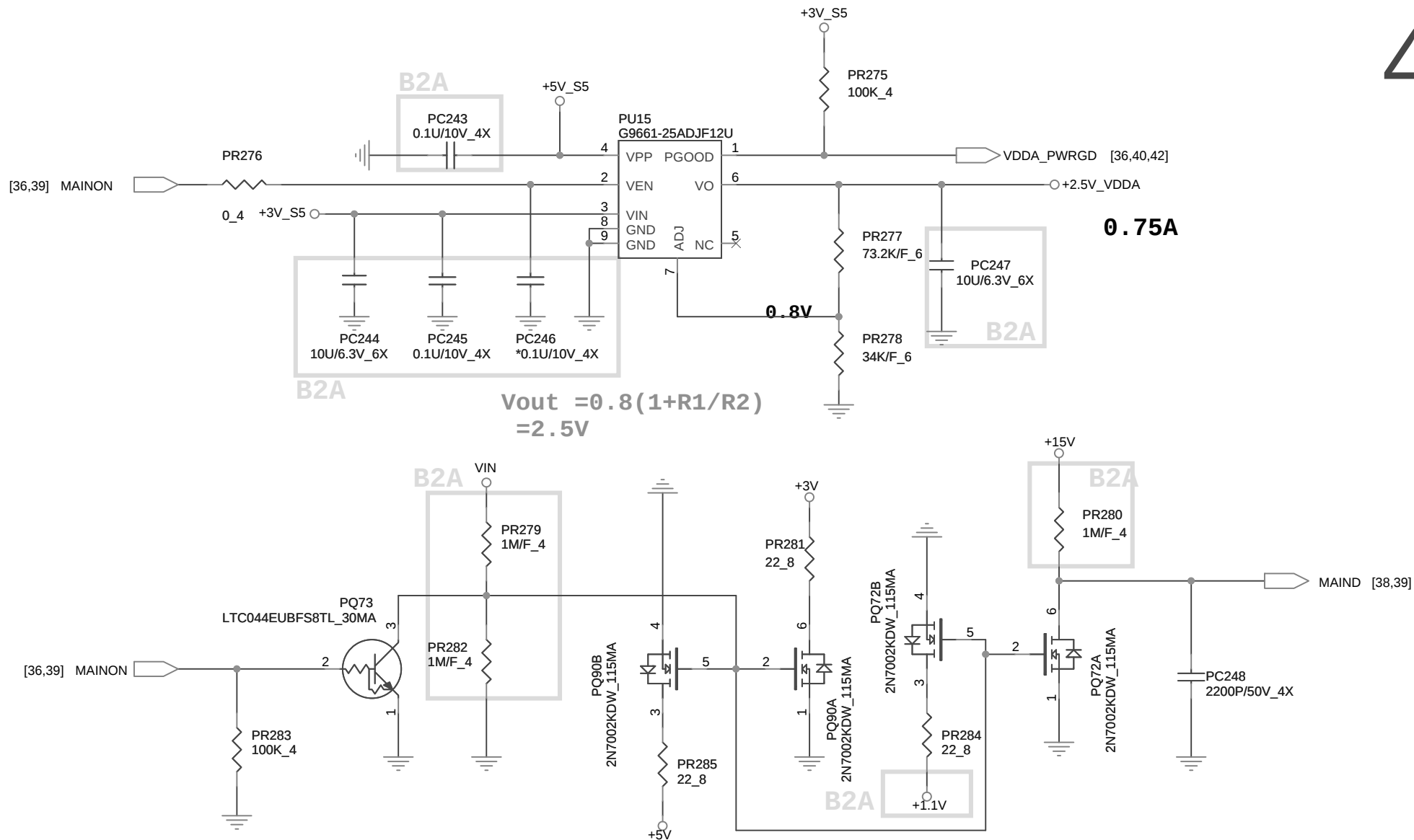






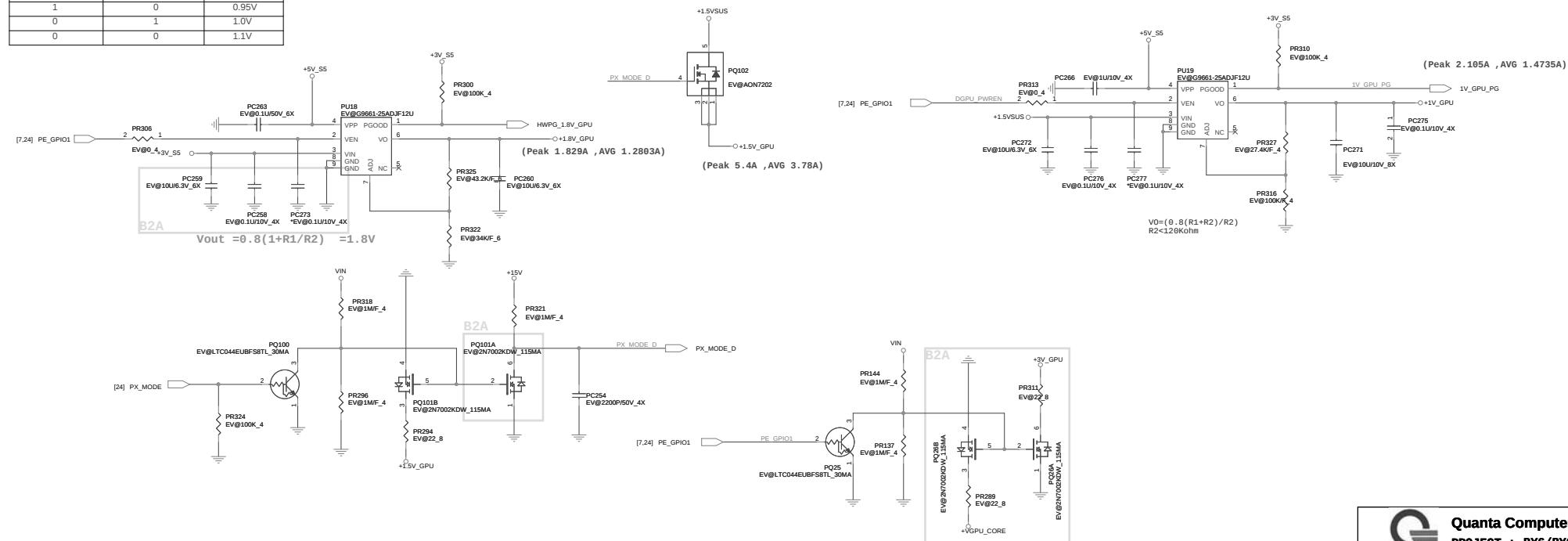
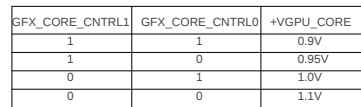
VDD_CORE



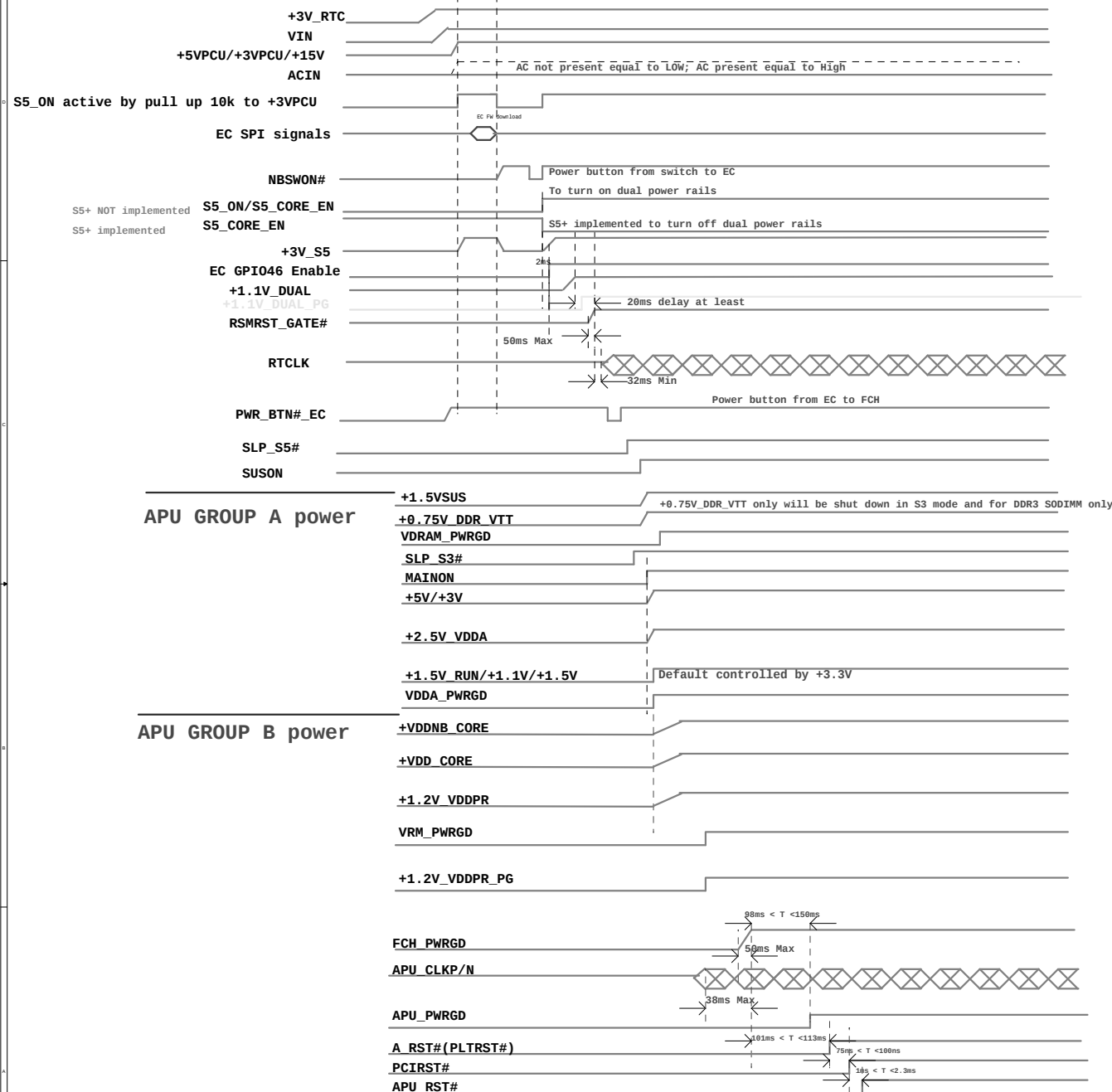


Quanta Computer Inc.
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BY6/BY6D Power On Sequence: S5 > S0



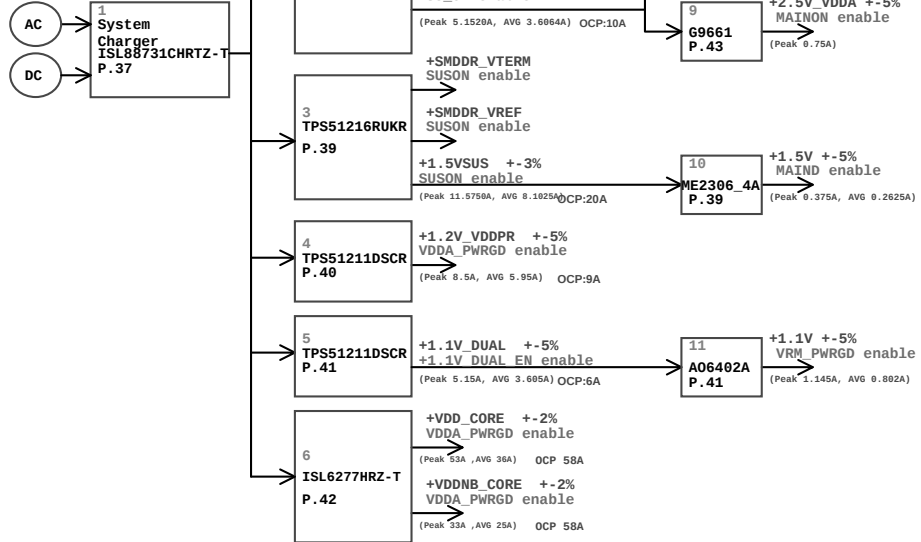
APU Power on sequence required:

Llano APU:

1. Group A (+1.5VSUS, +2.5V_VDDA) ramp before Group B
 (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M2/M3:

1. +3V_S5 ramp before +1.1V_DUAL
 2. +3V ramp before +1.1V
 3. +3V_RTC must ramp at least 5 secs before the +3V_S5



Power Distribution List

Power	Distribution

