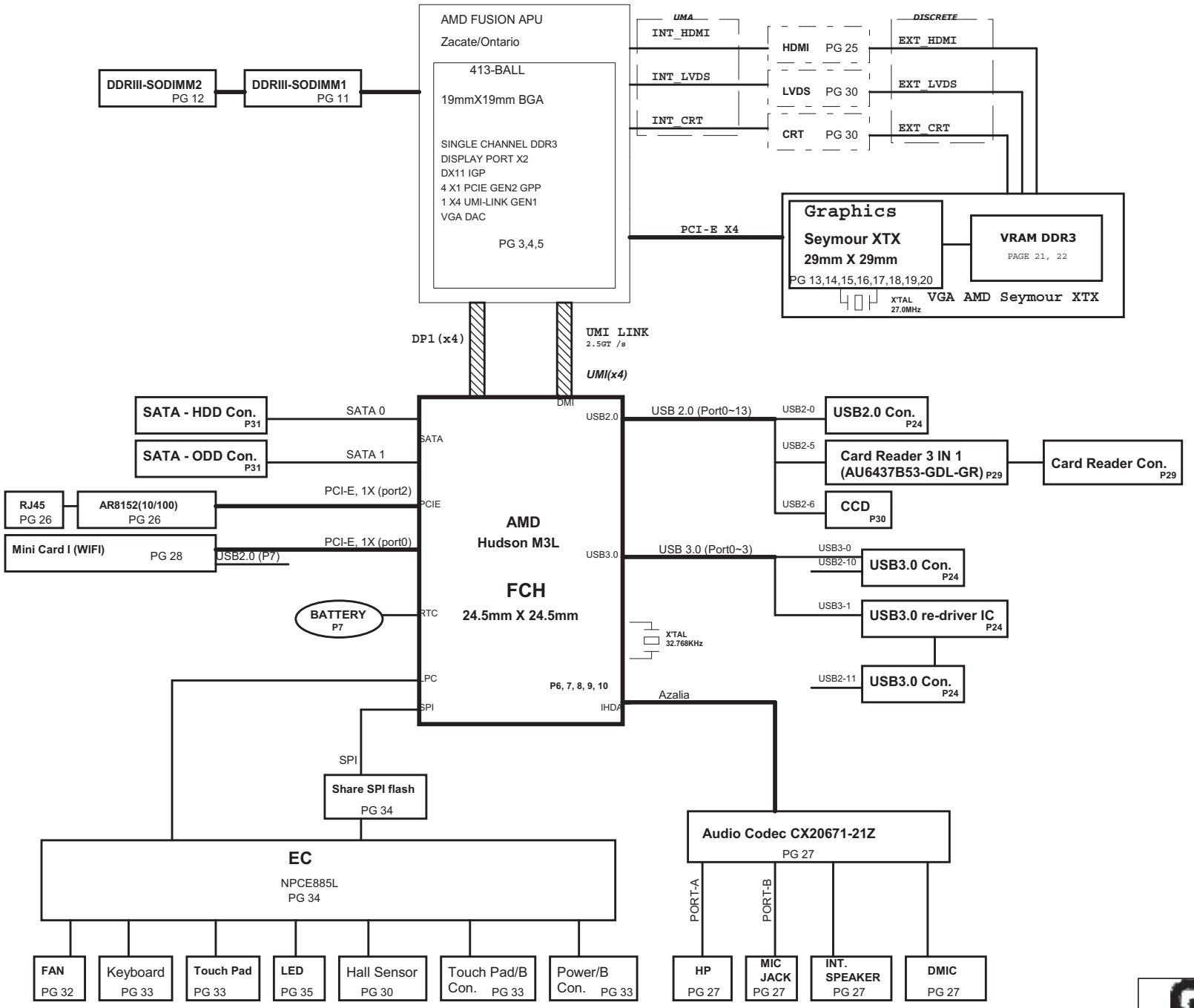
14" BY7D Brazos 2.0 Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



POWER SYSTEM

ISL88731CHRTZ-T	P36
RT8223P	P37
TPS51216RUKR	P38
TPS51211DSCR	P39
TPS51211DSCR	P40
TPS51211DSCR	P40
OZ8380ALN	P41
ISL95870AHRUZ	P42

CHARGER P36

+15V P37
+3VPCU
+3V_S5
+3V
+3V_GPU
+5VPCU
+5V_S5
+5V
DISCHARGE

+SMDDR_VTERM P38
+SMDDR_VREF
+1.5VSUS
+1.5V
+1.5V_GPU

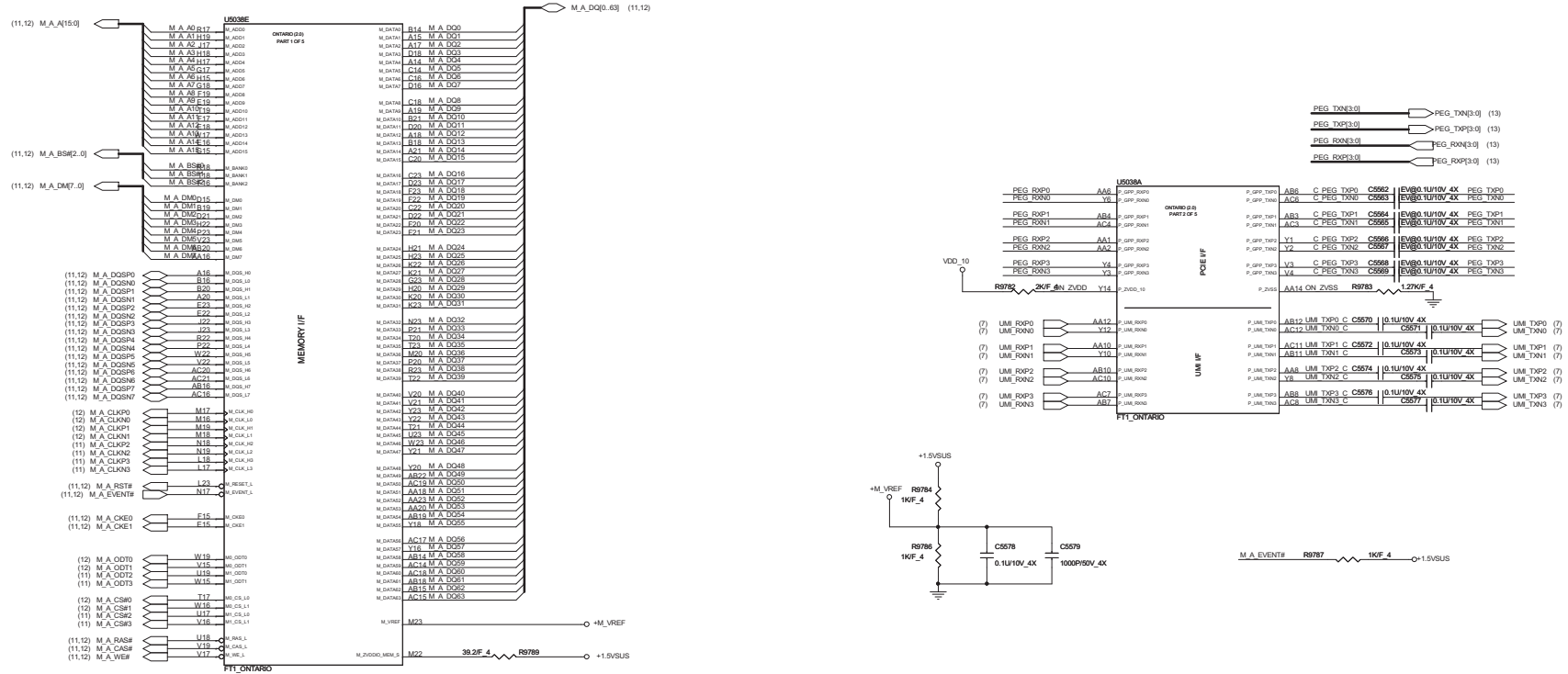
+1.0V P39
+1.0V_GPU

+1.1V_S5 P40
+1.1V
+1.8V
+1.8V_GPU

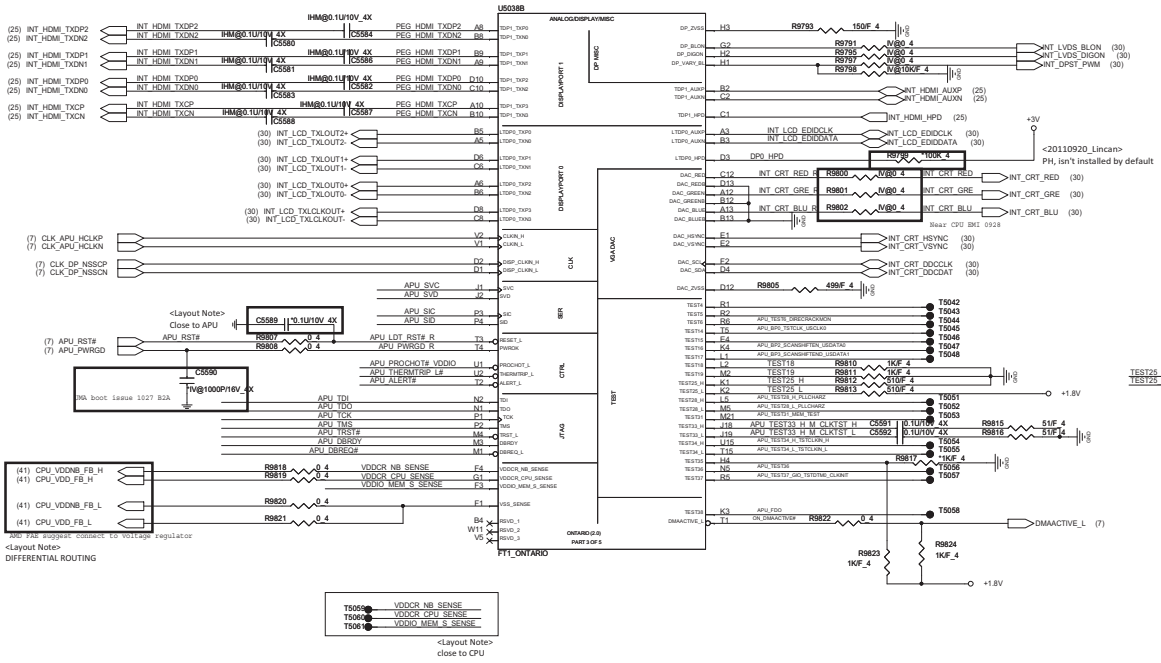
CPU_CORE P41
CPU_VDDNB_CORE

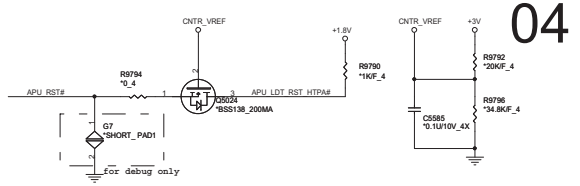
+VGPU_CORE P42

Quanta Computer Inc.
PROJECT : BY7D
Size | Document Number: Block Diagram | Rev: 1A
Date: Monday, March 12, 2012 | Sheet 1 of 45

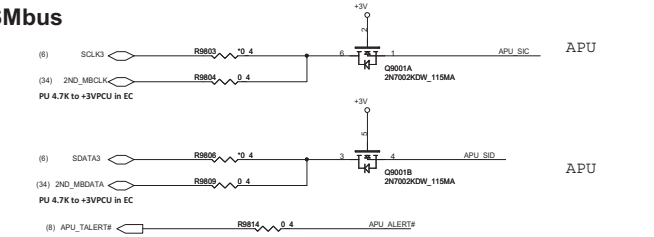


Quanta Computer Inc.			
PROJECT : BY7D			
Size	Document Number		Rev
	ONTARIO MEM & PCIE I/F(1/3)		1A
Date: Wednesday, March 21, 2012		Sheet 3 of 45	

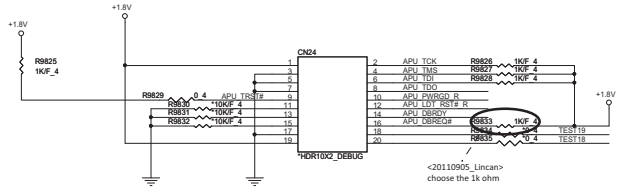




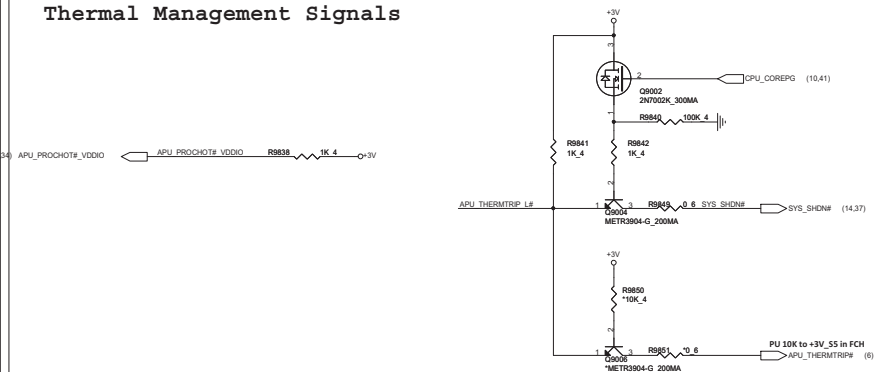
SMbus



HDT(Hardware Debug Tool) Connector



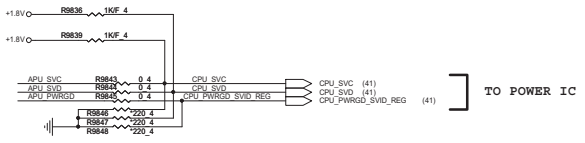
Thermal Management Signals



Serial VID

SI Change from AMD request

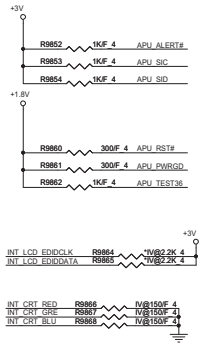
PV stage:add +1.5VSUS option
R540 R541 for Caspian CPU
power leakge issue



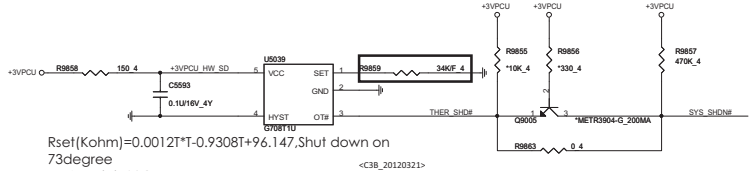
To indicate SVI interface is active

VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



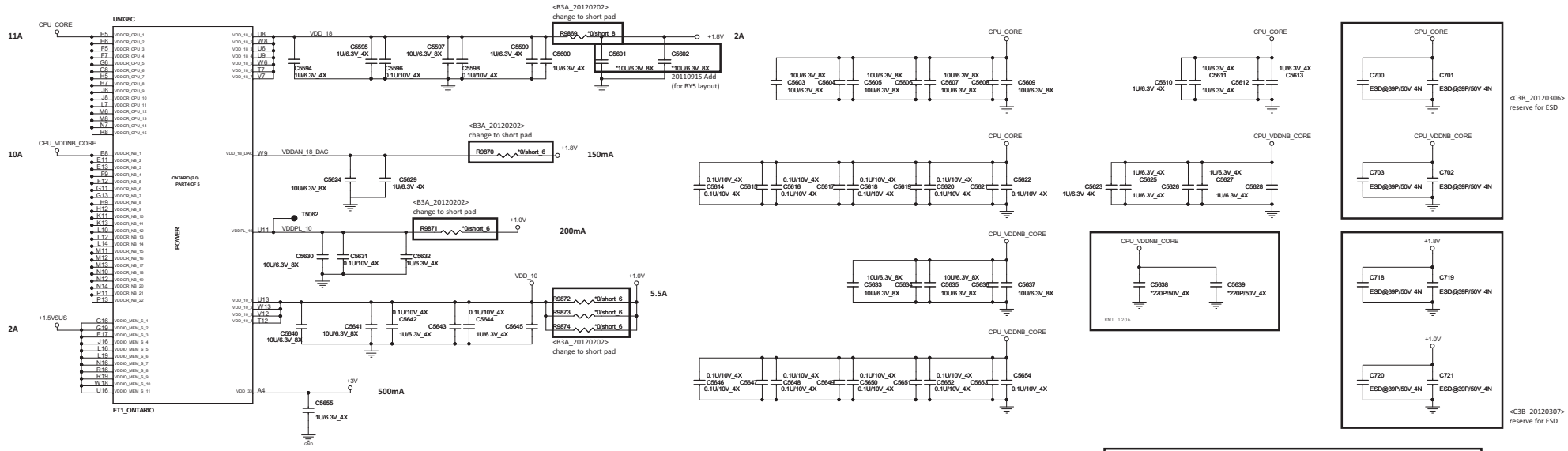
CPU Thermal sensor HW control (near CPU)

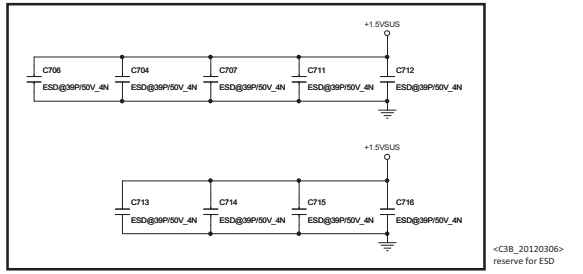


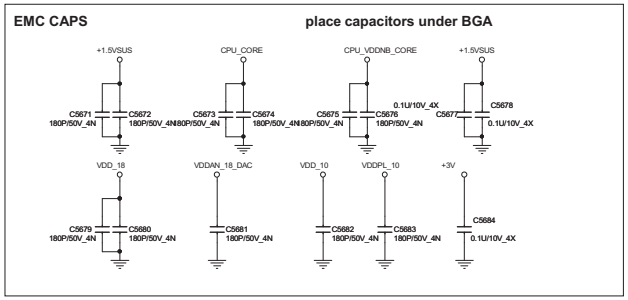
Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 73degree
Hysteresis is 30C

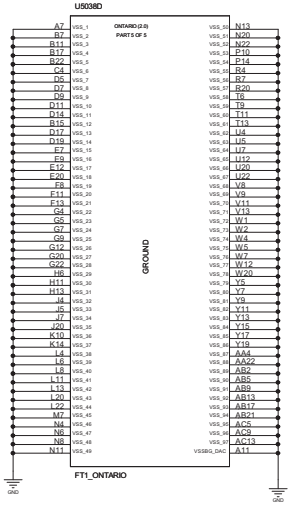
<C3B_20120321>
change R9859 to 34K ohm for thermal
(Thermal shutdown temperature: UMA is 73 degree, DIS is 74degree)

Quanta Computer Inc.
PROJECT : BY7D
Size: — Document Number: ONTATIO DISPLAY/CLK/MI(2/3) — Rev: 1A
Date: Wednesday, March 21, 2012 — Sheet 4 of 45









Quanta Computer Inc.
PROJECT : BY7D

Size	Document Number	Rev
	ONTARIO POWER & DECOUP(3/3)	1A
Date: Wednesday, March 21, 2012	Sheet 5 of 48	

Note :
PCIE_RST2# asserted during transition to S3/S4/S5
to reset PCIE devices in the FCH

NC,no install by default

+3V_S5
R383 *2.2K_4 FCH_TEST0
R382 *2.2K_4 FCH_TEST1
R344 *2.2K_4 FCH_TEST2

For Dimm

+3V
R272 2.2K_4 SMB_RUN_CLK
R270 2.2K_4 SMB_RUN_DAT
R271 *10K_4 GPIO65

CLK_REQG# Not Implemented: leave unconnected

For Lan&WiFi

+3V_S5
R396 2.2K_4 SMB_LAN_CLK
R384 2.2K_4 SMB_LAN_DAT

Note:
SCL0/SDA0: for SMBUS in the S0 power domain
SCL1/SDA1: for SMBUS in the S5 power domain

+3V_S5
R685 10K_4 APU_THERMTRIP#
R368 10K_4 USB_SC_OC#
R374 10K_4 USB_NORMAL_OC#
R377 10K_4 FCH_JTAG_TCK

+3V_S5
R407 10K_4 PCIE_WAKE#
R375 2.2K_4 PWR_BTN#

Note:
LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported

T92 FCH_JTAG_TCK
T93 FCH_JTAG_TDI
T94 FCH_JTAG_RST#

To Azalia

HDaudio interface are +3V_S5

(27) ACZ_SDOUT ACZ_SDOUT R392 33_4 ACZ_SDOUT_R
(27) ACZ_SYNC ACZ_SYNC R391 33_4 ACZ_SYNC_R
(27) ACZ_BITCLK ACZ_BITCLK R406 33_4 ACZ_BCLK_R
C571 *22P/50V_4N
(27) ACZ_RST# ACZ_RST# R357 33_4 ACZ_RST#_R
(27) ACZ_SDIN0 ACZ_SDIN0

+3V_S5
R662 10K_4
G2 *SHORT_PAD
SYS_RST#

+3V_S5
R286 *10K_4
G5 *SHORT_PAD
KSO_5

For LAN,WLAN
(26,28) FCH_PCIE_RST# R678 33_4
(7,28,29,34) PLTRST# D43 B130LAW-7-F_1A
R438 *0_4
C844 150P/50V_4N

PCIE_RST2#

T84 GEVENT22#
T77 GEVENT21#
(34) SLP_S3# SLP_S3#
(34) SLP_S5# SLP_S5#
(34) DNBSWON# DNBSWON# R682 0_4 PWR_BTN#
(10) FCH_PWRGD FCH_PWRGD
FCH_TEST0
T95 FCH_TEST1
FCH_TEST2
(34) EC_A20GATE EC_A20GATE
(34) EC_KBRST# EC_KBRST#
(34) EC_EXT_SCI# EC_EXT_SCI#
T100 GEVENT23#
(34) LPCPD# SYS_RST#
PCIE_WAKE#
(26,28) PCIE_WAKE# GEVENT20#
T80 APU_THERMTRIP#
(4) APU_THERMTRIP# C379 33P/50V_4N +3VO R288 10K/F_4 WD_PWRGD
(34) RSMRST_GATE# R430 0_4 RSMRST# R432 22K_4

<B3A_20120130>
add for EMI (BOT: -9090, 5240)
SMB_LAN_CLK
C601
E@2200P/50V_4X

(26) FCH_PCIE_LAN_CLKREQ# FCH_PCIE_LAN_CLKREQ#
(8) BOARD_ID8 BOARD_ID8
(8) BOARD_ID9 BOARD_ID9
(27) PCBEEP PCBEEP
(11,12,33) SMB_RUN_CLK SMB_RUN_CLK
(11,12,33) SMB_RUN_DAT SMB_RUN_DAT
(26,28) SMB_LAN_CLK SMB_LAN_CLK
(26,28) SMB_LAN_DAT SMB_LAN_DAT
T34 GPIO62
(28) FCH_PCIE_WLAN_CLKREQ# FCH_PCIE_WLAN_CLKREQ#
T29 GPIO51
(8) SPI_HOLD# SPI_HOLD#
GPIO65

Note: M3L doesn't have VGA_PD function
Note :
GPIO[48:65] integrated PU 8.2K to +3V

Note :
Gevent[12:18]# integrated PU 10K to +3V_S5
(Integrated PU is not supported when the pin is configured for USB over current function)

T81 FCH_BLINK
T79 GEVENT6#
T83 GEVENT17#
T86 GEVENT15#
T87 FCH_JTAG_TDO
FCH_JTAG_TCK
FCH_JTAG_TDI
FCH_JTAG_RST#
(24,34) USB_SC_OC# USB_SC_OC# R711 *0_4
(24,34) USB_NORMAL_OC# USB_NORMAL_OC# R710 *0_4

ACZ_BCLK_R
ACZ_SDOUT_R
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2_R
ACZ_SDIN3_R
ACZ_SYNC_R
ACZ_RST#_R
R734 *10KX8

T65
(8,33) BOARD_ID10
T42

KSO_5
T71

T66 KSO_0
T67 KSO_1
T68 KSO_2
T69 KSO_3
T70 KSO_4
T72 KSO_6
T73 KSO_7
T74 KSO_8
T75 KSO_9
T76 KSO_10
T78 KSO_11
T82 KSO_12
T85 KSO_13
T88 KSO_14
T89 KSO_15
T90 KSO_16
T91 KSO_17

KSO_[17:0] provided test points (follow checklist)

HUDSON-M3

Part 4 of 5

U3A

PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166

PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226

USBCLK/14M_25M_48M_OSC
USB_RCOMP R647 11.8K/F_6
USB_FSD1P/GPIO186 T157
USB_FSD1N T156
USB_FSD0P/GPIO185 T159
USB_FSD0N T158

USB_HSD13P/N
USB_HSD12P/N
USB_HSD11P/N
USB_HSD10P/N
USB_HSD9P/N
USB_HSD8P/N
USB_HSD7P/N
USB_HSD6P/N
USB_HSD5P/N
USB_HSD4P/N
USB_HSD3P/N
USB_HSD2P/N
USB_HSD1P/N
USB_HSD0P/N

USBSS_CALRP R646 1K@1K/F_4
USBSS_CALRN R642 1K@1K/F_4
+FCH_VDD_11_SSUSB_S

USB_SS_TX3P/N
USB_SS_RX3P/N
USB_SS_TX2P/N
USB_SS_RX2P/N
USB_SS_TX1P/N
USB_SS_RX1P/N
USB_SS_TX0P/N
USB_SS_RX0P/N

USB_SS_TX/RX[3,2]P/N,USB_HSD[13, 12, 9, 4]P/N,USB_FSD[1,0]P/N signal pairs do not exist on Hudson-M3L/D3L

SCL2/GPIO193 SMB_EC_CLK R318 *0_4 MBCLK
SDA2/GPIO194 SMB_EC_DAT R315 *0_4 MBDATA
SCL3_LV/GPIO195 SCLK3
SDA3_LV/GPIO196 SDATA3
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
EC_PWM2

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

EMBEDDED CTRL

USB 3.0 / USB 2.0 / USB 1.1 / USB MISC / ACPI / WAKE UP EVENTS / GPIO / HD AUDIO / USB OC

Hudson-M3

MBCLK (34,36)
MBDATA (34,36)
SCLK3 (4)
SDATA3 (4)
EC_PWM2 (10)

HUB3

Reserve USB2.0/3.0 option (Left Up)
USB3.0 S&C (Right)

Note :
USB 2.0 and USB 3.0 signal pair combinations to a single USB 3.0 connector:
- USB_SS_TX/RX1P/N and USB_HSD11P/N
- USB_SS_TX/RX0P/N and USB_HSD10P/N

<Layout Note>
USB P/N pairs with trace lengths up to 10"

HUB2

WLAN
CCD on LVDS
Card Reader

HUB1

USB2.0 debug port (Left Down)
USB3.0 Port 2
USB3.0 S&C

Note:
SCL2/SDA2: for SMBUS in the S5 power domain
SCL3/SDA3: for SMBUS in the S5 power domain

+3V_S5 R15 0_4 R599 10K_4 SMB_EC_CLK
R600 10K_4 SMB_EC_DAT
+3V_S5 R14 0_4 R593 10K_4 SCLK3
+3V R594 *0_4 R595 10K_4 SDATA3

SCL2/SDA2:
SMBUS Implemented: PU 2.2K to +3V_S5
SMBUS Not Implemented: PU 10K to +3V_S5
SCL3/SDA3:
Low Voltage SMBUS Implemented: PU 10K to APU_VDDIO (+3V)
Low Voltage SMBUS Not Implemented: PU 10K to +3V_S5

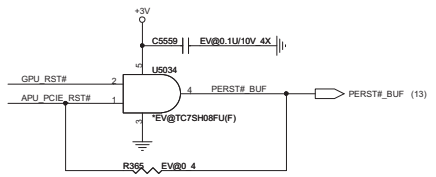
EC will Conflict with FCH, did not mount R315&R318

EC	FCH	Device I2C_Device(S)			
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		EEPROM	APU		ALL
I2Ce_3(M)		VGA Thermal			
	I2Cf_3(M)			APU	S5
	I2Cf_1(M)	Lan	WLan		S5
	I2Cf_0(M)	Dimm	Clk Gen		S0

Quanta Computer Inc.
PROJECT : BY7D
Size | Document Number: FCH 1/5(GPIO/USB/AZ) | Rev: 1A
Date: Wednesday, March 21, 2012 | Sheet 6 of 45

Note :
PCIE_RST# asserted during transition to S3/S4/S5 to reset PCIE devices in the APU
A_RST# asserted during transition to S3/S4/S5 to reset all devices in the FCH or connected to it, except the ACPI logic in the FCH.

APU_PCIE_RST# IS FOR PCIE DEVICES ON APU



Net	GPIO		I/O	Power Well	DOS
GFXPG_1V_EN	GPIO28	DGPU_PWRGD	I	+3.3V	"0->1"
PE_GPIO0	GPIO44	DGPU_RST#	O	+3.3V	"0->1"
PE_GPIO1	GPIO45	DGPU_PWREN	O	+3.3V	"0->1"

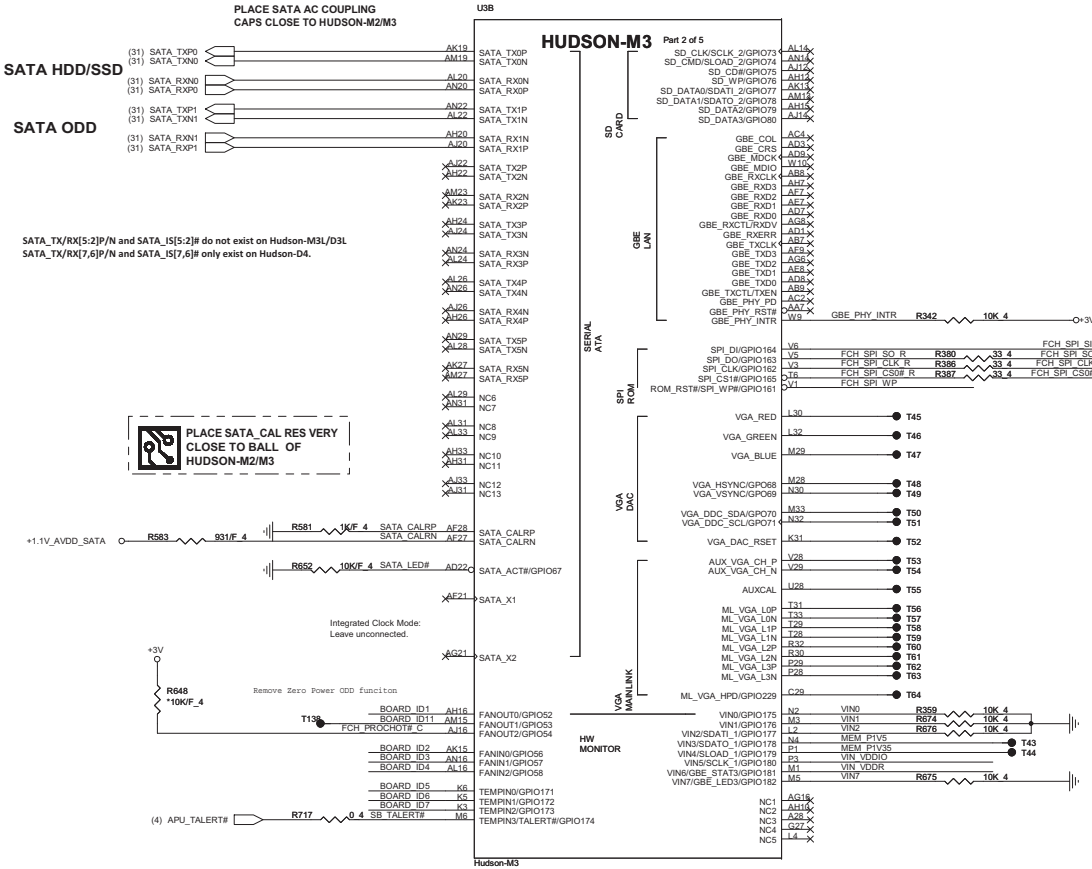
Note: CLK_FCH_SRCP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_PCIE_VGAP/N is 100MHZ SSC
Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable

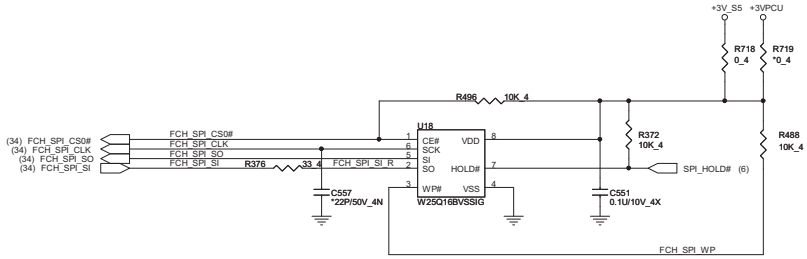
<B3A_20120131> change to 0 ohm for layout routing

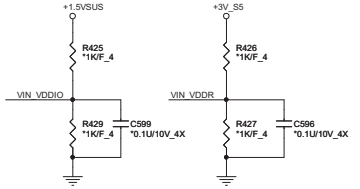
<B3A_20120207>
change C397,C381 to 27pF (crystal vendor suggest)
Main source: BG625000737
2nd source: BG625000486

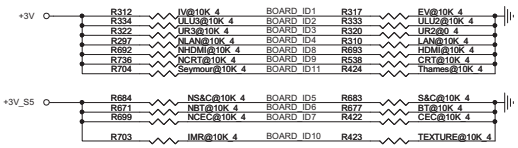
Quanta Computer Inc.					
PROJECT : BY7D					
Size	Document Number				Rev
	FCH 2/5(ACPI/PCI/CLK)				1A
Date: Wednesday, March 21, 2012		Sheet 7	of	45	

SPI Shared Flash



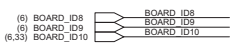


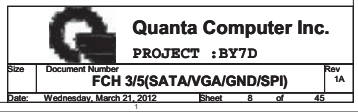




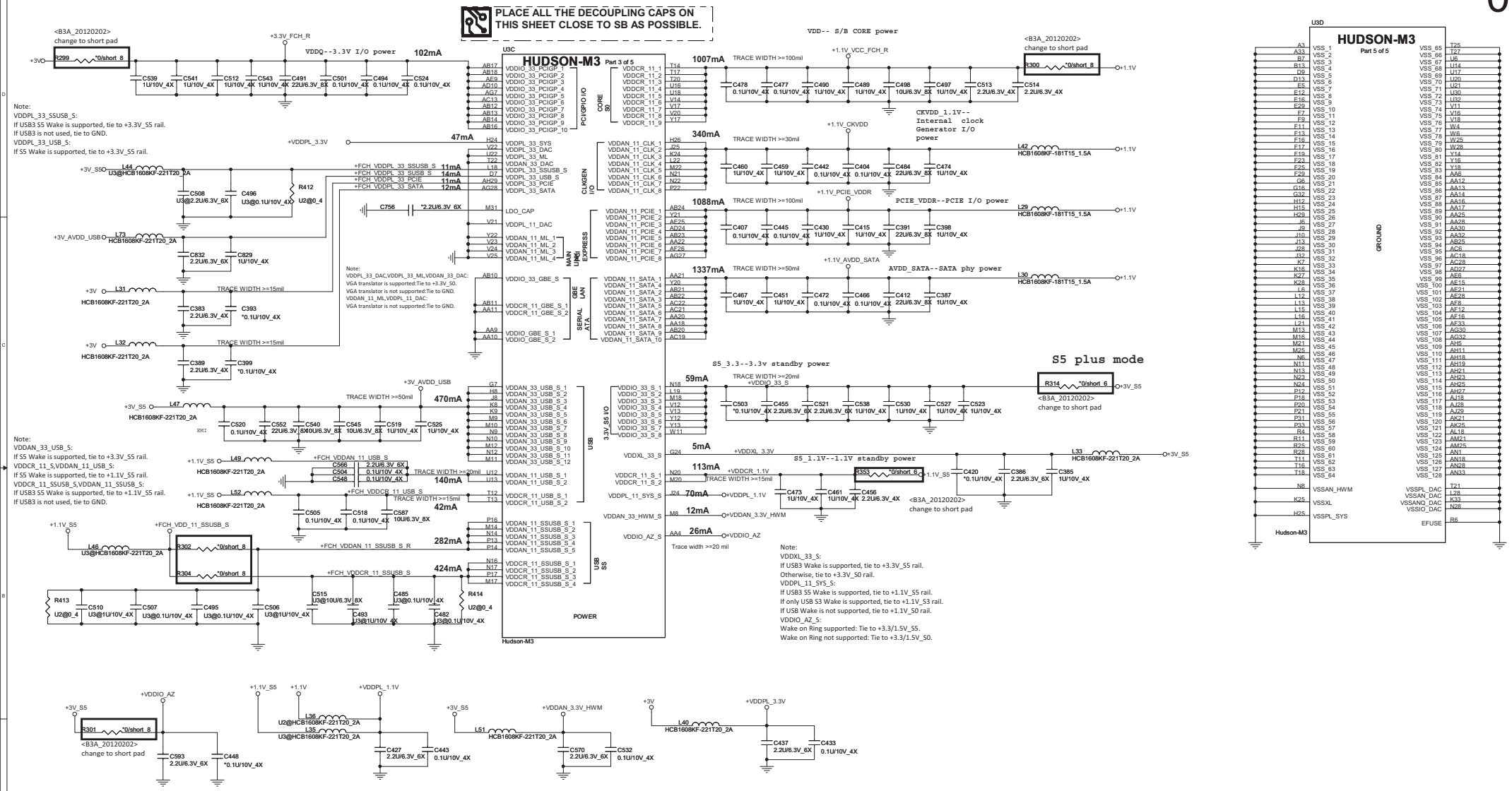
BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11
UMA SKU VGA SKU	H L										
ULU3 ULU2		H L									
UR3 UR2			H L								
W/O LAN W LAN				H L							
W/O S&C W S&C					H L						
W/O BT W BT						H L					
W/O CEC W CEC							H L				
W/O HDMI W HDMI								H L			
W/O CRT W CRT									H L		
Metal/IMR TEXTURE										H L	
Seymour Thames											H L





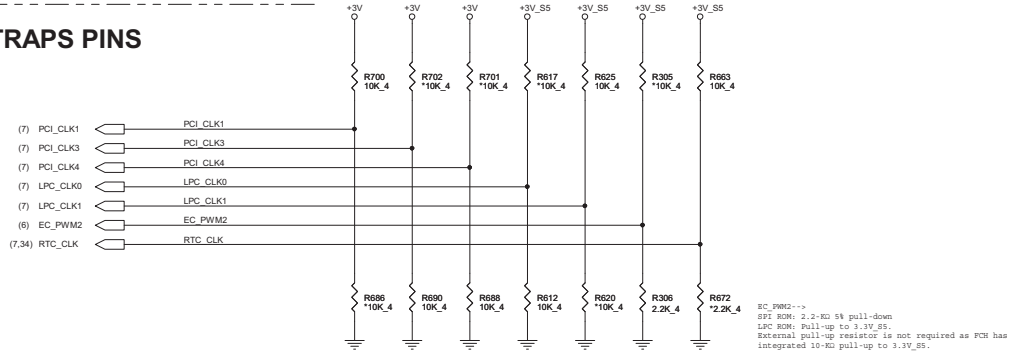
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



Quanta Computer Inc.				
PROJECT : BY7D				
Size	Document Number			Rev
	FCH 4/5(POWER)			1A
Date: Wednesday, March 21, 2012		Sheet 9	of	45

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

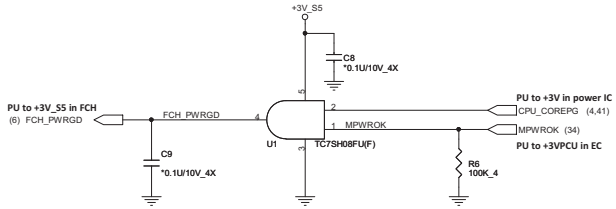


Remove PCI_CLK2 function

REQUIRED STRAPS

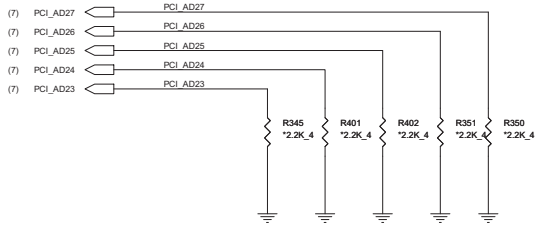
	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

FCH POWER GOOD CIRCUIT



DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

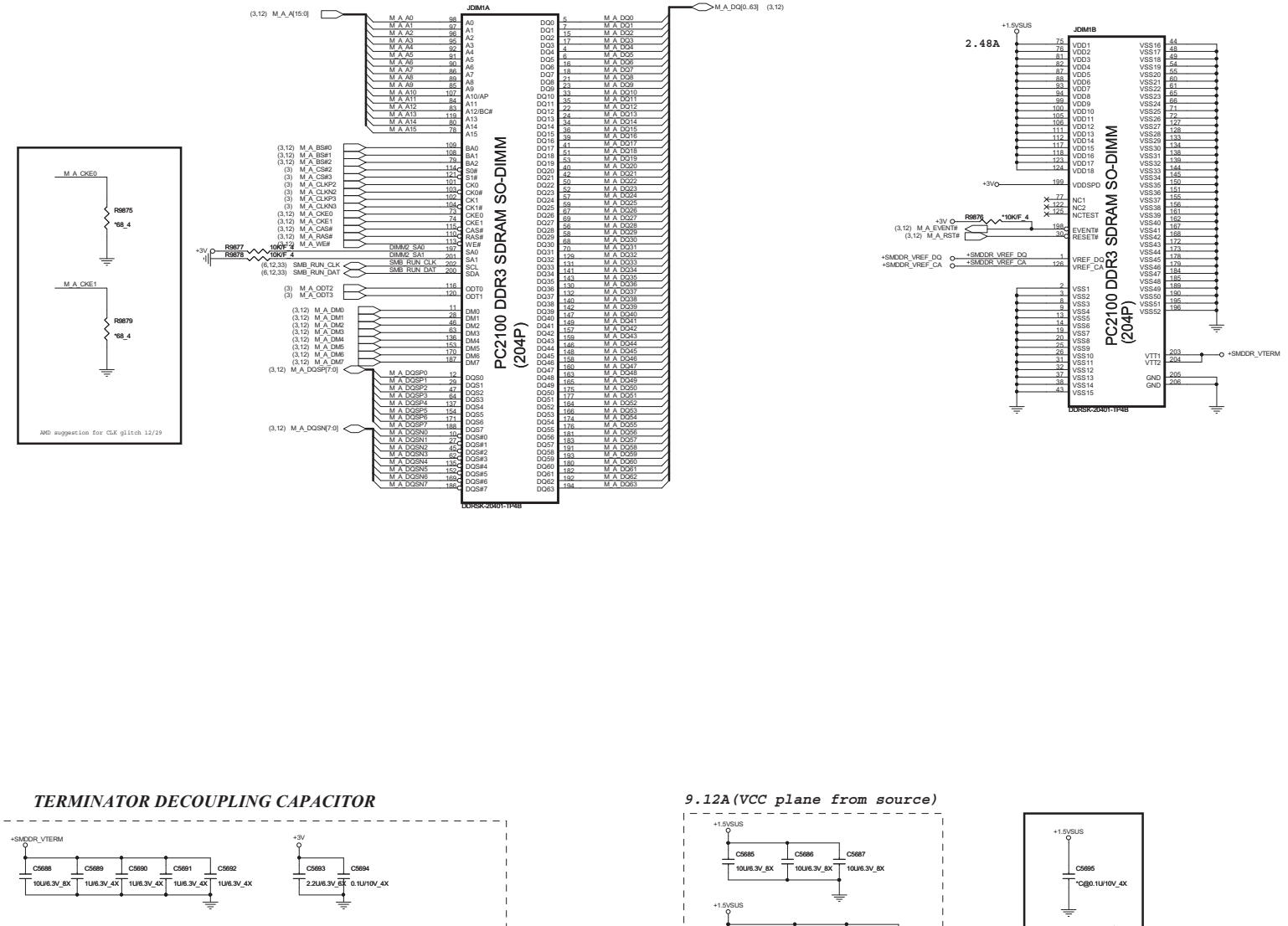


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

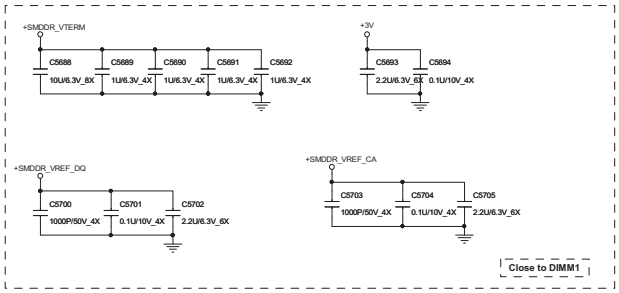
Quanta Computer Inc.
PROJECT : BY7D

Size	Document Number	Rev
	FCH 5/5(STRAP & PWRGD)	1A

Date: Monday, March 19, 2012 Sheet 10 of 45



TERMINATOR DECOUPLING CAPACITOR



9.12A(VCC plane from source)

Quanta Computer Inc.

PROJECT : BY7D

Size	Document Number	Rev
	DDRIII SODIMM1	1A
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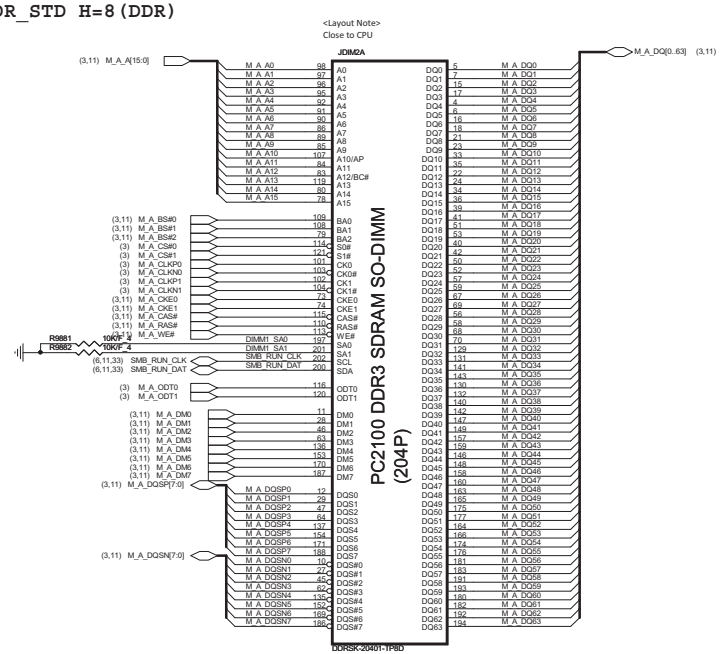
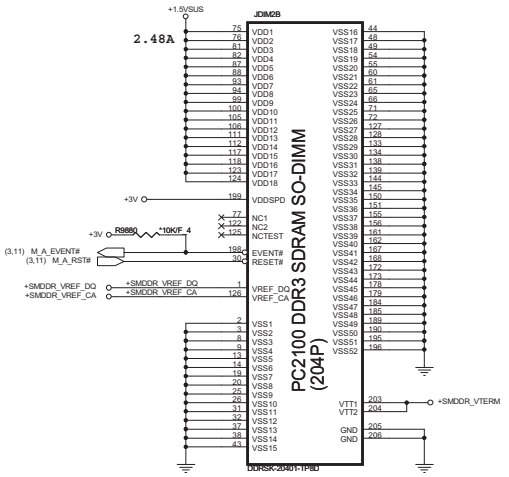
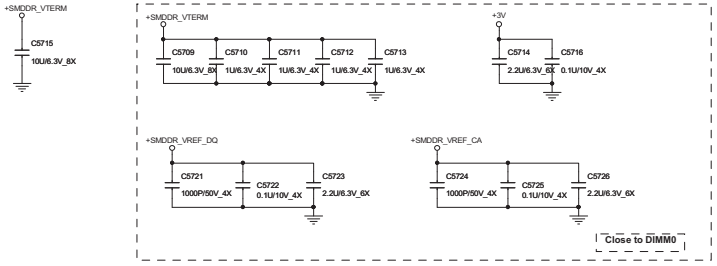
DDR_STD H=8(DDR)

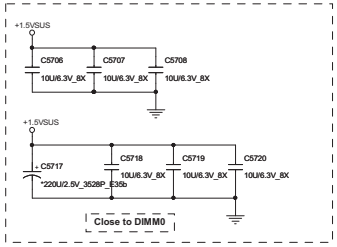


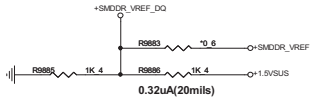


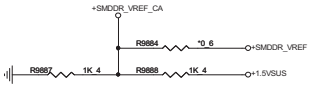
TERMINATOR DECOUPLING CAPACITOR



9.12A(VCC plane from source)



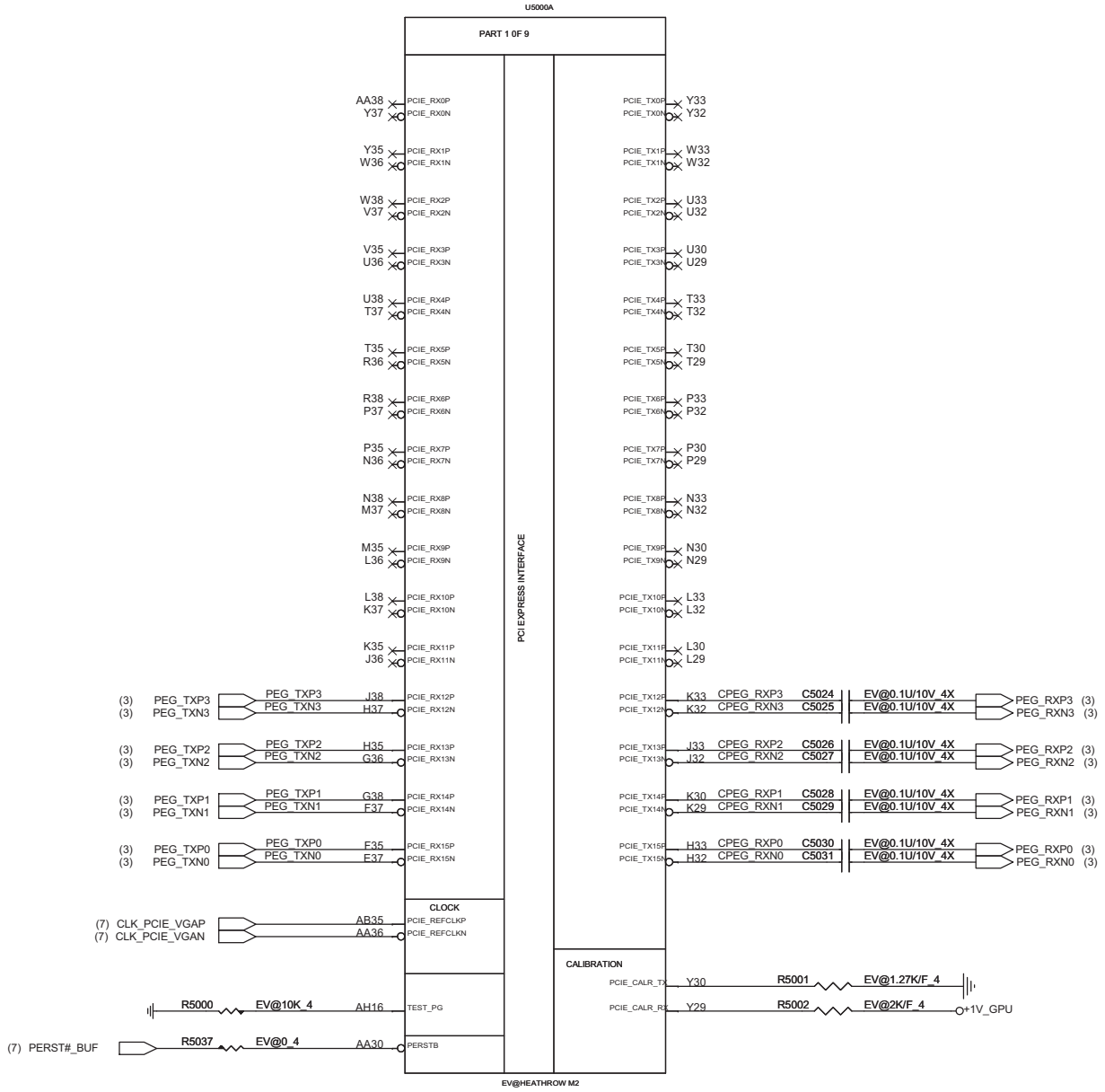




Quanta Computer Inc.

PROJECT : BY7D

Size	Document Number	Rev
	DDRIII SODIMM2	1A
Date: Monday, March 19, 2012	Sheet 12 of 48	

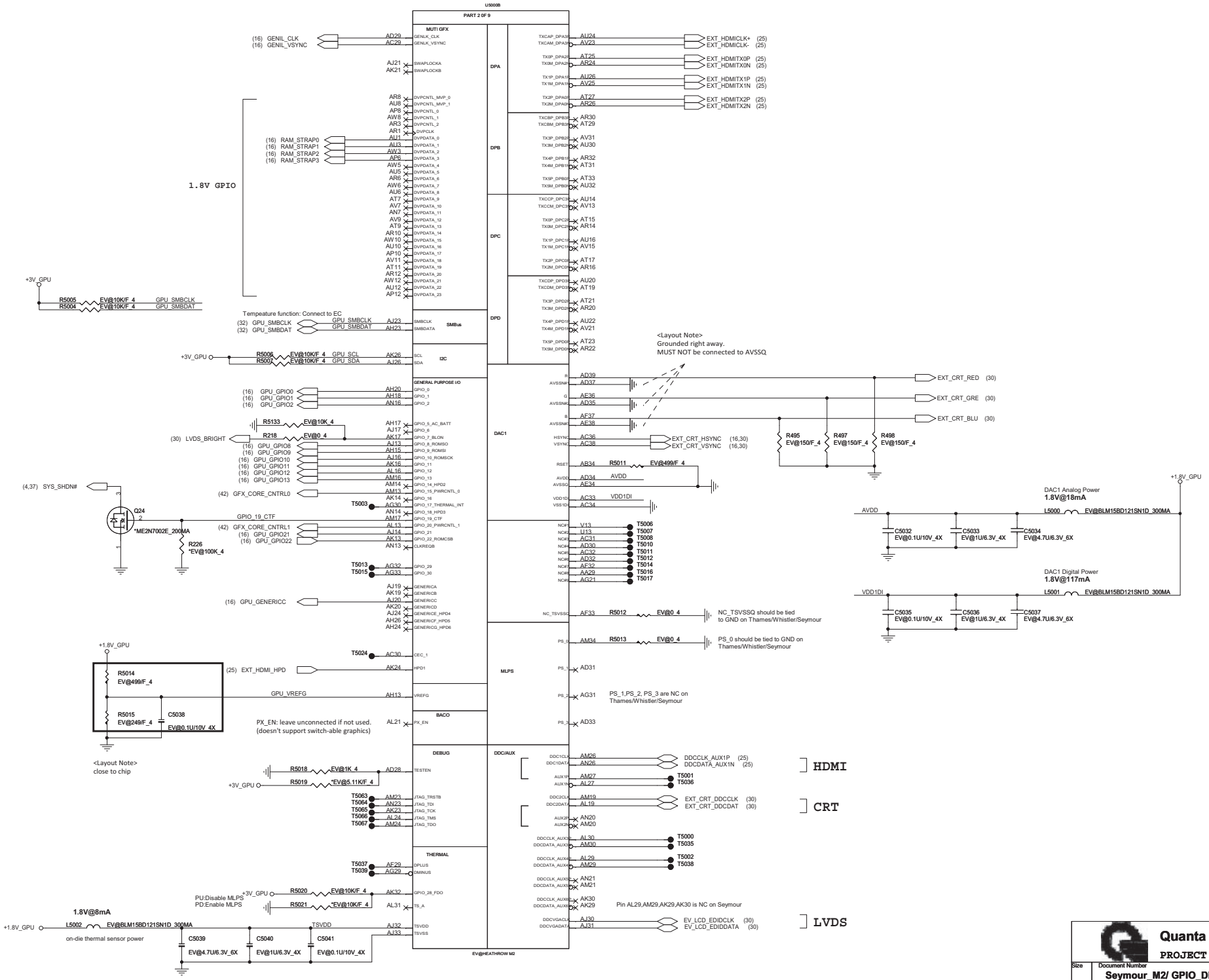


Seymour Power-on sequence

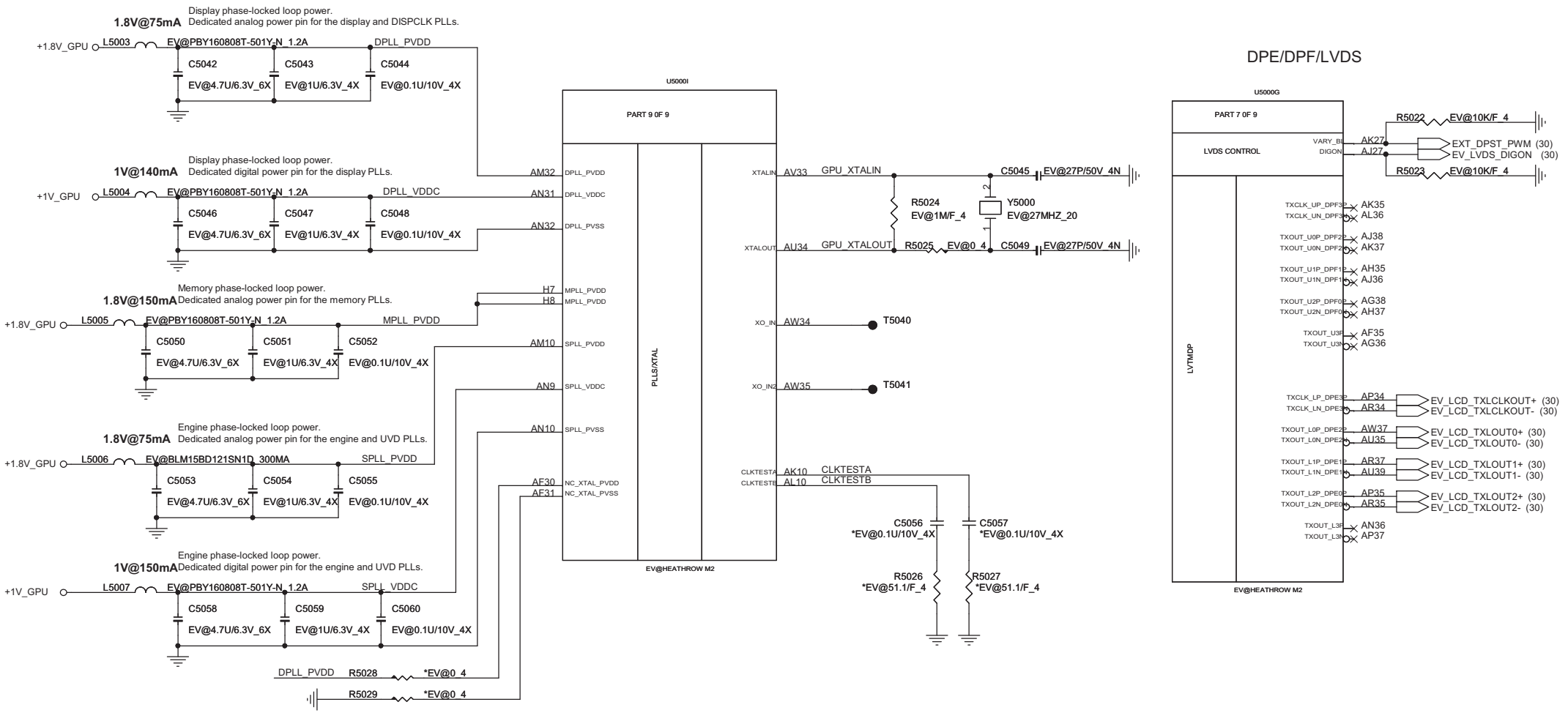
1 => +1V_GPU
2 => +3V_GPU
3 => +VGPU_CORE,+1.5V_GPU
4 => +1.8V_GPU

PEG

Intel platform: Lane0 ~ Lane15
Brazos platform: Lane12 ~ Lane15
Comal and Sabine platform: Lane8 ~Lane15



Quanta Computer Inc.		
PROJECT : BY7D		
Size	Document Number: Seymour_M2/ GPIO_DP_CRT_I2C	Rev: 1A
Date: Wednesday, March 21, 2012	Sheet 14 of 45	

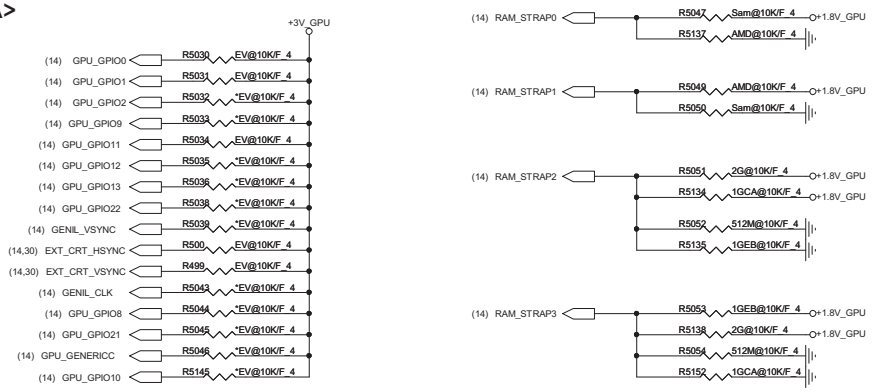


Quanta Computer Inc.

PROJECT : BY7D

Size	Document Number	Rev
	Seymour_M2/ XTAL_LVDS	1A
Date: Wednesday, March 21, 2012	Sheet 15 of 45	

<VGA>



DDR3 Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 4	512MB	0	0	0	1
	K4W2G1646C-HC11 (128M*16,C-die)	AKD5MGWT500 * 4	1GB	0	1	0	1
	K4W2G1646E-HC11 (128M*16,E-die)	AKD5MGWT500 * 4	1GB	1	0	0	1
	K4W2G1646C-HC11 (128M*16)	AKD5MGWT500 * 8	2GB	1	1	0	1
AMD	23EY2387MC11 (64M*16)	AKD5EZWT700 * 4	512MB	0	0	1	0
	23EY4187MA11 (128M*16,A-die)	AKD5DZWT700 * 4	1GB	0	1	1	0
	23EY4187MB11 (128M*16,B-die)	TBD * 4	1GB	1	0	1	0
	23EY4187MA11 (128M*16)	AKD5DZWT700 * 8	2GB	1	1	1	0

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET

STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	GENLK_CLK	Reserved	0
RESERVED	PS_1[2]	GPIO8	Reserved	0
RESERVED	NA	GPIO21	Reserved	0
RESERVED	NA	GENERICC	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

System Memory Aperture size

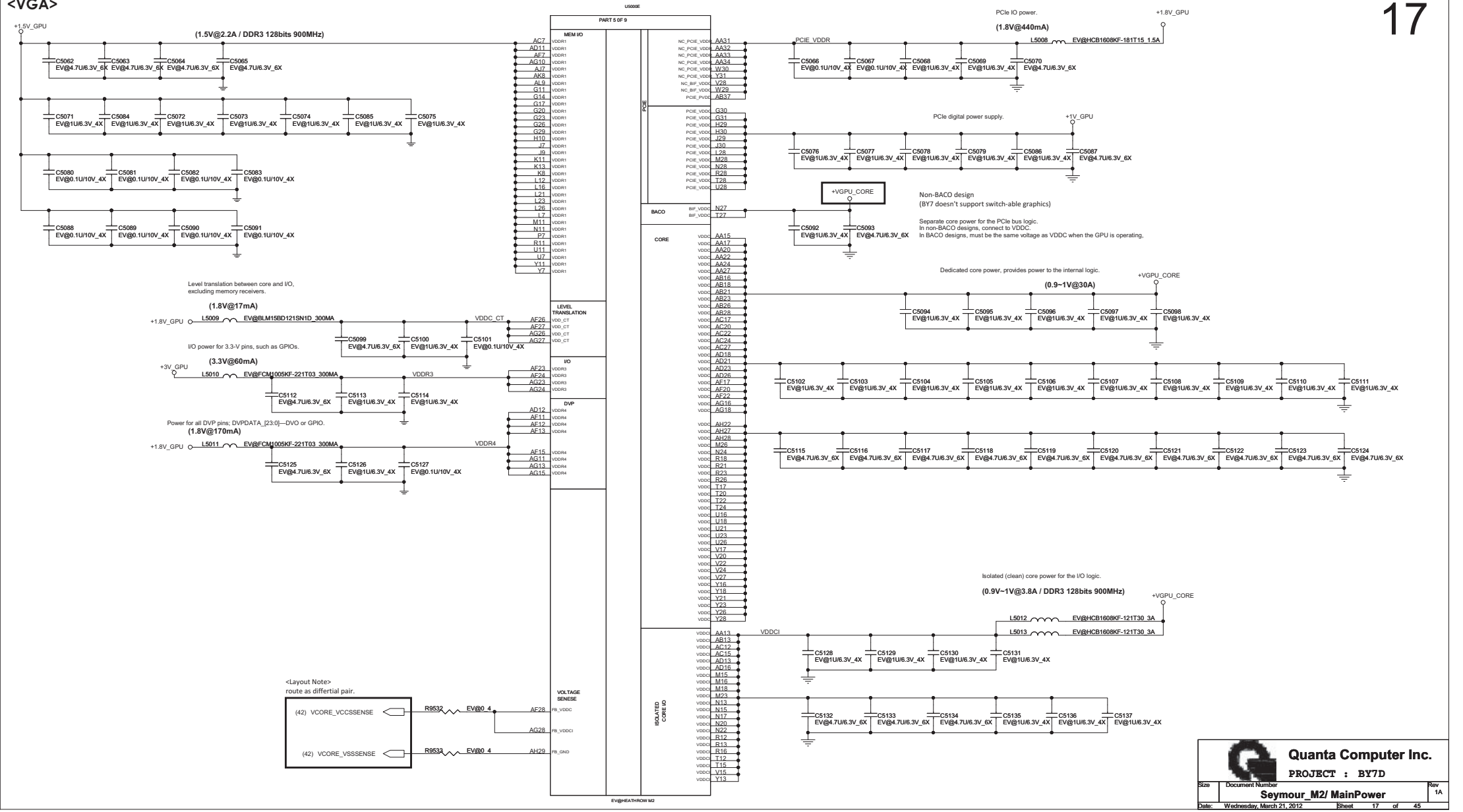
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1

EEPROM

Quanta Computer Inc.
PROJECT : BY7D

Size	Document Number	Rev
	Seymour_M2/ STRAPS_Thermal	1A
Date: Monday, March 19, 2012	Sheet 16 of 45	

<VGA>



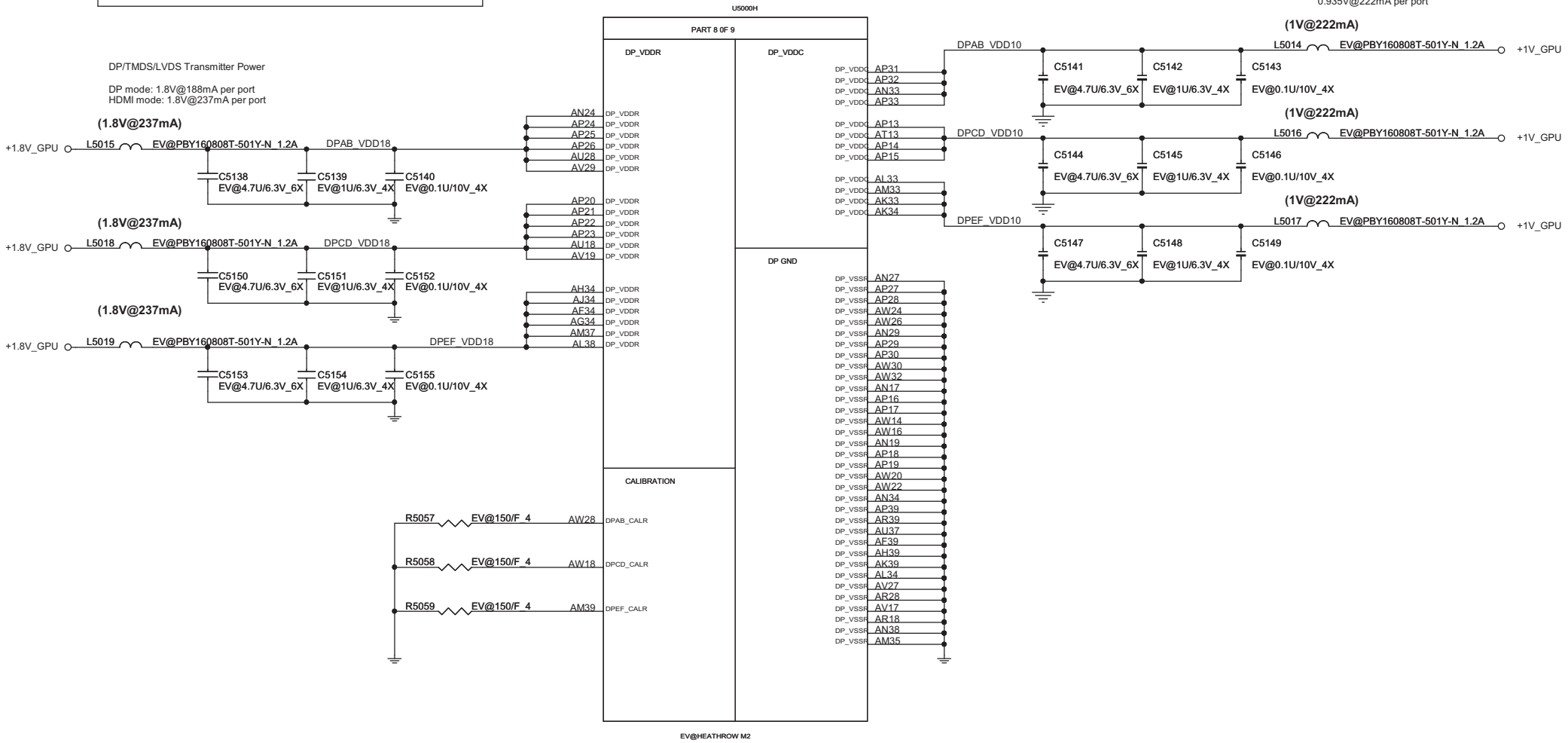
Quanta Computer Inc.			
PROJECT : BY7D			
Size	Document Number		Rev
	Seymour_M2/ MainPower		1A
Date: Wednesday, March 21, 2012	Sheet 17 of 45		

<VGA>

For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

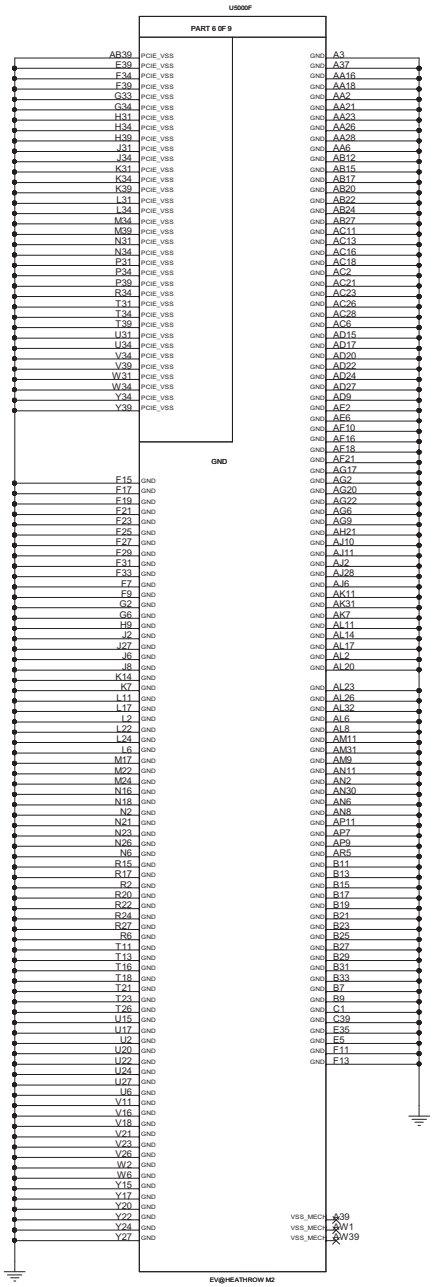
For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

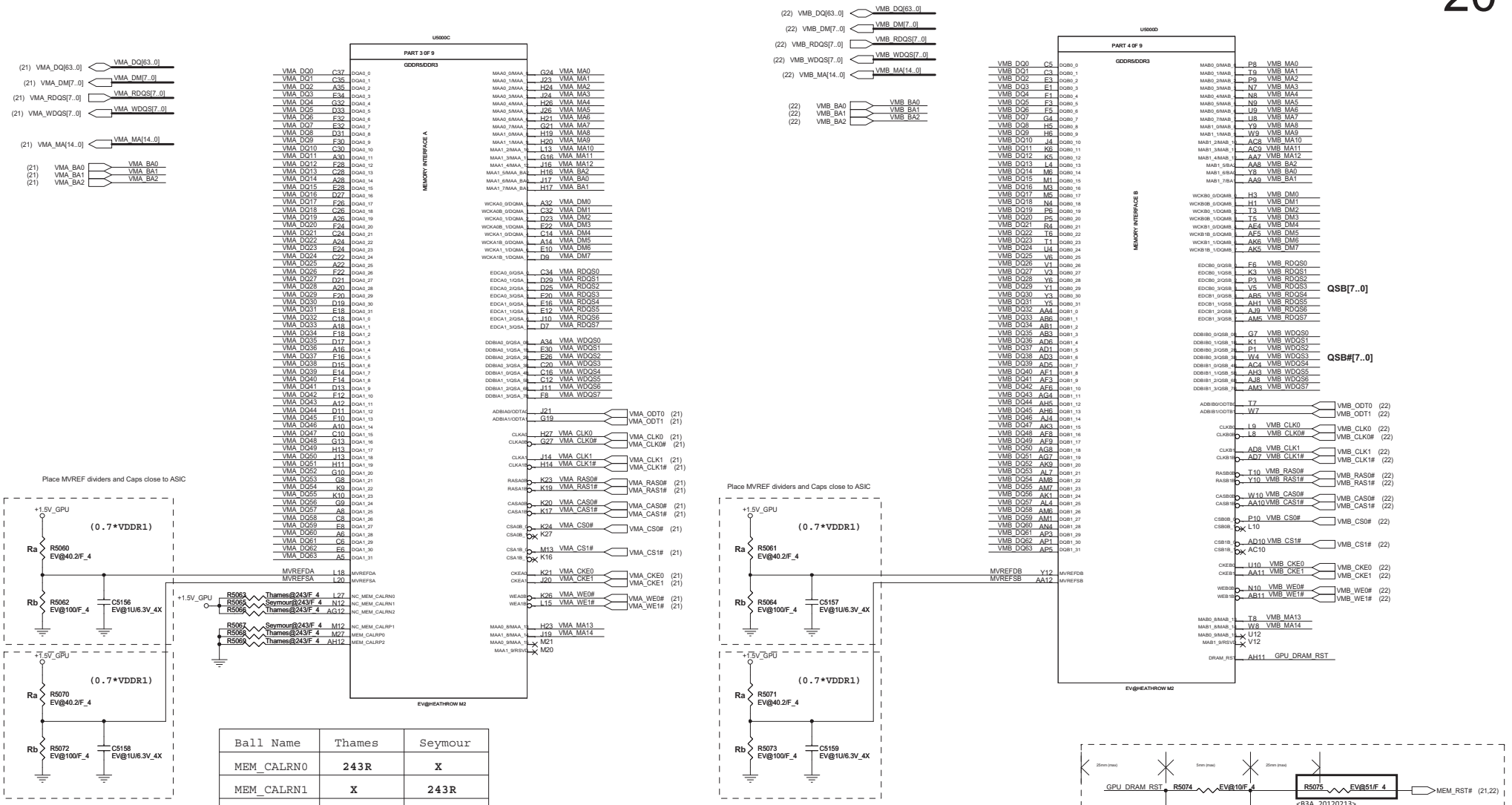


Quanta Computer Inc.
PROJECT : BY7D

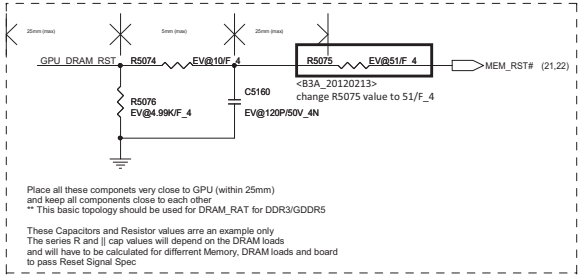
Size	Document Number	Rev
	Seymour_M2/ DP_Powers	1A
Date: Wednesday, March 21, 2012	Sheet 18 of 45	



Quanta Computer Inc.		
PROJECT : BY7D		
Size	Document Number: Seymour_M2/ GND	Rev: 1A
Date: Wednesday, March 21, 2012	Sheet 19 of 45	



Ball Name	Thames	Seymour
MEM_CALRN0	243R	X
MEM_CALRN1	X	243R
MEM_CALRN2	243R	X
MEM_CALRP0	243R	X
MEM_CALRP1	X	243R
MEM_CALRP2	243R	X

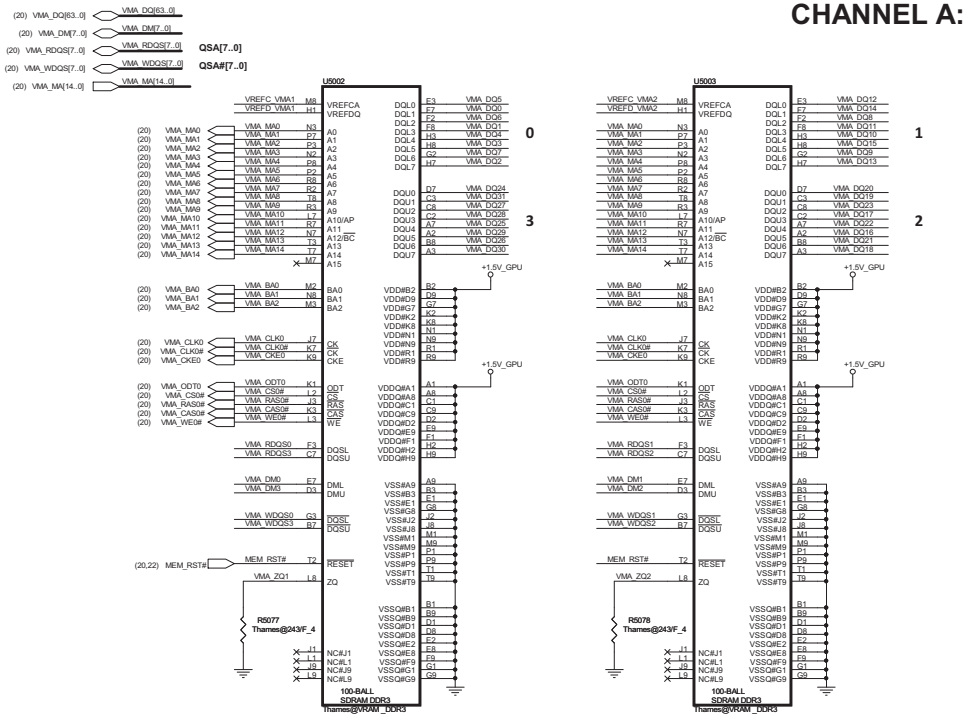


Quanta Computer Inc.

PROJECT : BY7D

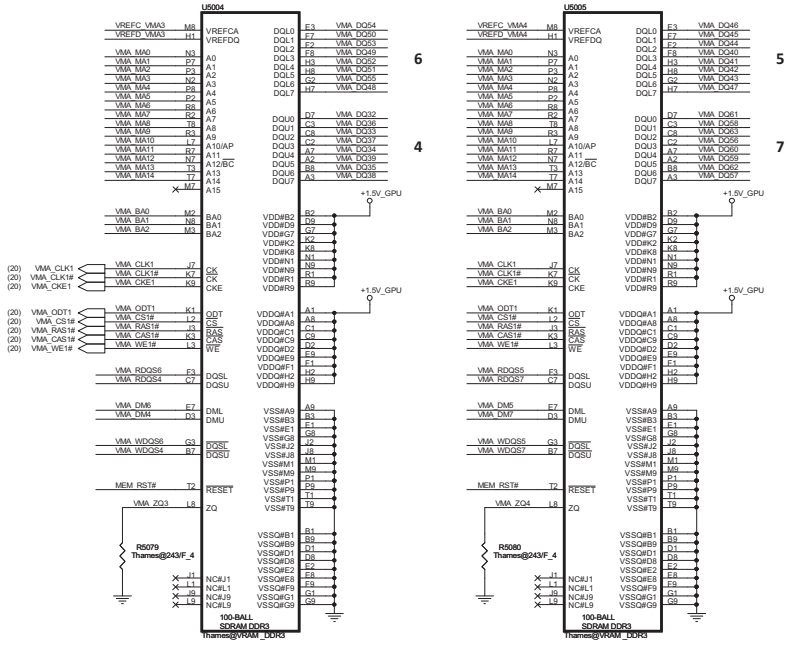
Size	Document Number	Rev
	Seymour_M2/ MEM Interface	1A
Date: Wednesday, March 21, 2012	Sheet 20 of 45	

CHANNEL A: 512MB DDR3 (64M*16*4pcs) <VGA>



TOP Left

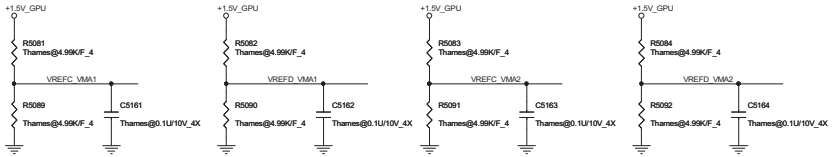
BOT Left



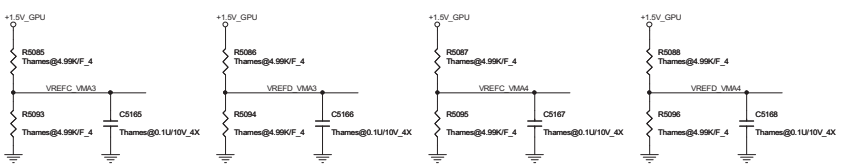
TOP Right

BOT Right

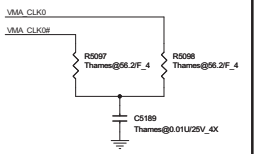
Group-A0 VREF



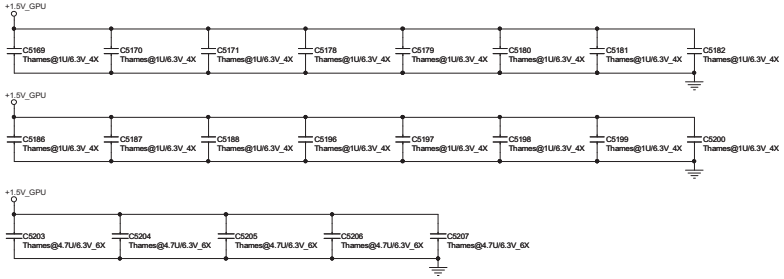
Group-A1 VREF



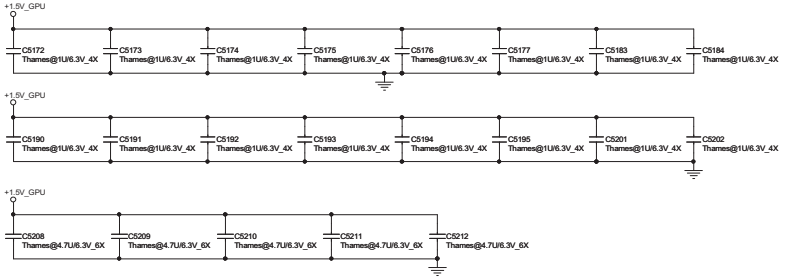
MEM_A0 CLK



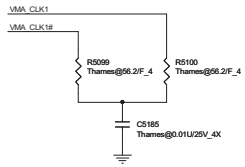
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK

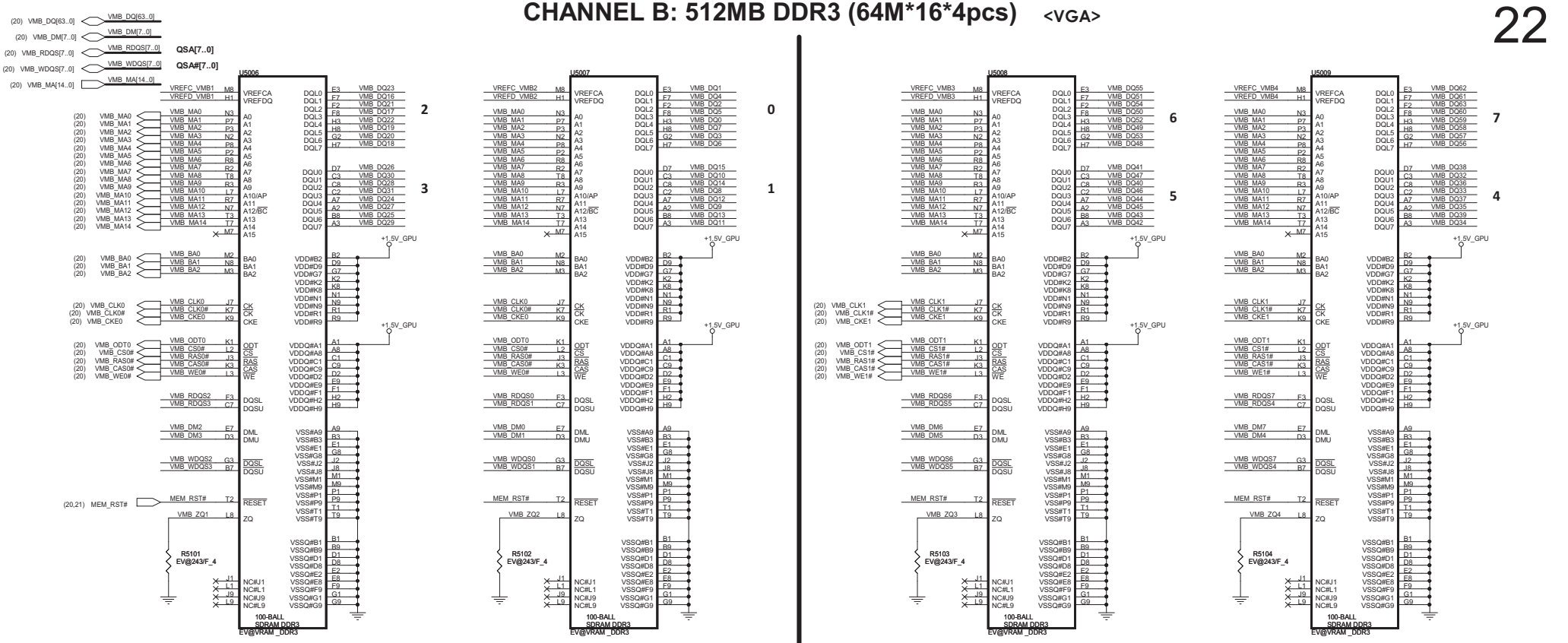


Quanta Computer Inc.

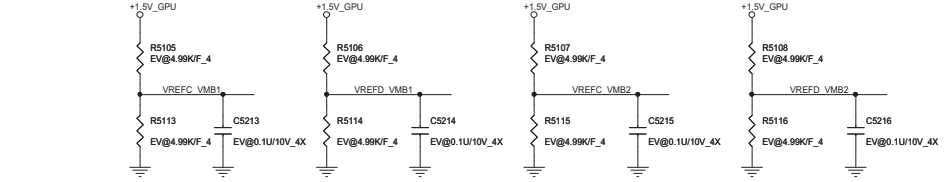
PROJECT : BY7D

Size	Document Number	Rev
	VRAM_A: DDR3*4PCS	1A
Date: Monday, March 19, 2012	Sheet 21 of 45	

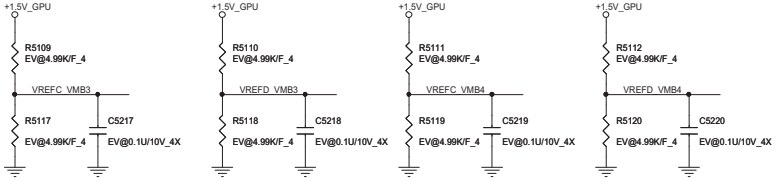
CHANNEL B: 512MB DDR3 (64M*16*4pcs) <VGA>



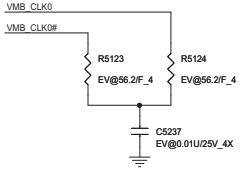
Group-B0 VREF



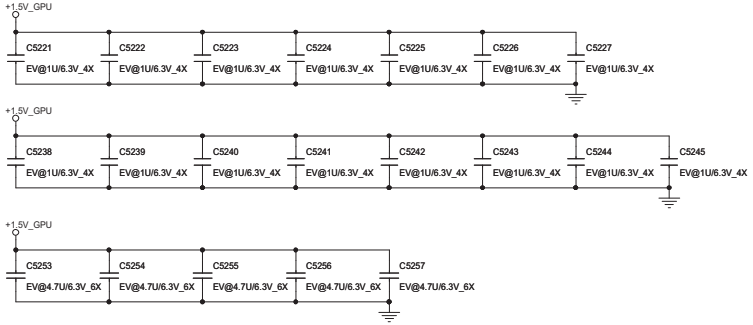
Group-B1 VREF



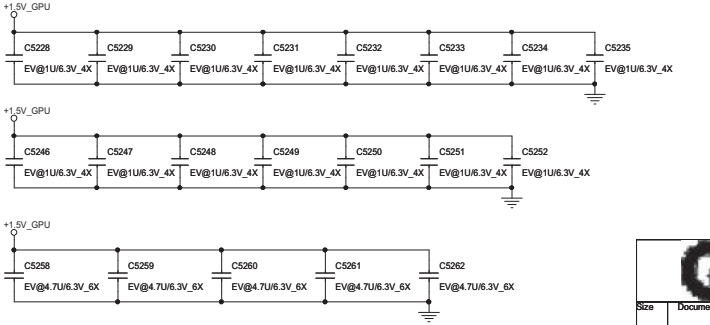
MEM_B0 CLK



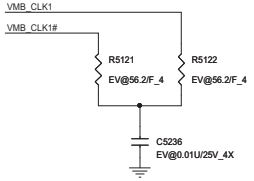
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.

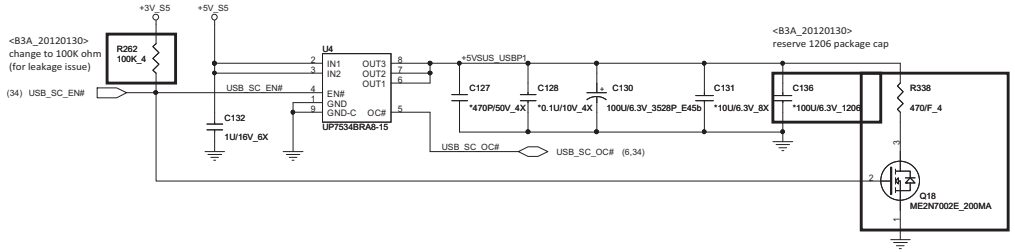
PROJECT : BY7D

Size	Document Number	Rev
	VRAM_B: DDR3*4PCS	1A

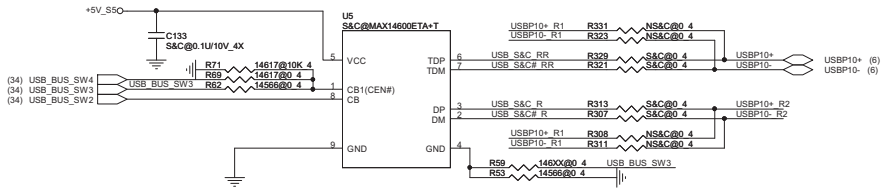
Date: Wednesday, March 21, 2012 Sheet 22 of 45

Non-BACO design
(Brazos doesn't support Muxless Switch-able Graphics)

USB 3.0 Power switch <USB> <U3B>



USB w S&C MAXIM solution <SLC>

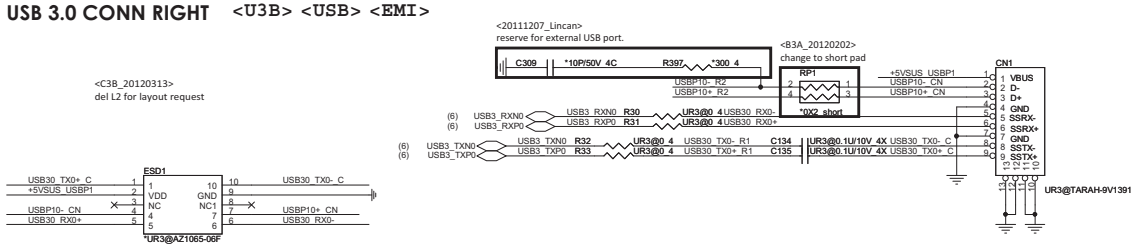


14566/14600		
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM for 14566
1	0	Pass-Through(USB) mode for 14600
1	1	pass-through(USB) with CDP Emulation for 14600

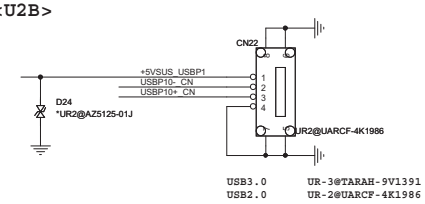
14617			
CB0	CB1	CB2	Status
X	X	1	Force Apple 2A Charger Mode
0	0	0	Autodetection charger mode
0	1	0	Force-Dedicated Charger Mode
1	0	0	USB Pass-Through Mode Connect DP/DM to TDP/TDM
1	1	0	USB Pass-Through Mode with CDP Emulation.Auto connect DP/DM to TDP/TDM depending on CDP status

	R69	R62	R59	R53	R71
14566		V		V	
14600			V		
14617(with CB2)	V		V		
14617(no CB2)			V		V

USB 3.0 CONN RIGHT <U3B> <USB> <EMI>

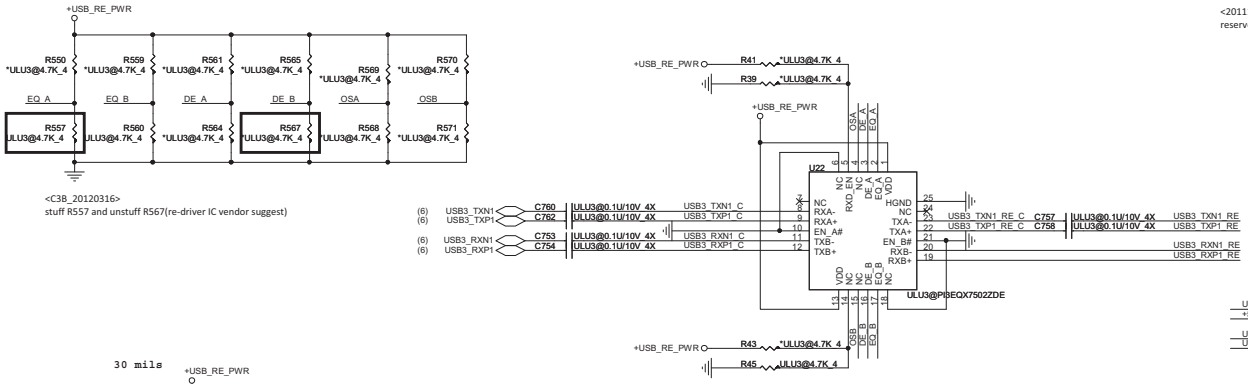


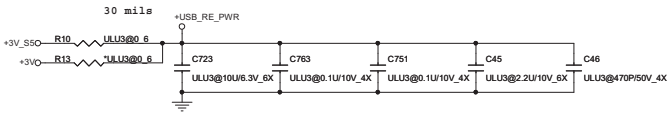
USB 2.0 CONN RIGHT <U3B> <U2B>



USB3.0 UR-3@TARAH-9V1391
USB2.0 UR-2@UARCF-4K1986

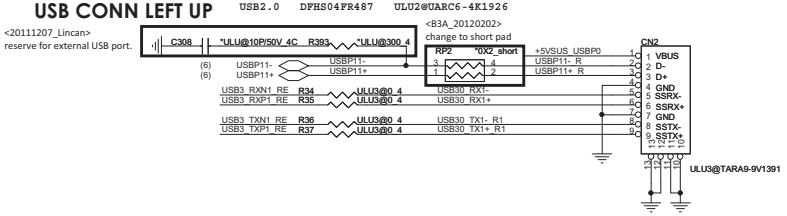
USB 3.0 Power switch

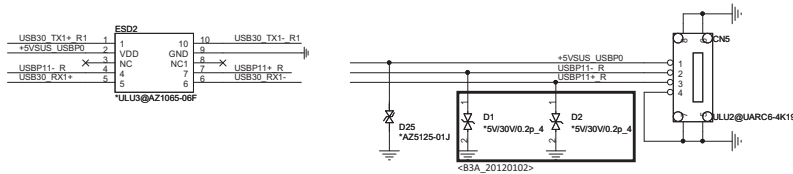




USB CONN LEFT UP

USB3.0 DFHS09FR085 ULU3@TARA9-9V1391
USB2.0 DFHS04FR487 ULU2@UARC6-4K1926

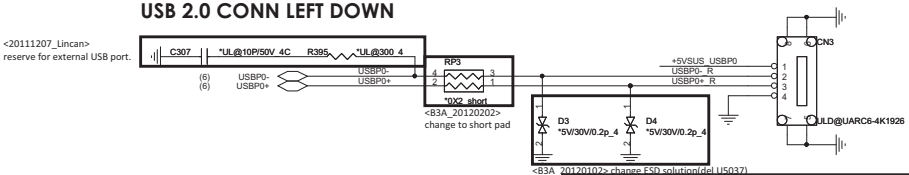




<B3A_20120102>
change ESD solution(del U5037)

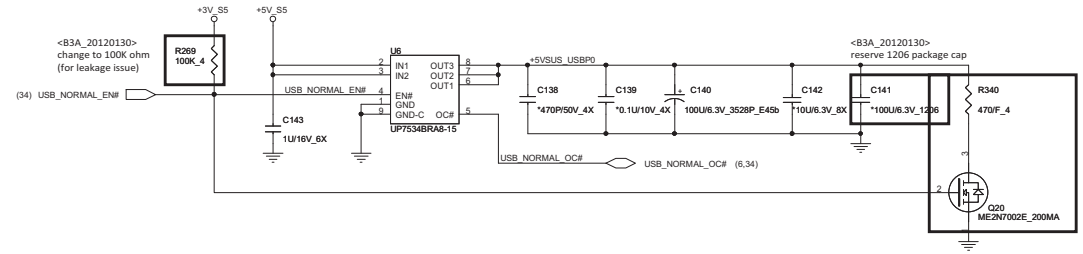
<C3B_20120313>
del L3 for layout request

USB 2.0 CONN LEFT DOWN

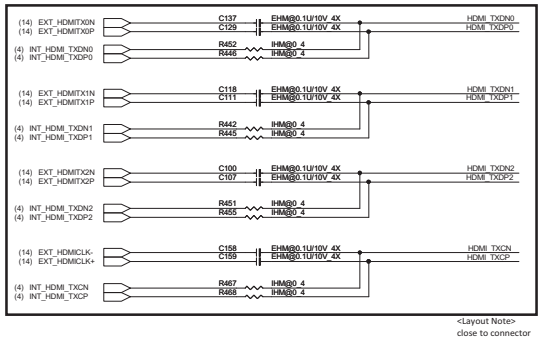


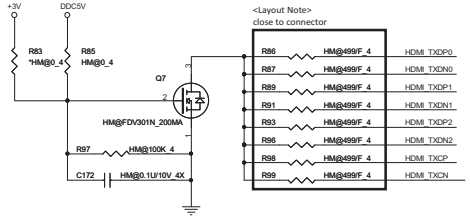
<B3A_20120102> change ESD solution(del U5037)

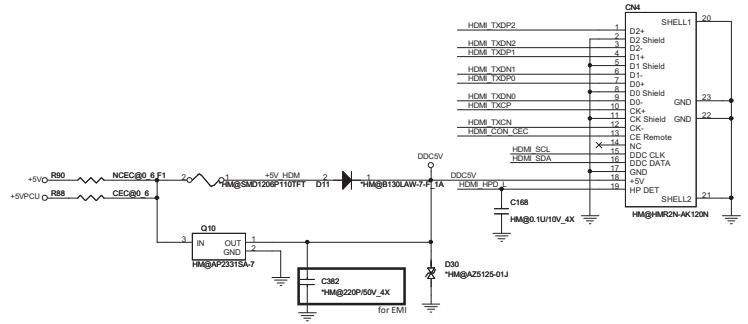
<C3B_20120313>
del L4 for layout request



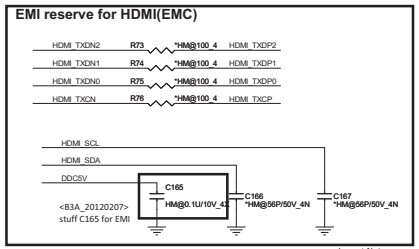
HDMI

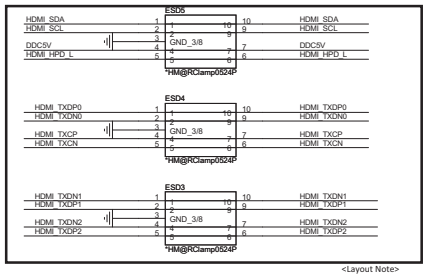


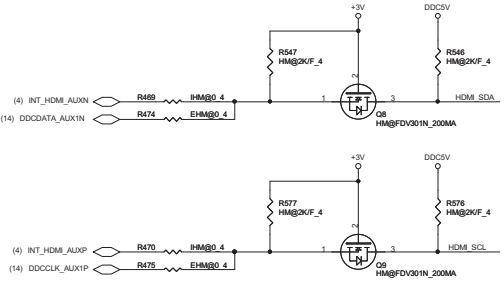




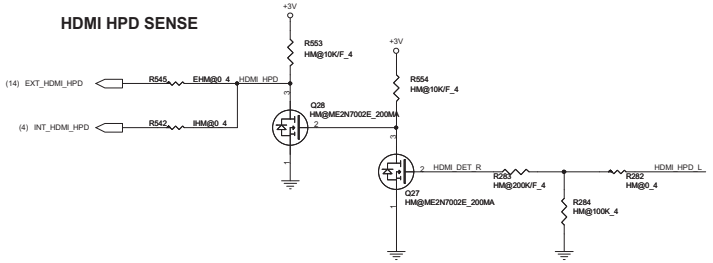
EMI reserve for HDMI(EMC)



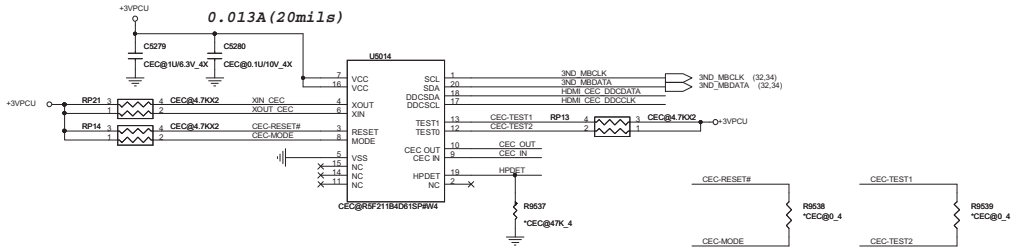




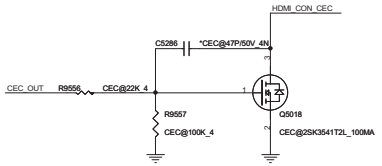
HDMI HPD SENSE



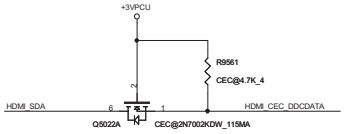
HDMI *CEC* <CEC>



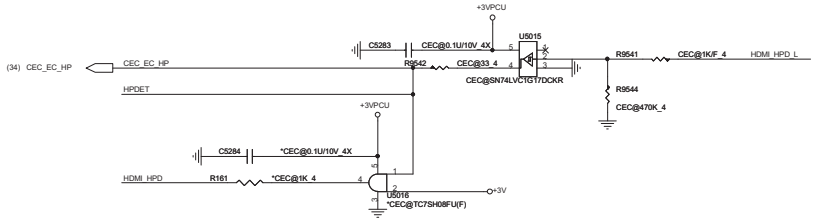
CEC Output <CEC> (To Connect)



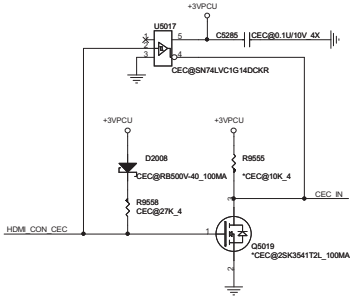
CEC SMBus Level Shift <CEC> (To CECC)

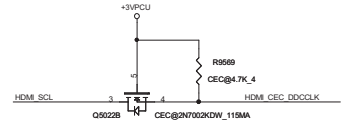


CEC HotPlug <CEC>



CEC Input <CEC> (To CECC)





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	HDMI/CEC	1A
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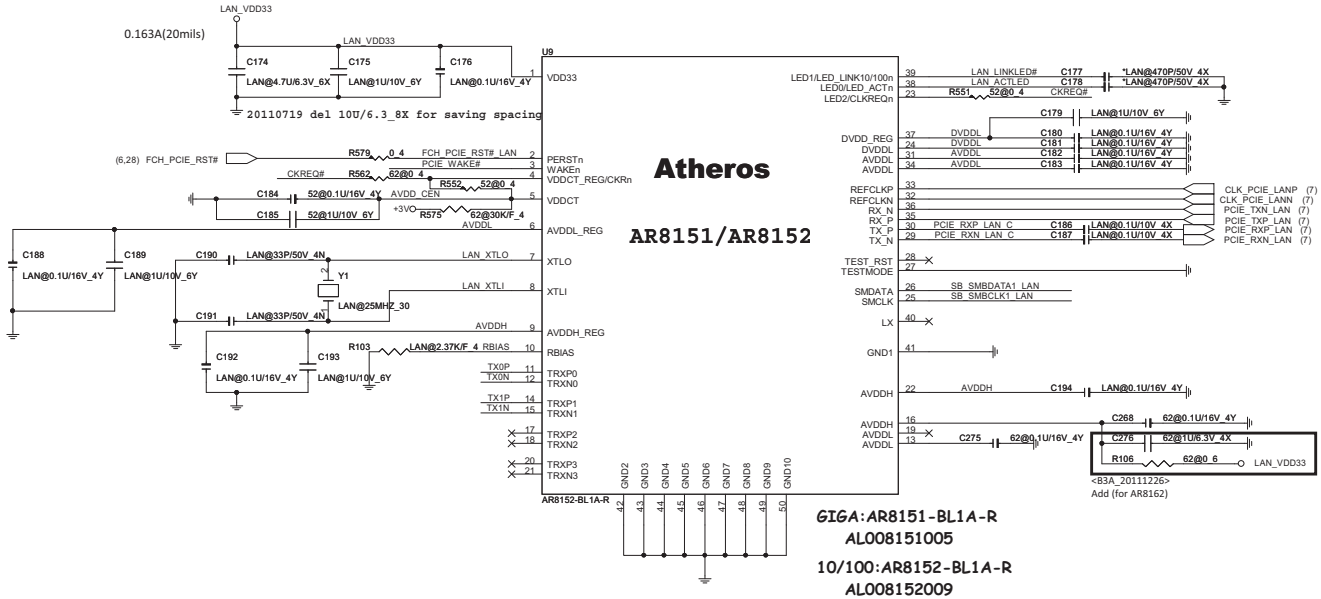
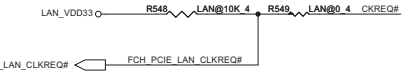
Atheros Lan <LAN> <LNG>

AR8152,AR8162 Co-Lay

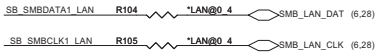


<LAN> <LNG> <LN1>

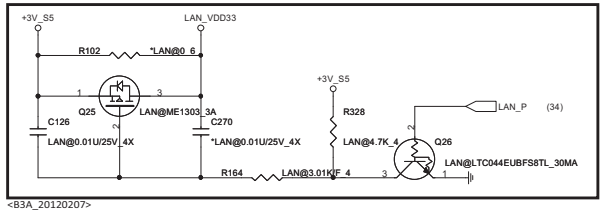


LAN-Wake up function <LAN>

LAN-SM-Bus <LAN>



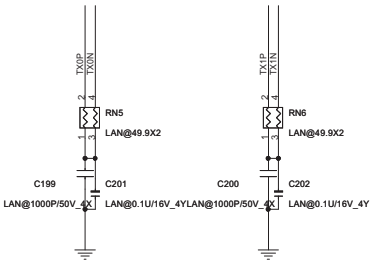
separate LAN power for RTC wakeup support on S5



<B3A_20120207>
stuff C126,Q25,R164,R328,Q26
unstuff R102

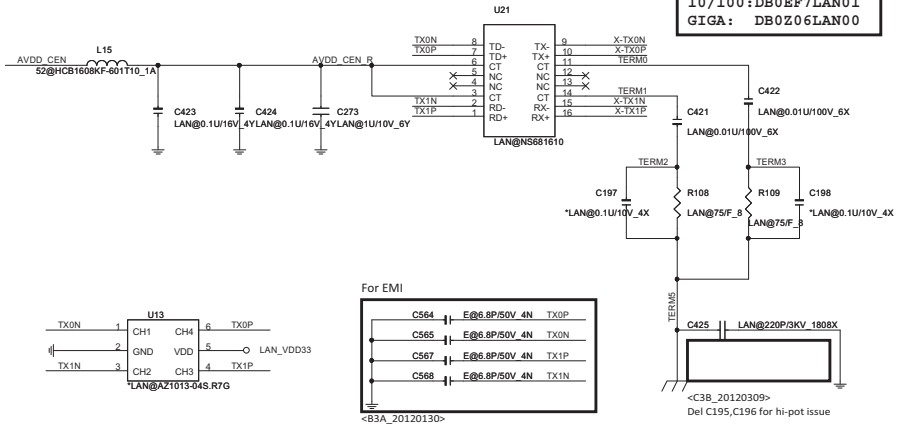
PLACE NEAR LAN IC SIDE

<LAN> <LNG>

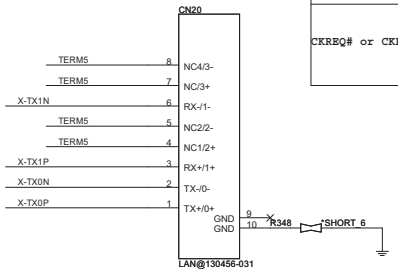


TRANSFORMER CONN <LAN> <LNG>

10/100:DB0EF7LAN01
GIGA: DB0Z06LAN00



RJ45 <LAN> <LNG> <LN1>



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Power on Strapping pin

LAN_ACTLED R110 LAN@5.1K/F_6

LAN_LINKLED# R111 LAN@5.1K/F_6

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Size	Document Number	Rev
	ATHEROS LAN (AR8152B)	1A

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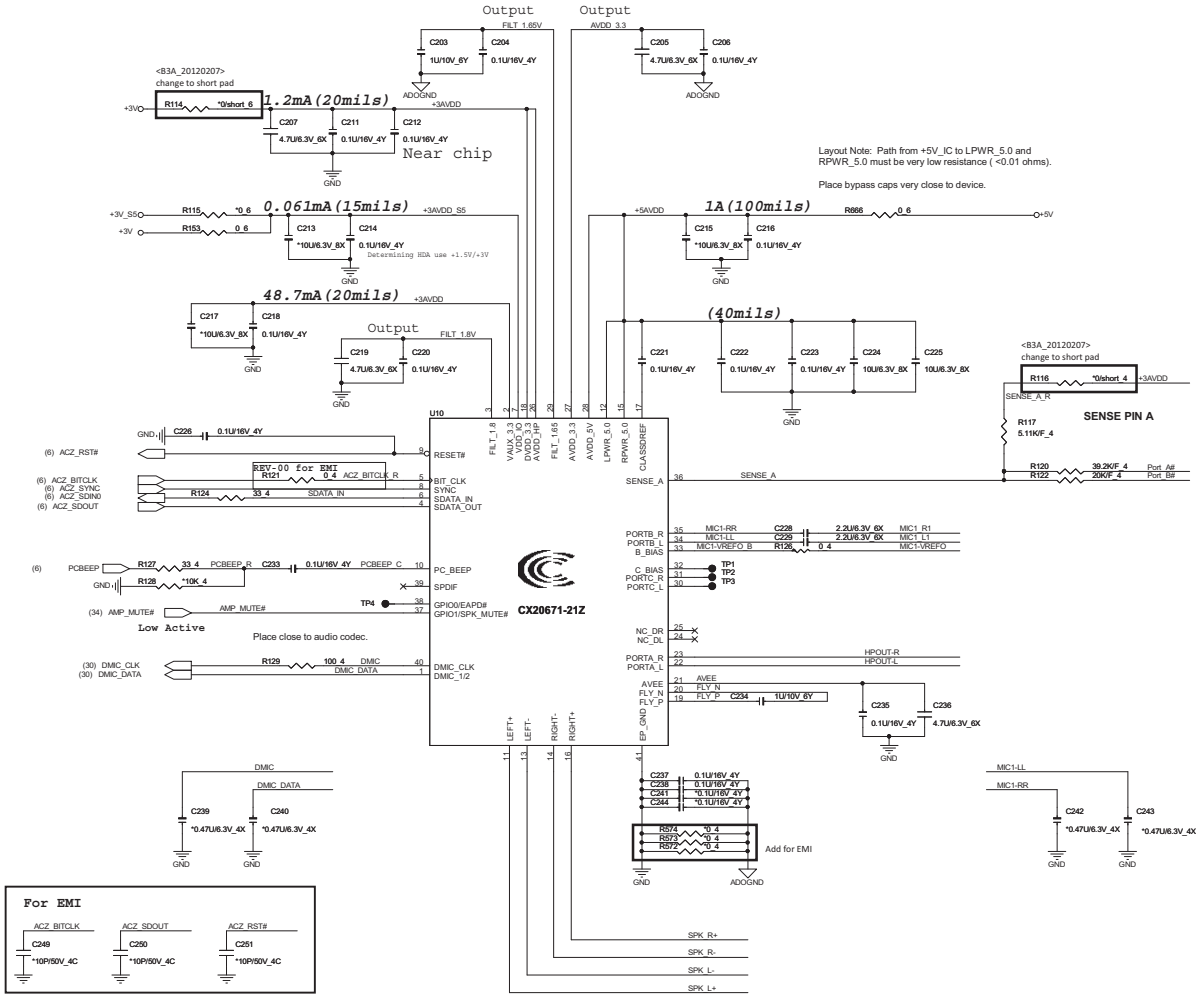
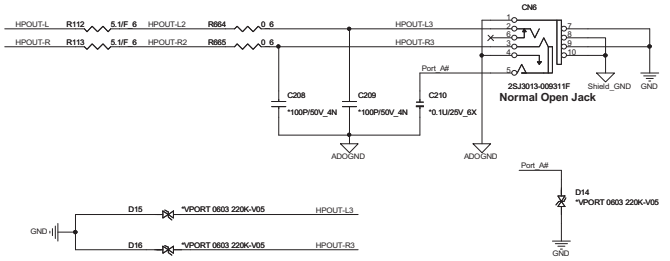
Codec (CX20671-21Z) <ADO> <EMI>

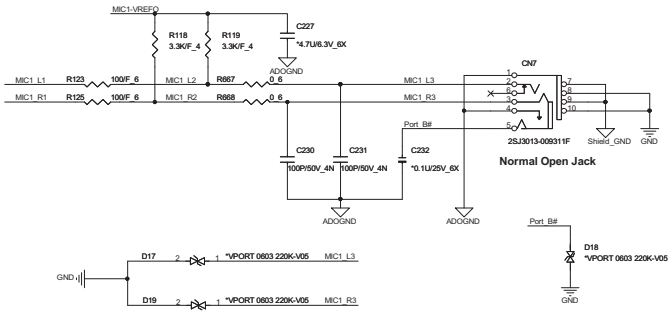


For EMI

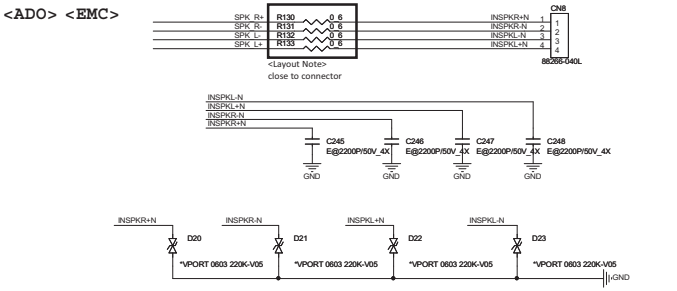
HP <ADO> <EMC>



External MIC <ADO> <EMC>



Internal Speaker <ADO> <EMC>



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Size	Document Number	Rev
	AUDIO CODEC (CX20671-21Z)	1A
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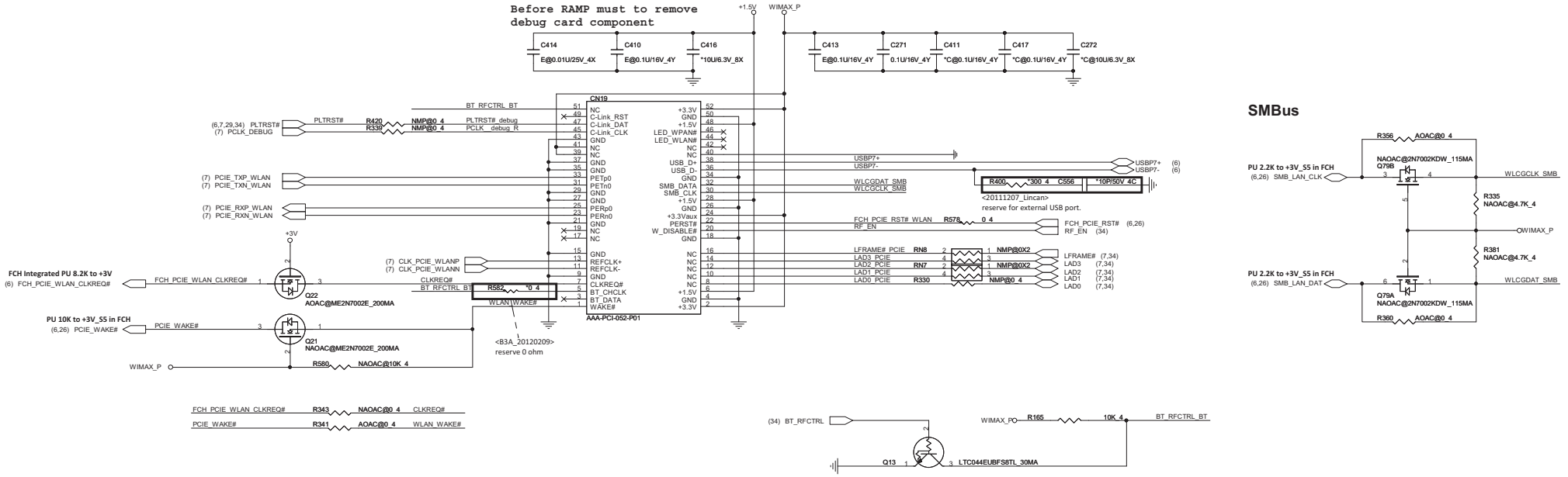
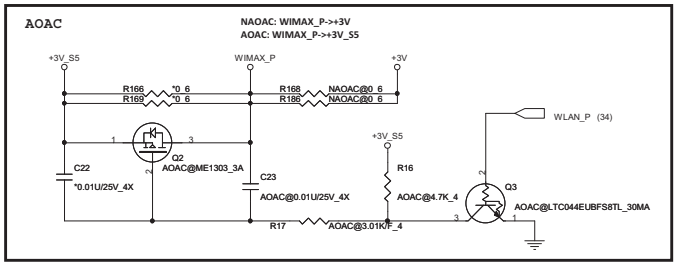


SMBus



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Size	Document Number: MINI CARD		Rev: 1A
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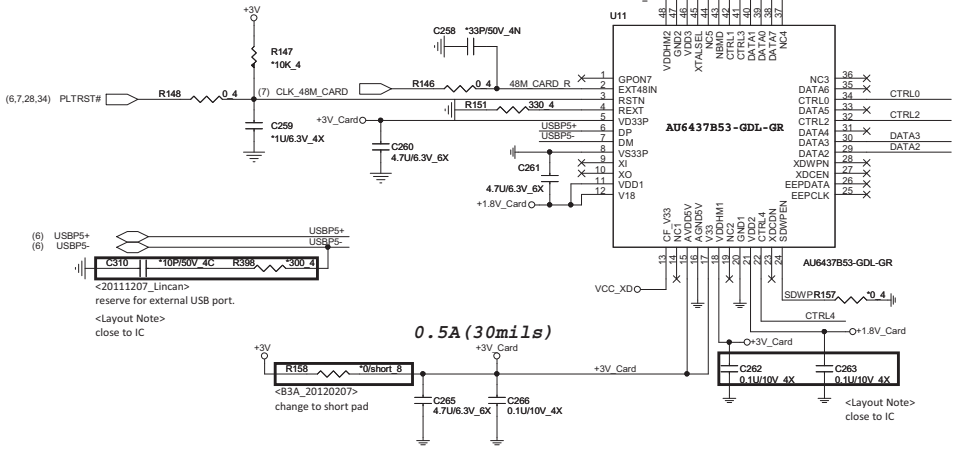
2 IN 1 CARD READER (Type: MMC/SD) <MMC>

Card Reader (AU6437B53-GDL-GR)



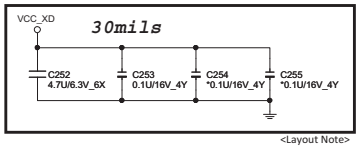
Clock input selection
1 : 48MHz input (default)
0 : 12MHz input

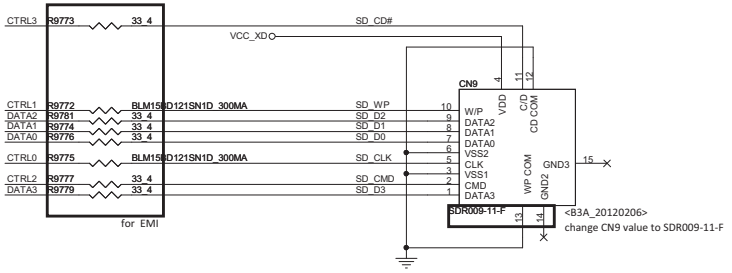
NBMD Power saving mode enable
1 : enable (default)
0 : disable

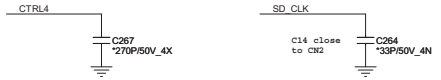
CTRL0 trace surround with GND

	SD	XD	MS
CTRL0	SDCLK	XDALE	MSBS
CTRL1	SDWP	XDCLE	MSCLK
CTRL2	SDCMD	XDRBD	
CTRL3	SDCDN	XDWRN	
CTRL4		XDRDN	MSINS

SD write protect enable
1 : decided by SDWP(default)
0 : SD always write-able







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	CARD READER	1A
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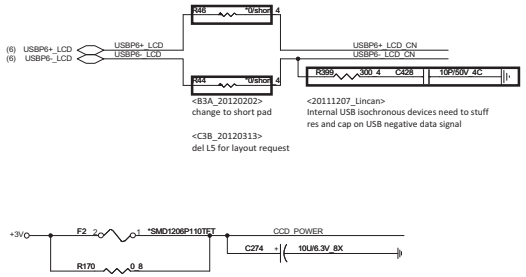
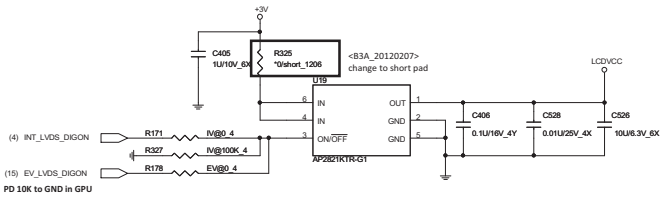
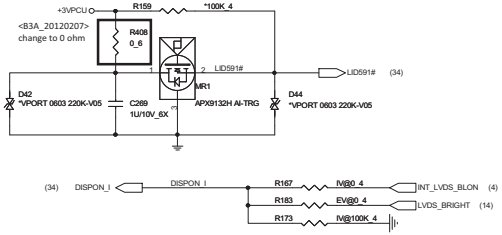
CCD [CCD]



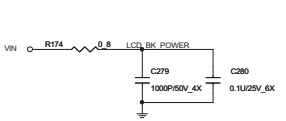
LCD POWER SWITCH <LDS>



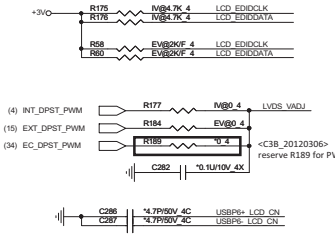
HALL SENSOR&BACK LIGHT SWITCH <HSR>

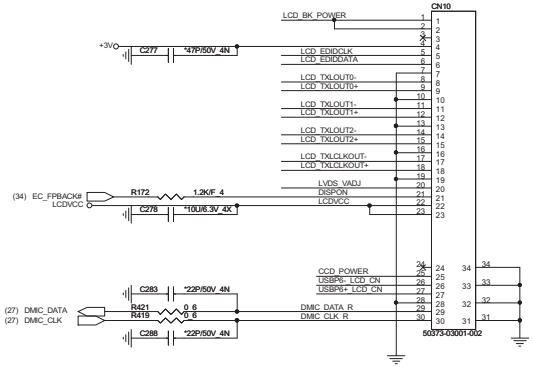


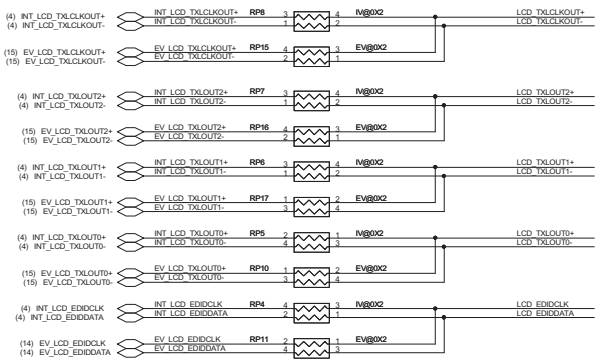
LCD Panel Module [LDS]

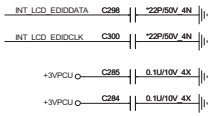


LVDS Enable

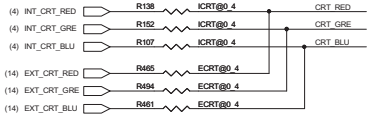


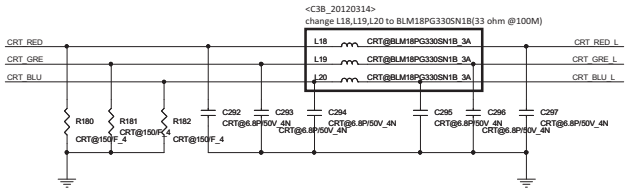


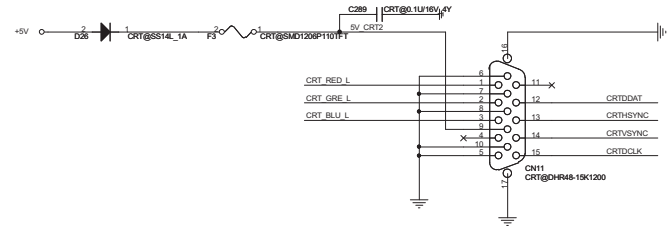


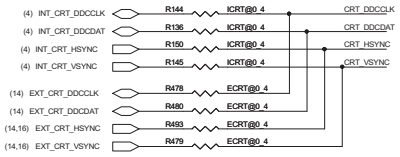


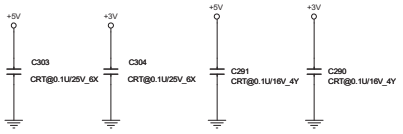
CRT [CRT]

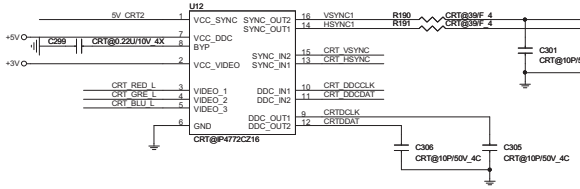


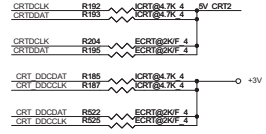












Quanta Computer Inc.
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	LVDS/CCD/DRT	1A
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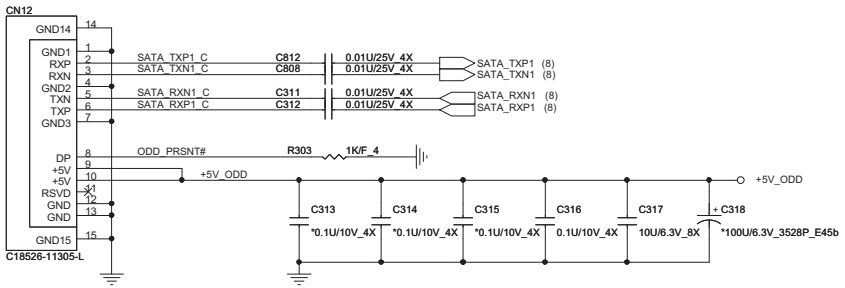
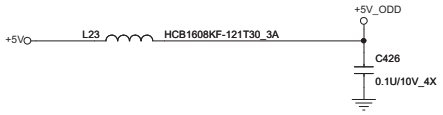
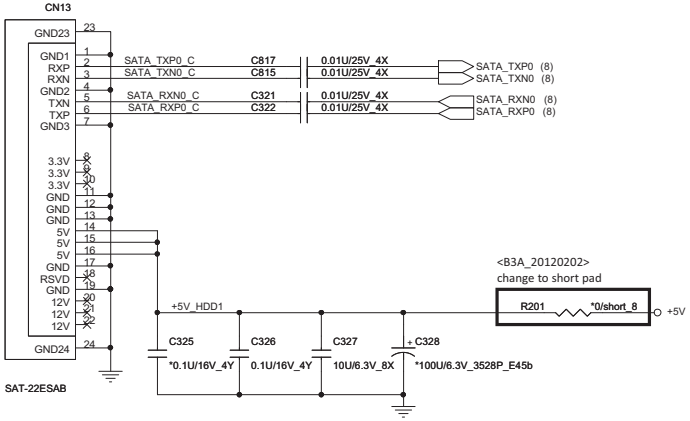
SATA ODD [ODD]



ODD Zero power [OZP]



SATA HDD [HDD]



Quanta Computer Inc.

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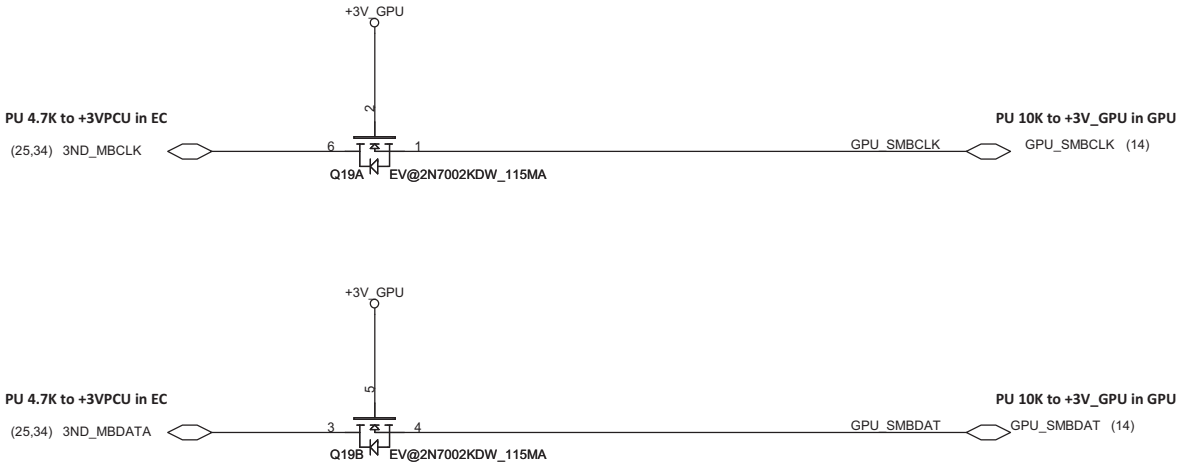
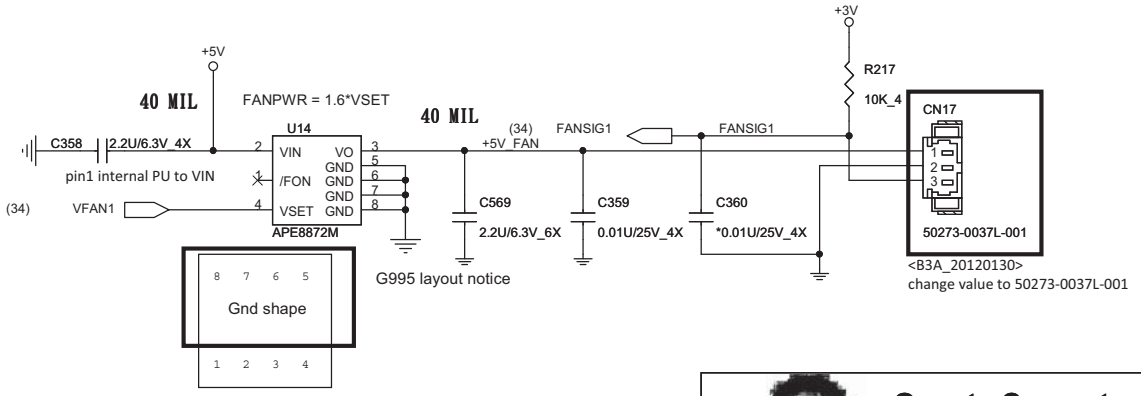
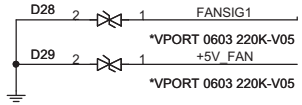
Thermal Sensor <THC>



Thermal	dGPU Int Thermal
EC(M) 3ND_SMB	
EC(M) 3ND_SMB	dGPU int SMBUS
dGPU(M) SMB	dGPU int SMBUS

FAN Control <THC>





Quanta Computer Inc.

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	THERMAL	1A

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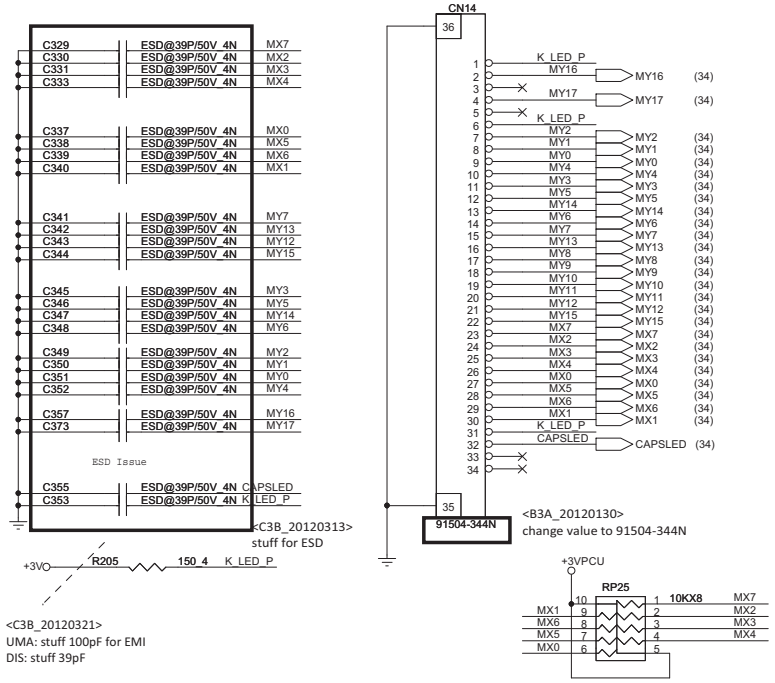
KEY BOARD Connector <KBC> <EMI>

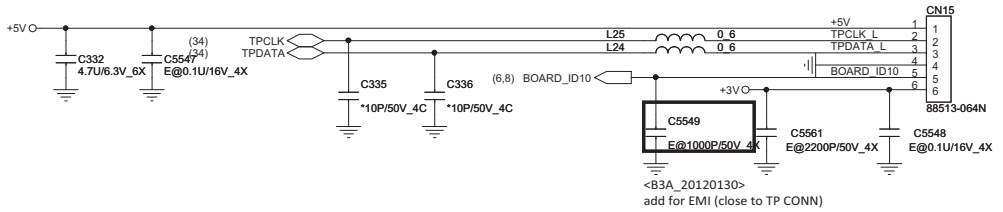


<C3B_20120313>
stuff for ESD

<B3A_20120130>
change value to 91504-344N

<C3B_20120321>
UMA: stuff 100pF for EMI
DIS: stuff 39pF

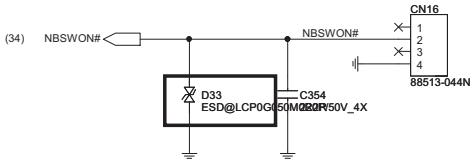
TOUCH PAD BOARD <TPD> <EMI>



<B3A_20120130>
add for EMI (close to TP CONN)

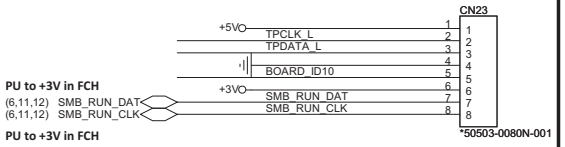
ID_Detect	default
Metal/IMR	H
TEXTURE	L

Power Board (UIF) <PSW>

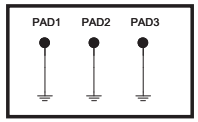


<C3B_20120316>
stuff ESD solution for power board

TP board <TPD>

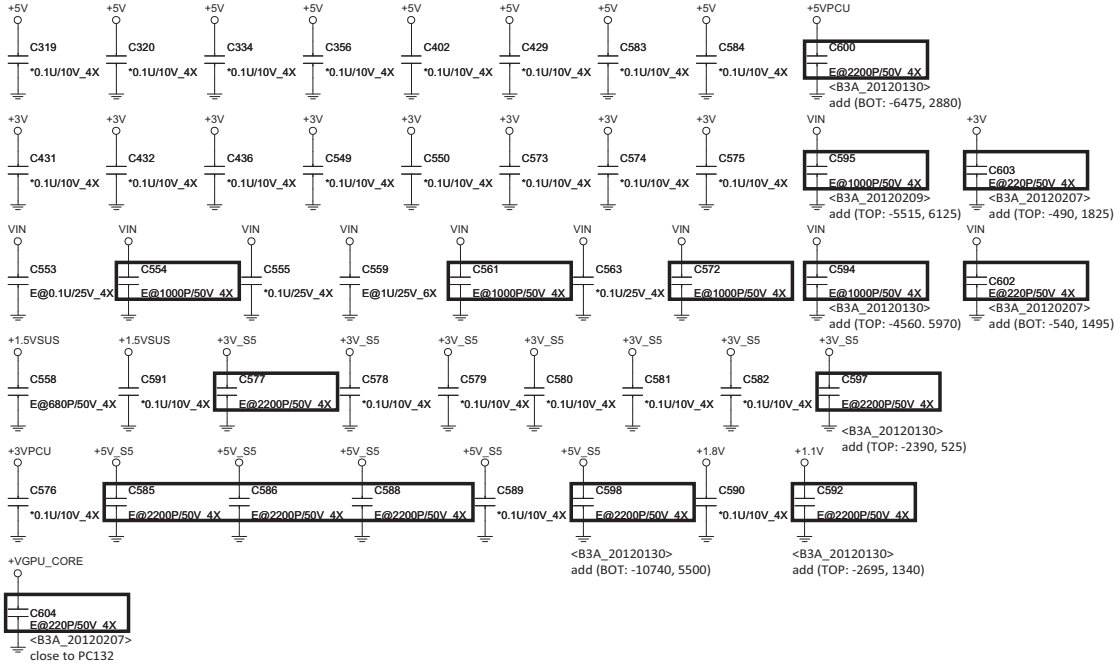


EMI Pad <OTH>

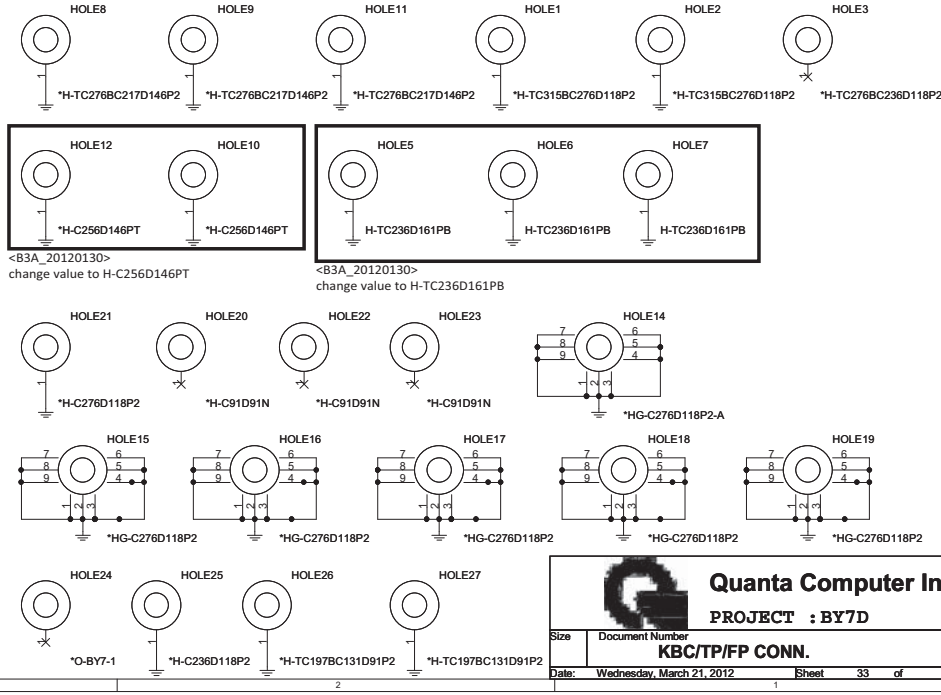


<C3B_20120312>
add Pad1 for EMI

EMI PAD <EMI>



HOLE <OTH>



<B3A_20120130>
change value to H-C256D146PT

<B3A_20120130>
change value to H-TC236D161PB

Quanta Computer Inc.
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	KBC/TP/FP CONN.	1A

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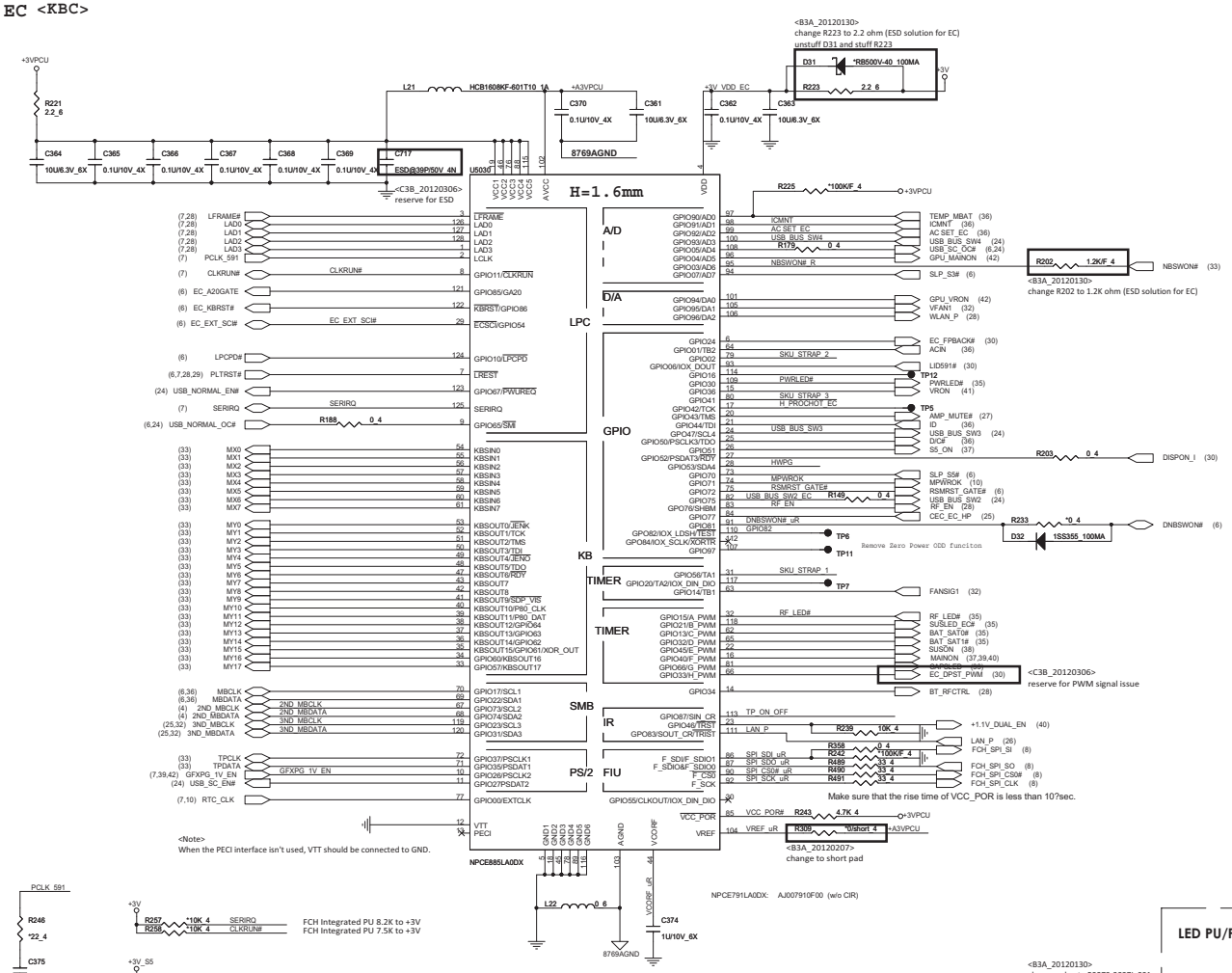
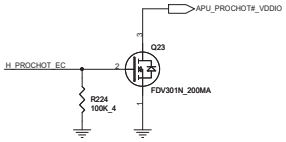
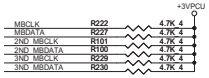
EC <KBC>



Intel Turbo mode only <CPU>



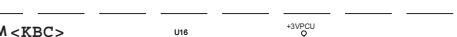
SM BUS PU <KBC>



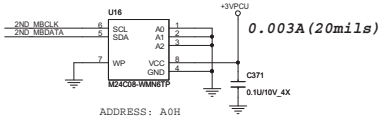
SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	3D Sensor	32H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H
	Touch Sensor	58H
	HDMI CEC	34H
	Light Sensor	52H

Strap <KBC> *SHBM*



ID EEPROM <KBC>

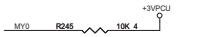


SPI FLASH <KBC>

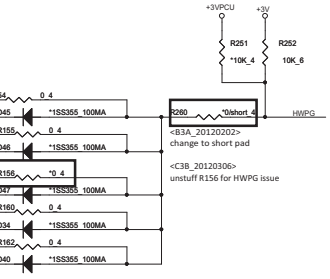
BY6-A1A Del SPI ROM

MX25L3205DM2I-12G: AKE39FP0Z00
W25Q16BVSSIG: AKE38FP0N01

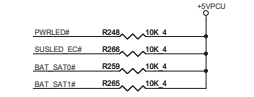
INTERNAL KEYBOARD STRIP SET <KBC>



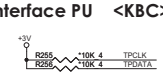
HWPG circuit <KBC>

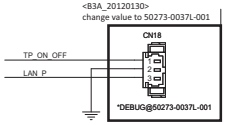


LED PU/PD <LED>



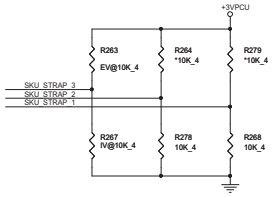
TP interface PU <KBC>



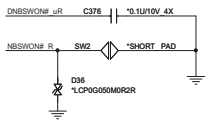


SKU strap pin <KBC>

SKU_STRAP_1(GPIO56)	SKU_STRAP_2(GPIO02)	SKU_STRAP_3(GPIO41)	SKU
0	0	0	Brazos UMA
0	0	1	Brazos DIS
0	1	0	COMAL UMA
0	1	1	COMAL DIS
1	0	0	Deccan UMA
1	0	1	Deccan DIS



Power Button <KBC>



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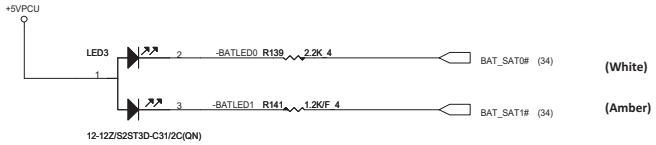
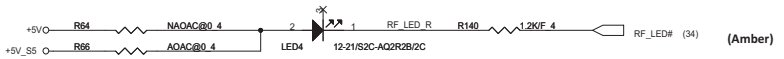
LED <LED>

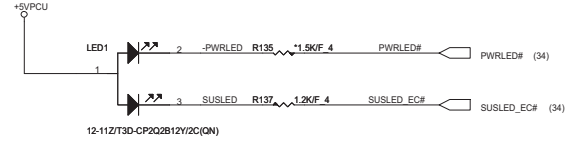
BATERRY



RF LED <LED>

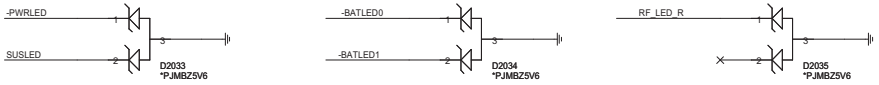


POWER <LED>



LED P/N	Behavior	res
BEWY0007ZA0 (White/Amber)	power on: White LED bright sleep: Amber LED blink	R135: stuff 1.5K R137: stuff 1.2K
BEWH0051Z00 (White)	power on: White LED bright sleep: White LED blink	R135: unstuff R137: stuff 1.5K

ESD Protect <ESD>



Quanta Computer Inc.

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Size	Document Number	Rev
	LED	1A

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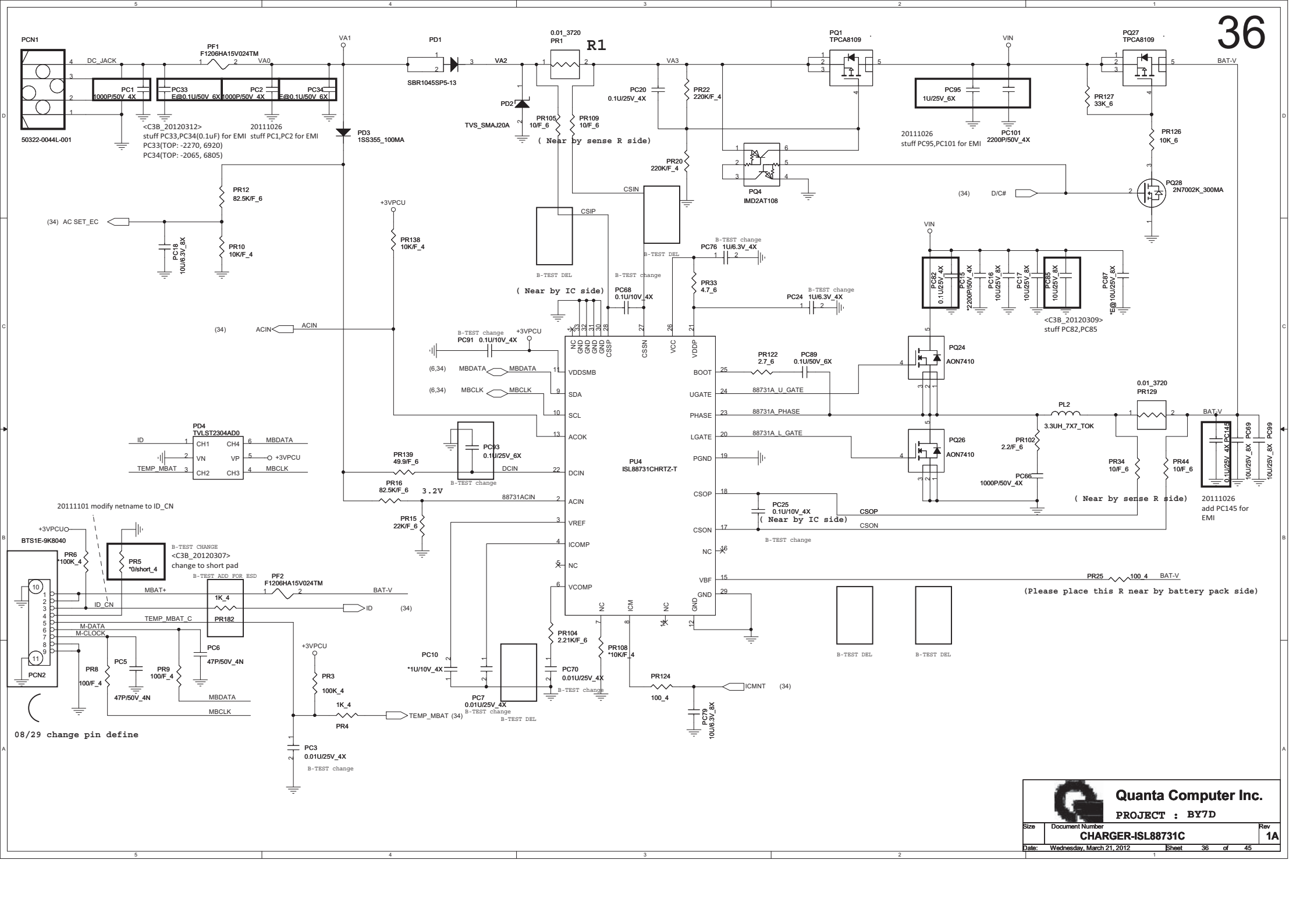
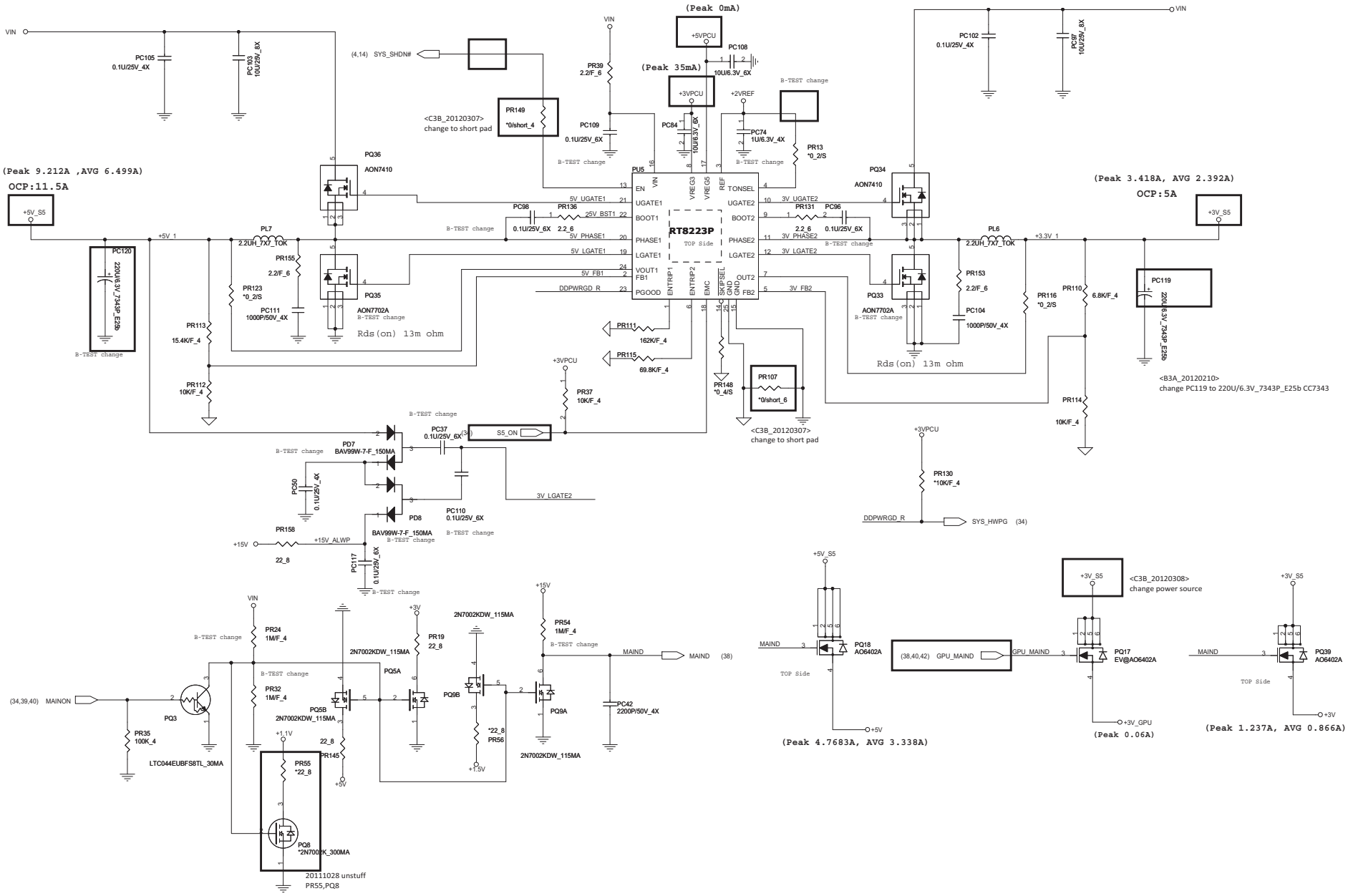
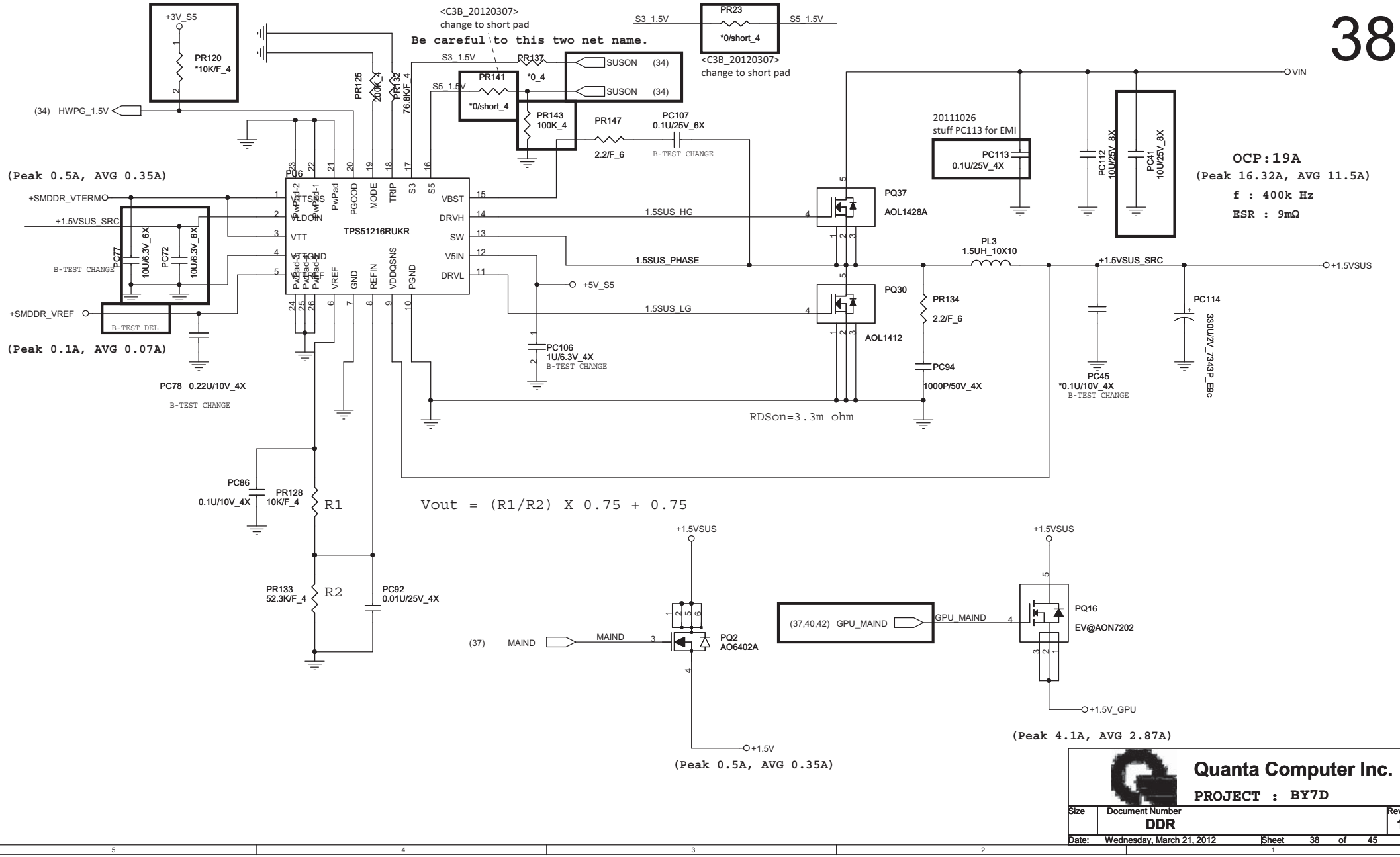


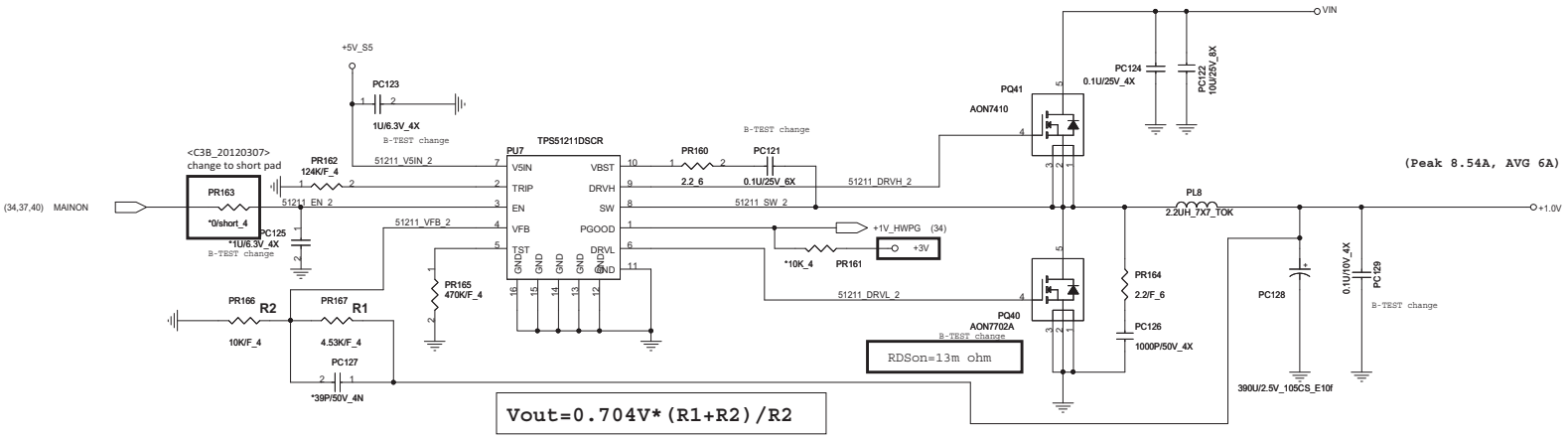
Quanta Computer Inc.		
PROJECT : BY7D		
Size	Document Number: CHARGER-ISL88731C	Rev: 1A
Date: Wednesday, March 21, 2012	Sheet 36 of 45	

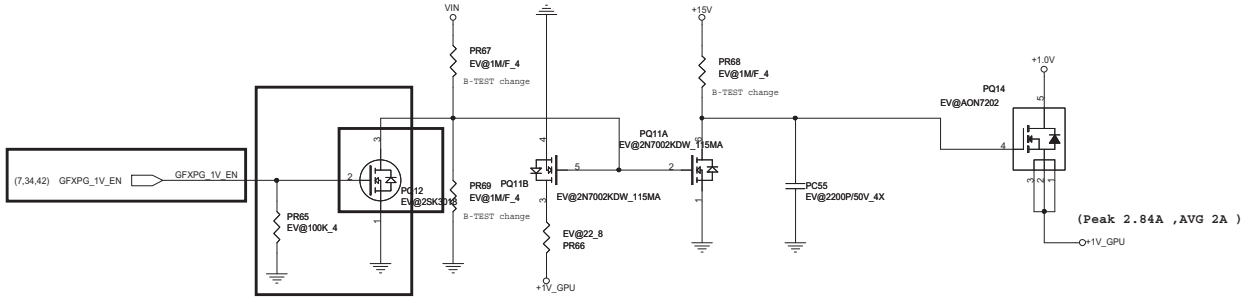


Quanta Computer Inc.		
PROJECT : BY7D		
Size	Document Number: System 3V/5V(TPS51123A)	Rev: 1A
Date: Wednesday, March 21, 2012	Sheet 37 of 45	



Quanta Computer Inc.		
PROJECT : BY7D		
Size	Document Number: DDR	Rev: 1A
Date: Wednesday, March 21, 2012	Sheet 38 of 45	





Quanta Computer Inc.		
PROJECT : BY7D		
Size	Document Number: +1.0V	Rev: 1A
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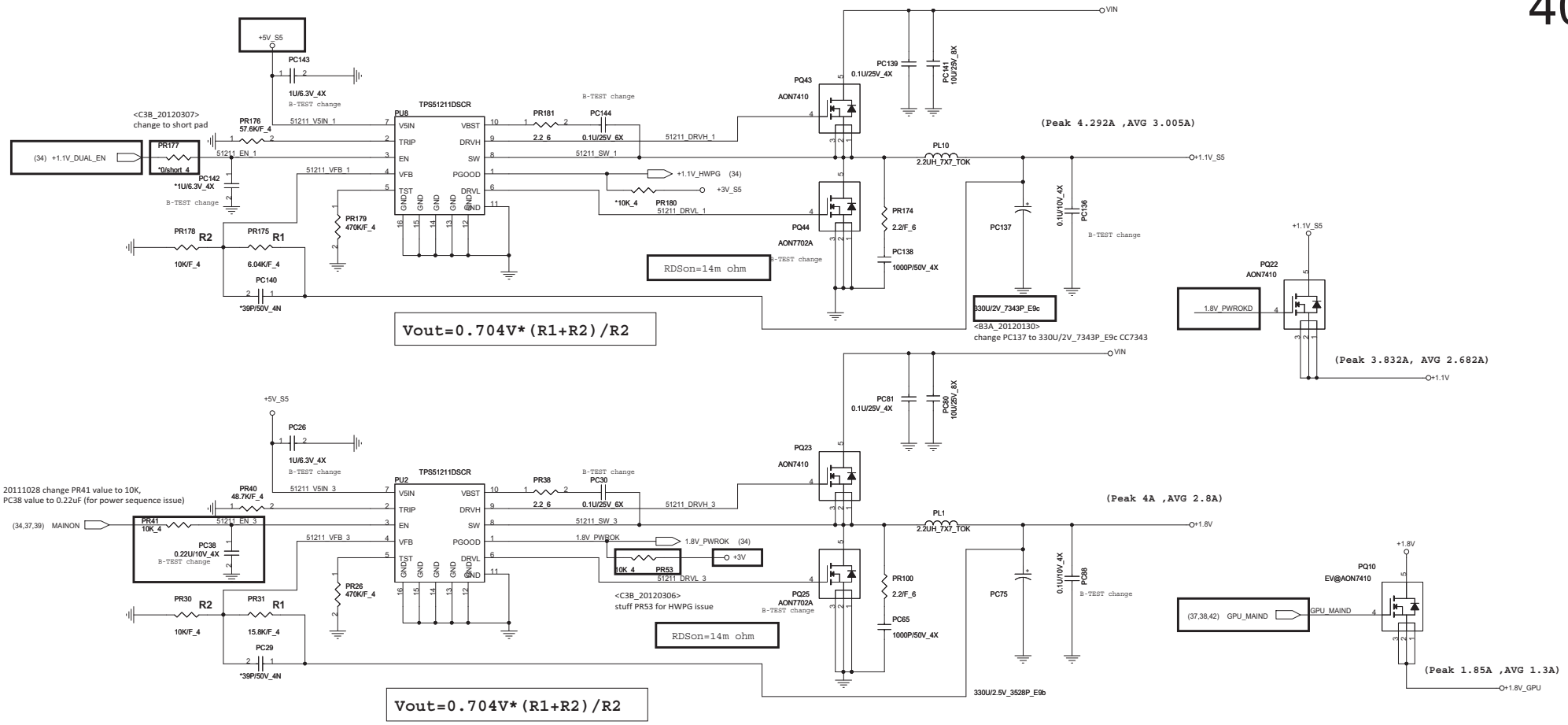

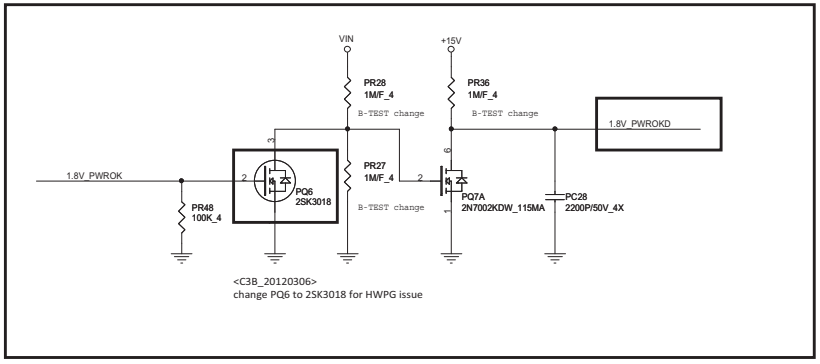

Quanta Computer Inc.		
PROJECT : BY7D		
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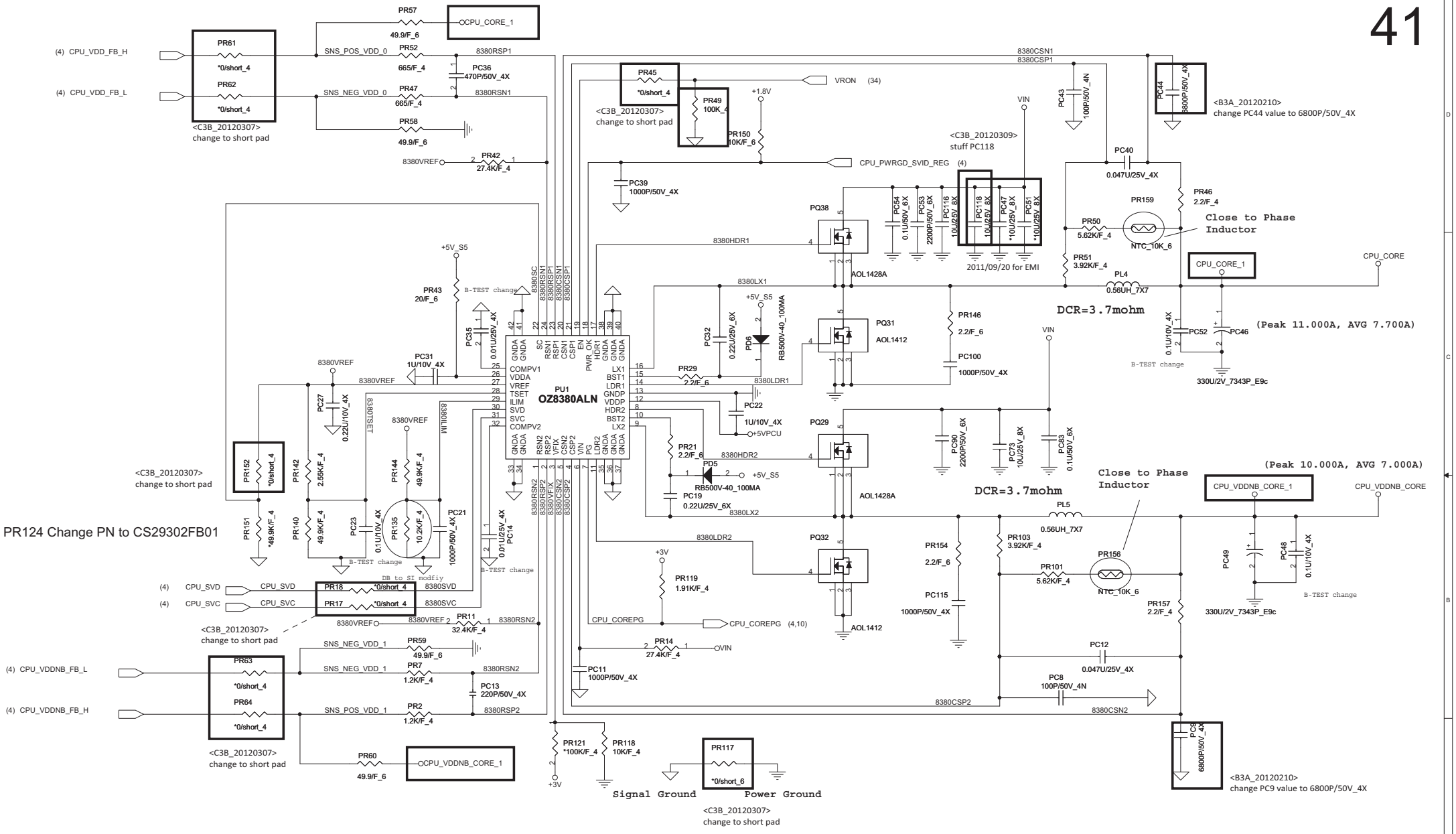

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	CPU CORE		1A
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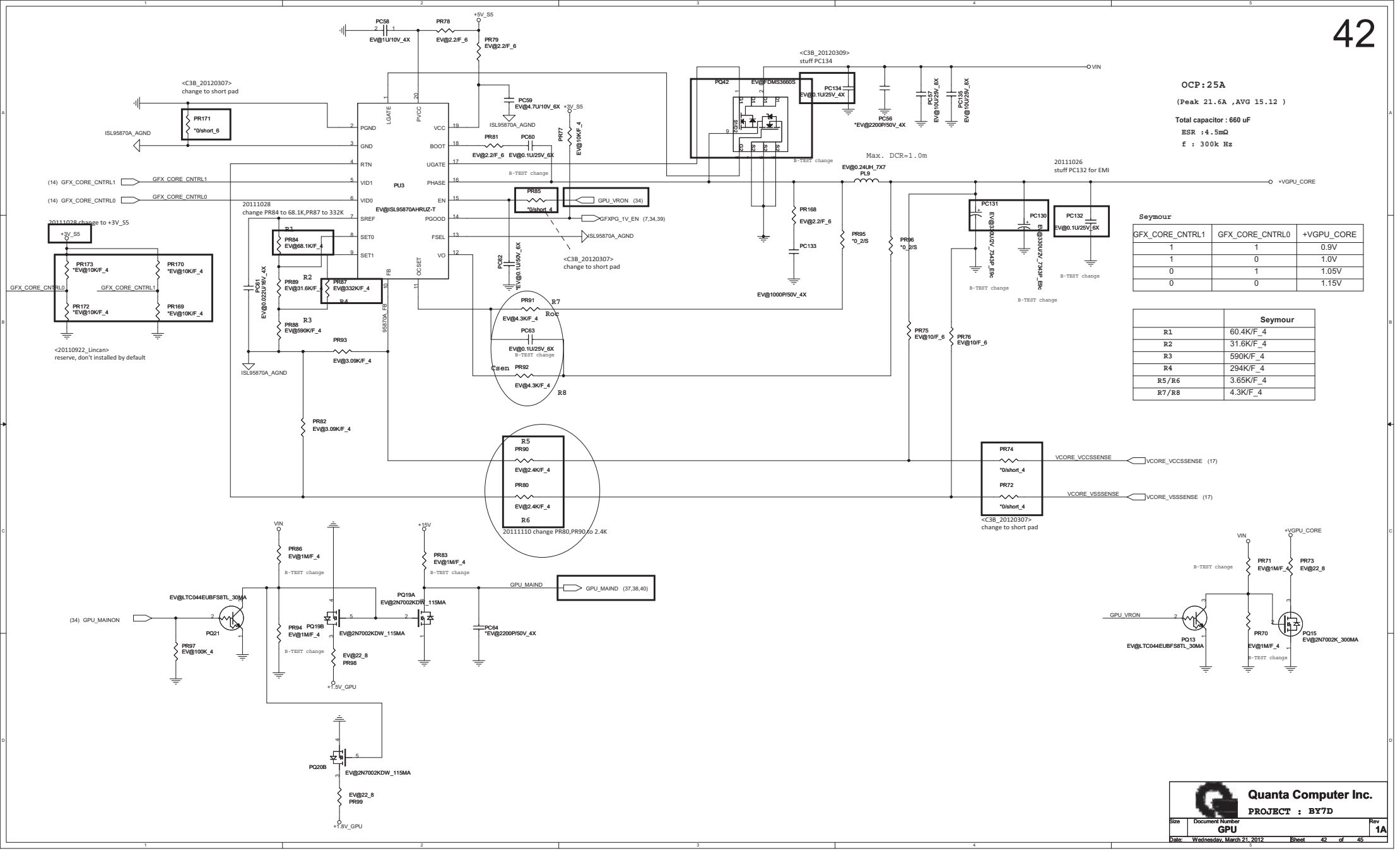

OCP:25A

(Peak 21.6A ,AVG 15.12)

Total capacitor : 660 uF
ESR :4.5mΩ
f : 300k Hz

Seymour

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	1.0V
0	1	1.05V
0	0	1.15V

	Seymour
R1	60.4K/F_4
R2	31.6K/F_4
R3	590K/F_4
R4	294K/F_4
R5/R6	3.65K/F_4
R7/R8	4.3K/F_4

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	GPU	1A

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