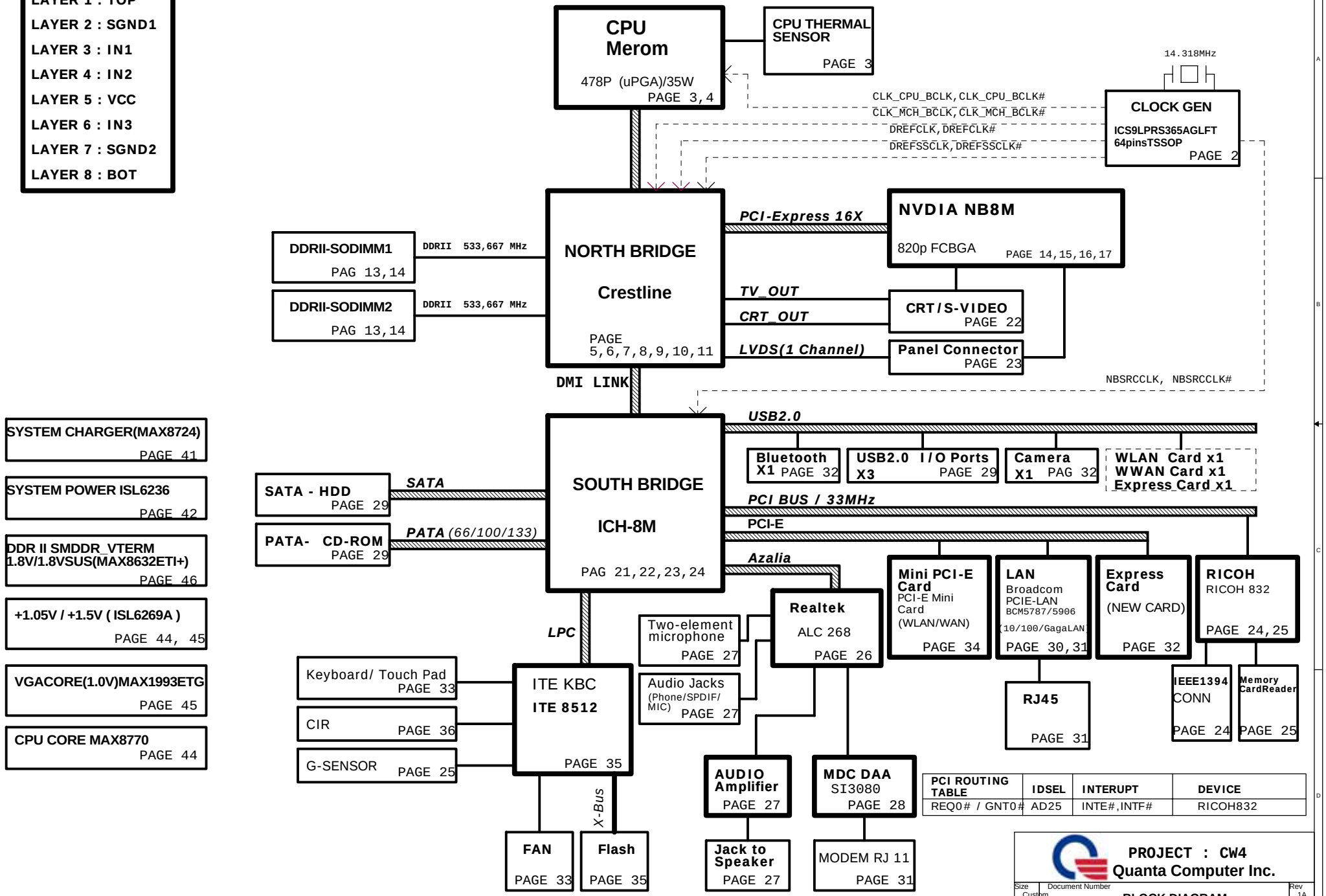
CW4 BLOCK DIAGRAM

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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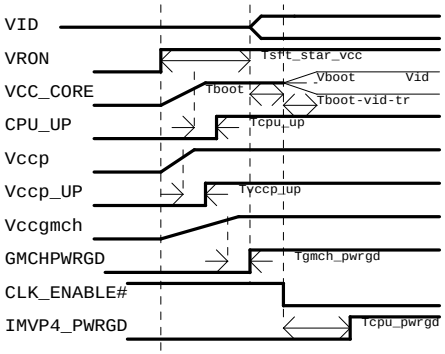
Board Stack up Description

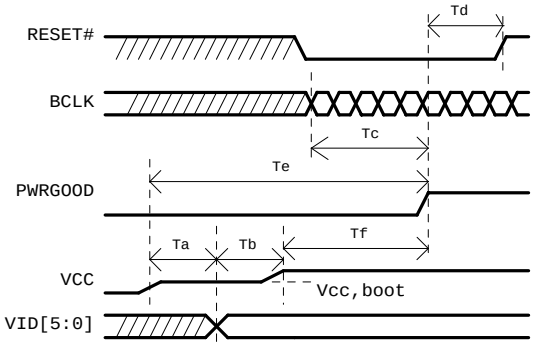
PCB Layers

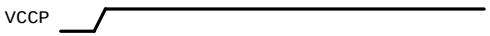
Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



YONAH Power-up Timing Specifications



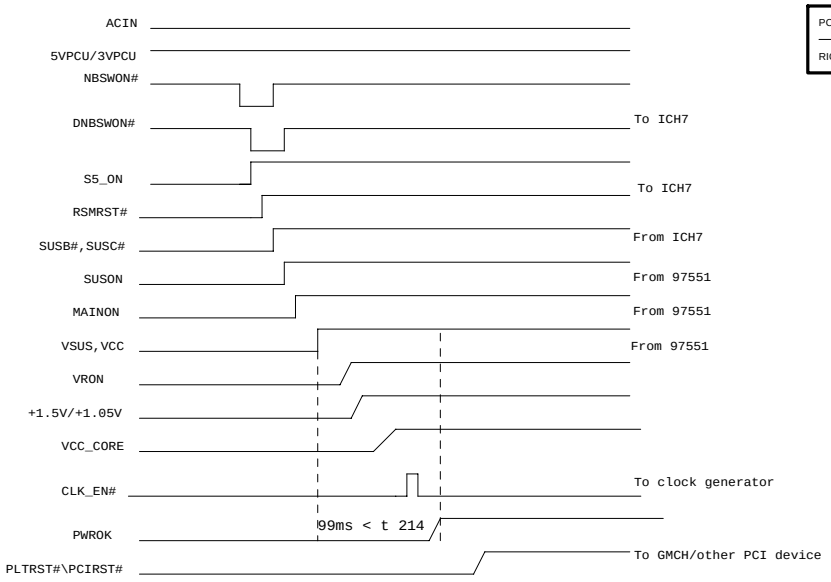


Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5/1.5V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.8VSUS	X	X			SUSON
SMDDR_VTERM/+2.5V/+3V/+5V/+12V	X				MAINON
+VCC_GFX_CORE/+1.2V_GFX_PCIE	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

ACIN POWER ON TIMING



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
RICOH832	AD25	REQ0# / GNT0#	INT E#/F#

PROJECT : CW4
Quanta Computer Inc.

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Custom	SYSTEM INFORMATION	1A

Date: Friday, November 03, 2006 Sheet 2 of 44

L36 HI0805R800R-00 +CK_VDD_MAIN
C396 22U/10V/12 C346 .1U/10V/04 C364 .1U/10V/04 C378 .1U/10V/04 C372 .1U/10V/04 C389 .1U/10V/04

L35 HI0805R800R-00 VDDCPU
C377 22U/10V/12 C375 .1U/10V/04

L34 HI0805R800R-00 +CK_VDD_MAIN2
C350 22U/10V/12 C361 .1U/10V/04 C338 .1U/10V/04 C368 .1U/10V/04 C348 .1U/10V/04 C359 .1U/10V/04 C363 .1U/10V/04

Y2 14.318MHZ
CG_XIN — C391 27P/50V/04
CG_XOUT — C392 27P/50V/04

CLK_3GPLLREQ# R171 10K/04
NEW-CARD_CLK_REQ# R167 10K/04
PCIE_LANREQ# R232 10K/04

internal have already build-in 33ohm damping resistor

U7 CK505

+CK_VDD_MAIN	16	VDDPLL3	
	9	VDD48	
	2	VDDPCI	
	61	VDDREF	
	39	VDDSRC	
VDDCPU	55	VDDCPU	
+CK_VDD_MAIN2	12	VDD96I/O	
	20	VDDPLL3I/O	
	26	VDDSRCI/O	
	45	VDDSRCI/O	
	36	VDDSRCI/O	
	49	VDDCPU_IO	
	48	NC	
CG_XIN	60	X1	
CG_XOUT	59	X2	
21 CK_PWG	56	CK_PWRGD/PD#	
CLK_BSEL1 R223 0 FSB	57	FSLB/TEST_MODE	
14,35 CGCLK_SMB	64	SCLK	
14,35 CGDAT_SMB	63	SDATA	
	15	GND	
	19	GND	
	11	GND48	
	52	GNDCPU	
	8	GNDPCI	
	58	GNDREF	
	23	GNDSRC	
	29	GNDSRC	
	42	GNDSRC	

CPUCLKT0	54	RHCLK_CPU	RP49 4 3 1 2 4P2R-S-0 CLK_CPU_BCLK 4
CPUCLKC0	53	RHCLK_CPU#	CLK_CPU_BCLK# 4
CPUCLKT1	51	RHCLK_MCH	RP47 4 3 1 2 4P2R-S-0 CLK_MCH_BCLK 6
CPUCLKC1	50	RHCLK_MCH#	CLK_MCH_BCLK# 6
CPUT2_ITP/SRCT8	47	CPU_ITP	RP45 4 3 1 2 *4P2R-S-0 CLK_CPU_ITP T68
CPUT2_ITP/SRCC8	46	CPU_ITP#	CLK_CPU_ITP# T69
DOTT_96/SRCT0	13	R_DOT96	RP48 2 1 4 3 4P2R-S-0 DREFCLK 7
DOTC_96/SRCC0	14	R_DOT96#	DREFCLK# 7
27MHz_Nonss/SRCCLK1/SE1	17	R_DREFSSCLK	RP46 2 1 4 3 *4P2R-S-0 DREFSSCLK 7
27Mhz_ss/SRCCLC1/SE2	18	R_DREFSSCLK#	DREFSSCLK# 7
SRCCLKT2/SATACL	21	RSRC_SATA	RP43 2 1 4 3 4P2R-S-0 CLK_PCIE_SATA 19
SRCCLKC2/SATACL	22	RSRC_SATA#	CLK_PCIE_SATA# 19
SRCCLKT3/CR#_C	24	R_CLK_PCIE_VGA	RP41 2 1 4 3 4P2R-S-0 CLK_PCIE_VGA 15
SRCCLKC3/CR#_D	25	R_CLK_PCIE_VGA#	CLK_PCIE_VGA# 15
SRCCLKT4	27	RSRC1_LAN	RP39 2 1 4 3 4P2R-S-0 CLK_PCIE_LAN 31
SRCCLKC4	28	RSRC1_LAN#	CLK_PCIE_LAN# 31
PCI_STOP#	38	PM_STPPCI#	PM_STPPCI# 21
CPU_STOP#	37	PM_STPCPU#	PM_STPCPU# 21
SRCCLKT6	41	RSRC_ICH	RP40 4 3 1 2 4P2R-S-0 CLK_PCIE_ICH 20
SRCCLKC6	40	RSRC_ICH#	CLK_PCIE_ICH# 20
SRCCLKT7/CR#_F	44	CLK_PCIE_MINI	RP42 4 3 1 2 4P2R-S-0 CLK_PCIE_MINI 35
SRCCLKC7/CR#_E	43	CLK_PCIE_MINI_#	CLK_PCIE_MINI# 35
SRCCLKT9	30	RSRC_MCH	RP37 2 1 4 3 4P2R-S-0 CLK_PCIE_3GPLL 7
SRCCLKC9	31	RSRC_MCH#	CLK_PCIE_3GPLL# 7
SRCCLKT10	34	CLK_PCIE_NEW	RP38 2 1 4 3 4P2R-S-0 CLK_PCIE_NEW_C 33
SRCCLKC10	35	CLK_PCIE_NEW#	CLK_PCIE_NEW_C# 33
SRCCLKT11/CR#_H	33	NEW-CARD_CLK_REQ#_R	R168 475/F/03 NEW-CARD_CLK_REQ# NEW-CARD_CLK_REQ# 33
SRCCLKC11/CR#_G	32	CLK_3GPLLREQ#_R	R164 475/F/03 CLK_3GPLLREQ# CLK_3GPLLREQ# 7
PCICLK0/CR#_A	1	R_PCLK_8512	R239 33/04 PCLK_LPC_8512 36
PCICLK1/CR#_B	3		R236 475/F/03 PCIE_LANREQ# 31
PCICLK2/TME	4	PCLK_MINI_LPC	R219 33/04 PCLK_LPC_DEBUG 35
PCICLK3	5	PCI_ICH	T71
PCICLK4/27_SELECT	6	FCTSEL1	R233 33/04 PCI_CLK_5C832 25
PCI_F5/ITP_EN	7	ITP_EN	R206 33/04 PCLK_ICH 20
USB_48MHZ/FSLA	10	FSA	R204 33/04 CLKUSB_48 21
		FSC	R200 4.7K/04 CLK_BSEL0
			R225 4.7K/04 CLK_BSEL2
FSLC/TST_SL/REF	62		R228 33/04 14M_ICH 21

ICS9LPRS365BGLFT/SLG8SP512T

+3V R215 10K/04 PCLK_MINI_LPC R218 *4.7K/04

0=overclocking of CPU and SRC Allowed

1 = overclocking of CPU and SRC not Allowed

Q20 2N7002E/CH2507SPT R241 10K R242 10K
21,33 PDAT_SMB — CGDAT_SMB

Q19 2N7002E/CH2507SPT
21,33 PCLK_SMB — CGCLK_SMB

+3V R208 10K/04 FCTSEL1 R205 *10K/04

0=UMA
1 = External VGA

Disable ITP
10K/04 R216 ITP_EN

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CPU Clock select

4 CPU_BSEL0 — R194 0/04 CLK_BSEL0 R196 0/04 MCH_BSEL0 7
+1.05V — R197 *56/04 R198 1K/04
4 CPU_BSEL1 — R230 0/04 CLK_BSEL1 R224 0/04 MCH_BSEL1 7
+1.05V — R231 *0/04 R226 1K/04
4 CPU_BSEL2 — R240 0/04 CLK_BSEL2 R234 0/04 MCH_BSEL2 7
+1.05V — R238 *0/04 R237 1K/04

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

C395 *33P/50V/04 PCLK_LPC_8512
C394 *33P/50V/04 PCI_CLK_5C832
C369 *33P/50V/04 PCLK_ICH
C384 *33P/50V/04 PCLK_LPC_DEBUG
C367 *33P/50V/04 CLKUSB_48
C390 *33P/50V/04 14M_ICH
for EMI

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

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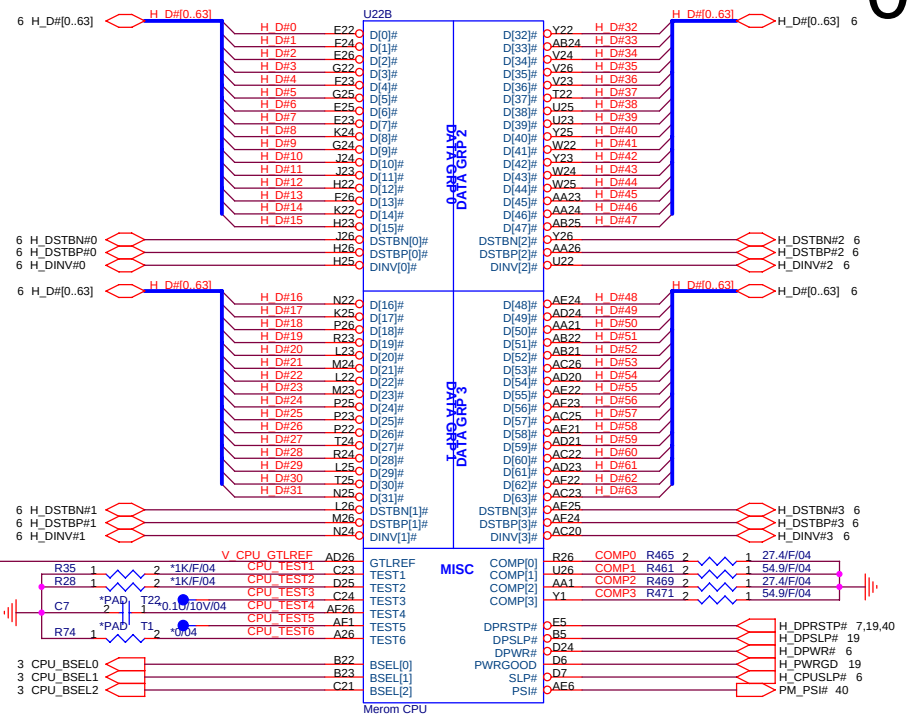
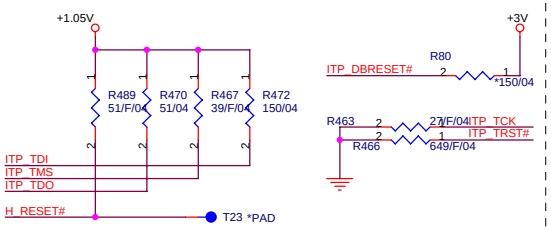
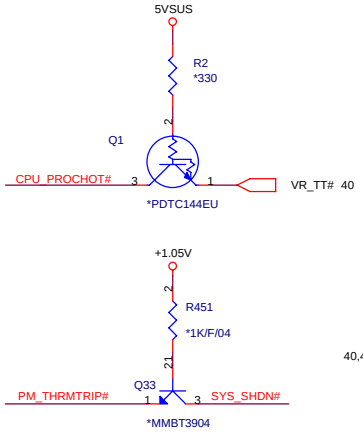
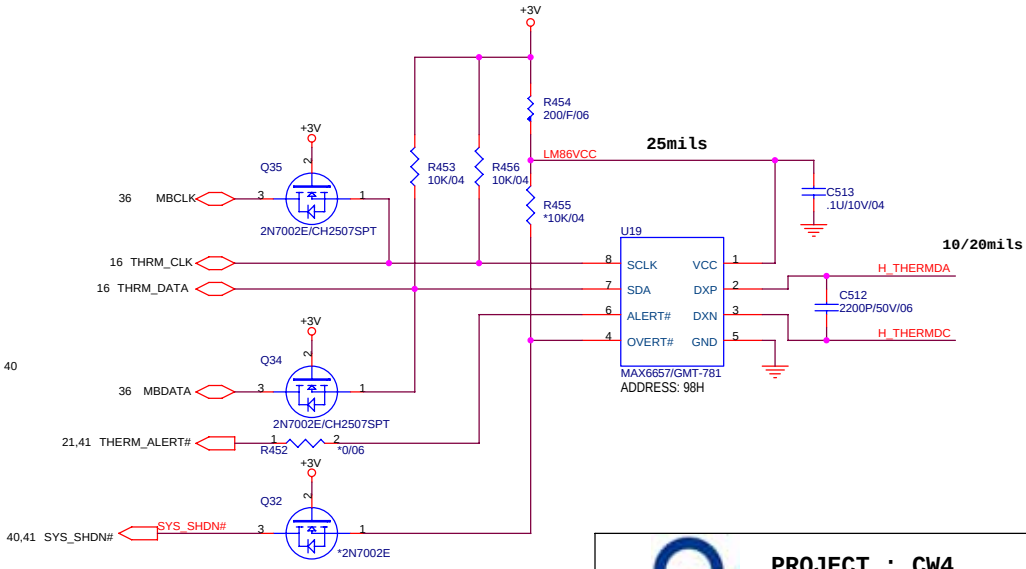
Layout Note:
Place voltage divider within 0.5" of GTLREF pin



Populate ITP700Flex for bringup







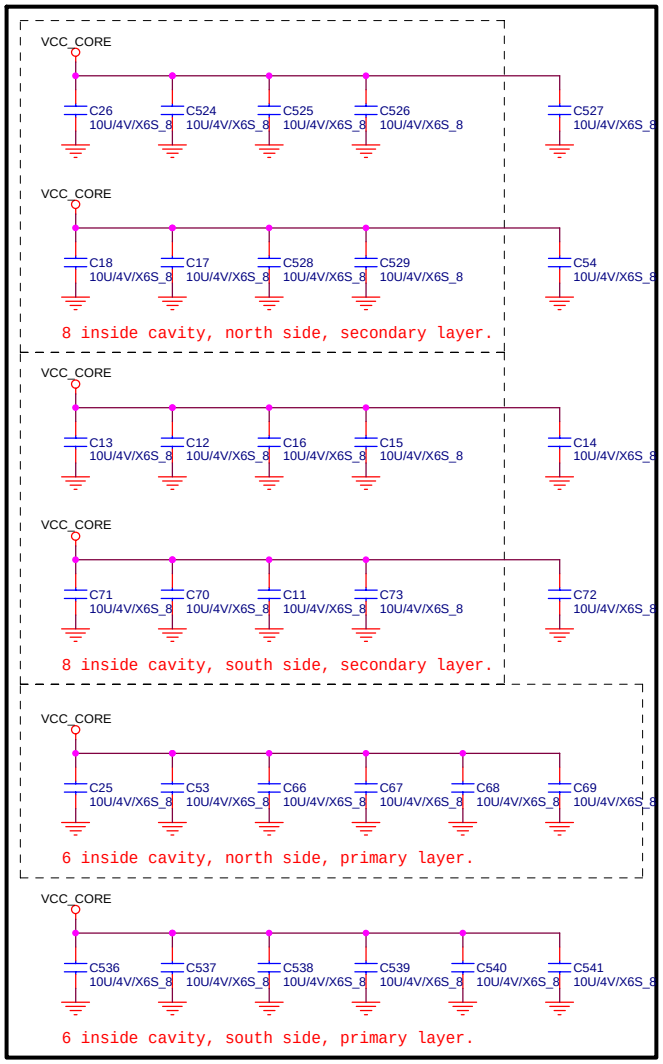
ITP disable guidelines

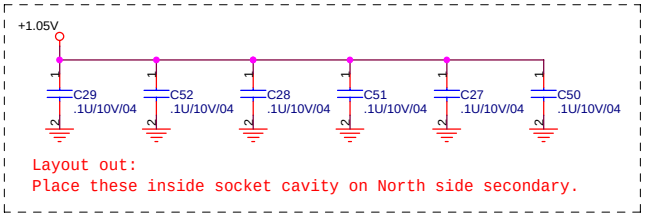
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom (HOST BUS)	1A

Date: Friday, November 03, 2006 Sheet 4 of 44

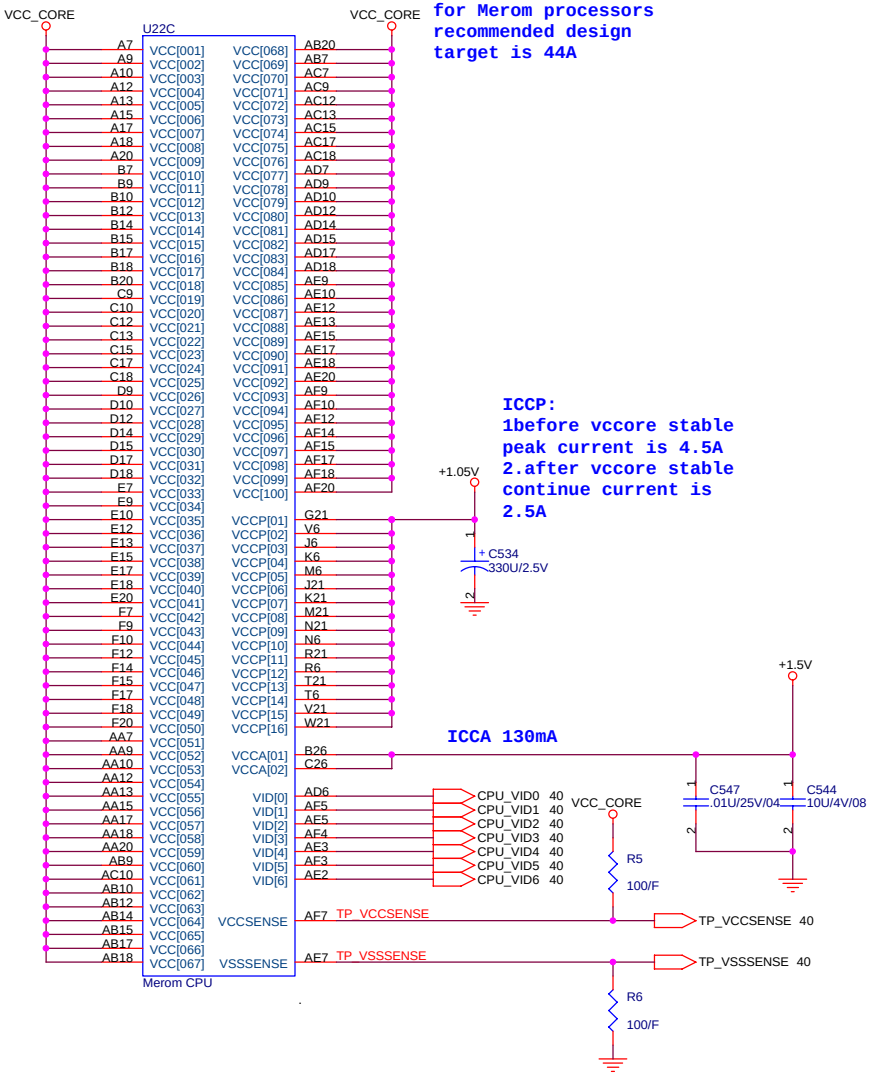


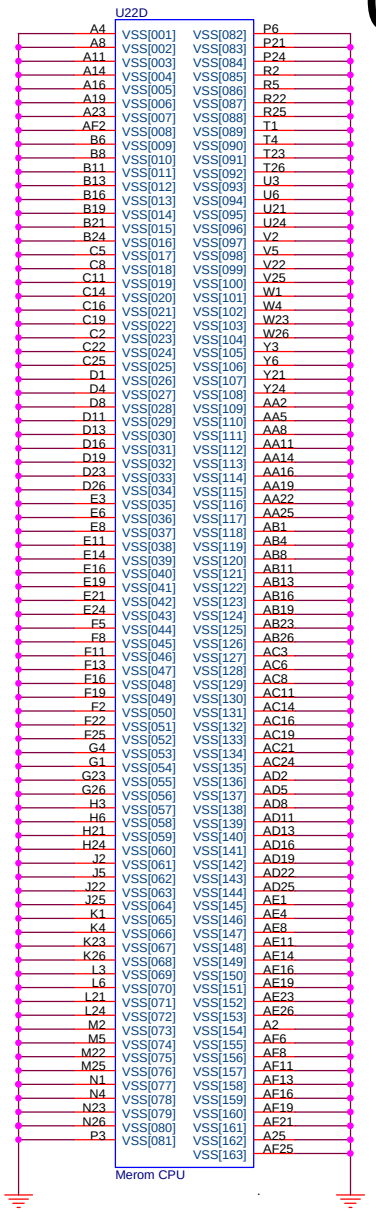


ICCODE:
for Merom processors
recommended design
target is 44A

ICCP:
1before vccore stable
peak current is 4.5A
2.after vccore stable
continue current is
2.5A

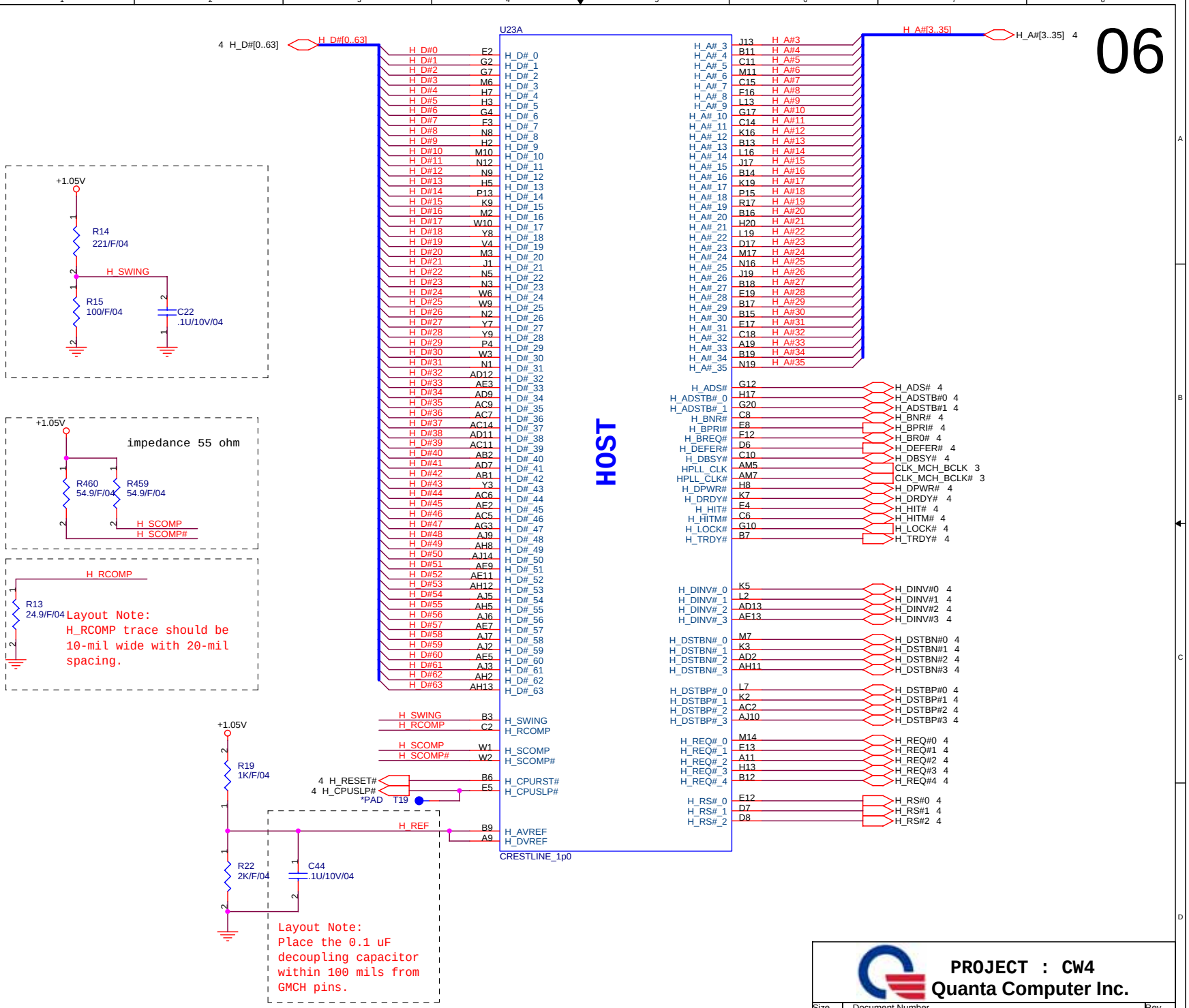
ICCA 130mA





PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom (POWER/NC)	1A
Date: Friday, November 03, 2006	Sheet 5 of 44	


06
U23A
HOST
CRESTLINE_1p0
4 H_D#[0..63]
H_D#[0..63]
H_A#[3..35]
H_A#[3..35] 4
+1.05V
R14
221/F/04
H_SWING
R15
100/F/04
C22
.1U/10V/04
+1.05V
impedance 55 ohm
R460
54.9/F/04
R459
54.9/F/04
H_SCOMP
H_SCOMP#
H_RCOMP
R13
24.9/F/04
Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.
+1.05V
R19
1K/F/04
R22
2K/F/04
C44
.1U/10V/04
H_REF
Layout Note:
Place the 0.1 uF
decoupling capacitor
within 100 mils from
GMCH pins.
4 H_RESET#
4 H_CPUSLP#
*PAD T19
PROJECT : CW4
Quanta Computer Inc.
Size Custom
Document Number
Crestline_A (HOST)
Rev 1A
Date: Friday, November 03, 2006
Sheet 6 of 44

WW22 update
--- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

CRESTLINE_1p0

CRT Discrete / UMA

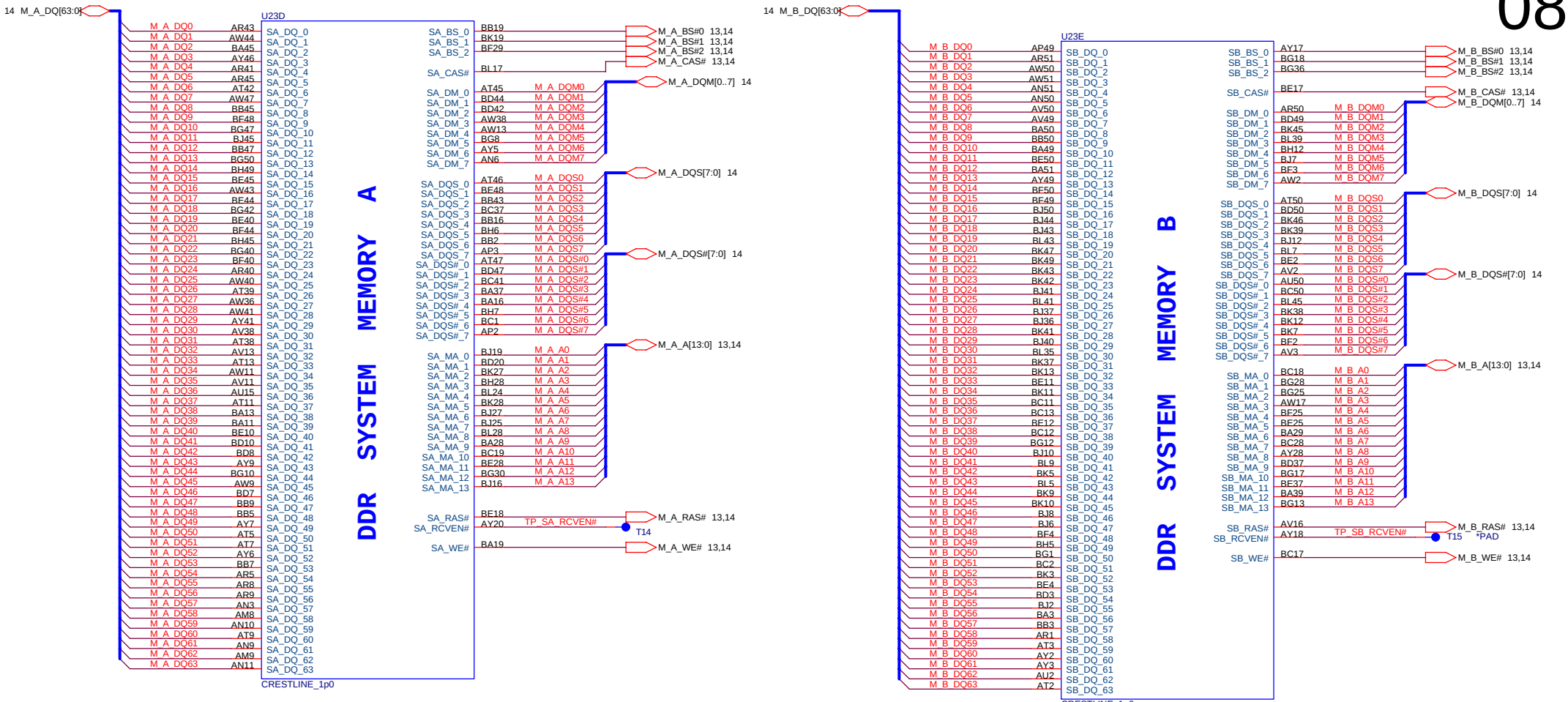
R48	NC	0
R49	NC	0
R2618	NC	39
R2627	0	1.3K/F
R2623	NC	39

Resistor Discret UMA

R64	0	NC
R60	0	NC
R64	0	NC
R60	0	NC
R74	0	150
R77	0	150
R65	0	150

PROJECT : CW4
Quanta Computer Inc.

Size: Custom | Document Number: Crestline_B (VGA,DMI) | Rev: 1A
Date: Friday, November 03, 2006 | Sheet 7 of 44



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_C (DDR2)	1A
Date: Friday, November 03, 2006	Sheet 8 of 44	

POWER

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

Ivcc (External GFX 1.310 A, integrate 1.572 A)

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity for VCC_AXG.

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external 6bx integrated Gfx
VCC_AXG	7.7	
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

Ivcc_AXM Controller supply current 540mA

Layout Note: Inside GMCH cavity.

Layout Note: Place close to GMCH edge.

Layout Note: Place C901 where LVDS and DDR2 taps.

Layout Note: Place on the edge.

CRESTLINE_1p0

CRESTLINE_1p0

PROJECT :	CW4
Quanta Computer Inc.	
Size: Custom	Document Number: Crestline_D (VCC,NCTF)
Rev: 1A	
Date: Friday, November 03, 2006	Sheet 9 of 44

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

IV&EV Dis/Enable setting

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

FB_120ohm+-25%_100mHz _200mA_0.2ohm DC

FB_180ohm+-25% 100mHz_1500mA_ 0.09ohm DC

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

FB_220ohm+-25%_100MHz _2A_0.1ohm DC

0.1Caps should be placed 200 mils with in its pins.

22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.

Ivcc_VTT FSB supply current 0.85A

Place on the edge.

Reserved L81 pad for inductor.

Place caps close to VCC_AXD.

Ivcc_DMI supply current 100mA

Place caps close to VCC_AXF

Ivcc_PEG supply current 1.2A

Ivcc_RX_DMI supply current 250mA

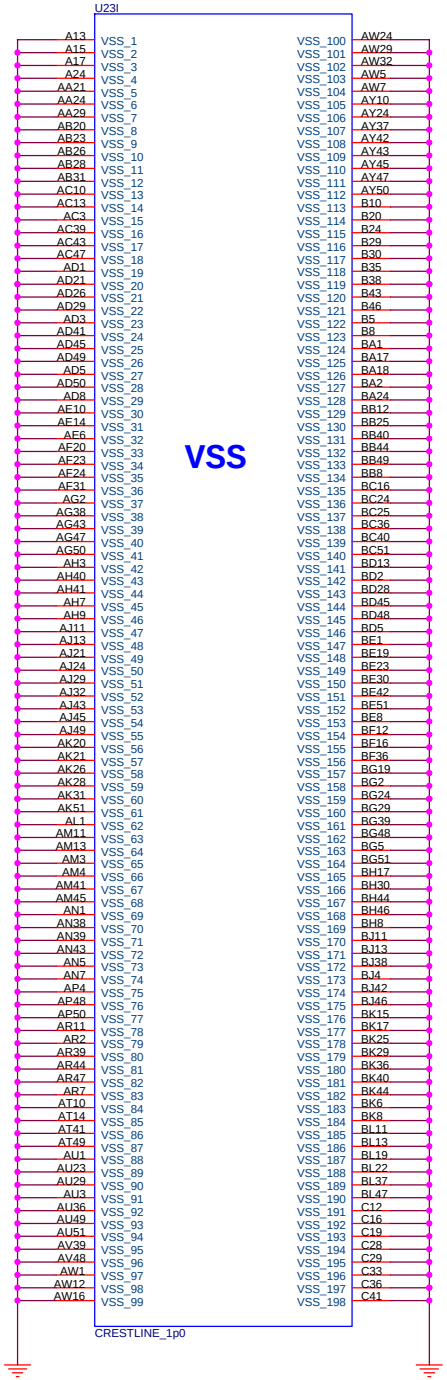
Ivcca_PEG_BG supply current 100mA

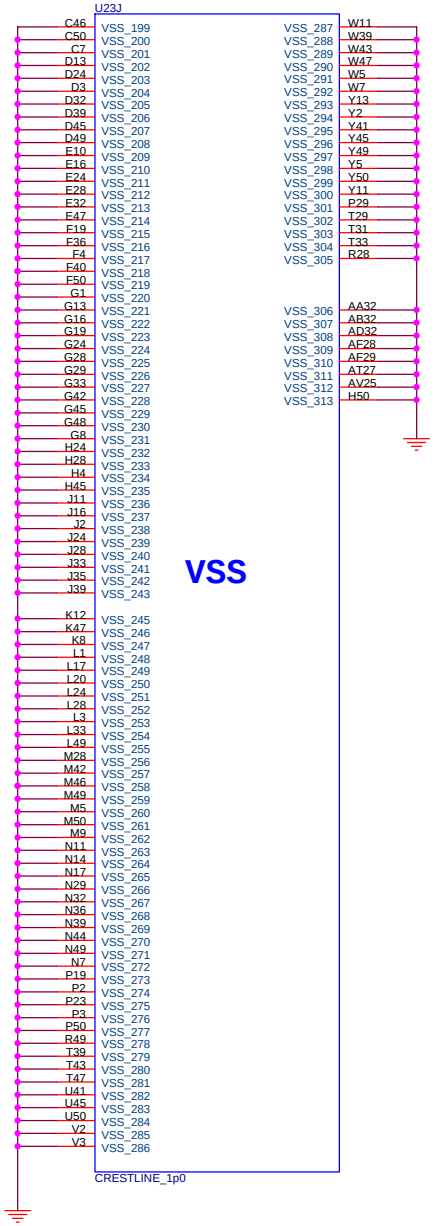
+3V_VCC_HV

40 mil wide

CRESTLINE_1p0

PROJECT :	CW4
Quanta Computer Inc.	
Size: Custom	Document Number: Crestline_E (POWER)
Rev: 1A	
Date: Friday, November 03, 2006	Sheet 10 of 44





PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_F (VSS)	1A

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Strap table

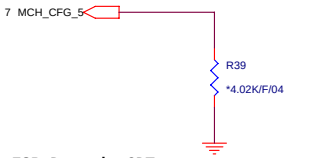
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

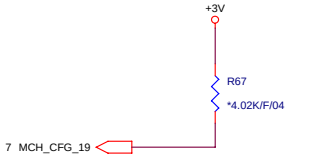
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



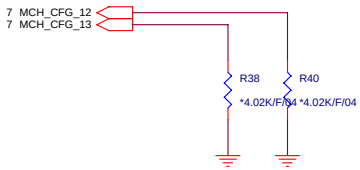
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



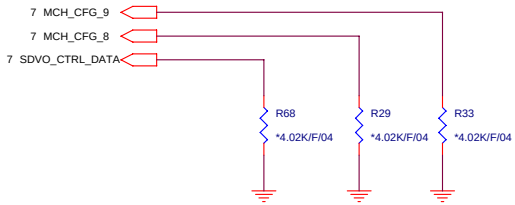
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

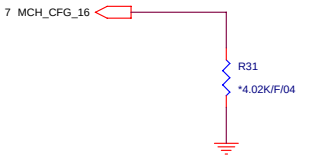


SDVO Present

Strap define at External DVI control page

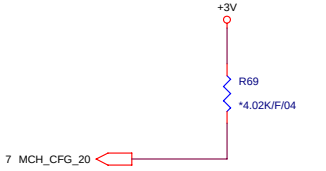
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_F Strap	1A
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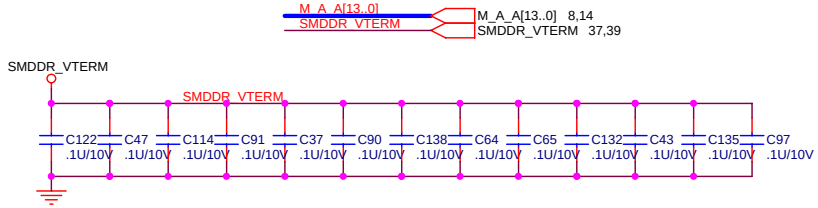
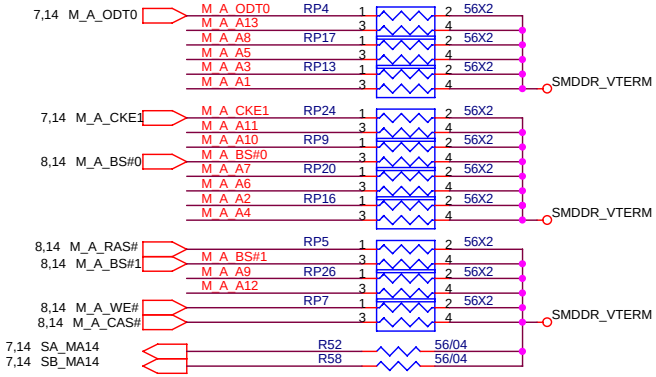
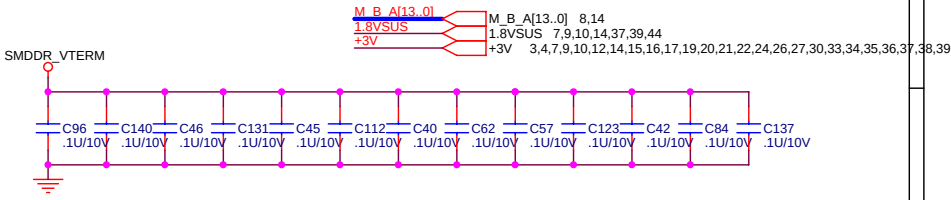
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

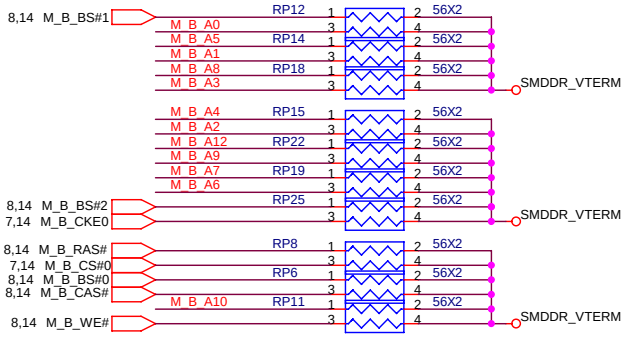


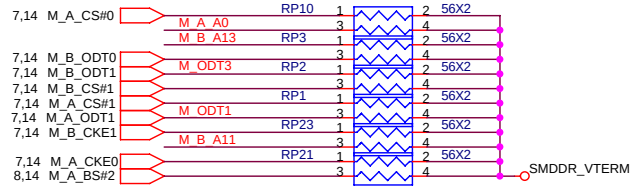


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
B	DDRII RES. ARRAY	1A

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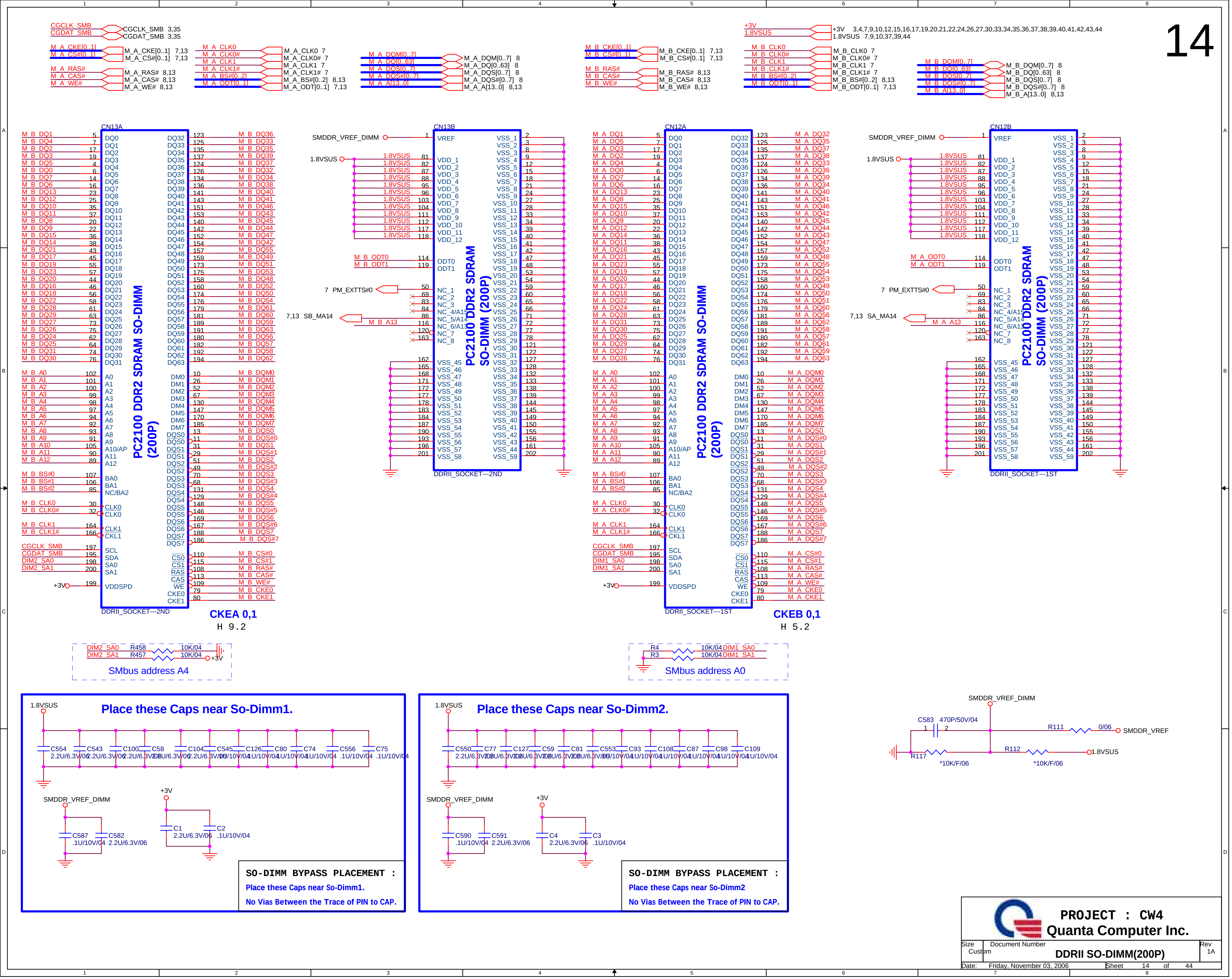
PC2100 DDR2 SDRAM SO-DIMM (200P)
CN13A
DDRII_SOCKET---2ND
CN13B
PC2100 DDR2 SDRAM SO-DIMM (200P)
CN12A
DDRII_SOCKET---1ST
CN12B
CKEA 0,1
H 9.2
CKEB 0,1
H 5.2
SMbus address A4
SMbus address A0
SMDDR_VREF_DIMM
SMDDR_VREF
1.8VSUS
+3V
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm2.
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.
PROJECT : CW4
Quanta Computer Inc.
Size Custom
Document Number
DDRII SO-DIMM(200P)
Rev 1A
Date: Friday, November 03, 2006
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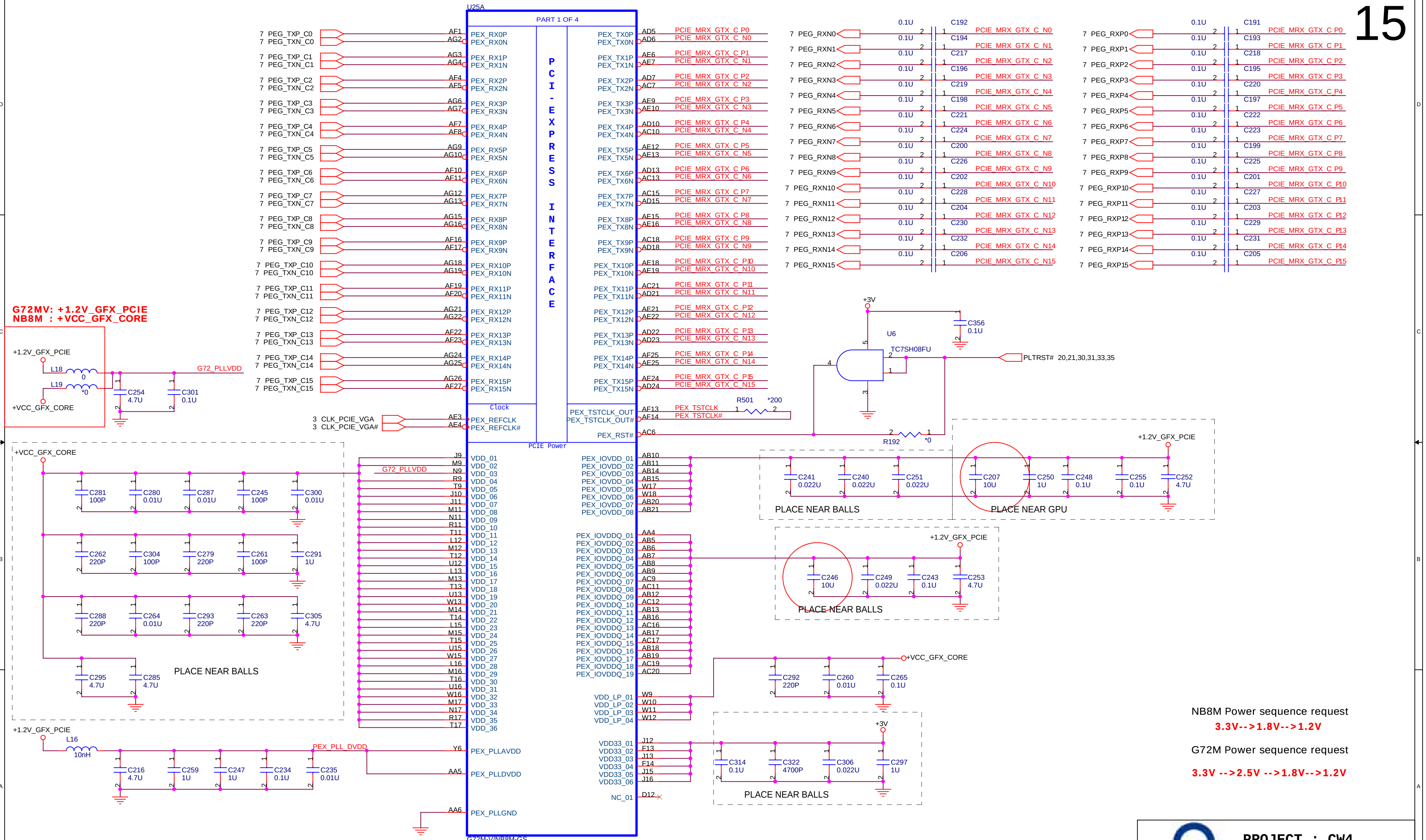

NB8M Power sequence request

3.3V-->1.8V-->1.2V

G72M Power sequence request

3.3V -->2.5V -->1.8V-->1.2V

PROJECT : CW4	Quanta Computer Inc.
Size: Custom	Document Number: VGA(NB8M-GS)(1 of 4) — Rev 1A
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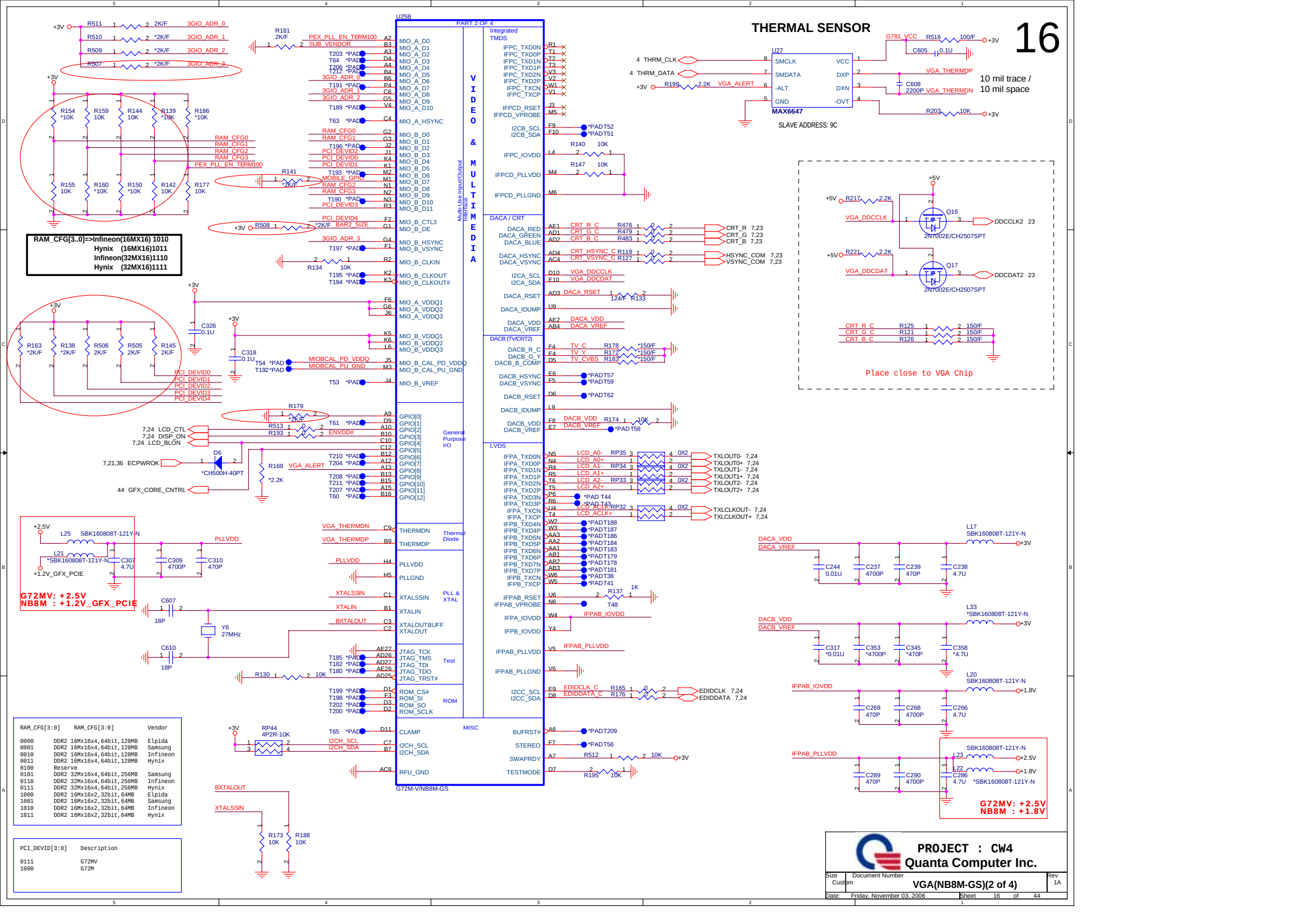

RAM_CFG[3:0]	RAM_CFG[3:0]	Vendor
0000	DDR2 16Mx16x4,64bit,128MB	Elpida
0001	DDR2 16Mx16x4,64bit,128MB	Samsung
0010	DDR2 16Mx16x4,64bit,128MB	Infineon
0011	DDR2 16Mx16x4,64bit,128MB	Hynix
0100	Reserve	
0101	DDR2 32Mx16x4,64bit,256MB	Samsung
0110	DDR2 32Mx16x4,64bit,256MB	Infineon
0111	DDR2 32Mx16x4,64bit,256MB	Hynix
1000	DDR2 16Mx16x2,32bit,64MB	Elpida
1001	DDR2 16Mx16x2,32bit,64MB	Samsung
1010	DDR2 16Mx16x2,32bit,64MB	Infineon
1011	DDR2 16Mx16x2,32bit,64MB	Hynix

PCI_DEVID[3:0]	Description
0111	G72MV
1000	G72M

FB_CMD[0..26] 18
FBD[0..63] 18
FBDQM[0..7] 18
FBDQS[0..7] 18
FBDQS#[0..7] 18

U25C

Part 3 of 4

MEMORY INTERFACE

FBD0	A26	FB_DQ0	G27	FB_CMD0	FB_CMD[0..26]
FBD1	C24	FB_DQ1	D25	FB_CMD1	
FBD2	B24	FB_DQ2	F26	FB_CMD2	
FBD3	A24	FB_DQ3	F25	FB_CMD3	
FBD4	C22	FB_DQ4	G25	FB_CMD4	
FBD5	A25	FB_DQ5	J25	FB_CMD5	
FBD6	B25	FB_DQ6	J27	FB_CMD6	
FBD7	D23	FB_DQ7	M26	FB_CMD7	
FBD8	G22	FB_DQ8	C27	FB_CMD8	
FBD9	J23	FB_DQ9	C25	FB_CMD9	
FBD10	E24	FB_DQ10	D24	FB_CMD10	
FBD11	F23	FB_DQ11	N27	FB_CMD11	
FBD12	J24	FB_DQ12	G24	FB_CMD12	
FBD13	F24	FB_DQ13	J26	FB_CMD13	
FBD14	G23	FB_DQ14	M27	FB_CMD14	
FBD15	H24	FB_DQ15	C26	FB_CMD15	
FBD16	D16	FB_DQ16	M25	FB_CMD16	
FBD17	E16	FB_DQ17	D26	FB_CMD17	
FBD18	D17	FB_DQ18	D27	FB_CMD18	
FBD19	F18	FB_DQ19	K26	FB_CMD19	
FBD20	E19	FB_DQ20	K25	FB_CMD20	
FBD21	E18	FB_DQ21	K24	FB_CMD21	
FBD22	D20	FB_DQ22	F27	FB_CMD22	
FBD23	D19	FB_DQ23	K27	FB_CMD23	
FBD24	A18	FB_DQ24	G26	FB_CMD24	
FBD25	B18	FB_DQ25	B27	FB_CMD25	
FBD26	A19	FB_DQ26	N24	FB_CMD26	
FBD27	B19	FB_DQ27			
FBD28	D18	FB_DQ28			
FBD29	C19	FB_DQ29			
FBD30	C16	FB_DQ30			
FBD31	C18	FB_DQ31			
FBD32	N26	FB_DQ32			
FBD33	N25	FB_DQ33			
FBD34	R25	FB_DQ34			
FBD35	R26	FB_DQ35			
FBD36	R27	FB_DQ36			
FBD37	T25	FB_DQ37			
FBD38	T27	FB_DQ38			
FBD39	T26	FB_DQ39			
FBD40	AB23	FB_DQ40			
FBD41	Y24	FB_DQ41			
FBD42	AB24	FB_DQ42			
FBD43	AB22	FB_DQ43			
FBD44	AC24	FB_DQ44			
FBD45	AC22	FB_DQ45			
FBD46	AA23	FB_DQ46			
FBD47	AA22	FB_DQ47			
FBD48	T24	FB_DQ48			
FBD49	T23	FB_DQ49			
FBD50	R24	FB_DQ50			
FBD51	R23	FB_DQ51			
FBD52	R22	FB_DQ52			
FBD53	T22	FB_DQ53			
FBD54	N23	FB_DQ54			
FBD55	P24	FB_DQ55			
FBD56	AA24	FB_DQ56			
FBD57	AA27	FB_DQ57			
FBD58	AA26	FB_DQ58			
FBD59	AB25	FB_DQ59			
FBD60	AB26	FB_DQ60			
FBD61	AB27	FB_DQ61			
FBD62	AA25	FB_DQ62			
FBD63	W25	FB_DQ63			

*PADT49

NB8M A VER:
NC

R151 0_4

*PADT47

FB_DQM0	D21	FBDQM0	
FB_DQM1	F22	FBDQM1	
FB_DQM2	F20	FBDQM2	
FB_DQM3	A21	FBDQM3	
FB_DQM4	V27	FBDQM4	
FB_DQM5	W22	FBDQM5	
FB_DQM6	V22	FBDQM6	
FB_DQM7	V24	FBDQM7	

read strobe

FB_DQS_RN0	A22	FBDQS#0
FB_DQS_RN1	E22	FBDQS#1
FB_DQS_RN2	F21	FBDQS#2
FB_DQS_RN3	B21	FBDQS#3
FB_DQS_RN4	V26	FBDQS#4
FB_DQS_RN5	W23	FBDQS#5
FB_DQS_RN6	V23	FBDQS#6
FB_DQS_RN7	W27	FBDQS#7

write strobe

FB_DQS_WP0	B22	FBDQS0
FB_DQS_WP1	D22	FBDQS1
FB_DQS_WP2	E21	FBDQS2
FB_DQS_WP3	C21	FBDQS3
FB_DQS_WP4	V25	FBDQS4
FB_DQS_WP5	W24	FBDQS5
FB_DQS_WP6	U24	FBDQS6
FB_DQS_WP7	W26	FBDQS7

18 FB_CLK0	L24	FB_CLK0
18 FB_CLK0#	K23	FB_CLK0#
18 FB_CLK1	M22	FB_CLK1
18 FB_CLK1#	N22	FB_CLK1#
T45 *PAD	M23	FB_REFCLK
T50 *PAD	M24	FB_REFCLK#
	K22	FB_DEBUG
	A16	FB_VREF
+3V	F12	I2CS_SCL
	F11	I2CS_SDA
	D14	FB_PLLVDD
	D13	FB_PLLAVDD
	C15	FB_PLLAGND

G72M-V/NB8M-GS

FBVTT_01	E15	
FBVTT_02	F15	
FBVTT_03	F16	
FBVTT_04	J17	
FBVTT_05	J18	
FBVTT_06	L19	
FBVTT_07	N19	
FBVTT_08	R19	
FBVTT_09	U19	
FBVTT_10	W19	
FBVDDQ_01	F17	
FBVDDQ_02	F19	
FBVDDQ_03	J19	
FBVDDQ_04	M19	
FBVDDQ_05	T19	
FBVDDQ_06	J22	
FBVDDQ_07	L22	
FBVDDQ_08	P22	
FBVDDQ_09	U22	
FBVDDQ_10	Y22	
FBCAL_PD_VDDQ	D15	FBCAL_PD_VDDQ
FBCAL_PU_GND	E13	FBCAL_PU_GND
FBCAL_TERM_GND	H22	FBCAL_TERM_GND

+1.8V
Rt R515 1K/F
FBVREF
Rb R514 1K/F
C602 0.1U

FBVREF = FBVDDQ * Rb/(Rt + Rb).
VREF = 0.5 * FBVDDQ.
DDR: 0.9V = 1.8V * 1K/(1K + 1K).

NB8M A VER:
STUFF

FB_CMD12 R149 FB_DEBUG
*0_4
FBVREF

G72MV: NC
NB8M : +1.2V_GFX_PCIE

G72MV: NC
NB8M : 2.2K

R180 2 *2.2K/F
R184 2 *2.2K/F

L60
*SBK160808T-121Y-N
+1.2V_GFX_PCIE
L59 0

C604 4.7U
C331 1U
C603 0.01U

+1.8V
R170 40/F
R158 *40/F
R162 30/F

U25D

Part 4 of 4

GND

B2	GND_01	GND_48	P14
E2	GND_02	GND_49	R14
H2	GND_03	GND_50	U14
L2	GND_04	GND_51	W14
P2	GND_05	GND_52	AC14
U2	GND_06	GND_53	AD14
Y2	GND_07	GND_54	N15
AC2	GND_08	GND_55	P15
AF2	GND_09	GND_56	R15
AF3	GND_10	GND_57	AF15
B5	GND_11	GND_58	N16
E5	GND_12	GND_59	P16
L5	GND_13	GND_60	R16
P5	GND_14	GND_61	AD16
U5	GND_15	GND_62	B17
Y5	GND_16	GND_63	E17
AC5	GND_17	GND_64	L17
H6	GND_18	GND_65	P17
AF6	GND_19	GND_66	U17
B8	GND_20	GND_67	AD17
E8	GND_21	GND_68	AF18
AD8	GND_22	GND_69	K19
K9	GND_23	GND_70	P19
P9	GND_24	GND_71	V19
V9	GND_25	GND_72	AD19
AD9	GND_26	GND_73	B20
AF9	GND_27	GND_74	E20
B11	GND_28	GND_75	AD20
E11	GND_29	GND_76	AF21
		GND_77	B23
L11	GND_31	GND_78	E23
P11	GND_32	GND_79	H23
U11	GND_33	GND_80	L23
AD11	GND_34	GND_81	P23
N12	GND_35	GND_82	U23
P12	GND_36	GND_83	Y23
R12	GND_37	GND_84	AC23
AD12	GND_38	GND_85	AF24
AF12	GND_39	GND_86	B26
N13	GND_40	GND_87	E26
P13	GND_41	GND_88	H26
R13	GND_42	GND_89	L26
B14	GND_43	GND_90	P26
E14	GND_44	GND_91	U26
J14	GND_45	GND_92	Y26
L14	GND_46	GND_93	AC26
N14	GND_47	GND_94	AF26

G72M-V/NB8M-GS

PLACE BELOW GPU

+1.8V

C256 4700P	C277 0.022U	C298 0.1U	C594 4700P	C324 0.1U	C325 4.7U	C302 1U
C275 4700P	C278 0.022U	C270 0.1U	C316 4700P	C313 0.022U	C334 0.1U	C360 4.7U
C312 4700P	C294 0.022U	C593 0.1U	C336 0.022U	C321 0.1U		C284 1U

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA(NB8M-GS)(3 of 4)	1A

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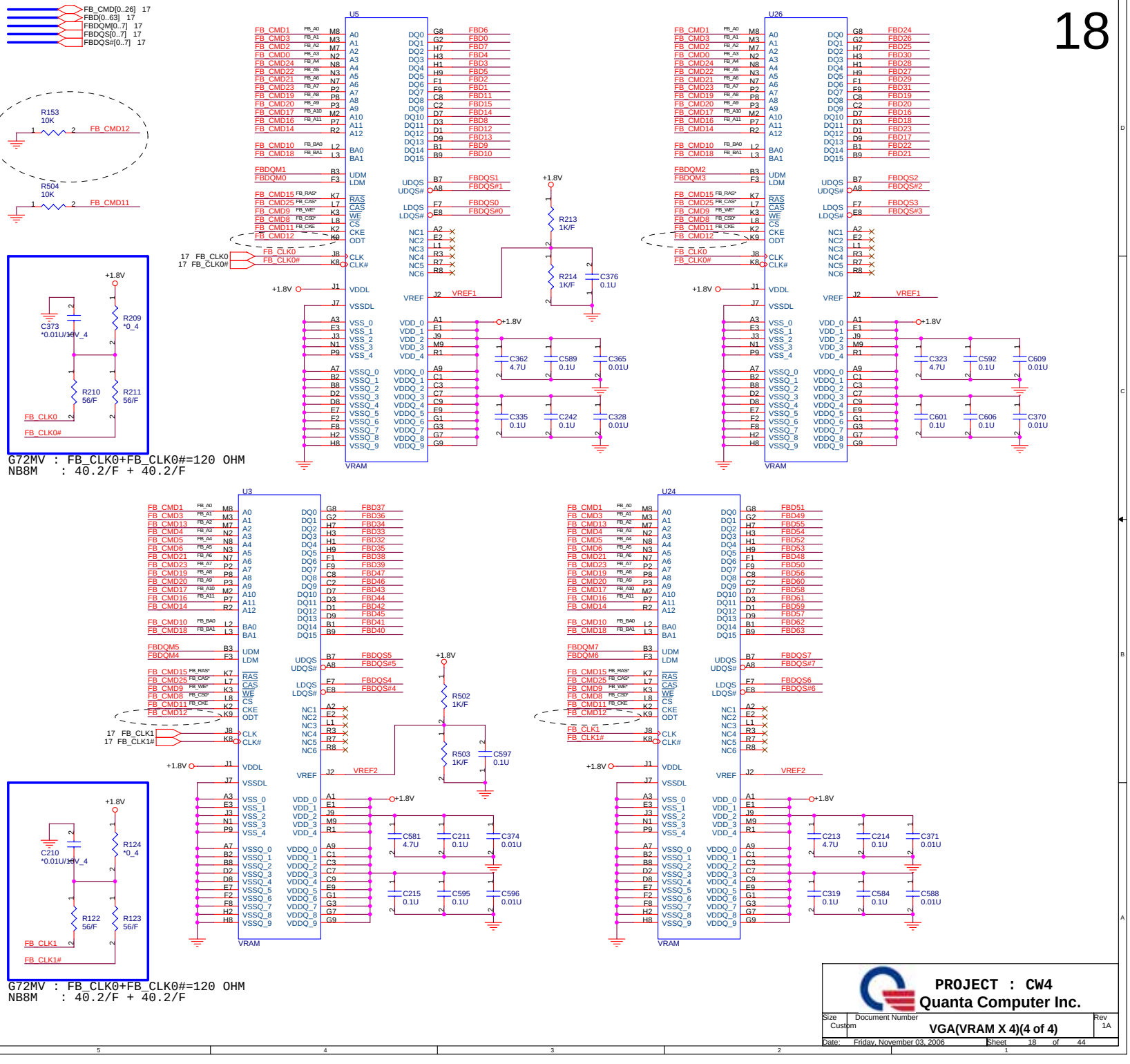
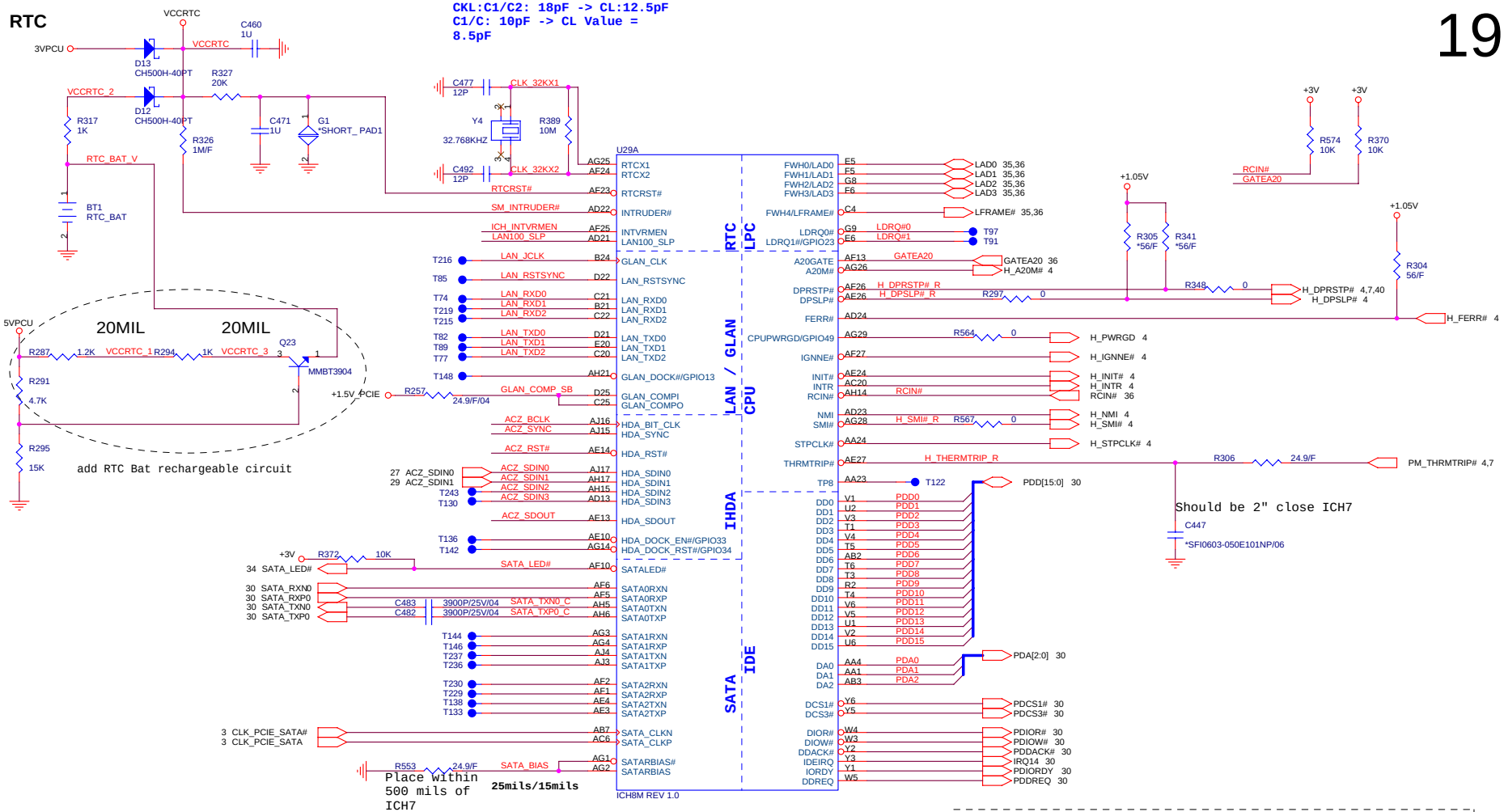


PROJECT : CW4			
Quanta Computer Inc.			
Size: Custom	Document Number: VGA(VRAM X 4)(4 of 4)		Rev: 1A
Date: Friday, November 03, 2006	Sheet 18 of 44		

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF



SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

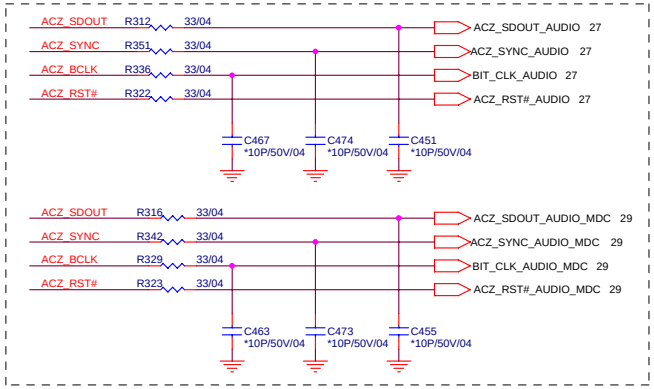
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8-M HOST (1 of 4)	1A
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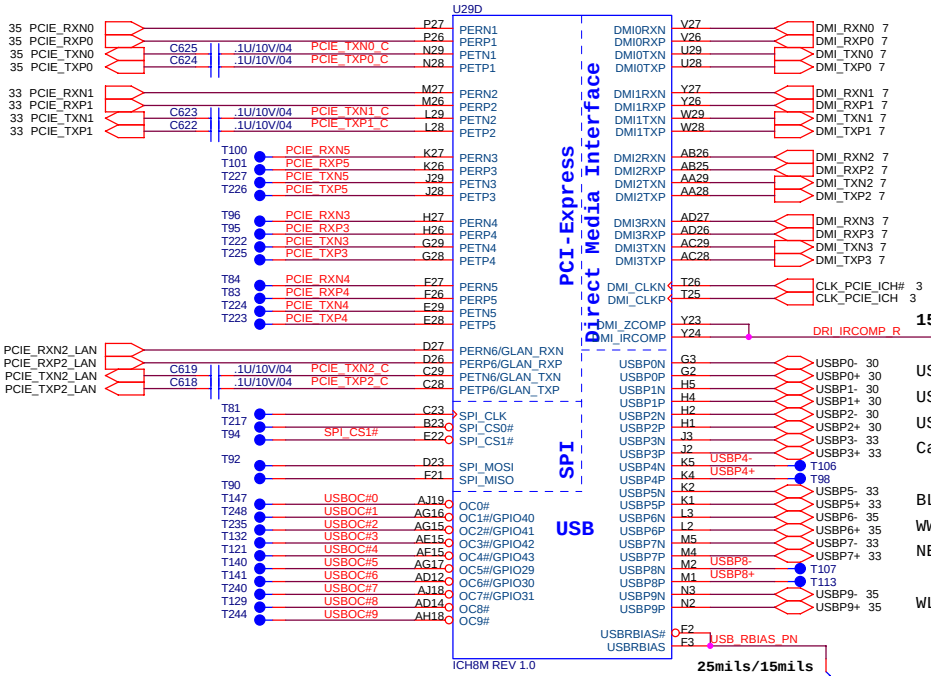
MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

PCIE-LAN



USB Connector

USB Connector

USB Connector

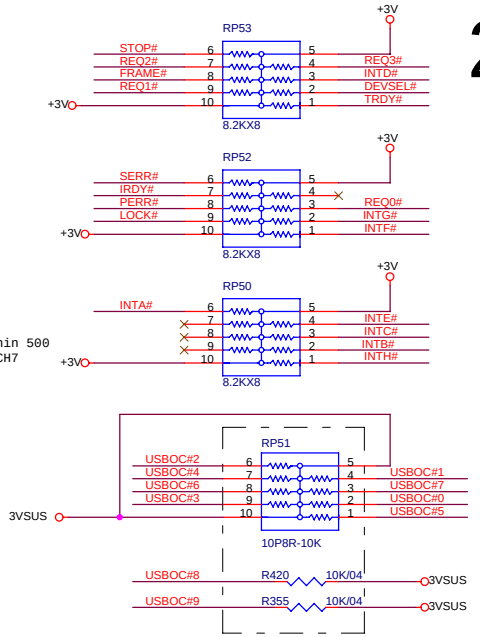
Carama USB

BLUETOOTH

WWAN

NEW CARD

WLAN



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

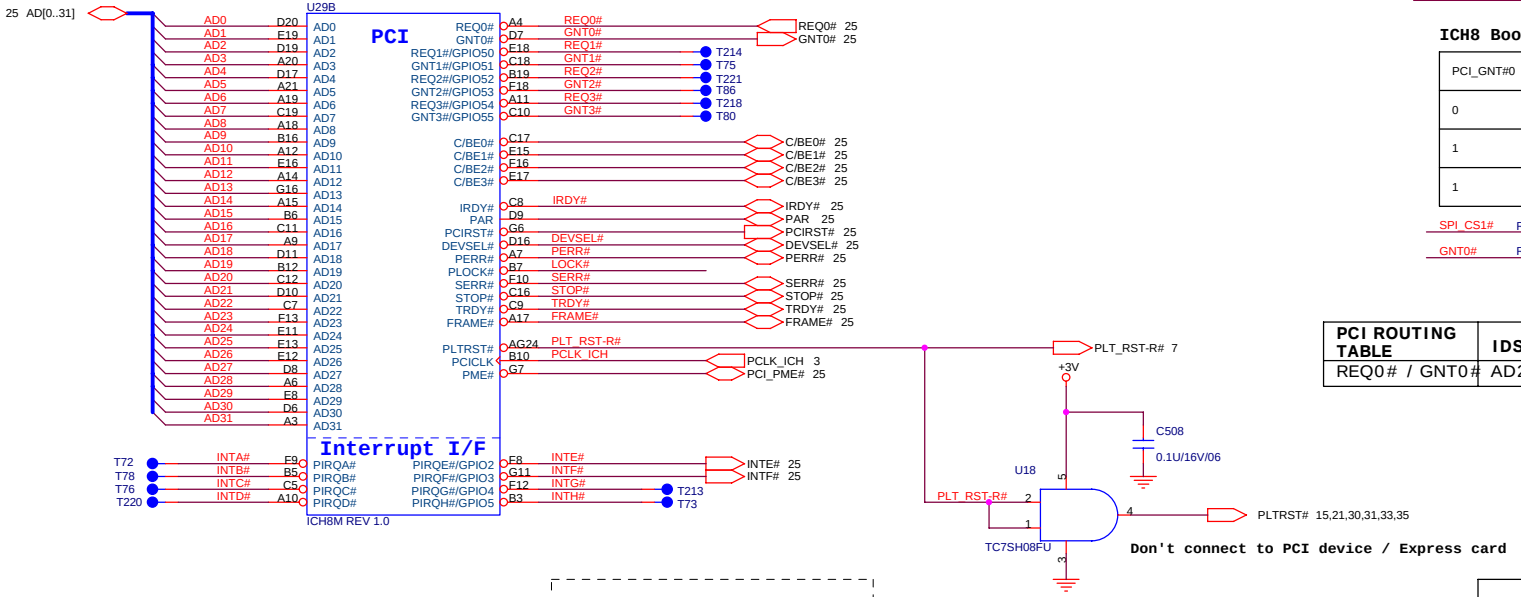
GNT3# R254 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

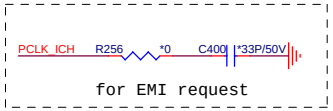
SPI_CS1# R263 *1K

GNT0# R255 *1K



Don't connect to PCI device / Express card

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8-M PCI E (2 of 4)	1A

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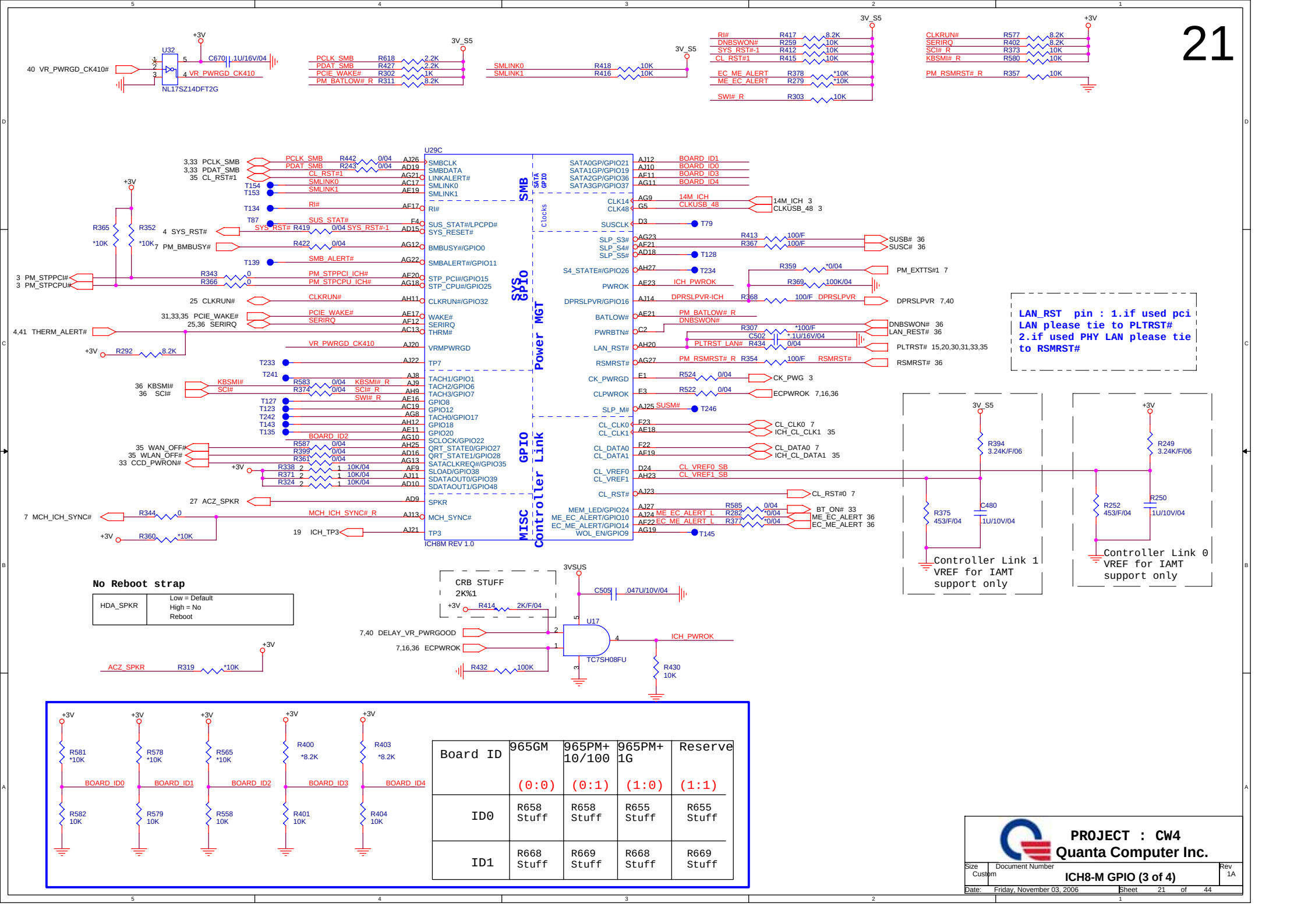
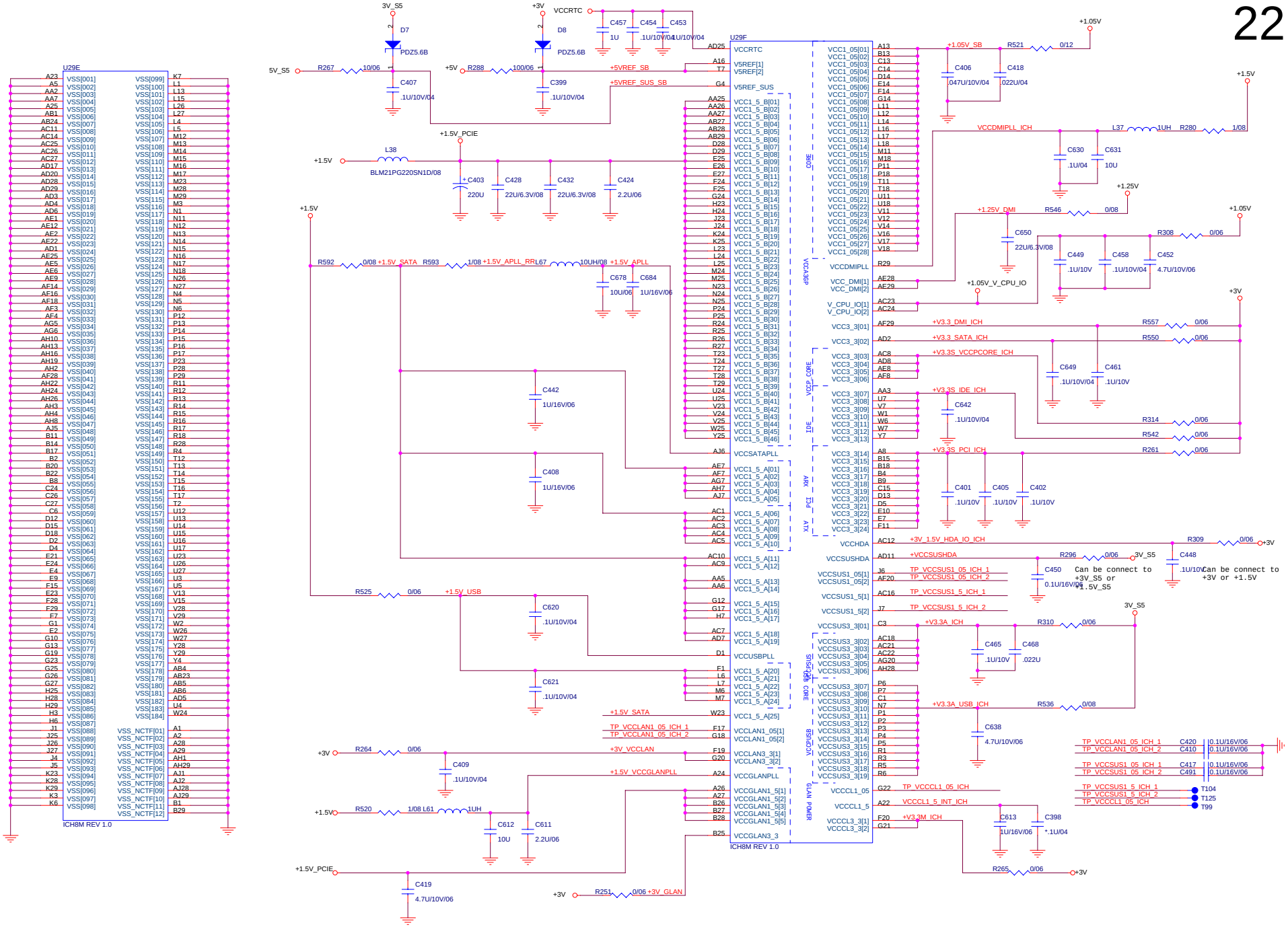
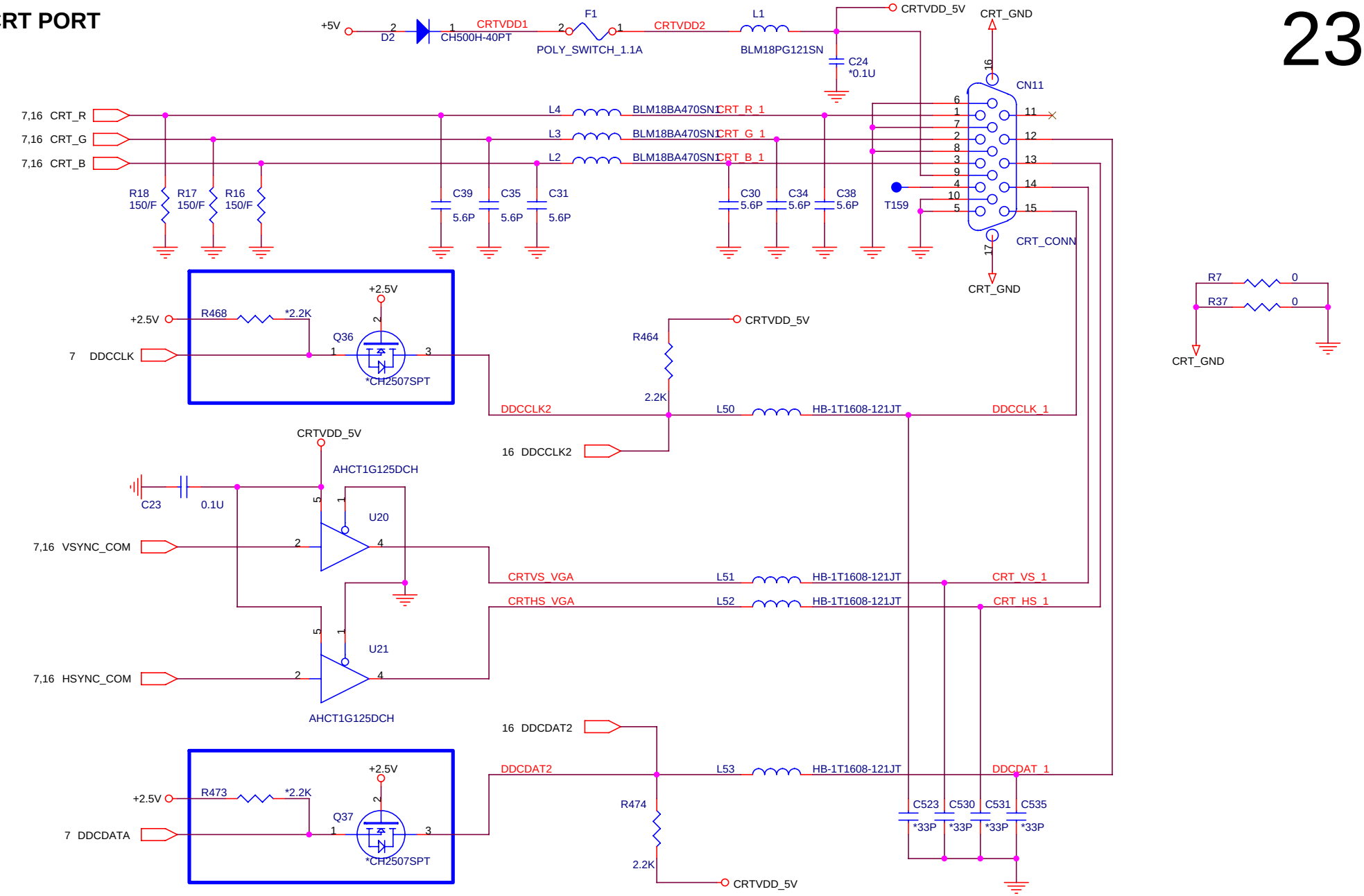

U29C
ICH8M REV 1.0
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
MEM_LED/GPIO24
ME_EC_ALERT/GPIO10
EC_ME_ALERT/GPIO14
WOL_EN/GPIO9
LAN_RST pin : 1.if used pci LAN please tie to PLTRST#
2.if used PHY LAN please tie to RSMRST#
Controller Link 1 VREF for IAMT support only
Controller Link 0 VREF for IAMT support only
No Reboot strap
HDA_SPKR
Low = Default
High = No Reboot
CRB STUFF
2K%1
U17
TC7SH08FU
Board ID
965GM (0:0)
965PM+ 10/100 (0:1)
965PM+ 1G (1:0)
Reserve (1:1)
ID0
ID1
PROJECT : CW4
Quanta Computer Inc.
ICH8-M GPIO (3 of 4)
Size Custom
Document Number
Rev 1A
Date: Friday, November 03, 2006
Sheet 21 of 44

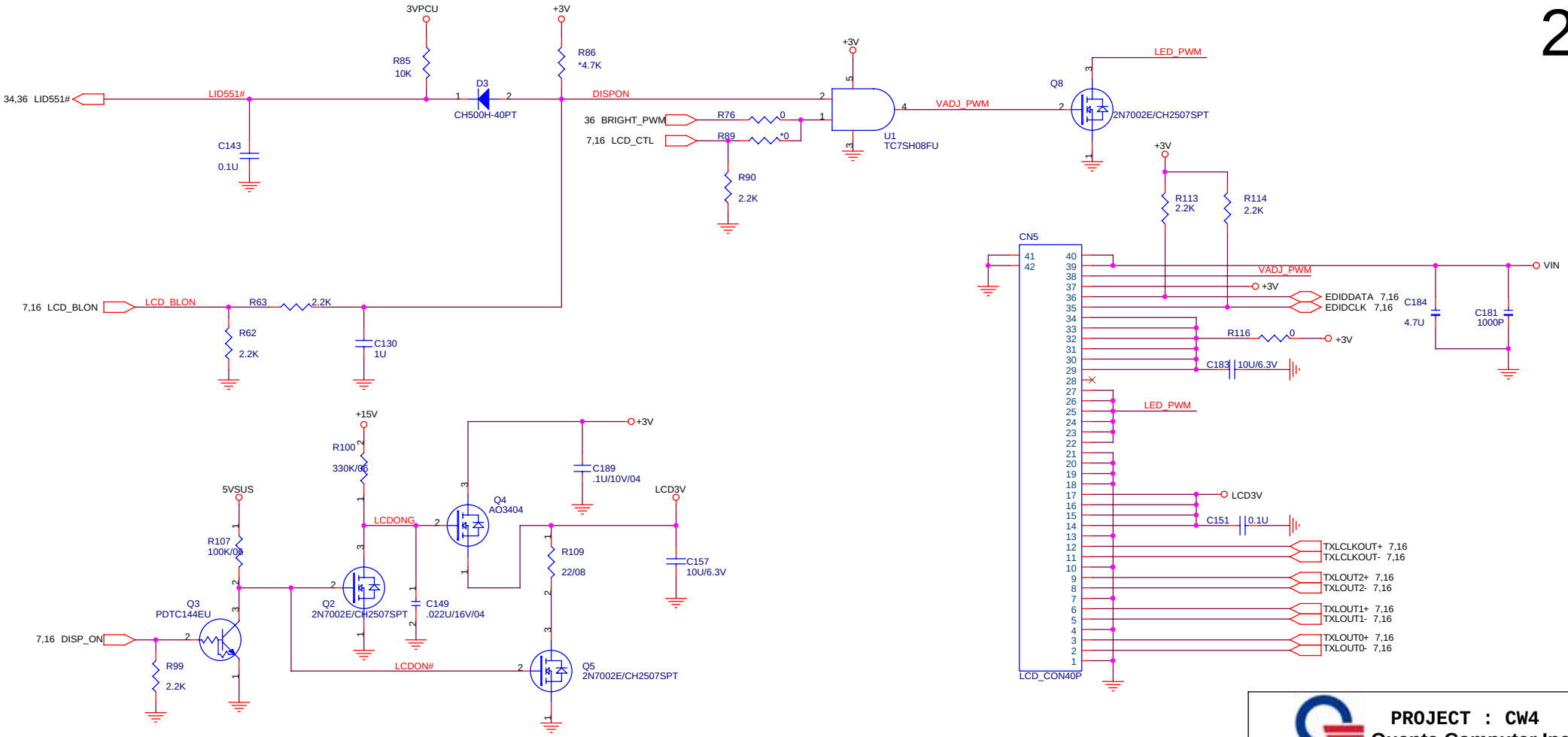


PROJECT : CW4	
Quanta Computer Inc.	
Size: Custom	Document Number: ICH8-M GPIO (3 of 4)
Rev: 1A	
Date: Friday, November 03, 2006	Sheet 22 of 44

CRT PORT

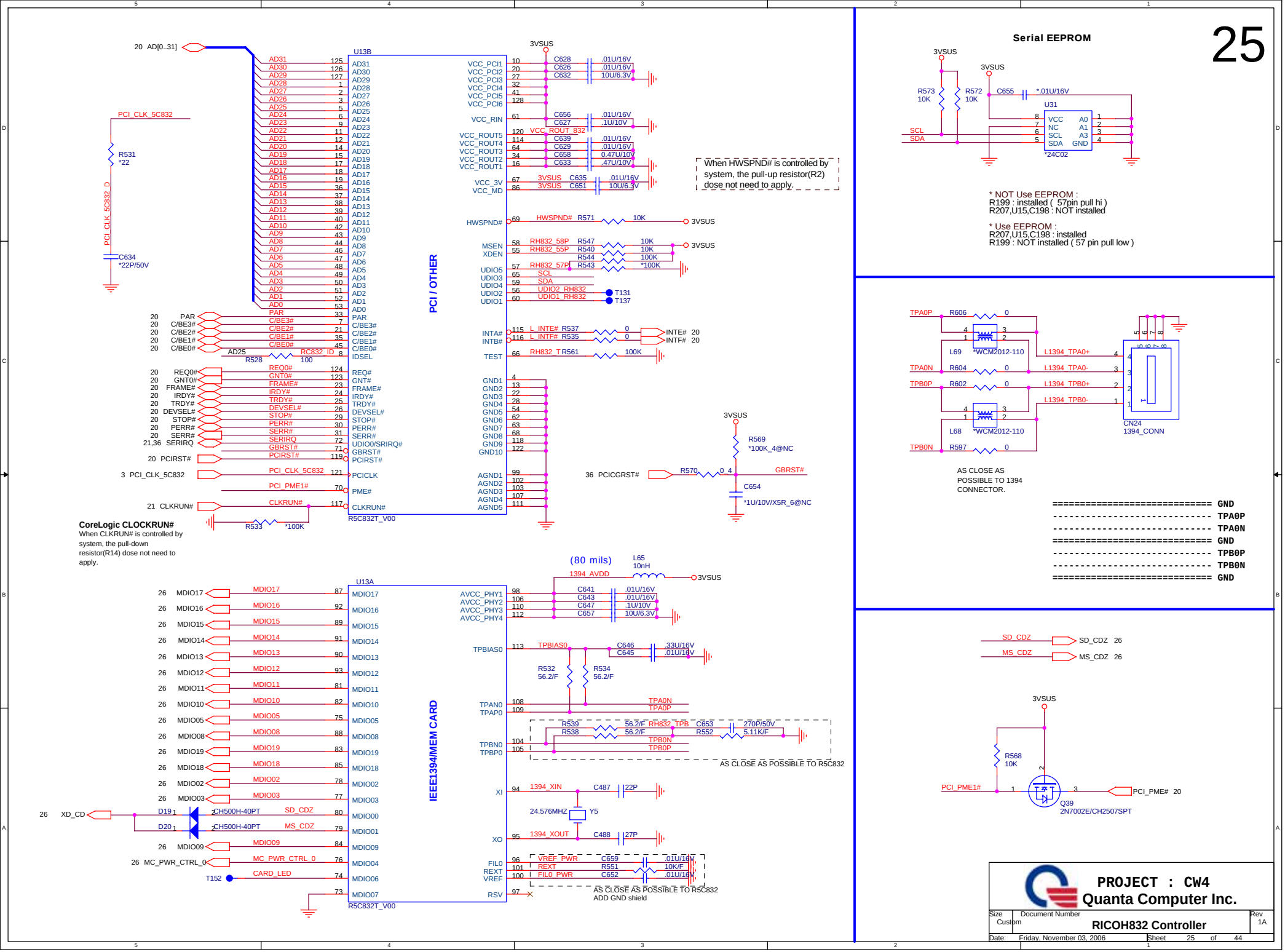


PROJECT : CW4		
Quanta Computer Inc.		
Size: Custom	Document Number: CRT CON	Rev: 1A
Date: Friday, November 03, 2006	Sheet 23 of 44	



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD & LID CON	1A
Date: Friday, November 03, 2006	Sheet 24 of 44	



Serial EEPROM

* NOT Use EEPROM :
R199 : installed (57pin pull hi)
R207,U15,C198 : NOT installed

* Use EEPROM :
R207,U15,C198 : installed
R199 : NOT installed (57 pin pull low)

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

```
============================== GND
------------------------------ TPA0P
------------------------------ TPA0N
============================== GND
------------------------------ TPB0P
------------------------------ TPB0N
============================== GND
```

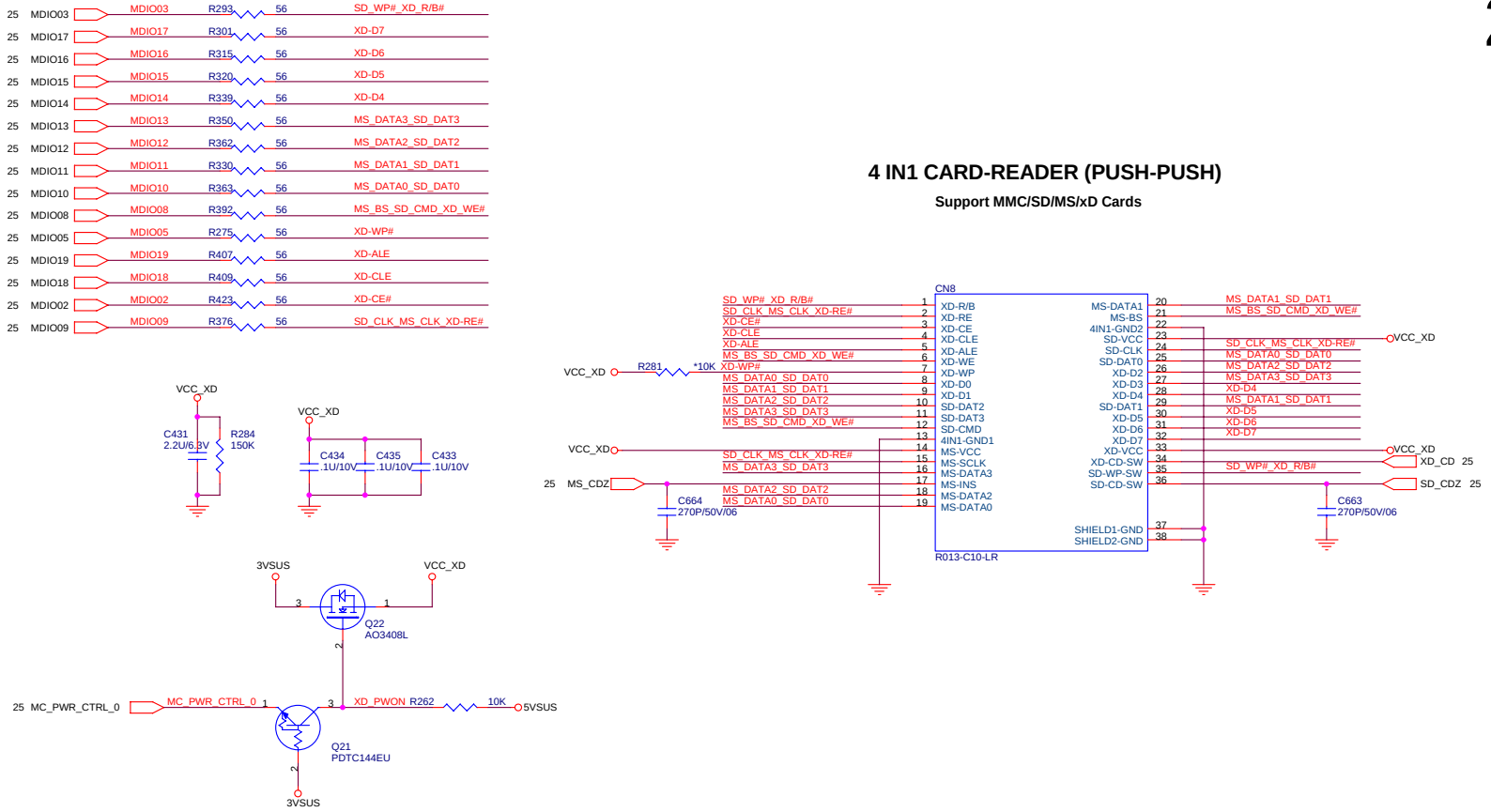
SD_CDZ 26
MS_CDZ 26

PROJECT : CW4
Quanta Computer Inc.

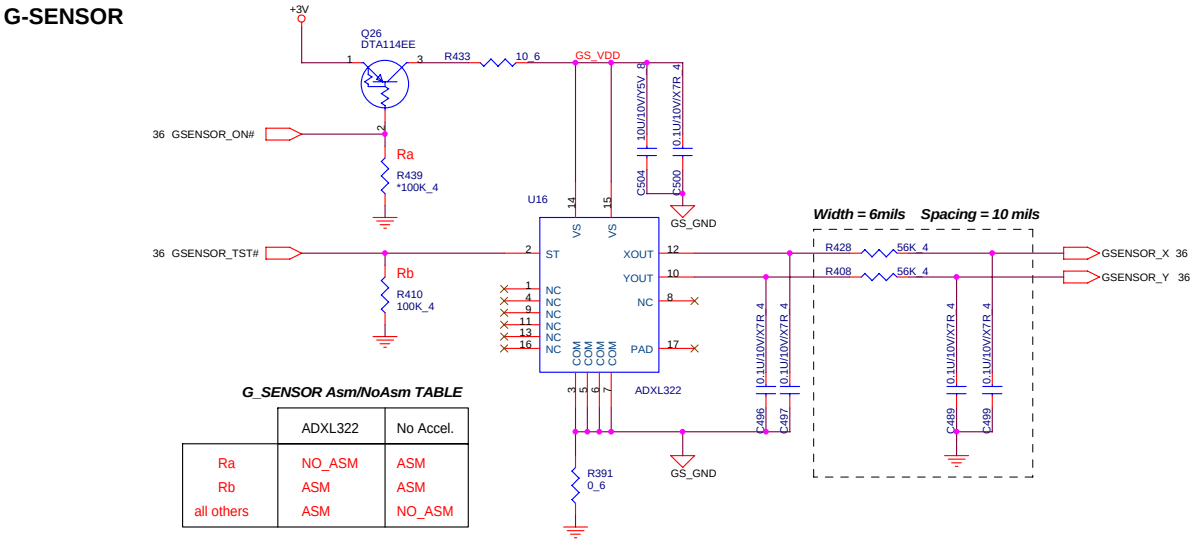
Size	Document Number	Rev
Custom	RICOH832 Controller	1A
Date: Friday, November 03, 2006	Sheet 25 of 44	

4 IN1 CARD-READER (PUSH-PUSH)

Support MMC/SD/MS/xD Cards



G-SENSOR

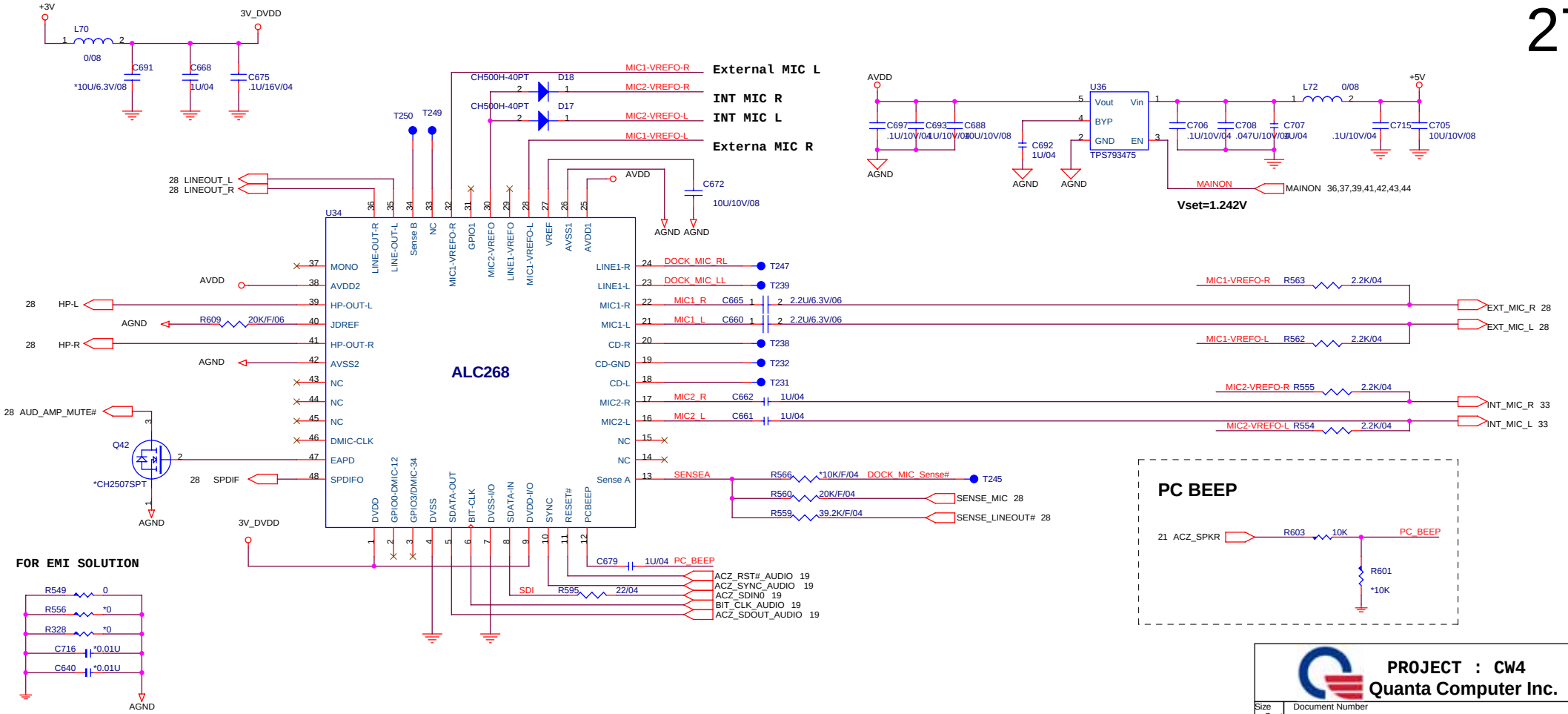


G_SENSOR Asm/NoAsm TABLE

	ADXL322	No Accel.
Ra	NO_ASM	ASM
Rb	ASM	ASM
all others	ASM	NO_ASM

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CARD-READER & G-SENSOR	1A
Date: Friday, November 03, 2006	Sheet 26 of 44	



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AZALIA ALC268	1A
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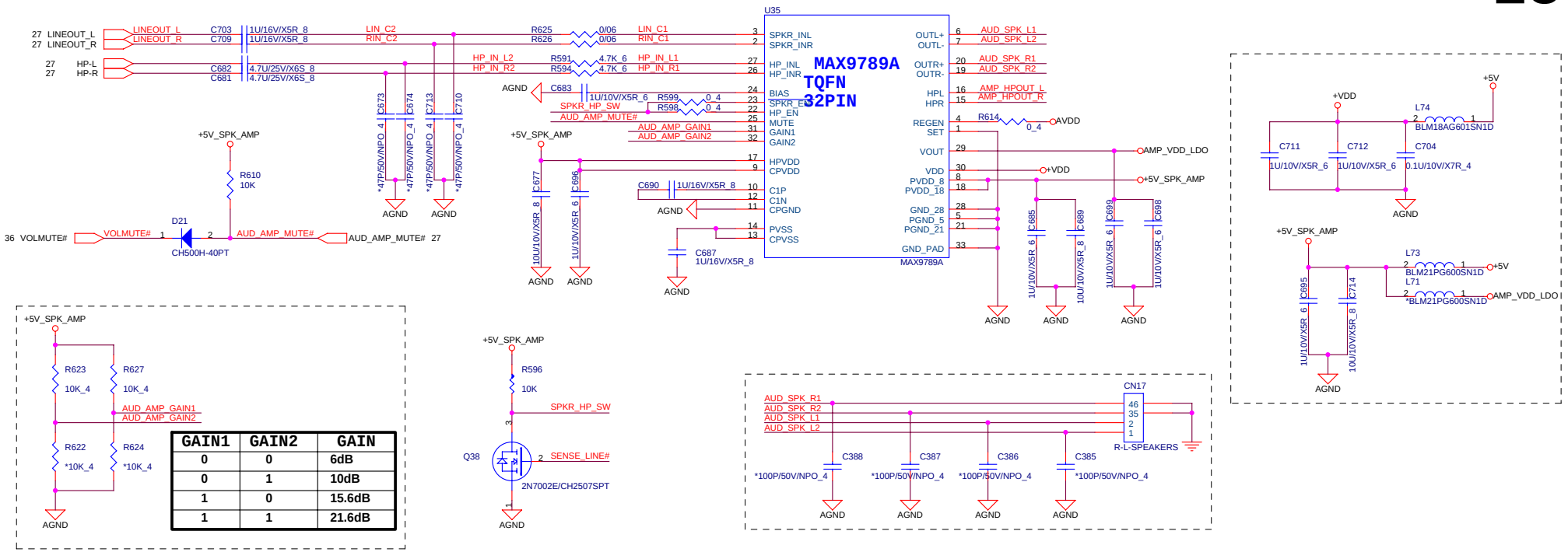
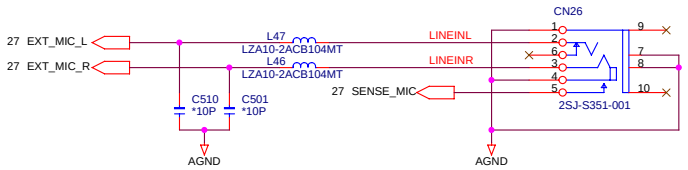
INTERNAL SPEAKER AMPLIFIER

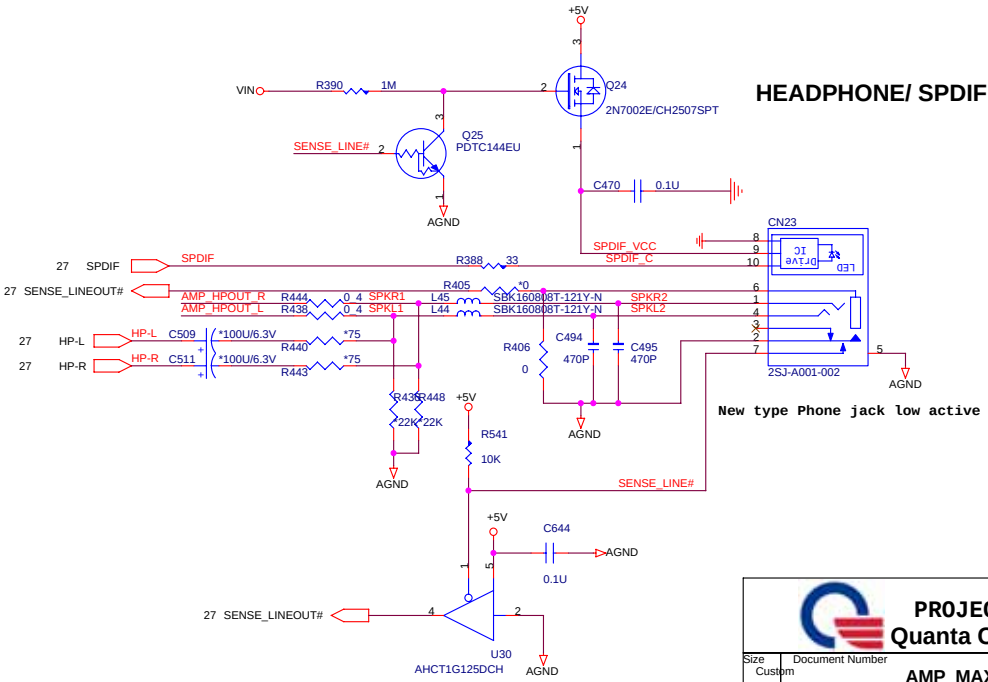


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

MIC-IN JACK



HEADPHONE/ SPDIF OUT



New type Phone jack low active

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_MAX9789A & JACK	1A
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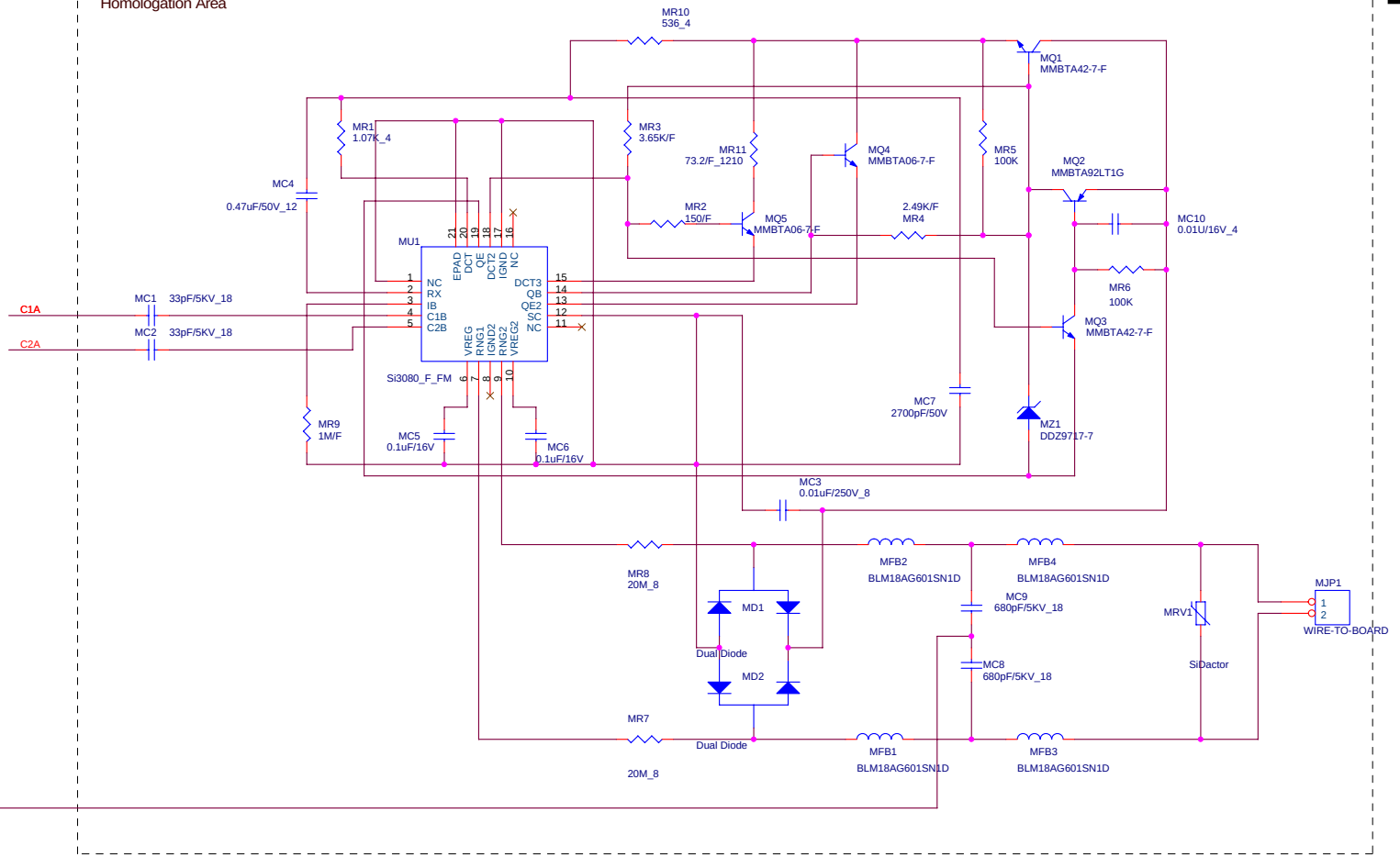
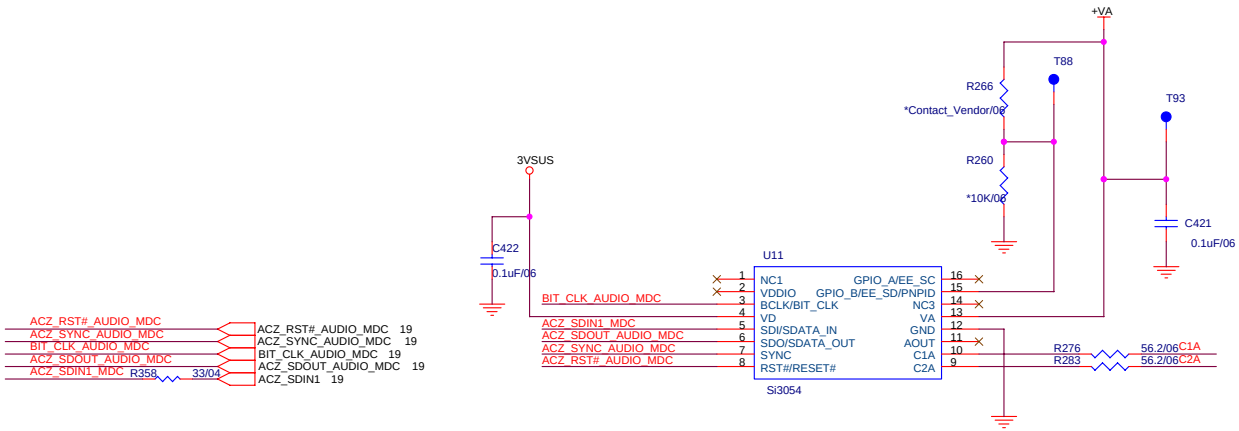
MODEM

No Ground Plane In DAA Section

Homologation Area





PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MODEM(SI3054+SI3080)	1A
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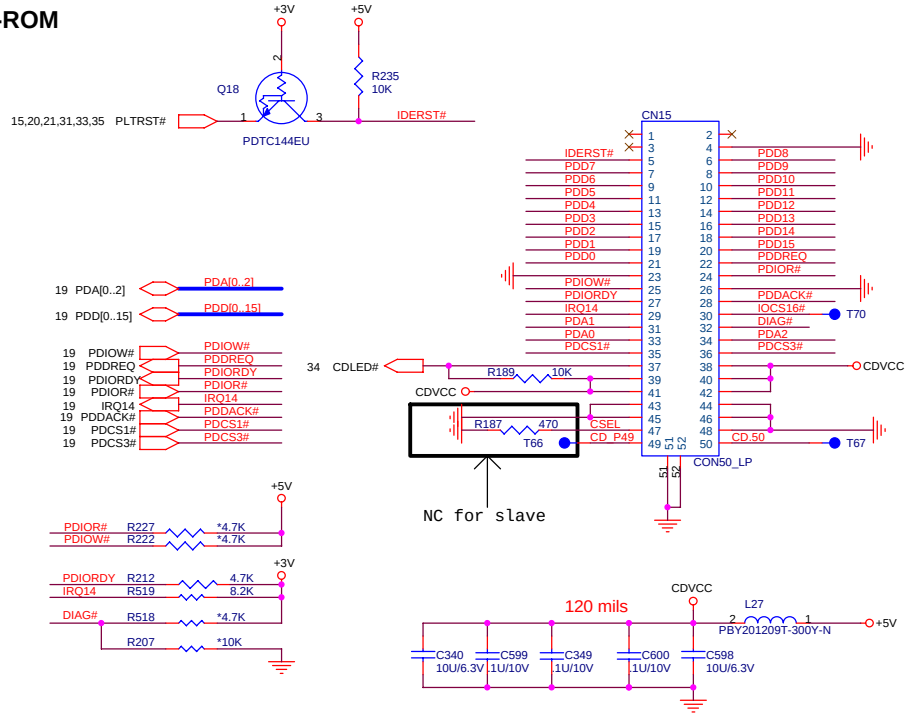
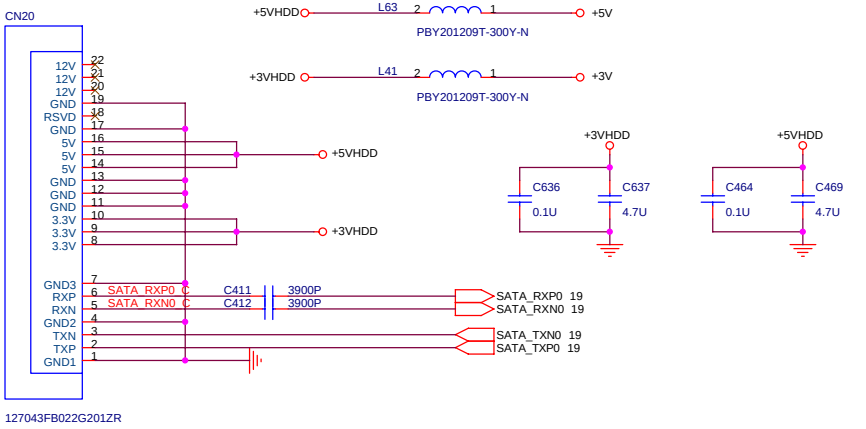
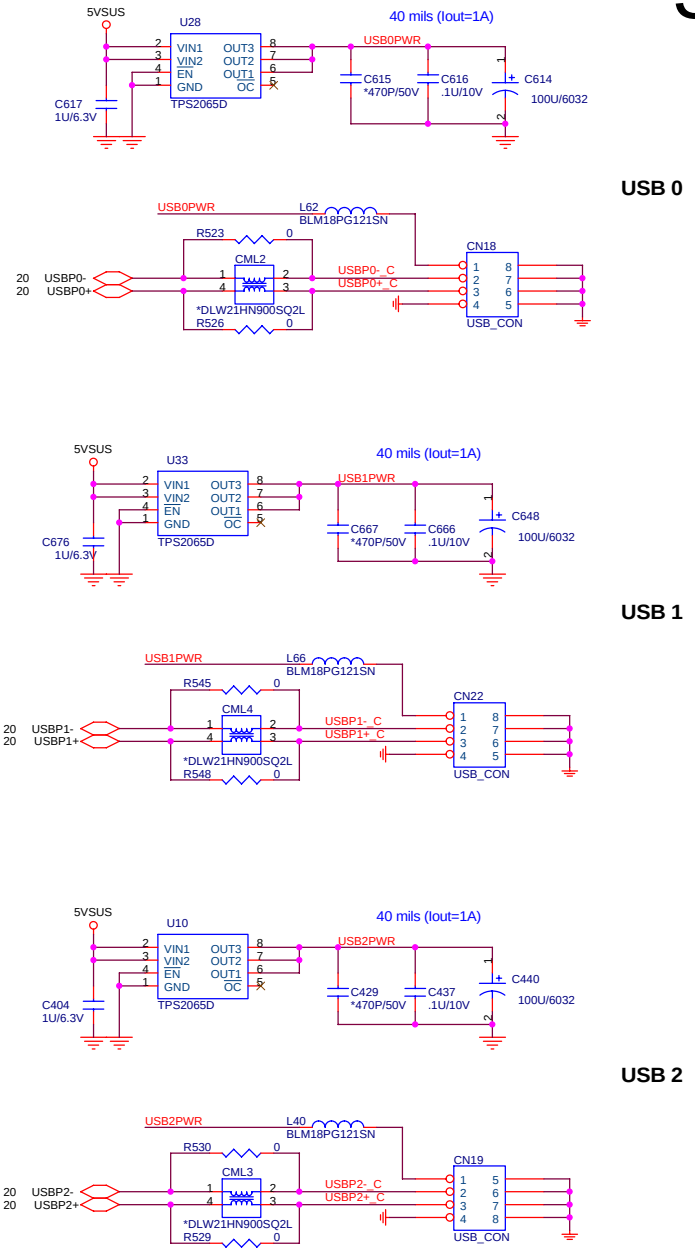
CD-ROM



SATA-HDD CONNECTOR



USBX3



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USBX3	1A

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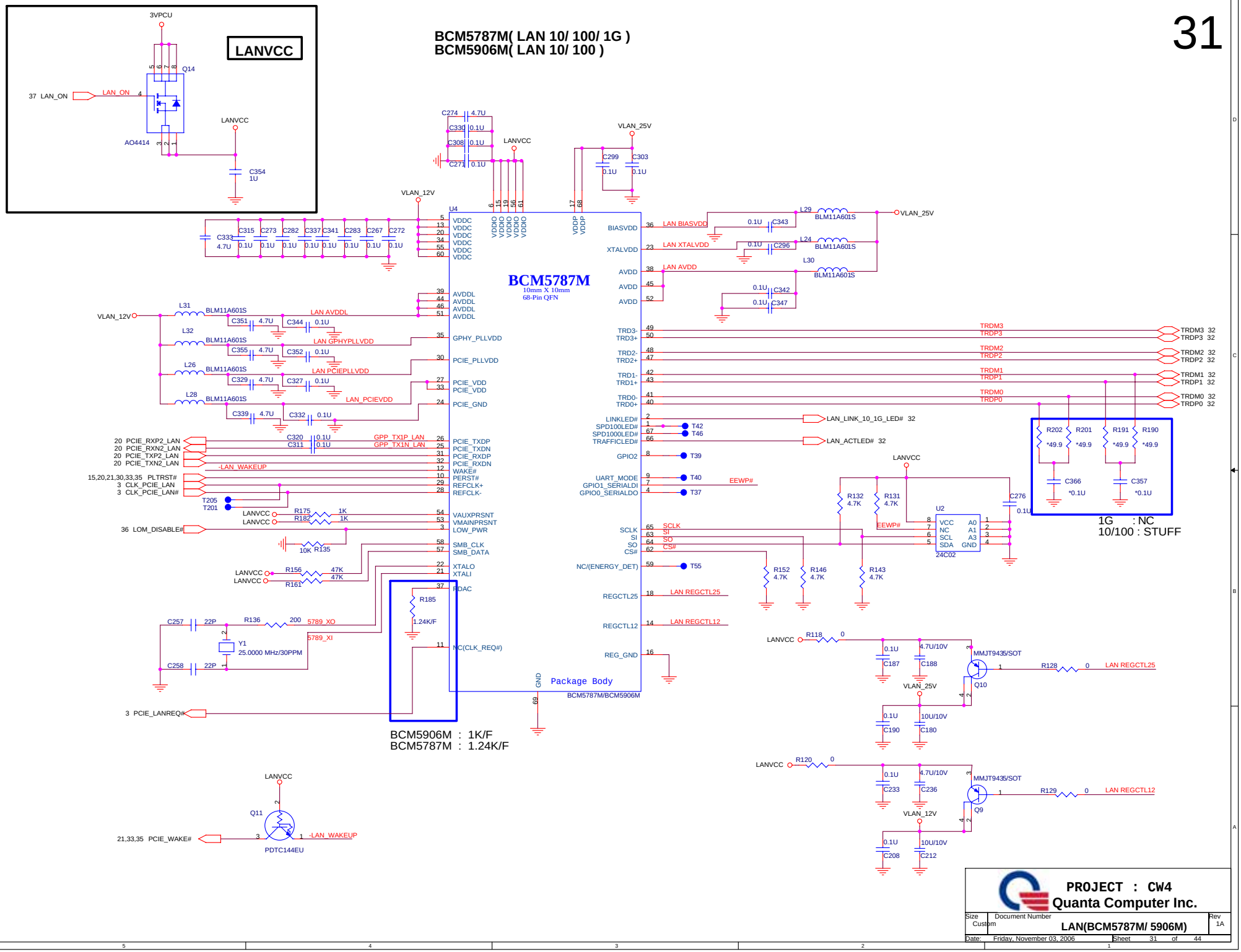
BCM5787M(LAN 10/ 100/ 1G)
BCM5906M(LAN 10/ 100)



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Quanta Computer Inc.			
Size: Custom	Document Number: LAN(BCM5787M/ 5906M)		Rev: 1A
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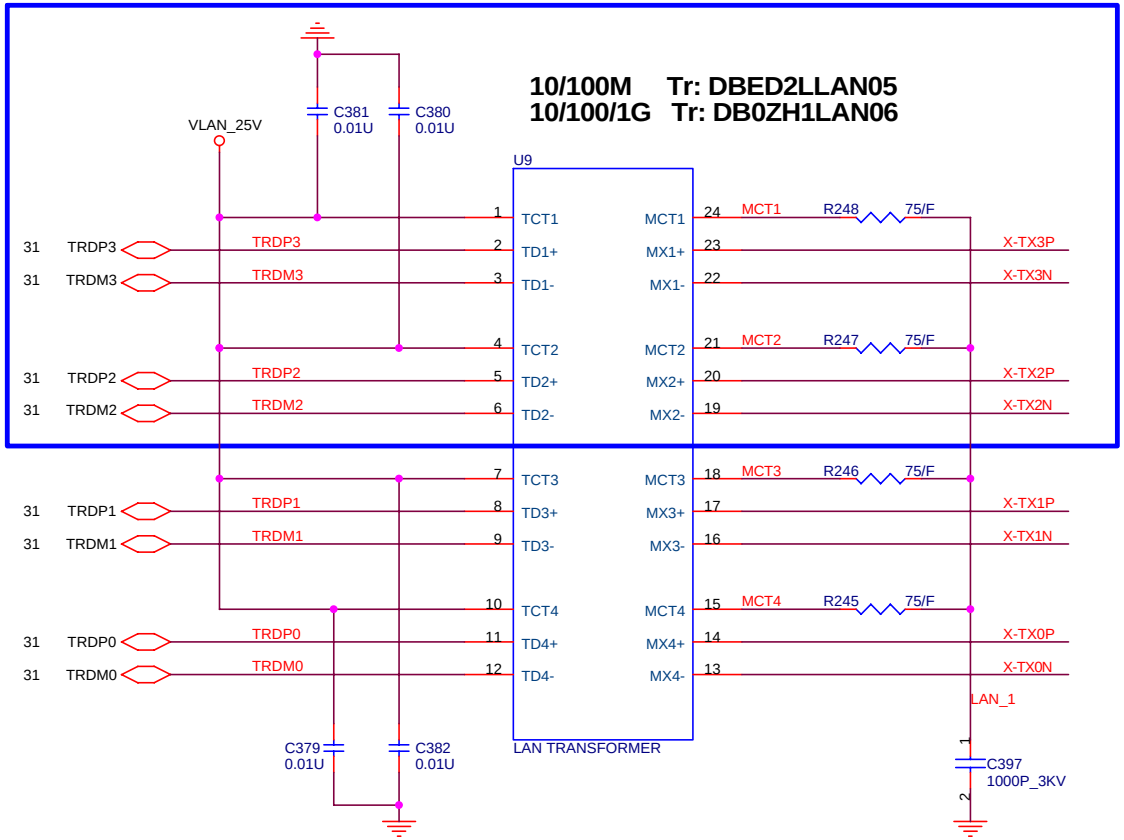
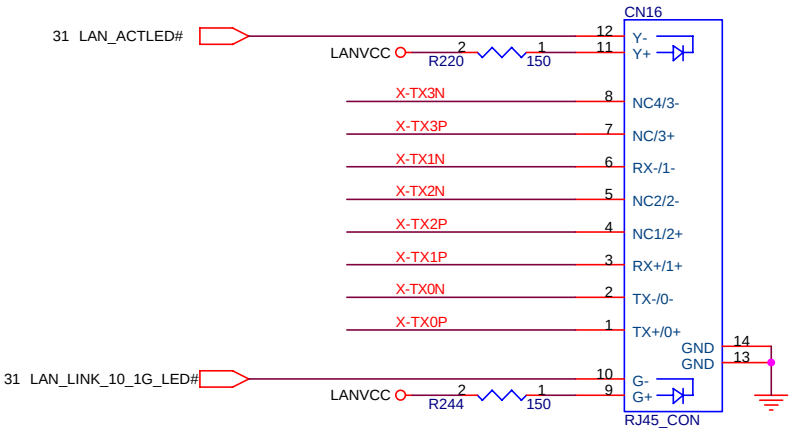
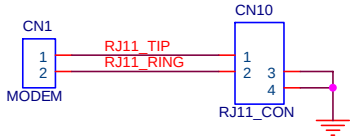
RJ45 Connector







PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RJ11/RJ45 CONNECTOR	1A
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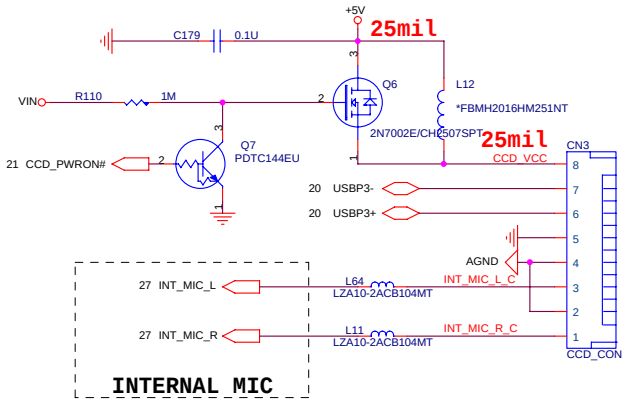
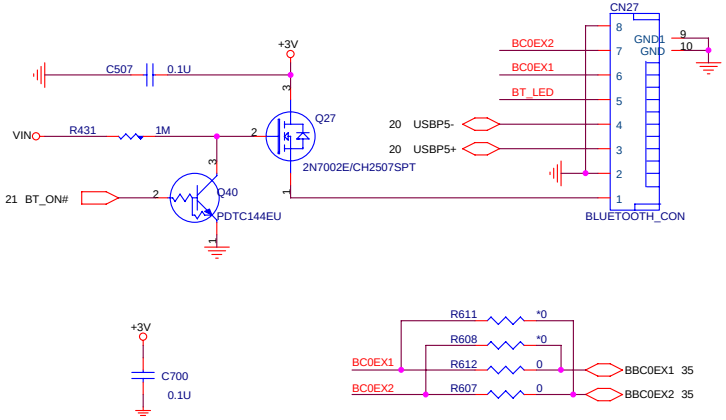
CCD MODULE

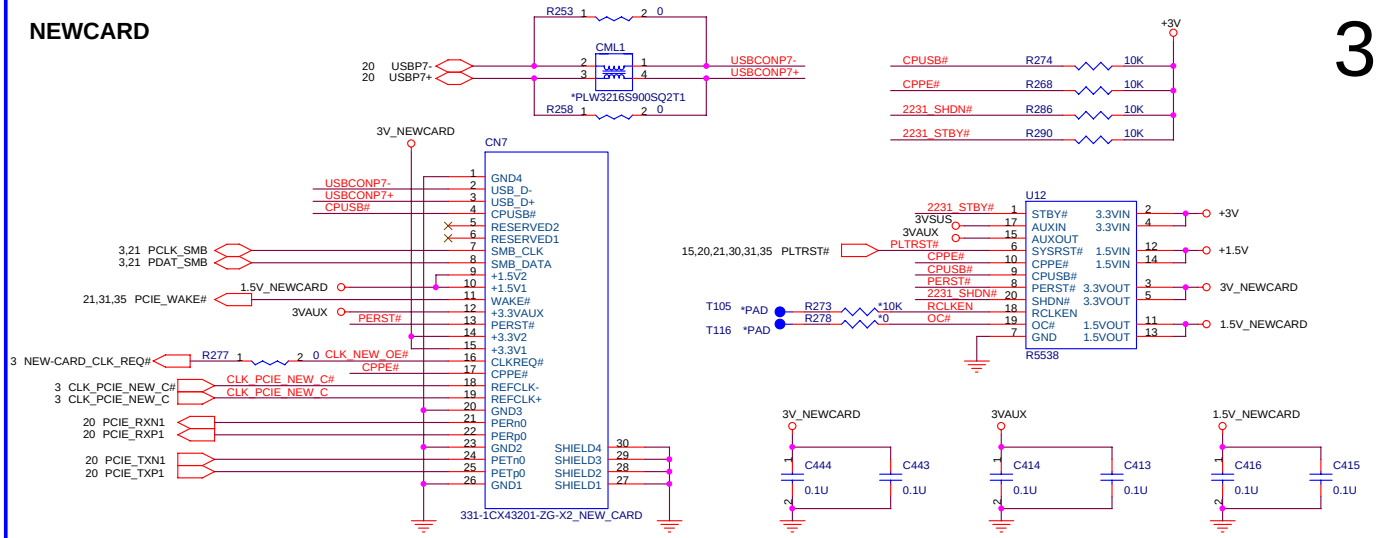


	High	Low
CCD_PWRON#	Disable	Enable

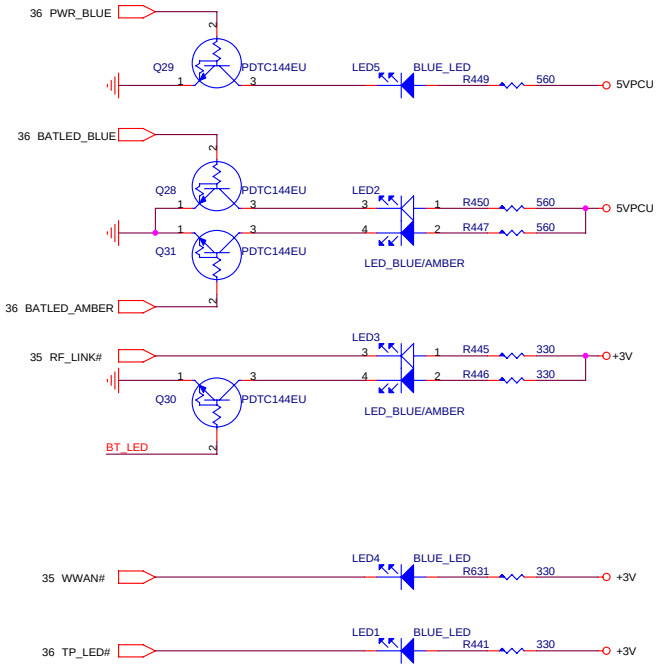
BLUETOOTH



NEWCARD



LED



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CCD, NEW CARD, B/T, LED	1A

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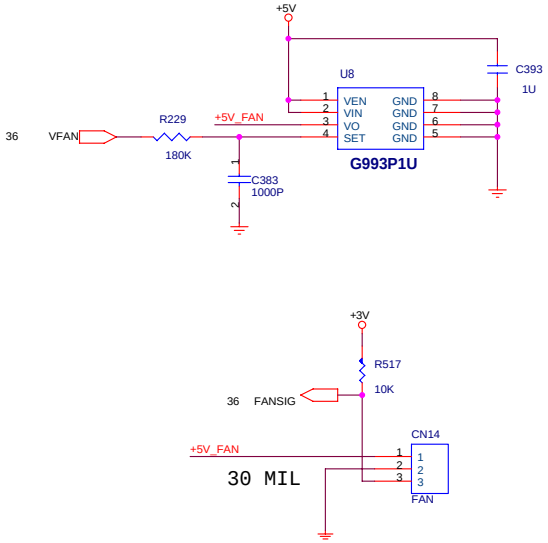
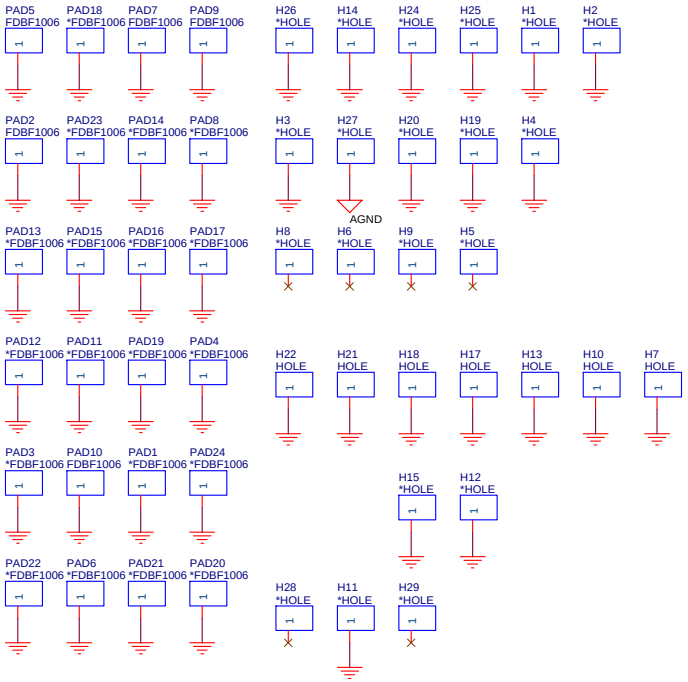
FAN CONTROL

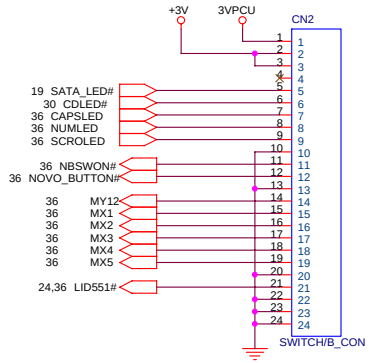


EMI PAD

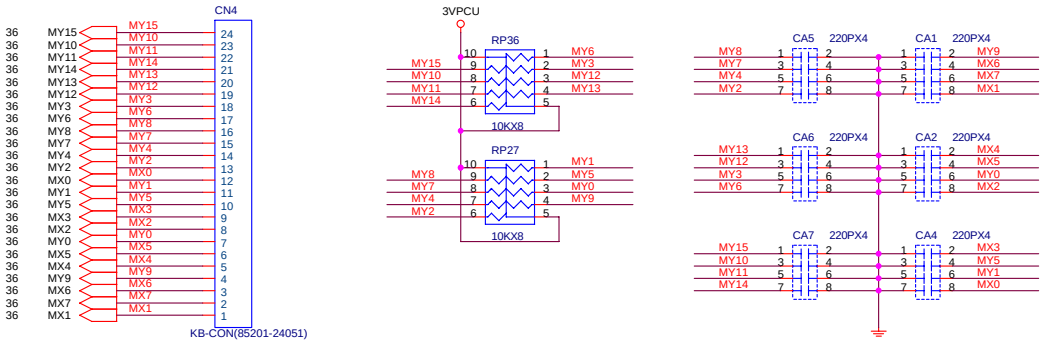


HOLES

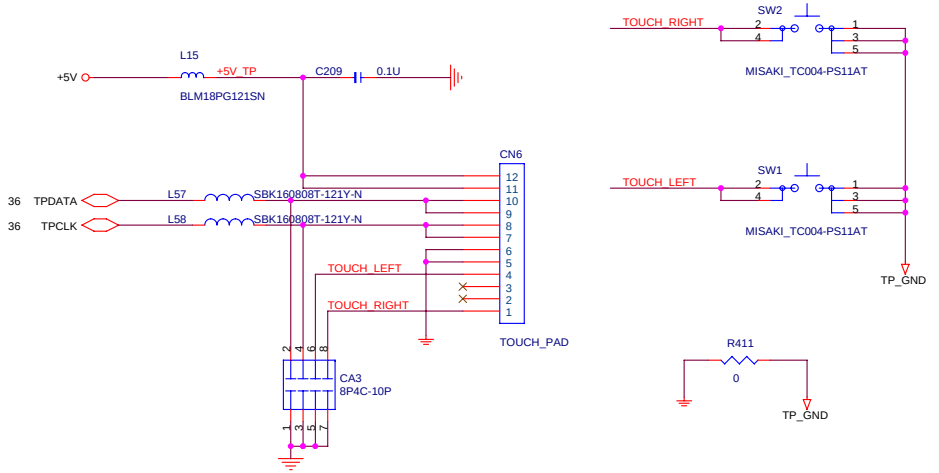
SWITCH BOARD CON.



KEYBOARD



TOUCH PAD



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Quanta Computer Inc.		
Size: Custom	Document Number: T/P,FAN,KB,T/B CON	Rev: 1A
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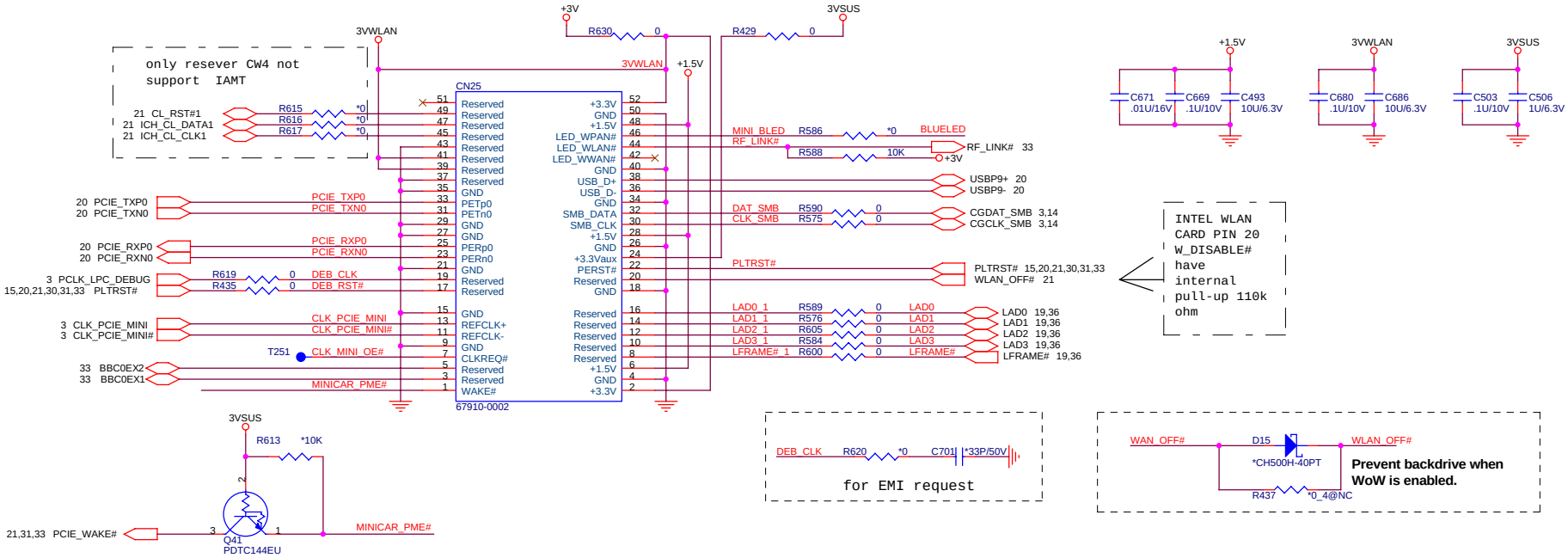
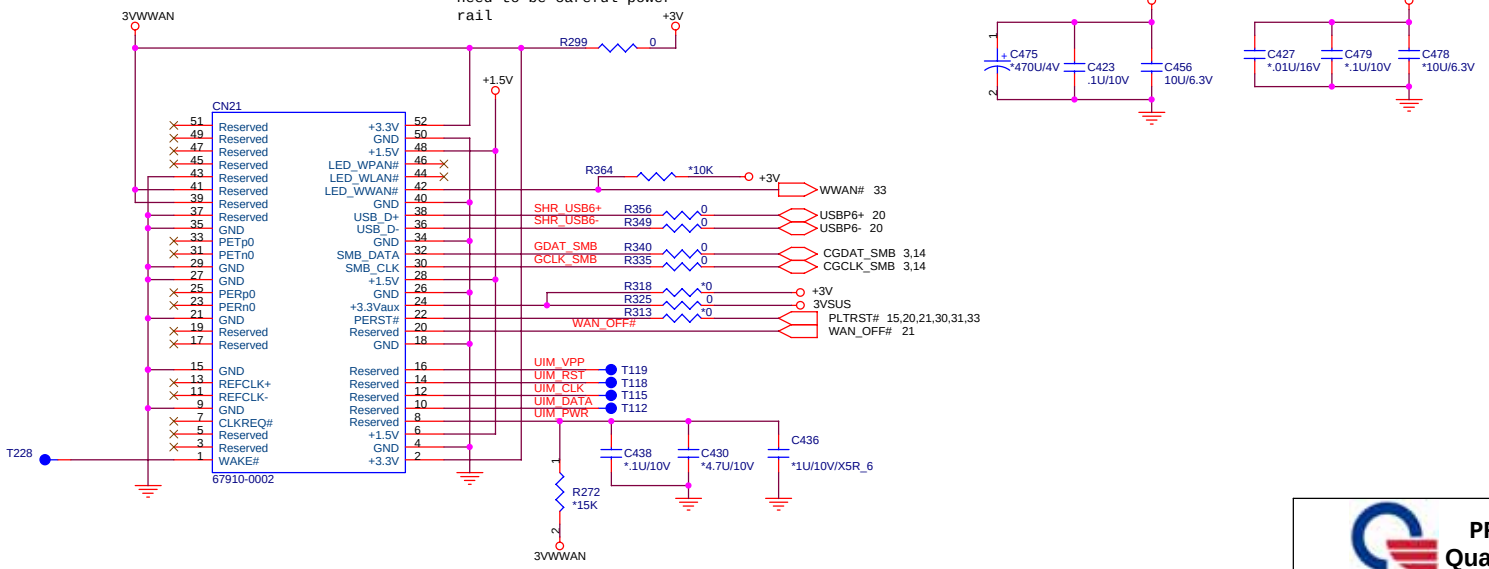
Mini PCI-E Card 1
WLAN



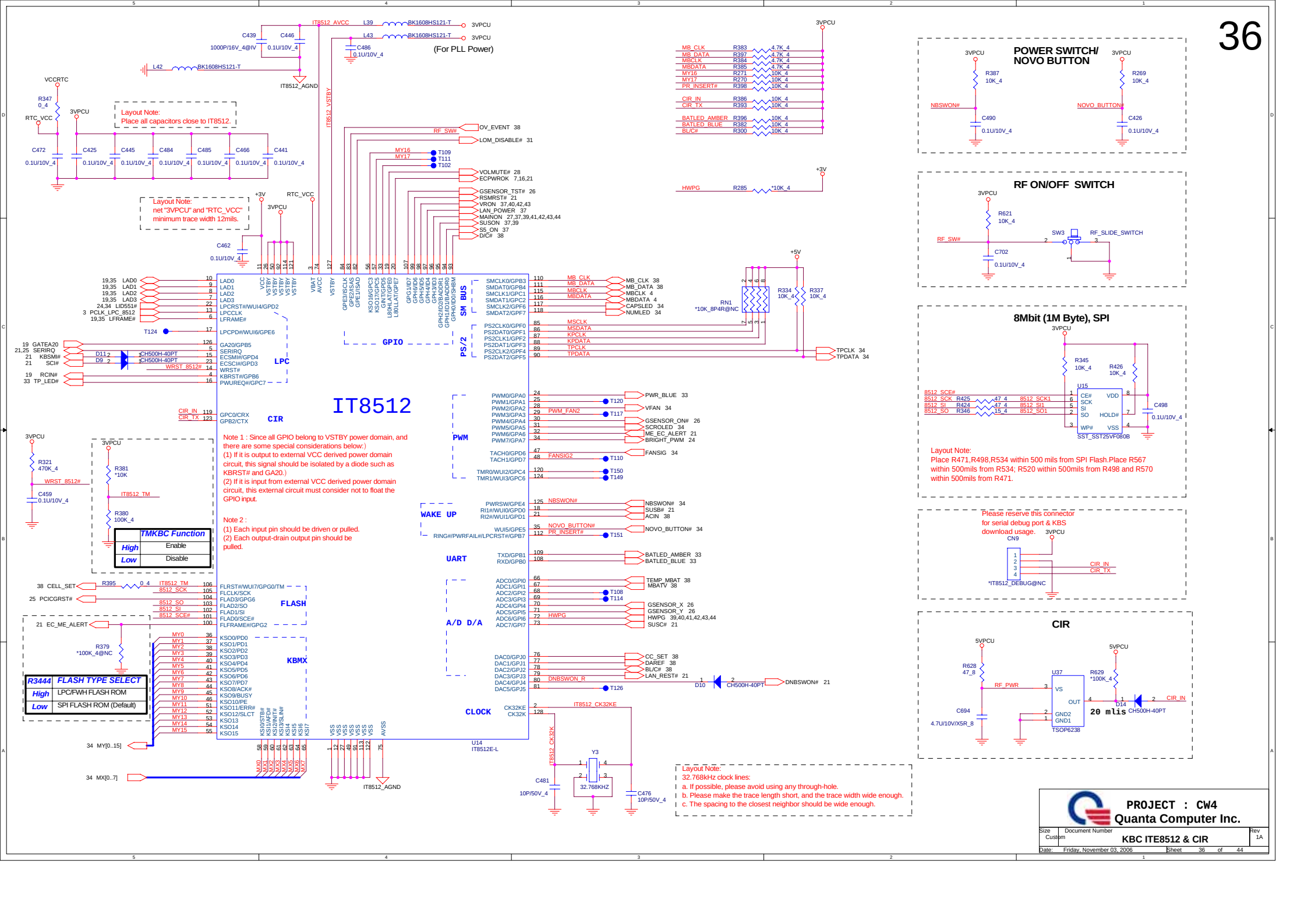
Mini PCI-E Card 2
WWAN(W/SIM)

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN & WWAN CON	1A
Date: Friday, November 03, 2006	Sheet 35 of 44	


IT8512
(For PLL Power)
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:)
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.)
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
TMKBC Function
High Enable
Low Disable
R3444 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
POWER SWITCH/ NOVO BUTTON
RF ON/OFF SWITCH
8Mbit (1M Byte), SPI
Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.
Please reserve this connector for serial debug port & KBS download usage.
CIR
PROJECT : CW4
Quanta Computer Inc.
KBC ITE8512 & CIR
Size Custom
Document Number
Rev 1A
Date: Friday, November 03, 2006
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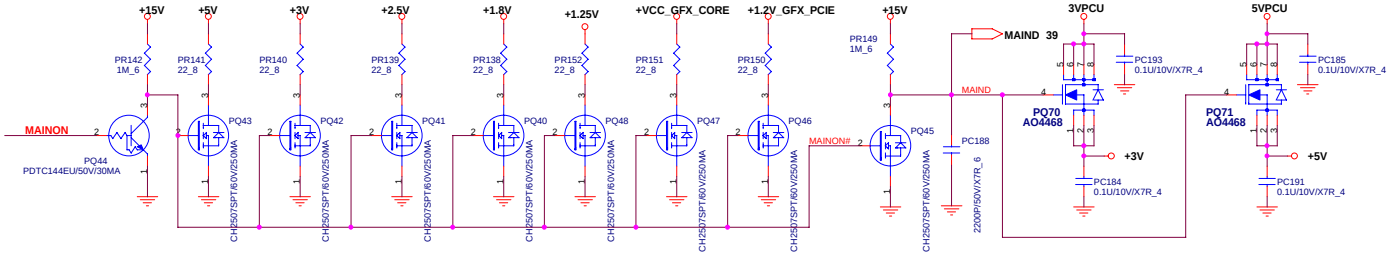
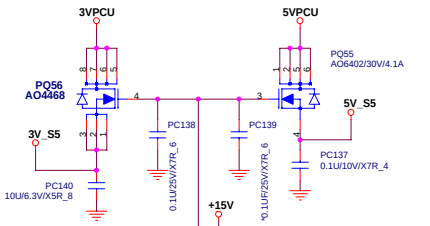
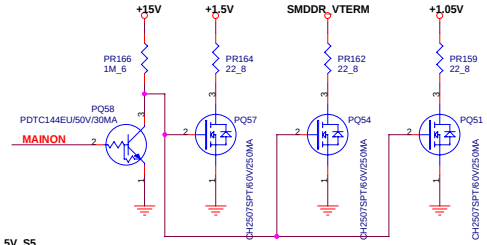
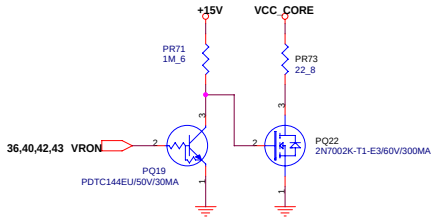
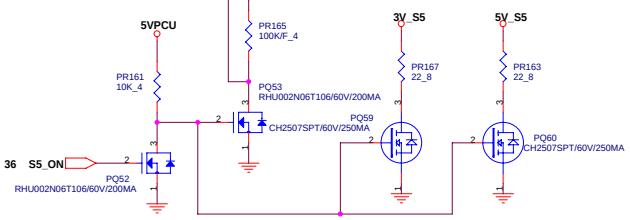
DISCHARGE

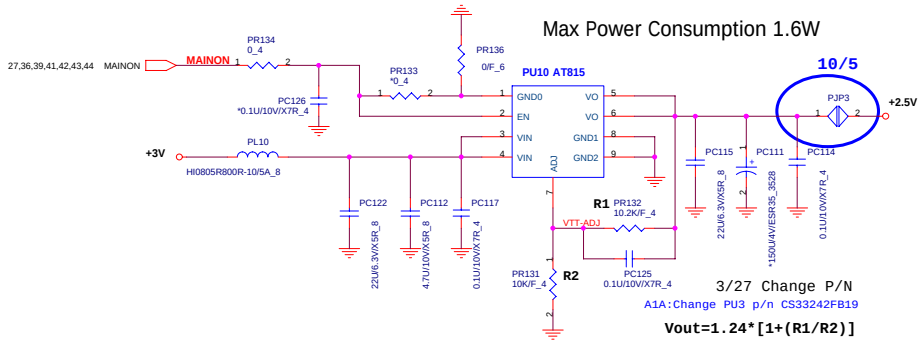


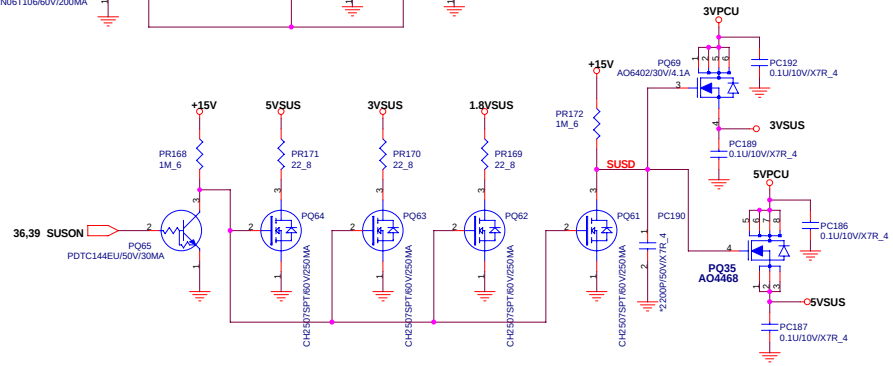


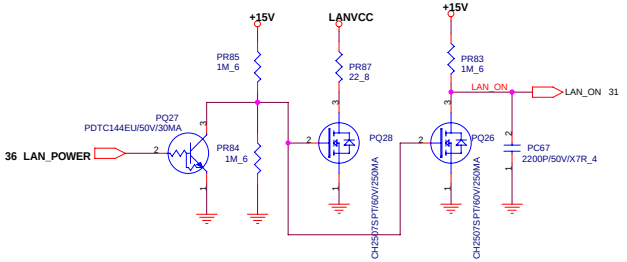












PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
C	DISCHARGE CIRCUIT	1A

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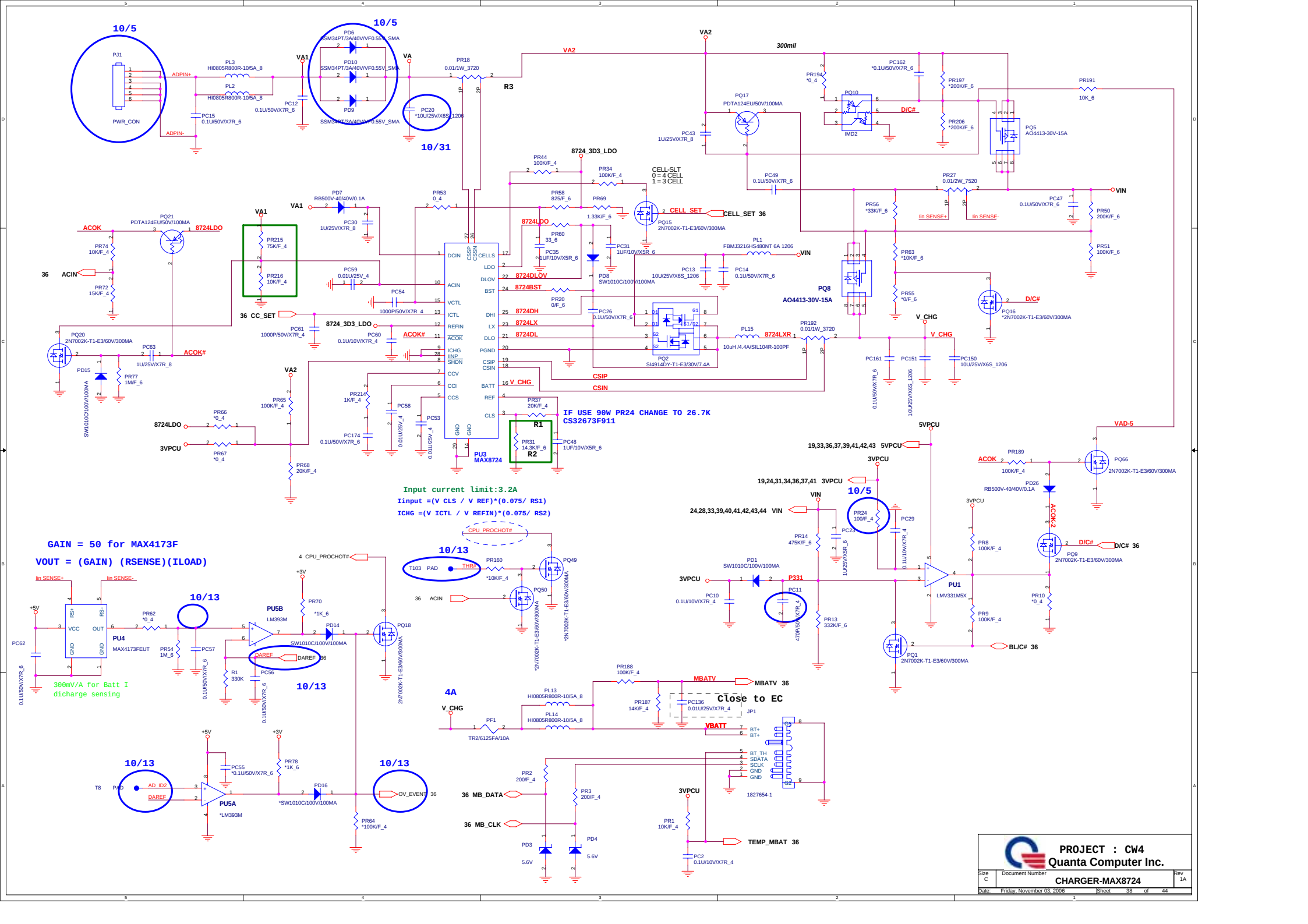

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Quanta Computer Inc.

Size	Document Number	Rev
C	CHARGER-MAX8724	1A

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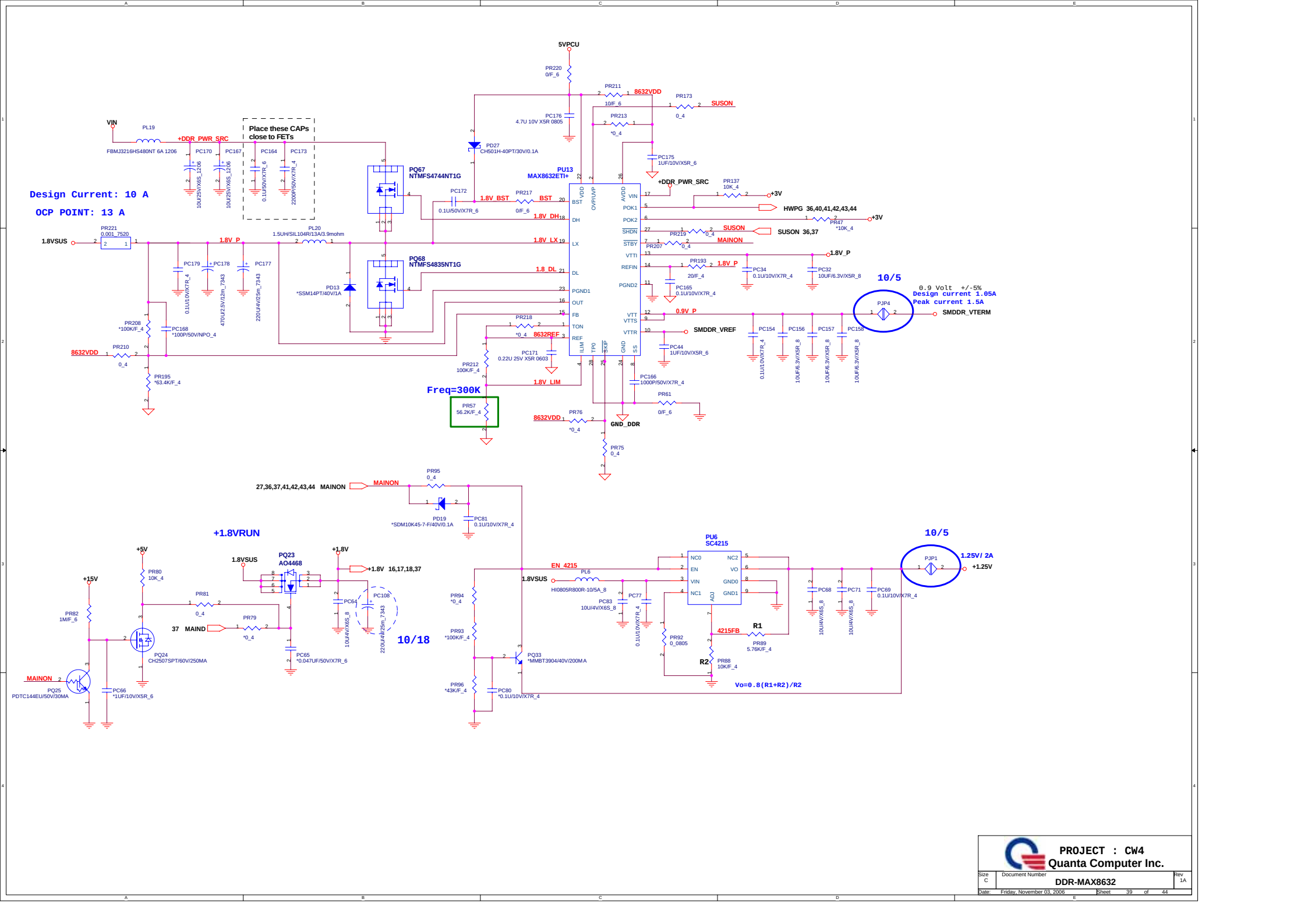
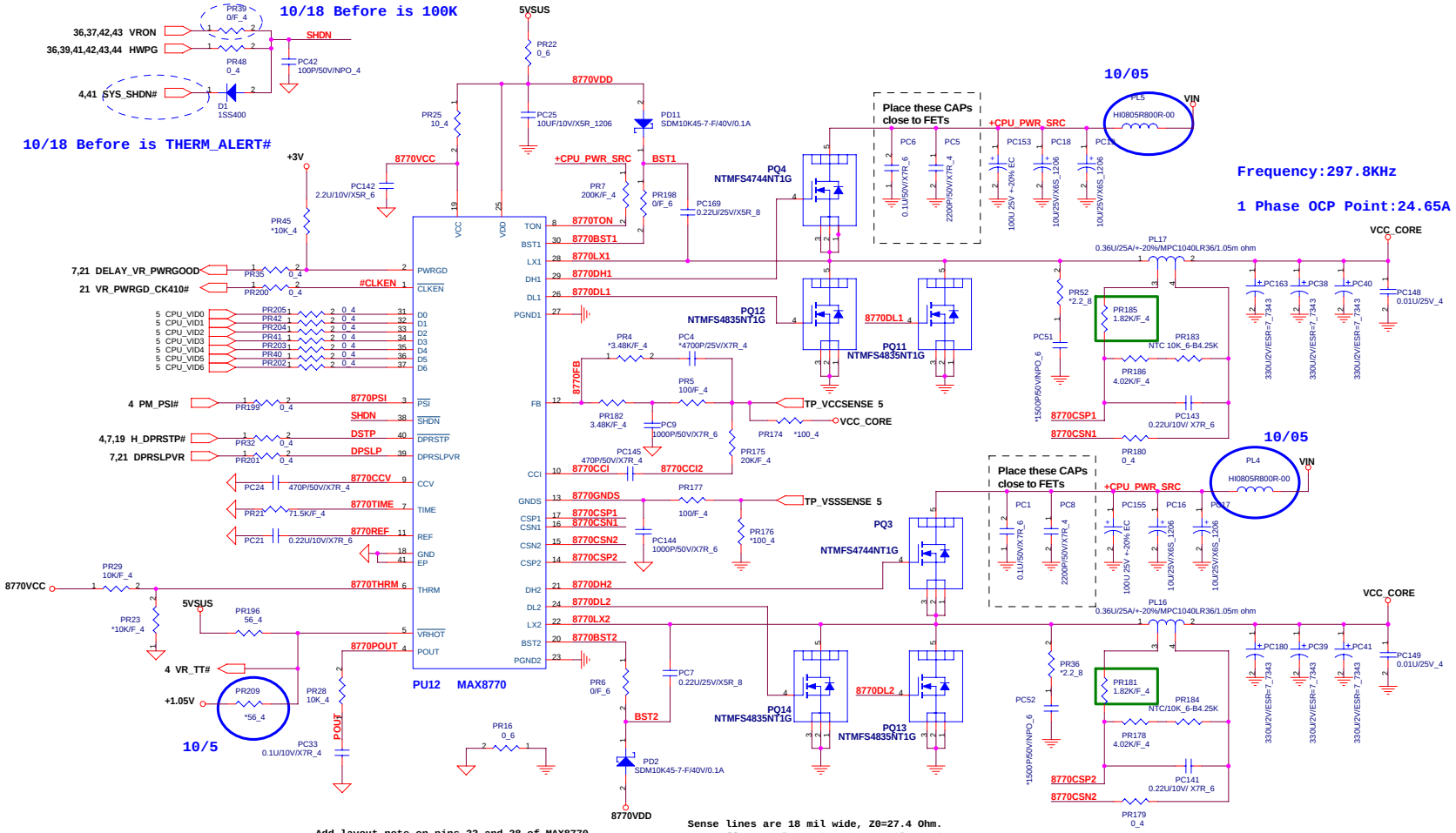

Design Current: 10 A
OCP POINT: 13 A
Place these CAPs close to FETs
Freq=300K
10/5
10/18
+1.8VRUN
Design current 1.05A
Peak current 1.5A
0.9 Volt +/-5%
1.25V/ 2A
Vo=0.8(R1+R2)/R2
PROJECT : CW4
Quanta Computer Inc.
DDR-MAX8632
Friday, November 03, 2006



PROJECT : CW4 Quanta Computer Inc.			
Size C	Document Number CPU Core (MAX8770)		Rev 1A
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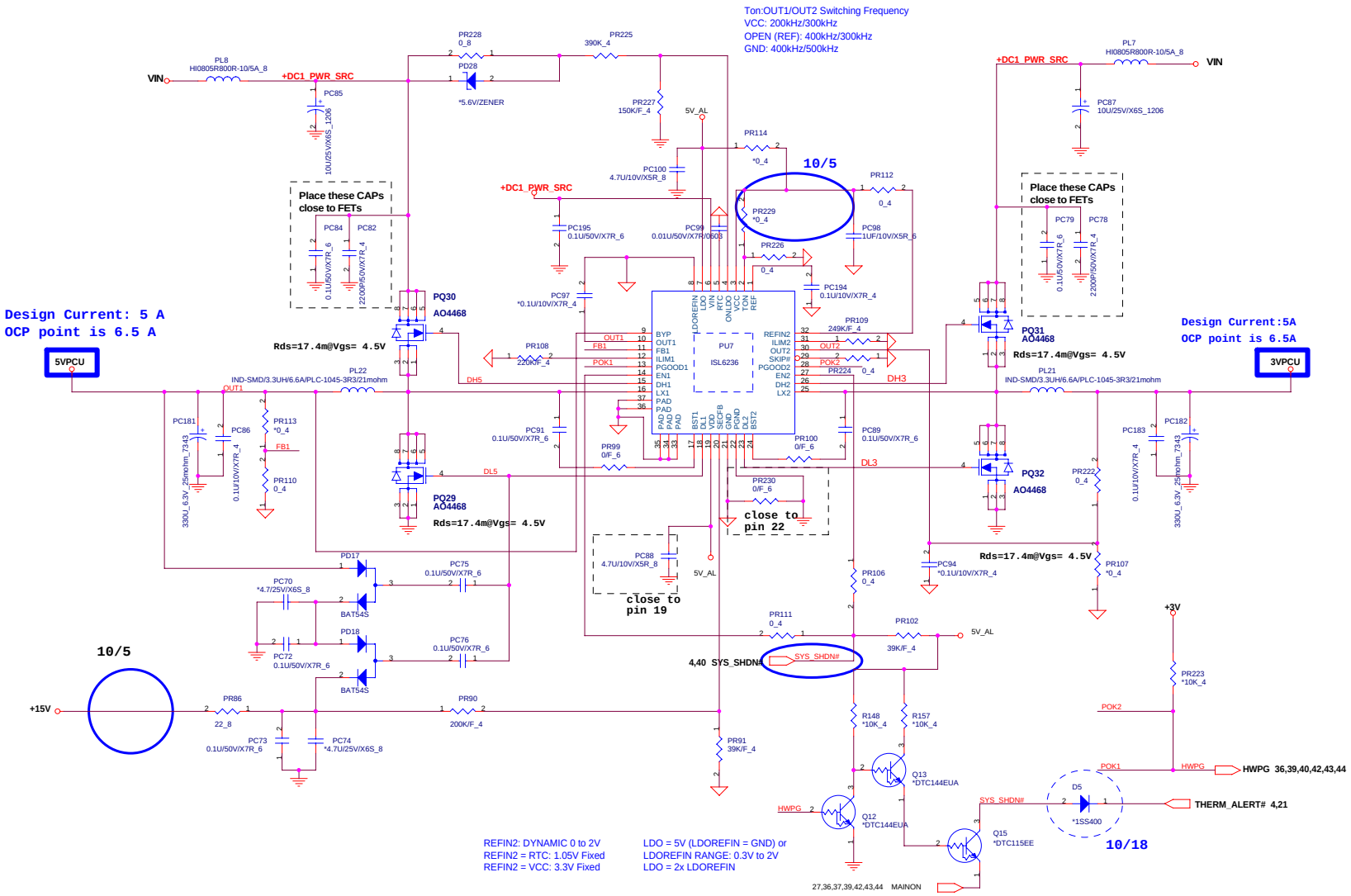
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
C	DC TO DC-ISL6236	1A

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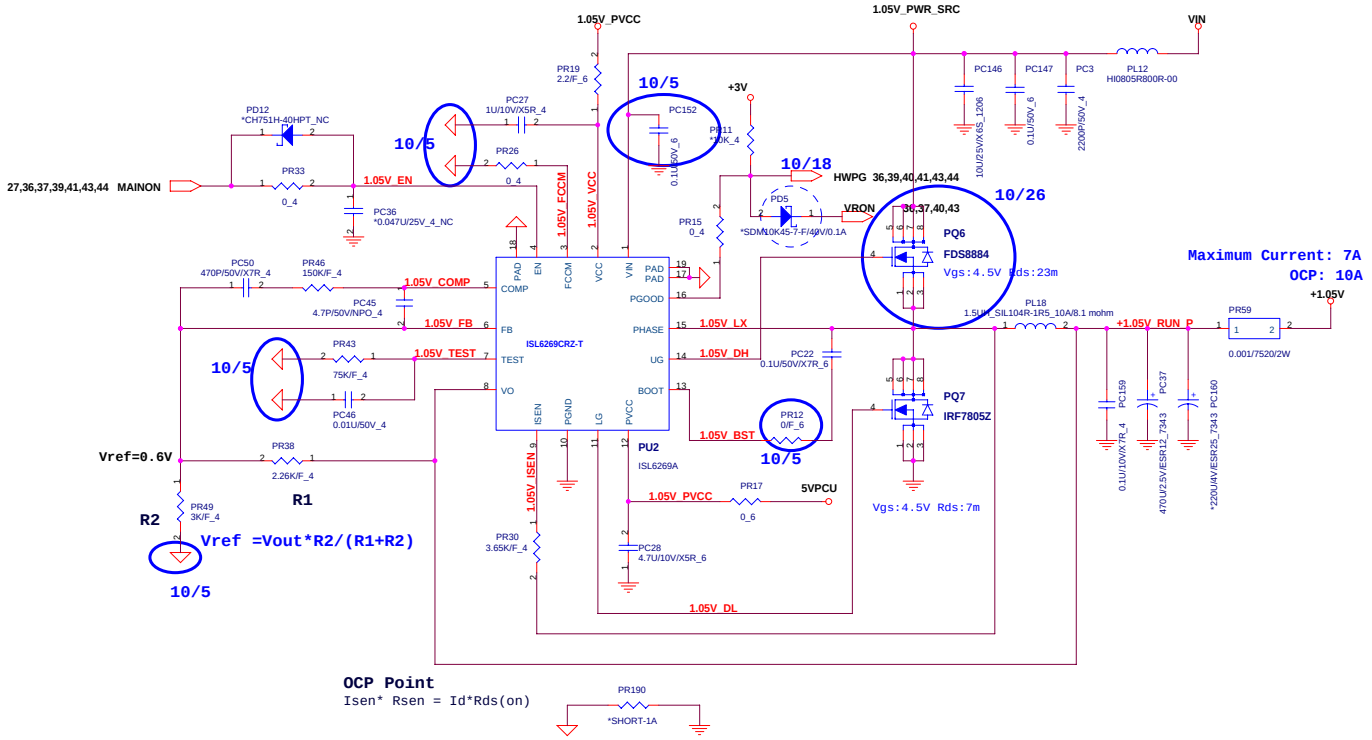

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
C	1.05V-ISL6269A	1A

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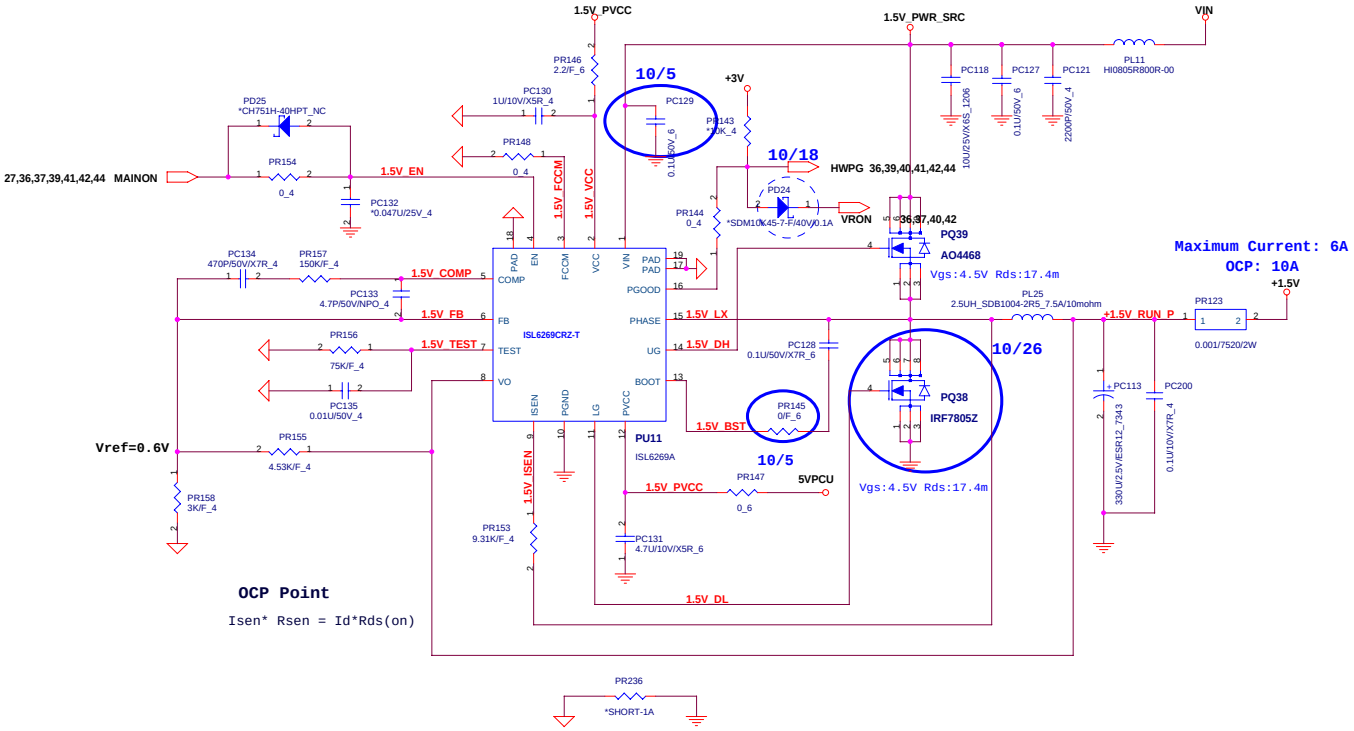

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
C	1.5V-ISL6269A	1A

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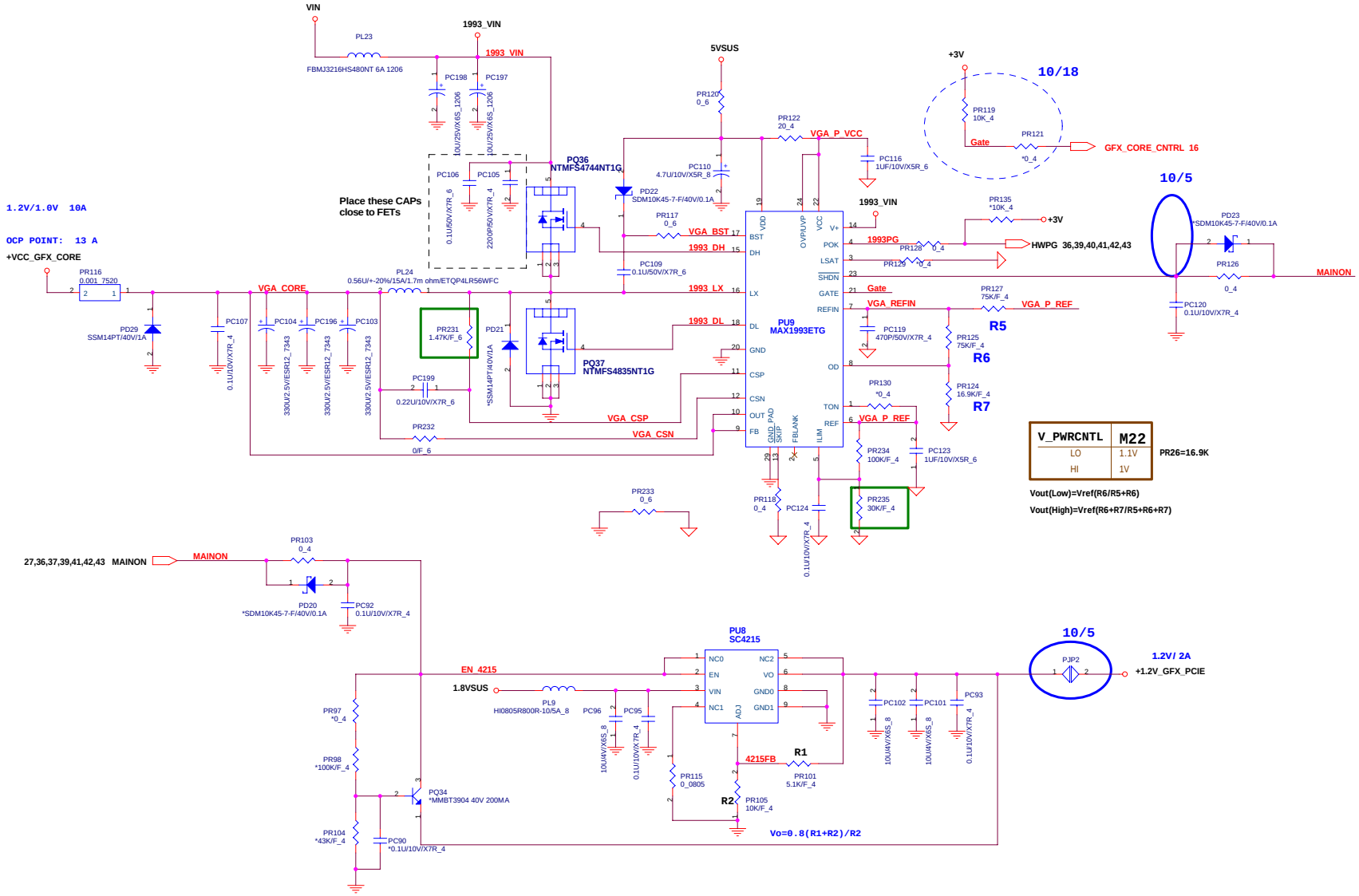

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Quanta Computer Inc.	
Size: C	Document Number: VGA (MAX1993)
Rev: 1A	
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