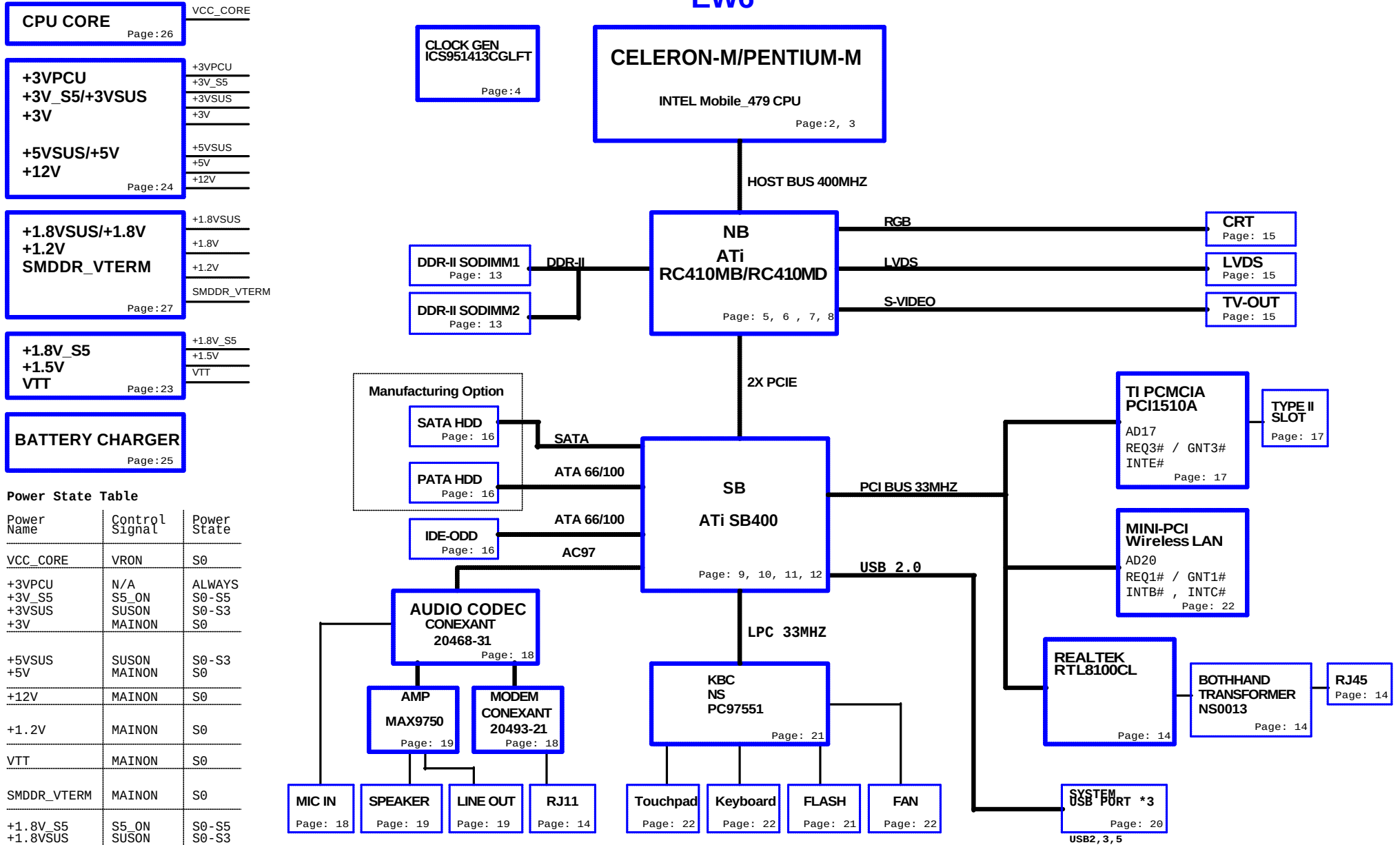


EW6



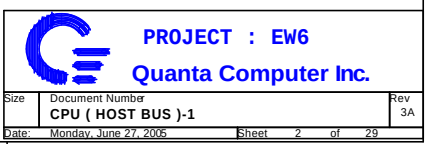
Power State Table

Power Name	Control Signal	Power State
VCC_CORE	VRON	S0
+3VPCU	N/A	ALWAYS
+3V_S5	S5_ON	S0-S5
+3VSUS	SUSON	S0-S3
+3V	MAINON	S0
+5VSUS	SUSON	S0-S3
+5V	MAINON	S0
+12V	MAINON	S0
+1.2V	MAINON	S0
VTT	MAINON	S0
SMDDR_VTERM	MAINON	S0
+1.8V_S5	S5_ON	S0-S5
+1.8VSUS	SUSON	S0-S3
+1.8V	MAINON	S0
+1.5V	MAINON	S0

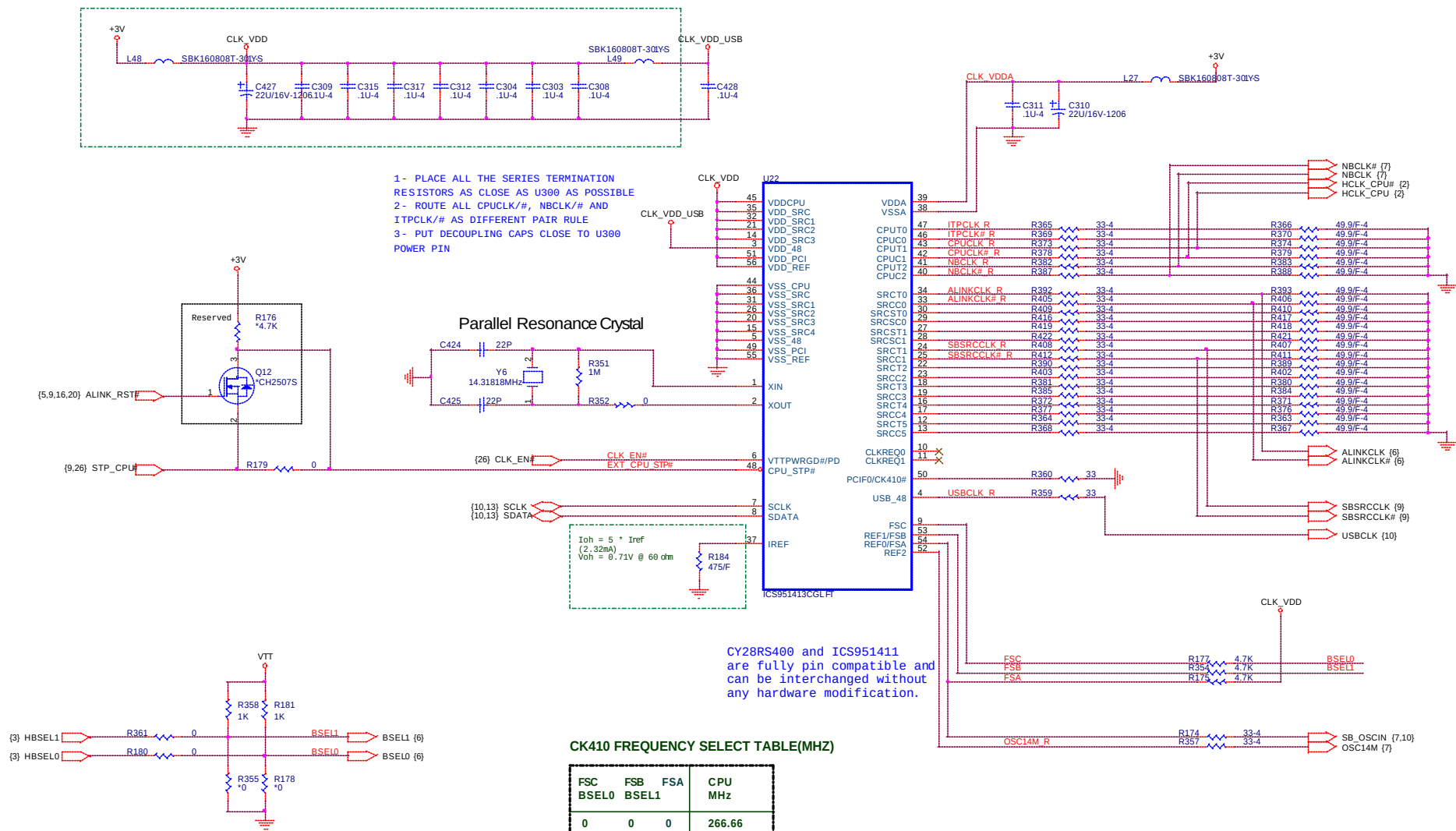


PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date:	Monday, June 27, 2006	Sheet 1 of 29



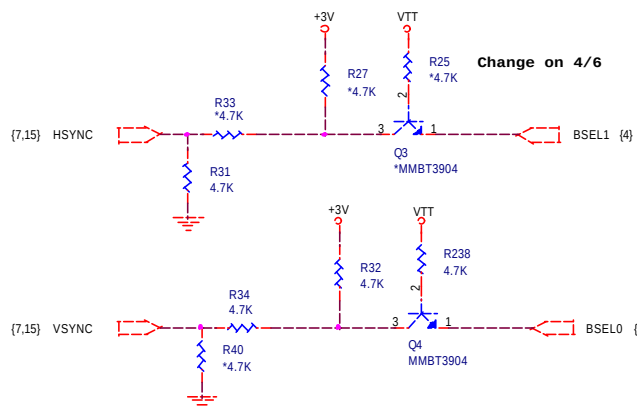
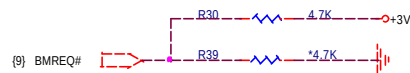
CLK



CY28RS400 and ICS951411 are fully pin compatible and can be interchanged without any hardware modification.

HBSEL1	HBSEL0	
0	0	133 MHz
0	1	100 MHz



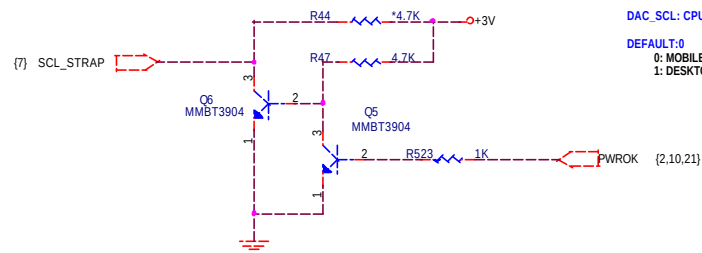


Change on 4/6

BSEL1	BSEL0	
0	0	133 MHz
0	1	100 MHz

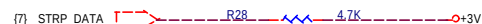
BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
DEFAULT: 101

101: 100 MHZ RC410MB
100: 133 MHZ RC410MD



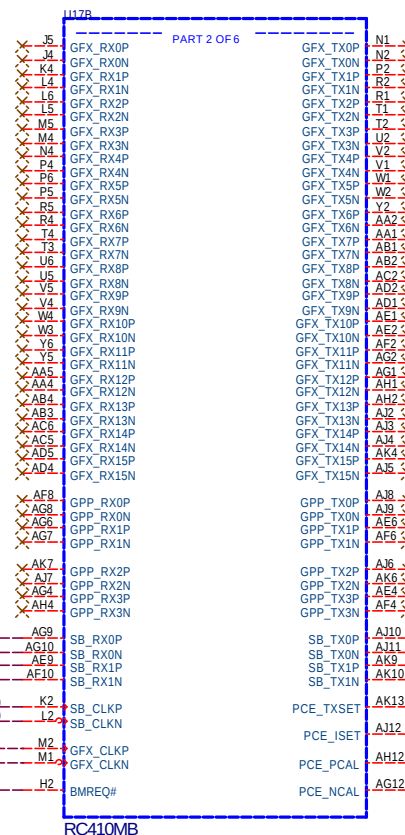
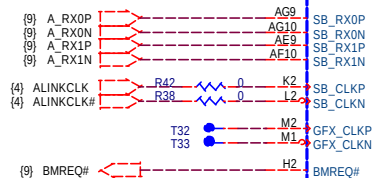
DAC_SCL: CPU VCC

DEFAULT: 0
0: MOBILE CPU
1: DESKTOP CPU



STRP_DATA: Debug strap

DEFAULT: 1
0: MEMORY CHANNEL STRAPING
1: EPROM STRAPING



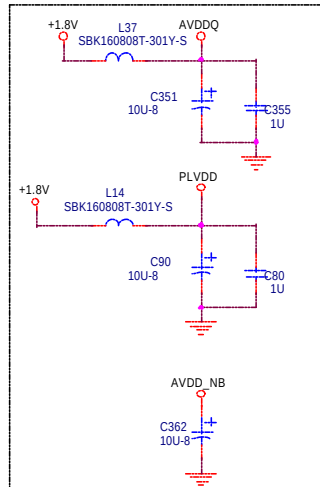
RC410MB



PROJECT : EW6
Quanta Computer Inc.

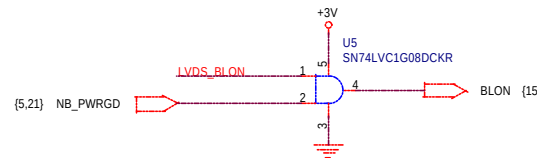
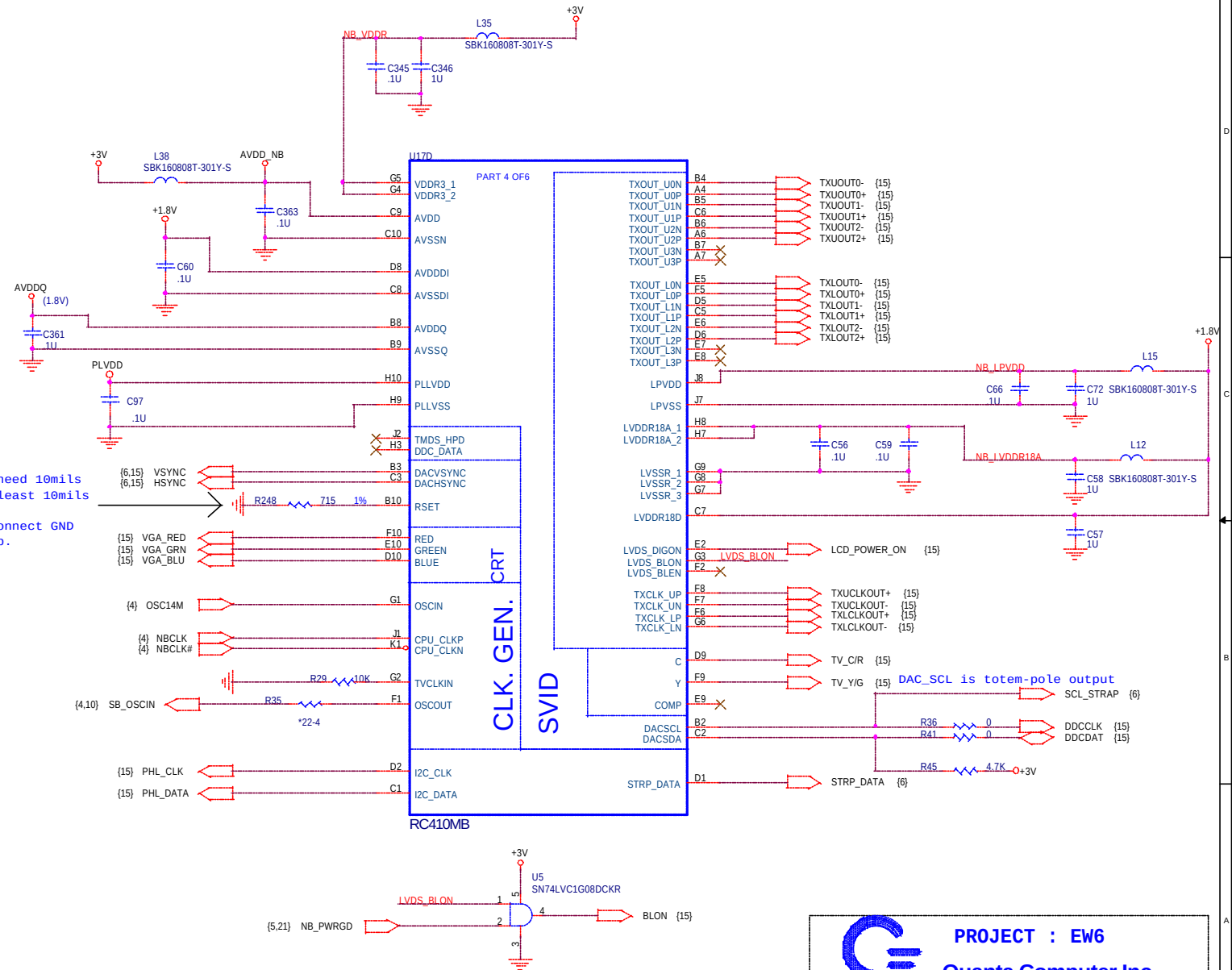
Size	Document Number	Rev
	RC400MB-PCIE LINK I/F	2A
Date	Monday, June 27, 2005	Sheet 6 of 29

CLG



PUT AVDD_NB, AVDDDI, AVDDQ, PLVDD DECOUPLING CAPS ON THE BOTTOM SIDE, CLOSE TO BALLS

RSET resistor need 10mils trace with at least 10mils spacing.
Also need to connect GND at AVSSQ HF cap.



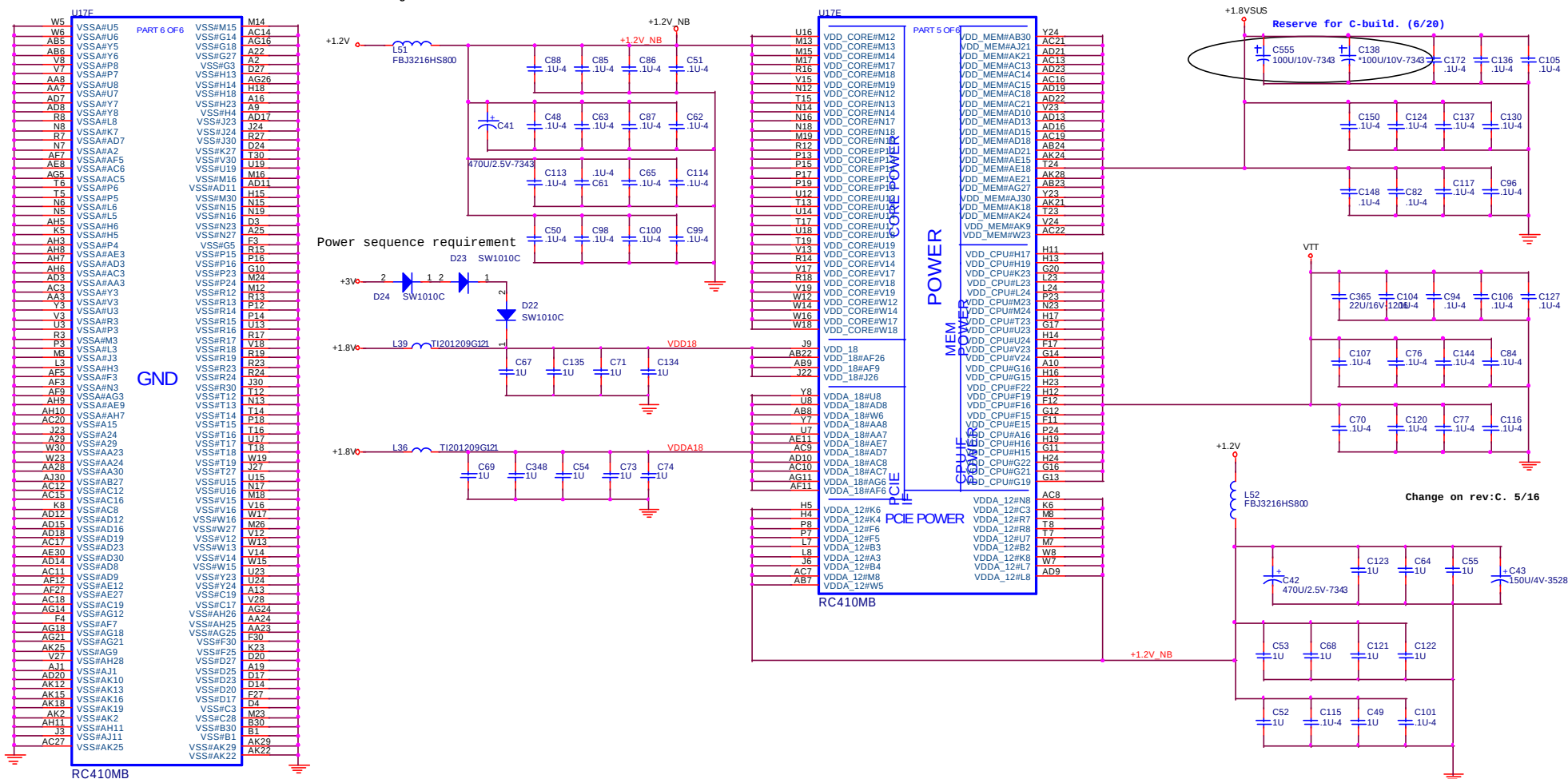
PROJECT : EW6

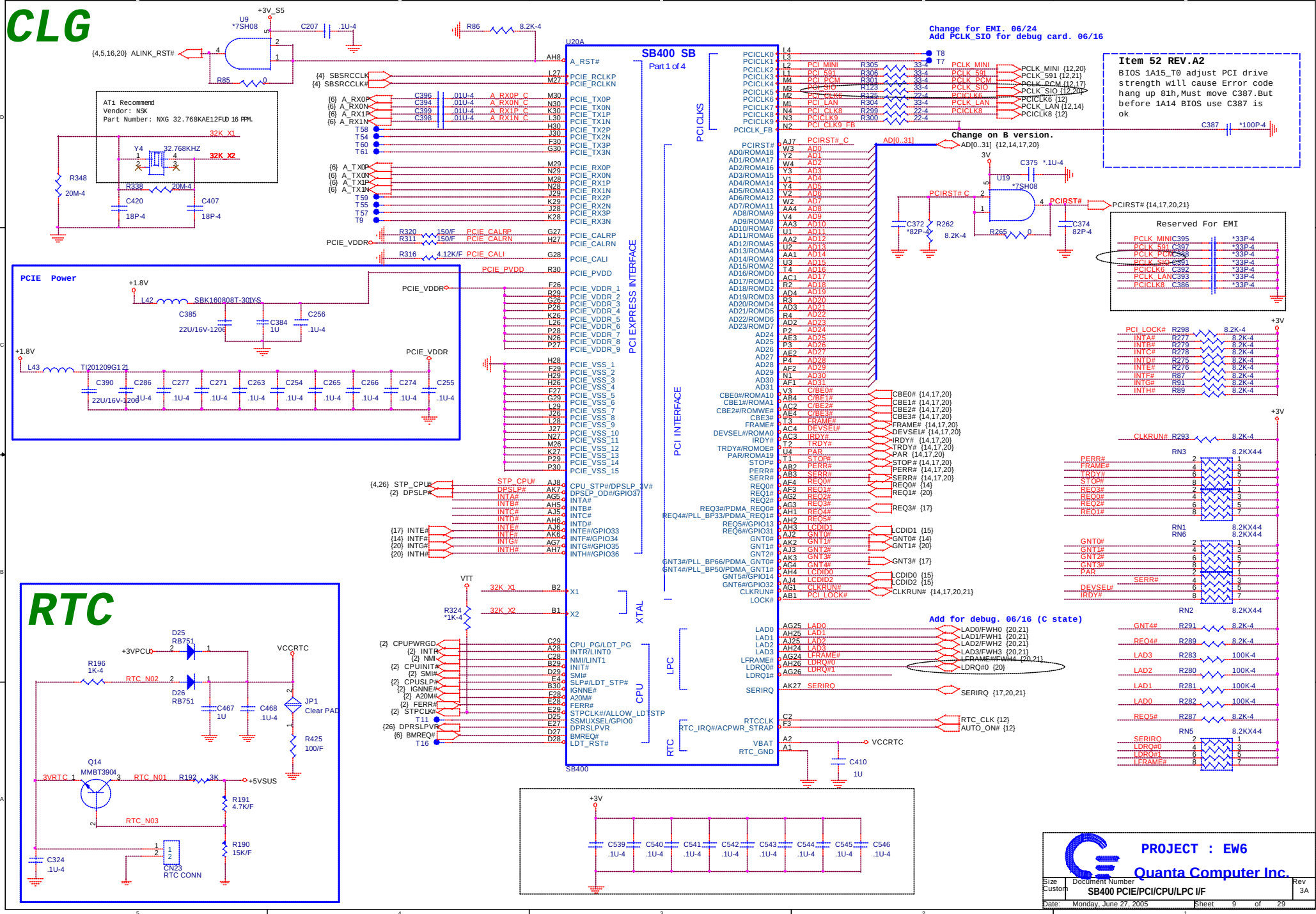
Quanta Computer Inc.

Size	Document Number	Rev
	RC400MB-VIDEO & CLKGEN	1B
Date:	Monday, June 27, 2005	Sheet 7 of 29

CLG

Change on rev:C. 5/16



CLG

PU/PD

H_THERMTRIP# R81 10K-4 +3V

PROCHOT# R153 10K-4 +3V_S5

EMAIL_LED# R166 4.7K-4

SUSB# R163 4.7K-4

SUSC# R162 4.7K-4

DNBSWON# R148 4.7K-4

TEMP_ALARM# R167 4.7K-4

PME# R164 4.7K-4

SWI# R165 10K-4

SCI# R161 10K-4

GPM7# R152 10K-4

GEVENTIS# R147 10K-4

ROM_CS#GPIO1 R156 4.7K-4

EXTENVNTJ# R333 4.7K-4

FPBACK# R164 4.7K-4

RST_THD0# R155 4.7K-4

SQATA R331 2.2K-4

SCLK R332 2.2K-4

GPIO11 R159 10K-4

GPIO3 R329 10K-4

GPIO8 R158 10K-4

GPIO9 R330 10K-4

PCSRV R334 10K-4

GPIO12 R160 10K-4

GPIO6 R161 10K-4

GPIO7 R335 4.7K-4

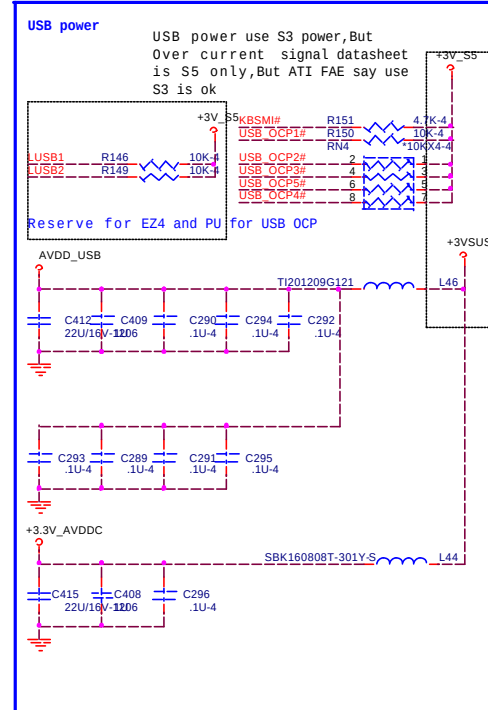
When using it as VGATE, connect it to VRMPG.

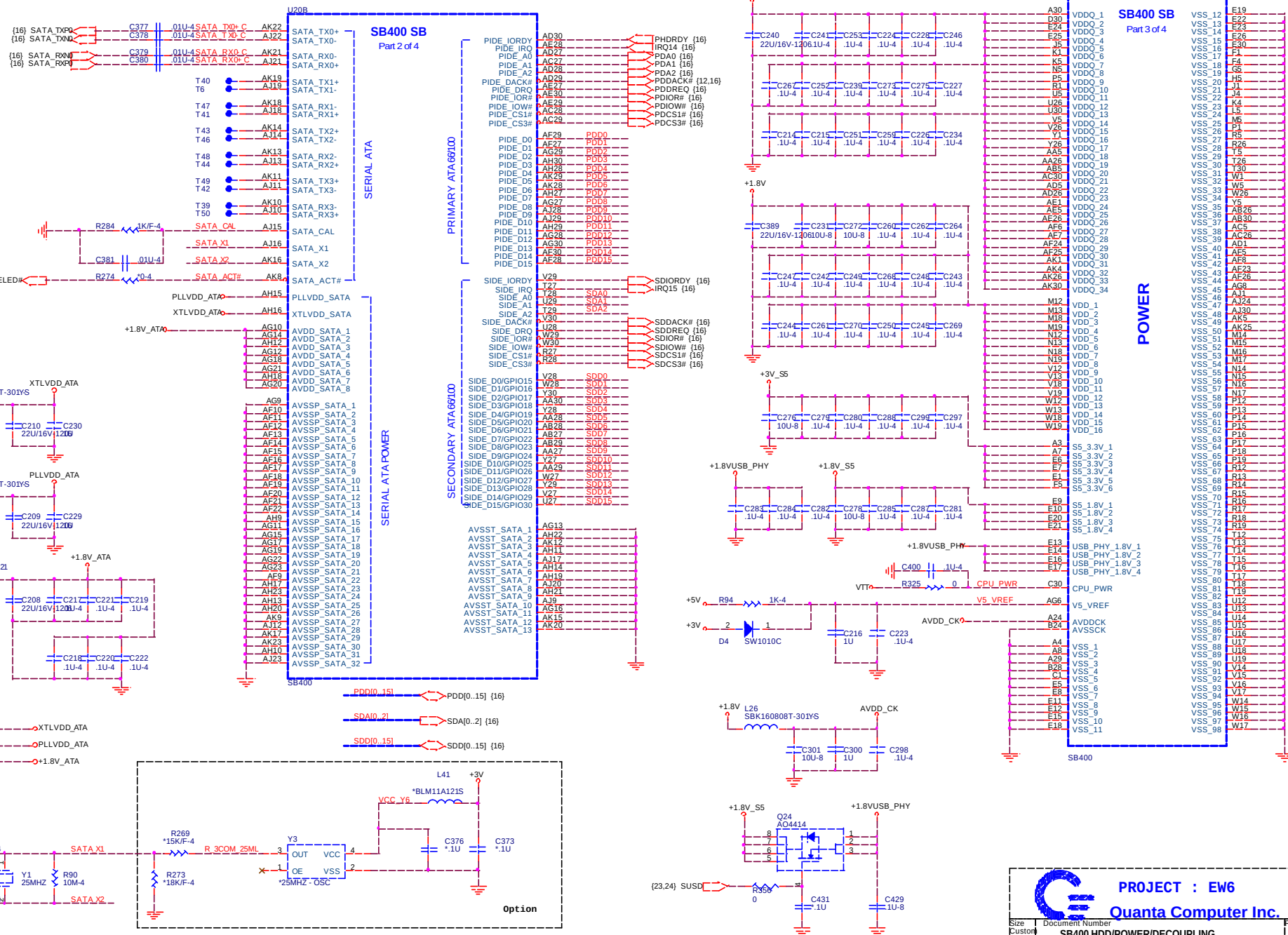
AC_SDIN2 R137 8.2K-4

AC_SDIN1 R138 10K-4

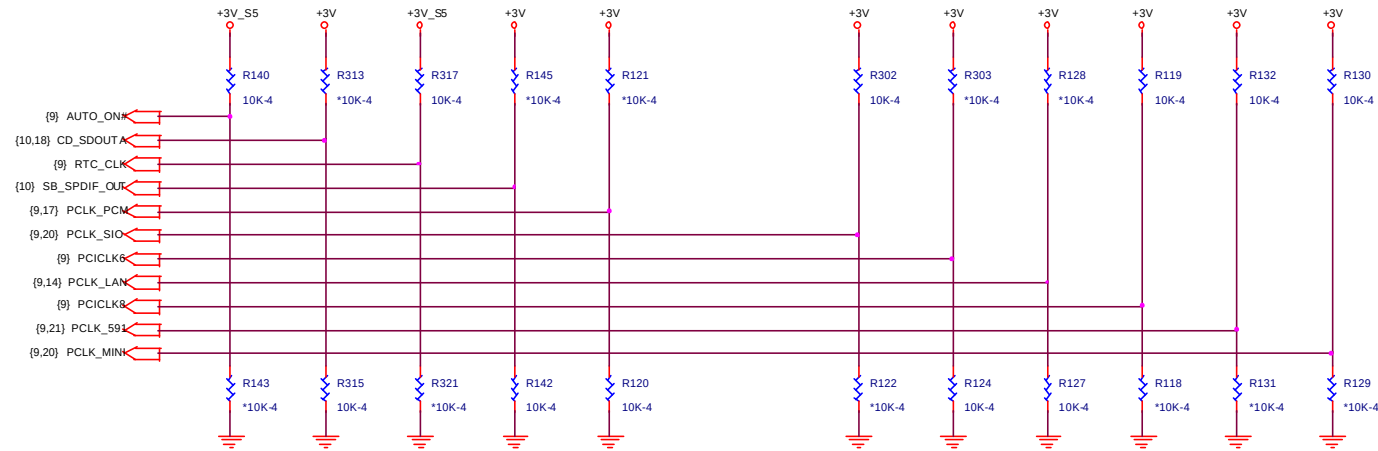
CO_SDINO R135 10K-4

AC_BITCLK_R R139 10K-4



CLG

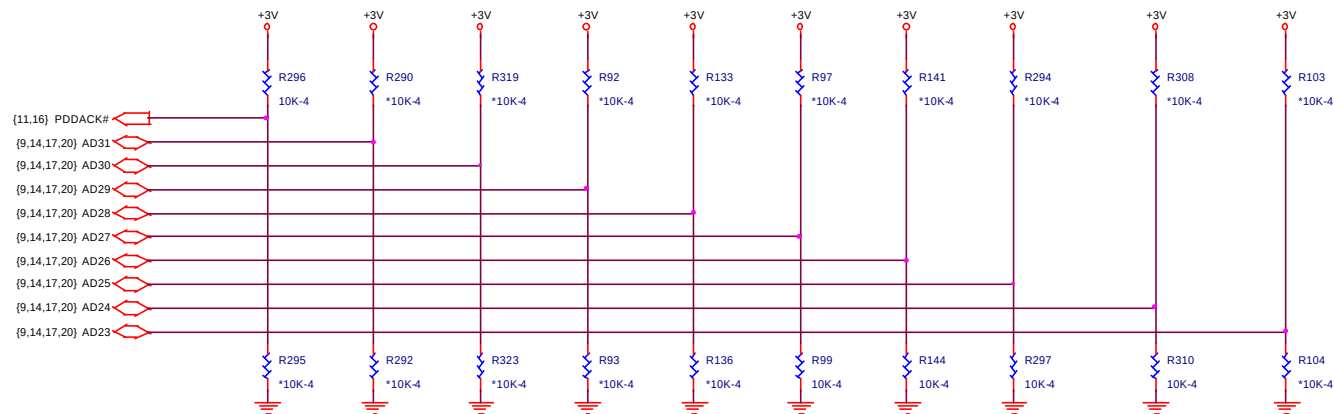
CLG



REQUIRED STRAPS

	ACPWRON	AC_SDO#	RTC_CLK	SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK3	PCI_CLK2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz use Internal PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8	H,H = PCI(X BUS) ROM L,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space) L,H = LPC ROM II (addresses mapped to below 1M) L,L = FWH ROM		USB PHY PWRDOWN DISABLE DEFAULT	48MHz OSC/Clock Buffer
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz use External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT			USB PHY PWRDOWN ENABLE	48MHz Crystal Pad DEFAULT

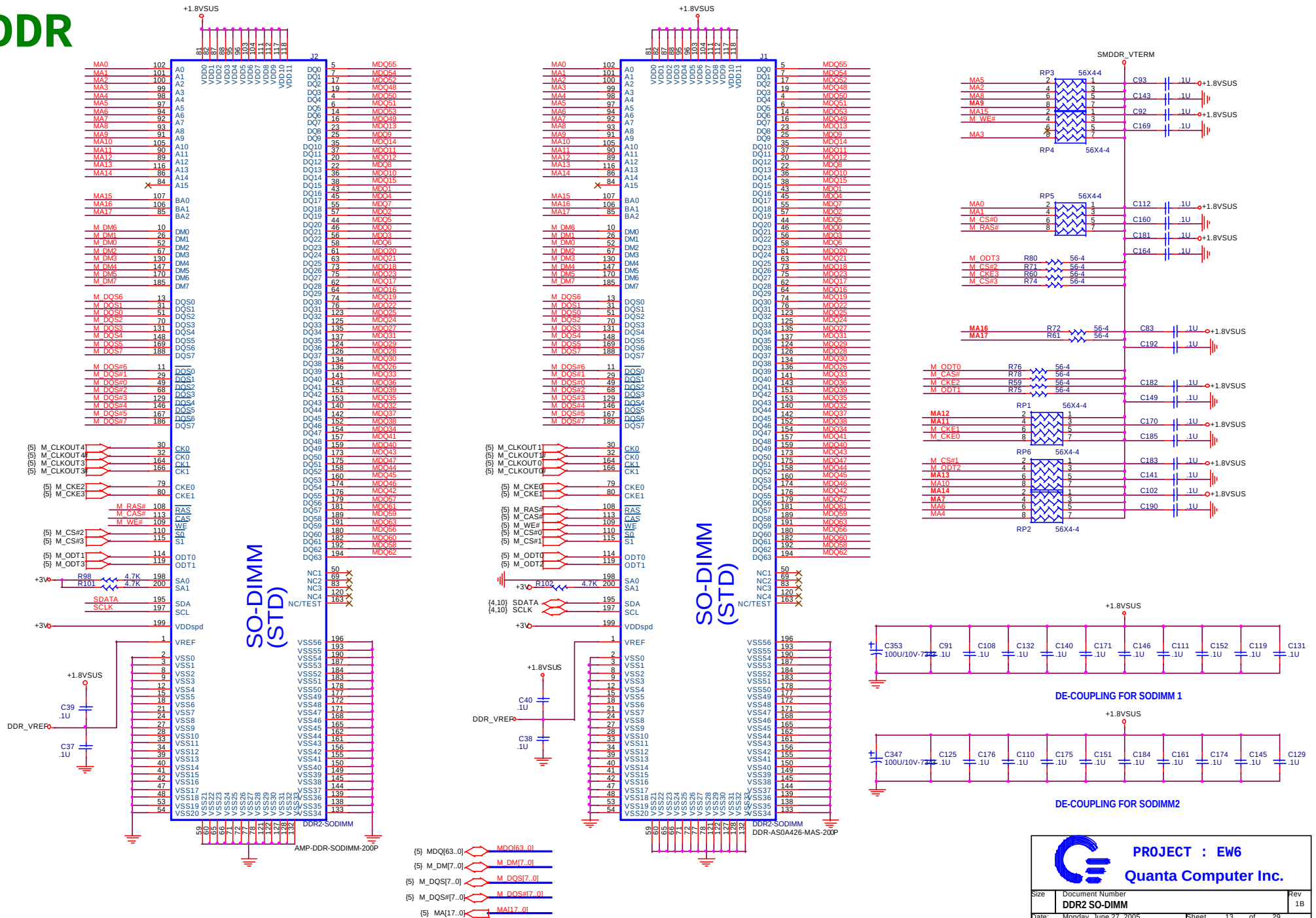
*This strap is only required if the strap on PCICLK4 is configured for External Clock.



DEBUG STRAPS

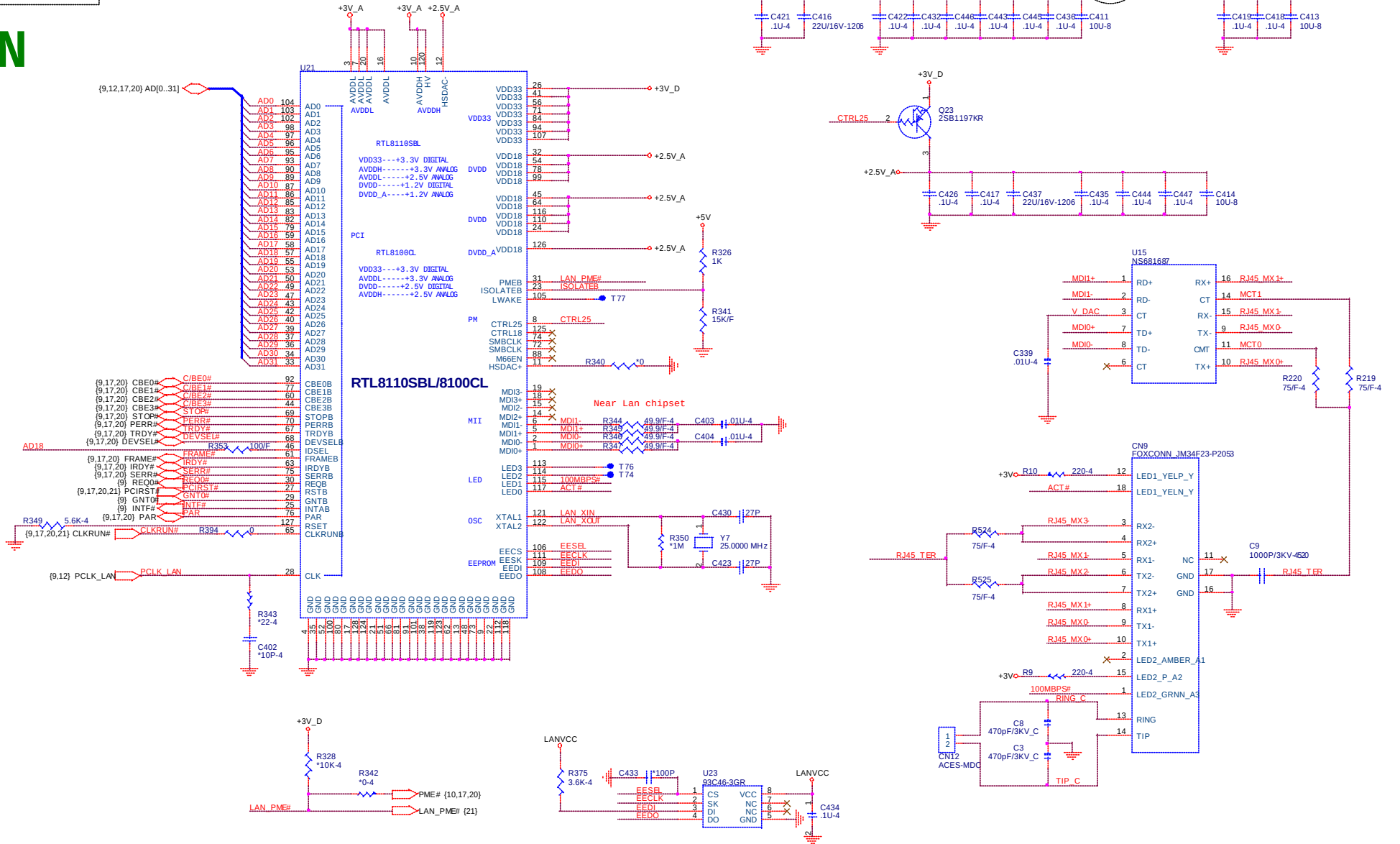
	PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

DDR

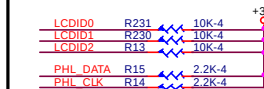
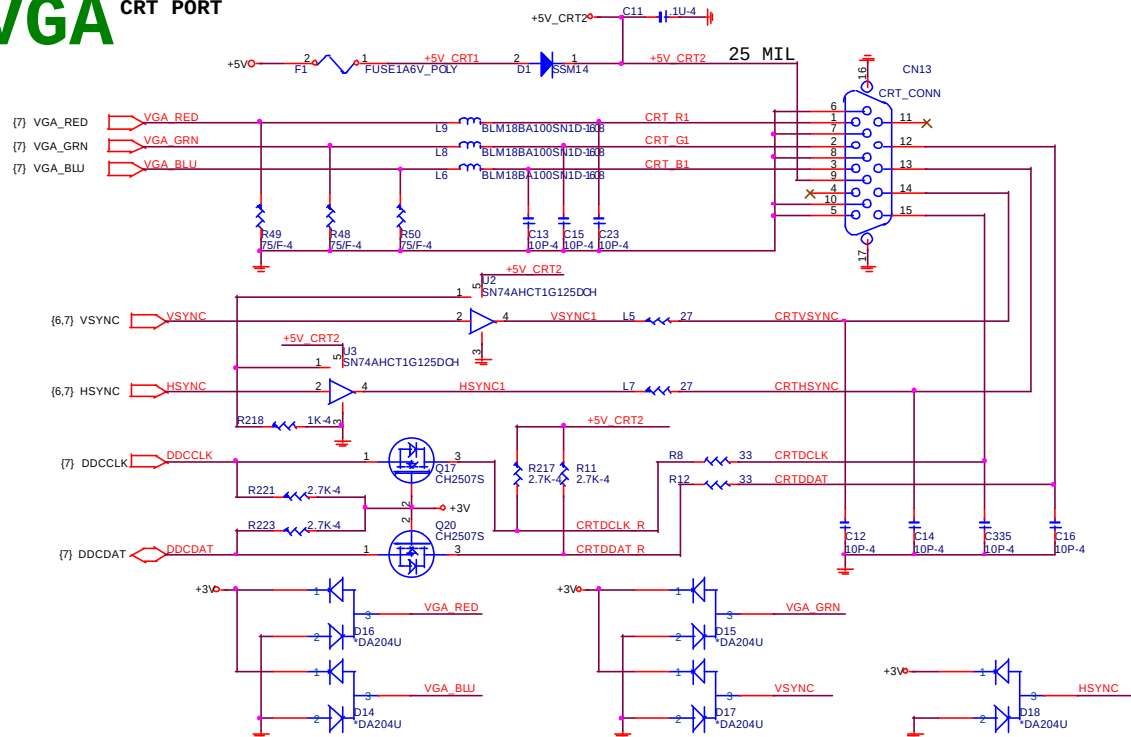


ID Select : AD18
Interrupt Pin : INTD#
Request Indicate : REQ0#
Grant Indicate : GNT0#

LAN

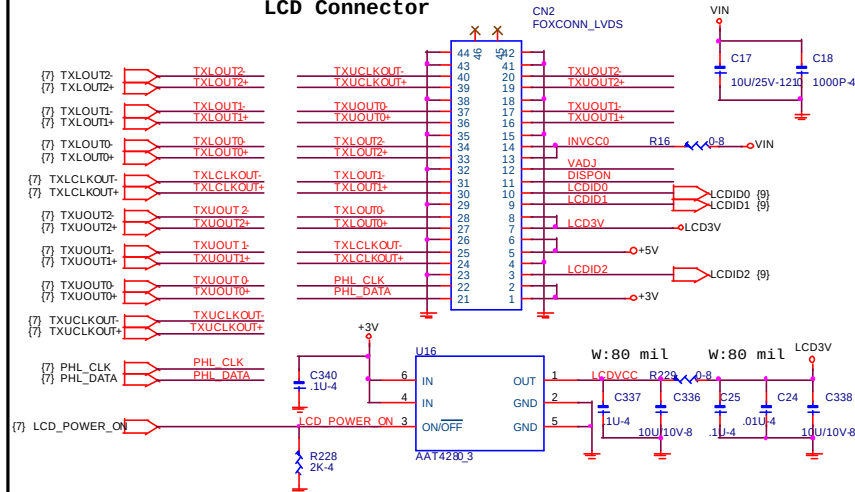


VGA CRT PORT

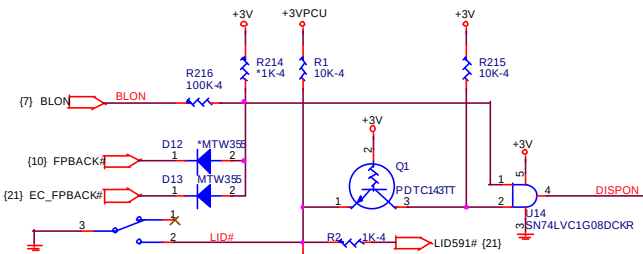
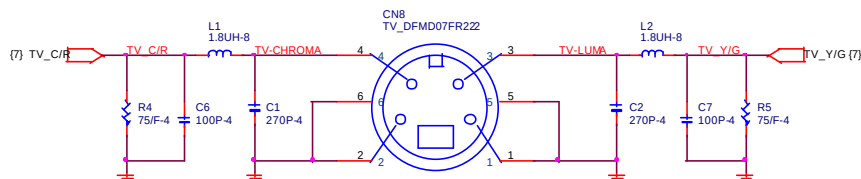


LCDID2	LCDID1	LCDID0	LCD TYPE	LCD CABLE P/N
0	0	0		
0	0	1		
0	1	0		
0	1	1	14" XGA	DD0ZL1LC000
1	0	0	15" XGA	DD0ZL1LC107
1	0	1	15" SXGA+	DD0ZL1LC204
1	1	0	15.4" WXGA	DD0ZL1LC301
1	1	1	15.4" WSXGA+	DD0ZL1LC409

LCD Connector



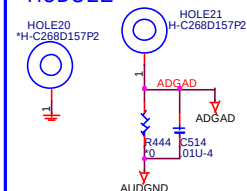
S-VIDEO



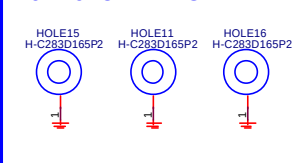
Lid Switch

Addition 0.1U fix ,Sagem

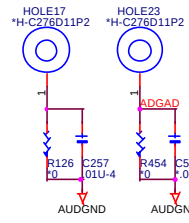
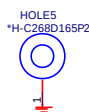
FOR MODEM MODULE



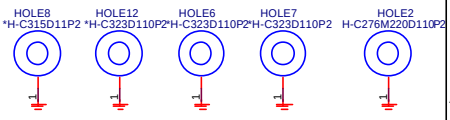
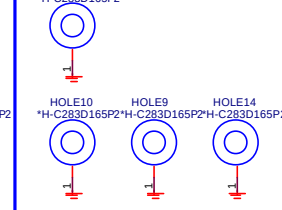
FOR CPU HEATSINK



OTH

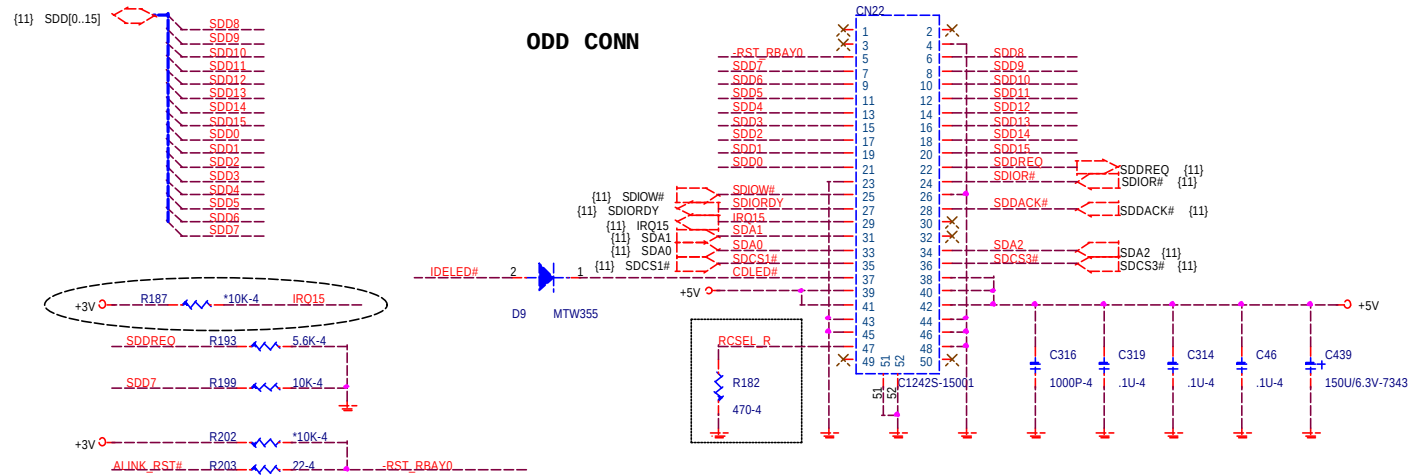
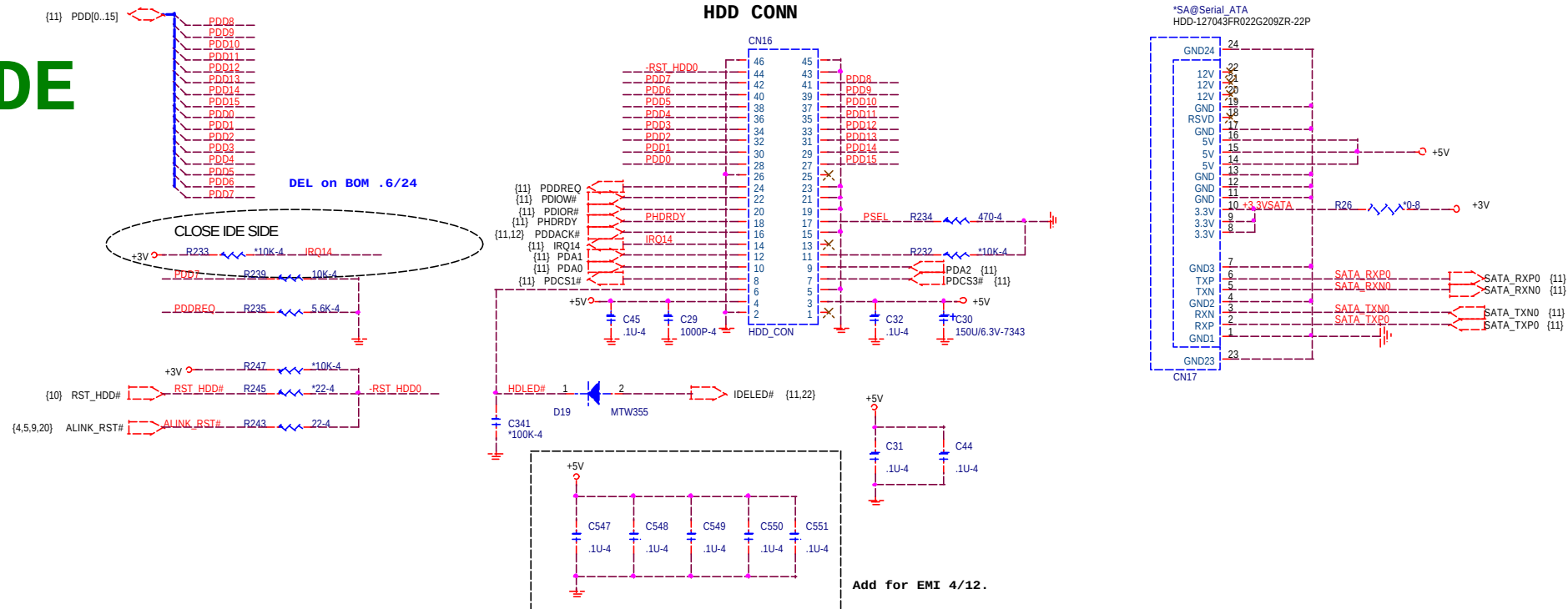


FOR NB HEATSINK



FOR M/B HOLE

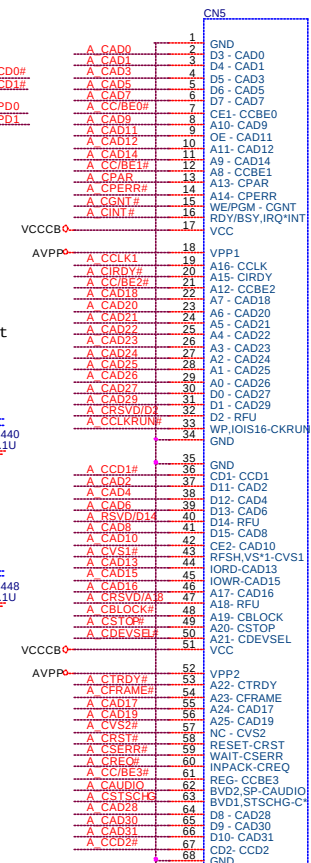
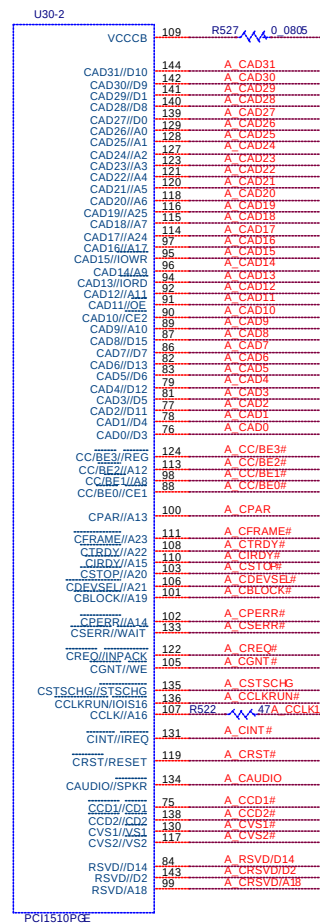
IDE




PROJECT : EW6
Quanta Computer Inc.

Size	Document Number HDD & CDROM	Rev 3A
Date	Monday, June 27, 2005	Sheet 16 of 29

CBS



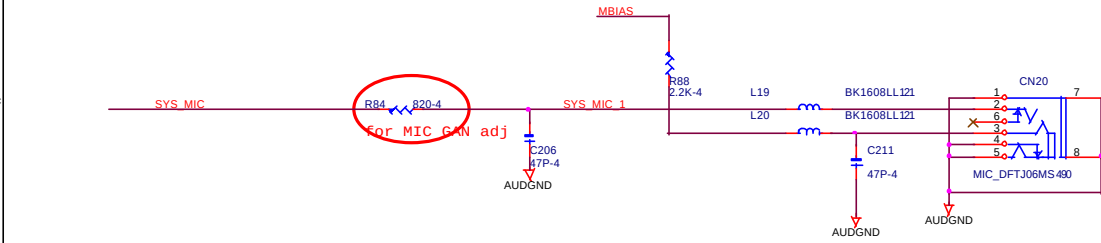
CARDBUS SLOT

PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
	PCMCIA CONTROLLER	18
Date:	Monday, June 27, 2005	Sheet 17 of 29

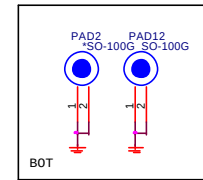
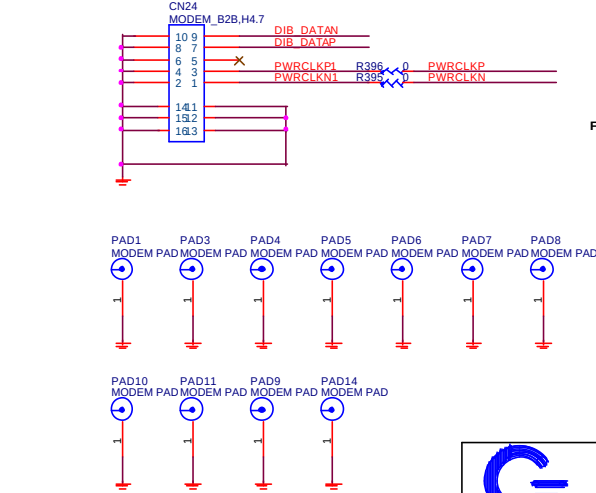
ADO

MIC

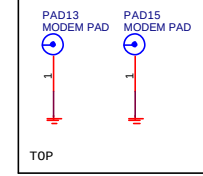


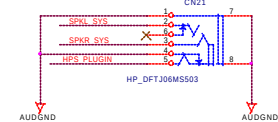
MODEM

MDC



For EMI. Change on C. 5/24.



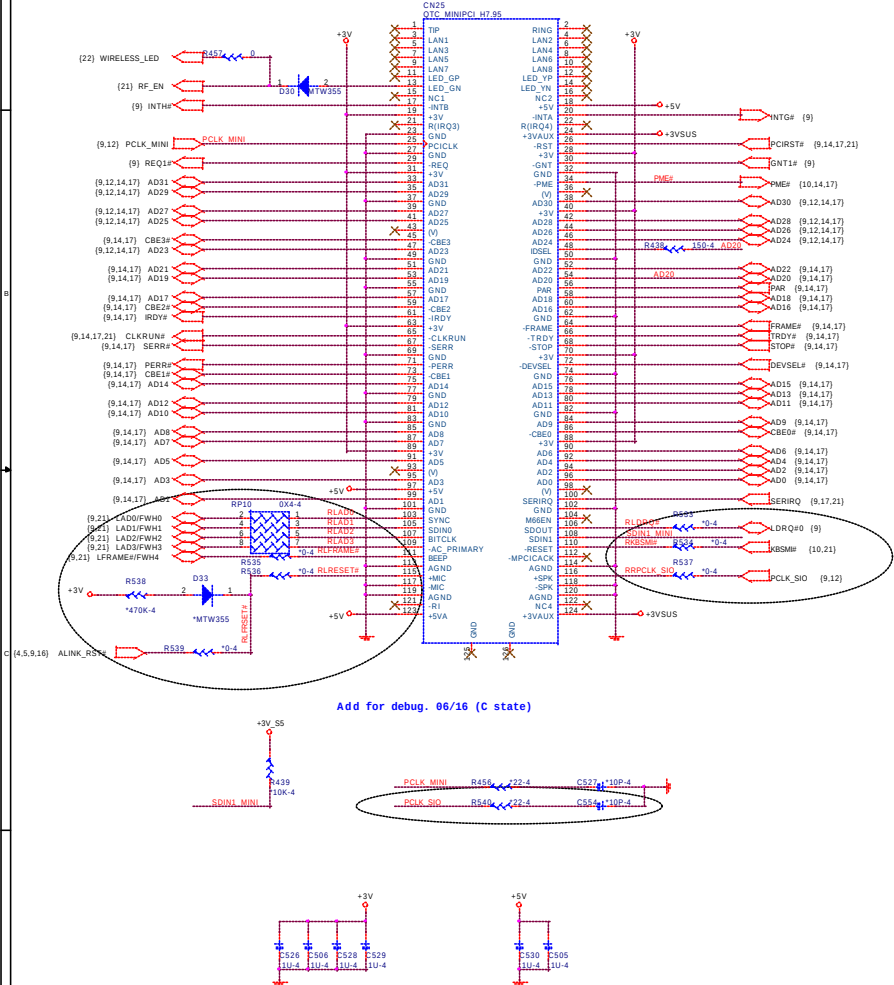


Size	Document Number	Re
	AUDIO AMP	2
Date:	Monday, June 27, 2005	Sheet 19 of 29

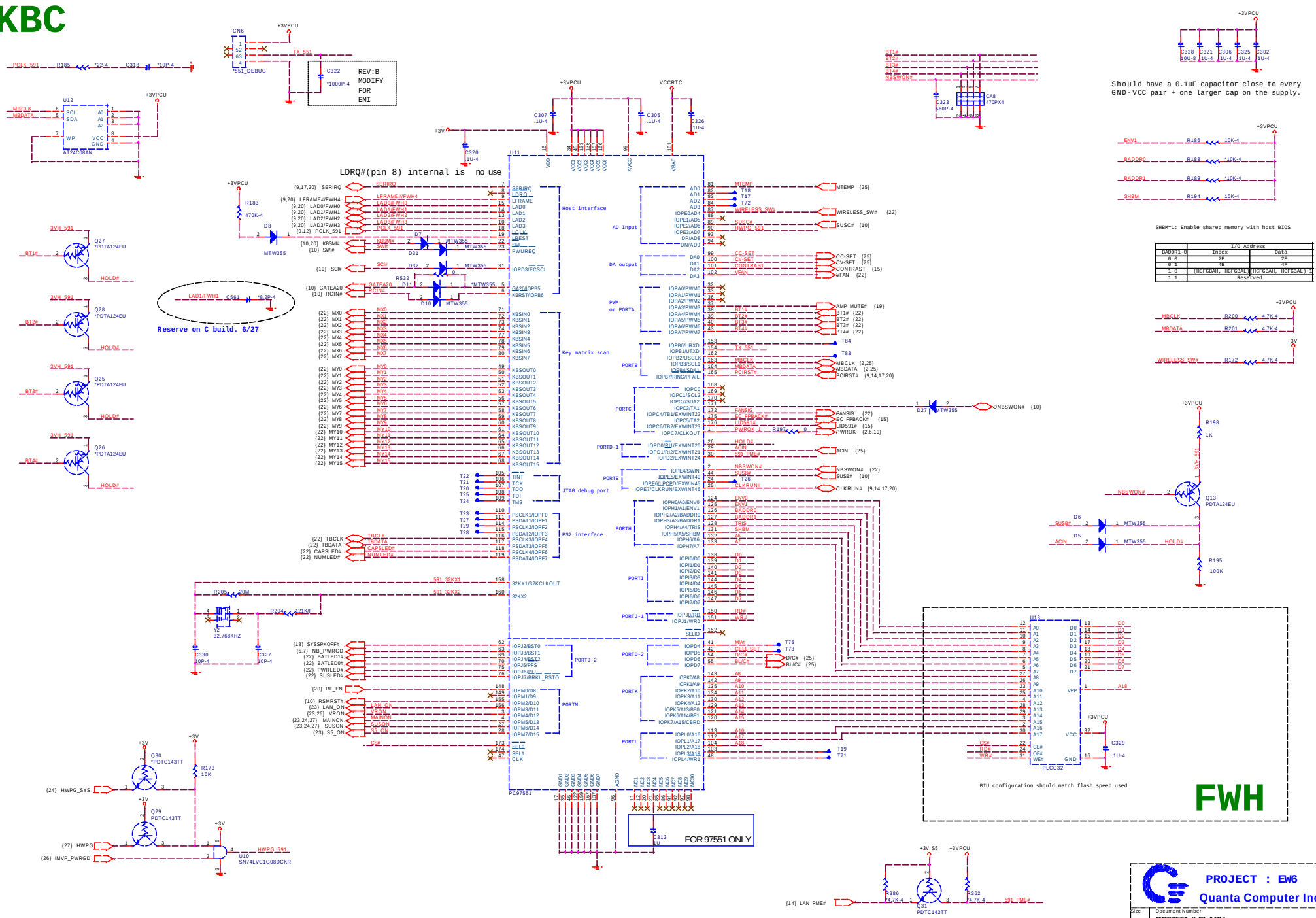
MPC

ID Select : AD20
Interrupt Pin : INTB#, INTCH#
Request Indicate : REQ1#
Grant Indicate : GNT1#

MINI-PCI

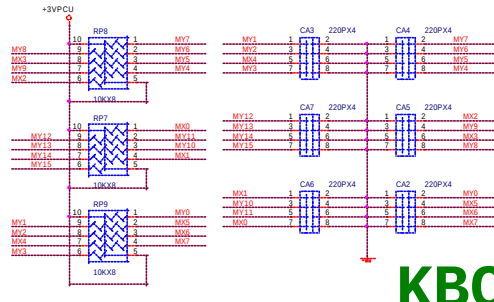
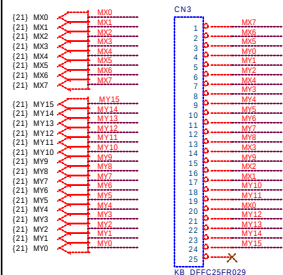


KBC



FWH

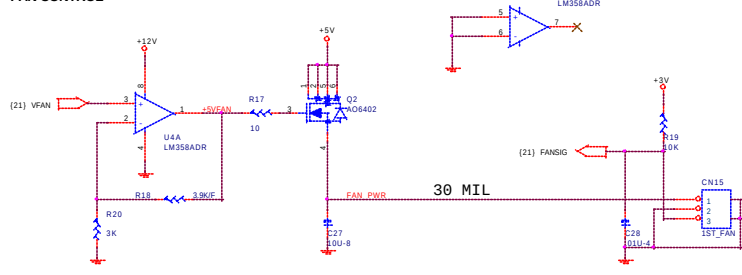
INT K/B



KBC

THM

FAN CONTROL

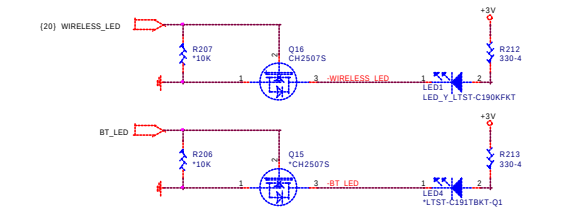
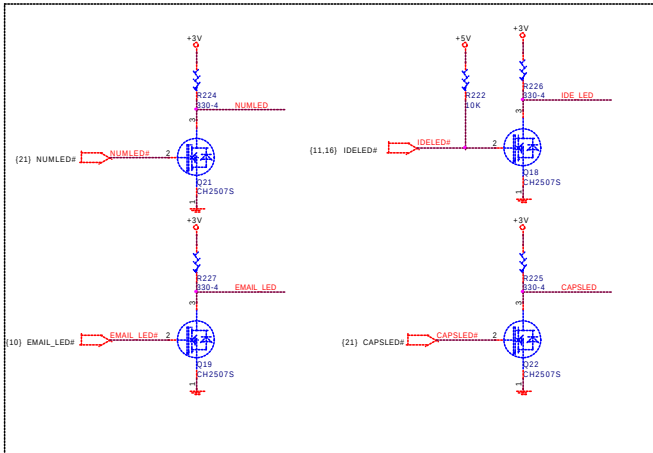
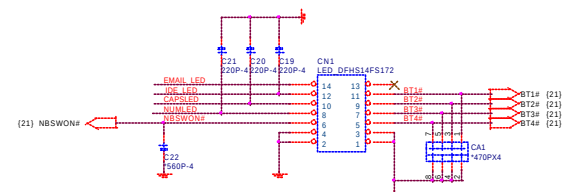
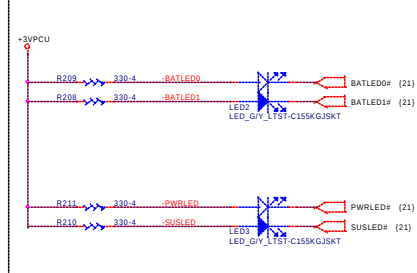
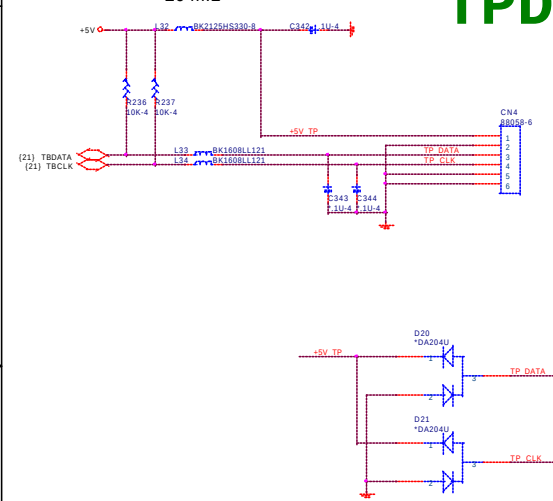


TOUCH PAD

20 MIL

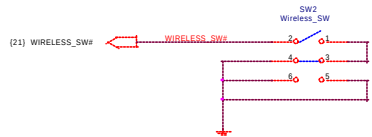
TPD

UIF

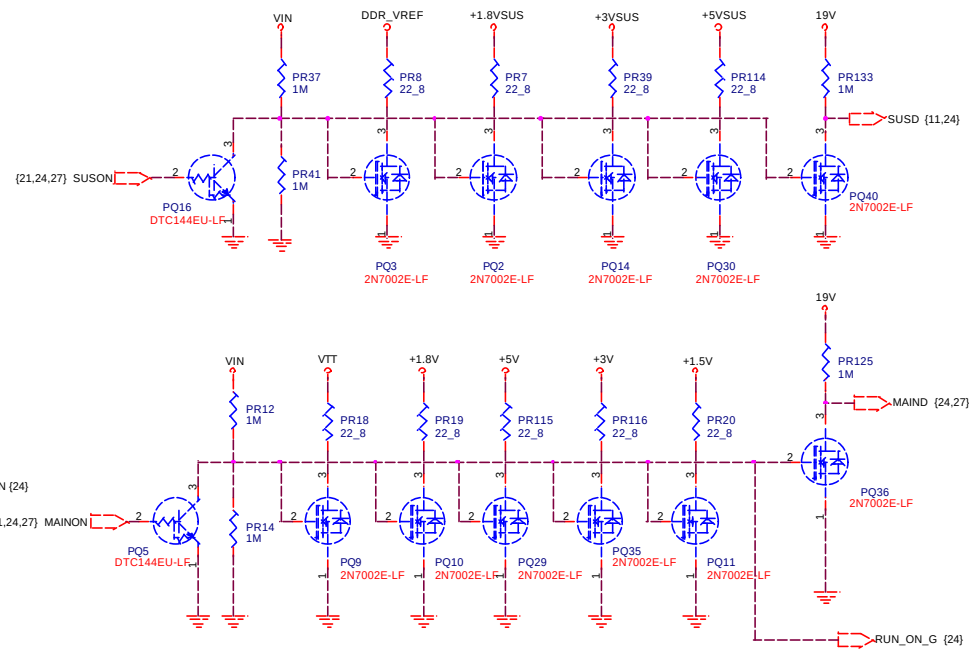
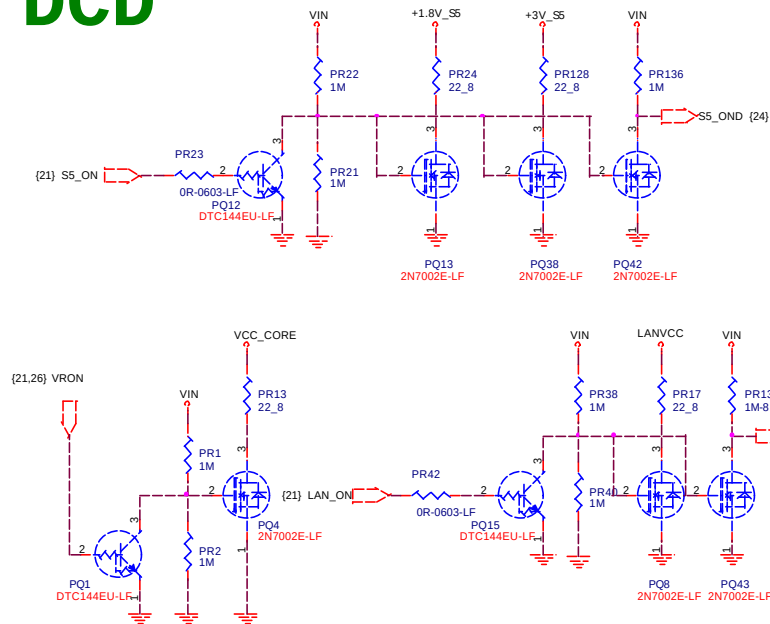


SWITCH

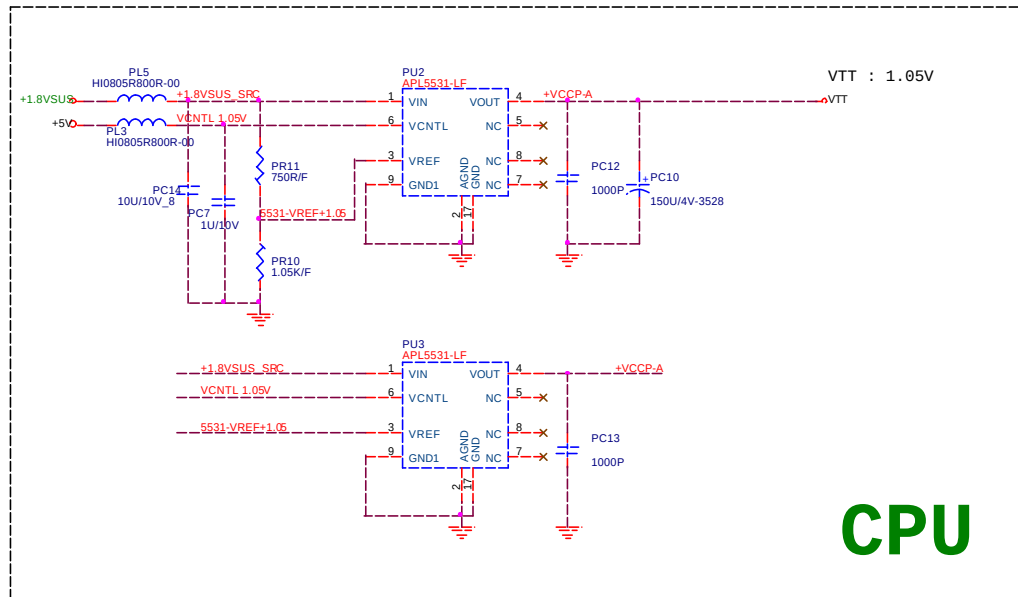
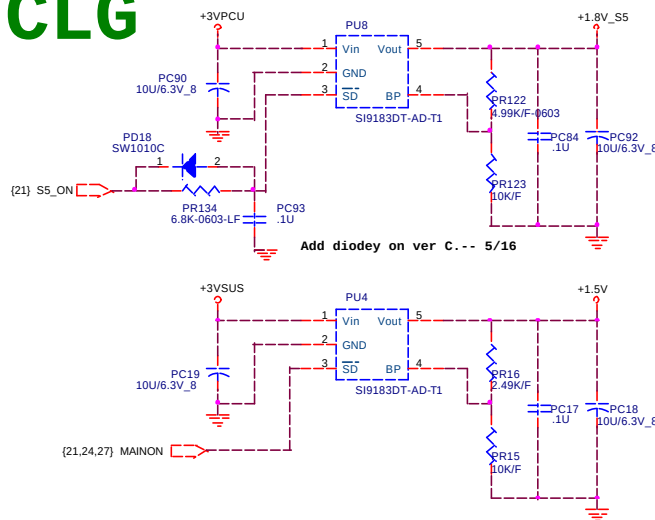
UIF



DCD



CLG



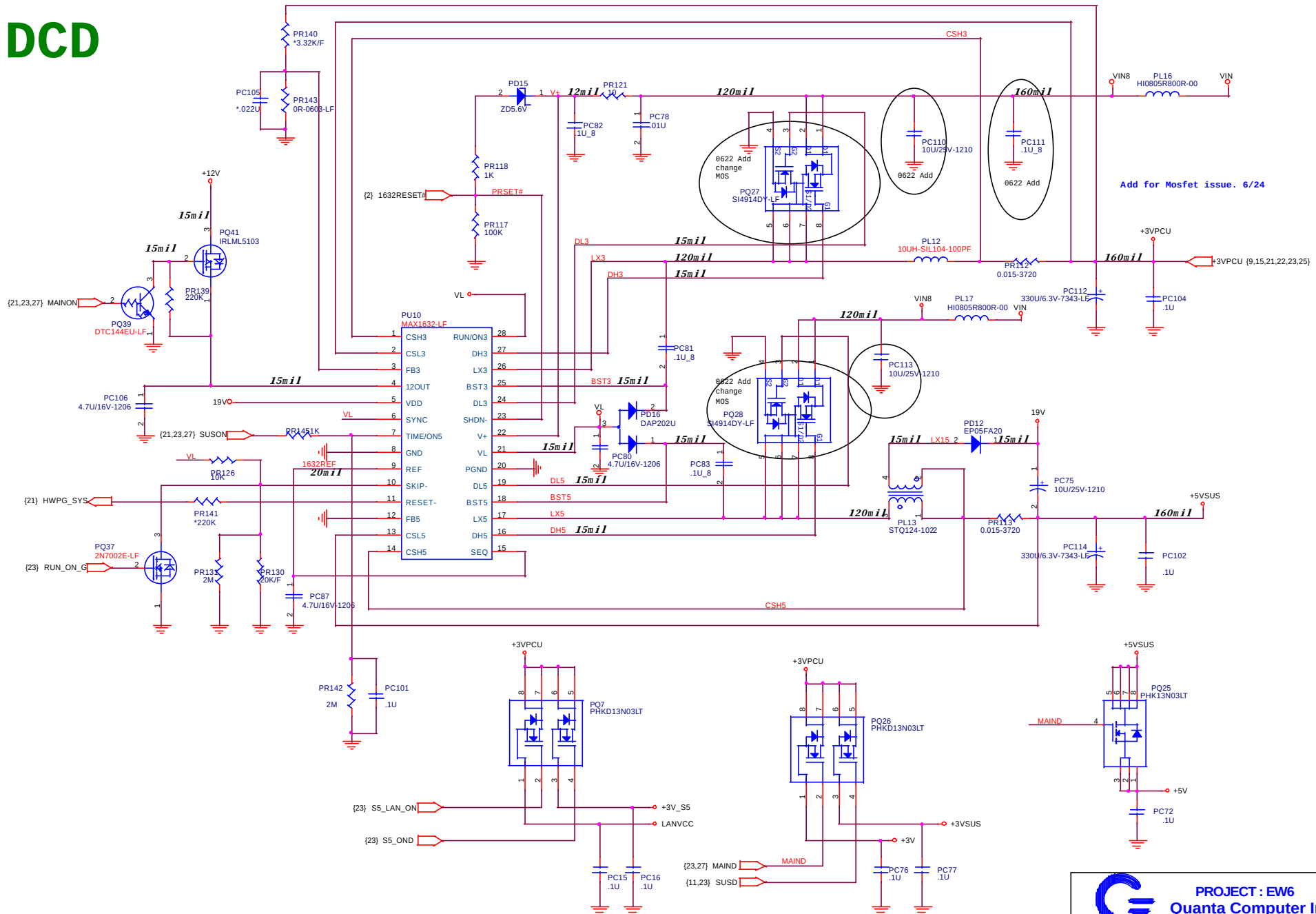
CPU



PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHAGE&+1.8V	2A
Date:	Monday, June 27, 2005	Sheet 23 of 29

DCD



PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM POWER MAX1632	3A
Date:	Monday, June 27, 2005	Sheet 24 of 29

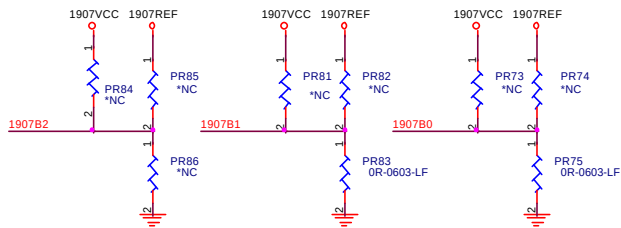
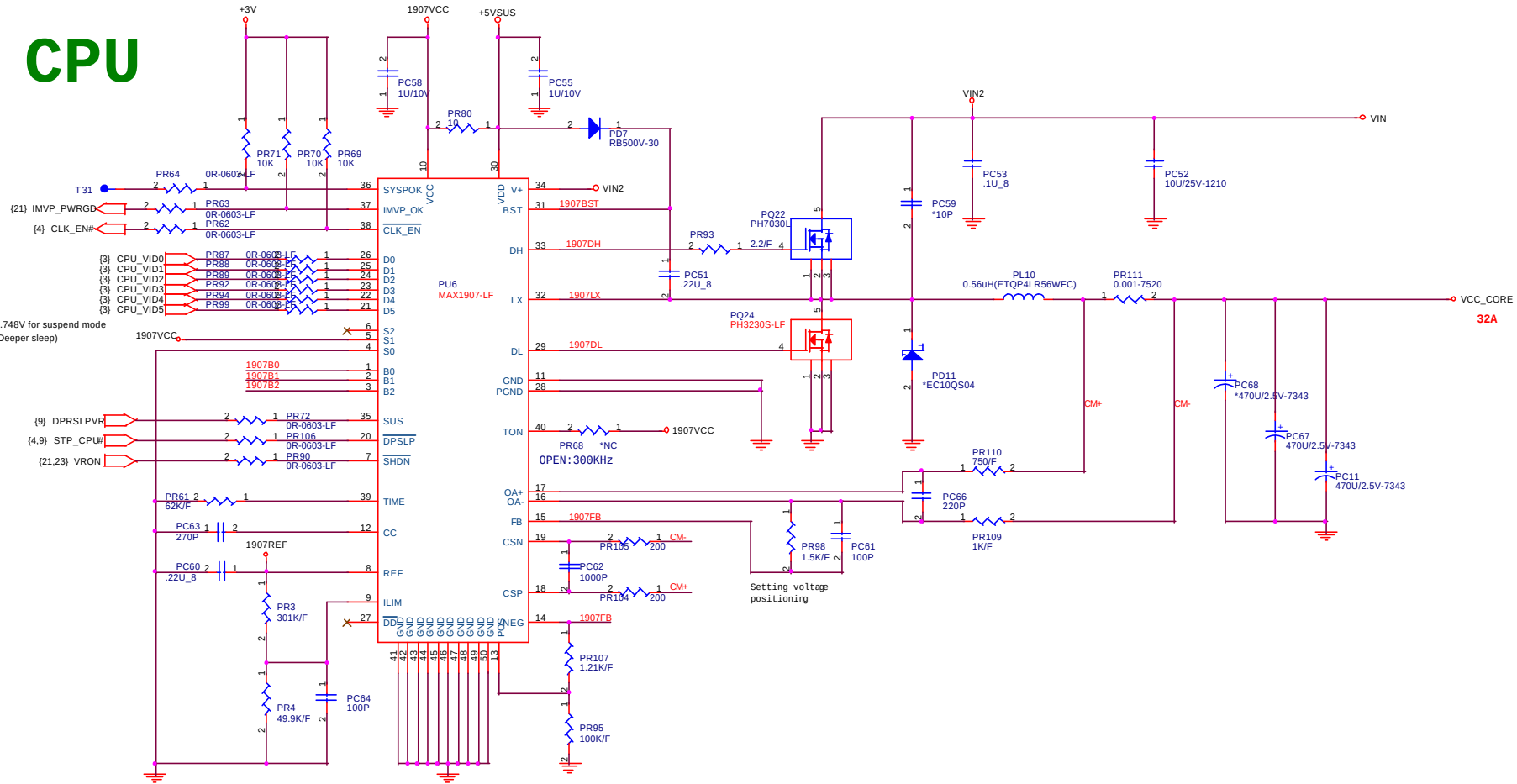
PBC

Regulate resistor feedback sensor for battery watt

PROJECT : EW6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BATTERY CHARGER	3A
Date	Monday, June 27, 2005	Sheet 25 of 29

CPU



Setting boot
voltage=1.2V

SUSPEND MODE (SUS=HIGH)				Output
S2	S1	S0		
✓	OPEN	VCC	GND	0.748V

VCC_BOOT				Output
B2	B1	B0		
✓	OPEN	GND	GND	1.708V
	REF	REF	REF	1.372V
	OPEN	OPEN	OPEN	1.036V
	VCC	VCC	VCC	0.700V
	REF	VCC	VCC	1.212V

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V



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