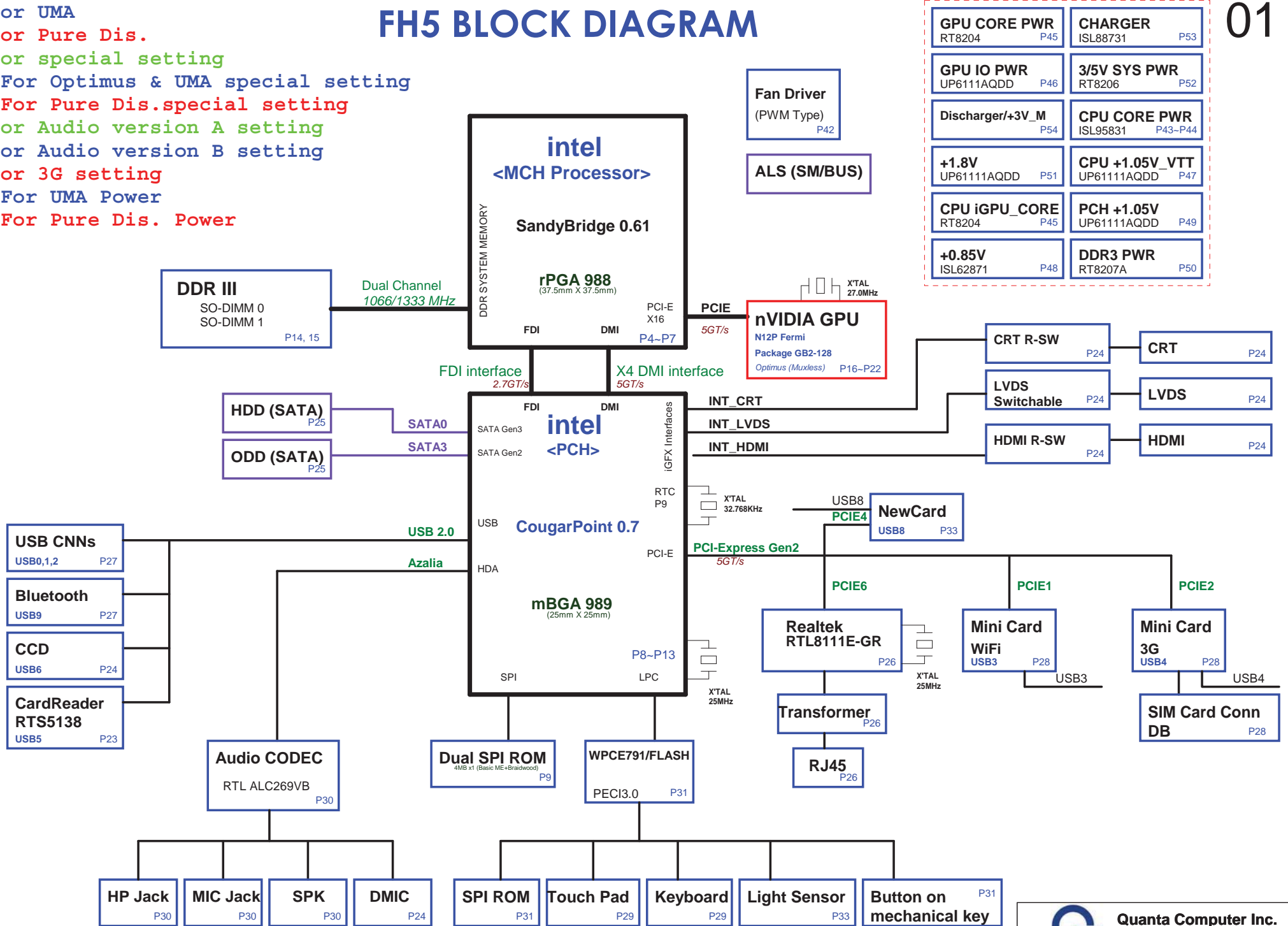


# FH5 BLOCK DIAGRAM

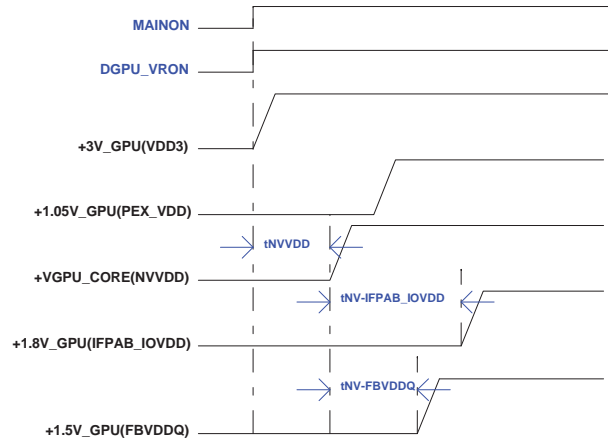
**IV@ For UMA**  
**EV@ For Pure Dis.**  
**SP@ For special setting**  
**SPI@ For Optimus & UMA special setting**  
**SPE@ For Pure Dis.special setting**  
**VA@ For Audio version A setting**  
**VB@ For Audio version B setting**  
**@3G For 3G setting**  
**PIV@ For UMA Power**  
**PEV@ For Pure Dis. Power**



<b>GPU CORE PWR</b> RT8204 P45	<b>CHARGER</b> ISL88731 P53
<b>GPU IO PWR</b> UP6111AQDD P46	<b>3/5V SYS PWR</b> RT8206 P52
<b>Discharger/+3V_M</b> P54	<b>CPU CORE PWR</b> ISL95831 P43-P44
<b>+1.8V</b> UP6111AQDD P51	<b>CPU +1.05V_VTT</b> UP6111AQDD P47
<b>CPU iGPU_CORE</b> RT8204 P45	<b>PCH +1.05V</b> UP6111AQDD P49
<b>+0.85V</b> ISL62871 P48	<b>DDR3 PWR</b> RT8207A P50

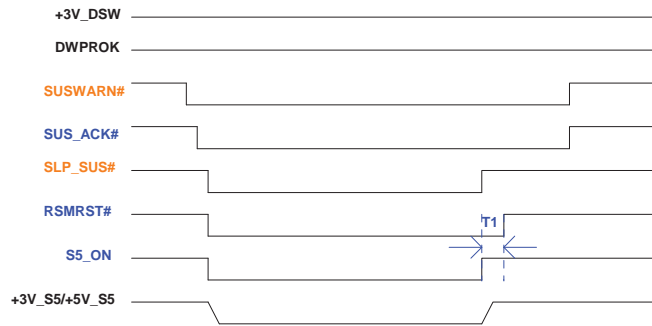
Note:  
HM65 does not support USB 6 & 7  
HM65 does not support SATA 2 & 3

### N12P-GE Power Up Sequence



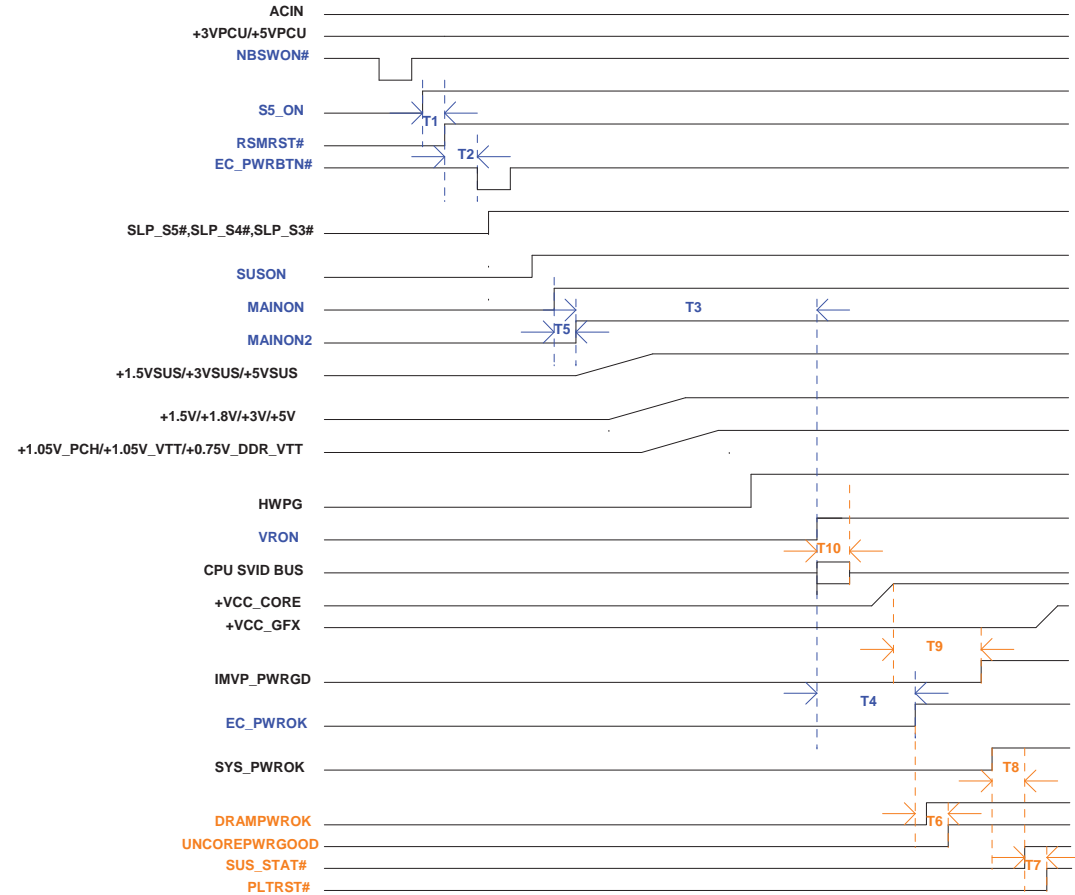
N12P-GE Power up Sequence  
 tINVDD>0  
 tINV-IFPAB\_IOVDD>0  
 tINV-FBVDDQ>0

### Deep S4/S5 off-on Sequence

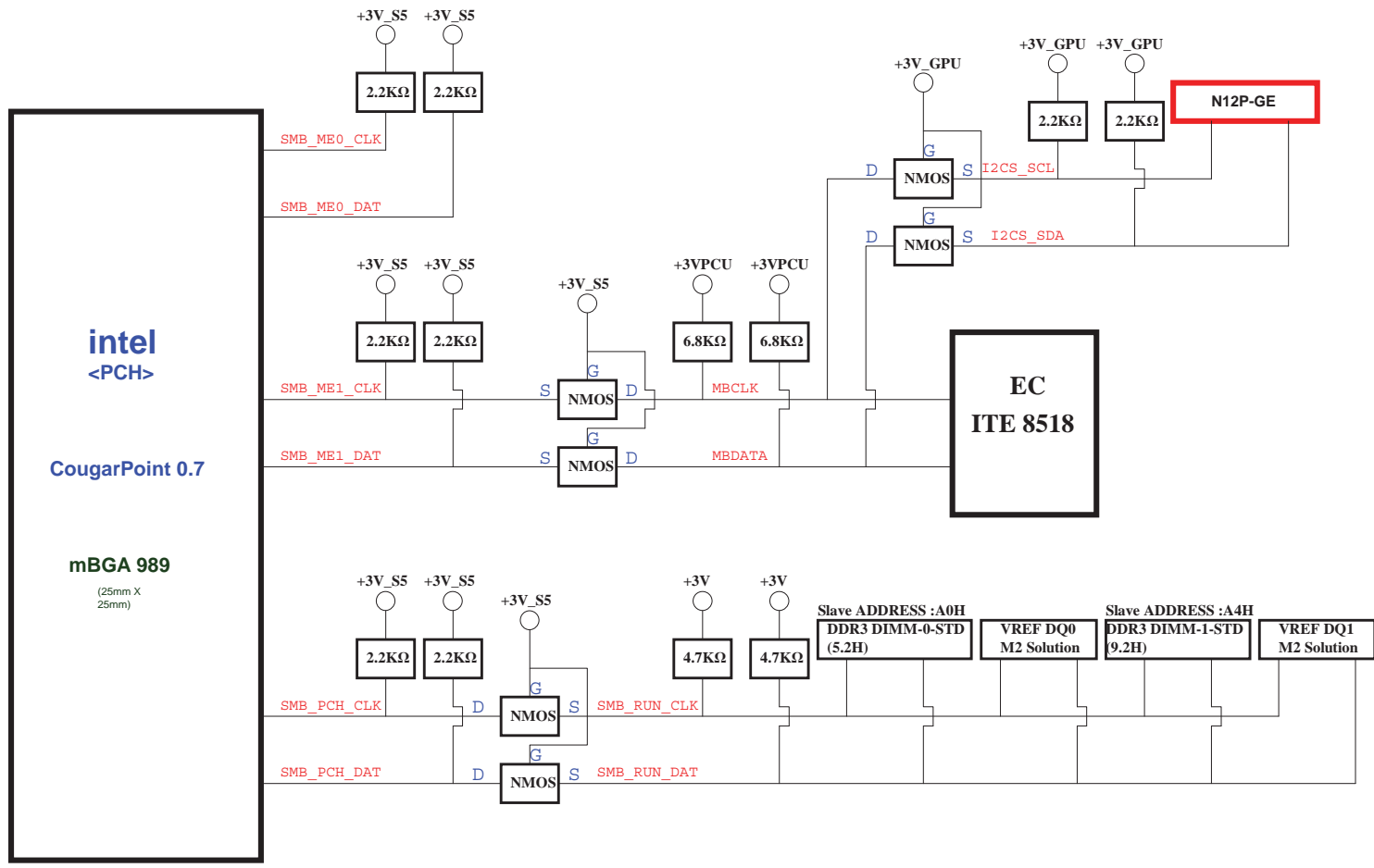


Deep S4/S5 Sequence  
 T1: S5\_ON TO RSMRST# = 30ms (spec:mini 10ms)

### MS15-UMA Power-ON Sequence

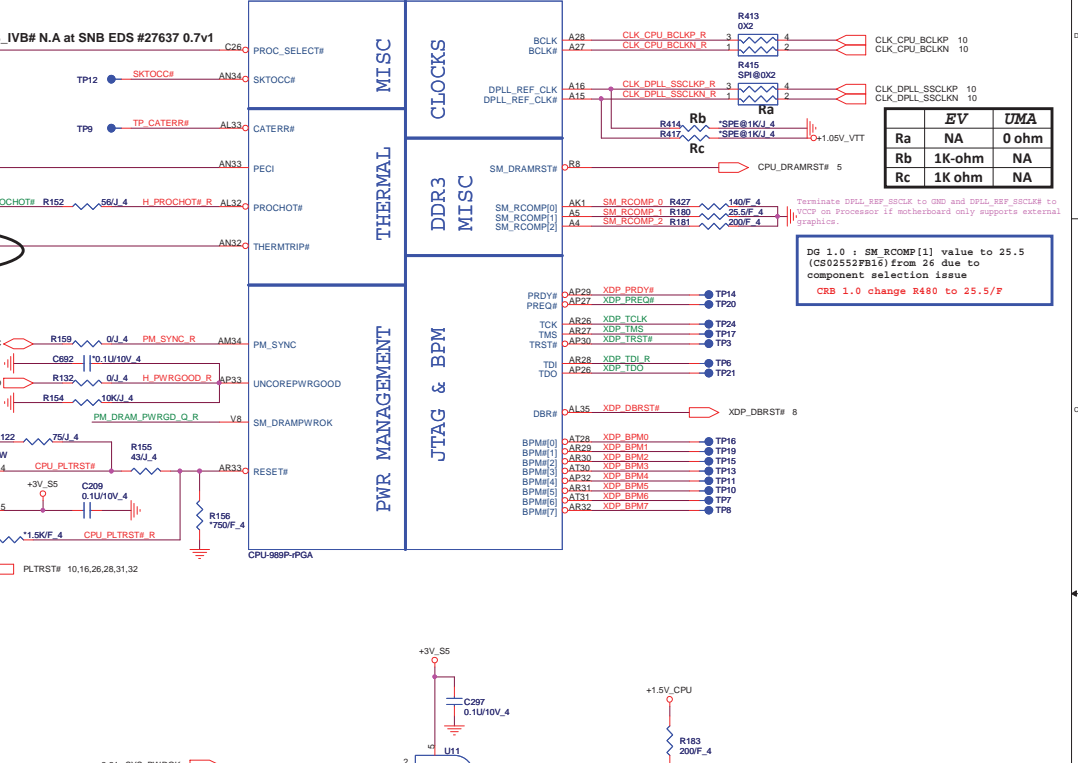
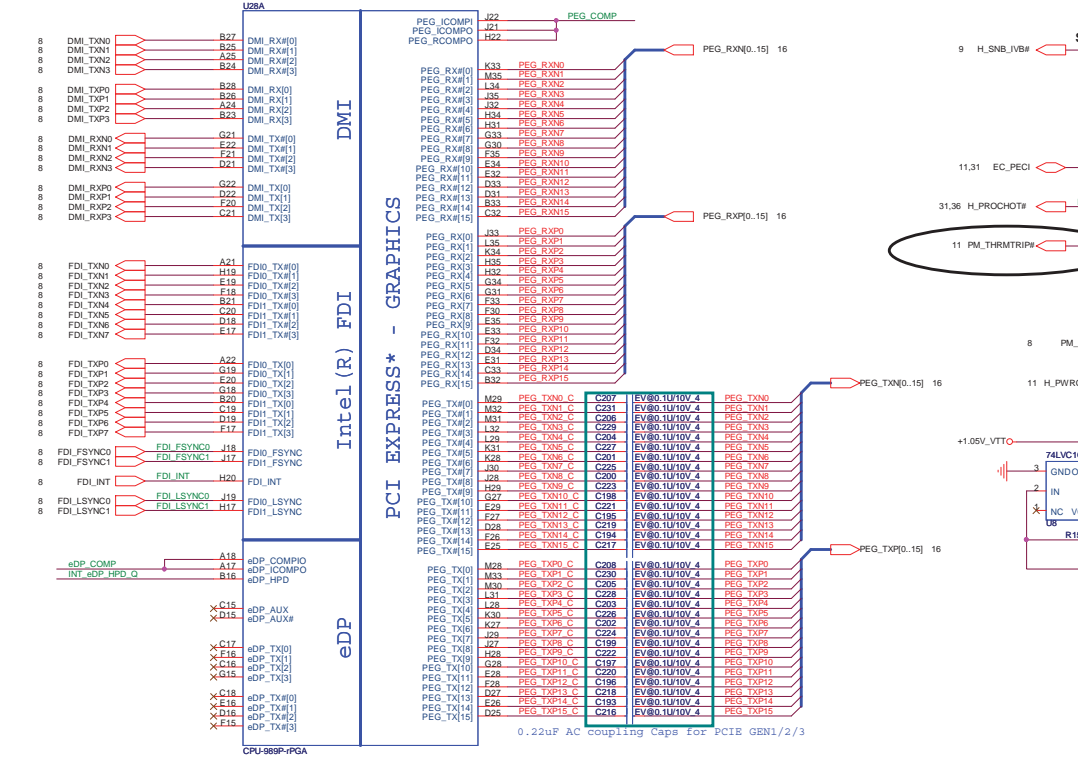


System Power Sequence  
 T1: S5\_ON TO RSMRST# = 30ms (spec:mini 10ms)  
 T2: RSMRST# TO EC\_PWRBTN# = 110ms (spec:mini 100ms)  
 T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)  
 T4: VRON TO EC\_PWROK = 10ms (HWPG NEED TO BE HIGH at that time)  
 T5: MAINON TO MAINON2 = 500us  
 T6: EC\_PWROK to UNCOREPWROK = 2ms(Min)  
 T7: SUS\_STAT# to PLTRST# = 60us(Min)  
 T8: SYS\_PWROK to SUS\_STAT# = 1ms(Min)  
 T9: +VCC\_CORE to IMVP\_PWRGD = 5ms(Max)  
 T10: VRON to accept SVID command. = 5ms(Max)



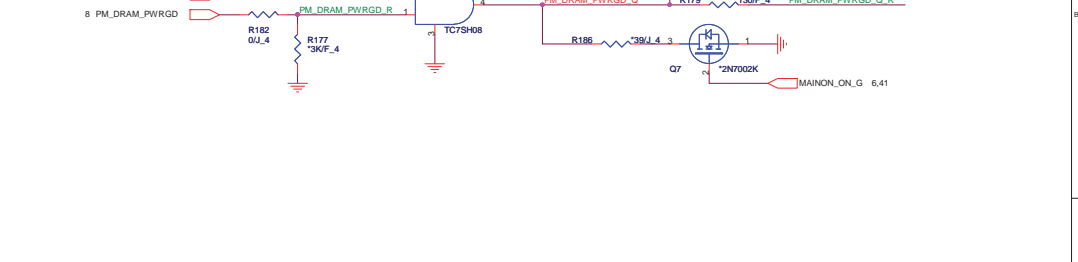
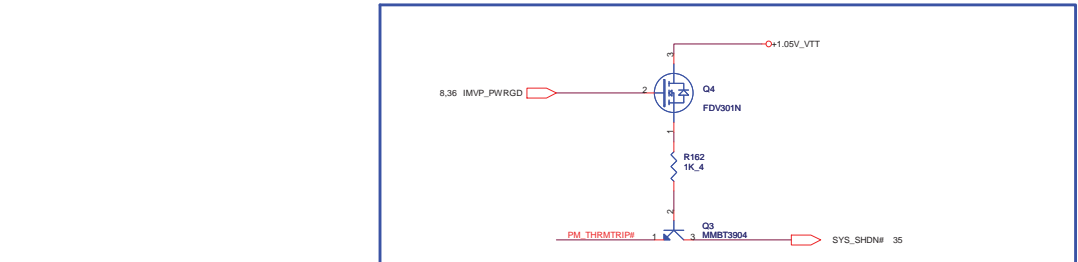
Sandy Bridge Processor (DMI, PEG, FDI)

Sandy Bridge Processor (CLK, MISC, JTAG)



	EV	UMA
Ra	NA	0ohm
Rb	1K-ohm	NA
Rc	1K ohm	NA

Terminate DPLL\_REF\_SCLK to GND and DPLL\_REF\_SCLK# to VCC on Processor. If motherboard only supports external graphics.  
 DG 1.0 : SM\_RCOMP[1] value to 25.5 (C803527F18) from 26 due to component selection issue  
 CRB 1.0 change R480 to 25.5/F



**FDI Disabling (Discrete Only)**

FDI\_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

**DP & PEG Compensation**

eDP\_COMP and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG\_ICOMPI and RCOMP0 signals should be routed within 500 mils typical impedance = 43 mohms

PEG\_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

**eDP Hot-plug**

CAD Note: Place PU resistor within 2 inches of CPU

HPD disable

**Processor pull-up(CPU)**

1.05V\_VTT

H\_PROCHOT# R130 62J.4

XDP\_TDO R165 51J.4

XDP\_TMS R163 51J.4

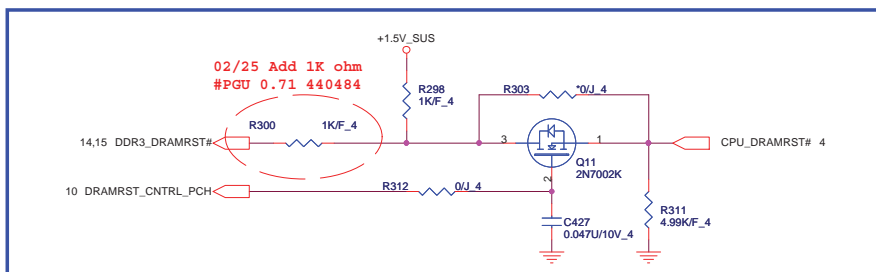
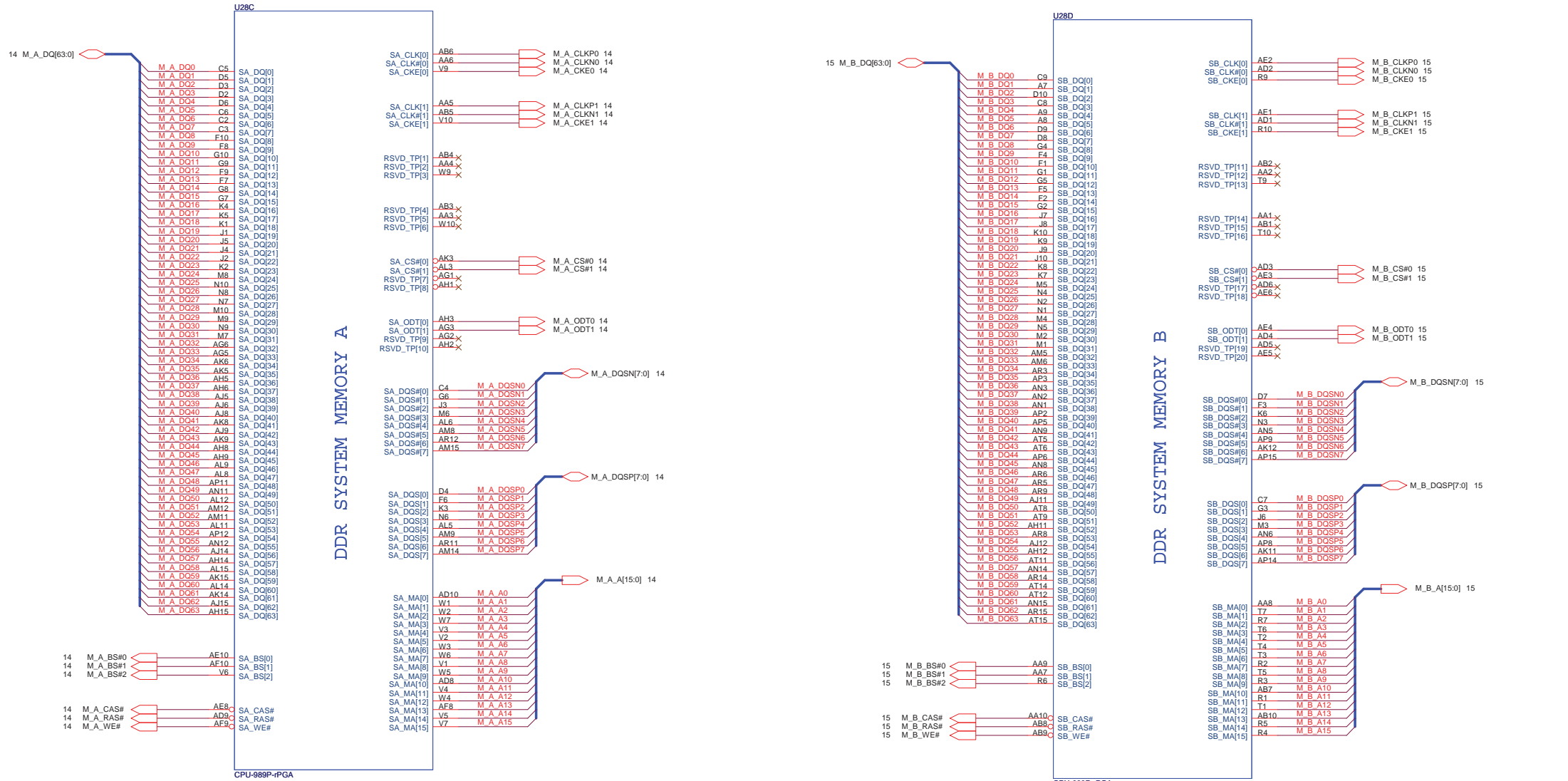
XDP\_TDI\_R R166 51J.4

XDP\_PREQ# R164 51J.4

XDP\_TCLK R168 51J.4

XDP\_TRST# R153 51J.4

# Sandy Bridge Processor (DDR3)



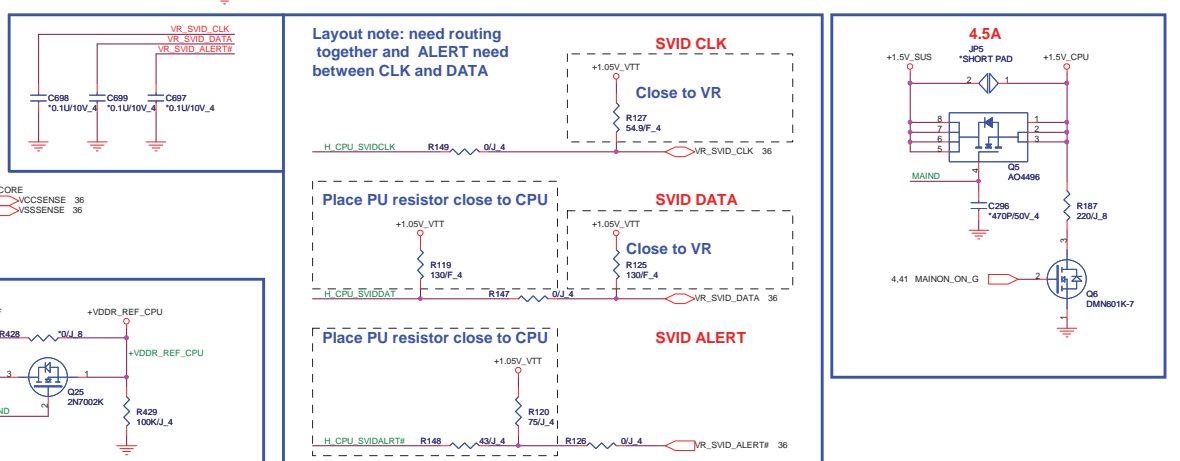
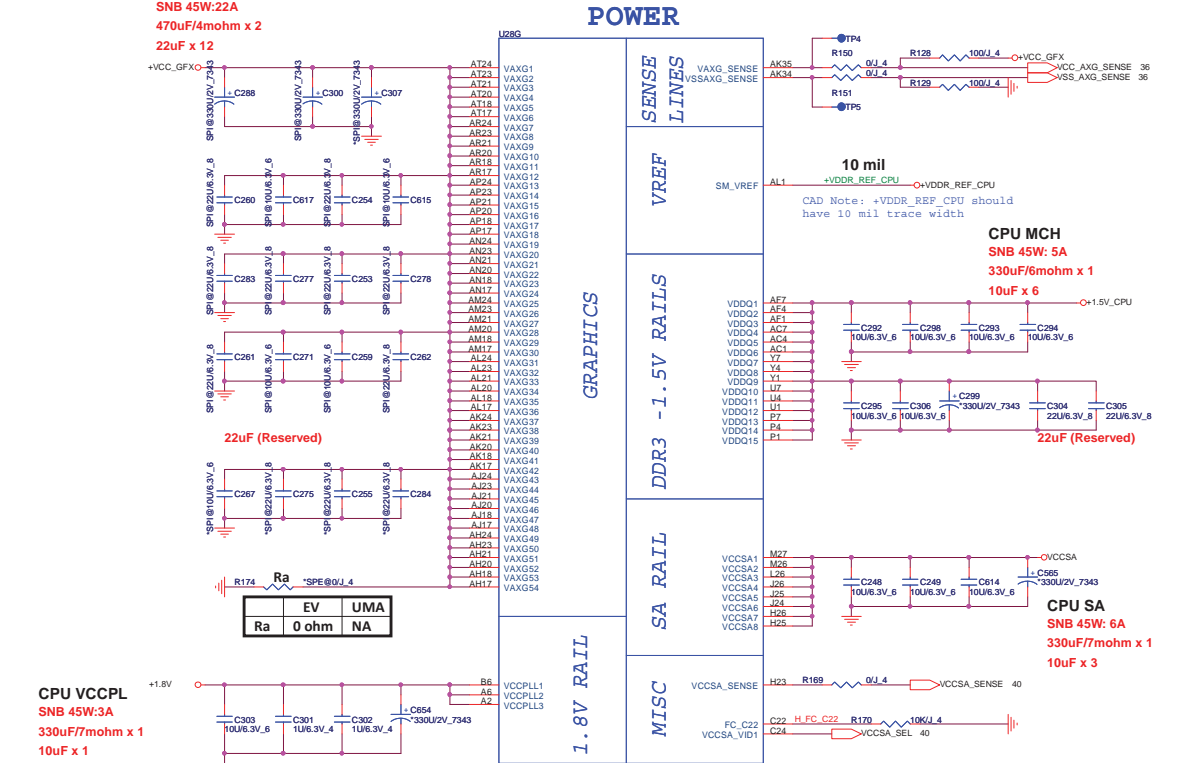
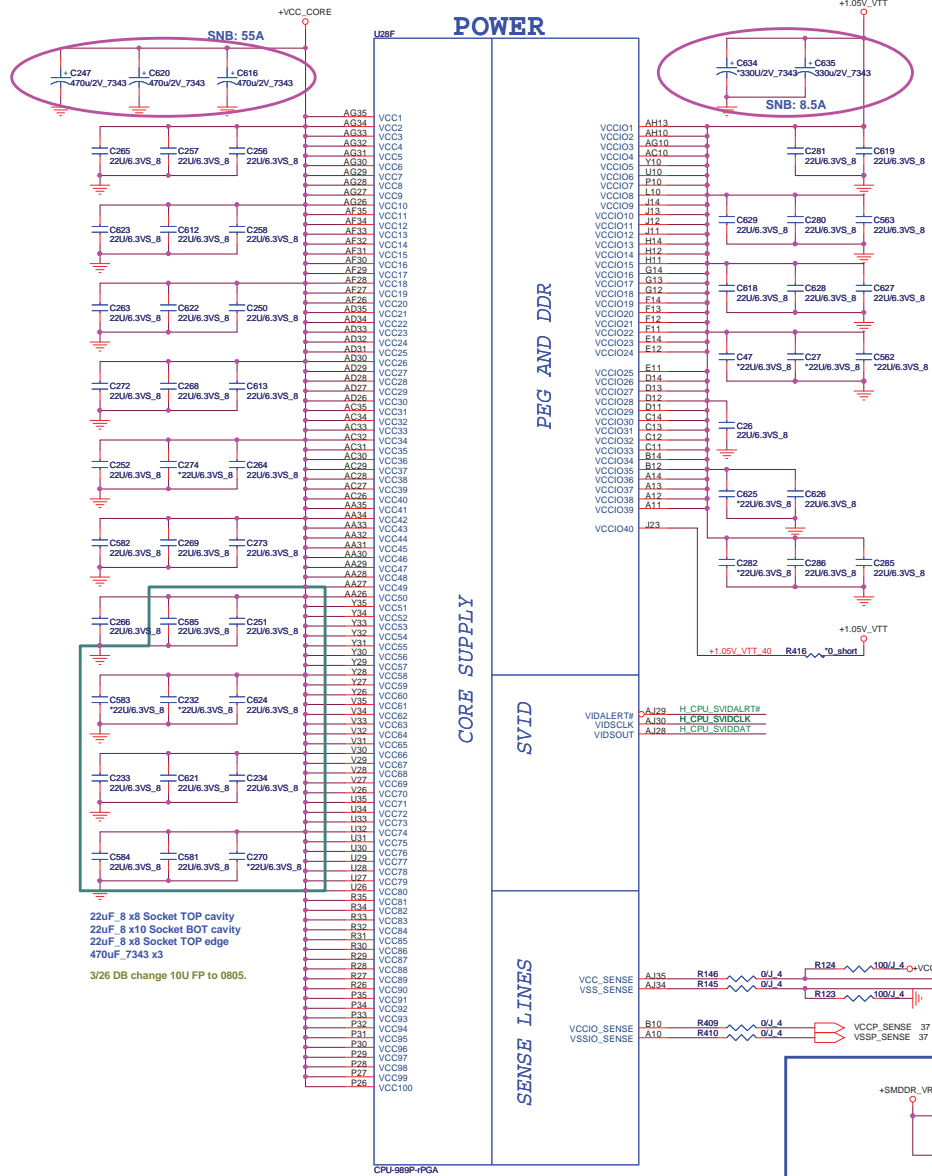
**Quanta Computer Inc.**  
**PROJECT : FHS**

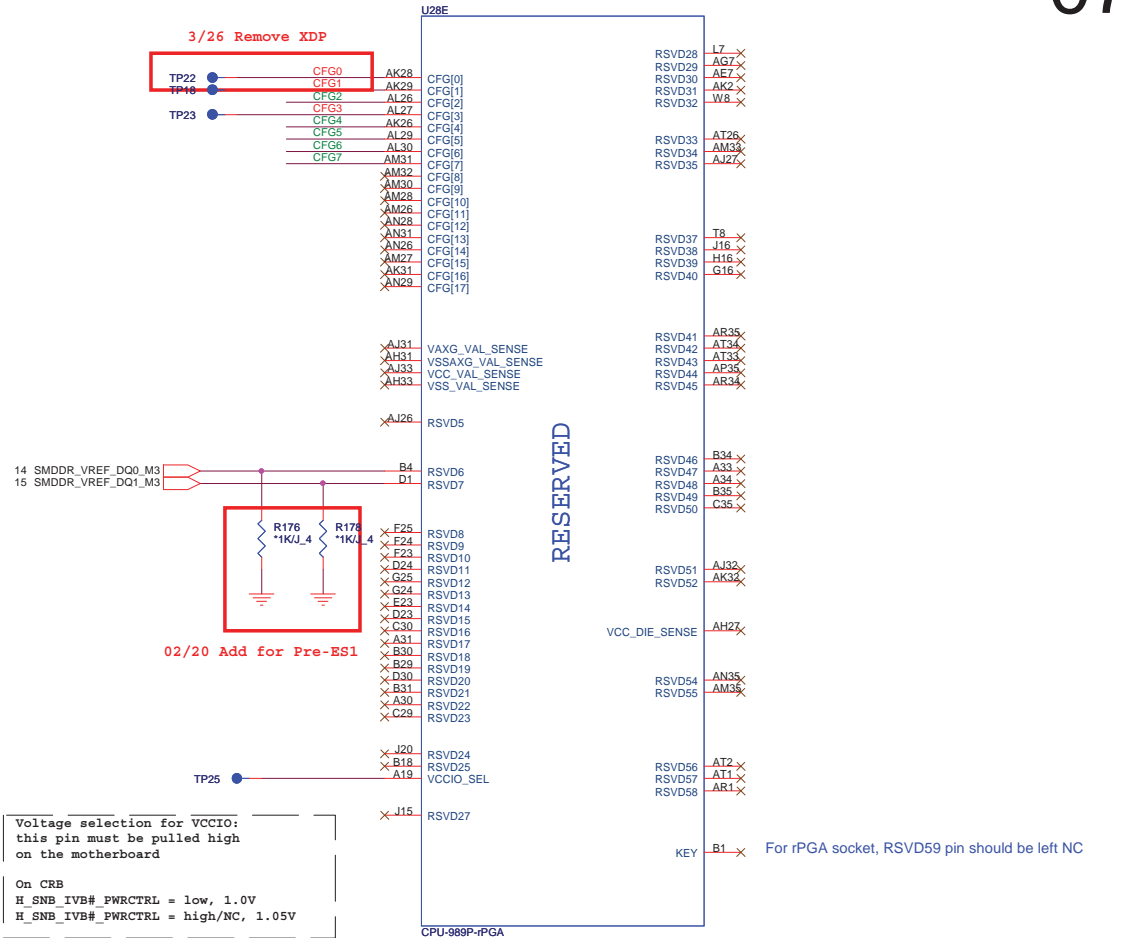
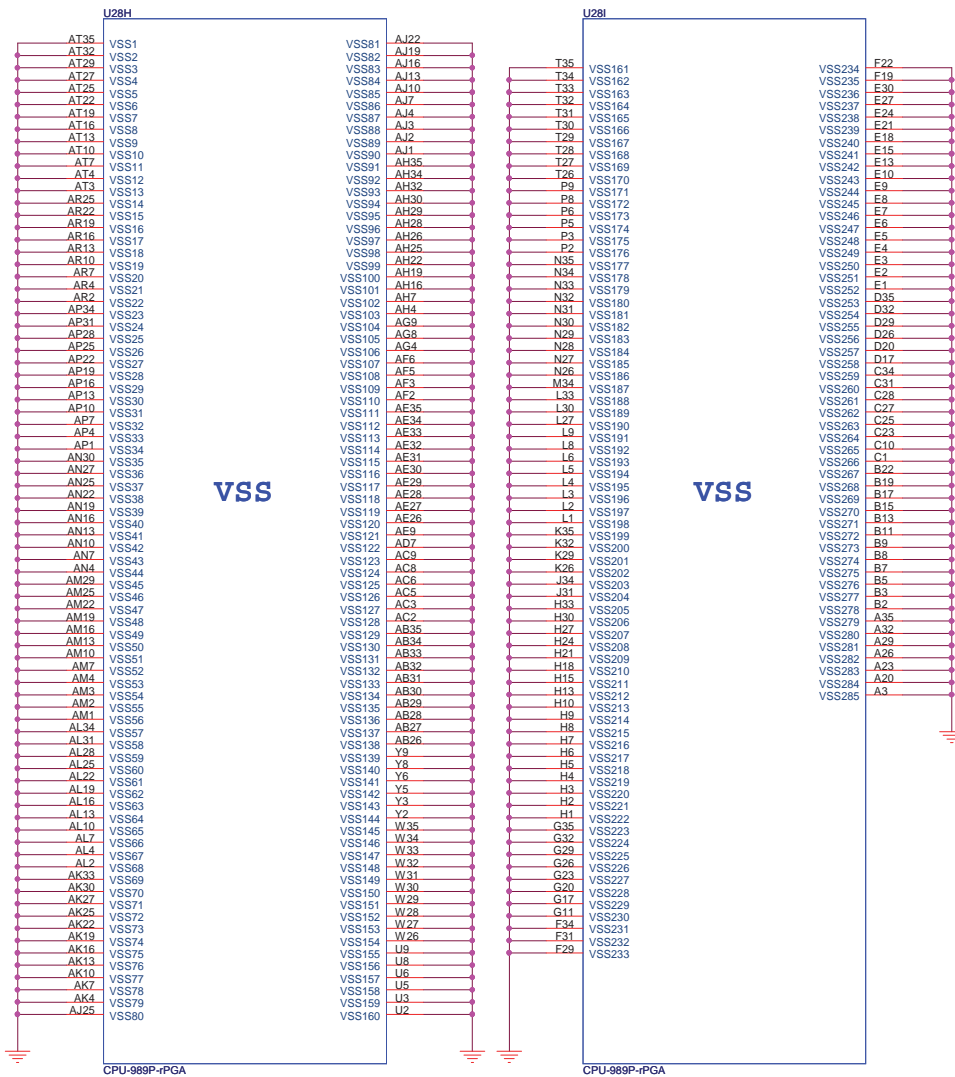
Size	Document Number	Rev
	<b>Sandy Bridge 2/4</b>	1A
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SPI@ For Optimus & UMA  
SPE@ For Pure Dis.  
SP@ For special setting

Sandy Bridge Processor (GRAPHIC POWER)

Sandy Bridge Processor (POWER)





Voltage selection for VCCIO:  
 this pin must be pulled high  
 on the motherboard

On CRB  
 H\_SNB\_IVB#\_PWRCTRL = low, 1.0V  
 H\_SNB\_IVB#\_PWRCTRL = high/NC, 1.05V

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PEG Static x4 Lane)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)  
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

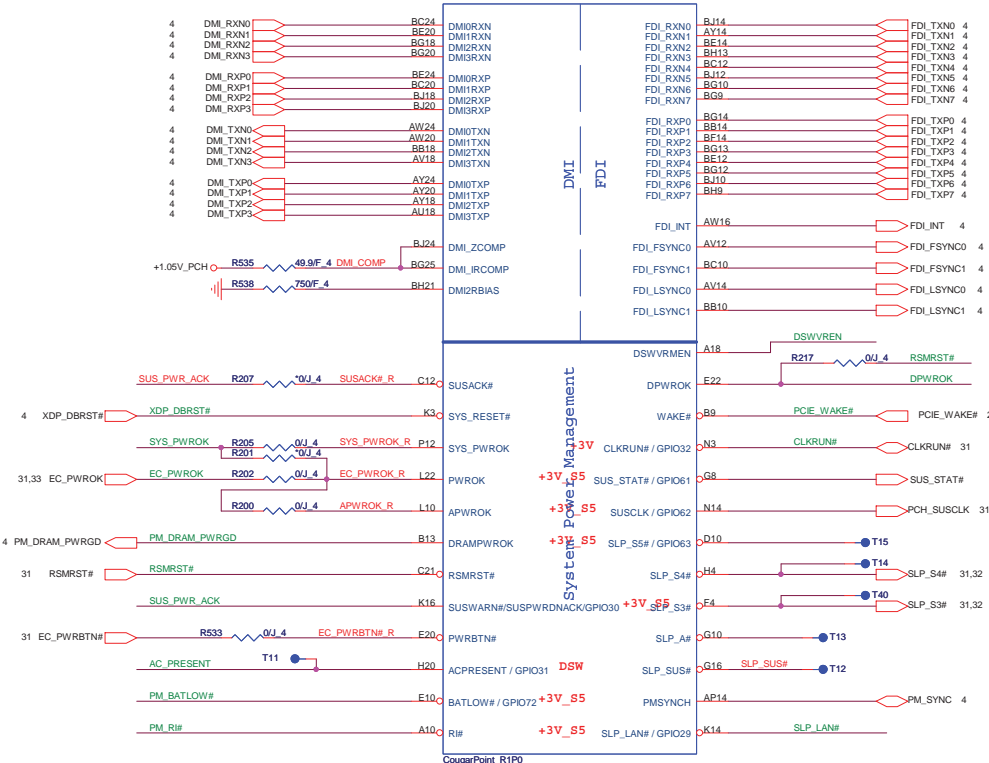
**Quanta Computer Inc.**  
 PROJECT : FH5

Size Document Number Rev 1A  
 Sandy Bridge 4/4  
 Date: Monday, September 27, 2010 Sheet 7 of 41



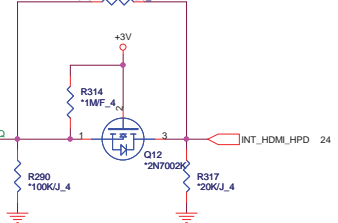
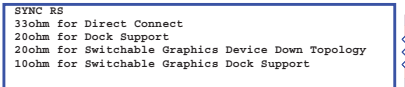
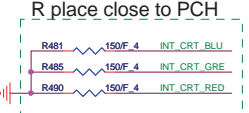
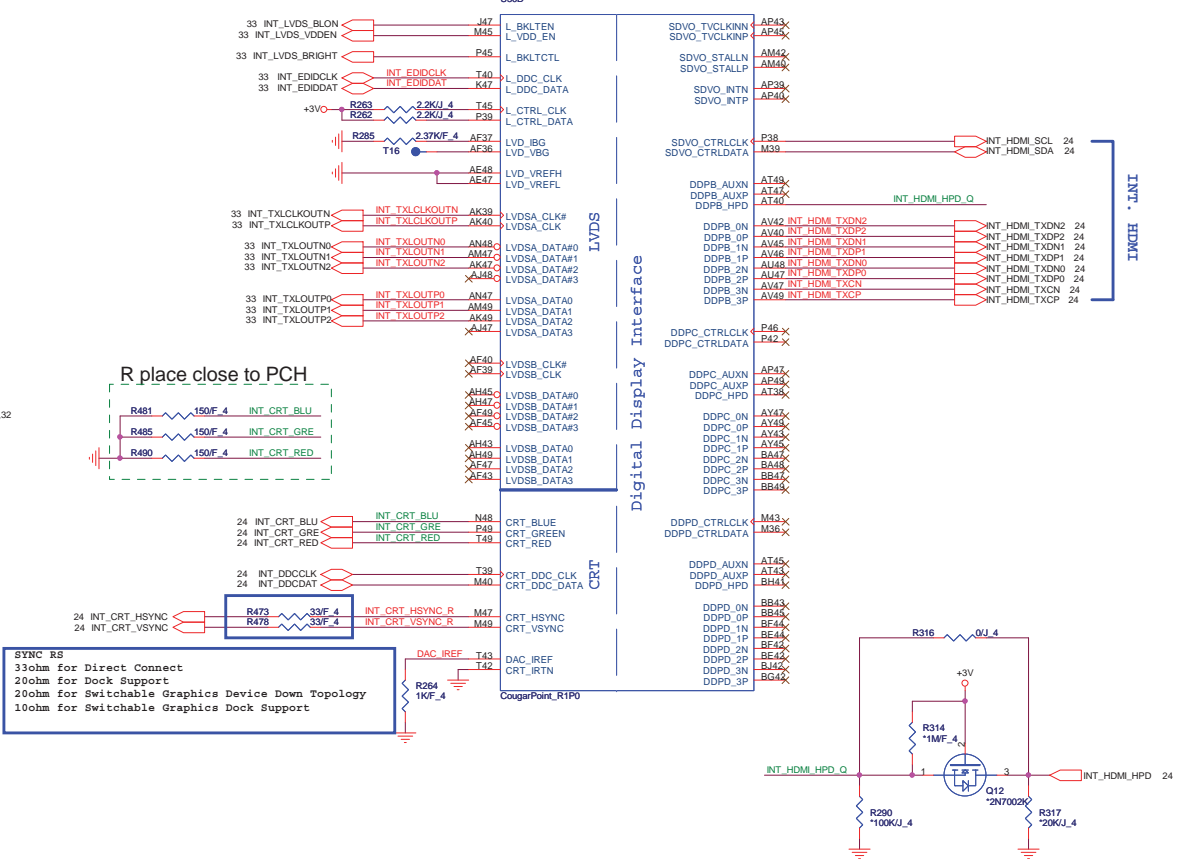
### Cougar Point (DMI, FDI, PM)

U30C

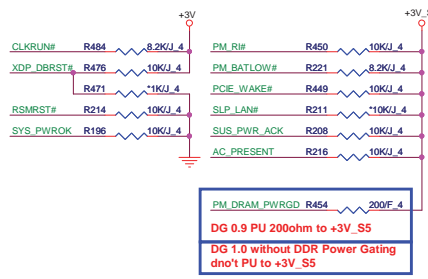


### Cougar Point (LVDS, DDI)

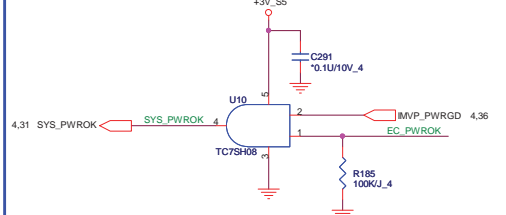
U30D



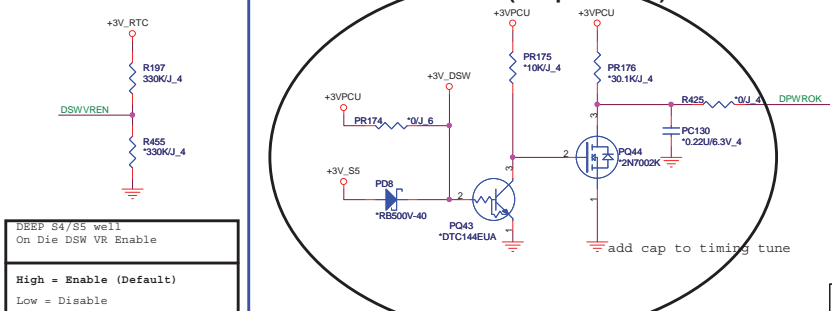
### PCH Pull-high/low(CLG)



### System PWR\_OK(CLG)



### DPWROK FOR DSW (Deep Sx Well)

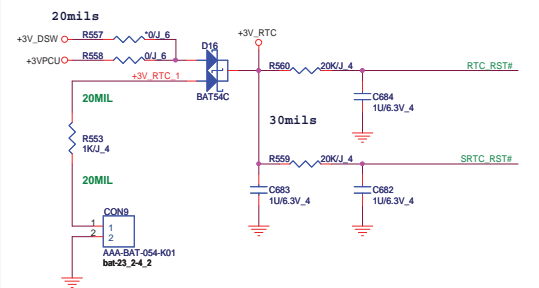


DEEP S4/S5 well  
On Die DSW VR Enable

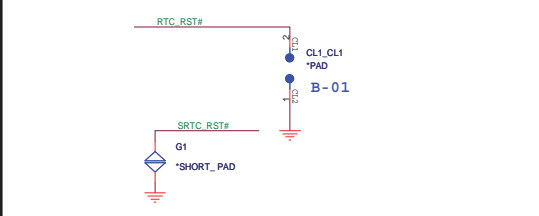
High = Enable (Default)  
Low = Disable



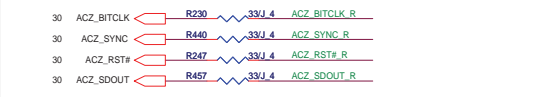
RTC Circuitry(RTC)



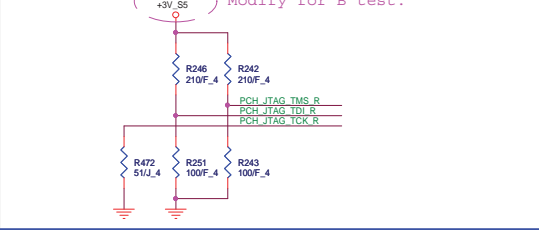
RESET JUMP (Near ROOM DOOR)



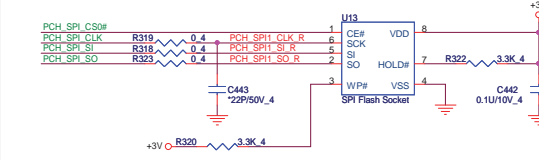
HDA Bus(CLG)



PCH JTAG Debug (CLG)

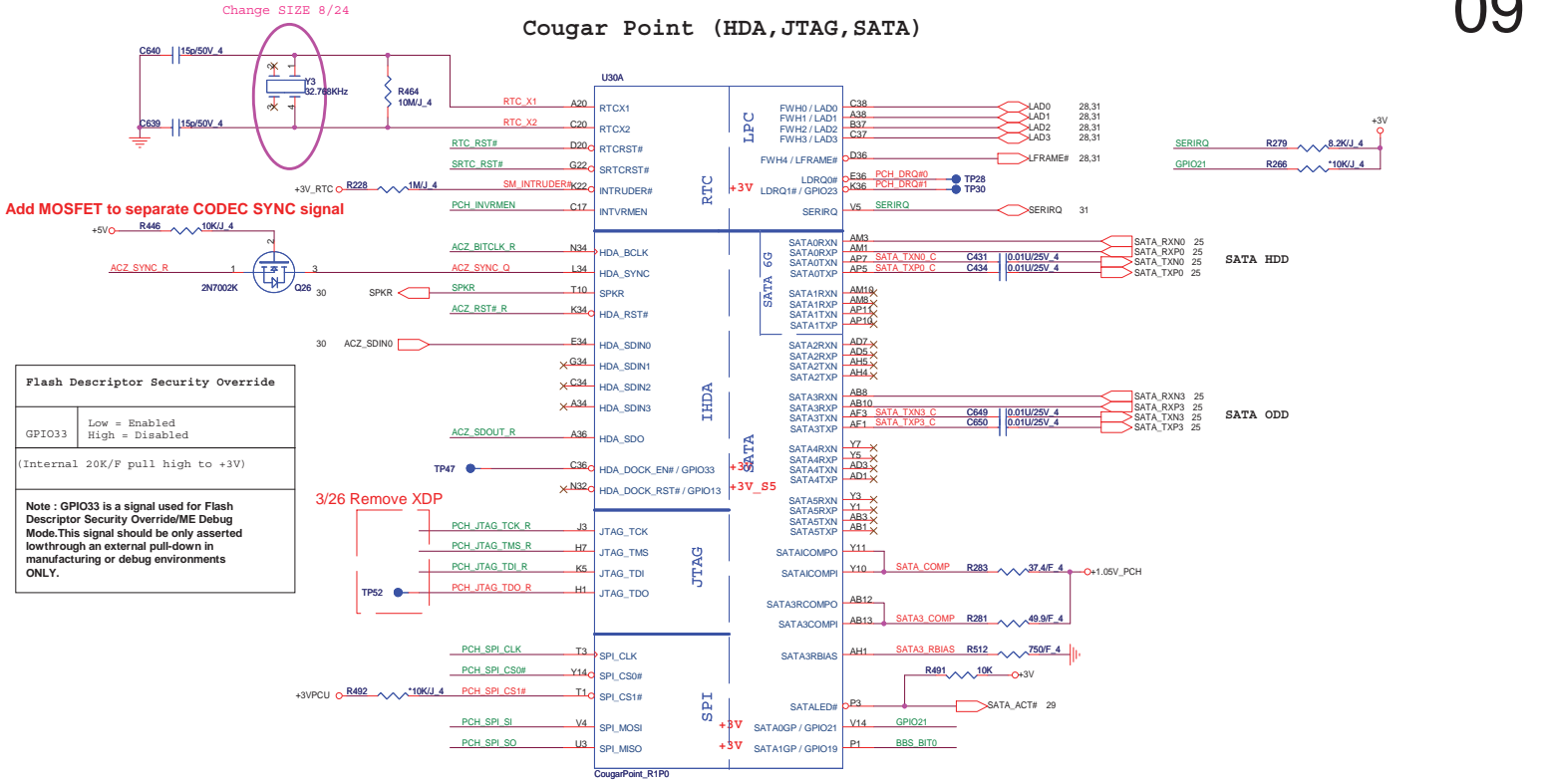


PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH2 (CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting internal PD	PWROK	0 = Default (weak pull-down) 1 = Setting to No-Reboot mode	+3V - R508 - 10KJ 4 - SPKR									
GNT3# / GPIO55	Top-Block Swap Override internal PU	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R237 - 10KJ 4 - PCI_GNT3# 10									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC - R195 - 330KJ 4 - PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1] internal PU	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	+3V - R465 - 10KJ 4 R475 - 10KJ 4
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0] internal PU	PWROK		R468 - 10KJ 4 R489 - 10KJ 4 - BBS_BIT0 10									
HDA_SDO	Flash Descriptor Security internal PD	RSMRST	0 = Default (weak pull-up 20K) 1 = Override	+3V - R441 - 10KJ 4 - ACZ_SDOUT_R 31 - ME_WTR# - R436 - 0.4									
DF_TVS	DMI/FDI Termination voltage internal PD	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-up 20K)	R522 - 2.2KJ 4 - 0+1.8V R523 - 10KJ 4 - DF_TVS 11 H_SNB_IVB# 4									
GPIO28	On-die PLL Voltage Regulator internal PU	RSMRST#	0 = Disable 1 = Enable (Default)	R270 - 10KJ 4 - PLL_OVR_EN 11									
HDA_SYNC	On-Die PLL VR Voltage Select internal PD	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 - R434 - 10KJ 4 - ACZ_SYNC_Q <b>Need check schematic</b>									
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Intel ME TLS with no confidentiality 1 = Intel ME TLS with confidentiality	+3V_S5 - R241 - 1K 4 - PCH_GPIO15 11									

Default weak pull-up on GNT0/1#  
[Need external pull-down for LPC BIOS]

GNT[3:0]# functionality is not available on Mobile. Used as GPIO only.

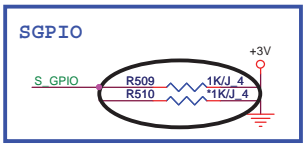
Default weak pull-up on GNT0/1#  
[Need external pull-down for LPC BIOS]

R8361 change to 1K ohm follow Dg1.0 and chklst 1.0  
It needs to be connected to PROC\_SELECT with a 1k±5% pull-up resistor to PCH VCCPND rail and a 4.7k±5% series resistor.

New Add in CPT EDS Rev1.0 at 0316  
, Needs to be pulled High for Huron River platform.

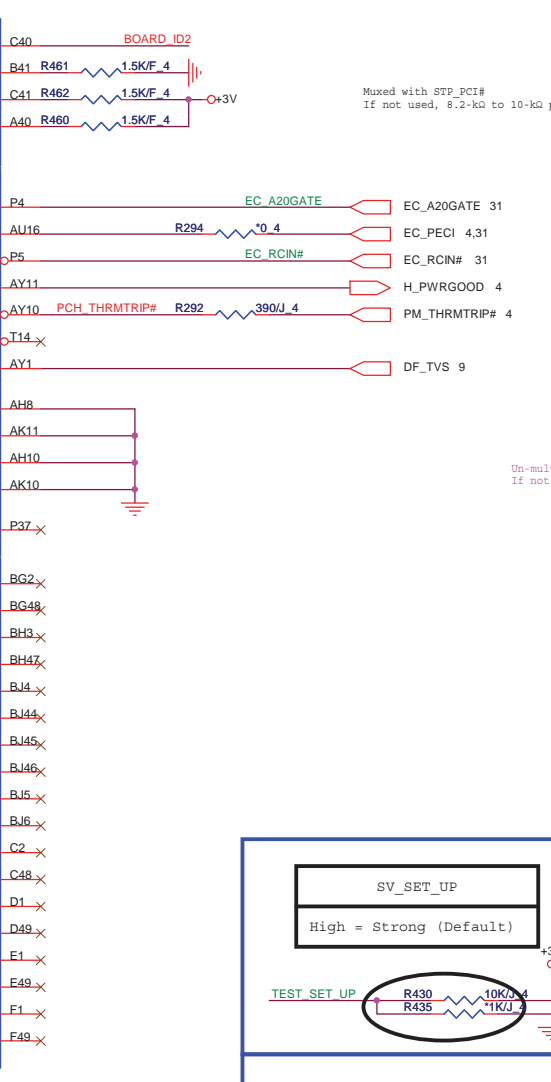
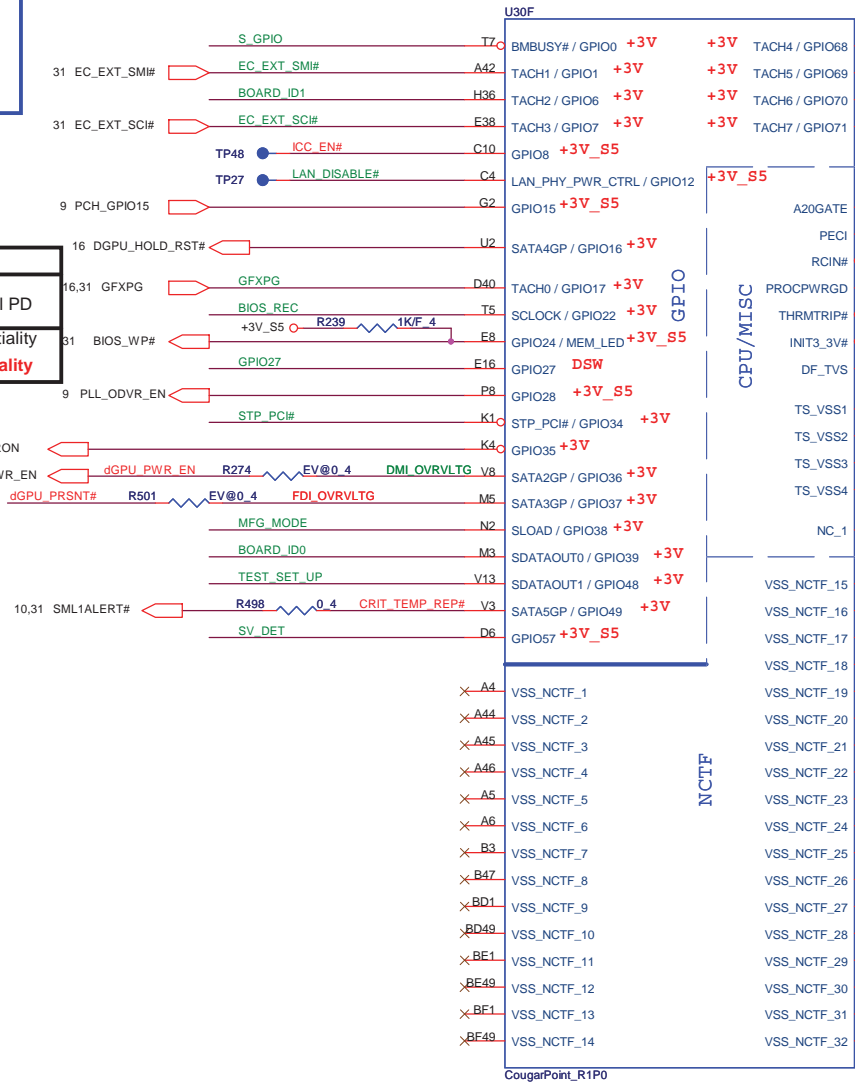


# Cougar Point (GPIO, VSS\_NCTF, RSVD)

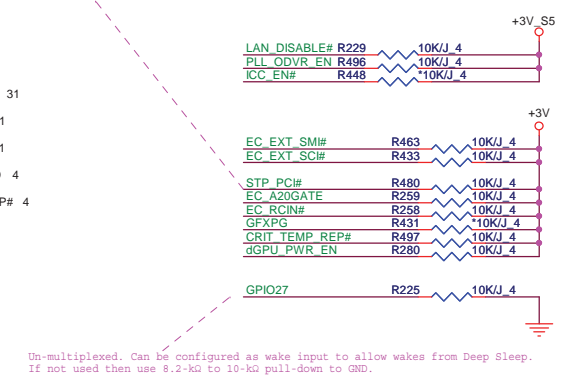


**GPIO15**  
 Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD  
 0 = Intel ME TLS with no confidentiality  
 1 = Intel ME TLS with confidentiality

GPUCORE\_ON 31,39,41 dGPU\_VRON  
 GPU\_PWR\_ON 41 dGPU\_PWR\_EN

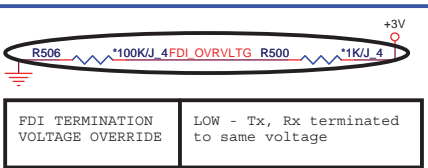


## GPIO Pull-up/Pull-down(CLG)

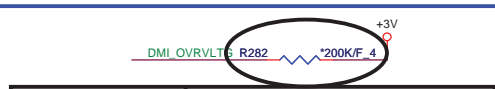


Un-multiplexed. Can be configured as wake input to allow wakes from Deep Sleep. If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

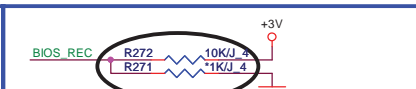
SATA[3:2]GP/GPIO[37:36] internal Pull-down 20K  
 SATA2GP/GPIO36 (FDI\_OVRVLTG) & SATA3GP/GPIO37 (DMI\_OVRVLTG)  
 Sampled at Rising edge of PWROK.  
 Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)  
 NOTE: This signal should NOT be pulled high when strap is sampled



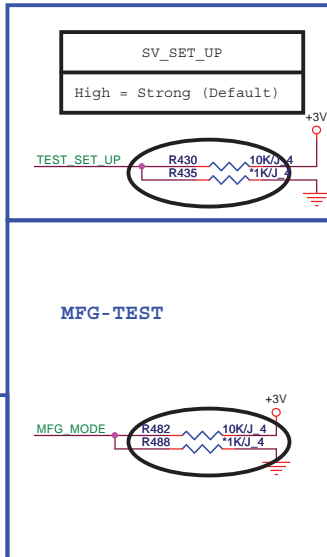
**FDI TERMINATION VOLTAGE OVERRIDE**  
 Low - Tx, Rx terminated to same voltage



**DMI TERMINATION VOLTAGE OVERRIDE**  
 Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

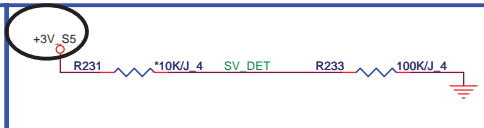


**BIOS RECOVERY**  
 High = Disable (Default)  
 Low = Enable



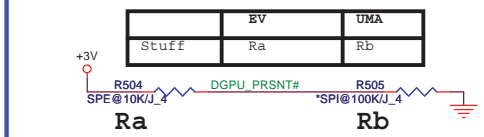
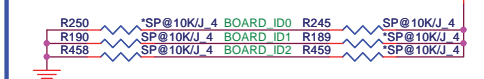
**SV\_SET\_UP**  
 High = Strong (Default)

**MFG-TEST**



[ID0:D1]	0:0	0:1	1:0	1:1
Fuction	UMA	Optimus (Hynix)	Optimus (Samsung)	Rev.

Board ID2 reserve PD

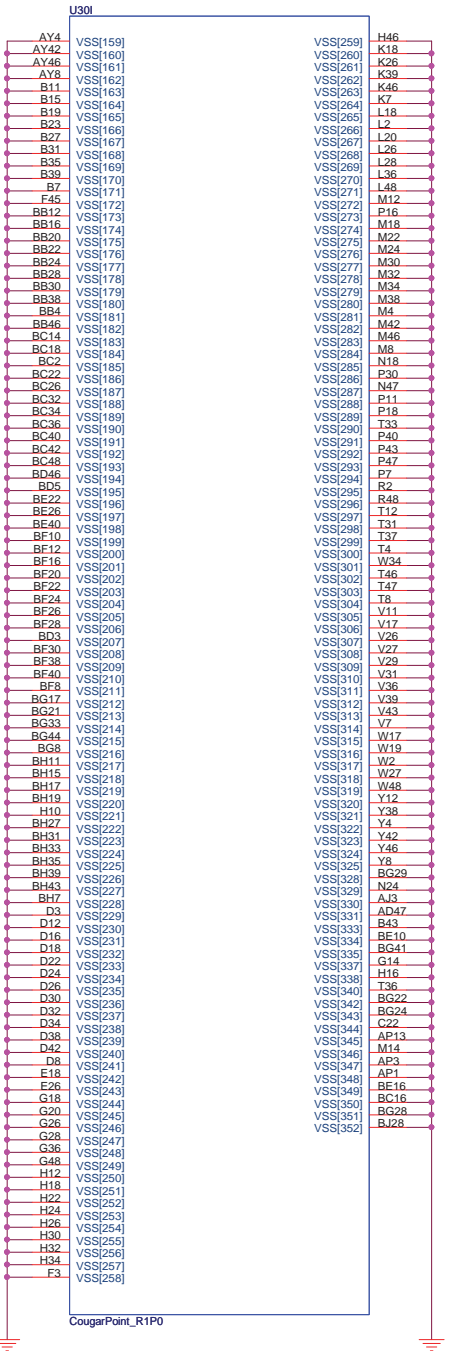
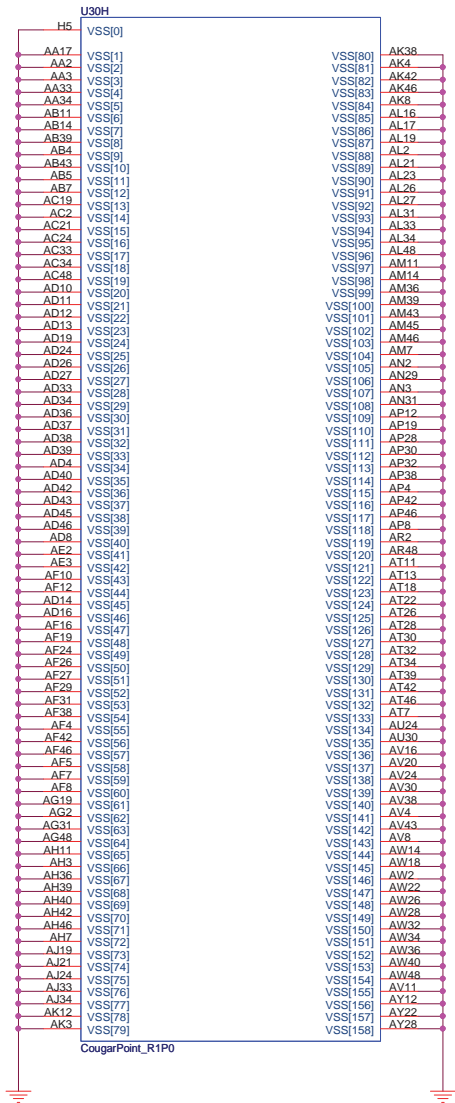


	EV	UMA
Stuff	Ra	Rb

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**PROJECT : FH5**



IBEX PEAK-M (GND)



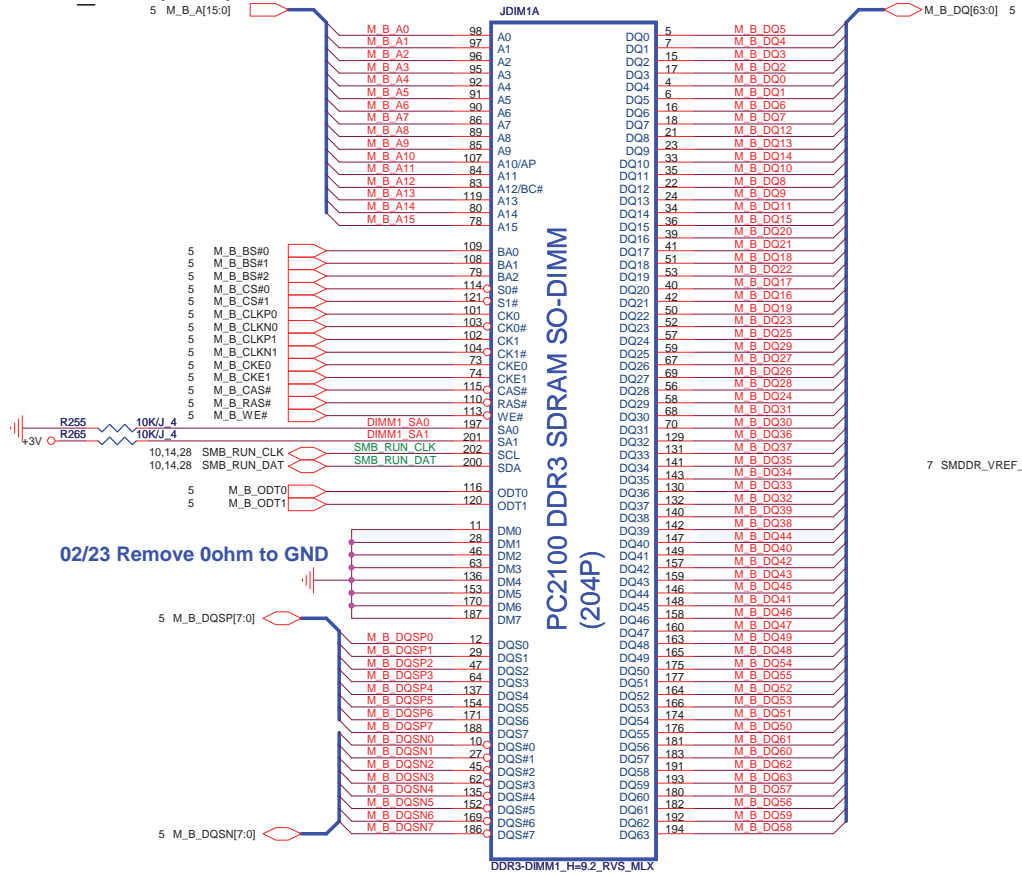
**Quanta Computer Inc.**  
PROJECT : FH5

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	<b>Cougar Point 6/6</b>	1A
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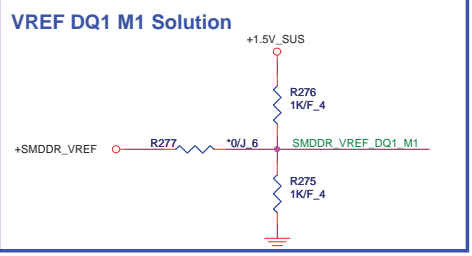
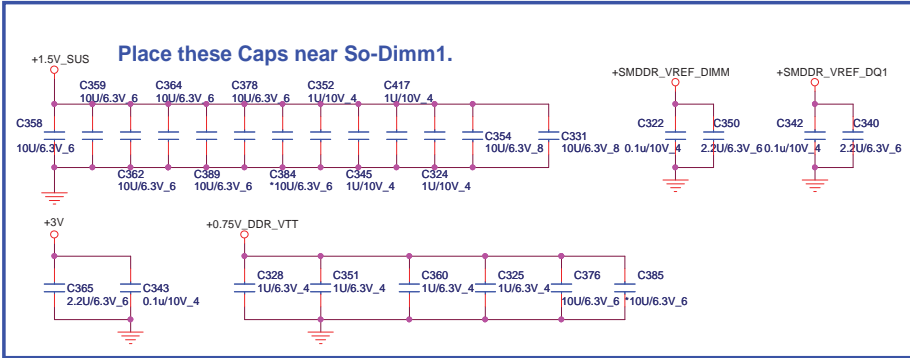




DDR\_RVS (DDR)



02/23 Remove 0ohm to GND

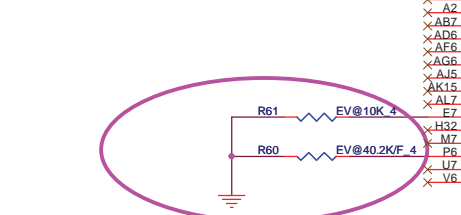
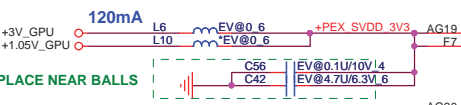
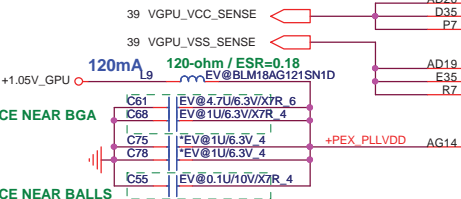
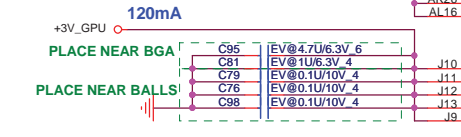
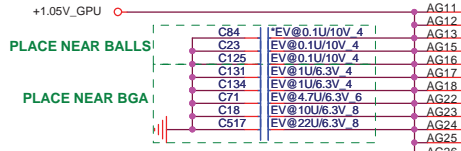
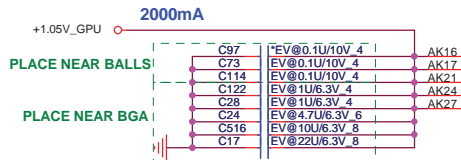


	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

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PROJECT : FH5

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	<b>DDR3 SO-DIMM-1</b>	1A
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PEX\_IOVDD+PEX\_IOVDDQ+PEX\_PLLVDD >2.2A



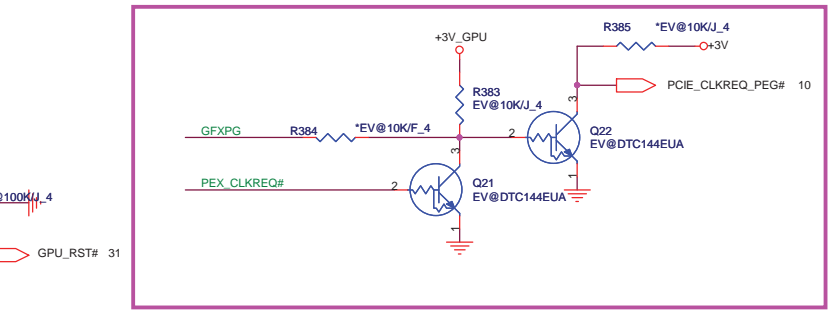
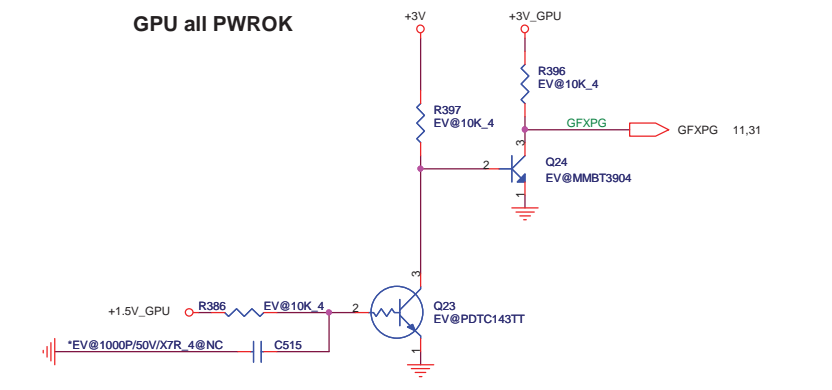
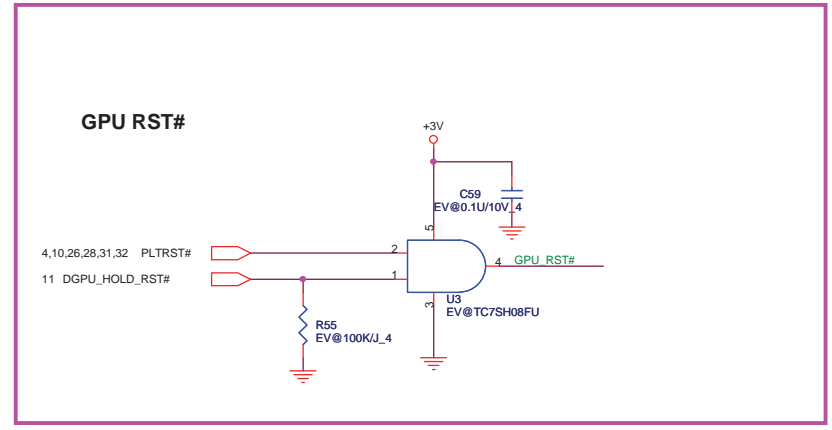
U23A  
fcbg973-mvidia-n12p-ge  
COMMON

PEX_IOVDD_1	AK16
PEX_IOVDD_2	AK17
PEX_IOVDD_3	AK21
PEX_IOVDD_4	AK24
PEX_IOVDD_5	AK27
PEX_IOVDDQ_1	AG11
PEX_IOVDDQ_2	AG12
PEX_IOVDDQ_3	AG13
PEX_IOVDDQ_4	AG15
PEX_IOVDDQ_5	AG16
PEX_IOVDDQ_6	AG17
PEX_IOVDDQ_7	AG18
PEX_IOVDDQ_8	AG22
PEX_IOVDDQ_9	AG23
PEX_IOVDDQ_10	AG24
PEX_IOVDDQ_11	AG25
PEX_IOVDDQ_12	AG26
PEX_IOVDDQ_13	AG15
PEX_IOVDDQ_14	AJ14
PEX_IOVDDQ_15	AJ15
PEX_IOVDDQ_16	AJ19
PEX_IOVDDQ_17	AJ21
PEX_IOVDDQ_18	AJ22
PEX_IOVDDQ_19	AJ24
PEX_IOVDDQ_20	AJ25
PEX_IOVDDQ_21	AJ27
PEX_IOVDDQ_22	AK18
PEX_IOVDDQ_23	AK20
PEX_IOVDDQ_24	AK23
PEX_IOVDDQ_25	AK26
PEX_IOVDDQ_26	AL16

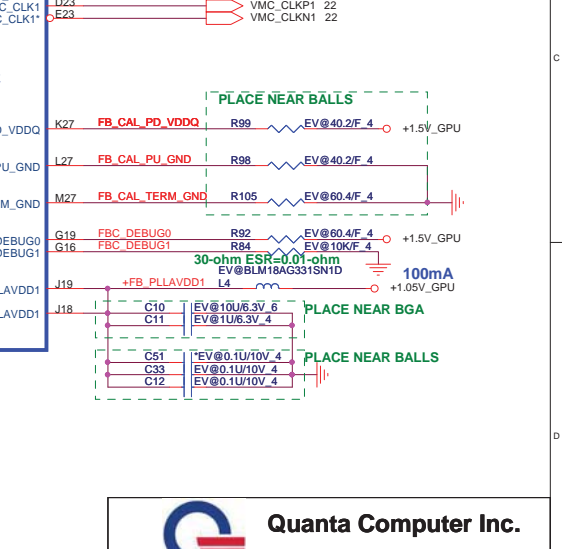
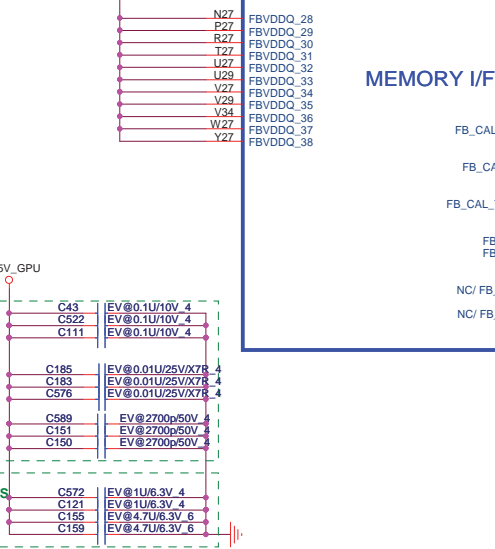
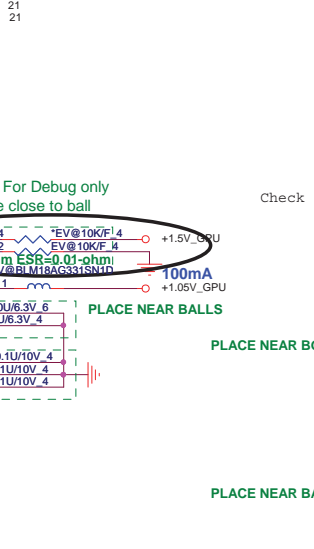
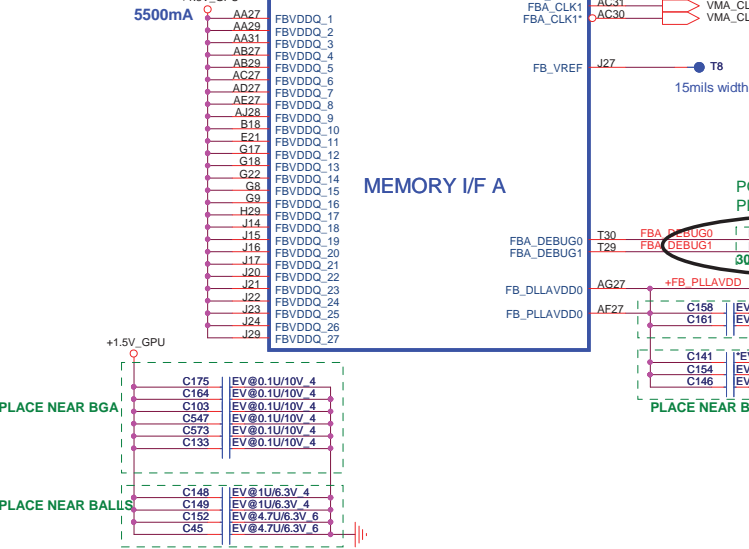
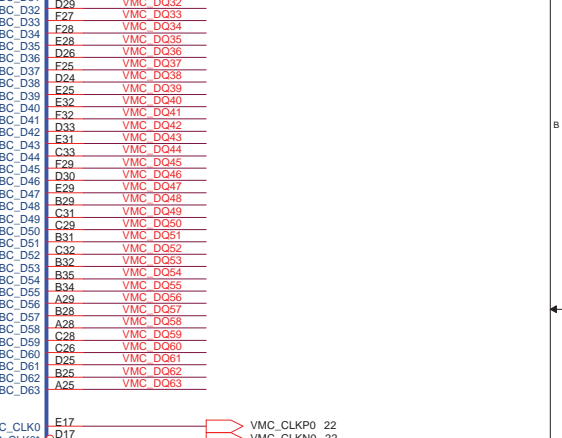
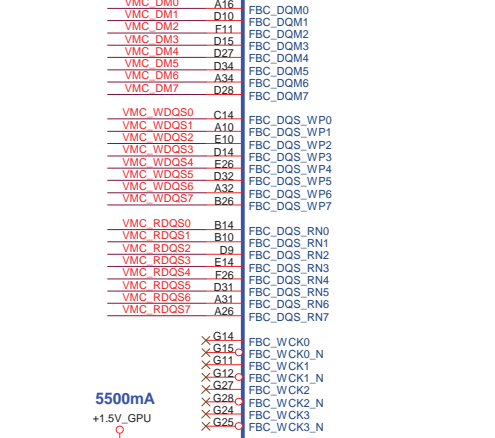
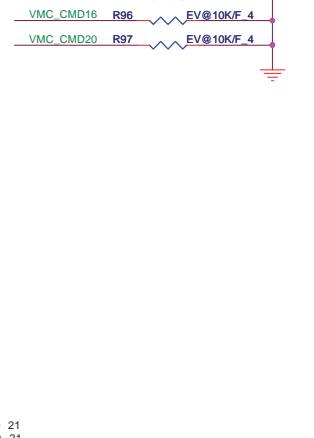
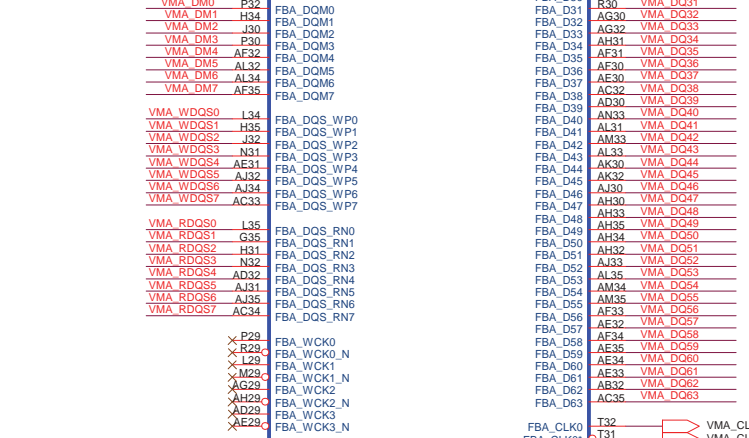
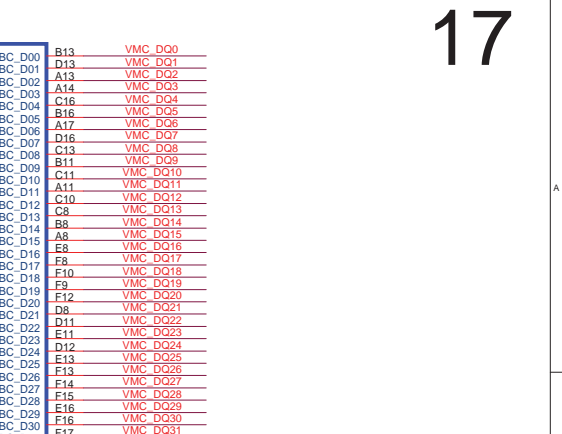
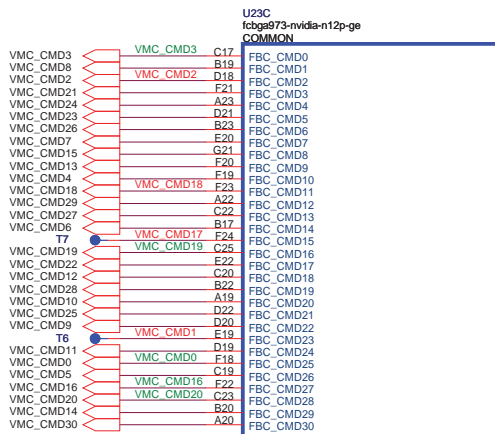
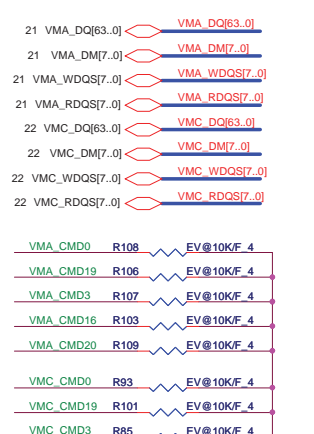
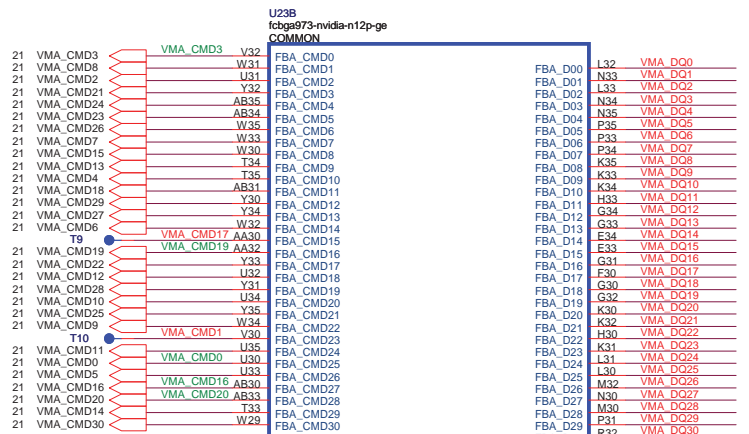
PCI EXPRESS

PEX_TX0	AL17	PEG RXP15 C	C80	EV@0.1U/10V_4	PEG_RXP15_4
PEX_TX0	AM17	PEG RXN15 C	C89	EV@0.1U/10V_4	PEG_RXN15_4
PEX_TX1	AM18	PEG RXP14 C	C109	EV@0.1U/10V_4	PEG_RXP14_4
PEX_TX1	AM19	PEG RXN14 C	C102	EV@0.1U/10V_4	PEG_RXN14_4
PEX_TX2	AK19	PEG RXP13 C	C113	EV@0.1U/10V_4	PEG_RXP13_4
PEX_TX2	AK19	PEG RXN13 C	C108	EV@0.1U/10V_4	PEG_RXN13_4
PEX_TX3	AL20	PEG RXP12 C	C106	EV@0.1U/10V_4	PEG_RXP12_4
PEX_TX3	AM20	PEG RXN12 C	C112	EV@0.1U/10V_4	PEG_RXN12_4
PEX_TX4	AM21	PEG RXP11 C	C120	EV@0.1U/10V_4	PEG_RXP11_4
PEX_TX4	AM22	PEG RXN11 C	C123	EV@0.1U/10V_4	PEG_RXN11_4
PEX_TX5	AK22	PEG RXP10 C	C124	EV@0.1U/10V_4	PEG_RXP10_4
PEX_TX5	AK22	PEG RXN10 C	C127	EV@0.1U/10V_4	PEG_RXN10_4
PEX_TX6	AL23	PEG RXP9 C	C129	EV@0.1U/10V_4	PEG_RXP9_4
PEX_TX6	AM23	PEG RXN9 C	C137	EV@0.1U/10V_4	PEG_RXN9_4
PEX_TX7	AM24	PEG RXP8 C	C128	EV@0.1U/10V_4	PEG_RXP8_4
PEX_TX7	AM25	PEG RXN8 C	C136	EV@0.1U/10V_4	PEG_RXN8_4
PEX_TX8	AK25	PEG RXP7 C	C130	EV@0.1U/10V_4	PEG_RXP7_4
PEX_TX8	AK25	PEG RXN7 C	C138	EV@0.1U/10V_4	PEG_RXN7_4
PEX_TX9	AL26	PEG RXP6 C	C143	EV@0.1U/10V_4	PEG_RXP6_4
PEX_TX9	AM26	PEG RXN6 C	C145	EV@0.1U/10V_4	PEG_RXN6_4
PEX_TX10	AM27	PEG RXP5 C	C144	EV@0.1U/10V_4	PEG_RXP5_4
PEX_TX10	AM28	PEG RXN5 C	C147	EV@0.1U/10V_4	PEG_RXN5_4
PEX_TX11	AL28	PEG RXP4 C	C160	EV@0.1U/10V_4	PEG_RXP4_4
PEX_TX11	AK28	PEG RXN4 C	C153	EV@0.1U/10V_4	PEG_RXN4_4
PEX_TX12	AK29	PEG RXP3 C	C162	EV@0.1U/10V_4	PEG_RXP3_4
PEX_TX12	AL29	PEG RXN3 C	C157	EV@0.1U/10V_4	PEG_RXN3_4
PEX_TX13	AM29	PEG RXP2 C	C165	EV@0.1U/10V_4	PEG_RXP2_4
PEX_TX13	AM30	PEG RXN2 C	C168	EV@0.1U/10V_4	PEG_RXN2_4
PEX_TX14	AM31	PEG RXP1 C	C167	EV@0.1U/10V_4	PEG_RXP1_4
PEX_TX14	AM32	PEG RXN1 C	C170	EV@0.1U/10V_4	PEG_RXN1_4
PEX_TX15	AK32	PEG RXP0 C	C171	EV@0.1U/10V_4	PEG_RXP0_4
PEX_TX15	AP32	PEG RXN0 C	C173	EV@0.1U/10V_4	PEG_RXN0_4

PEX_REFCLK	AR16	CLK_PCIE_VGAP	10	
PEX_REFCLK*	AR17	CLK_PCIE_VGAN	10	
PEX_TSTCLK_OUT	AJ17	PEX TSTCLK	R89	EV@200K/J_4
PEX_TSTCLK_OUT*	AJ18	PEX TSTCLK#		
PEX_RST#	AM16	VGA_RST#	R87	EV@0/J_4
PEX_CLKREQ#	AR13	PEG CLKREQ#	R401	EV@10K/J_4
PEX_TERM	AG21	PEG_TERM	R94	EV@2.49K/F_4
TESTMODE	AP35	TESTMODE	R110	EV@10K/J_4



Ffor N12P-GE, they can be unstuffed by default



MEMORY I/F A

POP For Debug only Place close to ball

MEMORY I/F C

PLACE NEAR BALLS

PLACE NEAR BGA

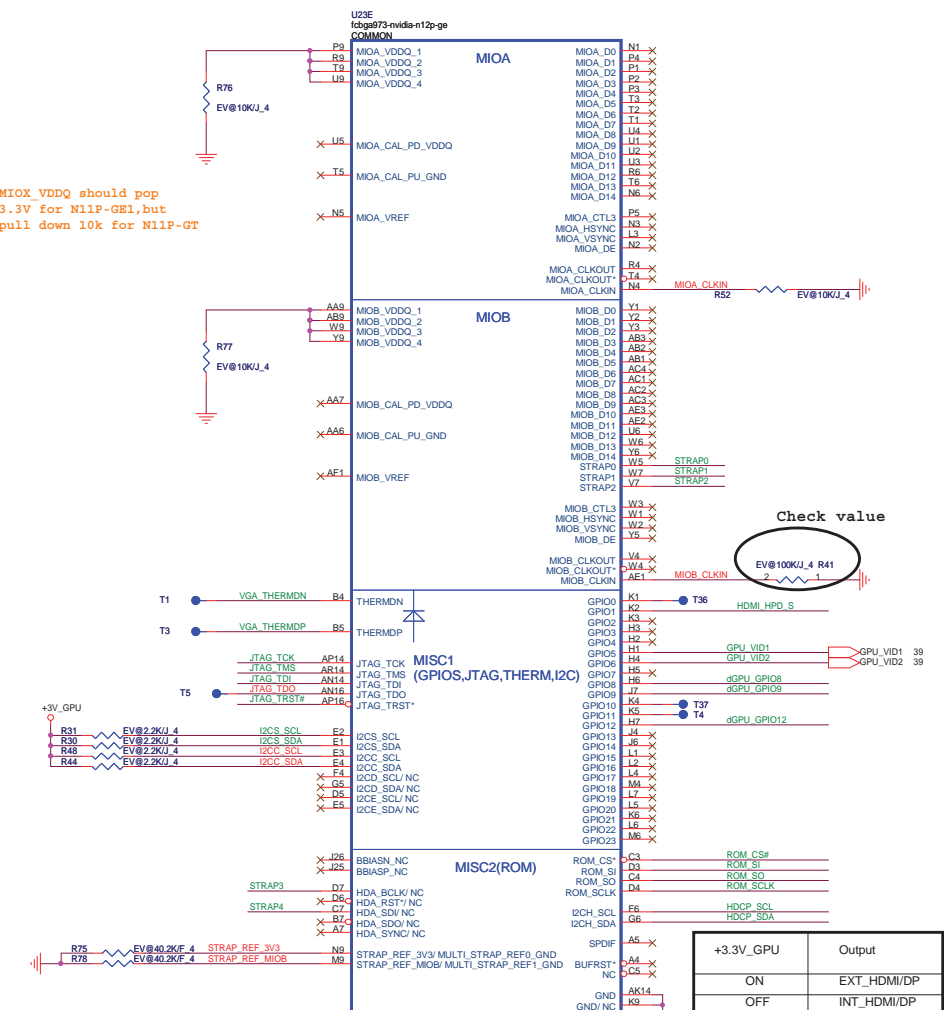
PLACE NEAR BALLS

PLACE NEAR BALLS

**Quanta Computer Inc.**  
PROJECT : FH5  
N12P-GE (MEMORY I/F) 2/5  
Rev 1A

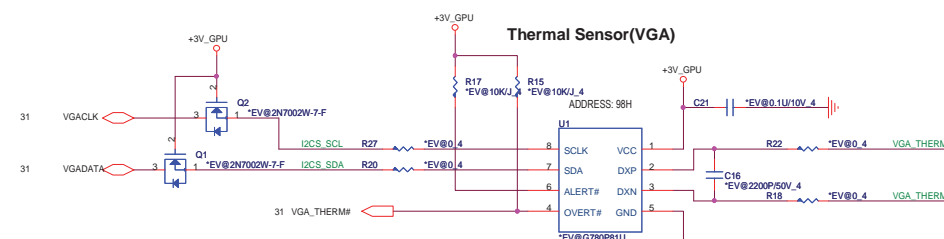
Size: Document Number: N12P-GE (MEMORY I/F) 2/5  
Date: Monday, September 27, 2010 Sheet 17 of 41





MIOX\_VDDQ should pop 3.3V for N11P-GE1, but pull down 10k for N11P-GT

Check value EV@10KJ\_4 R41 2 1



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0011
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVICE[3]	PCI_DEVICE[2]	PCI_DEVICE[1]	PCI_DEVICE[0]	0101
STRAP3	SOR_EXPOSED[3]	SOR_EXPOSED[2]	SOR_EXPOSED[1]	SOR_EXPOSED[0]	TBD
STRAP4	Reserve	Reserve	PCI_MAX_SPEED	DP_PLL_VDD3	TBD

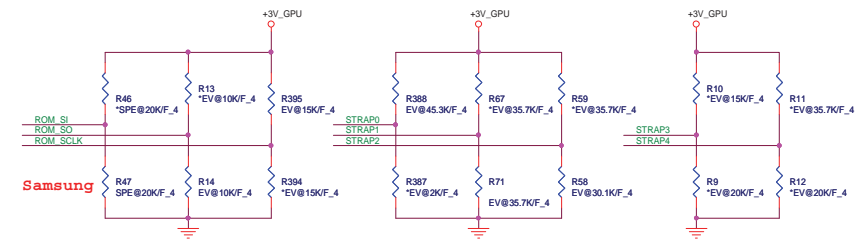
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKDSLGH500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKDSLZWTW01	AKDSLZWTW00	H5TQ1G63BFR-11C
0x6(0110)	800MHz 1GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW01	H5TQ2G63BFR-12C
0x7(0111)	800MHz 1GB(128M*16) Samsung	AKD5MGGT501	AKD5MGGT502	K4W2G1646E-HC12

4.99K/F\_4 ==> CS24992FB26  
 10K/F\_4 ==> CS31002FB26  
 15K/F\_4 ==> CS31502FB24  
 20K/F\_4 ==> CS32002FB29  
 30.1K/F\_4 ==> CS33012FB18  
 35.7K/F\_4 ==> CS33572FB13  
 45.3K/F\_4 ==> CS34532FB18

ROM\_SI Strap Bit for RAM Mapping



N11P-GE1 DevID is 0x0DFE, so pull up ROM\_SCLK with 15Kohm and STRAP2 pull up 35Kohm

GPIO ASSIGNMENTS

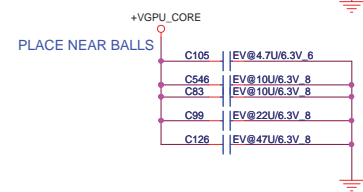
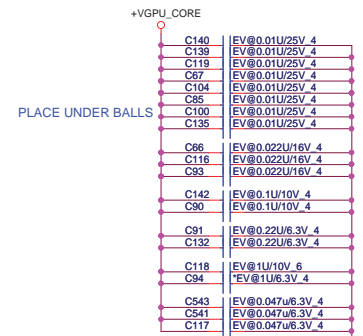
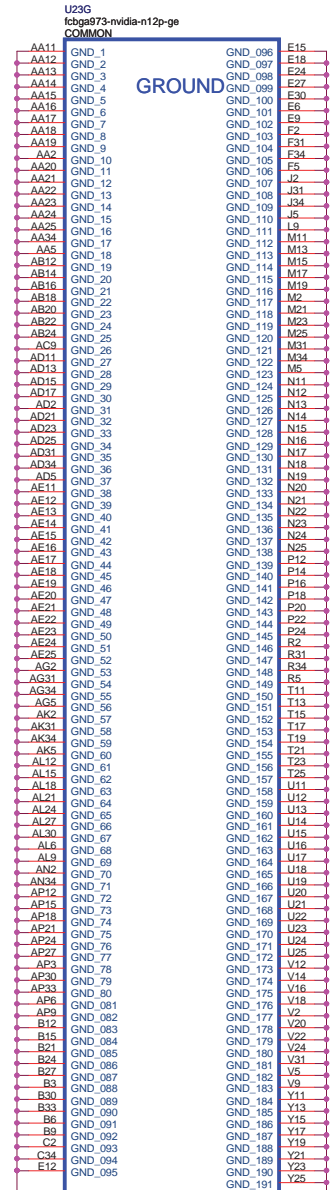
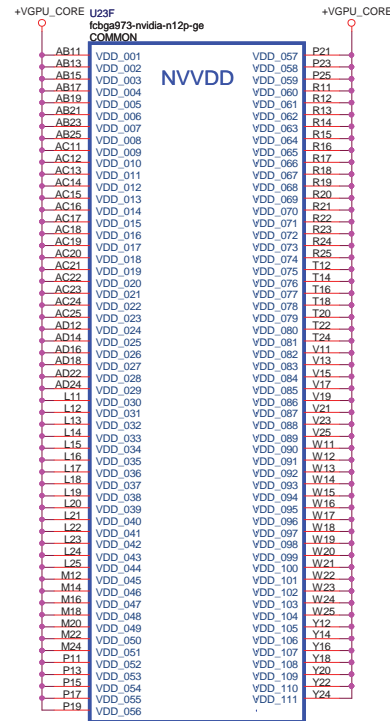
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	N/A	
3	OUT	N/A	
4	OUT	N/A	
5	OUT	N/A	NV_VDD VID0
6	OUT	N/A	NV_VDD VID1
7	OUT	N/A	NV_VDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI_SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

NV VID Table for N12P-GE

GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	0.825V
1	0	0.9V
0	1	0.95V
1	1	TBD

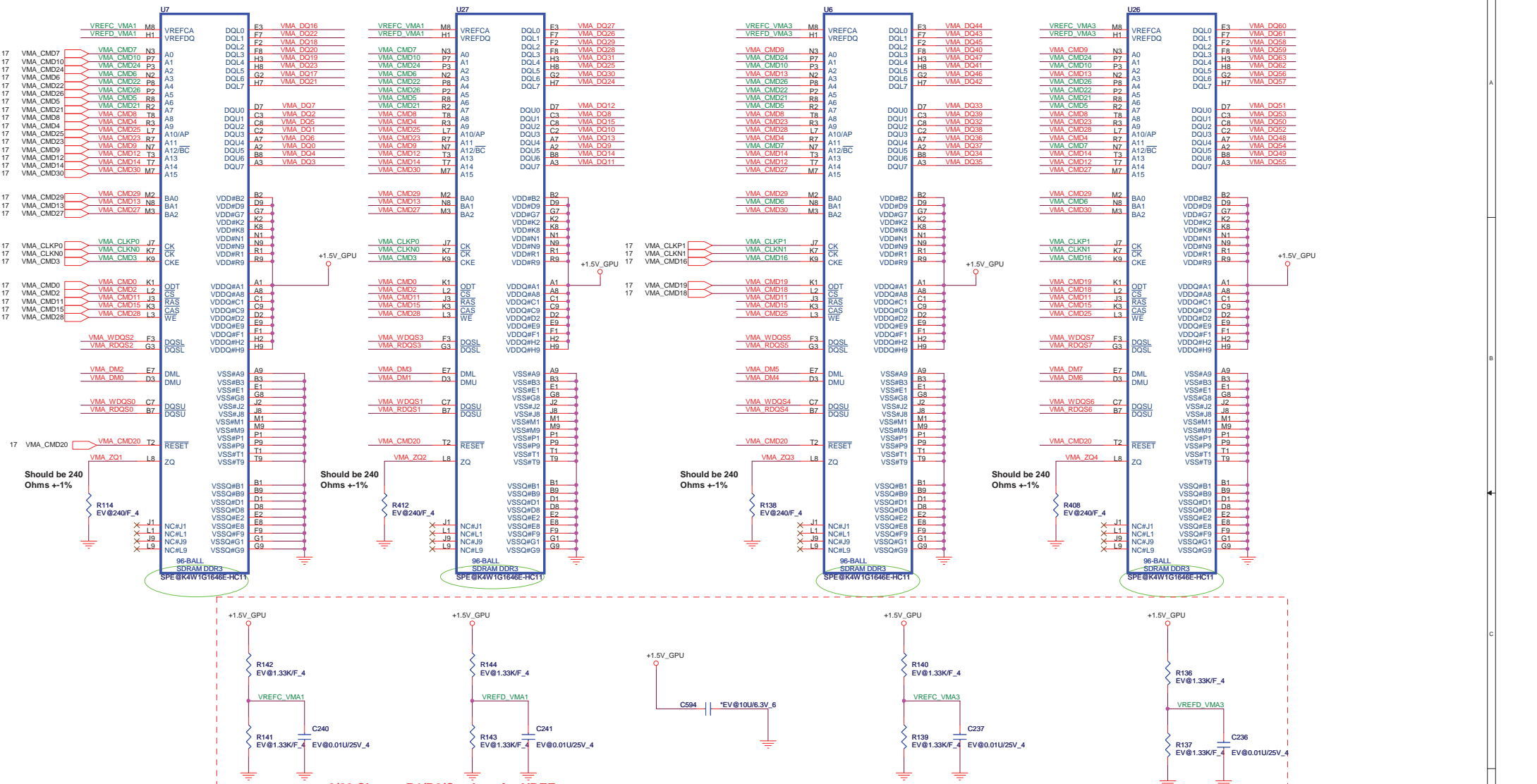
Modify 8/18





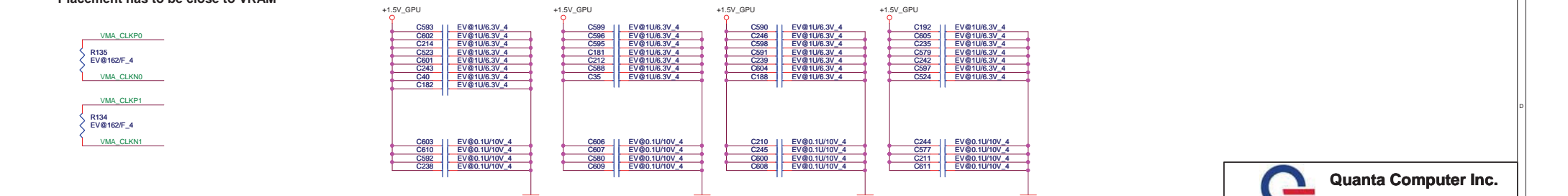


# CHANNEL A: 512MB/1024MB DDR3



Placement has to be close to VRAM

3/22 Change R1/R2/C values for VREF



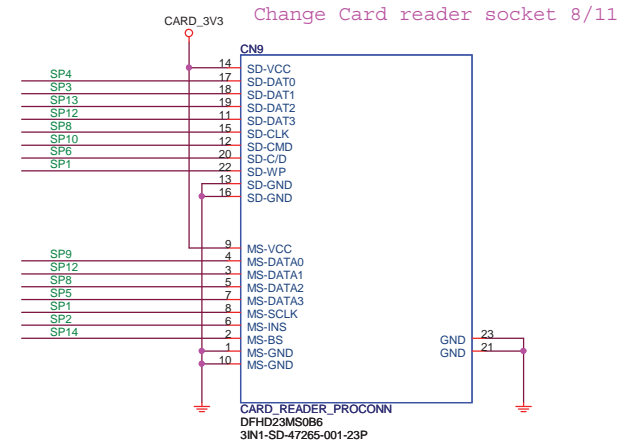
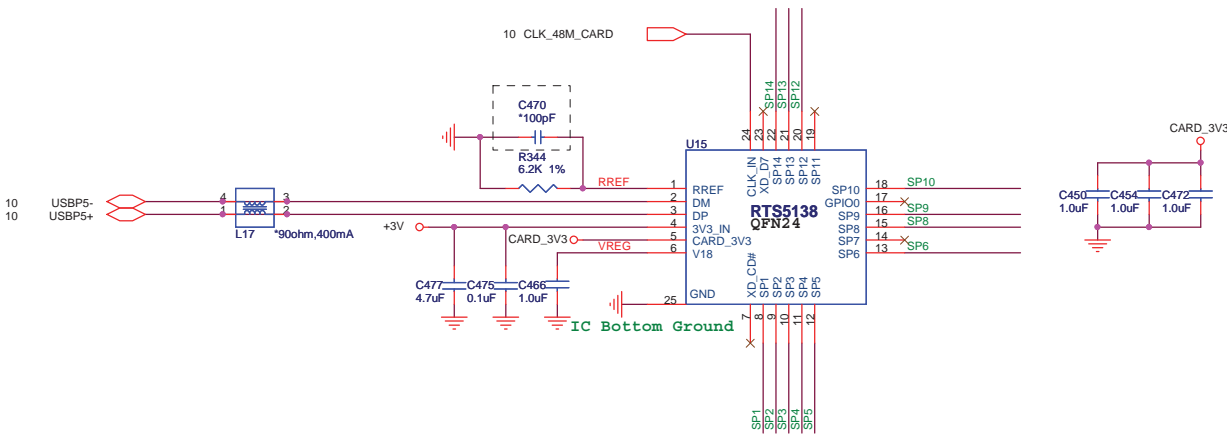
GE1 FOR 243 BUT GT/E REQUIRE CHECK FAE



# RST5138 SIDO

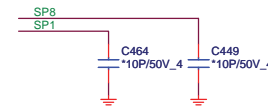
## SD/SDHC CARD READER

## SD/MS CONNDETOR



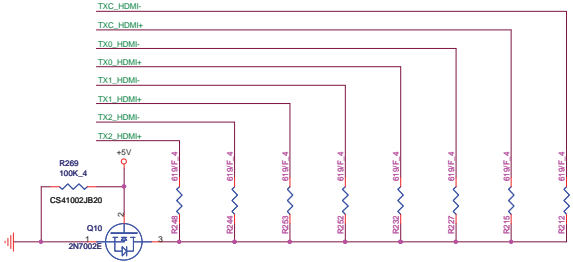
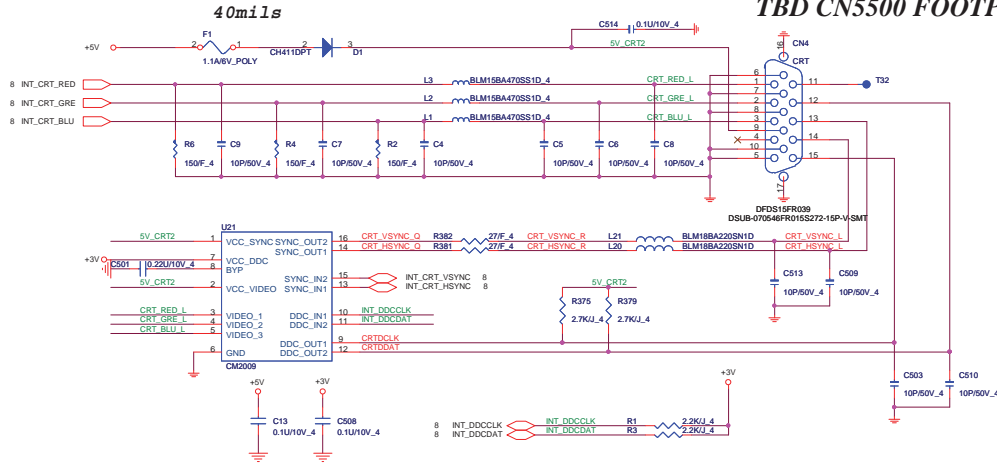
### Share Pin

Share Pin	XD	MS	SD
SP1	XDR/B#	MS_CLK	SD_WP
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#		SD_D1
SP4	XD_CLE	MS_D7	SD_D0
SP5	XD_ALE	MS_D3	SD_D7
SP6	XD_WE#		SD_CD#
SP7	XD_WP	MS_D6	SD_D6
SP8	XD_D0	MS_D2	SD_CLK
SP9	XD_D1	MS_D0	SD_D5
SP10	XD_D2		SD_CMD
SP11	XD_D3	MS_D4	SD_D4
SP12	XD_D4	MS_D1	SD_D3
SP13	XD_D5	MS_D5	SD_D2
SP14	XD_D6	MS_BS	



CRT CONN/DDC LEVEL SHIFT

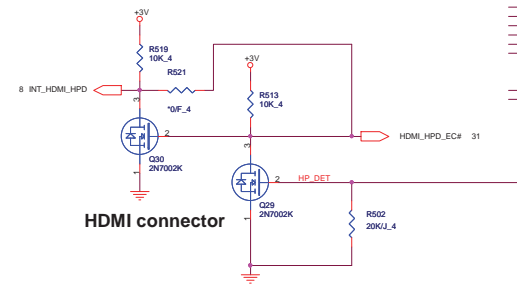
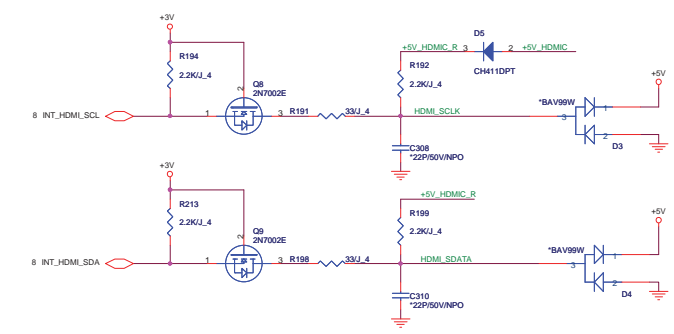
TBD CN5500 FOOTPRINT



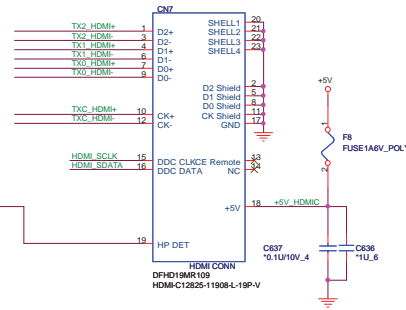
PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET AVOID STUBS TO ALL DIFFERENTIAL TRACES

INT-HDMI

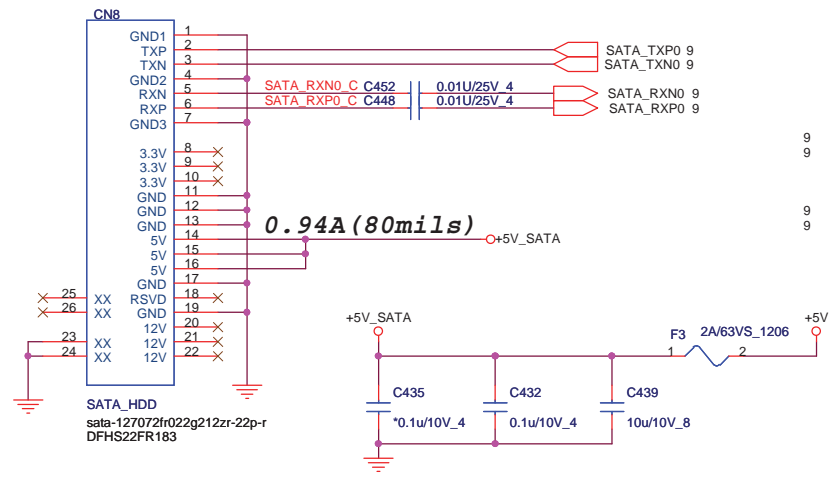
		PLACE AC CAP CLOSE TO CONNECTOR		
8 INT_HDMI_TXCN	INT_HDMI_TXCN	C311	0.1u/10V_4	TXC_HDMI+
8 INT_HDMI_TXCP	INT_HDMI_TXCP	C312	0.1u/10V_4	TXC_HDMI-
8 INT_HDMI_TXDN0	INT_HDMI_TXDN0	C327	0.1u/10V_4	TX0_HDMI+
8 INT_HDMI_TXDP0	INT_HDMI_TXDP0	C329	0.1u/10V_4	TX0_HDMI-
8 INT_HDMI_TXDN1	INT_HDMI_TXDN1	C313	0.1u/10V_4	TX1_HDMI+
8 INT_HDMI_TXDP1	INT_HDMI_TXDP1	C318	0.1u/10V_4	TX1_HDMI-
8 INT_HDMI_TXDN2	INT_HDMI_TXDN2	C330	0.1u/10V_4	TX2_HDMI+
8 INT_HDMI_TXDP2	INT_HDMI_TXDP2	C323	0.1u/10V_4	TX2_HDMI-



HDMI CONN

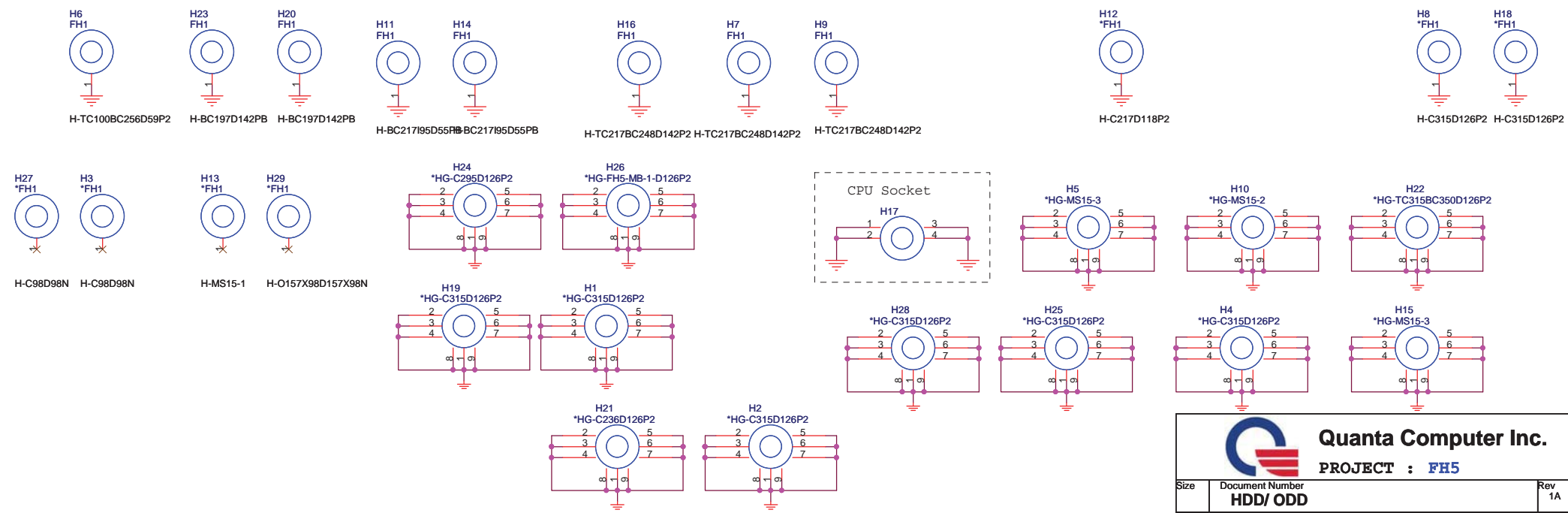
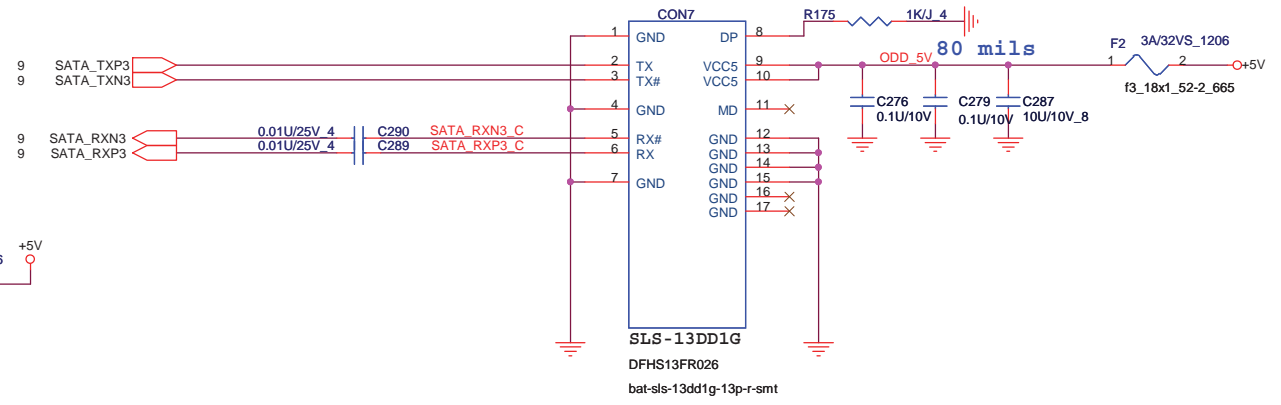


# 2.5" SATA HDD



# SATA ODD

## ODD CONN

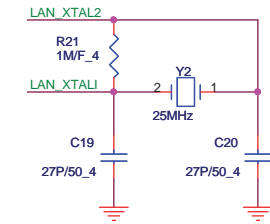


**Quanta Computer Inc.**  
PROJECT : FH5

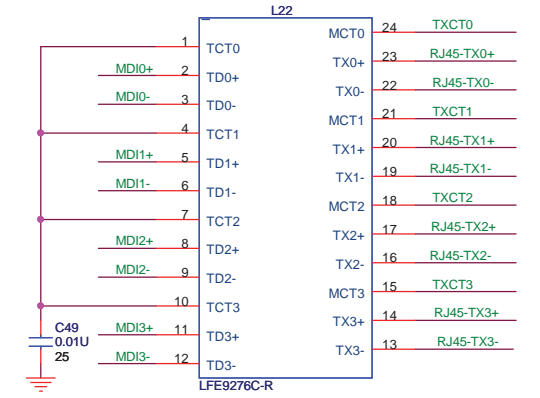
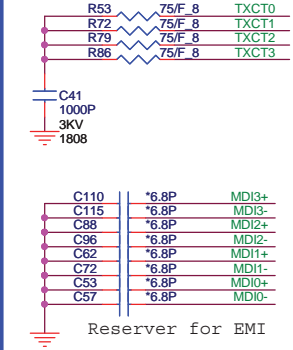
Size	Document Number	Rev
	<b>HDD/ ODD</b>	1A
Date:	Monday, September 27, 2010	Sheet 25 of 41

# LAN EEPROM(DEL)

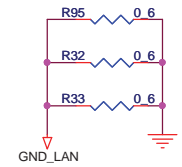
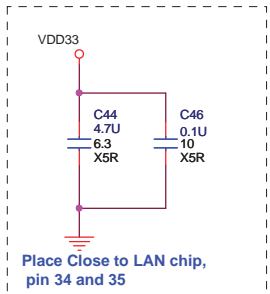
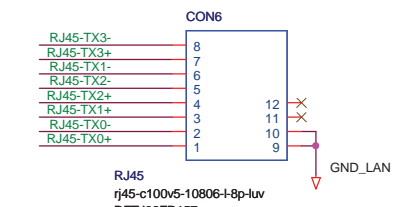
## X'tal 25MHz



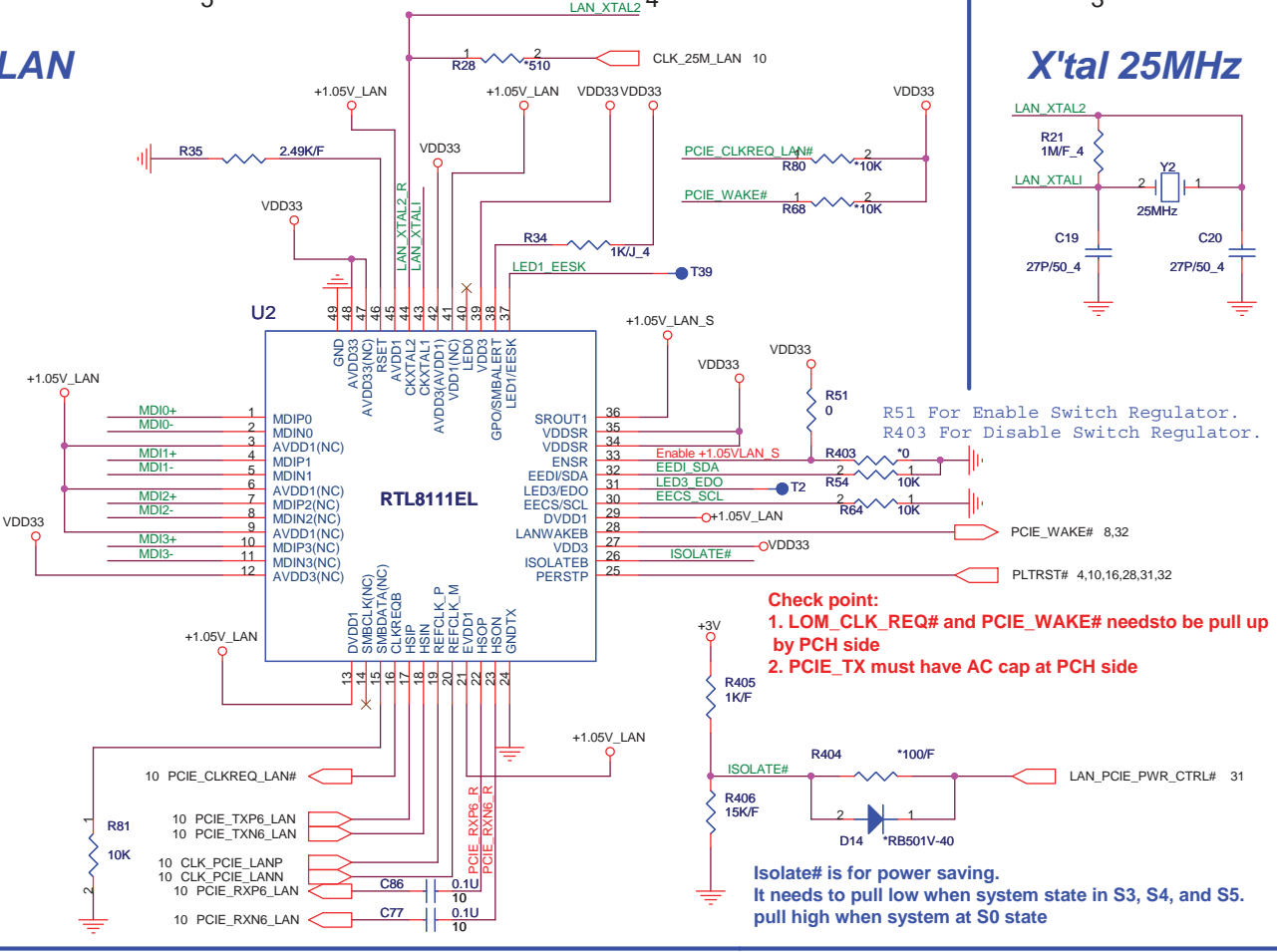
## Transformer



## RJ45



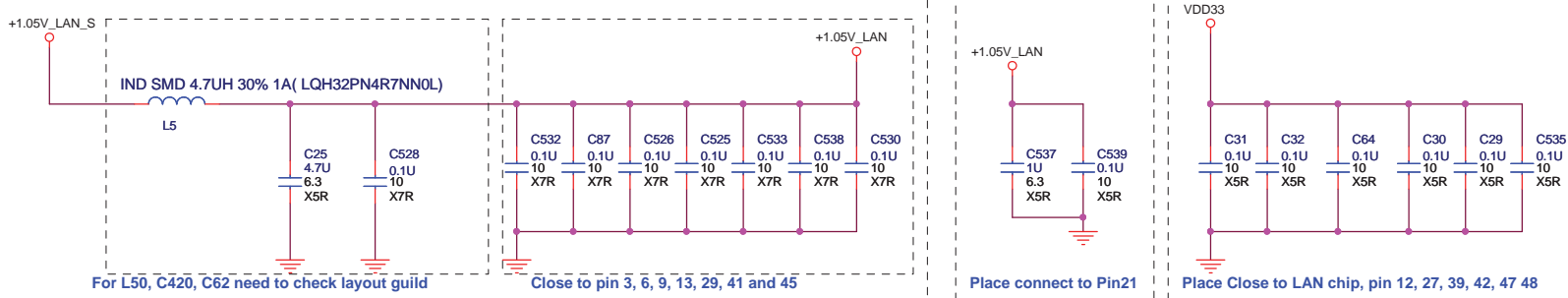
# LAN



**Check point:**  
 1. LOM\_CLK\_REQ# and PCIE\_WAKE# need to be pull up by PCH side  
 2. PCIE\_TX must have AC cap at PCH side

**Isolate# is for power saving.**  
 It needs to pull low when system state in S3, S4, and S5. pull high when system at S0 state

# LAN Power



For L50, C420, C62 need to check layout guid

Close to pin 3, 6, 9, 13, 29, 41 and 45

Place connect to Pin21

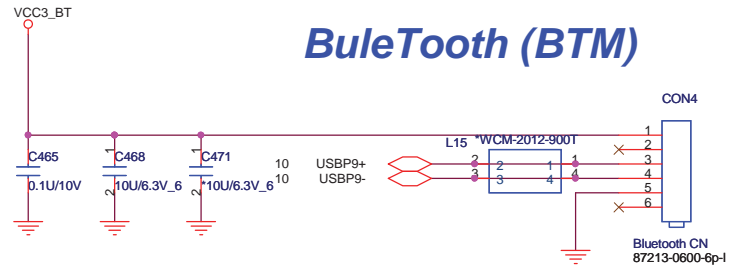
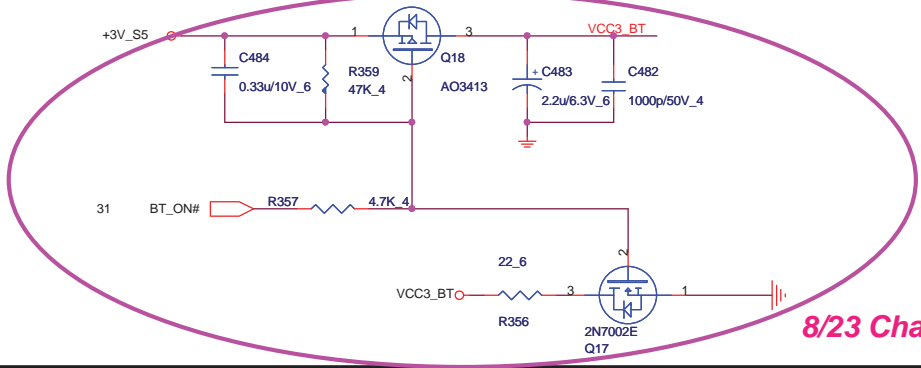
Place Close to LAN chip, pin 12, 27, 39, 42, 47 48

REQ by layout

**Quanta Computer Inc.**  
**PROJECT : FH5**  
**LAN\_RTL8111E-GR/RJ45**

Size	Document Number	Rev
		1A
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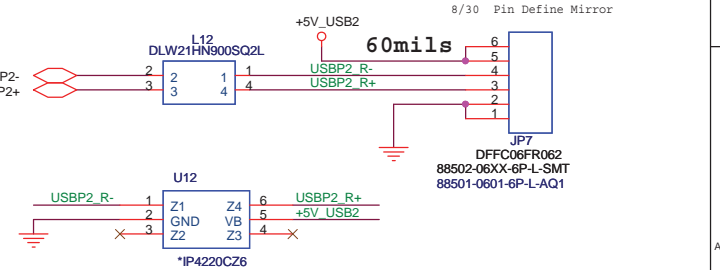
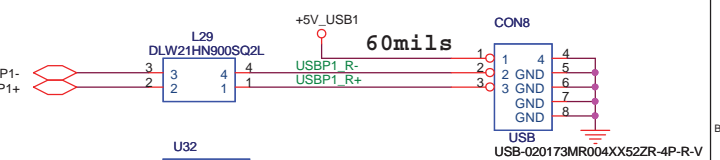
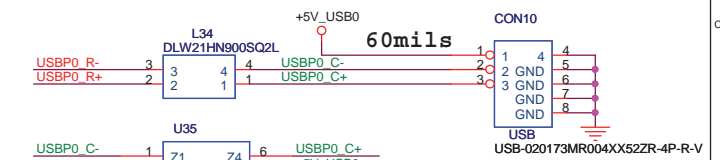
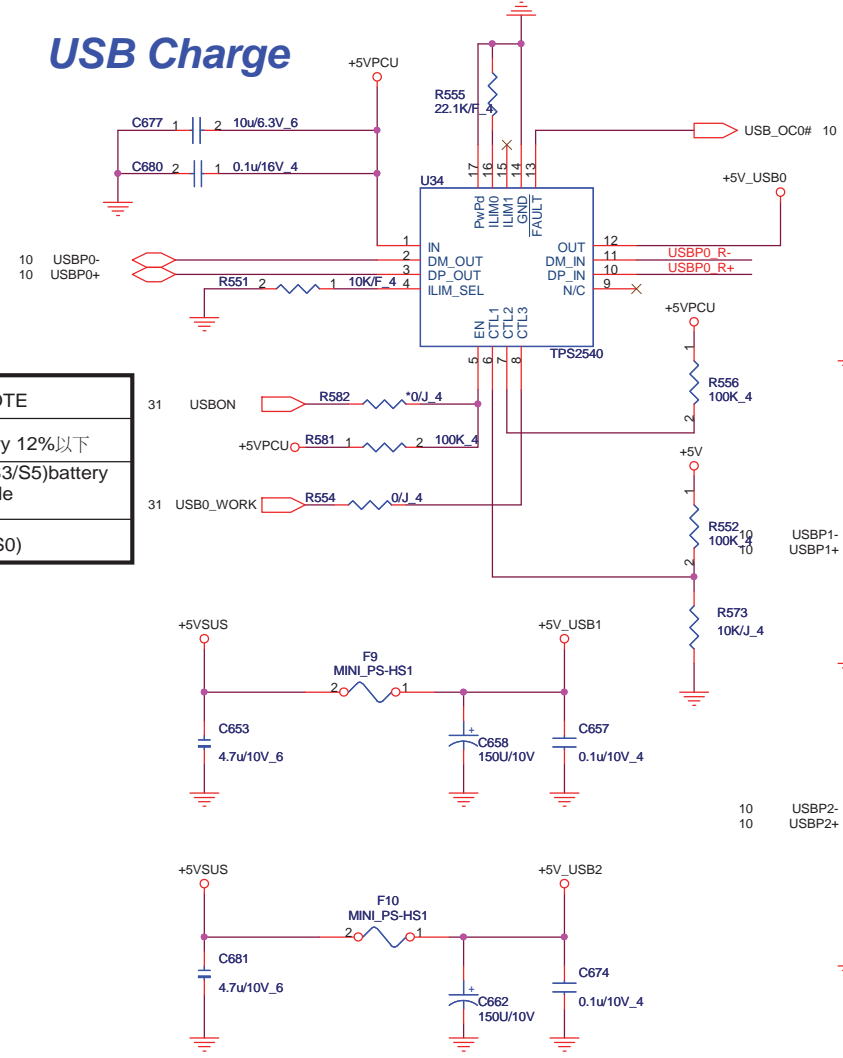




8/23 Change BT on circuit.

### USB Connector

### USB Charge



	CTL1	CTL2	CTL3	NOTE
ES(PG1.1)	0	1	0	SDP(S3/S5)battery 12%以下
	0	1	1	DCP, Auto-detect(S3/S5)battery 12%以上 or AC mode
	1	1	0	SDP(S0)

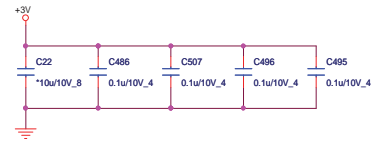
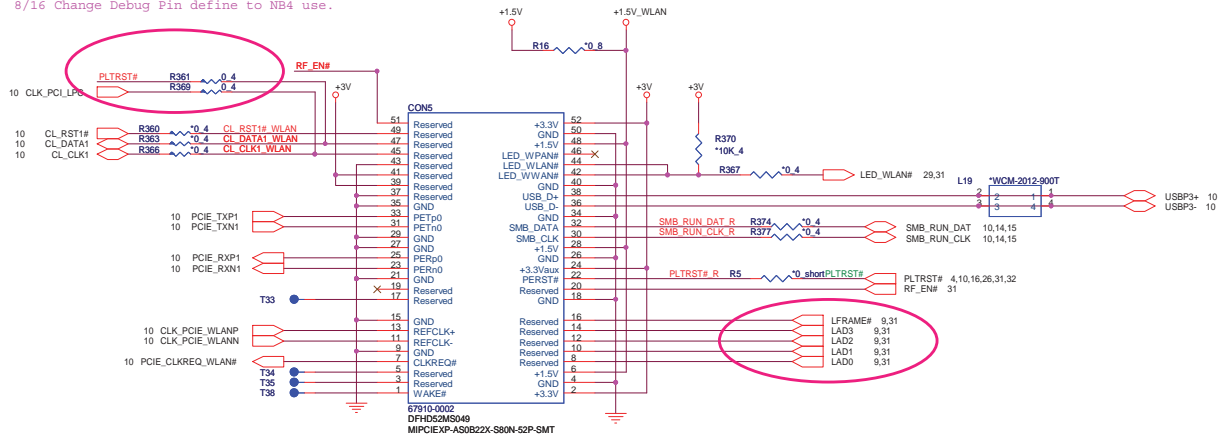
USB0_WORK	Mode
Low - S5 - 1.8A	DCP, Auto-detect
High - S0/S3 - 1.5A USB wake up with S3	CDP, BC Spec 1.1 == PCH HOST

	R321	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

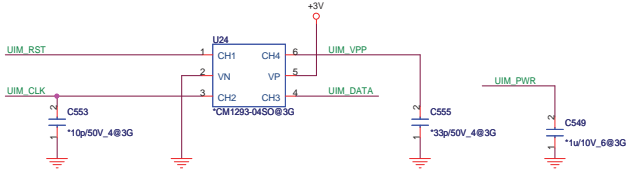
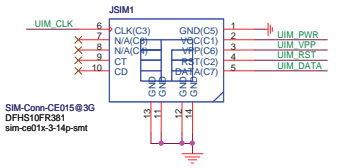
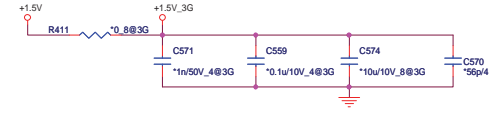
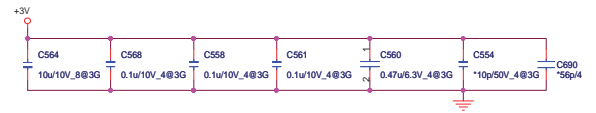
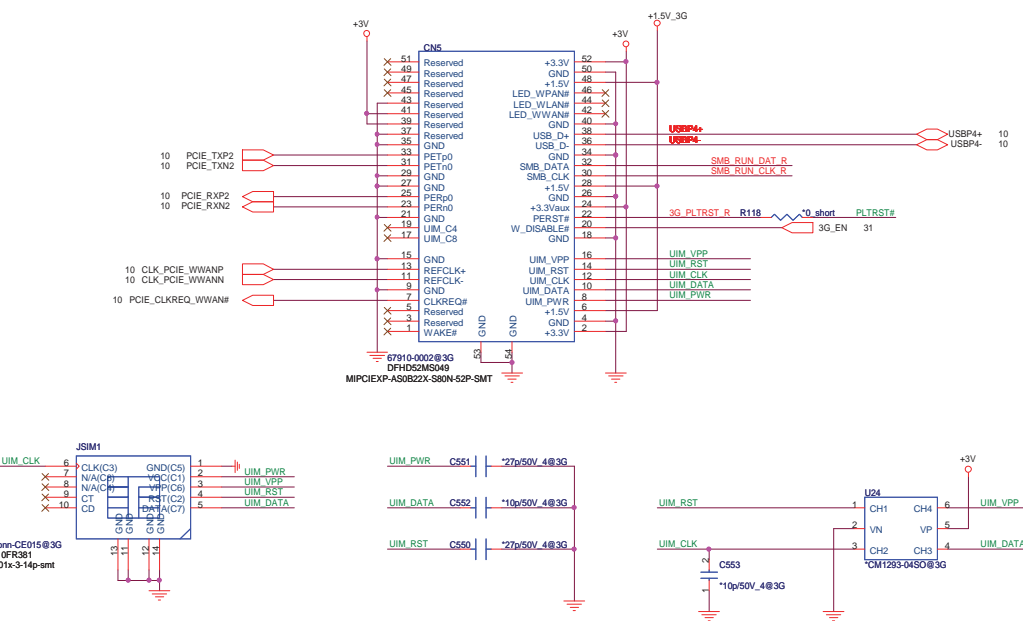
Applied Now

MINI CARD (WLAN)

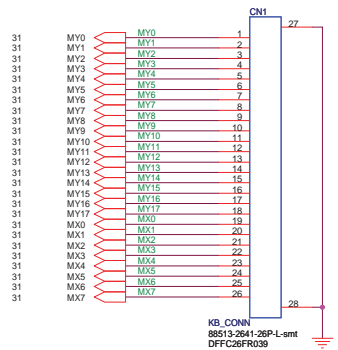
8/16 Change Debug Pin define to NB4 use.



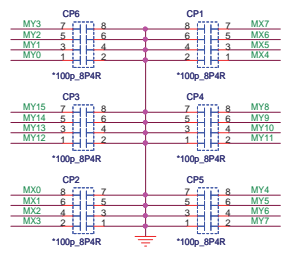
Mini Card2-3G(MNC)



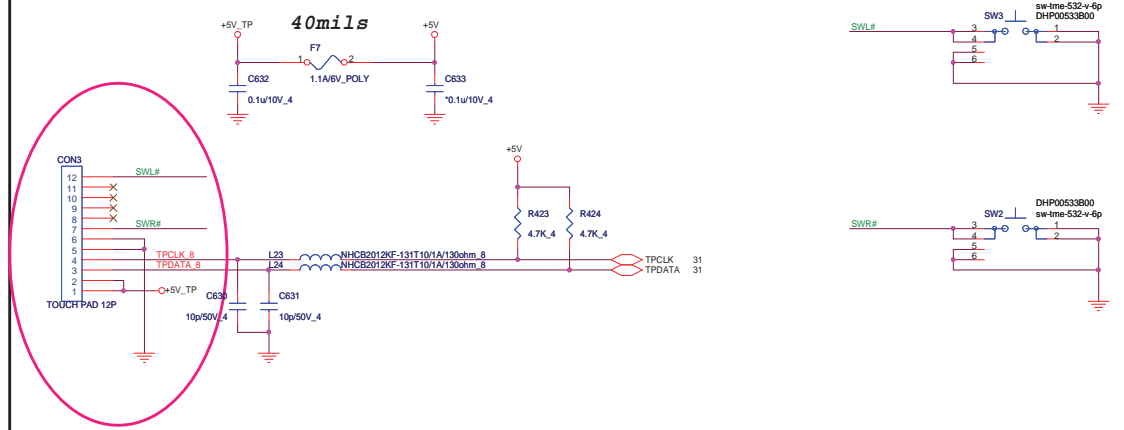
### Keyboard(KBC)



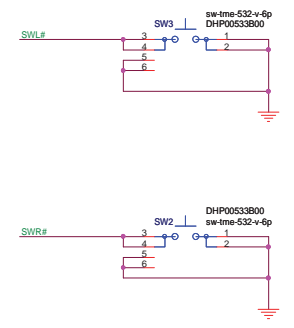
For EMI Reserve Caps for debug



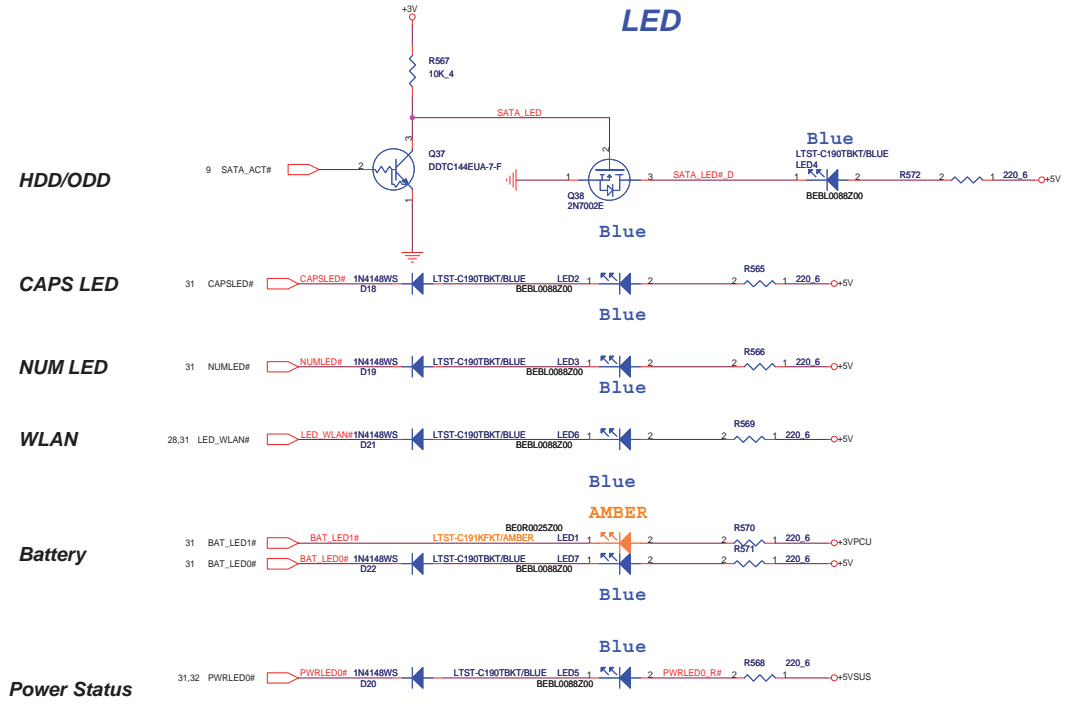
### Touch Pad



8/23 Change TP to 12 pin conn.



### LED



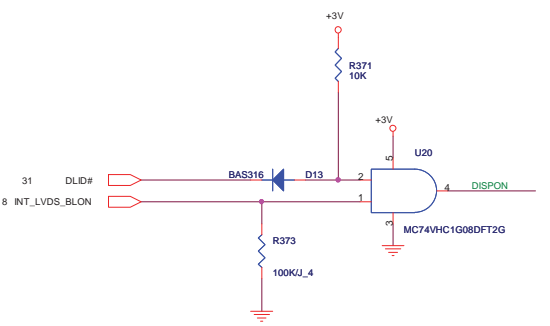




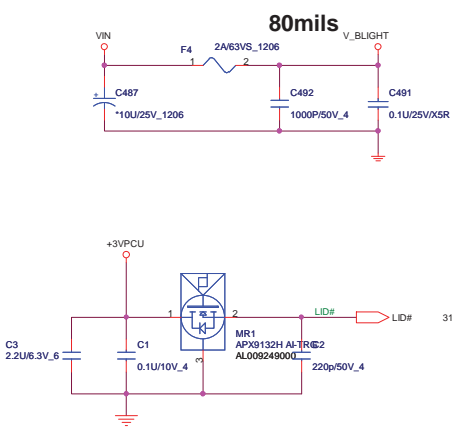




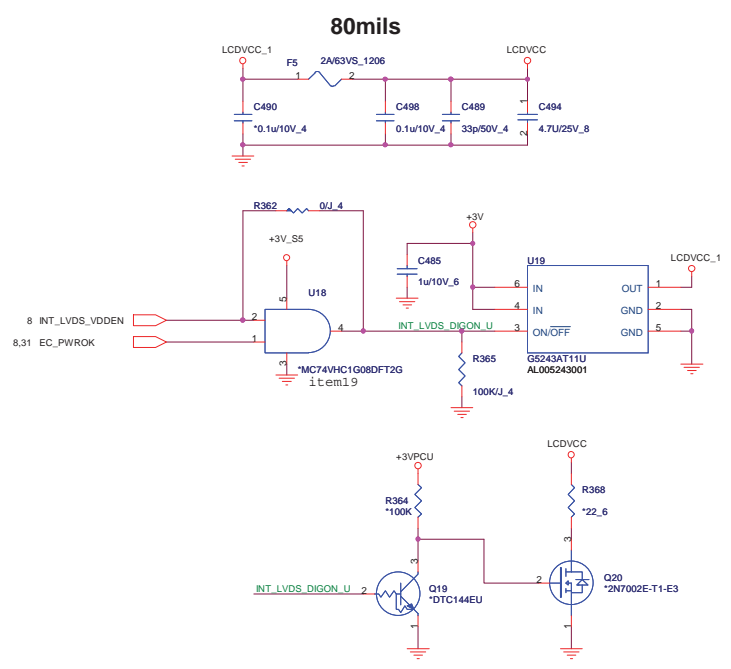
### BACKLIGHT Control(LVDS)



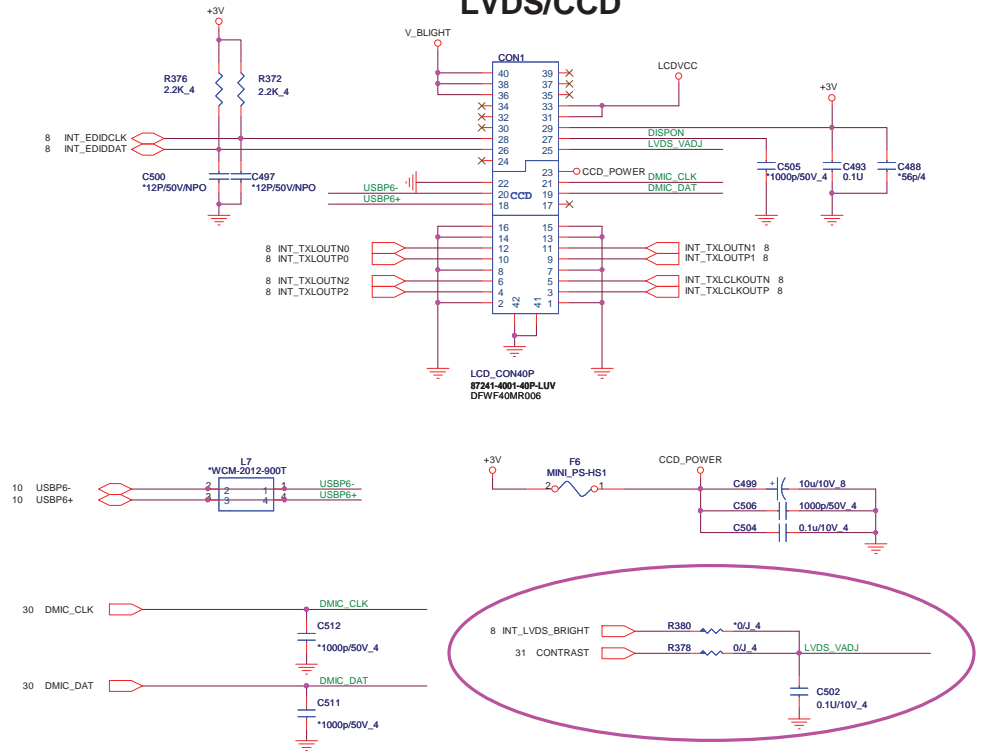
### BACKLIGHT POWER

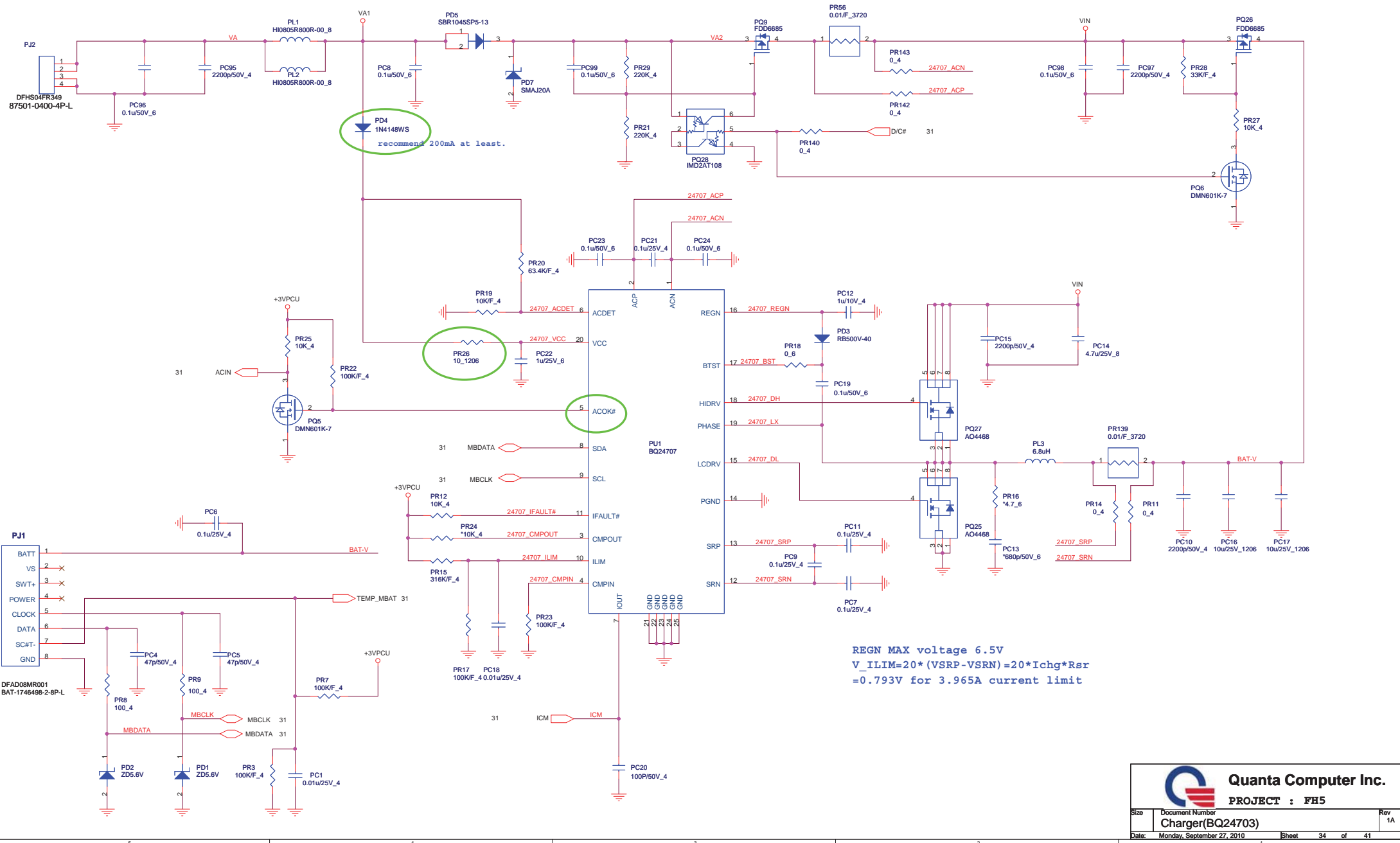


### LED Panel POWER SWITCH(LVDS)




### LVDS/CCD

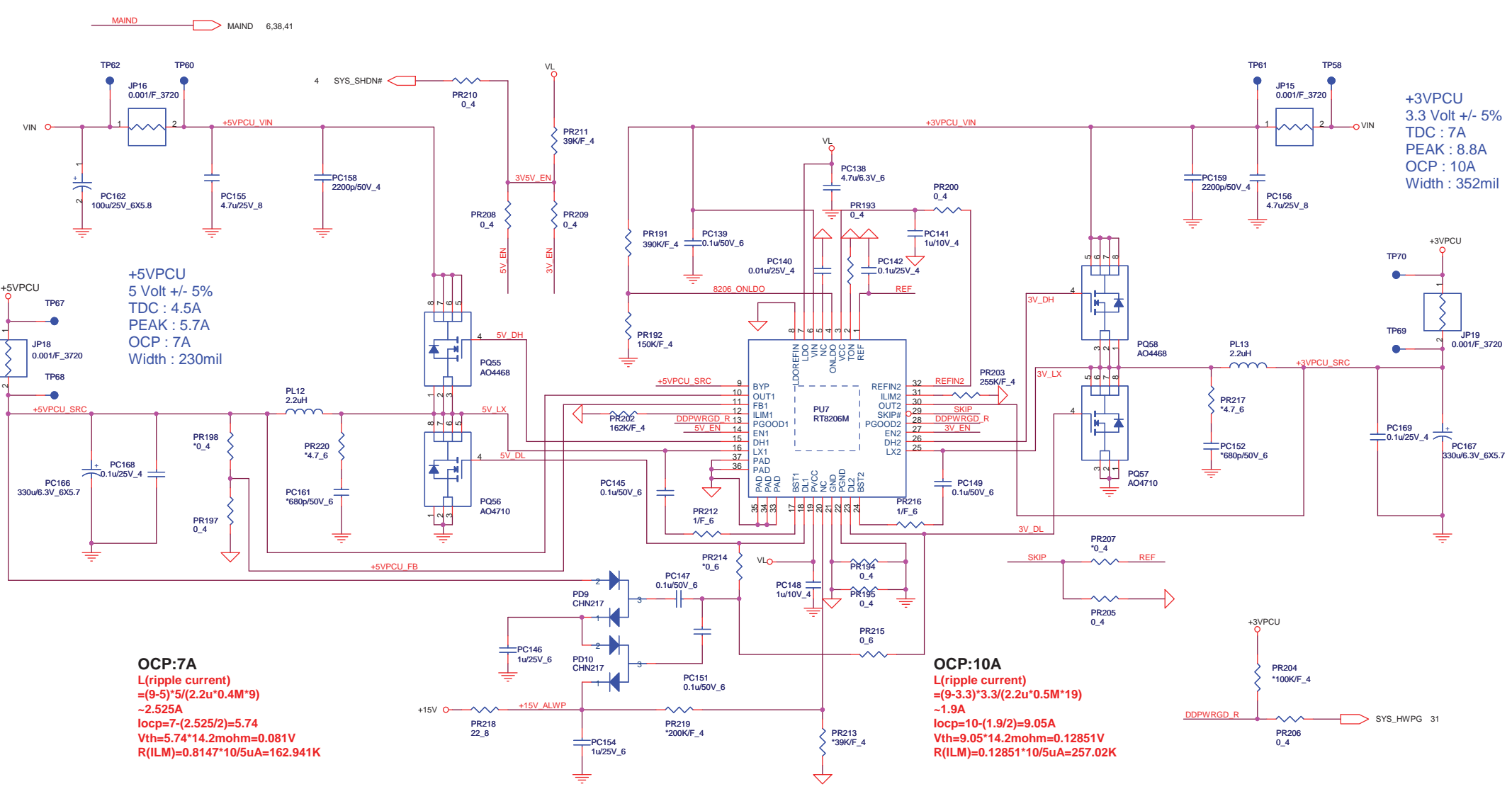




recommend 200mA at least.

REGN MAX voltage 6.5V  
 $V_{ILIM} = 20 * (V_{SRP} - V_{SRN}) = 20 * I_{chg} * R_{sr}$   
 $= 0.793V$  for 3.965A current limit

 <b>Quanta Computer Inc.</b> <b>PROJECT : FH5</b>		
Size	Document Number	Rev
	<b>Charger(BQ24703)</b>	<b>1A</b>
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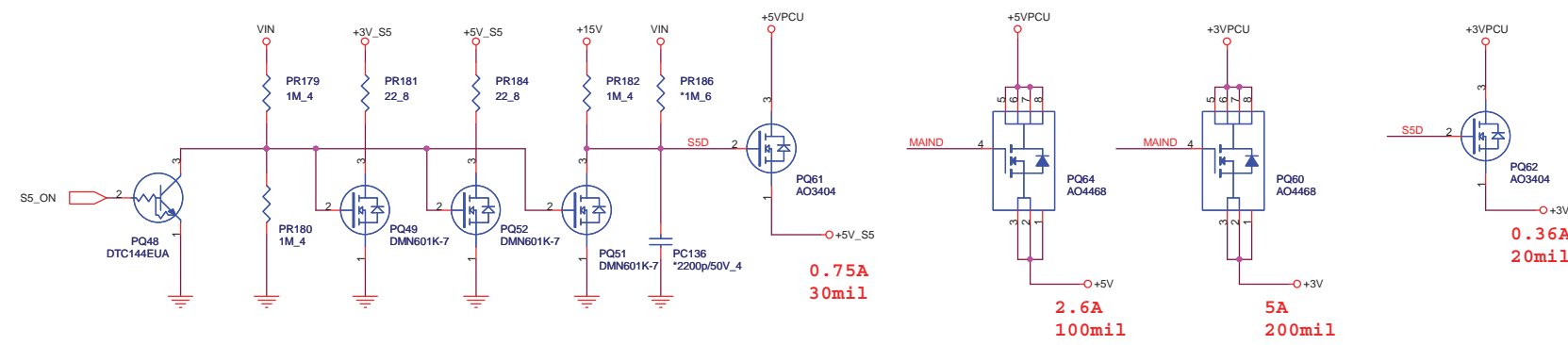


**+5VPCU**  
 5 Volt +/- 5%  
 TDC : 4.5A  
 PEAK : 5.7A  
 OCP : 7A  
 Width : 230mil

**+3VPCU**  
 3.3 Volt +/- 5%  
 TDC : 7A  
 PEAK : 8.8A  
 OCP : 10A  
 Width : 352mil

**OCP:7A**  
 $L(\text{ripple current}) = (9-5) \cdot 5 / (2.2 \mu \cdot 0.4 \text{M} \cdot 9) \approx 2.525 \text{A}$   
 $I_{\text{ocp}} = 7 - (2.525 / 2) = 5.74$   
 $V_{\text{th}} = 5.74 \cdot 14.2 \text{mohm} = 0.081 \text{V}$   
 $R(\text{ILM}) = 0.8147 \cdot 10 / 5 \mu \text{A} = 162.941 \text{K}$

**OCP:10A**  
 $L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.5 \text{M} \cdot 19) \approx 1.9 \text{A}$   
 $I_{\text{ocp}} = 10 - (1.9 / 2) = 9.05 \text{A}$   
 $V_{\text{th}} = 9.05 \cdot 14.2 \text{mohm} = 0.12851 \text{V}$   
 $R(\text{ILM}) = 0.12851 \cdot 10 / 5 \mu \text{A} = 257.02 \text{K}$



**0.75A**  
30mil

**2.6A**  
100mil

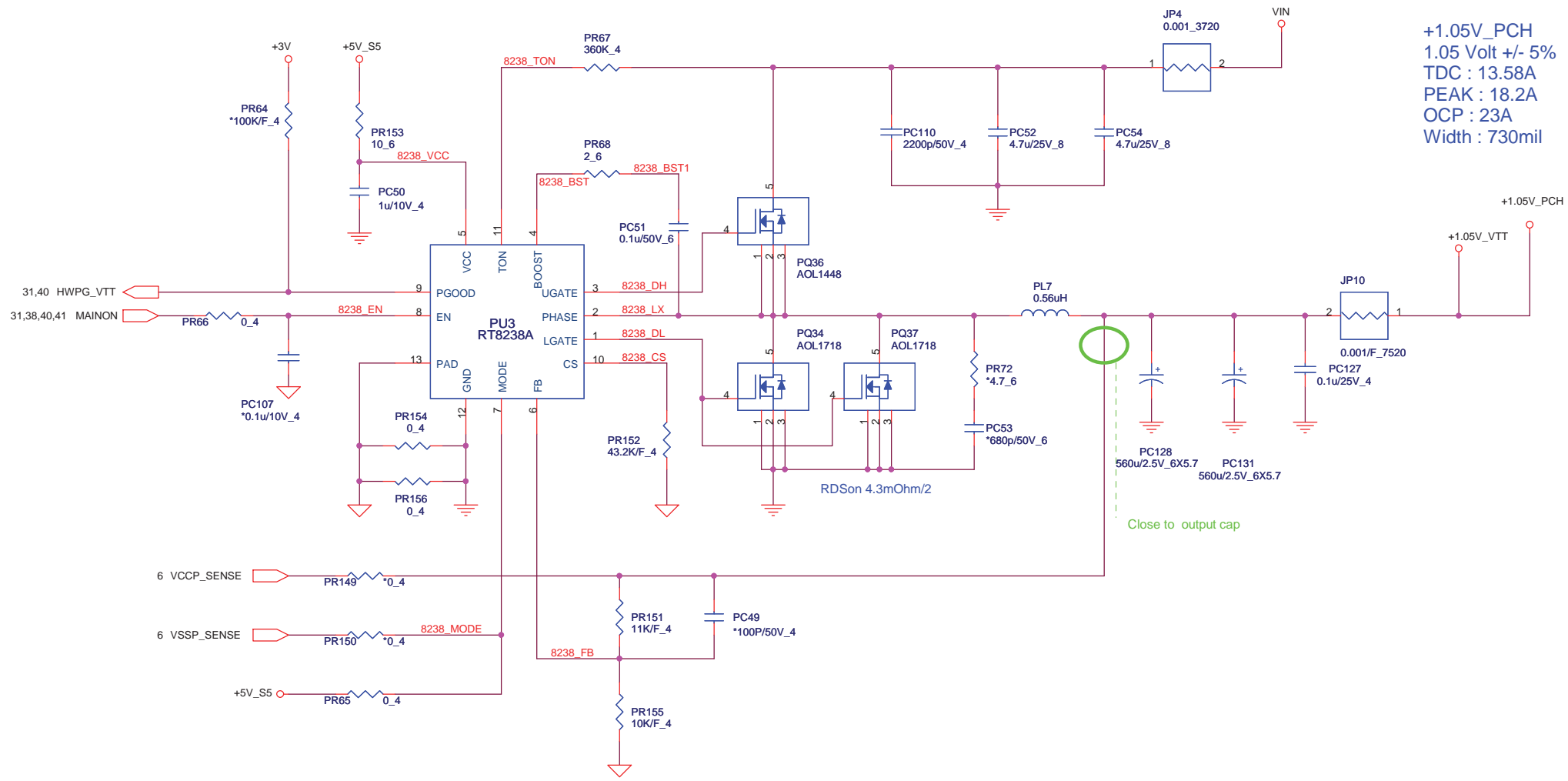
**5A**  
200mil

**0.36A**  
20mil

**Quanta Computer Inc.**  
**PROJECT : FH5**

Size	Document Number	Rev
	<b>SYSTEM 5V/3V (RT8206)</b>	1A
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+1.05V\_PCH  
 1.05 Volt +/- 5%  
 TDC : 13.58A  
 PEAK : 18.2A  
 OCP : 23A  
 Width : 730mil

Current limit = 10uA \* Rth / RDson

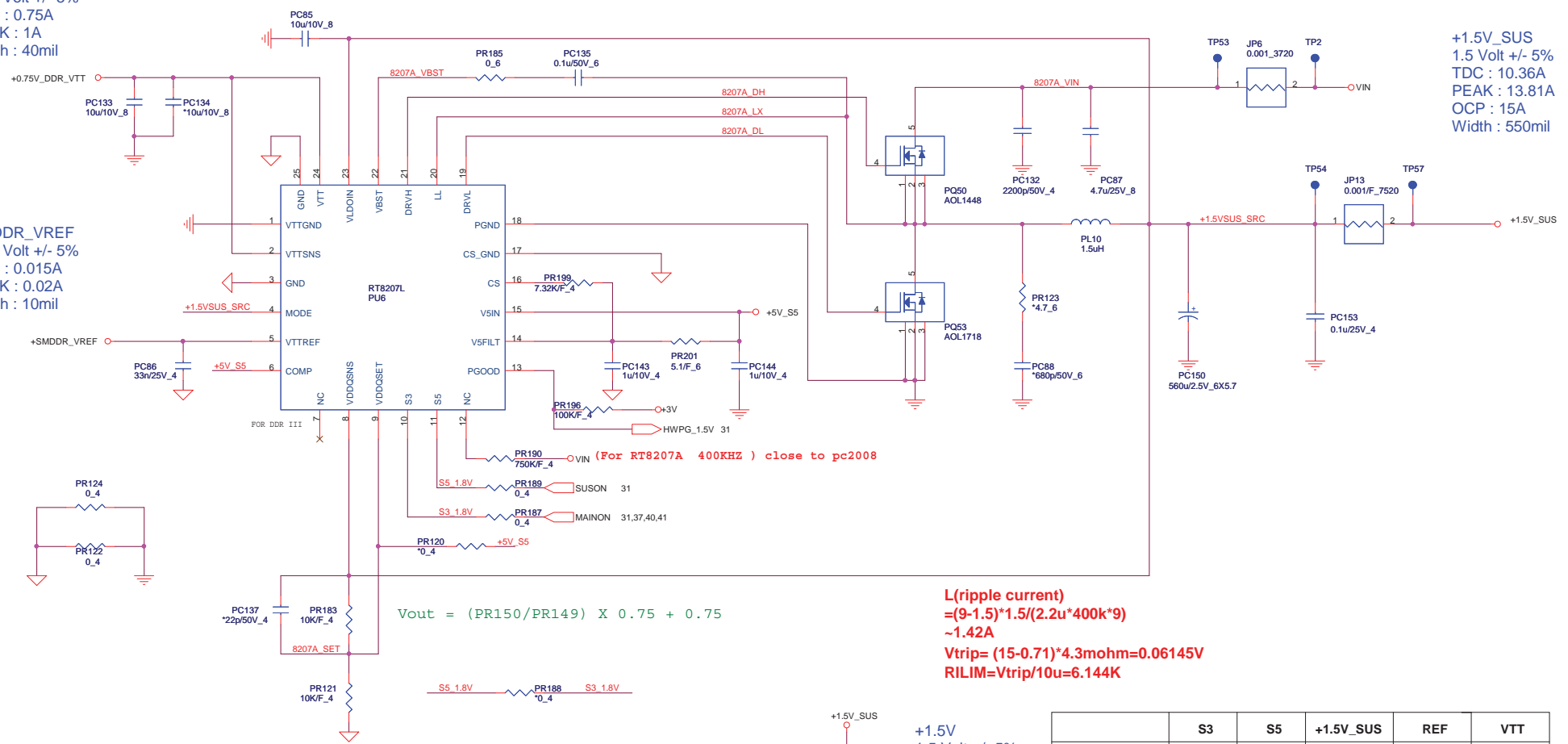
$$VOUT = (1 + R1/R2) * 0.5$$

 <b>Quanta Computer Inc.</b> PROJECT : FH5		Size	Document Number	Rev
			<b>+PCH&amp;VTT (RT8238A)</b>	1A
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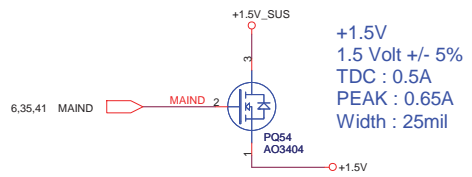
+0.75V\_DDR\_VTT  
 0.75 Volt +/- 5%  
 TDC : 0.75A  
 PEAK : 1A  
 Width : 40mil

SMDDR\_VREF  
 0.75 Volt +/- 5%  
 TDC : 0.015A  
 PEAK : 0.02A  
 Width : 10mil

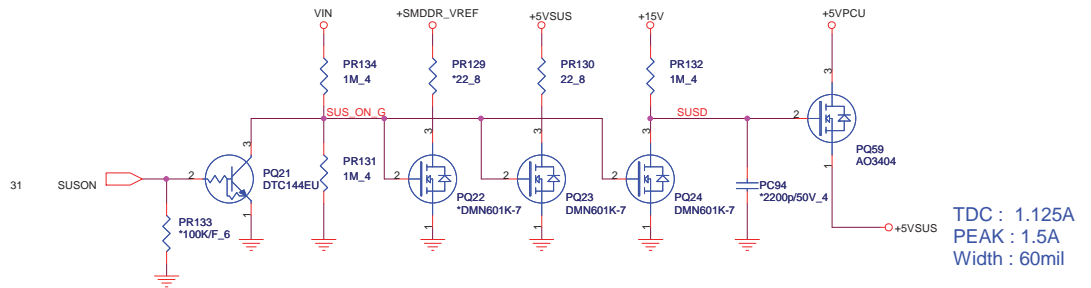
+1.5V\_SUS  
 1.5 Volt +/- 5%  
 TDC : 10.36A  
 PEAK : 13.81A  
 OCP : 15A  
 Width : 550mil



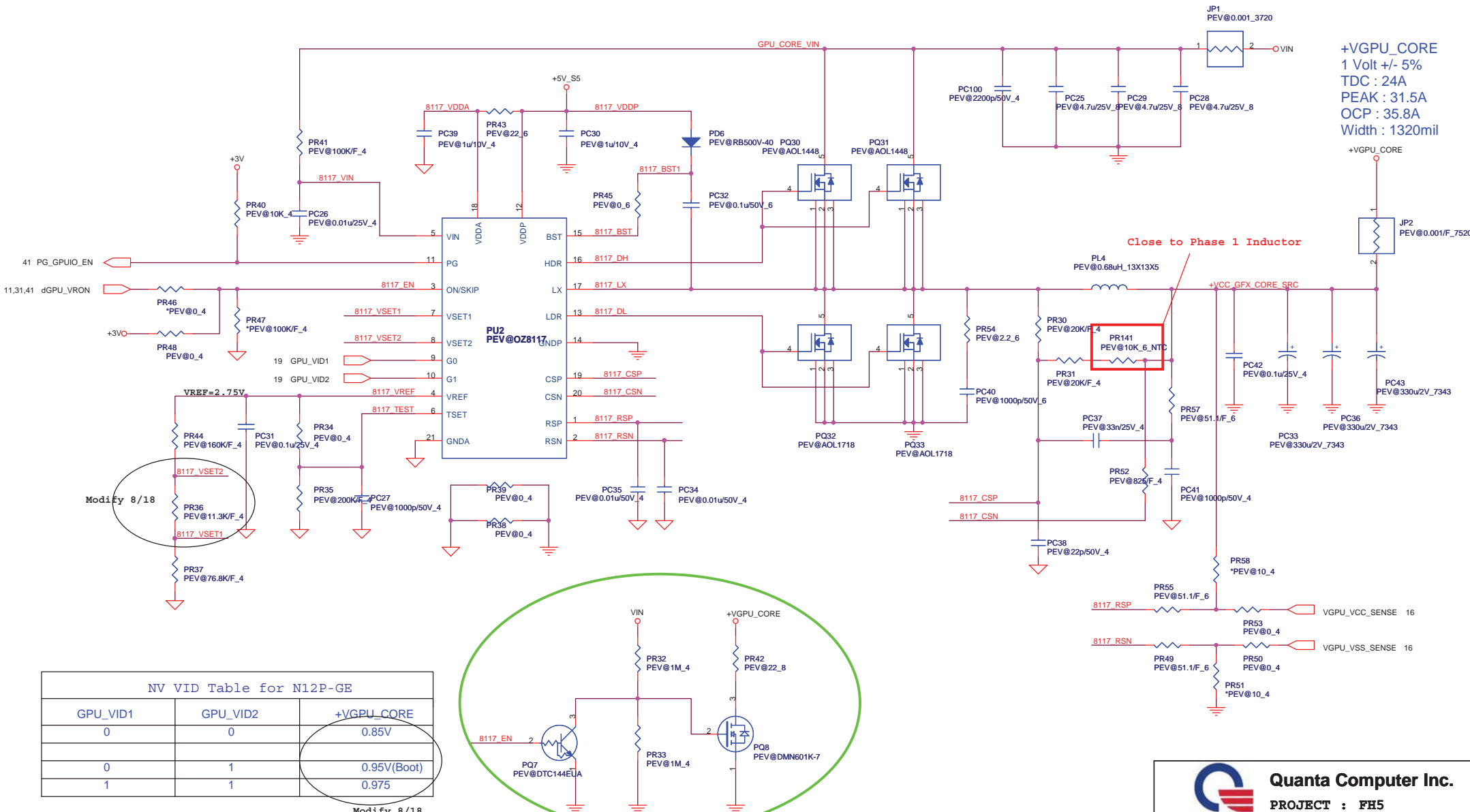
L(ripple current)  
 =(9-1.5)\*1.5/(2.2u\*400k\*9)  
 ~1.42A  
 Vtrip=(15-0.71)\*4.3mohm=0.06145V  
 RILIM=Vtrip/10u=6.144K



	S3	S5	+1.5V_SUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF







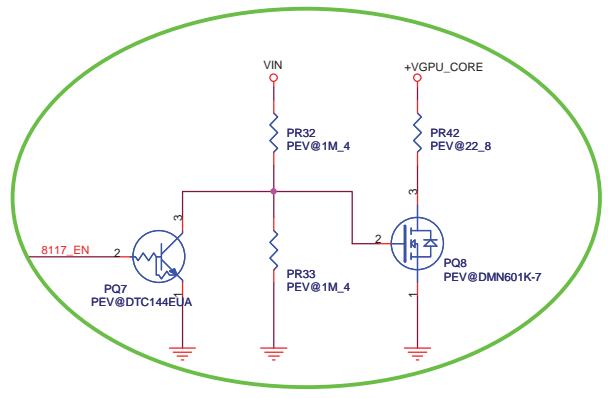
+VGPU\_CORE  
 1 Volt +/- 5%  
 TDC : 24A  
 PEAK : 31.5A  
 OCP : 35.8A  
 Width : 1320mil


Close to Phase 1 Inductor

Modify 8/18

GPU VID1	GPU VID2	+VGPU_CORE
0	0	0.85V
0	1	0.95V(Boot)
1	1	0.975

Modify 8/18

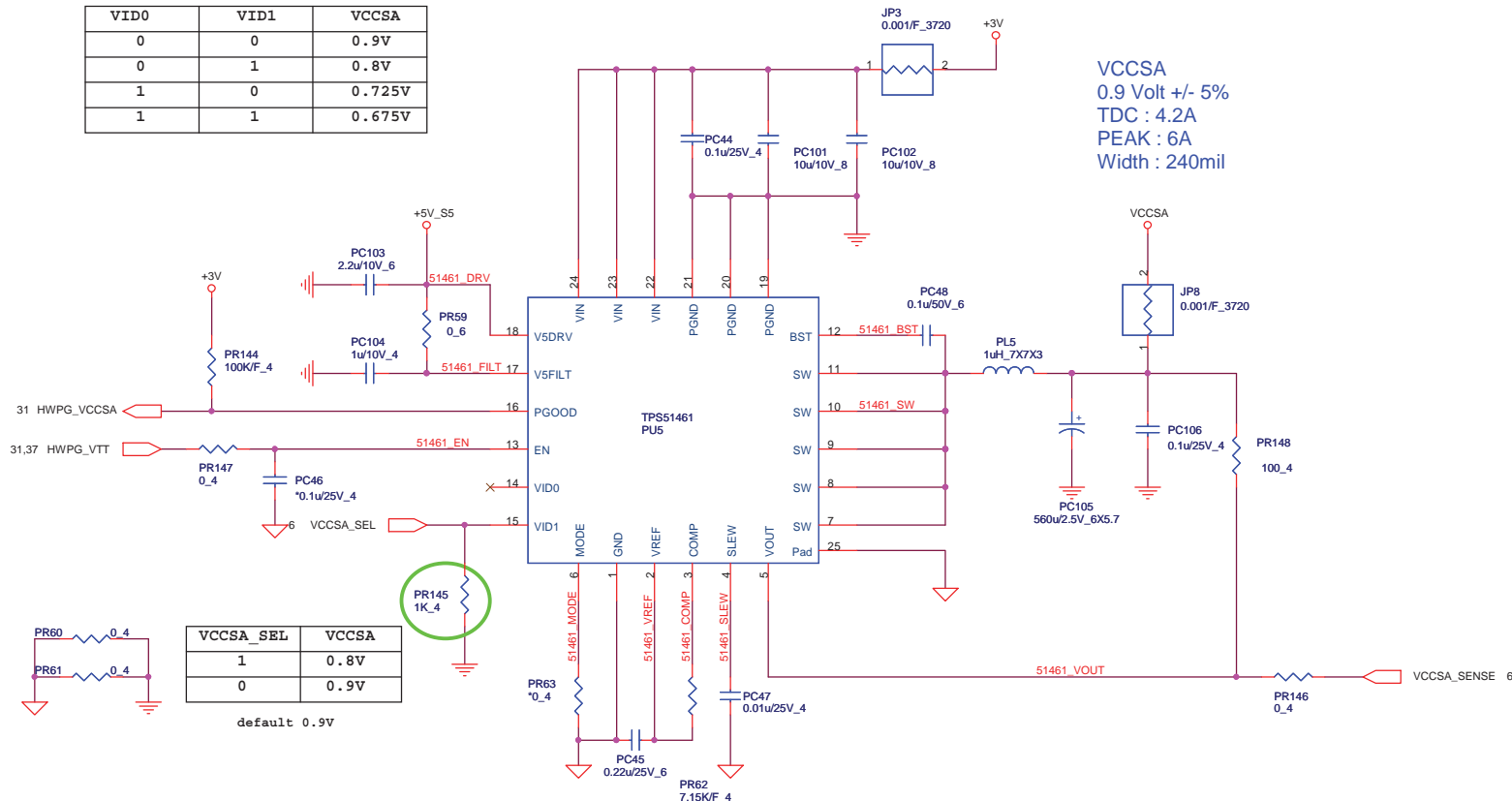




**Quanta Computer Inc.**  
 PROJECT : FH5

Size	Document Number	Rev
	<b>GPU CORE(OZ8117)</b>	1A
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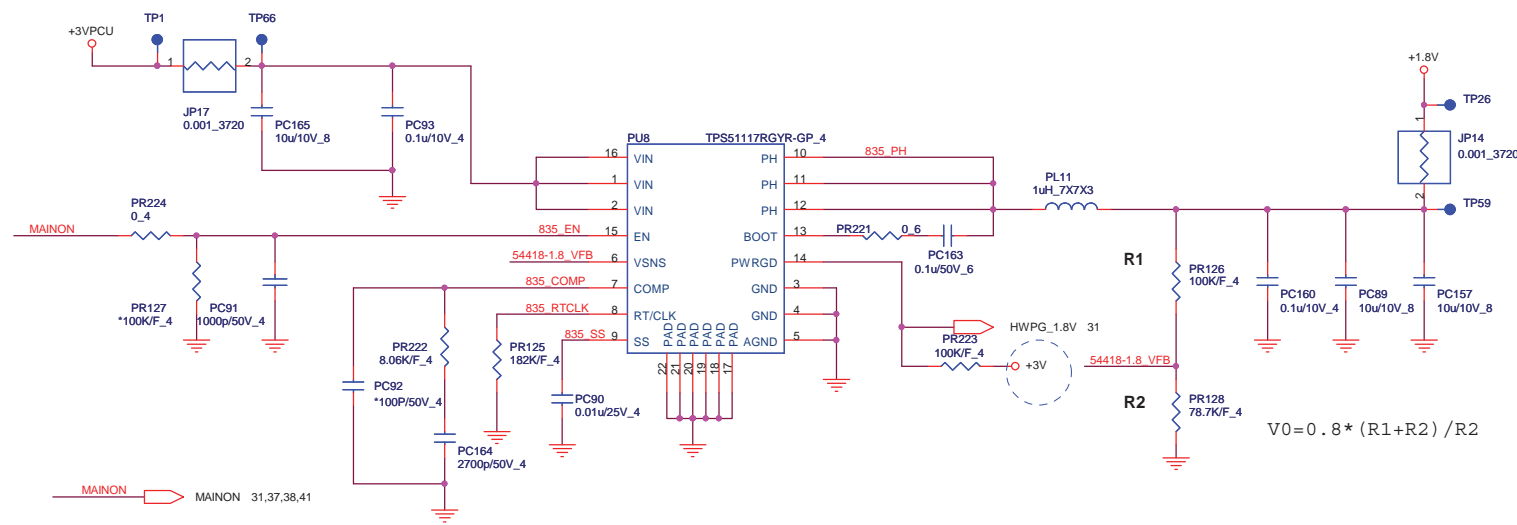
VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



VCCSA  
0.9 Volt +/- 5%  
TDC : 4.2A  
PEAK : 6A  
Width : 240mil

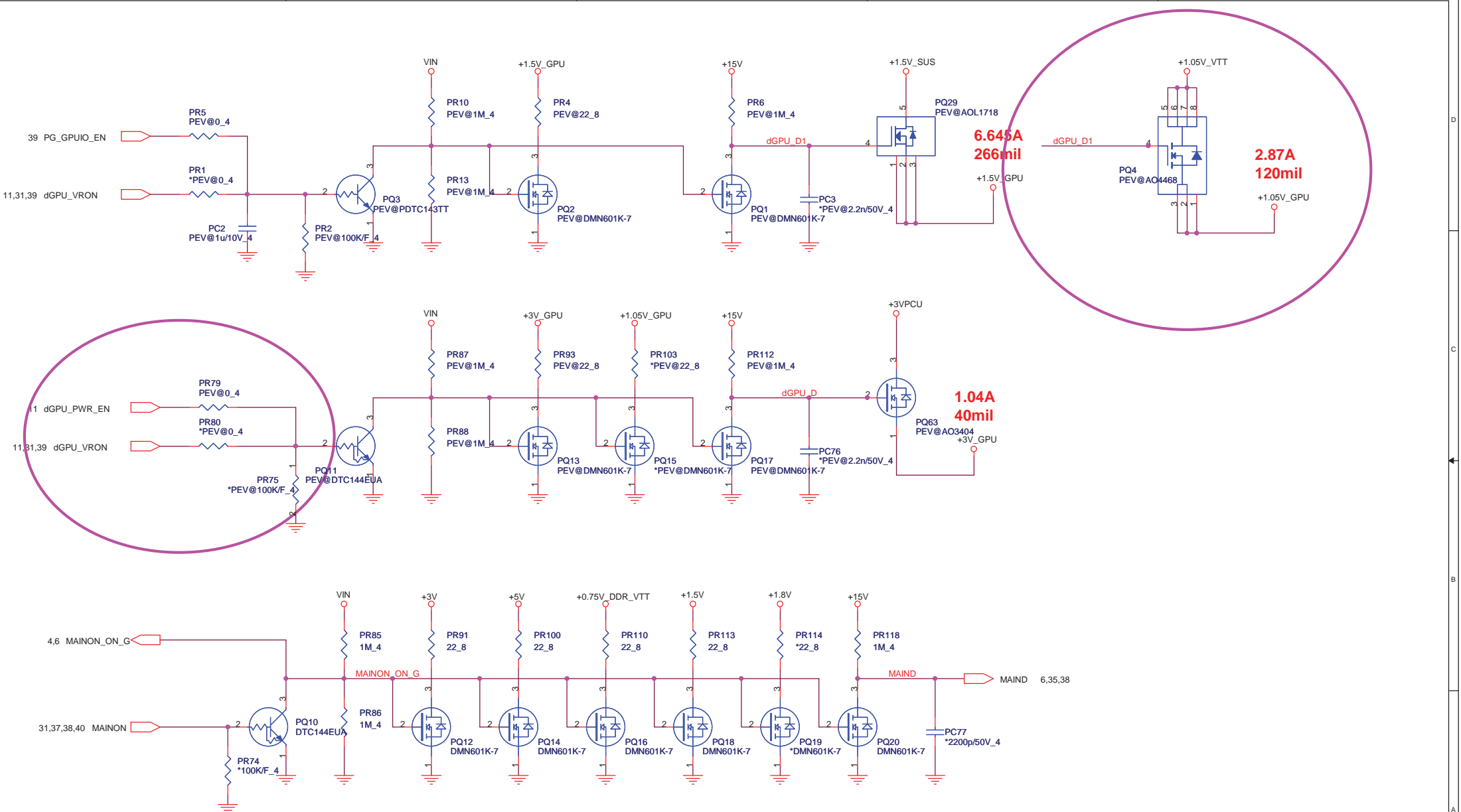
VCCSA_SEL	VCCSA
1	0.8V
0	0.9V


default 0.9V



+1.8V  
1.8 Volt +/- 5%  
TDC : 1.34A  
PEAK : 1.78A  
Width : 71mil

$$V0 = 0.8 * (R1 + R2) / R2$$





**Quanta Computer Inc.**  
PROJECT : FH5

Size	Document Number	Rev
	Discharger	1A
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Model

FH5 MB

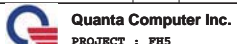
REV

CHANGE LIST

B

2010/09/20	<p>page 33: Change +VIN to VIN.</p> <p>page 30 : Del Q16 ,R351.</p> <p>page 10 : Add Q27 and Q28.</p> <p>page 26 : Change CON6 RJ45 Conn to DFTJ08FR157.</p>
2010/09/22	<p>page 10: Change USB port6 ot port10.</p>
2010/09/22	<p>page 31 : Del CN3 Netname ,NBSWON#, SLP_S3# ,+VCC_GFX,+VCC_CORE,H_PWRGOOD, RSMRST#, SLP_S4# ,SUS_STATE#.</p> <p>page 31 : Reserve R351 ,R574-R580 for Power sequence resistor.</p> <p>page 31 : Reserve C692 for H_PWRGOOD.</p> <p>page 9: Change JTAG VCC +3VPCU to +3V_S5.</p>
2010/09/23	<p>page 31 : Change CON2 VCC from +3V to +3V_S5.</p> <p>page 12 : Reserve C693,C694,C695,C696 for BSD.</p> <p>Page36 : PC61 - PC63 change value from *1000p/50V_4 (CH21006JB10) to *0.1u/50V_6 (CH41006K911)</p> <p>Page36 : PC62 - PC112 - PC116 - PC119 change value from 1000p/50V_4 (CH21006JB10) to 0.1u/50V_6 (CH41006K911)</p> <p>Page36 : PC72 change value from *PIV01000p/50V_4 (CH21006JB10) to * PIV00.1u/50V_6 (CH41006K911)</p> <p>Page36 : PC74 - PC122 - PC125 change value from PIV01000p/50V_4 (CH21006JB10) to PIV00.1u/50V_6 (CH41006K911)</p> <p>Page38 : PR190 changes value from 620K/F_4 (CS46202FB00) to 750K/F_4 (CS47502FB14)</p> <p>Page39 : PR44 changes value from PEV0169K/F_4 (CS41692FB12) to PEV0160K/F_4 (CS41602FB00)</p> <p>Page39 : PR36 changes value from PEV021.5K/F_4 (CS32152FB17) to PEV011.3K/F_4 (CS31132FB07)</p> <p>Page39 : PR37 changes value from PEV082K/F_4 (CS38202FB14) to PEV076.8K/F_4 (CS37682FB00)</p> <p>page36 :PL6 - PL8 - PL9 change footprint from CHOKE-BTQP4LR36WFC-4P-SMT to CHOKE-PCMB104T-R45MN-4P-SMT</p> <p>page06 Reserve C697,C698,C699 for VID.</p>
2010/09/24	<p>page06 Del R28 , add R21,C19,C20,Y2 , use crystal to provide 25M CLK.</p> <p>page36 Del PC57,PC58 ,ADD PC170,171,PC78,PC73,PC55 for C state issue.</p> <p>page38 Change PR199 to 7.32K_4(CS27322FB12), change 1.5V_SUS OCP value.</p>
2010/09/27	<p>Page39 : PL4 change P/B from CV+68*0M200 to DC+68Z0M001</p> <p>Page24 : C4,C5,C6,C7,C8,C9 change from2.2P/50V_4 to 10P/50V_4(CH01006JB08).</p> <p>page 27 : Change U34 Ctrl1 1 -&gt;3 behavior,add R554 , R581,del R582.</p>

3C



DOC NO.	PROJECT MODEL : FH5	APPROVED BY:	DATE: 2010/09/20
Change list	PART NUMBER:	DRAWING BY:	REVISION: 1A