

SUZHOU-D

CPU : AMD Caspin
Chip Set : AMD RX881+SB710
Remarks : Tigris Platform

Model Name : Suzhou-D
PBA Name : MAIN
PCB Code : GCE :
NAN :
HAN :
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.11.10

Design	CHECK	APPROVAL
XIE BIN	GUO LEI	BC LEE

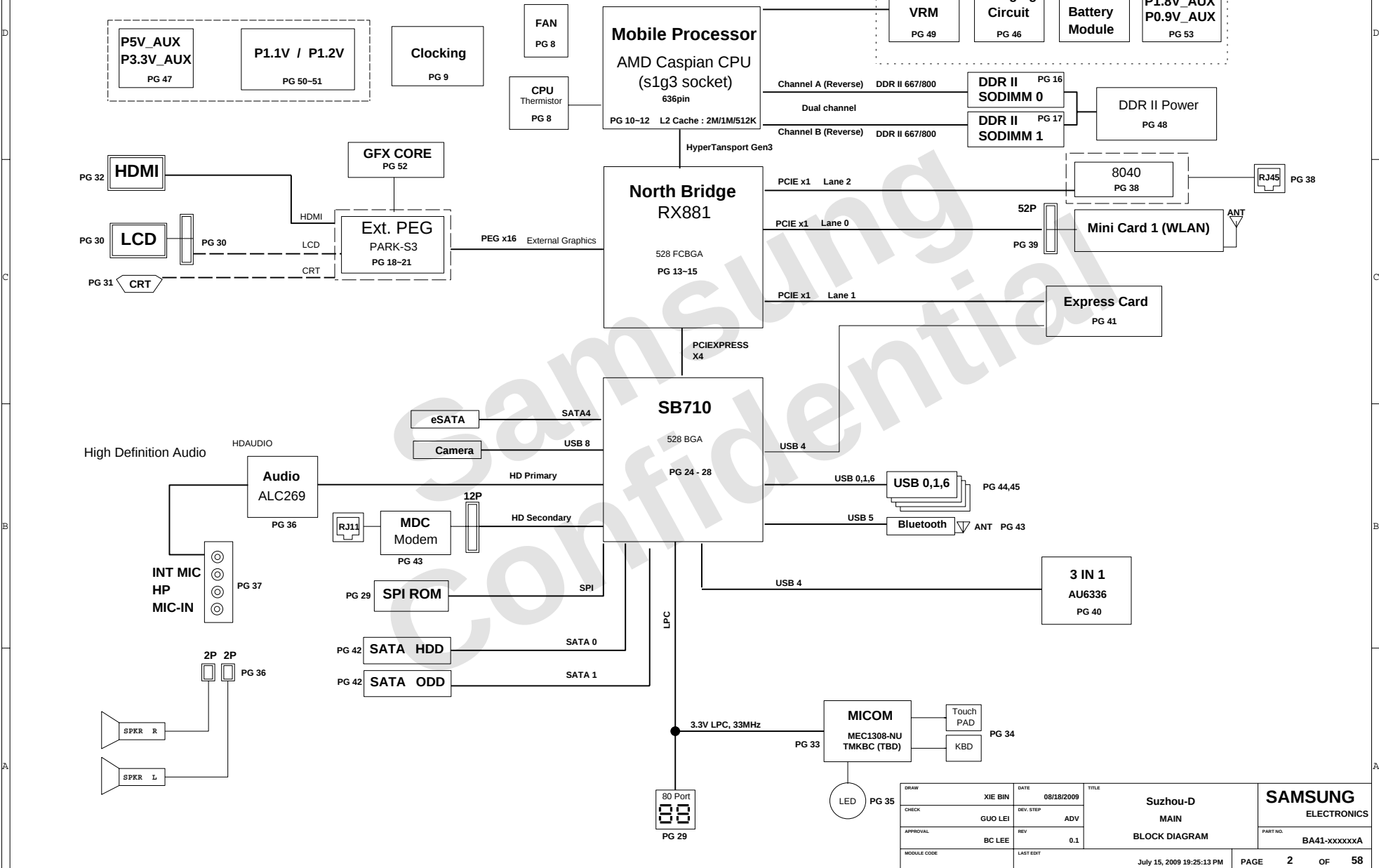
Owner : SEC Mobile R & D Signature : X

Table of Contents

Page. 1	----	COVER
Page. 2	----	OPERATION BLOCK DIAGRAM
Page. 3	----	BOARD INFORMATION
Page. 4	----	POWER DIAGRAM
Page. 5	----	POWE RAILS ANALYSIS
Page. 6	----	TIMING DIAGRAM, POWER ON
Page. 7	----	CLOCK DISTRIBUTION
Page. 8	----	THERMAL SENSOR&FAN CONTROL
Page. 9	----	CLOCK GEN.
Page. 10~12	----	S1g3 CPU
Page. 13~15	----	RX881M
Page. 16~17	----	SODIMM DDR2
Page. 18~22	----	SB710
Page. 23	----	SPI BIOS ROM
Page. 24~27	----	PARK-S3
Page. 28~29	----	gDDR3
Page. 30	----	LVDS (LCD CONNECTOR)
Page. 31	----	CRT CONNECTOR
Page. 32	----	HDMI CONNECTOR
Page. 33	----	MICOM
Page. 34	----	KBD CONN & TOUCHPAD
Page. 35	----	LED LOGIC
Page. 36~37	----	AUDIO
Page. 38	----	LOM(Marvell 88E8040)
Page. 39	----	WLAN
Page. 40	----	MEMORY CARD (AU6336)
Page. 41	----	EXPRESS CARD
Page. 42	----	HDD & ODD
Page. 43	----	MDC CONN. & BLUETOOTH
Page. 44	----	USB CONNECTOR
Page. 45	----	SUB BOARD_POWER SWITCH
Page. 46	----	CHARGER
Page. 47	----	P3.3V_AUX & P5.0V_AUX & P12V_ALW
Page. 48	----	DDR2 POWER & P0.9V_AUX
Page. 49	----	CPU VRM
Page. 50~51	----	CHIPSET POWER(P1.1V & P1.2V)
Page. 52	----	GFX POWER
Page. 53	----	gDDR3 POWER & P1.0V
Page. 54	----	SWITCHED POWER (P5.0V & P3.3V & P 2.5V & P1.8V & P1.2V_AUX)
Page. 55	----	POWER DISCHARGER
Page. 56	----	MOUNT HOLE
Page. 57	----	TEST POINT

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	MAIN		ELECTRONICS
APPROVAL	BC LEE	REV	0.1	COVER		PART NO. BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	1	OF 58

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE0	Core Voltage for CPU
CPU_CORE1	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.1V	VTT for M92,RX881
P1.2V	Core Voltage for SB710
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V_AUX	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_STB	5.0V always power rail
P12.0V_ALW	12.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB710	Real Time Clock
Crystal	10MHz	MICOM	MECL308-NU
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	88E8040
Crystal	25MHz	SATA	SB710

I²C / SMB Address

Devices	Address	Hex	Bus
SB710	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	NC
3	NC
4	3 IN 1
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	EXPRESS CARD

PCI Express Assign

PORT #	ASSIGNED TO
0	Mini Card (WLAN)
1	EXPRESS CARD
2	LOM
3	NC
4	NC
5	NC

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0(strap0)
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REVISION HISTORY

See rev notes for more information.

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	MAIN	MAIN	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	BOARD INFORMATION	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	3	OF 58

POWER DIAGRAM

Rev 0.1

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AC Adapter

Battery DC

VDC

P3.3V_MICOM

MICOM LED SB710

P5.0V_STB

USB N Charger

P12.0V_ALW

KBC3_SUSPWR
(CHP3_S4_STATE*)

P1.8V_AUX

AMD S1G3
SODIMM (DDR II)

P5V_AUX

USB connector

P0.9V_AUX

DDR II-Termination

P1.2V_AUX

SB710

P3.3V_AUX

SB710
EXPRESS CARD
WLAN
LAN
MDC
THERMAL
LVDS
LED

P1.2V_LAN

LAN

KBC3_PWRON
(CHP3_SLPS3*)

P1.8V

RX881
PARK
gDDR-3 for PARK
eSATA Reapter
AU6336

P5.0V

THERMAL CRT HDMI
SB710 MICOM AUDIO
ODD HDD CAMERA
TOUCH PAD

EGFX_CORE

PARK

P1.0V

PARK

P1.5V

CK505
WLAN
EXPRESS CARD

P2.5V

S1G3

P3.3V

CK505 THERMAL RX881
DDR2 PARK CRT
LVDS HDMI SB710
SPI WLAN LEDS
LAN AUDIO EXPRESS CARD
HDD BT AU6336

KBC3_VRON

CPU_CORE0,1

S1G3

P1.2V

S1G3
RX881
SB710

P1.1V

RX881
PARK

Power On/Off Table by S-state

Rail \ State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V_AUX	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

S5-S4

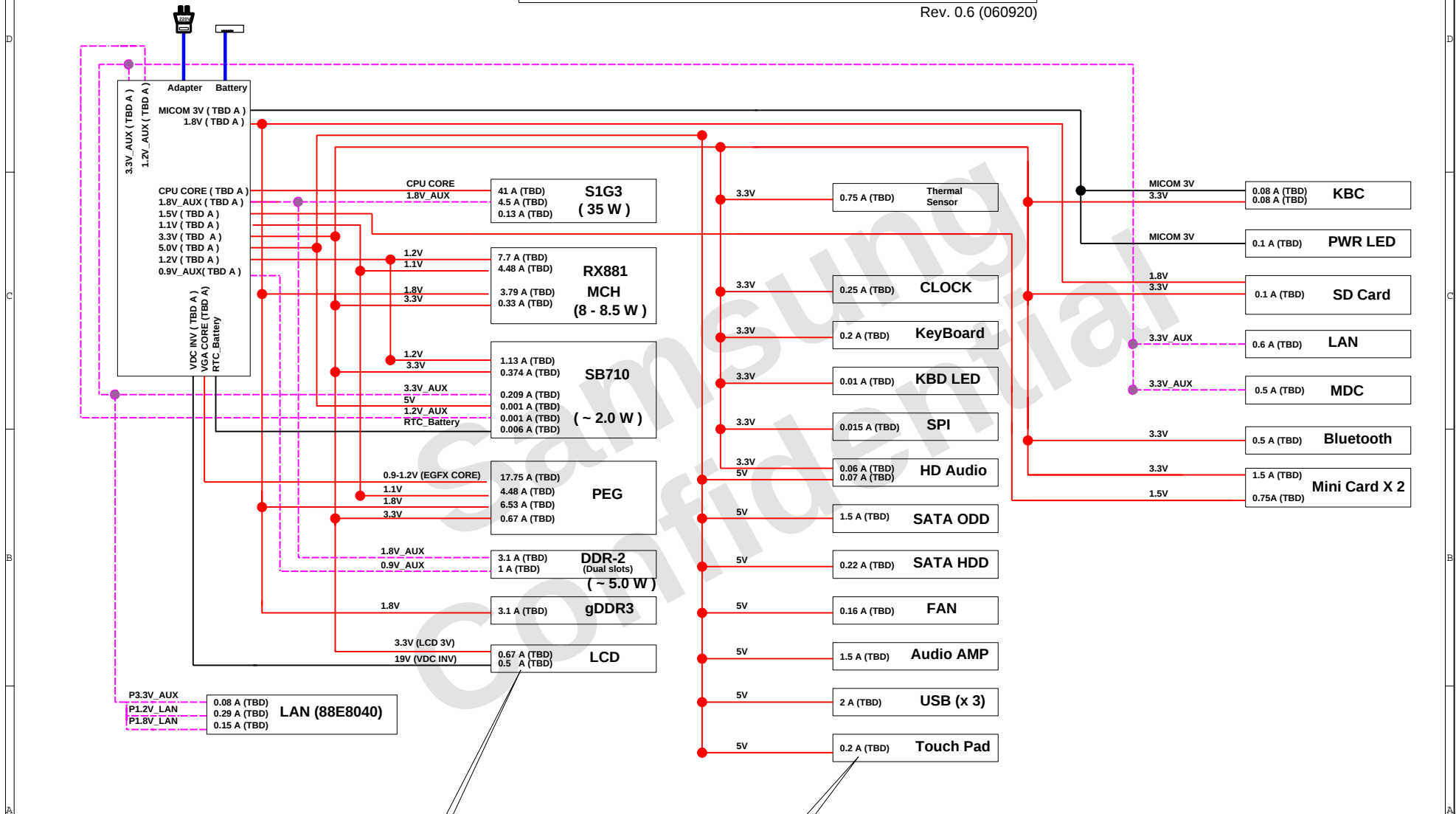
S3

S0

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D MAIN	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
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APPROVAL	BC LEE	REV	0.1			
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	4 OF 58	

POWER RAILS ANALYSIS

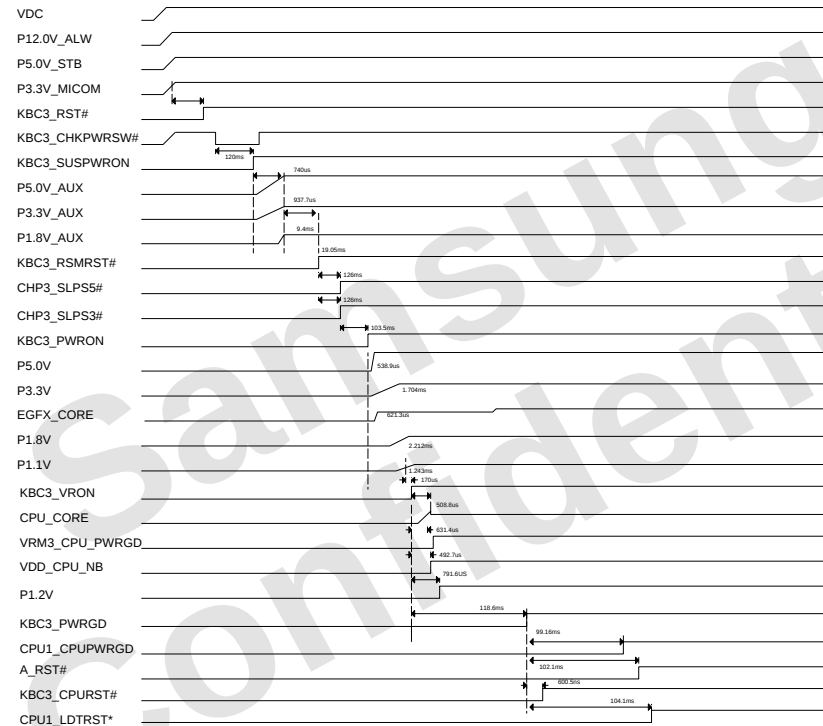
Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

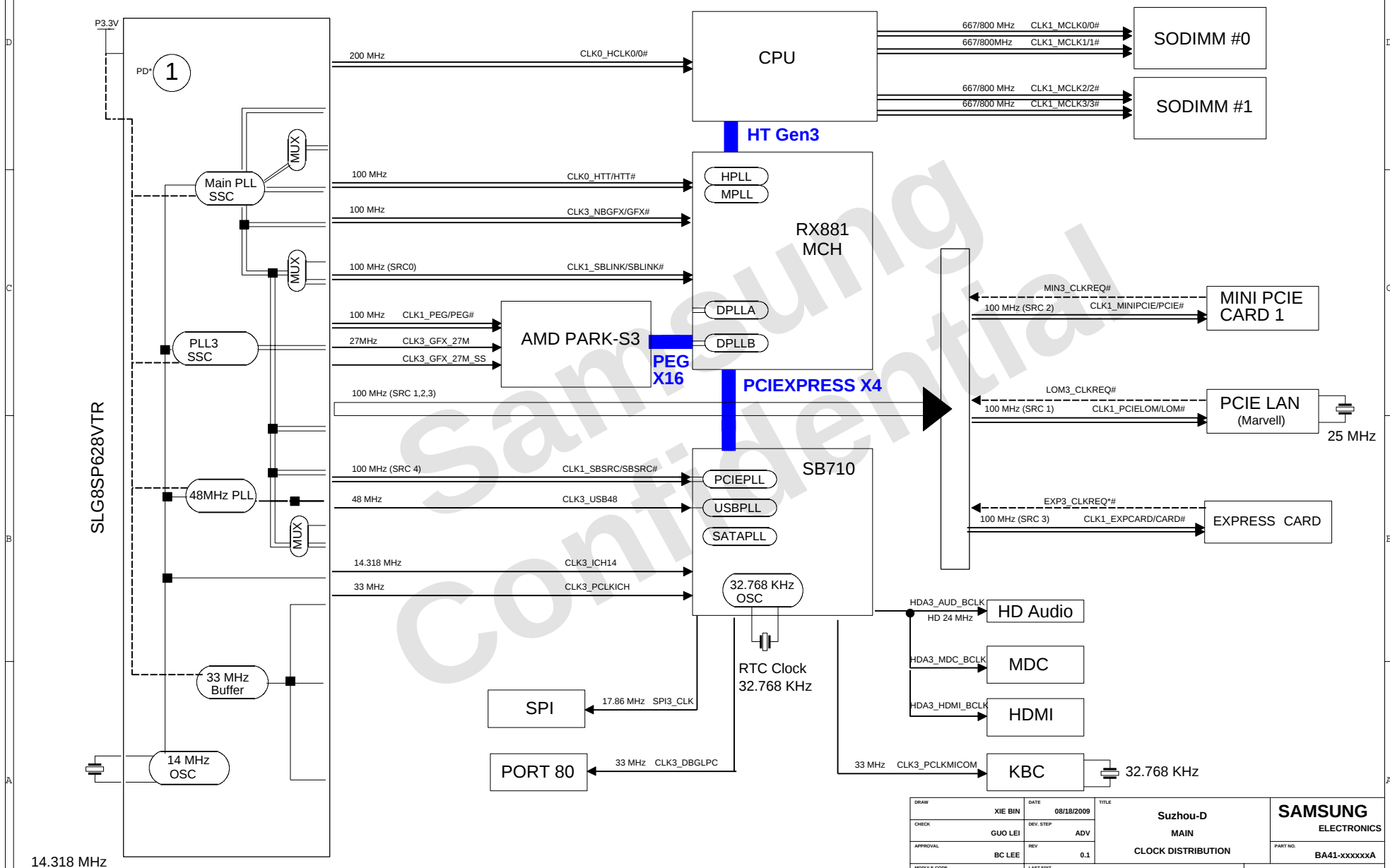
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APPROVAL	BC LEE	REV	0.1	POWER RAILS ANALYSIS	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT				
				July 15, 2009 19:25:13 PM	PAGE	5 OF 58

Timing Diagram, Power ON Rev..1.0 2009-08-27



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CHECK	GUO LEI	DEV. STEP	ADV	MAIN		ELECTRONICS
APPROVAL	BC LEE	REV	0.1	TIMING DIAGRAM	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	6	OF 58

CLOCK DISTRIBUTION



14.318 MHz

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	MAIN	MAIN	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	CLOCK DISTRIBUTION	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	7 OF 58

The schematic diagram illustrates the internal circuitry of the EMC2112-BP-TR module. Key components and connections include:

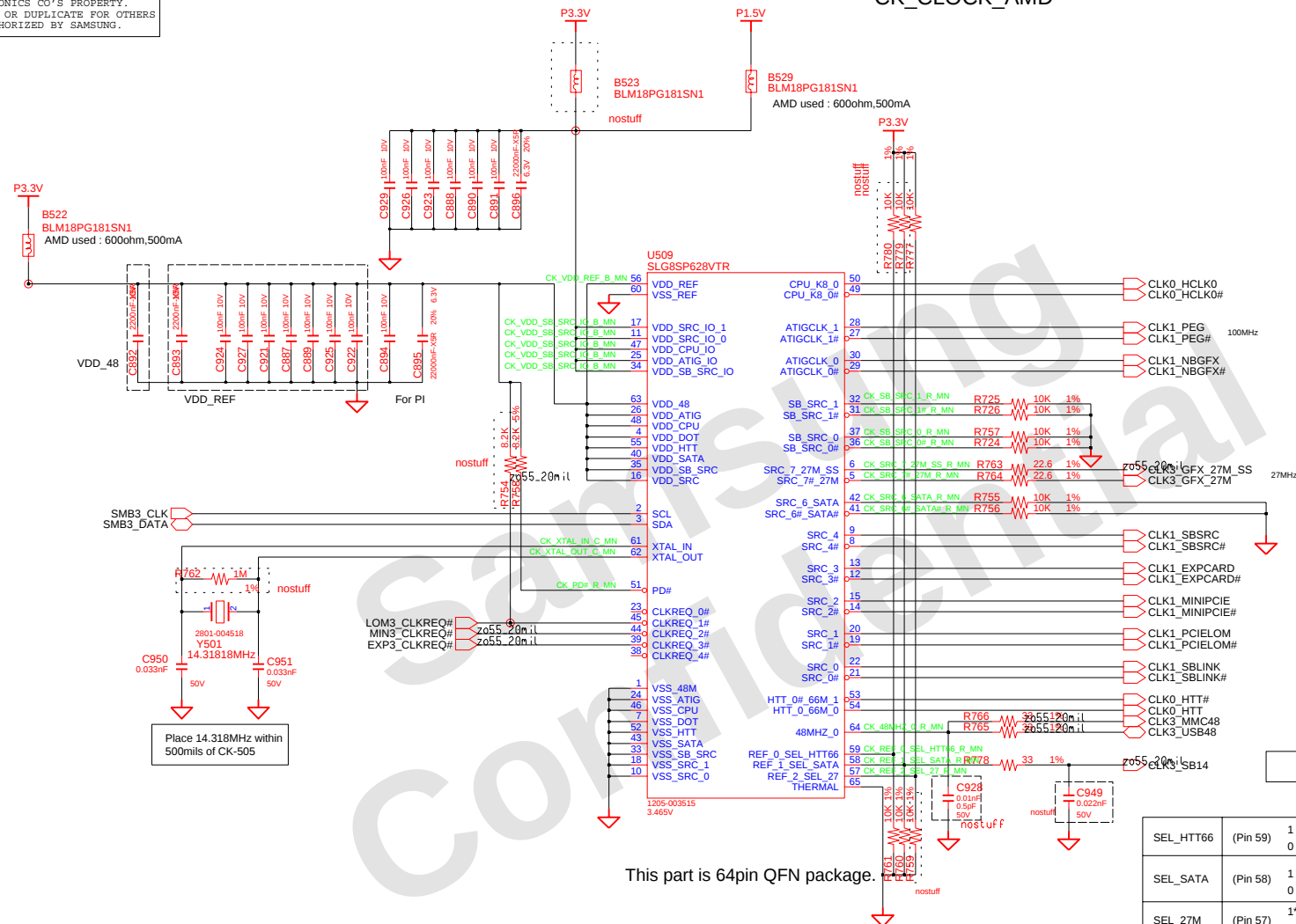
- Power Supply:** P5.0V, P3.3V_AUX, P3.3V, and P1.8V rails are shown with associated decoupling capacitors (C86, C94, C88, C92, C1512, C1513, C71, C72, C85).
- Resistors:** Various resistors (R76, R78, R68, R67, R65, R66, R72, R43) are used for signal conditioning and pull-up/pull-down.
- Sensor Chip:** U5: EMC2112-BP-TR is the central component, with pins for VDD, VDD_5V, VDD_5V_2, RESET#, ADDR_SEL, SHDN_SEL, TRIP_SET, CLK, GND, and THERMAL_PAD.
- Temperature Sensing:** The THERMAL_PAD pin is connected to a 95 degree C sensor. The module also includes a temperature sensor (CHP3_THRMTRIP#) and a fan speed sensor (FAN5_VDD, FAN3_FDBACK#).
- Signal Processing:** The module outputs signals for THM3_ALERT#, THM3_STP#, CPU2_THERMDC, CPU2_THERMDA, and GFX3_THERMDN/GFX3_THERMDP.
- Connectors:** J2: HDR-4P-1R-SMD is used for fan speed sensing, and J1: 4P-1R-SMD is used for temperature sensing.

SHDN_SEL MODE	
0	CH1(CPU MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

Line Width = 20 mil

DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D THERMAL SENSOR EMC2112	SAMSUNG ELECTRONICS
CHECK	GUO LEI	REV. STEP	ADV		
APPROVAL	BC LEE	REV	0.1		
MODULE CODE	LAST EDIT				
July 15, 2009 19:25:13 PM					PAGE 8 OF 58

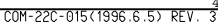
CK_CLOCK_AMD



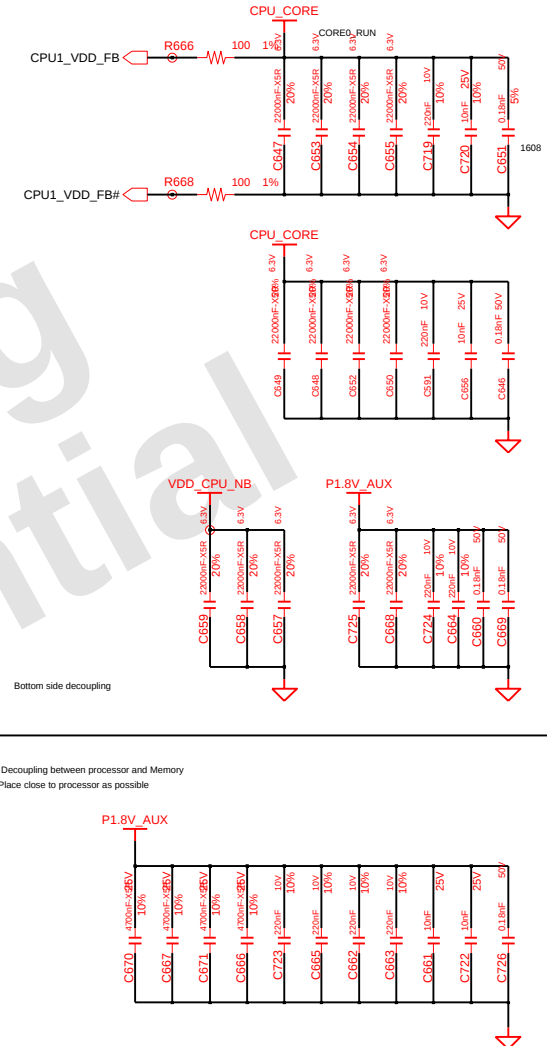
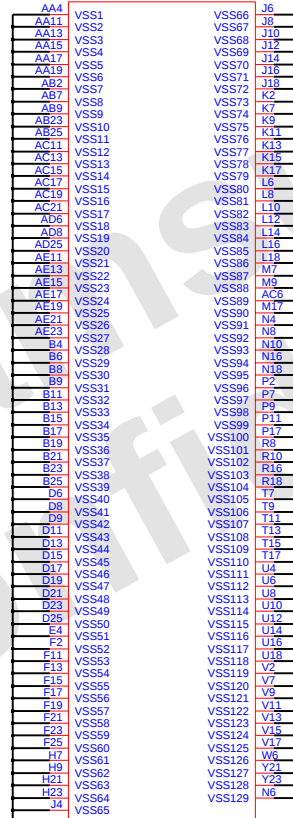
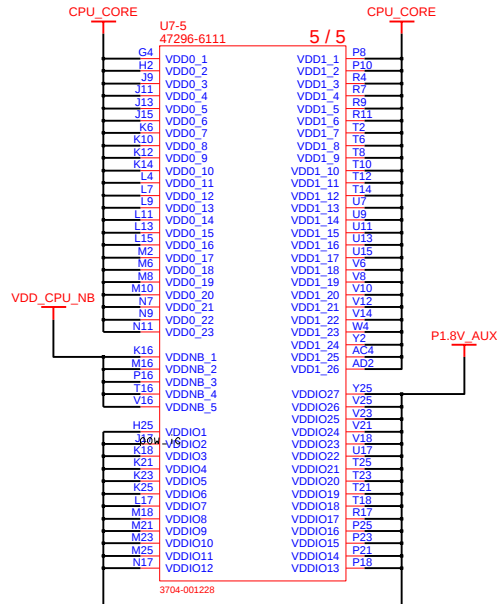
CLK REQ	DEVICE	SRC PORT
CLK REQ 0	-	SB Link
CLK REQ 1	LOM3_CLKREQ#	LOM
CLK REQ 2	MIN3_CLKREQ#	MINI CARD
CLK REQ 3	EXP3_CLKREQ#	EXP CARD
CLK REQ 4	-	SB_SRC

SEL_HTT66	(Pin 59)	1 0 *	66MHz 3.3V single HTT clock 100MHz differential clock
SEL_SATA	(Pin 58)	1 0 *	SRC6 diff. clock 100MHz spreading diff. clock
SEL_27M	(Pin 57)	1 ⁺ 0	27MHz/27MHz_SS graphics clock SRC7 diff. clock

DRAW	XIE BIN	DATE	08/18/2009	TITLE Suzhou-D Main_Clock_Circuit CK for AMD CPU	SAMSUNG ELECTRONICS	
CHECK	GUO LEI	REV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1			
MODULE CODE	LAST EDIT					

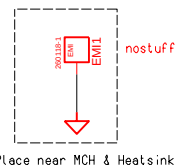
D:/Users/mentor/Suzhou-D/Suzhou-D adv1 0826

CPU_Caspian



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	Caspian CPU	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	S1G3 CPU (3/3)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	12 OF 58

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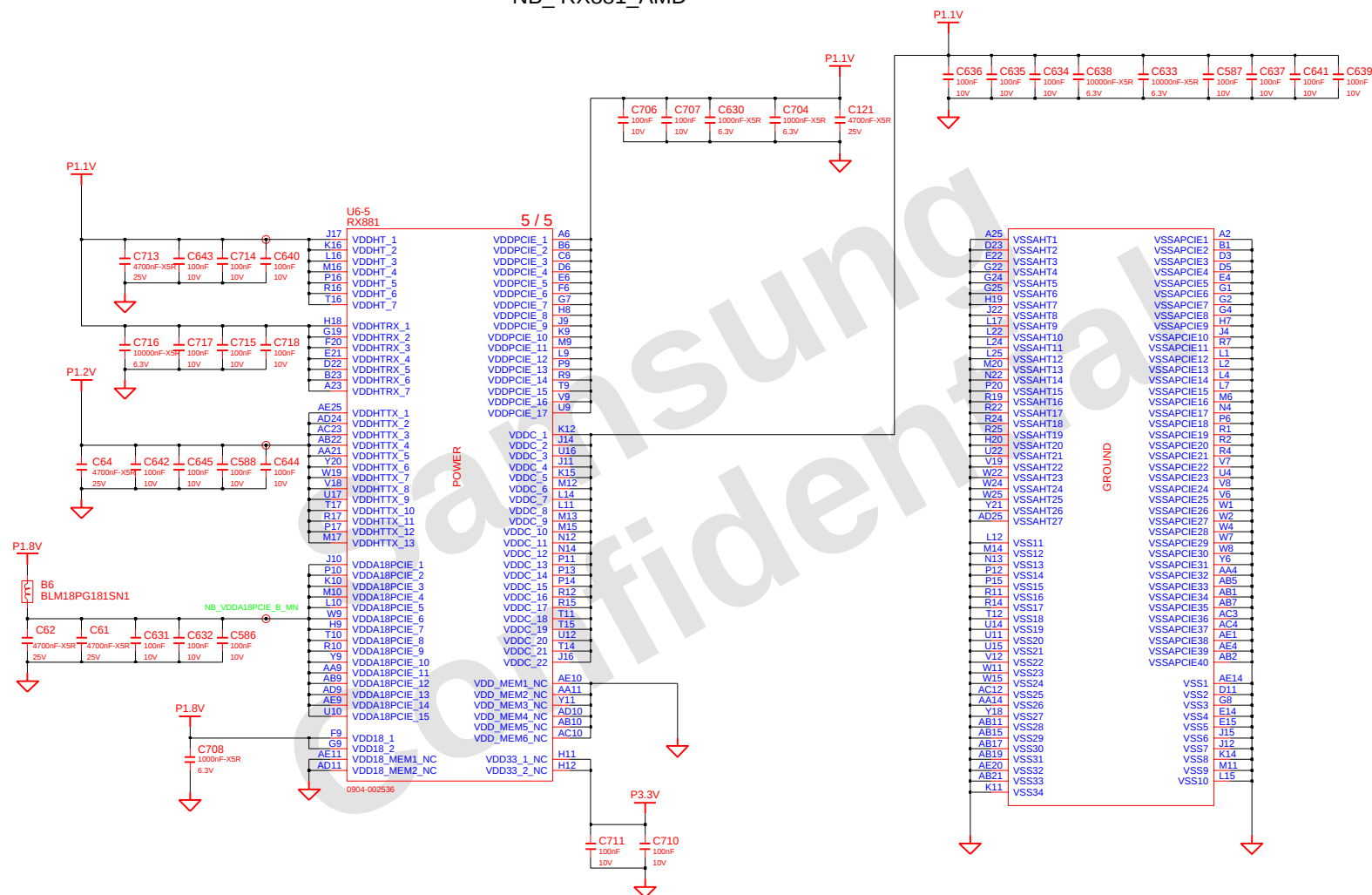
COM-22C-015 (1996.6.5) REV. 3

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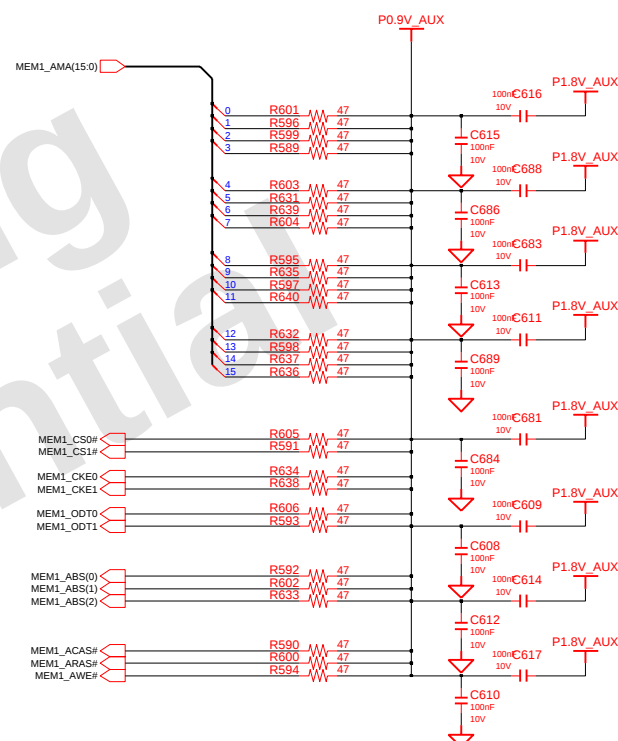
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APPROVAL	BC LEE	REV	0.1			
PART NO. BA41-xxxxxxA						
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	14 OF 58

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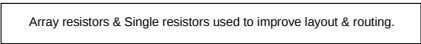
NB RX881 AMD



DRAW		XIE BIN		DATE	08/18/2009		TITLE		Suzhou-D		SAMSUNG ELECTRONICS				
CHECK		GUO LEI		REV. STEP		ADV		MCH							
APPROVAL		BC LEE		REV		0.1		RX881 (3/3)							
								PART NO.				BA41-xxxxxxA			
MODULE CODE				LAST EDIT				July 15, 2009 19:25:13 PM				PAGE	15	OF	58



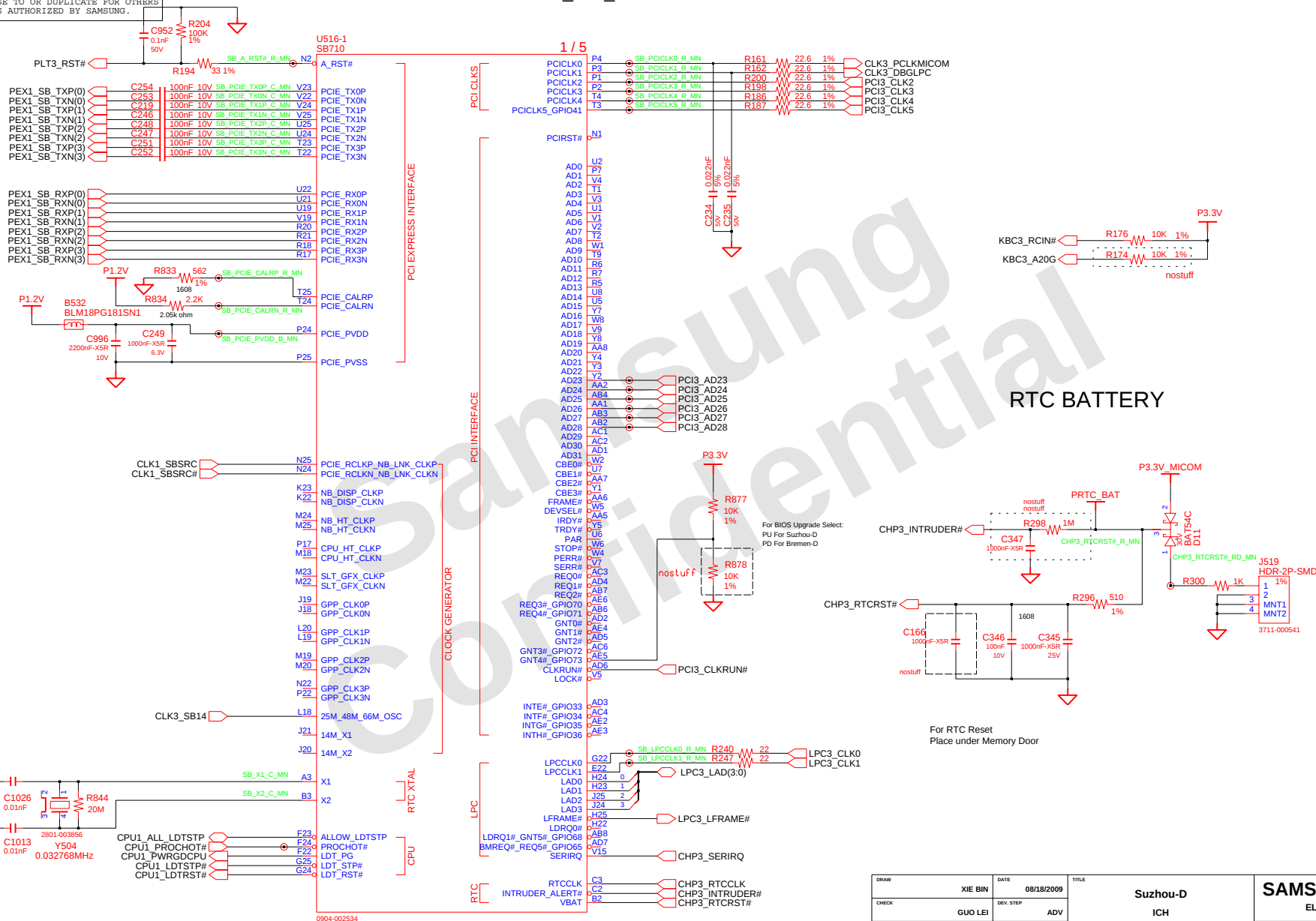
COM-22C-015(1996.6.5) REV. 3



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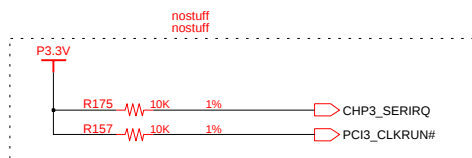
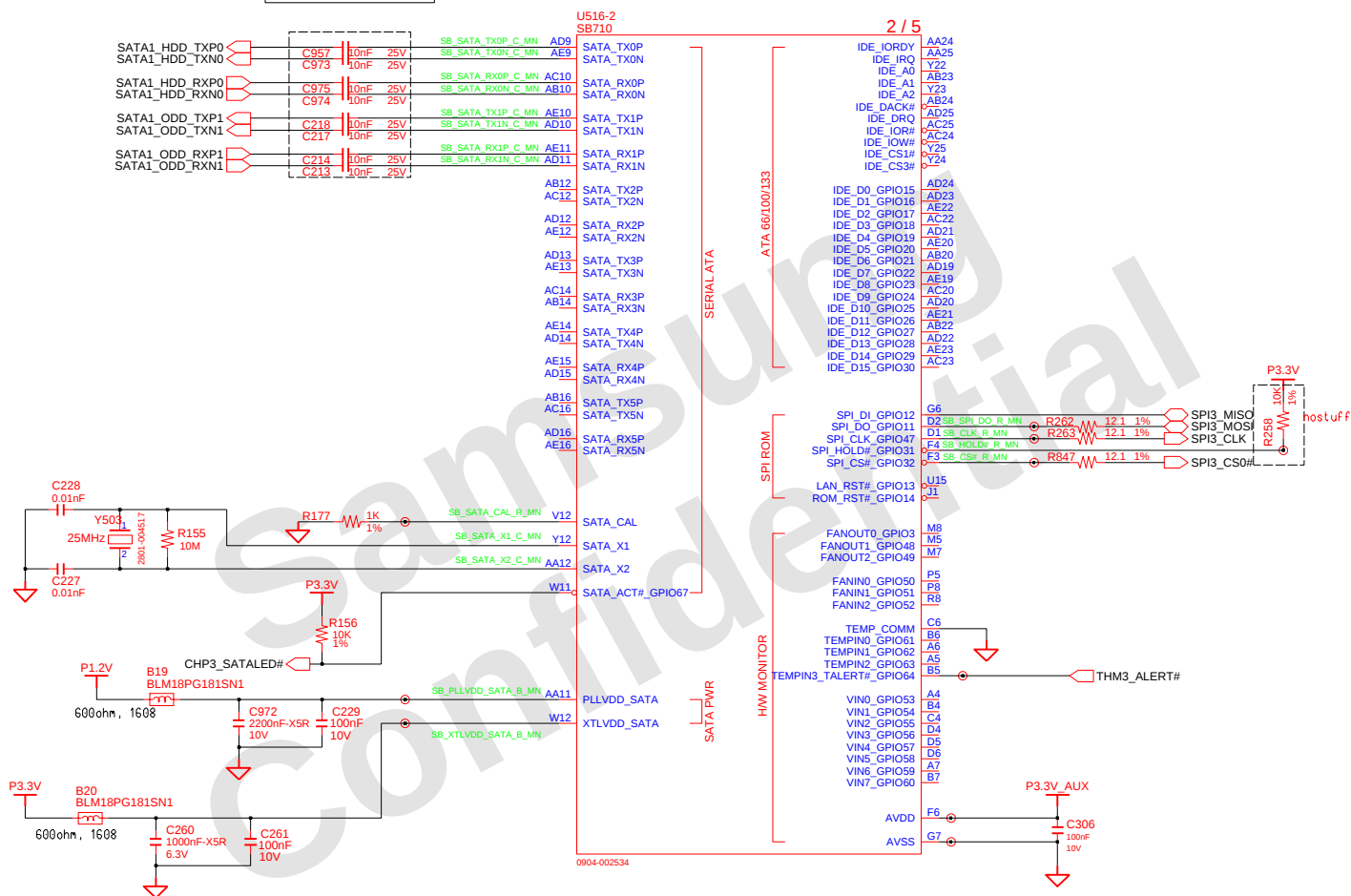
SB 710 AMD



DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D ICH SB710 (1/5)		
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1		PART NO.	BA41-xxxxxxA
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Route to connector side closely

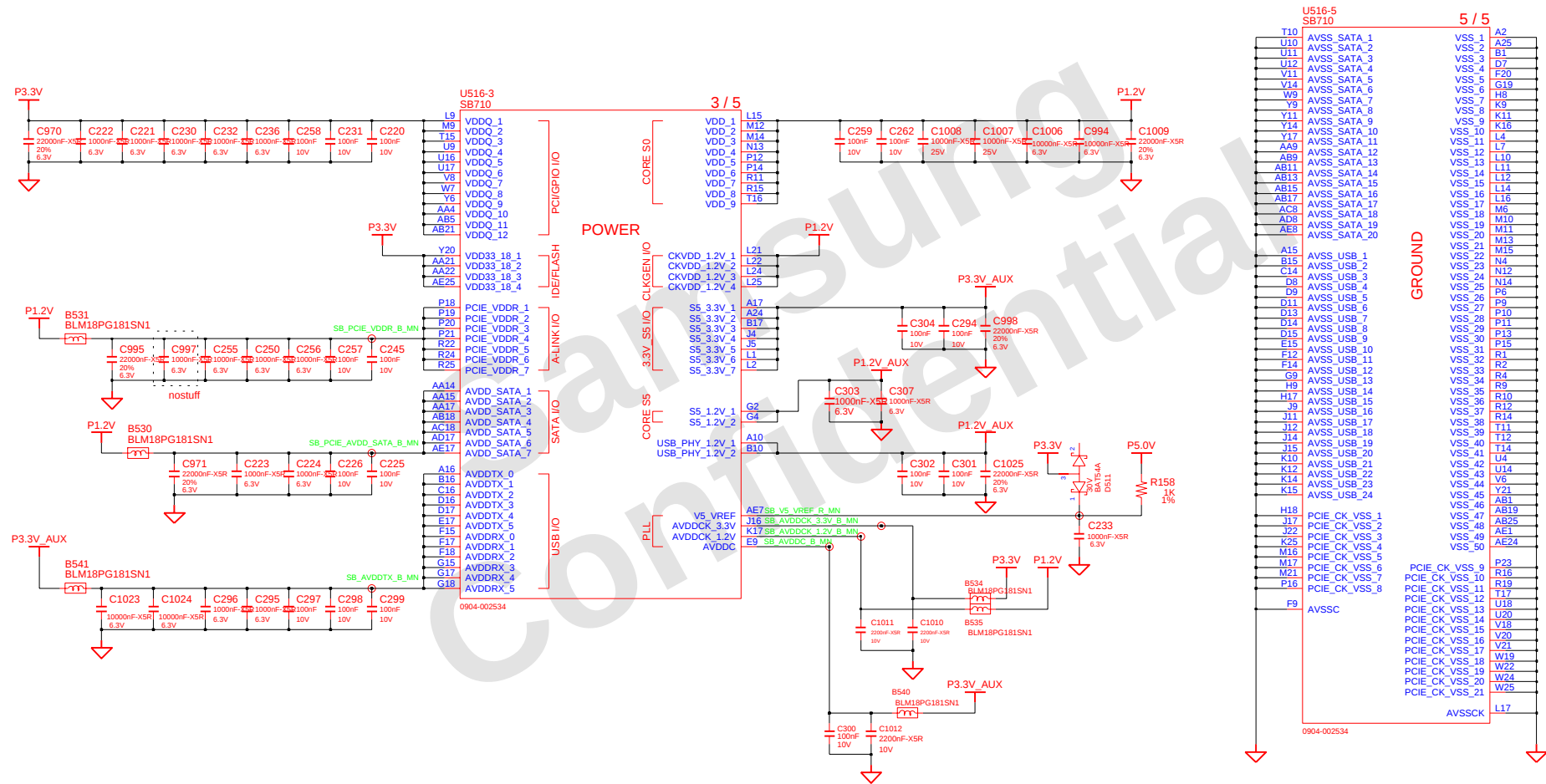


LPC option ; These are used with LPC

DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D ICH SB710 (2/5)	SAMSUNG ELECTRONICS
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SB_710_AMD

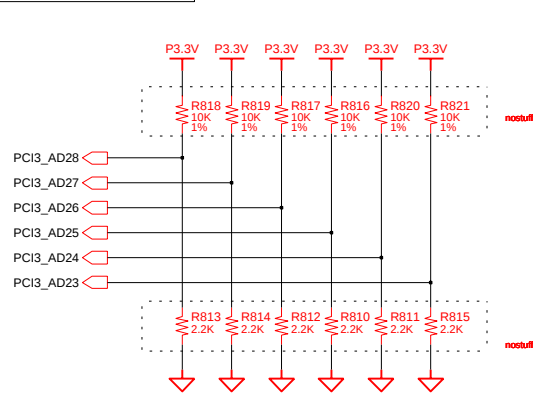


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxxA
CHECK	GUO LEI	DEV. STEP	ADV	ICH		
APPROVAL	BC LEE	REV	0.1	SB710 (4/5)		
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 21 OF 58	

Strap

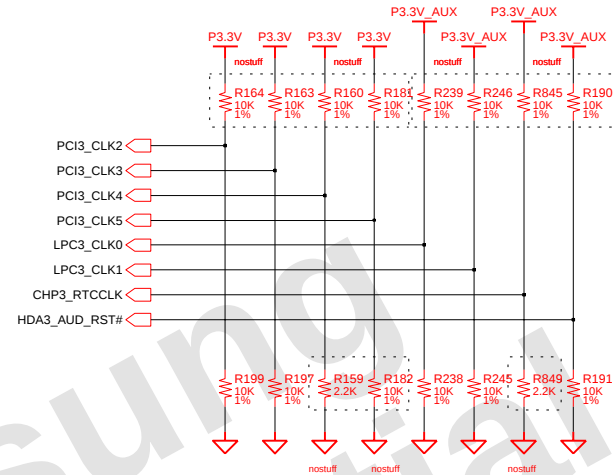
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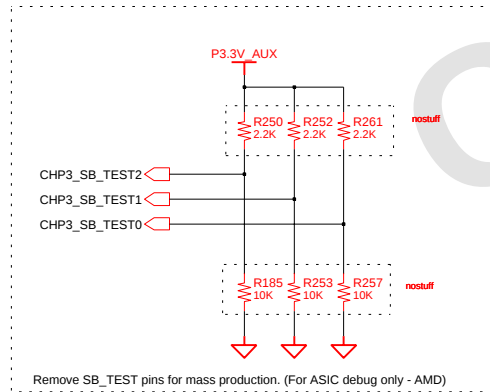


DEBUG STRAPS

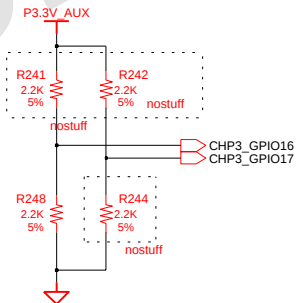
	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED



	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
STRAP HIGH	BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT
STRAP LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT



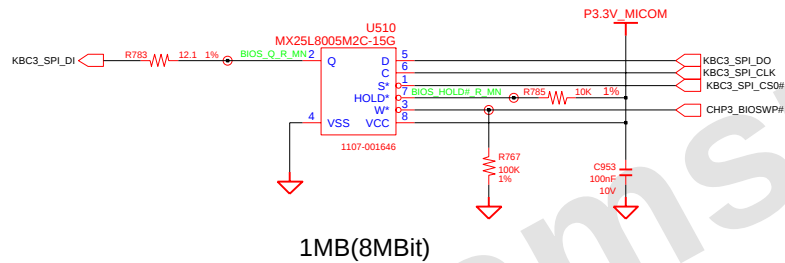
Remove SB_TEST pins for mass production. (For ASIC debug only - AMD)



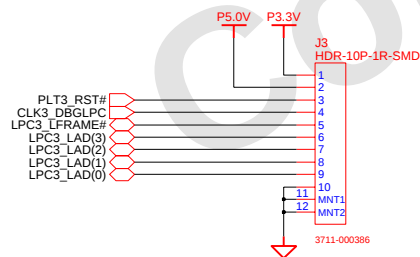
GPIO17	GPIO16
ROM TYPE	
NC, NC = RSVD	
NC, L = SPI ROM	
L, NC = LPC ROM	
L, L = FWH ROM	

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	ICH	ICH	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	SB710 Strap(5/5)	PART NO.	BA41-xxxxxxA
MODULE CODE	LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	22	OF 58

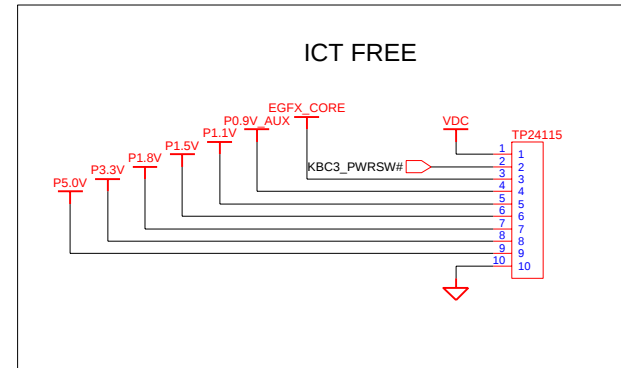
SPI_BIOS_ROM



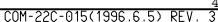
80H DECODER CONNECTOR



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
WITH INITIAL POST VALUE		88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TEST CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	C2	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	DA	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DC	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DE	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY "PRESS... SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

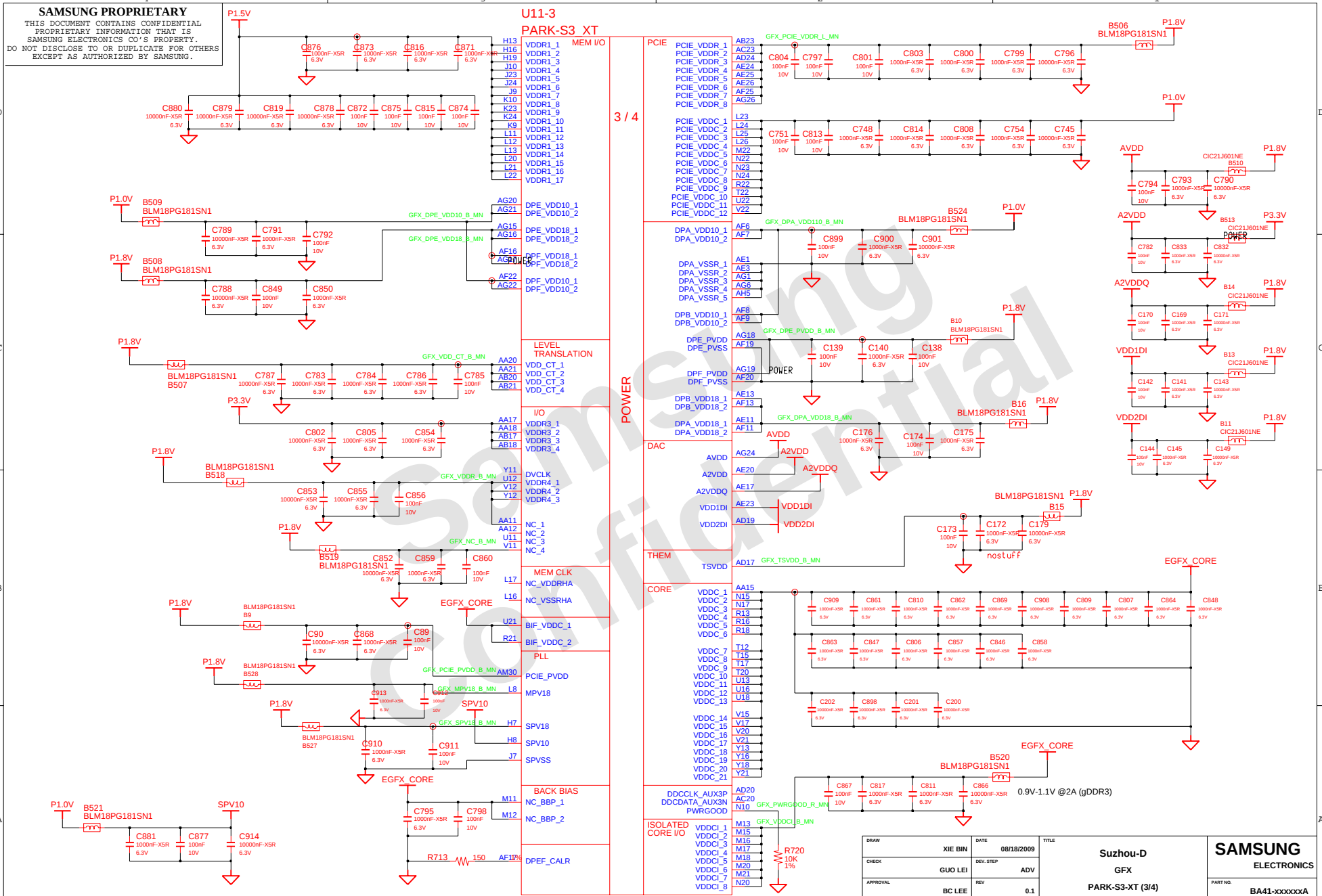


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV		SPI_BIOS_ROM	ELECTRONICS
APPROVAL	BC LEE	REV	0.1		SPI_BIOS_ROM	PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxA
				July 15, 2009 19:25:13 PM	PAGE	23 OF 58

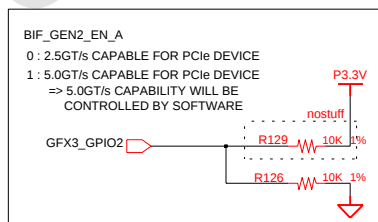
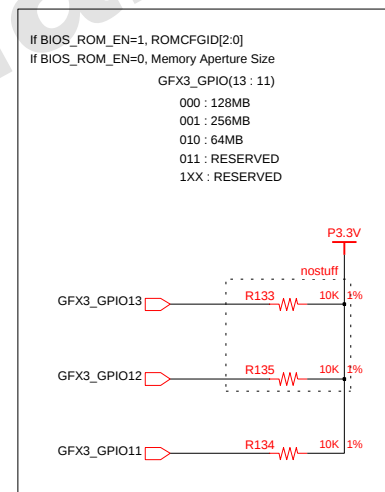
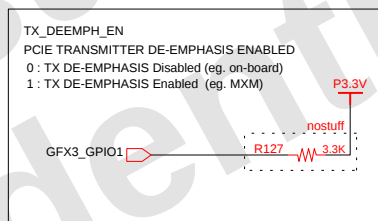
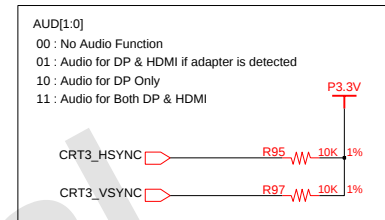
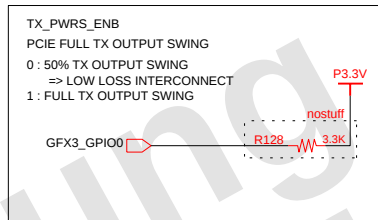
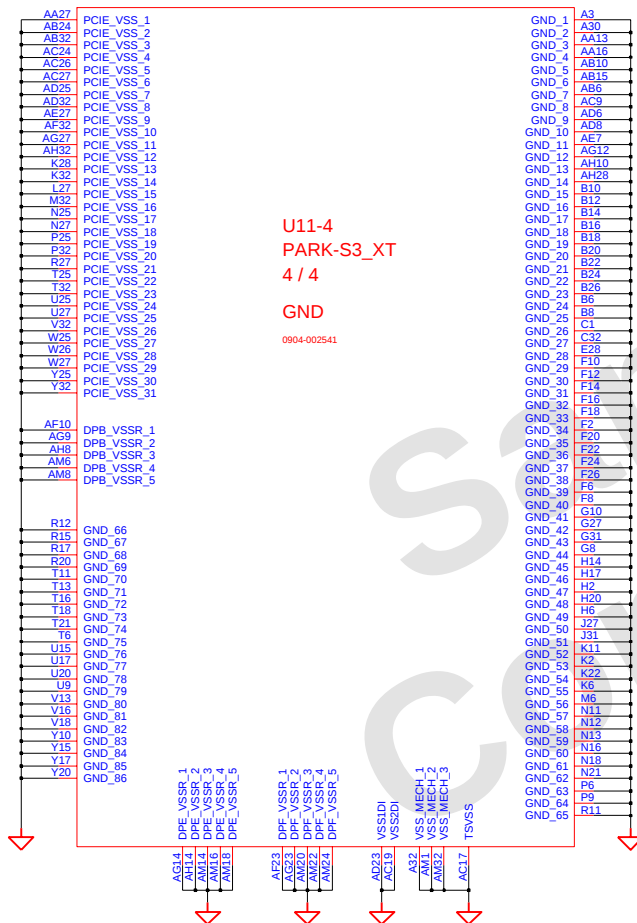


DRAW	XIE BIN	DATE	08/18/2009	TITLE Suzhou-D GFX PARK-S3-XT (2/4)			
CHECK	GUO LEI	DEV. STEP	ADV				
APPROVAL	BC LEE	REV	0.1		PART NO. BA41-xxxxxxA		
MODULE CODE	LAST EDIT				July 15, 2009 19:25:13 PM	PAGE	25 OF 58

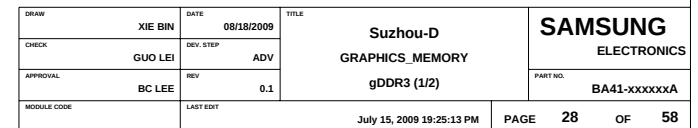
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PARK Straps

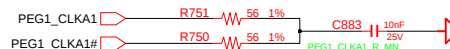
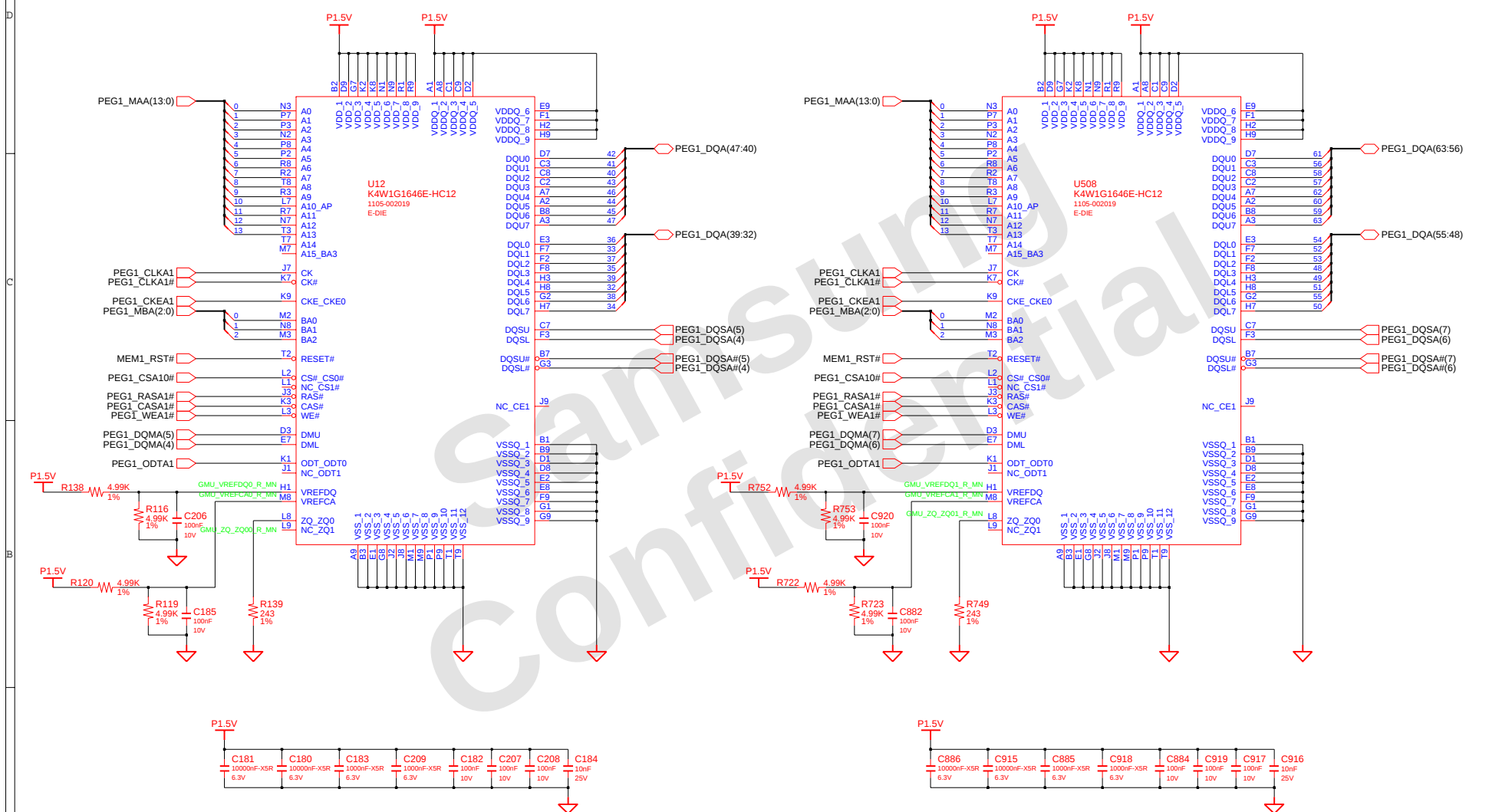


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	GFX	GFX	
APPROVAL	BC LEE	REV	0.1	PARK-S3-XT (4/4)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	27	OF 58



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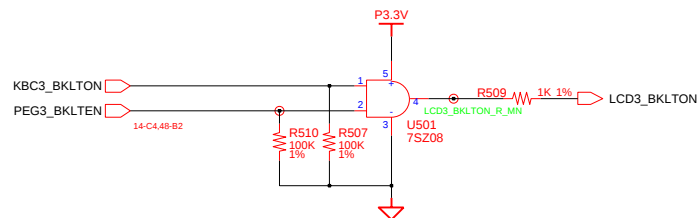
A-channel Upper Data



DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D GRAPHICS MEMORY gDDR3 (2/2)	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	0.1		
PART NO. BA41-xxxxxxA					
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 29 OF 58

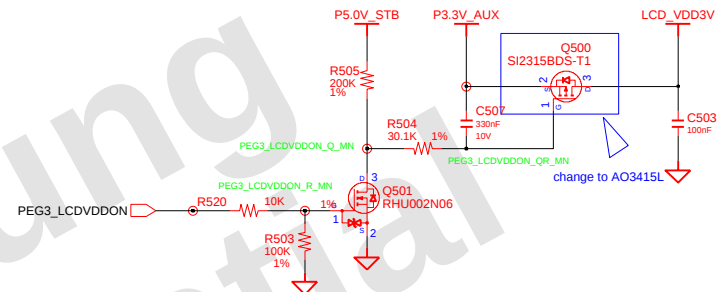
LVDS

Backlight On

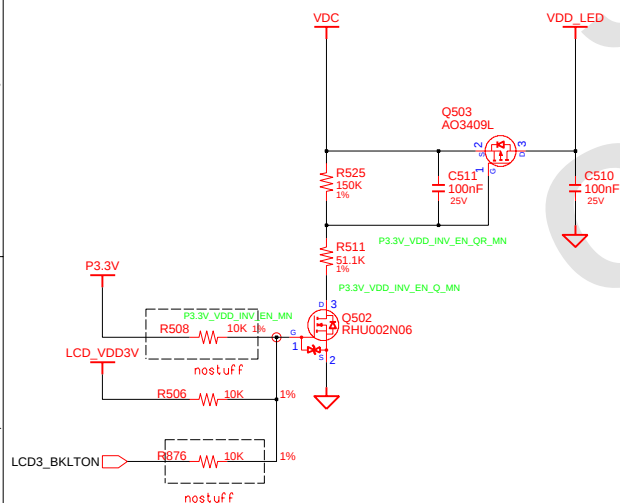


LCD Power

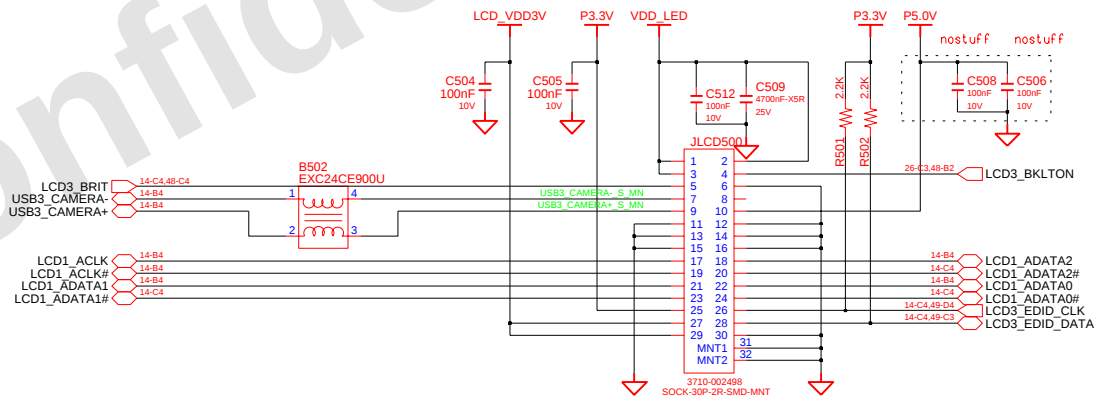
EBL Purpose



Converter Power



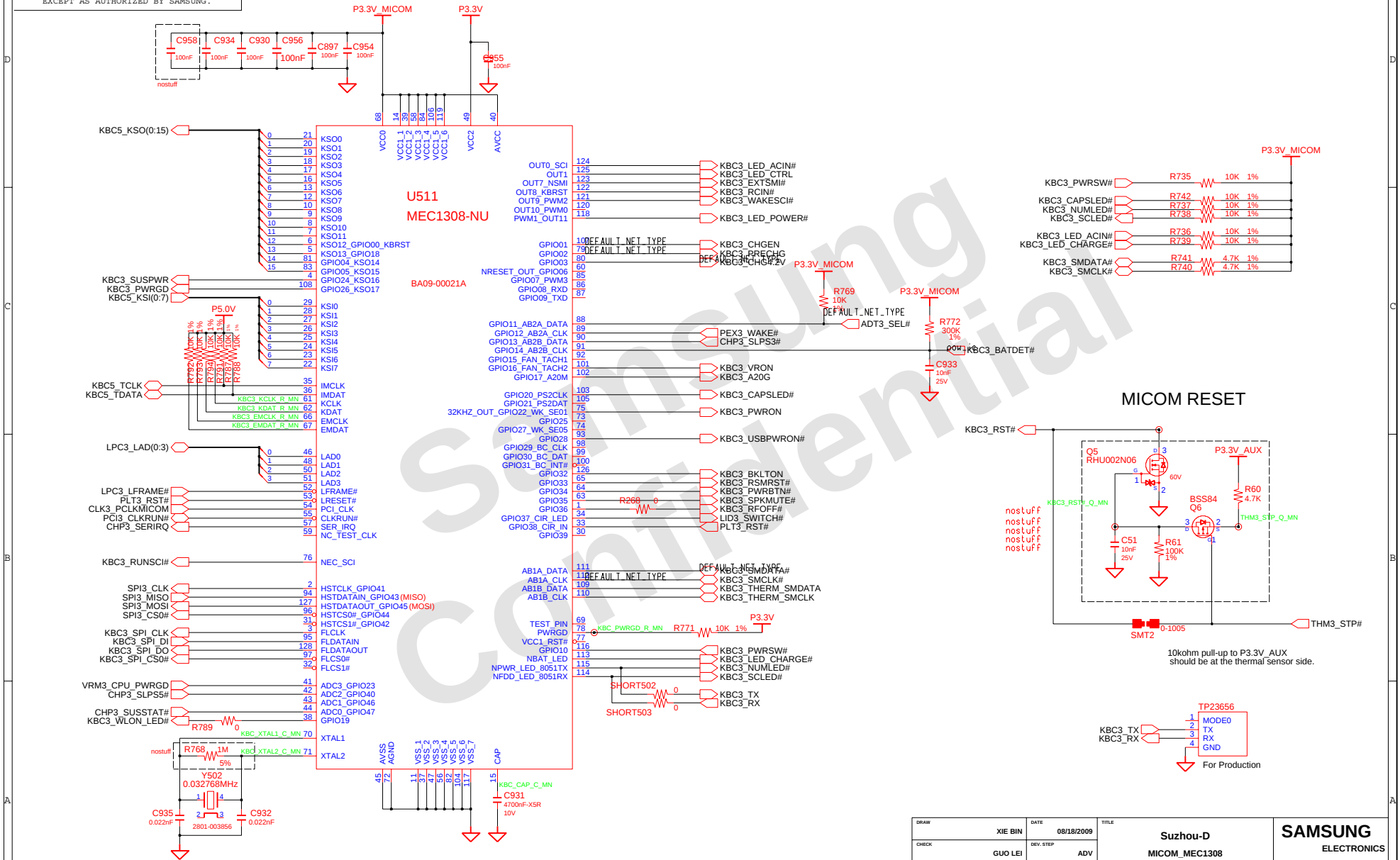
Camera + LCD Connector



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			PART NO. BA41-xxxxxxA
APPROVAL	BC LEE	REV	0.1	GRAPHICS_IF (1/2)		
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	30	OF 58

MICOM_MEC1308-NU

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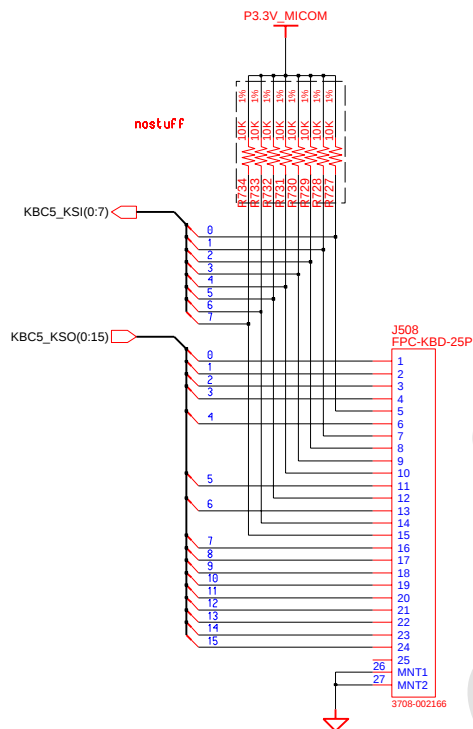


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D
CHECK	GUO LEI	DEV. STEP	ADV		MICOM_MEC1308
APPROVAL	BC LEE	REV	0.1		MICOM_MEC1308
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	33 OF 58

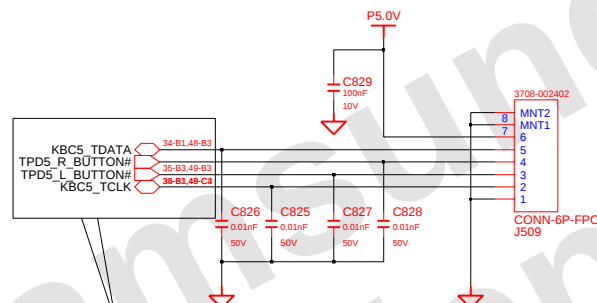
SAMSUNG
ELECTRONICS
PART NO.
BA41-xxxxxxA

Micom Glue Logic

KEYBOARD

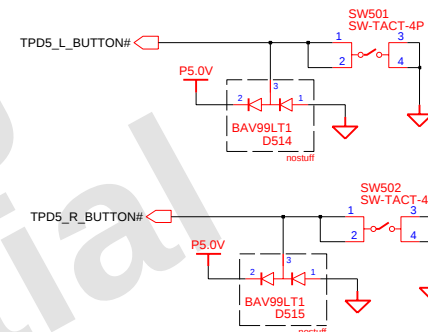


TOUCHPAD

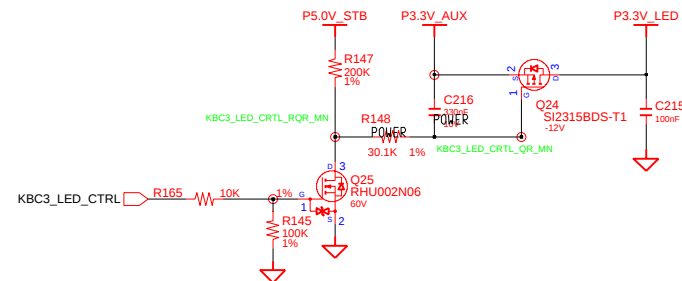


Confirm that there are PU on Touch PAD module side or micom.

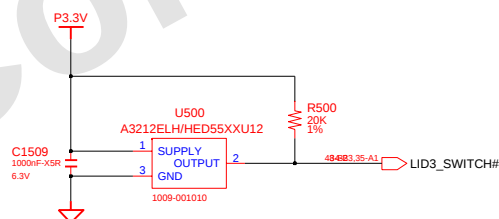
TOUCHPAD BUTTON



TOUCHPAD LED POWER



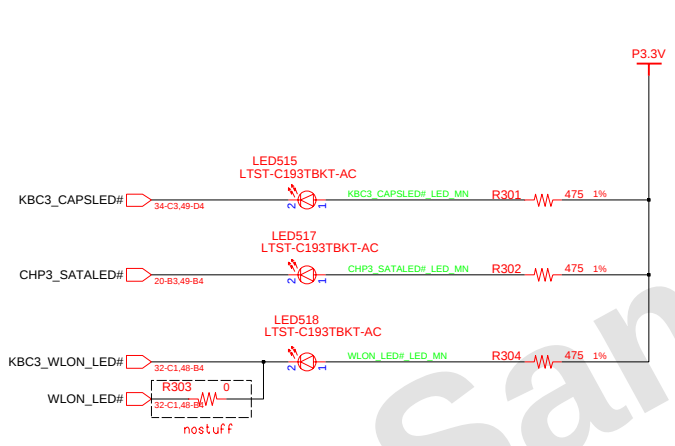
LID SWITCH



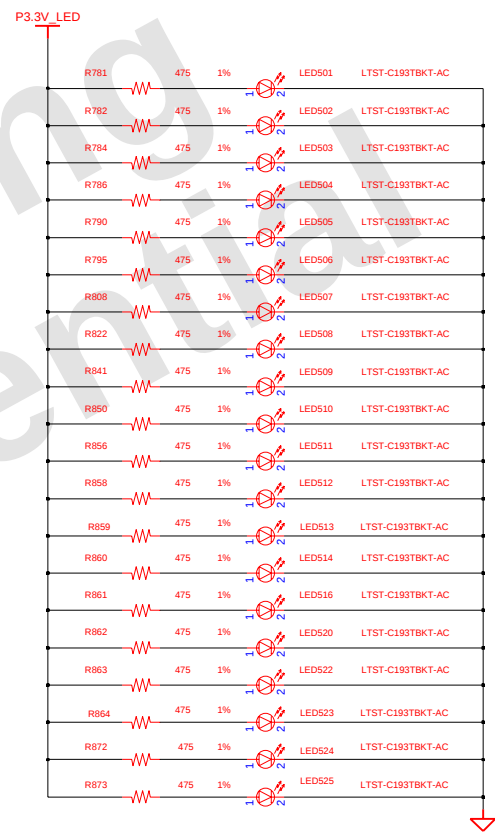
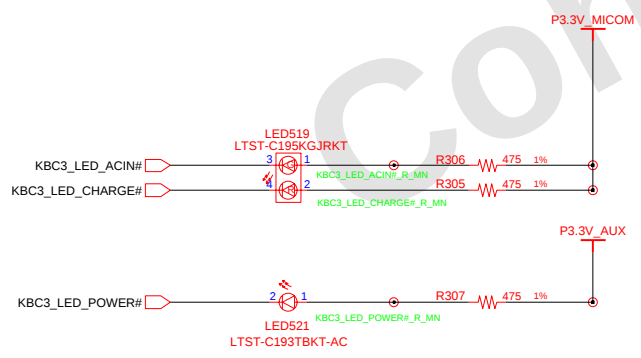
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CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1	MICOM_GLUE		PART NO. BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	34	OF 58

LEDs

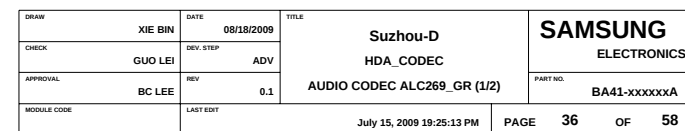
FUNCTION KEY LED



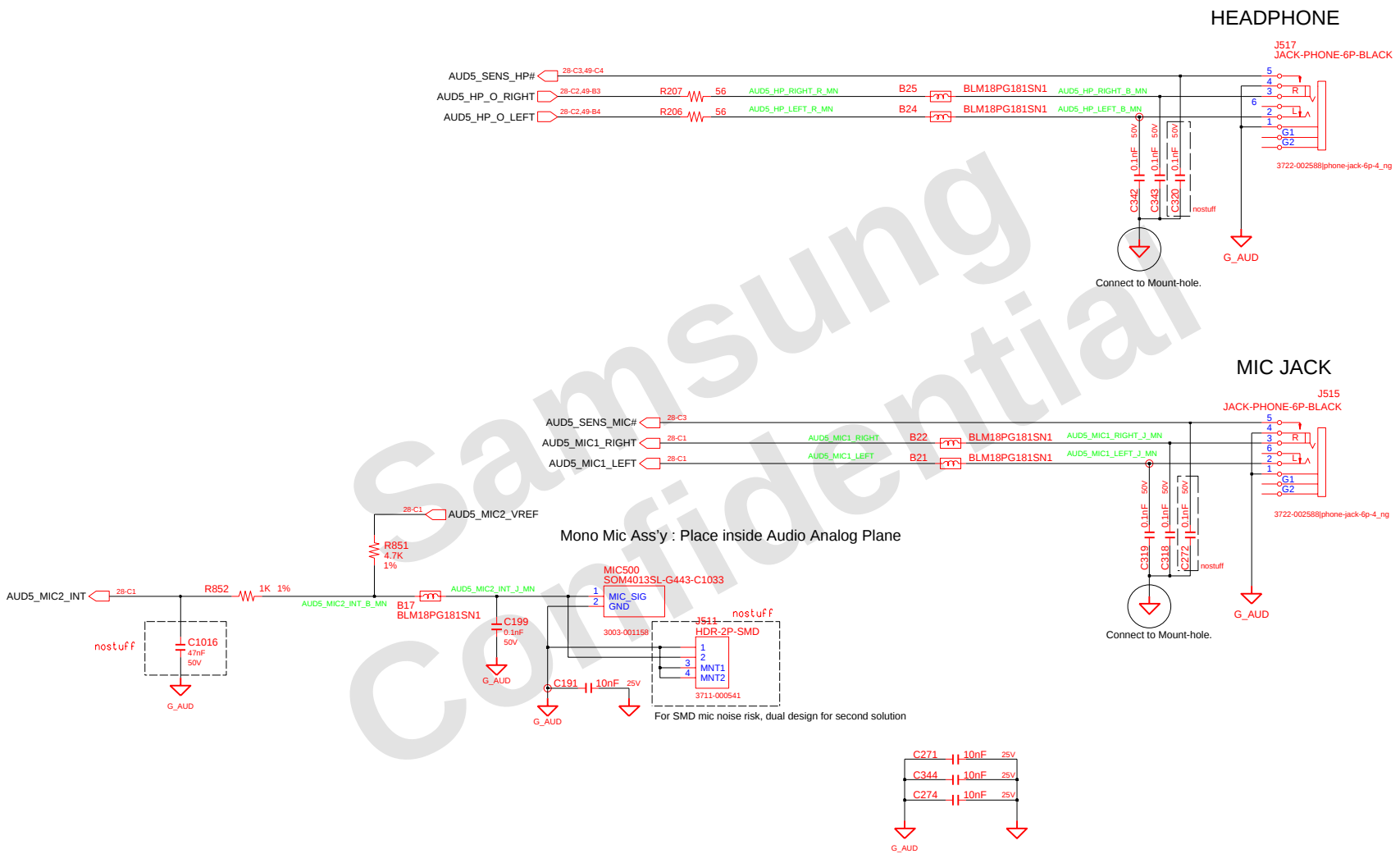
ADAPTERIN/CHARGING LED



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	LED_SWITCH	LED_SWITCH	ELECTRONICS
APPROVAL	BC LEE	REV	0.1			PART NO.
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM			BA41-xxxxxxA
					PAGE	35 OF 58

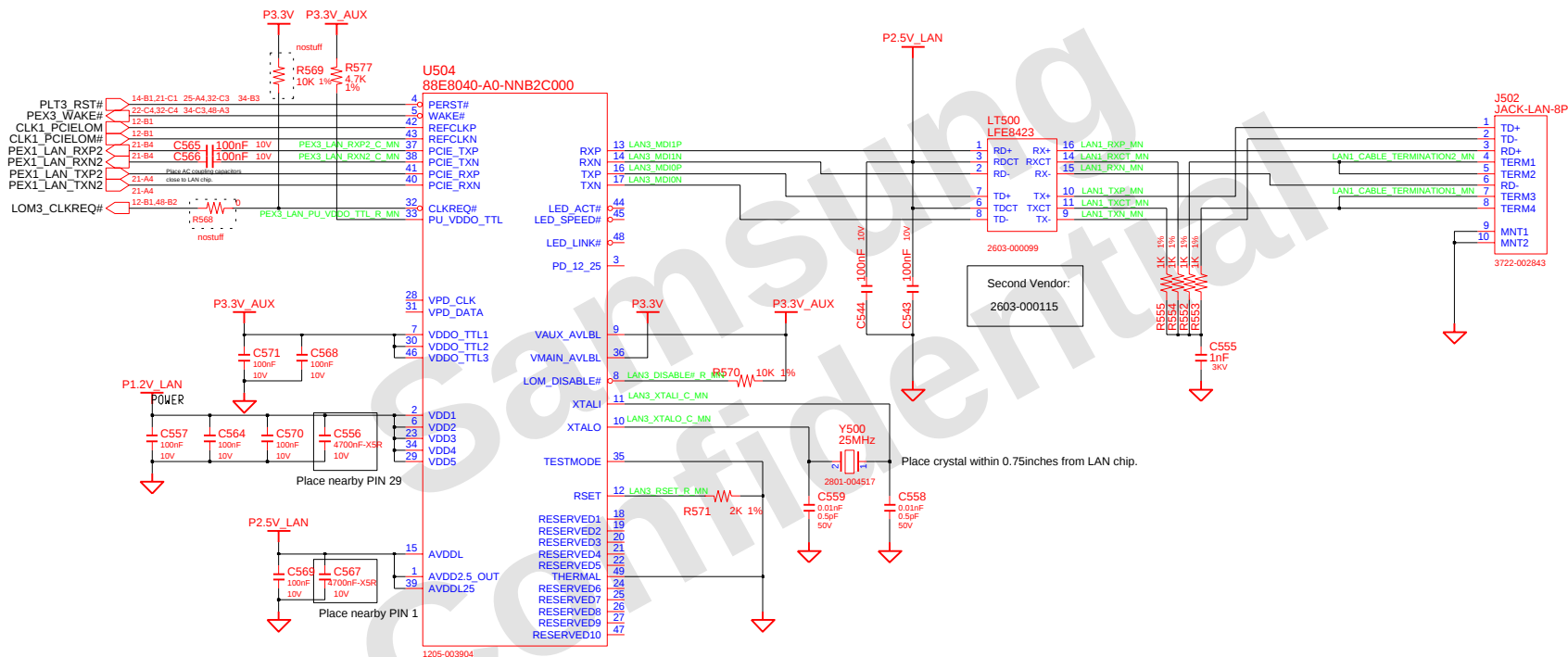


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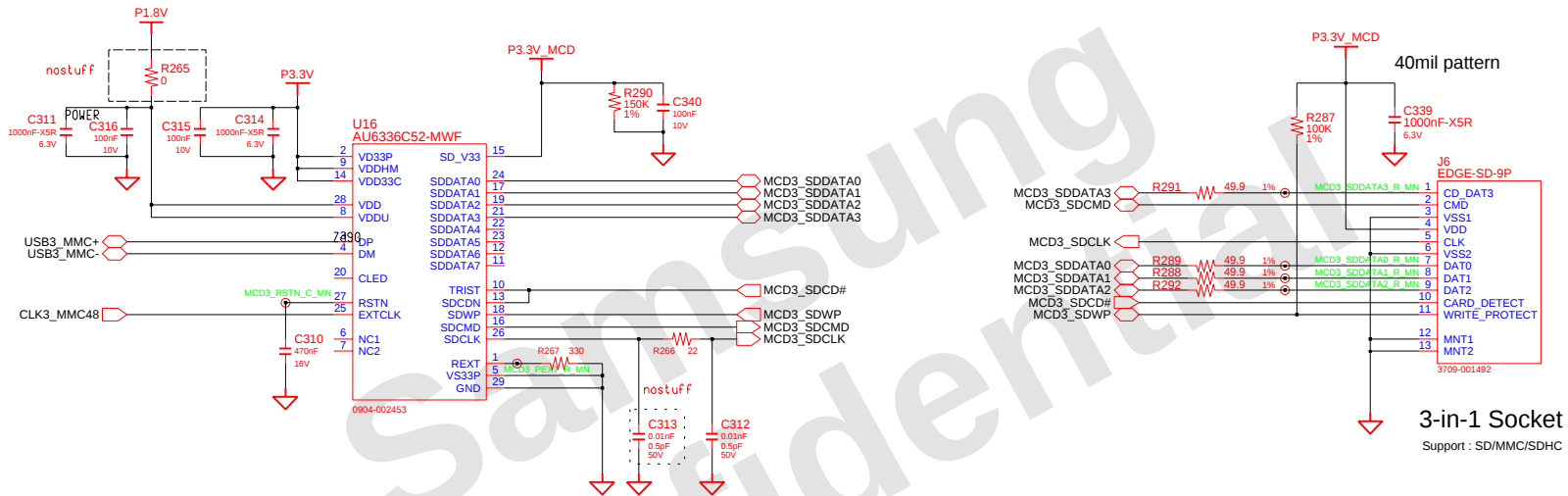
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	HDA_CODEC	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	AUDIO CODEC ALC269_GR (2/2)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	37	OF 58

LAN Controller (Marvell 88E8040)



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	LAN	LAN	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	LAN_Marvell 88E8040	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	38	OF 58

Card Reader (AU6336)

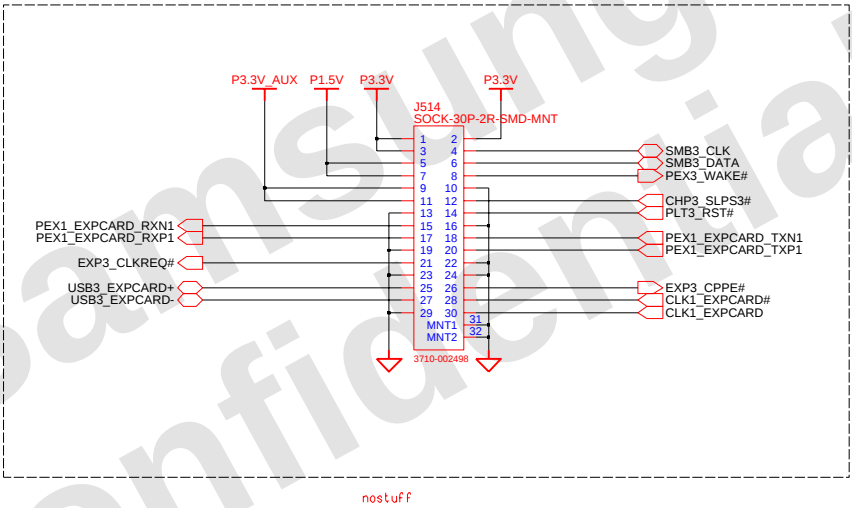


MCD3_SD_SPD	SD v1.0 Clock Option
PU / PD : No Stuff	24 MHz (default)
PU : Stuff, PD : No Stuff	15 MHz

MCD3_CLK_IN	827S Clock Source option
PU : X, PD : X	12MHz, fixed S/N
PU : No Stuff, PD : Stuff	12MHz, no S/N
PU : Stuff, PD : No Stuff	48MHz

DRAW	XIE BIN	DATE	08/18/2009	TITLE Suzhou-D MULTICARD 3 IN 1 CARD		SAMSUNG ELECTRONICS				
CHECK	GUO LEI	DEV. STEP	ADV							
APPROVAL	BC LEE	REV	0.1							
				PART NO.		BA41-xxxxxxA				
MODULE CODE		LAST EDIT			July 15, 2009 19:25:13 PM		PAGE	40	OF	58

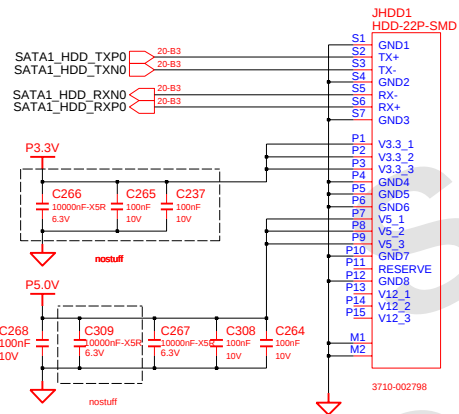
Express Card Connector



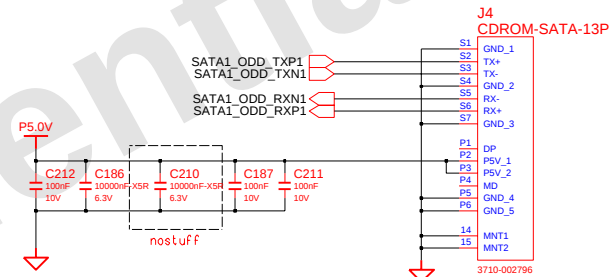
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1	EXPRESS CARD		PART NO. BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	41	OF 58

SATA I/F CONN

SATA HDD CONN



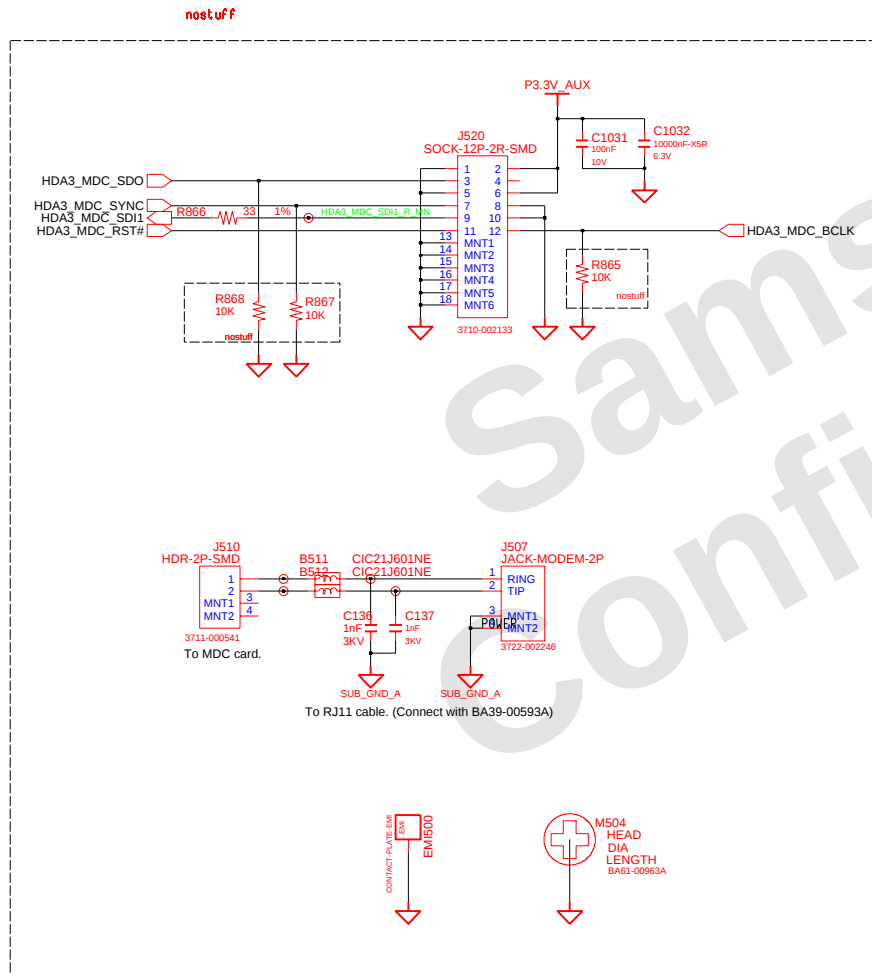
ODD CONN



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D SATA_DEVICES HDD & ODD SUB BONNECTOR	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			PART NO. BA41-xxxxxxA
APPROVAL	BC LEE	REV	0.1			
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 42 OF 58	

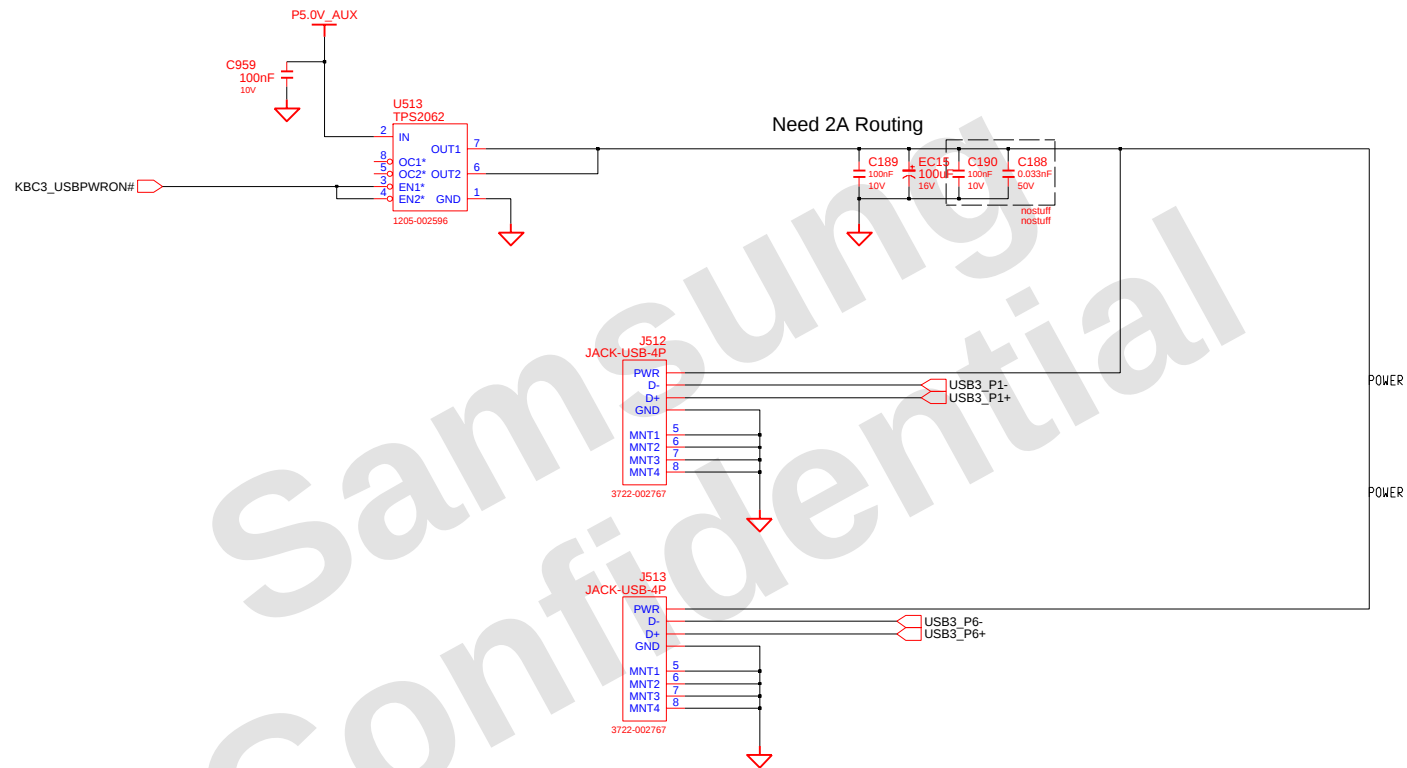
MDC Connector

BLUETOOTH



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	HDA_MODEM & BLUETOOTH		ELECTRONICS
APPROVAL	BC LEE	REV	0.1	MODEM & BLUETOOTH	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	43	OF 58

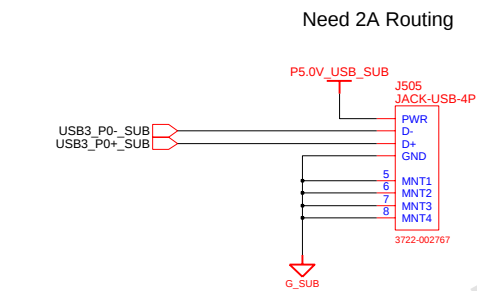
LEFT USB PORT



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	USB_CONNECTOR	USB_CONNECTOR	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	USB_CONNECTOR (1/2)	PART NO.	BA41-xxxxxxA
MODULE CODE	LAST EDIT			July 15, 2009 19:25:13 PM	PAGE	44 OF 58

USB PORT & POWER S/W SUB B'D

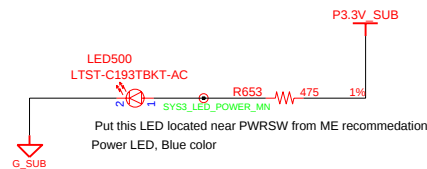
TOP RIGHT USB PORT



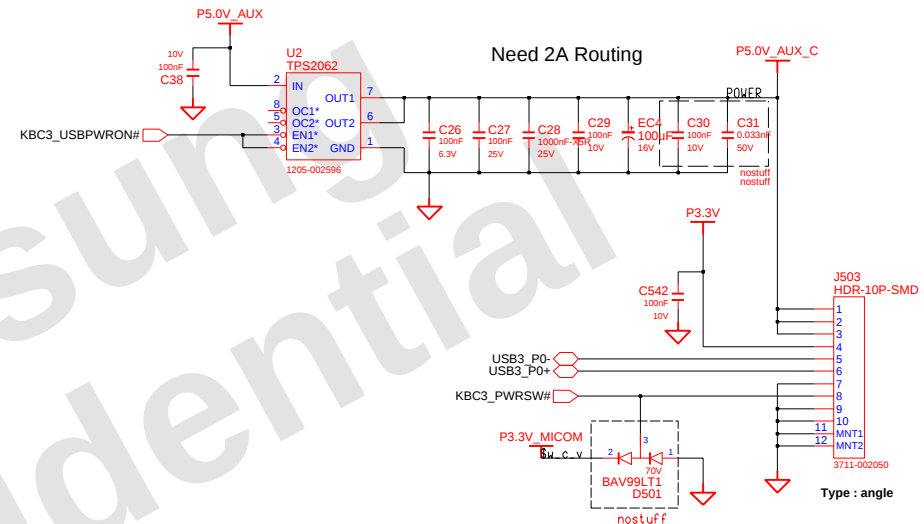
Power Button



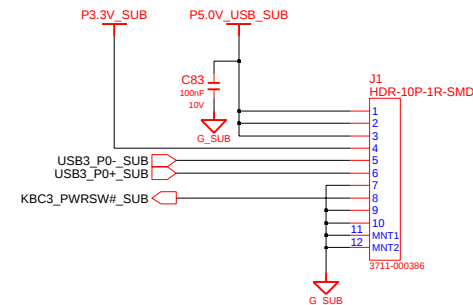
Power ON LED



MAIN TO SUB USB CONN

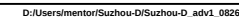


SUB TO MAIN USB CONN



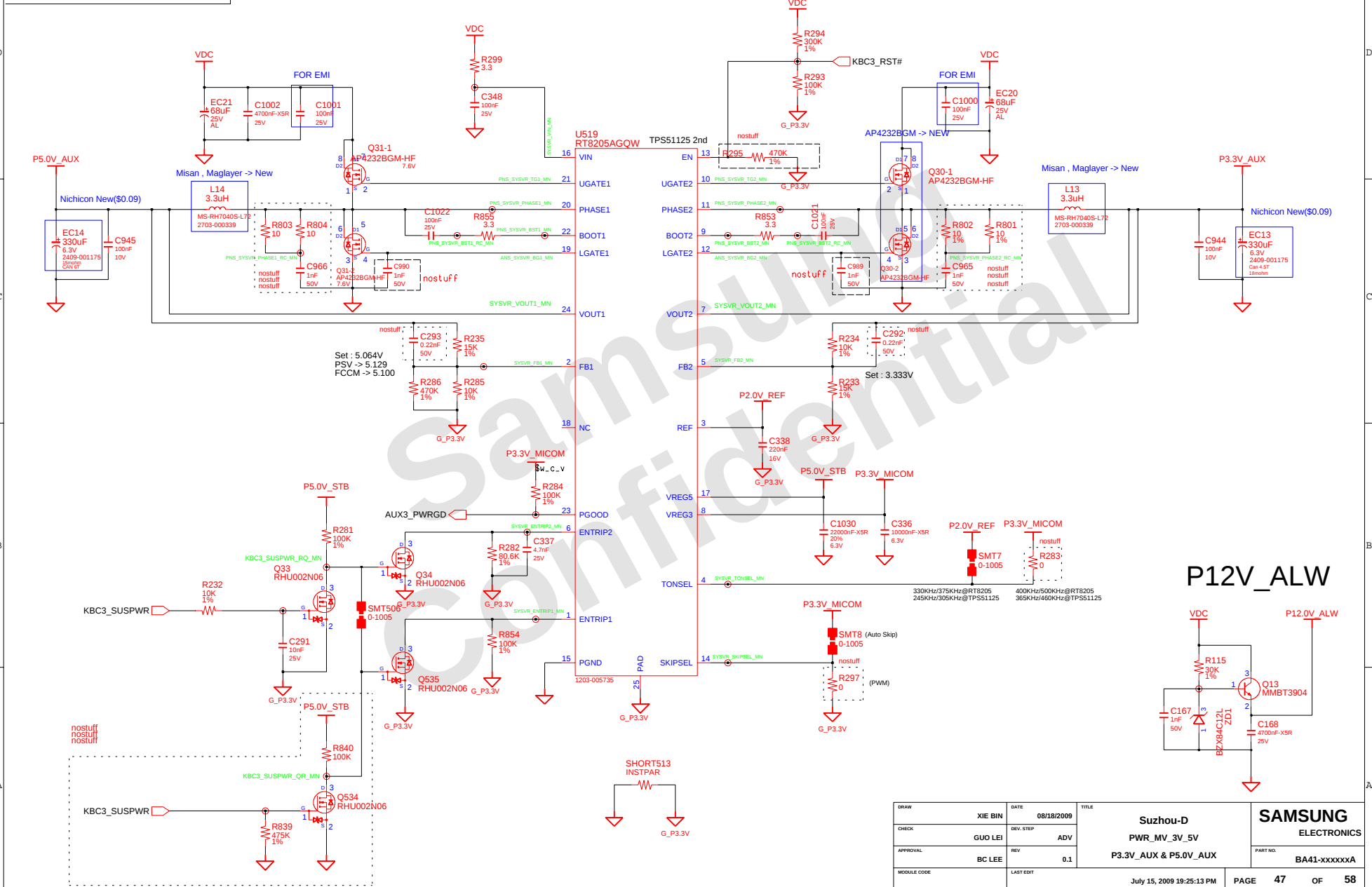
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	USB_CONNECTOR	USB_CONNECTOR	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	USB_CONNECTOR (2/2)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	45 OF 58

CHARGER & POWER MANAGEMENT

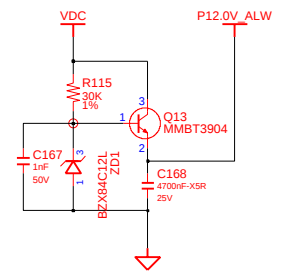


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P3.3V_AUX & P5.0V_AUX

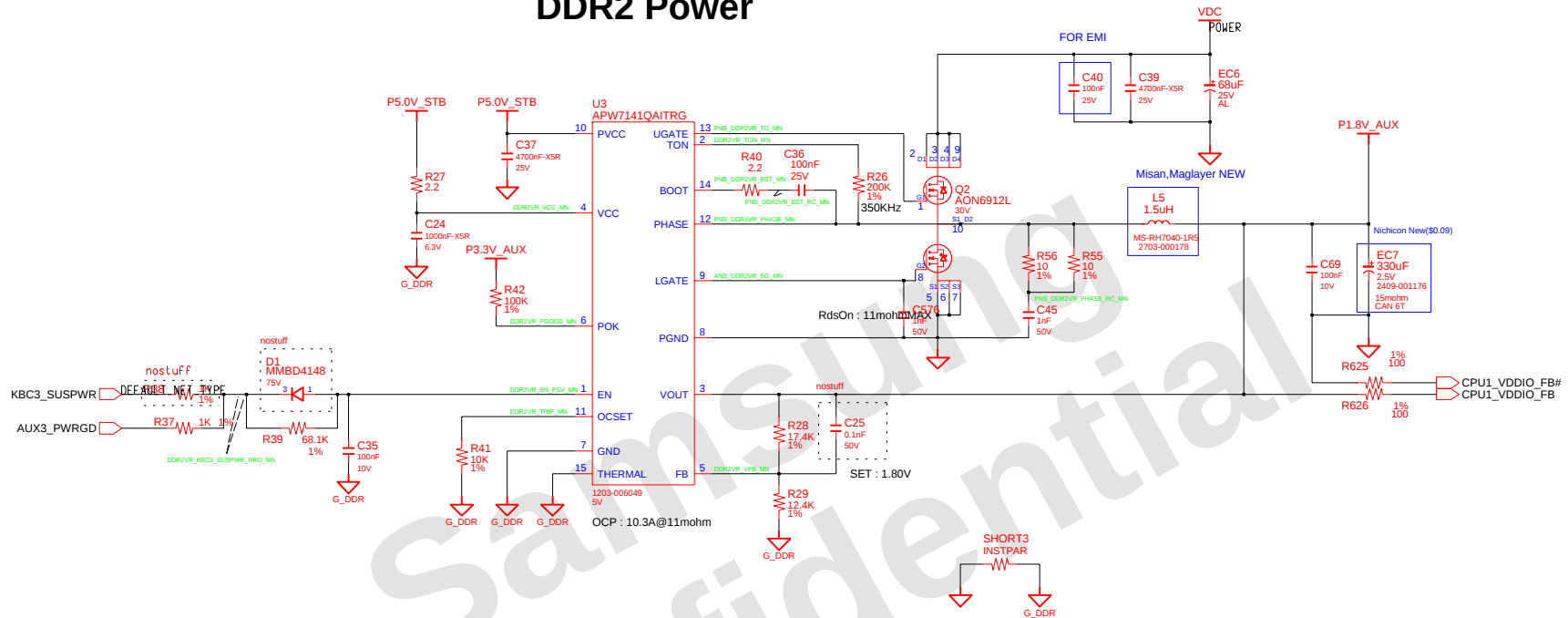


P12V_ALW

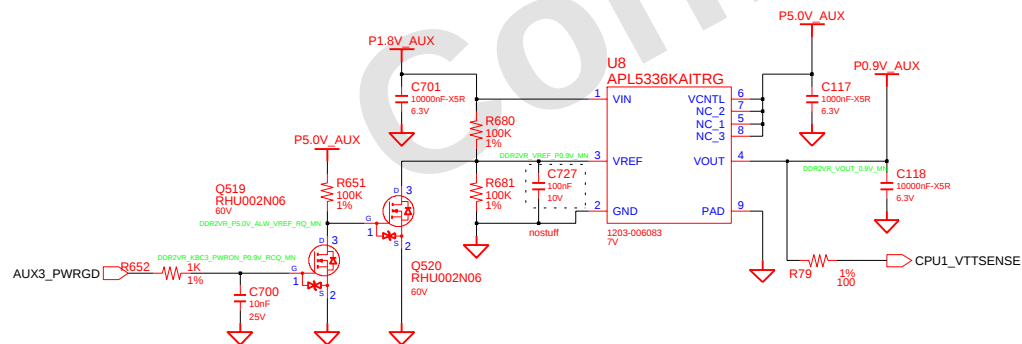


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV		PWR_MV_3V_5V	ELECTRONICS
APPROVAL	BC LEE	REV	0.1		P3.3V_AUX & P5.0V_AUX	PART NO.
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM			BA41-xxxxxA
					PAGE	47 OF 58

DDR2 Power



DDR2 VTT(P0.9V_AUX)

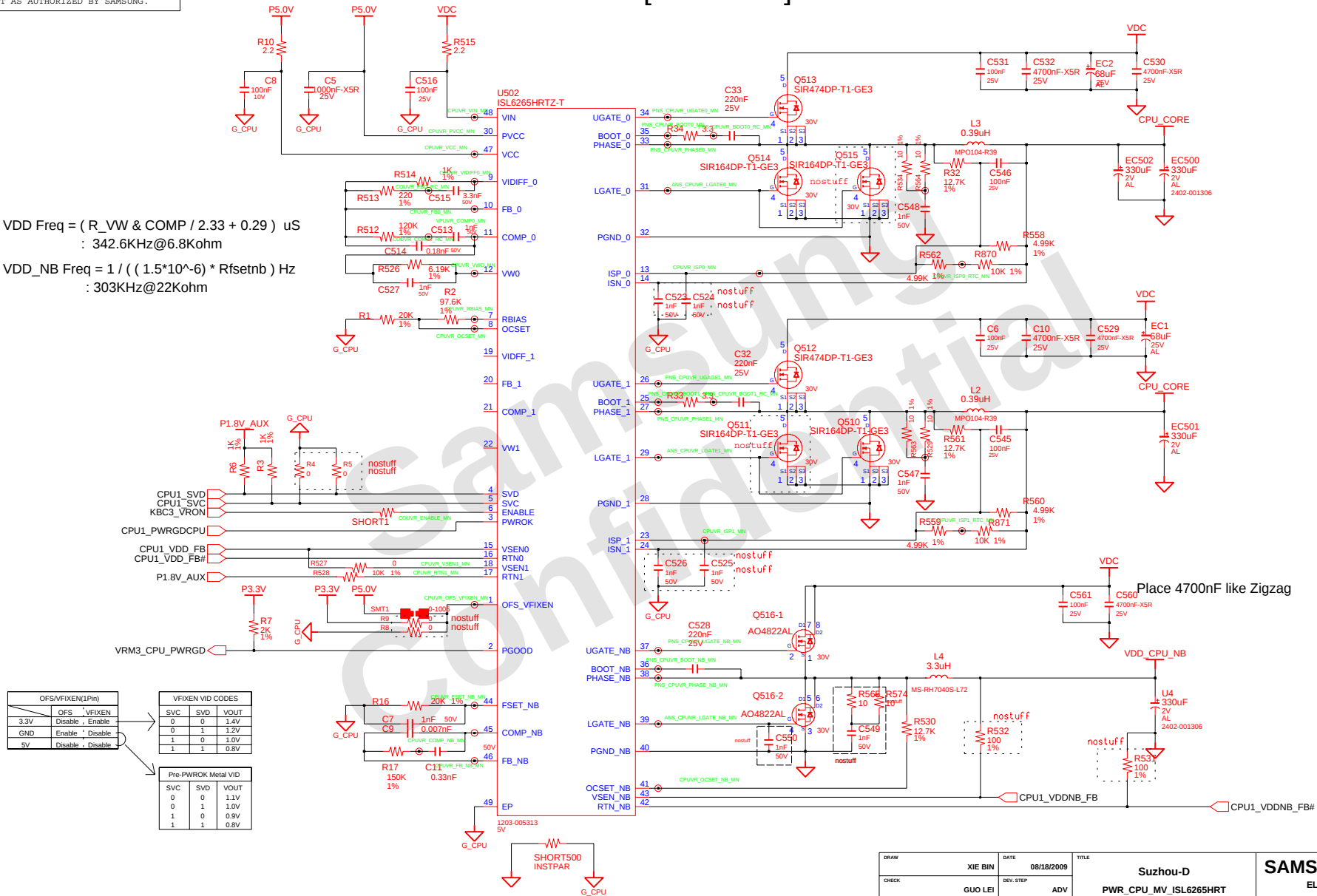


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	PWR_MEMORY	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	DDR2 POWER	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	48 OF 58

CPU VRM [INTERSIL]

VDD Freq = $(R_{VW} \& COMP / 2.33 + 0.29) \mu s$
: 342.6KHz@6.8Kohm

VDD_NB Freq = $1 / ((1.5 \cdot 10^{-6}) \cdot R_{fsetnb}) Hz$
: 303KHz@22Kohm

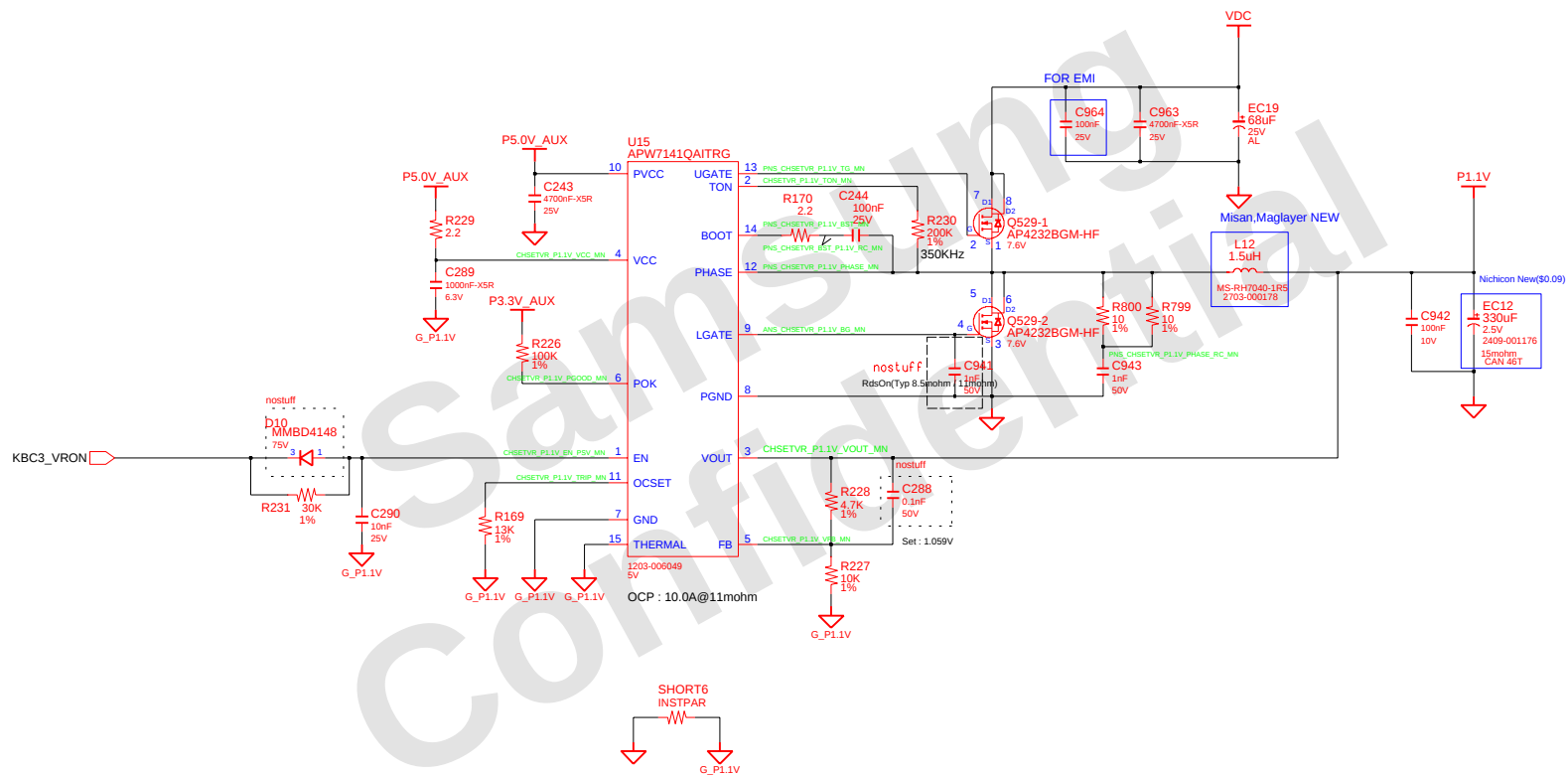


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D
CHECK	GUO LEI	DEV. STEP	ADV		PWR_CPU_MV_ISL6265HRT
APPROVAL	BC LEE	REV	0.1		CPU VRM (IMVP6+)
MODULE CODE		LAST EDIT			
July 15, 2009 19:25:13 PM					PAGE 49 OF 58

SAMSUNG
ELECTRONICS
PART NO.
BA41-xxxxxA

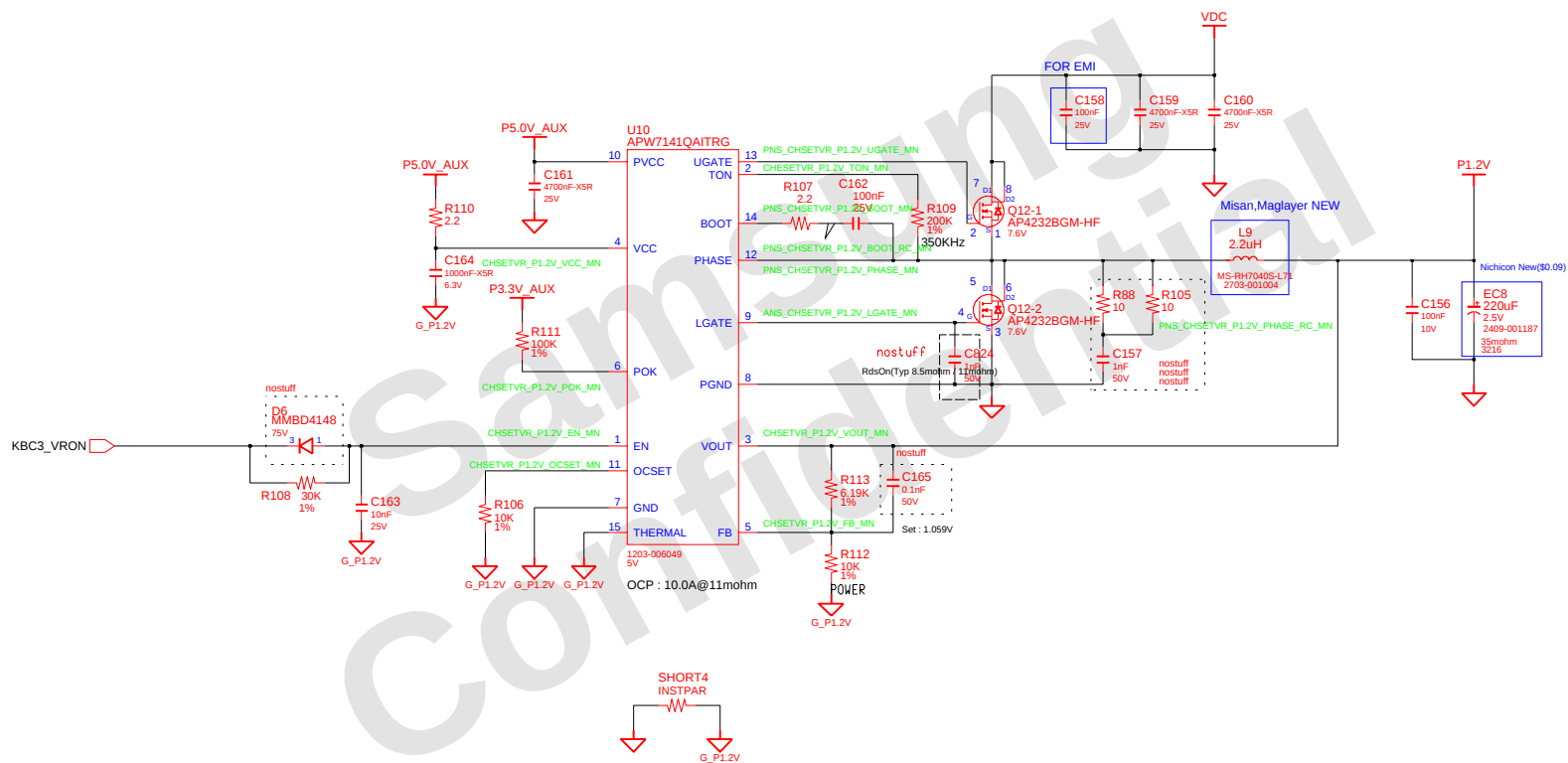
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CHIPSET POWER(P1.1V)



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	PWR_MV_RX881		
APPROVAL	BC LEE	REV	0.1	P1.1V	PART NO. BA41-xxxxxA	
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 50 OF 58	

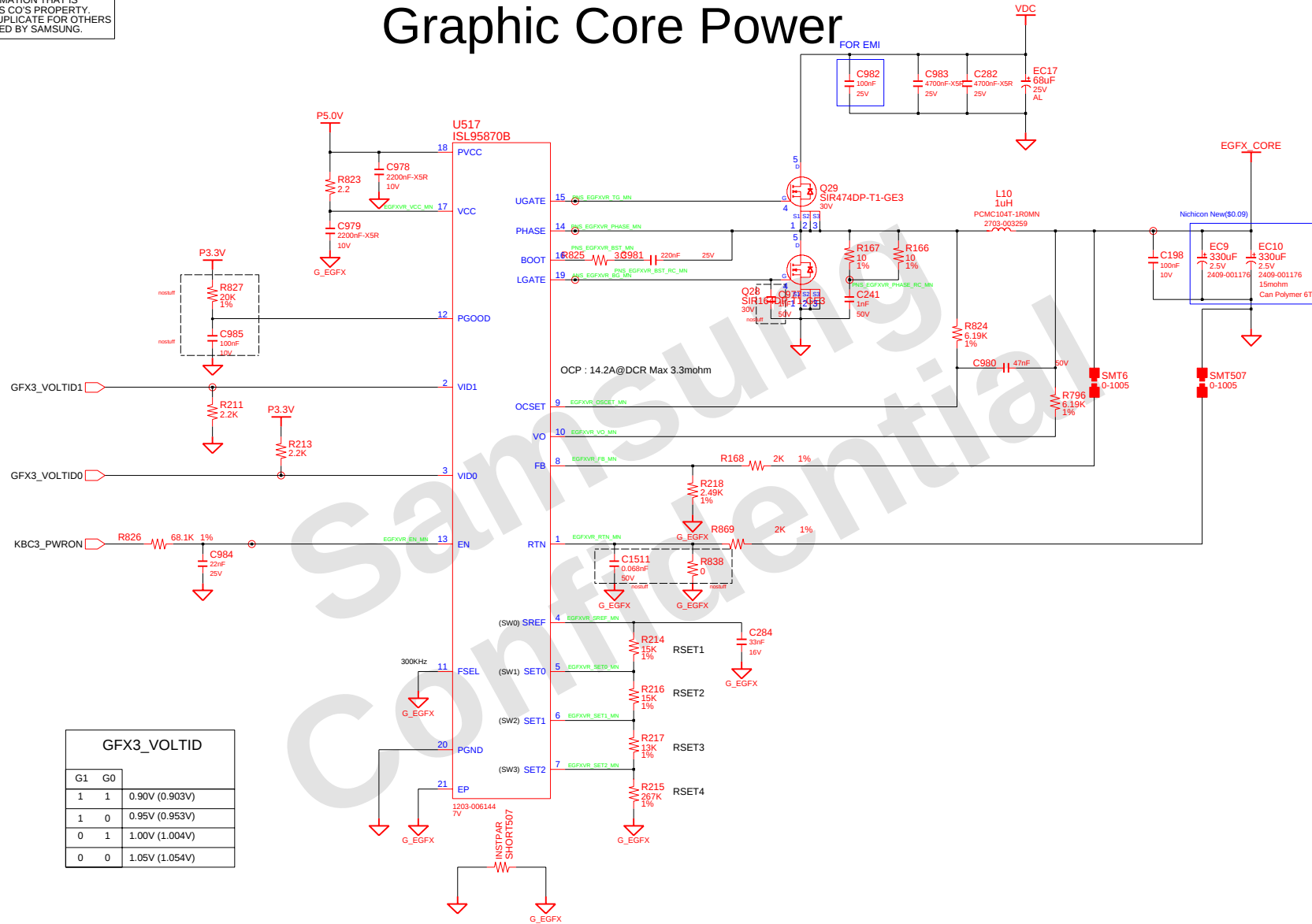
CHIPSET POWER(P1.2V)



DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D PWR_MV_RX881 P1.2V	SAMSUNG ELECTRONICS	
CHECK	GUO LEI	DEV. STEP	ADV		PART NO.	BA41-xxxxxxxA
APPROVAL	BC LEE	REV	0.1			
MODULE CODE	LAST EDIT				July 15, 2009 19:25:13 PM	PAGE 51 OF 58

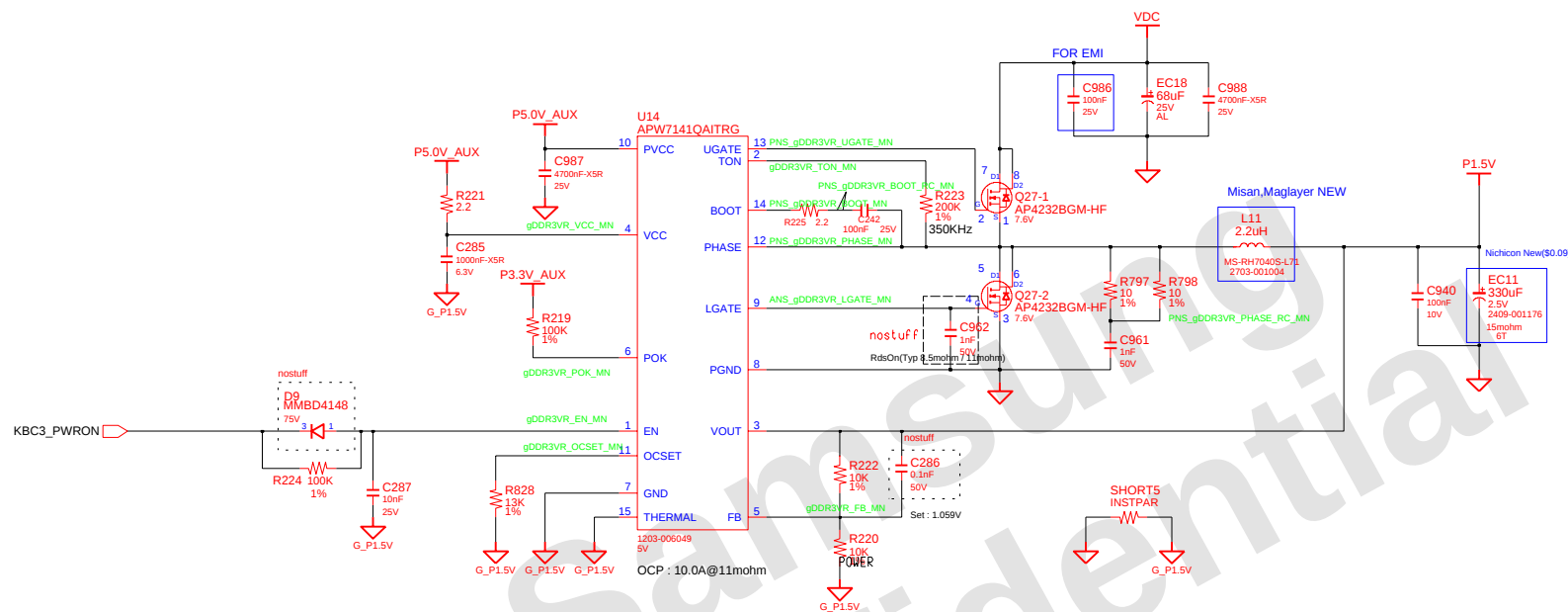
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Graphic Core Power

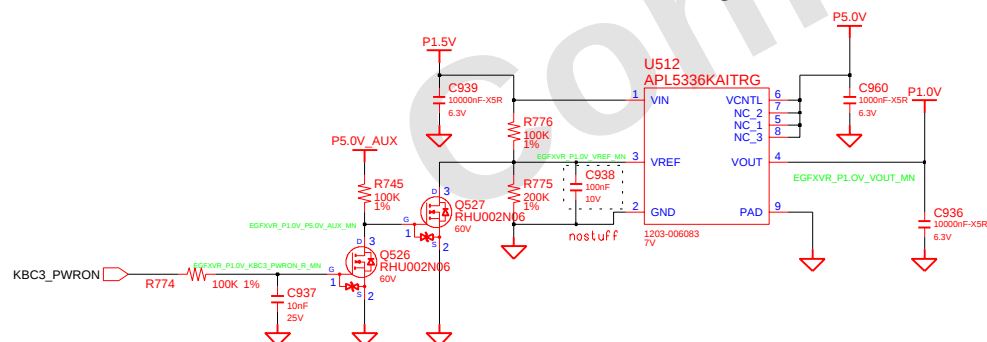


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	PWR GFX		ELECTRONICS
APPROVAL	BC LEE	REV	0.1	GFX POWER		PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxxA
				July 15, 2009 19:25:13 PM	PAGE	52 OF 58

gDDR3 POWER(P1.5V)



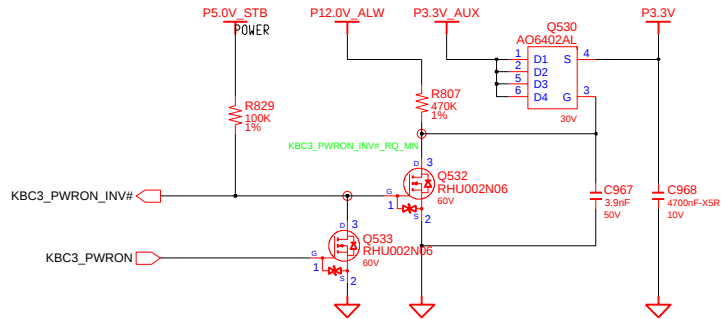
P1.0V



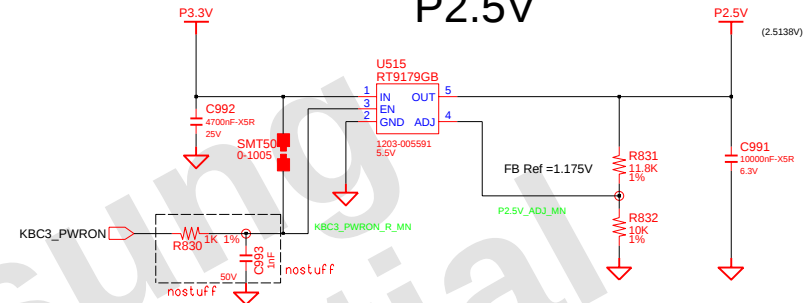
COM-22C-015(1996.6.5) REV. 3

Switched Power

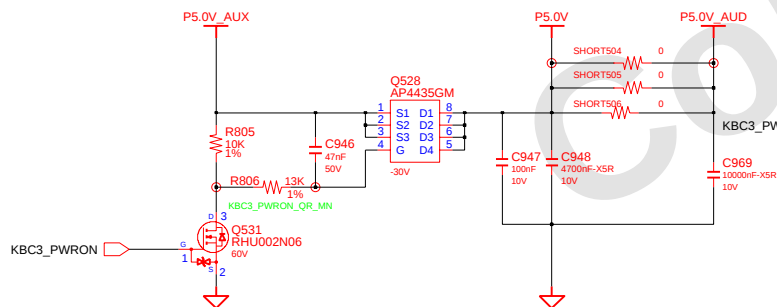
Switched Power On (P3.3V)



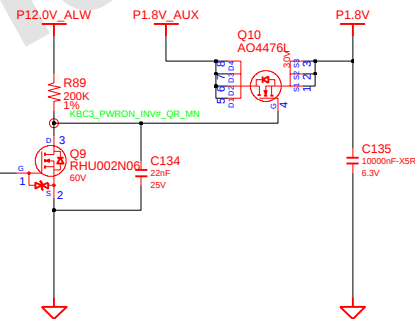
P2.5V



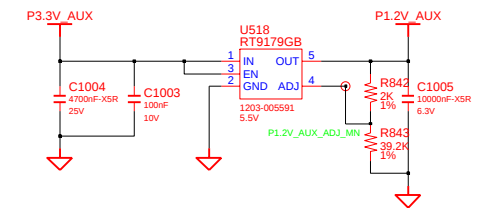
Switched Power On (P5.0V)



Switched Power On (P1.8V)

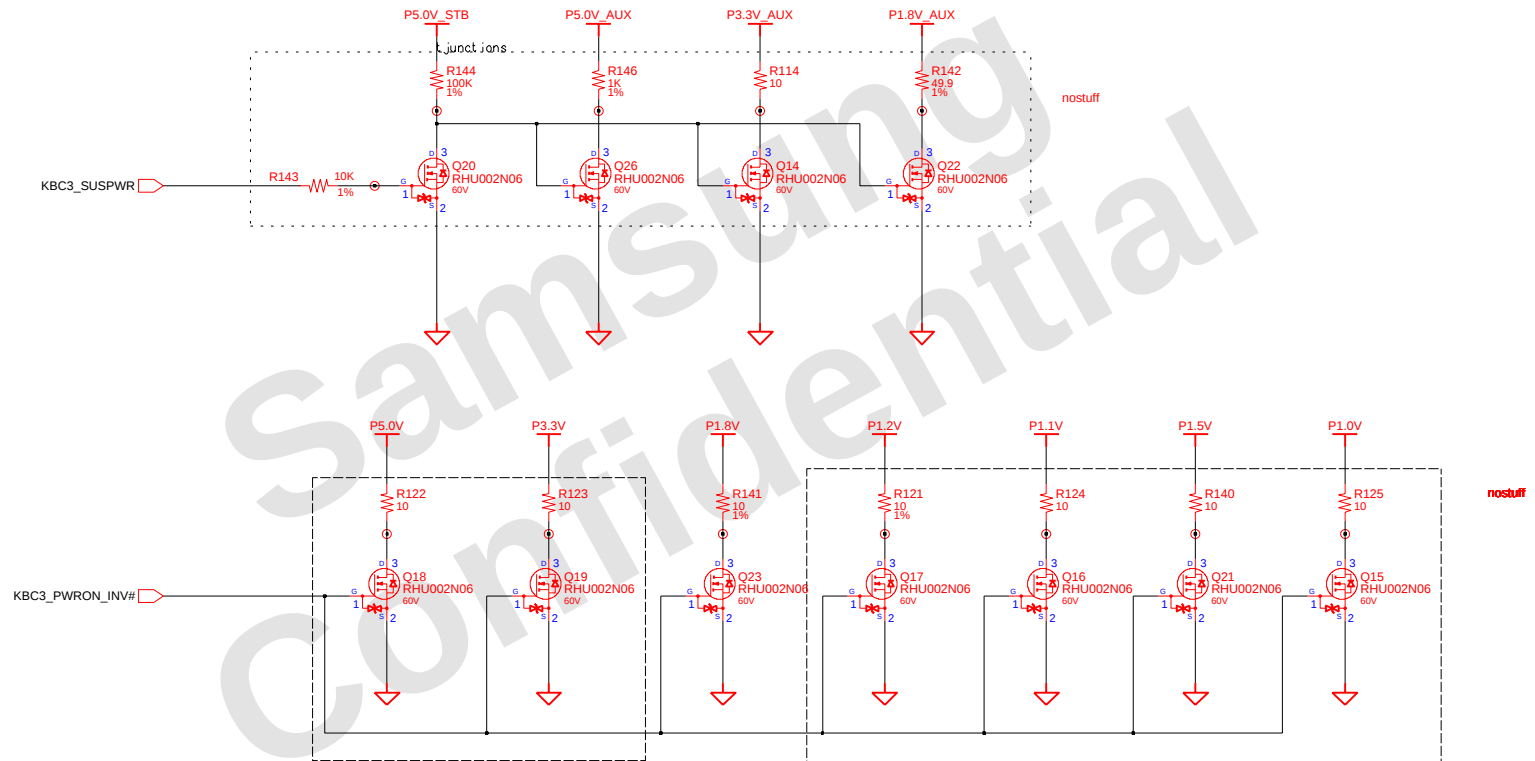


P1.2V_AUX



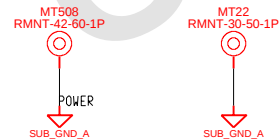
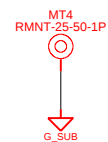
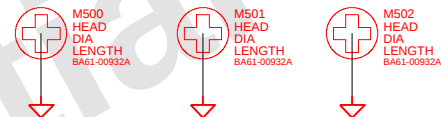
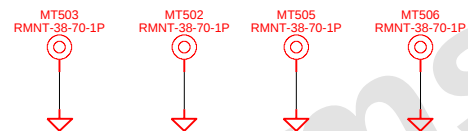
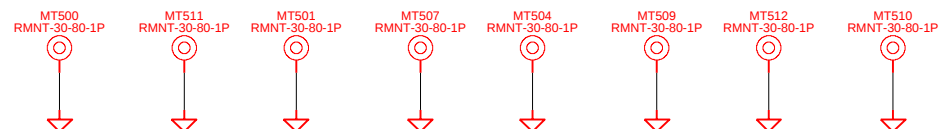
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	PWR_SWITCH		
APPROVAL	BC LEE	REV	0.1	SWITCH POWER		
MODULE CODE		LAST EDIT				
					July 15, 2009 19:25:13 PM	PAGE 54 OF 58

POWER DISCHARGER



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxxA
CHECK	GUO LEI	DEV. STEP	ADV	PWR_CPU_MV_IDISCHARGER		
APPROVAL	BC LEE	REV	0.1	DISCHARGER LOGIC		
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE 55 OF 58		

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DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D MAIN MOUNT HOLE	
CHECK	GUO LEI	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	0.1		
PART NO. BA41-xxxxxxA					
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 56 OF 58

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- ☐ CHGVR_EN_MN
- ☐ CHP3_GPIO16
- ☐ CHP3_GPIO17
- ☐ CHP3_RTCCLK
- ☐ CHP3_SERIRQ
- ☐ CHP3_SLPS3#
- ☐ CHP3_SLPS5#
- ☐ CK_PD#_R_MN
- ☐ CPU1_ALERT#
- ☐ CRT3_DDDCLK
- ☐ GFX_NC_B_MN
- ☐ KBC3_BKLTON
- ☐ KBC3_PRECHG
- ☐ KBC3_PWRSW#
- ☐ KBC3_RFOFF#
- ☐ KBC3_SCLED#
- ☐ KBC3_SMCLK#
- ☐ KBC3_SPI_DI
- ☐ KBC3_SPI_DO
- ☐ KBC5_KSI(0)
- ☐ KBC5_KSI(1)
- ☐ KBC5_KSI(2)
- ☐ KBC5_KSI(3)
- ☐ KBC5_KSI(4)
- ☐ KBC5_KSI(5)
- ☐ KBC5_KSI(6)

KBC5_KSI(7)
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KBC5_KSQ(8)
KBC5_KSQ(9)
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LPC3_LAD(2)
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BAT3_DETECT#
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CHGVR_CSIP_MN
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CPU1_LDTRSTP#
CPU1_DDCDATA_MN
EXPFXR_VO_MN
EGXPV_CLKREQ#
KBC3_BATDET#
KBC3_CHGA2V_MN
KBC3_CHGMIB#
KBC3_NUMLED#
KBC3_PWRBTN#
KBC3_RSMRST#
KBC3_RSTNC#
KBC3_TEMP#
KBC3_SPI_CLK
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KBC5_KSQ(11)
KBC5_KSQ(12)
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LD3_LFPRQ#
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MCDD3_SDDATA4
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MCDD3_EXTSTS1#
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CHGVR_RDY_MN
CHGVR_WDOP_MN
CHGVR_VDDP_MN
CHP3_NE_PWRGR#
CHP3_SALED#F#
CHP3_TEST0#
CHP3_SE_TEST2
CHP3_SUUSTAT#
CPU1_VDDIO_FB#
CPU1_VDDNB_FB#
CPU1_CFGSENSE#
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 PMS_SYSVR_TG1_MN
 PMS_SYSVR_TG2_MN
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 SDI_DCCL_SDA_R,M
 TH_SHDN_SCL_R,M
 WLON_LED_LED_MN
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 CHGVR_VCOMP_RC,M
 CPUF_TEST25_H_R,M
 CPUF_TEST25_L_R,M
 CPUF_CLKTESTA_C,M
 GFCR_CPK_CPD_R,M
 GFCR_TESTEN_2_R,M
 KBC3_TSEN_SMDATA
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 PMS_EGFCVR_BST_MN
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 GFCF_DPA0_CAL_R,M
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 GFCF_DPLD_VDD0_B,M
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 CHESVR_P12V_FB_MN
 CHESVR_P12V_VREF_MN
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 CHESVR_P12V_OSCET_MN
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 CHESVR_P11V_PG00D_MN
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 CHGVR_P33V_MICOM_RQ_MM
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 G. REF_A_SEL_HTTG6_R_MM
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 A2VDDQ
 CPU0_CORE
 CPU0_CORE
 DPC_PVD0
 DPC_PVD0
 DPC_VDD18
 G. CHG
 G. CPU
 G. DDR
 G. DDP
 G. SUB
 G. EGFX
 G. P11V
 G. P12V
 G. P15V
 G. P15V
 G. P33V
 LCD_VDD3V
 P25V
 P25V_AUX
 P12V_AUX
 P12V_LAN
 P18V_AUX
 P20V_REF
 P23V_LAN
 P33V_LED
 P33V_LED
 UDD_LED
 P33V_MCD
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 P50V_AUX
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 VDDC
 VDD01DI
 VDD01DI
 VCC_CRT

○ VCC_CRT
○ VDD_LED

DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D Test Point		
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1			
MODULE CODE		LAST EDIT			July 15, 2009 19:25:13 PM	PAGE 57 OF 58