

BONN-E/BONN-C

CPU : Intel Penryn
Chip Set : PM45 & ICH9M
Graphic : M96/M92/gDDR3 1g bit
Remarks : Montevina Platform

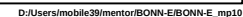
Model Name : BONN-E/BONN-C
PBA Name : MAIN
PCB Code : GCE : BA41-01060A
 NAN : BA41-01061A
 HAN : BA41-01062A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2009.04.11

Design	CHECK	APPROVAL

Owner : SEC Mobile R & D Signature : X

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DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	MAIN	COVER	ELECTRONICS
APPROVAL	BL Lee	REV	REV 1.0			PART NO. BA41-01060A
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	1	OF 67



BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

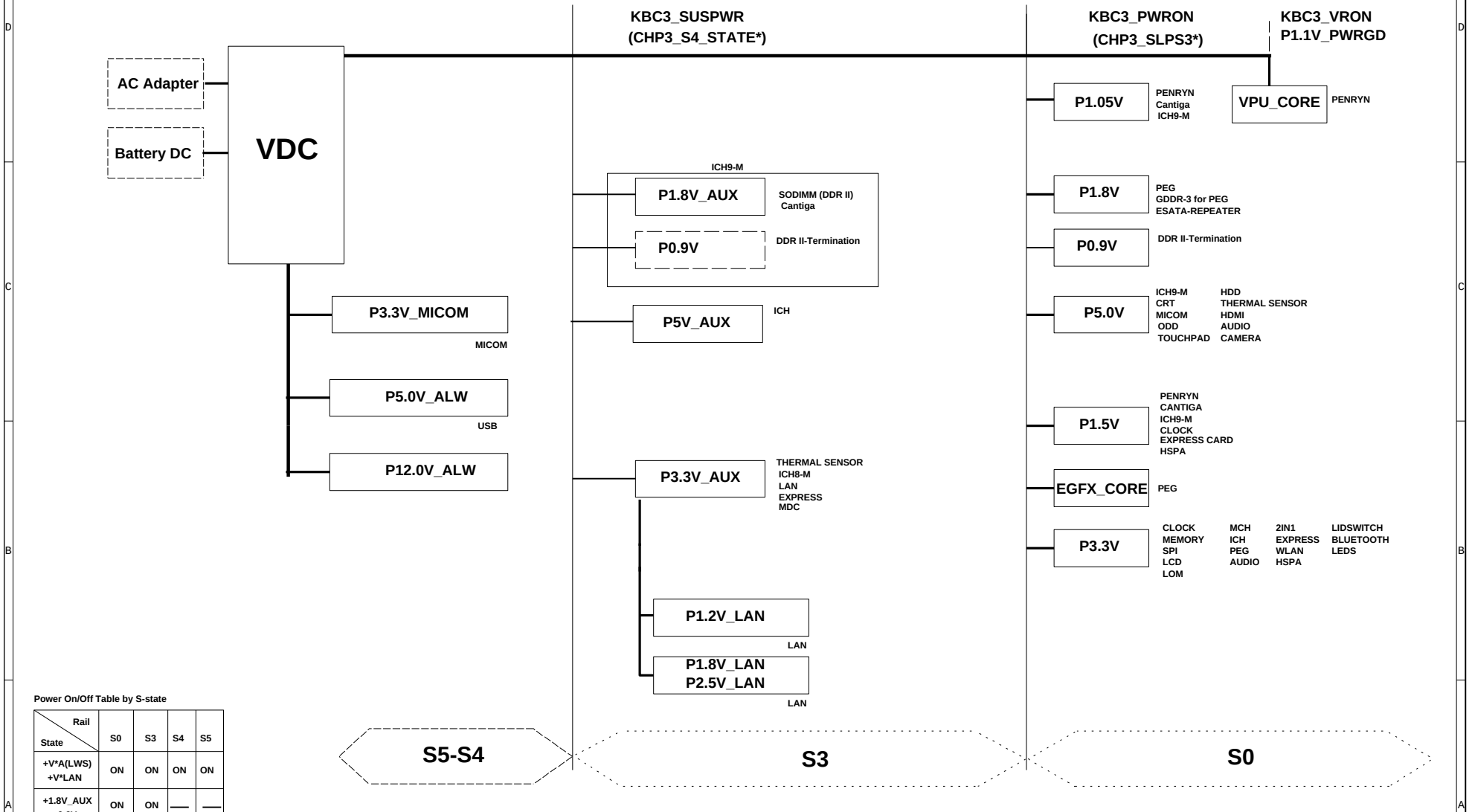
REVISION HISTORY

See rev notes for more information.

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	NC
1	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
2	SYSTEM PORT 2	2	NC
3	NC	3	LOM
4	NC	4	Mini Card 2 (ROBSON or DVB-T)
5	Bluetooth	5	NC
6	Mini PCI Express 2		
7	Camera		
8	NC		
9	NC		

DRAW	MS Yang	DATE	12/05/2008	BONN-E MAIN BOARD INFO	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP		
APPROVAL	BL Lee	REV	REV 1.0		
MODULE CODE	undefined	LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	3 OF 67

POWER DIAGRAM



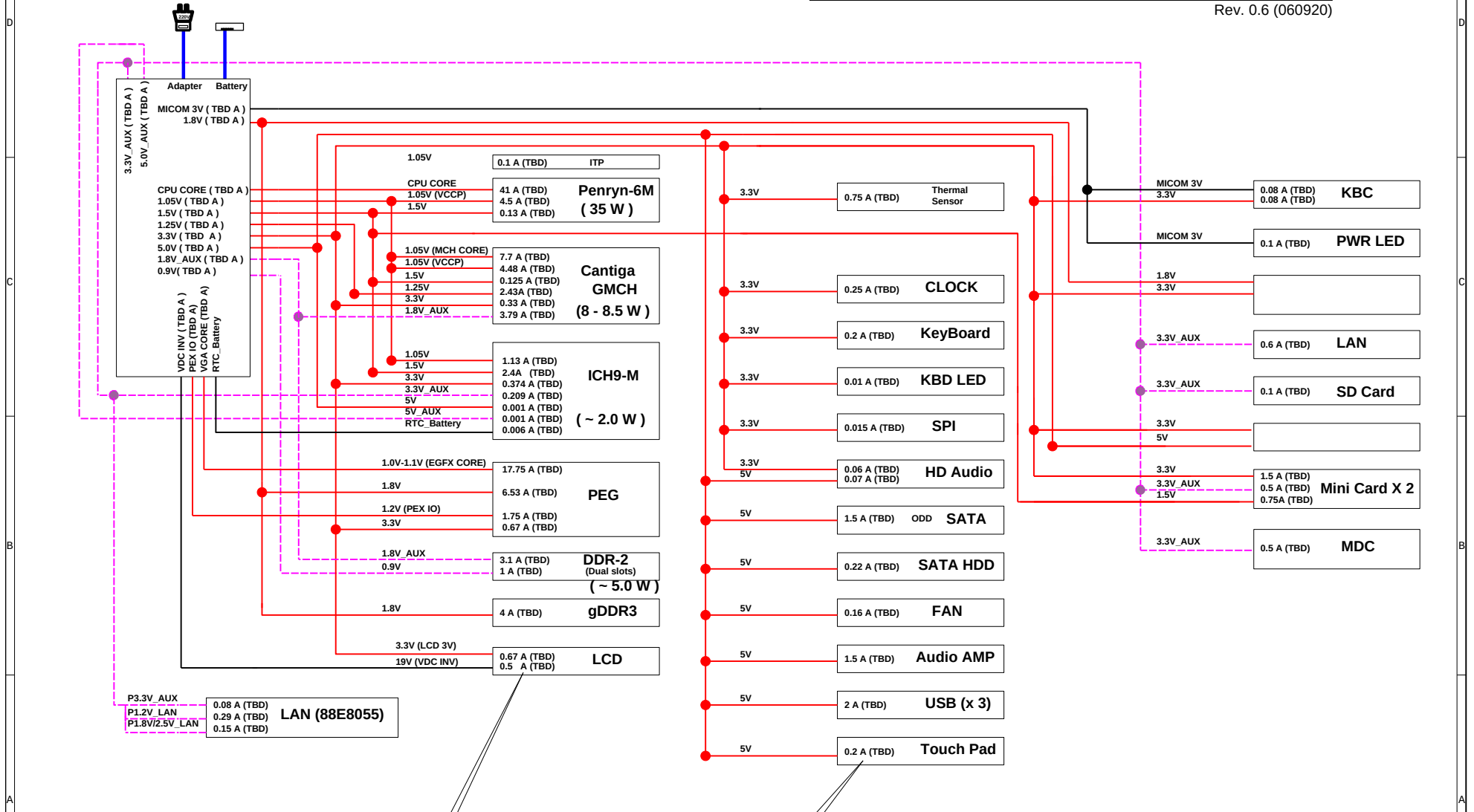
Power On/Off Table by S-state

Rail	S0	S3	S4	S5
+V*A(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	—	—
+1.8V_AUX	ON	ON	—	—
+0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E MAIN	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP			
APPROVAL	BL Lee	REV	REV 1.0		POWER DIAGRAM	PART NO. BA41-01060A
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POWER RAILS ANALYSIS

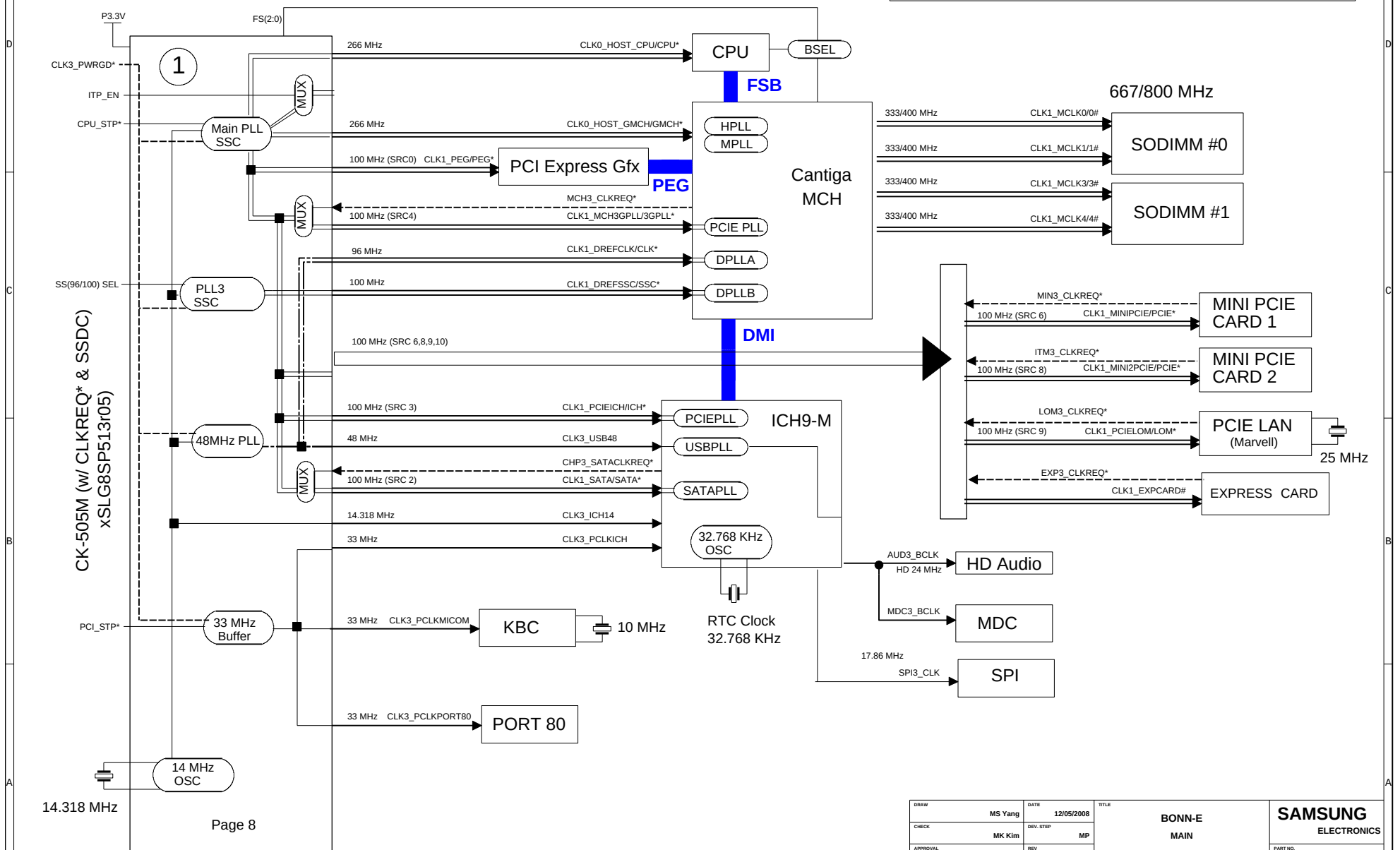
Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E MAIN POWER RAILS	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP			
APPROVAL	BL Lee	REV	REV 1.0			
MODULE CODE	undefined	LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	5	OF 67

CLOCK DISTRIBUTION Rev. 0.1

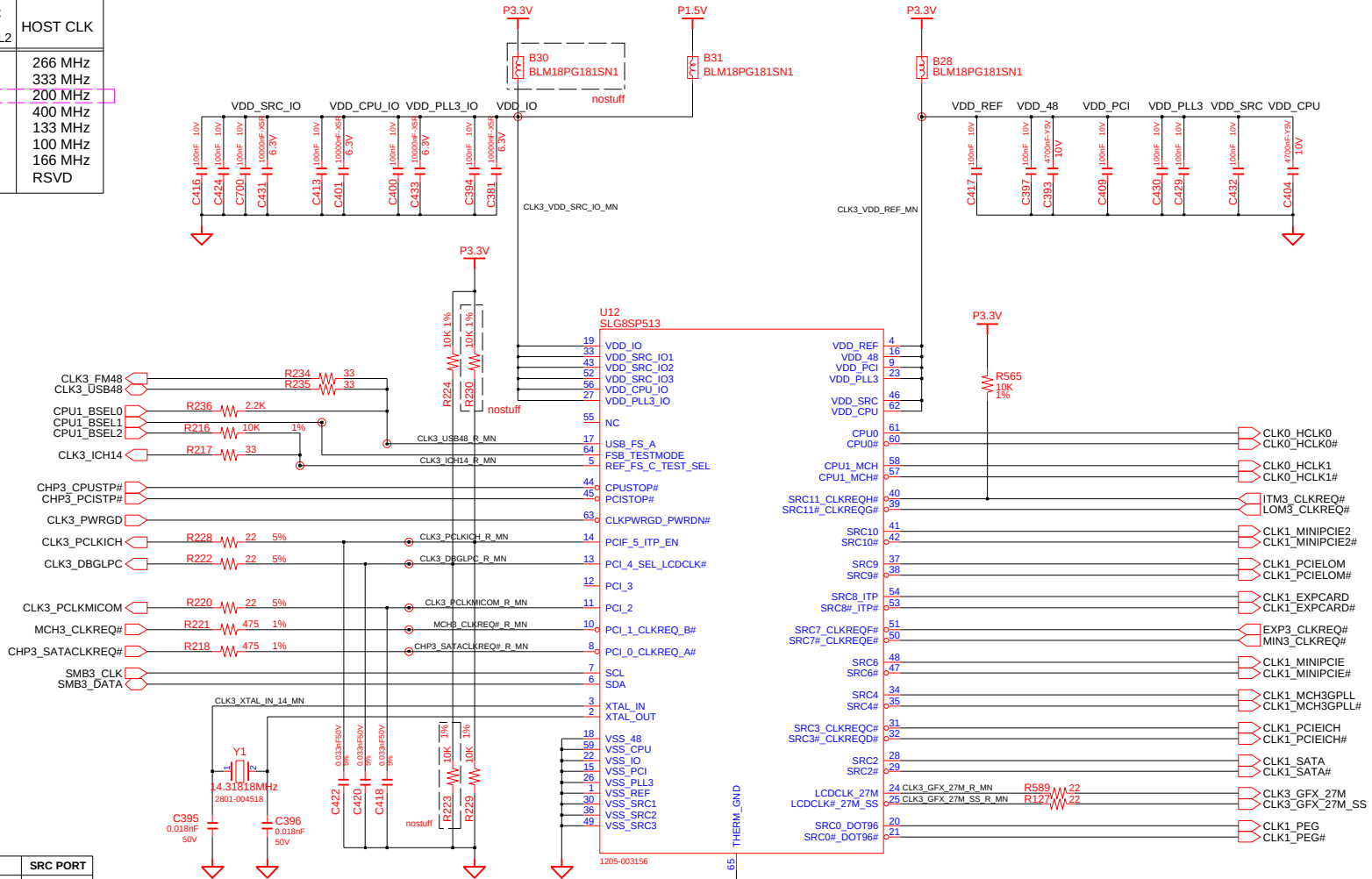


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CK505M

FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

Place 14.318MHz within
 500mils of CK-505

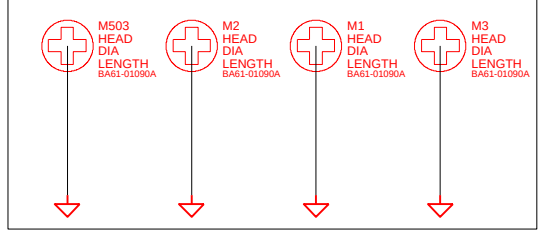
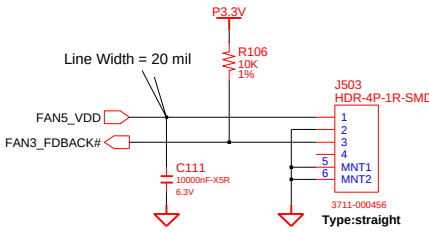
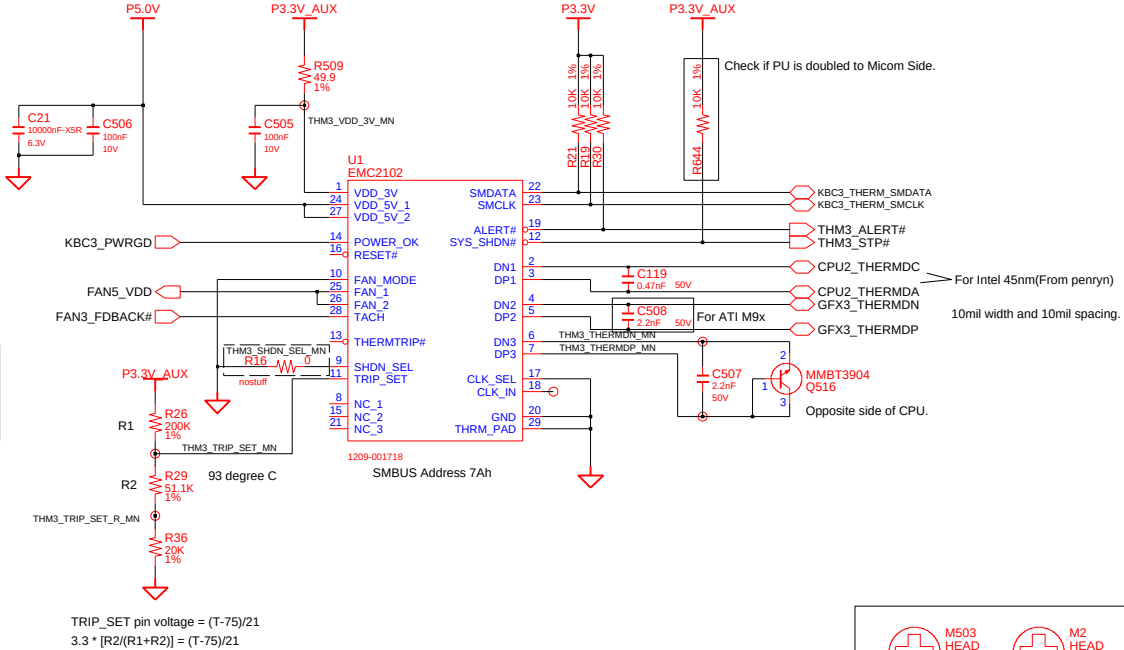
This part is 64pin QFN package.

IDT : 1205-003159
 SL : 1205-003533

DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	DEV. STEP	MP	MAIN_CLOCK_CIRCUIT	CK_Clock_505M	ELECTRONICS
APPROVAL	BL Lee	REV	REV 1.0			PART NO.
MODULE CODE	undefined	LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	8	OF 67

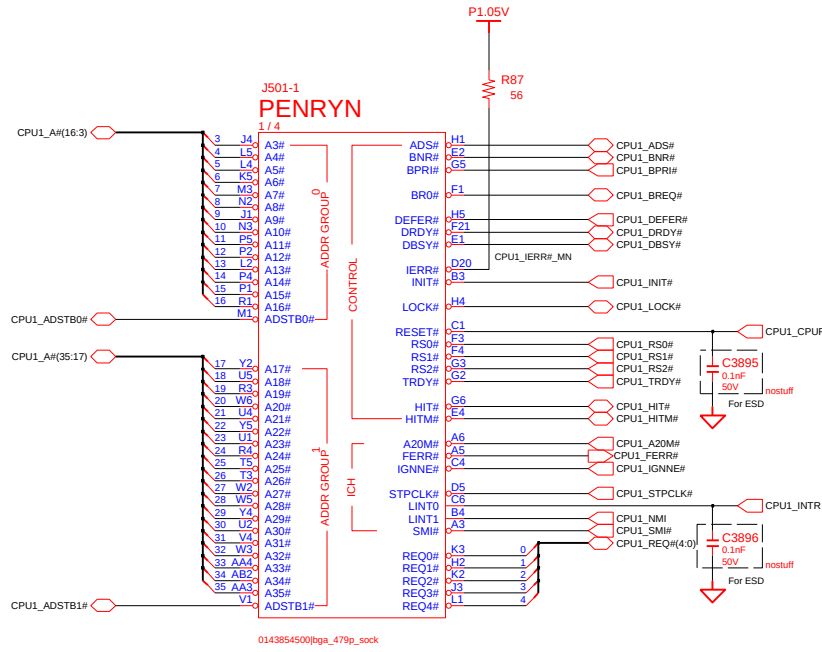
THERMAL SENSOR & FAN CONTROL

SHDN_SEL MODE	
0	CH1(INTEL MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

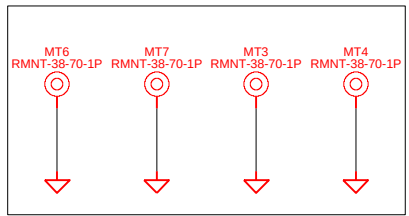


To support heatsink

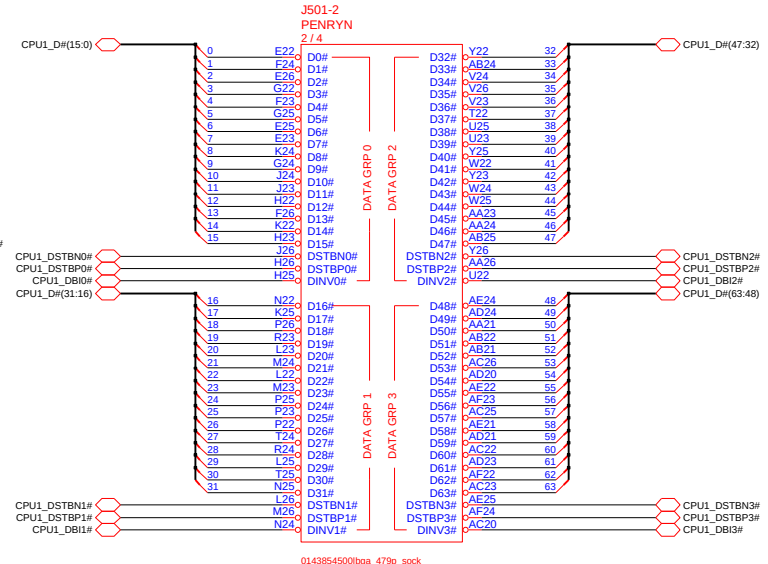
DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	THERMAL SENSOR	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	THERMAL SENSOR EMC2102	PART NO.	BA41-01060A
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	9	OF 67



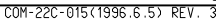
CPU Socket : 3704-001153



CPU mount



DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	REV. STEP	MP		CPU	ELECTRONICS	
APPROVAL	BL Lee	REV 1.0		PENRYN (1/3)	PART NO.	BA41-01060A
MODULE CODE	undefined	LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	10	OF 67



*Yonah Processor (2.33 GHz / 800 MHz : TBD)

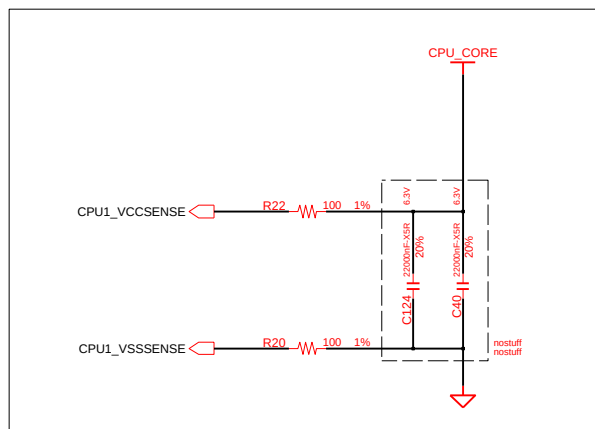
GND test points within 100mil of the VCC/VSSense at the end of the line. Route the VCC/VSSense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

		Pull-down
FSB 1067 MHz FSB 800 MHz		BSEL0, BSEL1, BSEL2 BSEL0, BSEL2

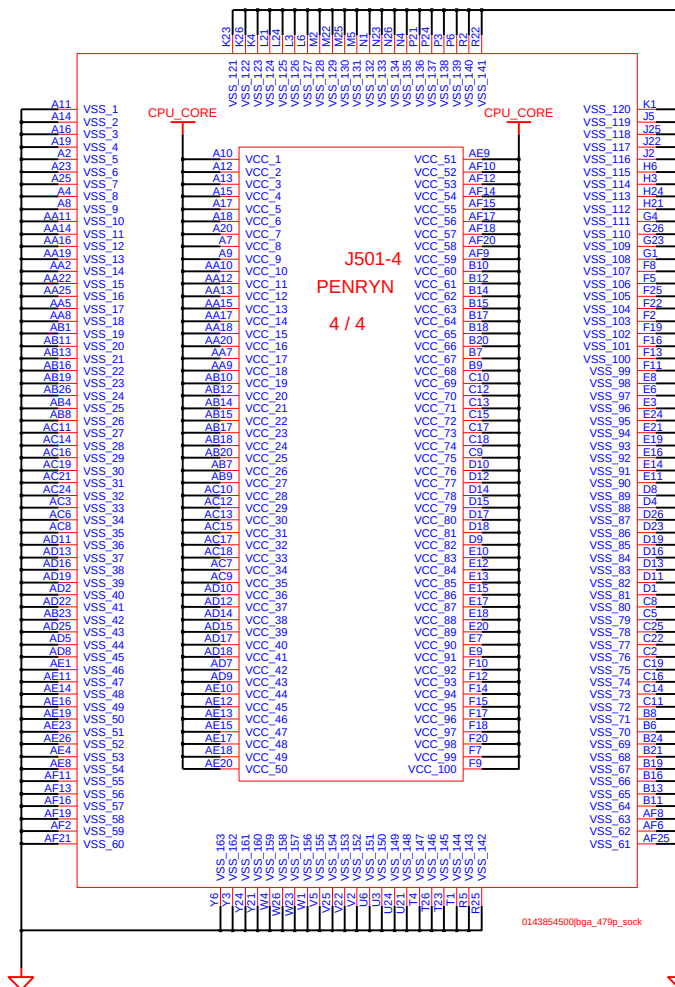
D:/Users/mobile39/mentor/BONN-E/BONN-E mp10

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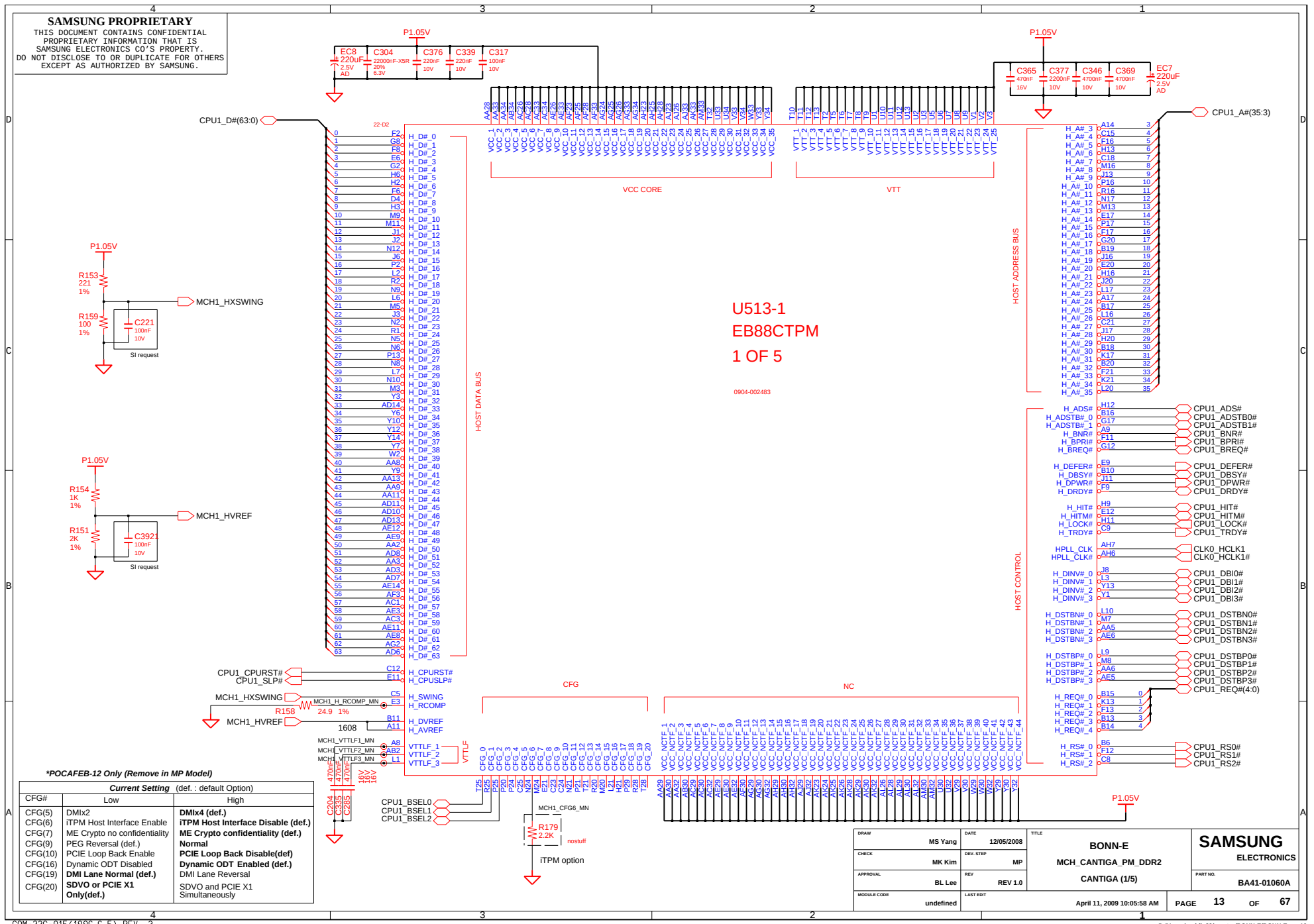


Prodizer used



DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP	CPU		
APPROVAL	BL Lee	REV	REV 1.0	PENRYN (3/3)	PART NO.	
MODULE CODE	undefined	LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	12 OF 67	

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D:/Users/mobile39/mentor/BONN-E/BONN-E mp1

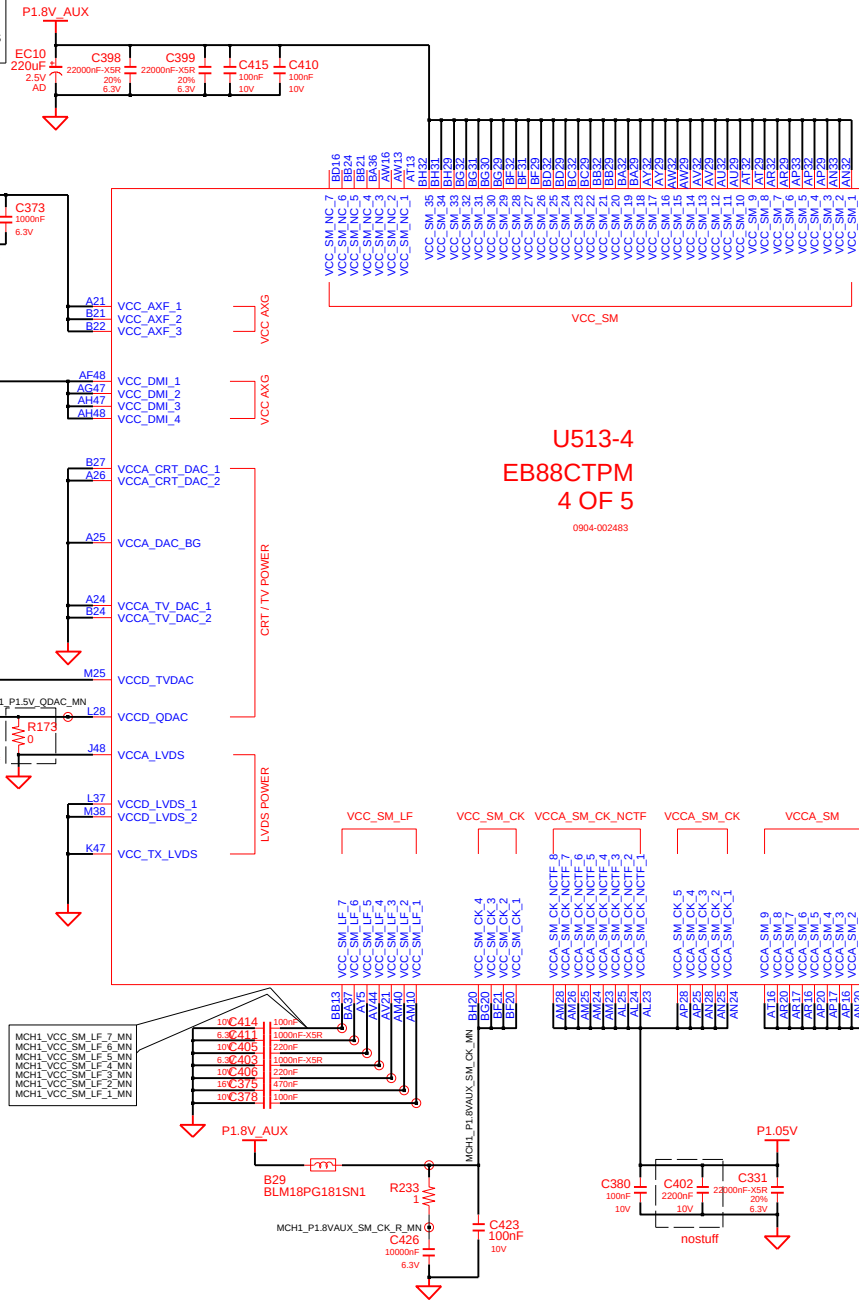
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D

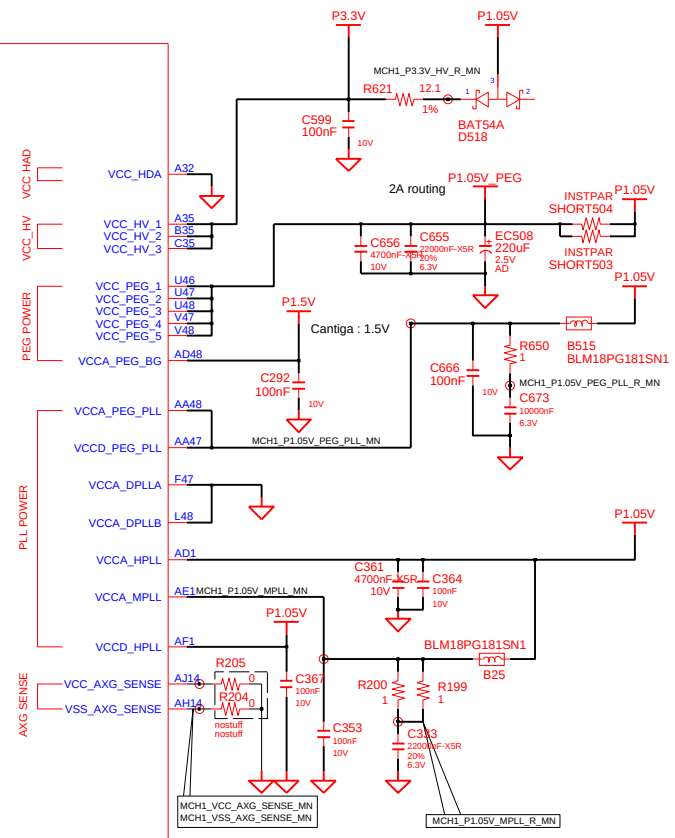
C

B

A

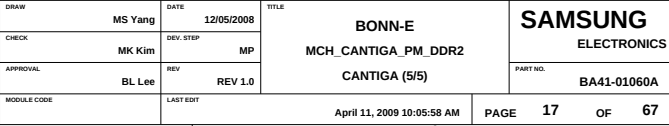


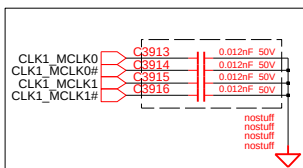
U513-4
EB88CTPM
4 OF 5
0904-002483



DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP		MCH_CANTIGA_PM_DDR2	
APPROVAL	BL Lee	REV	REV 1.0		CANTIGA (4/5)	
MODULE CODE		LAST EDIT				
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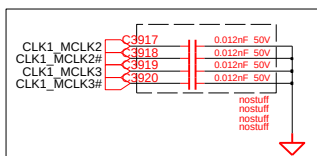
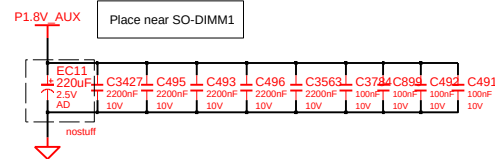
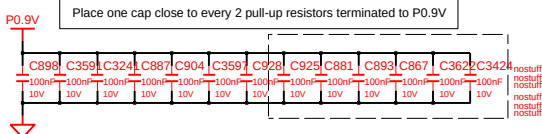
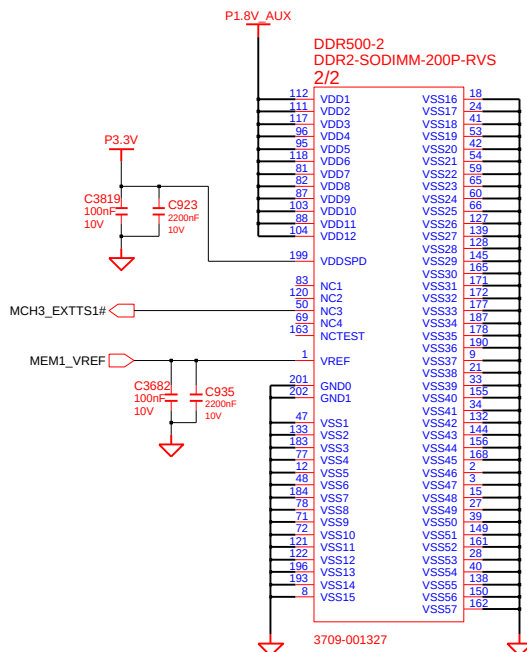
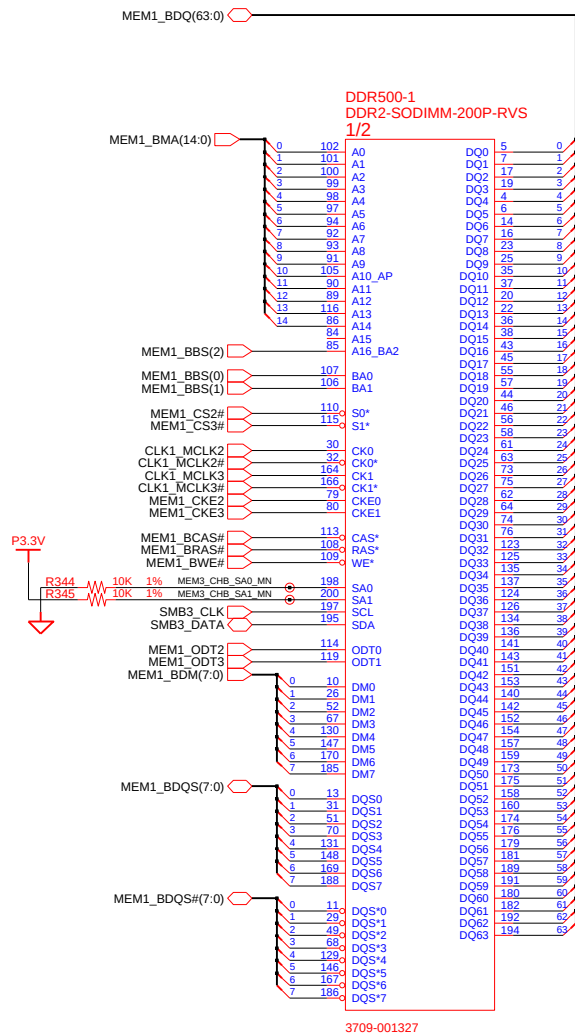




DRAW	MS Yang	DATE	12/05/2008	BONN-E SODIMM_DDR2 SODIMM_DDR2 #1	SAMSUNG ELECTRONICS
CHECK	MK Kim	DEV. STEP	MP		
APPROVAL	BL Lee	REV	REV 1.0		
MODULE CODE	LAST EDIT				
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					PART NO. BA41-01060A

Timing diagram for the R320-R333 memory array. The diagram shows data signals for MEM1_BMA[14:0], MEM1_CS2#, MEM1_CS3#, MEM1_CKE2, MEM1_CKE3, MEM1_ODT2, MEM1_ODT3, MEM1_BBS[0], MEM1_BBS[1], MEM1_BBS[2], MEM1_BCAS#, and MEM1_BRAS#. The signals are connected to a memory array with addresses 0 to 14. The array is connected to a 9V power supply (P0_9V). The signals are labeled with their respective memory addresses and values.

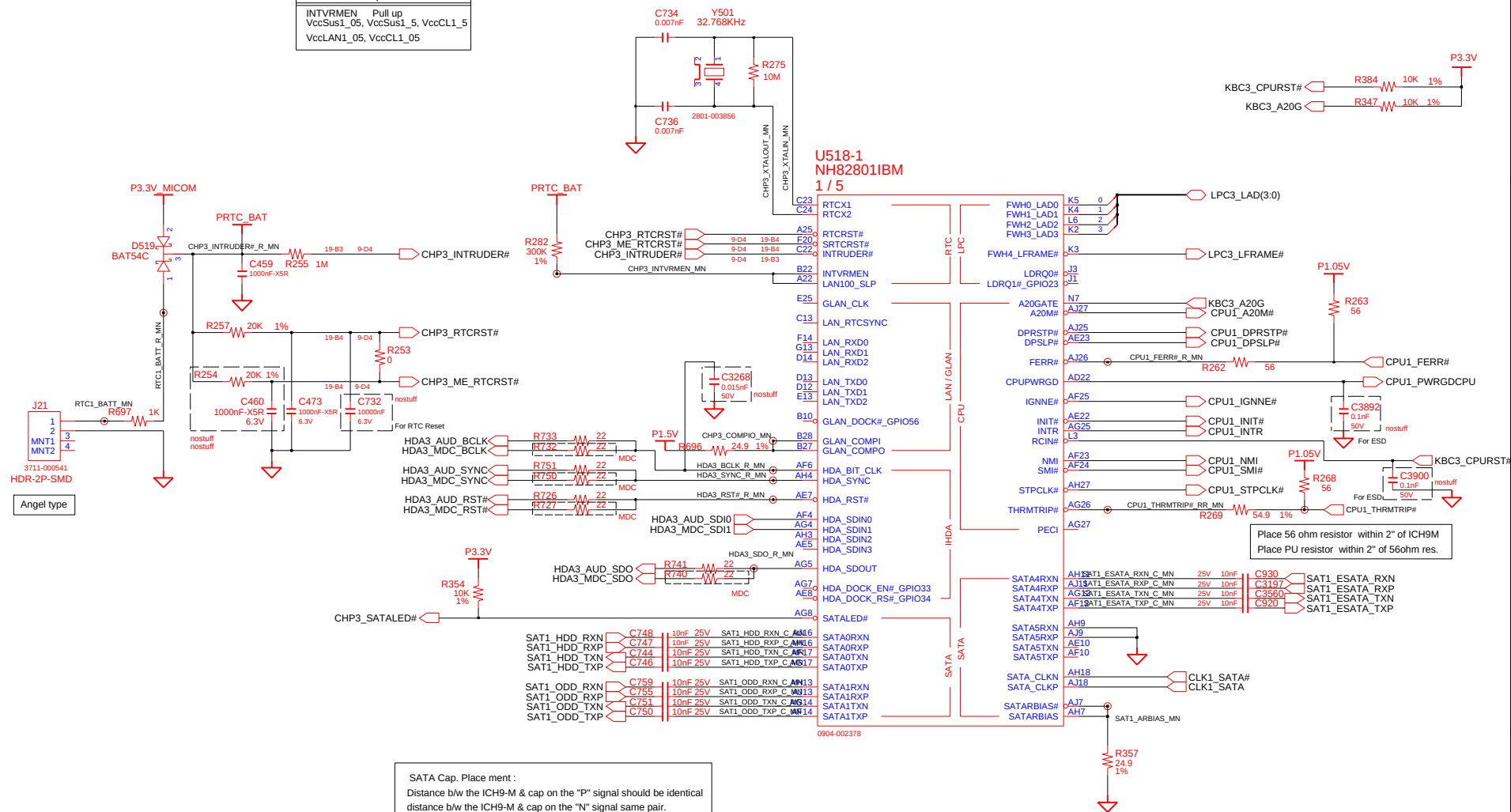
Signal	Address	Value
MEM1_BMA[14:0]	0	R338
MEM1_BMA[14:0]	1	R320
MEM1_BMA[14:0]	2	R337
MEM1_BMA[14:0]	3	R319
MEM1_BMA[14:0]	4	R336
MEM1_BMA[14:0]	5	R318
MEM1_BMA[14:0]	6	R334
MEM1_BMA[14:0]	7	R335
MEM1_BMA[14:0]	8	R317
MEM1_BMA[14:0]	9	R316
MEM1_BMA[14:0]	10	R322
MEM1_BMA[14:0]	11	R332
MEM1_BMA[14:0]	12	R315
MEM1_BMA[14:0]	13	R342
MEM1_BMA[14:0]	14	R333
MEM1_CS2#		R341
MEM1_CS3#		R325
MEM1_CKE2		R314
MEM1_CKE3		R313
MEM1_ODT2		R343
MEM1_ODT3		R326
MEM1_BBS[0]		R321
MEM1_BBS[1]		R339
MEM1_BBS[2]		R331
MEM1_BCAS#		R324
MEM1_BRAS#		R340
MEM1_RWE#		R323



EMC request

DRAW	MS Yang	DATE	12/05/2008	BONN-E SODIMM_DDR2 SODIMM_DDR2 #2	SAMSUNG ELECTRONICS
CHECK	MK Kim	DEV. STEP	MP		
APPROVAL	BL Lee	REV	REV 1.0		
PART NO.		BA41-01060A			
MODA.E CODE		LAST EDIT April 11, 2009 10:05:58 AM			PAGE 19
					OF 67

Internal VR Strap
INTVRMEN Pull up VccSus1_05, VccSus1_5, VccCL1_5 VccLAN1_05, VccCL1_05

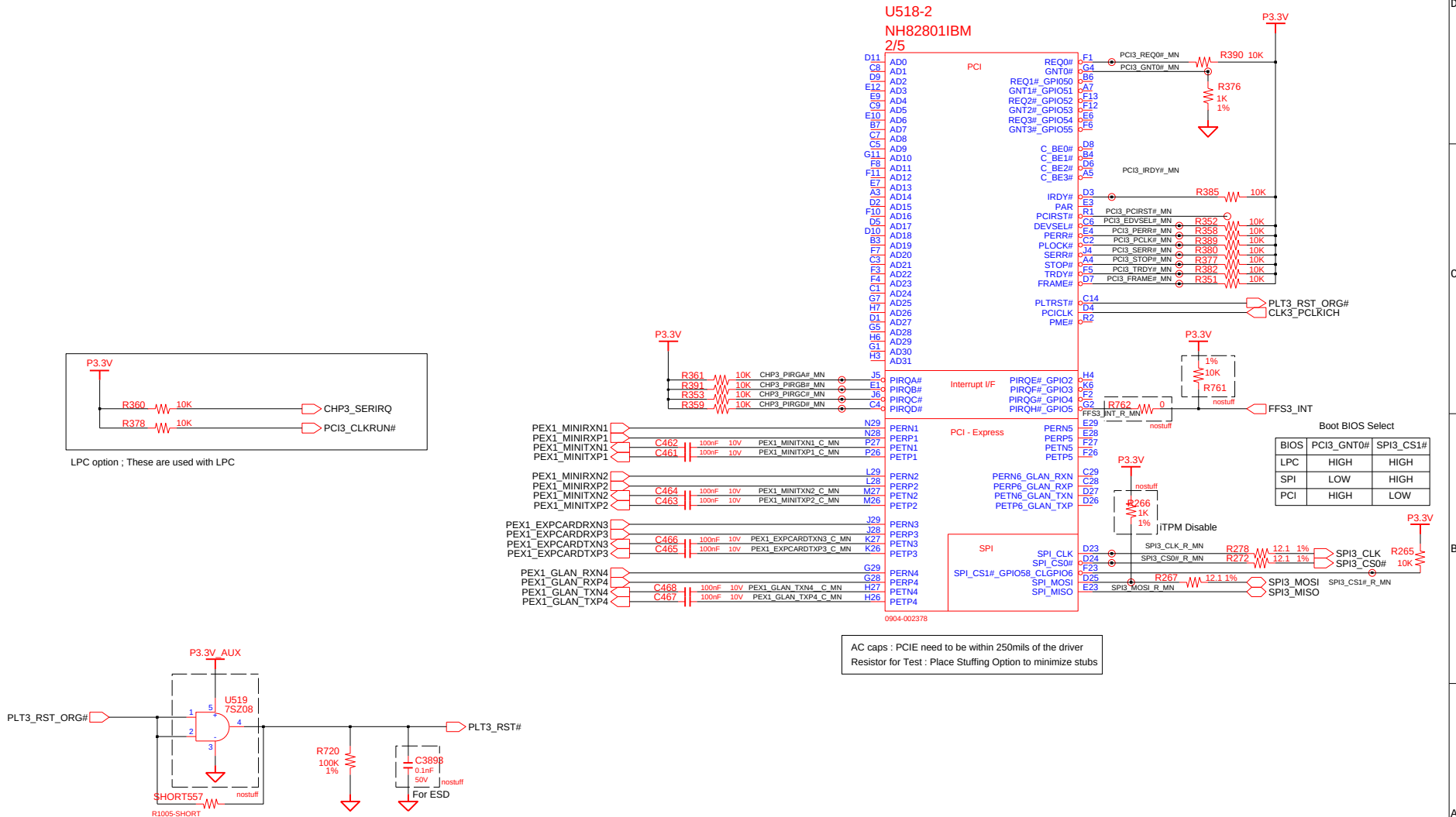


SATA Cap. Place ment :
Distance b/w the ICH9-M & cap on the "P" signal should be identical
distance b/w the ICH9-M & cap on the "N" signal same pair.

DRAW	MS Yang	DATE	12/05/2008	BONN-E ICH_9M_B ICH9-M (1/5)	SAMSUNG ELECTRONICS PART NO. BA41-01060A			
CHECK	MK Kim	DEV. STEP	MP					
APPROVAL	BL Lee	REV	REV 1.0					
MODULE CODE	LAST EDIT							
				April 11, 2009 10:05:58 AM	PAGE	20	OF	67

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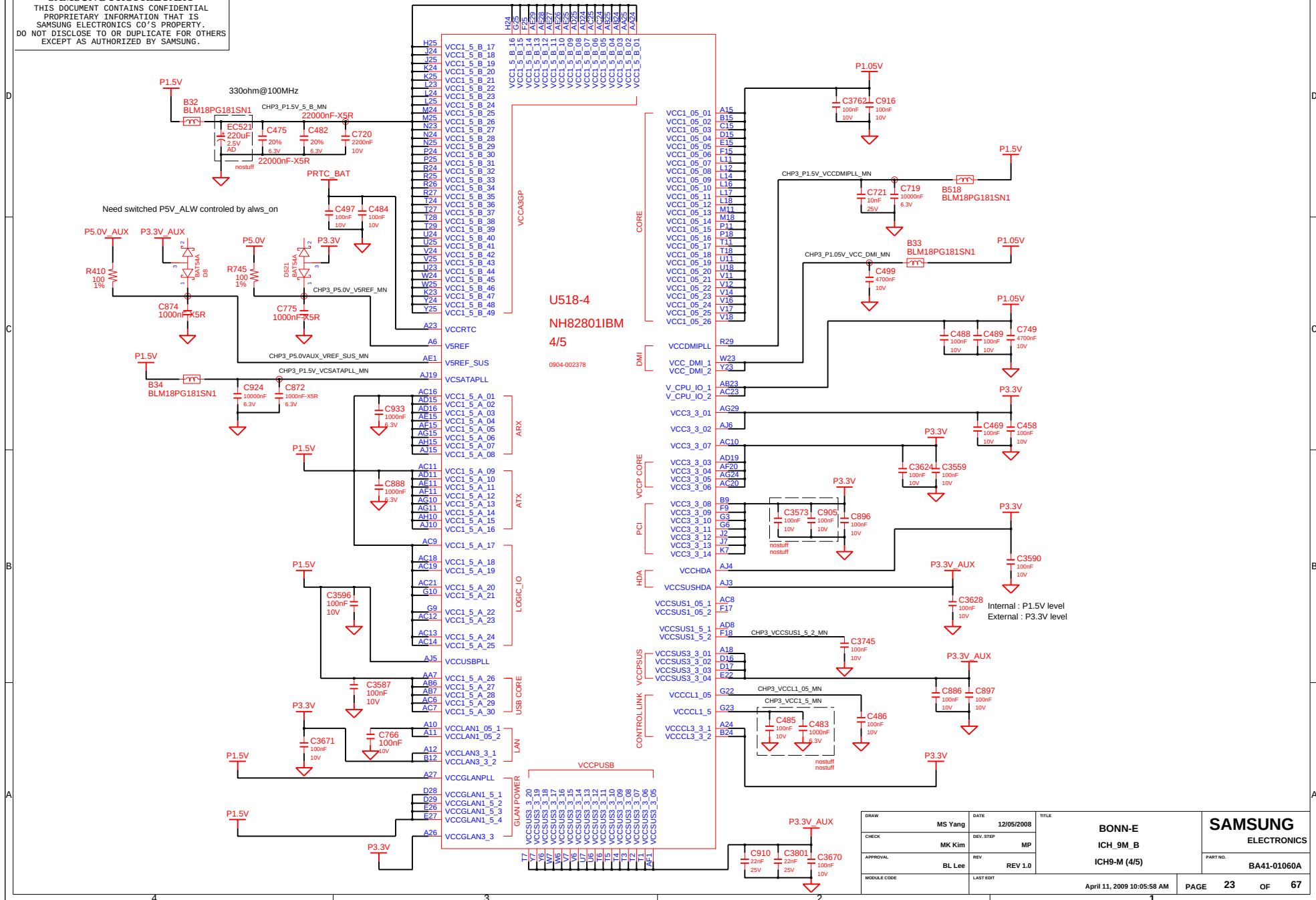
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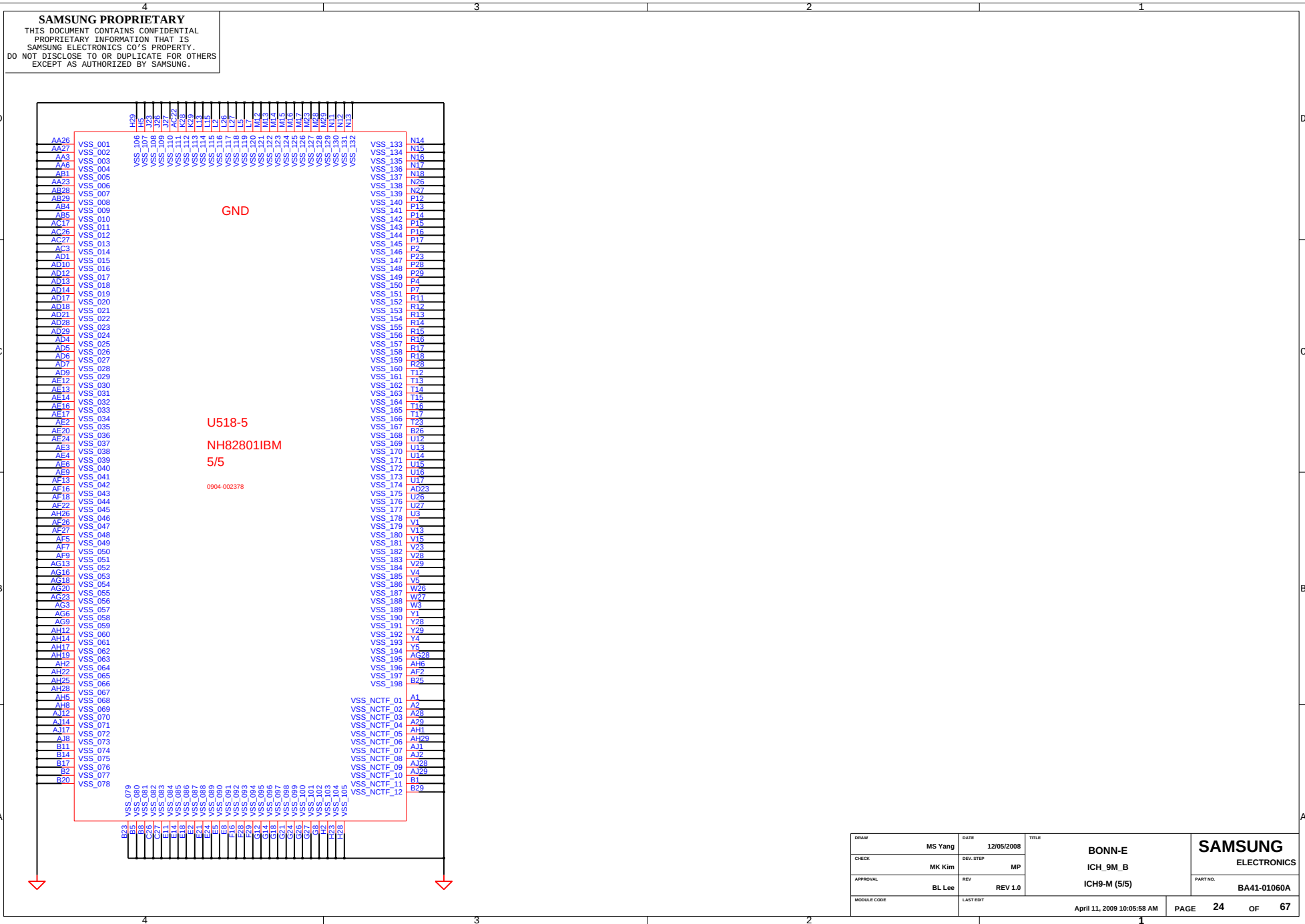


DRAW	MS Yang	DATE	12/05/2008	TITLE		BONN-E ICH_9M_B ICH9-M (2/5)		SAMSUNG ELECTRONICS	
CHECK	MP	DEV. STEP							
APPROVAL	REV	REV 1.0							
		BL Lee				PART NO.		BA41-01060A	
MODULE CODE		undefined		LAST EDIT		April 11, 2009 10:05:58 AM		PAGE	21 OF 67

High	No Woofer
Low	Sub-Woofer

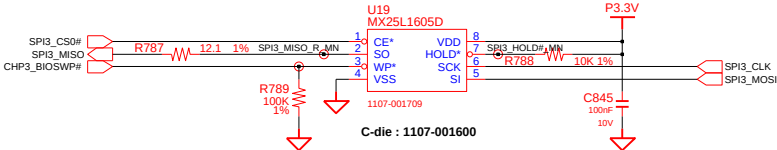






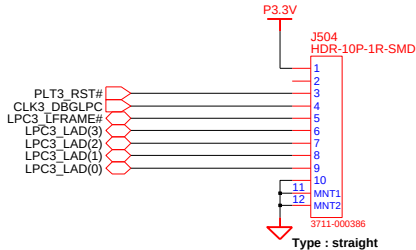
SPI_BIOS_ROM

16MBit



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
0A	SET IN POST LAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
WITH INITIAL POST VALUE		88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE HW INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D6	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D8	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	DA	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DC	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DE	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY * PRESS * SETUP *	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

80H DECODER CONNECTOR



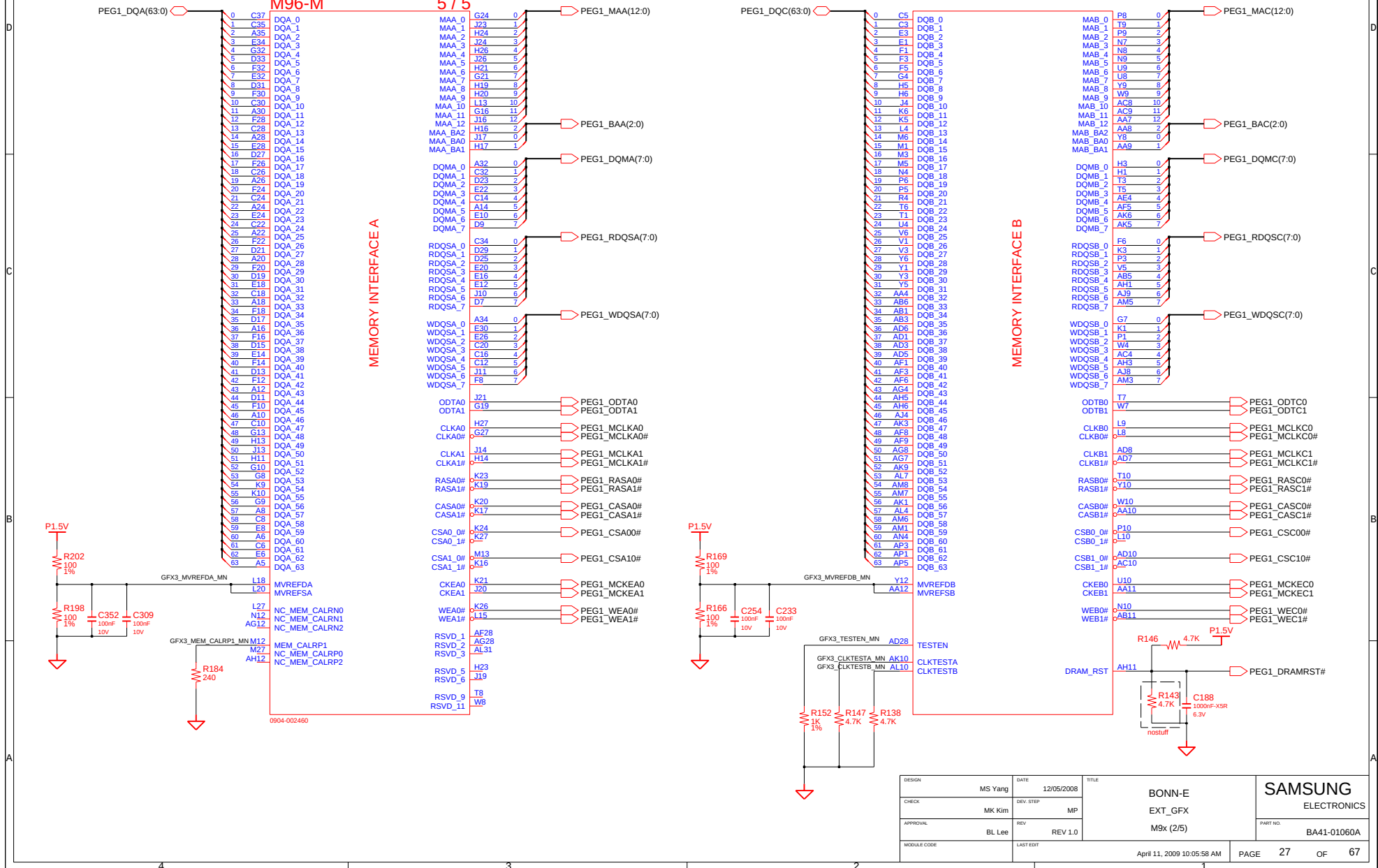
DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	SPI_BIOS_ROM	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	SPI_BIOS_ROM	PART NO.	BA41-01060A
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	25	OF 67

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U510-5
M96-M

5 / 5

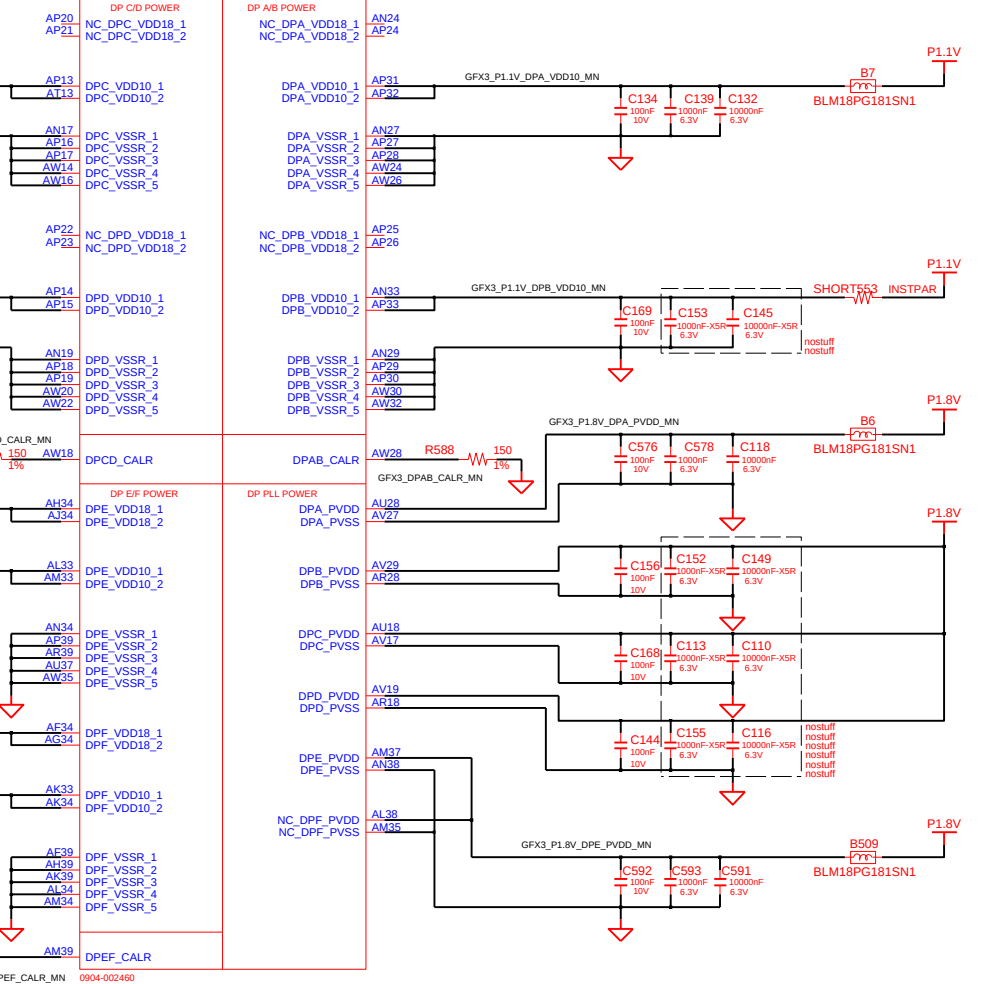
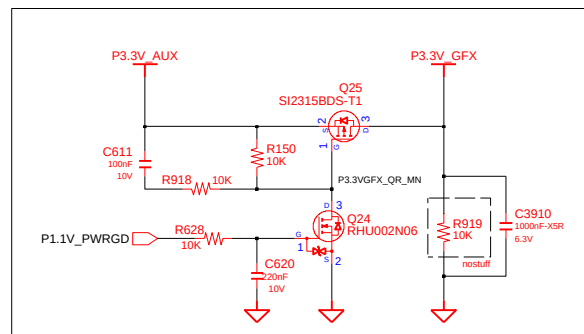


DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	EXT_GFX	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	M9x (2/5)	PART NO.	BA41-01060A
MODULE CODE		LAST EDIT			April 11, 2009 10:05:58 AM	PAGE 27 OF 67

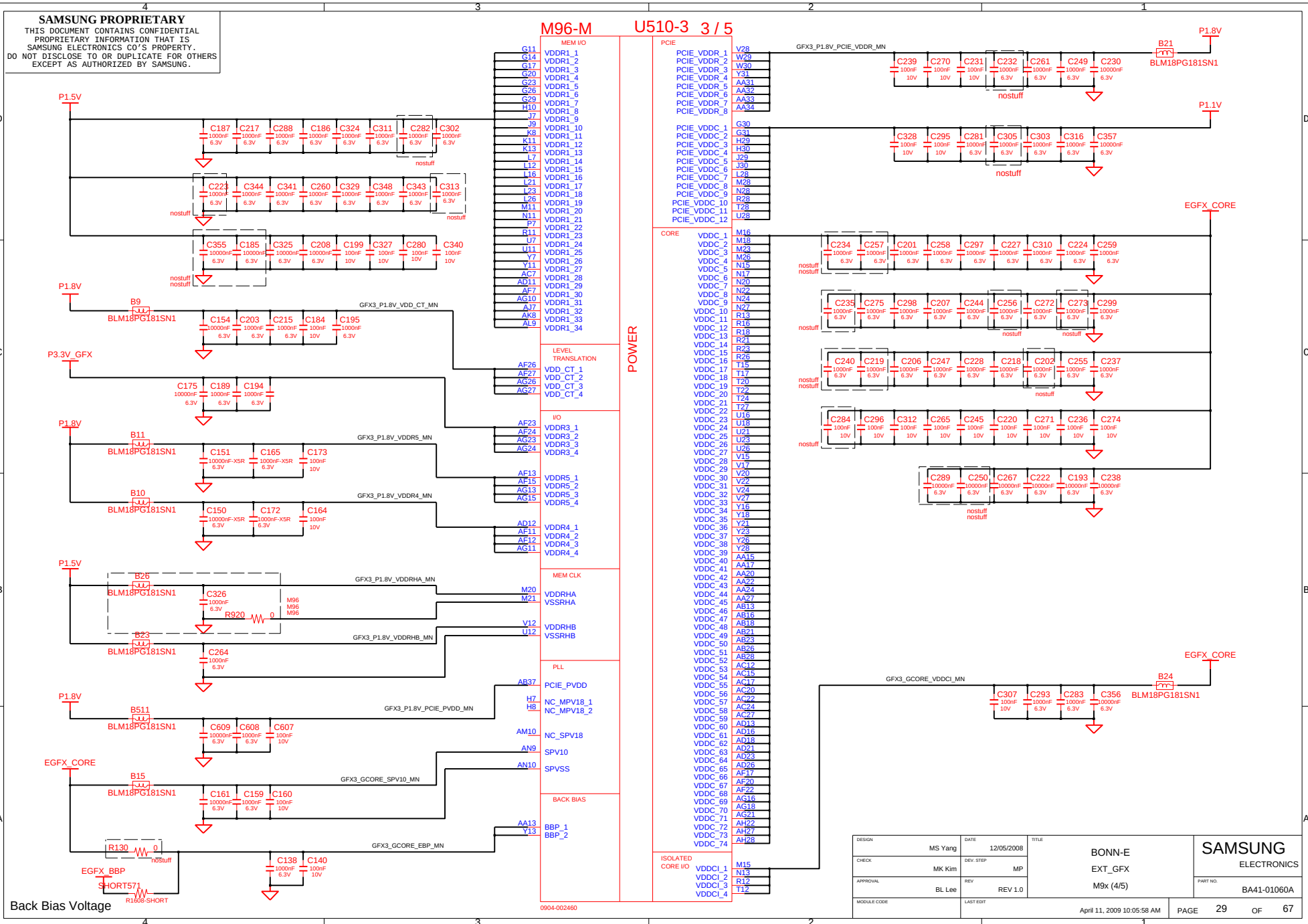
U510-4
M96-M

4 / 5

P3.3V_GFX CONTROL CIRCUIT



DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E EXT_GFX M9x (3/5)	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP			
APPROVAL	BL Lee	REV	REV 1.0			
MODULE CODE		LAST EDIT				
April 11, 2009 10:05:58 AM						PAGE 28 OF 67



4

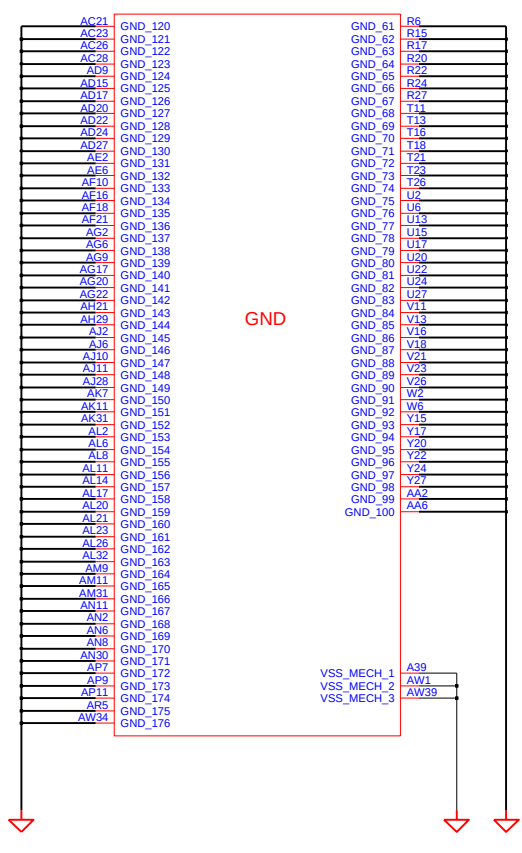
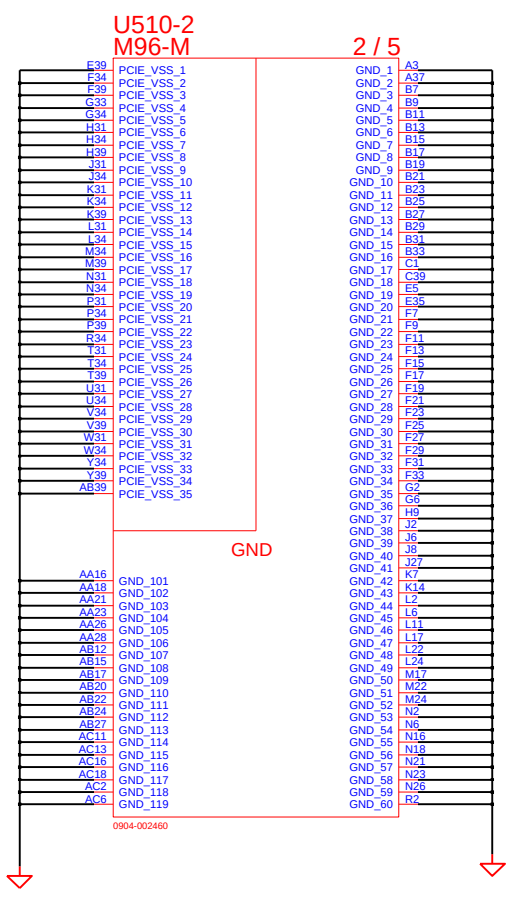
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D

C

B

A



D

C

B

A

DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP	EXT_GFX	PART NO.	
APPROVAL	BL Lee	REV	REV 1.0	M9x (5/5)	BA41-01060A	
MODULE CODE		LAST EDIT		April 11, 2009 10:05:58 AM	PAGE 30 OF 67	

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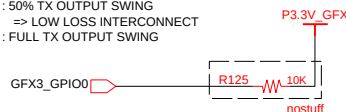
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M9X STRAPS

TX_PWRS_ENB

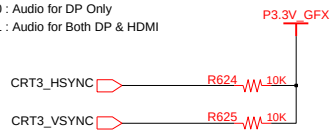
PCIE FULL TX OUTPUT SWING

0 : 50% TX OUTPUT SWING
=> LOW LOSS INTERCONNECT
1 : FULL TX OUTPUT SWING



AUD[1:0]

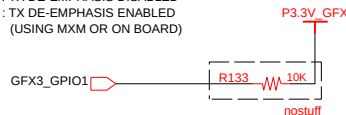
00 : No Audio Function
01 : Audio for DP & HDMI if adapter is detected
10 : Audio for DP Only
11 : Audio for Both DP & HDMI



TX_DEEMPH_EN

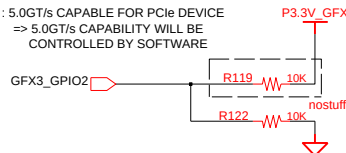
PCIE TRANSMITTER DE-EMPHASIS ENABLED

0 : TX DE-EMPHASIS DISABLED
1 : TX DE-EMPHASIS ENABLED
(USING MXM OR ON BOARD)



BIF_GEN2_EN_A

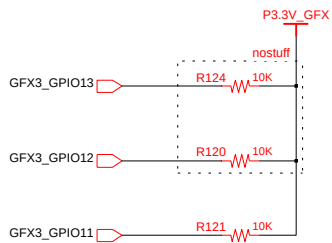
0 : 2.5GT/s CAPABLE FOR PCIe DEVICE
1 : 5.0GT/s CAPABLE FOR PCIe DEVICE
=> 5.0GT/s CAPABILITY WILL BE
CONTROLLED BY SOFTWARE



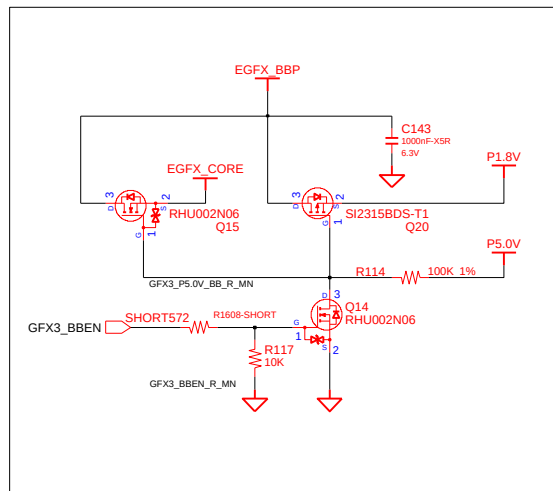
If BIOS_ROM_EN=1, ROMCFGID[2:0] (INTERNAL PULL DOWN)
If BIOS_ROM_EN=0, Memory Aperture Size

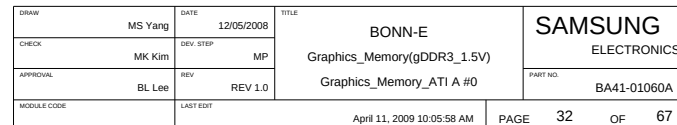
GFX3_GPIO(13 : 11)

000 : 128MB
001 : 256MB
010 : 64MB
011 : RESERVED
1XX : RESERVED

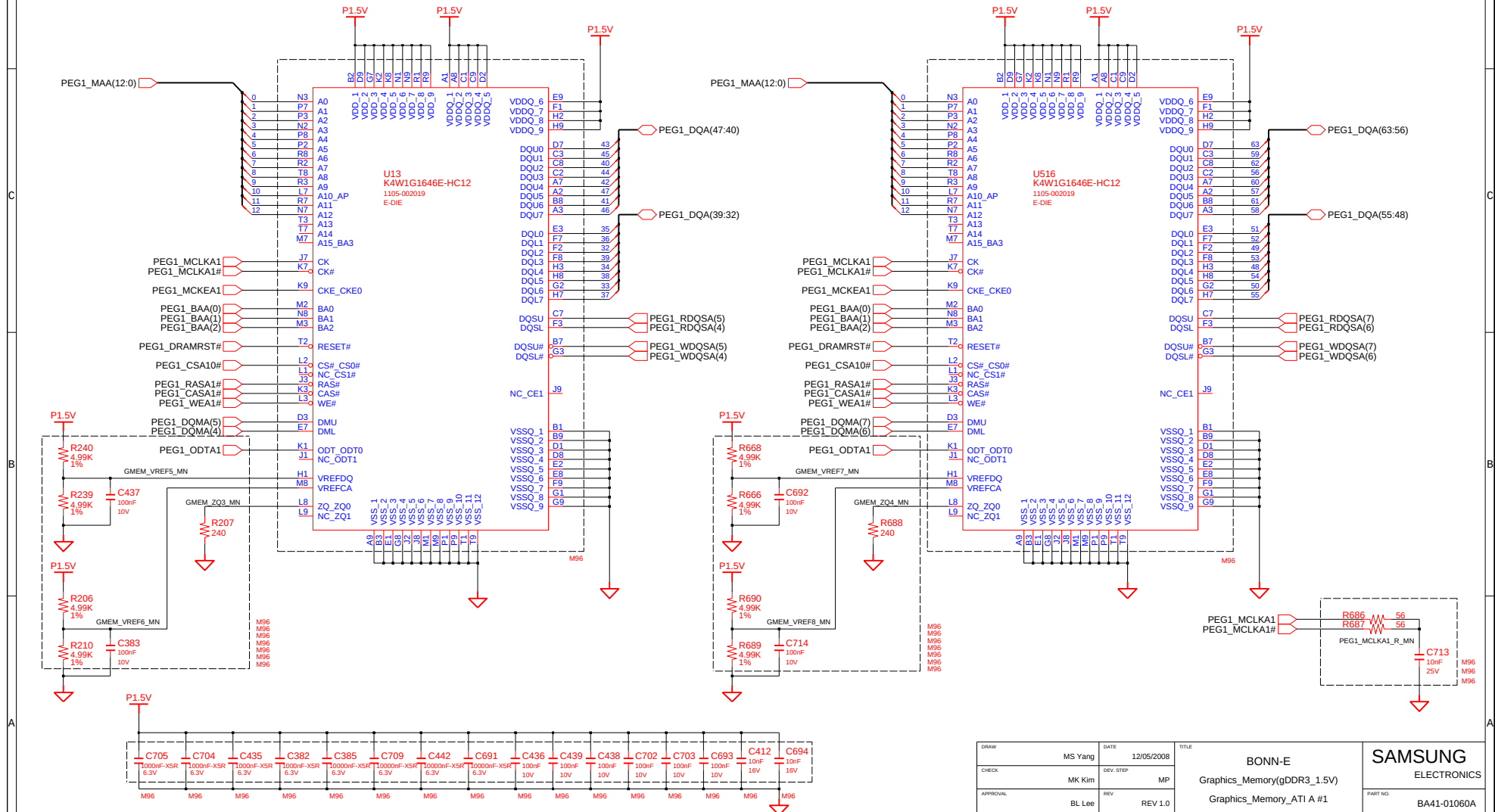


BACK BIAS LOGIC





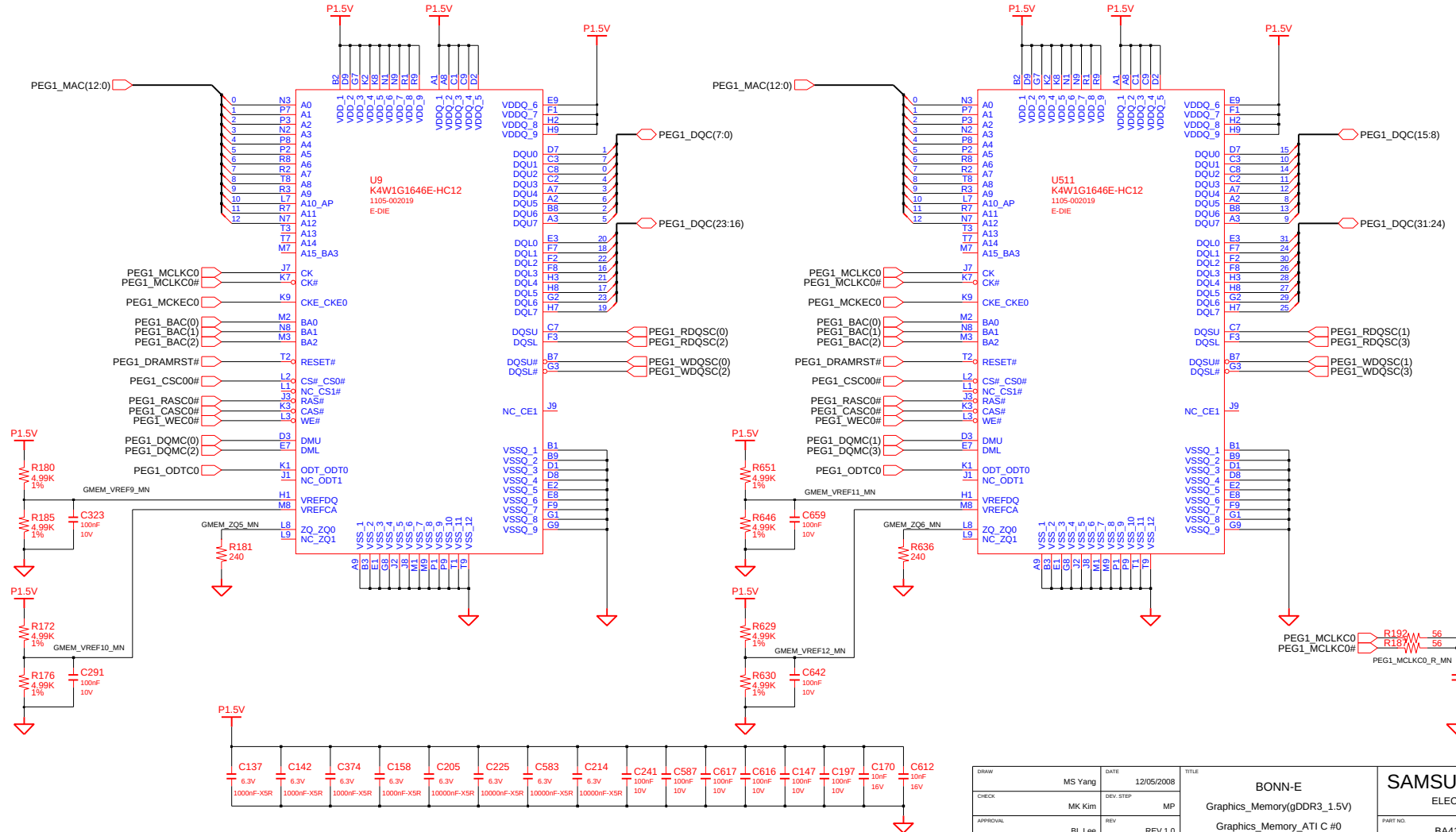
A-Channel #1



B-Channel #0

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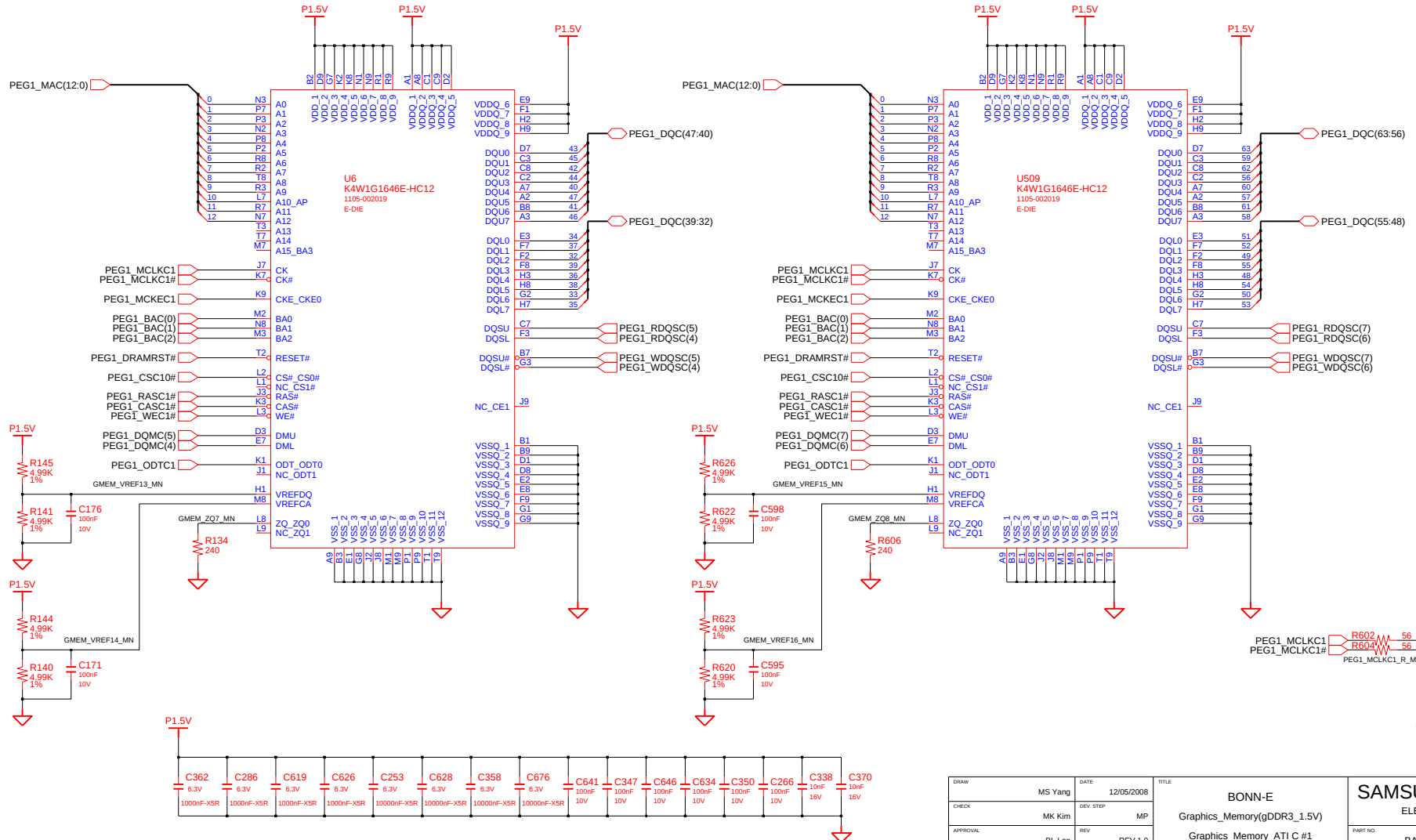


DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG ELECTRONICS
CHECK	MP	REV. STEP	MP	Graphics_Memory(gDDR3_1.5V)	PART NO.	BA41-01060A
APPROVAL	BL Lee	REV	REV 1.0	Graphics_Memory_ATI C #0	April 11, 2009 10:05:58 AM	PAGE 34 OF 67
MODULE CODE		LAST EDIT				

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B-Channel #1



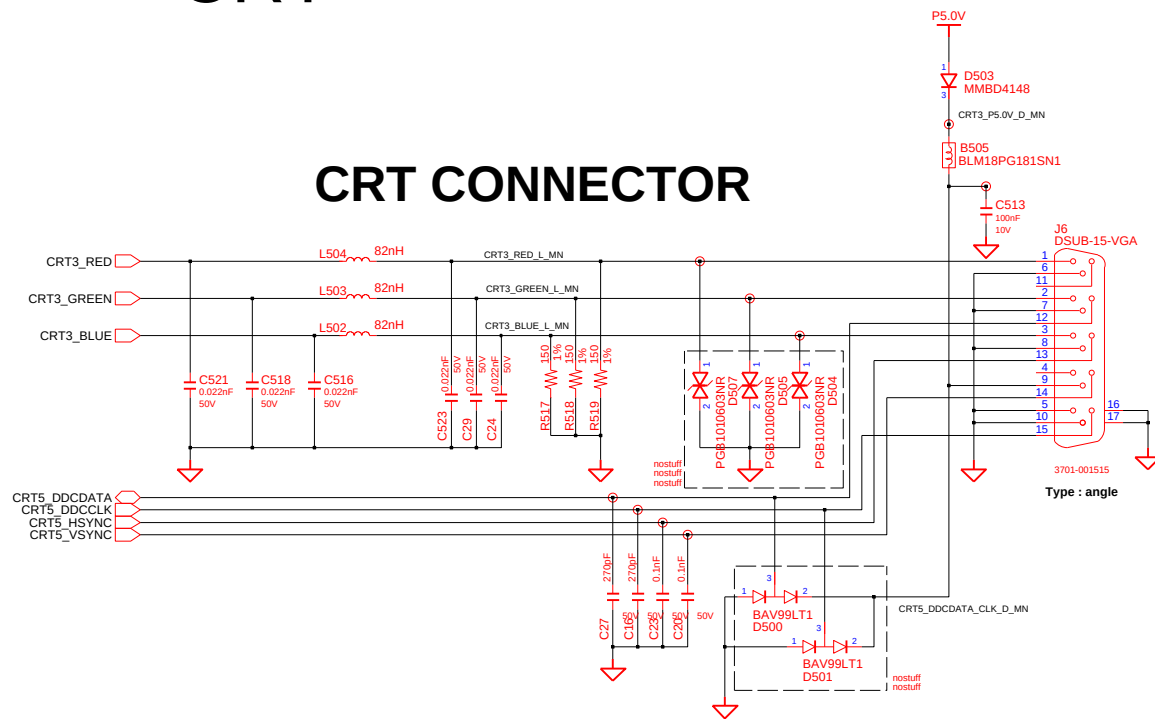
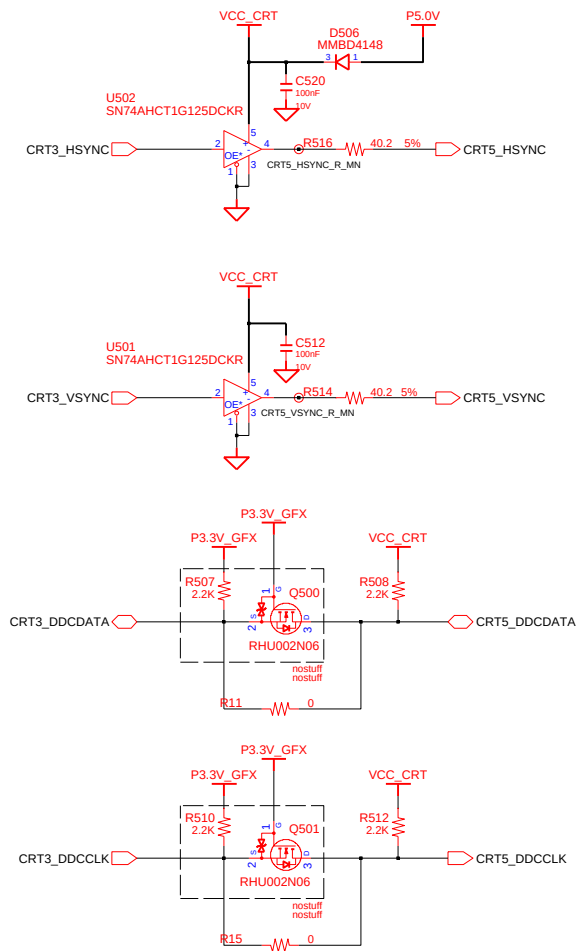
DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP	Graphics_Memory(gDDR3_1.5V)		
APPROVAL	BL Lee	REV	REV 1.0	Graphics_Memory_ATI C #1		
MODULE CODE	LAST EDIT		PART NO. BA41-01060A			
				April 11, 2009 10:05:58 AM		PAGE 35 OF 67

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CRT

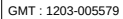
CRT CONNECTOR



Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	GRAPHICS_IF	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	CRT	PART NO.	BA41-01060A
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	37	OF 67

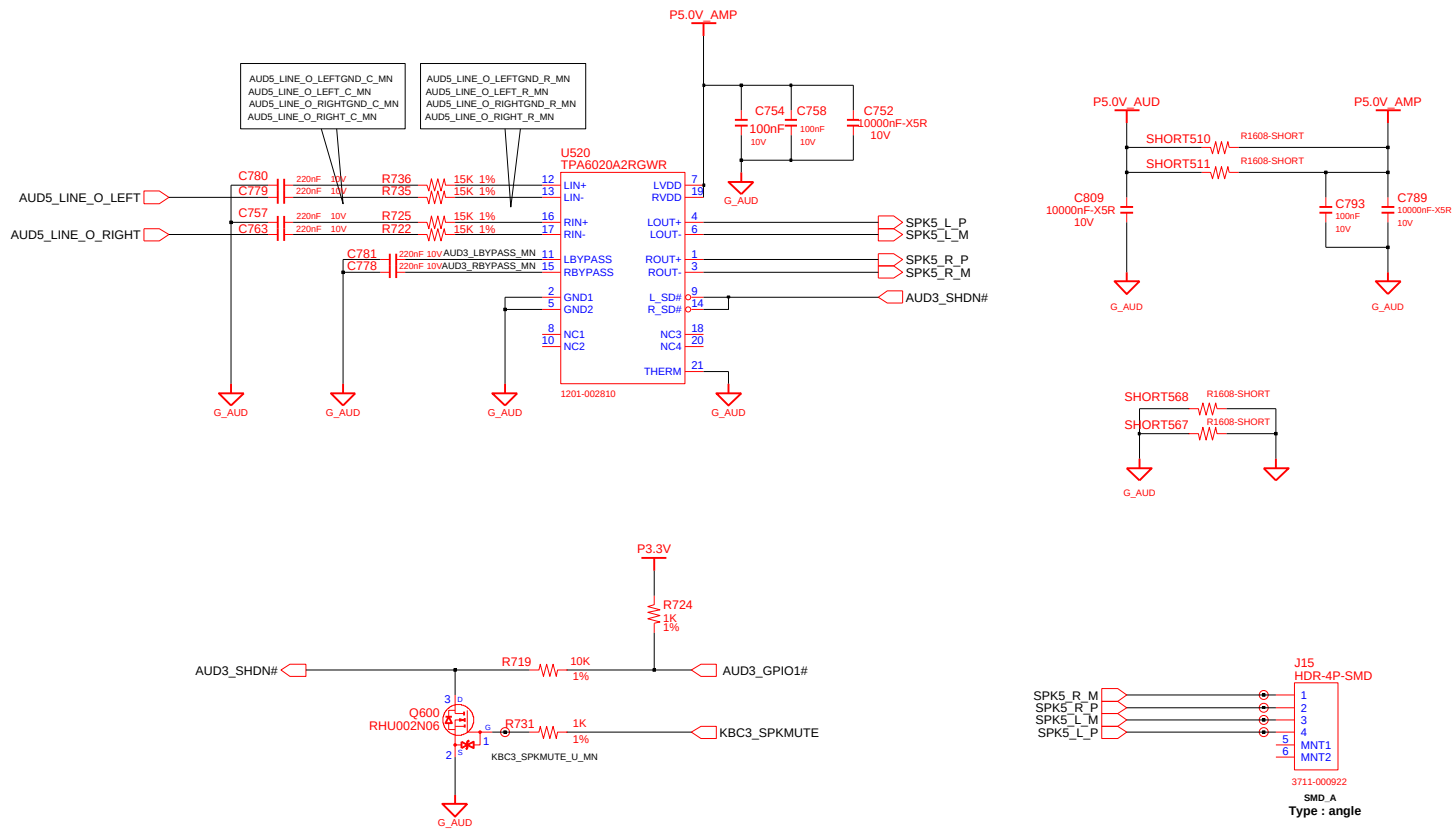
U524
AL C272-GR



DESIGN	MS Yang	DATE	12/05/2008	BONN-E HDA_CODEC AUDIO CODEC ALC272	SAMSUNG ELECTRONICS	
CHECK	MK Kim	DEV. STEP	MP		PART NO.	BA41-01060A
APPROVAL	BL Lee	REV	REV 1.0			
MODULE CODE		LAST EDIT			April 11, 2009 10:05:58 AM	PAGE 39 OF 67

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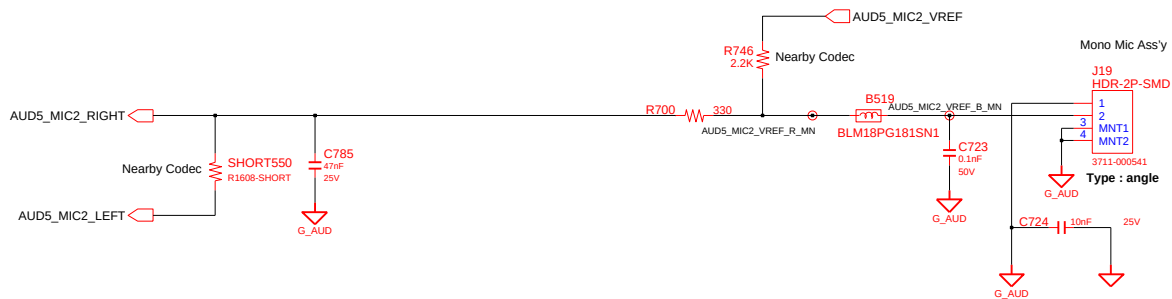
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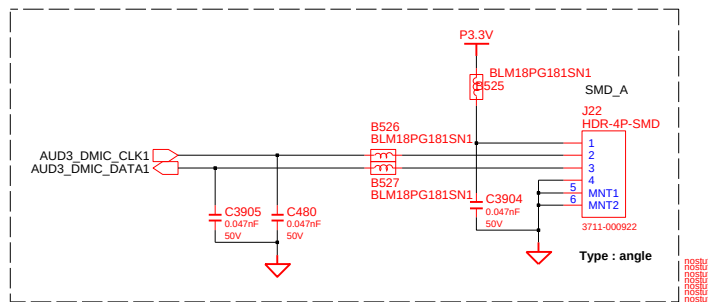
DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP		HDA_CODEC	
APPROVAL	BL Lee	REV	REV 1.0		SPK AMP TPA6017	
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	40	OF 67

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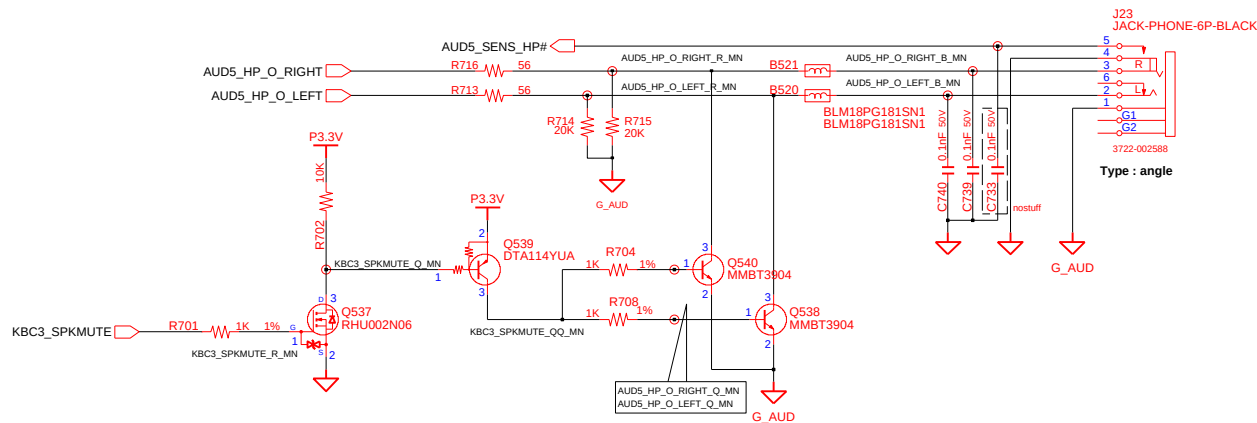
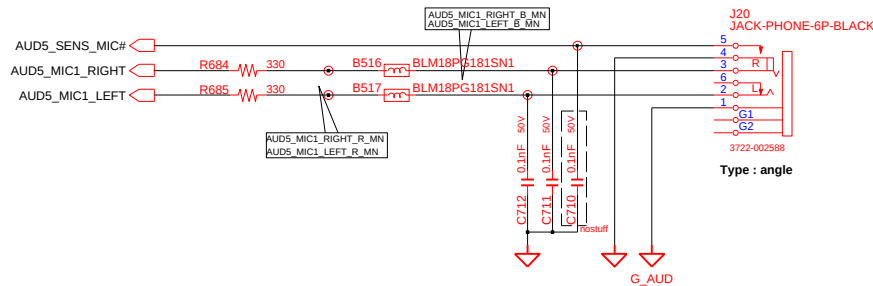
Digital MIC CONNECTOR



DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	HDA_CODEC	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	MIC AMP LMV358	PART NO.	BA41-01060A
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	41	OF 67

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HEADPHONE(BLACK)**MIC JACK(BLACK)**

DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP		HDA_CODEC	
APPROVAL	BL Lee	REV	REV 1.0		H/P JACK AND MIC JACK	
MODULE CODE		LAST EDIT		April 11, 2009 10:05:58 AM	PAGE 42 OF 67	PART NO. BA41-01060A

D

[illegible]

Sub-Woofers

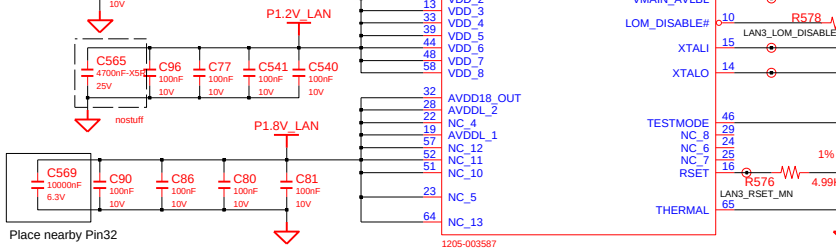
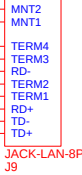


Sub-Woofer



COM-22C-015(1996.6.5) REV. 3

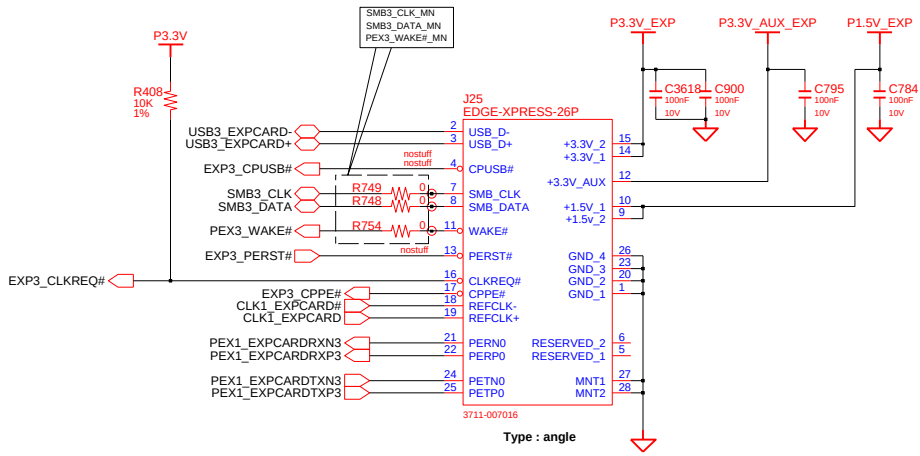
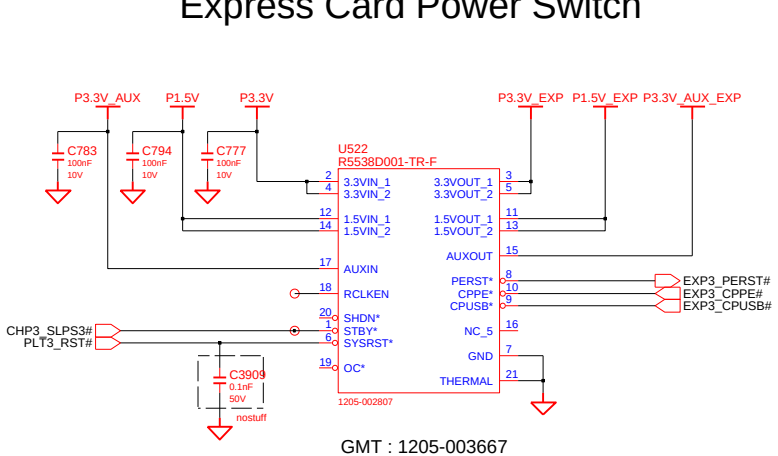
LFE9261A-R	LAN3214-50
2603-000107	2603-000110



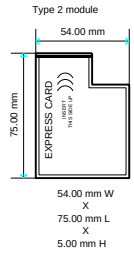
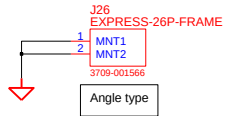
DESIGN	MS Yang	DATE	12/05/2008	BONN-E LAN LAN_MARVELL_8057	SAMSUNG ELECTRONICS				
CHECK	MK Kim	DEV. STEP	MP		PART NO.	BA41-01060A			
APPROVAL	BL Lee	REV	REV 1.0						
MODULE CODE	LAST EDIT				April 11, 2009 10:05:58 AM	PAGE	44	OF	67

Express Card

Express Card Power Switch

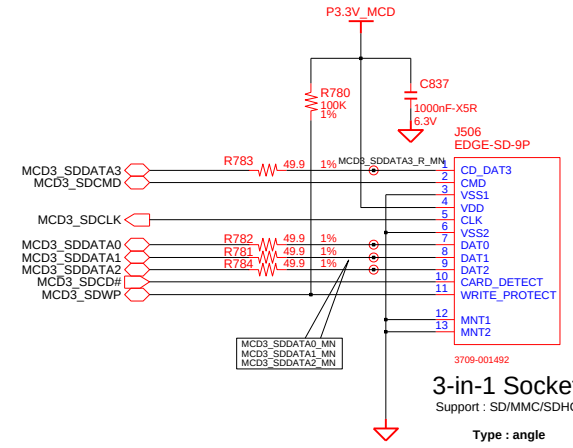
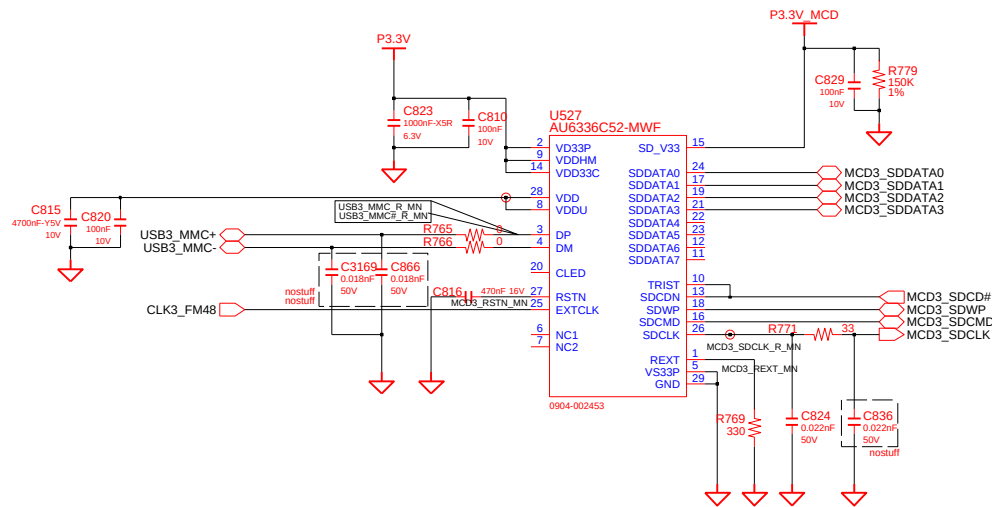


TYPE - II



DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	EXPRESS CARD	EXPRESS CARD	ELECTRONICS
APPROVAL	BL Lee	REV	REV 1.0			PART NO.
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	45	OF 67

3 IN 1 CARD (AU6336)



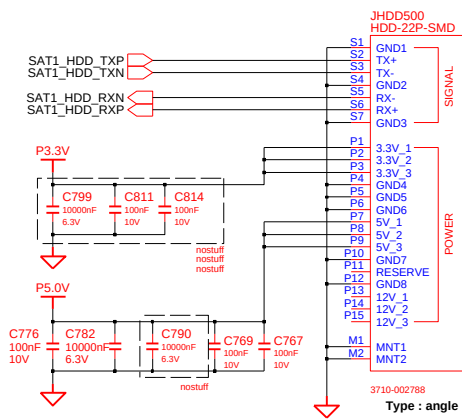
3-in-1 Socket
Support : SD/MMC/SDHC
Type : angle

DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	MULTICARD	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	2 IN 1 CARD	PART NO.	BA41-01060A
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	46	OF 67

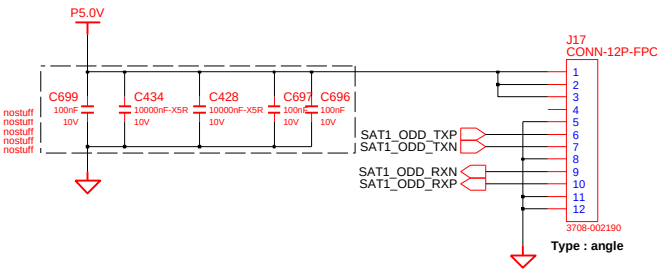


SATA I/F CONNN

SATA HDD CONN



MAIN TO SUB SATA ODD CONN



DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E SATA_DEVICES HDD & ODD SUB CONNECTOR	PART NO.	BA41-01060A
CHECK	MK Kim	REV. STEP	MP				
APPROVAL	BL Lee	REV	REV 1.0				
MODULE CODE		LAST EDIT					
				April 11, 2009 10:05:58 AM	PAGE	48	OF 67

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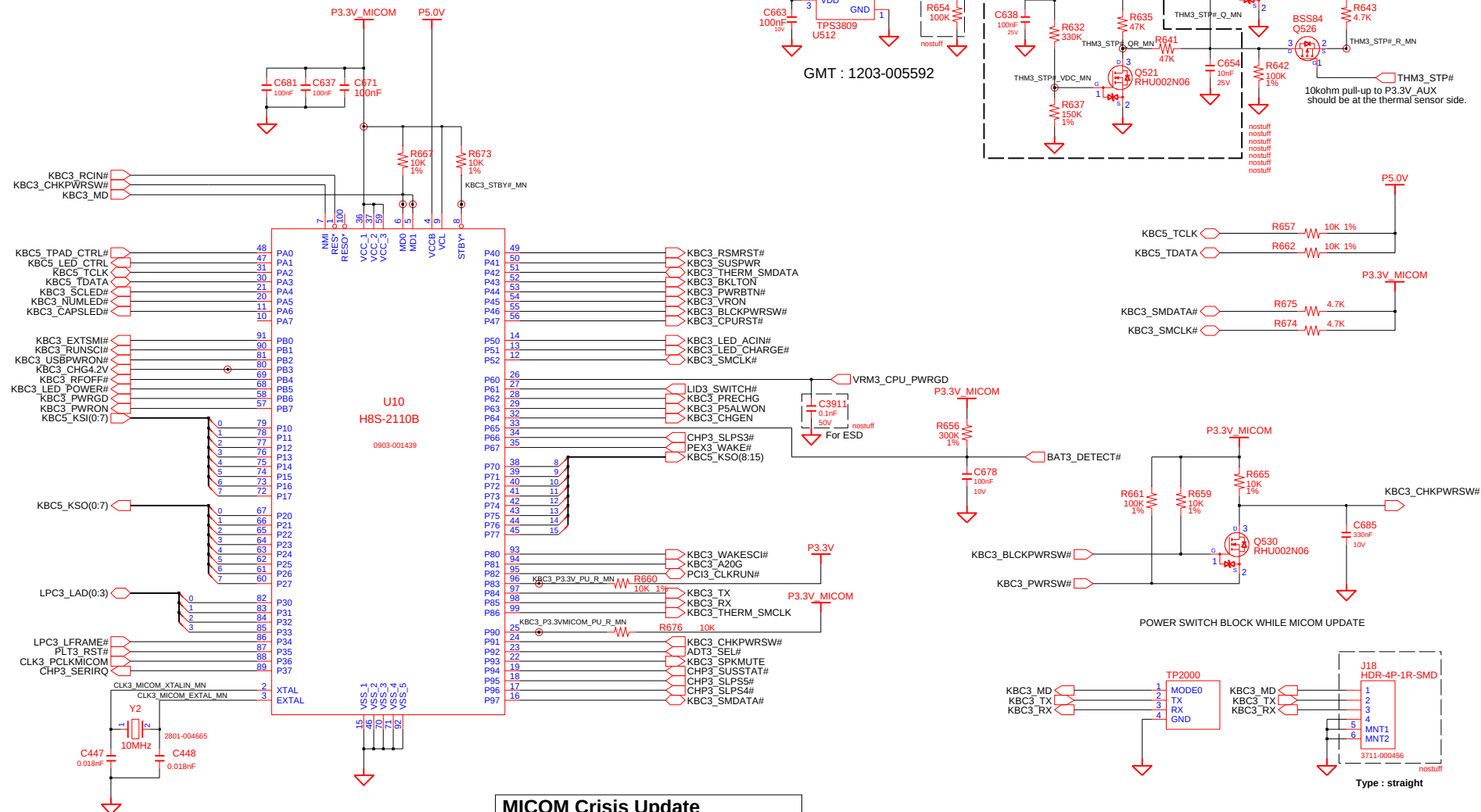
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D

C

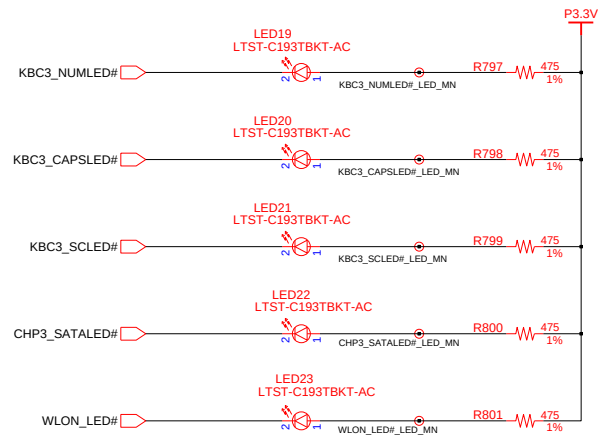
B

A

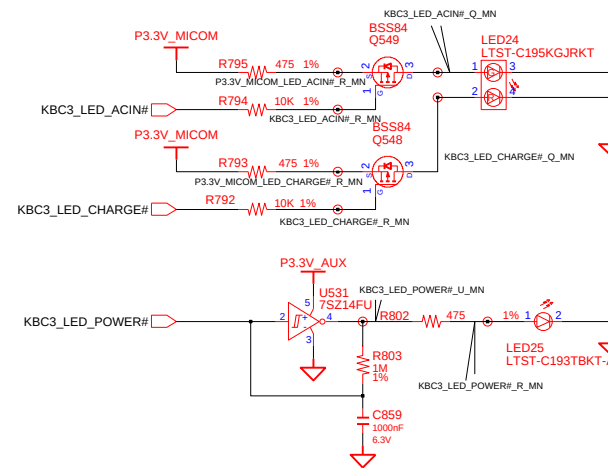


DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E MICOM	SAMSUNG ELECTRONICS
CHECK	MK Kim	REV. STEP	MP			PART NO.
APPROVAL	BL Lee	REV	REV 1.0		MICOM_Renesas2110_100p	BA41-01060A
MODULE CODE		LAST EDIT				

FUNCTION KEY LED

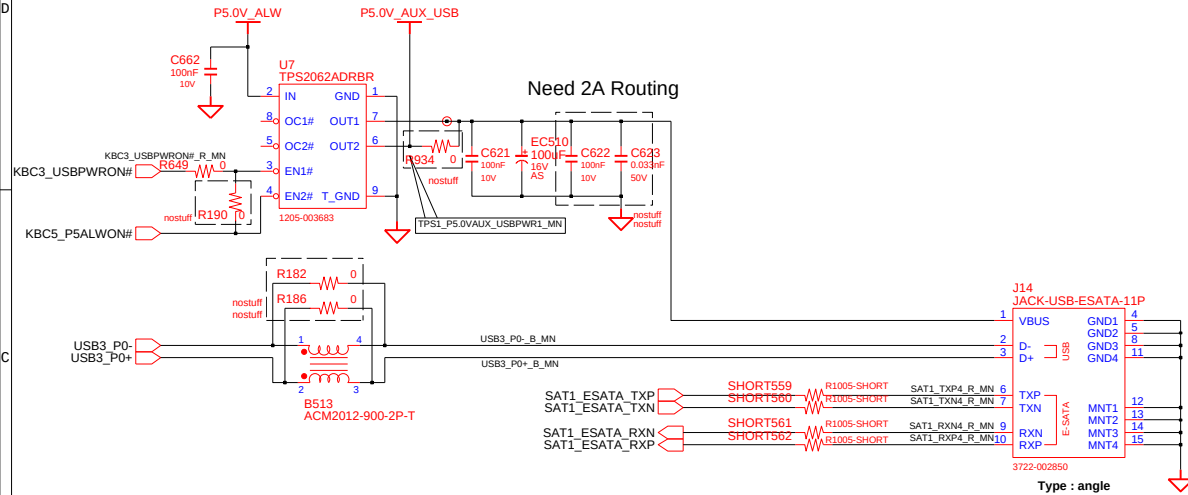


ADAPTERIN/CHARGING LED

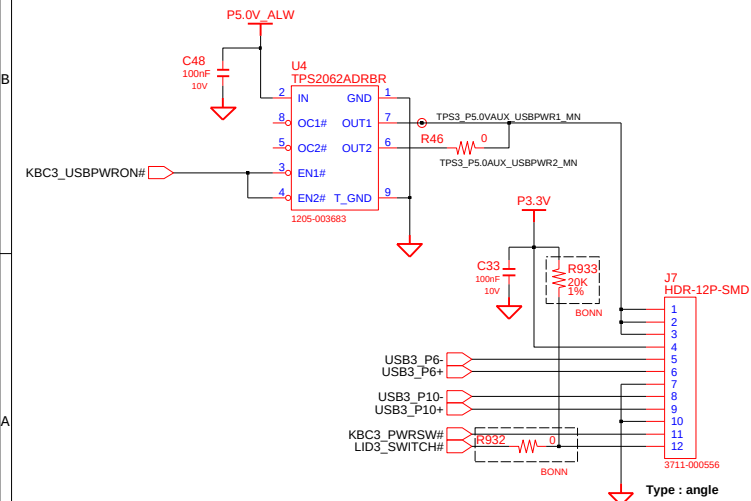


DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP		LED_SWITCH	ELECTRONICS
APPROVAL	BL Lee	REV	REV 1.0		LED_SWITCH	PART NO.
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	51	OF 67
						BA41-01060A

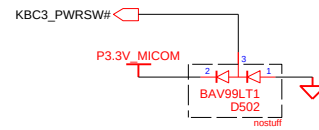
USB + eSATA CONNECTOR



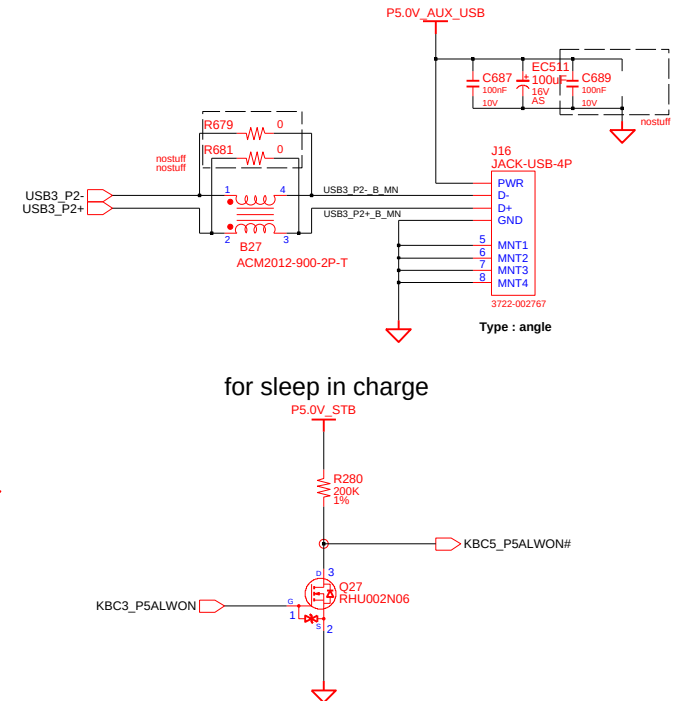
USB SUB B'D CONNECTOR



PLACE CLOSE TO USB SUB B'D Conenctor

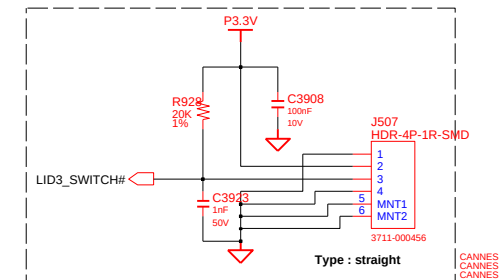


USB Single connector



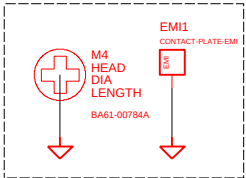
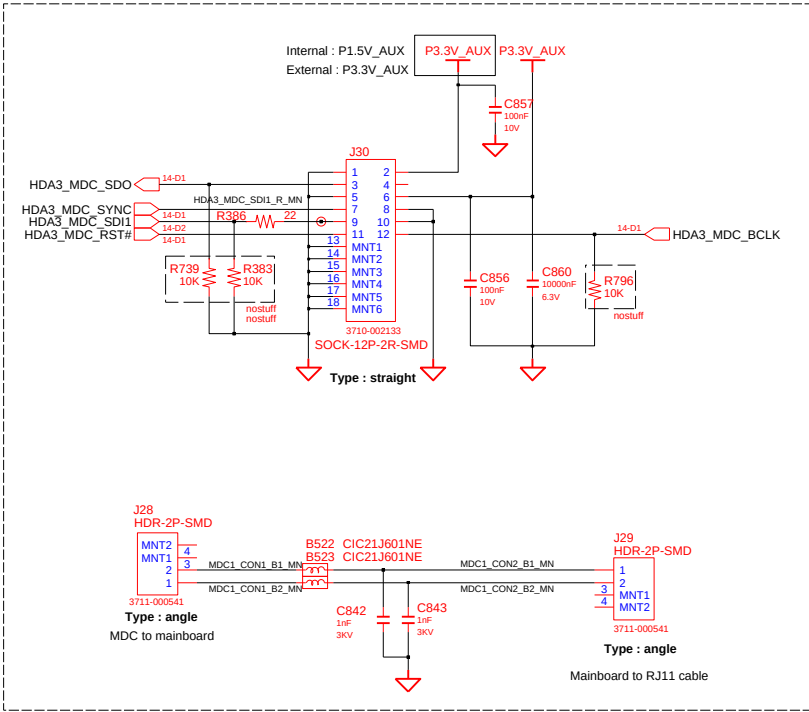
for sleep in charge

LID SWITCH for Canne



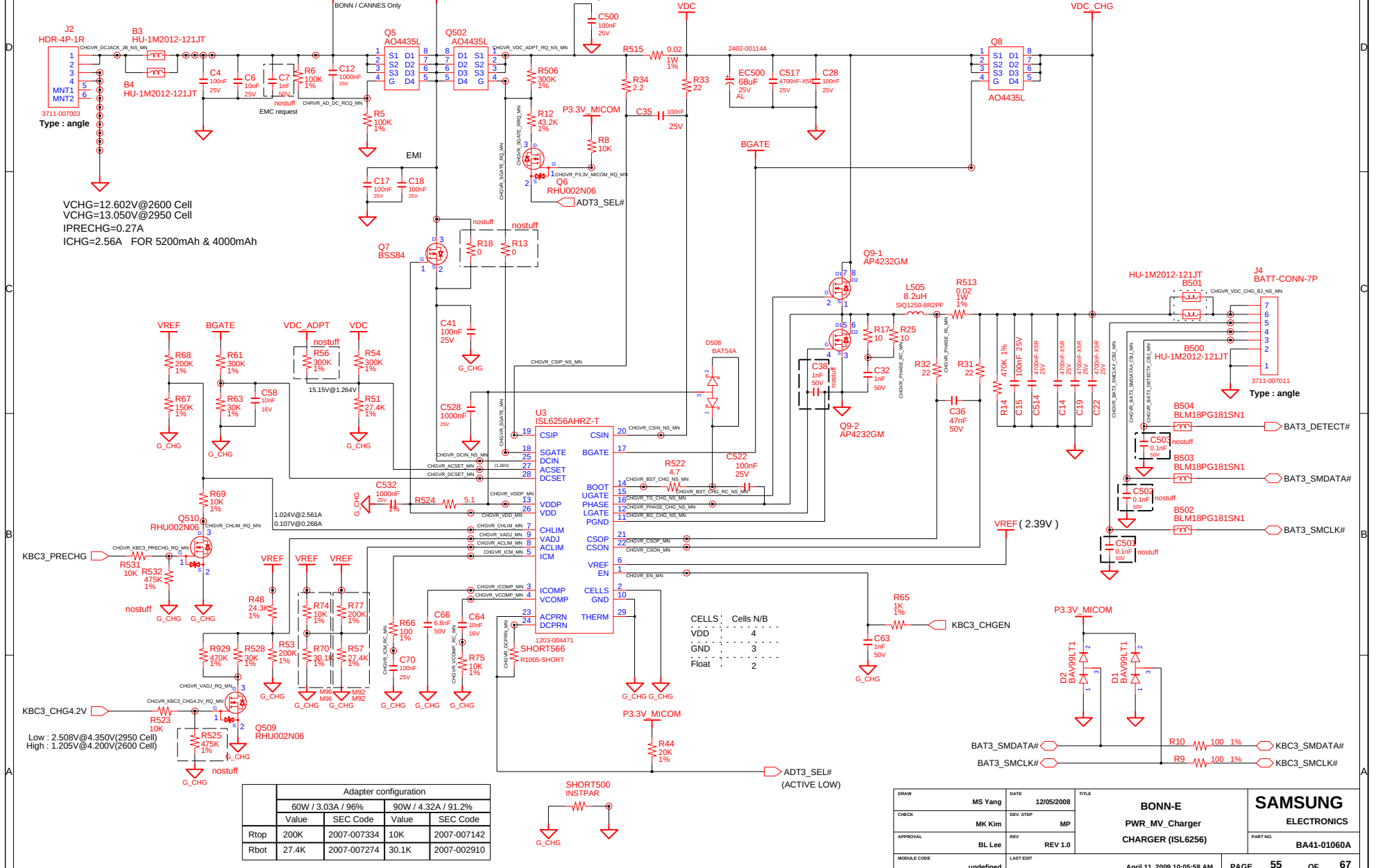
DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	DEV. STEP	MP		USB_CONN	USB & eSATA	ELECTRONICS
APPROVAL	REV	REV 1.0				PART NO.
MODULE CODE	LAST EDIT					BA41-01060A
April 11, 2009 10:05:58 AM						PAGE 52 OF 67

MDC connector

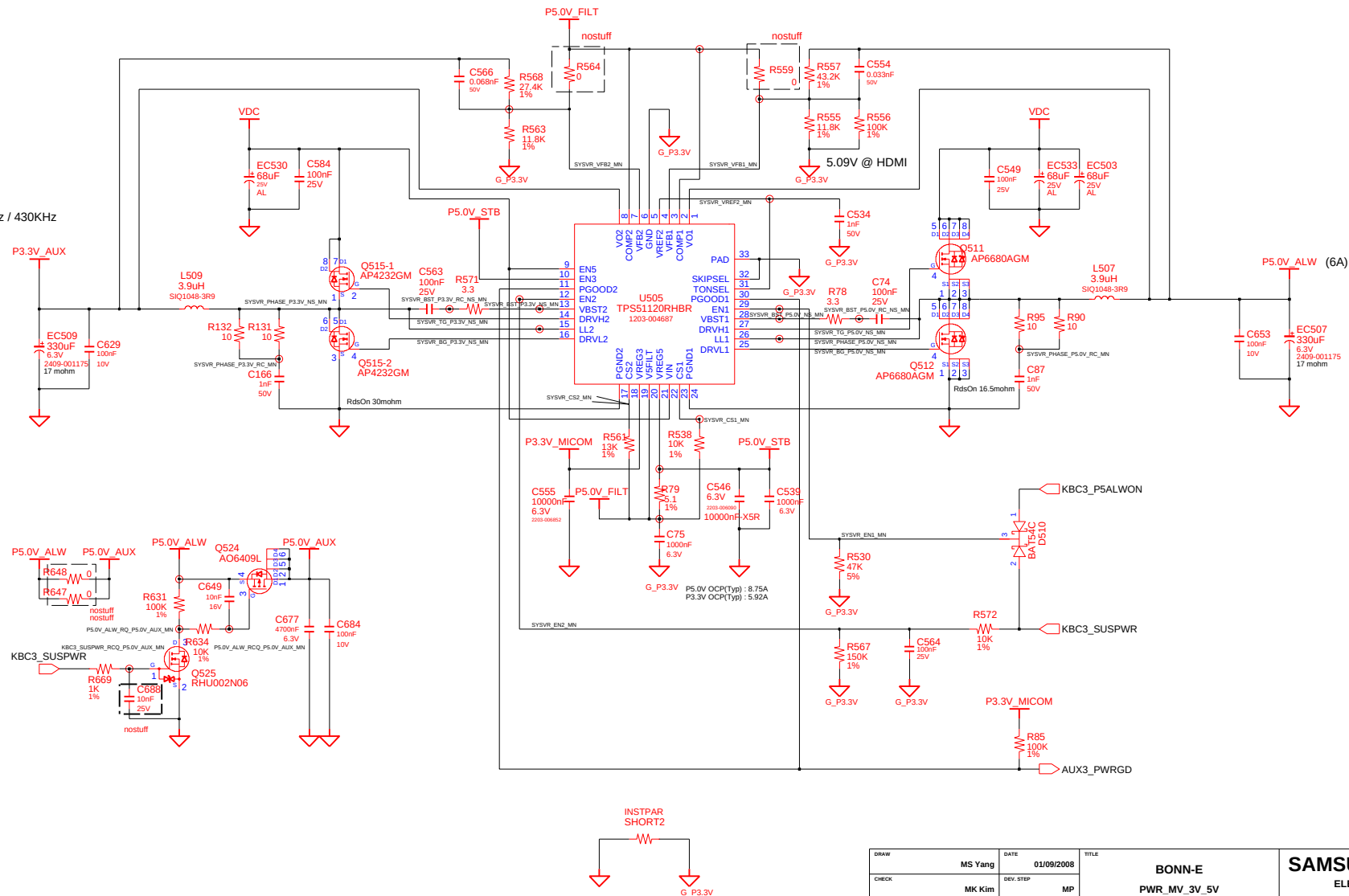


DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	DEV. STEP	MP	MDC CONNECTOR	MDC CONNECTOR	ELECTRONICS
APPROVAL	BL Lee	REV	REV 1.0			PART NO. BA41-01060A
MODULE CODE	undefined	LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	54	OF 67

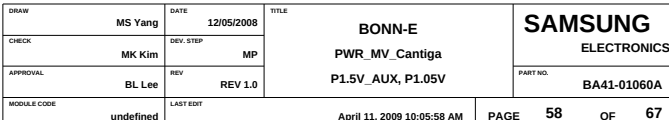
CHARGER & POWER MANAGEMENT



TONSEL VREF2
5V / 3.3V : 280KHz / 430KHz
(4A)

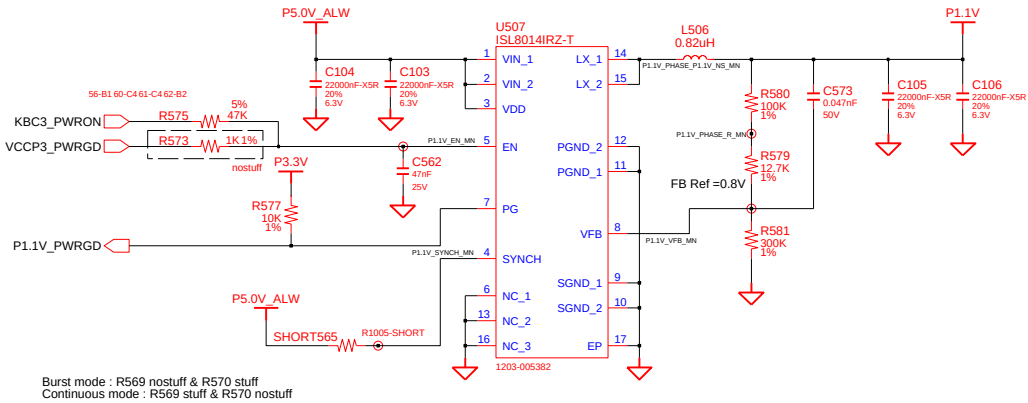


DRAW	MS Yang	DATE	01/09/2008	BONN-E PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX	SAMSUNG ELECTRONICS	
CHECK	MK Kim	DEV_STEP	MP			
APPROVAL	BL Lee	REV	REV 1.0		PART NO.	BA41-01060A
MODA.E CODE	undefined	LAST EDIT	April 11, 2009 10:05:58 AM		PAGE	56 OF 67



P1.1V

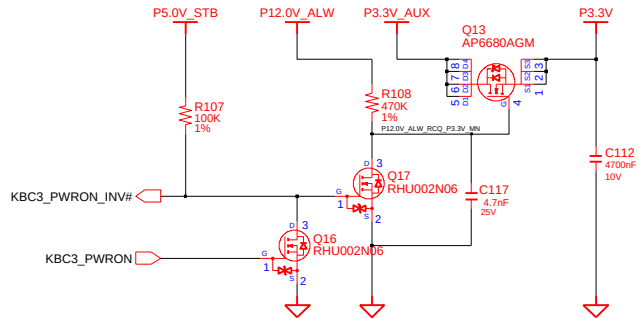
P1.1V(External Gfx)



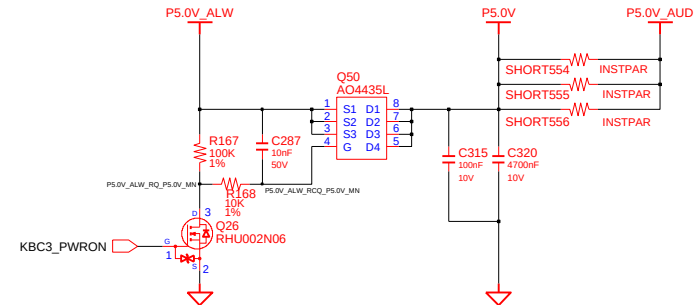
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CHECK	MK Kim	REV. STEP	MP	PWR_MV_Switched	PART NO.	ELECTRONICS
APPROVAL	BL Lee	REV	REV 1.0	P1.1V	BA41-01060A	
MODULE CODE	LAST EDIT			April 11, 2009 10:05:58 AM	PAGE	61 OF 67

Switched Power

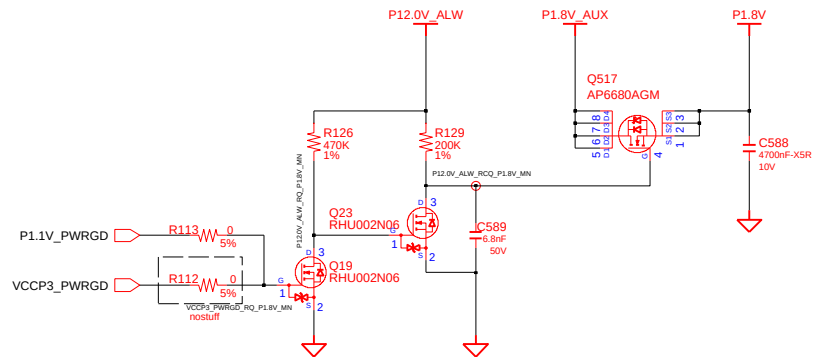
Switched Power On (P3.3V)



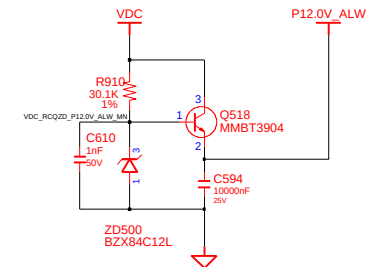
Switched Power On (P5.0V)



Switched Power On (P1.8V)

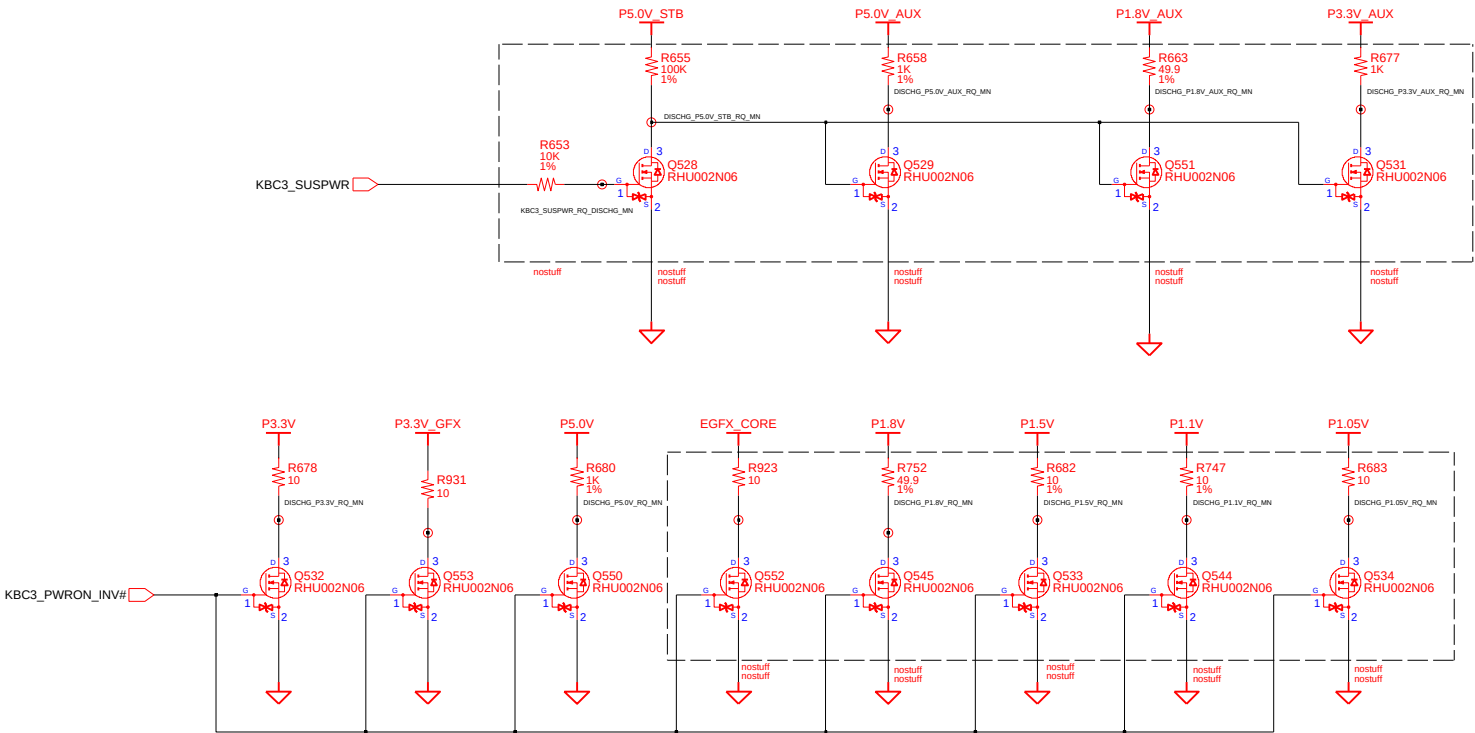


P12.0V_ALW



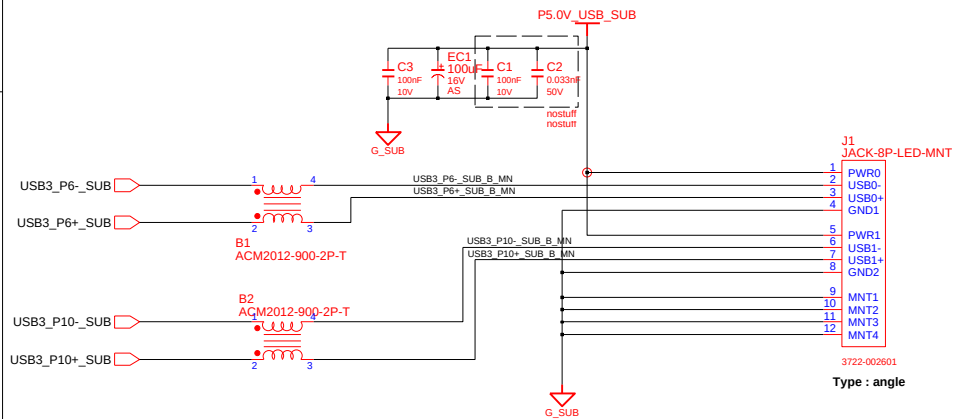
DRAWN	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	PWR_MV_SWITCHED	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	SWITCHED POWER	PART NO.	BA41-01060A
MODULE CODE		LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	62	OF 67

POWER DISCHARGER

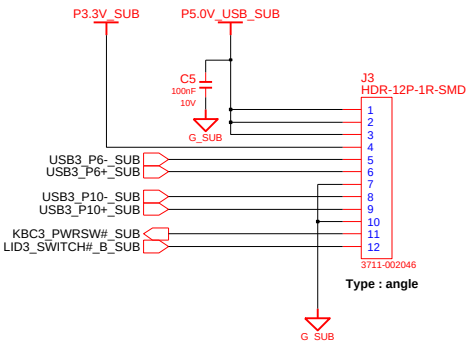


DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	PWR_MV_DISCHARGER	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	DISCHARGING LOGIC	PART NO.	BA41-01060A
MODULE CODE	undefined	LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	63	OF 67

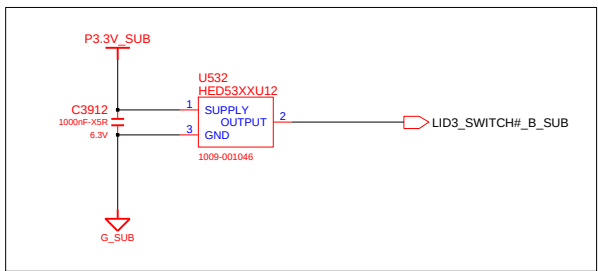
2 USB PORT & POWER S/W SUB B'D



SUB TO MAIN USB CONN



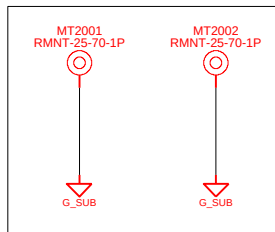
LID_SWITCH (Bonn only)



Power ON LED



Power Switch Button

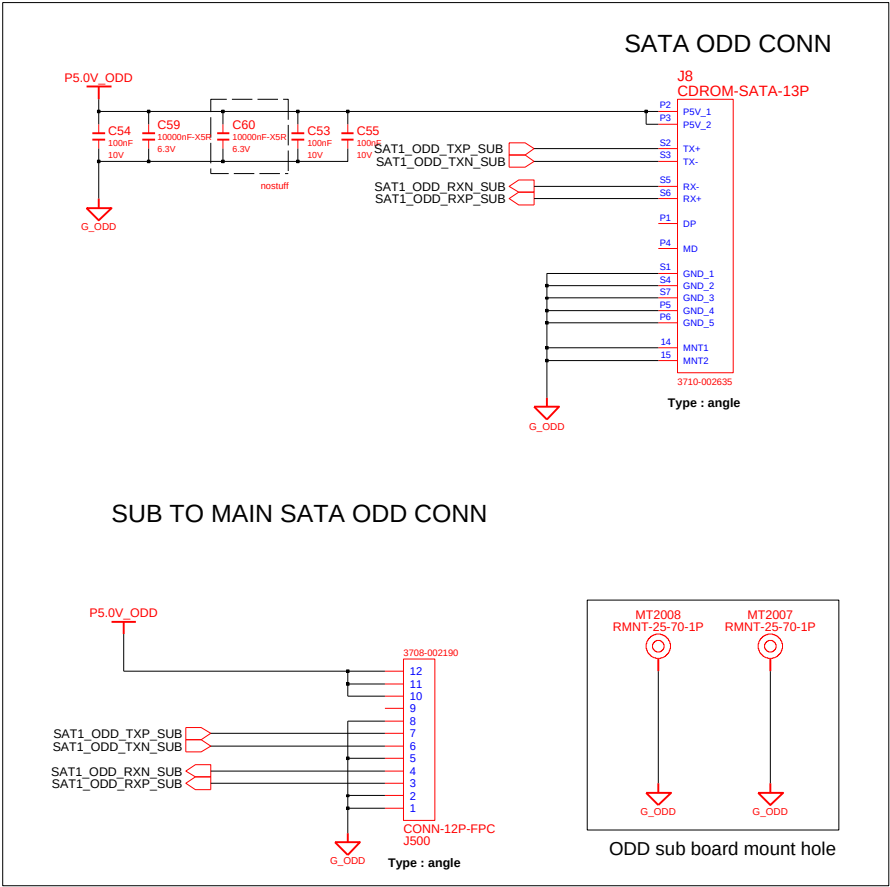


USB sub board mount hole

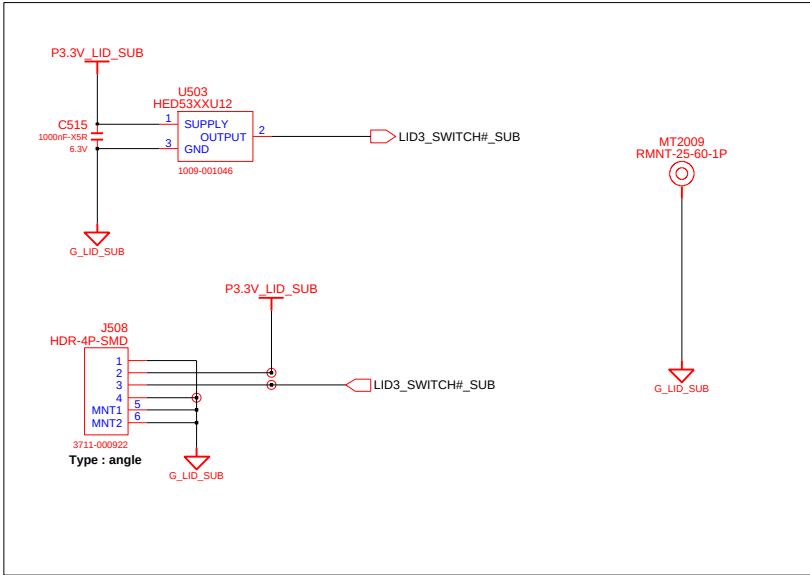
DESIGN	MS Yang	DATE	12/05/2008	TITLE	BONN-E SUB BOARD1	SAMSUNG ELECTRONICS
CHECK	MK Kim	DEV. STEP	MP	REV	2 USB & POWER SW	PART NO. BA41-01060A
APPROVAL	BL Lee	REV	REV 1.0	LAST EDIT	April 11, 2009 10:05:58 AM	PAGE 64 OF 67
MODULE CODE						

SATA ODD & LID SW SUB BOARD

SATA ODD SUB BOARD

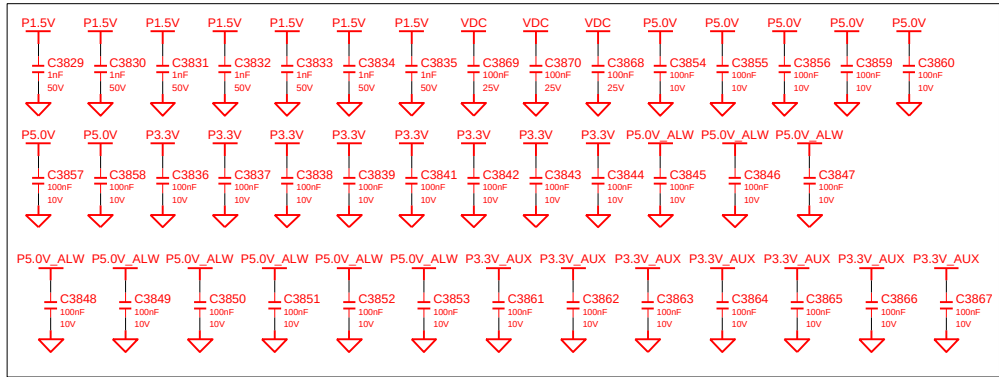


LID SWITCH SUB BOARD (Canne only)

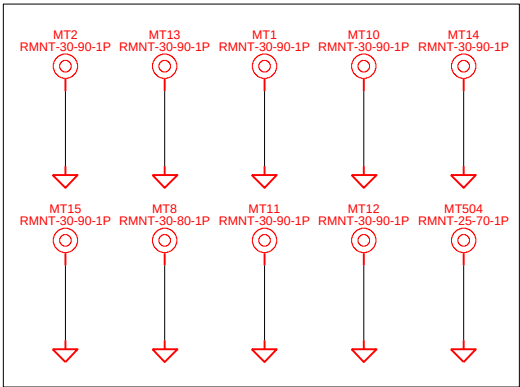


DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	SUB BOARD2	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	SATA ODD SUB BOARD	PART NO.	BA41-01060A
MODULE CODE	undefined	LAST EDIT	April 11, 2009 10:05:58 AM	PAGE	65	OF 67

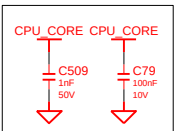
Mainboard Mount ((30,80)x9), (30,90)x9), (25,70)x1))



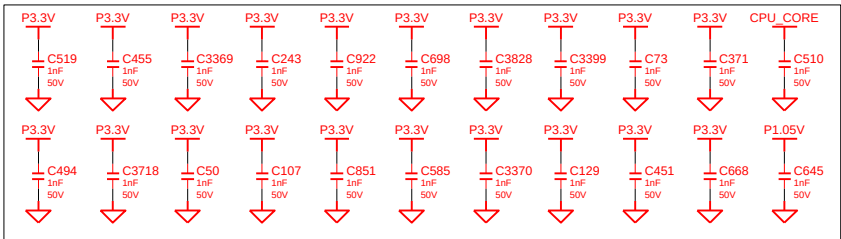
Add for EMC, 2009.01.06



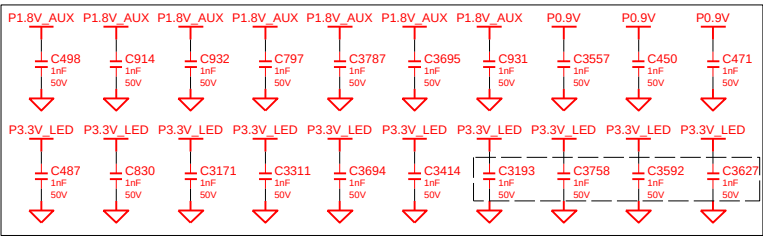
Top : (30,80) x 9
Bot : (30,90) x 9



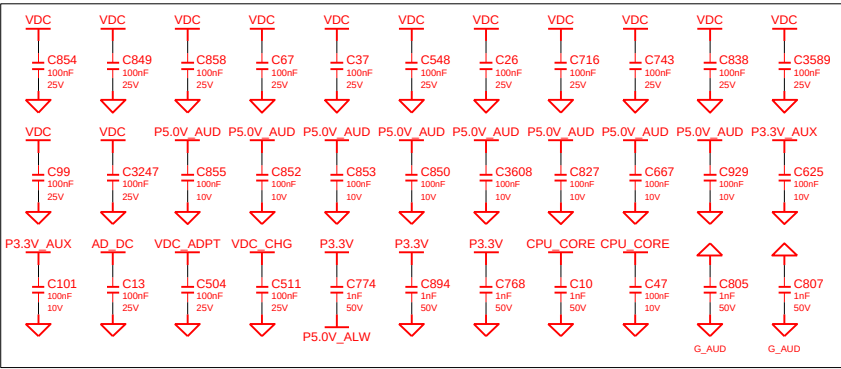
Add for EMC (Top), 2008.11.19



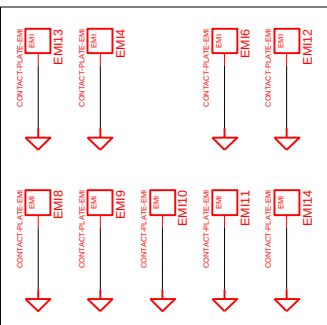
Add for EMC (5th Layer), 2008.11.19



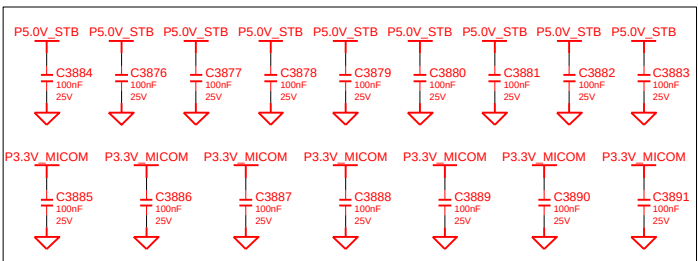
Add for EMC (Bottom), 2008.11.19



Add for EMC (Bottom), 2008.11.19



Add for EMC, 2009.01.07



Add for EMC, 2009.02.02

DRAW	MS Yang	DATE	12/05/2008	TITLE	BONN-E	SAMSUNG
CHECK	MK Kim	REV. STEP	MP	ICT PORT	ICT PORT	ELECTRONICS
APPROVAL	BL Lee	REV	REV 1.0	ICT PORT	ICT PORT	PART NO.
MODULE CODE		LAST EDIT				BA41-01060A
				April 11, 2009 10:05:58 AM	PAGE	66 OF 67

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0_SPI3_MISO
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0_THM3_STP#
0_VRM_ISEN1
0_WLON_LED#
0_AUD3_SHDN#
0_AUX3_PWRGD#
0_PLT3_RST#
0_CLK3_PWRGD#
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0_CPU1_A20M#
0_CPU1_BPRI#
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0_CPU1_BSEL1
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 CLK3, DBGLPC
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 CPU1, DPLSP1
 CPU1, DPLSP2
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 CPU1, V1D1
 CPU1, V1D2
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- ☒ G_P3.3V
- ☒ P1.05V
- ☒ P1.1V
- ☒ P1.1V_DPE
- ☒ P1.8V
- ☒ P1.8V_A2VDD
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- ☒ P1.8V_DPE
- ☒ P1.8V_VDDDD
- ☒ P3.3V_GEX

DESIGN	MS Yang	DATE	12/05/2008	BONN-E TEST POINT TEST POINT	SAMSUNG ELECTRONICS	
CHECK	MK Kim	DDV-STEP	MP		PART NO.	BA41-01060A
APPROVAL	BL Lee	REV	REV 1.0			
MODULE CODE	LAST EDIT			April 11, 2009 10:05:58 AM	PAGE 67	OF 67