# BREMEN-D

CPU : AMD Caspin
Chip Set : AMD RX881 + SB710
Remarks : Tigris Platform
Park-XT M2

Model Name : Bremen-D
PBA Name : MAIN
PCB Code : GCE :
NAN :
HAN :
Dev. Step : PV
Revision : 1.4
T.R. Date : 2009.11.10

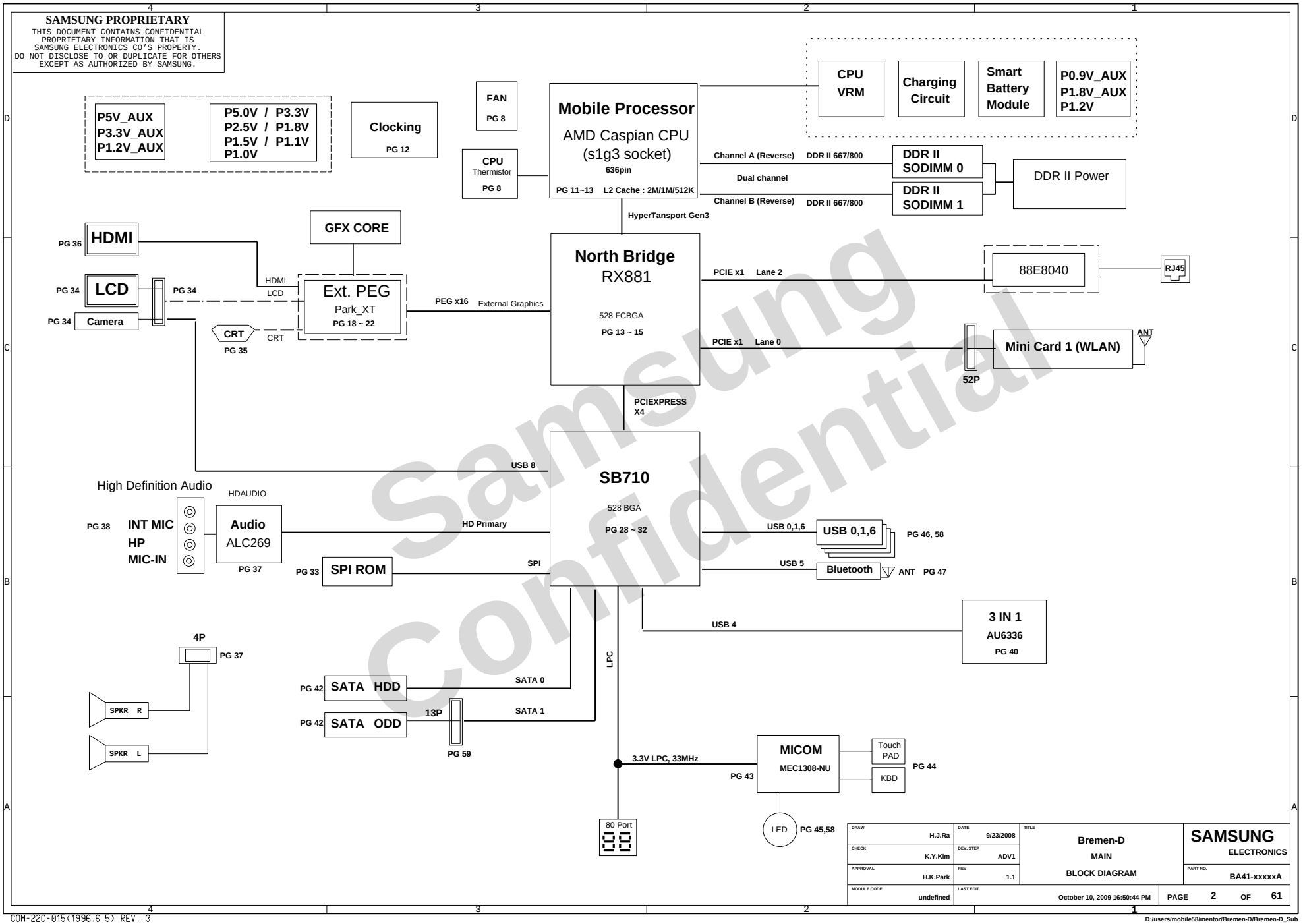
| Design | CHECK | APPROVAL |
|---|---|---|
| | | |
| | | |

■ *Owner : SEC Mobile R & D* *Signature :* *X*

## Table of Contents



| | | | |
|---|---|---|---|
| DRAW: XIE, BIN | DATE: 10/10/2008 | TITLE: Bremen-D MAIN COVER | SAMSUNG ELECTRONICS |
| CHECK: GUO, LEI | DEV. STEP: PV | | |
| APPROVAL: LEE, BC | REV: 1.0 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October, 28, 2009 11:35:37 AM | PAGE 1 OF | |






| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D MAIN BLOCK DIAGRAM | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 2 OF 61 | |

# BOARD INFORMATION

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### Voltage Rails

| | |
|---|---|
| VDC | Primary DC system power supply (7 to 21V) |
| CPU_CORE | Core Voltage for CPU |
| EGFX_CORE | Core Voltage for GPU |
| P1.1V | VTT for RX881 |
| P1.2V | Core Voltage for SB710, CPU_VDLT, RX881 |
| P3.3V_MICOM | 3.3V always power rail (for Micom) |
| P1.5V | 1.5V switched power rail (off in S3-S5) |
| P1.8V | 1.8V switched power rail (off in S3-S5) |
| P1.8V_AUX | 1.8V power rail for DDR (off in S4-S5) |
| P1.0V | 0.9V power rail for DDR (off in S3-S5) |
| P2.5V | 2.5V switched power rail (off in S3-S5) |
| P3.3V | 3.3V switched power rail (off in S3-S5) |
| P3.3V_AUX | 3.3V switched on power rail (off in S4-S5) |
| P5.0V | 5.0V switched power rail (off in S3-S5) |
| P5.0V_AUX | 5.0V switched on power rail (off in S4-S5) |
| P5.0V_STB | 5.0V always power rail |
| P12.0V_ALW | 12.0V always power rail |

### Crystal / Oscillator

| TYPE | FREQUENCY | DEVICE | USAGE |
|---|---|---|---|
| Crystal | 32.768KHz | SB710 | Real Time Clock |
| Crystal | 10MHz | MICOM | MEC1308-NU |
| Crystal | 14.318MHz | CLOCK-Generator | CK-505 |
| Crystal | 25MHz | LAN | 88E8040 |
| Crystal | 25MHz | SATA | SB710 |

### USB PORT Assign

| PORT # | ASSIGNED TO |
|---|---|
| 0 | SYSTEM PORT 0 |
| 1 | SYSTEM PORT 1 |
| 2 | NC |
| 3 | NC |
| 4 | 3 IN 1 |
| 5 | Bluetooth |
| 6 | SYSTEM PORT 2 |
| 7 | NC |
| 8 | Camera |
| 9 | NC |
| 10 | NC |

### PCI Express Assign

| PORT # | ASSIGNED TO |
|---|---|
| 0 | Mini Card (WLAN) |
| 1 | NC |
| 2 | LOM |
| 3 | NC |
| 4 | NC |
| 5 | NC |

### I²C / SMB Address

| Devices | Address | Hex | Bus |
|---|---|---|---|
| S710 | Master | - | SMBUS Master |
| CPU Thermal Sensor | 0111 101x | 7Ah | Thermal Sensor |
| SODIMM0 | 1010 000x | A0h | - |
| SODIMM1 | 1010 010x | A4h | - |
| Thermal Sensor on SODIMM0 | 0011 000x | 30h | - |
| Thermal Sensor on SODIMM1 | 0011 010x | 34h | - |
| CK-505M (Clock Generator) | 1101 0010 | D2h | Clock, Unused Clock Output Disable |
| Gfx (DTS) | | 41h | Gfx Thermal SMBUS Slave ID |

### LCD Pannel Detect (TBD)

| Devices | Resolution | PANNEL_DETECT_0(strap0) |
|---|---|---|



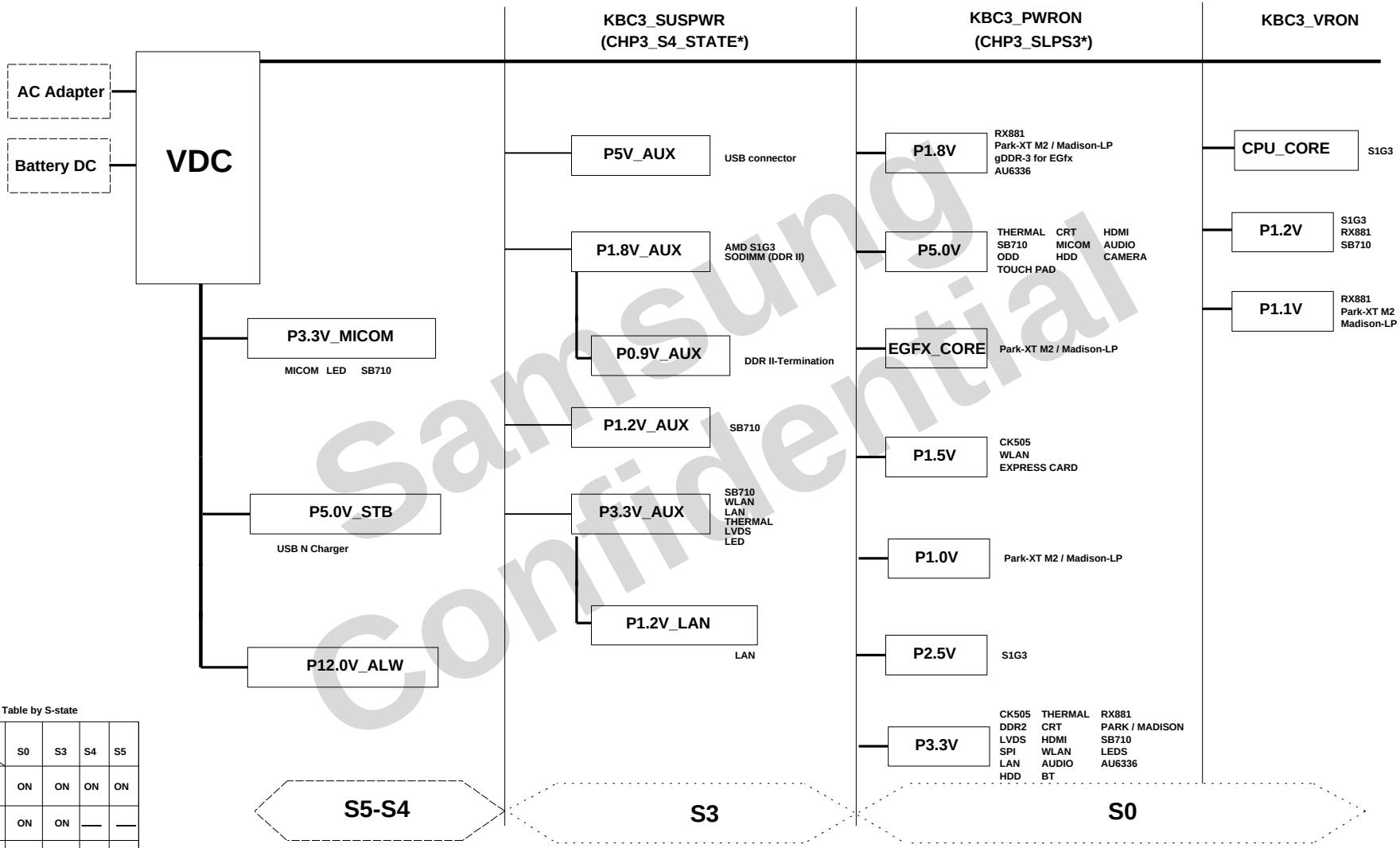
## REVISION HISTORY

See rev notes for more information.

| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 08/18/2009 | TITLE: Bremen-D MAIN BOARD INFORMATION | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 3 OF 61 | |

# POWER DIAGRAM

Rev 0.3





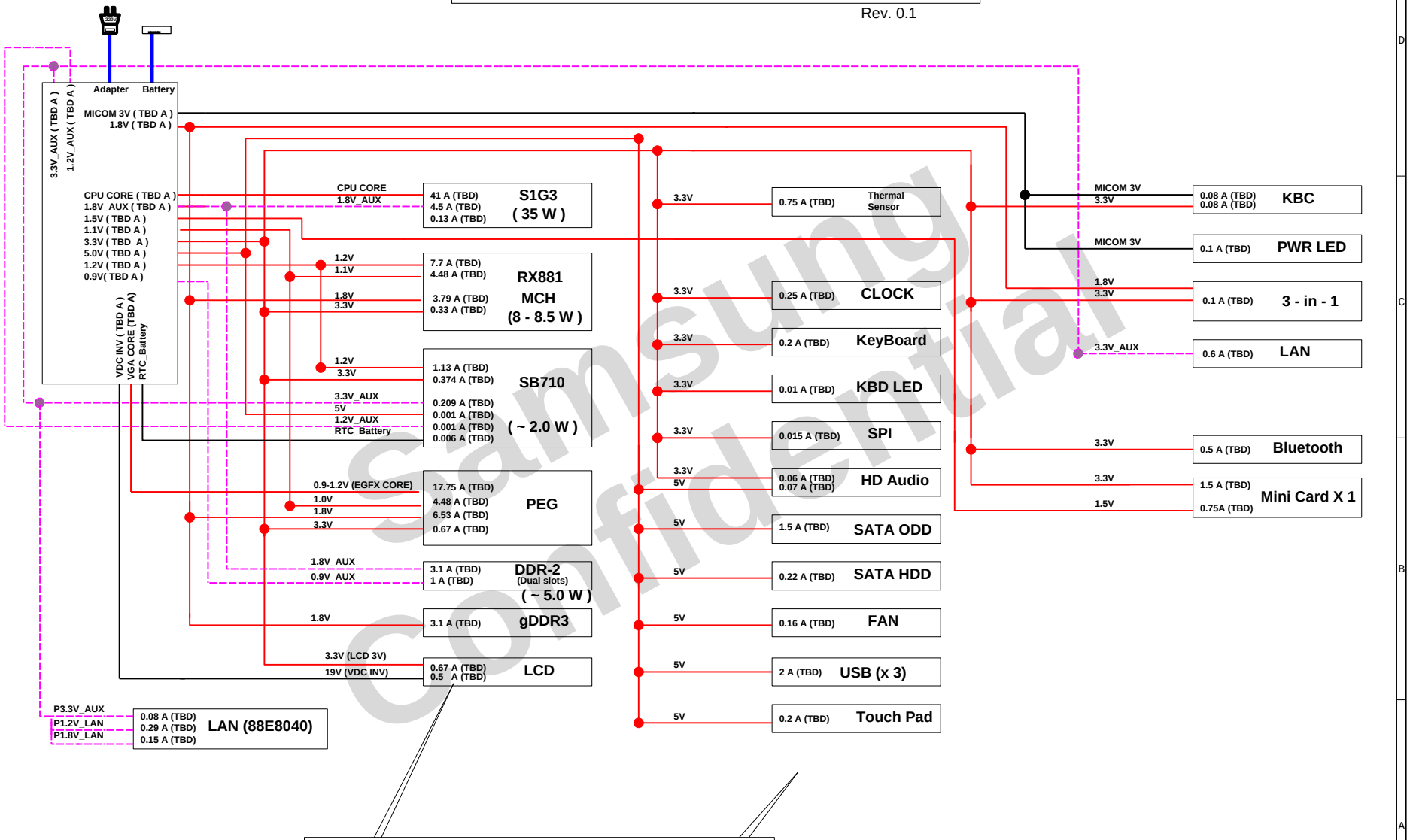

**Power On/Off Table by S-state**

| Rail / State | S0 | S3 | S4 | S5 |
|---|---|---|---|---|
| +V*A(LWS) +V*LAN | ON | ON | ON | ON |
| +1.8V_AUX +0.9V_AUX | ON | ON | — | — |
| +V*AUX | ON | ON | — | — |
| +V | ON | — | — | — |
| +V* (CORE) | ON | — | — | — |

| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 08/18/2009 | TITLE: Bremen-D / MAIN / POWER DIAGRAM | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 4 OF 61 | |

# POWER RAILS ANALYSIS

Rev. 0.1




Value by Datasheet/Application notes (Value by measurement)



| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 08/18/2009 | TITLE Bremen-D MAIN POWER RAILS ANALYSIS | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 5 OF 61 | |

# POWER SEQUENCE

Rev. 0.3

**Host Boot / ME Off**
(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

**Host / ME Boot**
(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

**Host S5 / ME Boot**
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

RTC Battery — PRTC_BAT — CHP3_RTCRST# — 1

POWER S/W — 4) POWER_SW* — 4

MICOM — 7
- 9) KBC3_RSMRST#
- 20) KBC3_CPURST# — 20
- 17) KBC3_PWRGD — 17
- 110ms Delay
- 16)VRM3_CPU_PWRGD
- 5) KBC3_SUSPWR — 5
- 11) KBC3_PWRON — 11
- 14) KBC3_VRON — 14
- 10) CHP3_SLPS5#/4#/3# — 8

SB710 — Sheet 28-32
- 6) P3.3V_AUX
- 6-1) P1.2V_AUX
- VRMPWRGD
- PWROK
- CL_PWROK
- 17) KBC3_PWRGD
- 21) PLT3_RST# — 21
- 22) CPU1_LDTRST# — 22
- 15)VRM3_CPU_PWRGD
- 19) CPU1_PWRGDCPU — 19
- 18) CHP3_NB_PWRGD — 18

CPU VRM — DC/DC B'd
- 16) VRM3_CPU_PWRGD — 16
- 19) CPU1_PWRGDCPU
- 14) KBC3_VRON
- 15) CPU_CORE — 15

CPU — (Test Option) — Sheet 9 - 11
- 15) P1.2V
- 12) P2.5V

GMCH — Sheet 13-15
- PWRGOOD
- SYSRESET#
- 18) CHP3_NB_PWRGD (Back up)
- 17) KBC3_PWRGD
- 21) PLT3_RST*
- 12) P1.8V
- 12) P3.3V
- 15) P1.1V

PCIe Devices — 21
- 6) P3.3V_AUX
- 12) P3.3V
- 10) P1.5V

PEG — 21
- 12) P1.8V
- 13) P1.0V
- 11-1) P3.3V

DDR2 Memory
- 8) P1.8V_AUX
- 8-1) P0.9V_AUX

APW7141 (DDR2 POWER) — Sheet 50 — 8
- 3) P5.0V_STB
- 2) VDC
- 7) AUX3_PWRGD
- 8) P1.8V_AUX

10K / 10K
- 8-1) MEM1_VREF — 13

APL5336 — 11
- 12) P1.5V
- 11) KBC3_PWRON
- 13) P1.0V

AP4435 — 12
- 12) P5.0V

ISL95870B — 12
- 11) KBC3_PWRON
- 6) P5.0V_AUX
- 6) P3.3V_AUX
- 12) GFX_CORE

AO6402 — Sheet 56 — 11
- 6) P3.3V_AUX
- 11) KBC3_PWRON
- 12) P3.3V

AO6402 — Sheet 56
- 8) P1.8V_AUX
- 11-1) KBC3_PWRON_INV#
- 12) P1.8V

RT9179
- 6) P3.3V_AUX
- 6-1) P1.2V_AUX

APL5336
- 8) P1.8V_AUX
- 6) P5.0V_AUX
- 8-1) P0.9V_AUX

RT9179
- 6) P5.0V_AUX
- 12) P2.5V

APW7141
- 11) KBC3_PWRON
- 2) VDC
- 12) P1.5V

APW7141
- 14) KBC3_VRON
- 2) VDC
- 15) P1.2V

APW7141
- 14) KBC3_VRON
- 2) VDC
- 15) P1.1V

RT8205A — P3.3V_AUX & P5V_AUX — 3
- P5.0V_STB
- P3.3V_MICOM — 6
- 6) P5.0V_AUX
- 6) P3.3V_AUX
- 7) AUX3_PWRGD — 7

ICSL6255 — AC_DC / Battery — 2
- Adapter
- Battery
- 2) VDC
- 2-1) P12.0V_ALW

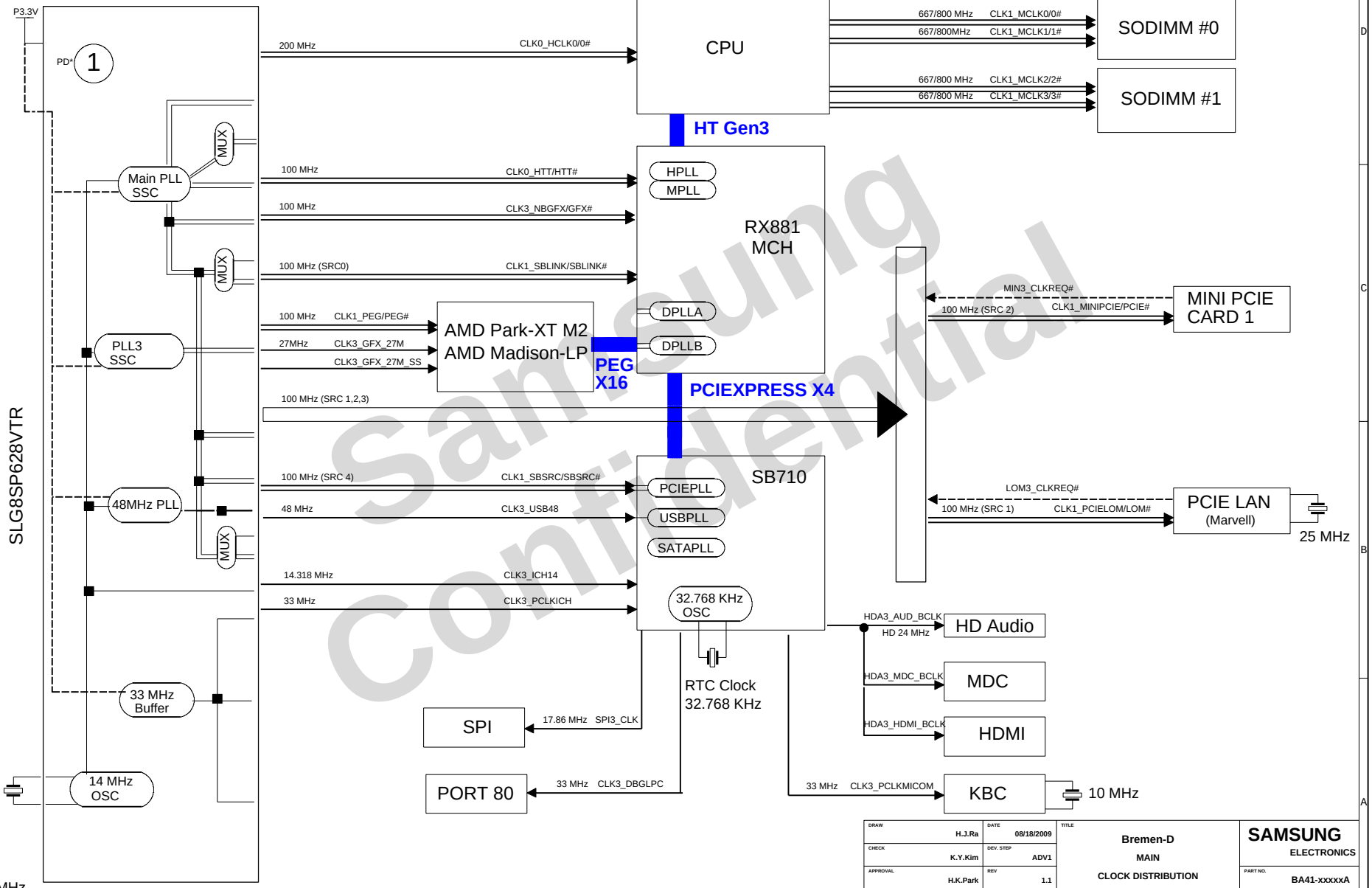
LOM Marvell — Sheet 39
- 6-1) P1.2V_LAN
- 6-1) P2.5V_LAN

- 3) P3.3V_MICOM
- 8) KBC3_SUSPWR
- 11) KBC3_PWRON
- 11-1) KBC3_PWRON_INV#



| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / MAIN / POWER SEQUENCE | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 6 OF 61 | |

# CLOCK DISTRIBUTION



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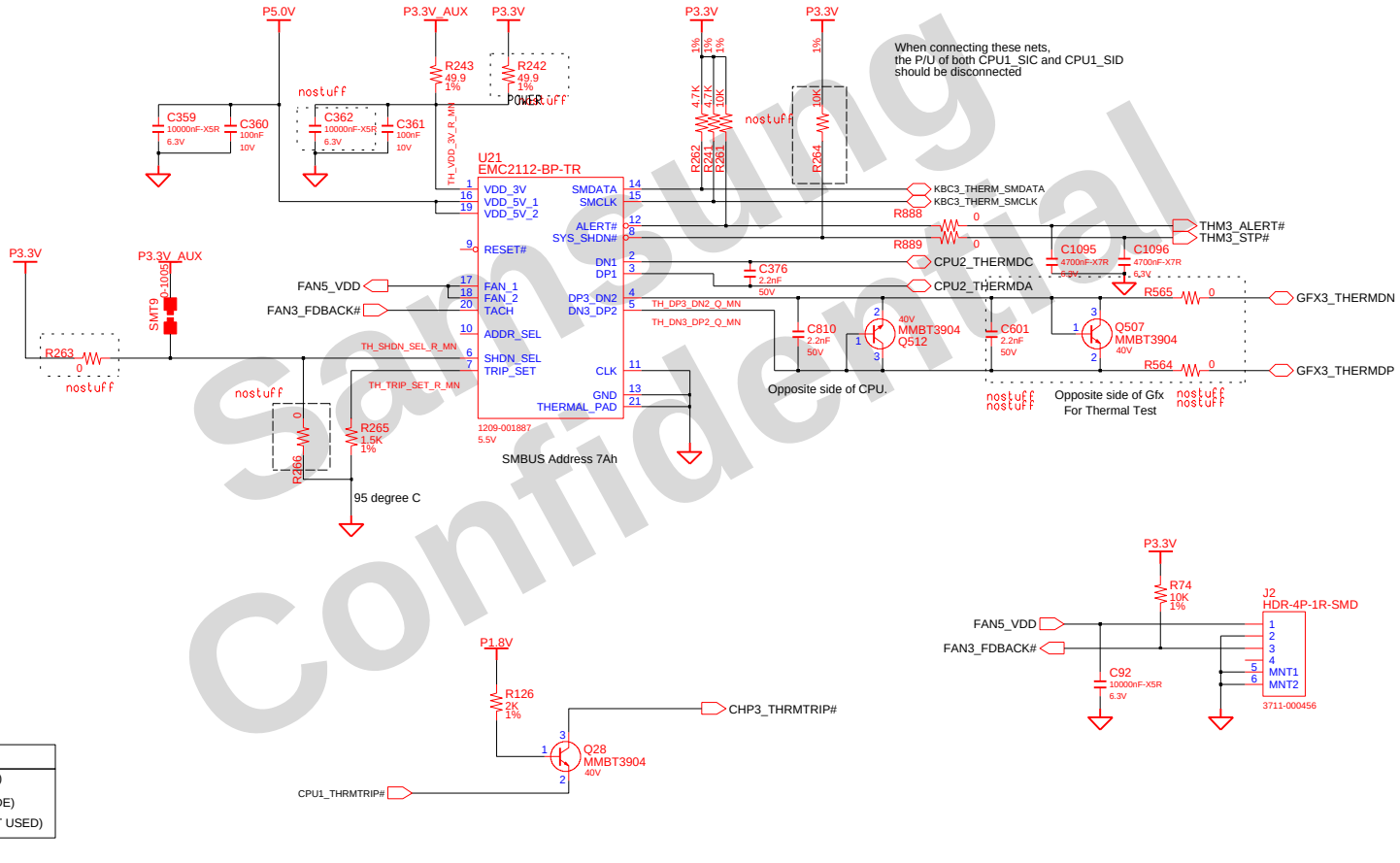
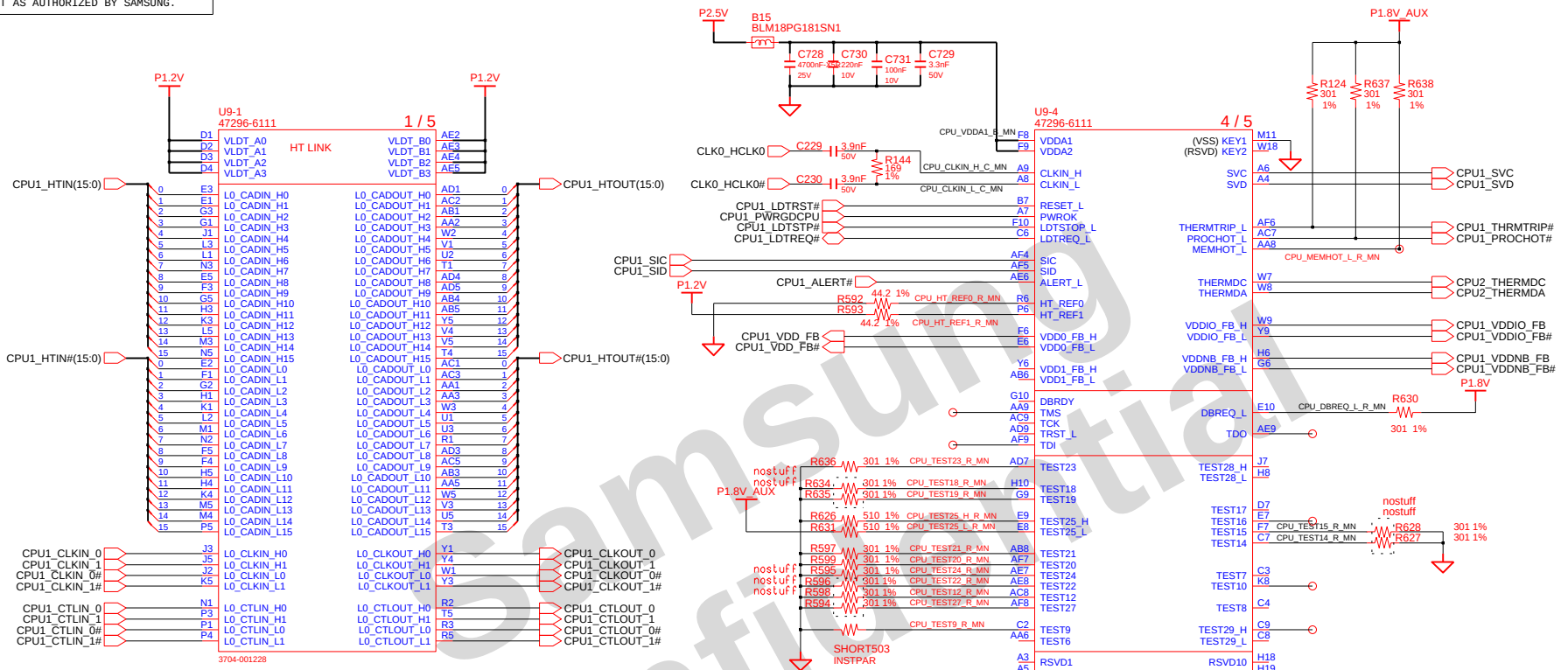
| DRAW H.J.Ra | DATE 08/18/2009 | TITLE Bremen-D MAIN CLOCK DISTRIBUTION | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 7 OF 61 | |

# THERMAL SENSOR & FAN CONTROL



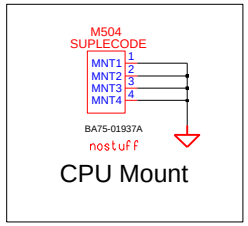

| SHDN_SEL MODE | |
|---|---|
| 0 | CH1(CPU MODE) |
| HIGH Z | CH3(DIODE MODE) |
| 1 | N/A (SHDN# NOT USED) |

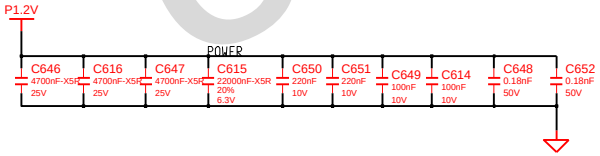
| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D THERMAL SENSOR THERMAL SENSOR EMC2112 | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 8 OF 61 | |

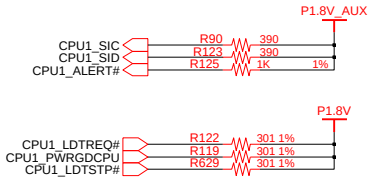


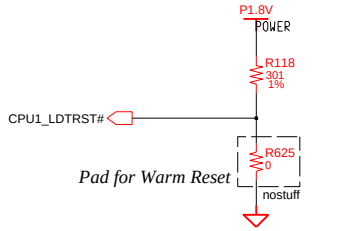

CPU Socket : 0185482000 (3704-001228)

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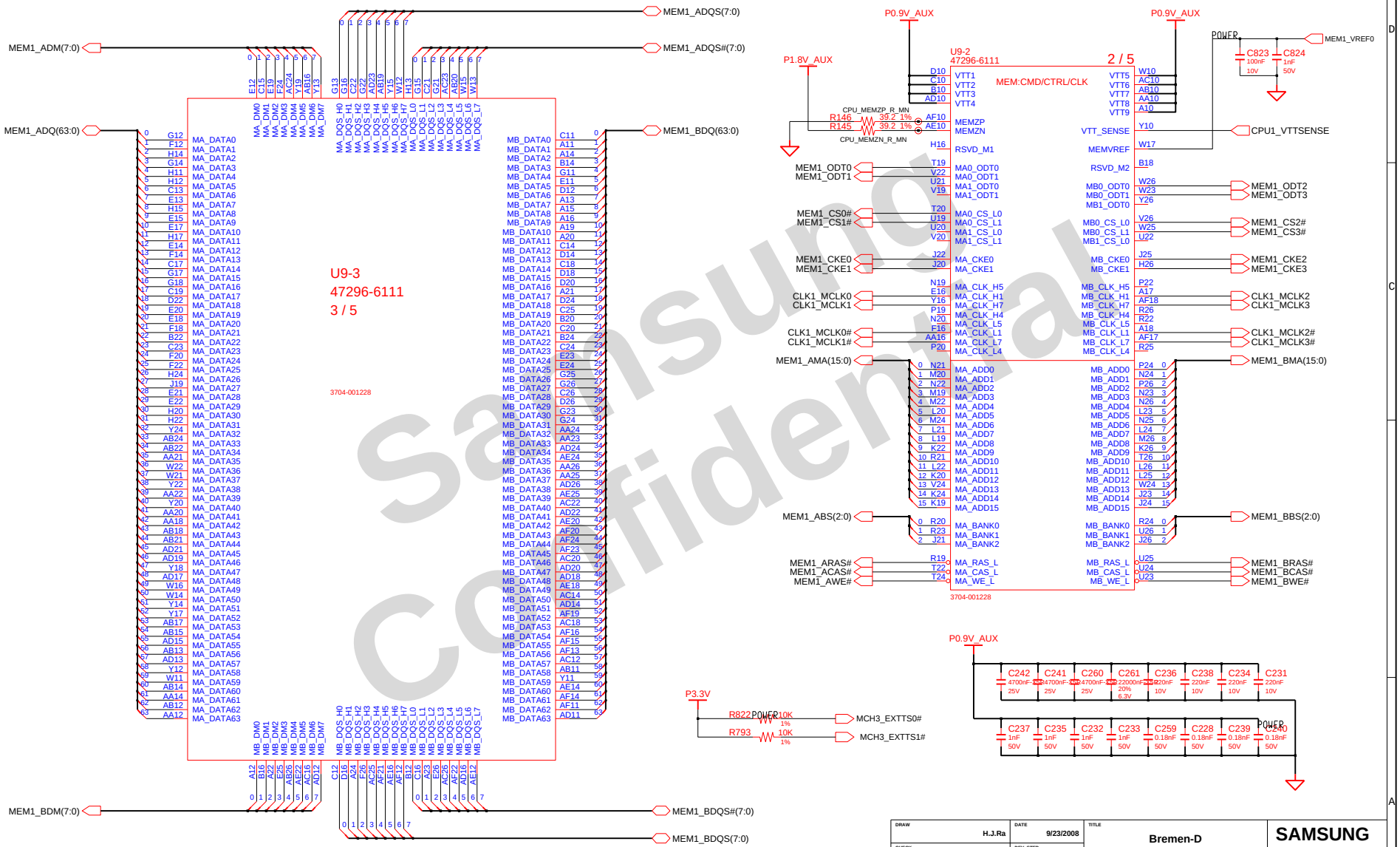
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / CPU / Caspian (1/3) | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 9 OF 61 | |

# CPU_Caspian



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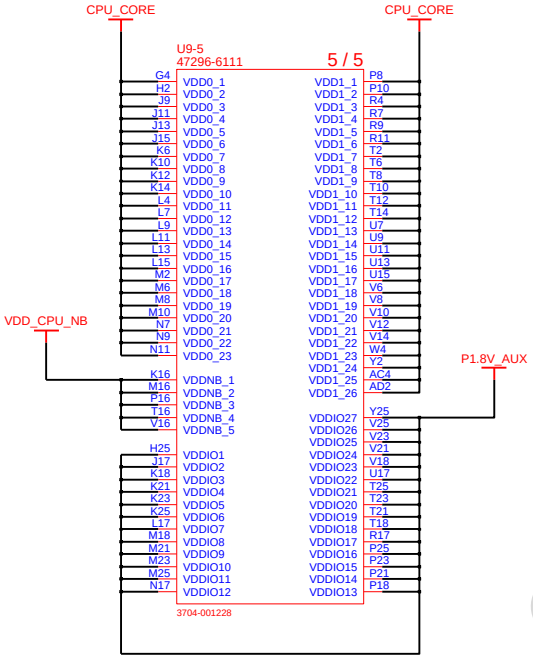
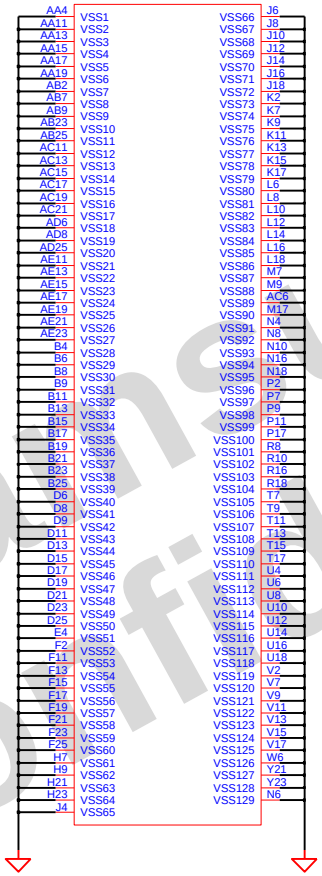
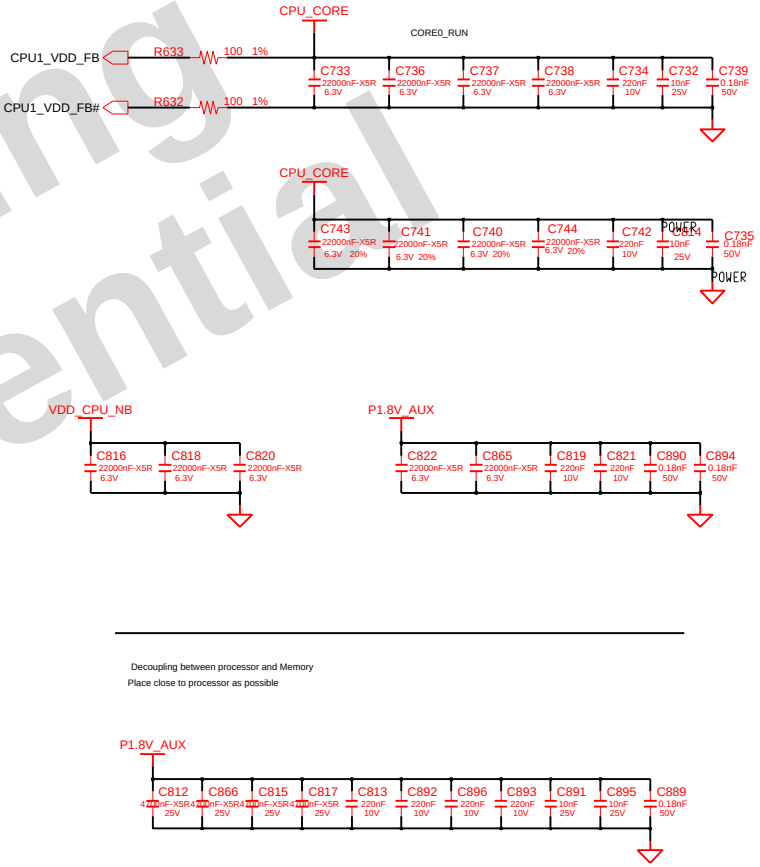
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D CPU Caspian (2/3) | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE undefined | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 10 OF 61 | |

# CPU_Caspian



## Bottom side decoupling

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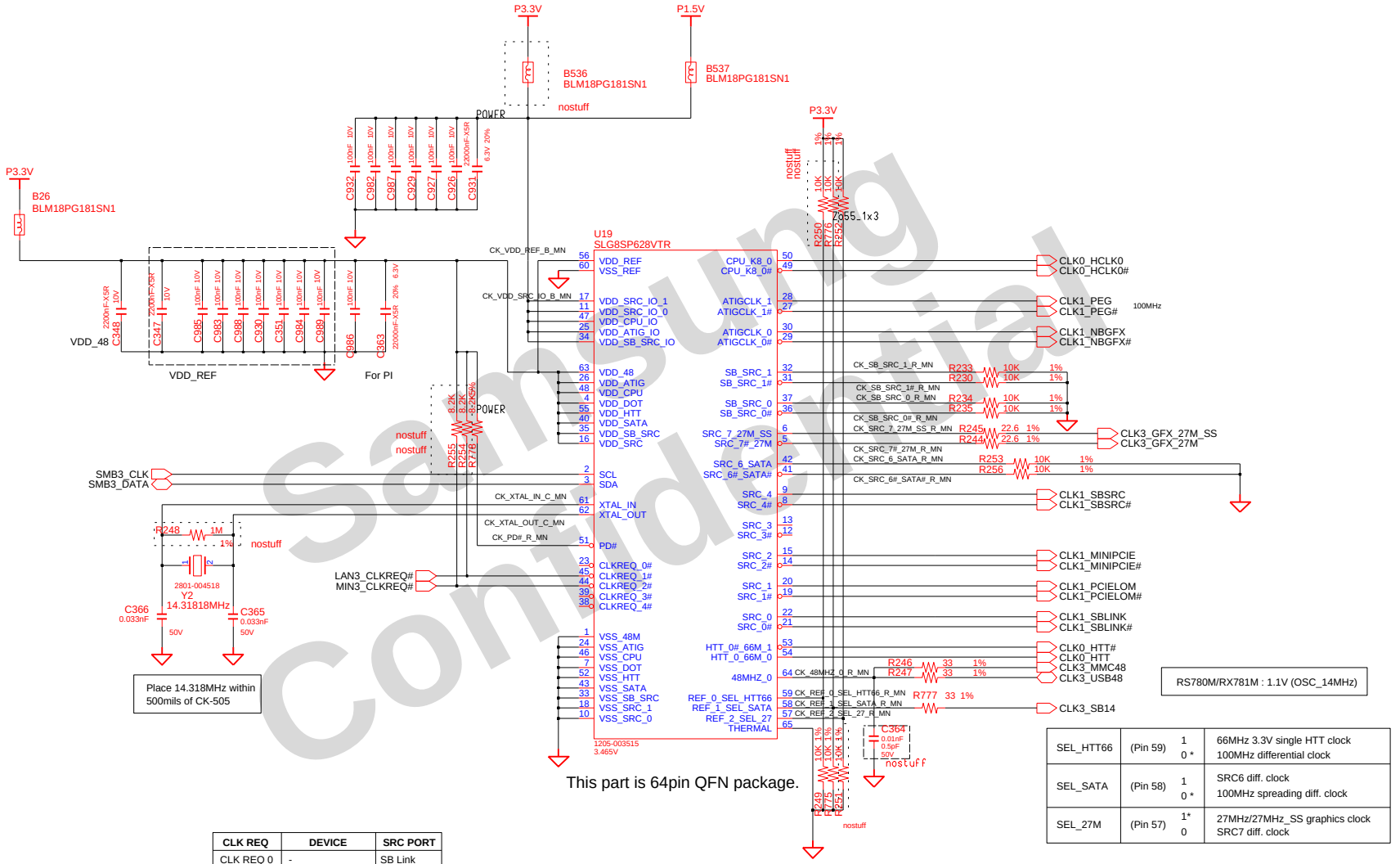
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 11 OF 61 | |

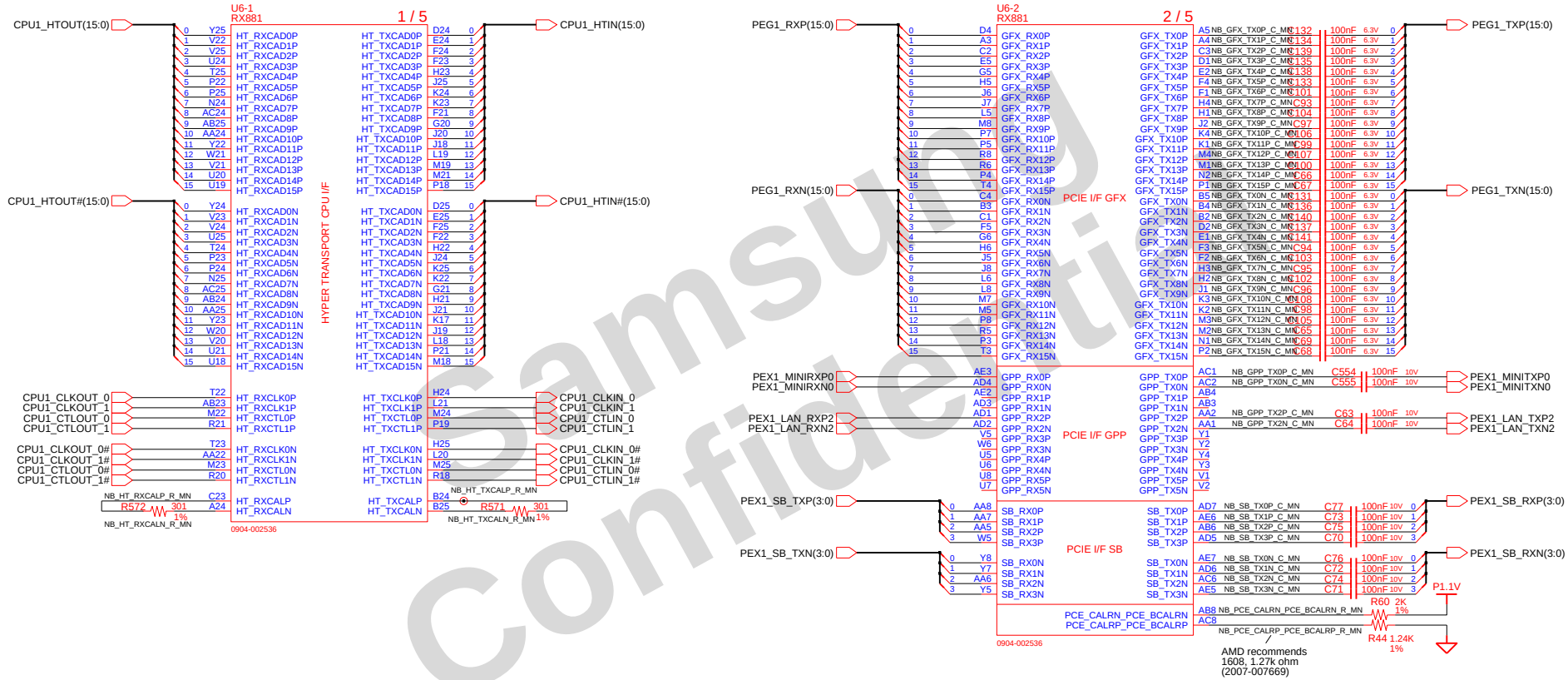



| CLK REQ | DEVICE | SRC PORT |
|---|---|---|
| CLK REQ 0 | - | SB Link |
| CLK REQ 1 | LOM3_CLKREQ# | LOM |
| CLK REQ 2 | MIN3_CLKREQ# | MINI CARD |
| CLK REQ 3 | | |
| CLK REQ 4 | - | SB_SRC |

| | | | |
|---|---|---|---|
| SEL_HTT66 | (Pin 59) | 1<br>0 * | 66MHz 3.3V single HTT clock<br>100MHz differential clock |
| SEL_SATA | (Pin 58) | 1<br>0 * | SRC6 diff. clock<br>100MHz spreading diff. clock |
| SEL_27M | (Pin 57) | 1*<br>0 | 27MHz/27MHz_SS graphics clock<br>SRC7 diff. clock |

| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D<br>MAIN_CLOCK_CIRCUIT<br>CK_Clock_505M | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE undefined | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 12 OF 61 | |

# NB_ RX881_AMD

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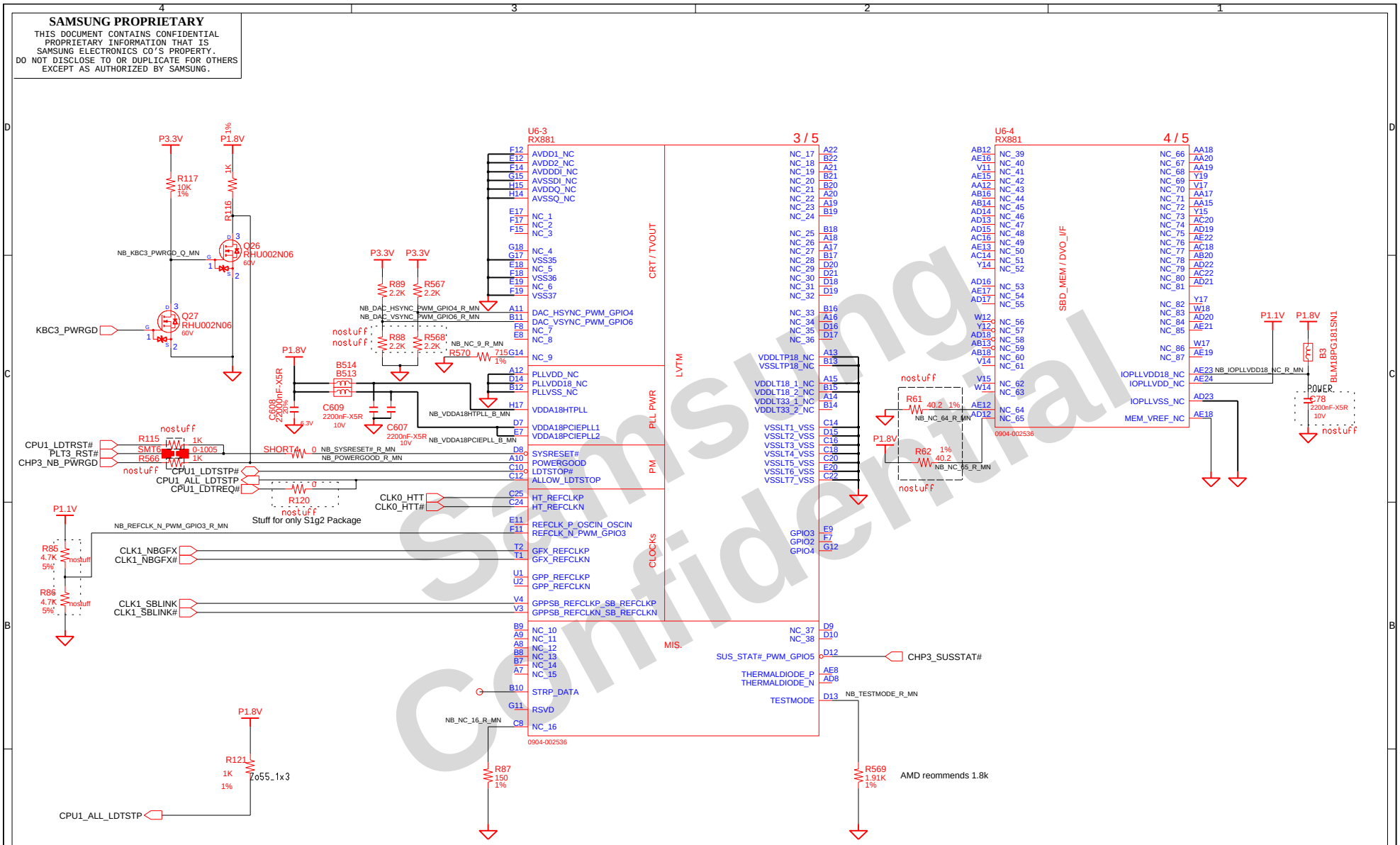
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / MCH_DDR2 / RX881 (1/3) | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 13 OF 61 | |




| | | | |
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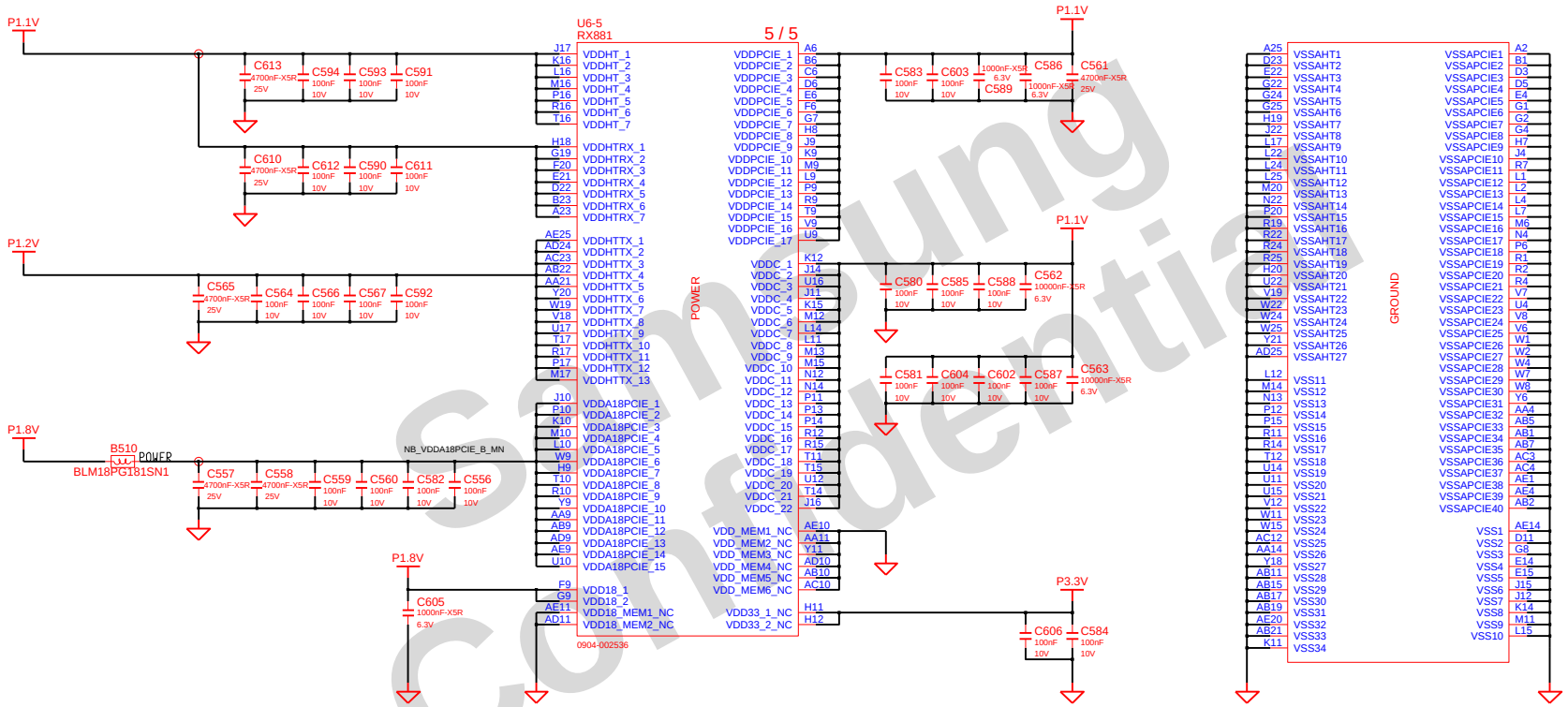
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 14 OF 61 | |



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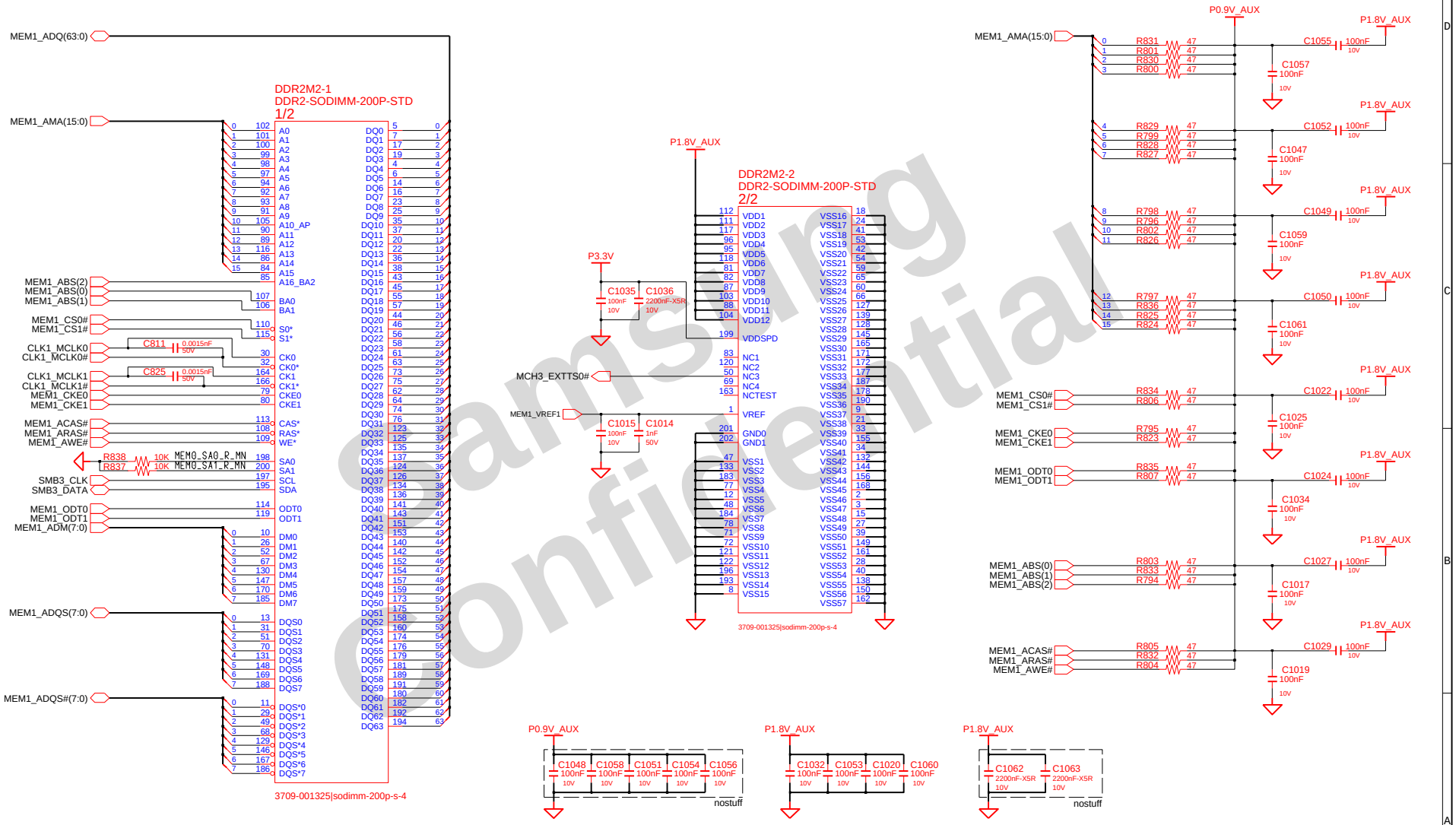
| CHECK K.Y.Kim | DEV. STEP ADV1 | | PART NO. BA41-xxxxxA |
| APPROVAL H.K.Park | REV 1.1 | | |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 15 OF 61 | |

# DDR SO-DIMM #0






| | | | |
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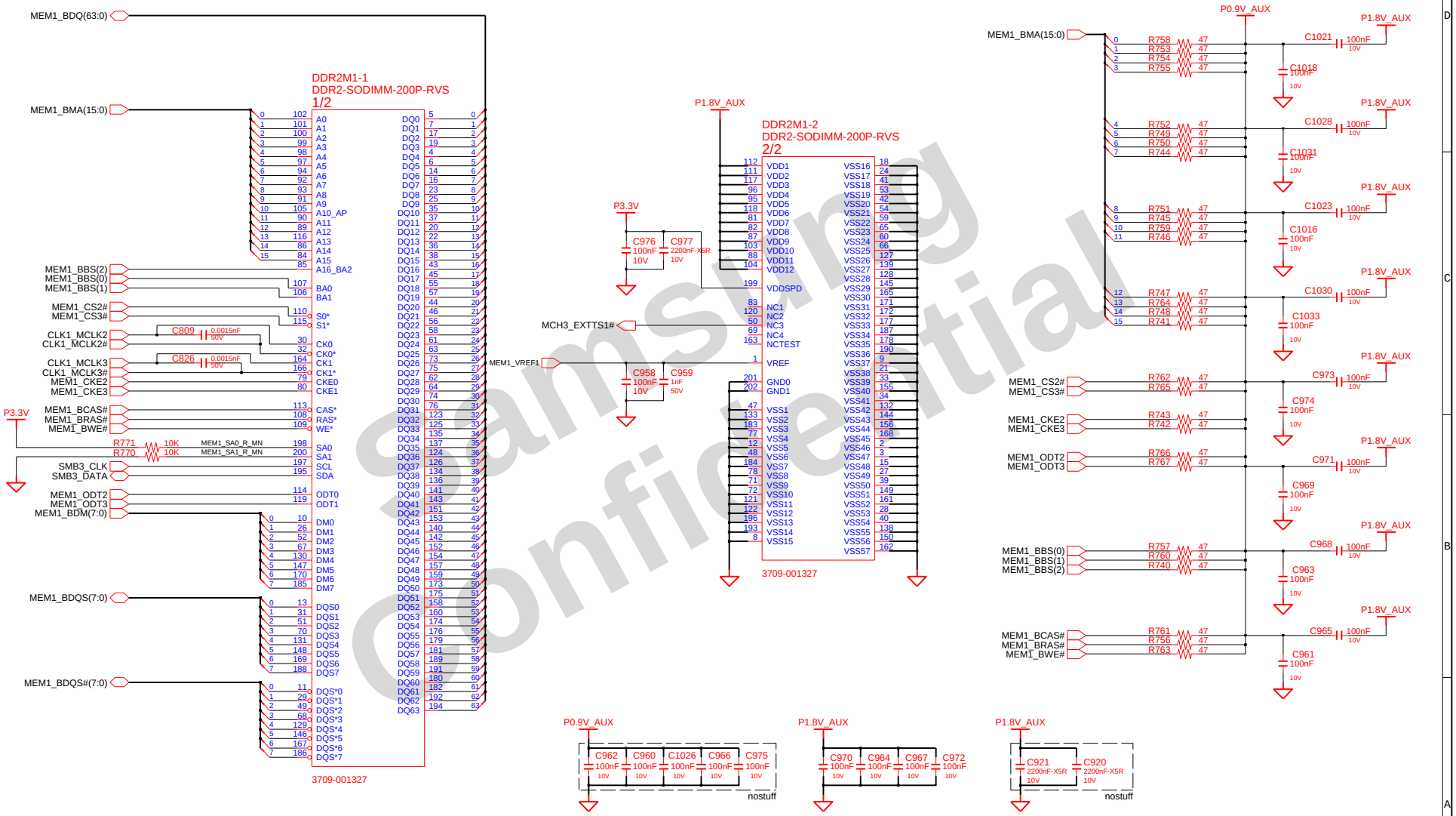
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D SODIMM_DDR2 SODIMM_DDR2 (1/2) | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 16 OF 61 | |

# DDR SO-DIMM #1

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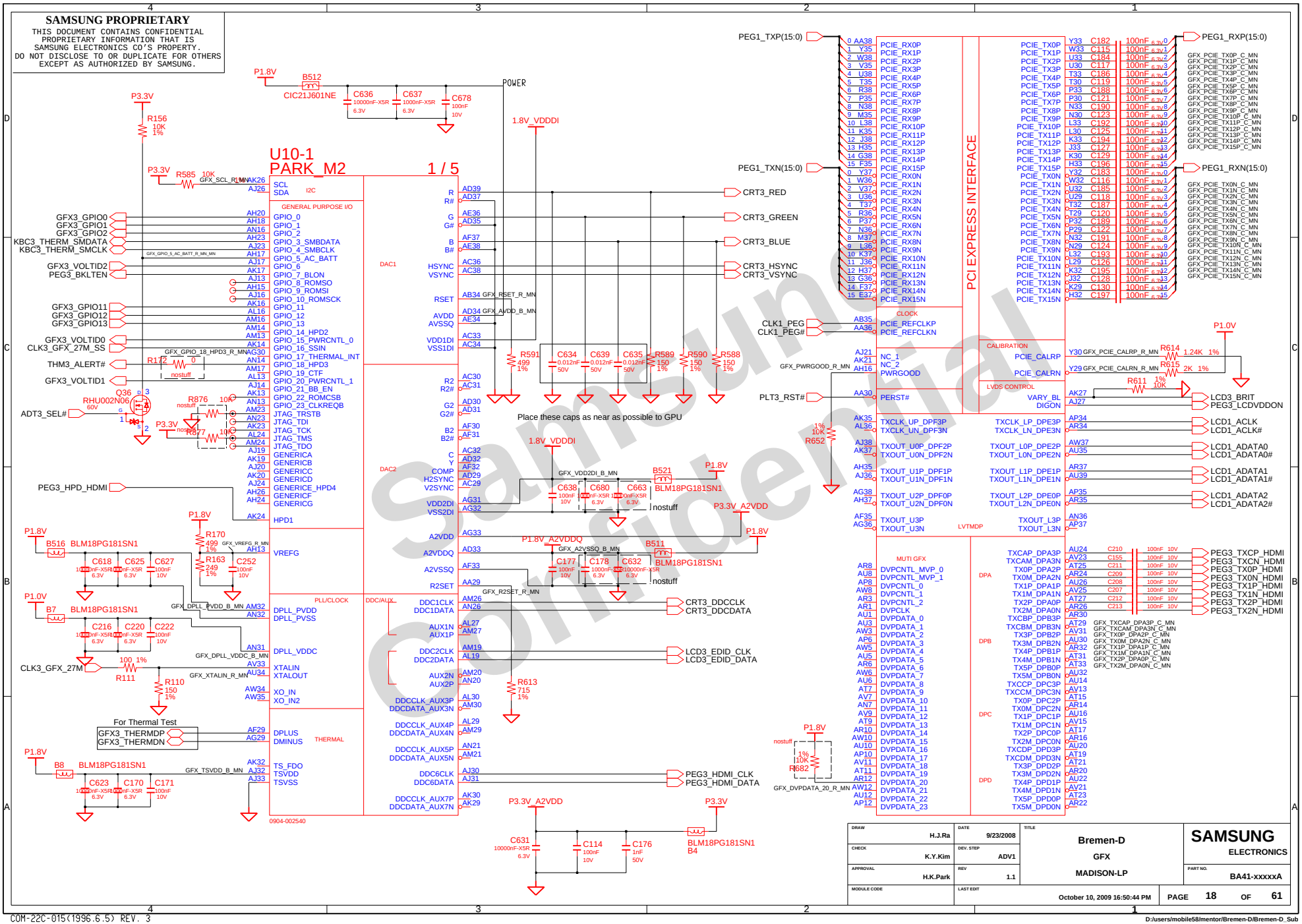
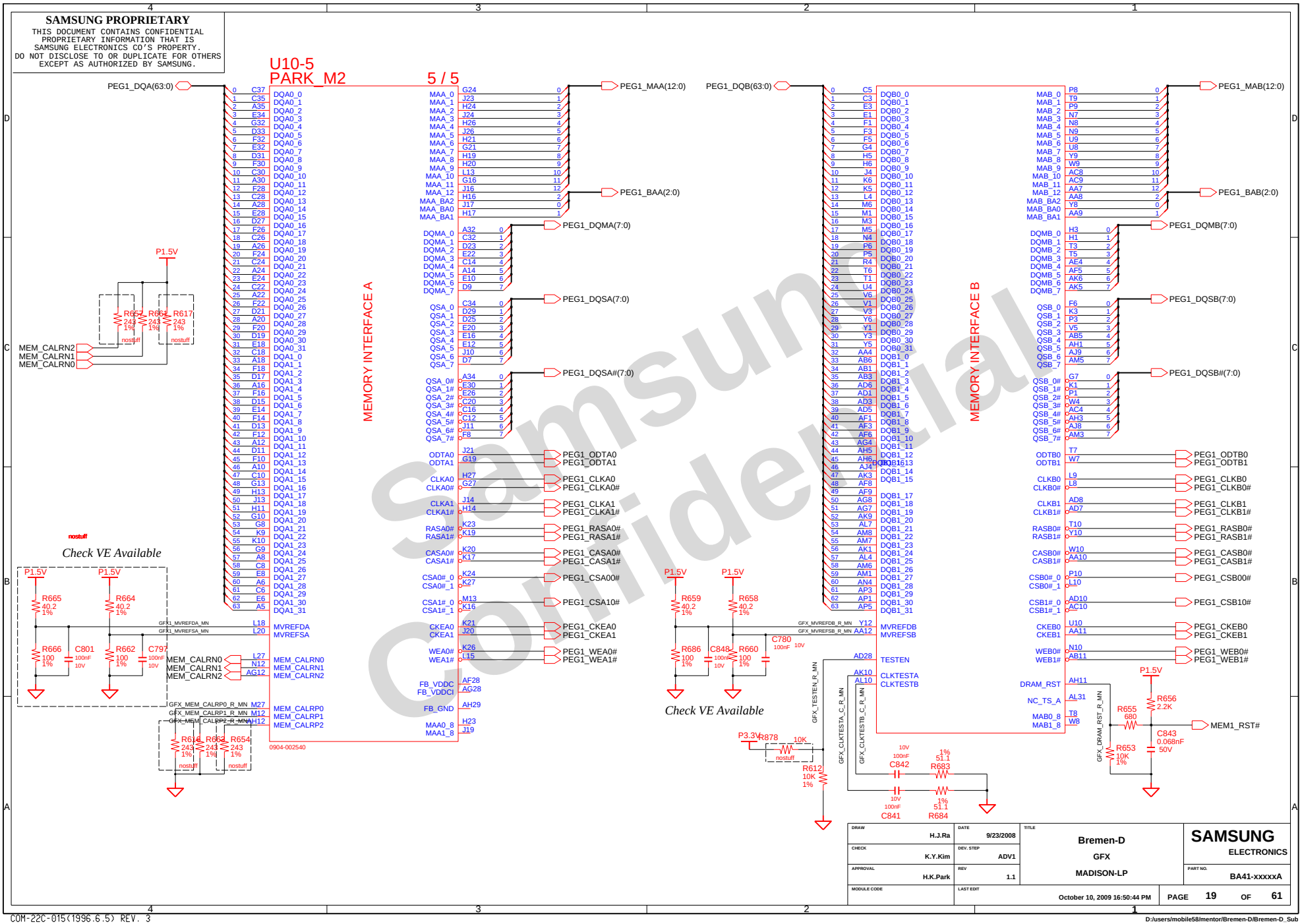
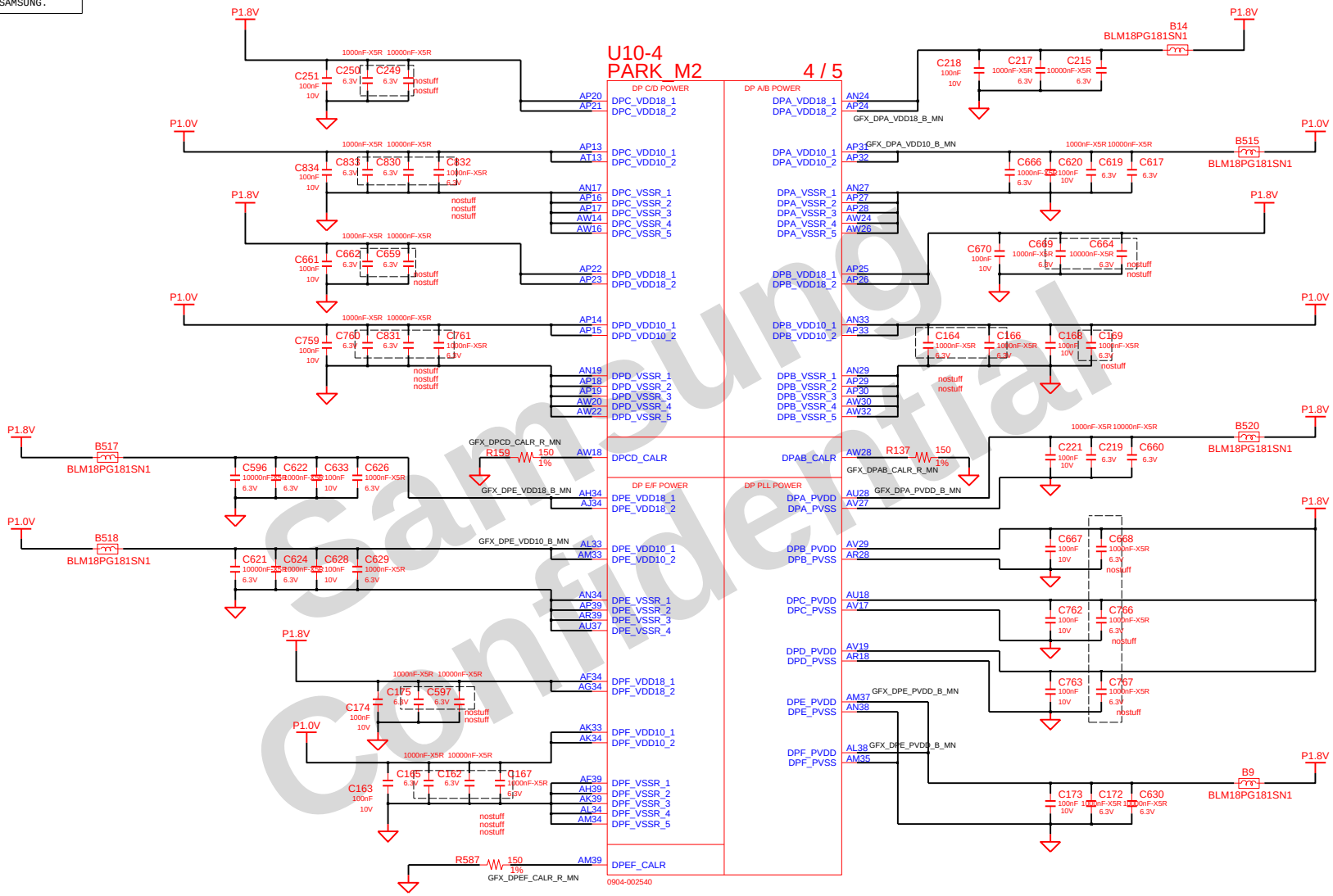
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D SODIMM_DDR2 SOCIMM_DDR2 (2/2) | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 17 OF 61 | |







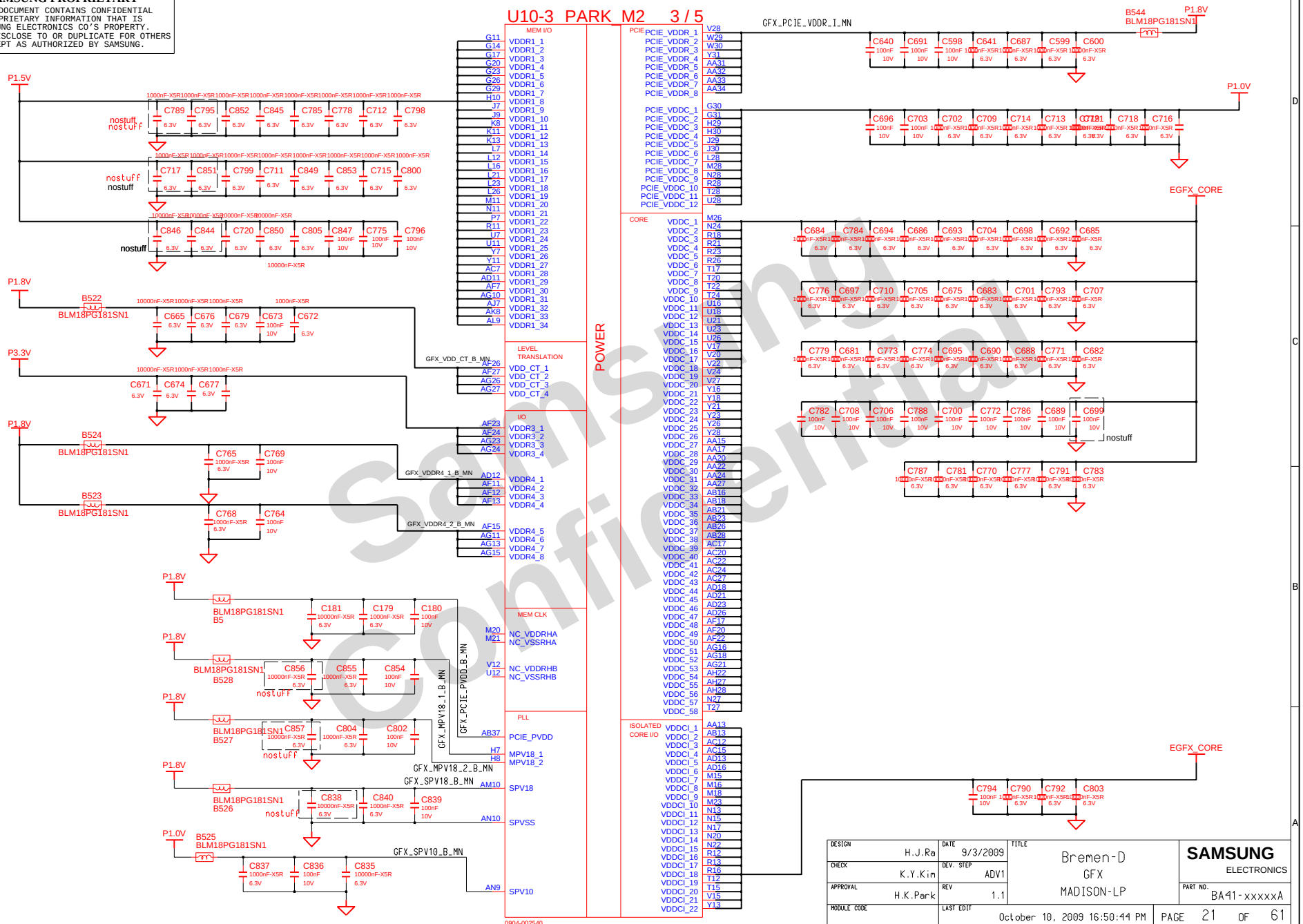

| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D GFX MADISON-LP | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 19 OF 61 | |





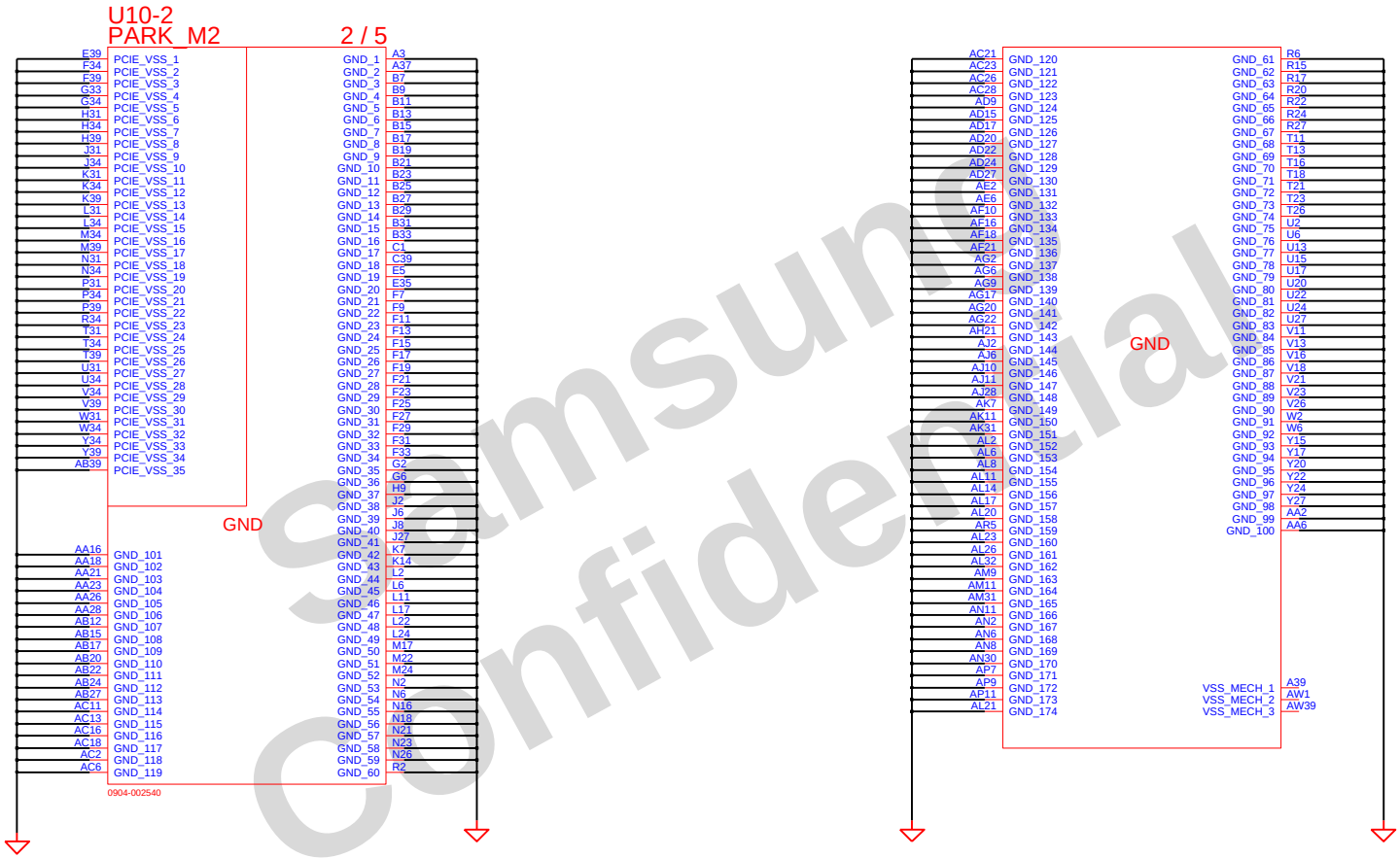

| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/3/2009 | TITLE: Bremen-D GFX MADISON-LP | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 20 OF 61 | |

# U10-3 PARK_M2 3 / 5






| | | | |
|---|---|---|---|
| DESIGN H.J.Ra | DATE 9/3/2009 | TITLE Bremen-D GFX MADISON-LP | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 21 OF 61 | |



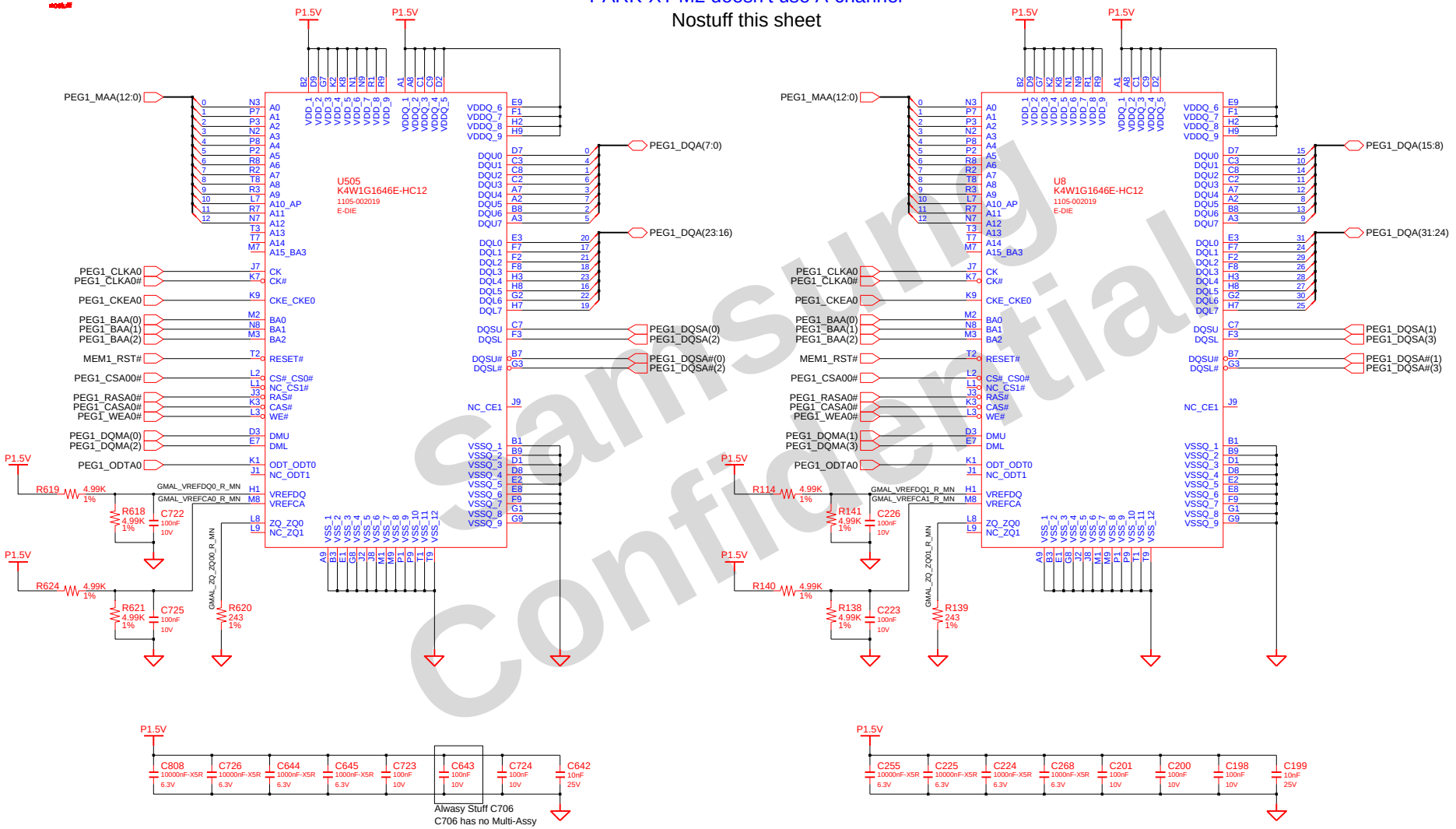



| | | | |
|---|---|---|---|
| DESIGN H.J.Ra | DATE 9/3/2009 | TITLE Bremen-D GFX MADISON-LP | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 22 OF 61 | |

# A-channel Lower Data

PARK-XT M2 doesn't use A-channel

Nostuff this sheet



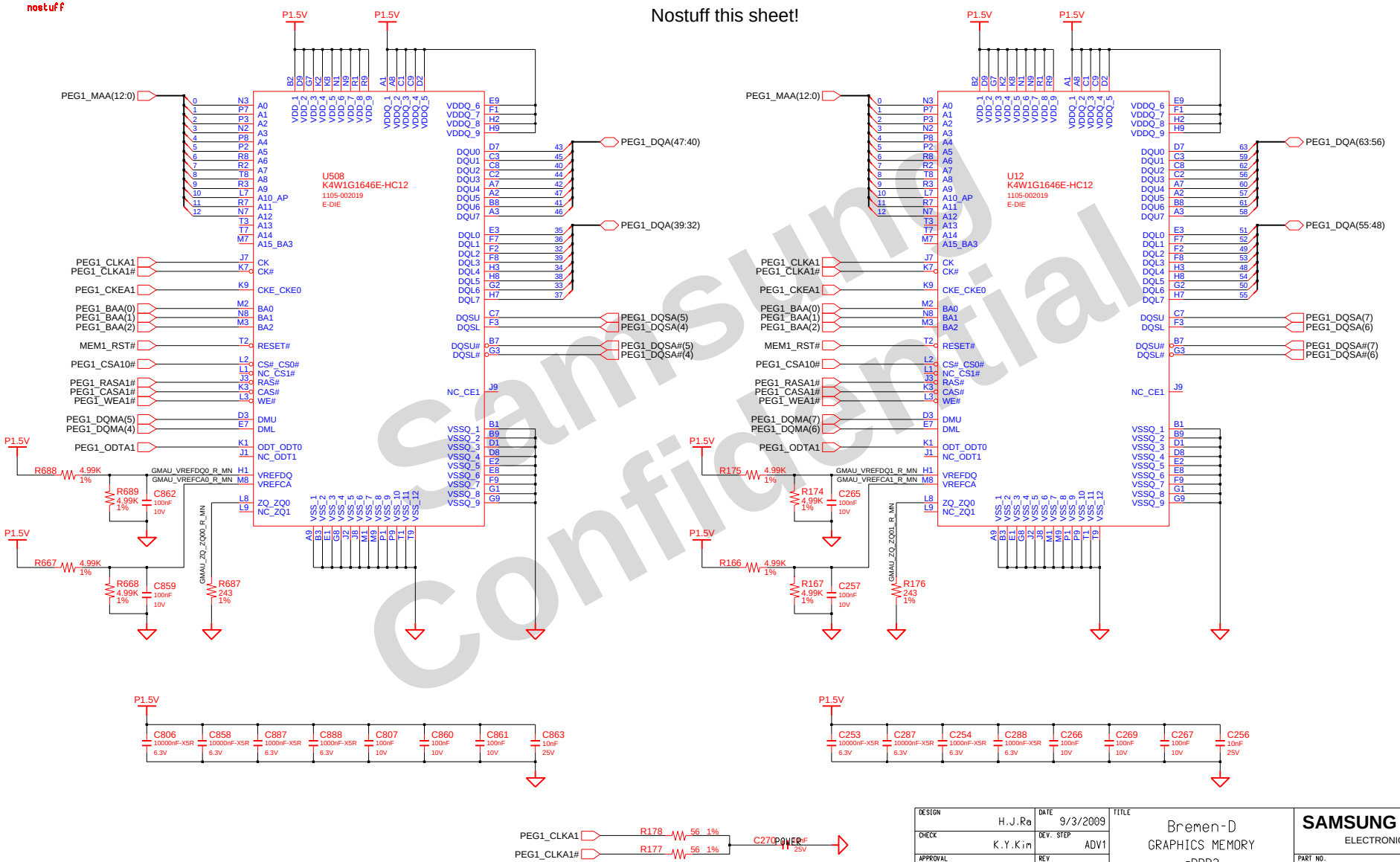



| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/3/2009 | TITLE: Bremen-D GRAPHICS MEMORY gDDR3 | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | PART NO.: BA41-xxxxxA |
| APPROVAL: H.K.Park | REV: 1.1 | | |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 23 OF 61 | |

# A-channel Upper Data

## PARK-XP M2 doesn't use A-channel

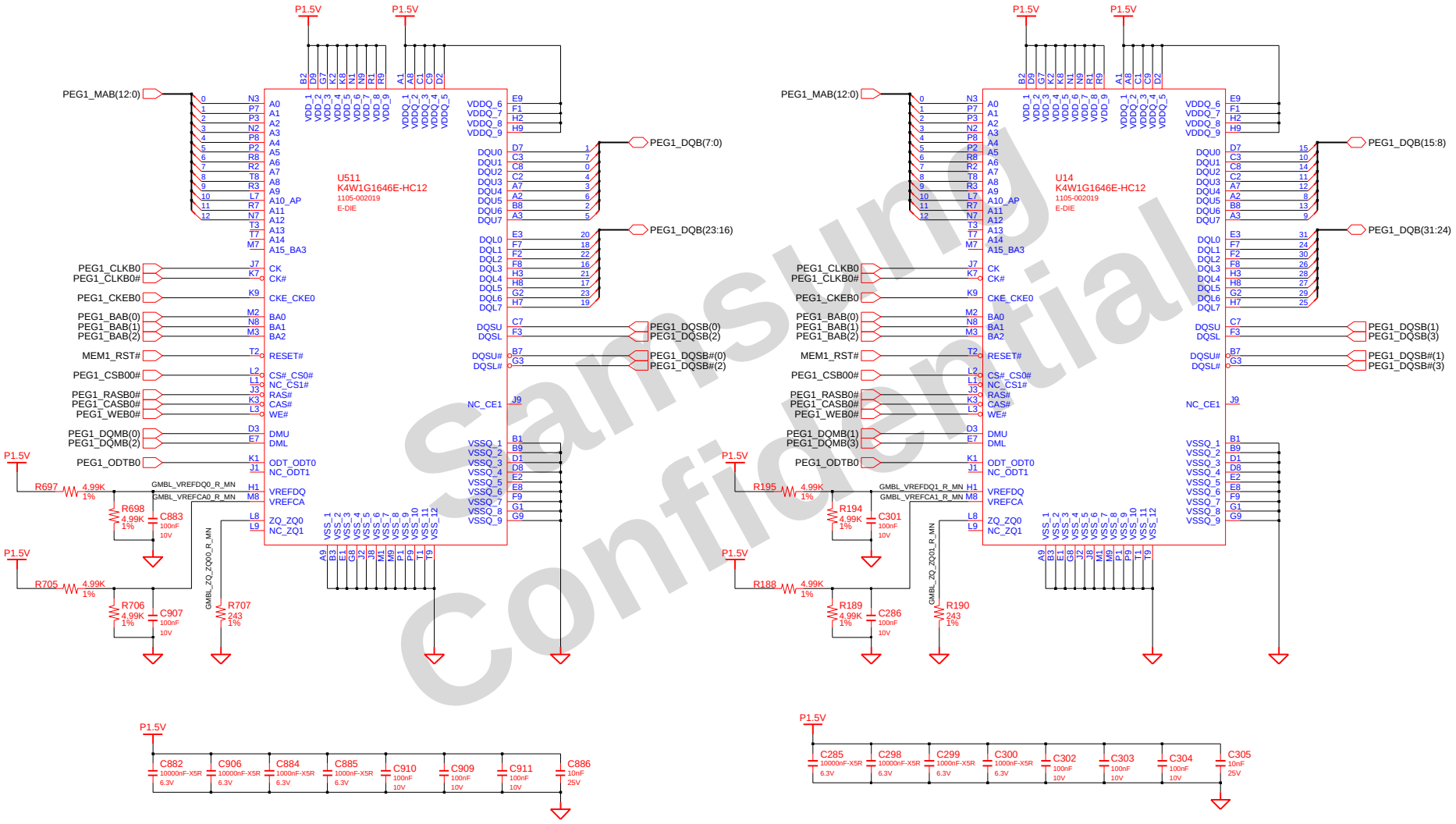
Nostuff this sheet!






| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/3/2009 | TITLE: Bremen-D GRAPHICS MEMORY gDDR3 | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 24 OF 61 | |

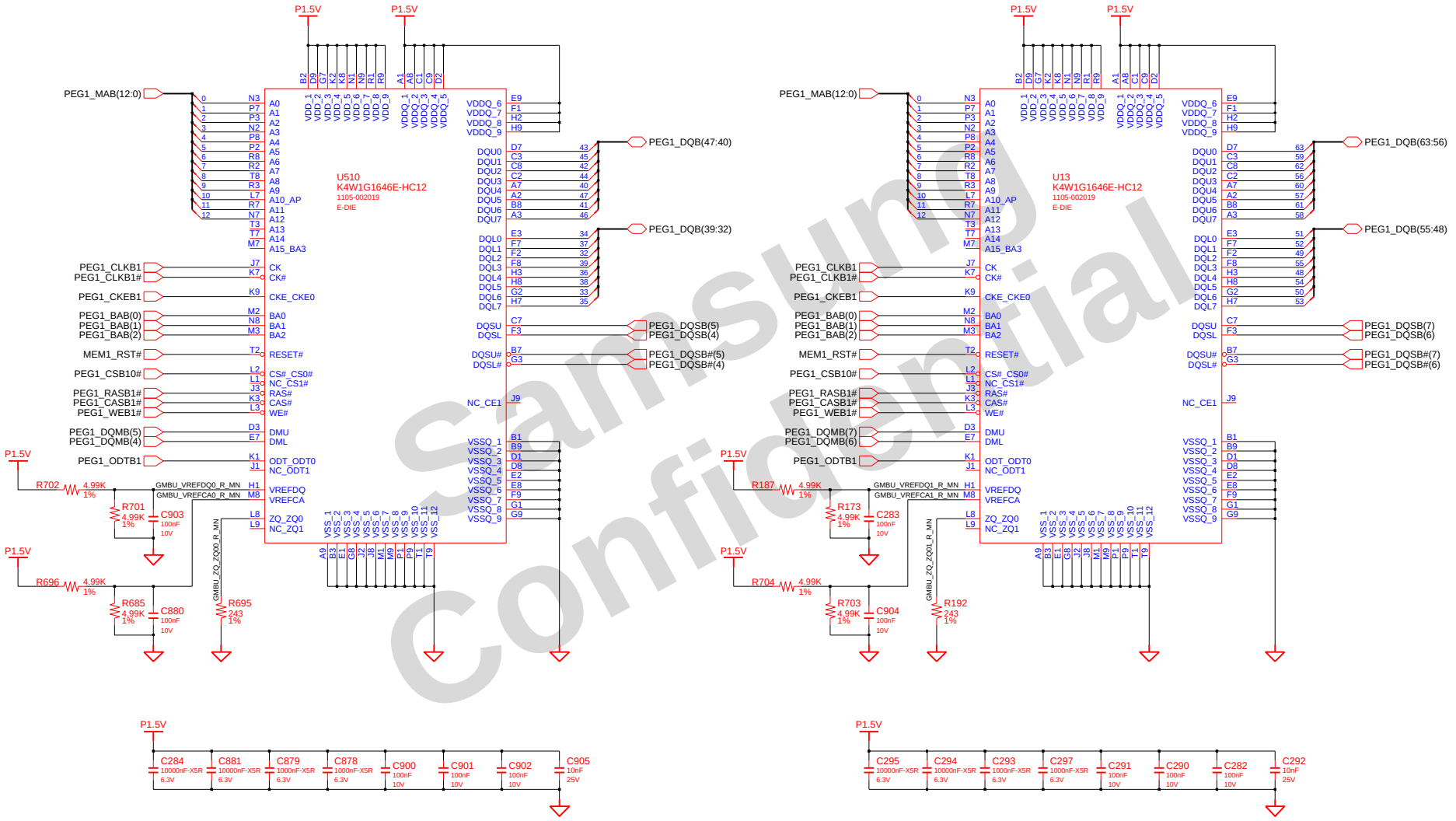
# B-channel Lower Data






| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/3/2009 | TITLE: Bremen-D GTAPHICS MEMORY gDDR3 | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 25 OF 61 | |

# B-channel Upper Data





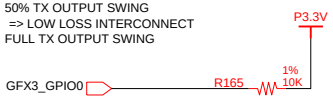

| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/3/2009 | TITLE: Bremen-D GRAPHICS MEMORY gDDR3 | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | PART NO.: BA41-xxxxxA |
| APPROVAL: H.K.Park | REV: 1.1 | | |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 26 OF 61 | |

# Park XT Straps

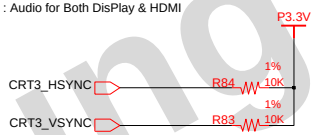
TX_PWRS_ENB

PCIE FULL TX OUTPUT SWING (Internal P/D)

0 : 50% TX OUTPUT SWING
=> LOW LOSS INTERCONNECT
1 : FULL TX OUTPUT SWING




AUD[1:0] (Internal P/D)
00 : No Audio Function
01 : Audio for DisplayPort only
10 : Audio for DisplayPort and HDMI if dongle is detected
11 : Audio for Both DisPlay & HDMI

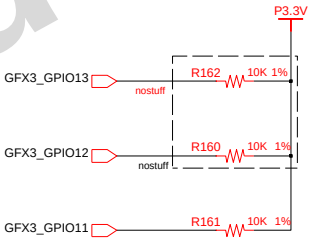



TX_DEEMPH_EN

PCIE TRANSMITTER DE-EMPHASIS ENABLE (Internal P/D)
0 : TX DE-EMPHASIS Disabled (eg. on-board)
1 : TX DE-EMPHASIS Enabled (eg. MXM)

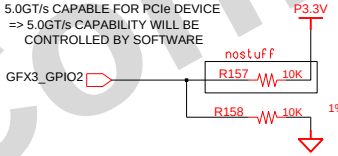

BIOS_ROM_EN => GPIO_22_ROMCSB (Internal P/D)
If BIOS_ROM_EN=1, ROMCFGID[2:0] (Internal P/D)
If BIOS_ROM_EN=0, Memory Aperture Size (Internal P/D)

GFX3_GPIO(13 : 11)
000 : 128MB
001 : 256MB
010 : 64MB
011 : RESERVED
1XX : RESERVED



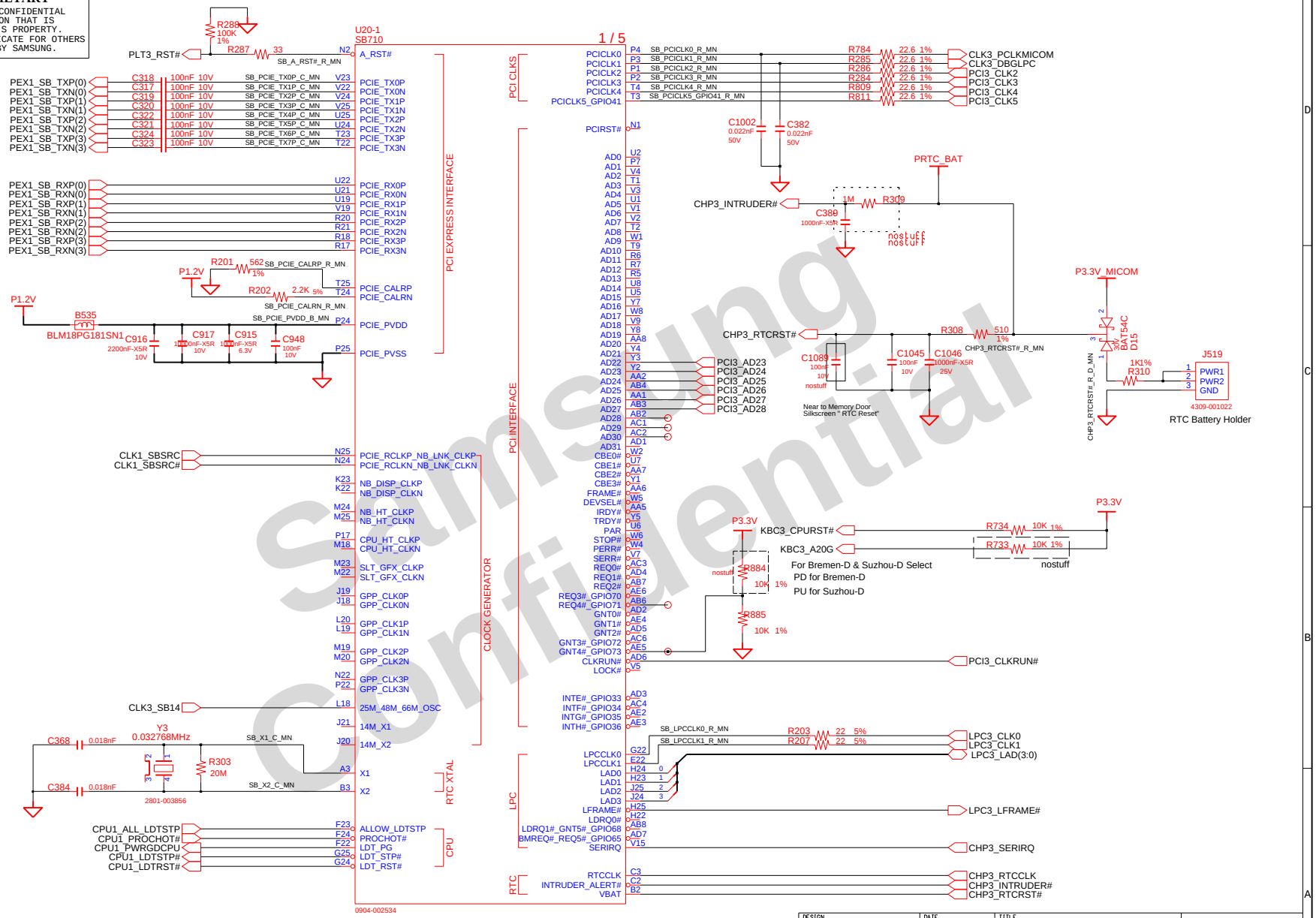

BIF_GEN2_EN_A

0 : 2.5GT/s CAPABLE FOR PCIe DEVICE
1 : 5.0GT/s CAPABLE FOR PCIe DEVICE
=> 5.0GT/s CAPABILITY WILL BE CONTROLLED BY SOFTWARE



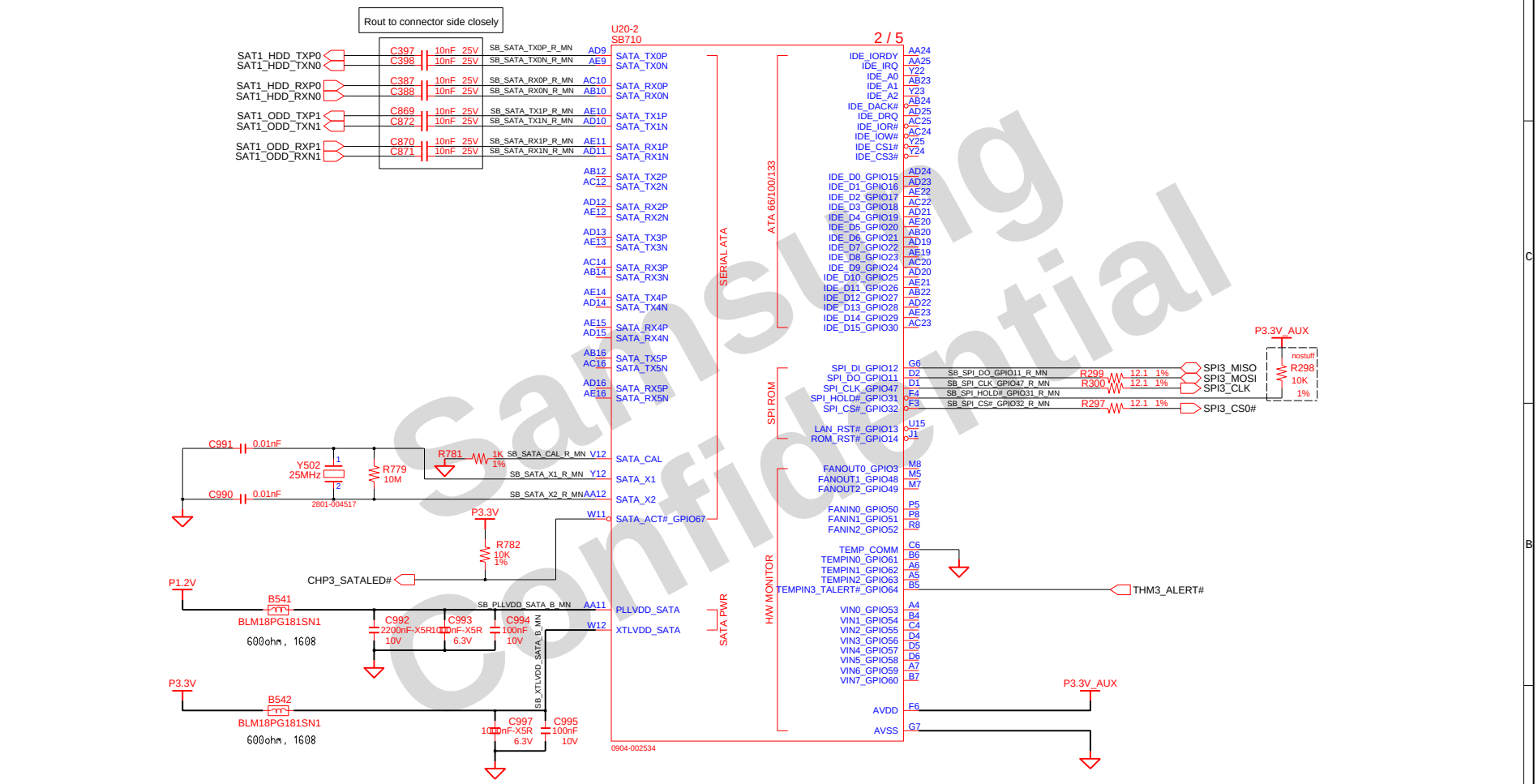



| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/3/2009 | TITLE: Bremen-D GFX MADISON-LP | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 27 OF 61 | |



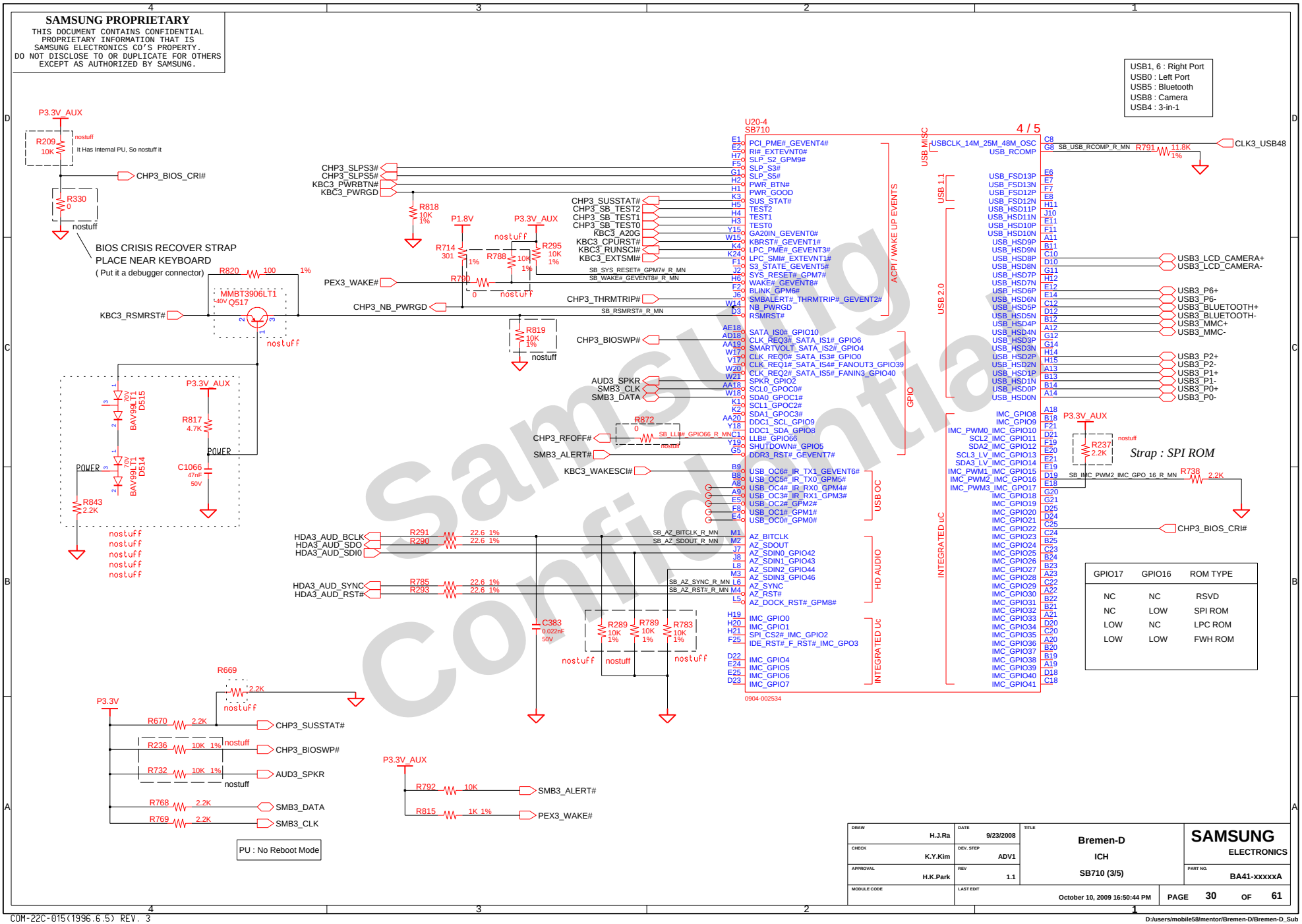



| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/3/2009 | TITLE: Bremen-D ICH SB710 (1/5) | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 28 OF 61 | |



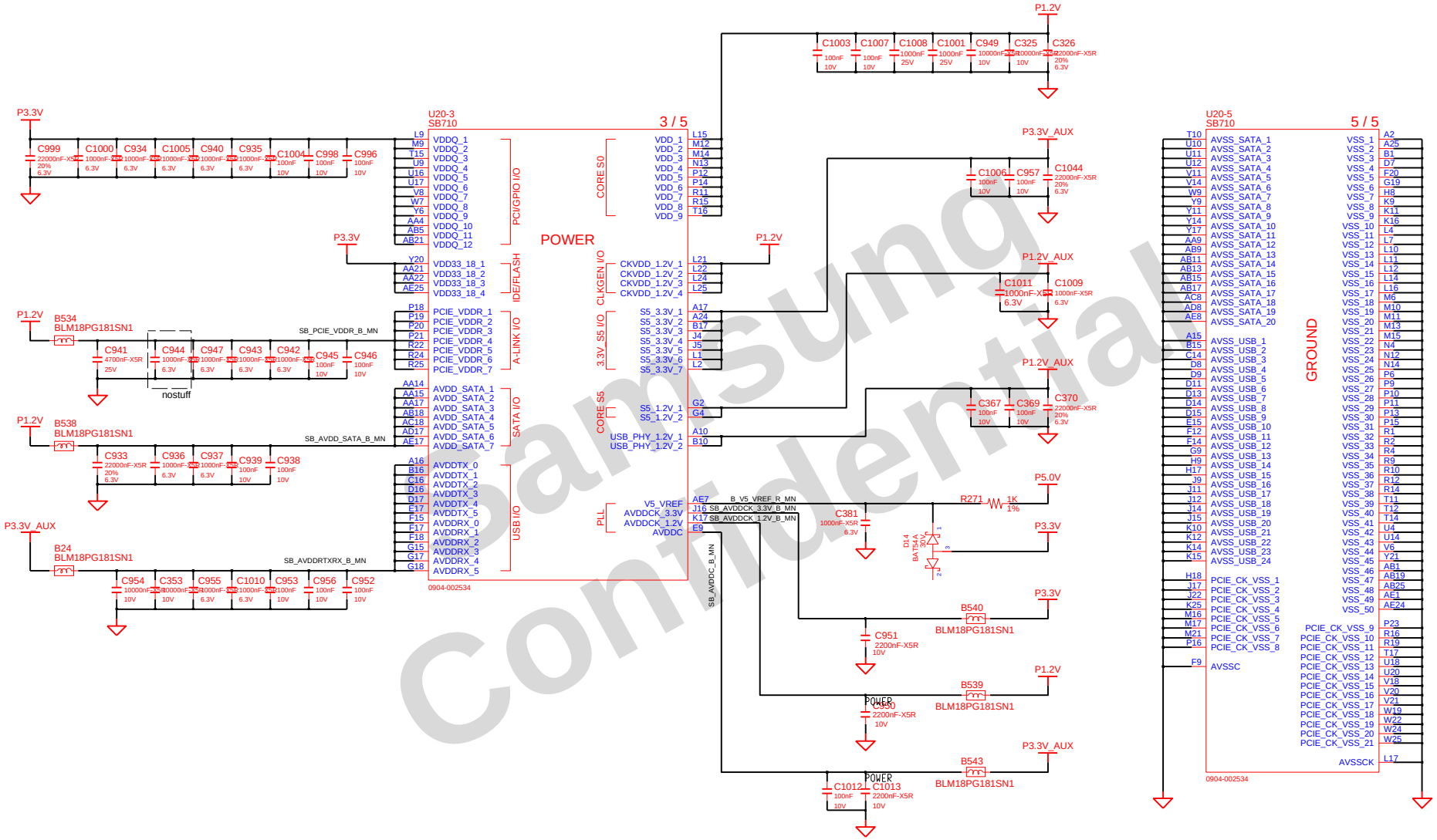



| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/3/2009 | TITLE: Bremen-D ICH SB710 (2/5) | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | PART NO.: BA41-xxxxxA |
| APPROVAL: H.K.Park | REV: 1.1 | | |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 29 OF 61 | |



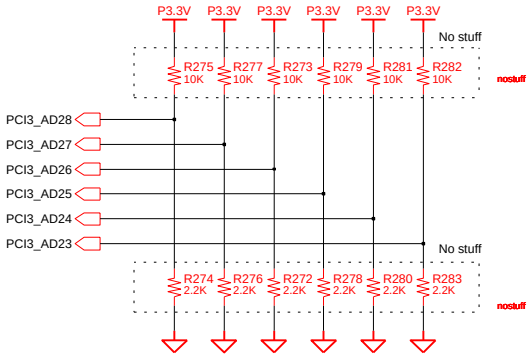


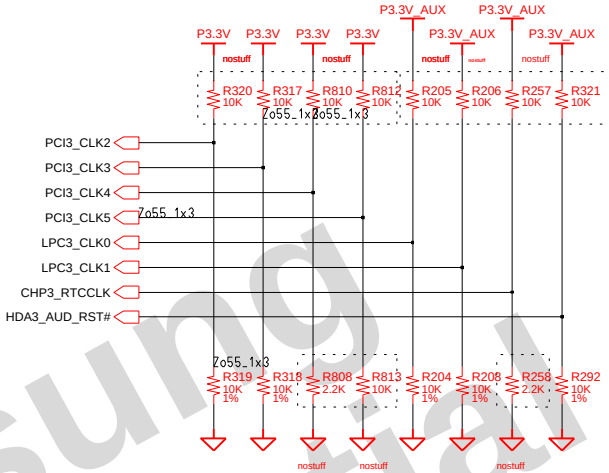

| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D ICH SB710 (3/5) | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 30 OF 61 | |






| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D ICH SB710 (4/5) | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE undefined | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 31 OF 61 | |

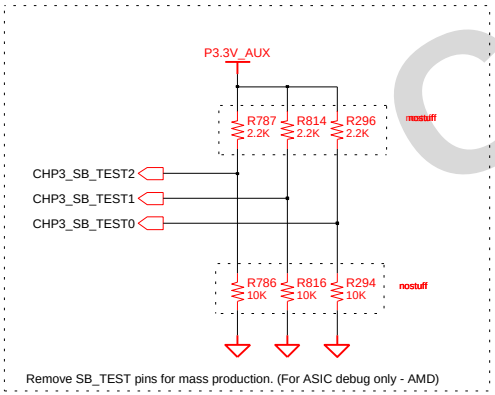



## DEBUG STRAPS

| | PCI3_AD(28) | PCI3_AD(27) | PCI3_AD(26) | PCI3_AD(25) | PCI3_AD(24) | PCI3_AD(23) |
|---|---|---|---|---|---|---|
| STRAP HIGH | USE LONG RESET | USE PCI PLL | USE ACPI BCLK | USE IDE PLL | USE DEFAULT PCIE STRAPS | BOOTFAILTIMER DISABLED |
| STRAP LOW | USE SHORT RESET | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | USE EEPROM PCIE STRAPS | BOOTFAILTIMER ENABLED |

| | PCI3_CLK2 | PCI3_CLK3 | PCI3_CLK4 | PCI3_CLK5 | LPC3_CLK0 | LPC3_CLK1 | RTC_CLK | AUD_RST# |
|---|---|---|---|---|---|---|---|---|
| STRAP HIGH | BOOTFAIL TIMER ENABLED | USER DEBUG STRAPS | RESERVED | RESERVED | EC ENABLED | CLKGEN ENABLED | INTERNAL RTC | ENABLE PCI MEM BOOT |
| STRAP LOW | BOOTFAIL TIMER DISABLED | IGNORE DEBUG STRAPS | RESERVED | RESERVED | EC DISABLED | CLKGEN DISABLED | EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK) | DISABLE PCI MEM BOOT |



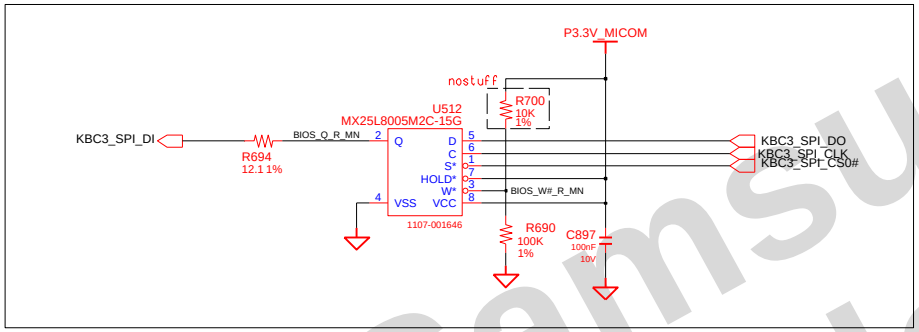

Remove SB_TEST pins for mass production. (For ASIC debug only - AMD)



| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / ICH / SB710 STRAPS (5/5) | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 32 OF 61 | |

# SPI_BIOS_ROM

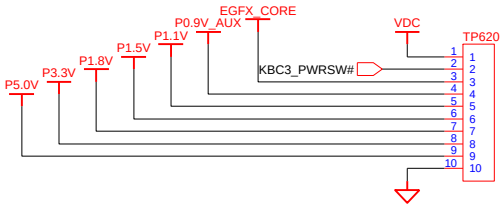
8MBit



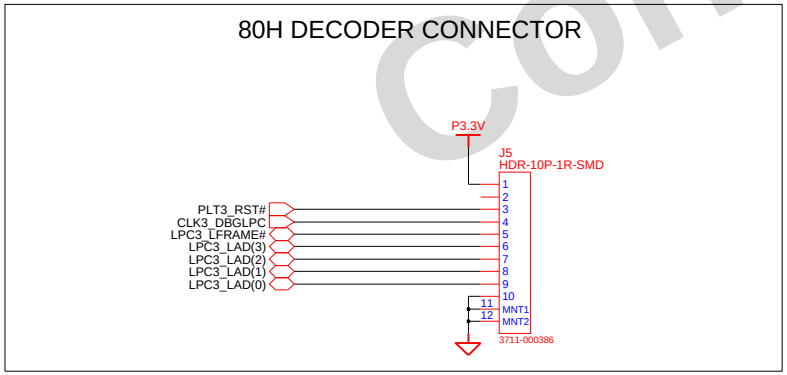

| | |
|---|---|
| 02 VERIFY REAL MODE | 66 CONFIGURE ADVANCE CACHE REG. |
| 03 DISABLE NMI | 6A DISPLAY EXTERNAL CACHE SIZE |
| 04 GET CPU TYPE | 6C DISPLAY SHADOW MESSAGE |
| 06 INIT. SYSTEM H/W | 6E DISPLAY NON-DISPOSABLE SEGMENT |
| 08 INIT. CHIPSET REG. | 70 DISPLAY ERROR MESSAGE |
| 09 SET IN POST FLAG | 72 CHECK FOR CONFIGURATION ERROR |
| 0A INIT CPU REG | 74 TEST REAL-TIME CLOCK |
| 0B CPU CACHE ON | 76 CHECK FOR KEYBOARD EERROR |
| 0C INIT.CACHE TO POST | 7C SETUP HARDWARE INTERRUPT VECTOR |
| OE INIT. I/O VALUE | 7E TEST COPROCESSER IF PRESENT |
| 0F ENABLE THE L-BUS IDE | 80 DISABLE ON-BOARD I/O PORT |
| 10 INIT. POWER MANAGER | 82 DETECT AND INSTALL EXT.RS232C |
| 11 LOAD ALTERNATE REG. | 84 DETECT AND INSTALL EXT.PARALLEL |
| 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 RE-INIT. ON-BOARD I/O PORT |
| 14 INIT. KEYBOARD CONTROLLER | 88 INIT. BIOS DATA ROM |
| 16 CHECK CHECKSUM | 8A INIT.EXTENDED BIOS DATA AREA |
| 18 8254 TIMER INIT | 8C INIT. FDD CONTROLLER |
| 1A 8237 DMA CONTROLLER INIT. | 9A SHADOW OPTION ROMS |
| 1C RESET INTERRUP CONTROLLER | 9C SETUP POWER MANAGEMENT |
| 20 TEST DRAM REFRESH | 9E ENABLE H/W INTERRUPT |
| 22 TEST 8742 KEYBOARD CONTROLLER | A0 SET TIME OF DAY |
| 24 SET ES SEGMENT REG. TO 4GB | A4 INIT. TYPEMATIC RATE |
| 26 ENABLE A20 | A8 ERASE F2 PROMPT |
| 28 AUTO SIZING DRAM | AA SCAN FOR F2 KEY STROKE |
| 32 COMPUTE THE CPU SPEED | AC ENTER SETUP |
| 34 TESET CMOS RAM | AE CLEAR IN POST FLAG |
| 38 SHADOW SYSTEM BIOS ROM | B0 CHECK FOR ERRORS |
| 3A AUTO SIZING CACHE | B2 POST DONE-PREPARE TO BOOT O/S |
| 3C CONFIGURE ADVANCED CHIPSET REG. | B4 ONE BEEP |
| 3D LOAD ALTER REG. WITH CMOS VALUE | B6 CHECK PASSWORD (OPTION) |
| 42 INIT. INTERRUPT VECTOR | B7 ACPI INIT |
| 44 INIT. BIOS INTERRUPT | BA DMI INIT |
| 46 CHECK ROM COPYRIGHT NOTICE | BE CLEAR SCREEN |
| 47 INIT. I20 SUPPORT IF INSTALLED | C0 TRY BOOT WITH INT19 |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS | D0 INTERRUPT HANDLER ERROR |
| 49 INIT. PCI BUS AND DEVICE | D2 UNKNOWN INTERRUPT ERROR |
| 4A INIT. ALL VIDEO BIOS ROM | D4 PENDING INTERRUPT ERROR |
| 4C SHADOW VIDEO BIOS ROM | D6 SHUTDOWN 5 |
| 50 DISPLAY CPU TYPE AND SPEED | D8 SHUTDOWN ERROR |
| 52 TEST KEYBOARD | DA EXTENDED BLOCK MOVE |
| 54 SET KEYCLICK IF ENABLED | DC SHUTDOWN 10 |
| 56 ENABLE KEYBOARD | 89 ENABLE NMI |
| 58 TEST FOR UNEXPECTED INTERRUPTS | 90 INIT. HDD CONTROLLER |
| 5A DISPLAY " PRESS ..... SETUP" | 91 INIT. LOCAL BUS HDD CONTROLLER |
| 5C TEST RAM GETWEEN 512K AND 640K | 92 JUMP TO USER PATCH 2 |
| 60 TEST EXTENDED MEMORY | 94 DISABLE A20 ADDRESS LINE |
| 62 TEST EXTENDED MEMORY ADDRESS LINE | 96 CLEAR HUGE ES SEGMENT REG. |
| 64 JUMP TO USER PATCH 1 | 98 SEARCH FOR OPTION ROMS |

Pins for ICT FREE should be rearranged.

ICT FREE



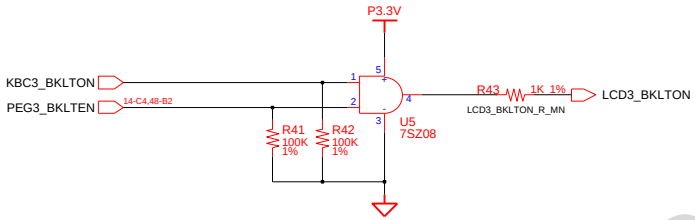

## 80H DECODER CONNECTOR



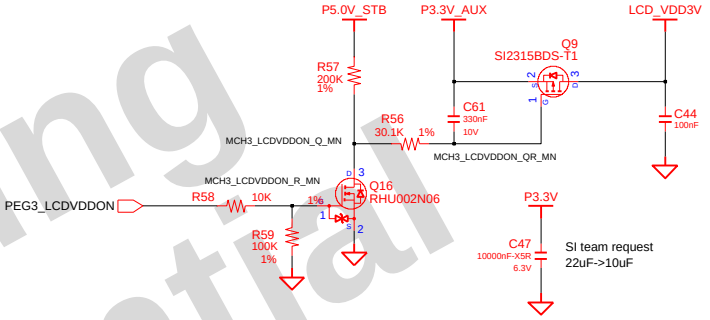

| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D SPI_BIOS_ROM SPI_BIOS_ROM | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 33 OF 61 | |

# LVDS

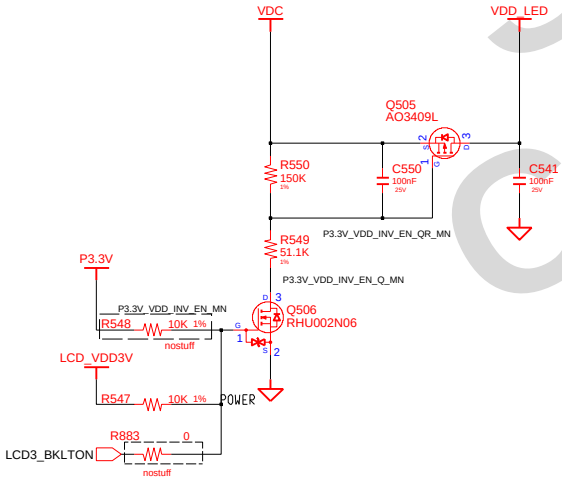
## Backlight On



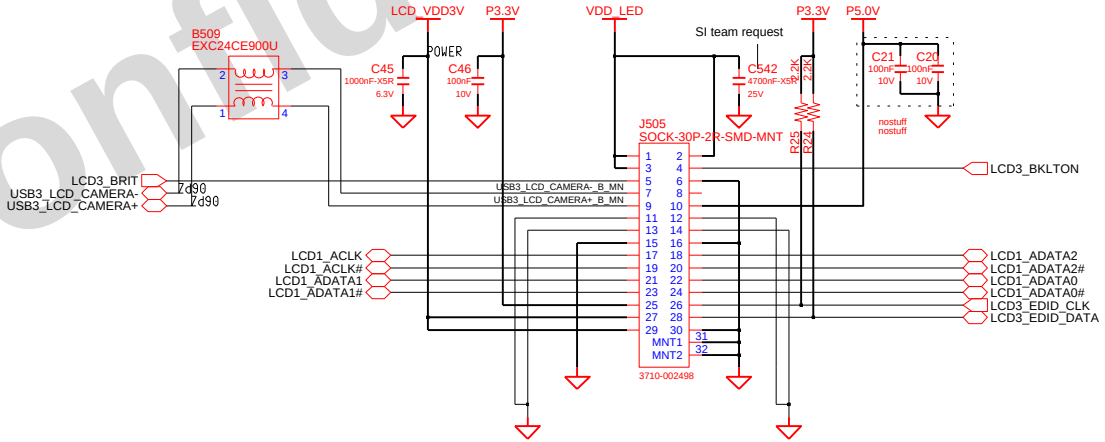

## LCD Power EBL Purpose




## LED Power



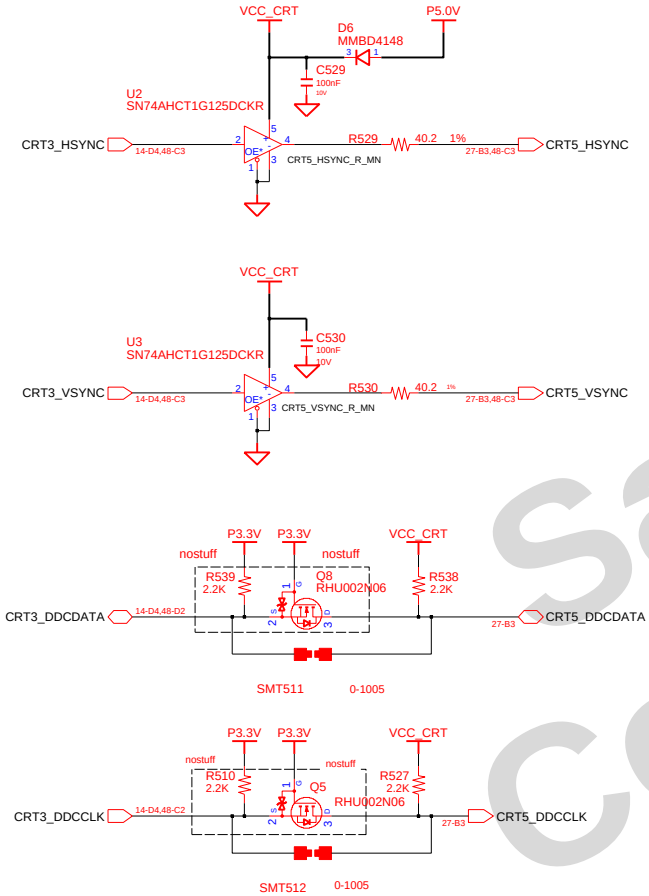

## Camera + LCD Connector



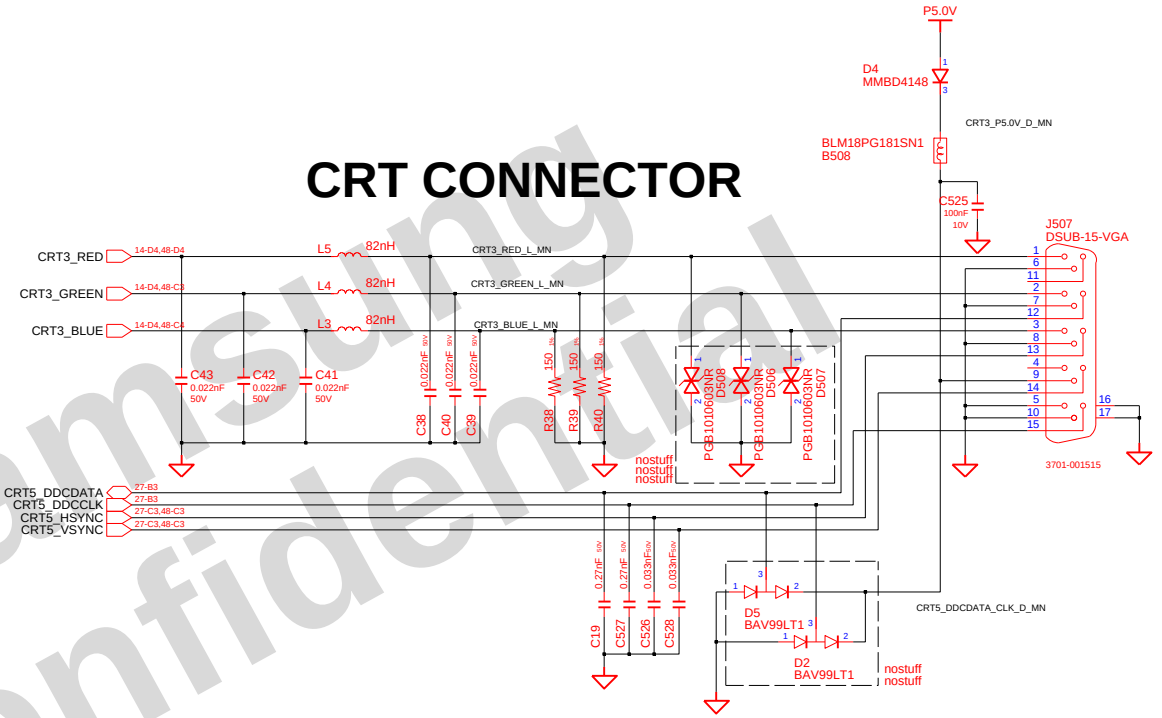



| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / GRAPHICS_IF / LVDS | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 34 OF 61 | |

# CRT




## CRT CONNECTOR



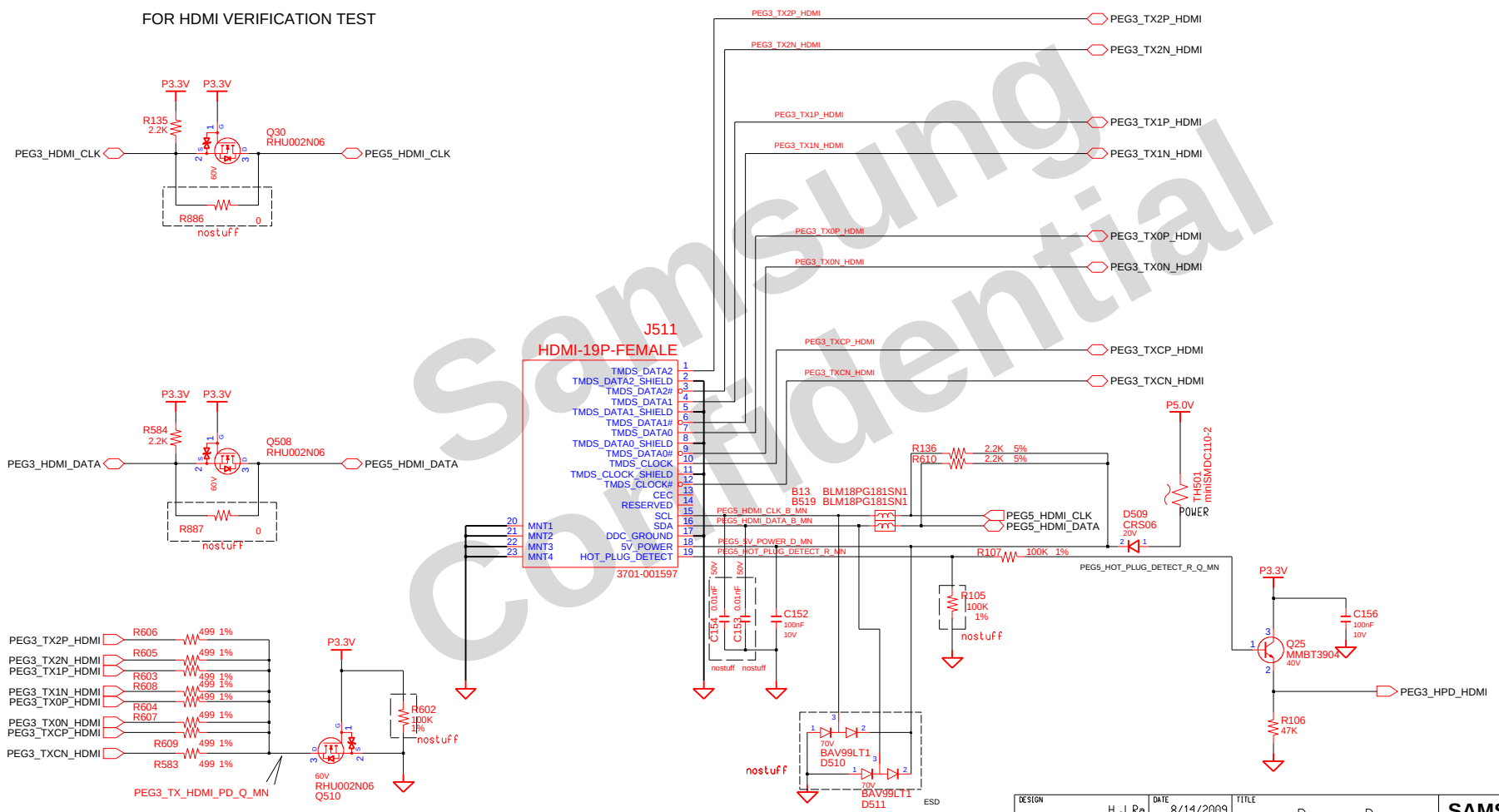

Check "CRT3_DDCCLK/DATA" Voltage Level

2N06 Can be replaced with SM6K2



| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / GRAPHICS_IF / CRT | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 35 OF 61 | |

# HDMI

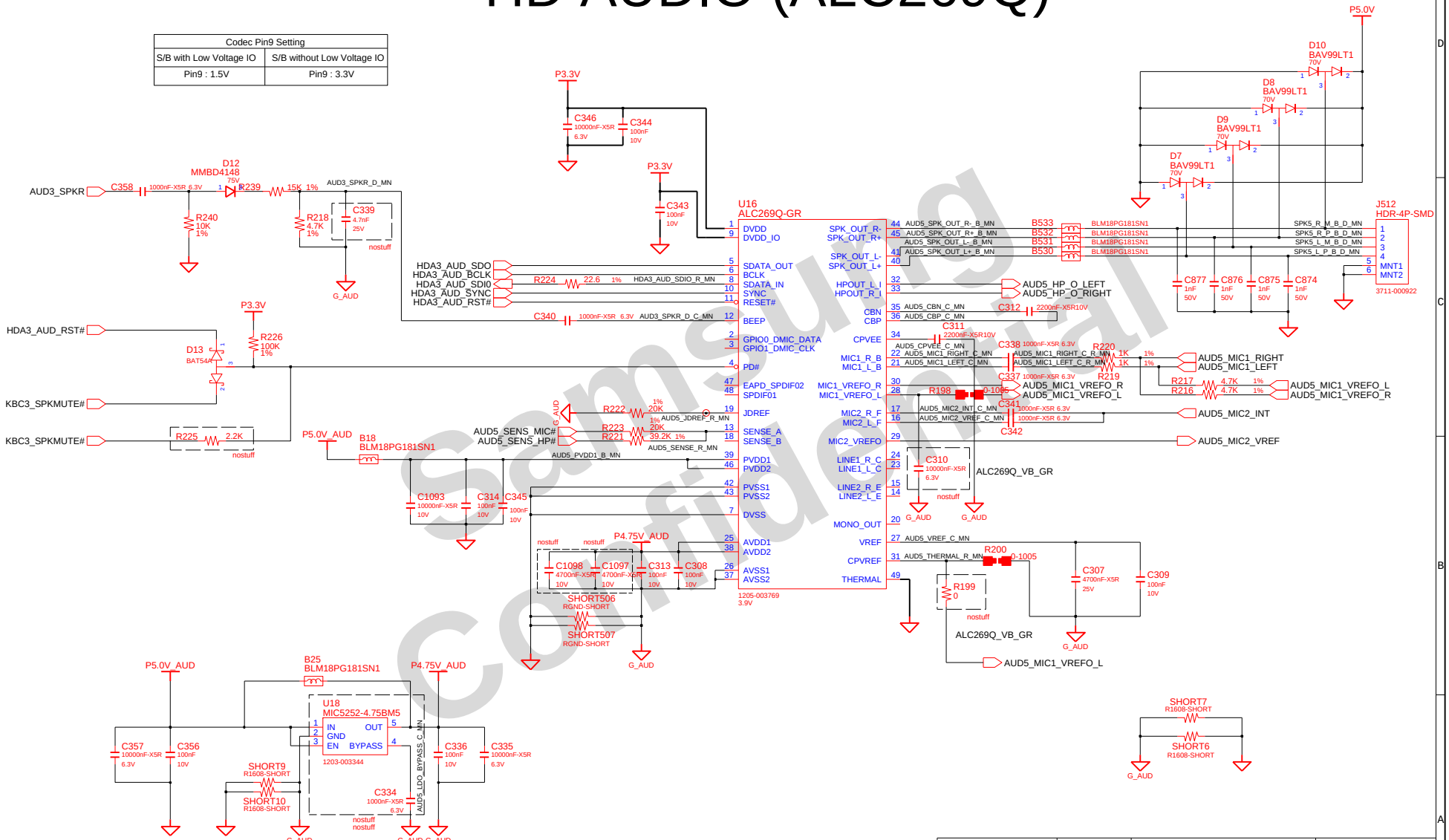





| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 8/14/2009 | TITLE: Bremen-D HDMI HDMI | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 36 OF 61 | |

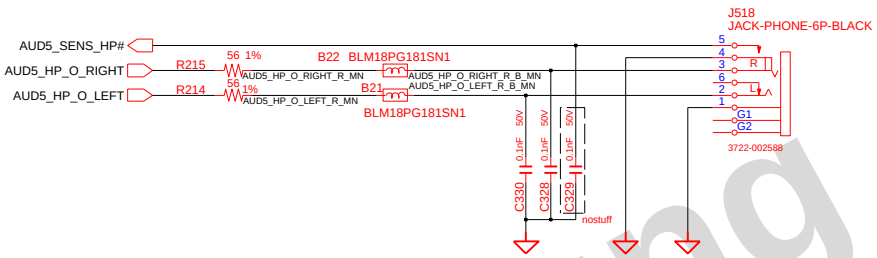
# HD AUDIO (ALC269Q)

| Codec Pin9 Setting | |
|---|---|
| S/B with Low Voltage IO | S/B without Low Voltage IO |
| Pin9 : 1.5V | Pin9 : 3.3V |

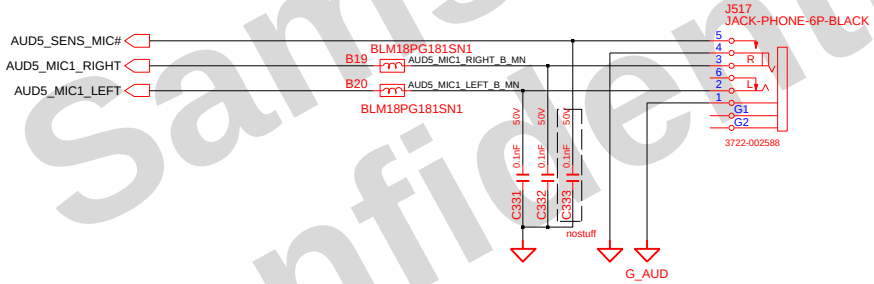


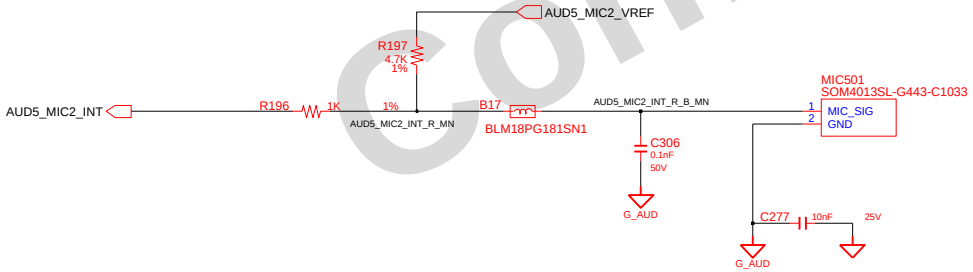

| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D<br>HDA_CODEC<br>AUDIO CODEC ALC269Q_GR | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 37 OF 61 | |

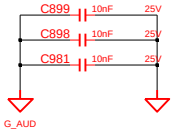
## HEADPHONE(BLACK)




## MIC JACK(BLACK)



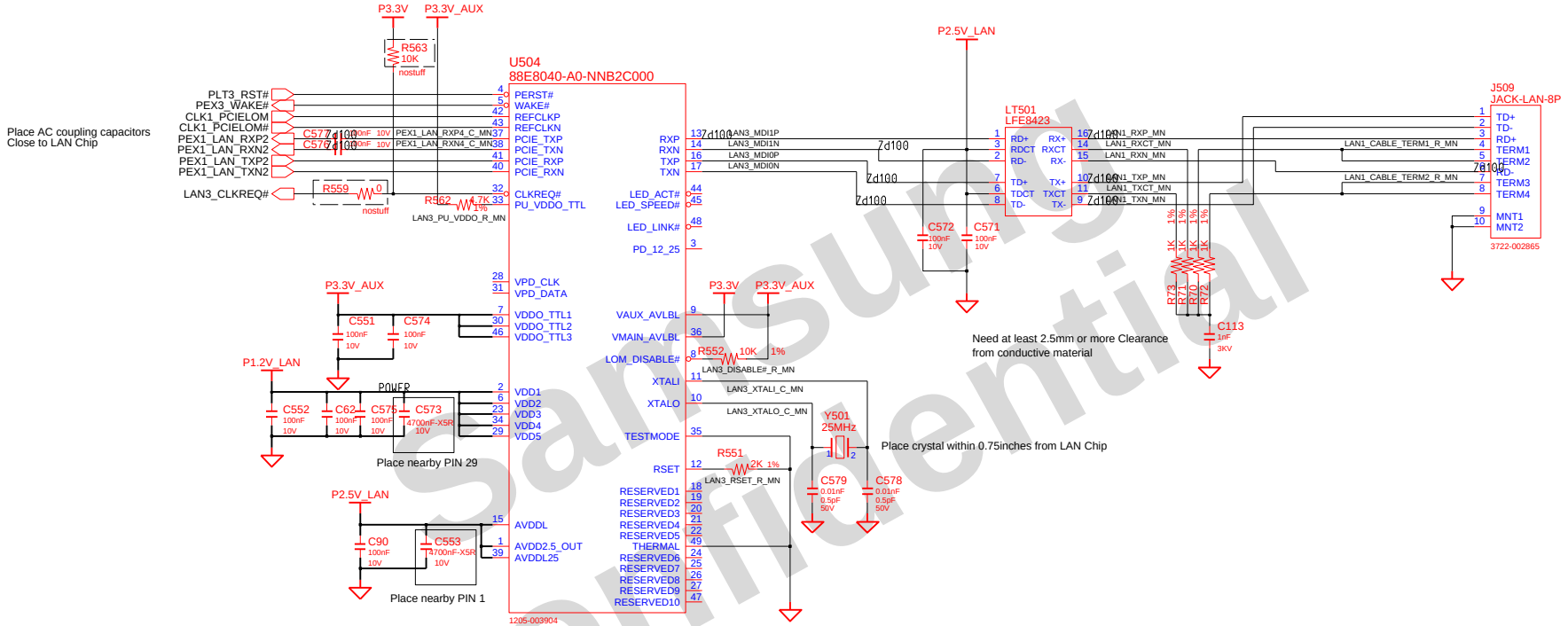






| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / HDA_CODEC / AUDIO INPUT/OUTPUT | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 38 OF 61 | |

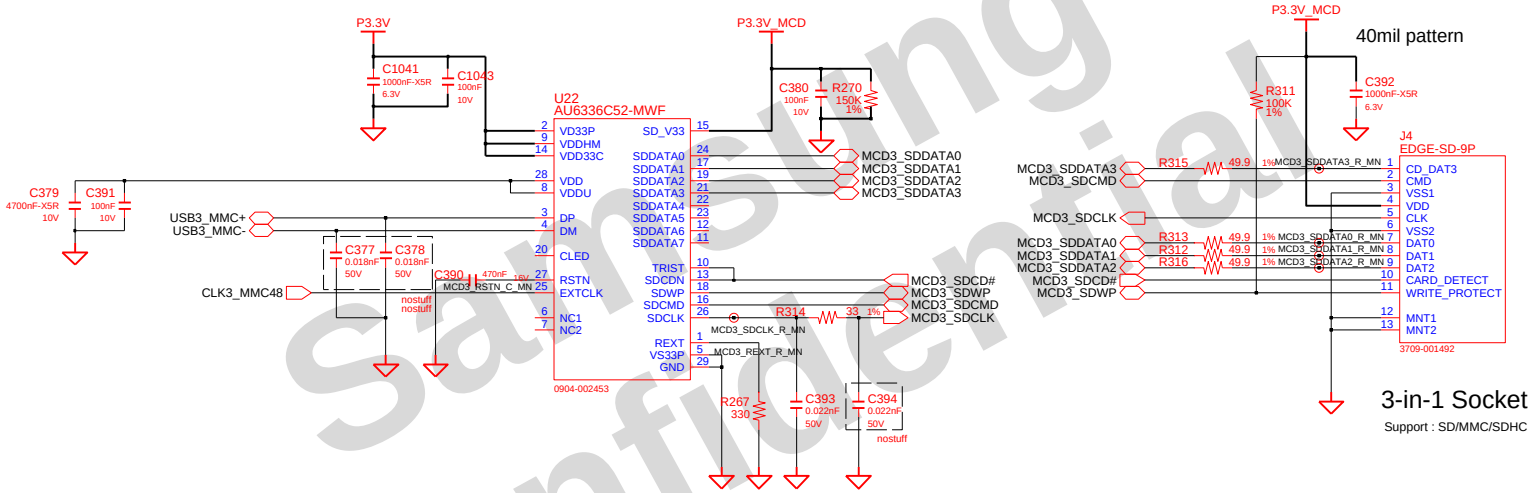
# LAN Controller (88E8040)






| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / LAN / LAN_MARVELL_8040 | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 39 OF 61 | |

# 3 IN 1 CARD (AU6336)

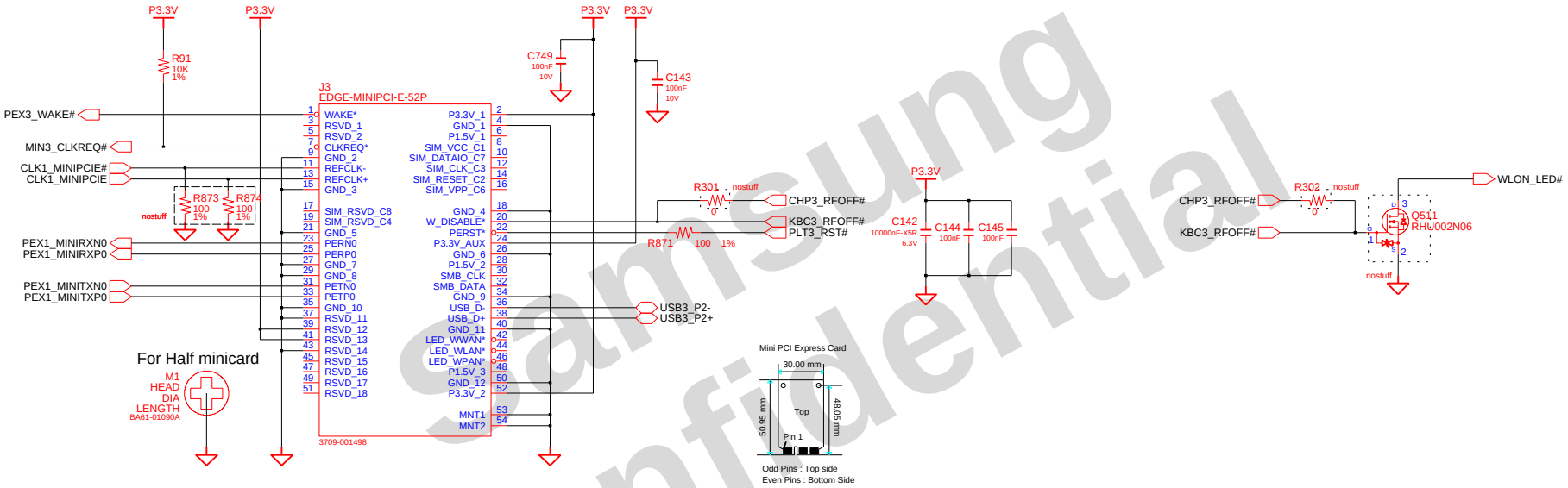





| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D MULTICARD 3 IN 1 CARD | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 40 OF 61 | |

# Wireless LAN

## WLAN, 4mm

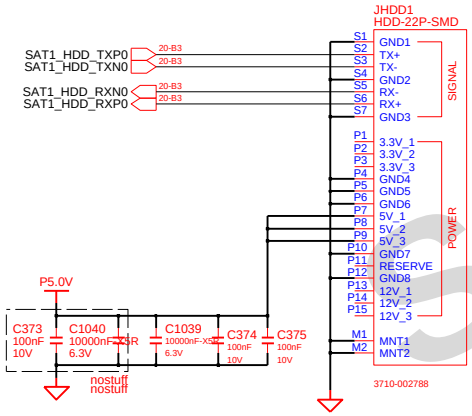




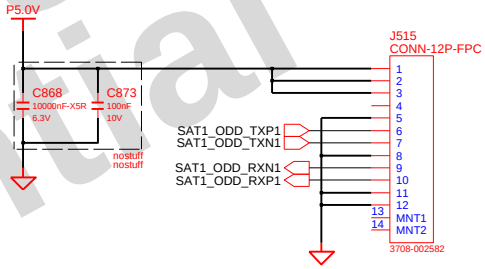

| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / MINI_PCIE_CONN / WLAN | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 41 OF 61 | |

# SATA I/F CONN

## SATA HDD CONN



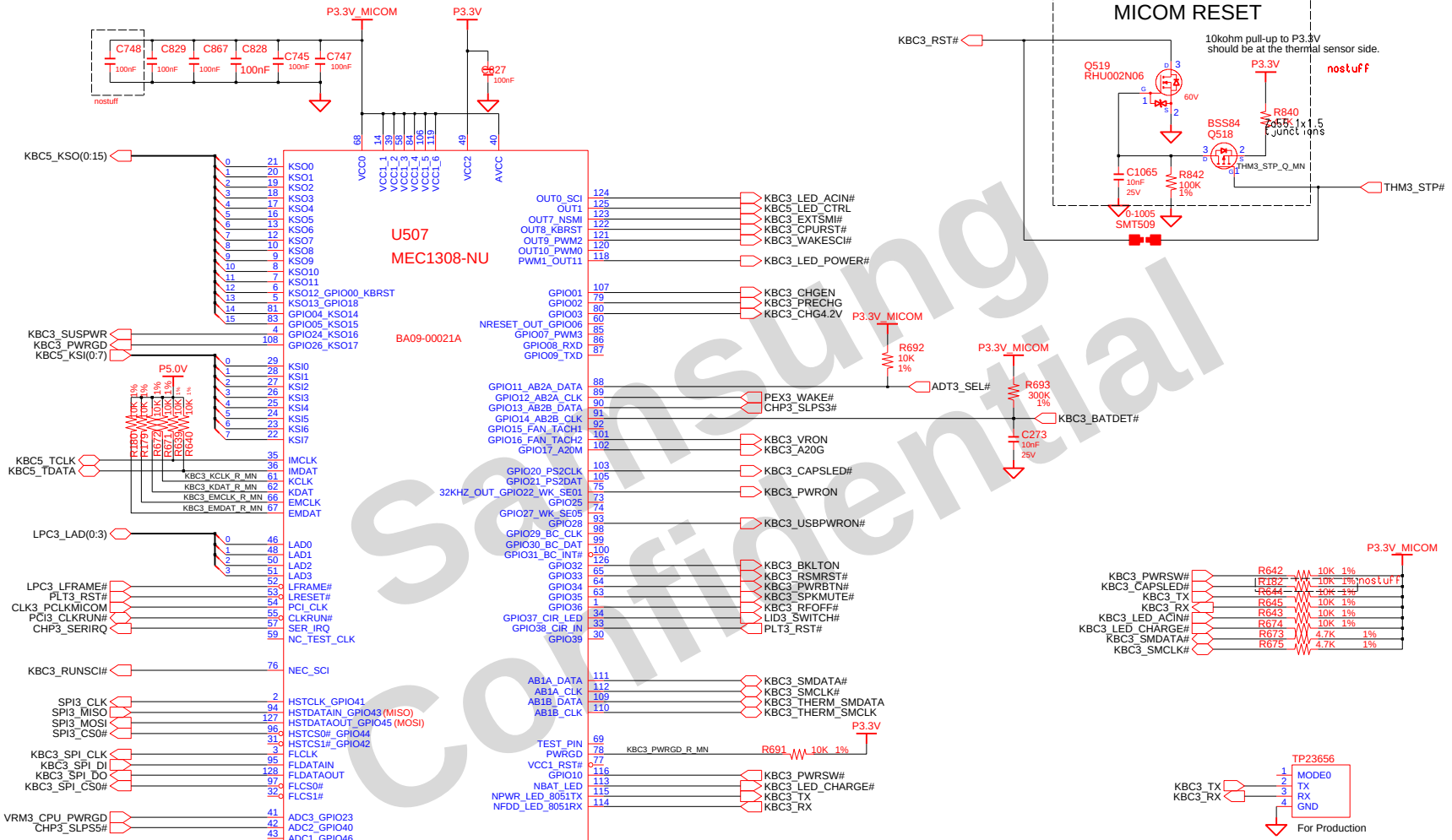

## MAIN TO SUB SATA ODD CONN






| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D<br>SATA_DEVICES<br>HDD & ODD SUB CONNECTOR | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 42 OF 61 | |

# MICOM_MEC1308





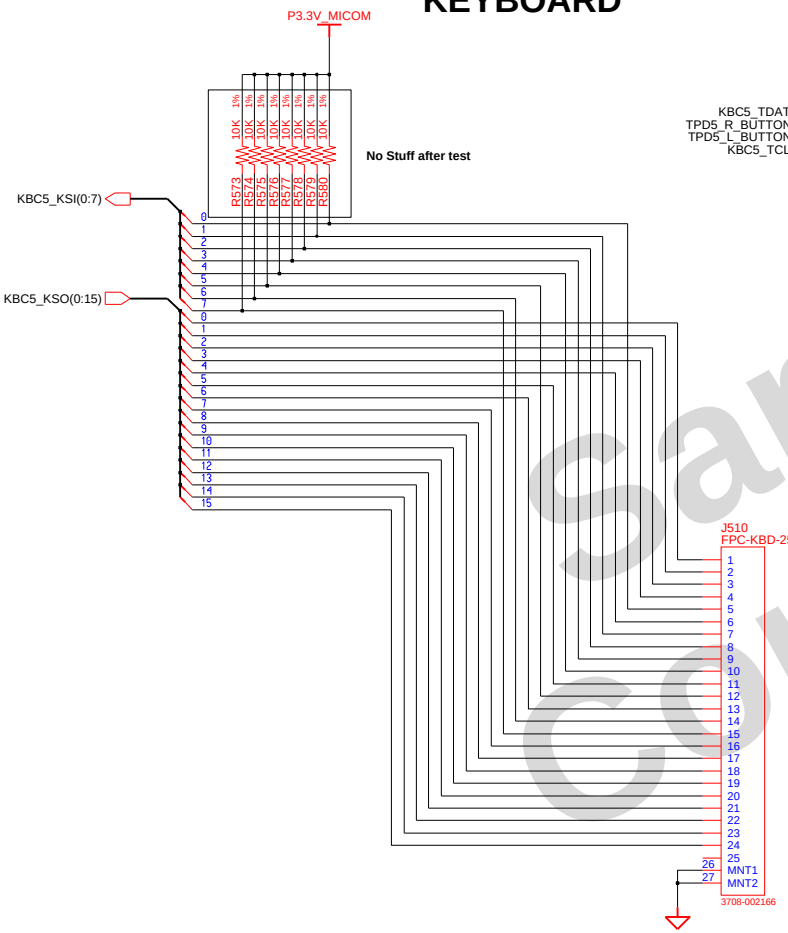

## MICOM Crisis Update

Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

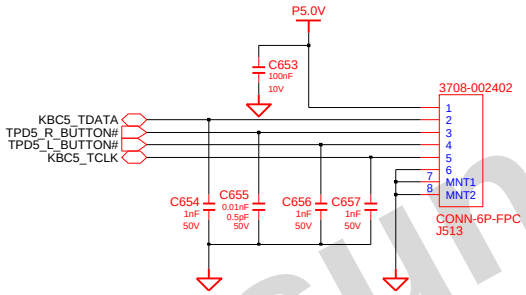
| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D MICOM MICOM_SMSC MEC1308 | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | PART NO. BA41-xxxxxA |
| APPROVAL H.K.Park | REV 1.1 | | |
| MODULE CODE | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 43 OF 61 | |

# Micom Glue Logic

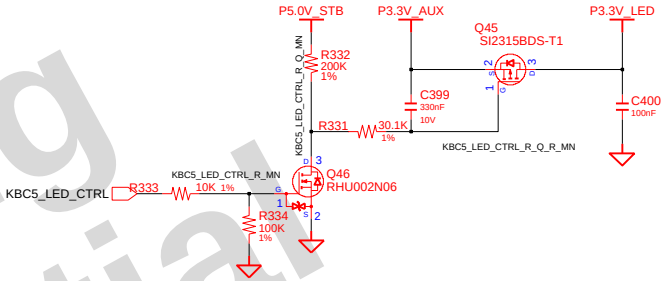
## KEYBOARD



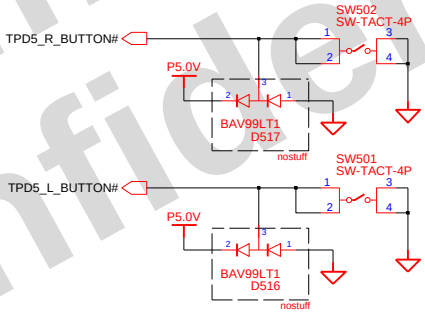

## TOUCHPAD



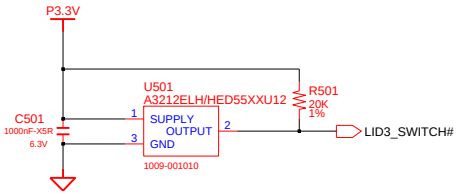

## TOUCHPAD LED

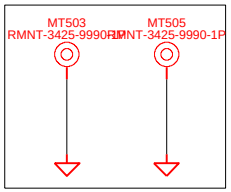



## TOUCHPAD BUTTON




## LID SWITCH



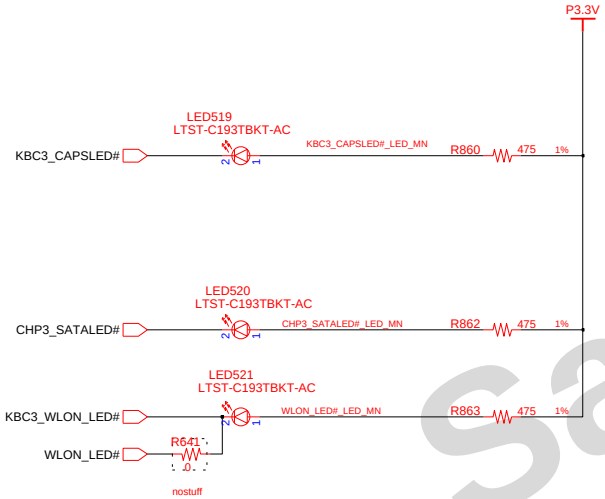

Keyboard Mount(for 15")



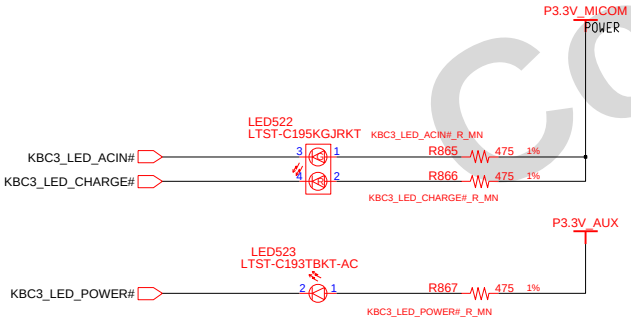
| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D<br>MICOM GLUE LOGIC<br>KETBOARD & TOUCHPAD | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 44 OF 61 | |

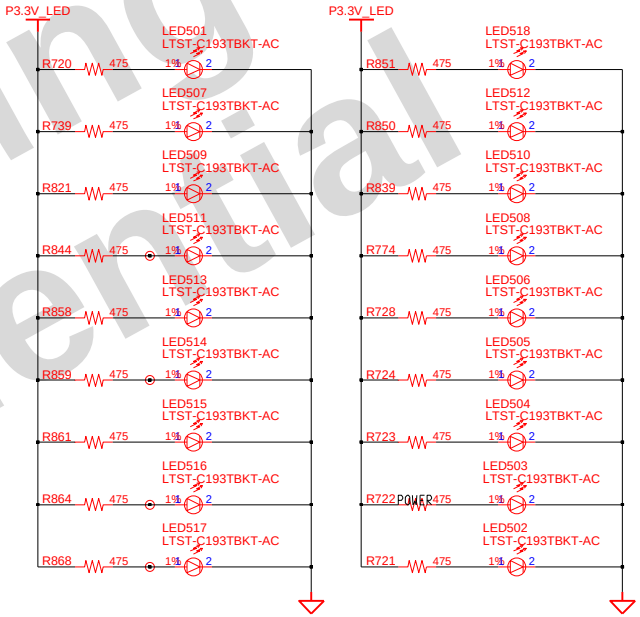
# LEDs

## FUNCTION KEY LED




## ADAPTERIN/CHARGING LED

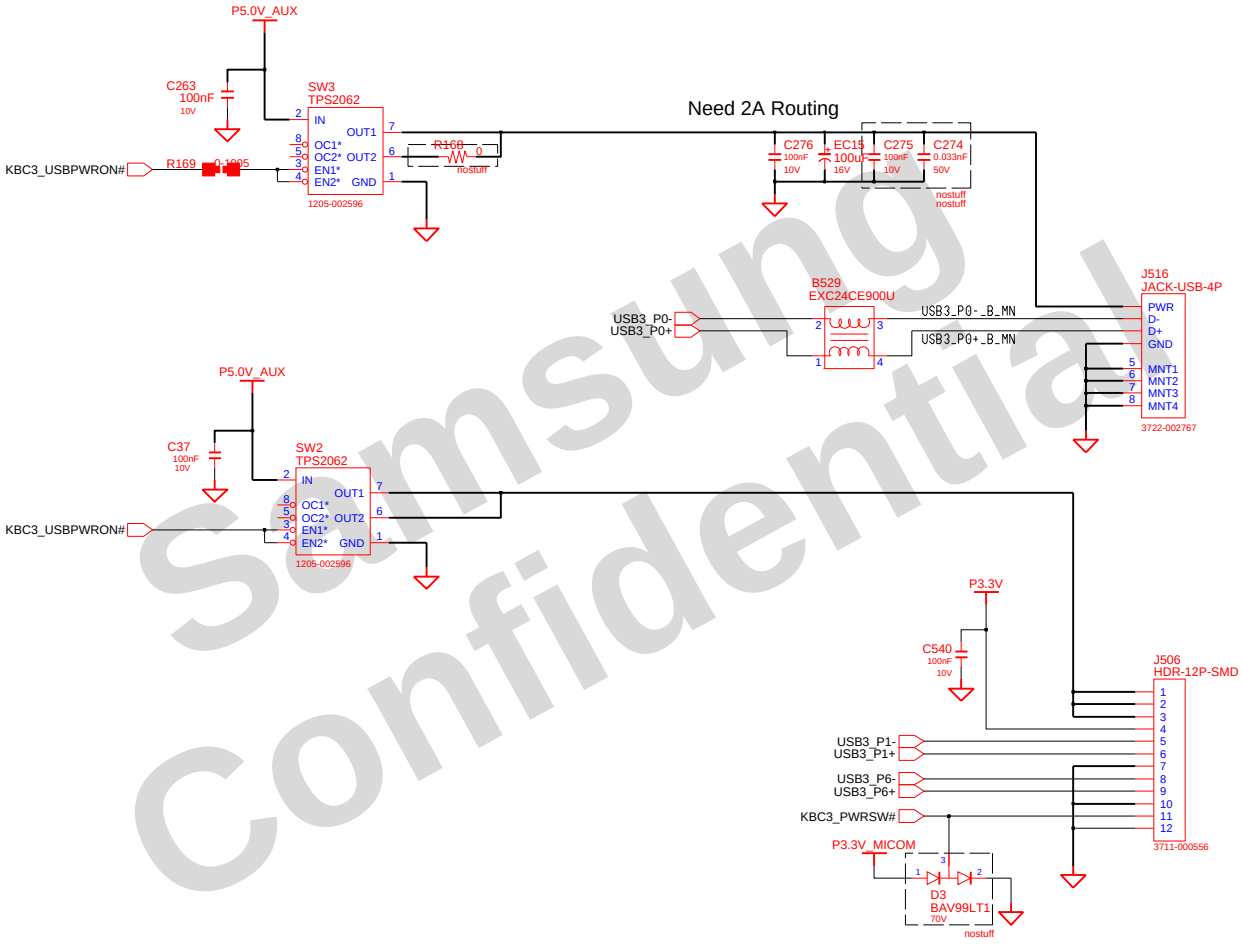





| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D LED_SWITCH LED_SWITCH | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 45 OF 61 | |

# USB Single connector

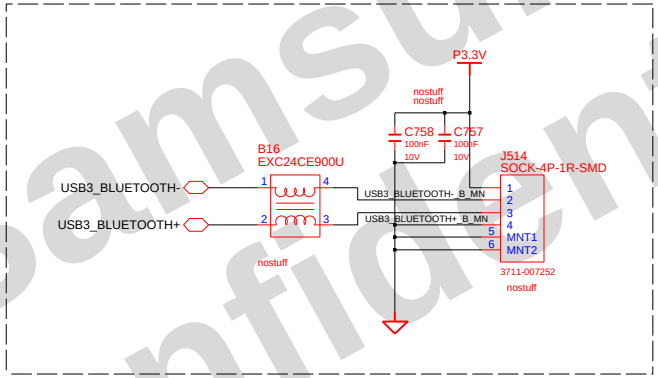





| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / USB_CONN / USB | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 46 OF 61 | |

# USB I/F Devices

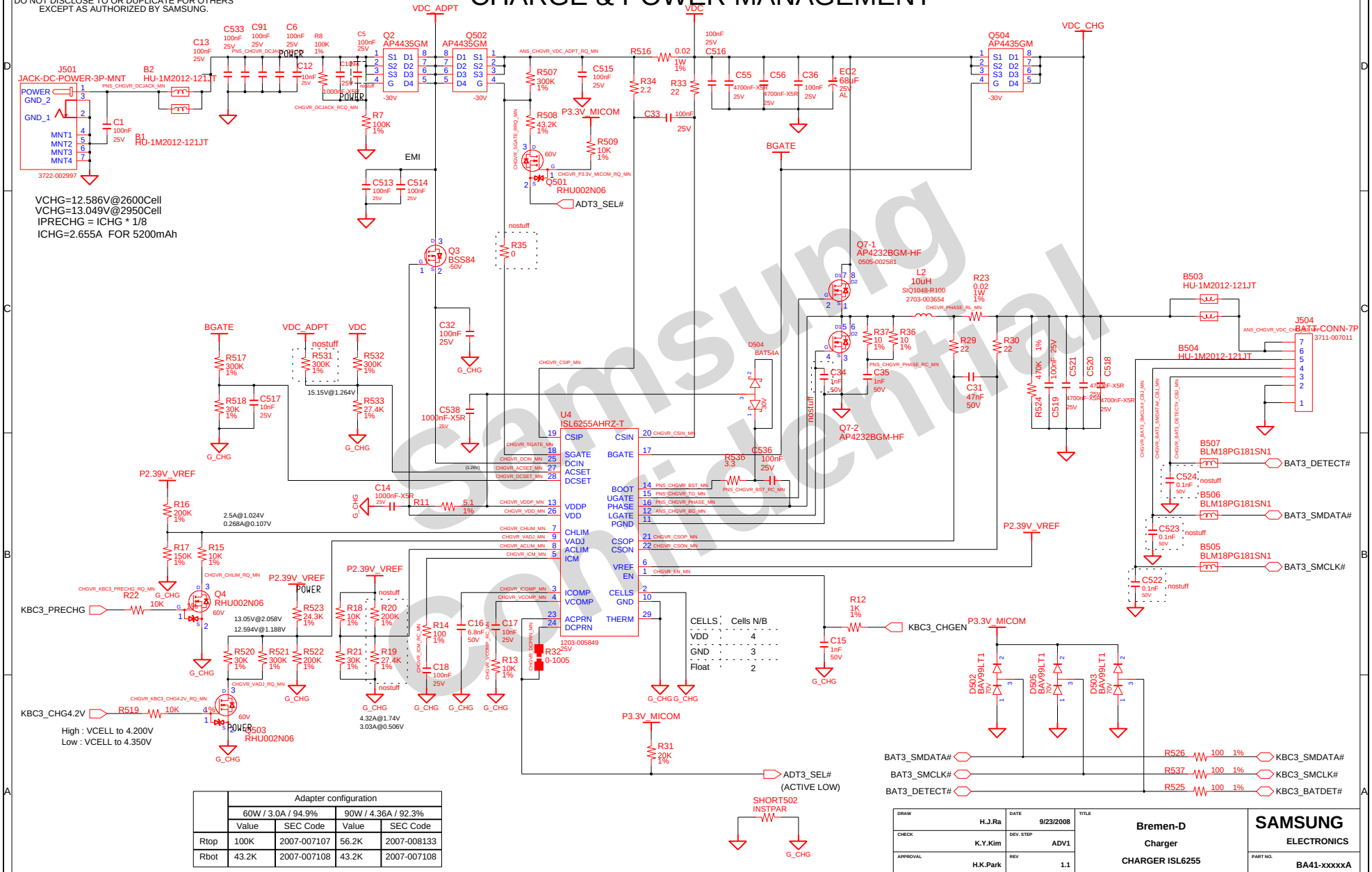
## Bluetooth Interface






| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D<br>USB_DEVICES<br>BLUETOOTH | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 47 OF 61 | |

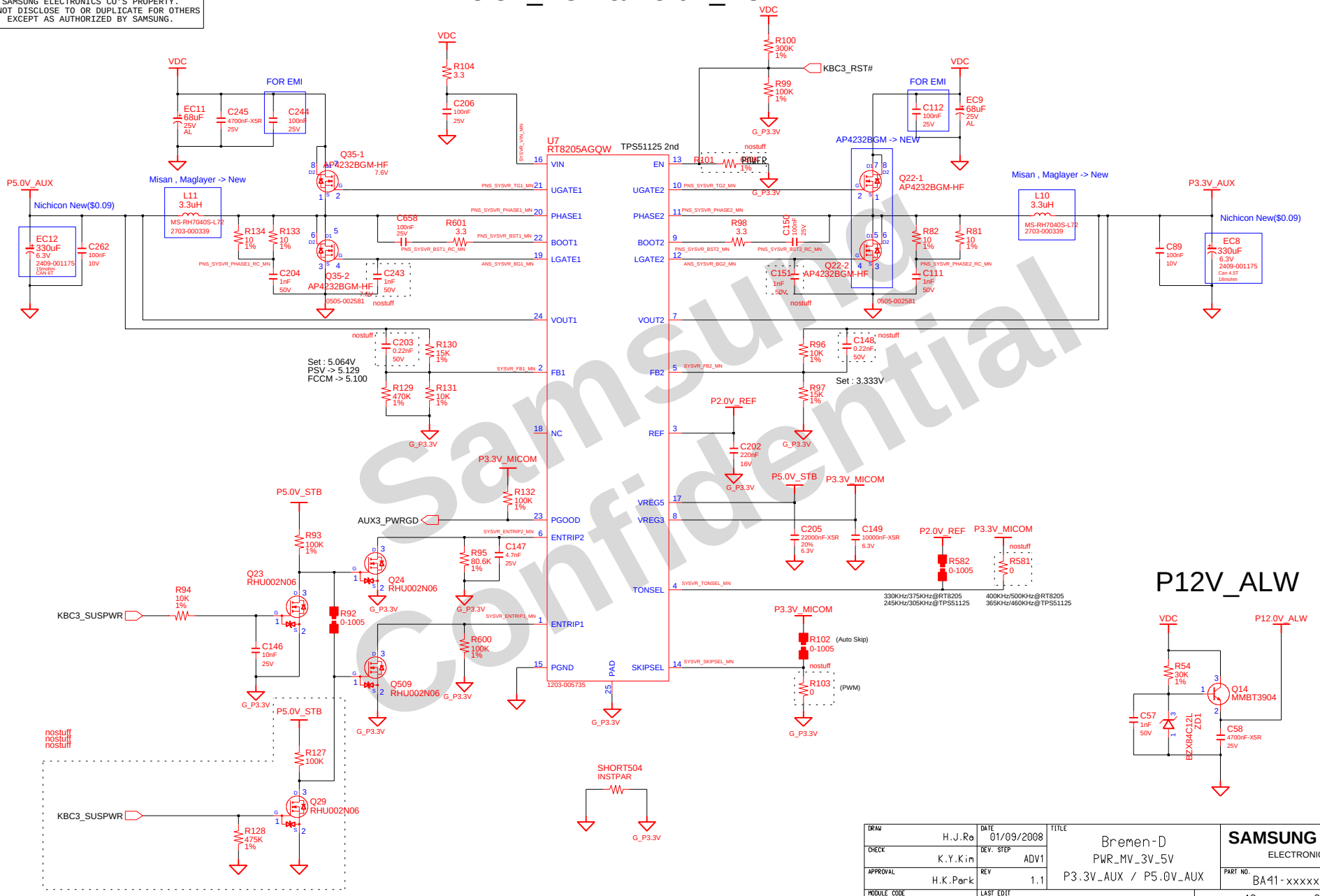
# CHARGE & POWER MANAGEMENT




| | Adapter configuration | | | |
|---|---|---|---|---|
| | 60W / 3.0A / 94.9% | | 90W / 4.36A / 92.3% | |
| | Value | SEC Code | Value | SEC Code |
| Rtop | 100K | 2007-007107 | 56.2K | 2007-008133 |
| Rbot | 43.2K | 2007-007108 | 43.2K | 2007-007108 |

| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D Charger CHARGER ISL6255 | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE undefined | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 48 OF 61 | |

# P3.3V_AUX & P5.0V_AUX



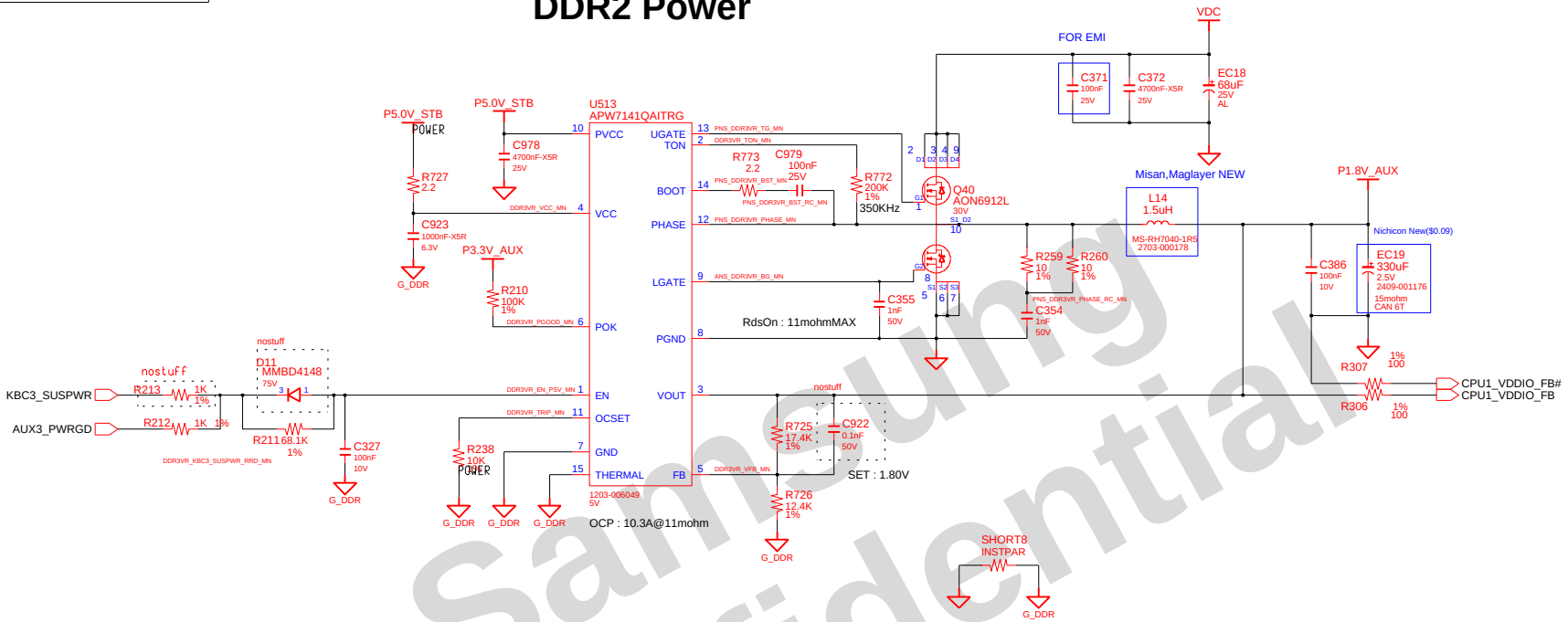



## P12V_ALW

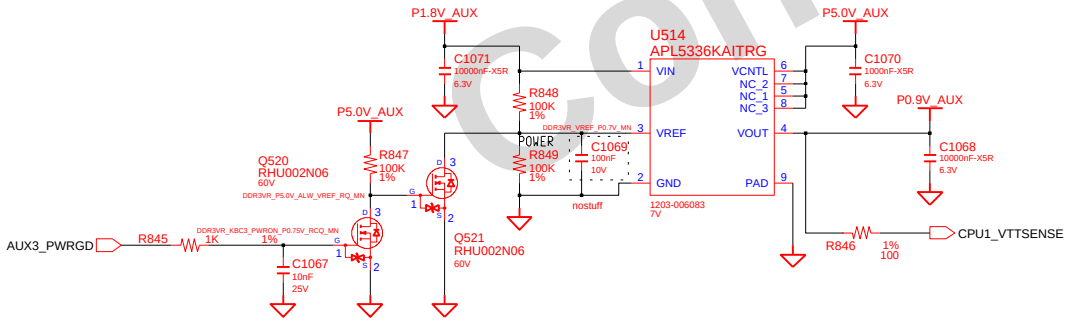


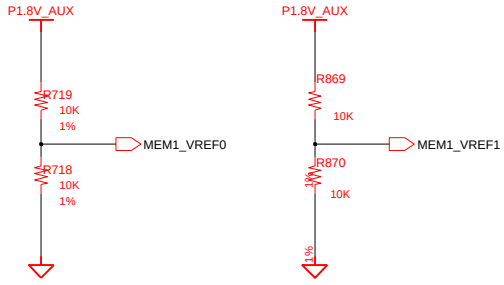

| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 01/09/2008 | TITLE: Bremen-D PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 49 OF 61 | |

# DDR2 Power



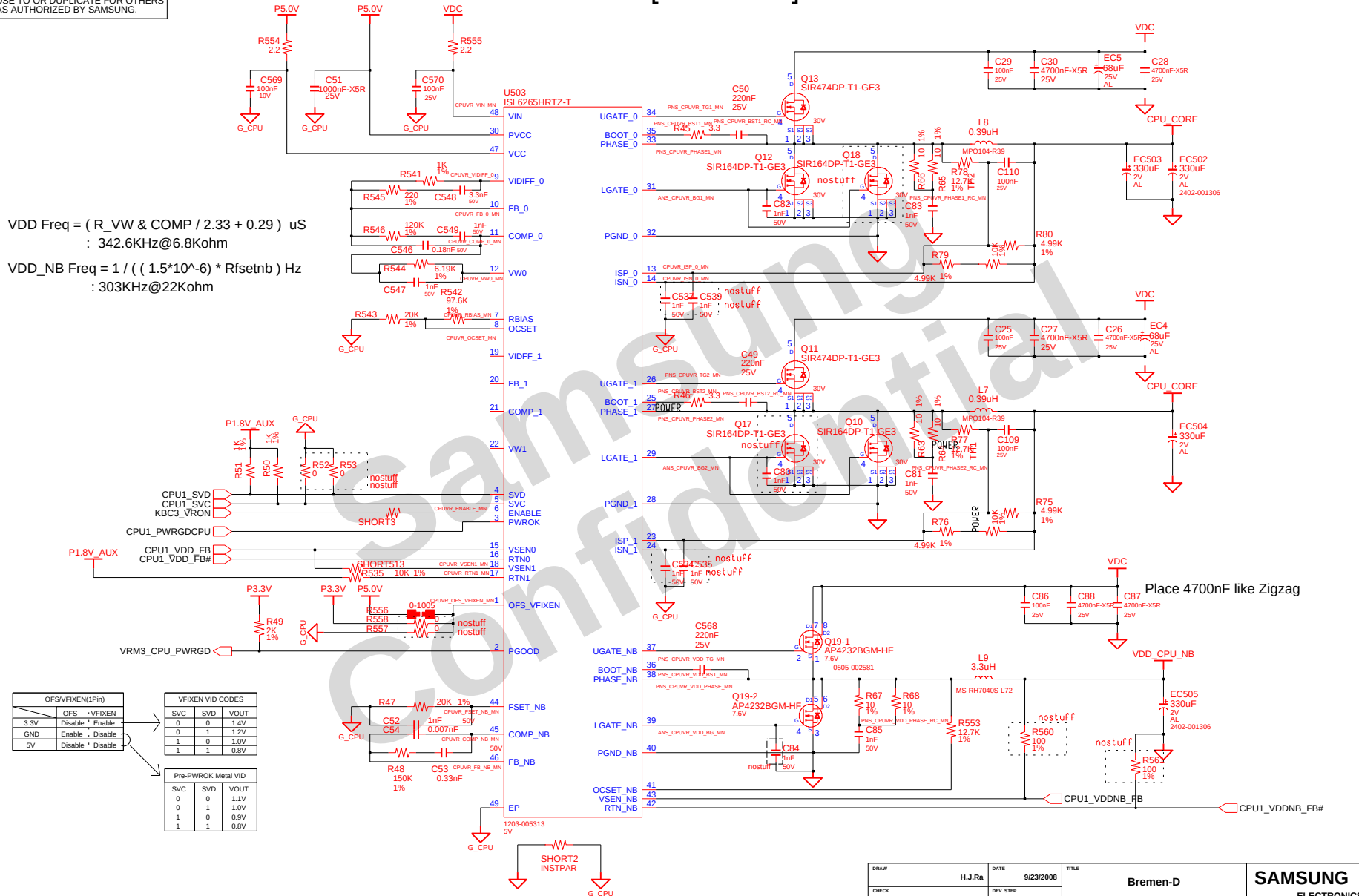

# DDR2 VTT(0.9V_AUX)




| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D PWR_MEMORY DDR2 POWER | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | | |
| APPROVAL H.K.Park | REV 1.1 | | PART NO. BA41-xxxxxA |
| MODULE CODE undefined | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 50 OF 61 | |

# CPU VRM [INTERSIL]






| | | | |
|---|---|---|---|
| DRAW | H.J.Ra | DATE | 9/23/2008 |
| CHECK | K.Y.Kim | DEV. STEP | ADV1 |
| APPROVAL | H.K.Park | REV | 1.1 |
| MODULE CODE | undefined | LAST EDIT | October 10, 2009 16:50:44 PM |

TITLE: Bremen-D
PWR CPU MV ISL6265HRT
CPU VRM

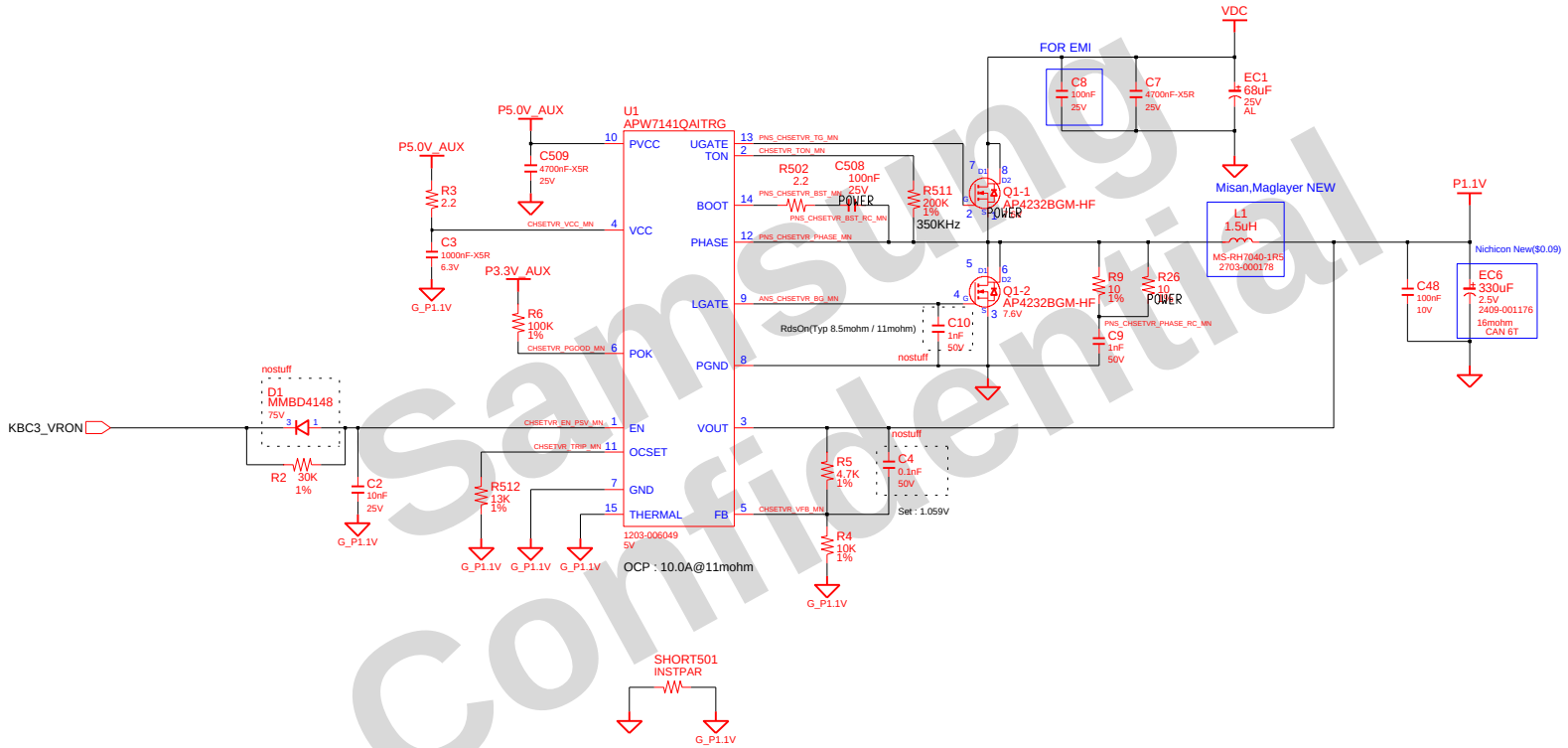
SAMSUNG ELECTRONICS
PART NO. BA41-xxxxxA





D:/users/mobile58/mentor/Bremen-D/Bremen-D_Sub

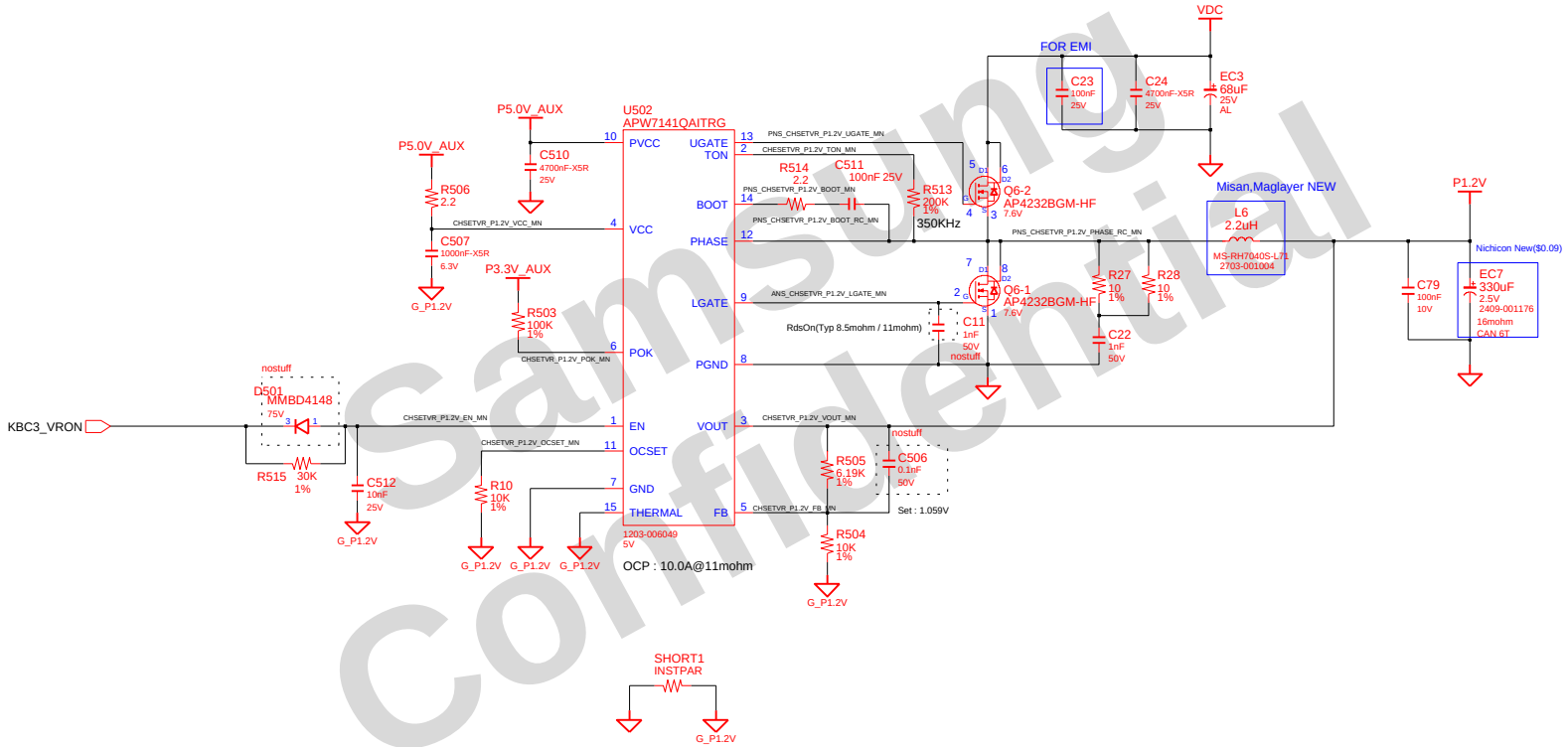
# CHIPSET POWER(P1.1V)






| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 9/3/2009 | TITLE: Bremen-D PWR MV RX881 P1.1V | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 52 OF 61 | |

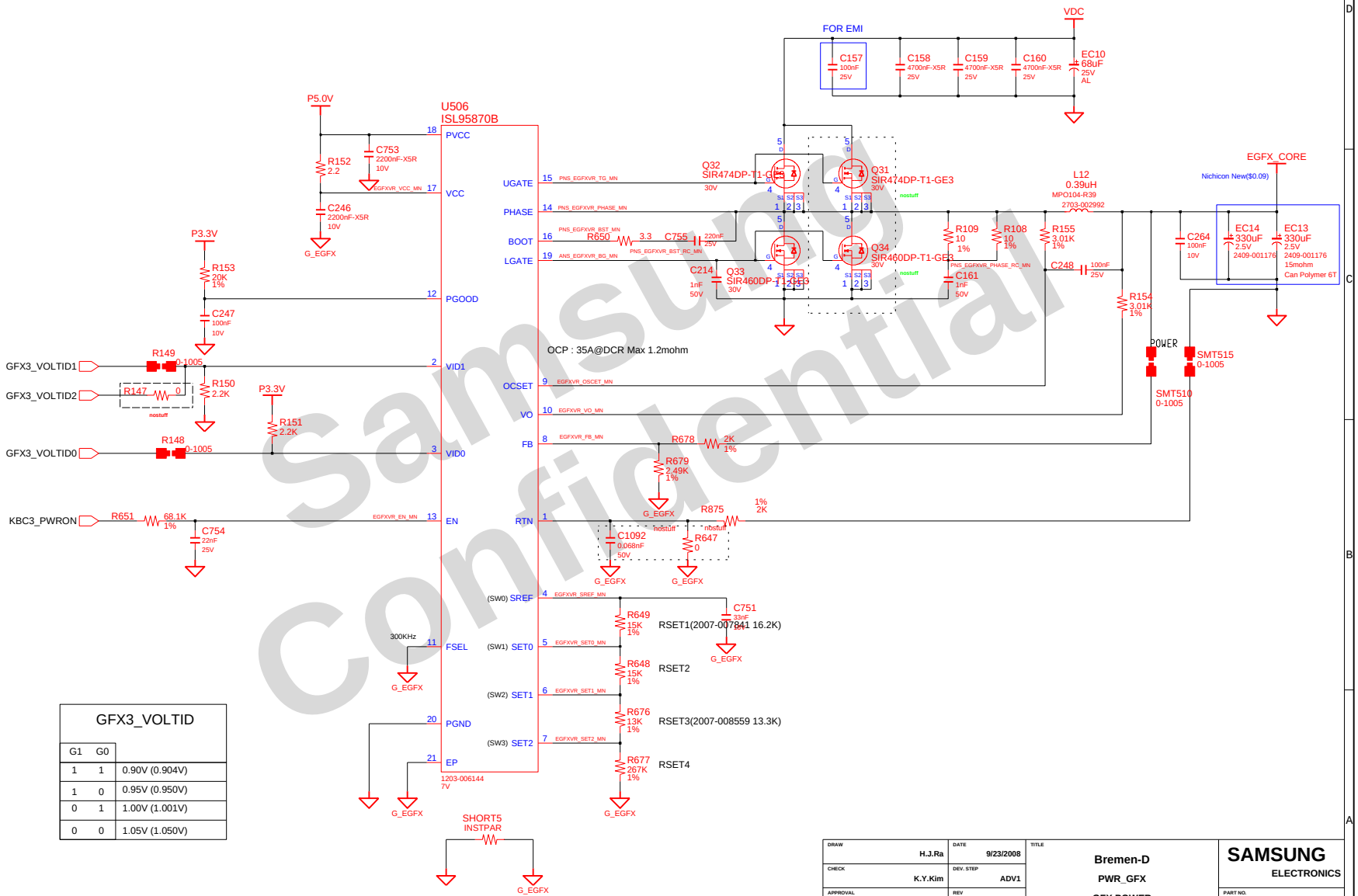
# CHIPSET POWER(P1.2V)






| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D<br>PWR MV RX881<br>P1.2V | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 53 OF 61 | |

# Graphic Core Power




## GFX3_VOLTID

| G1 | G0 | |
|---|---|---|
| 1 | 1 | 0.90V (0.904V) |
| 1 | 0 | 0.95V (0.950V) |
| 0 | 1 | 1.00V (1.001V) |
| 0 | 0 | 1.05V (1.050V) |

| | | | |
|---|---|---|---|
| DRAW | H.J.Ra | DATE | 9/23/2008 |
| CHECK | K.Y.Kim | DEV. STEP | ADV1 |
| APPROVAL | H.K.Park | REV | 1.1 |
| MODULE CODE | | LAST EDIT | October 10, 2009 16:50:44 PM |

TITLE: Bremen-D / PWR_GFX / GFX POWER

SAMSUNG ELECTRONICS

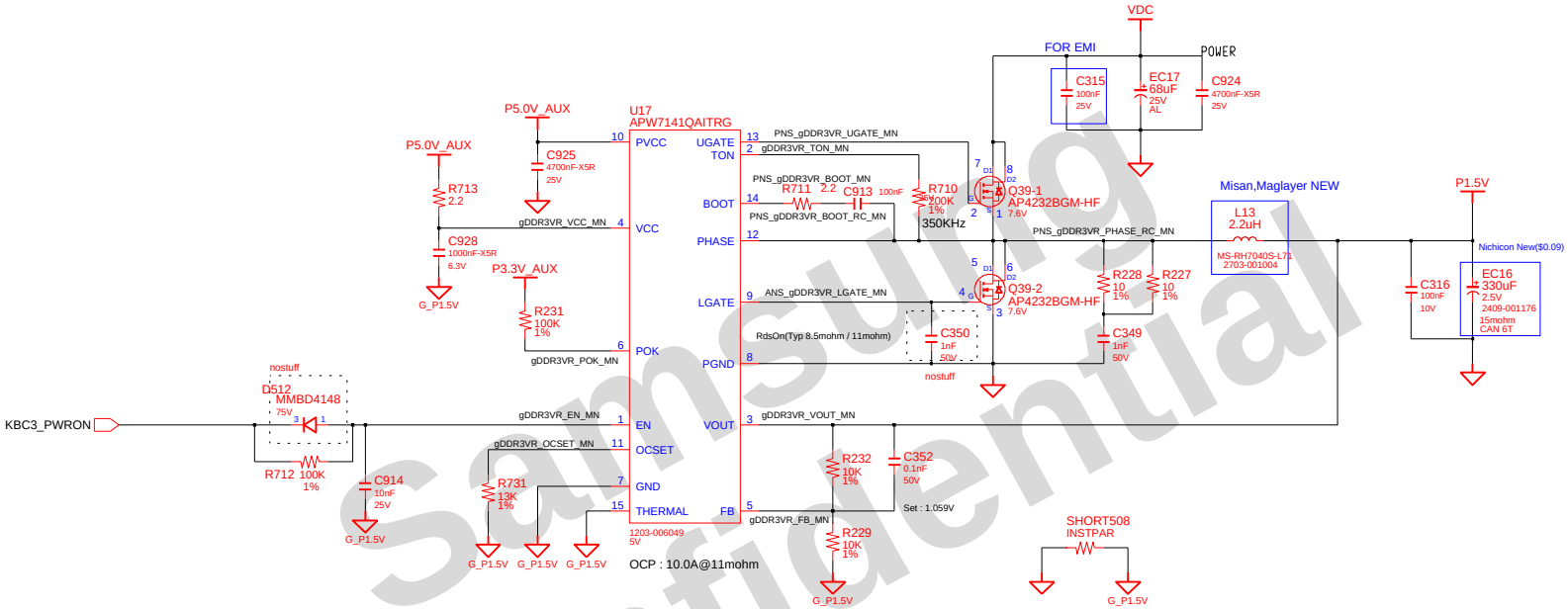
PART NO. BA41-xxxxxA



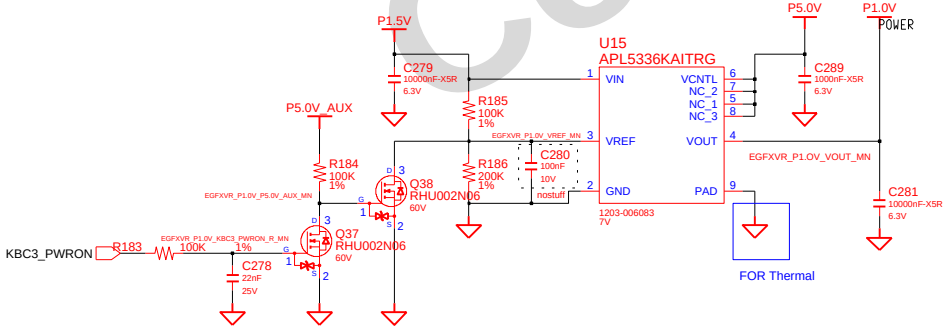


D:/users/mobile58/mentor/Bremen-D/Bremen-D_Sub

# gDDR3 POWER(P1.5V)



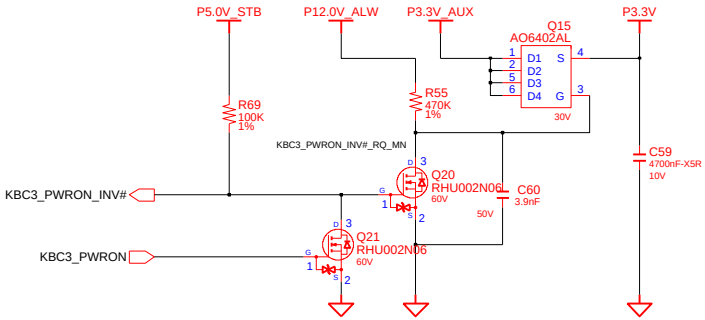

# P1.0V



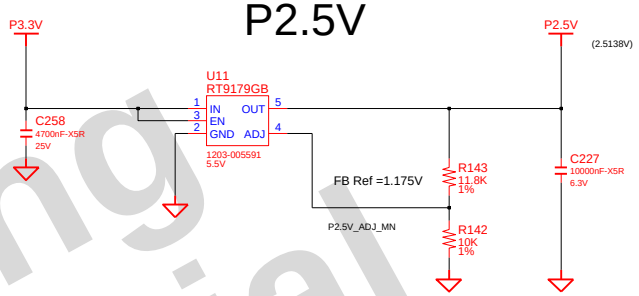

| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D<br>PWR_GFX MEMORY<br>gDDR3 POWER | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 55 OF 61 | |

# Switched Power

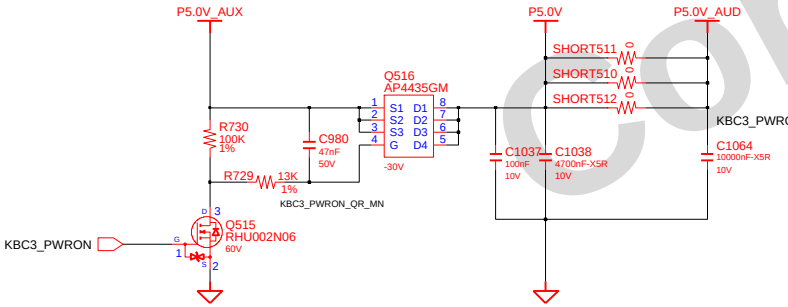
## Switched Power On (P3.3V)



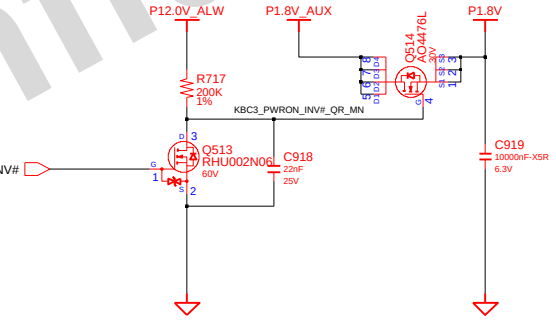

## P2.5V



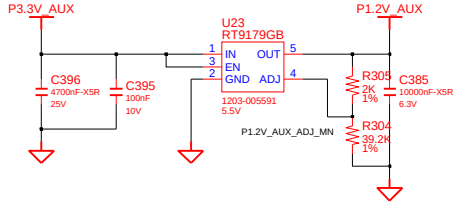

## Switched Power On (P5.0V)




## Switched Power On (P1.8V)



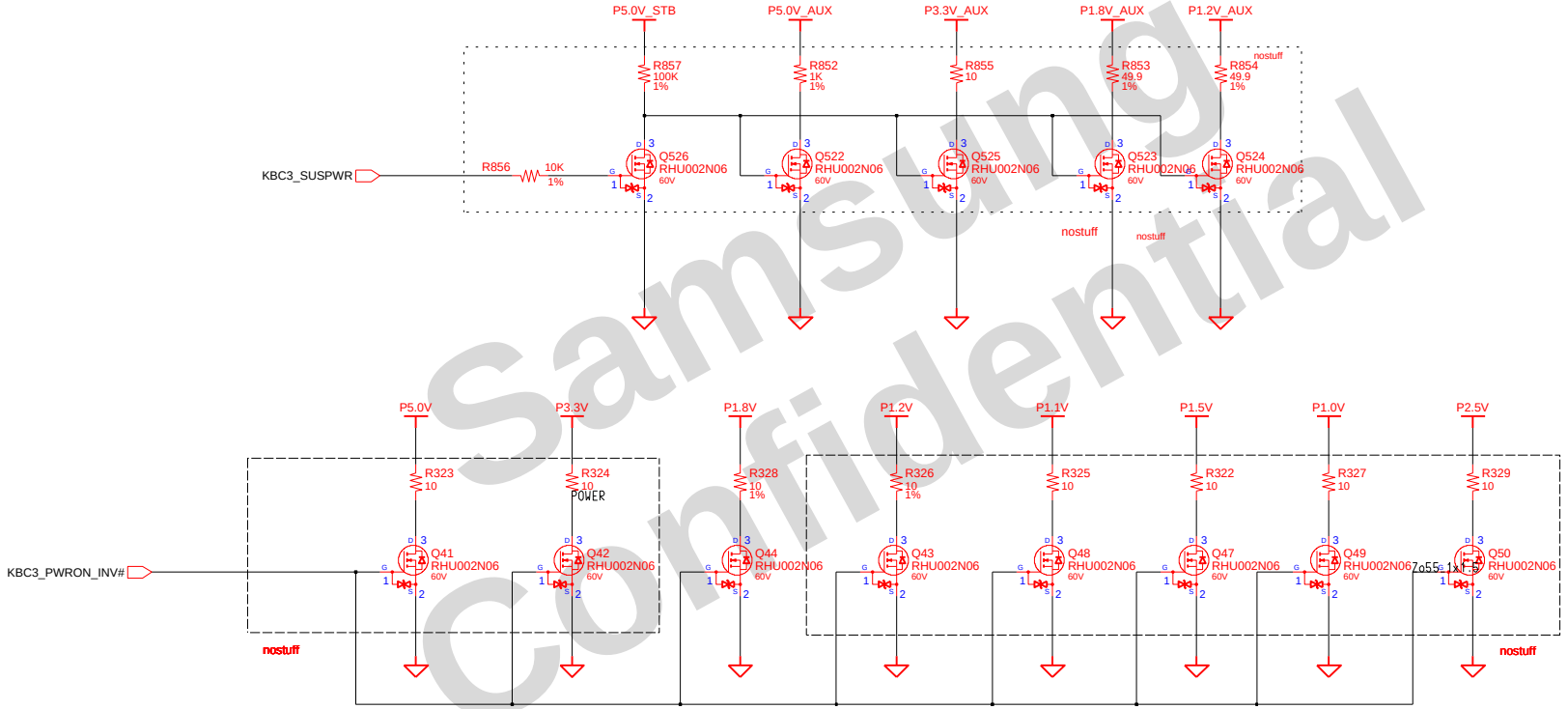

## P1.2V_AUX






| | | | |
|---|---|---|---|
| DESIGN: H.J.Ra | DATE: 8/22/2009 | TITLE: Bremen-D<br>PWR_MV_SWITCHED<br>SWITCHED POWER | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 56 OF 61 | |

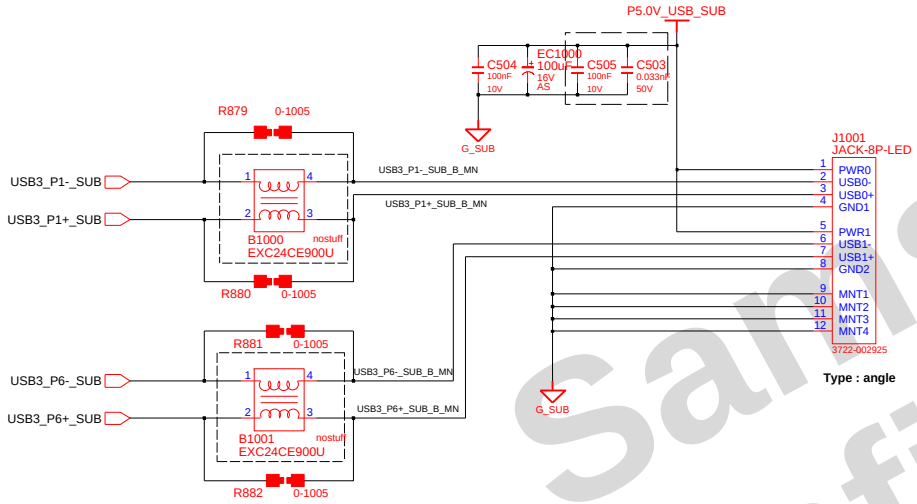
# POWER DISCHARGER





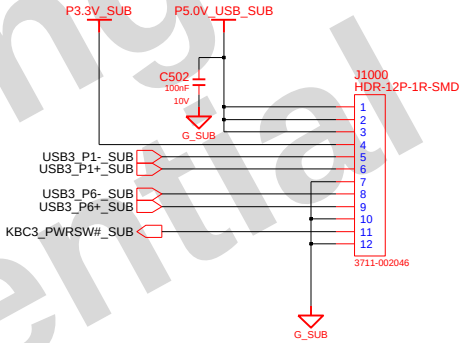

| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | PWR_MV_DISCHARGER | |
| APPROVAL: H.K.Park | REV: 1.1 | DISCHARGER LOGIC | PART NO.: BA41-xxxxxA |
| MODULE CODE: undefined | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 57 OF 61 | |

# 2 USB PORT & POWER S/W SUB B'D

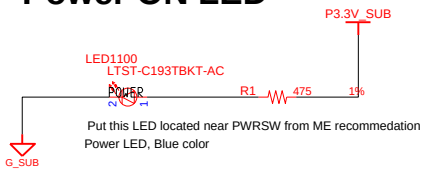



Type : angle

## SUB TO MAIN USB CONN

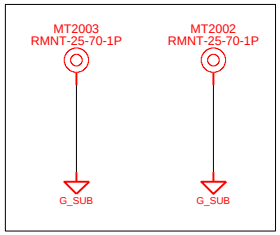



## Power ON LED




Put this LED located near PWRSW from ME recommedation
Power LED, Blue color

## Power Button

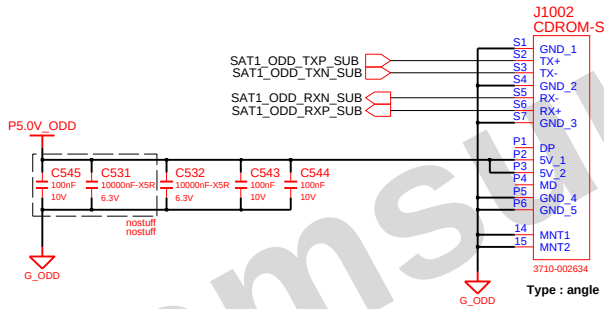

USB sub board mount hole



| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / SUB BOARD1 / USB PORT, POWER SW SUB BOARD | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 58 OF 61 | |

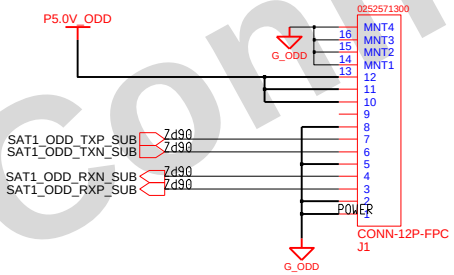
# SATA ODD SUBBOARD

## SATA ODD CONN

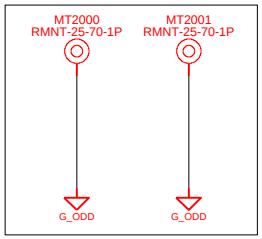



Type : angle

## SUB TO MAIN SATA ODD CONN




Type : angle

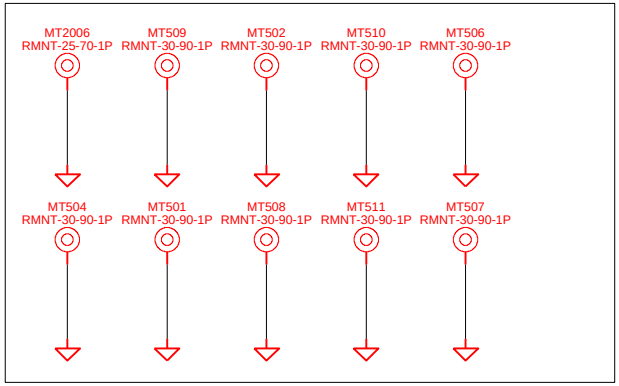



ODD sub board mount hole

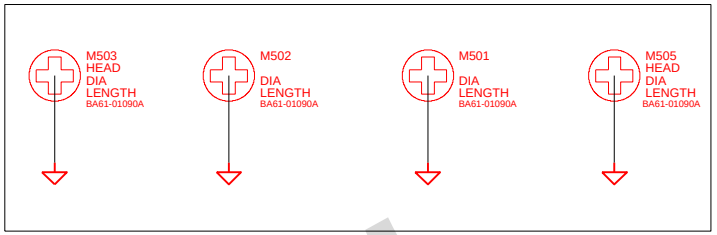


| | | | |
|---|---|---|---|
| DRAW H.J.Ra | DATE 9/23/2008 | TITLE Bremen-D | SAMSUNG ELECTRONICS |
| CHECK K.Y.Kim | DEV. STEP ADV1 | SUB BOARD2 | |
| APPROVAL H.K.Park | REV 1.1 | SATA ODD SUB BOARD | PART NO. BA41-xxxxxA |
| MODULE CODE undefined | LAST EDIT October 10, 2009 16:50:44 PM | PAGE 59 OF 61 | |

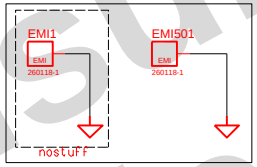
## Mainboard Mount



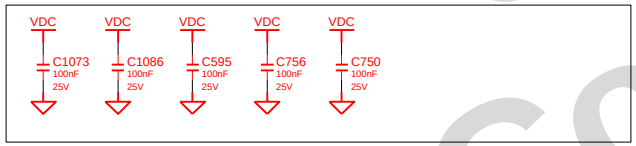

(30,90) x 7, (25,70) x 1



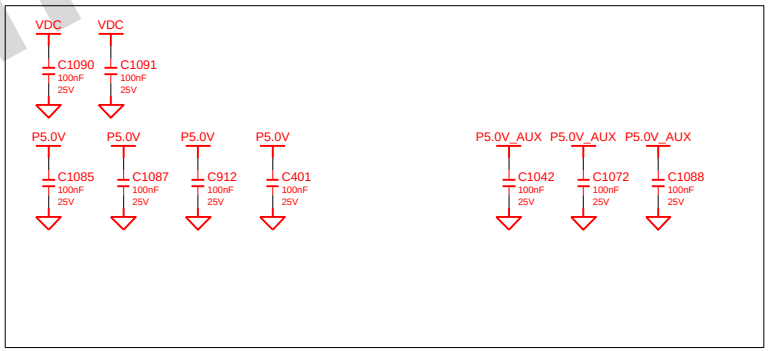

To Support Heatsink




EMI Finger




Add for EMC (Bottom)




Add for EMC (Bottom)

| | | | |
|---|---|---|---|
| DRAW: H.J.Ra | DATE: 9/23/2008 | TITLE: Bremen-D / MAIN / MOUNT HOLE | SAMSUNG ELECTRONICS |
| CHECK: K.Y.Kim | DEV. STEP: ADV1 | | |
| APPROVAL: H.K.Park | REV: 1.1 | | PART NO.: BA41-xxxxxA |
| MODULE CODE: | LAST EDIT: October 10, 2009 16:50:44 PM | PAGE 60 OF 61 | |

- ADT3_SEL#
- ANS_CHGVR_BG_MN
- ANS_CHGVR_VDC_ADPT_RQ_MN
- ANS_CHGVR_VDC_CHG_BJ_MN
- ANS_CHSETVR_BG_MN
- ANS_CHSETVR_P1.2V_LGATE_MN
- ANS_CPUVR_BG1_MN
- ANS_CPUVR_BG2_MN
- ANS_CPUVR_VDD_BG_MN
- ANS_DDR3VR_BG_MN
- ANS_EGFXVR_BG_MN
- ANS_GDDR3VR_LGATE_MN
- ANS_SYSVR_BG1_MN
- ANS_SYSVR_BG2_MN
- AUX3_PWRGD
- BAT3_DETECT#
- BAT3_SMCLK#
- BAT3_SMDATA#
- BIOS_0_R_MN
- BIOS_W#_R_MN
- B_VS_VREF_R_MN
- CHESETVR_P1.2V_TON_MN
- CHGVR_ACLIM_MN
- CHGVR_ACSET_MN
- CHGVR_BAT3_DETECT#_CBJ_MN
- CHGVR_BAT3_SMCLK#_CBJ_MN
- CHGVR_BAT3_SMDATA#_CBJ_MN
- CHGVR_CHLIM_MN
- CHGVR_CHLIM_RQ_MN
- CHGVR_CSIN_MN
- CHGVR_CSIP_MN
- CHGVR_CSON_MN
- CHGVR_CSOP_MN
- CHGVR_DCIN_MN
- CHGVR_DCJACK_RCQ_MN
- CHGVR_DCPRN_MN
- CHGVR_DCSET_MN
- CHGVR_EN_MN
- CHGVR_ICM_MN
- CHGVR_ICM_RC_MN
- CHGVR_ICOMP_MN
- CHGVR_KBC3_CHG4.2V_RQ_MN
- CHGVR_KBC3_PRECHG_RQ_MN
- CHGVR_P3.3V_MICOM_RQ_MN
- CHGVR_PHASE_RL_MN
- CHGVR_SGATE_MN
- CHGVR_SGATE_RRQ_MN
- CHGVR_VADJ_MN
- CHGVR_VADJ_RQ_MN
- CHGVR_VCOMP_MN
- CHGVR_VCOMP_RC_MN
- CHGVR_VDDP_MN
- CHGVR_VDD_MN
- CHP3_BIOSWP#
- CHP3_BIOS_CRI#
- CHP3_INTRUDER#
- CHP3_NB_PWRGD
- CHP3_PFOFF#
- CHP3_RTCCLK
- CHP3_RTCRST#_R_D_MN
- CHP3_SATALED#
- CHP3_SATALED#_LED_MN
- CHP3_SB_TEST0
- CHP3_SB_TEST1
- CHP3_SB_TEST2
- CHP3_SERIRQ
- CHP3_SLPS3#
- CHP3_SLPS5#
- CHP3_SUSSTAT#
- CHP3_THRMTRIP#
- CHSETVR_EN_PSV_MN
- CHSETVR_P1.2V_EN_MN
- CHSETVR_P1.2V_FB_MN
- CHSETVR_P1.2V_OCSET_MN
- CHSETVR_P1.2V_POK_MN
- CHSETVR_P1.2V_VCC_MN
- CHSETVR_PGOOD_MN
- CHSETVR_TON_MN
- CHSETVR_TRIP_MN
- CHSETVR_VCC_MN
- CHSETVR_VFB_MN
- CPU1_LDTREQ#
- CPU1_ALL_LDTSTP
- CPU1_LDTRST#
- CPU1_LDTSTP#
- CPU1_PROCHOT#
- CPU1_PWRGDCPU
- CPU1_SIC
- CPU1_SID
- CPU1_SVC
- CPU1_SVD
- CPU1_THRMTRIP#
- CPU1_VDDIO_FB
- CPU1_VDDIO_FB#
- CPU1_VDDNB_FB
- CPU1_VDDNB_FB#
- CPU1_VDD_FB
- CPU1_VDD_FB#
- CPU1_VTTSENSE
- CPUVR_COMP_0_MN
- CPUVR_COMP_NB_MN
- CPUVR_ENABLE_MN
- CPUVR_FB_0_MN
- CPUVR_FB_NB_MN
- CPUVR_FSET_NB_MN
- CPUVR_ISP_0_MN
- CPUVR_OCSET_MN
- CPUVR_OFS_VFIXEN_MN
- CPUVR_RBIAS_MN
- CPUVR_RTN1_MN
- CPUVR_VIDIFF_0
- CPUVR_VIN_MN
- CPUVR_VSEN1_MN
- CPUVR_VW0_MN
- CPU_DBREQ_L_R_MN
- CPU_VDDA1_B_MN
- CRT3_BLUE
- CRT3_BLUE_L_MN
- CRT3_DDCCLK
- CRT3_DDCDATA
- CRT3_GREEN
- CRT3_GREEN_L_MN
- CRT3_HSYNC
- CRT3_P5.0V_D_MN
- CRT3_RED
- CRT3_RED_L_MN
- CRT3_VSYNC
- CRT5_DDCCLK
- CRT5_DDCDATA
- CRT5_VDDCDATA_CLK_D_MN
- CRT5_HSYNC_R_MN
- CRT5_VSYNC_R_MN
- DDR3VR_EN_PSV_MN
- DDR3VR_KBC3_PWRON_P0.75V_RCQ_MN
- DDR3VR_KBC3_SUSPWR_RRD_MN
- DDR3VR_P5.0V_ALW_VREF_RQ_MN
- DDR3VR_PGOOD_MN
- DDR3VR_TON_MN
- DDR3VR_TRIP_MN
- DDR3VR_VCC_MN
- DDR3VR_VFB_MN
- EGFXVR_EN_MN
- EGFXVR_FB_MN
- EGFXVR_P1.0V_KBC3_PWRON_R_MN
- EGFXVR_P1.0V_P5.0V_AUX_MN
- EGFXVR_P1.0V_VREF_MN
- EGFXVR_P1.0V_VOUT_MN
- EGFXVR_SET0_MN
- EGFXVR_SET1_MN
- EGFXVR_SET2_MN
- EGFXVR_SREF_MN
- EGFXVR_VCC_MN
- EGFXVR_VO_MN
- FAN3_FDBACK#
- FAN5_VDD
- GDDR3VR_EN_MN
- GDDR3VR_FB_MN
- GDDR3VR_OCSET_MN
- GDDR3VR_POK_MN
- GDDR3VR_TON_MN
- LCD3_BRIT
- LCD3_EDID_CLK
- GDDR3VR_VCC_MN
- GFX1_MVREFDA_MN
- GFX1_MVREFSA_MN
- GFX3_GPIO2
- GFX3_VOLTID0
- GFX3_VOLTID1
- GFX3_VOLTID2
- GFX_AVDD_B_MN
- GFX_CLKTESTA_C_R_MN
- GFX_DPA_VDD10_B_MN
- GFX_DPA_VDD18_B_MN
- GFX_DPCD_CALR_R_MN
- GFX_DPEF_CALR_R_MN
- GFX_DPE_PVDD_B_MN
- GFX_DPE_VDD10_B_MN
- GFX_DPE_VDD18_B_MN
- GFX_DPLL_PVDD_B_MN
- GFX_DPLL_VDDC_B_MN
- GFX_DVPDATA_20_R_MN
- GFX_GPIO_18_HPD3_R_MN
- GFX_GPIO_5_AC_BATT_R_MN_MN
- GFX_MPV18_1_B_MN
- GFX_MPV18_2_B_MN
- GFX_MVREFDB_R_MN
- GFX_PCIE_PVDD_B_MN
- GFX_PCIE_VDDR_I_MN
- GFX_SCL_R_MN
- GFX_SPV10_B_MN
- GFX_SPV18_B_MN
- GFX_TSVDD_B_MN
- GFX_VDDR4_1_B_MN
- GFX_VDDR4_2_B_MN
- GFX_VDD_CT_B_MN
- GFX_VREFG_R_MN
- GMAL_VREFCA0_R_MN
- GMAL_VREFCA1_R_MN
- GMAL_VREFDQ0_R_MN
- GMAL_VREFDQ1_R_MN
- GMAU_VREFCA0_R_MN
- GMAU_VREFDQ0_R_MN
- GMAU_VREFDQ1_R_MN
- GMAU_ZQ_ZQ00_R_MN
- GMAU_ZQ_ZQ01_R_MN
- GMBL_VREFCA0_R_MN
- GMBL_VREFCA1_R_MN
- GMBL_VREFDQ0_R_MN
- GMBL_VREFDQ1_R_MN
- GMBL_ZQ_ZQ00_R_MN
- GMBU_VREFCA0_R_MN
- GMBU_VREFCA1_R_MN
- GMBU_VREFDQ0_R_MN
- GMBU_ZQ_ZQ00_R_MN
- GMBU_ZQ_ZQ01_R_MN
- KBC3_A20G
- KBC3_BATDET#
- KBC3_BKLTON
- KBC3_CAPSLED#
- KBC3_CAPSLED#_LED_MN
- KBC3_CHG4.2V
- KBC3_CHGEN
- KBC3_CPURST#
- KBC3_EMCLK_R_MN
- KBC3_EMDAT_R_MN
- KBC3_EXTSMI#
- KBC3_KCLK_R_MN
- KBC3_KDAT_R_MN
- KBC3_LED_ACIN#
- KBC3_LED_ACIN#_R_MN
- KBC3_LED_CHARGE#
- KBC3_LED_CHARGE#_R_MN
- KBC3_LED_POWER#
- KBC3_LED_POWER#_R_MN
- KBC3_PRECHG
- KBC3_PWRBTN#
- KBC3_PWRGD
- KBC3_PWRGD_R_MN
- KBC3_PWRON_INV#
- KBC3_PWRON_INV#_QR_MN
- KBC3_PWRON_INV#_RQ_MN
- KBC3_PWRON_QR_MN
- KBC3_PWRSW#
- KBC3_RFOFF#
- KBC3_RSMRST#
- KBC3_RST#
- KBC3_RUNSCI#
- KBC3_SMCLK#
- KBC3_SMDATA#
- KBC3_SPI_CLK
- KBC3_SPI_CS0#
- KBC3_SPI_DI
- KBC3_SPI_DO
- KBC3_SPKMUTE#
- KBC3_SUSPWR
- KBC3_THERM_SMCLK
- KBC3_THERM_SMDATA
- KBC3_USBPWRON#
- KBC3_VRON
- KBC3_WAKESCI#
- KBC3_WLON_LED#
- KBC5_KSI(0)
- KBC5_KSI(1)
- KBC5_KSI(2)
- KBC5_KSI(3)
- KBC5_KSI(4)
- KBC5_KSI(5)
- KBC5_KSI(6)
- KBC5_KSI(7)
- KBC5_KSO(0)
- KBC5_KSO(1)
- KBC5_KSO(10)
- KBC5_KSO(11)
- KBC5_KSO(12)
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- KBC5_KSO(14)
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- KBC5_KSO(4)
- KBC5_KSO(5)
- KBC5_KSO(6)
- KBC5_KSO(7)
- KBC5_KSO(8)
- KBC5_KSO(9)
- KBC5_LED_CTRL
- KBC5_LED_CTRL_R_MN
- KBC5_LED_CTRL_R_Q_MN
- KBC5_LED_CTRL_R_Q_R_MN
- KBC5_TCLK
- KBC5_TDATA
- LID_SWITCH#
- LPC3_CLKO
- LPC3_CLK1
- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)
- LPC3_LFRAME#
- MCD3_SDCD#
- MCD3_SDCLK
- MCD3_SDCMD
- MCD3_SDDATA0
- MCD3_SDDATA1
- MCD3_SDDATA2
- MCD3_SDDATA3
- MCD3_SDWP
- MCH3_EXTTS0#
- MCH3_EXTTS1#
- MEM0_SA0_R_MN
- MEM0_SA1_R_MN
- MEM_CALRN1
- NB_HT_RXCALN_R_MN
- NB_IOPLLVDD18_NC_R_MN
- NB_KBC3_PWRGD_Q_MN
- NB_PCE_CALRN_PCE_BCALRN_R_MN
- NB_PCE_CALRP_PCE_BCALRP_R_MN
- NB_POWERGOOD_R_MN
- NB_SYSRESET#_R_MN
- NB_TESTMODE_R_MN
- NB_VDDA18HTPLL_B_MN
- NB_VDDA18PCIEPLL_B_MN
- P1.2V_AUX_ADJ_MN
- P2.5V_ADJ_MN
- P3.3V_VDD_INV_EN_MN
- P3.3V_VDD_INV_EN_QR_MN
- P3.3V_VDD_INV_EN_Q_MN
- PEG3_BKLTEN
- PEG3_HDMI_CLK
- PEG3_HDMI_DATA
- PEG3_HPD_HDMI
- PEG3_LCDVDDON
- PEG5_5V_POWER_D_MN
- PEG5_HDMI_CLK
- PEG5_HDMI_DATA
- PEG5_HOT_PLUG_DETECT_R_MN
- PEX3_WAKE#
- PLT3_RST#
- PNS_CHGVR_BST_MN
- PNS_CHGVR_BST_RC_MN
- PNS_CHGVR_DCJACK_MN
- PNS_CHGVR_DCJACK_QB_MN
- PNS_CHGVR_PHASE_MN
- PNS_CHGVR_PHASE_RC_MN
- PNS_CHGVR_TG_MN
- PNS_CHSETVR_BST_MN
- PNS_CHSETVR_BST_RC_MN
- PNS_CHSETVR_P1.2V_BOOT_MN
- PNS_CHSETVR_P1.2V_BOOT_RC_MN
- PNS_CHSETVR_P1.2V_PHASE_RC_MN
- PNS_CHSETVR_P1.2V_UGATE_MN
- PNS_CHSETVR_PHASE_MN
- PNS_CHSETVR_PHASE_RC_MN
- PNS_CHSETVR_TG_MN
- PNS_CPUVR_BST1_MN
- PNS_CPUVR_BST1_RC_MN
- PNS_CPUVR_BST2_MN
- PNS_CPUVR_BST2_RC_MN
- PNS_CPUVR_PHASE1_MN
- PNS_CPUVR_PHASE1_RC_MN
- PNS_CPUVR_PHASE2_MN
- PNS_CPUVR_PHASE2_RC_MN
- PNS_CPUVR_TG1_MN
- PNS_CPUVR_TG2_MN
- PNS_CPUVR_VDD_BST_MN
- PNS_CPUVR_VDD_PHASE_MN
- PNS_CPUVR_VDD_PHASE_RC_MN
- PNS_CPUVR_VDD_TG_MN
- PNS_DDR3VR_BST_MN
- SB_PCIE_CALRN_R_MN
- SB_PCIE_CALRP_R_MN
- SB_PCIE_PVDD_B_MN
- PNS_DDR3VR_BST_RC_MN
- PNS_DDR3VR_PHASE_MN
- PNS_DDR3VR_PHASE_RC_MN
- PNS_DDR3VR_TG_MN
- PNS_EGFXVR_BST_MN
- PNS_EGFXVR_BST_RC_MN
- PNS_EGFXVR_PHASE_MN
- PNS_EGFXVR_PHASE_RC_MN
- PNS_EGFXVR_TG_MN
- PNS_GDDR3VR_BOOT_MN
- PNS_GDDR3VR_BOOT_RC_MN
- PNS_GDDR3VR_PHASE_RC_MN
- PNS_GDDR3VR_UGATE_MN
- PNS_SYSVR_BST1_MN
- PNS_SYSVR_BST1_RC_MN
- PNS_SYSVR_BST2_MN
- PNS_SYSVR_BST2_RC_MN
- PNS_SYSVR_PHASE1_MN
- PNS_SYSVR_PHASE1_RC_MN
- PNS_SYSVR_PHASE2_MN
- PNS_SYSVR_PHASE2_RC_MN
- PNS_SYSVR_TG1_MN
- PNS_SYSVR_TG2_MN
- SB_AVDDCK_1.2V_B_MN
- SB_AVDDCK_3.3V_B_MN
- SB_AVDDC_B_MN
- SB_AVDDTXRX_B_MN
- SB_AVDD_SATA_B_MN
- SB_IMC_PWM2_IMC_GPO_16_R_MN
- SB_LLB#_GPIO66_R_MN
- SB_PCIE_VDDR_B_MN
- SB_PLLVDD_SATA_B_MN
- SB_RSMRST#_R_MN
- SB_USB_RCOMP_R_MN
- SB_WAKE#_GEVENT8#_R_MN
- VRM3_CPU_PWRGD
- SMB3_ALERT#
- SMB3_CLK
- SMB3_DATA
- SPI3_CLK
- SPI3_CS0#
- SPI3_MISO
- SPI3_MOSI
- SYSVR_ENTRIP1_MN
- SYSVR_ENTRIP2_MN
- SYSVR_FB1_MN
- SYSVR_FB2_MN
- SYSVR_SKIPSEL_MN
- SYSVR_TONSEL_MN
- SYSVR_VIN_MN
- THM3_ALERT#
- THM3_STP#
- THM3_STPQ_MN
- TH_SHDN_SEL_R_MN
- TH_TRIP_SET_R_MN
- TH_VDD_3V_R_MN
- TPD5_L_BUTTON#
- TPD5_R_BUTTON#
- 1.8V_VDDDI
- 1.8V_VDDDI
- BGATE
- BGATE
- CPU_CORE
- CPU_CORE
- G_AUD
- G_AUD
- G_CHG
- G_CHG
- VCC_CRT
- VDC_ADPT
- VDC_ADPT
- VDC_CHG
- VDC_CHG
- VDD_CPU_NB
- VDD_CPU_NB
- G_CPU
- G_CPU
- G_DDR
- G_DDR
- G_EGFX
- G_EGFX
- G_P1.1V
- G_P1.1V
- G_P1.2V
- G_P1.2V
- G_P1.2V
- G_P1.5V
- G_P1.5V
- G_P3.3V
- G_P3.3V
- LCD_VDD3V
- LCD_VDD3V
- P0.9V_AUX
- P0.9V_AUX
- P1.2V
- P1.2V
- P1.2V_AUX
- P1.2V_AUX
- P1.2V_LAN
- P1.2V_LAN
- P1.8V_A2VDDQ
- P1.8V_A2VDDQ
- P1.8V_AUX
- P1.8V_AUX
- P12.0V_ALW
- P12.0V_ALW
- P2.0V_REF
- P2.39V_VREF
- P2.39V_VREF
- P2.5V
- P2.5V
- P2.5V_LAN
- P2.5V_LAN
- P3.3V_A2VDD
- P3.3V_A2VDD
- P3.3V_AUX
- P3.3V_AUX
- P3.3V_LED
- P3.3V_LED
- P3.3V_MCD
- P3.3V_MCD
- P3.3V_MICOM
- P3.3V_MICOM
- P4.75V_AUD
- P4.75V_AUD
- P5.0V_AUD
- P5.0V_AUD
- P5.0V_AUX
- P5.0V_AUX
- P5.0V_STB
- P5.0V_STB
- PRTC_BAT
- VCC_CRT
- VDD_LED