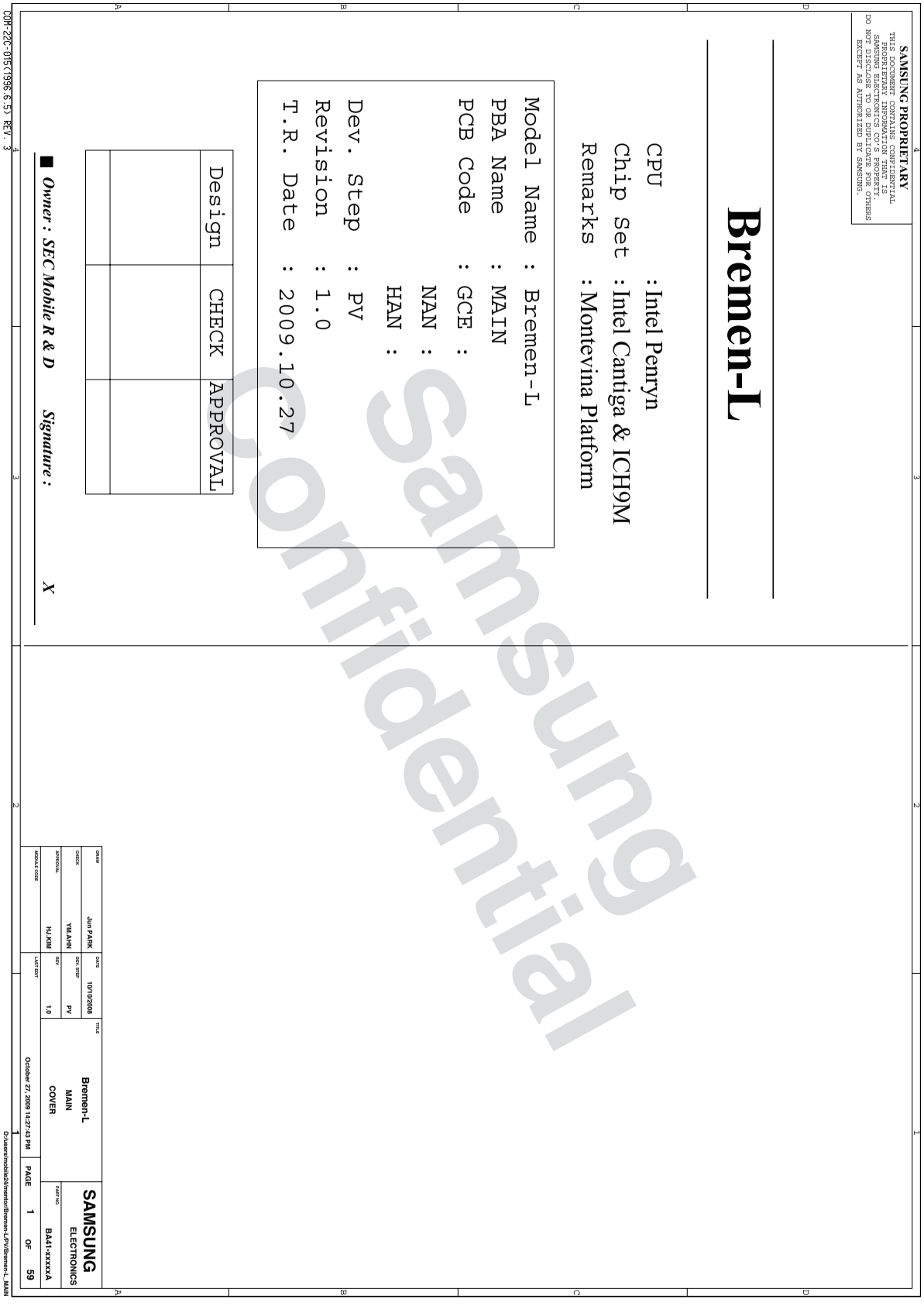
8. Block Diagram and Schematic



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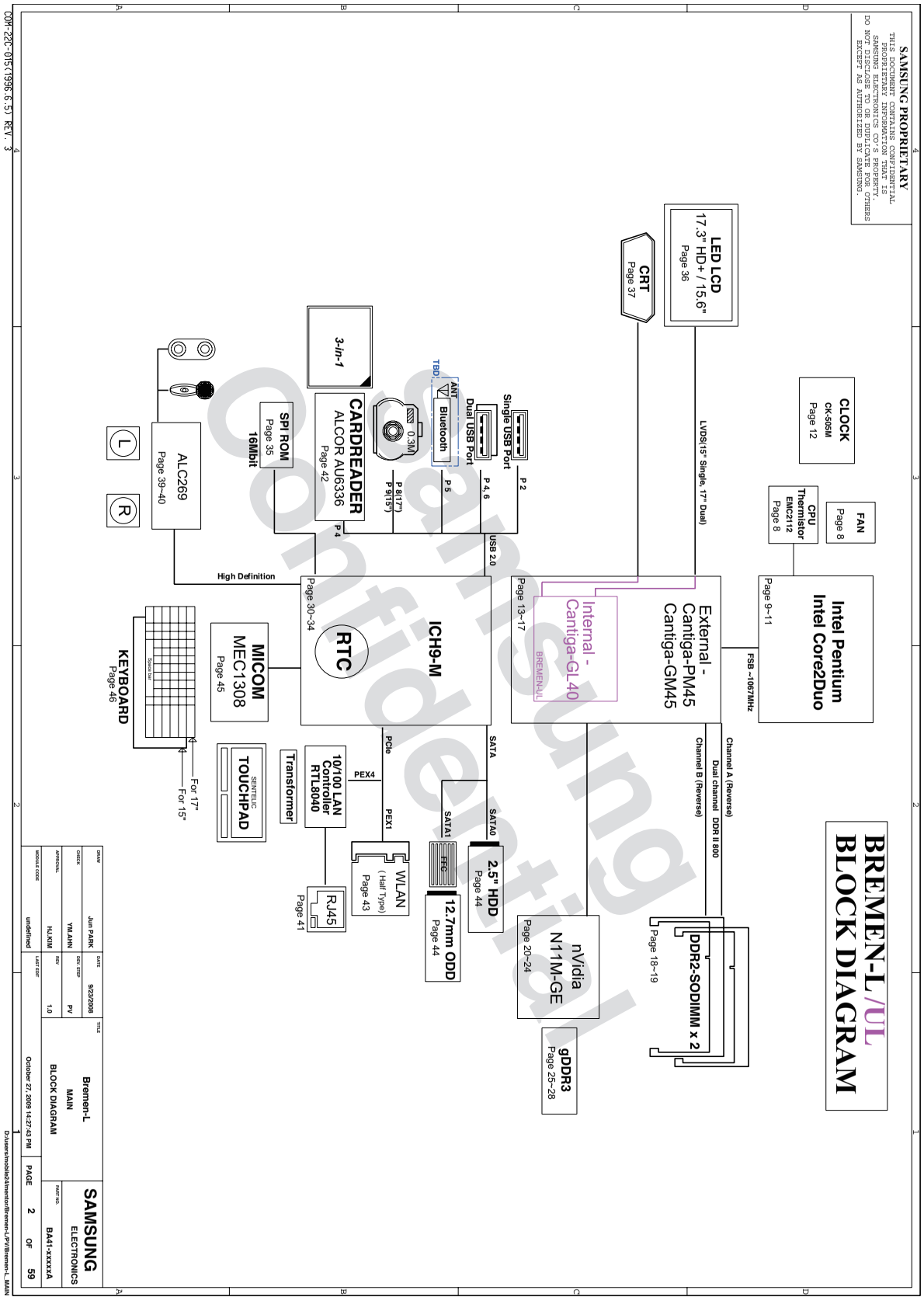


BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9M	**Master**		**SMBUS Master**
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 001X	A4h	
MICOM	**Master**		
BATTERY	0001 011X	16h	
EMC2102	0111 101X	7Ah	

USB PORT Assignation

Port Number		ASSIGNED TO	Port Number		ASSIGNED TO
UHCI_0	0	USB PORT (RIGHT, SUB)	UHCI_3	6	USB PORT (RIGHT, SUB)
	1			7	
UHCI_1	2	USB PORT (LEFT)	UHCI_4	8	CAMERA(17")
	3			9	CAMERA(15")
UHCI_2	4	CARD READER(AU6336)	UHCI_5	10	
	5	BLUETOOTH(TBD)		11	

SATA Assignation

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
SATA0	HDD	SATA1	ODD
SATA2	-	SATA3	-

PCI EXPRESS Assignation

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
PCIe1	WLAN	PCIe2	Wired LAN
PCIe3	-	PCIe4	-

Crystal / Oscillator

TYPE	PREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	
Crystal	10MHz	MICOM	
Crystal	14.318MHz	CLOCK-Generator	
Crystal	25MHz	LAN	

Voltage Rails

Power Rail	Descriptions	Power Rail	Descriptions
VDC_ADPT	Primary DC system power supply (9 to 19V)	***P1.05V_PEG***	P1.05V (Direct Media Interface Compensation)
VDC		***P5.0V***	5.0V Power Rail (off in S3-S5)
VDC_CHG	Charger Reference Voltage Source	***P3.3V***	3.3V Power Rail (off in S3-S5)
PRTC_BAT	3.3V supply for the RTC well.	***P1.05***	1.05V Power Rail (off in S3-S5)
P5.0V_ALW	5.0V always power well	***P0.9V***	DDR2 Termination
P12.0V_ALW	12.0V always power well	***P5.0V_AUX***	5.0V Power Rail (off in S4-S5)
P1.7V_VREF	Power Chip Reference	***P3.3V_AUX***	3.3V Power Rail (off in S4-S5)
P2.0V_VREF	Power Chip Reference	***P1.8_AUX***	1.8V Power Rail (off in S4-S5)
P5.0V_VREF_FILT	Power Chip Reference	***CPU_CORE***	Core Voltage for CPU
P3.3V_MICOM	Output voltage of RT8205AGQW (if VDC is removed, it will be off)	***AUD_P5V***	5.0V supply for Audio
		P4.75V_AUD	Auido Analog Voltage
LCD_VDD3V	3.3V (LED LCD)		
KBC3_CHG4.2V	To charge battery	***P5.0V_STB***	To charge USB device at sleep status
		P5.0V_ODD	5.0V supply at SUB_ODD Board
P1.2V_LAN		***EGFX_CORE***	nVidia Graphic Chip power
P2.5V_LAN	Internal Regulator's Power of LAN Controller	***P1.5V***	1.5V Power Rail (off in S3-S5)
		P1.5_AUX	1.5V Power Rail (off in S4-S5)
P3.3V_MCD	3.3V (3-in-1 Socket)	***P1.8V***	1.8V Power Rail (off in S3-S5)

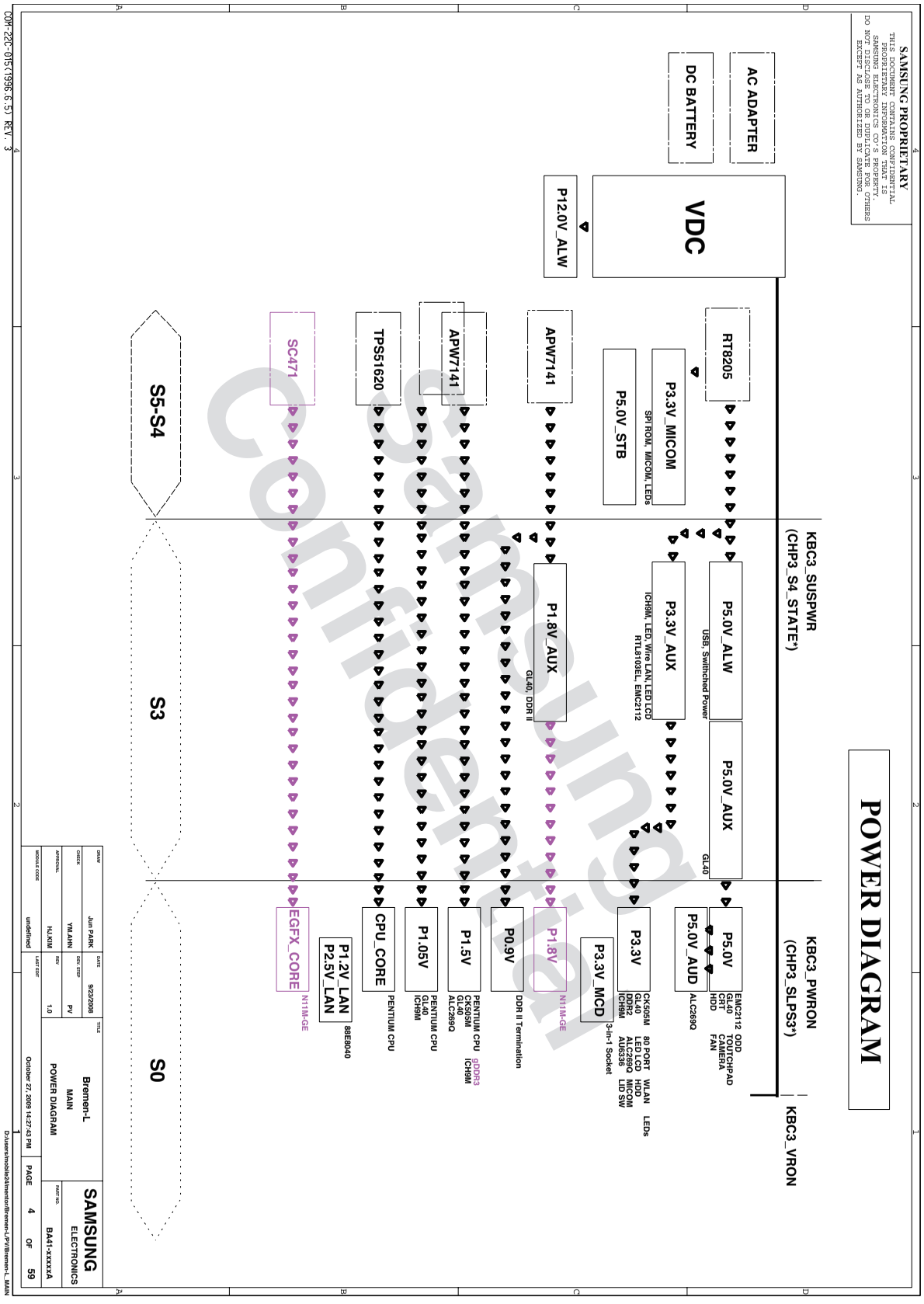
Power source of External

REVISION HISTORY

See rev notes for more information.

DRAW: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L / MAIN / BOARD INFO	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE: undefined	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 3 OF 59	

8. Block Diagram and Schematic



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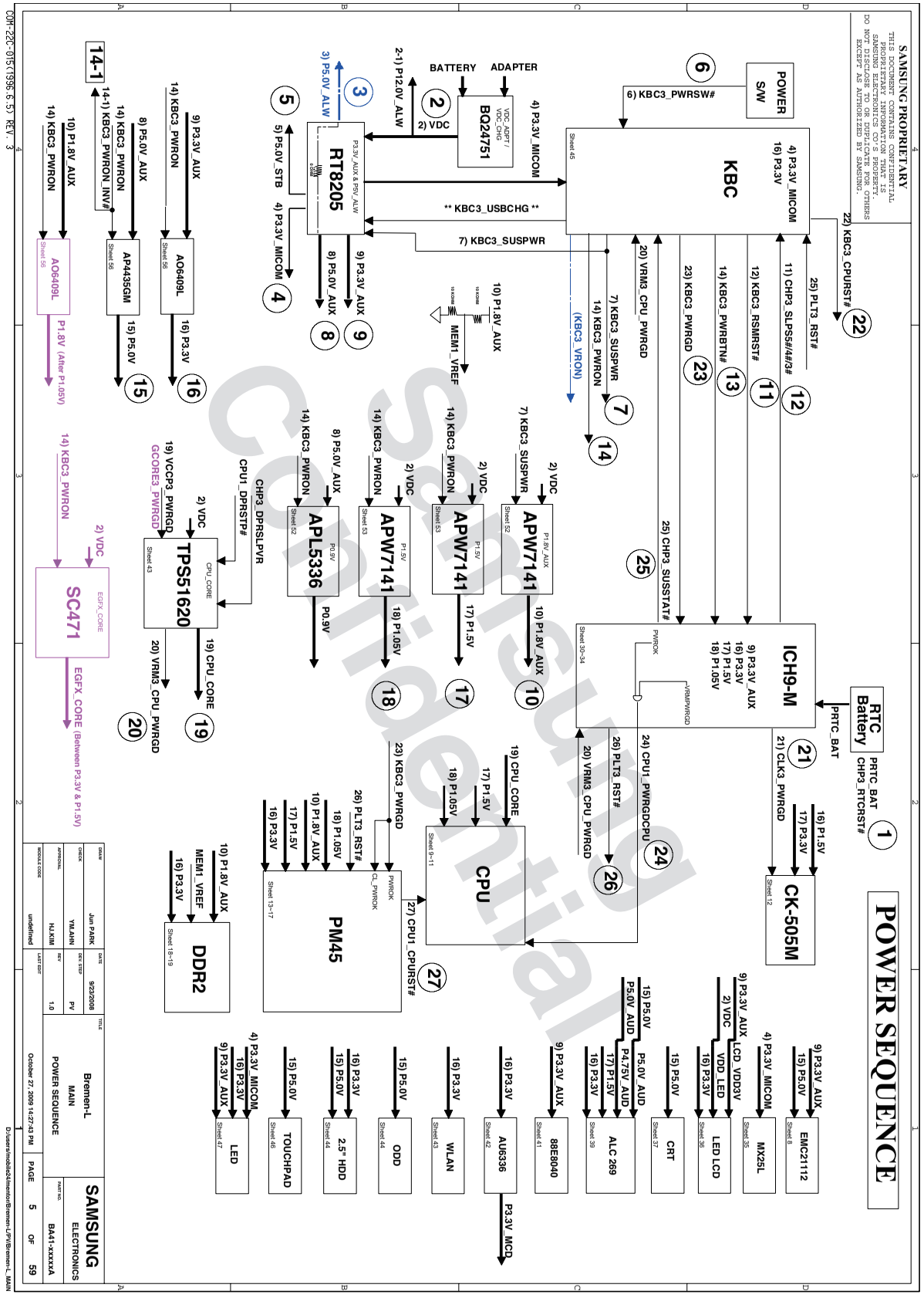

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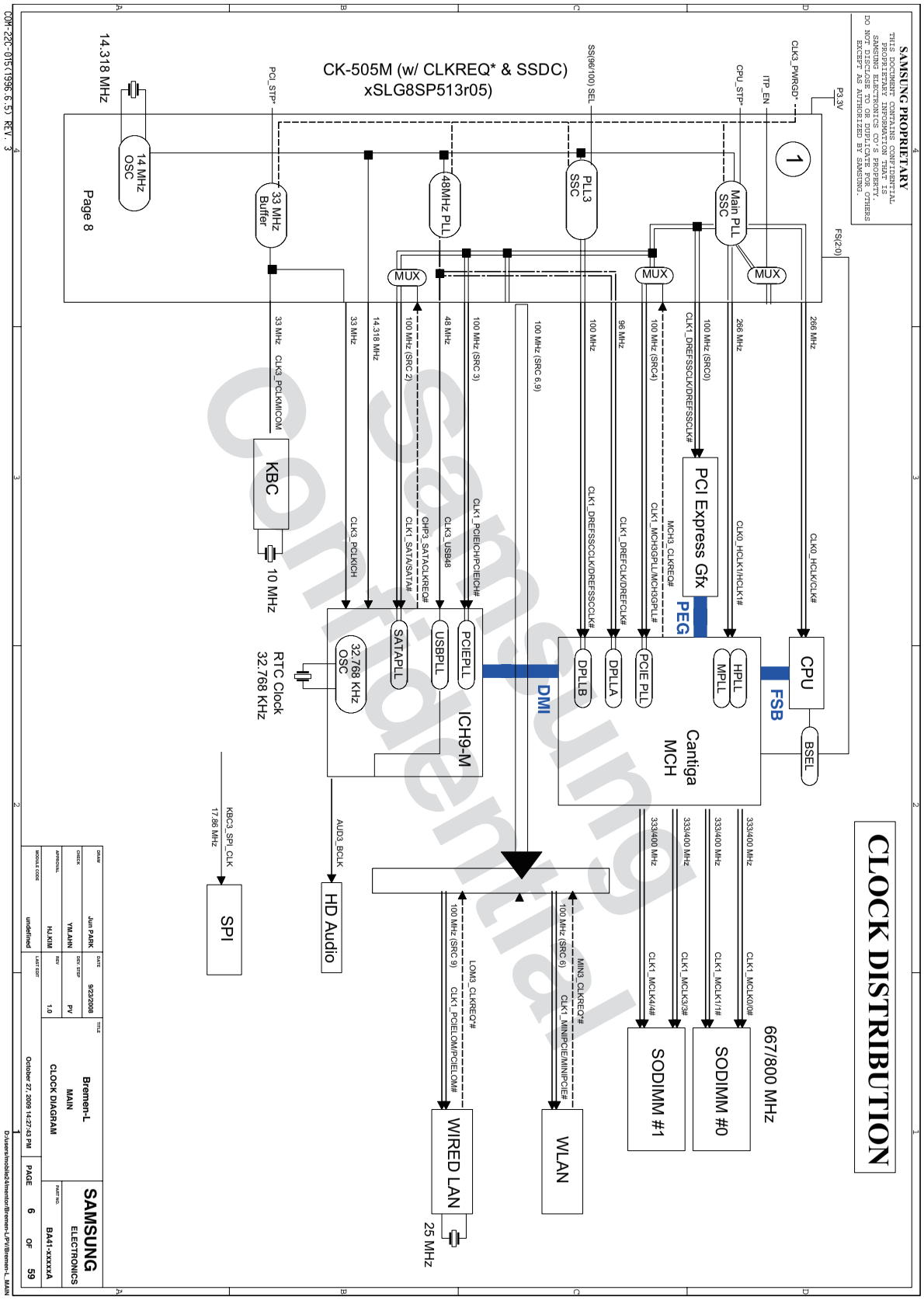
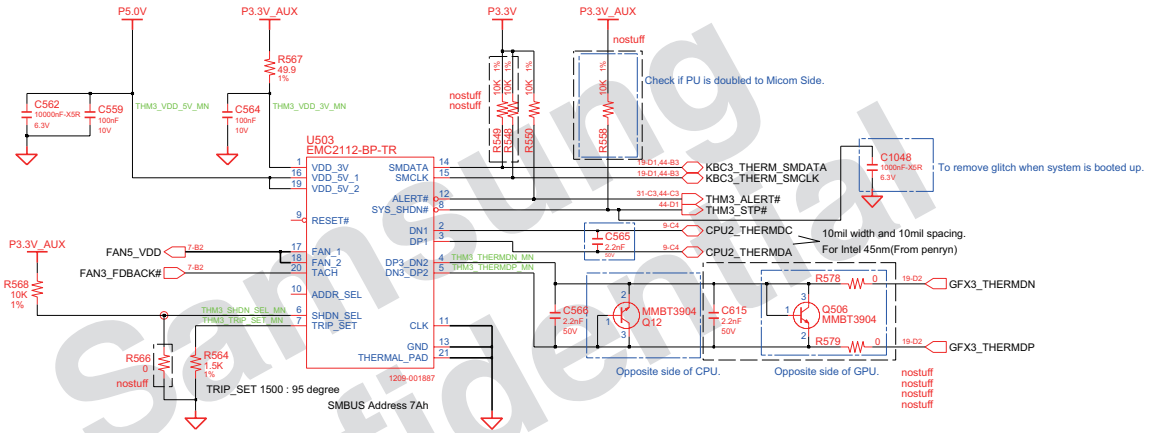
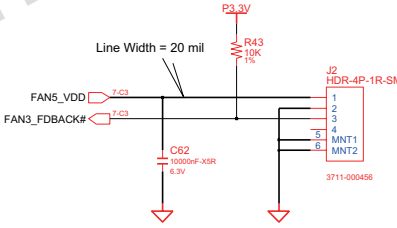


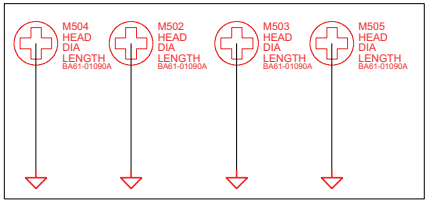
THERMAL SENSOR & FAN CONTROL



SHDN_SEL MODE	
0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

ADDRESSS_SEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb





To support heatsink

DESIGN: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L THERMAL SENSOR THERMAL SENSOR EMC2112	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 7 OF 59	

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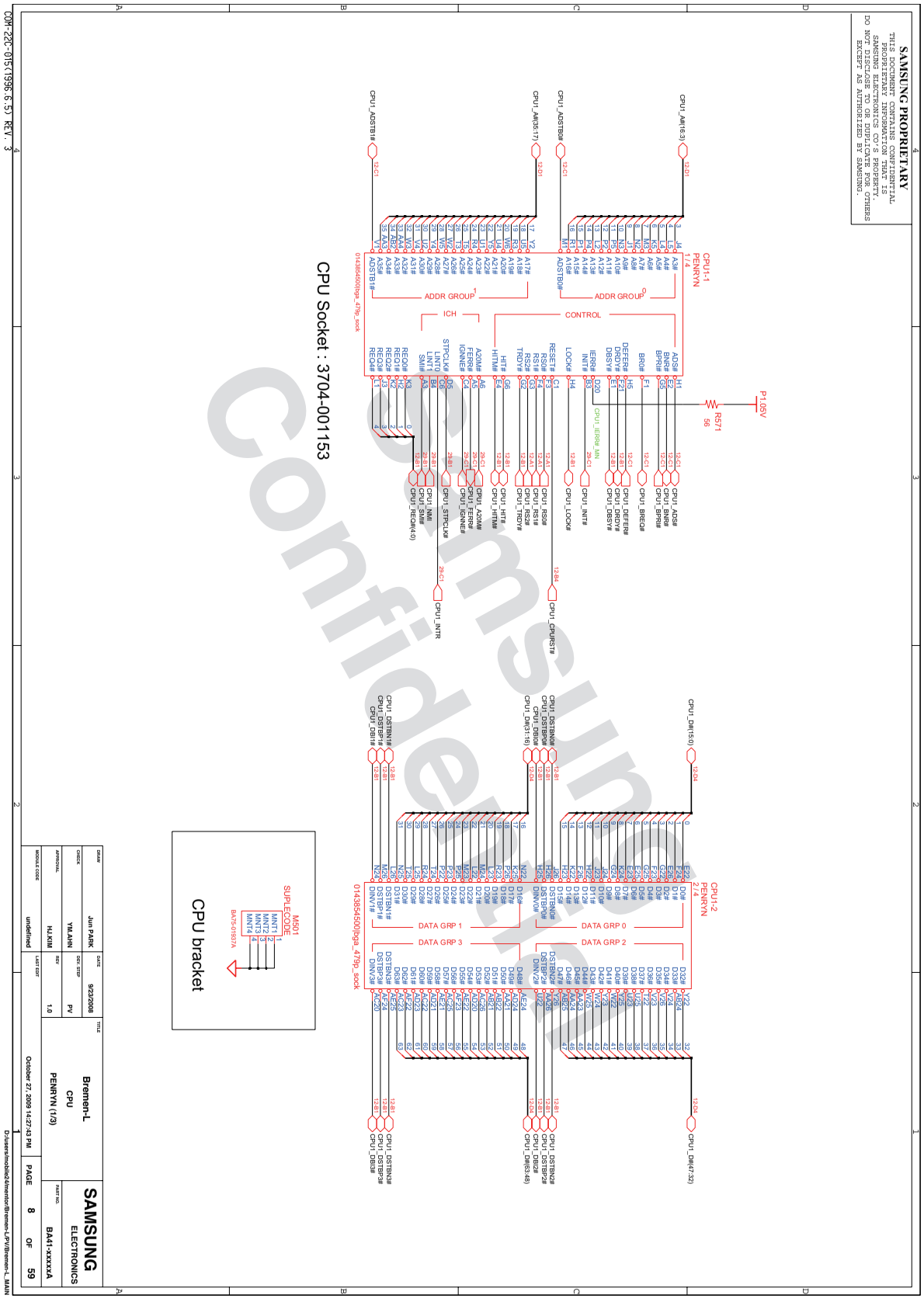
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

8. Block Diagram and Schematic



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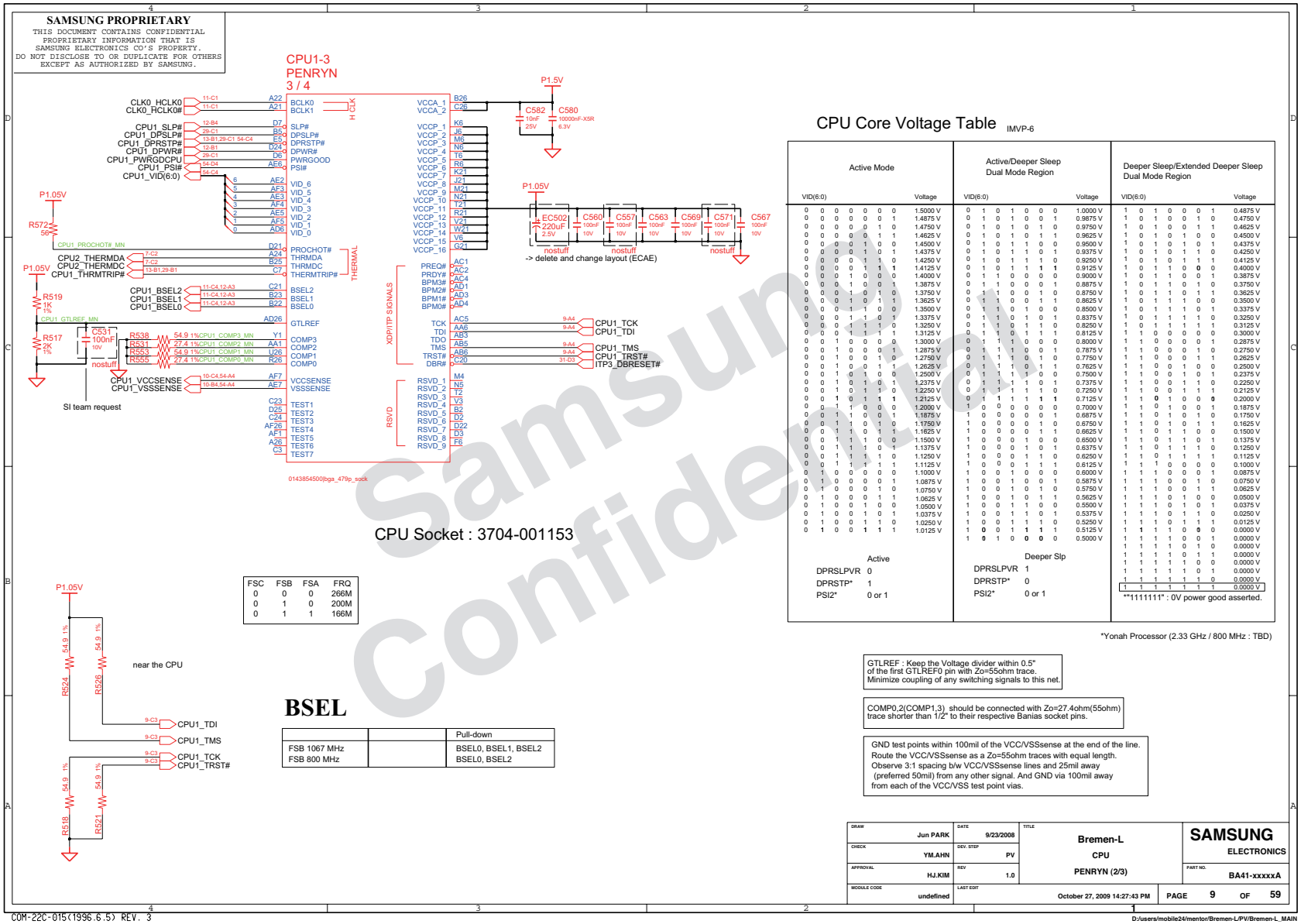

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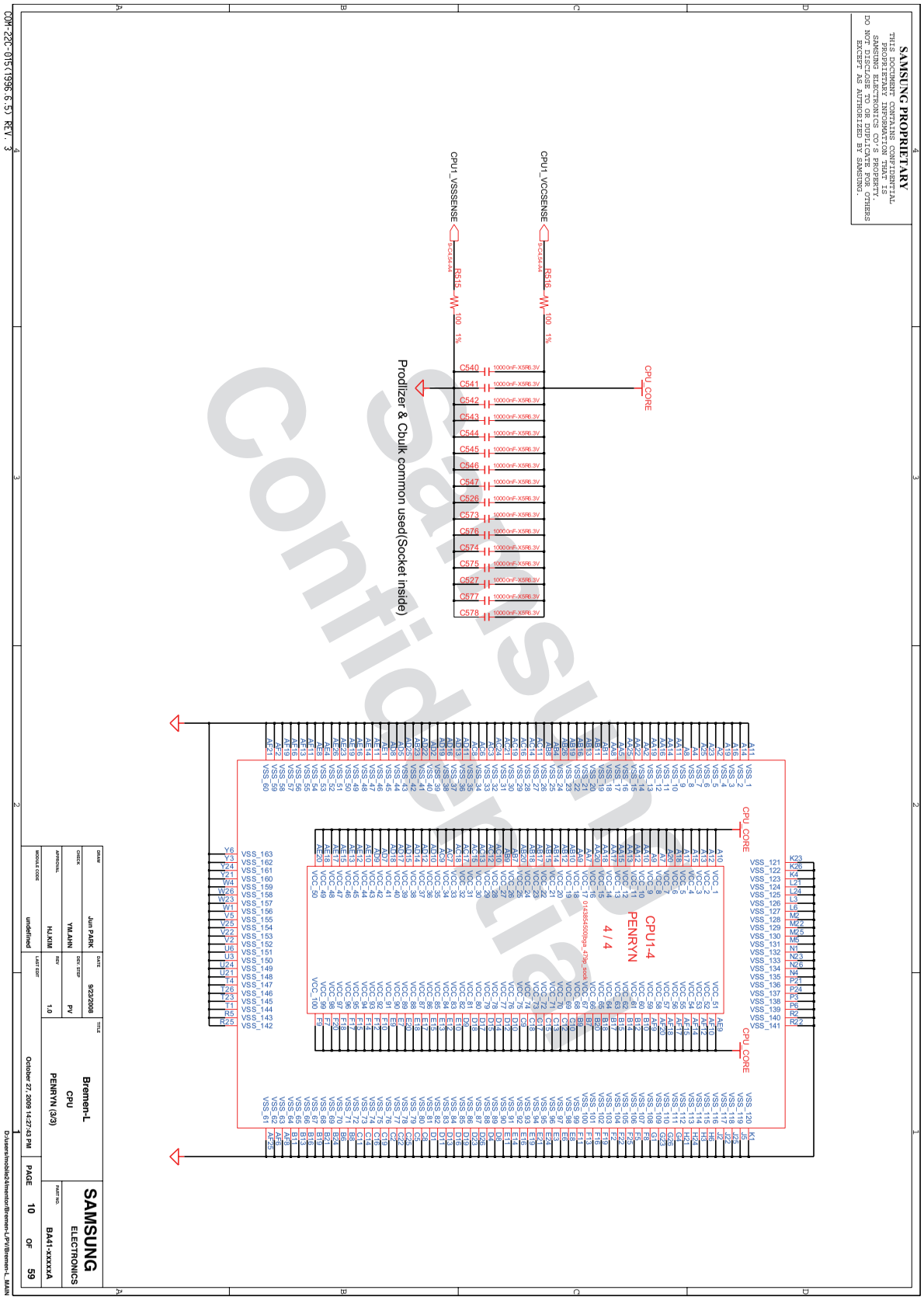

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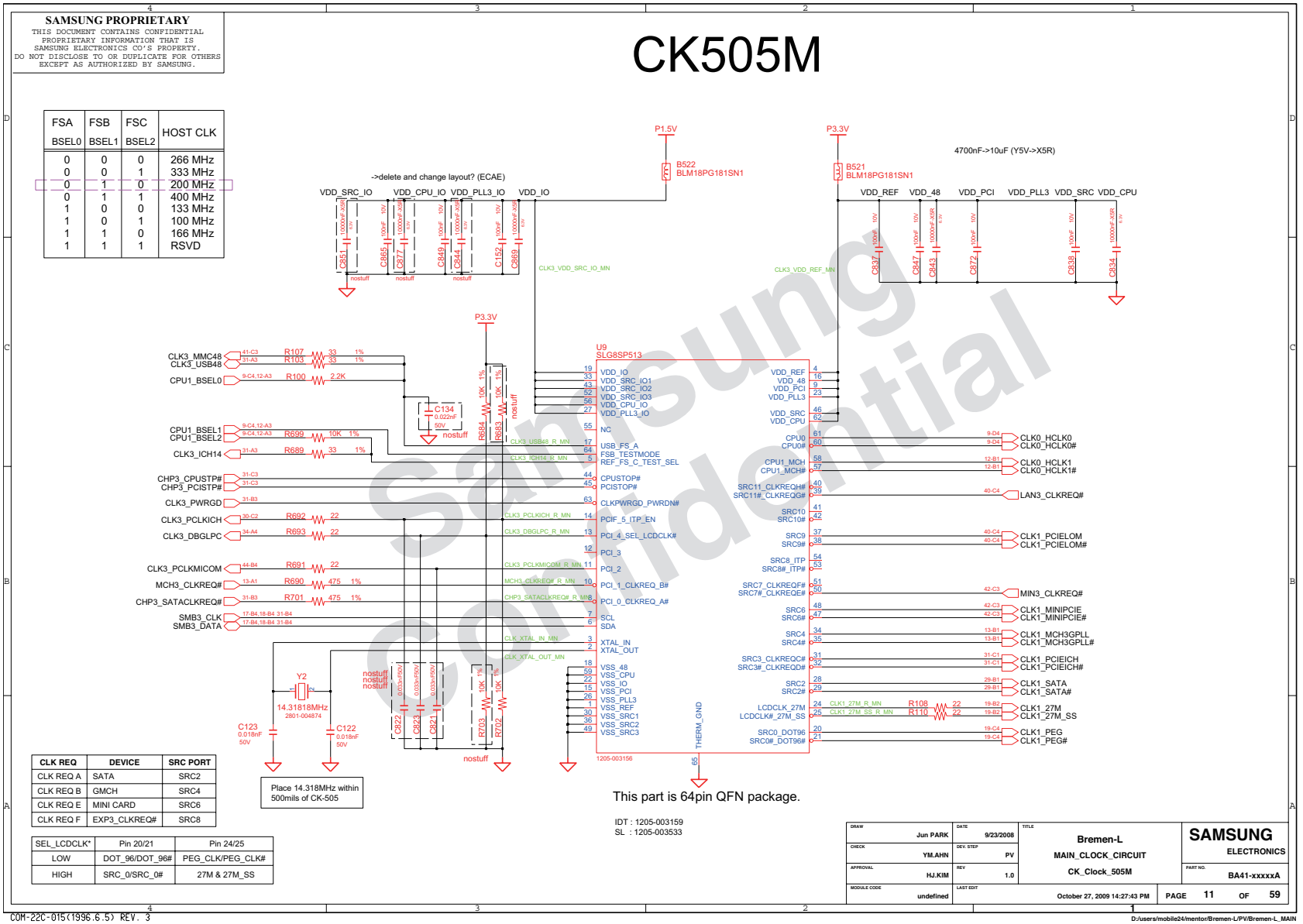

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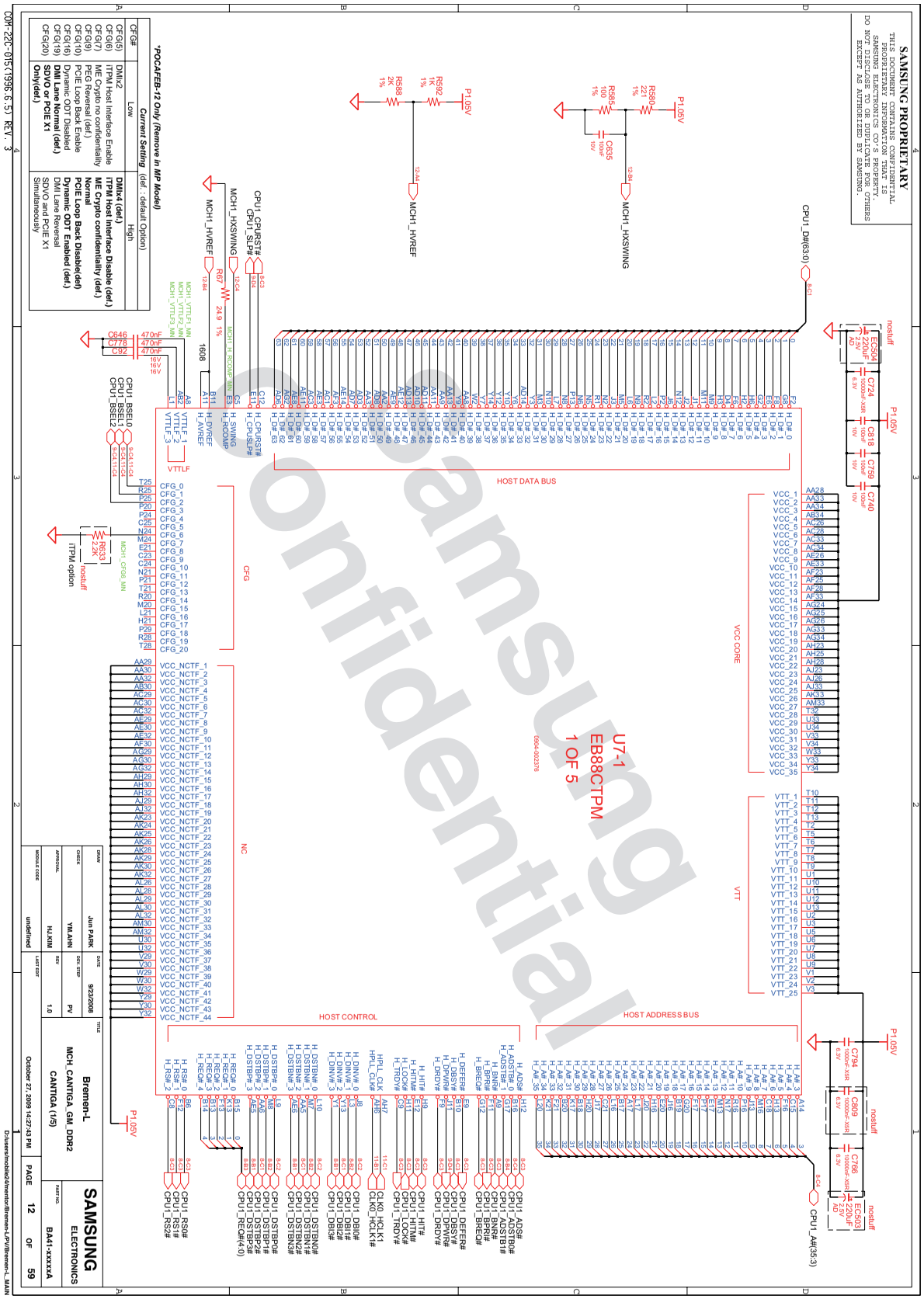

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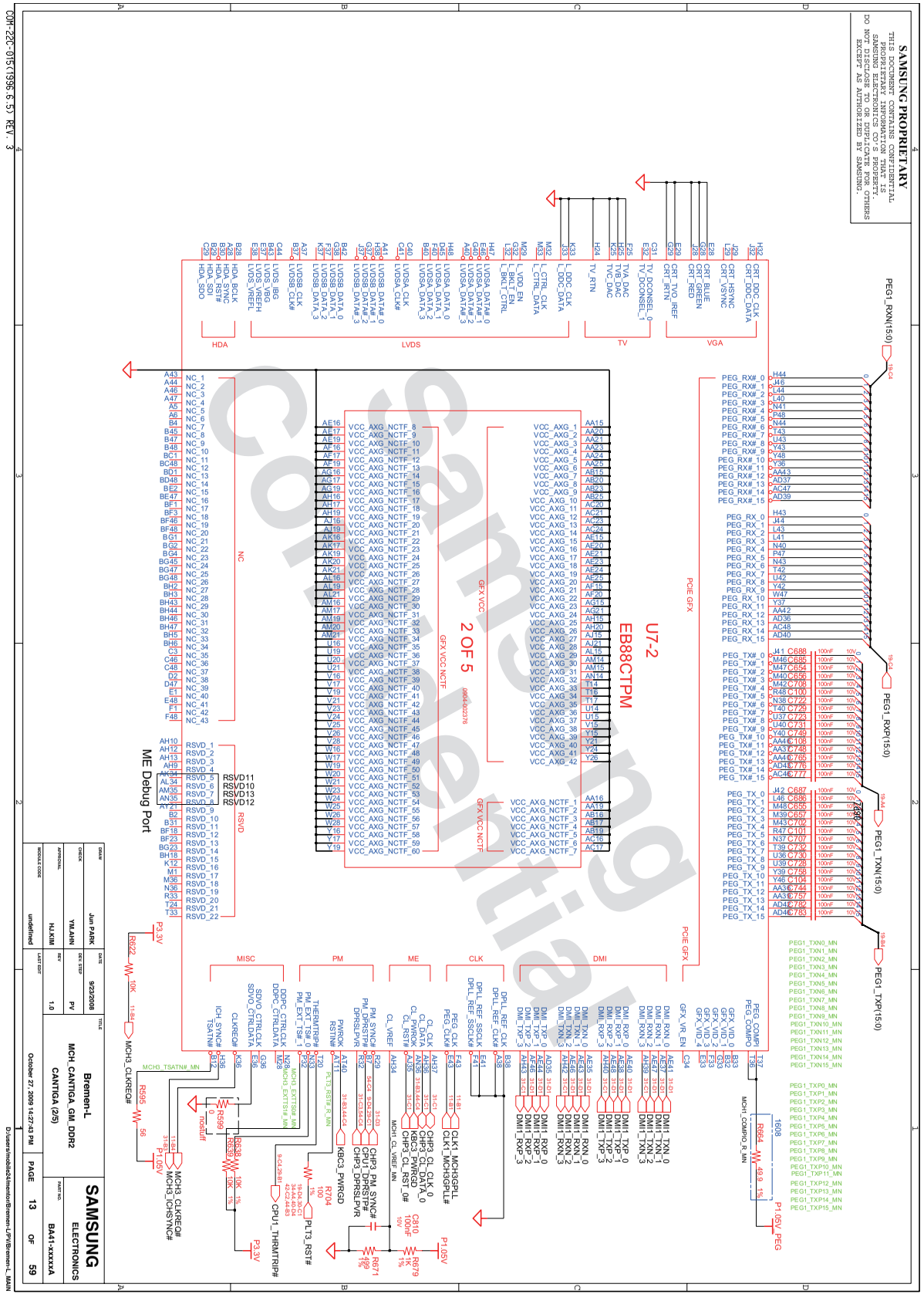

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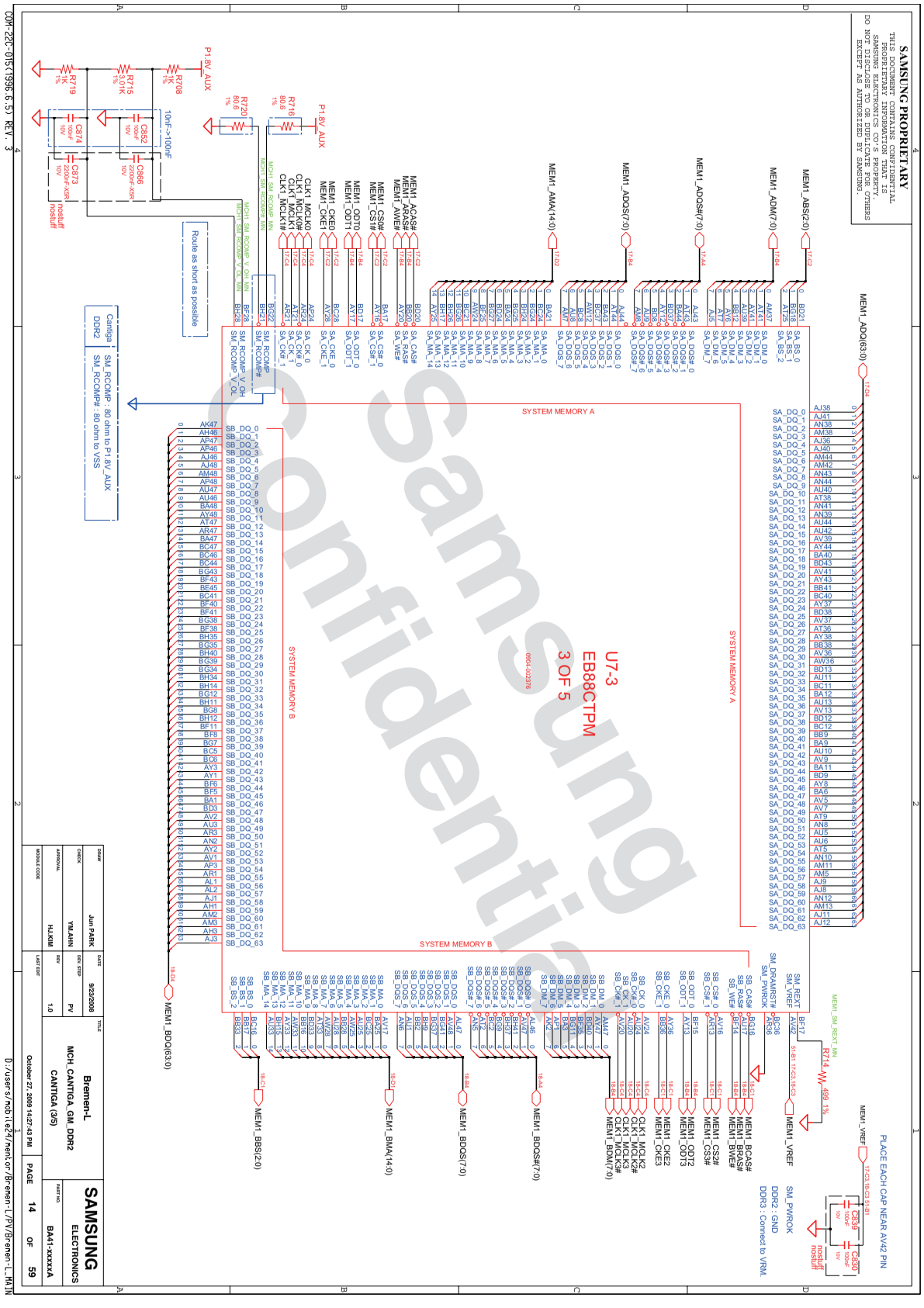

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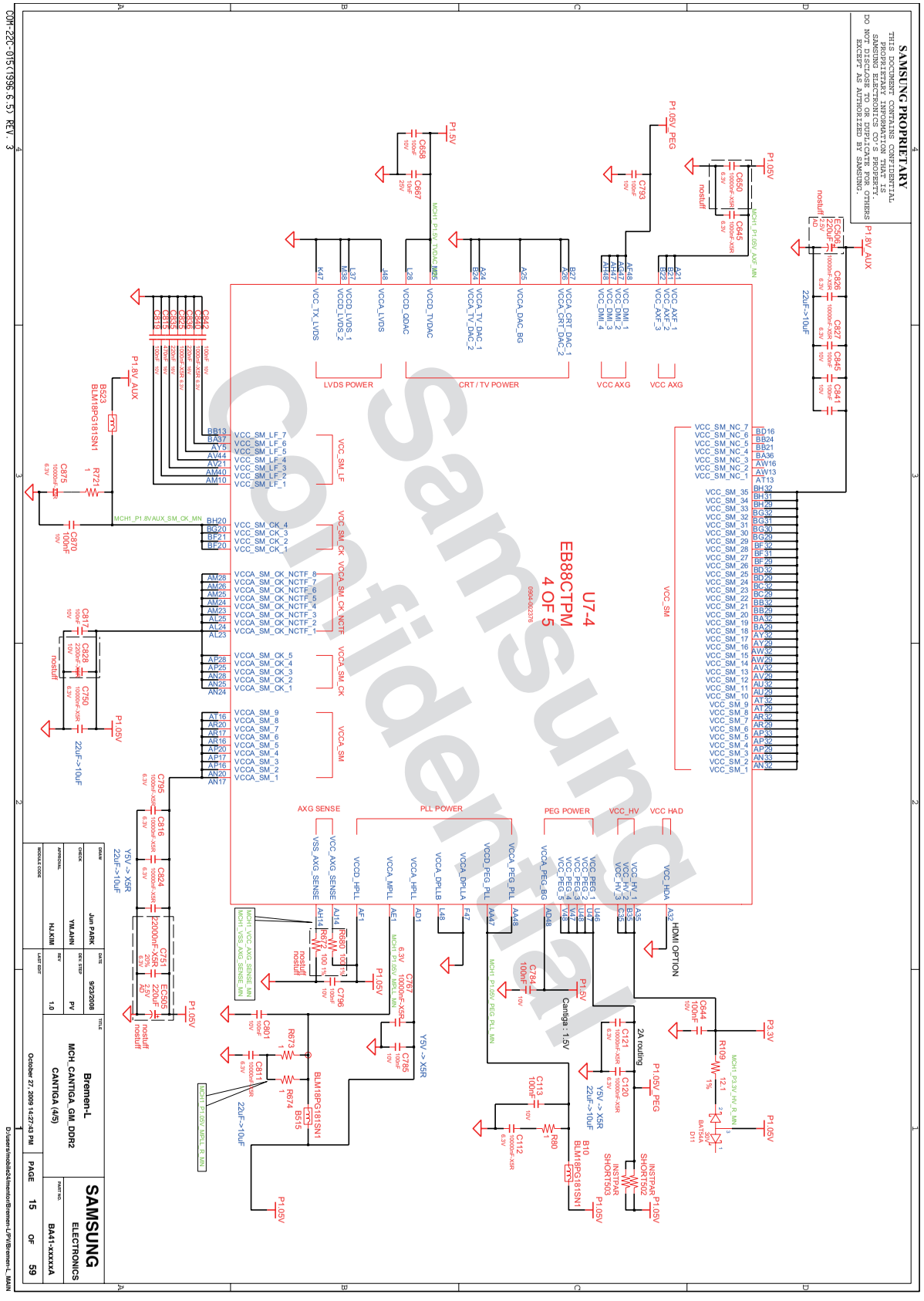

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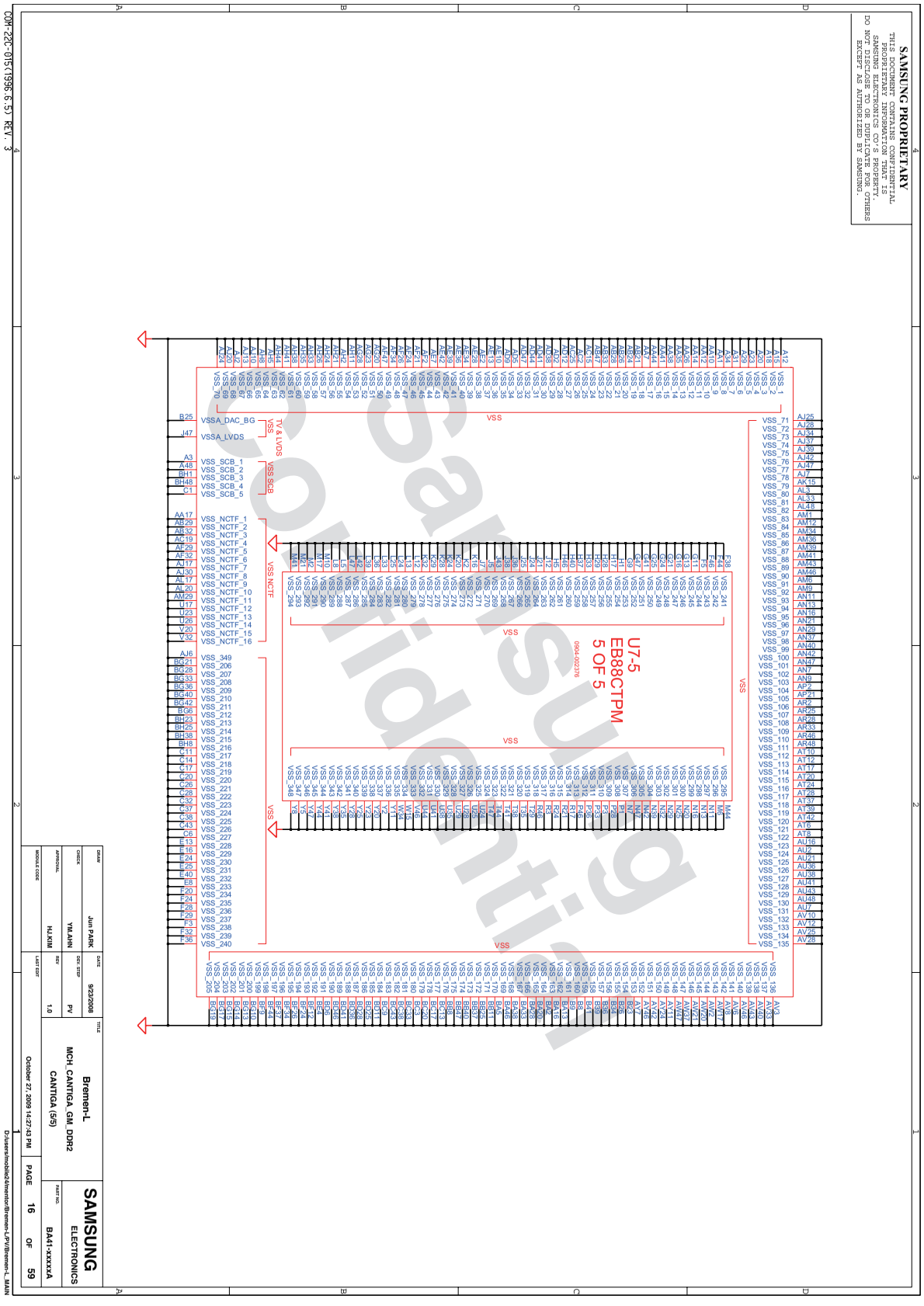

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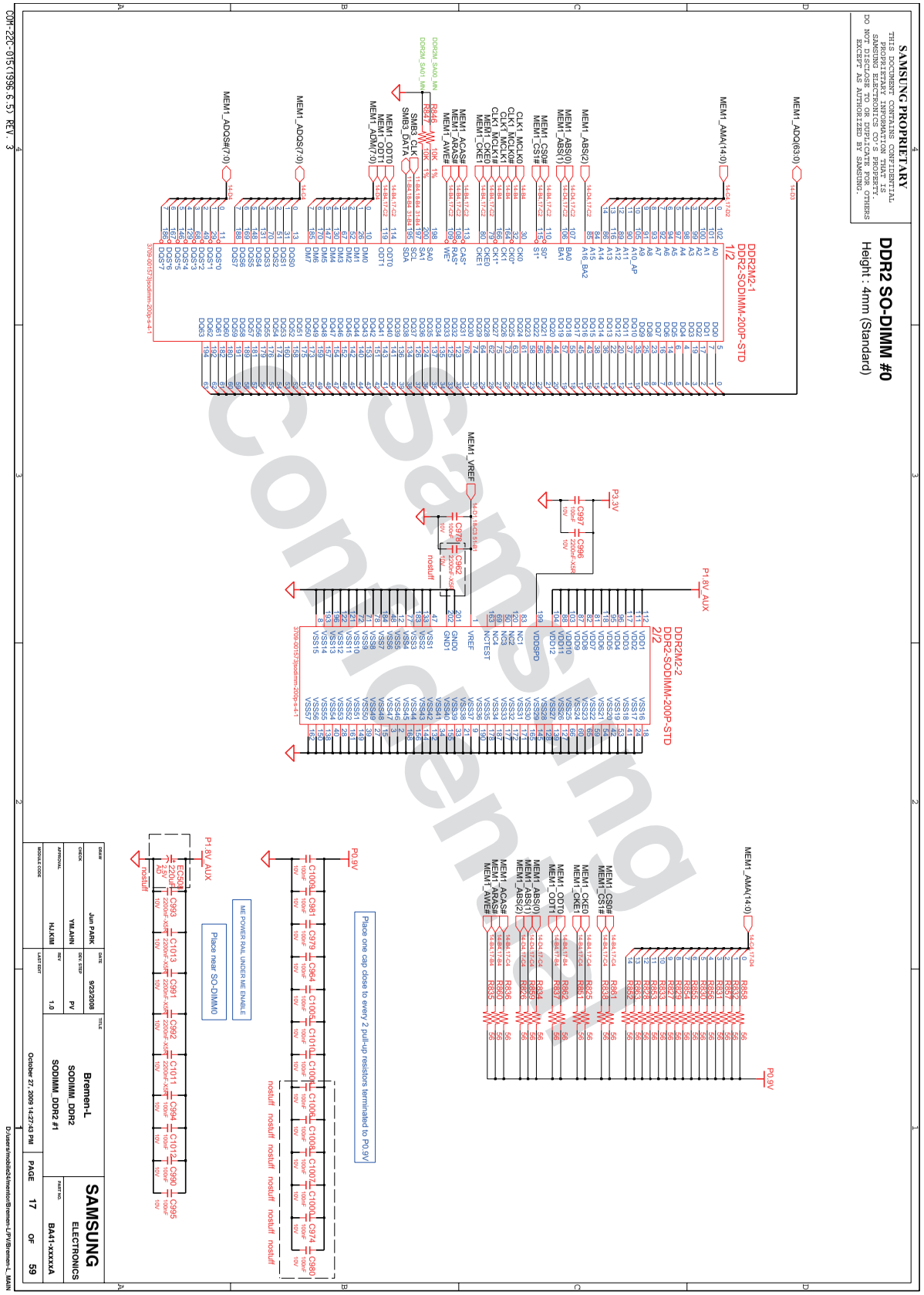
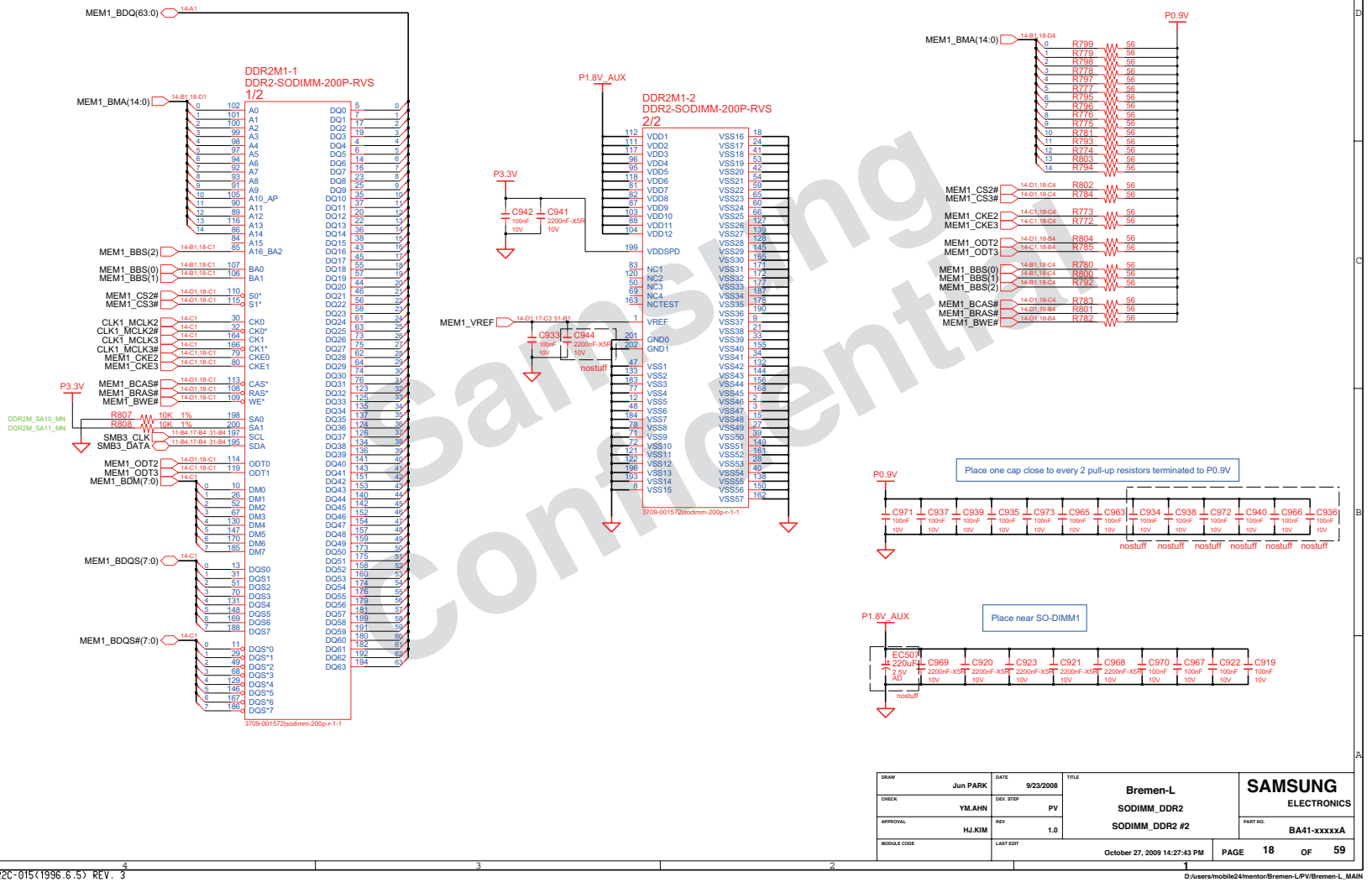


8. Block Diagram and Schematic

DDR2 SO-DIMM #1

Height : 4mm (Reverse)



DRAW: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV	SODIMM_DDR2	
APPROVAL: HJ.KIM	REV: 1.0	SODIMM_DDR2 #2	PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 18 OF 59	

COM-22C-015(1996.6.5) REV. 3

D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

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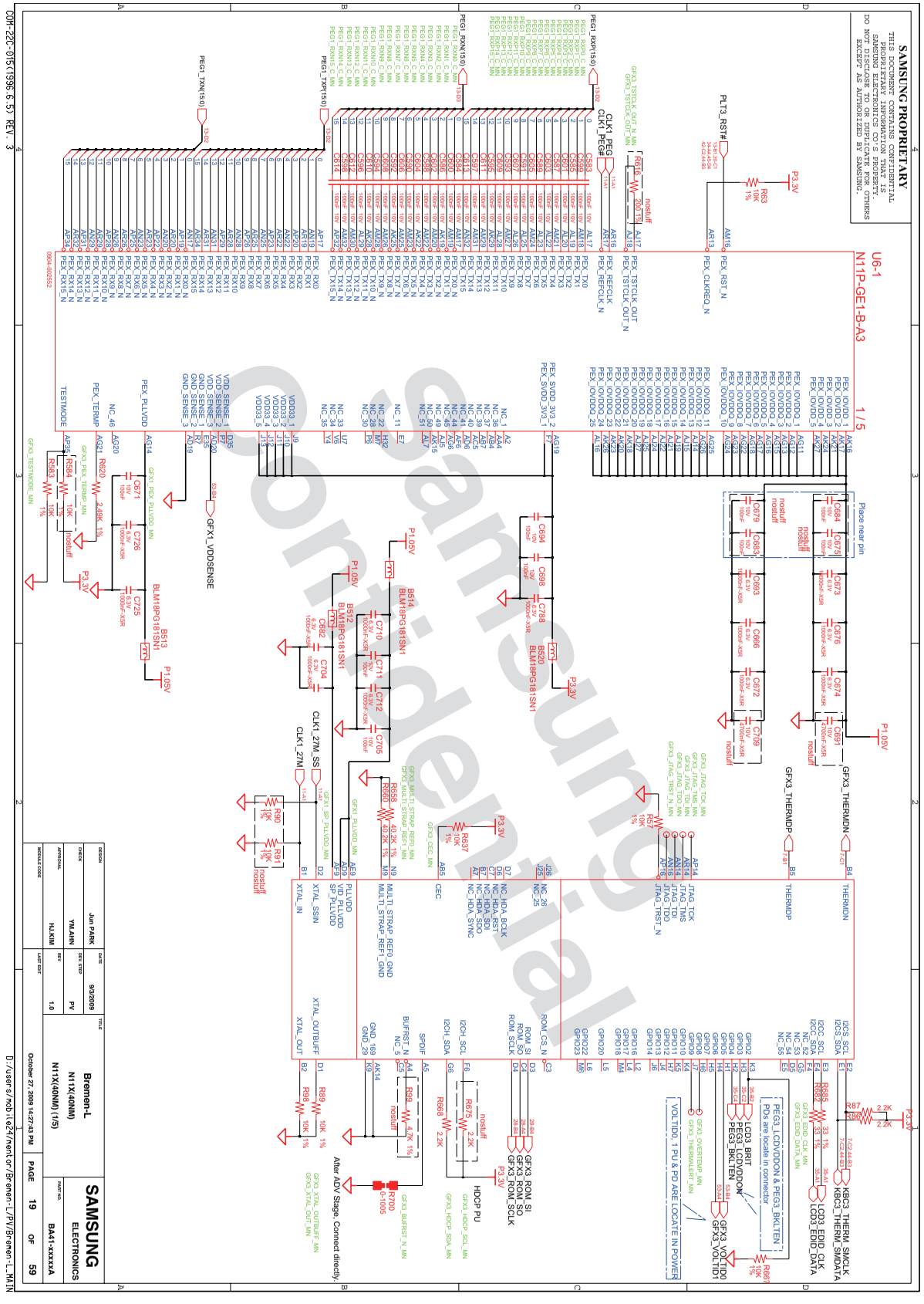

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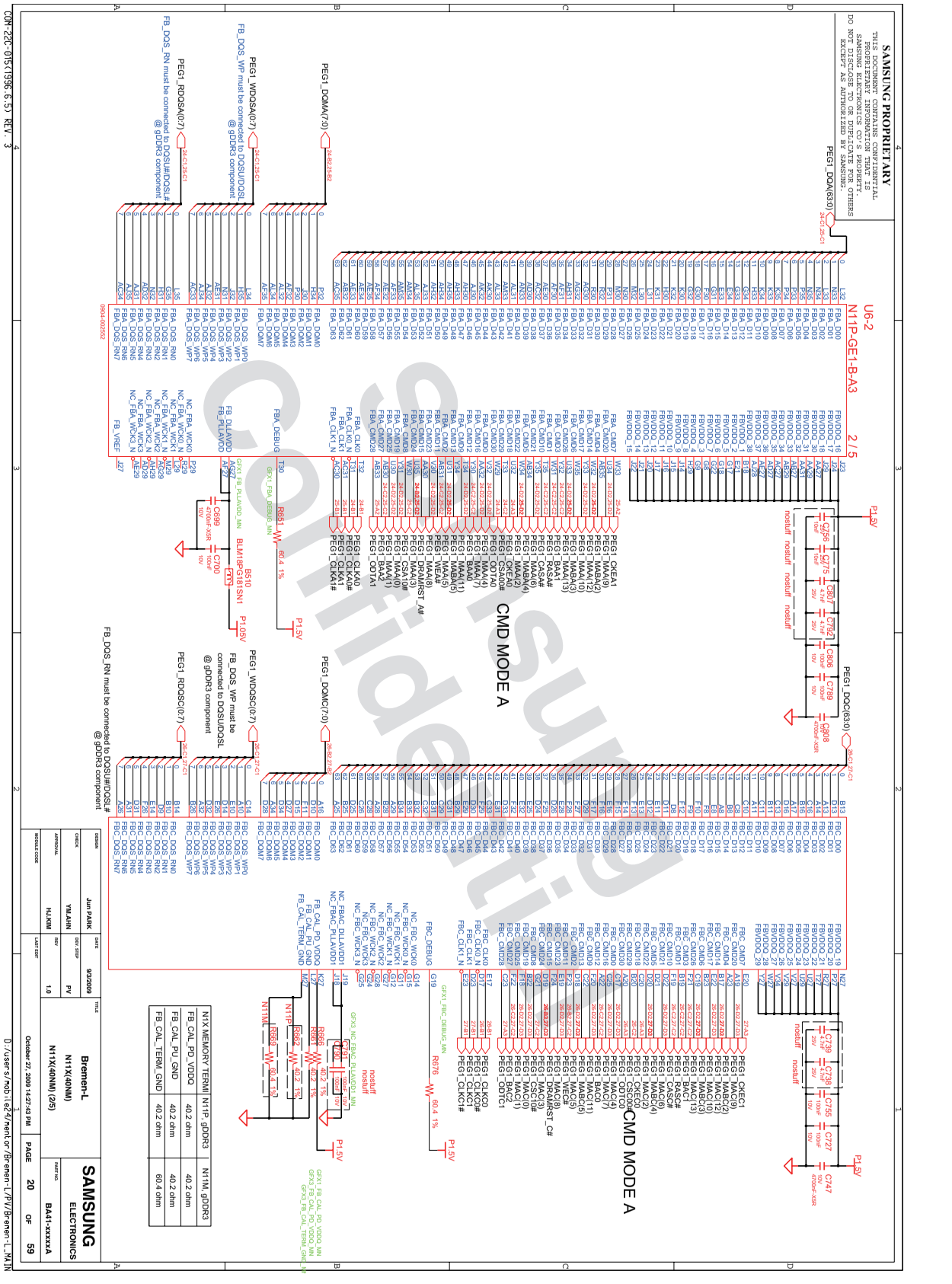

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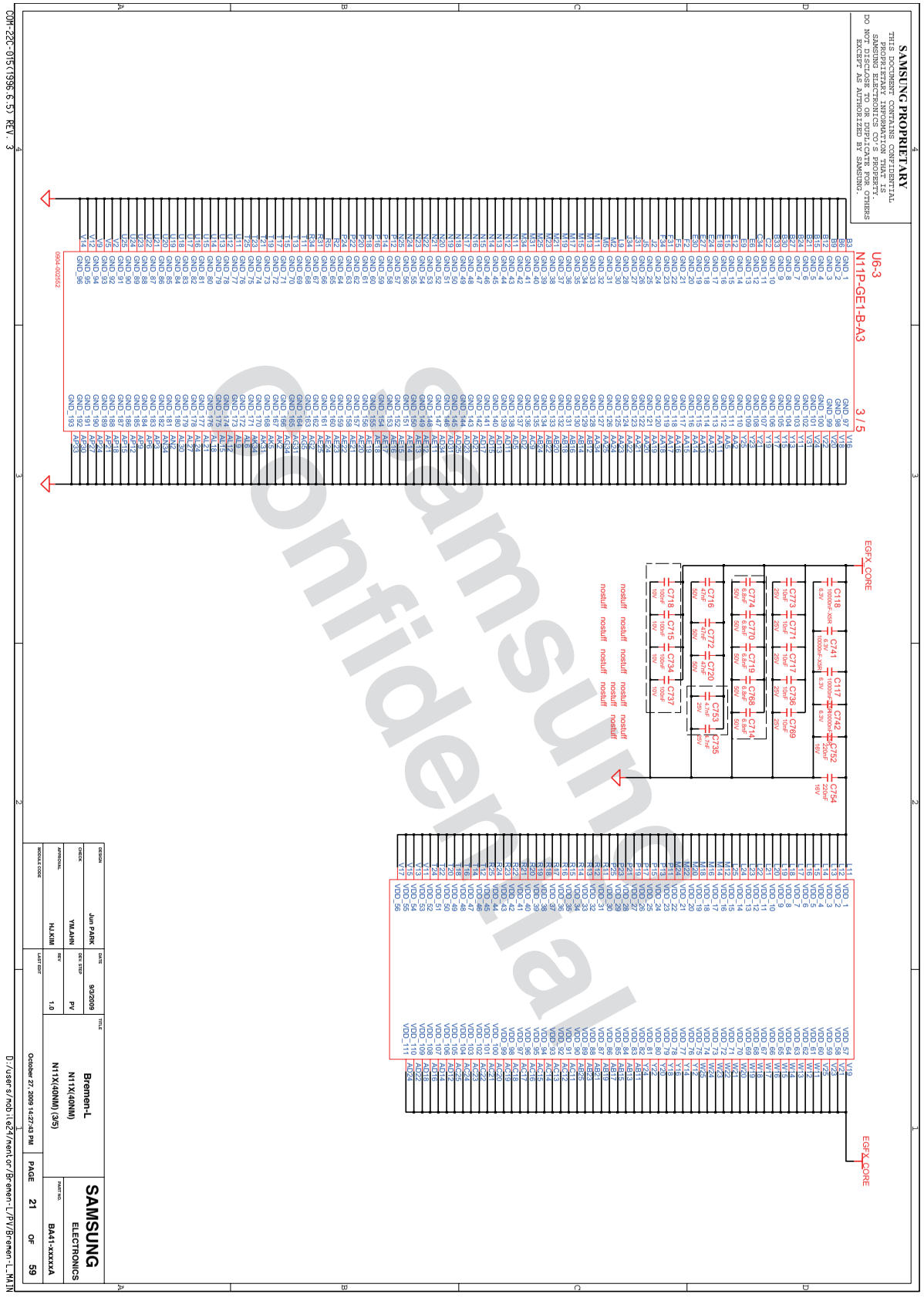

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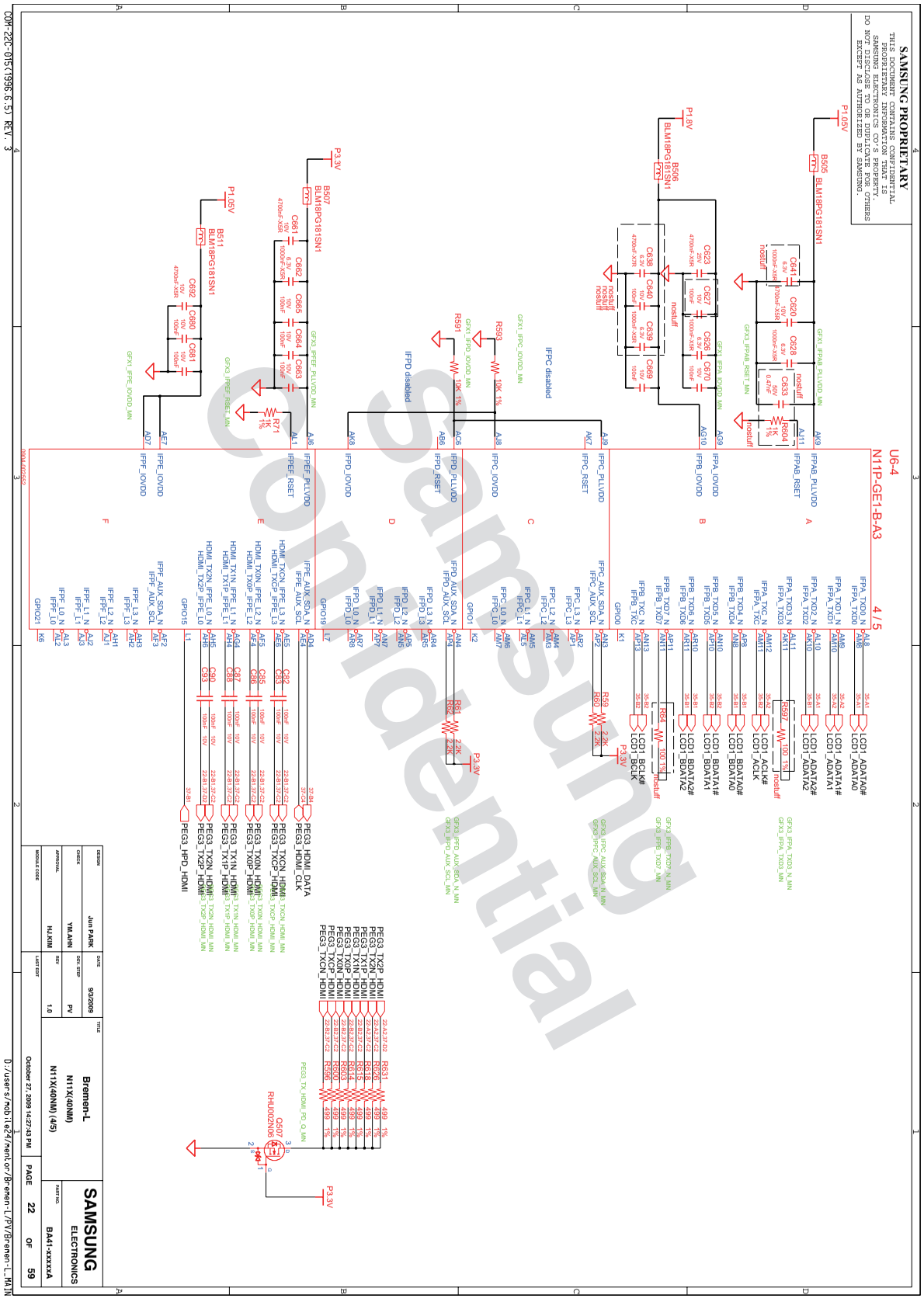

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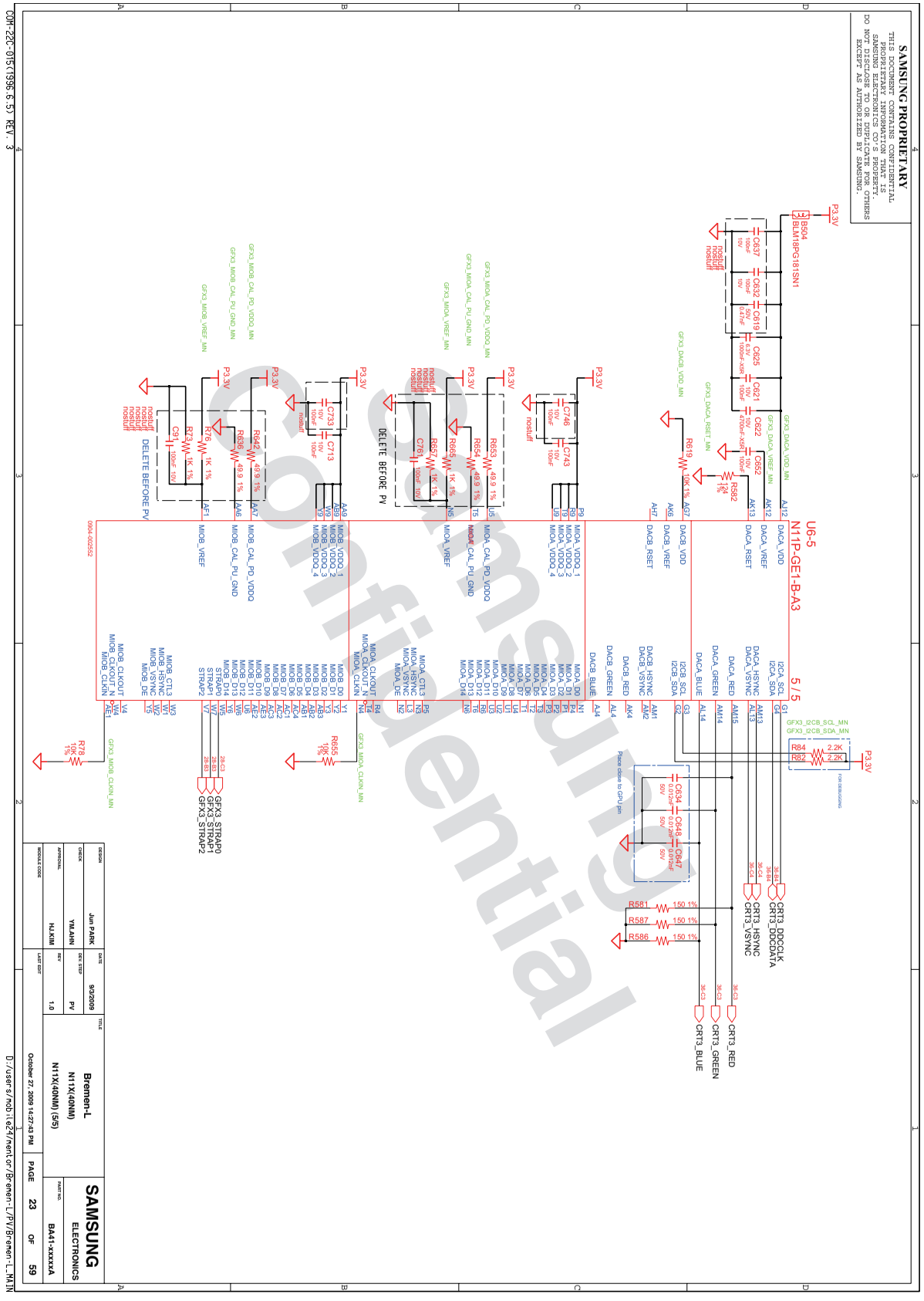

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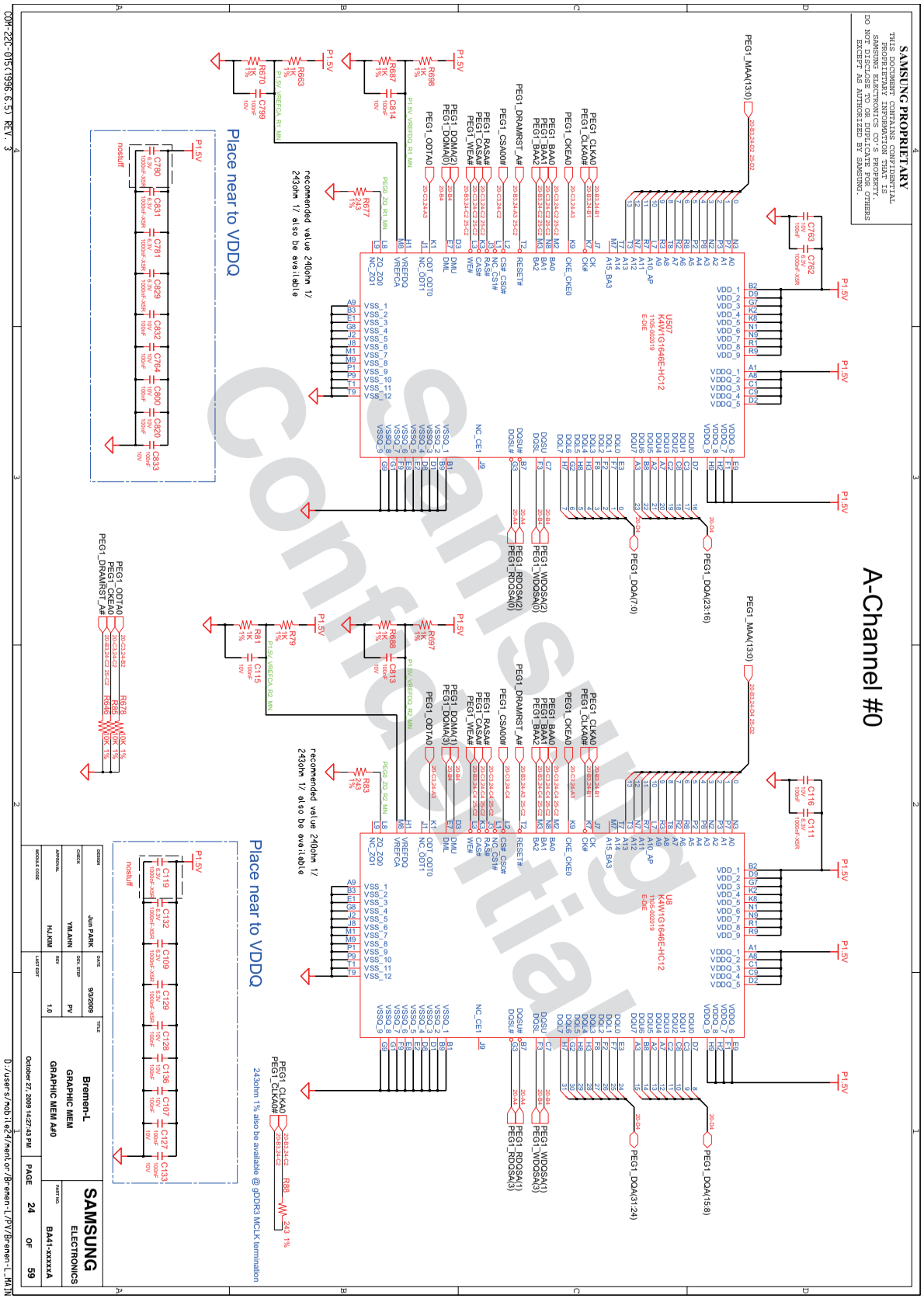

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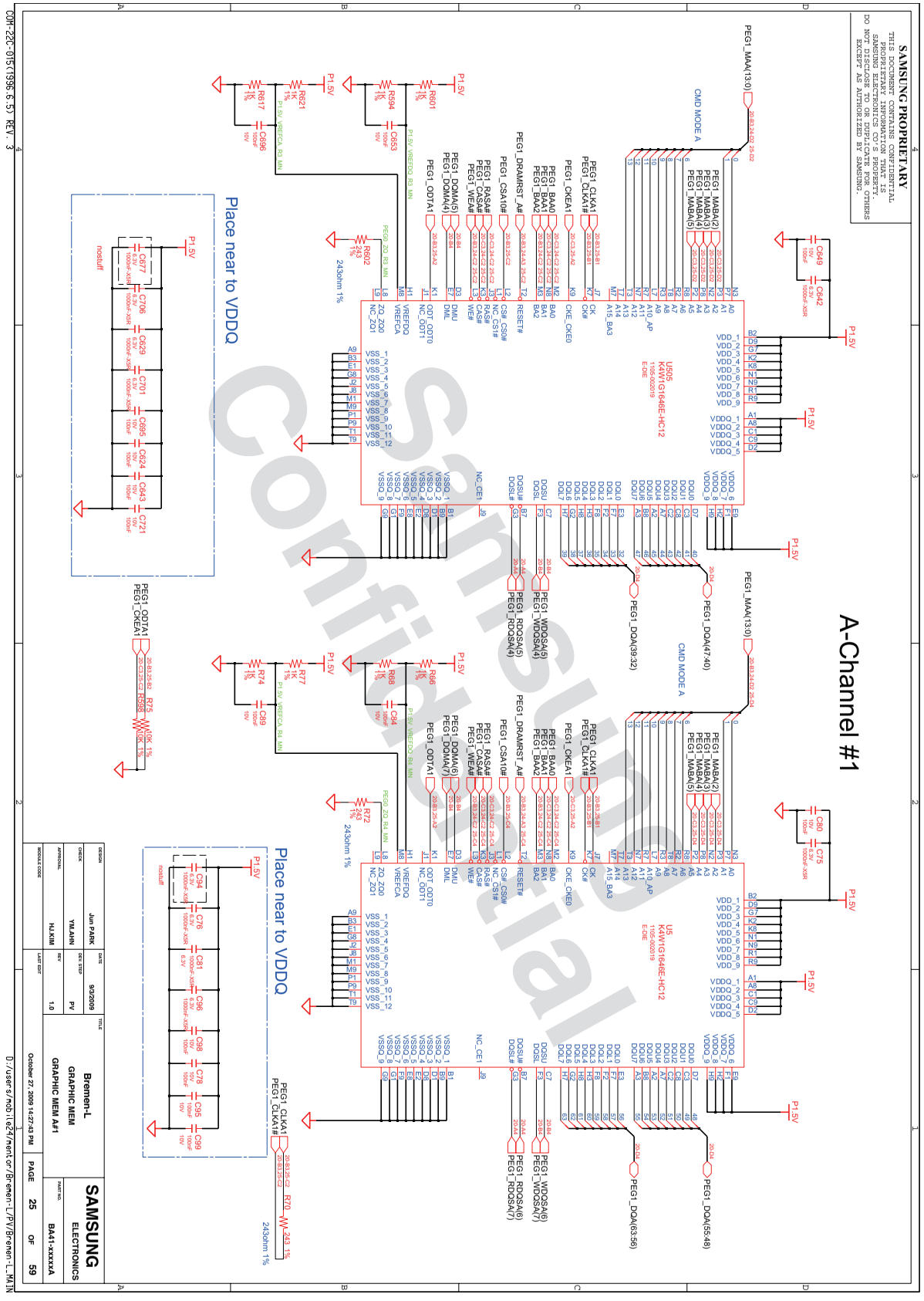

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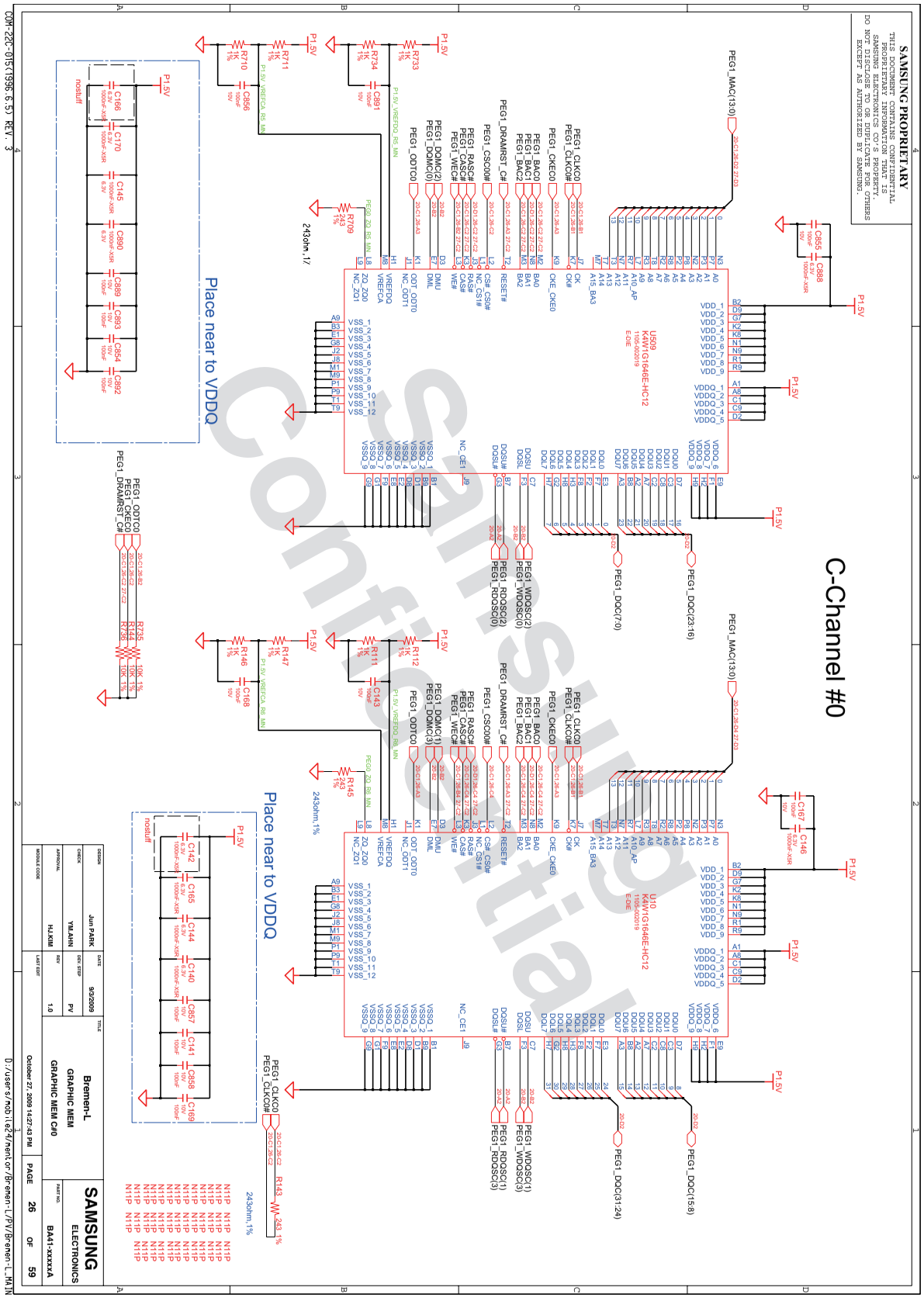

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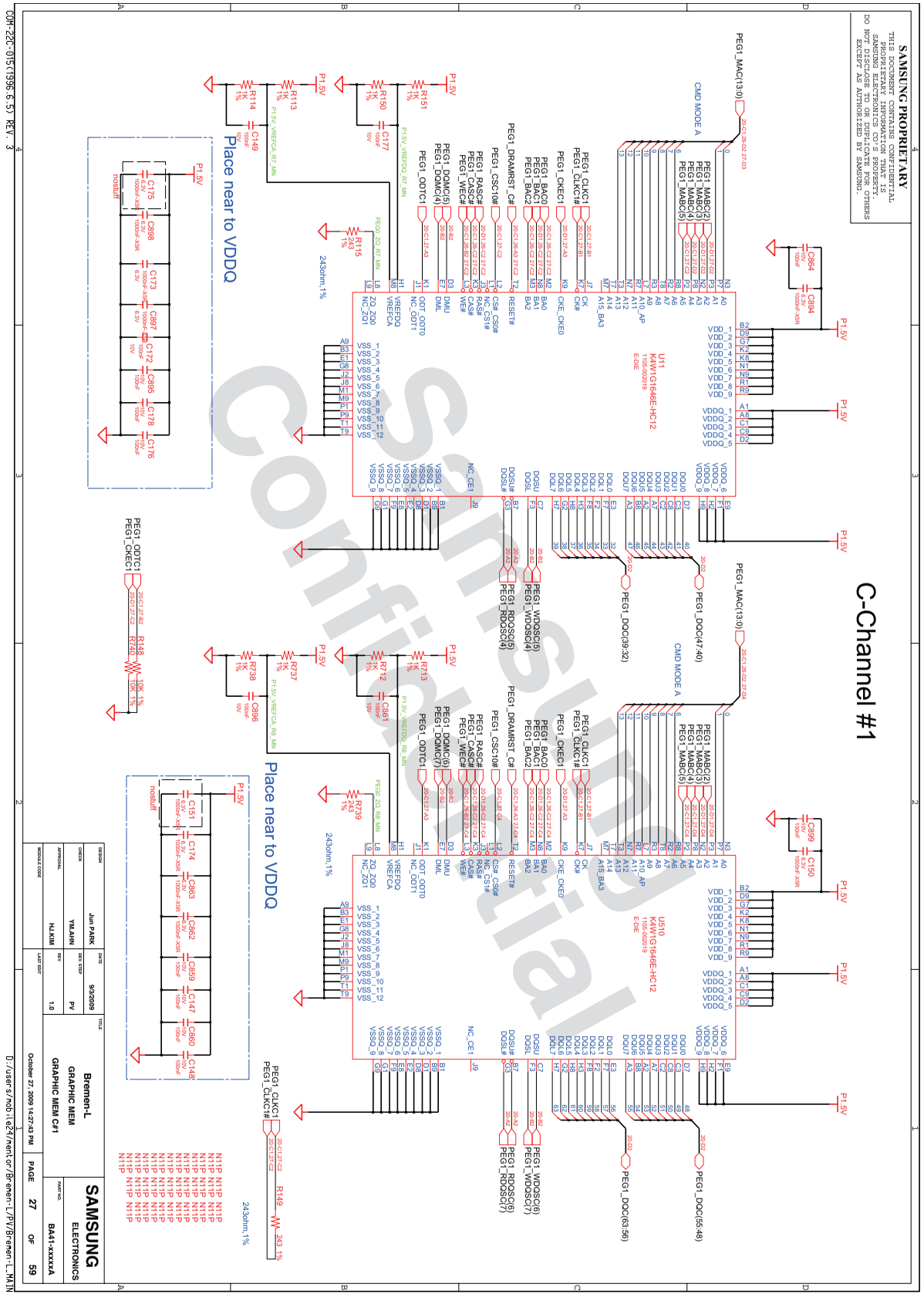

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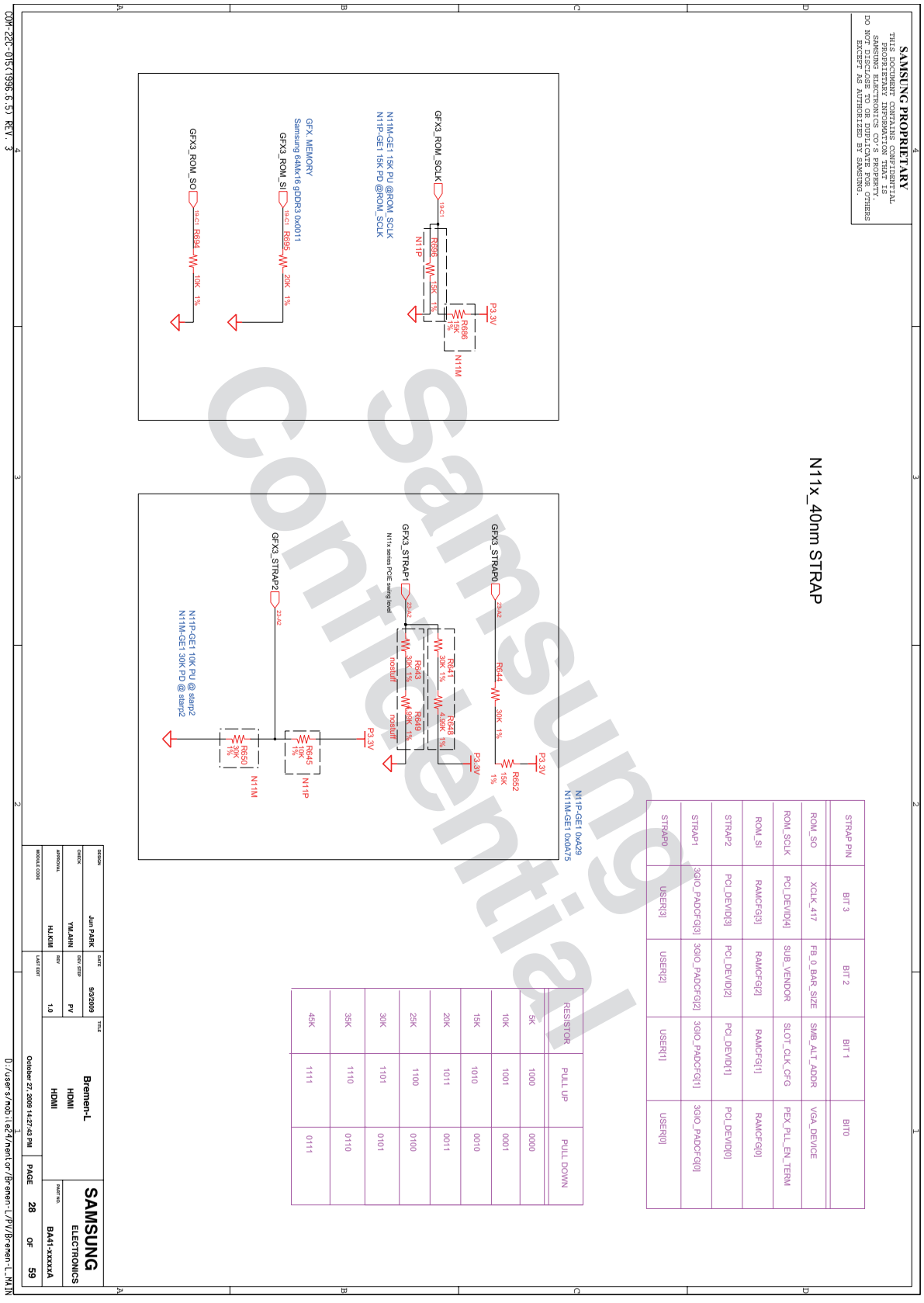
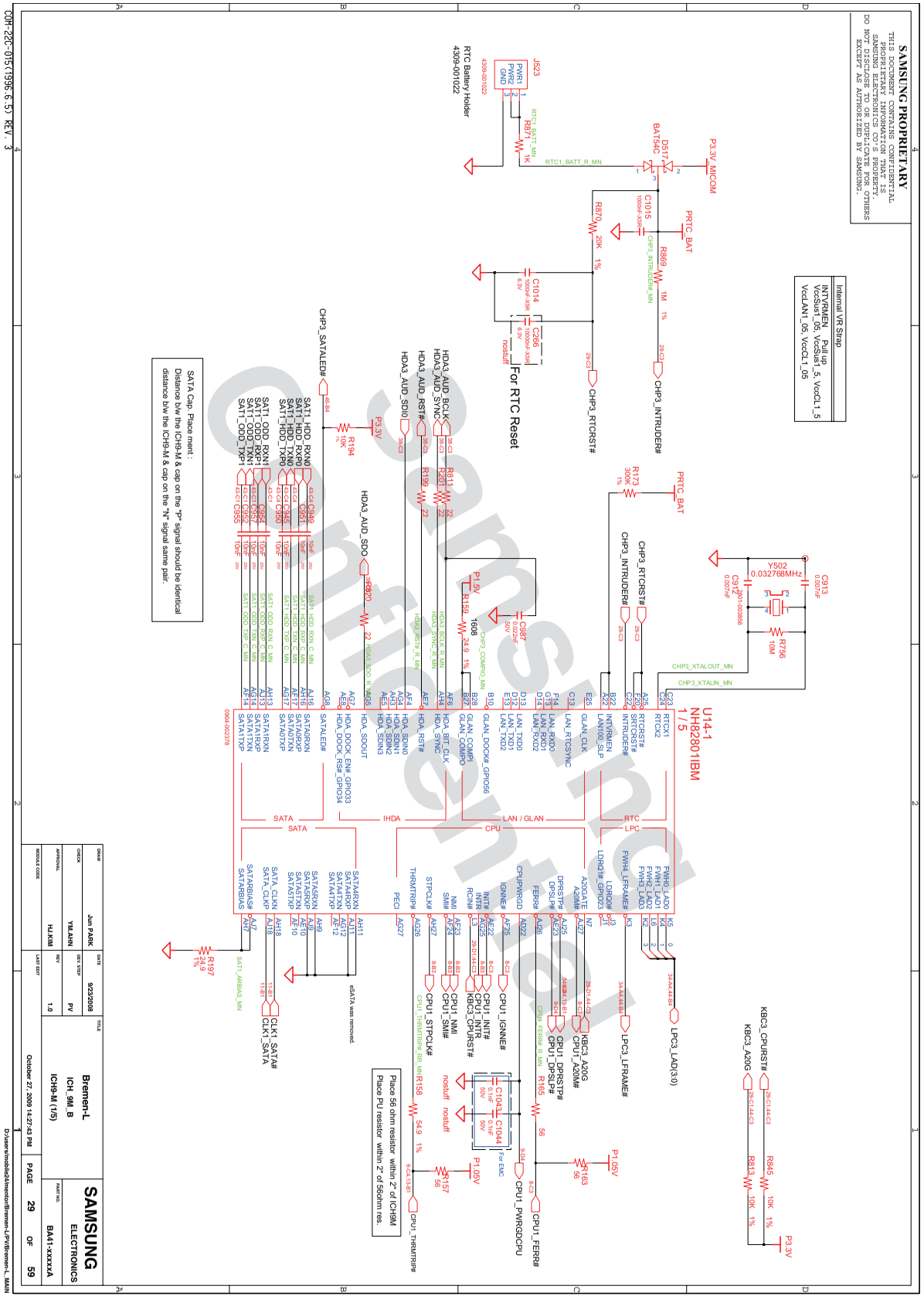


STRAP PIN	BIT 3	BIT 2	BIT 1	BIT0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

8. Block Diagram and Schematic



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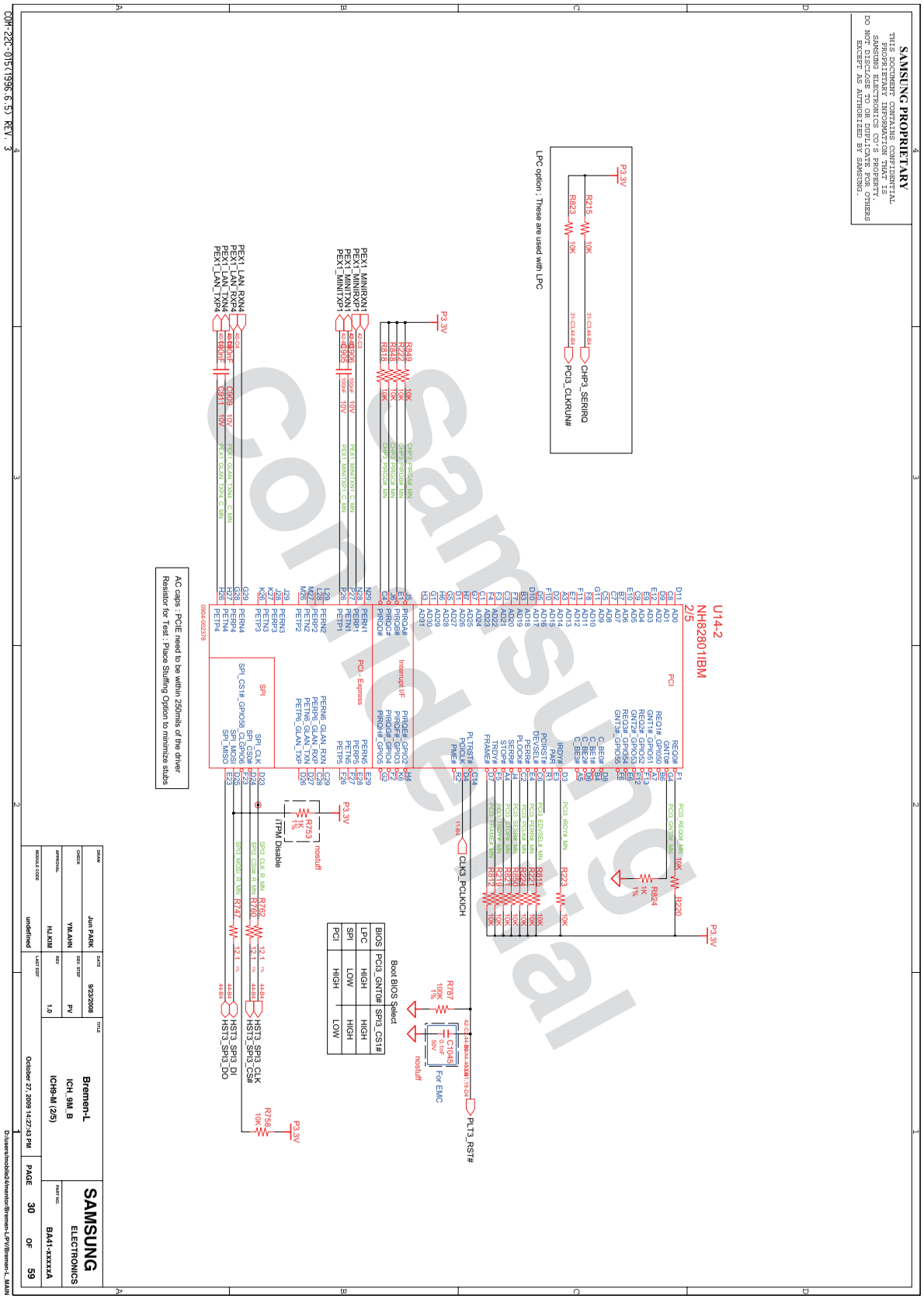

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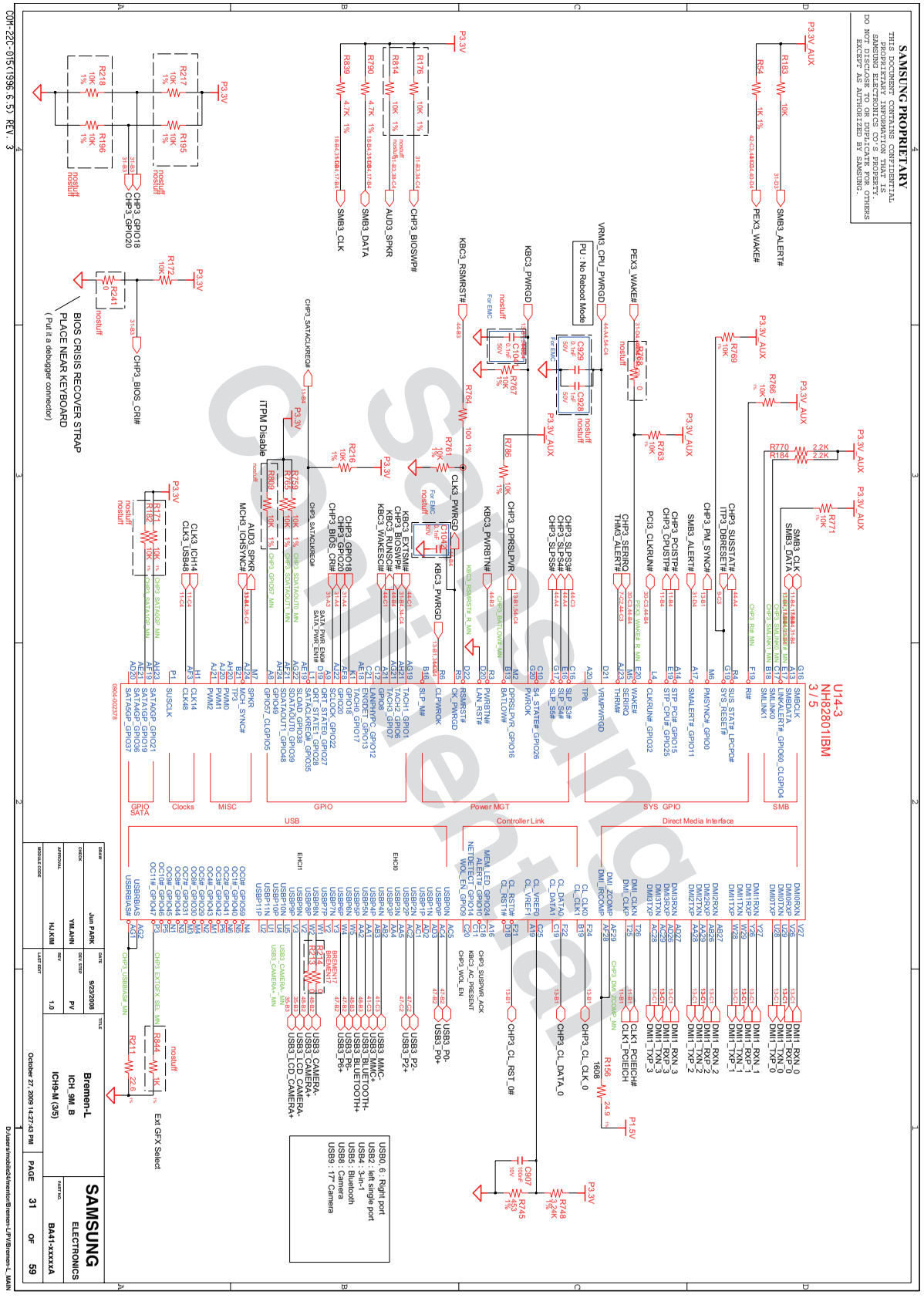

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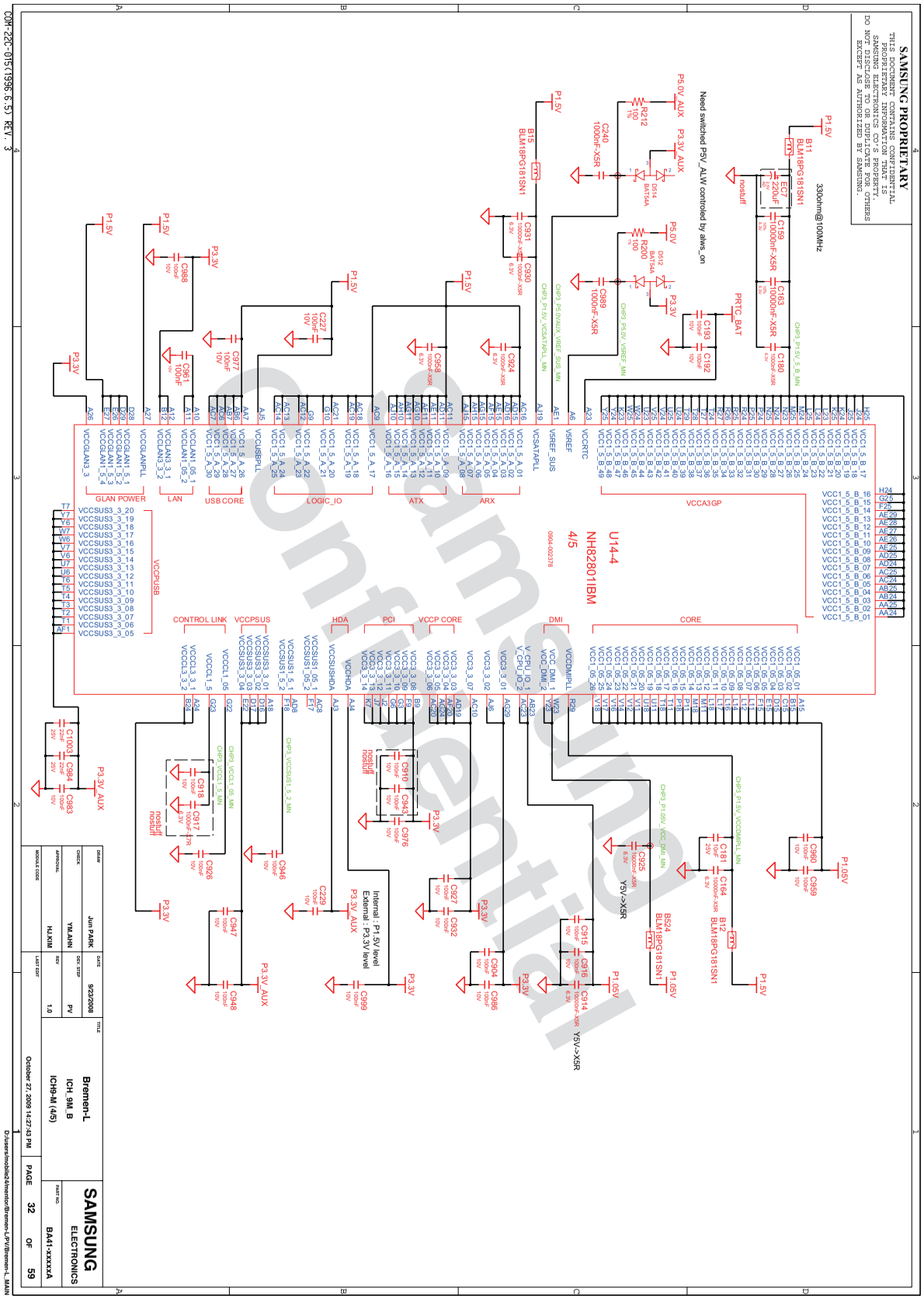

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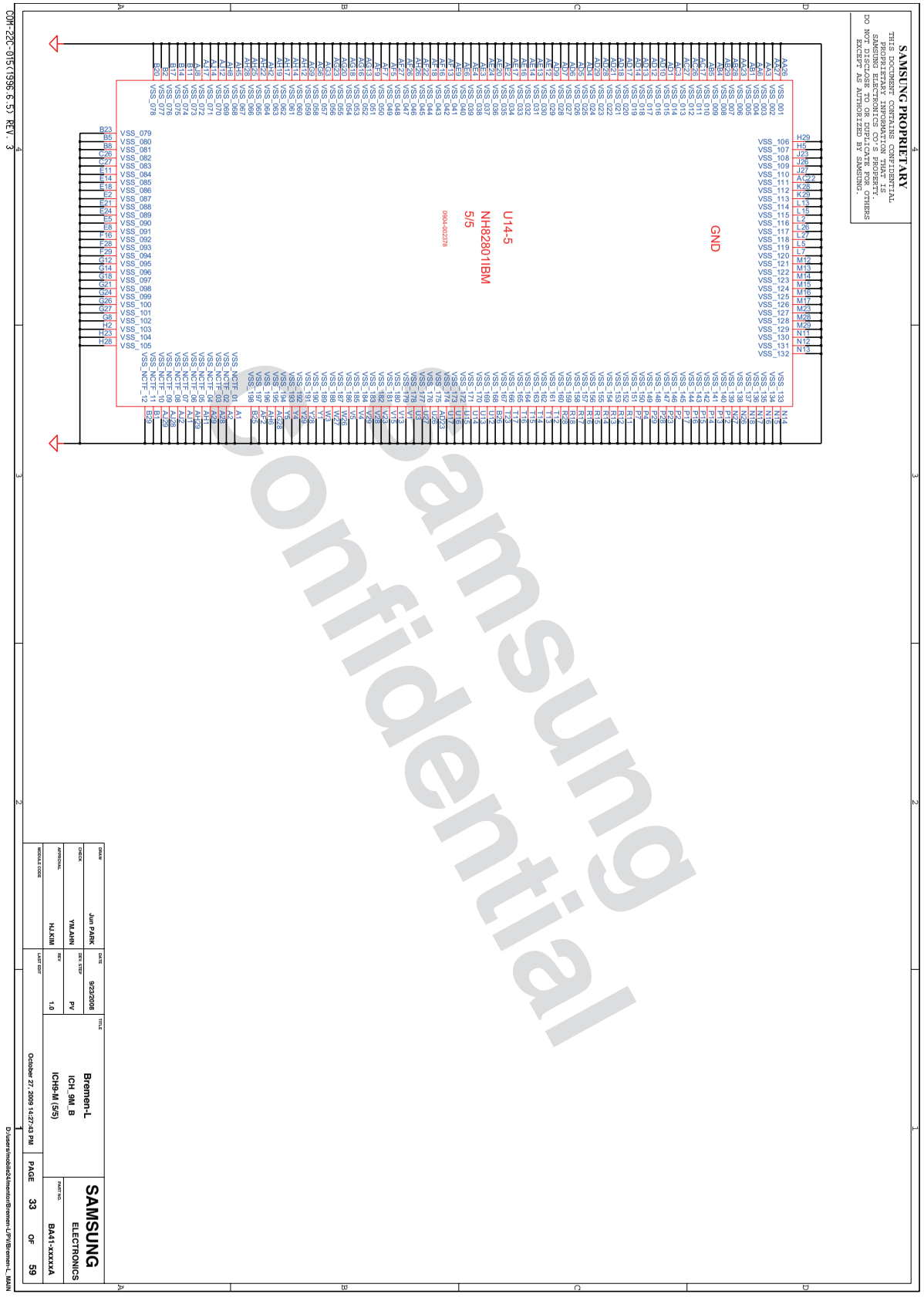
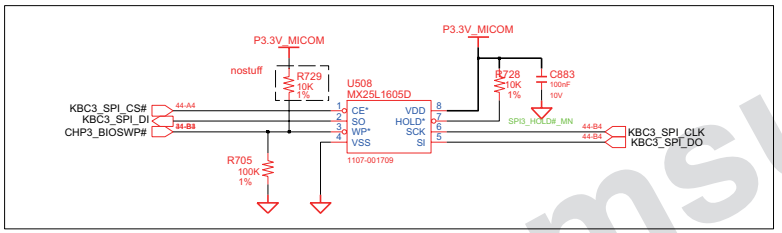


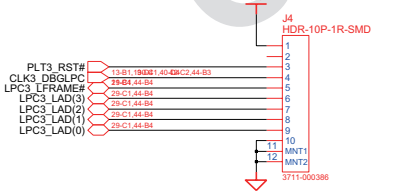
SPI_BIOS_ROM

16MBit



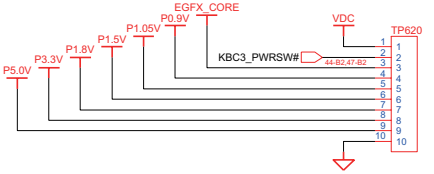
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUP CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY " PRESS F2 TO SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM GETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

80H DECODER CONNECTOR



80port will be removed in MP stage.

ICT FREE



DRAW	Jun PARK	DATE	9/23/2008
CHECK	YM.AHN	DEV. STEP	PV
APPROVAL	HJ.KIM	REV	1.0
MODULE CODE		LAST EDIT	October 27, 2009 14:27:43 PM

TITLE: Bremen-L / SPI_BIOS_ROM / SPI_BIOS_ROM

SAMSUNG ELECTRONICS

PART NO. BA41-xxxxxA

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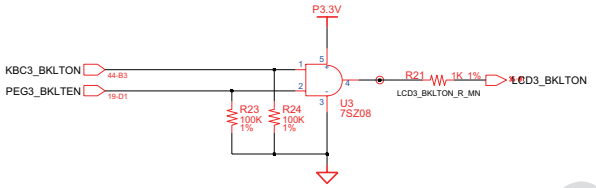
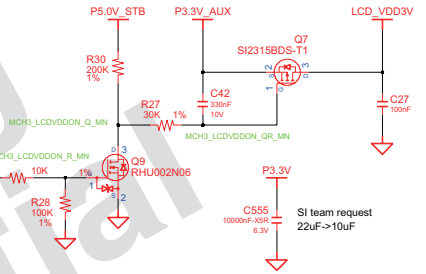
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

LVDS

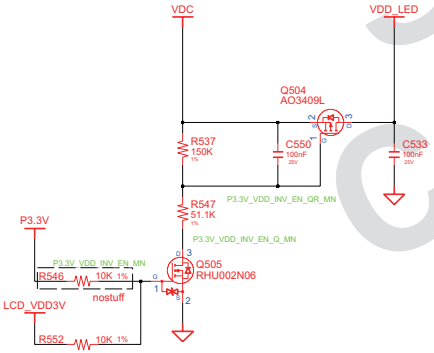
Backlight On



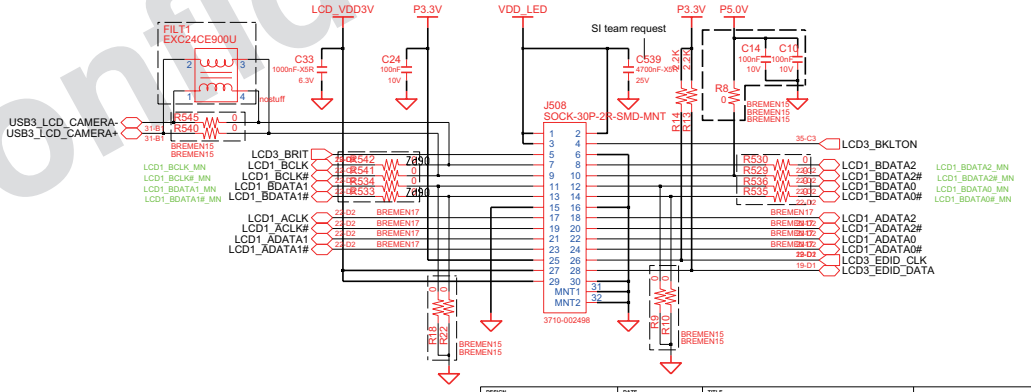
LCD Power EBL Purpose



LED Power



Camera + LCD Connector



DESIGN: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L / GRAPHICS_IF / LVDS	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 35 OF 59	

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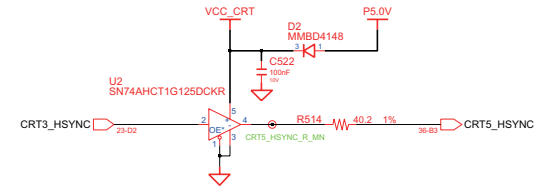
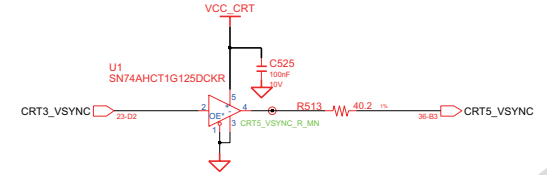
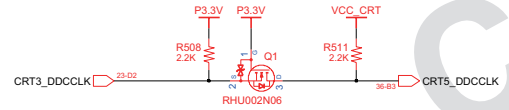
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

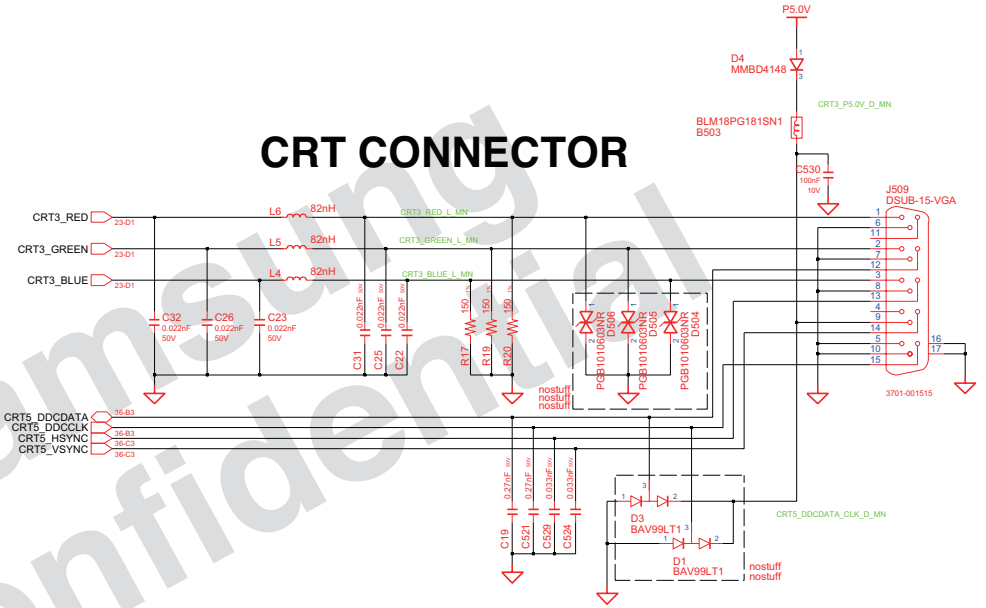
CRT







CRT CONNECTOR



Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DESIGN: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV	GRAPHICS_IF	
APPROVAL: HJ.KIM	REV: 1.0	CRT	PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 36 OF 59	

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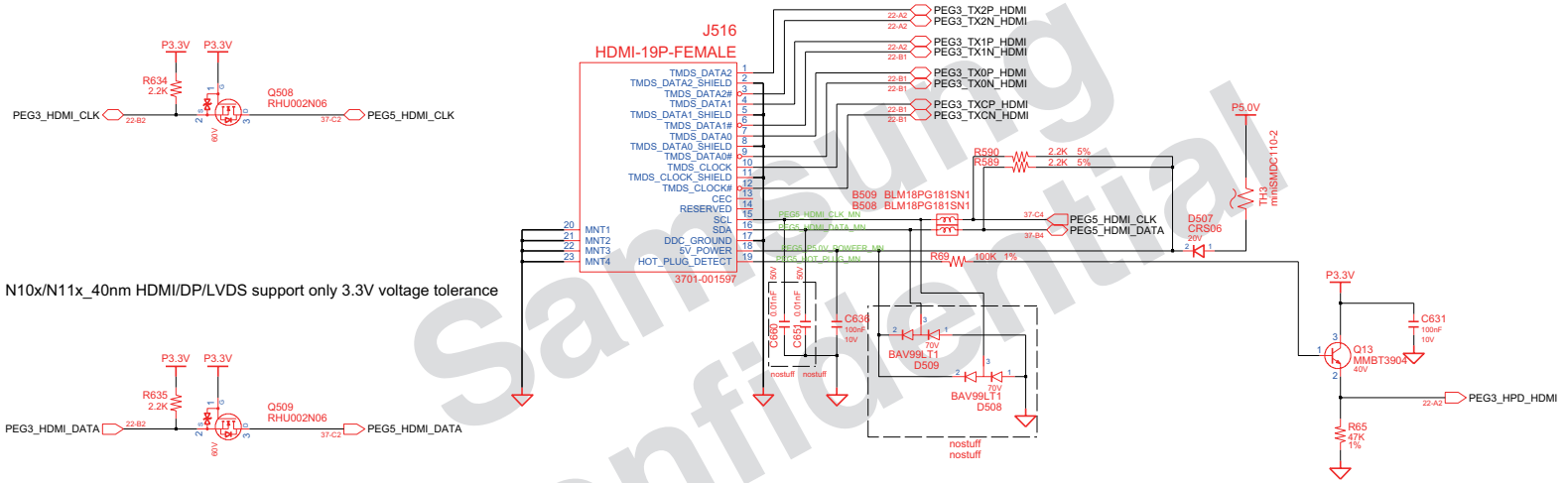
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

HDMI

FOR HDMI VERIFICATION TEST

N10x/N11x_40nm HDMI/DP/LVDS support only 3.3V voltage tolerance

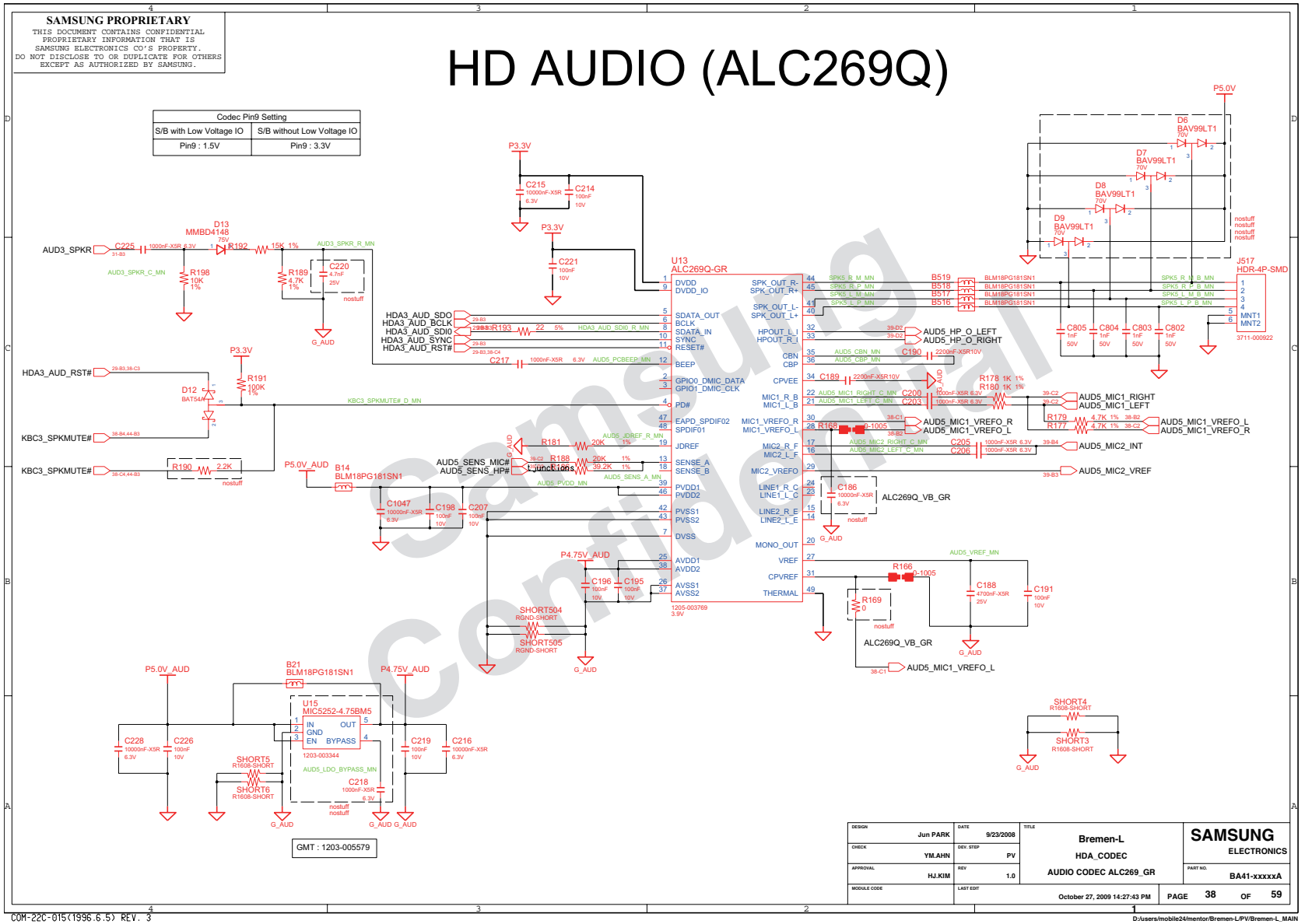


DESIGN: Jun PARK	DATE: 8/14/2009	TITLE: Bremen-L / HDMI / HDMI Connector	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 37 OF 59	

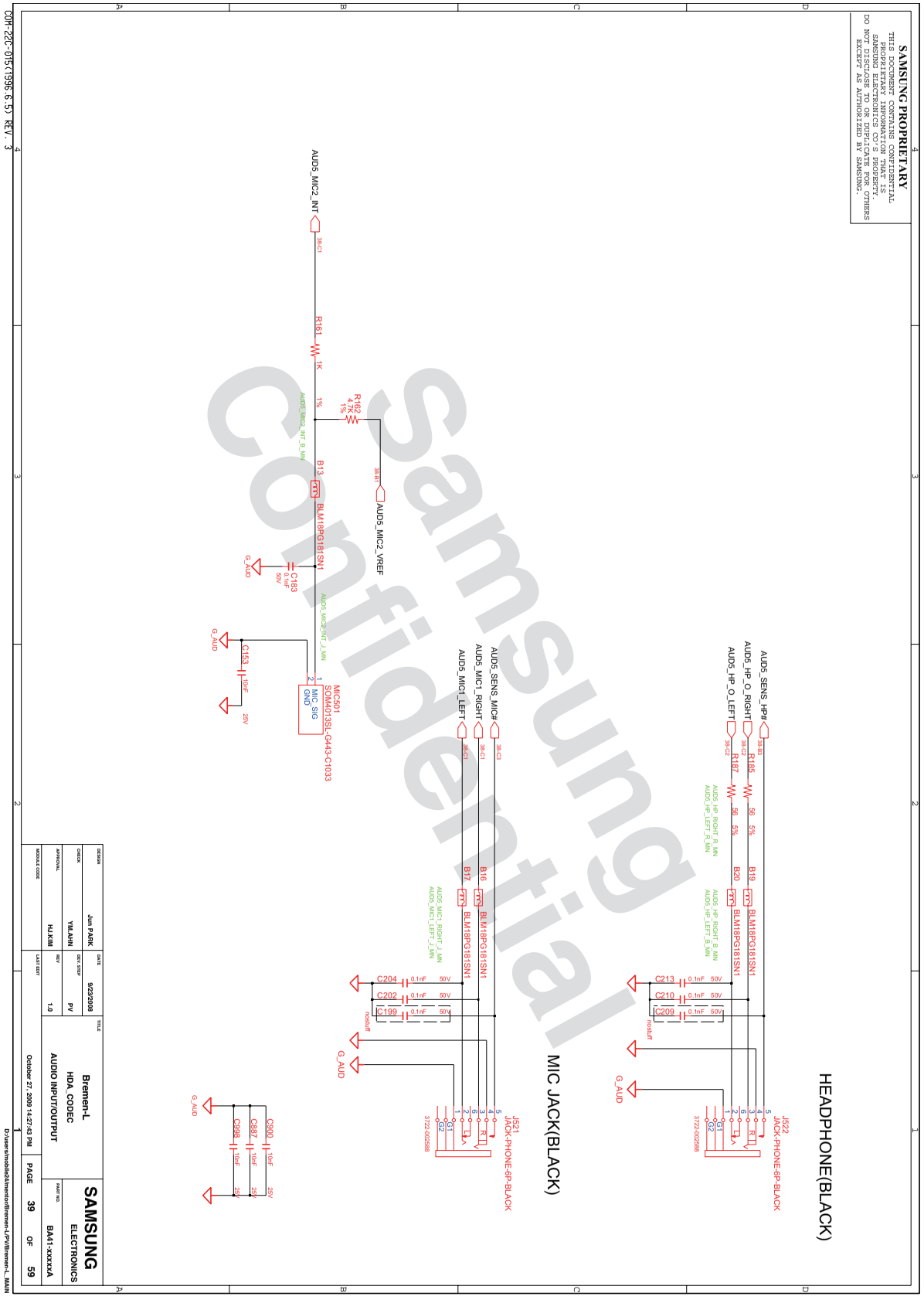
COM-22C-015(1996.6.5) REV. 3

D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

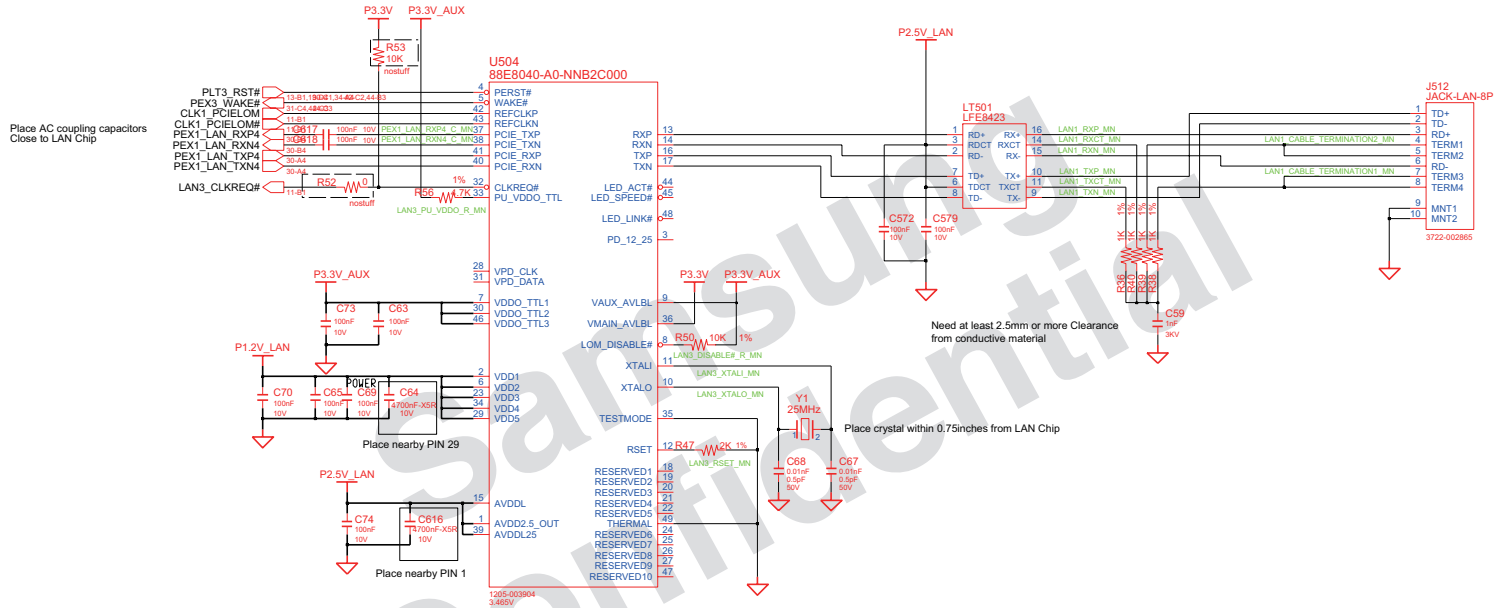
8. Block Diagram and Schematic



8. Block Diagram and Schematic



LAN Controller (88E8040)



DESIGN: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L LAN LAN_MARVELL_8057	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM		PAGE 40 OF 59

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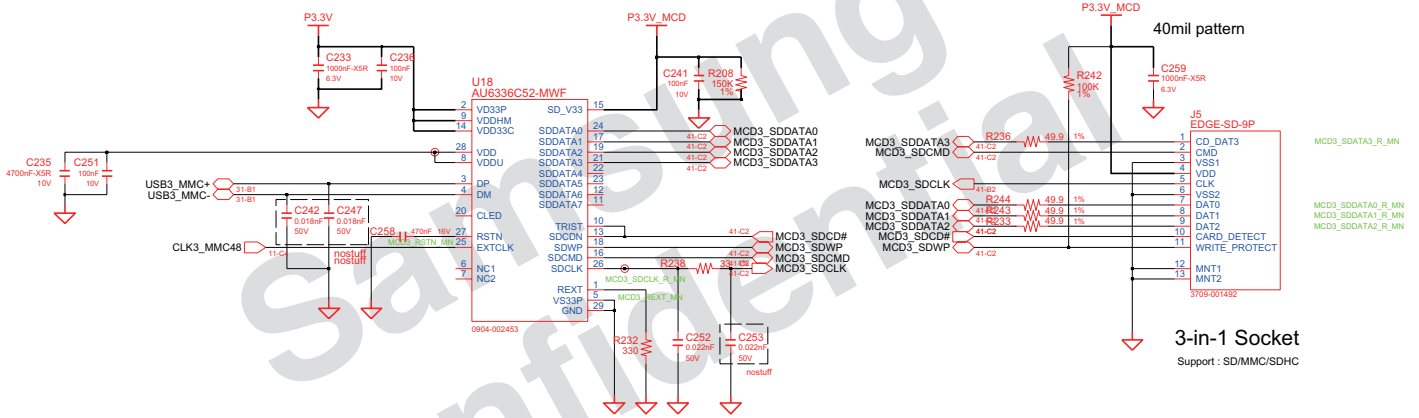
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

3 IN 1 CARD (AU6336)



DESIGN: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L MULTICARD 2 IN 1 CARD	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 41 OF 59	

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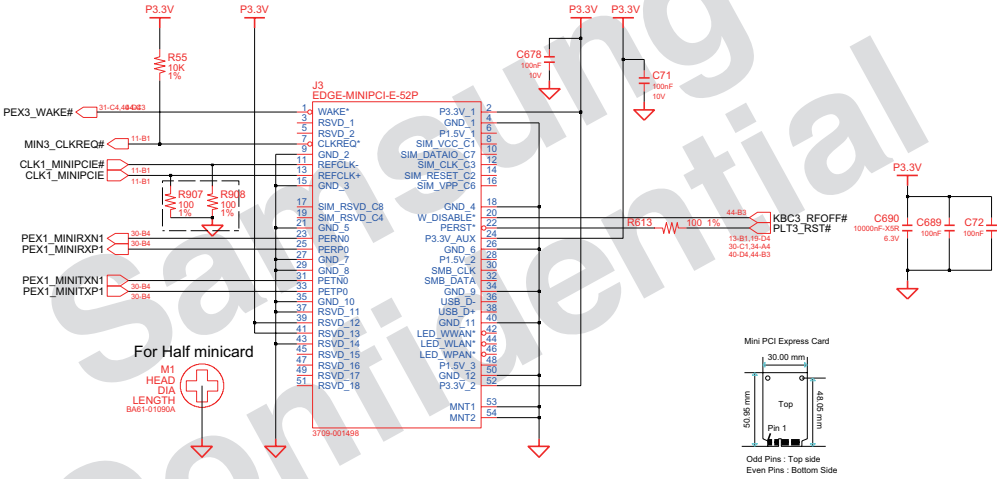
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

Wireless LAN

WLAN, 4mm



DESIGN: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV	MINI_PCIE_CONN	
APPROVAL: HJ.KIM	REV: 1.0	WLAN & HSDPA & SIM CARD	PART NO.: BA41-xxxxxA
MODULE CODE	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 42 OF 59	

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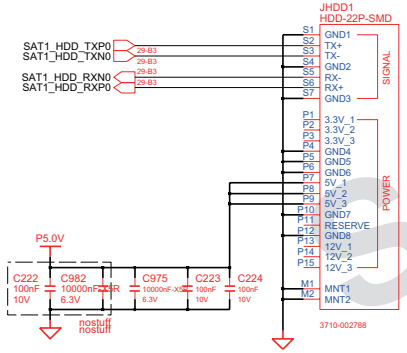
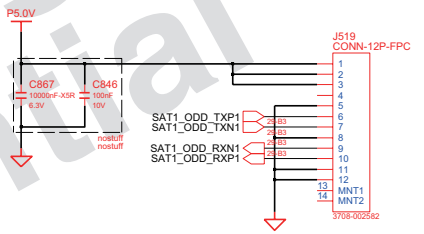
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

SATA I/F CONN

SATA HDD CONN



MAIN TO SUB SATA ODD CONN



DESIGN: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV	SATA_DEVICES	
APPROVAL: HJ.KIM	REV: 1.0	HDD & ODD SUB CONNECTOR	PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 43 OF 59	

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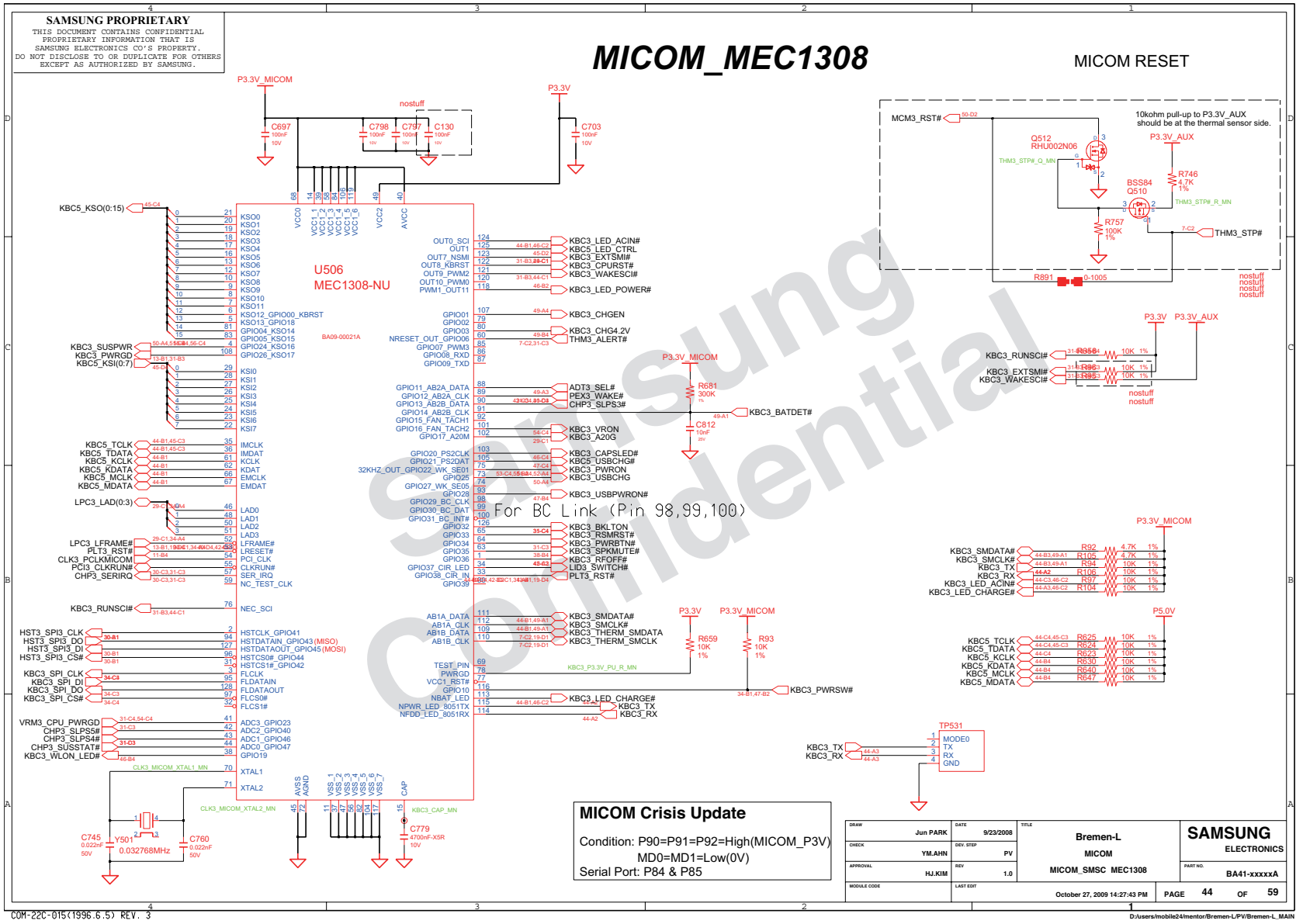
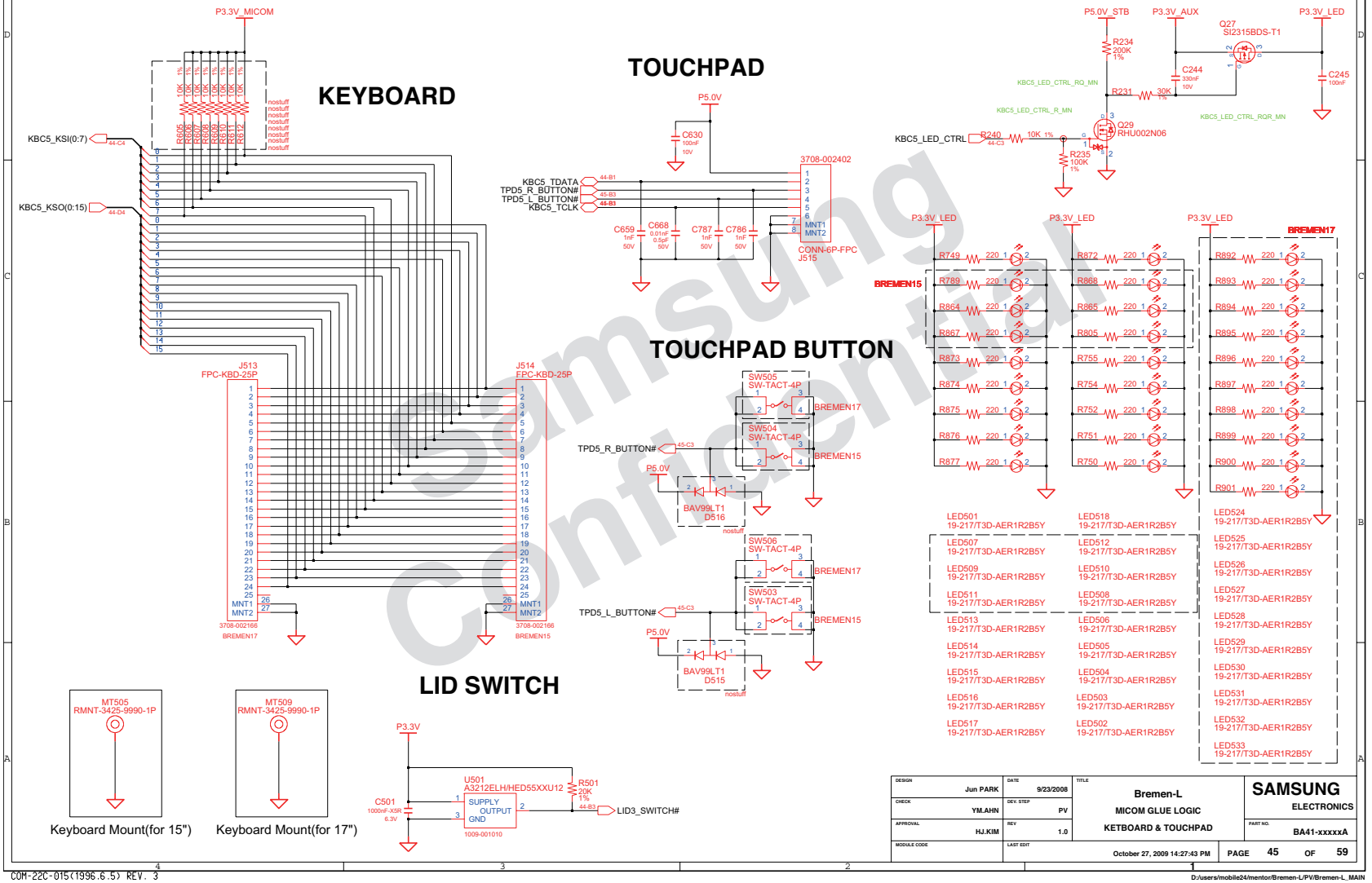
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

8. Block Diagram and Schematic



Micom Glue Logic



DESIGN: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L MICOM GLUE LOGIC KETBOARD & TOUCHPAD	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 45 OF 59	

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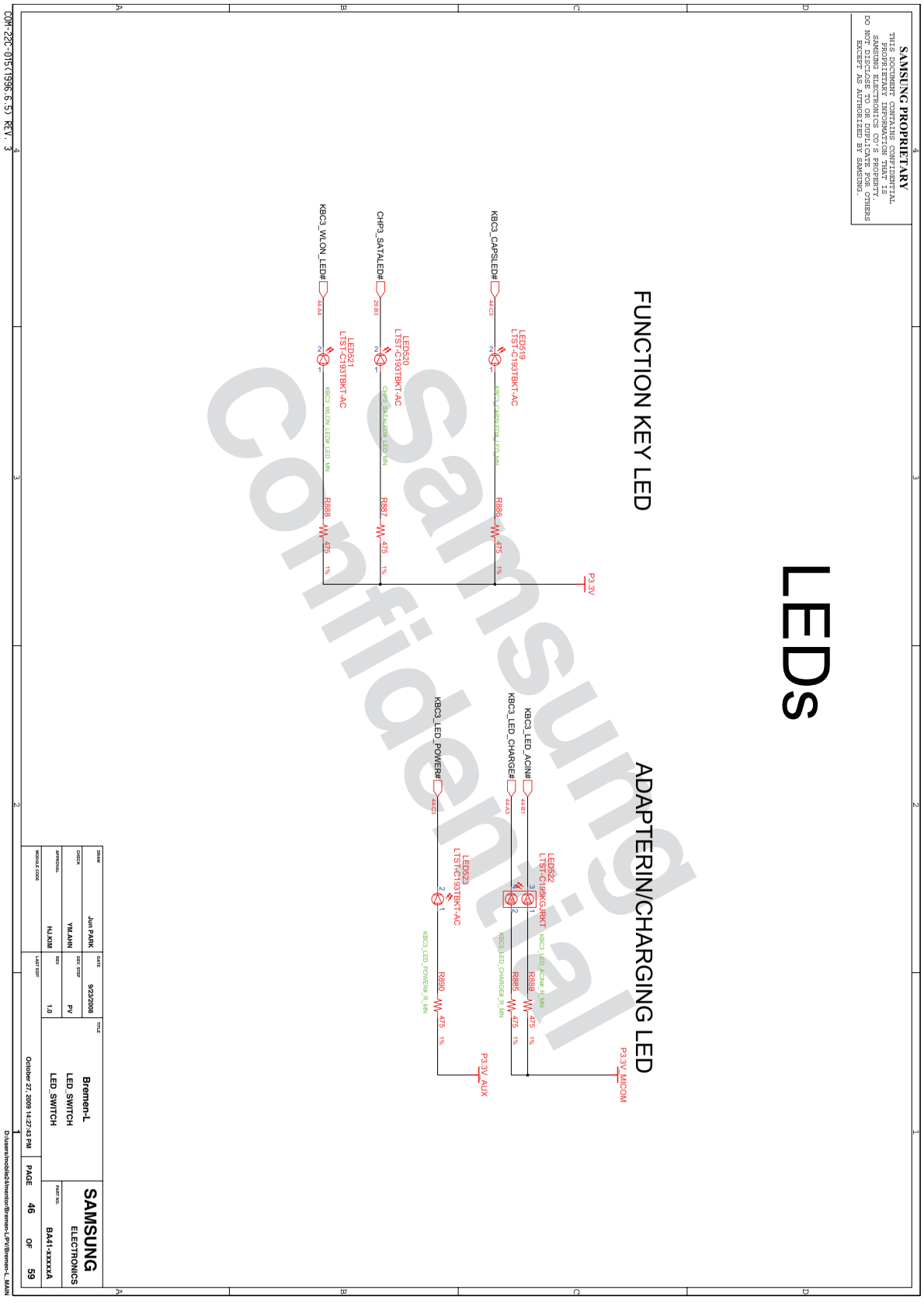
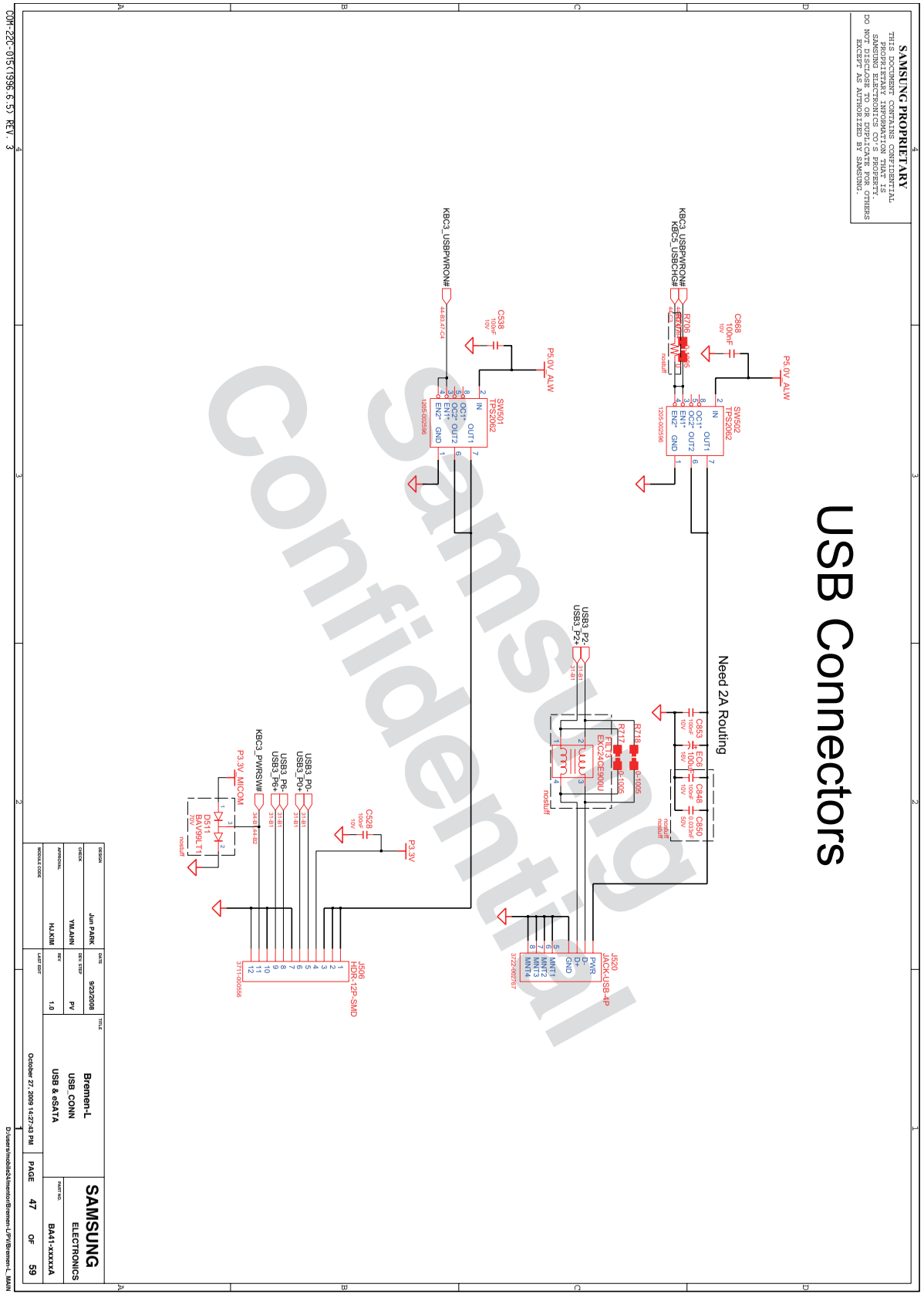
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

8. Block Diagram and Schematic

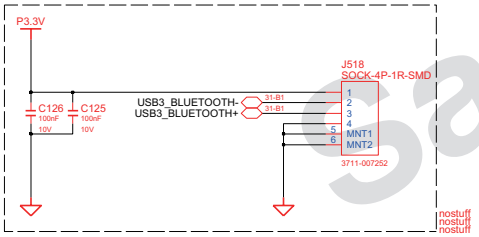


8. Block Diagram and Schematic

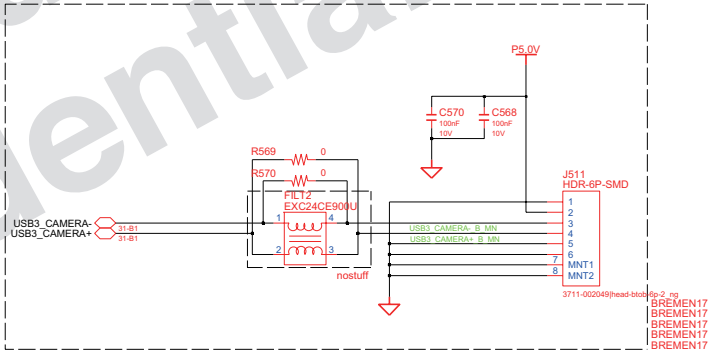


USB I/F Devices

Bluetooth Interface



CAMERA



DESIGN: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV	USB_DEVICES	
APPROVAL: HJ.KIM	REV: 1.0	BLUETOOTH & CAMERA	PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 48 OF 59	

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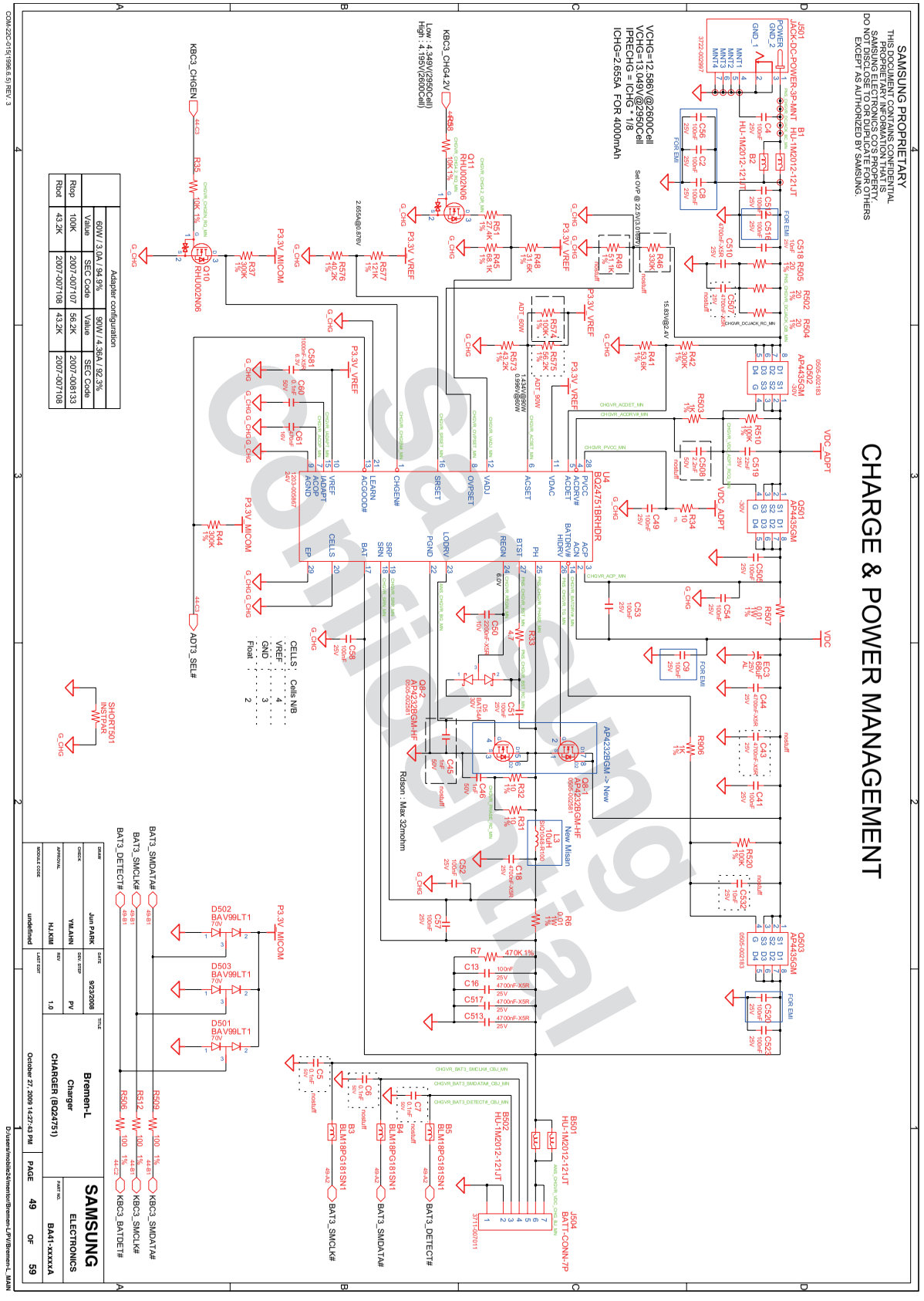
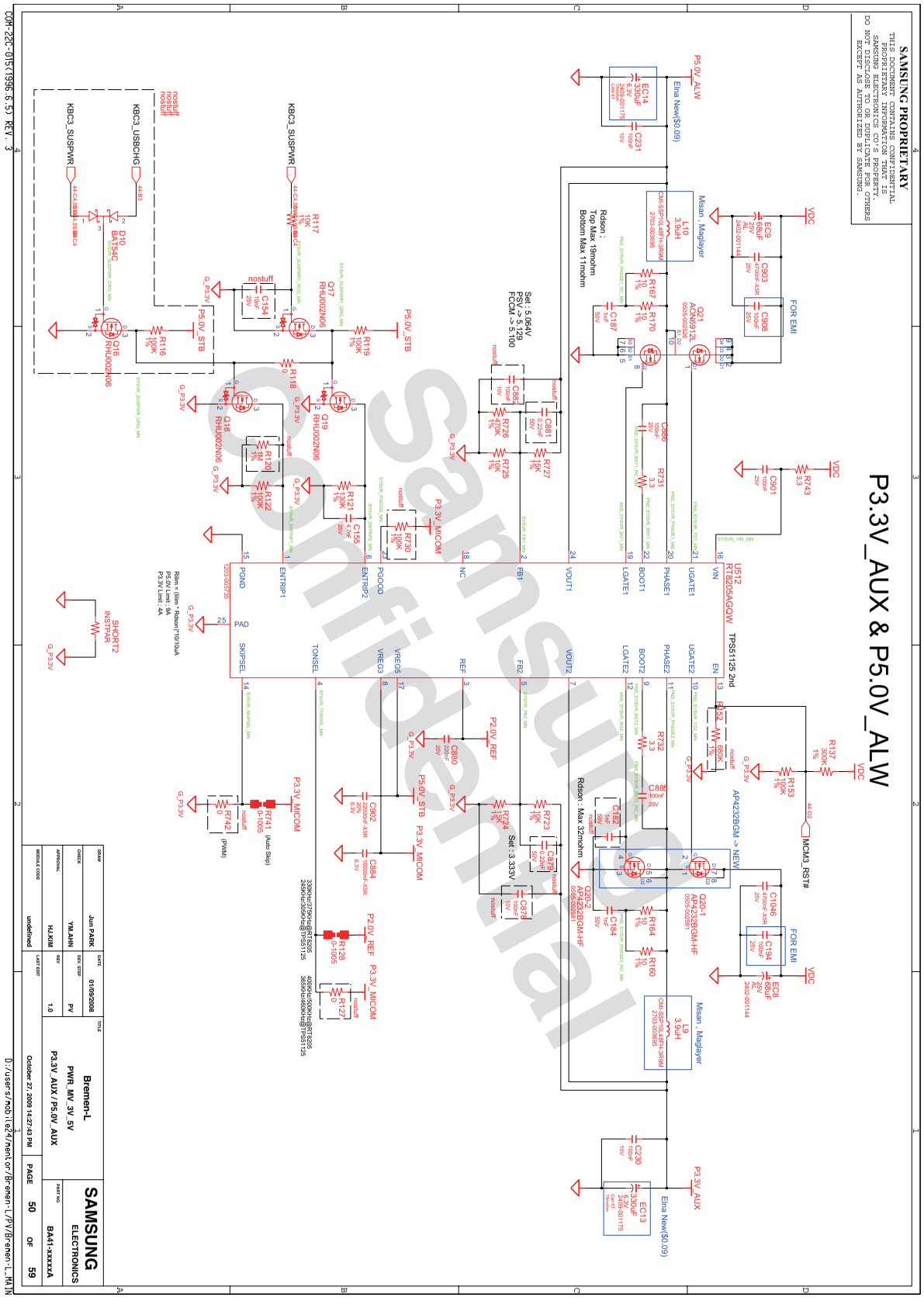
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

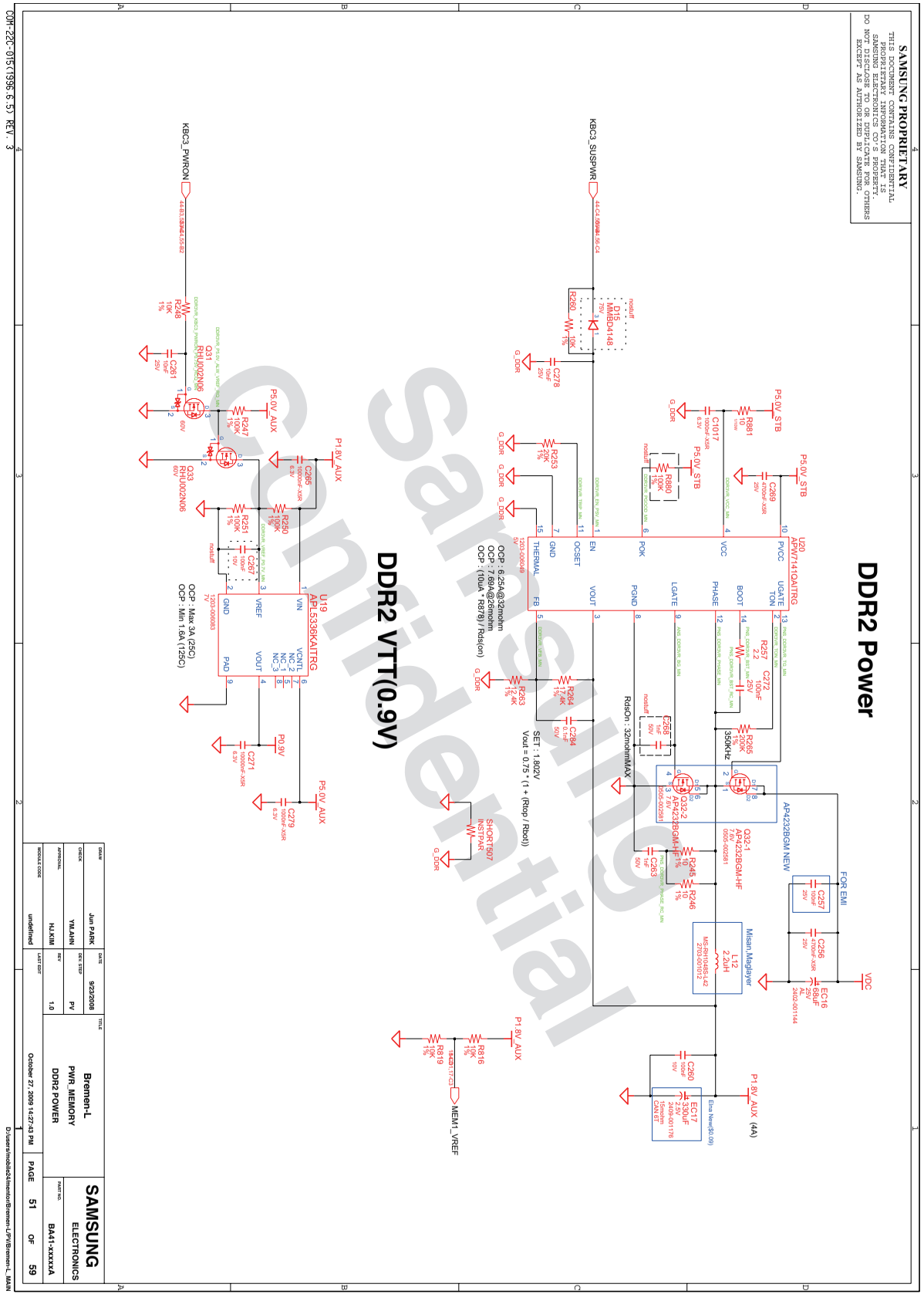
8. Block Diagram and Schematic



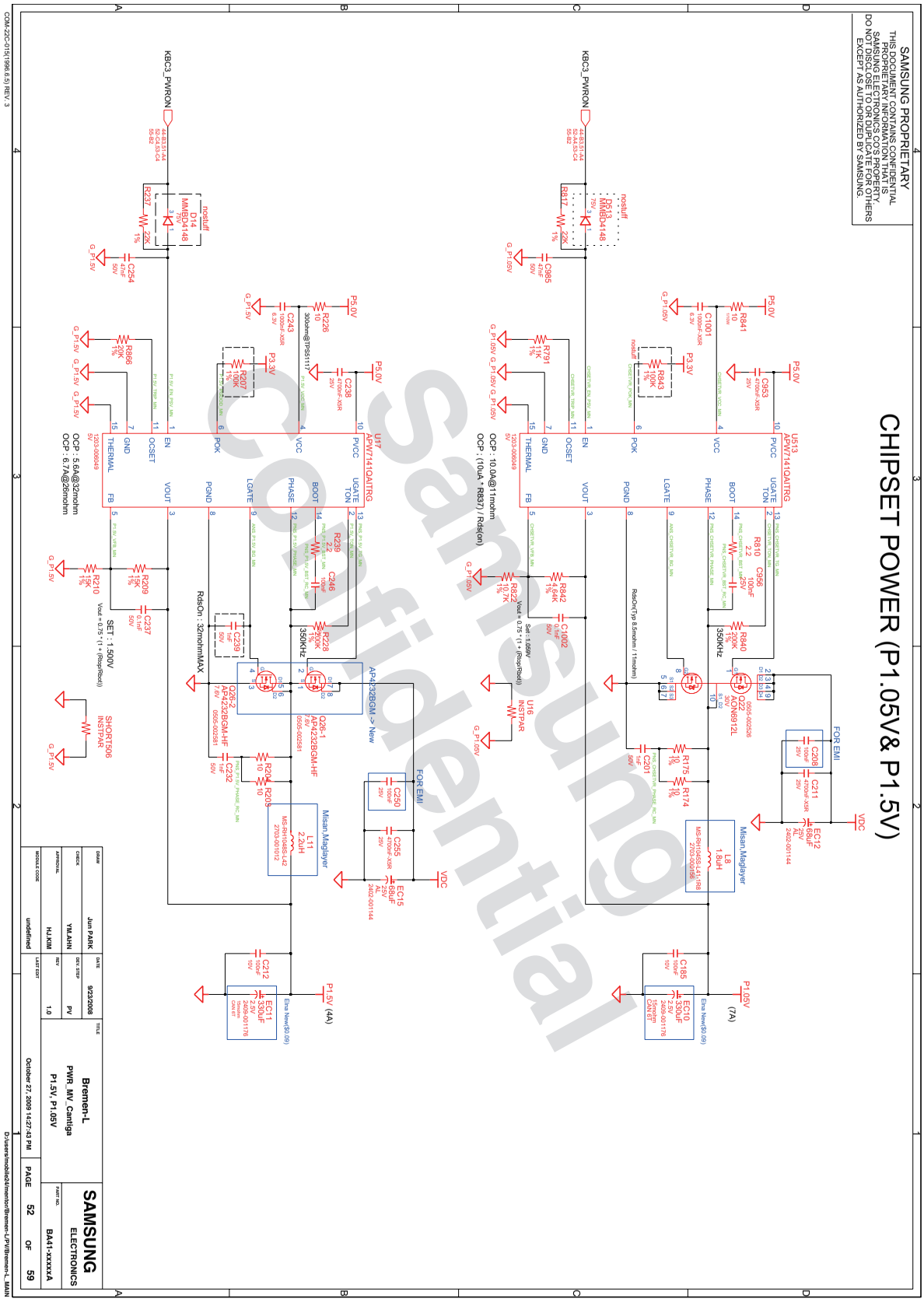
8. Block Diagram and Schematic



8. Block Diagram and Schematic

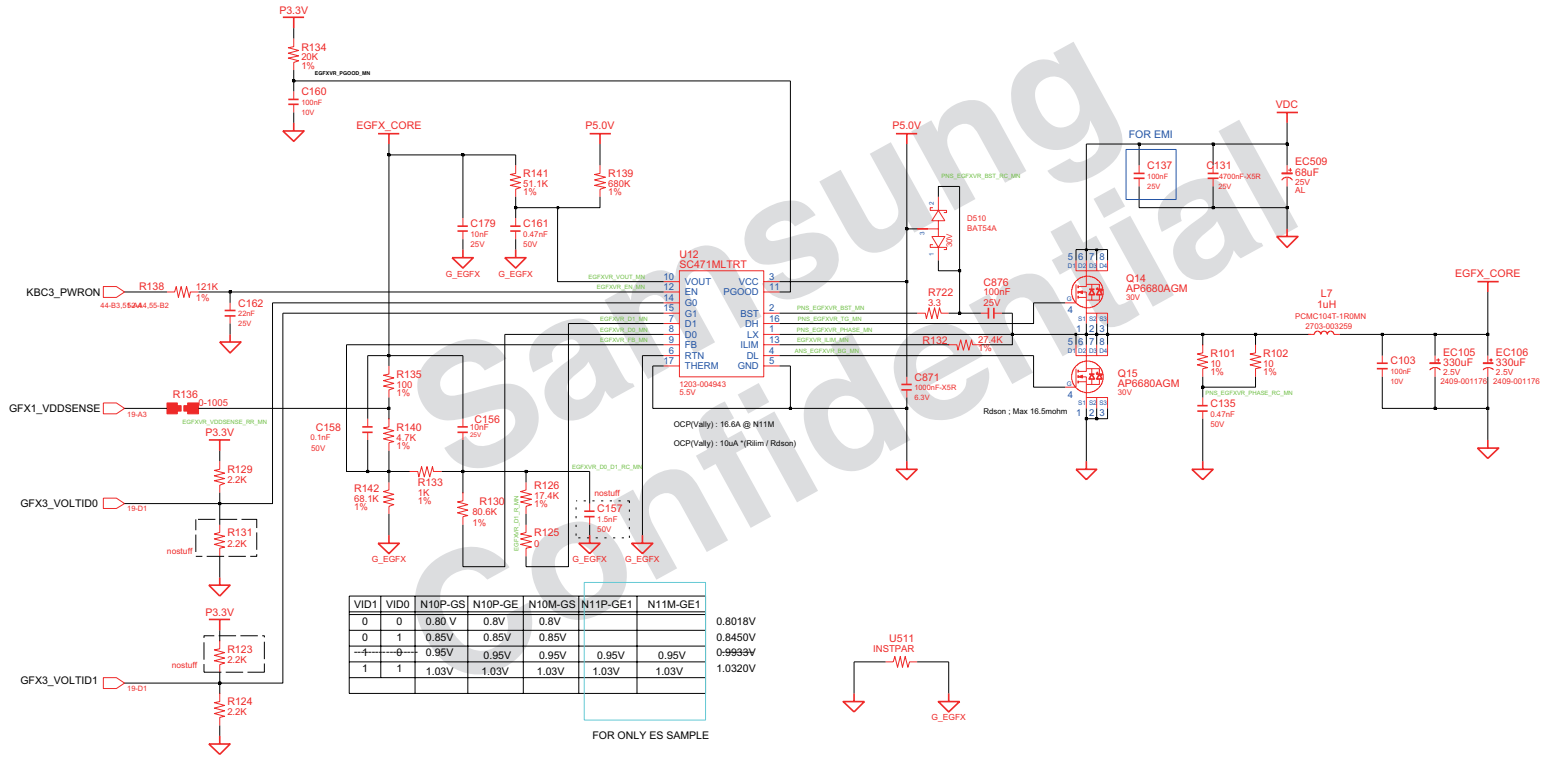


8. Block Diagram and Schematic



8. Block Diagram and Schematic

External Graphic Core Power



VID1	VID0	N10P-GS	N10P-GE	N10M-GS	N11P-GE1	N11M-GE1	
0	0	0.80 V	0.8V	0.8V			0.8018V
0	1	0.85V	0.85V	0.85V			0.8450V
~~1~~	~~0~~	0.95V	0.95V	0.95V	0.95V	0.95V	~~0.9933V~~
1	1	1.03V	1.03V	1.03V	1.03V	1.03V	1.0320V

FOR ONLY ES SAMPLE

DESIGN: Jun PARK	DATE: 9/3/2009	TITLE: Bremen-L PWR_MV_Cantiga EGFX CORE	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 53 OF 59	

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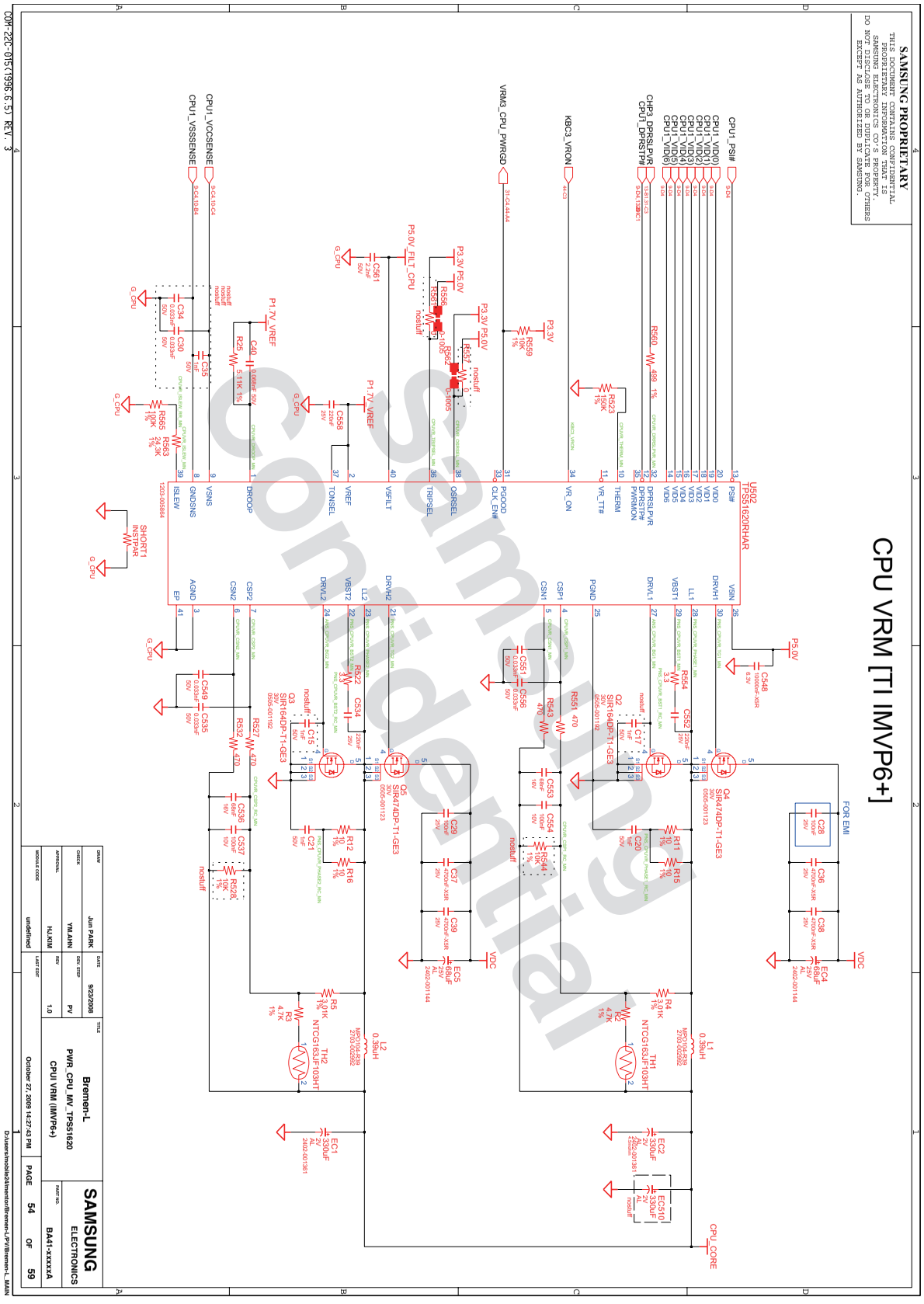
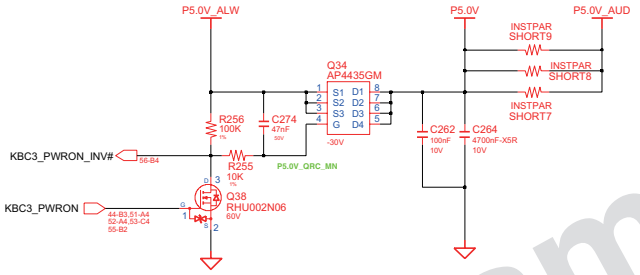
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

8. Block Diagram and Schematic

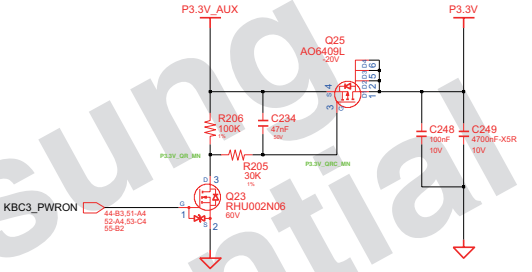


Switched Power

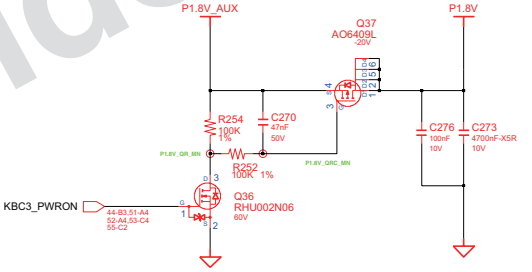
Switched Power On (P5.0V)



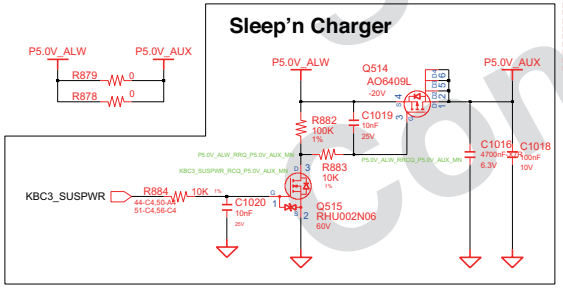
Switched Power On (P3.3V)



Switched Power On (P1.8V)



Sleep'n Charger



DRAW: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV	PWR_MV_SWITCHED	
APPROVAL: HJ.KIM	REV: 1.0	SWITCHED POWER	PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 55 OF 59	

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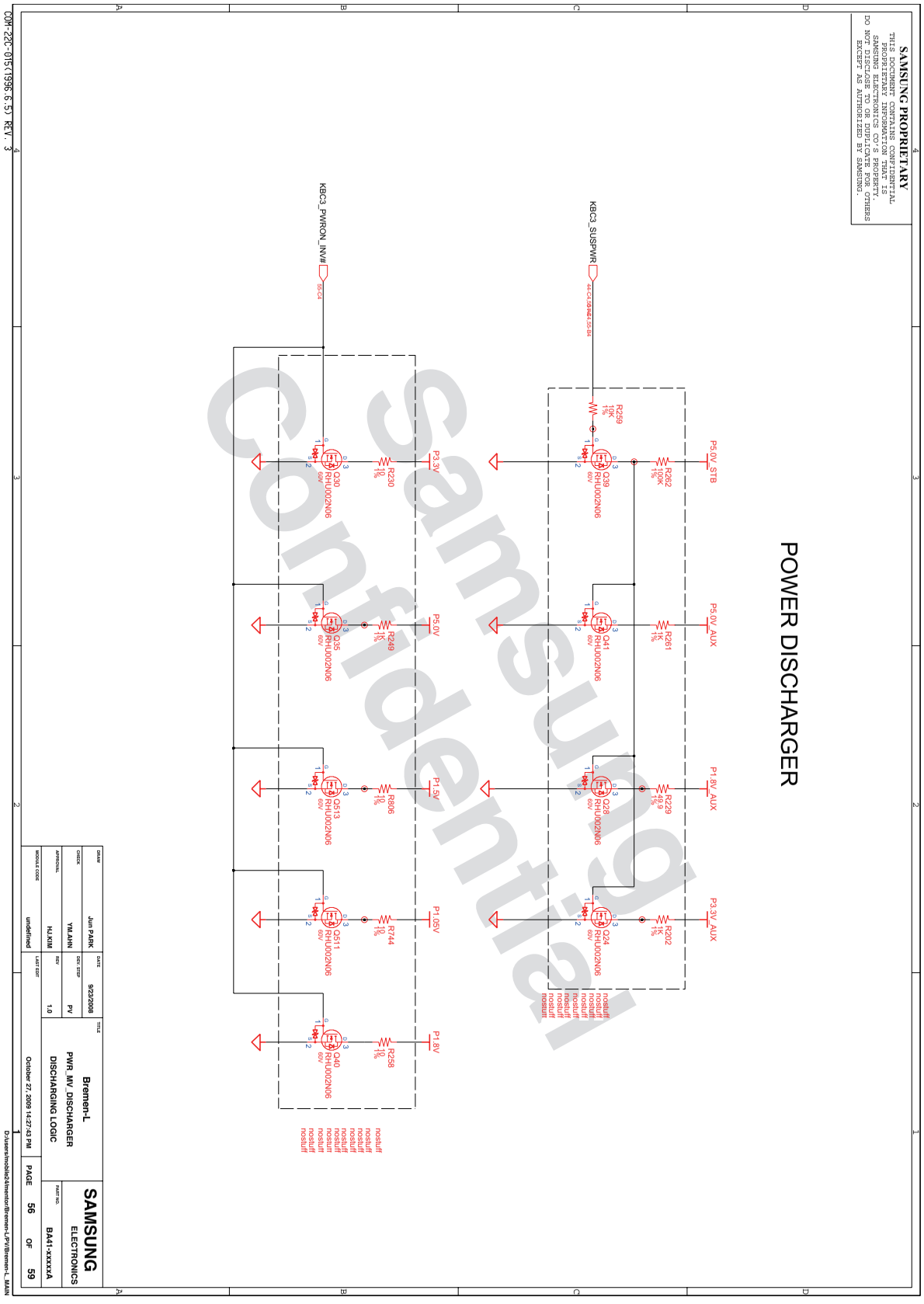
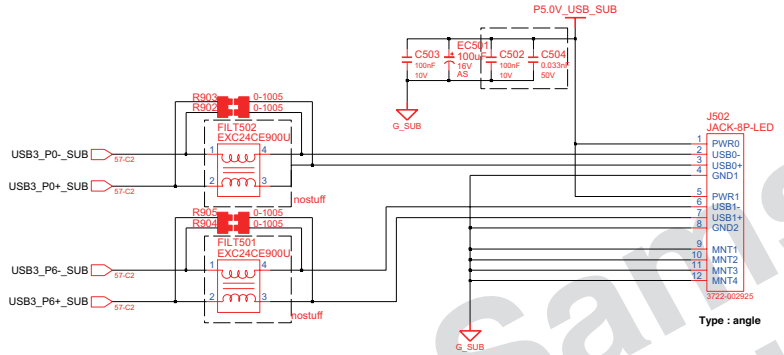
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

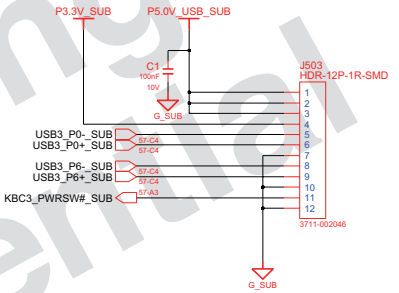
8. Block Diagram and Schematic



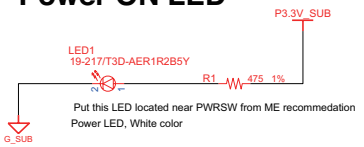
2 USB PORT & POWER S/W SUB B'D



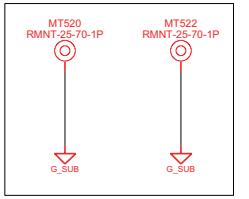
SUB TO MAIN USB CONN



Power ON LED



Power Button



USB sub board mount hole

DESIGN: Jun PARK	DATE: 8/22/2009	TITLE: Bremen-L SUB BOARD1 USB PORT, POWER SW SUBBOARD	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 57 OF 59	

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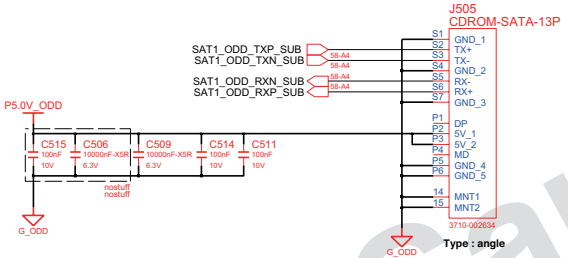
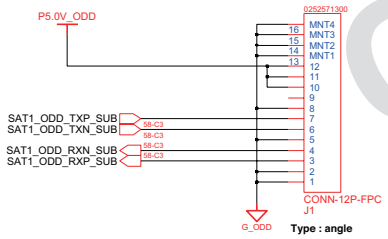
D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

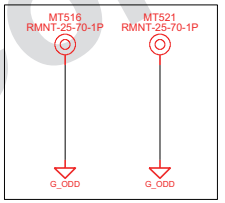
SATA ODD SUBBOARD

SATA ODD CONN



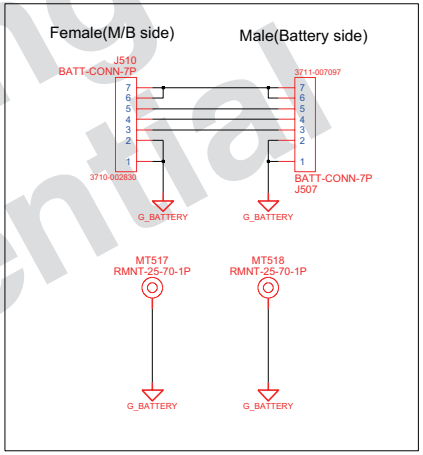
SUB TO MAIN SATA ODD CONN





ODD sub board mount hole

BATTERY SUBBOARD

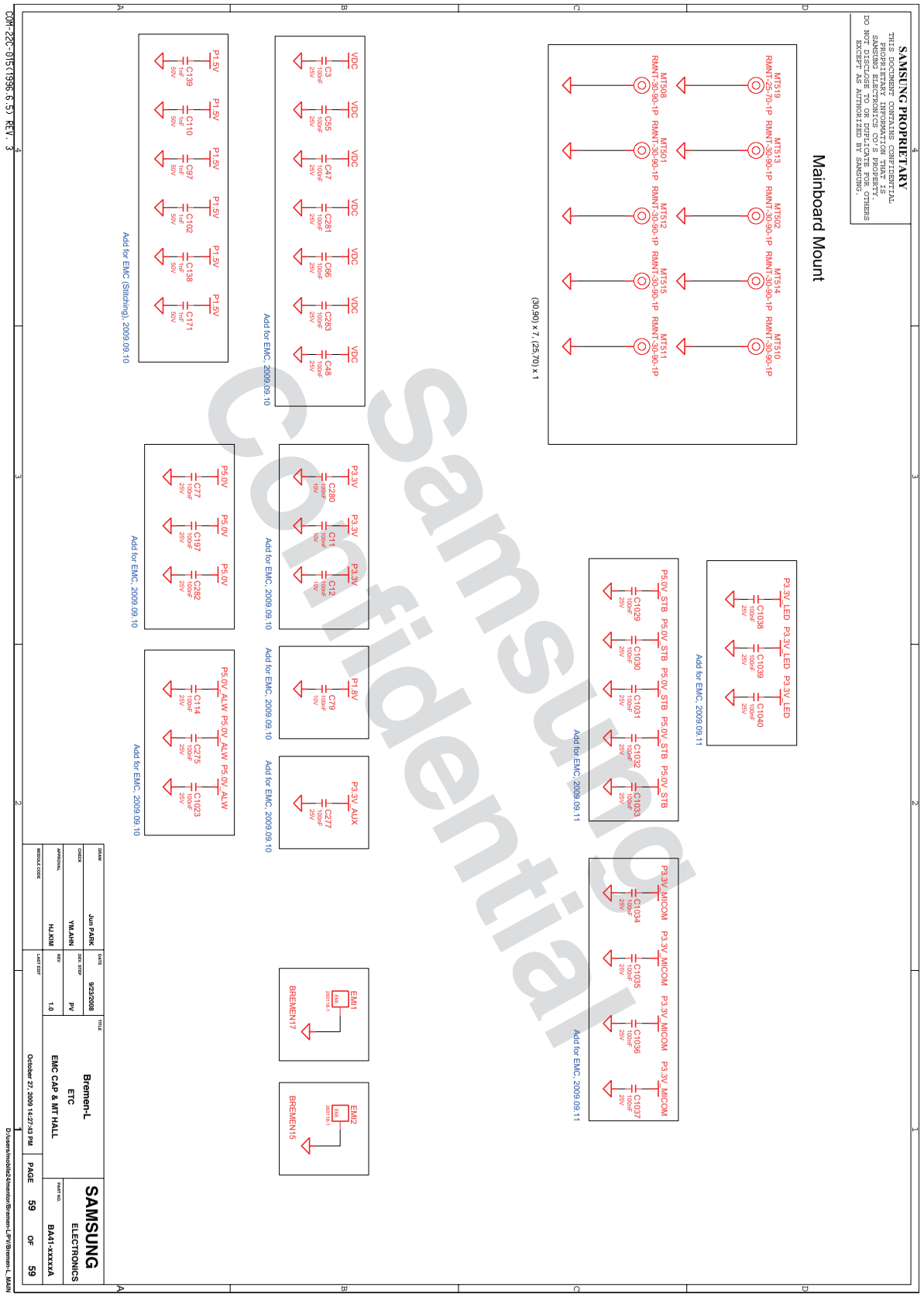


DRAW: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. STEP: PV	SUB BOARD2	
APPROVAL: HJ.KIM	REV: 1.0	SATA ODD SUB BOARD	PART NO.: BA41-xxxxxA
MODULE CODE: undefined	LAST EDIT: October 27, 2009 14:27:43 PM	PAGE 58 OF 59	

COM-22C-015(1996.6.5) REV. 3

D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L_MAIN

8. Block Diagram and Schematic



Bremen-UL

CPU : Intel Penryn
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : Bremen-UL
PBA Name : MAIN
PCB Code : GCE : BA41-01177A
NAN : BA41-01178A
HAN : BA41-01179A
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.10.19

Design	CHECK	APPROVAL

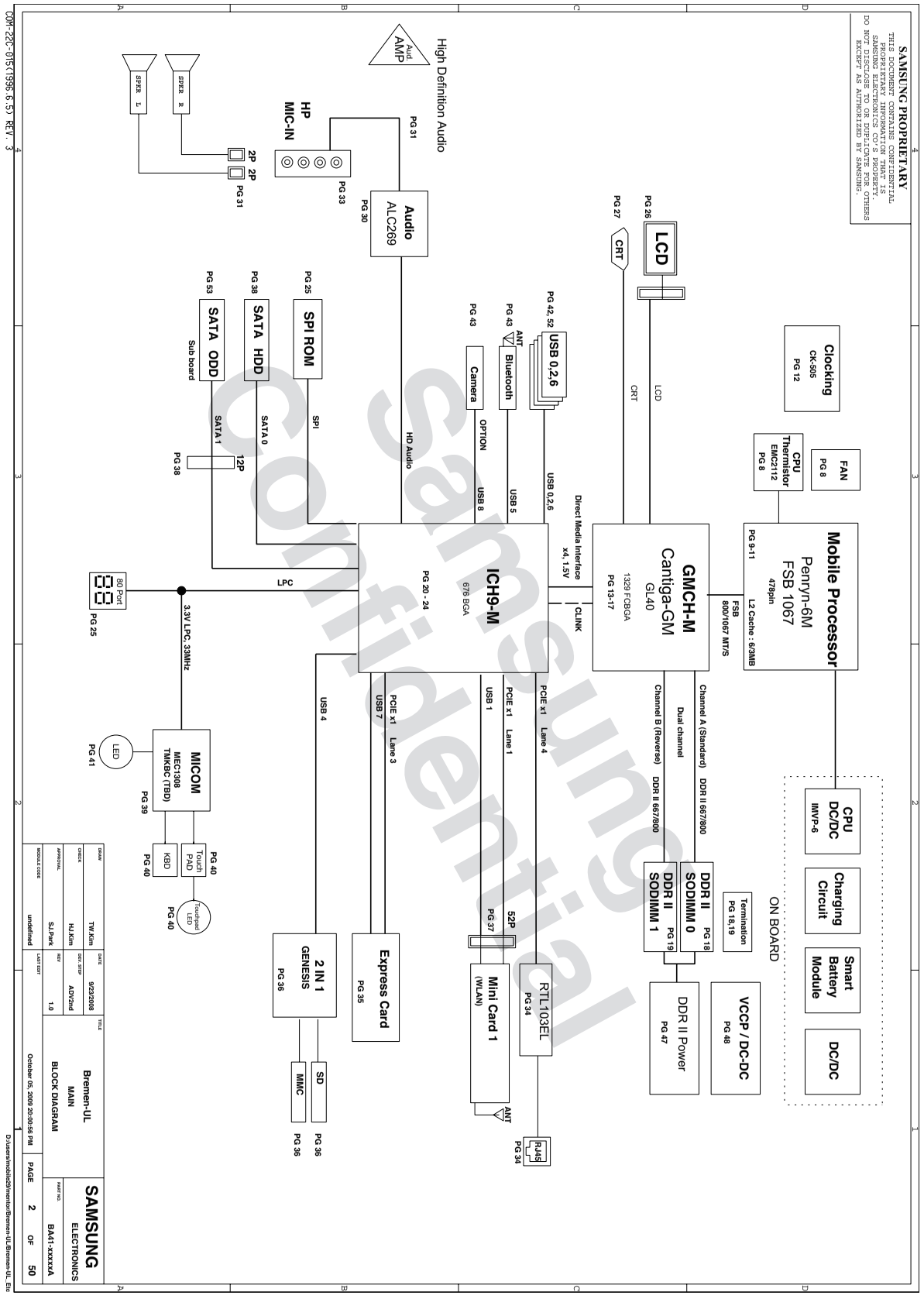
■ *Owner : SEC Mobile R & D* *Signature :* *X*

DRAW TW.Kim	DATE 10/10/2008	TITLE Bremen-UL MAIN COVER	SAMSUNG ELECTRONICS
CHECK HJ.Kim	DEV. STEP ADV2nd		
APPROVAL SJ.Park	REV 1.0		PART NO. BA41-xxxxxA
MODULE CODE	LAST EDIT October 05, 2009 20:00:56 PM	PAGE 1 OF 50	

COM-22C-015(1996.6.5) REV. 3

D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

8. Block Diagram and Schematic



8. Block Diagram and Schematic

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	RealTek 88E8057

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

I^2C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	SYSTEM PORT 2
3	NC
4	NC
5	Bluetooth
6	Mini PCI Express 2
7	Camera
8	NC
9	NC

PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	LOM
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

(This table will be update.)

REVISION HISTORY

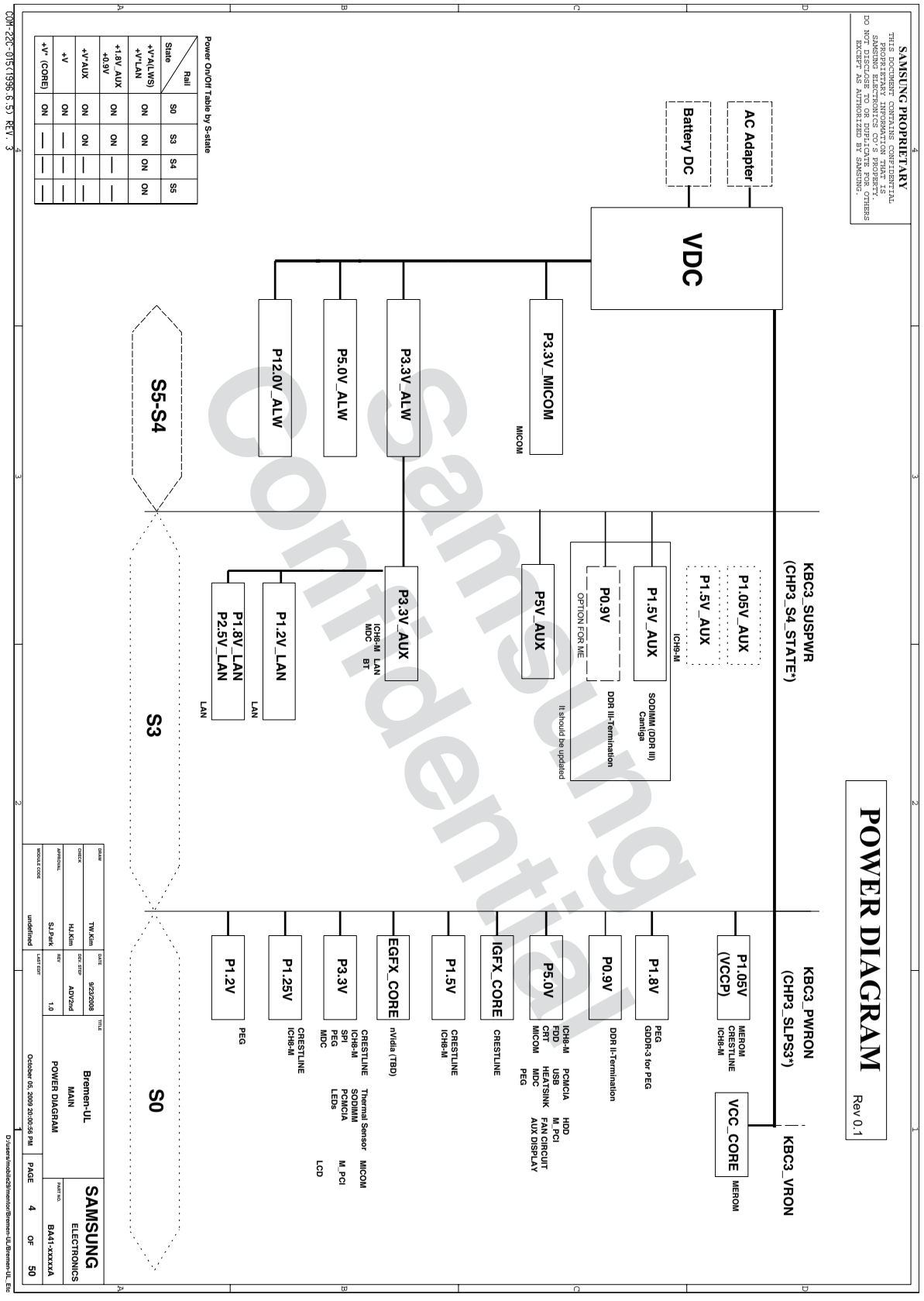
See rev notes for more information.

DRAW: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL / MAIN / BOARD INFO	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd		PART NO.: BA41-xxxxxA
APPROVAL: SJ.Park	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 3 OF 50	

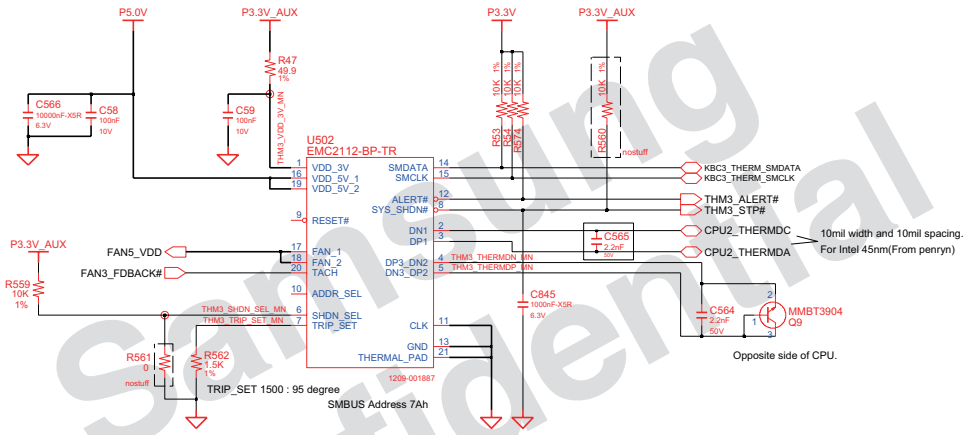
COM-22C-015(1996.6.5) REV. 3

D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

8. Block Diagram and Schematic

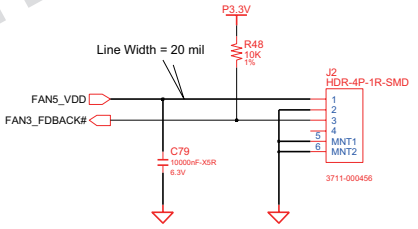


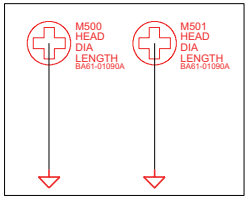
THERMAL SENSOR & FAN CONTROL



SHDN_SEL MODE	
0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

ADDRESSS_SEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb





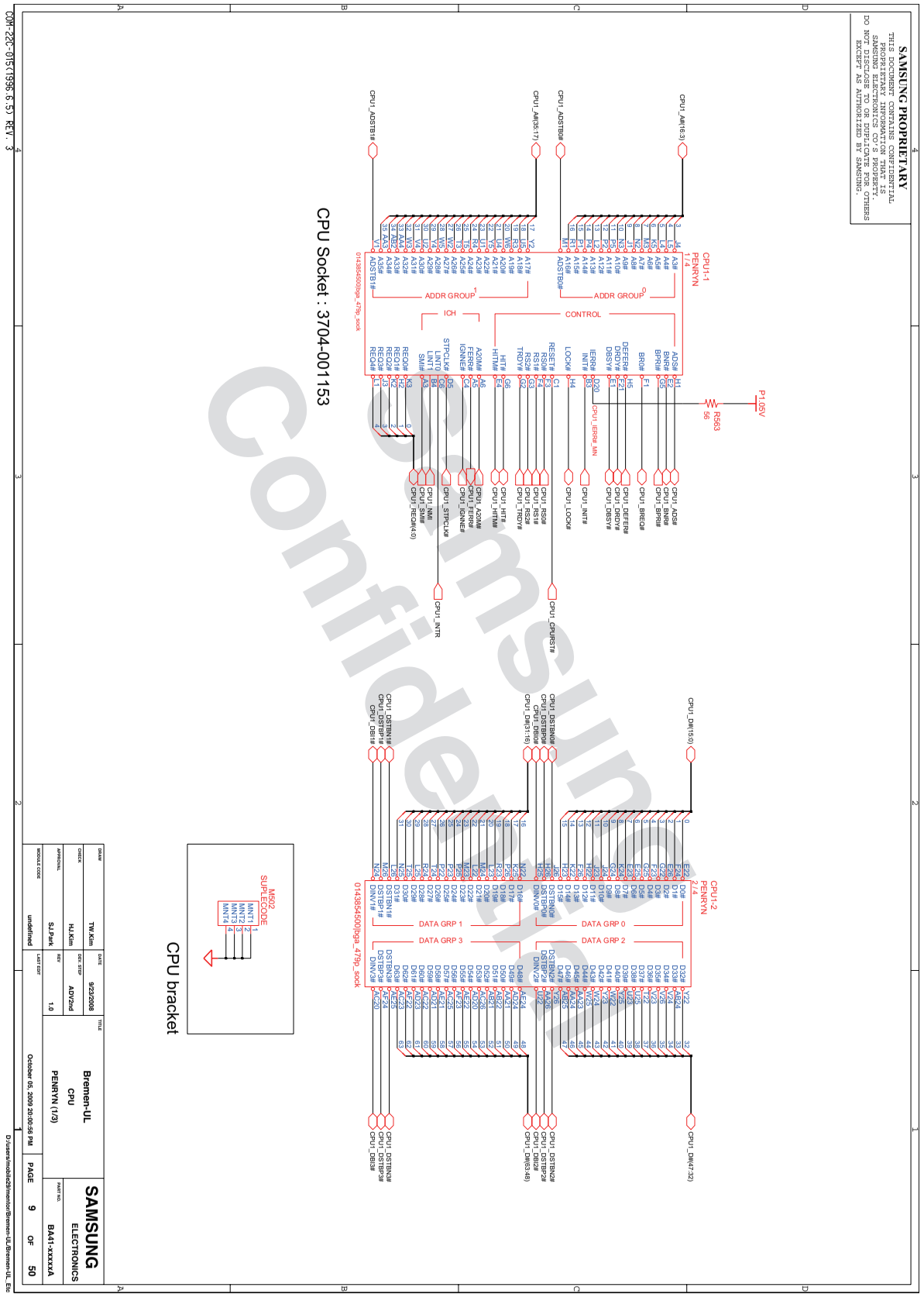
To support heatsink

DESIGN: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL THERMAL SENSOR THERMAL SENSOR EMC2112	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd		
APPROVAL: SJ.Park	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 05, 2009 20:00:56 PM		PAGE 8 OF 50

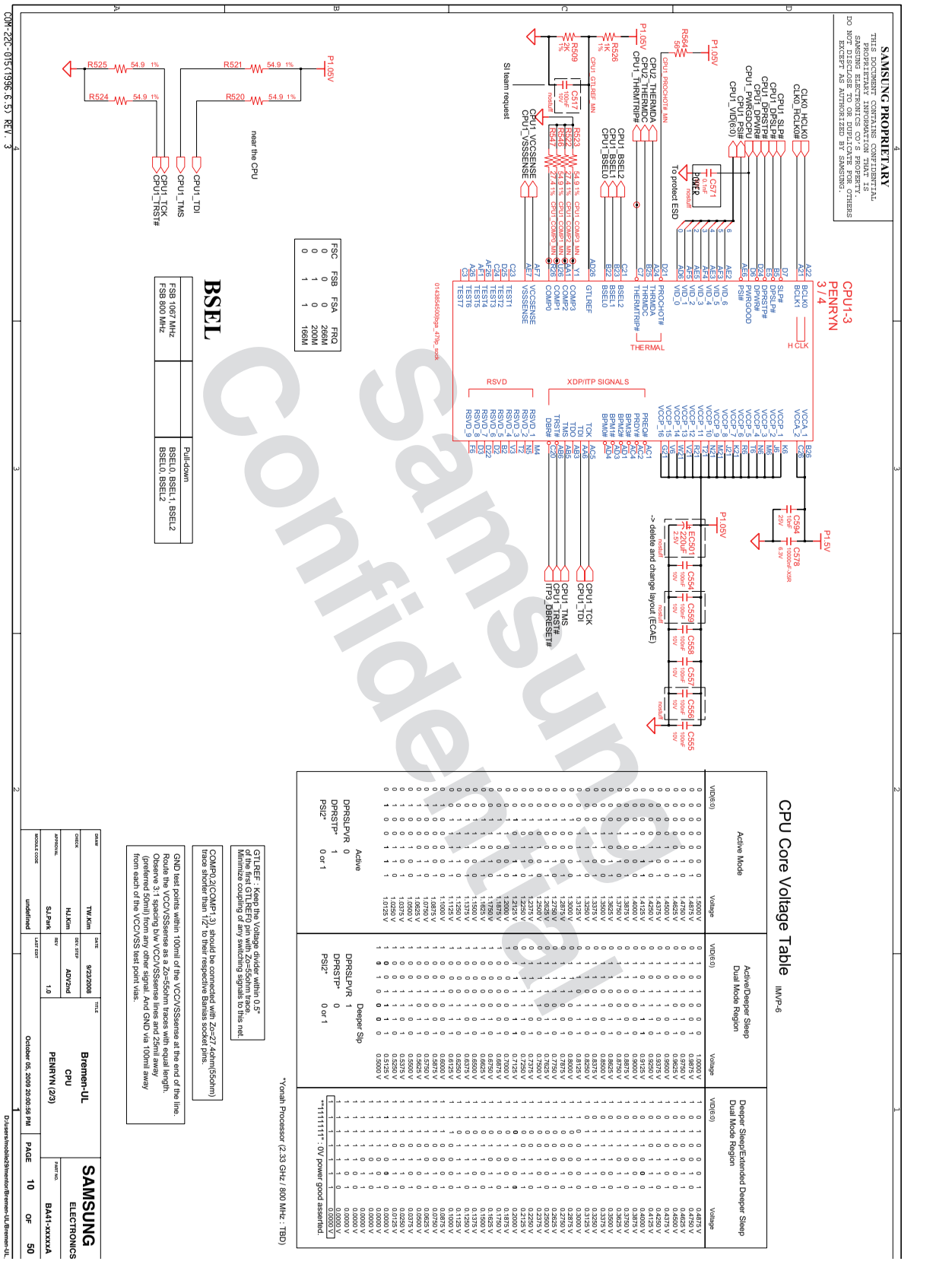
COM-22C-015(1996.6.5) REV. 3

D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

8. Block Diagram and Schematic



8. Block Diagram and Schematic



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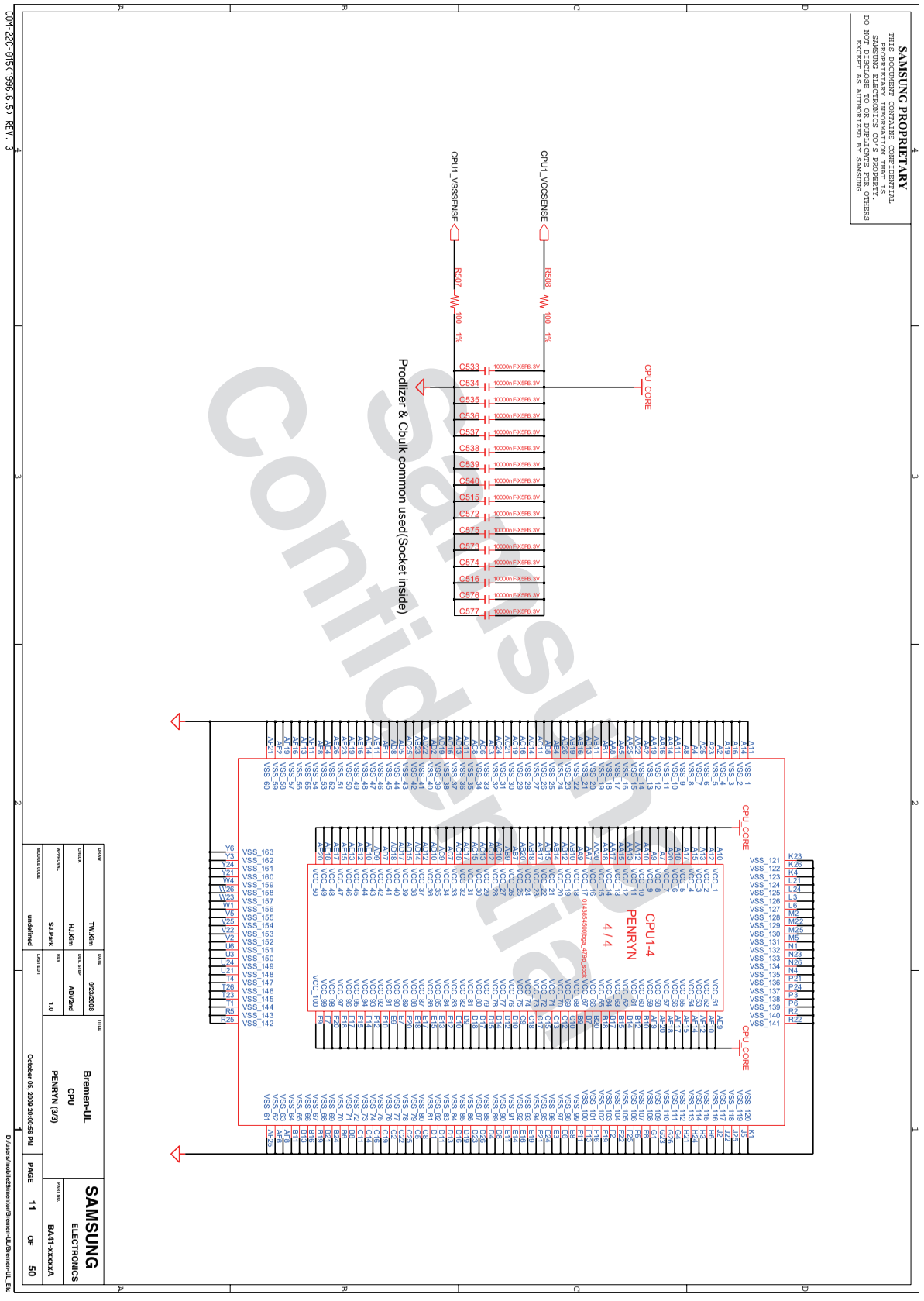

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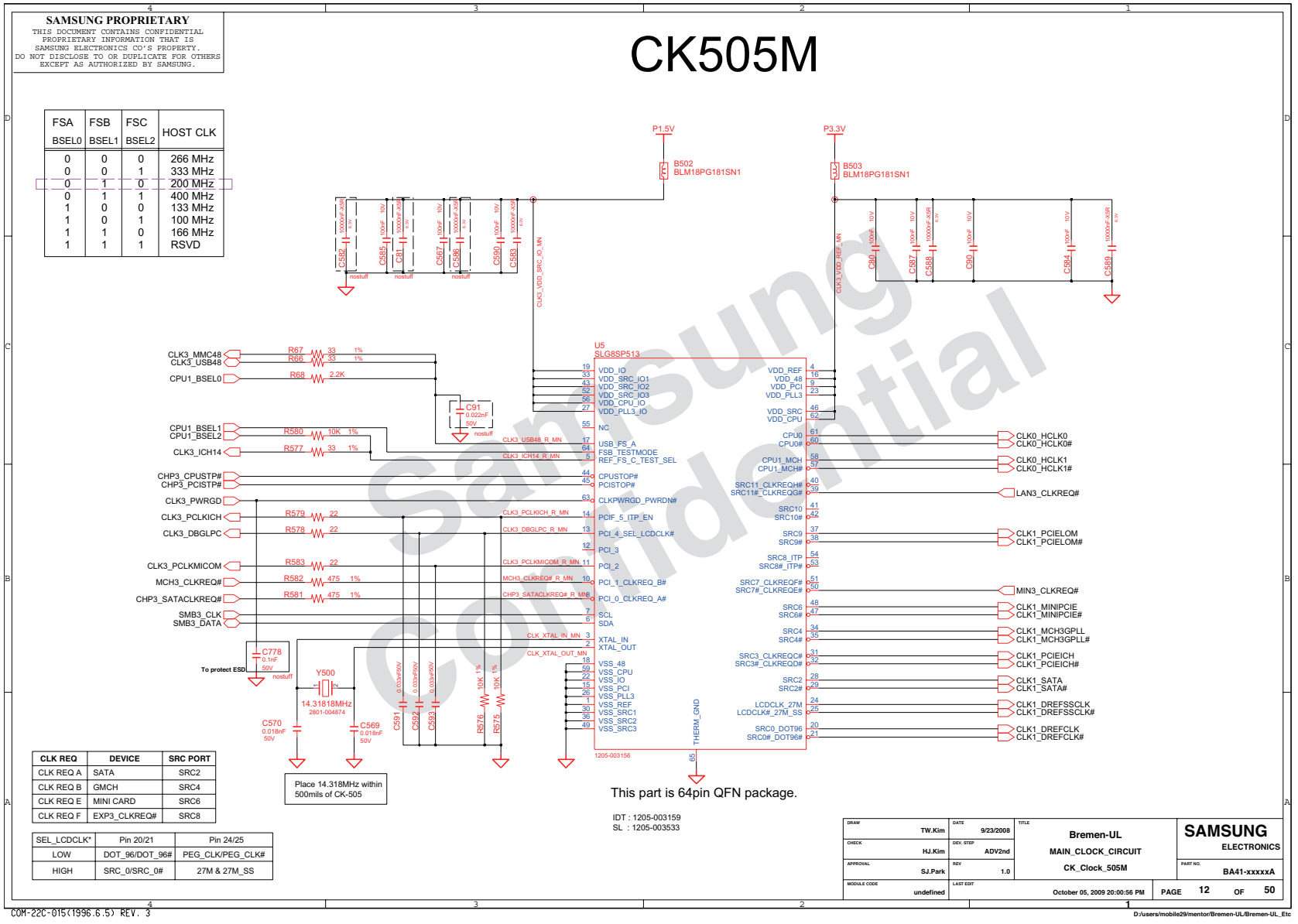

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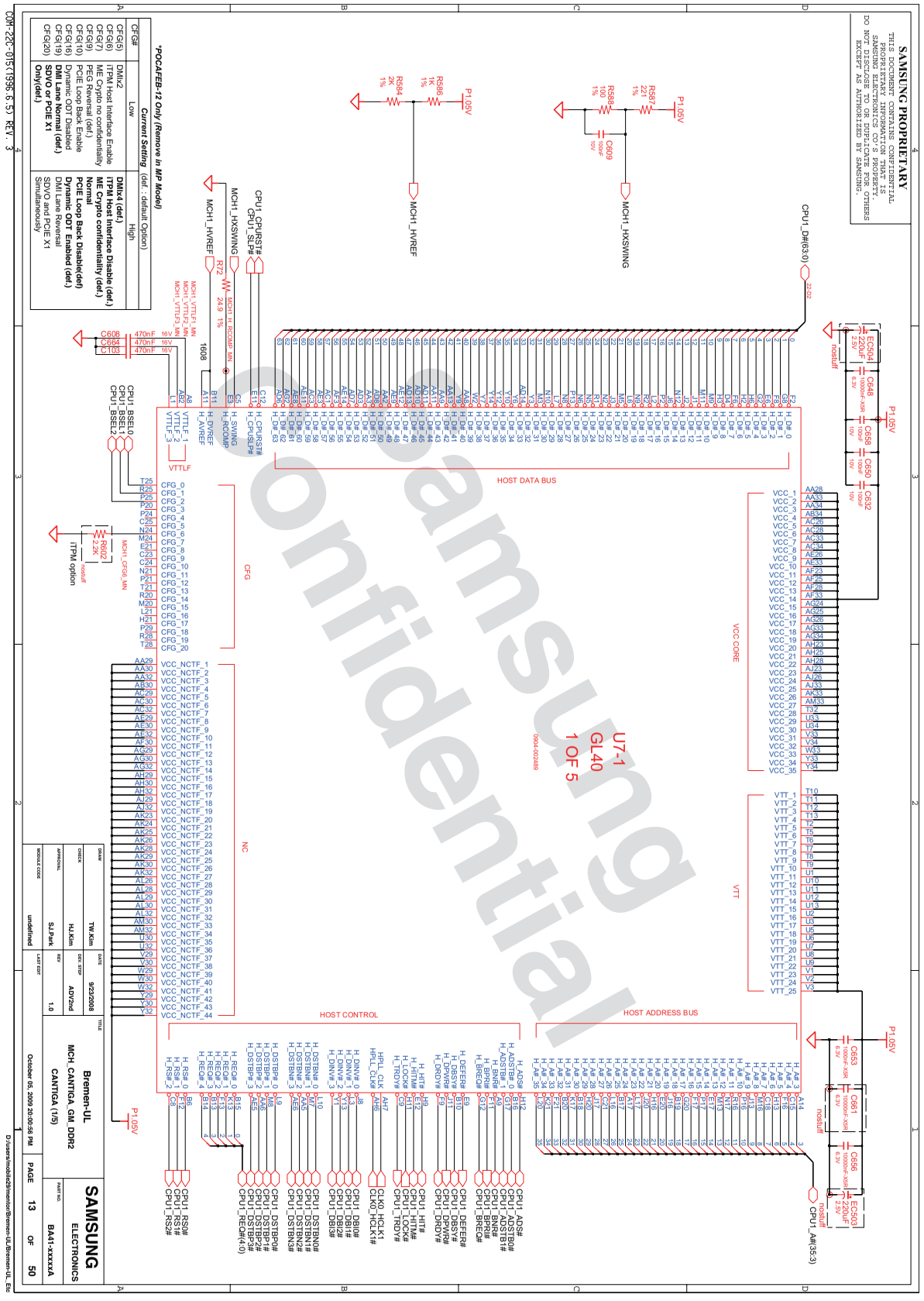
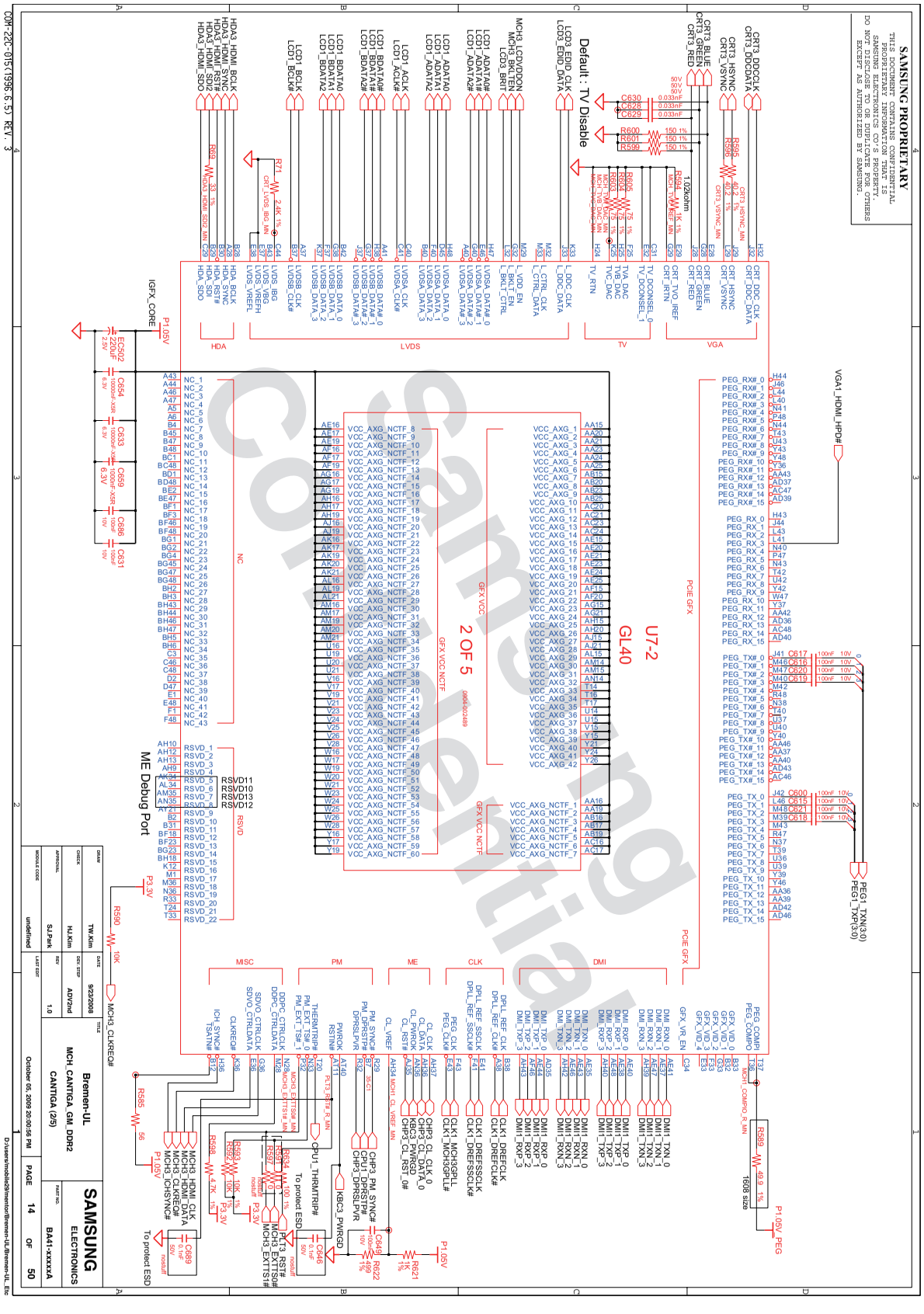
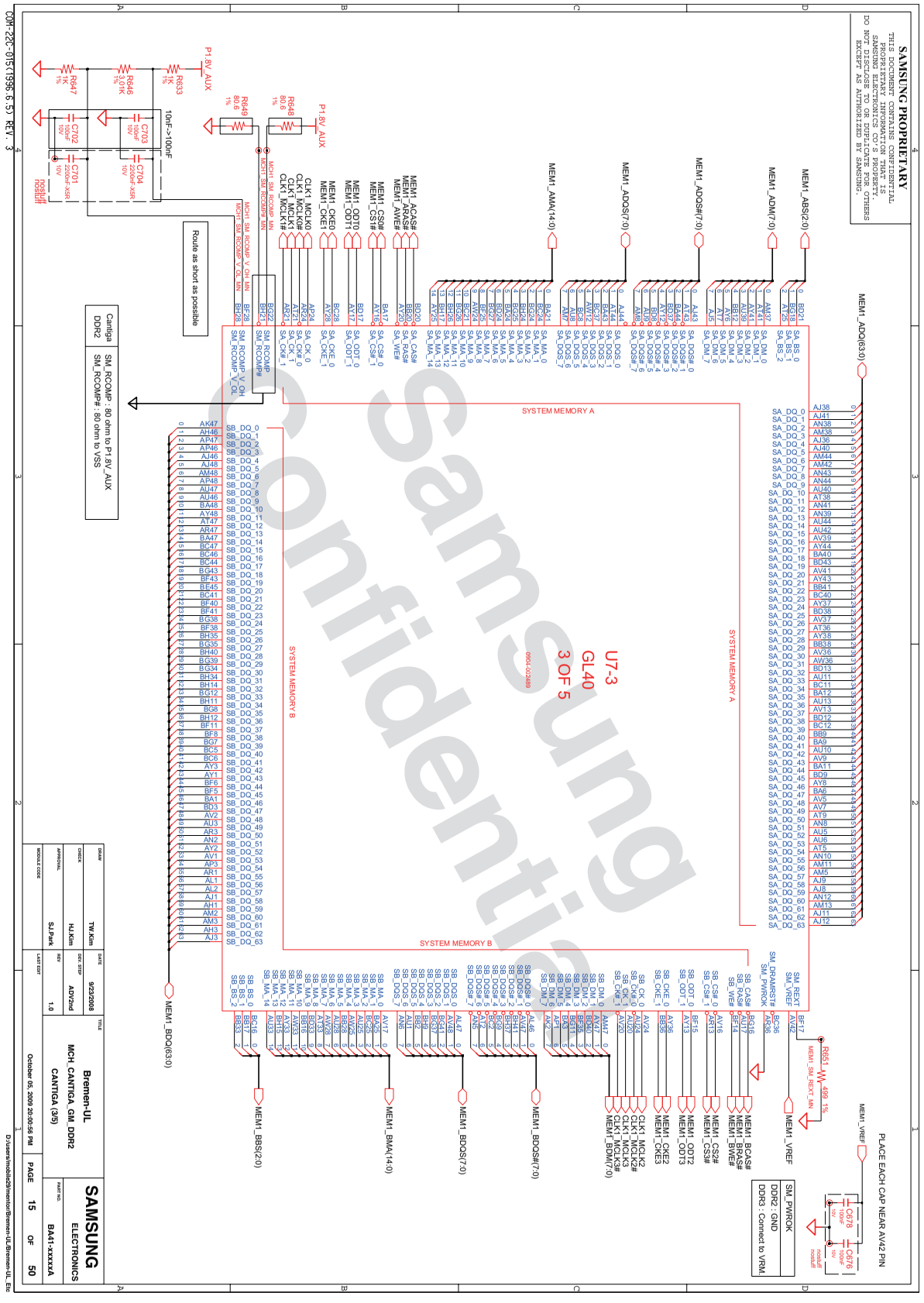


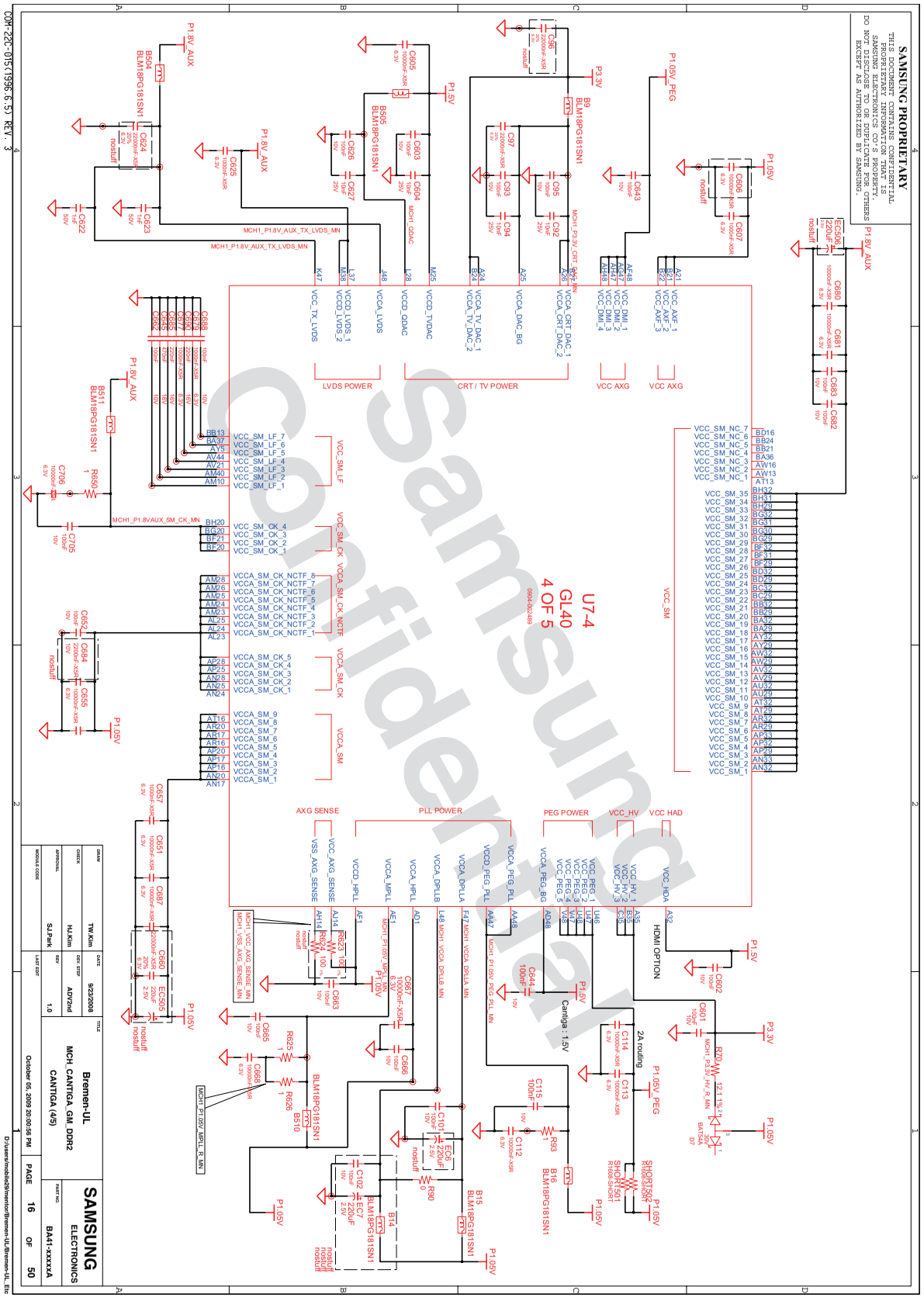
8. Block Diagram and Schematic



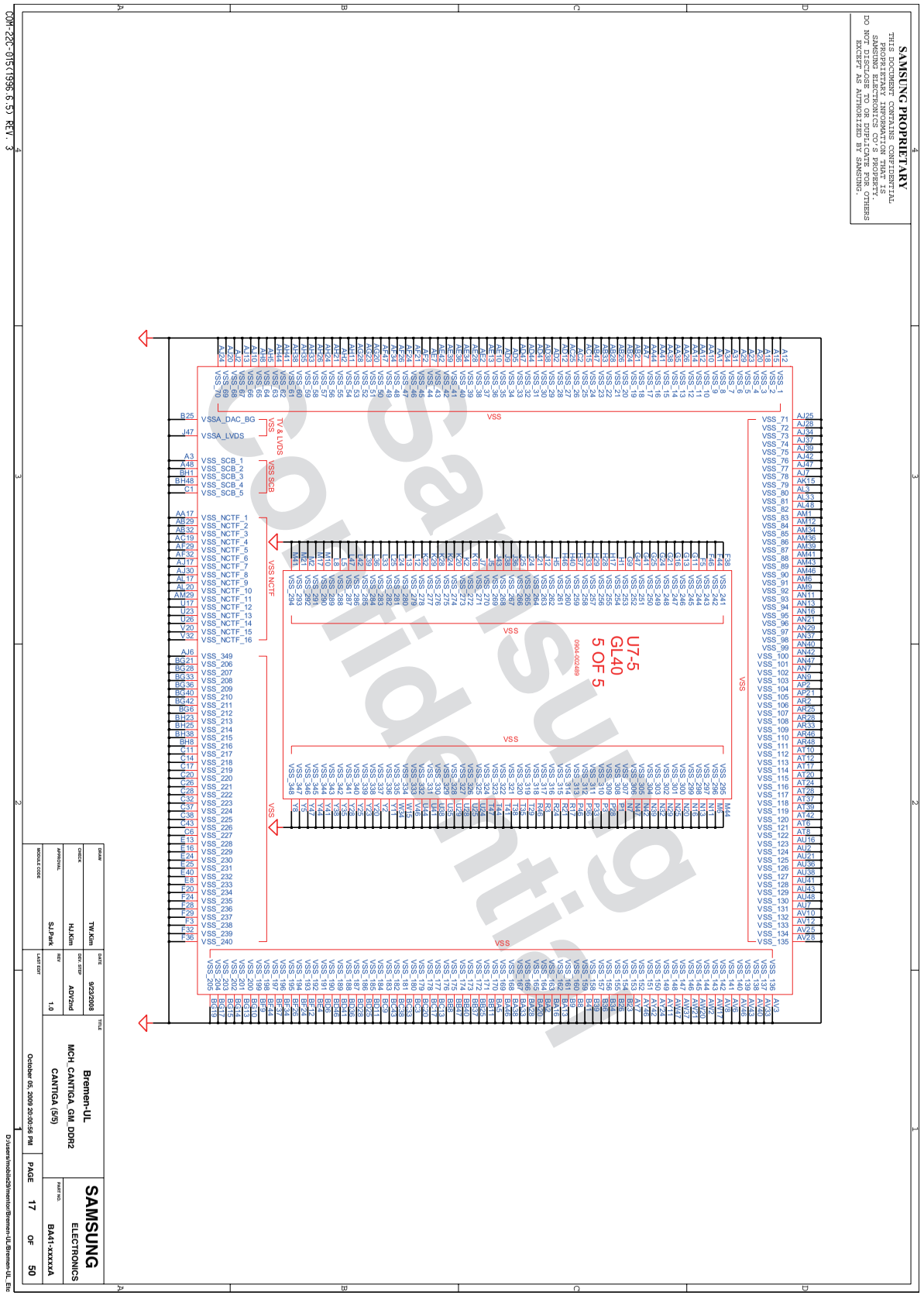
8. Block Diagram and Schematic



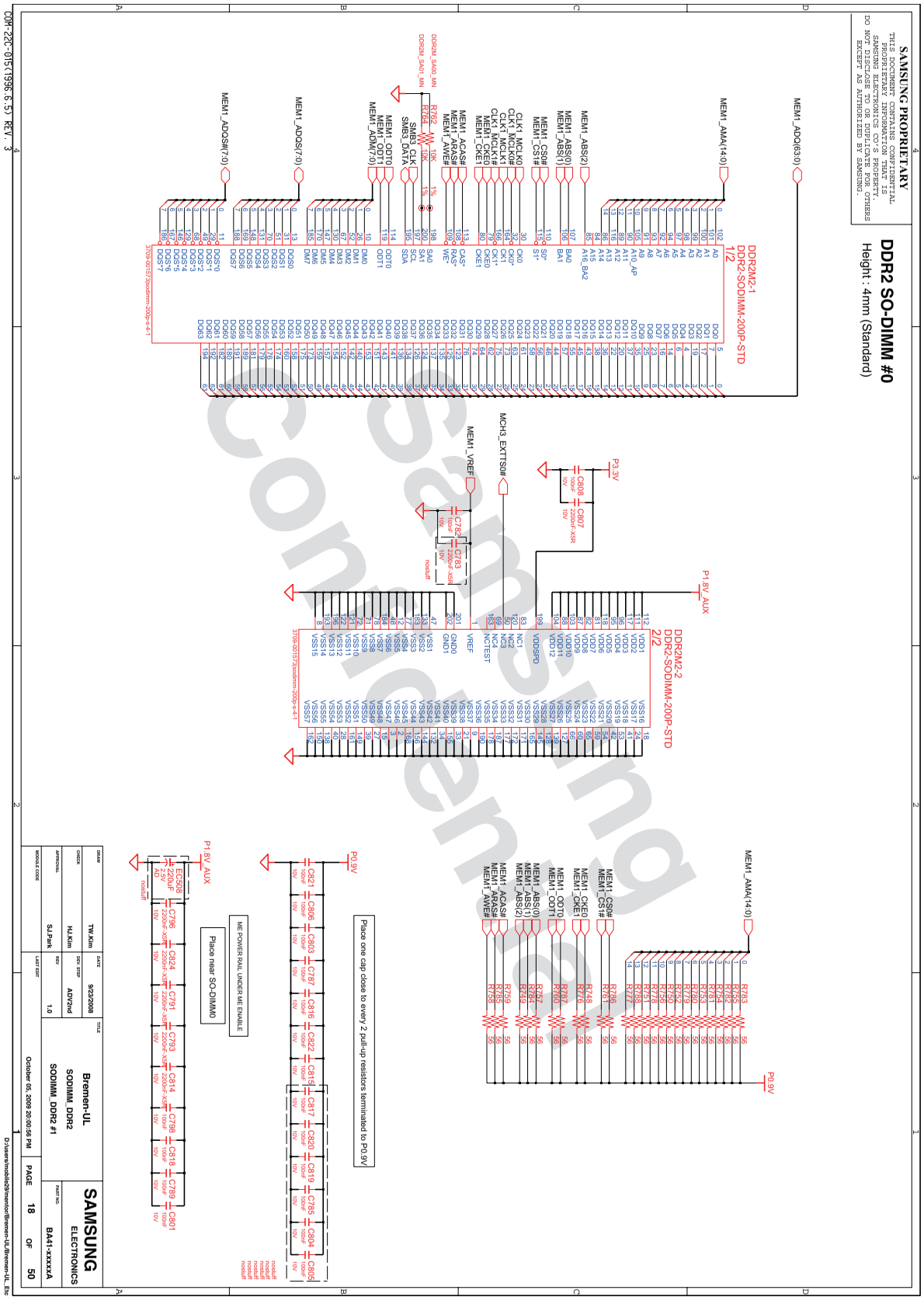
8. Block Diagram and Schematic



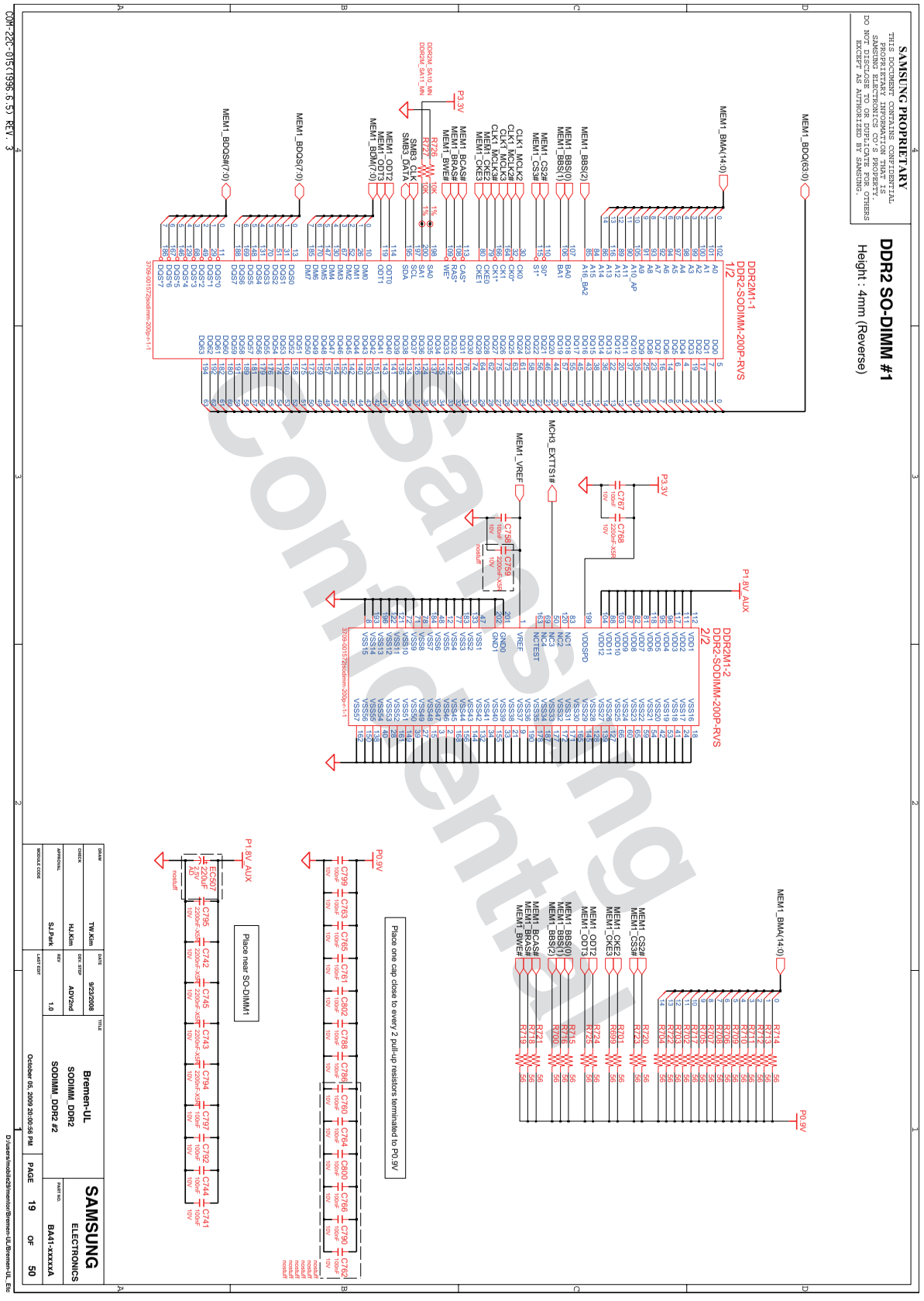
8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic



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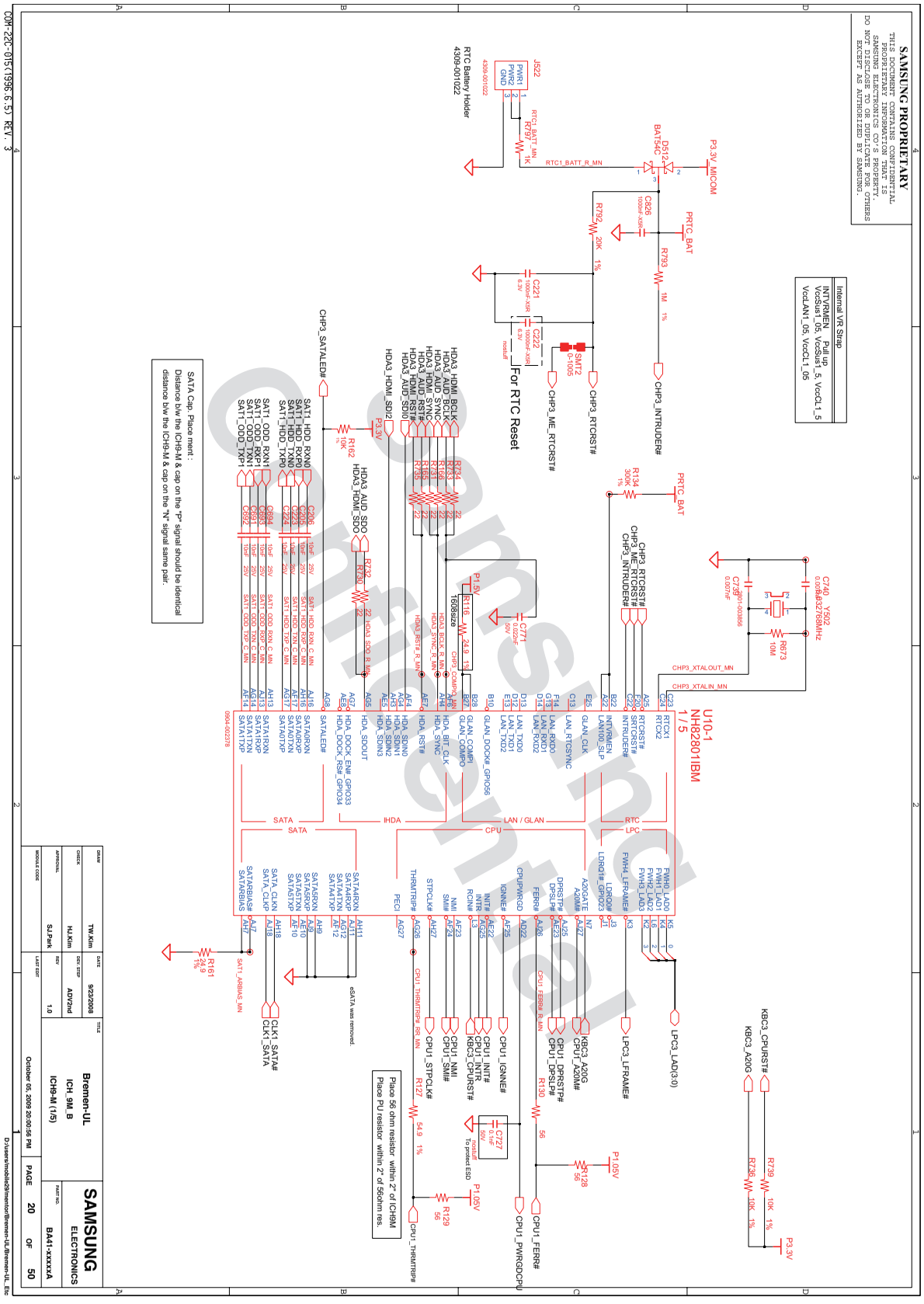
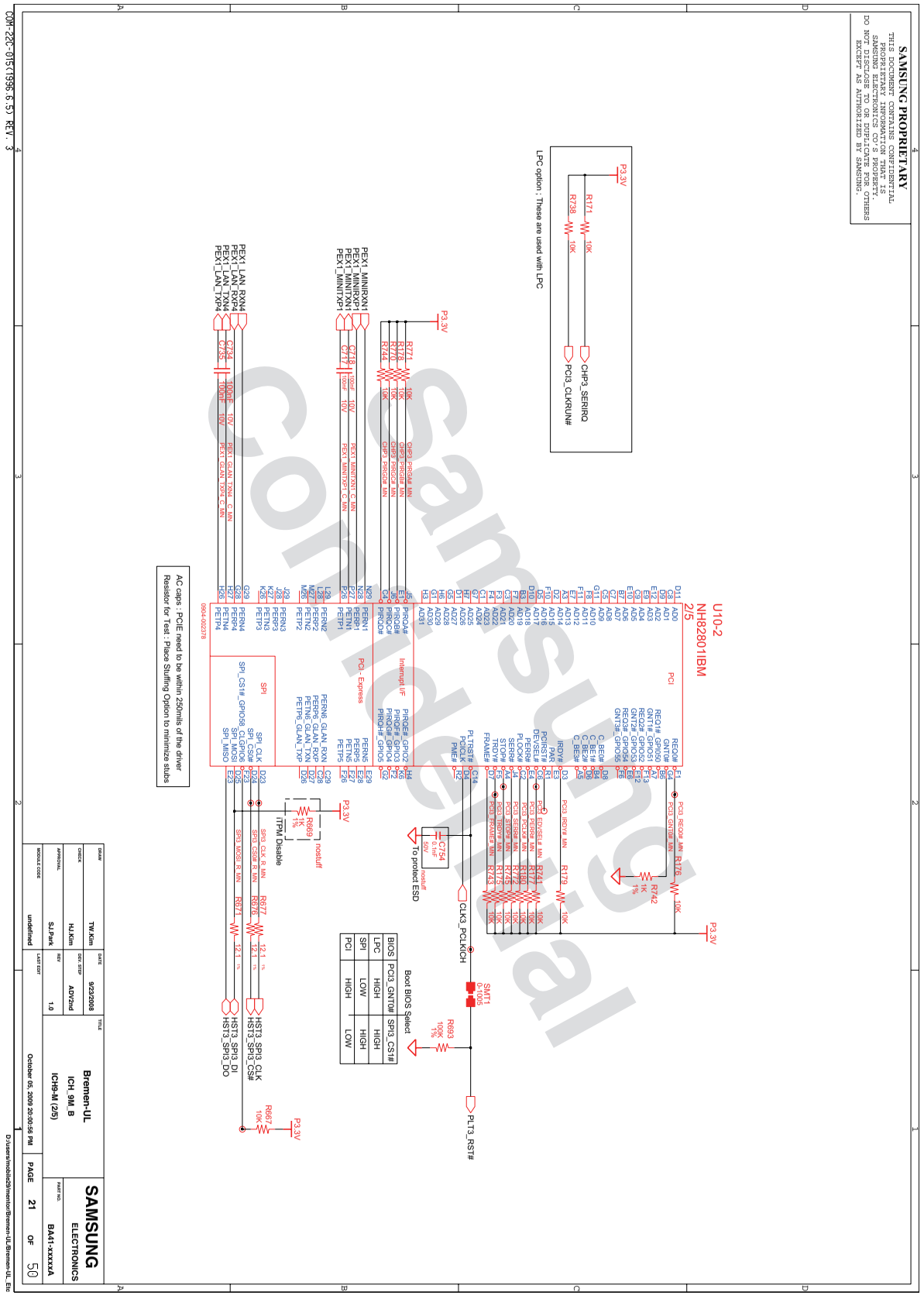


8. Block Diagram and Schematic



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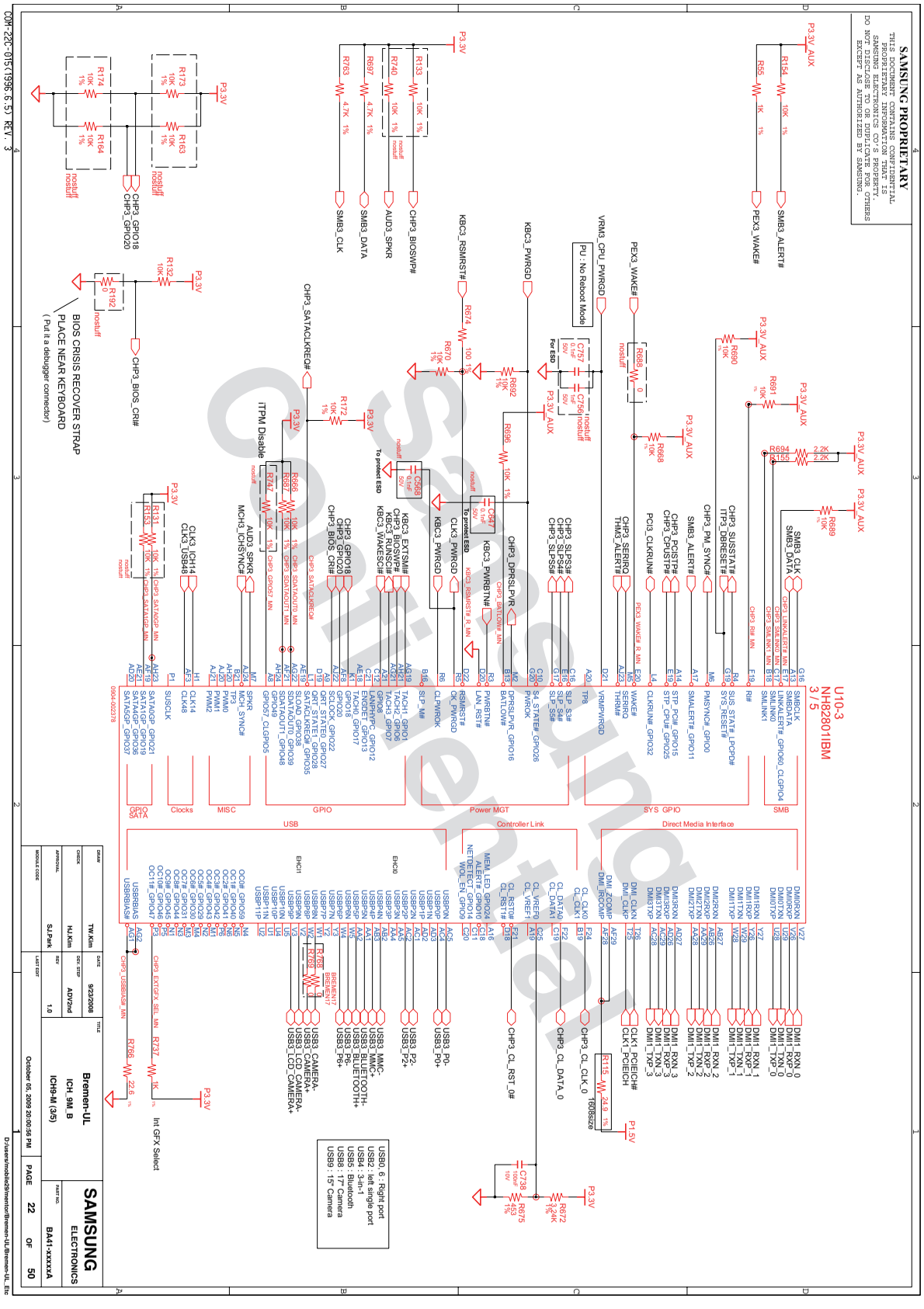

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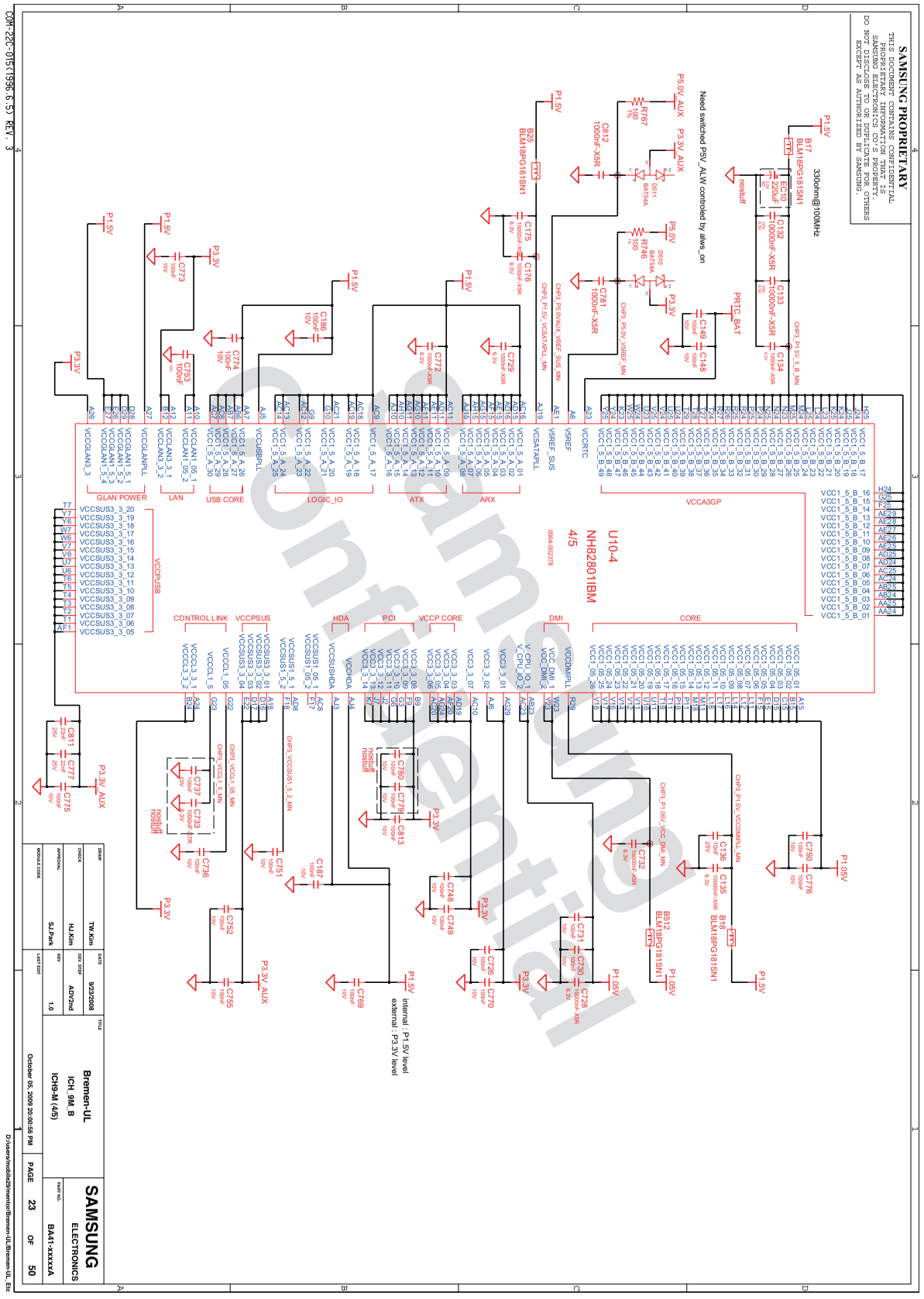
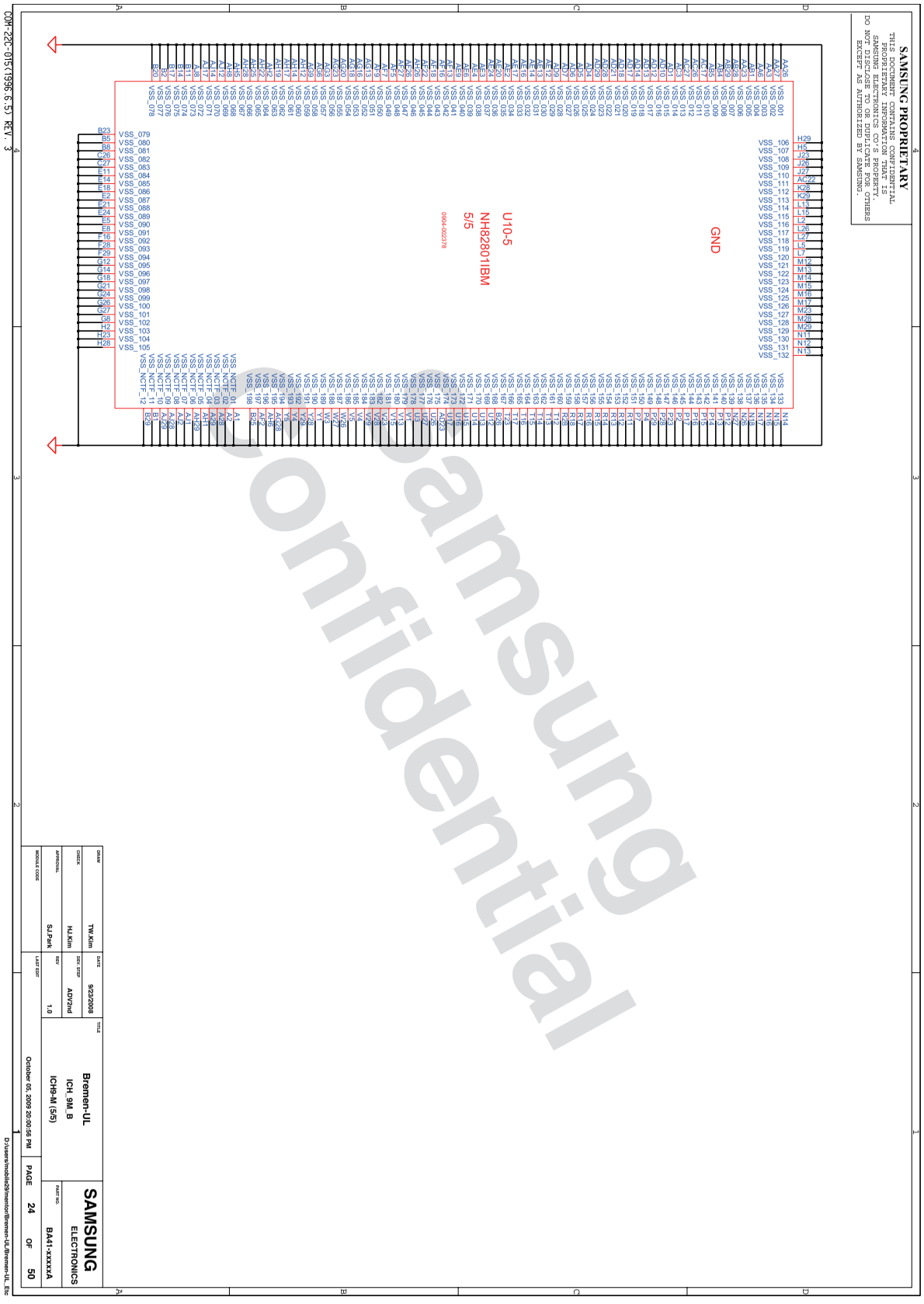
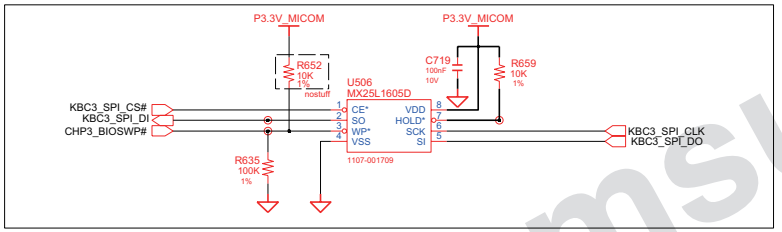


8. Block Diagram and Schematic

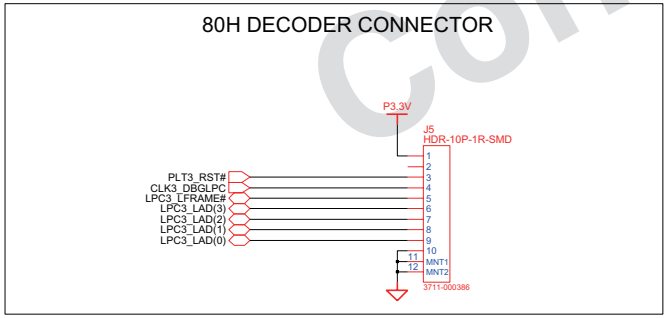


SPI_BIOS_ROM

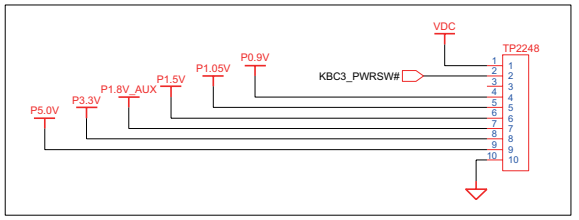
16MBit



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG.	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
OE	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
	WITH INITIAL POST VALUE	8A	INIT.EXTENDED BIOS DATA AREA
14	INIT. KEYBOARD CONTROLLER	8C	INIT. FDD CONTROLLER
16	CHECK CHECKSUM	9A	SHADOW OPTION ROMS
18	8254 TIMER INIT	9C	SETUP POWER MANAGEMENT
1A	8237 DMA CONTROLLER INIT.	9E	ENABLE H/W INTERRUPT
1C	RESET INTERRUP CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT. TYPEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ENTER SETUP
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
32	COMPUTE THE CPU SPEED	B0	CHECK FOR ERRORS
34	TESET CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
38	SHADOW SYSTEM BIOS ROM	B4	ONE BEEP
3A	AUTO SIZING CACHE	B6	CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	B7	ACPI INIT
3D	LOAD ALTER REG. WITH CMOS VALUE	BA	DMI INIT
42	INIT. INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT. BIOS INTERRUPT	C0	TRY BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT. I20 SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D6	SHUTDOWN 5
4A	INIT. ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	SHUTDOWN 10
52	TEST KEYBOARD	89	ENABLE NMI
54	SET KEYCLICK IF ENABLED	90	INIT. HDD CONTROLLER
56	ENABLE KEYBOARD	91	INIT. LOCAL BUS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 2
5A	DISPLAY " PRESS ..... SETUP"	94	DISABLE A20 ADDRESS LINE
5C	TEST RAM BETWEEN 512K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
60	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PATCH 1		



80port will be removed in MP stage.



TP for ICT free

DRAW	TW.Kim	DATE	9/23/2008	TITLE: Bremen-UL
CHECK	HJ.Kim	DEV. STEP	ADV2nd	SPI_BIOS_ROM
APPROVAL	SJ.Park	REV	1.0	SPI_BIOS_ROM & ICT FREE TP
MODULE CODE		LAST EDIT	October 05, 2009 20:00:56 PM	PAGE 25 OF 50

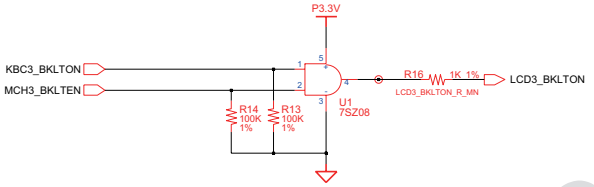
SAMSUNG ELECTRONICS
PART NO. BA41-xxxxxA

COM-22C-015(1996.6.5) REV. 3

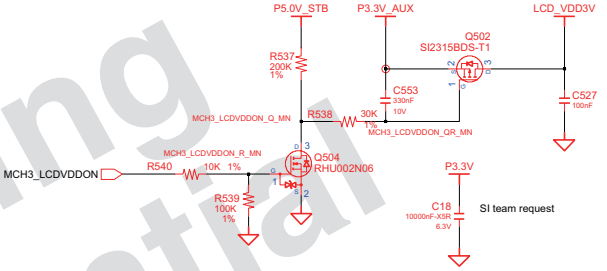
D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

LVDS

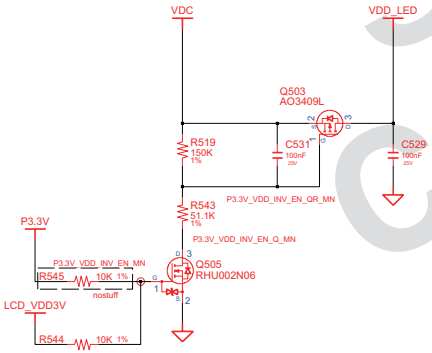
Backlight On



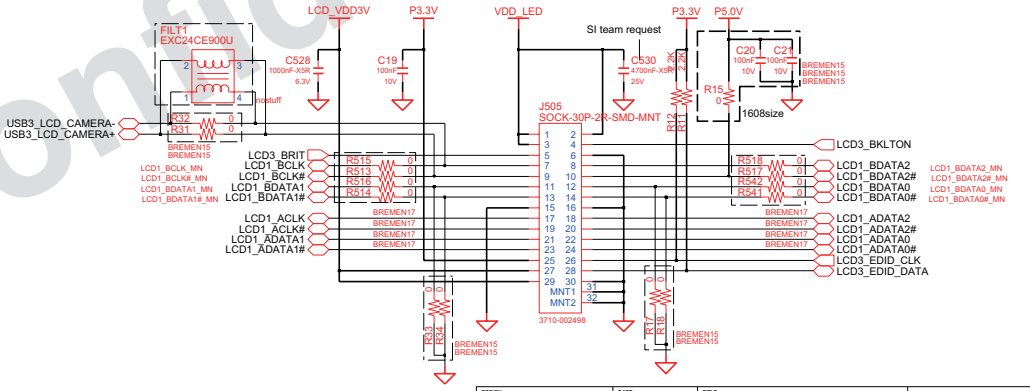
LCD Power EBL Purpose



LED Power



Camera + LCD Connector



DESIGN: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL GRAPHICS_IF LVDS	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd		
APPROVAL: SJ.Park	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 26 OF 50	

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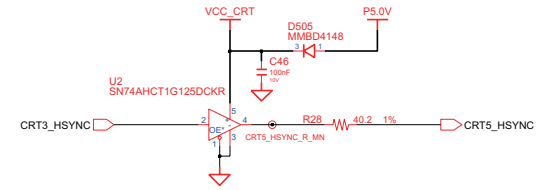
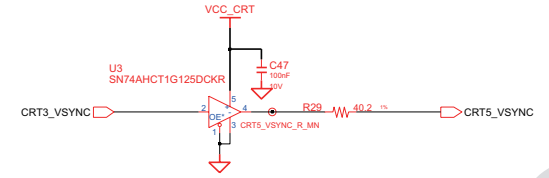
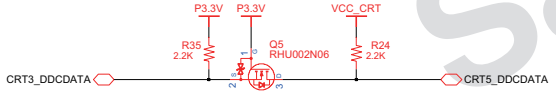
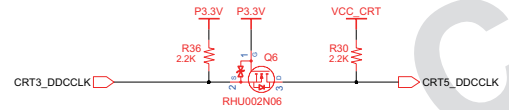
D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

CRT

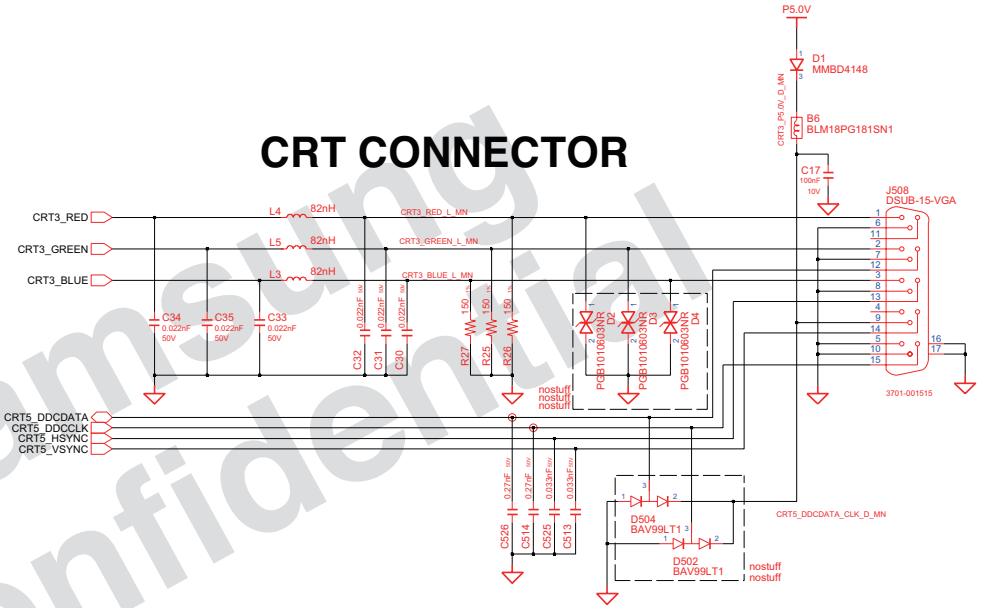








CRT CONNECTOR



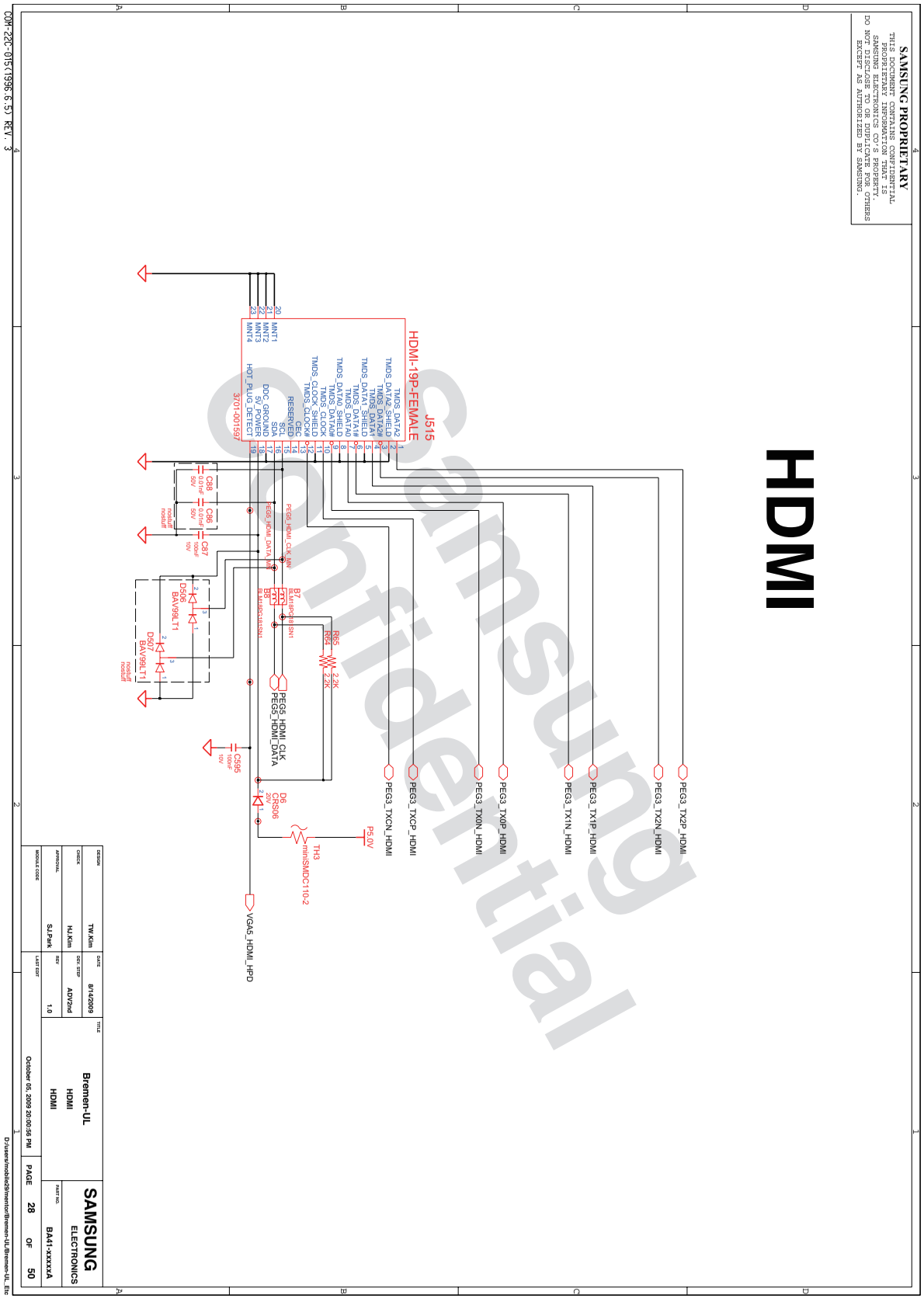
Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DESIGN: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL GRAPHICS_IF CRT	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd		PART NO.: BA41-xxxxxA
APPROVAL: SJ.Park	REV: 1.0		
MODULE CODE:	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 27 OF 50	

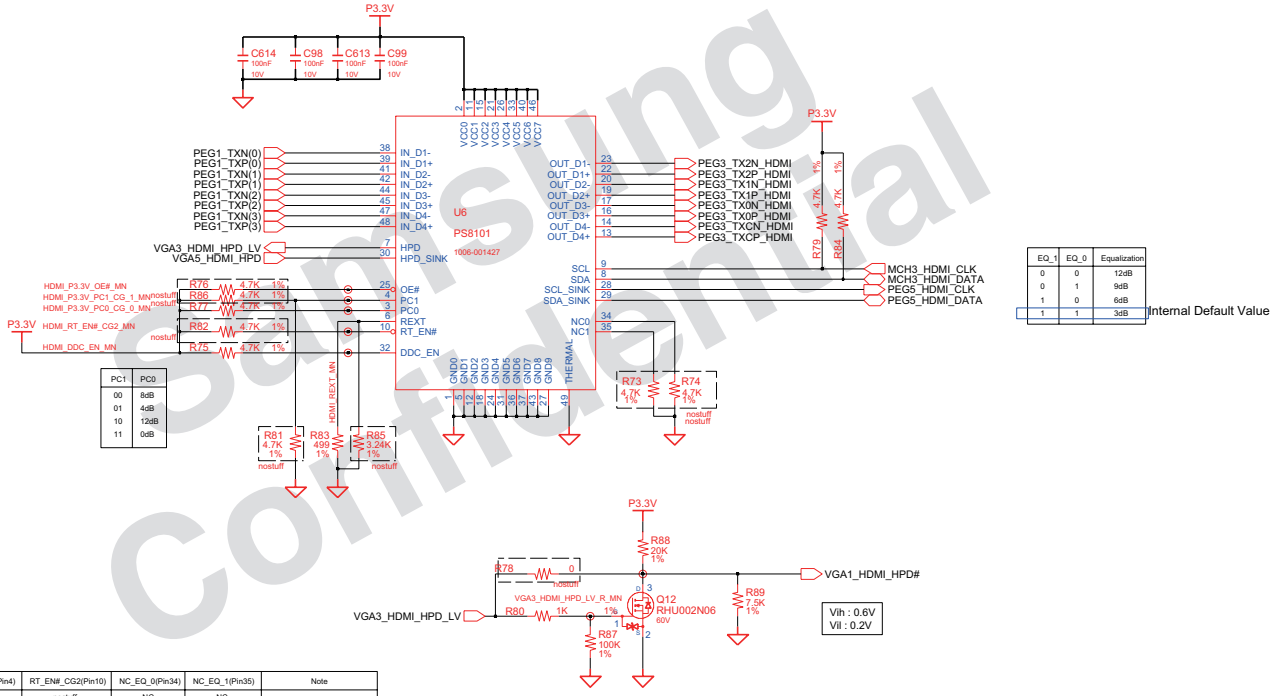
COM-22C-015(1996.6.5) REV. 3

D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

8. Block Diagram and Schematic



HDMI Level Shifter for Int. Graphic only



CG_2	CG_1	CG_0	Swing	Pre-amp	Slew rate
0	0	0	450mV	0dB	0dB
0	0	1	490mV	0dB	-3dB
0	1	0	450mV	0dB	-3dB
0	1	1	460mV	0dB	-4dB
1	0	0	340mV	0dB	0dB
1	0	1	400mV	2dB	0dB
1	1	0	400mV	2dB	0dB
1	1	1	420mV	0dB	0dB

PC1	PC0
00	8dB
01	4dB
10	12dB
11	0dB

EQ_1	EQ_0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB

HDMI Level Shifter	REXT(Pin6)	PC1_CG0(Pin3)	PC1_CG1(Pin4)	RT_EN#_CG2(Pin10)	NC_EQ_0(Pin34)	NC_EQ_1(Pin35)	Note
PS8101	499 phm	stuff	nostuff	nostuff	NC	NC	
ASM1442	3.4K(3.24~3.3K)	nostuff	nostuff	nostuff	nostuff	nostuff	Internal PU/PD exist CGs nostuff is 450mV swing

DESIGN: TW.Kim	DATE: 8/14/2009	TITLE: Bremen-UL / HDMI / HDMI level shifter	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd		PART NO.: BA41-xxxxxA
APPROVAL: SJ.Park	REV: 1.0		
MODULE CODE:	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 29 OF 50	

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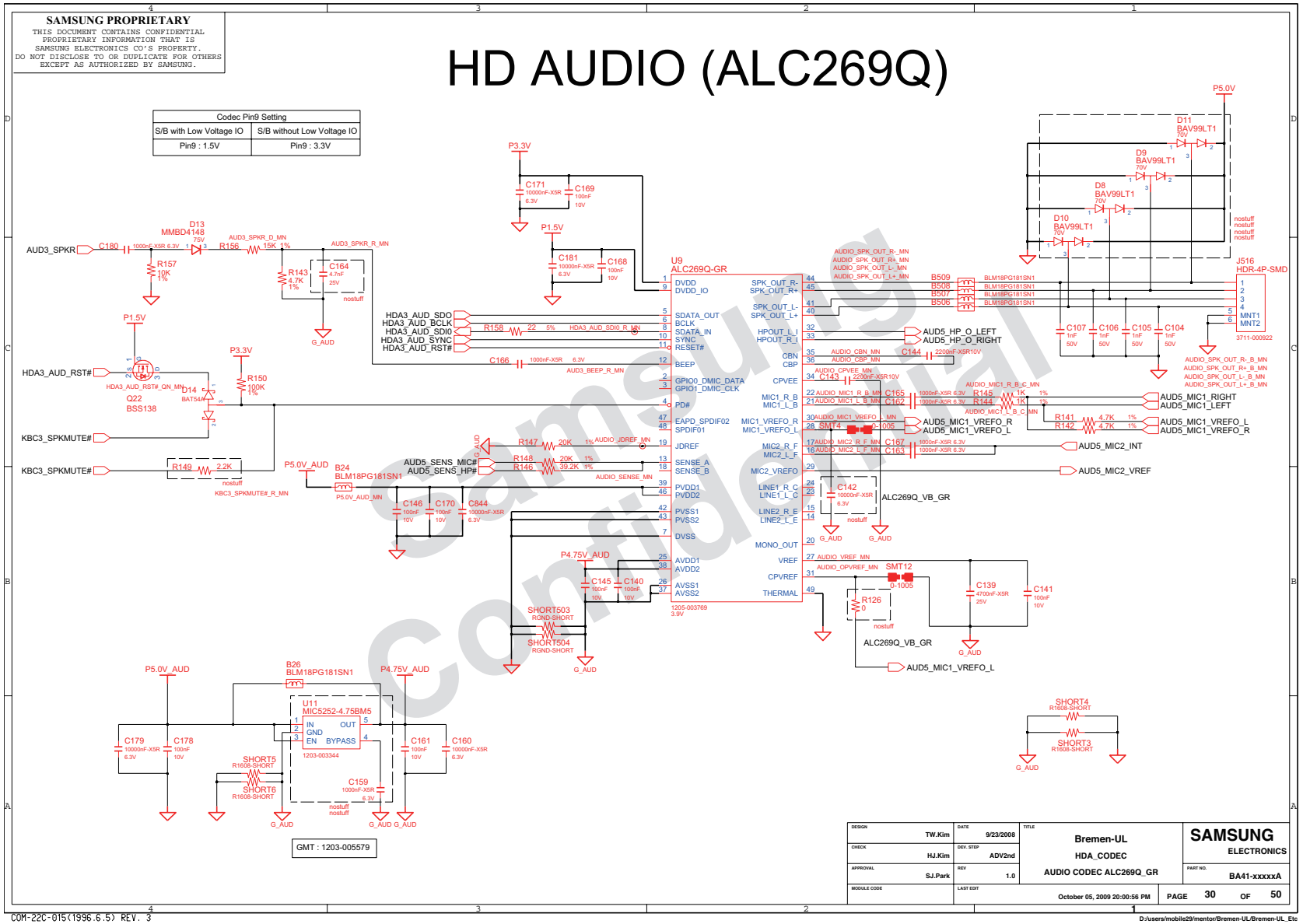
HD AUDIO (ALC269Q)

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

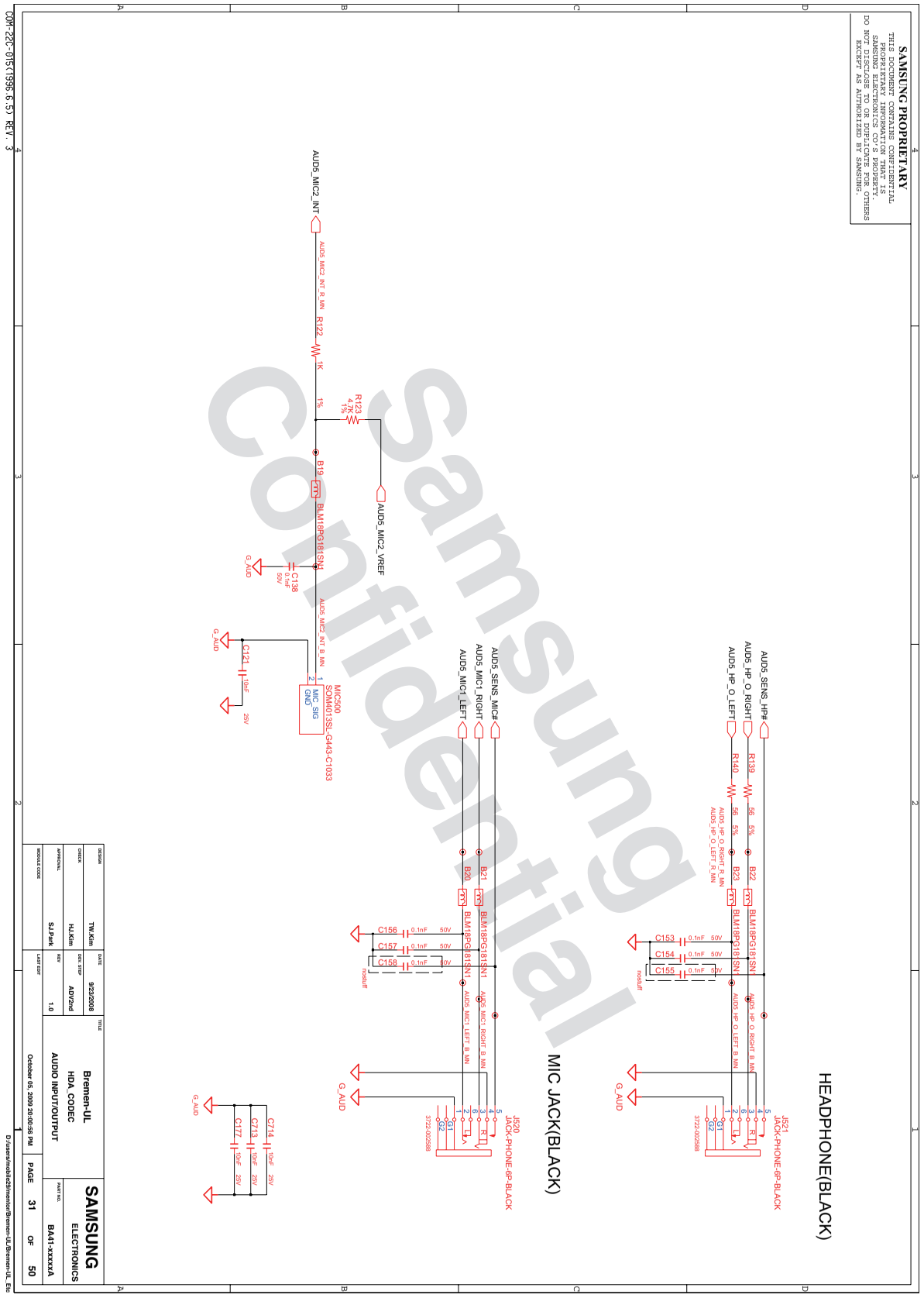


DESIGN: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd	HDA_CODEC	
APPROVAL: SJ.Park	REV: 1.0	AUDIO CODEC ALC269Q_GR	PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 30 OF 50	

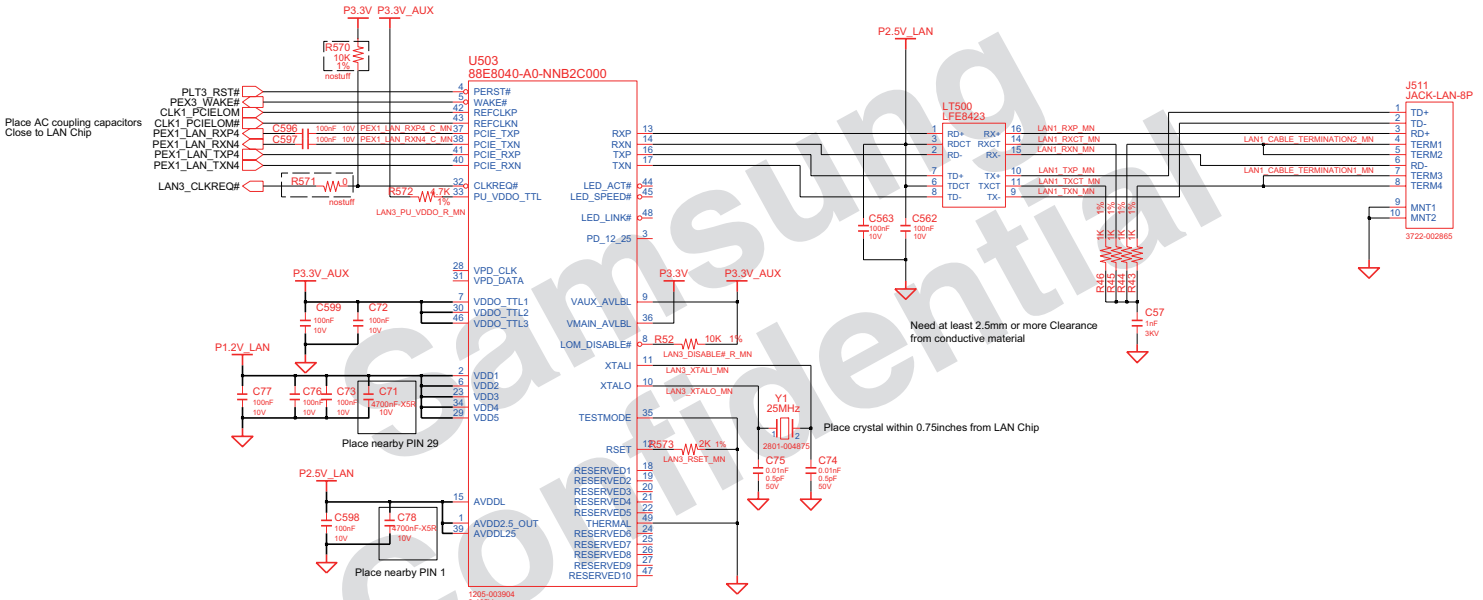
COM-22C-015(1996.6.5) REV. 3

D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

8. Block Diagram and Schematic



LAN Controller (88E8040)



DESIGN: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd	LAN	
APPROVAL: SJ.Park	REV: 1.0	LAN_MARVELL_8040	PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 32 OF 50	

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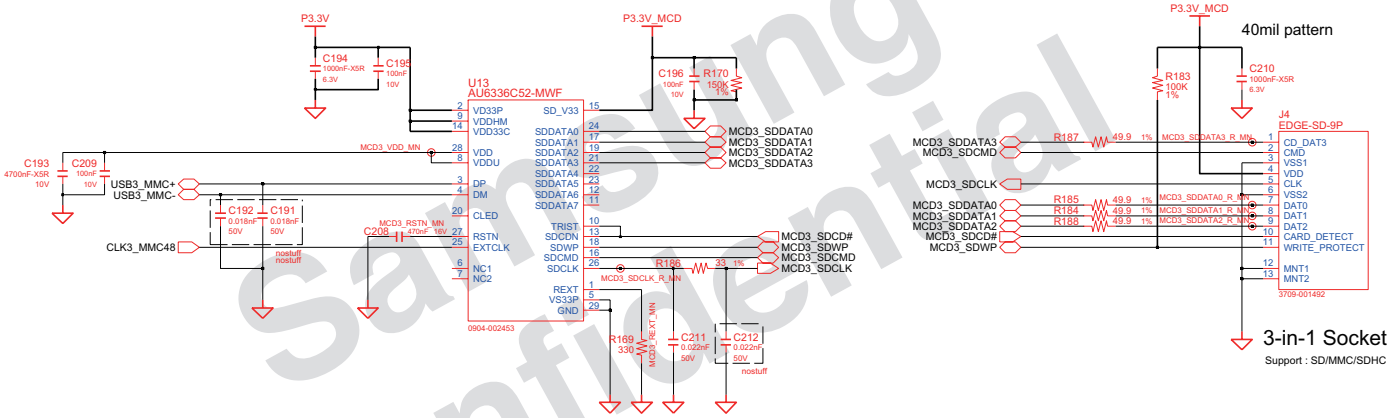
D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

3 IN 1 CARD (GL827S)



DESIGN: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL MULTICARD 3 IN 1 CARD	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd		
APPROVAL: SJ.Park	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 33 OF 50	

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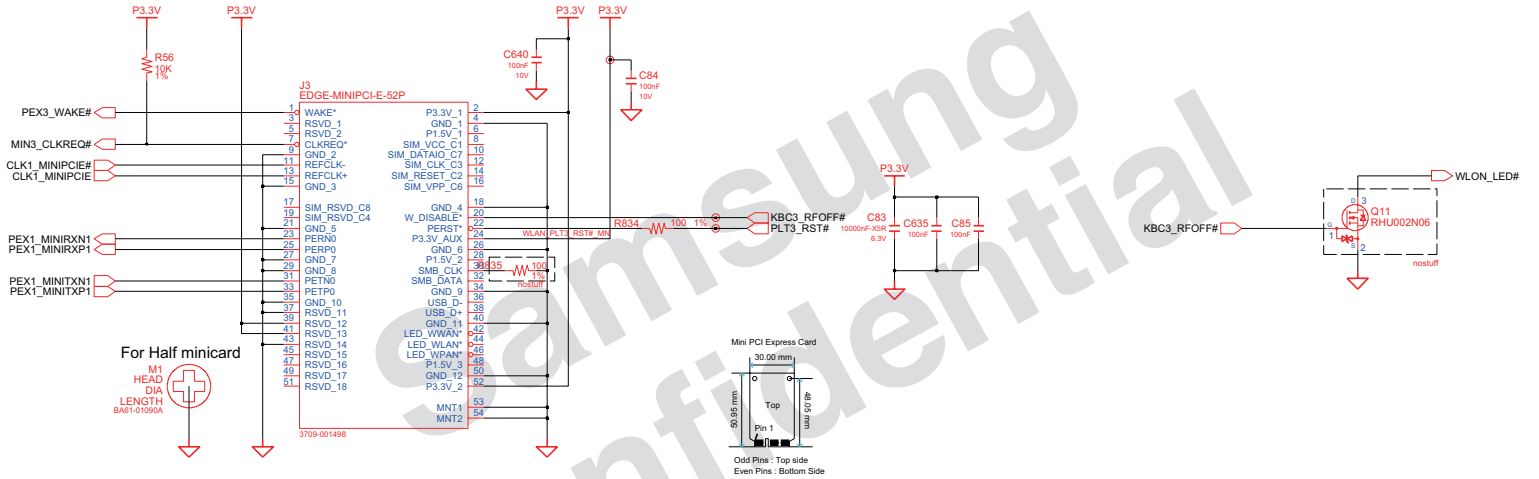
D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

Wireless LAN

WLAN, 4mm



DESIGN: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd	MINI_PCIE_CONN	
APPROVAL: SJ.Park	REV: 1.0	WLAN	PART NO.: BA41-xxxxxA
MODULE CODE	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 34 OF 50	

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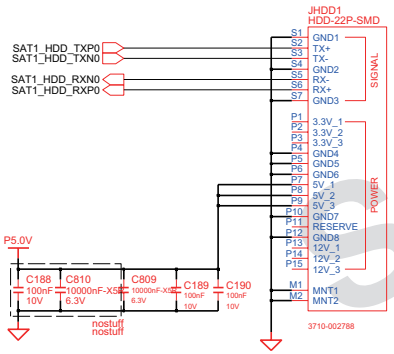
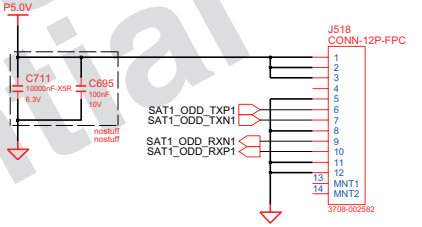
SATA I/F CONN

SATA HDD CONN



MAIN TO SUB SATA ODD CONN



DESIGN: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd	SATA_DEVICES	
APPROVAL: SJ.Park	REV: 1.0	HDD & ODD SUB CONNECTOR	PART NO.: BA41-xxxxxA
MODULE CODE	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 35 OF 50	

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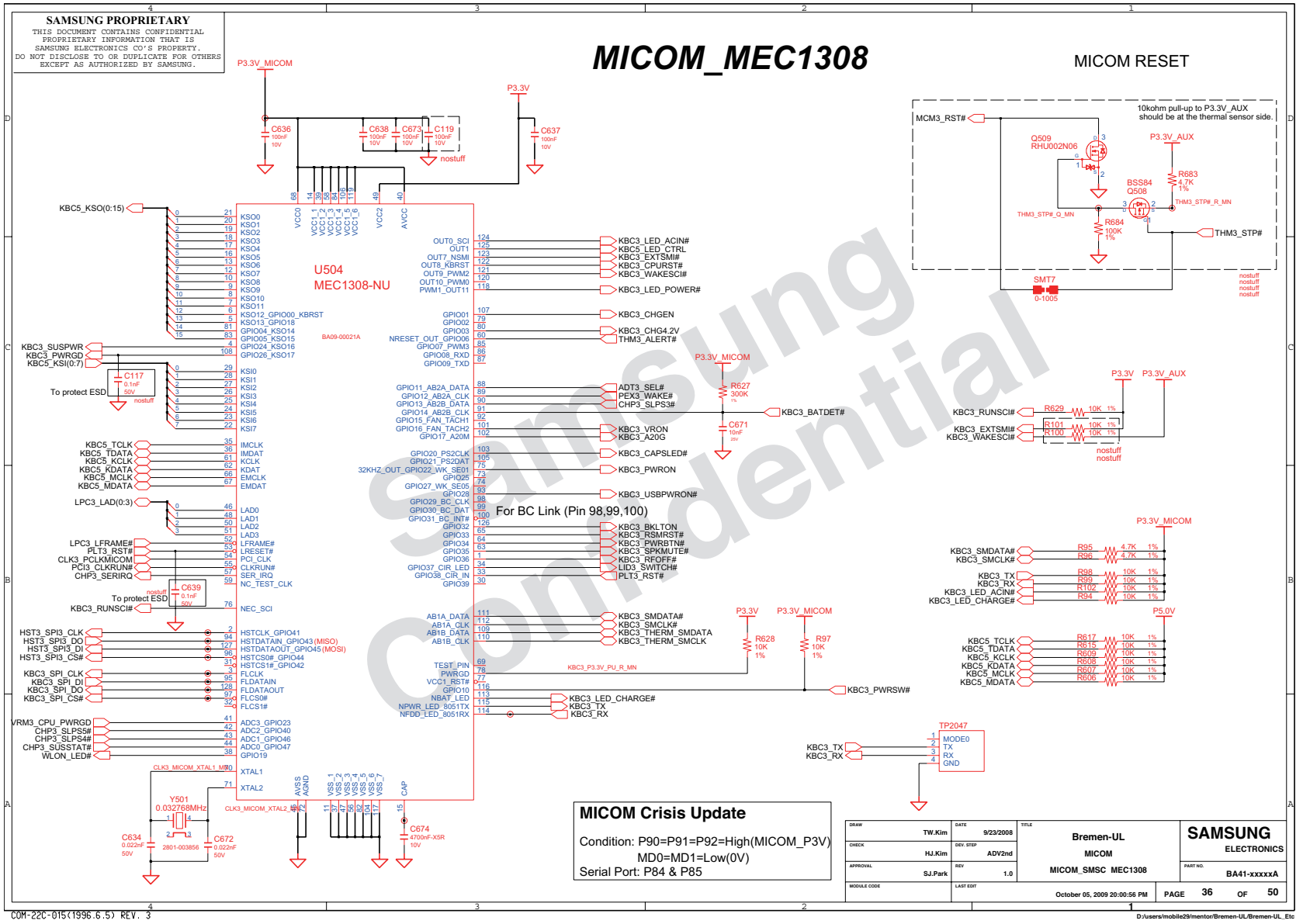
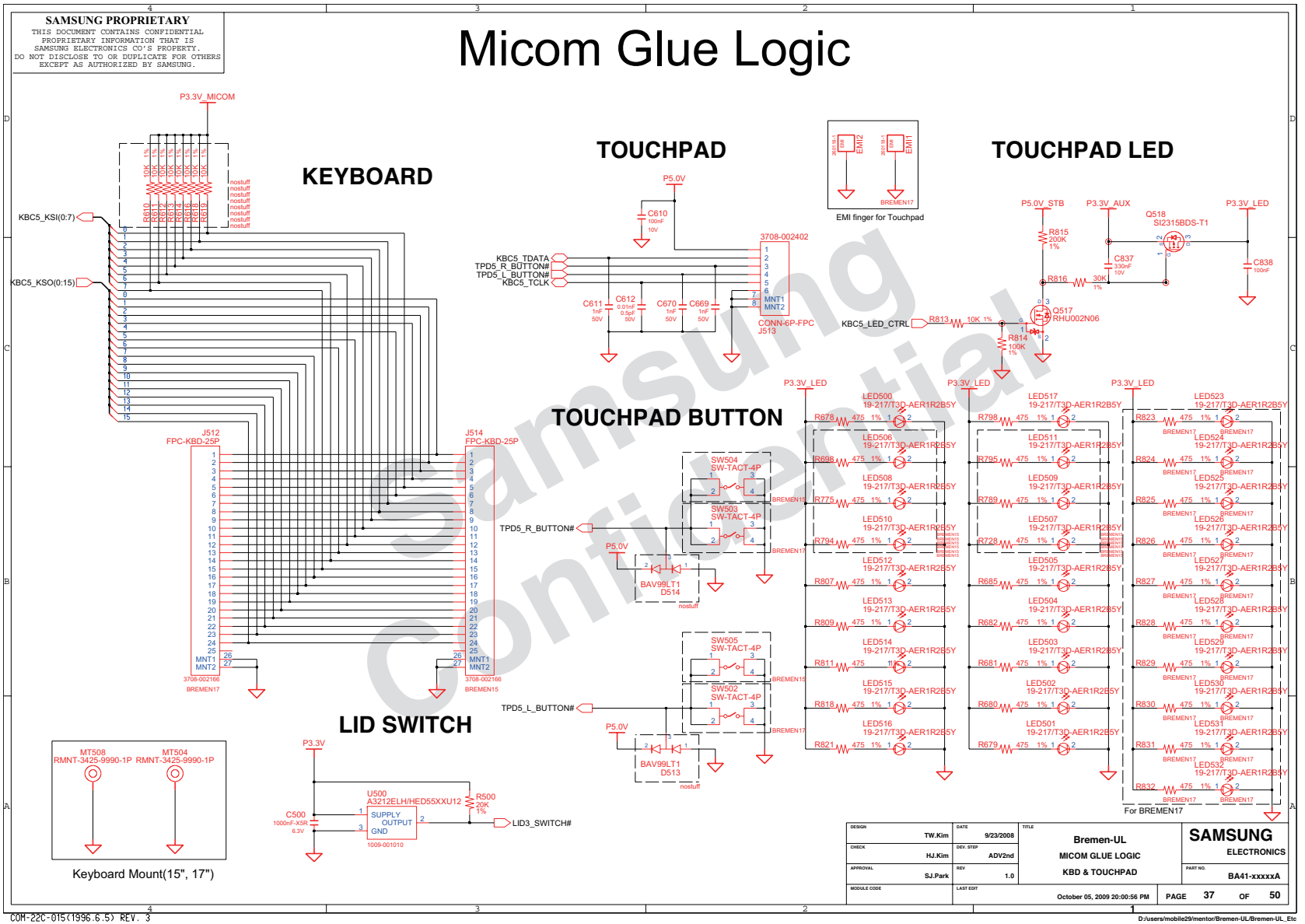
D:/users/mobile29/mentor/Bremen-UL/Bremen-UL_Etc

8. Block Diagram and Schematic



Micom Glue Logic



DESIGN: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd	MICOM GLUE LOGIC	
APPROVAL: SJ.Park	REV: 1.0	KBD & TOUCHPAD	PART NO.: BA41-xxxxxA
MODULE CODE	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 37 OF 50	

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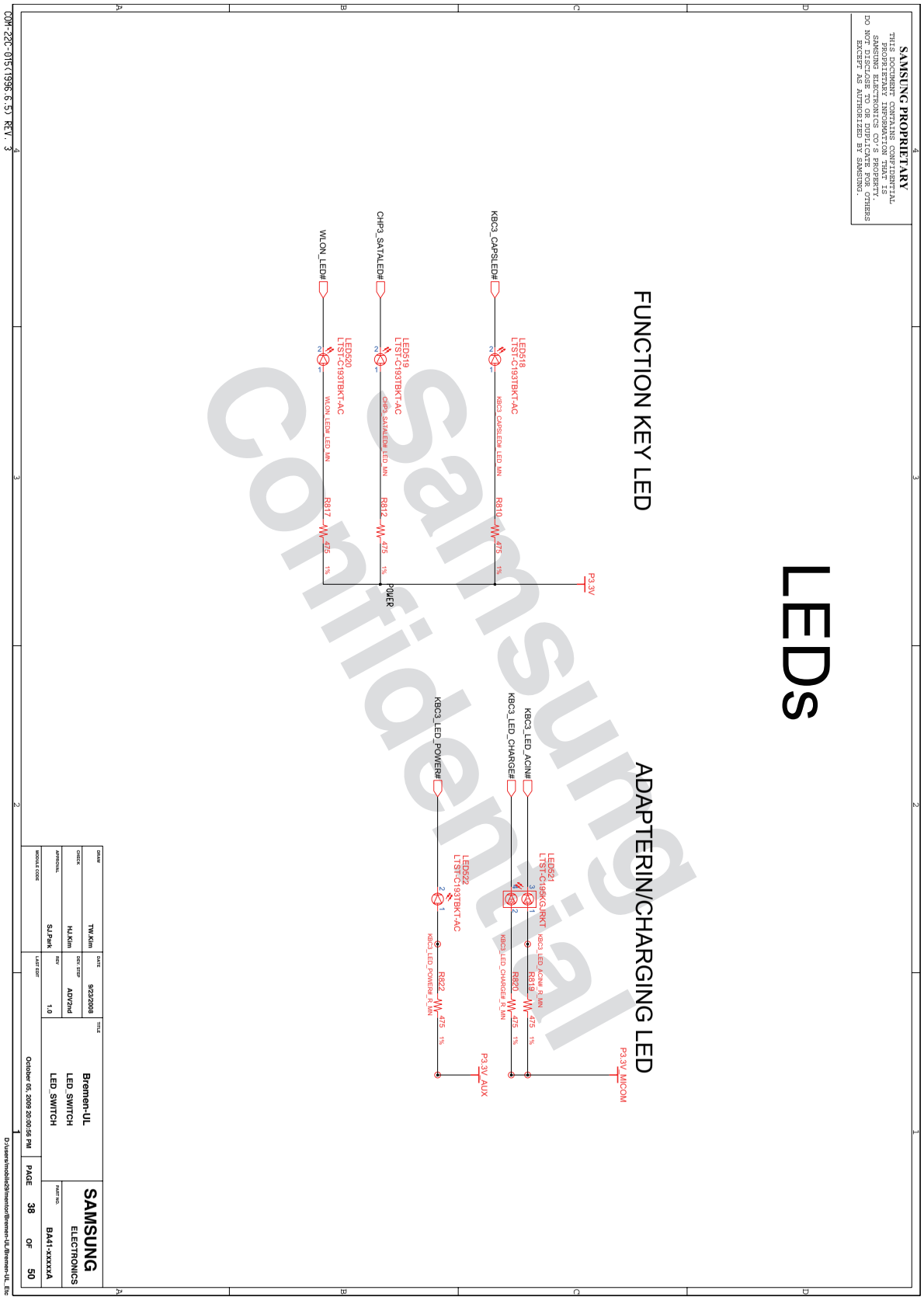
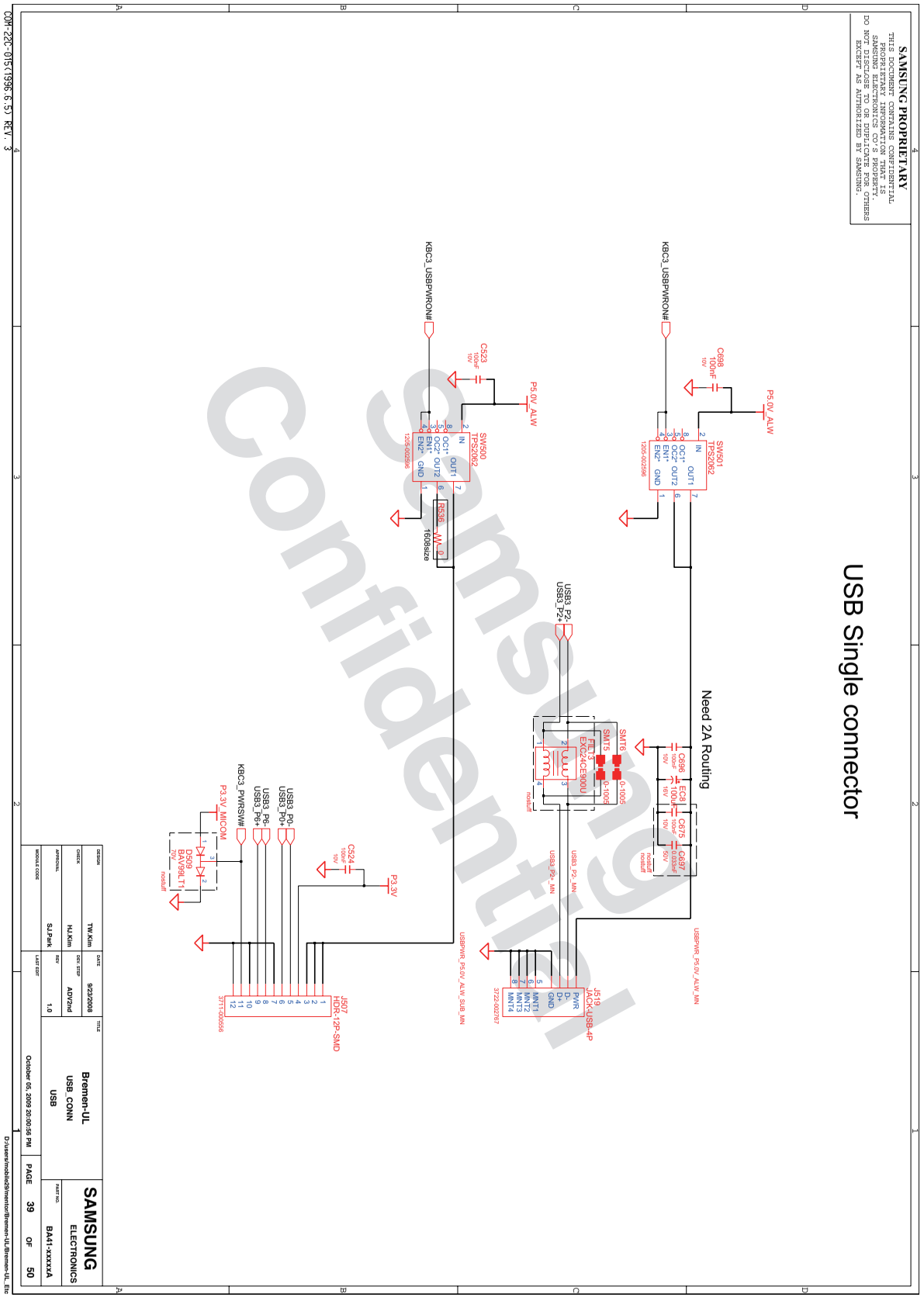
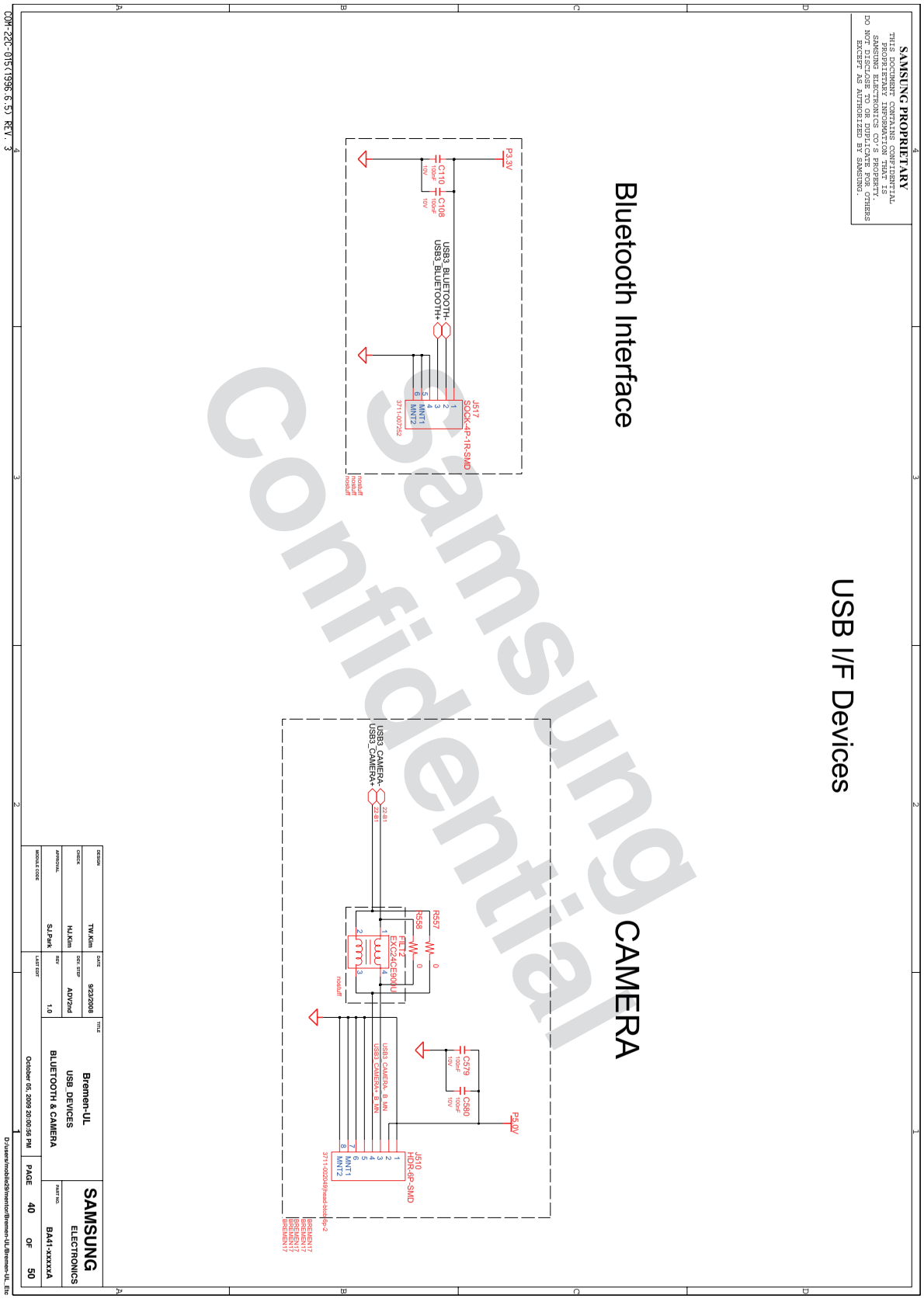
8. Block Diagram and Schematic



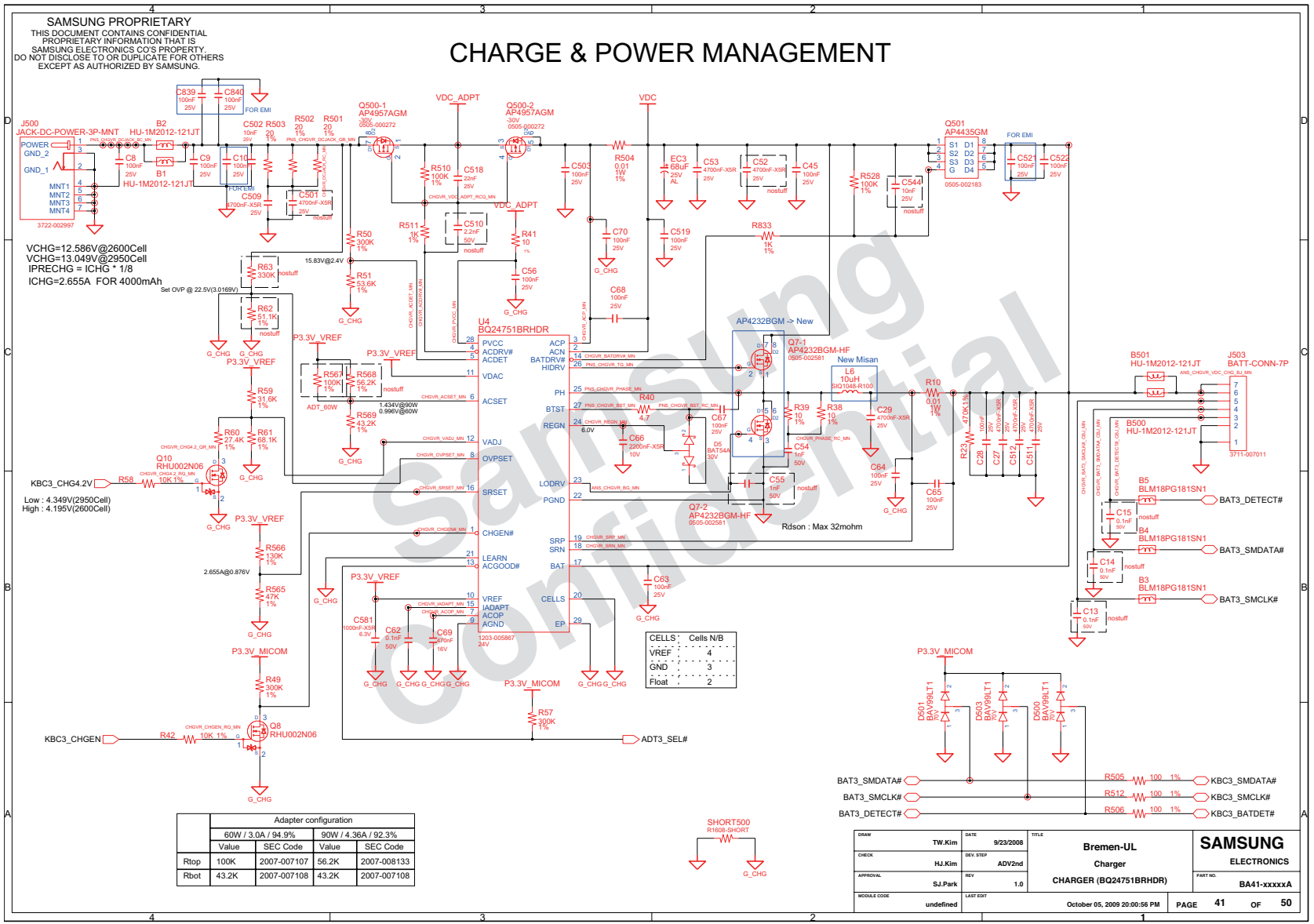
8. Block Diagram and Schematic



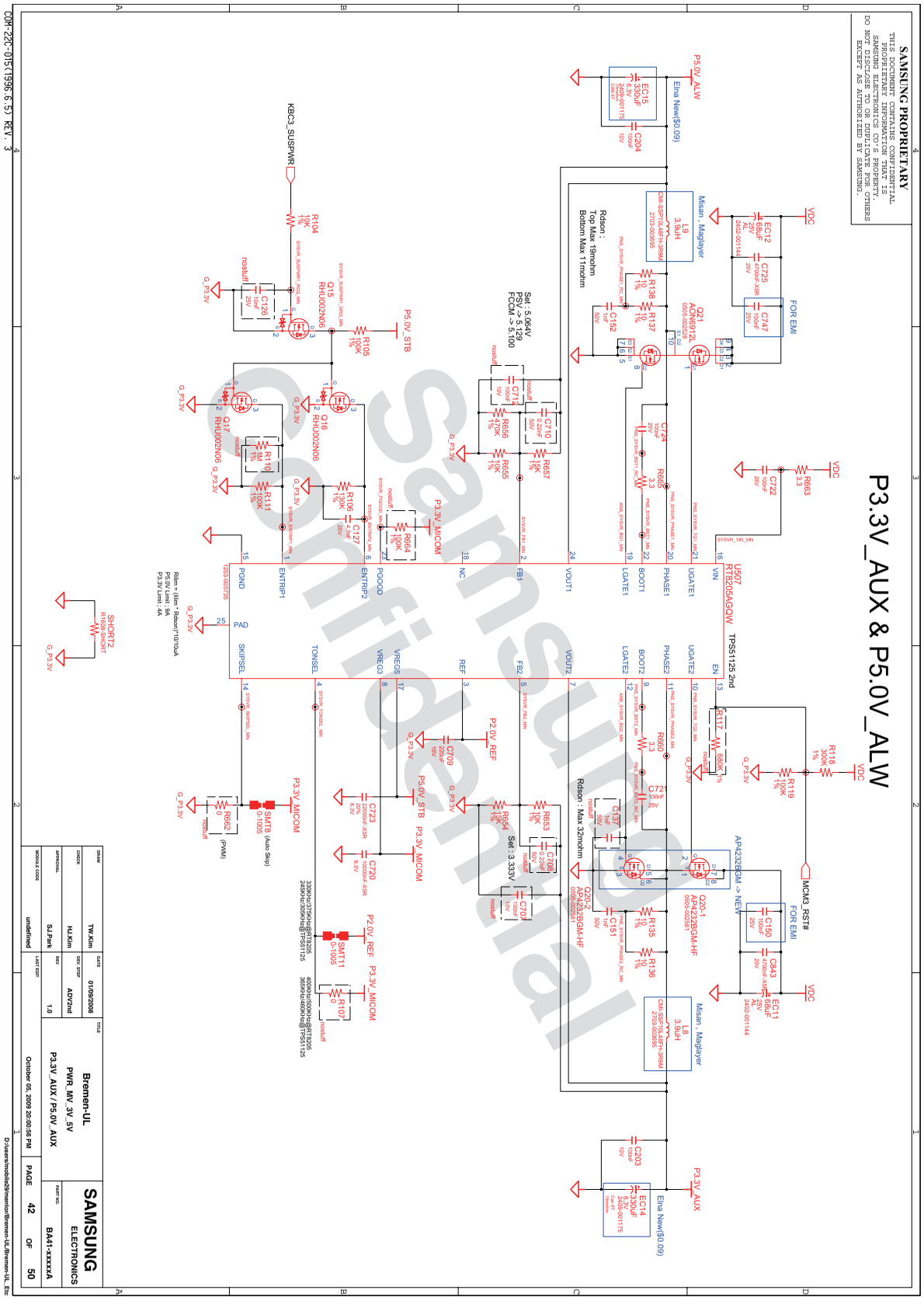
8. Block Diagram and Schematic



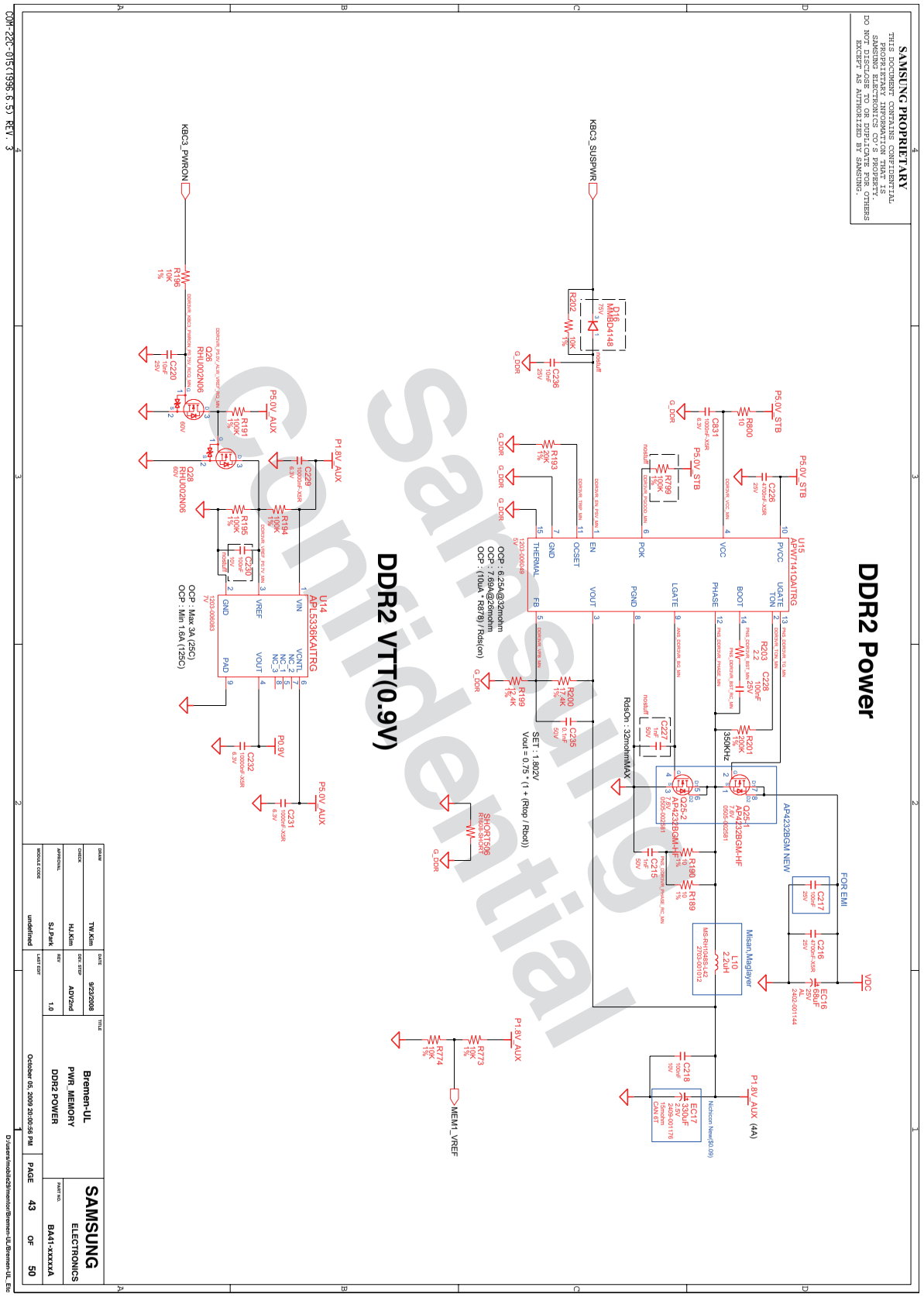
8. Block Diagram and Schematic



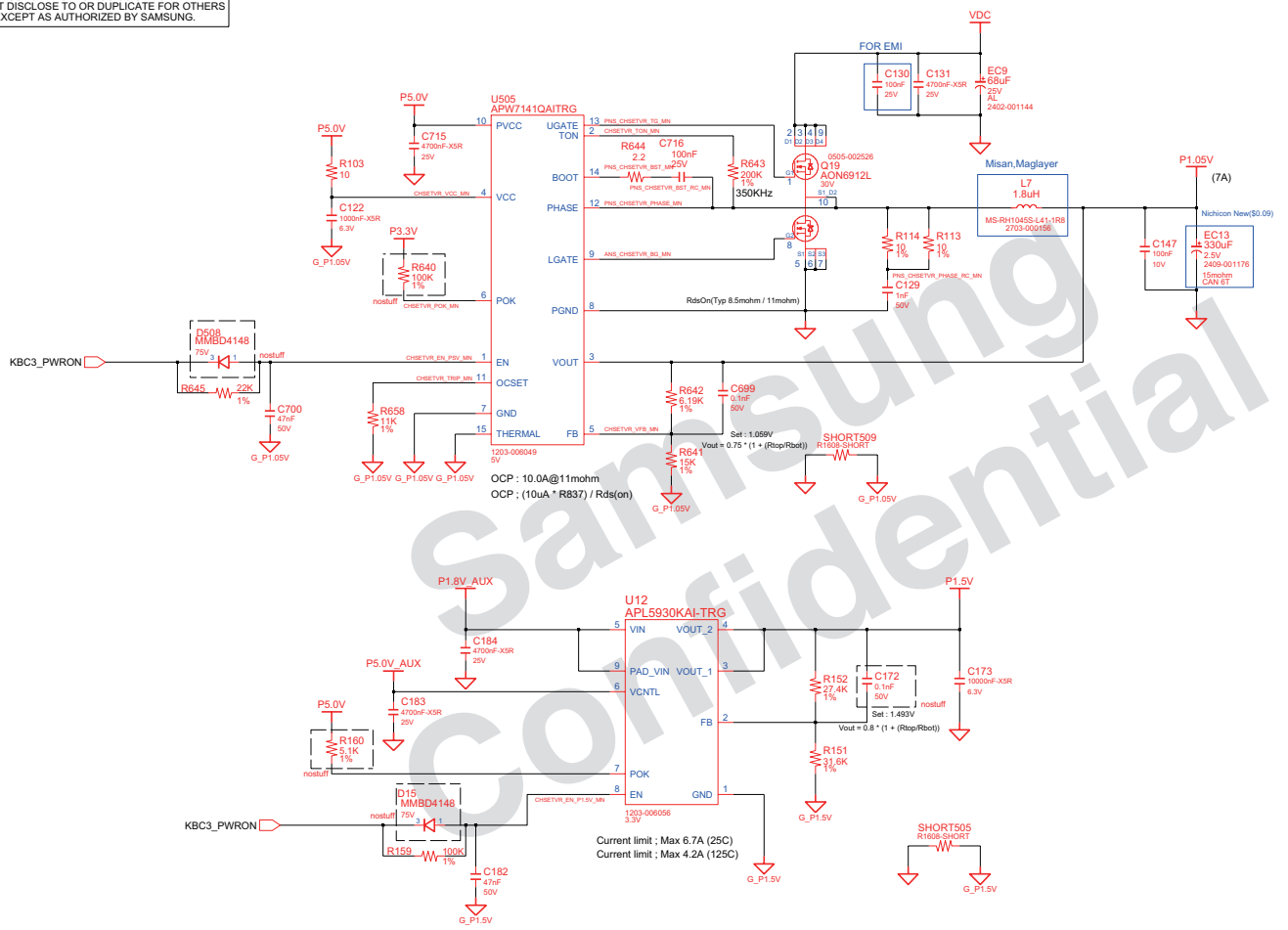
8. Block Diagram and Schematic



8. Block Diagram and Schematic



CHIPSET POWER (P1.05V& P1.5V)



DRAW TW.Kim	DATE 9/23/2008	TITLE Bremen-UL	SAMSUNG ELECTRONICS
CHECK HJ.Kim	DEV. STEP ADV2nd	PWR_MV_Cantiga	
APPROVAL SJ.Park	REV 1.0	P1.5V_AUX, P1.05V	PART NO. BA41-xxxxxA
MODULE CODE undefined	LAST EDIT October 05, 2009 20:00:56 PM	PAGE 44 OF 50	

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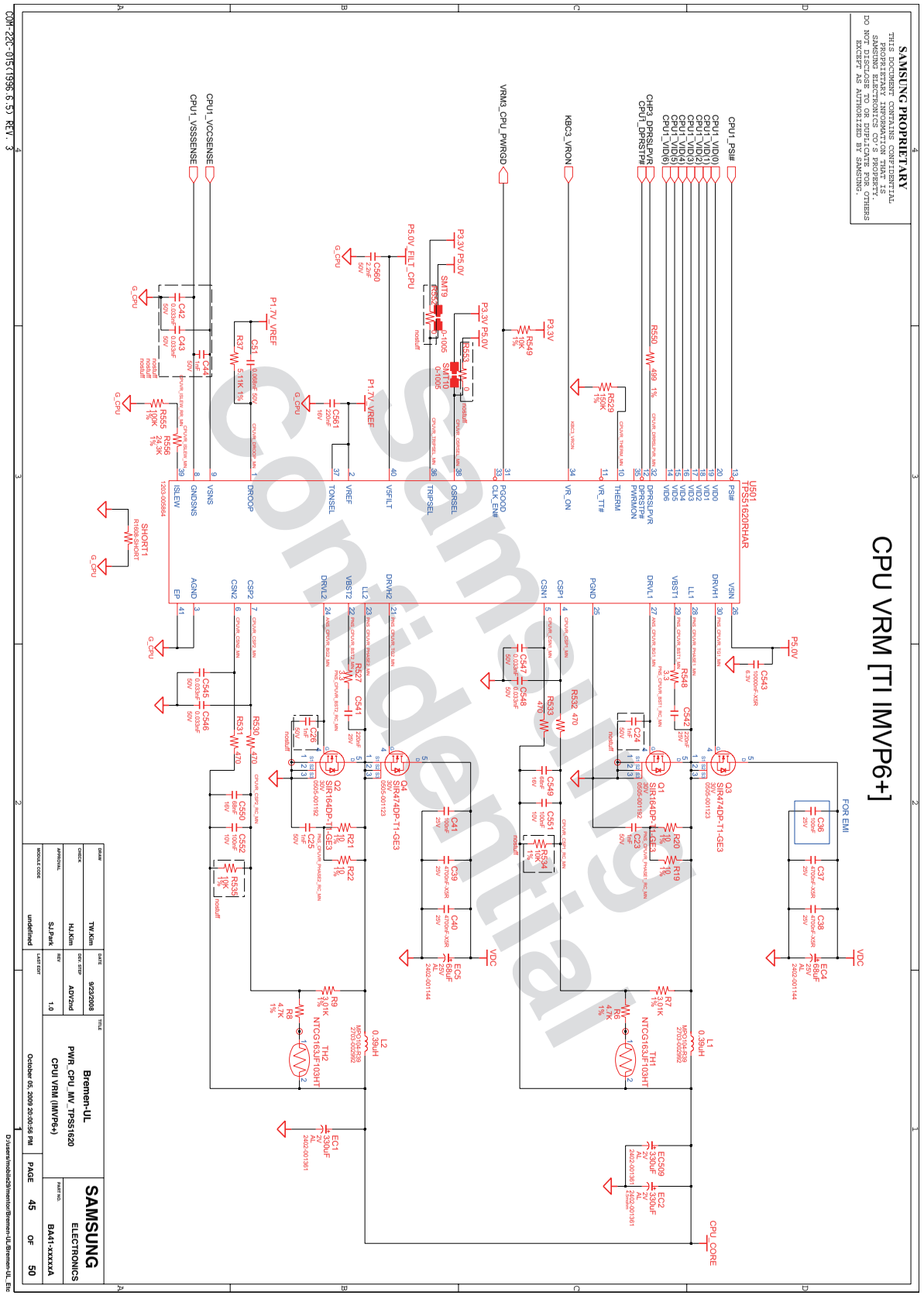
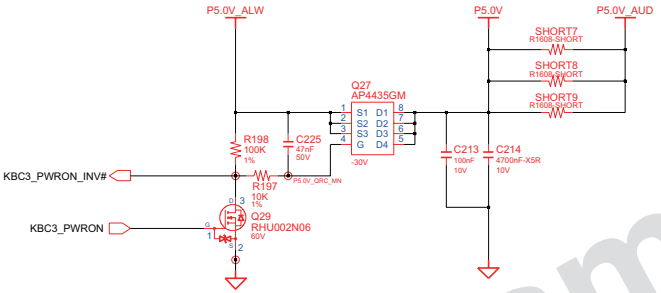
8. Block Diagram and Schematic

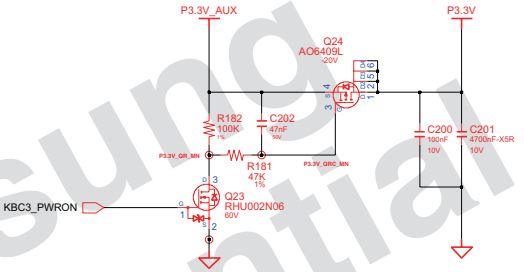


Switched Power

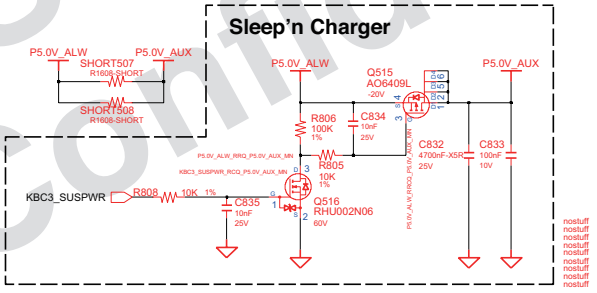
Switched Power On (P5.0V)



Switched Power On (P3.3V)



Sleep'n Charger



DRAW: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd	PWR_MV_SWITCHED	
APPROVAL: SJ.Park	REV: 1.0	SWITCHED POWER	PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 46 OF 50	

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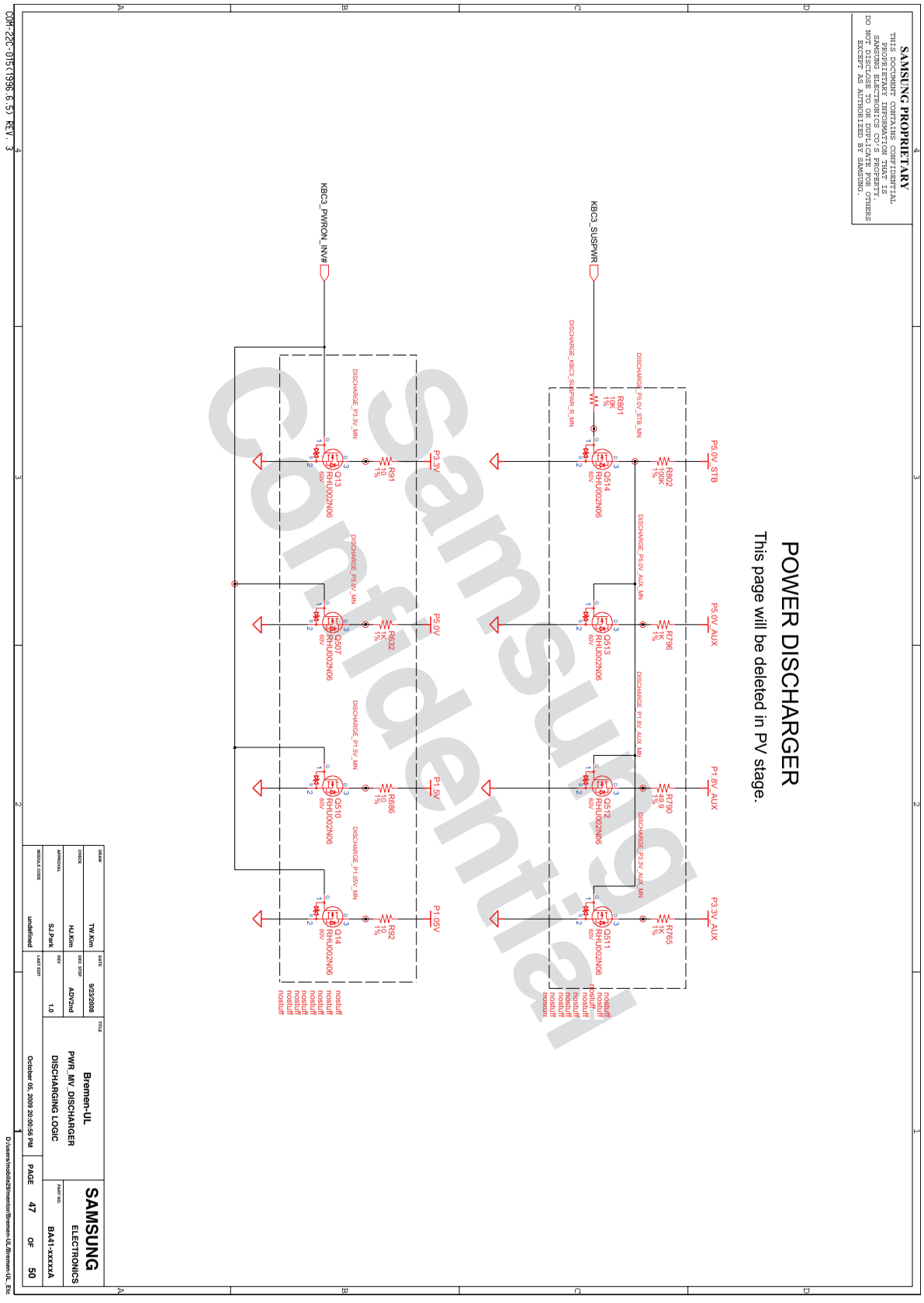
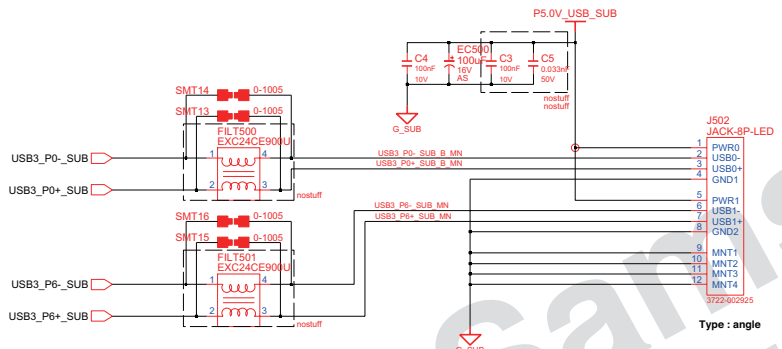
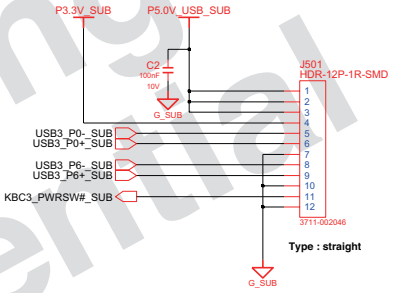
8. Block Diagram and Schematic



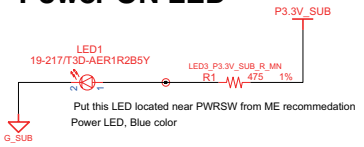
2 USB PORT & POWER S/W SUB B'D



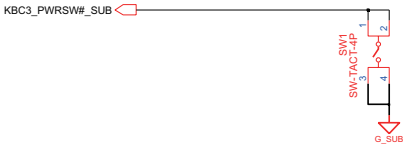
SUB TO MAIN USB CONN

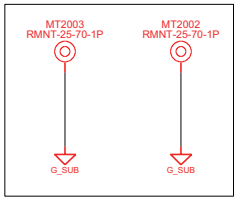


Power ON LED



Power Button





USB sub board mount hole

DESIGN: TW.Kim	DATE: 8/22/2009	TITLE: Bremen-UL	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd	SUB BOARD1	
APPROVAL: SJ.Park	REV: 1.0	USB SUB BOARD	PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 48 OF	

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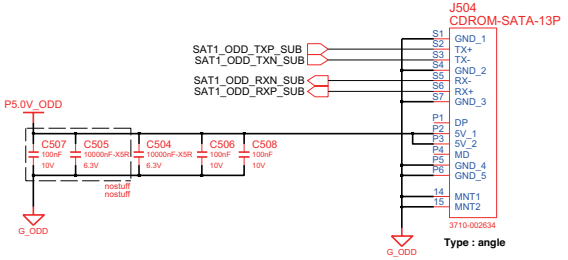
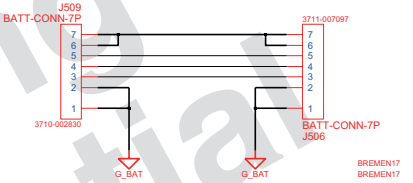
SATA ODD SUBBOARD

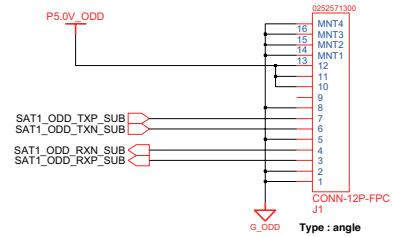
BATTTERY SUBBOARD (17")

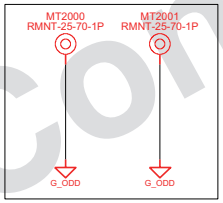
SATA ODD CONN



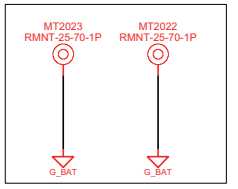


SUB TO MAIN SATA ODD CONN





ODD sub board mount hole



battery sub board mount hole

DRAW: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd	SUB BOARD2	
APPROVAL: SJ.Park	REV: 1.0	SATA ODD SUB BOARD	PART NO.: BA41-xxxxxA
MODULE CODE: undefined	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 49 OF 50	

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8. Block Diagram and Schematic