

OSLO2

CPU : Intel Penryn-6M (1067/800) MHz
 Chip Set : Intel Cantiga & ICH9M
 Remarks : Montevina Platform

Model Name : Oslo2_DDR3
 PBA Name : MAIN
 PCB Code : BA41-00866A
 BA41-00867A
 Dev. Step : MP
 Revision : 1.1
 T.R. Date : 2008. 05.15

DRAW	CHECK	APPROVAL
MS YANG TH LEE	TH LEE	MK KIM

■ Owner : SEC Mobile R & D Signature : X

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DRAW	MS YANG / Dany Lee	DATE	11/23/2007	TITLE	OSLO2	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		MAIN	
APPROVAL	MK KIM	REV	REV 1.1		COVER	
MODULE CODE		LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	PART NO. BA41-00866A
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BOARD INFORMATION**SCHEMATIC ANNOTATIONS AND BOARD INFORMATION****PCI Devices**

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Marvell LAN (88E8850)
Crystal	12MHz	Multi Card Reader	Alkor AU6371

LCD Pannel Detect (EDID)

Devices	Resolution	PANNEL_DETECT_0
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Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail for DDR (off in S4-S5)
P0.75V	0.75V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-m	Master	-	SMBUS Master
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
MICOM	Master	-	SMBUS Master
Battery	0001011x	16h	Battery
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor (EMC2012)

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 2
1	NC
2	SYSTEM PORT 1
3	Mini Card
4	Express Card
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	Multi Card Reader (7-in-1)
11	NC

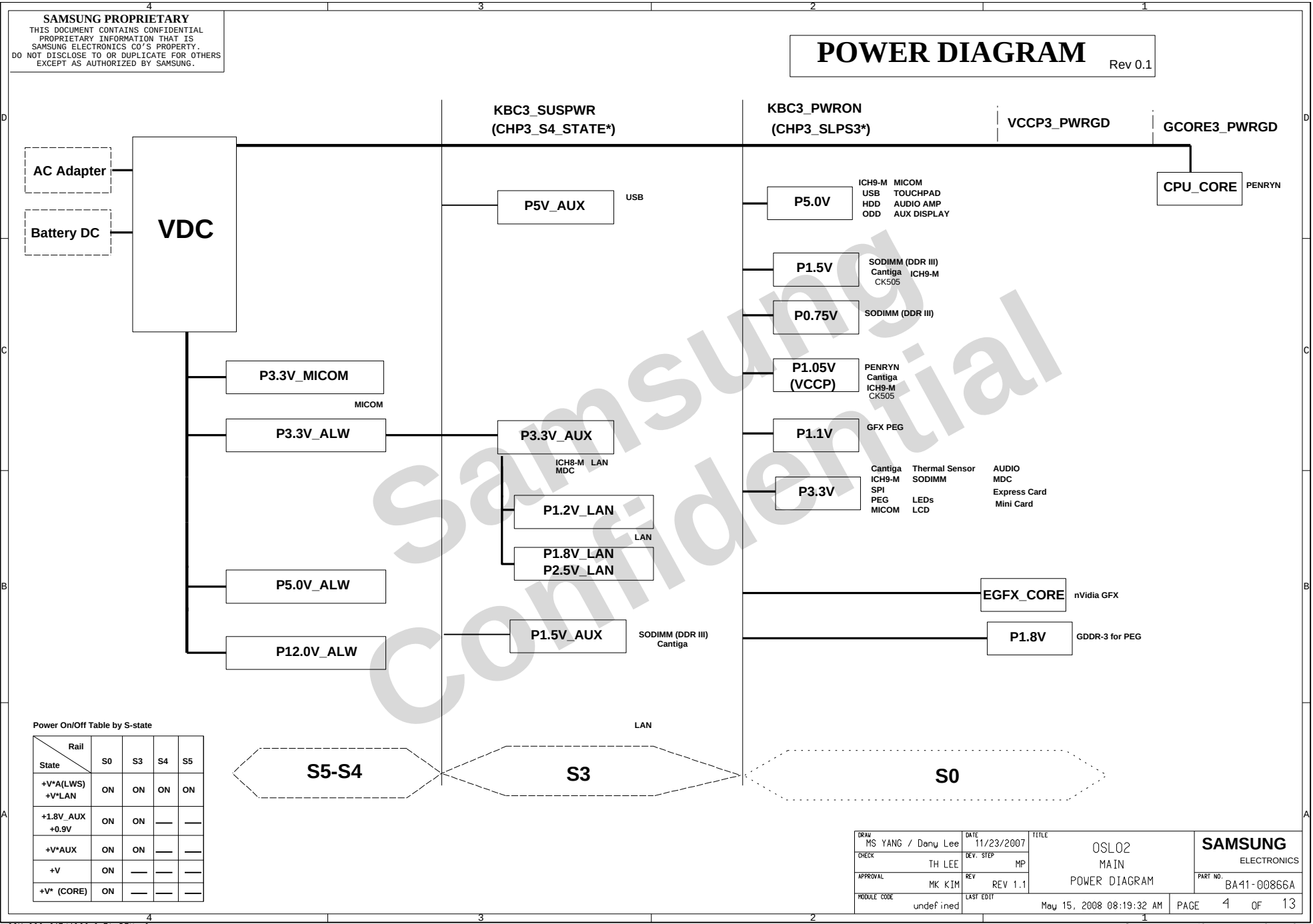
PCI Express Assign

PORT #	ASSIGNED TO
1	Mini Card 1 (WLAN)
2	Mini Card 2 (ROBSON or DVB-T)
3	Express Card
4	LOM
5	NC
6	NC

REVISION HISTORY

See rev notes for more information.

DRAW MS YANG / Dany Lee	DATE 11/23/2007	TITLE OSLO2 MAIN BOARD INFO	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE undefined	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 3 OF 13	

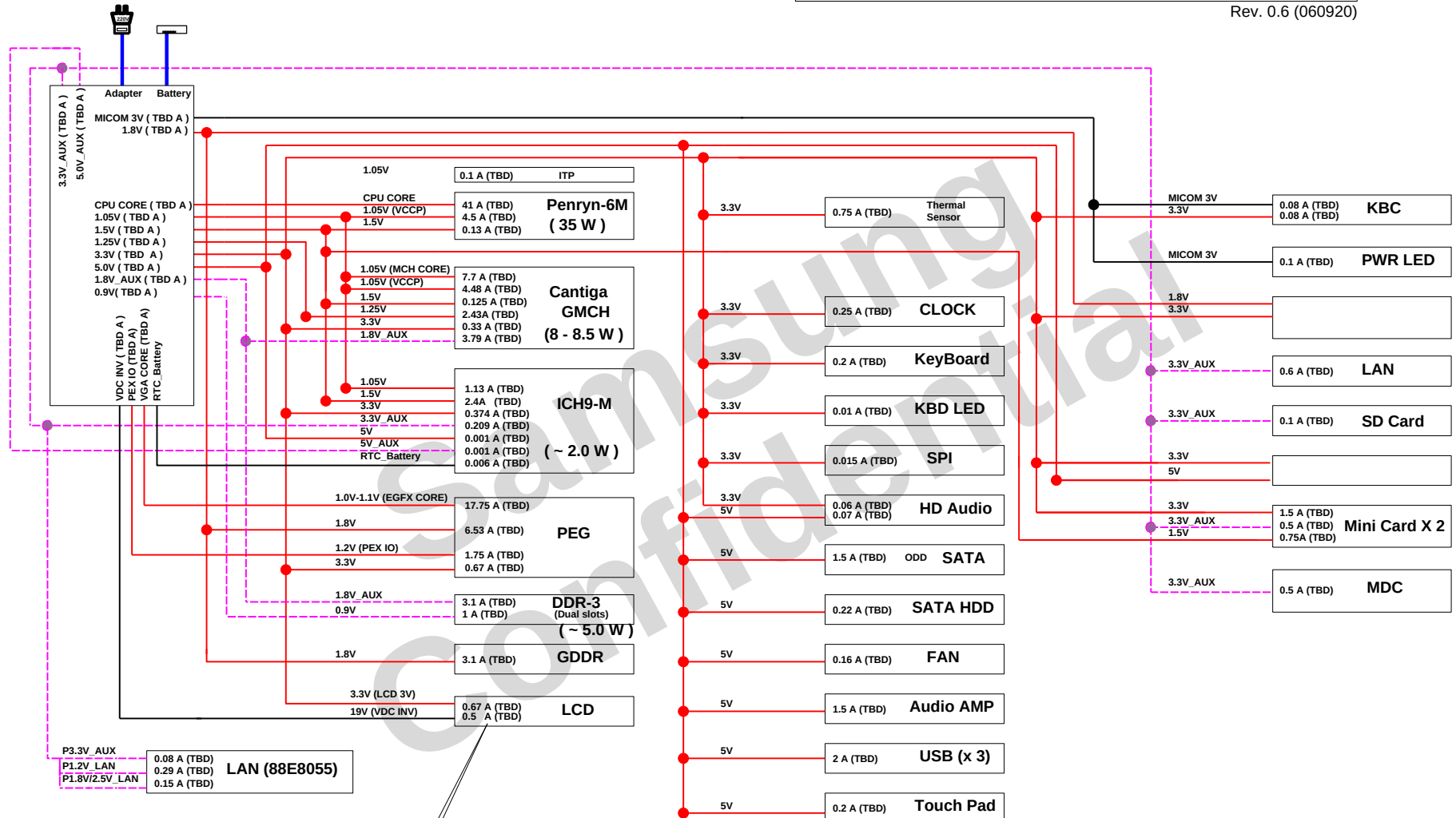


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POWER RAILS ANALYSIS

Rev. 0.6 (060920)

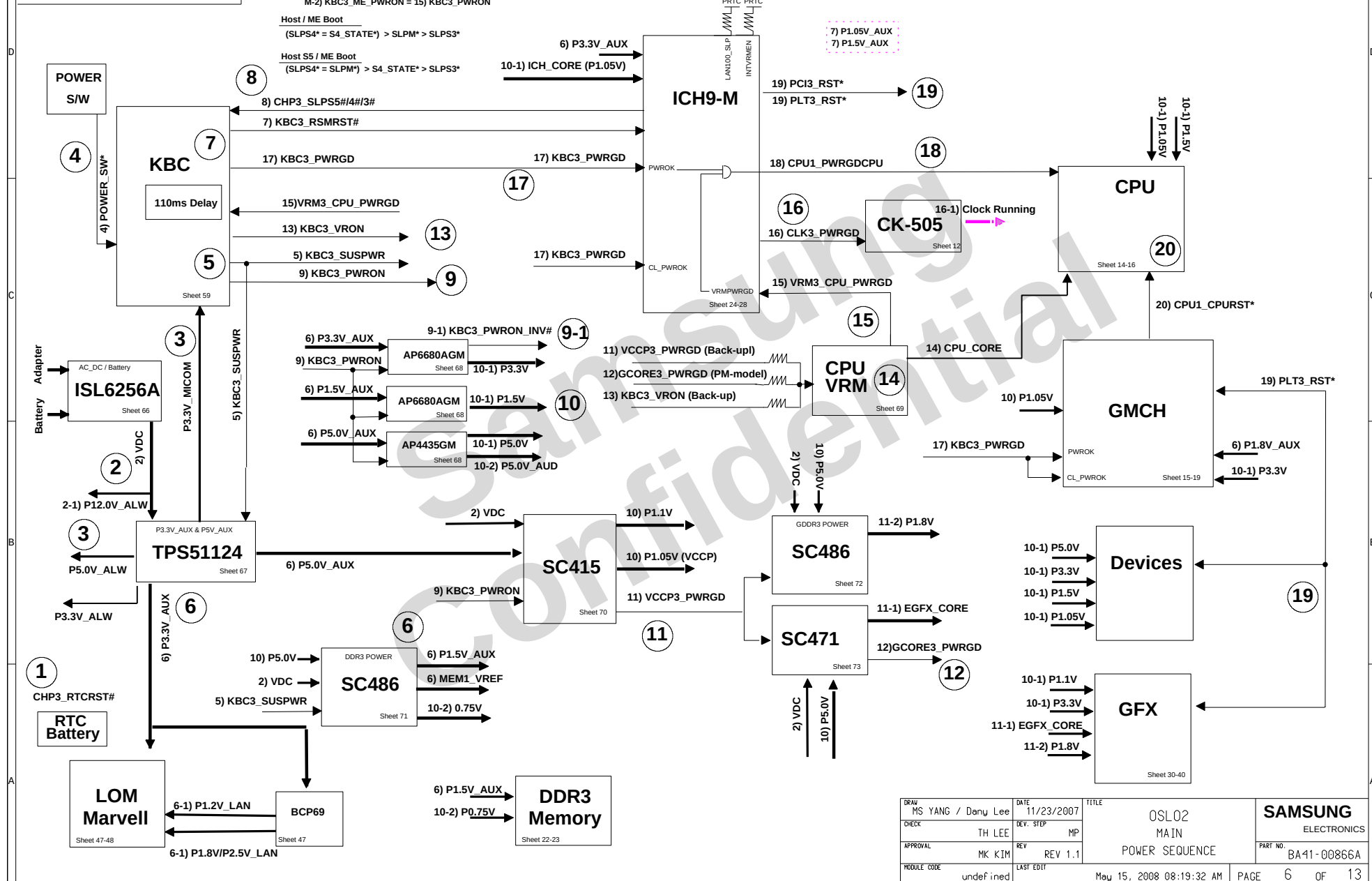


Value by Datasheet/Application notes (Value by measurement)

DRAW	MS YANG / Dany Lee	DATE	11/23/2007	TITLE	OSLO2	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	MAIN	POWER RAILS	
APPROVAL	MK KIM	REV	REV 1.1			PART NO. BA411-00866A
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	5	OF 13

POWER SEQUENCE

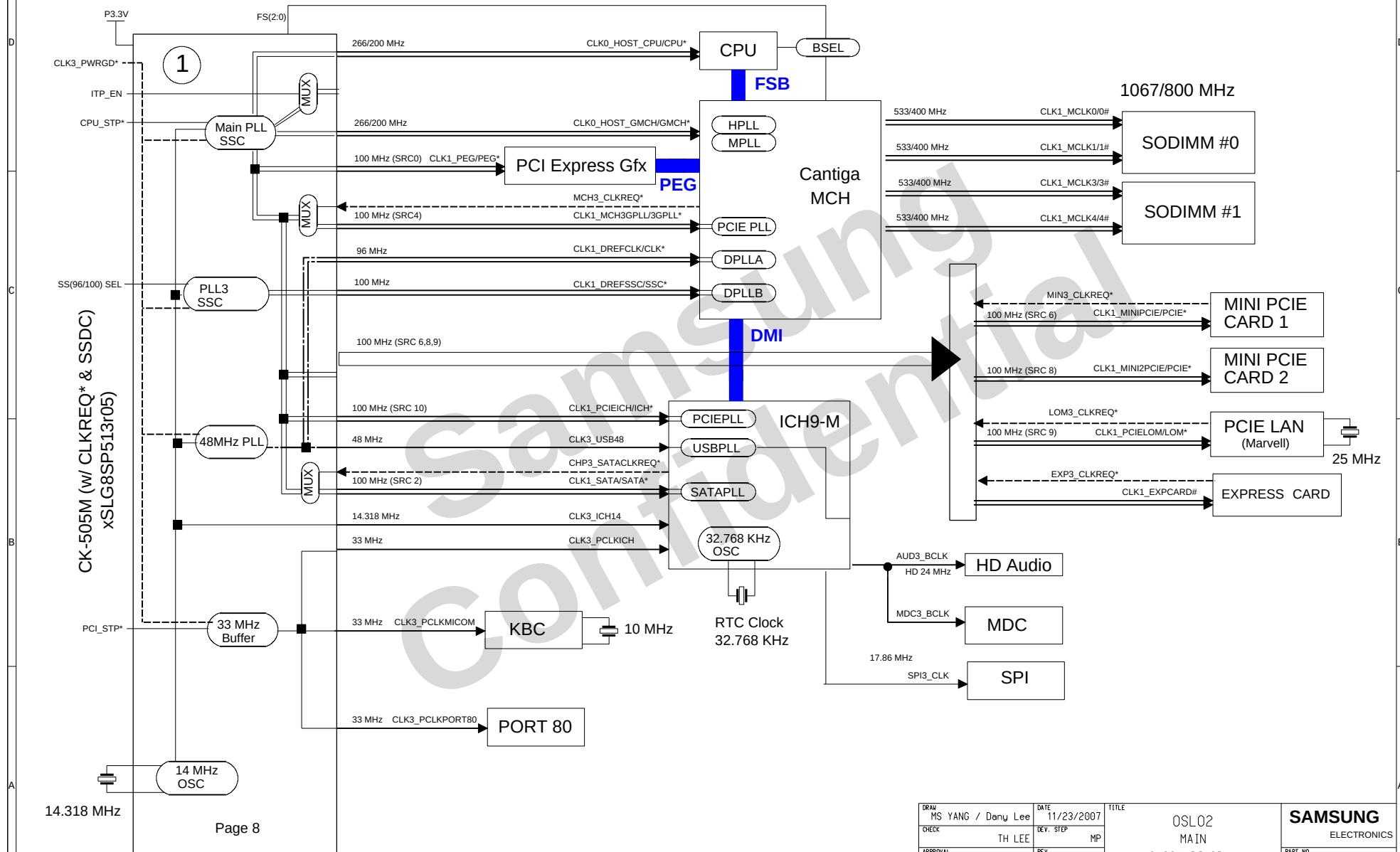
Rev. 0.9



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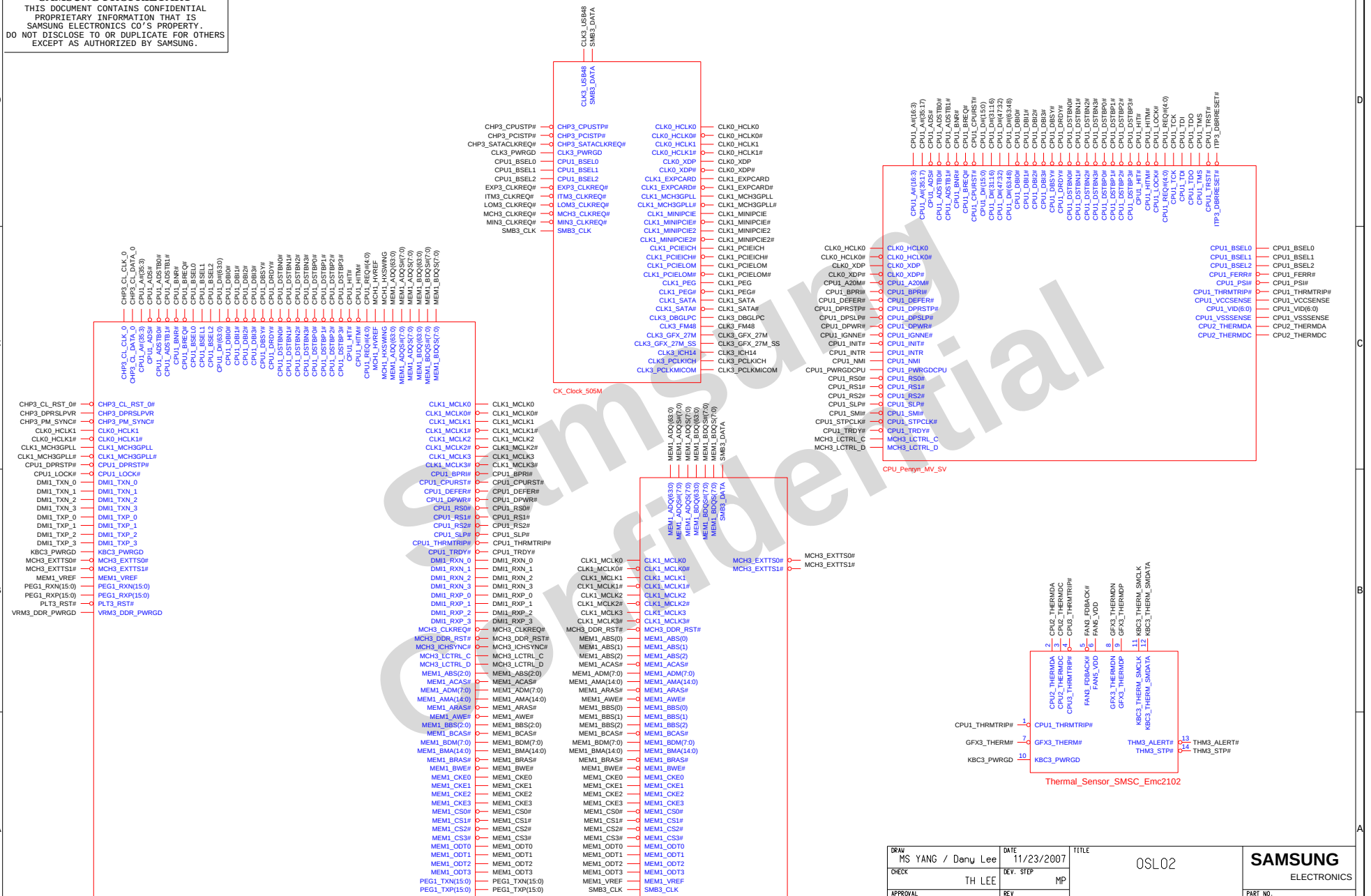
CLOCK DISTRIBUTION Rev. 0.1



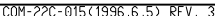
Page 8

DRAW	MS YANG / Dany Lee	DATE	11/23/2007	TITLE	OSLO2	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	MAIN		
APPROVAL	MK KIM	REV	REV 1.1	CLOCK DIAGRAM	PART NO.	BA11-00866A
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	7	OF 13

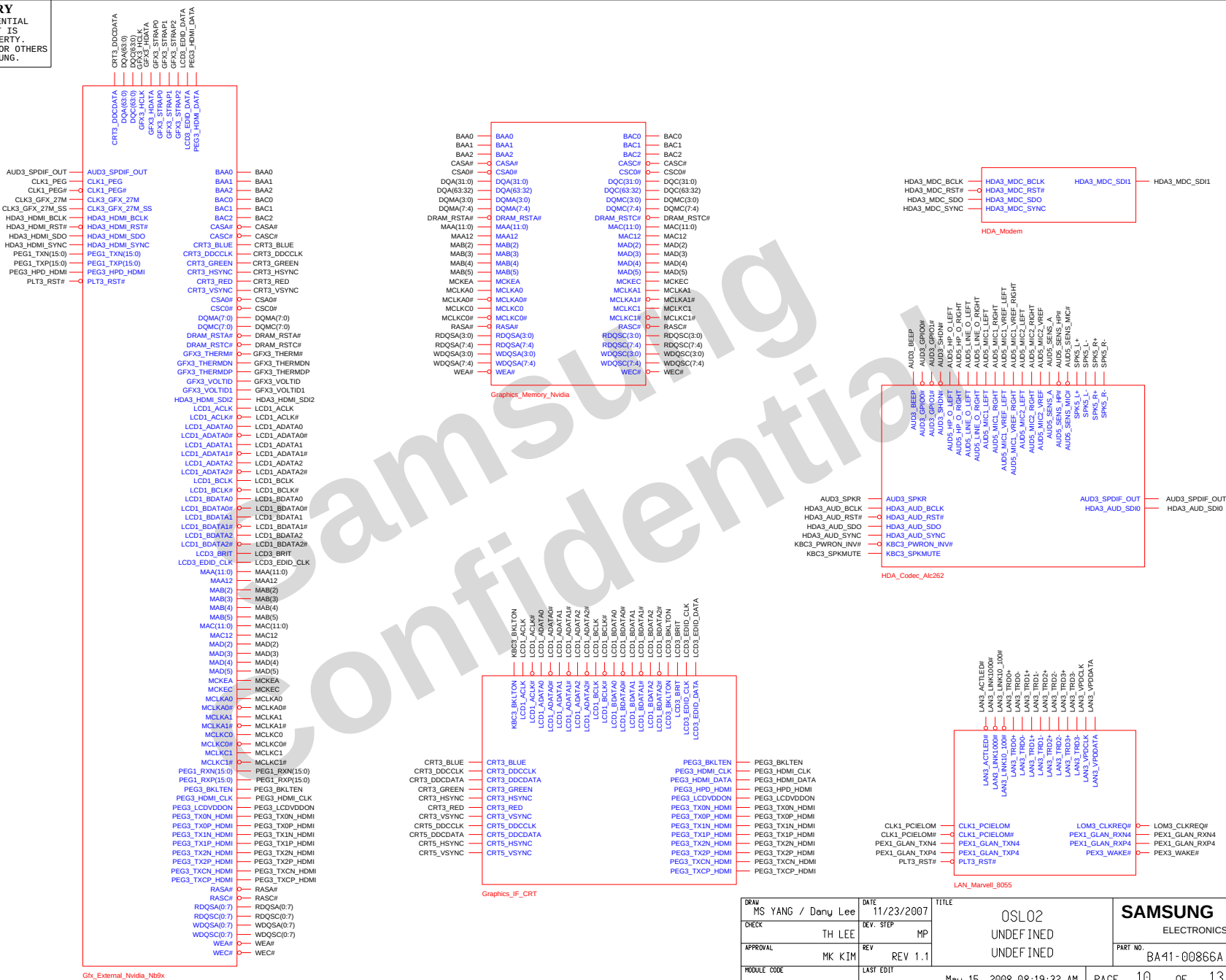
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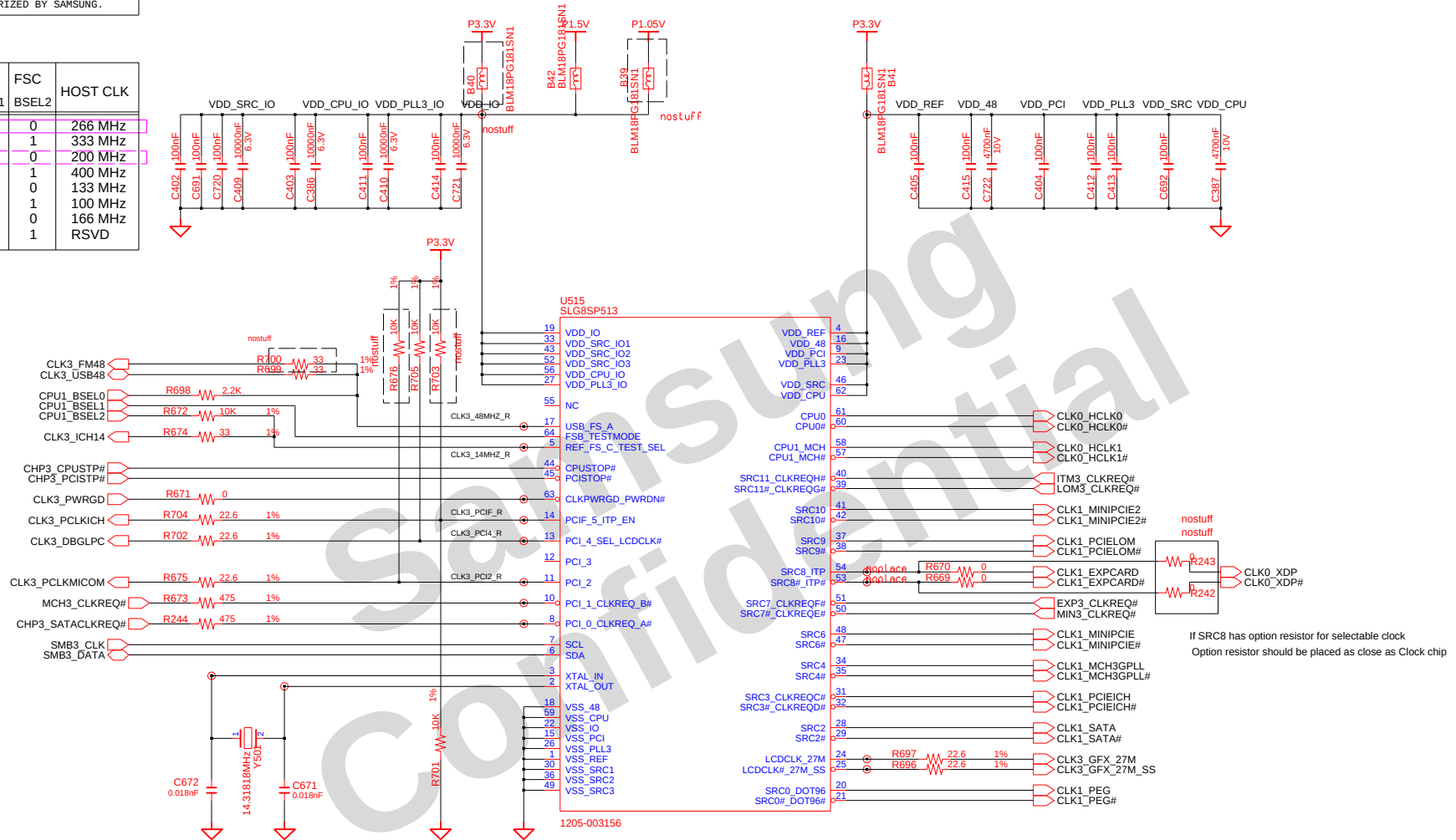
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D:/users/mobile16/mentor/oslo2/oslo2_pr
SRP Sheet Number: 11 of 76

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FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



If SRC8 has option resistor for selectable clock
Option resistor should be placed as close as Clock chip

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATACLKREQ#	SRC2
CLK REQ B	MCH3_CLKREQ#	SRC4
CLK REQ E	MIN3_CLKREQ#	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8
CLK REQ G	LOM3_CLKREQ#	SRC9

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

2nd source IDT, 1205-003159

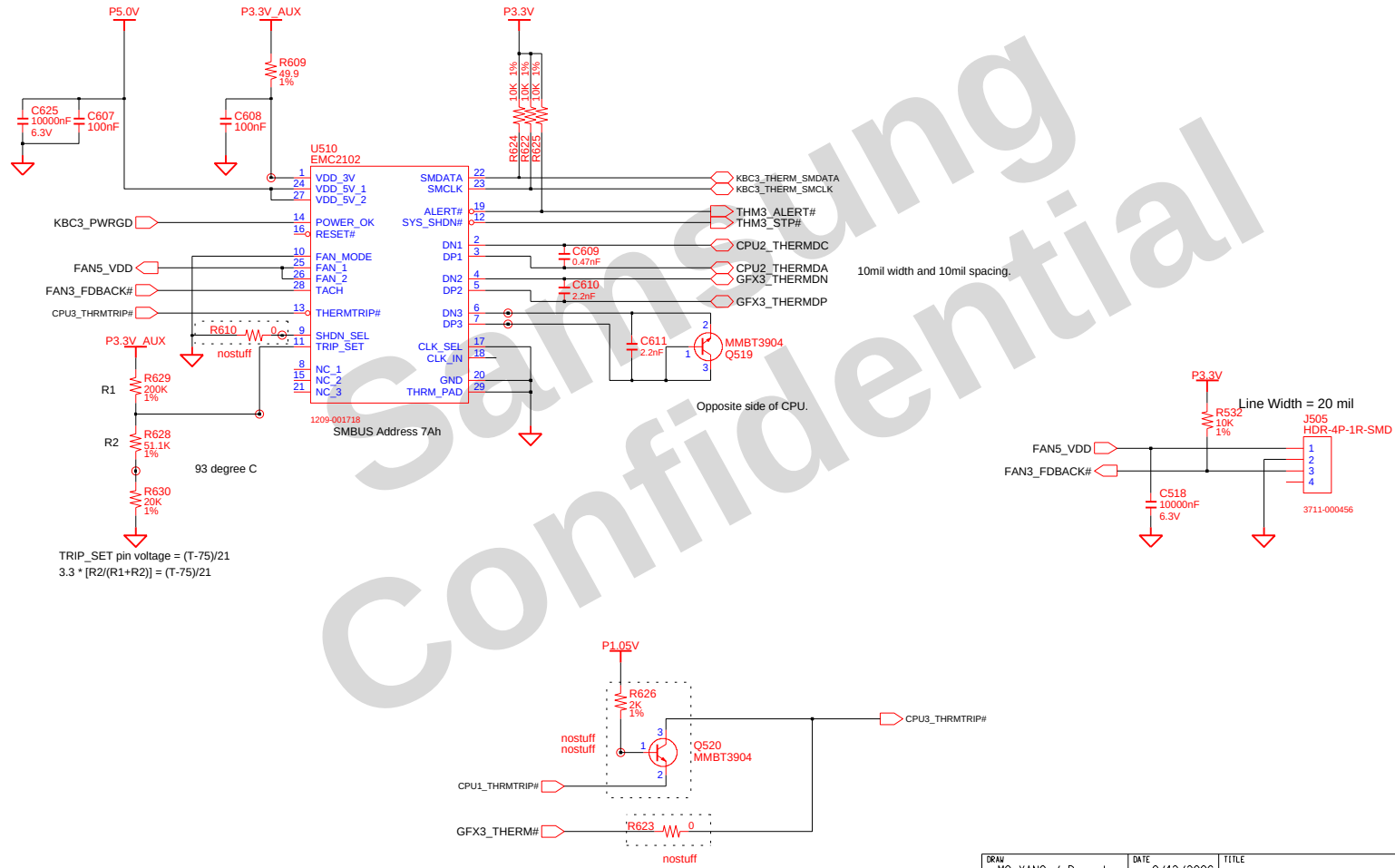
This part is 64pin QFN package.

DRAW MS YANG / Dany Lee		DATE 8/12/2006	TITLE OSL02		
CHECK TH LEE		DEV. STEP MP	Main_Clock_Circuit		
APPROVAL MK KIM		REV REV 1.1	CK_Clock_505M		
MODULE CODE undefined		LAST EDIT Mon 15, 2008 08:19:32 AM	PAGE 1	OF 1	

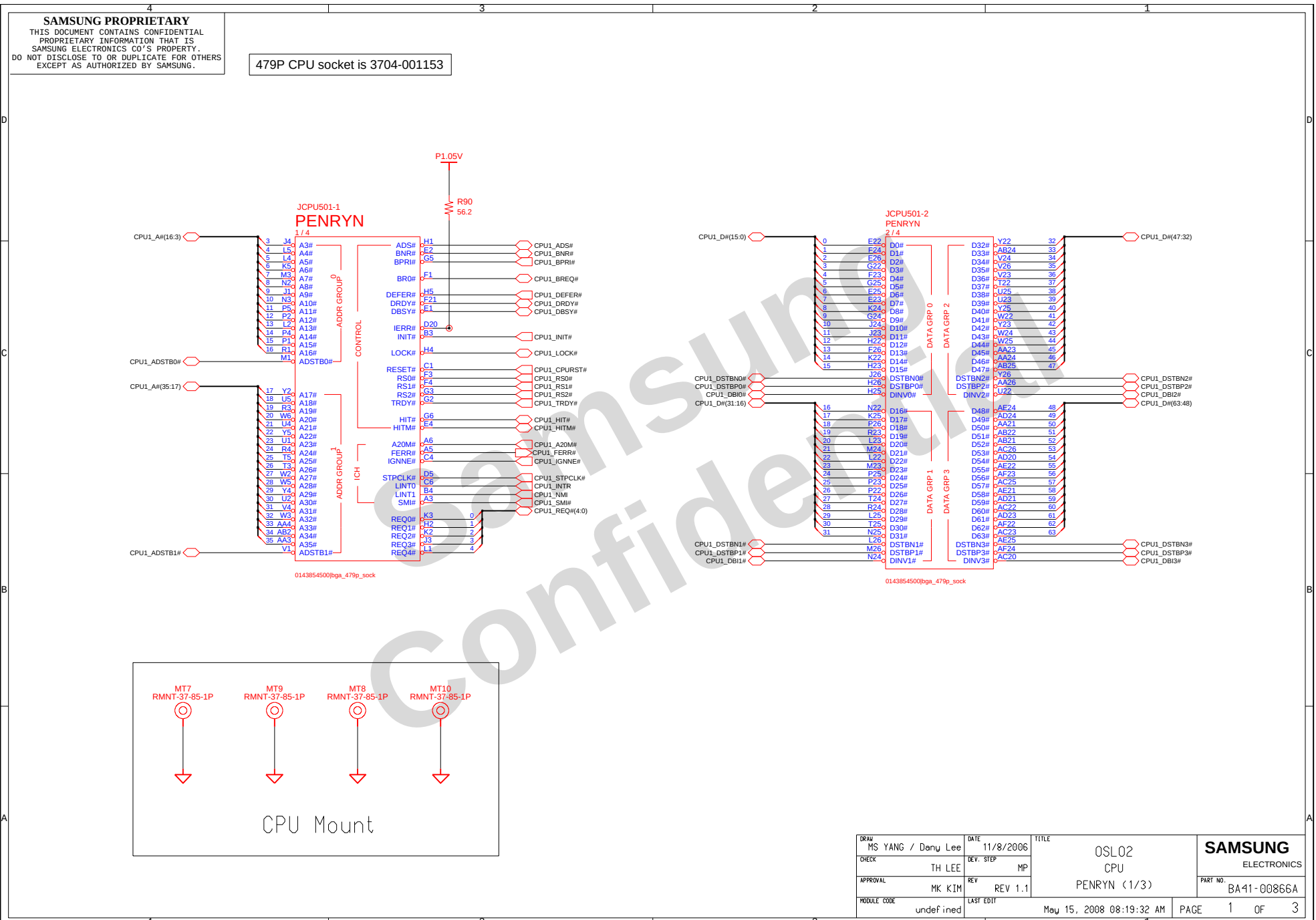
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THERMAL SENSOR & FAN CONTROL



DRW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	thermal_Sensor_SMSC_Emc2102	PART NO.	
APPROVAL	MK KIM	REV	REV 1.1	thermal_Sensor_SMSC_Emc2102	BA41-00866A	
MODULE CODE		LAST EDIT				
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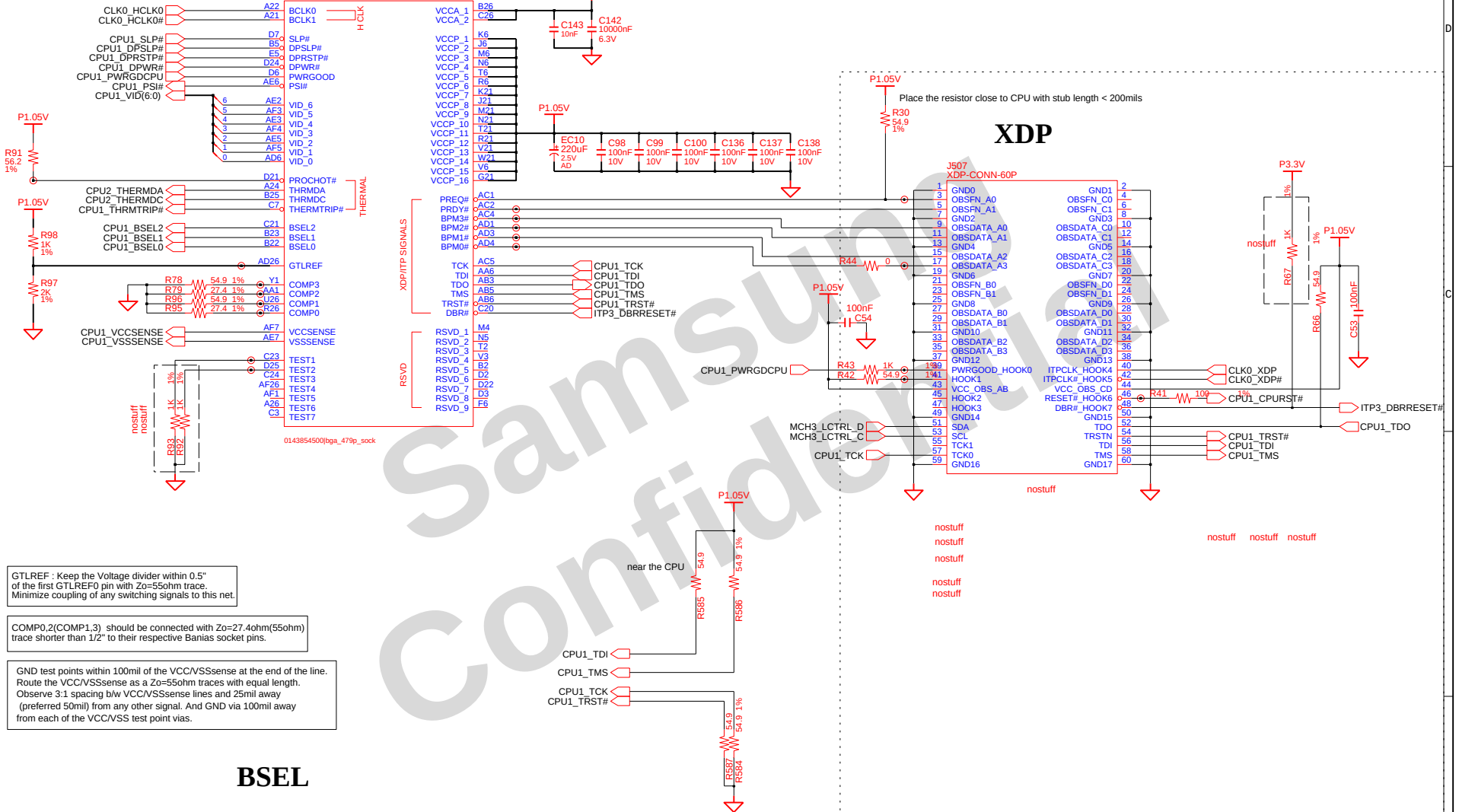


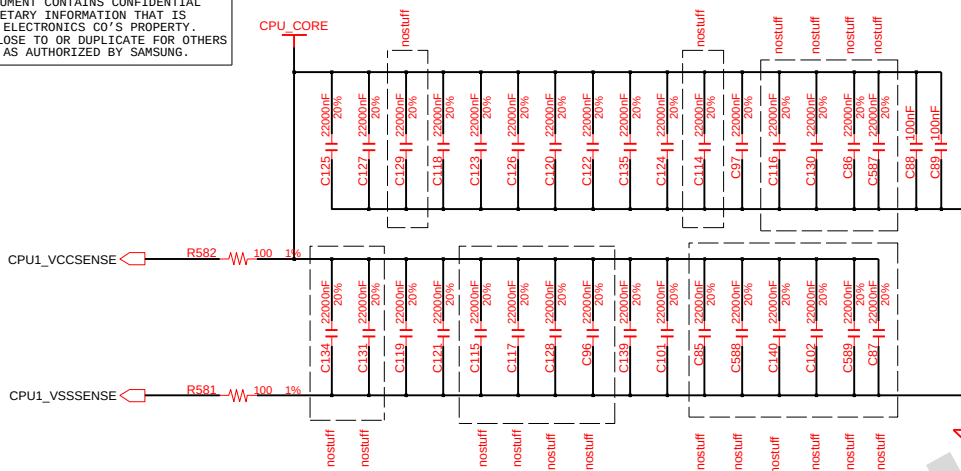
DRW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSLO2 CPU	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK	TH LEE	DEV. STEP	MP		PENRYN (1/3)	
APPROVAL	MK KIM	REV	REV 1.1			
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1 OF 3	

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JCPU501-3 PENRYN 3 / 4

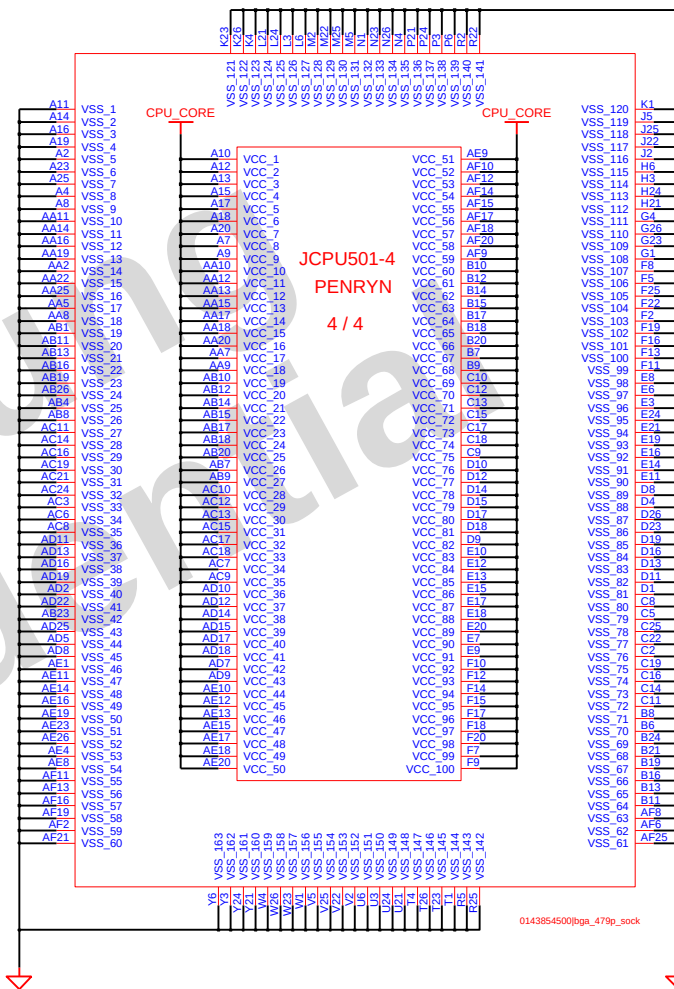




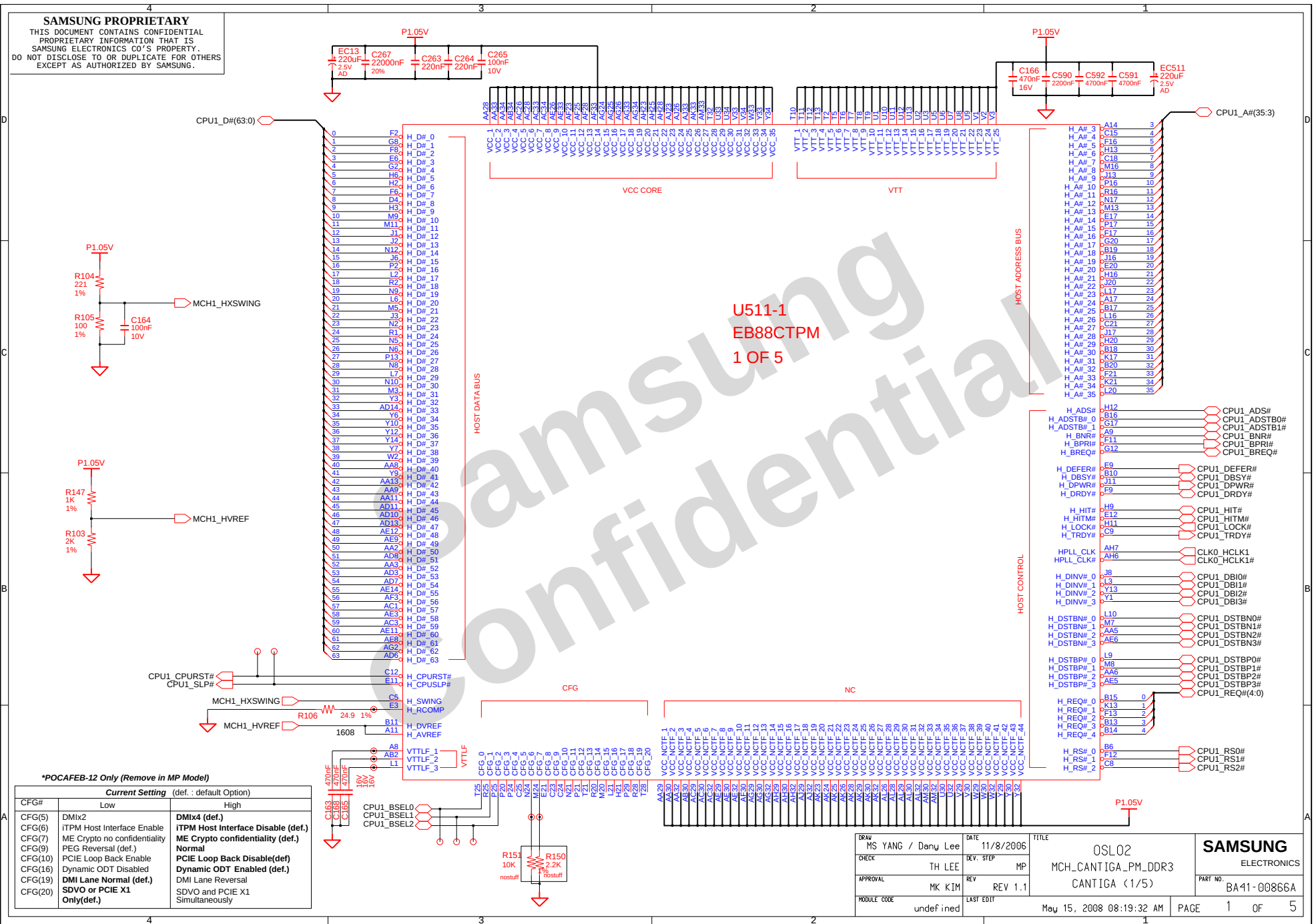
CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0 0	1.0000 V	1 0 1 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 0 1	0.9875 V	1 1 1 1 0 0 0 1	0.4750 V
0 0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 0 1 0	0.9750 V	1 0 1 1 0 0 0 1	0.4625 V
0 0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 0 1 1	0.9625 V	1 0 1 0 1 0 0 0	0.4500 V
0 0 0 0 0 1 0 0	1.4500 V	0 1 0 1 0 1 0 0	0.9500 V	1 0 1 1 0 1 0 1	0.4375 V
0 0 0 0 0 1 0 1	1.4375 V	0 1 0 1 0 1 0 1	0.9375 V	1 0 1 1 0 1 0 1	0.4250 V
0 0 0 0 0 1 1 0	1.4250 V	0 0 0 1 1 1 0 0	0.9250 V	1 1 1 1 0 1 0 1	0.4125 V
0 0 0 0 0 1 1 1	1.4125 V	0 1 0 1 0 1 1 1	0.9125 V	1 0 1 1 1 0 0 0	0.4000 V
0 0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0 0	0.9000 V	1 0 1 1 0 0 0 1	0.3875 V
0 0 0 0 1 0 0 1	1.3875 V	1 1 1 0 0 0 0 1	0.8875 V	1 0 1 1 1 0 0 1	0.3750 V
0 0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 0 0 1	0.8750 V	1 1 1 0 0 0 0 0	0.3625 V
0 0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 0 1 0	0.8625 V	1 0 0 1 1 1 0 0	0.3500 V
0 0 0 0 1 1 0 0	1.3500 V	0 0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 1 0 1	0.3375 V
0 0 0 0 1 1 0 1	1.3375 V	0 1 1 0 0 1 0 1	0.8375 V	1 0 1 1 1 1 0 1	0.3250 V
0 0 0 0 1 1 1 0	1.3250 V	0 1 1 1 1 1 0 0	0.8250 V	1 0 1 0 1 1 1 1	0.3125 V
0 0 0 0 1 1 1 1	1.3125 V	0 1 0 0 1 1 0 1	0.8125 V	1 1 1 0 0 0 0 0	0.3000 V
0 0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0 0	0.8000 V	1 1 1 0 0 0 0 0	0.2875 V
0 0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 0 1	0.7875 V	1 1 1 0 0 0 0 1	0.2750 V
0 0 0 1 0 0 1 0	1.2750 V	1 1 1 1 0 0 1 0	0.7750 V	1 1 1 0 0 0 0 1	0.2625 V
0 0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 0 1 1	0.7625 V	1 1 1 0 0 0 1 0	0.2500 V
0 0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0 0	0.7500 V	1 1 1 0 0 0 1 0	0.2375 V
0 0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 0 1	0.7375 V	1 1 1 0 0 0 1 1	0.2250 V
0 0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0 0	0.7250 V	1 1 1 0 0 0 1 1	0.2125 V
0 0 0 1 0 1 1 1	1.2125 V	1 0 0 0 1 1 1 1	0.7125 V	1 1 1 0 0 0 1 1	0.2000 V
0 0 0 1 1 0 0 0	1.2000 V	1 0 0 0 1 0 0 0	0.7000 V	1 1 1 0 0 0 1 1	0.1875 V
0 0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 0 0	0.6875 V	1 1 1 0 0 0 1 0	0.1750 V
0 0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 0 0 1	0.6750 V	1 1 1 0 0 0 1 0	0.1625 V
0 0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 0 0 1	0.6625 V	1 1 1 0 0 0 1 0	0.1500 V
0 0 0 1 1 1 0 0	1.1500 V	1 0 0 0 0 0 0 0	0.6500 V	1 1 1 0 0 0 1 0	0.1375 V
0 0 0 1 1 1 0 1	1.1375 V	1 0 0 0 0 1 0 0	0.6375 V	1 1 1 0 0 0 1 0	0.1250 V
0 0 0 1 1 1 1 0	1.1250 V	1 0 0 0 0 1 0 1	0.6250 V	1 1 1 0 0 0 1 1	0.1125 V
0 0 0 1 1 1 1 1	1.1125 V	1 0 0 0 0 1 1 0	0.6125 V	1 1 1 0 0 0 0 0	0.1000 V
0 0 1 0 0 0 0 0	1.1000 V	1 0 0 0 0 1 0 0	0.6000 V	1 1 1 1 0 0 0 0	0.0875 V
0 0 1 0 0 0 0 1	1.0875 V	1 0 0 0 0 1 0 0	0.5875 V	1 1 1 1 0 0 0 0	0.0750 V
0 0 1 0 0 0 1 0	1.0750 V	1 0 0 0 0 1 0 0	0.5750 V	1 1 1 1 0 0 0 1	0.0625 V
0 0 1 0 0 0 1 1	1.0625 V	1 0 0 0 0 1 0 1	0.5625 V	1 1 1 1 0 0 0 1	0.0500 V
0 0 1 0 0 1 0 0	1.0500 V	1 0 0 0 0 1 0 0	0.5500 V	1 1 1 1 0 0 0 1	0.0375 V
0 0 1 0 0 1 0 1	1.0375 V	1 0 0 0 0 1 0 0	0.5375 V	1 1 1 1 0 0 0 1	0.0250 V
0 0 1 0 0 1 1 0	1.0250 V	1 0 0 0 0 1 1 0	0.5250 V	1 1 1 1 0 0 0 1	0.0125 V
0 0 1 0 0 1 1 1	1.0125 V	1 0 0 0 0 1 1 1	0.5125 V	1 1 1 1 0 0 0 0	0.0000 V
		1 0 1 0 0 0 0 0	0.5000 V	1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
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				1 1 1 1 0 0 0 0	0.0000 V
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				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
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				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
				1 1 1 1 0 0 0 0	0.0000 V
			</		

*Yonah Processor (2.33 GHz / 800 MHz : TBD)



DRAW MS YANG / Dany Lee		DATE 11/8/2006		TITLE OSL02 CPU PENRYN (3/3)		SAMSUNG ELECTRONICS	
CHECK TH LEE		REV. STEP MP					
APPROVAL MK KIM		REV REV 1.1					
MODULE CODE undefined		LAST EDIT May 15, 2008 08:19:32 AM					
				PAGE		3 OF 3	

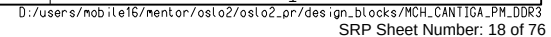


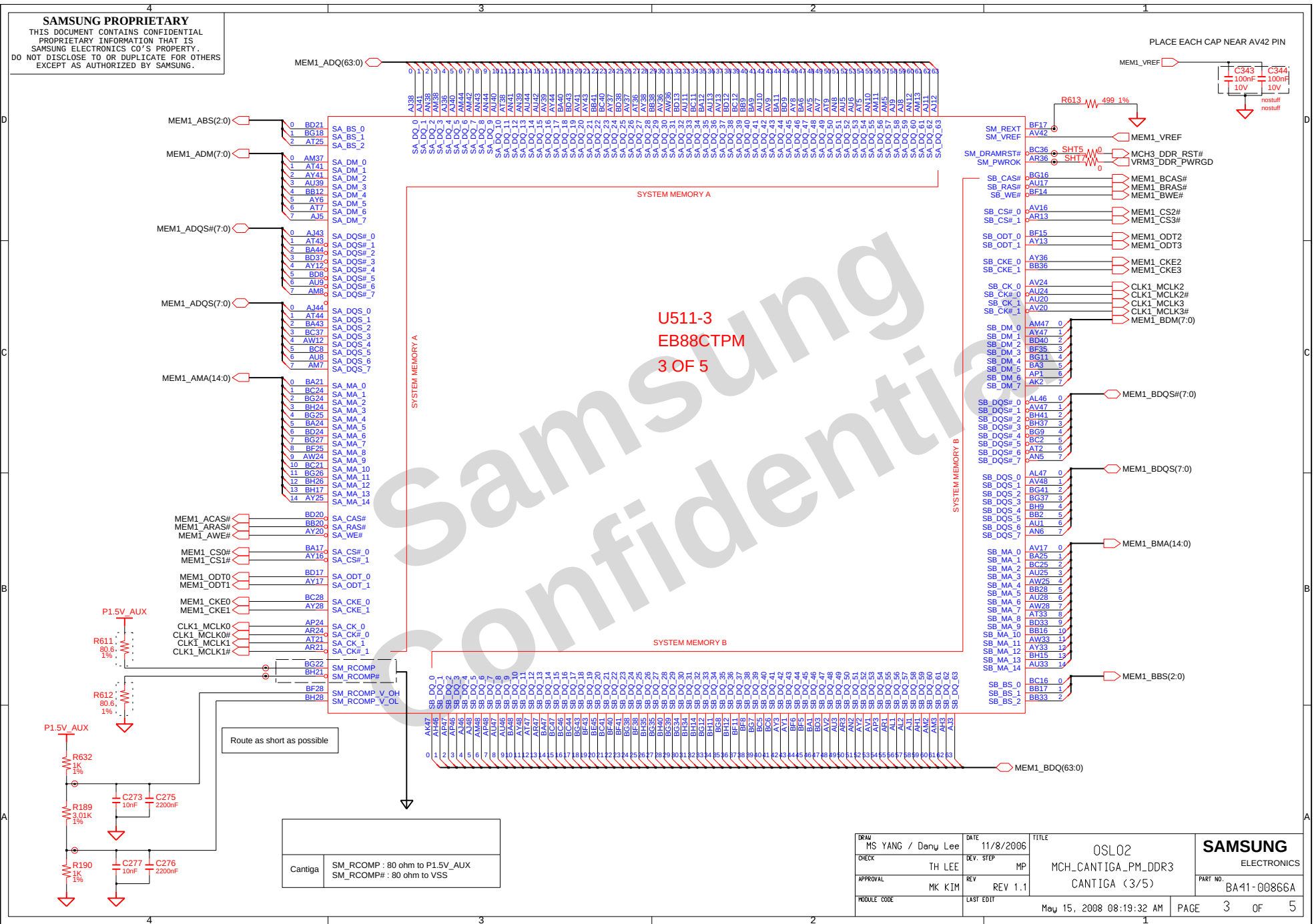
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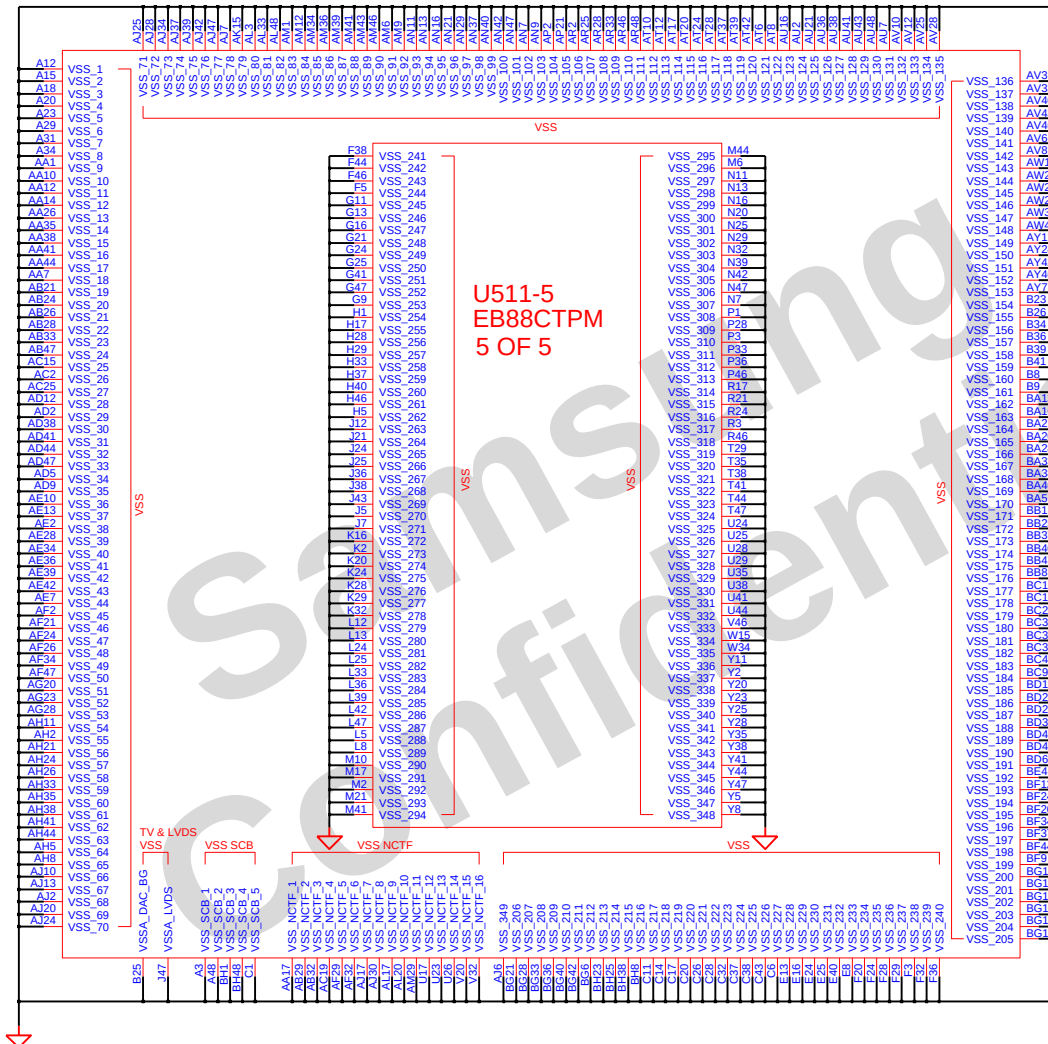
***POCAFEB-12 Only (Remove in MP Model)**

CFG#	Current Setting (def.: default Option)	High
CFG(5)	DMIx2	DMIx4 (def.)
CFG(6)	ITPM Host Interface Enable	ITPM Host Interface Disable (def.)
CFG(7)	ME Crypto no confidentiality	ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)	Normal
CFG(10)	PCIe Loop Back Enable	PCIe Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)	DMI Lane Reversal
CFG(20)	SDVO or PCIe X1 Only(def.)	SDVO and PCIe X1 Simultaneously

DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSLO2	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	MCH_CANTIGA_PM_DDR3		
APPROVAL	MK KIM	REV	1.1	CANTIGA (1/5)		PART NO. BA11-00866A
MODULE CODE	undefined	LAST EDIT		May 15, 2008 08:19:32 AM	PAGE	1 OF 5





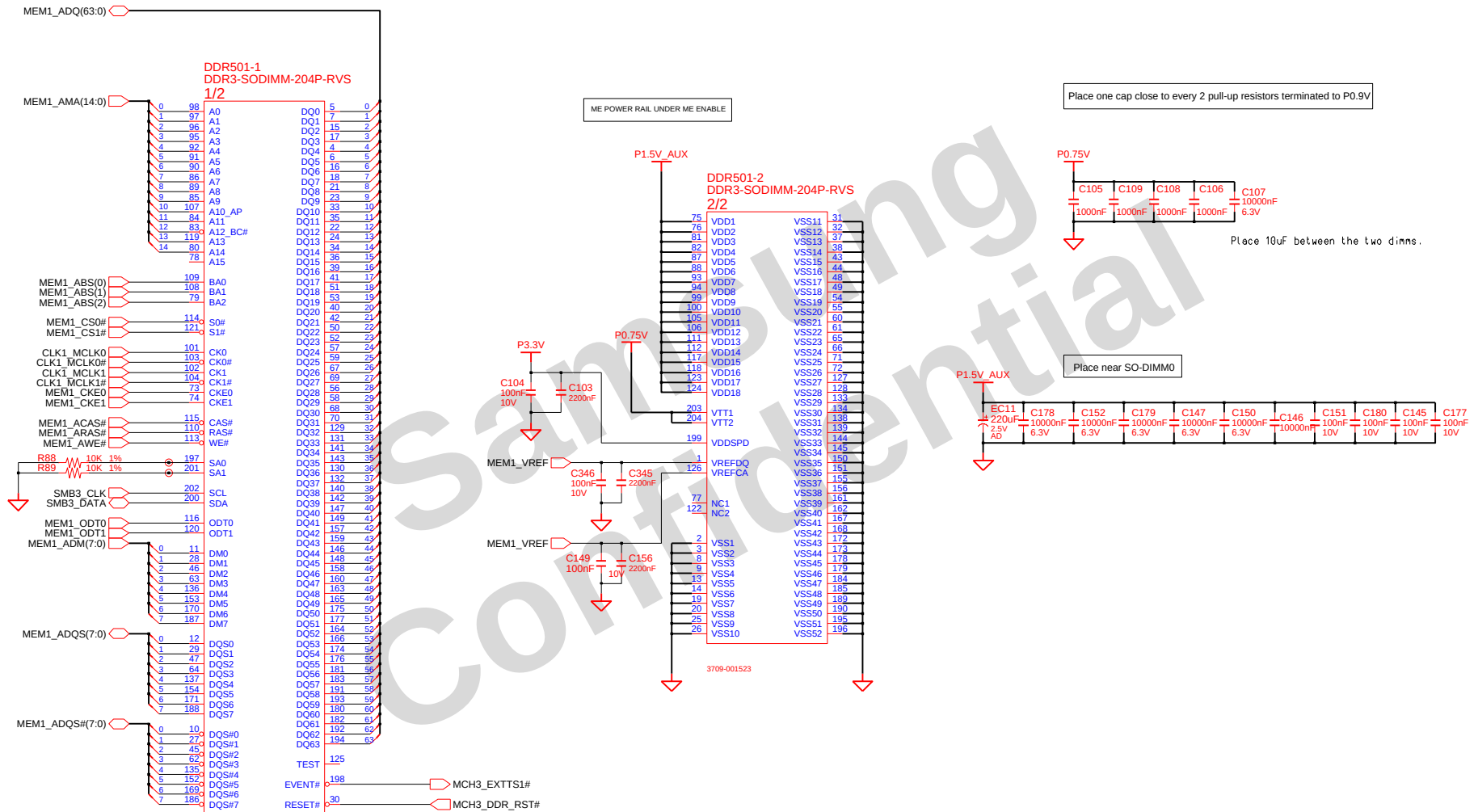


DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK	TH LEE	DEV. STEP	MP	MCH_CANTIGA_PM_DDR3		
APPROVAL	MK KIM	REV	REV 1.1	CANTIGA (5/5)		
MODULE CODE		LAST EDIT				
May 15, 2008 08:19:32 AM						PAGE 5 OF 5

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DDR SO-DIMM #0

Height : 5.2mm (Reverse)

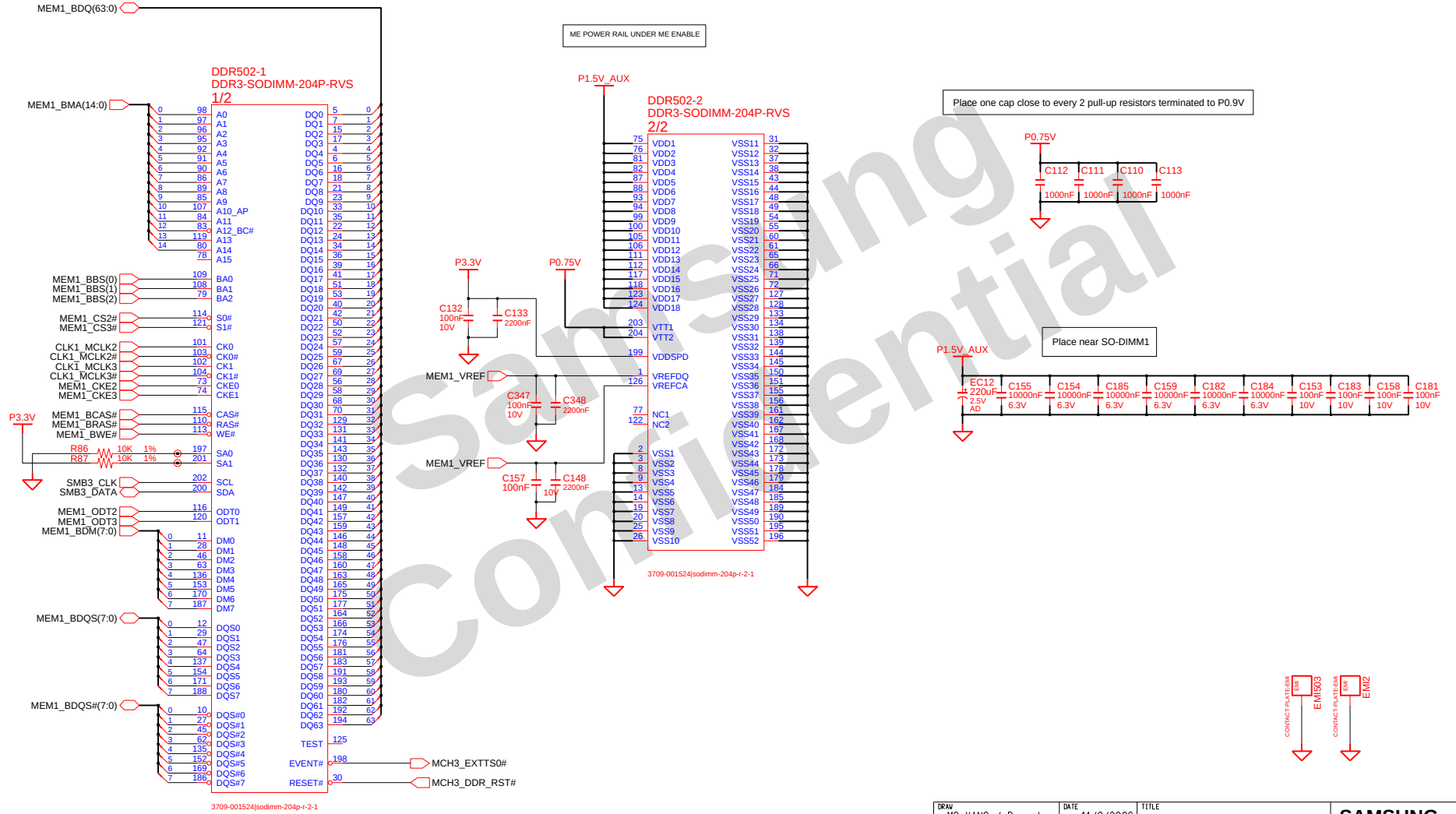


DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	SODIMM_REV	BA11-00866A	
APPROVAL	MK KIM	REV	REV 1.1	DDR3 CH A	PART NO.	
MODULE CODE		LAST EDIT				
May 15, 2008 08:19:32 AM				PAGE	1	OF 2

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DDR SO-DIMM #1

Height : 9.2mm (Reverse)



DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	REV. STEP	MP	SODIMM_REV	PART NO.	
APPROVAL	MK KIM	REV	1.1	DDR3 CH B	BA11-00866A	
MODULE CODE		LAST EDIT				

May 15, 2008 08:19:32 AM PAGE 2 OF 2

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U5-1 NH82801IBM 1 / 5

Internal VR Strap

INTVRMEN	Pull up	VccSus1_05, VccSus1_5, VccCL1_5
LAN100_SLP	Pull up	VccLAN1_05, VccCL1_05

SATA Cap. Place ment :
Distance b/w the ICH9-M & cap on the "P" signal should be identical
distance b/w the ICH9-M & cap on the "N" signal same pair.

Place 56 ohm resistor within 2" of ICH9M
Place PU resistor within 2" of 56ohm res.

It should be placed at memory door for easy-access

CR203 : 4301-000108

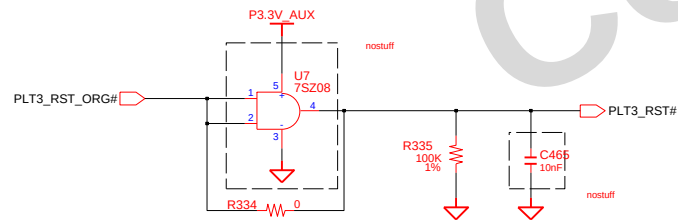
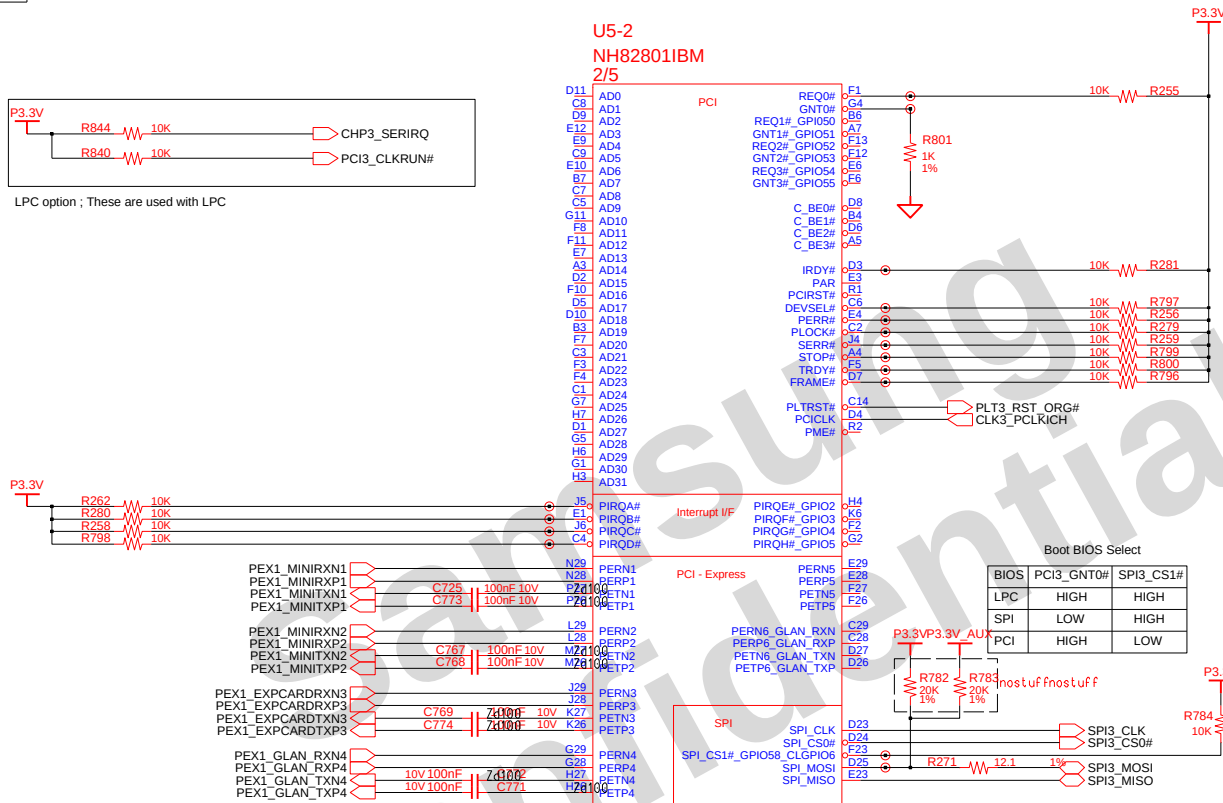
4309-001022

For RTC reset

DRW MS YANG / Dony Lee
DATE 11/8/2006
TITLE OSL02 ICH9-M (1/5)
DEV. STEP MP
APPROVAL MK KIM
REV 1.1
MODULE CODE
LAST EDIT
May 15, 2008 08:19:32 AM
PAGE 1 OF 5
SAMSUNG ELECTRONICS
PART NO. BA41-00866A

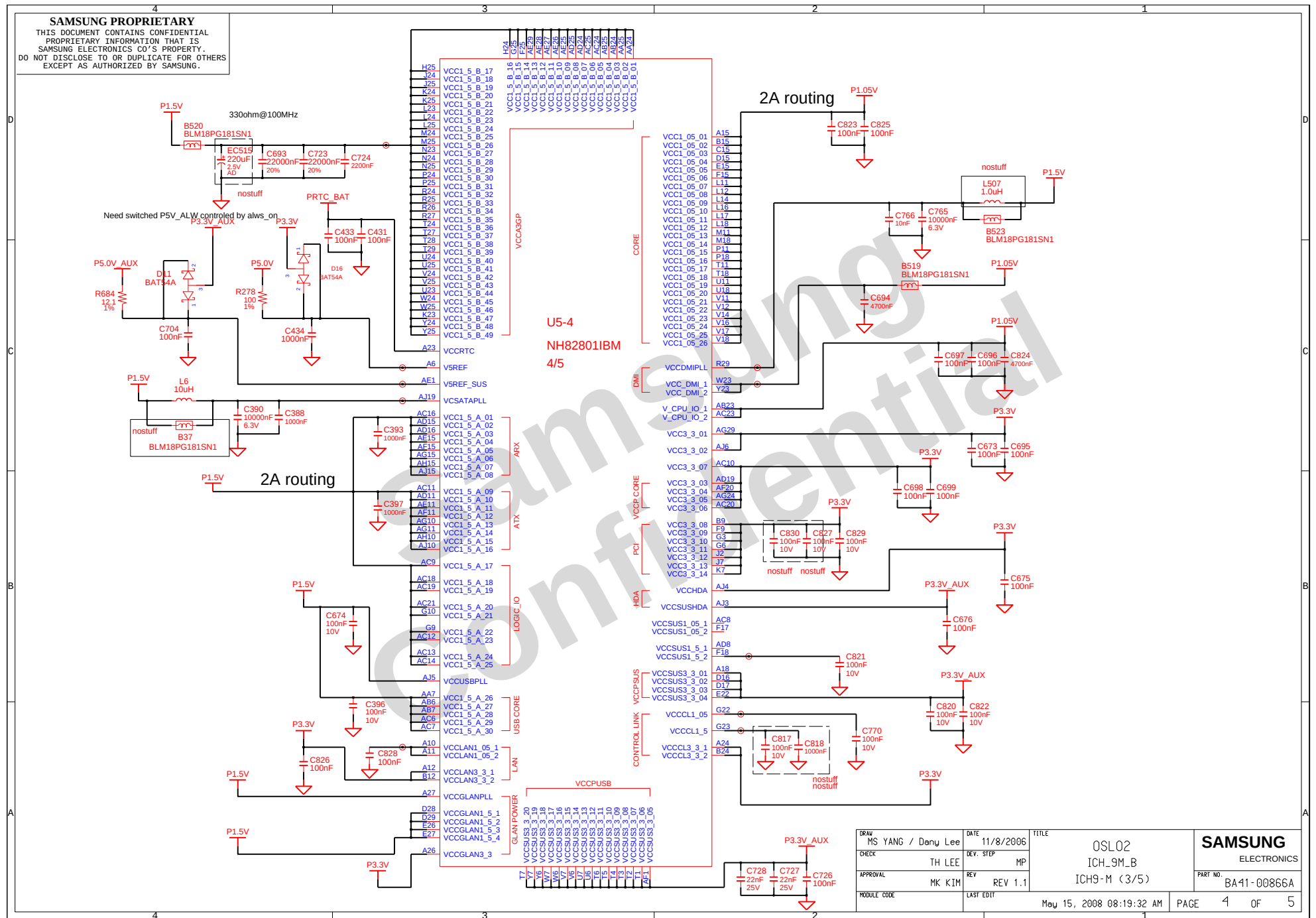
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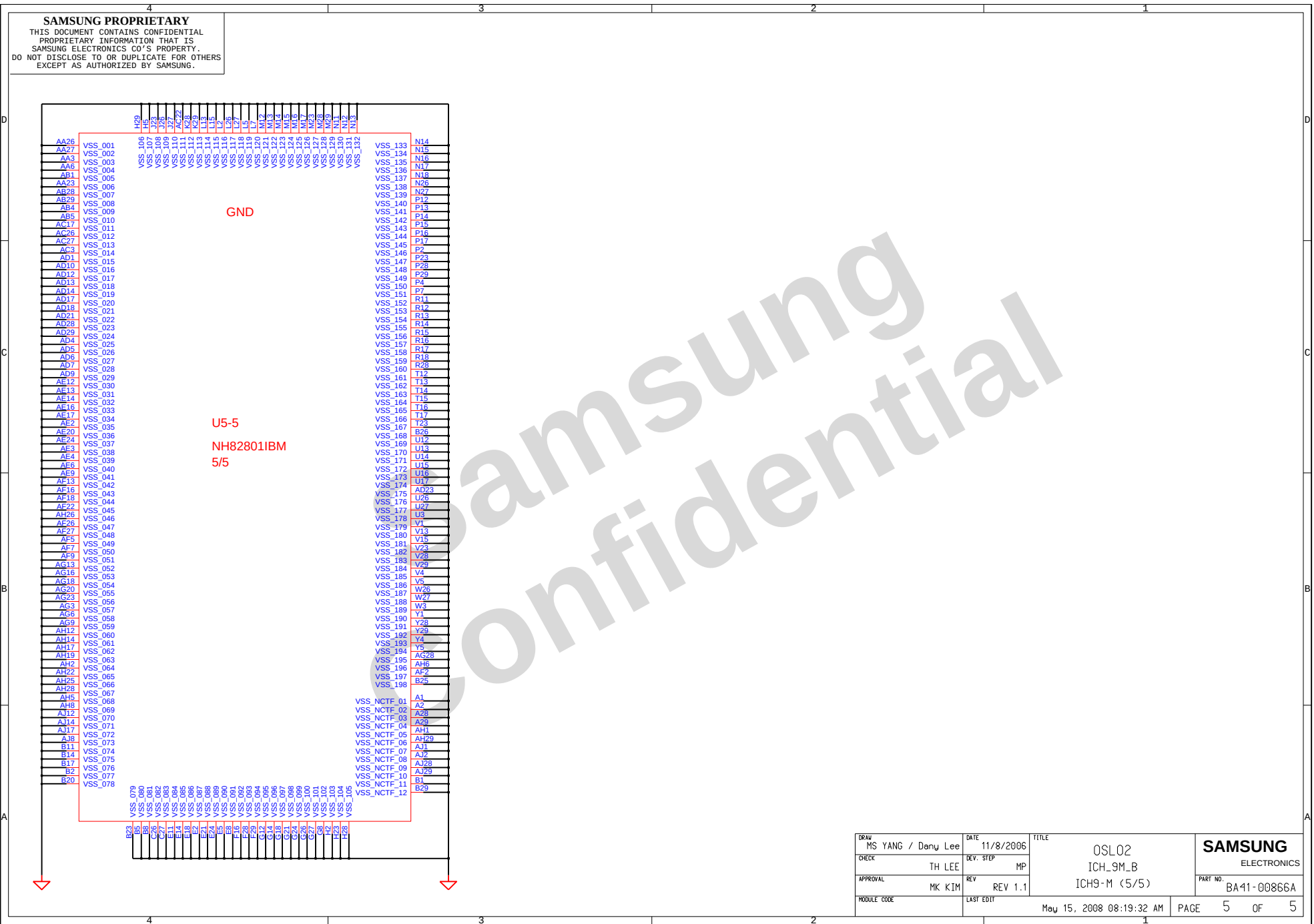
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DRAW MS YANG / Dany Lee	DATE 11/8/2006	TITLE OSL02 ICH_9M_B ICH9-M (2/5)	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE undefined	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 2 OF 5

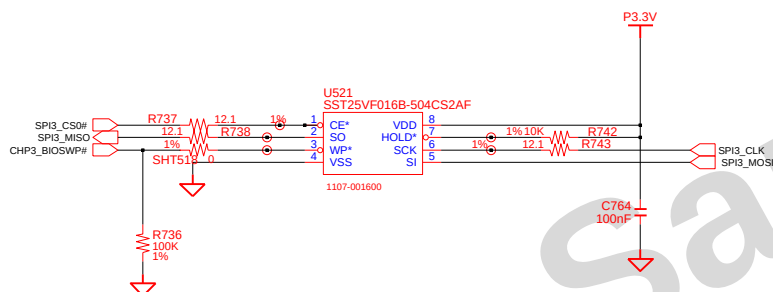
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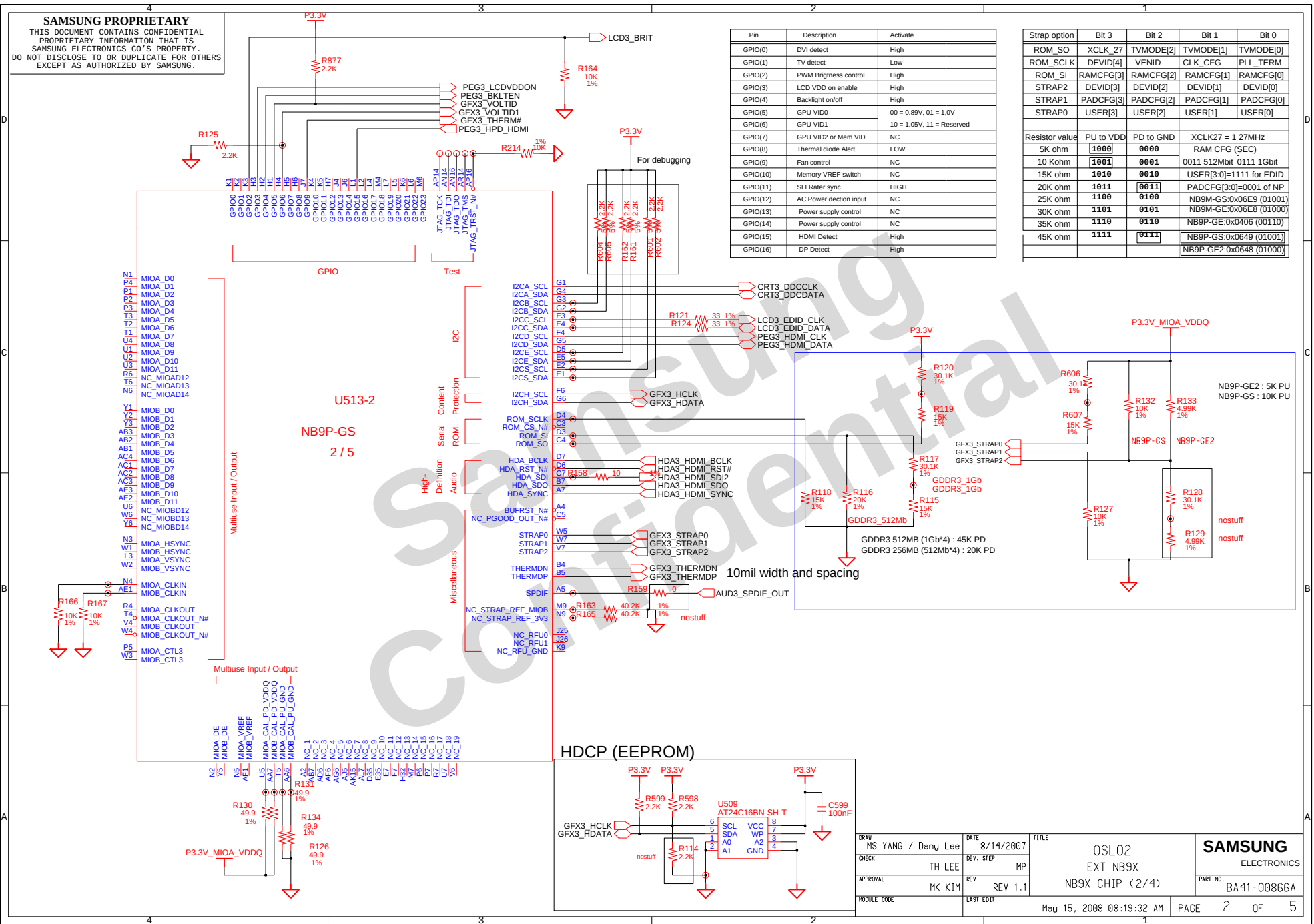
DRW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
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APPROVAL	MK KIM	REV	REV 1.1		ICH9-M (5/5)	PART NO. BA411-00866A
MODULE CODE		LAST EDIT				
				May 15, 2008 08:19:32 AM	PAGE	5 OF 5

SST - SST25VF016B
-> 1107-001600



02	VERIFY REAL MODE	56	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6A	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY " PRESS SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	
CHECK TH LEE	DEV. STEP MP	SPI_BIOS.ROM	
APPROVAL MK KIM	REV REV 1.1	SPI_BIOS.ROM	
MODULE CODE	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1 OF 1	



Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU VDD	00 = 0.89V, 01 = 1.0V
GPIO(6)	GPU VID1	10 = 1.05V, 11 = Reserved
GPIO(7)	GPU VID2 or Mem VID	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan control	NC
GPIO(10)	Memory VREF switch	NC
GPIO(11)	SU Rater sync	HIGH
GPIO(12)	AC Power dection input	NC
GPIO(13)	Power supply control	NC
GPIO(14)	Power supply control	NC
GPIO(15)	HDMI Detect	High
GPIO(16)	DP Detect	High

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_27	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

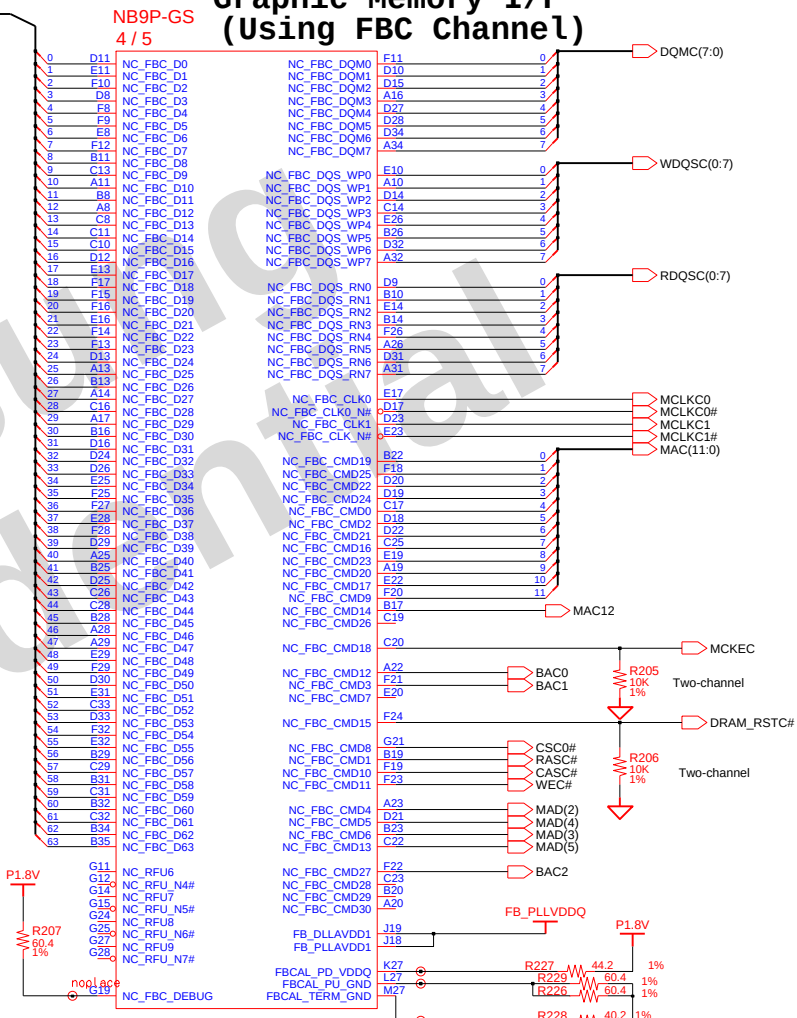
Resistor value	PU to VDD	PD to GND	XCLK27 = 1.27MHz
5K ohm	1000	0000	RAM CFG (SEC)
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit
15K ohm	1010	0010	USER[3:0]=1111 for EDID
20K ohm	1011	0011	PADCFG[3:0]=0001 of NP
25K ohm	1100	0100	NB9M-GS:0x06E9 (01001)
30K ohm	1101	0101	NB9M-GS:0x06E8 (01000)
35K ohm	1110	0110	NB9P-GS:0x0406 (00110)
45K ohm	1111	0111	NB9P-GS:0x0649 (01001)
			NB9P-GS:0x0648 (01000)

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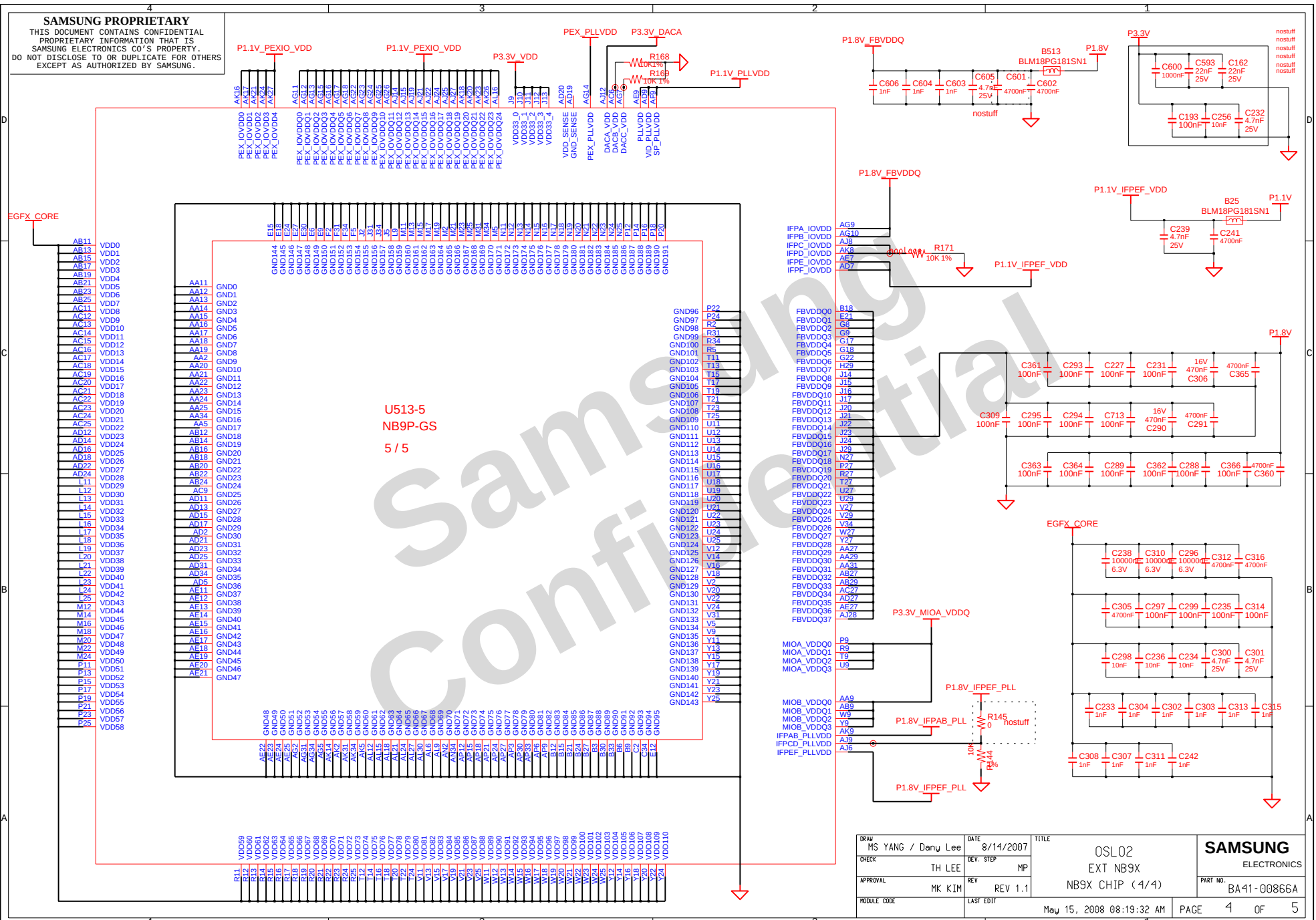
Graphic Memory I/F (Using FBA Channel)



Pin 19 connection diagram for BAC2. Pin 19 (NC_FBC_DEBUG) is connected to NC_FBC_CMD27 (F22), NC_FBC_CMD28 (C23), NC_FBC_CMD29 (B24), and NC_FBC_CMD30 (A20). Pin 19 is also connected to FB_PLLVDDQ (J19, J18), FB_DL1AVDD1 (K27, L27, M27), FBAL_PD_VDDQ (L27), FBAL_PU_GND (M27), and FBAL_TERM_GND (R227, R229, R226, R228).



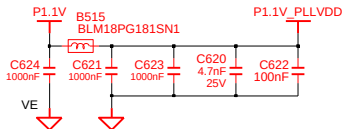
NAME	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSLO2 EXT NB9X NB9X CHIP (3/4)		
CHECK	TH LEE	DEV. STEP	MP			PART NO.	BA41-00866A
APPROVAL	MK KIM	REV	REV 1.1				
MODULE CODE	LAST EDIT		May 15, 2008 08:19:32 AM				



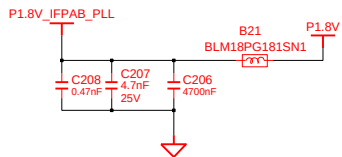
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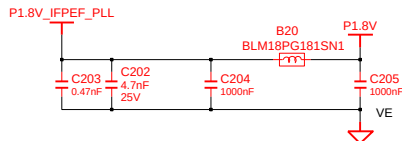
PLL_VDD



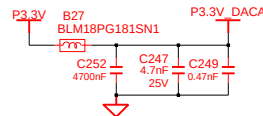
IFPAB_PLLVDD



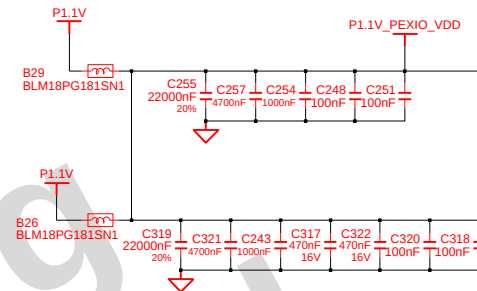
IFPEF_PLLVDD



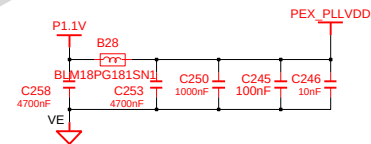
DACA/B/C



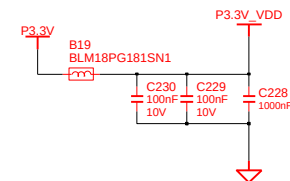
PEX_IOVDD (w PEX_IOVDDQ)



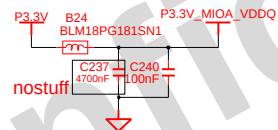
PEX_PLL_VDD



3.3V_VDD



MIOA/B_VDDQ

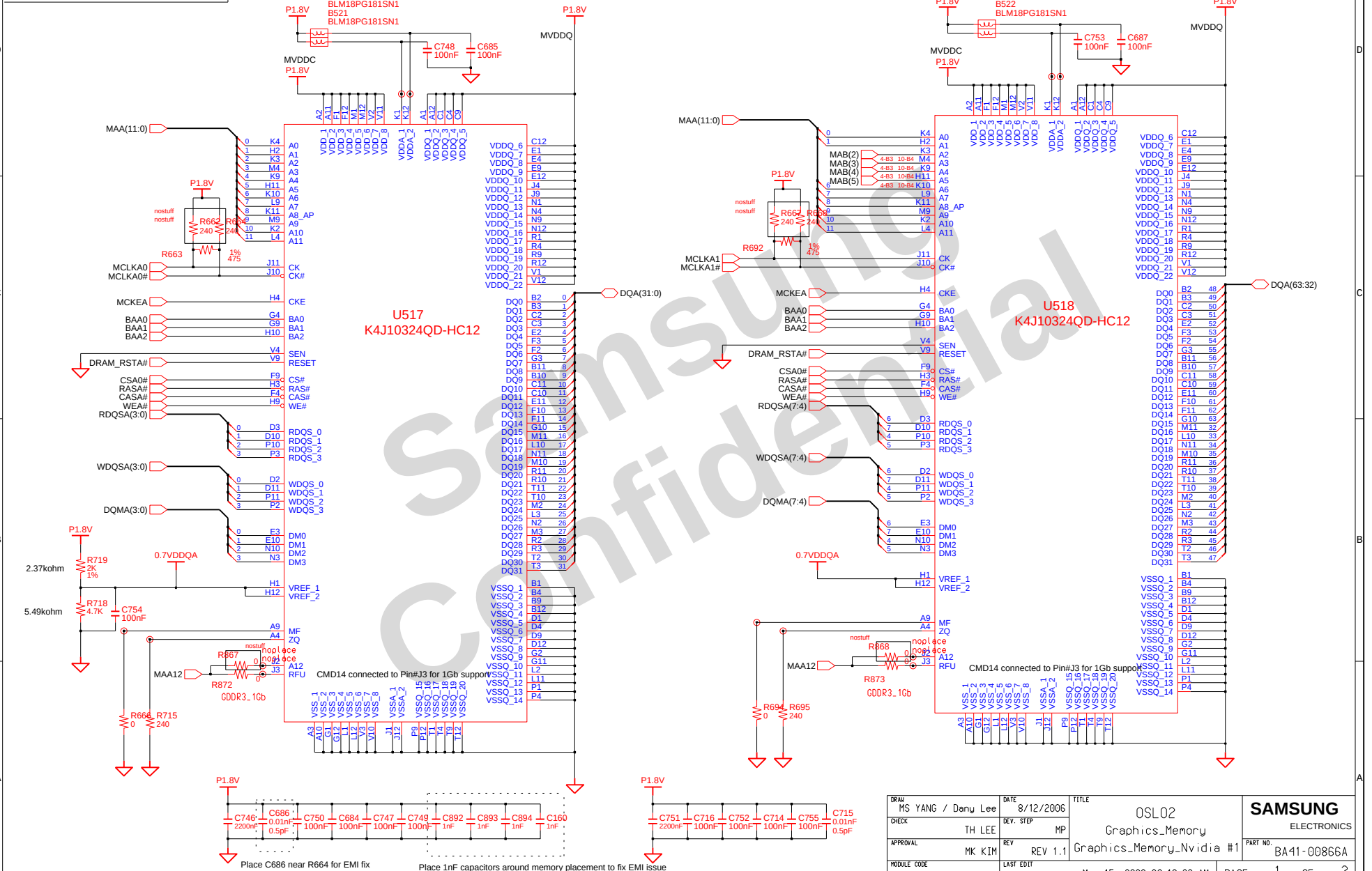


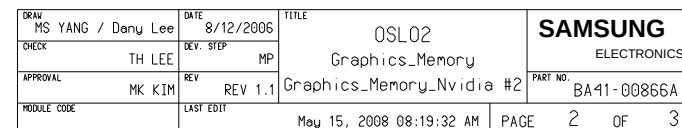
DRAW	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02 EXT NB9X NB9X POWER RAIL	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP			PART NO. BA11-00866A
APPROVAL	MK KIM	REV	REV 1.1			
MODULE CODE		LAST EDIT				

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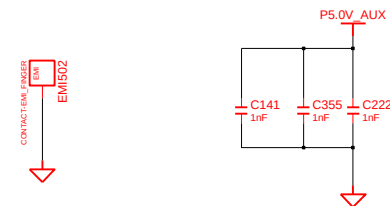
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A-channel





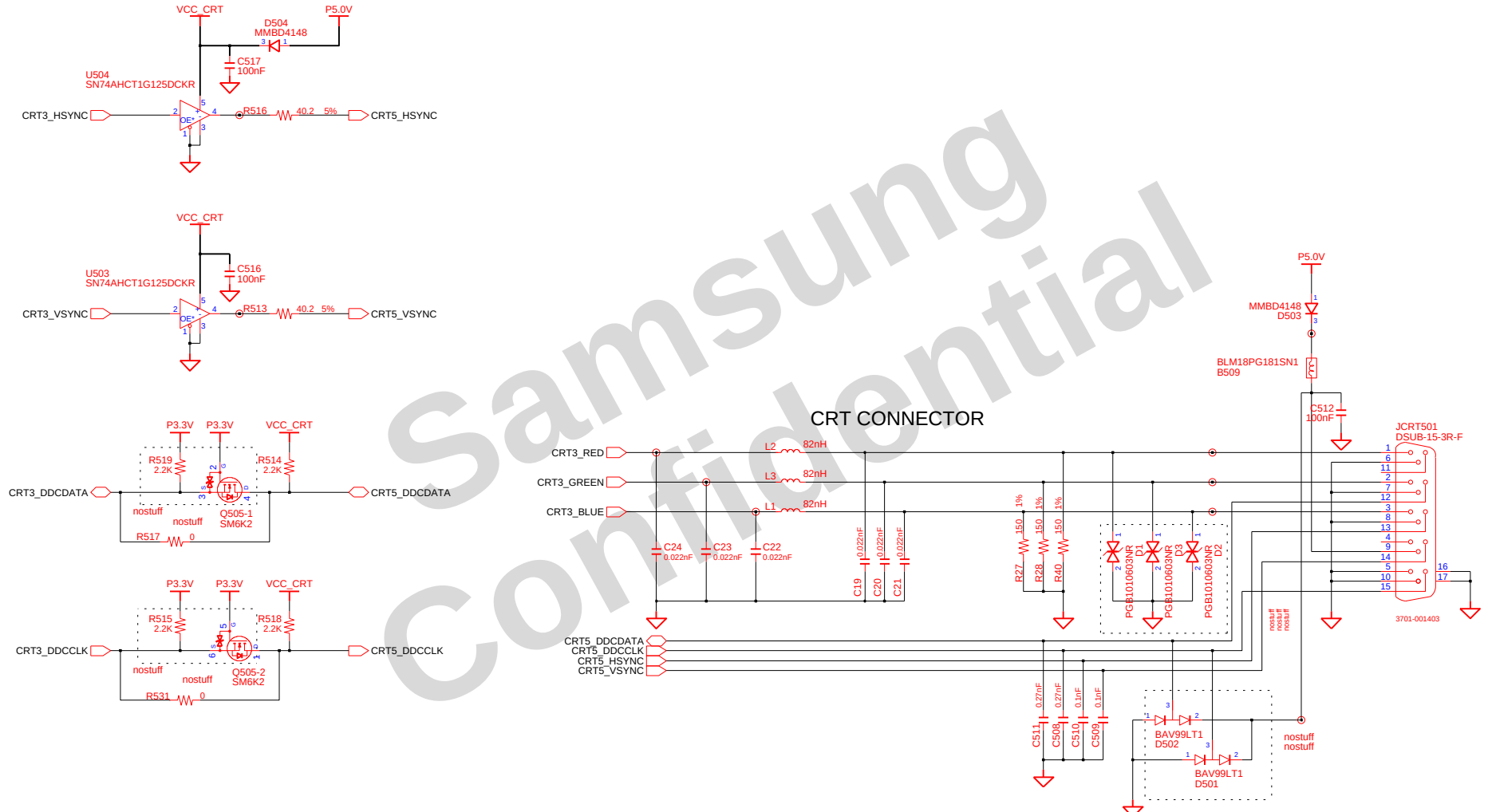
Place three 1nF capacitor around C-channel component



DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE			
CHECK	TH LEE	REV. STEP	MP				
APPROVAL	MK KIM	REV	REV 1.1	OSLO2 Graphics_Memory		PART NO.	BA41-00866A
MODULE CODE		LAST EDIT		Graphics_Memory.Nvidia #3			
				May 15, 2008 08:19:32 AM		PAGE	3 OF 3

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CRT CONNECTOR

DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	REV 1.1	
APPROVAL MK KIM	REV 1.1	LAST EDIT	
MODULE CODE	LAST EDIT		

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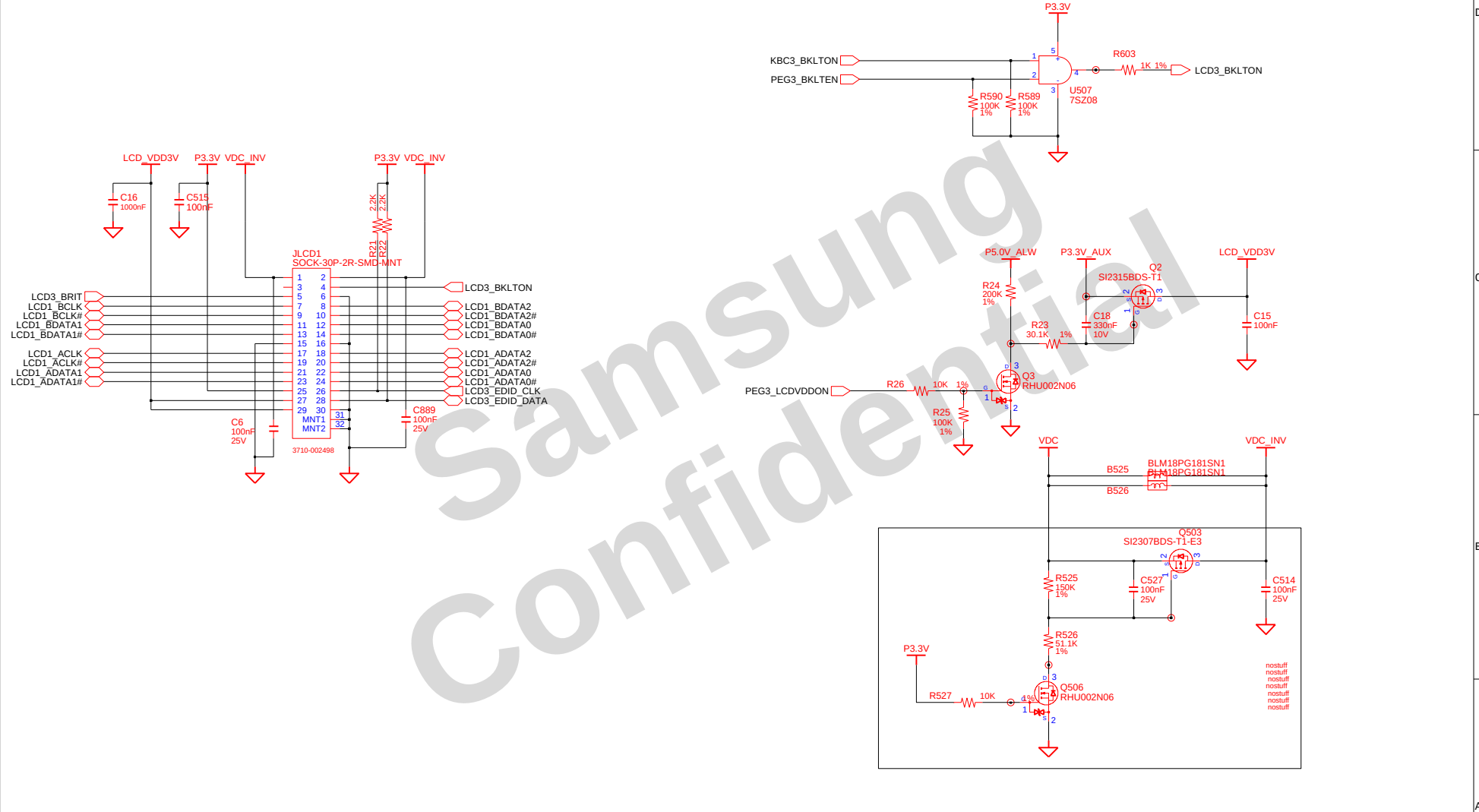
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D

C

B

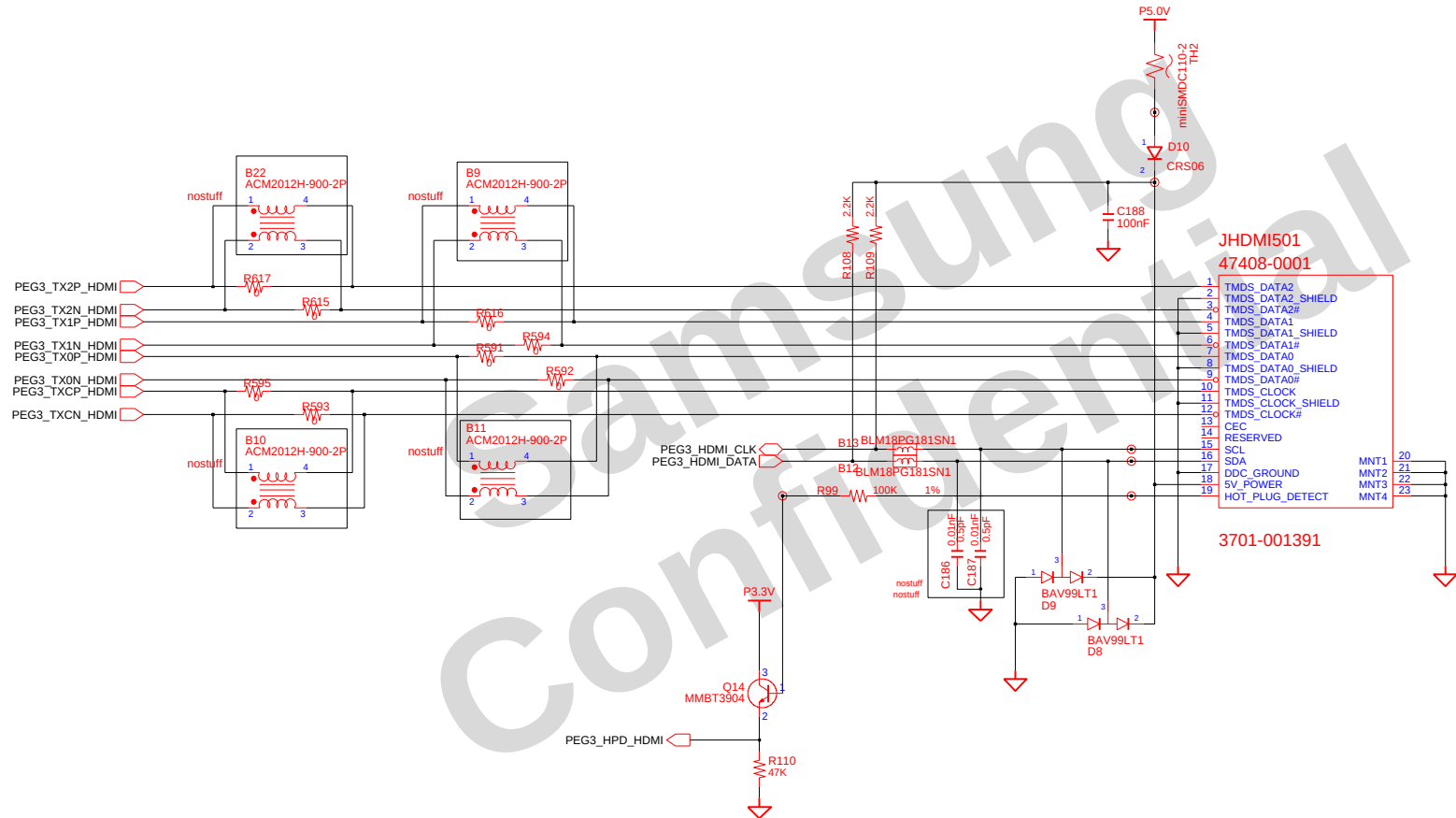
A



DRAW	MS YANG / Dany Lee	DATE	8/17/2007	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		UNDEFINED	
APPROVAL	MK KIM	REV	1.1			
MODULE CODE		LAST EDIT				
May 15, 2008 08:19:32 AM						PAGE 12
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DRAW MS YANG / Dany Lee	DATE 8/17/2007	TITLE OSL02 UNDEFINED	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 13 of 13

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U519 ALC262-VC2-GR

PC BEEP

For HDMI

ALL TYPE IS 1608

INSTPAR SHT510
R1608-SHORT

INSTPAR SHT519
R1608-SHORT

OSLO2
HDA_Codec_Alc262
HDA_Codec_Alc262 #1

SAMSUNG
ELECTRONICS
PART NO. BA41-00866A

DATE 8/12/2006
REV 1.1
LAST EDIT

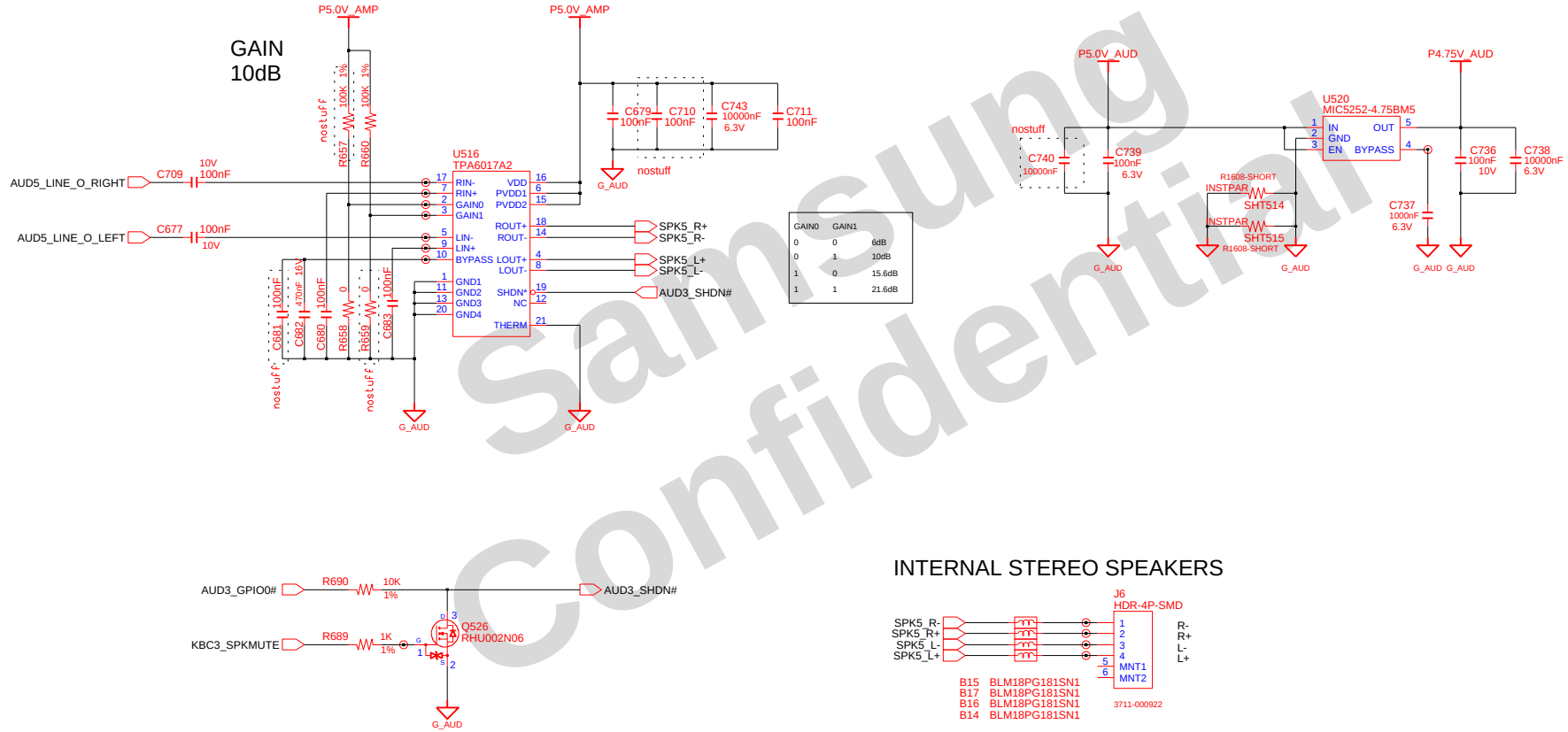
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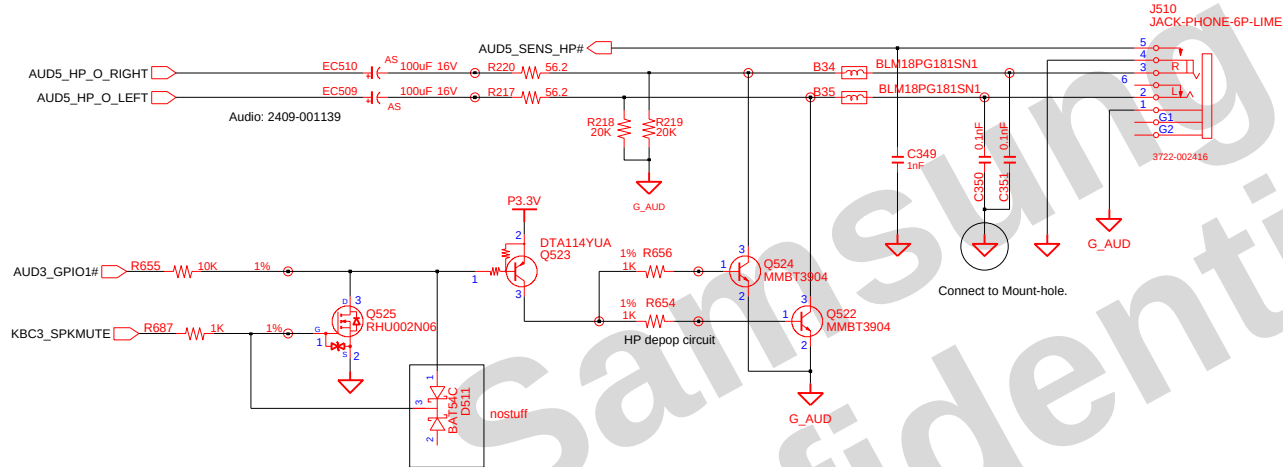
DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	HDA_Codec_Alc262	
APPROVAL MK KIM	REV 1.1	HDA_Codec_Alc262 #2	
MODULE CODE	LAST EDIT		

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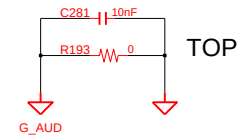
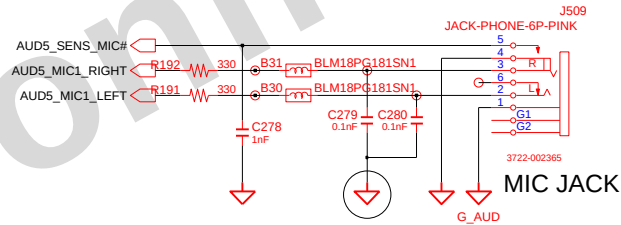
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HEADPHONE



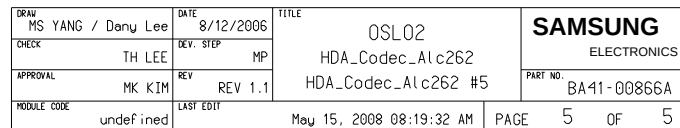
Connect to Mount-hole.



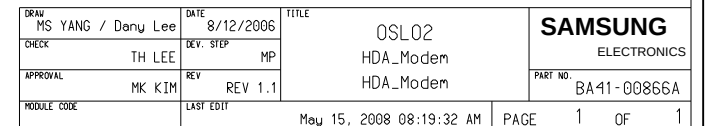
The traces led to Audio Jacks have the width over 10mil

DRW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	HDA_Codec_Alc262	
APPROVAL MK KIM	REV REV 1.1	HDA_Codec_Alc262 #4	
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 4 OF 5

A

[illegible]

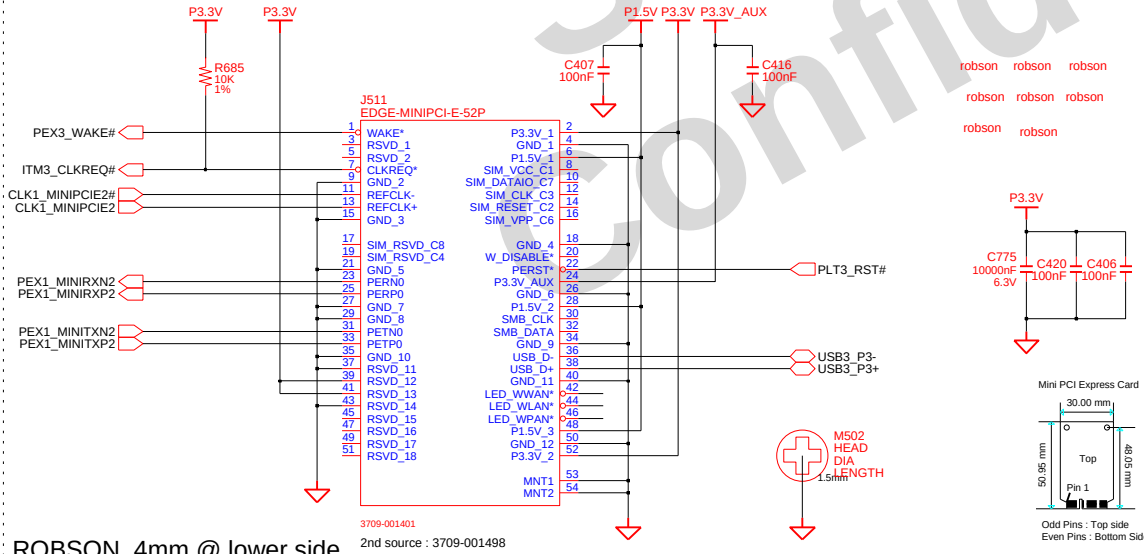
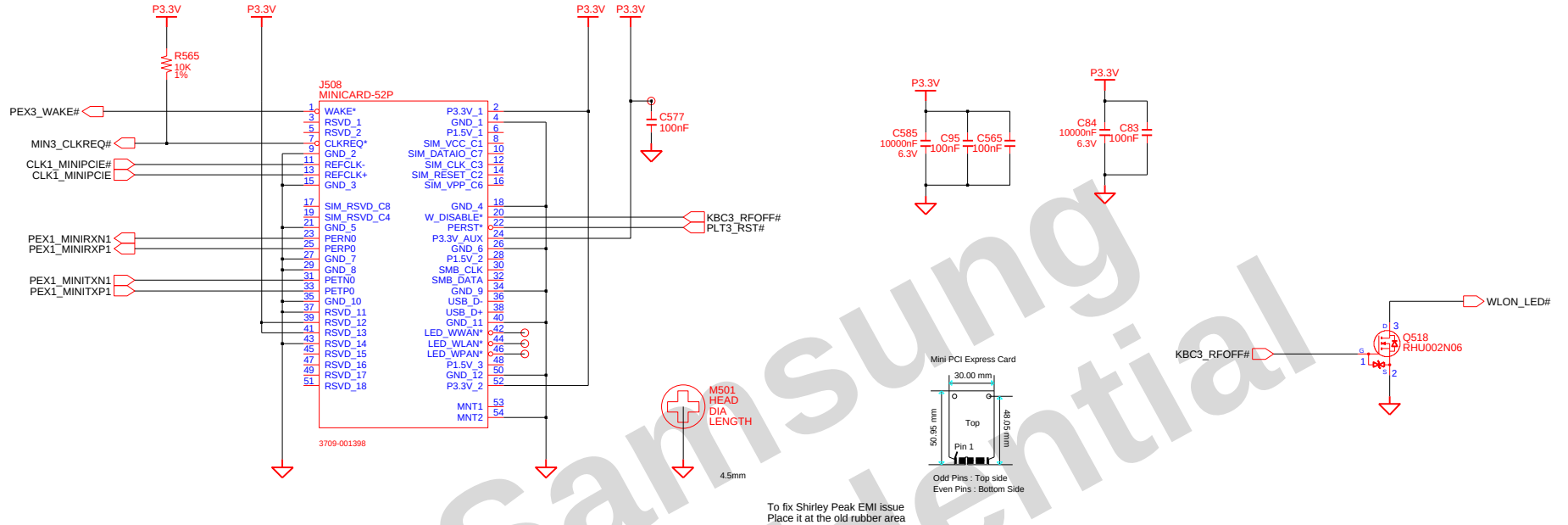
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WLAN, 7mm @ Upper side



ROBSON, 4mm @ lower side

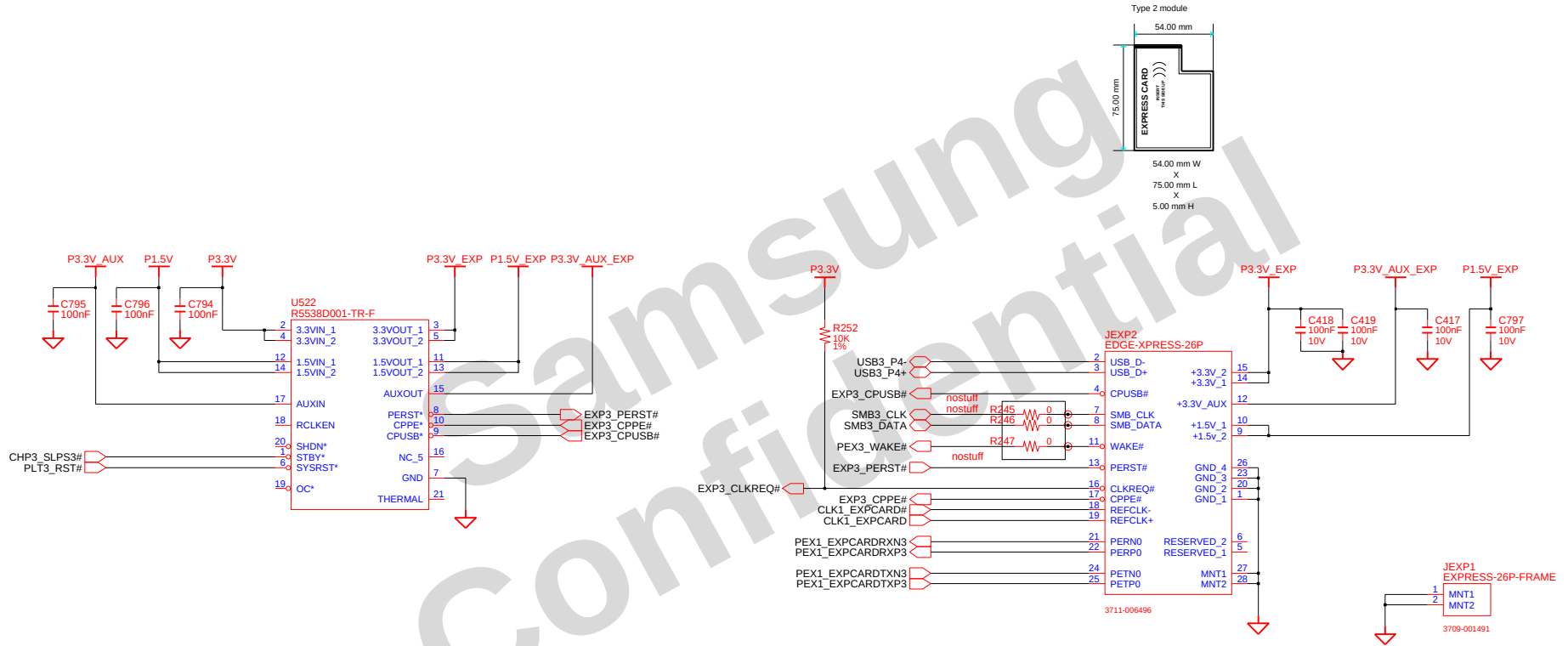
2nd source : 3709-001498

DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		PCIE_Minicard_Slot	
APPROVAL	MK KIM	REV	REV 1.1		PCIE_Minicard_Slot	PART NO. BA41-00866A
MODULE CODE	undefined	LAST EDIT				

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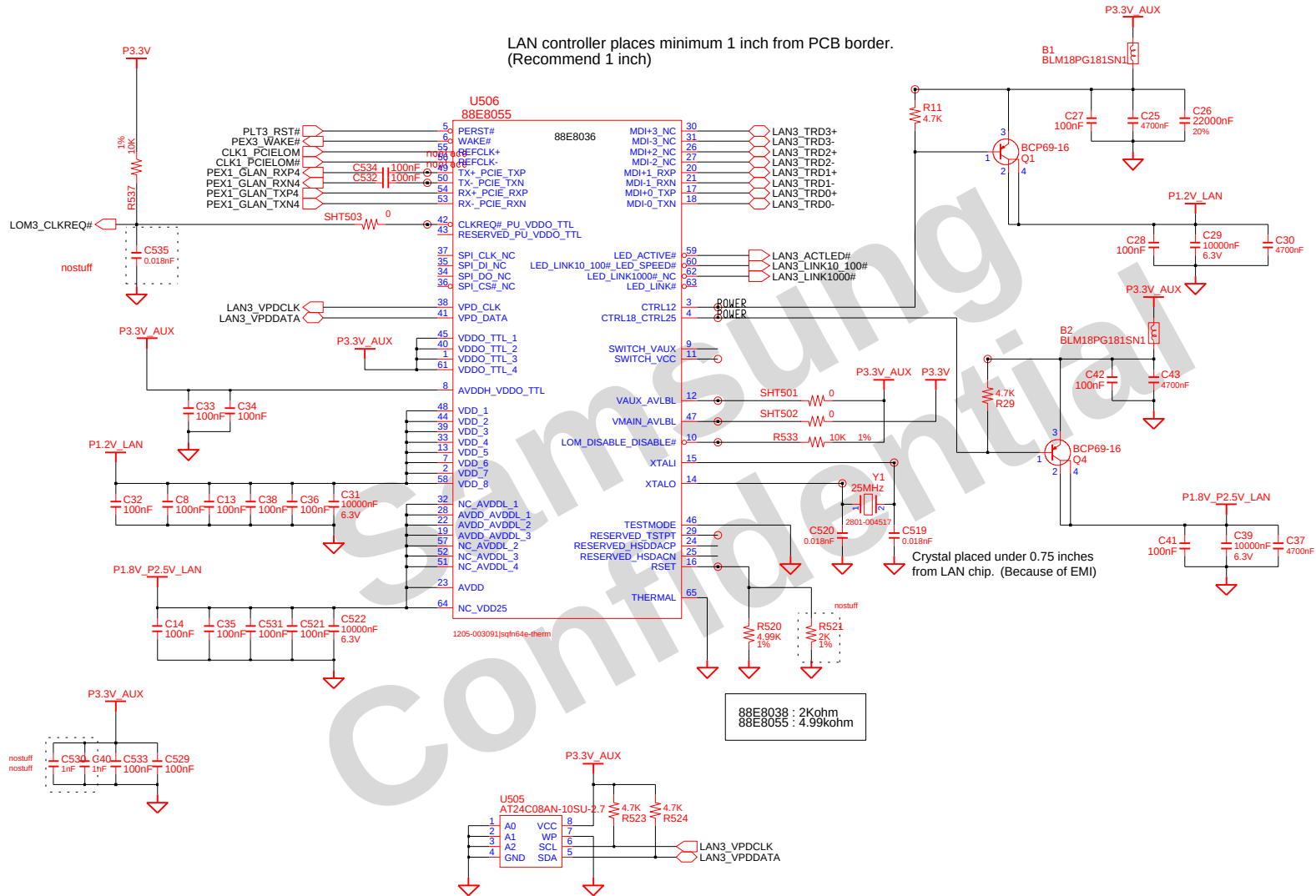


DRW MS YANG / Dany Lee	DATE	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP			
APPROVAL MK KIM	REV REV 1.1			PART NO. BA11-00866A
MODULE CODE undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	OF

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LAN controller places minimum 1 inch from PCB border.
(Recommend 1 inch)

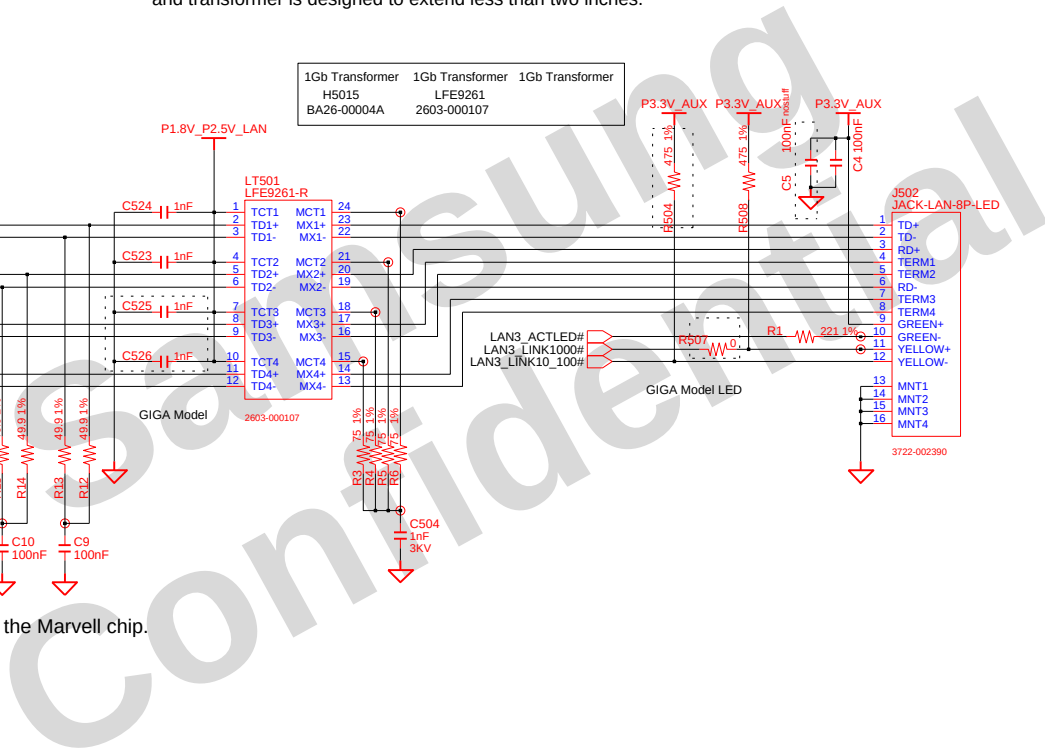


DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	LAN_Marvell_8055	
APPROVAL MK KIM	REV REV 1.1	LAN_Marvell_8055	
MODULE CODE	LAST EDIT		

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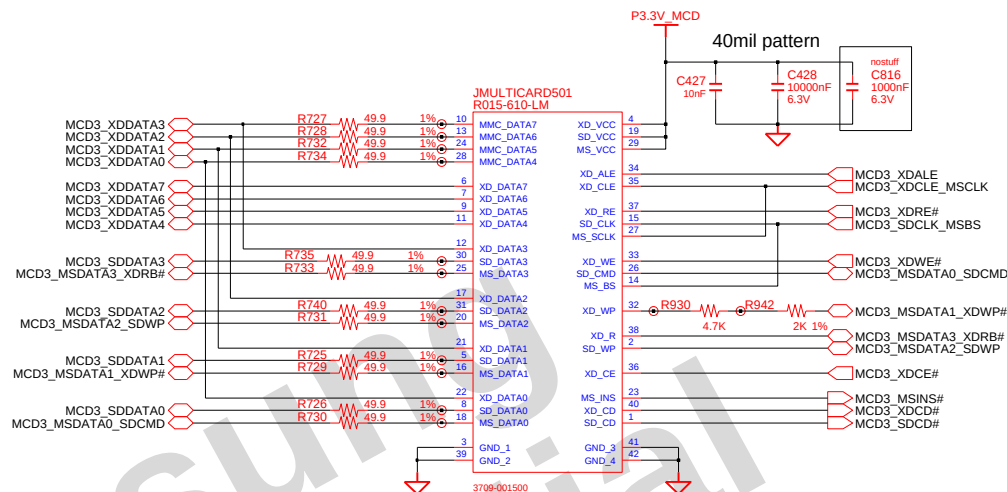
Place near to the Marvell chip.



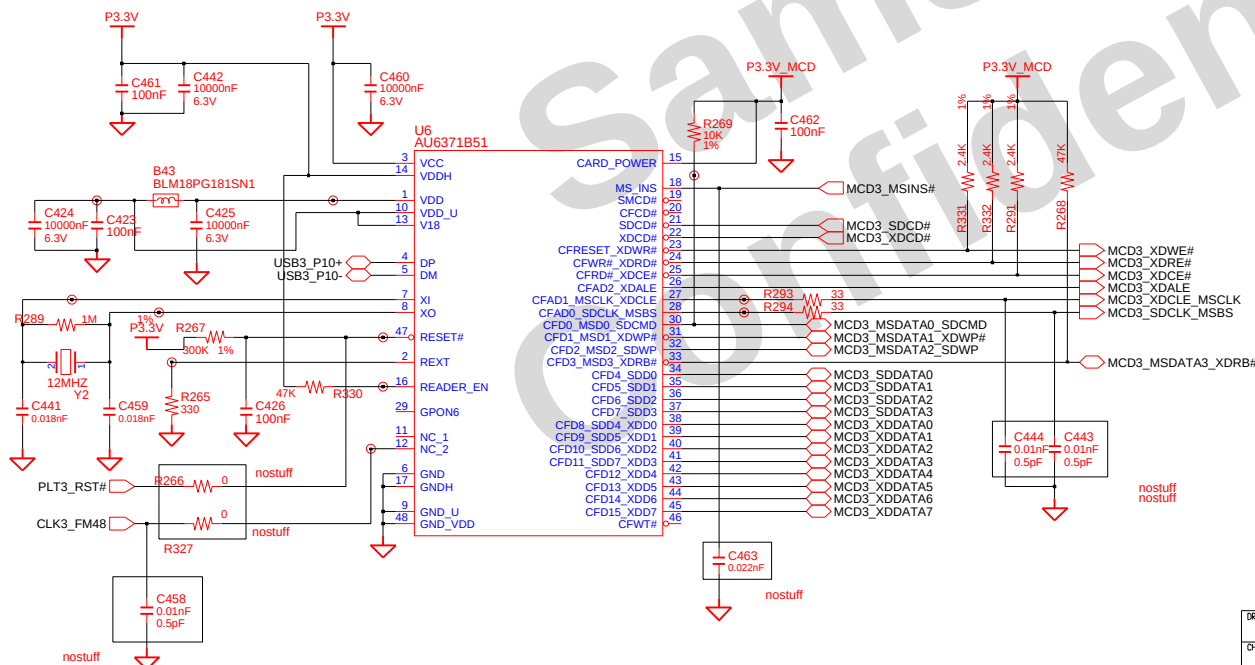
DRAW MS YANG / Dany Lee		DATE 8/12/2006	
CHECK TH LEE		DEV. STEP MP	
APPROVAL MK KIM		REV REV 1.1	
MODULE CODE		LAST EDIT	

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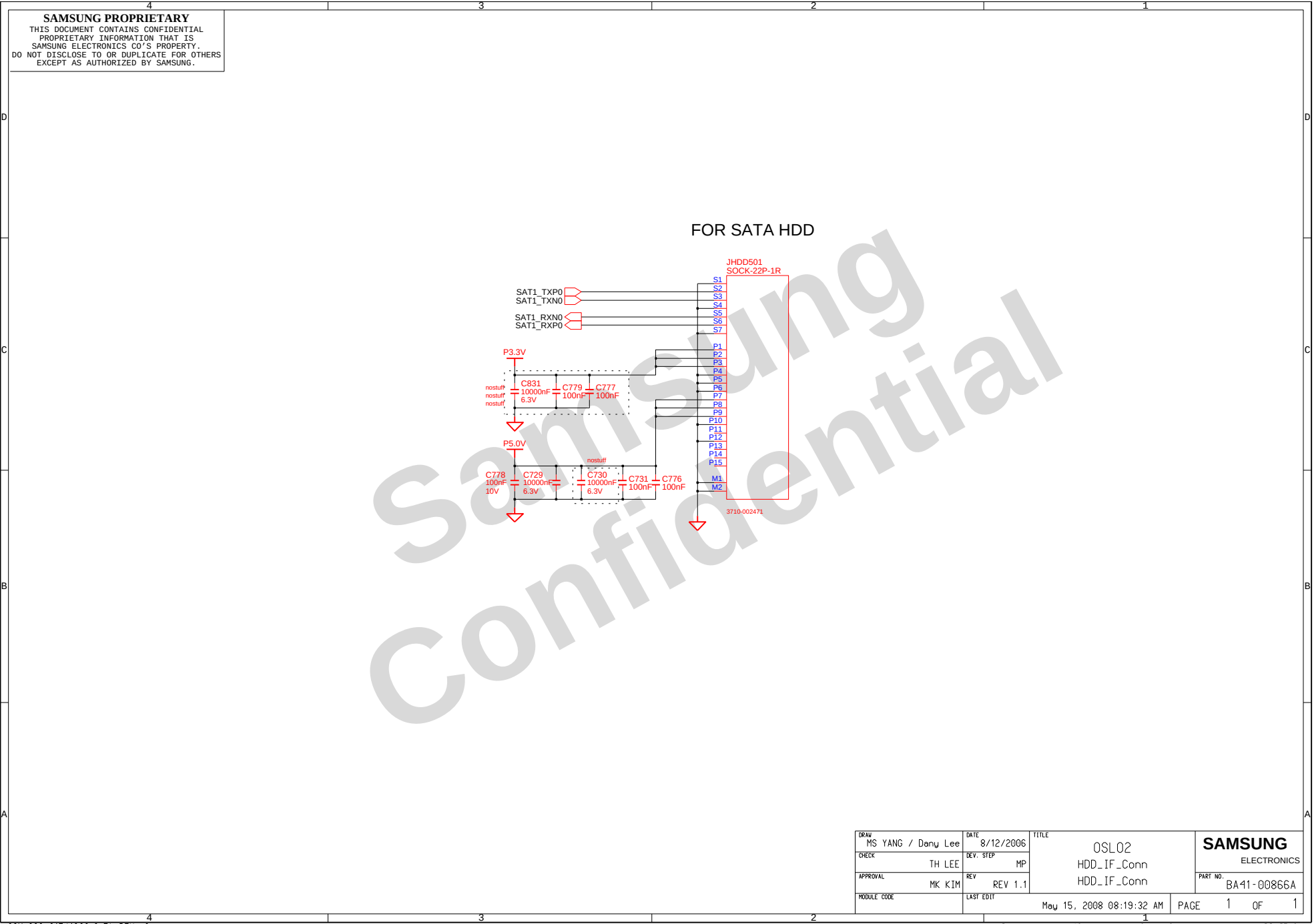
P3.3V_MCD distance between Controller and socket should be less than 2 inches

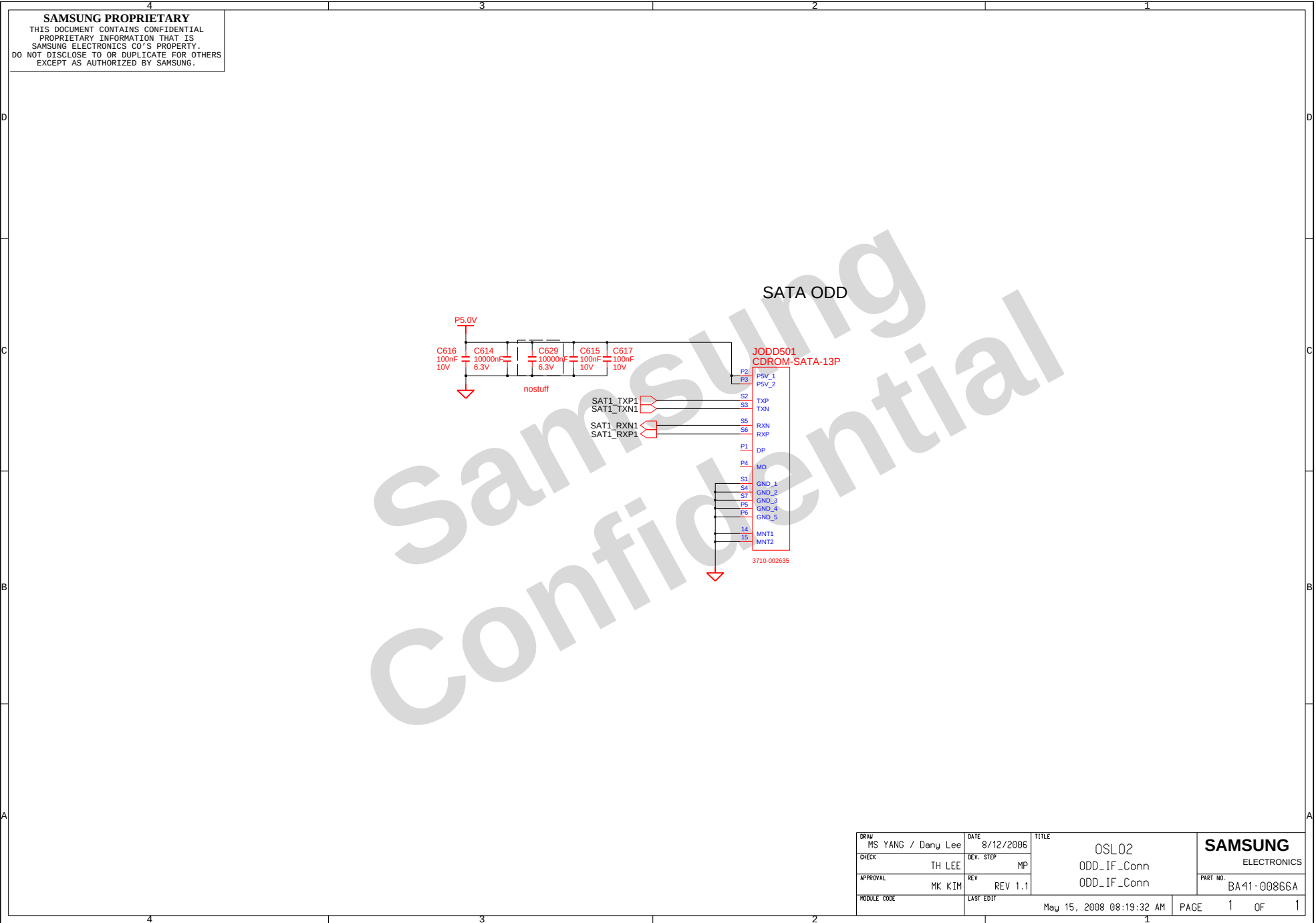


40 mil trace for medica card socket ground



DRAW	MS YANG / Dany Lee	DATE	8/17/2007	TITLE	OSL02 UNDEF INED	
CHECK	TH LEE	DEV. STEP	MP			
APPROVAL	MK KIM	REV	REV 1.1		PART NO.	
MODULE CODE		LAST EDIT		May 15, 2008 08:19:32 AM	PAGE 15	



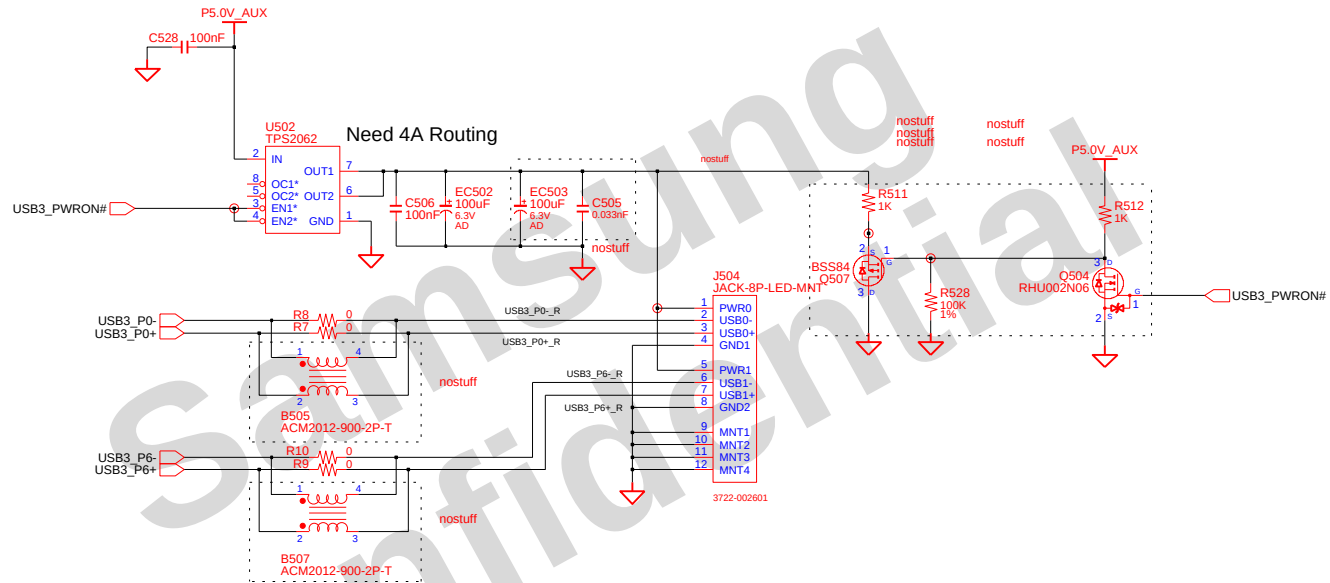


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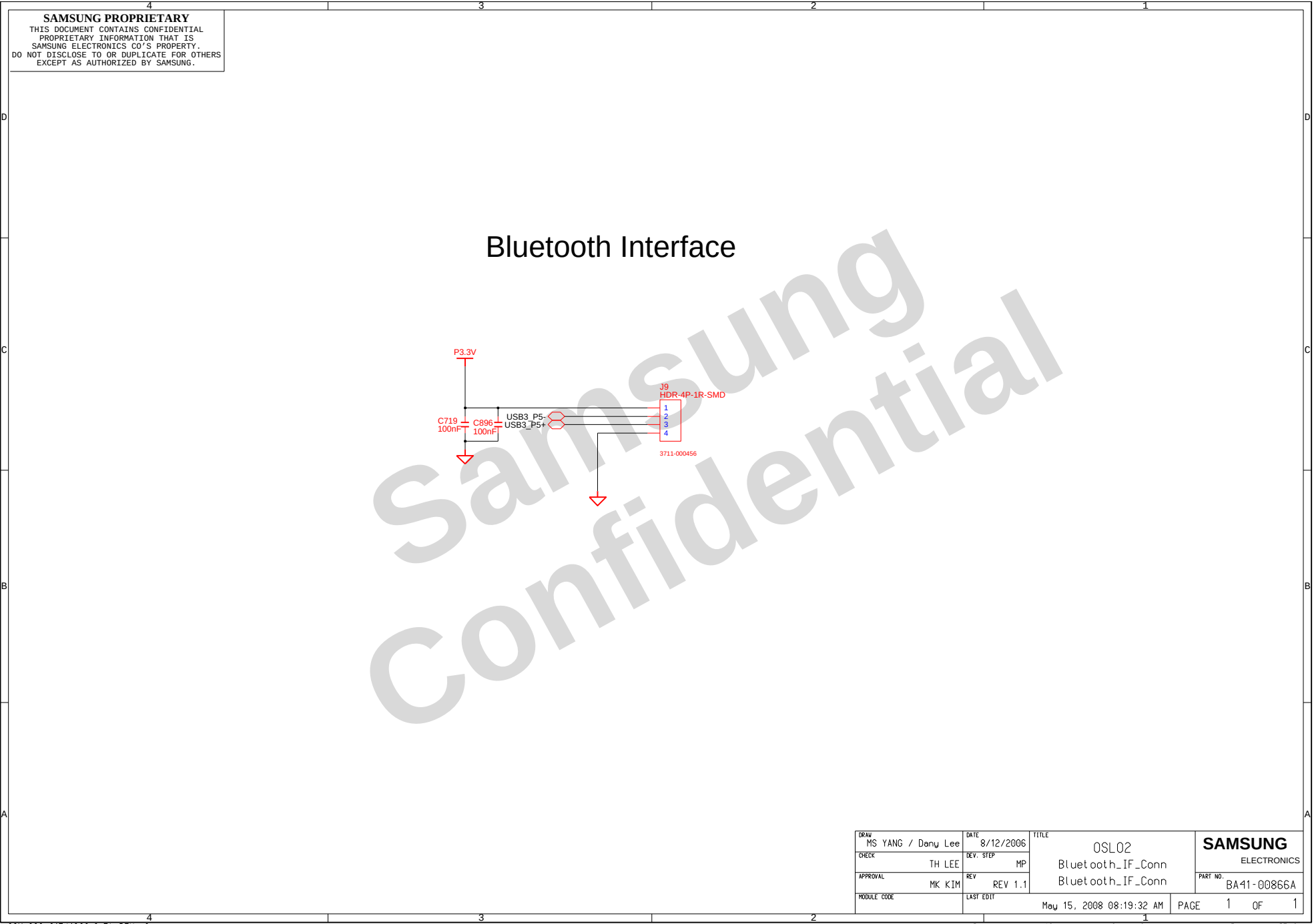
DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP	ODD_IF_Conn	
APPROVAL MK KIM	REV REV 1.1	ODD_IF_Conn	PART NO. BA41-00866A
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1

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2 PORT USB CONNECTOR



DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 USB_2Port USB_2Port	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	REV REV 1.1	
APPROVAL MK KIM	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1
MODULE CODE			



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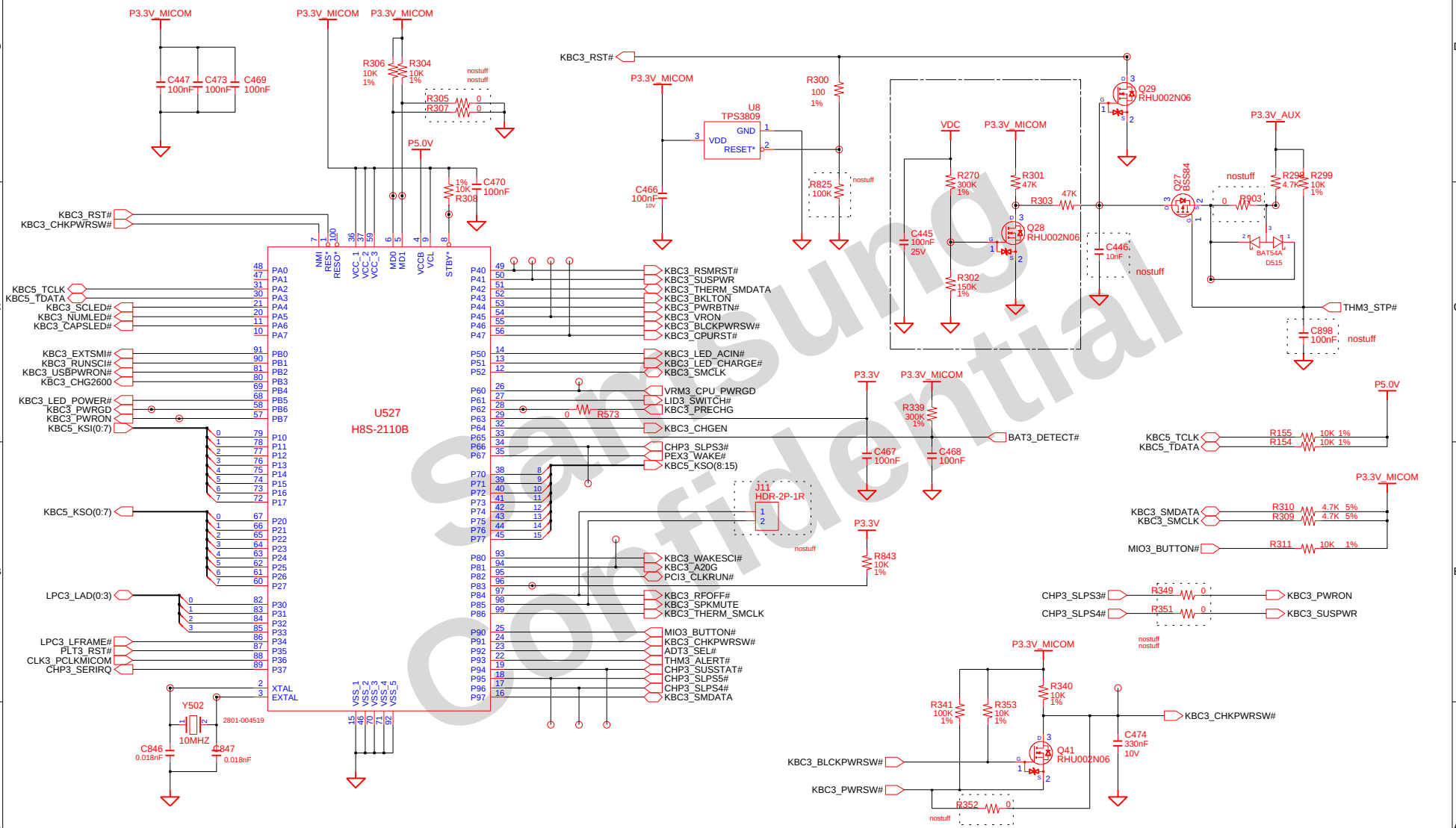
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COM-22C-015(1996.6.5) REV. 3



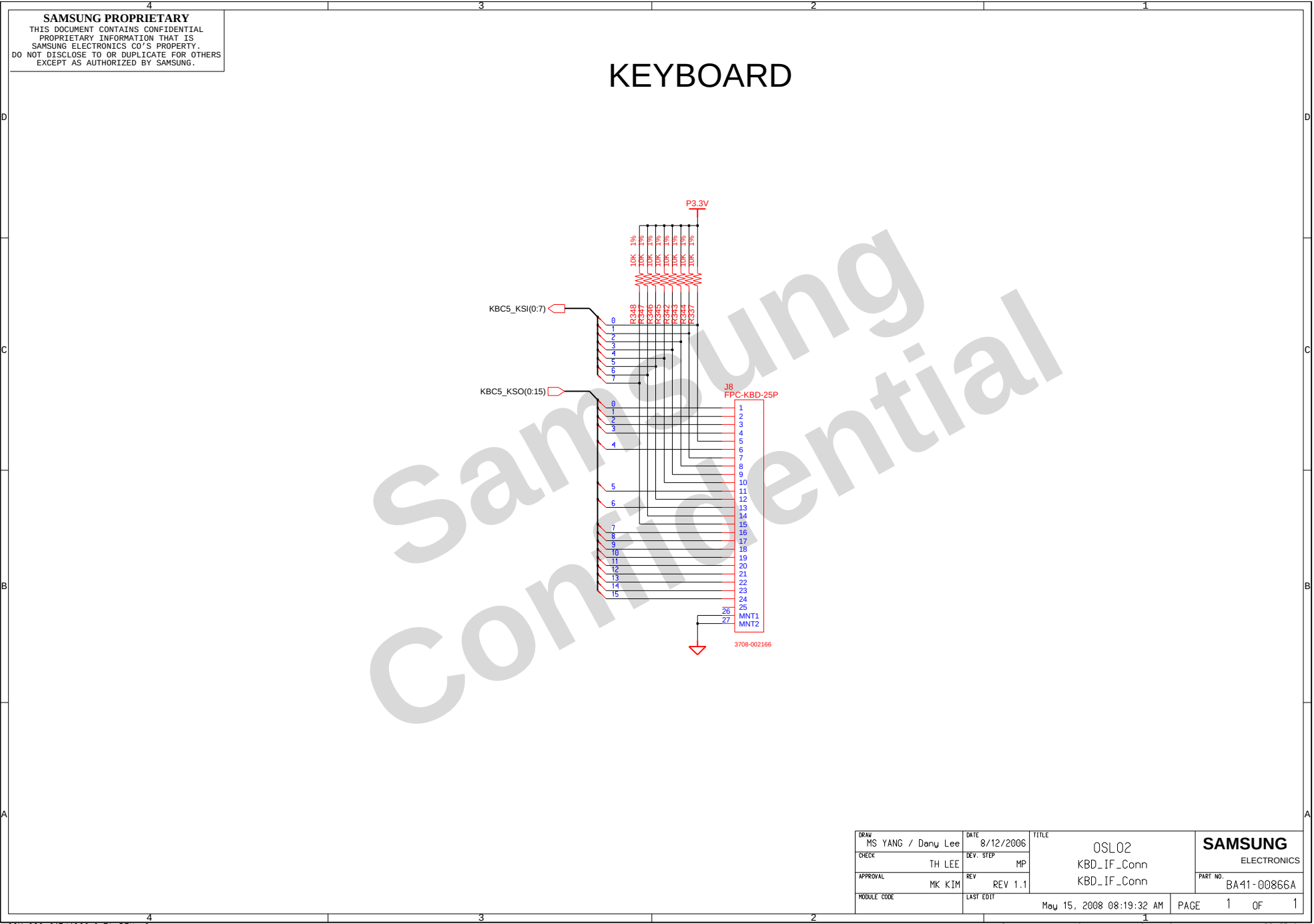
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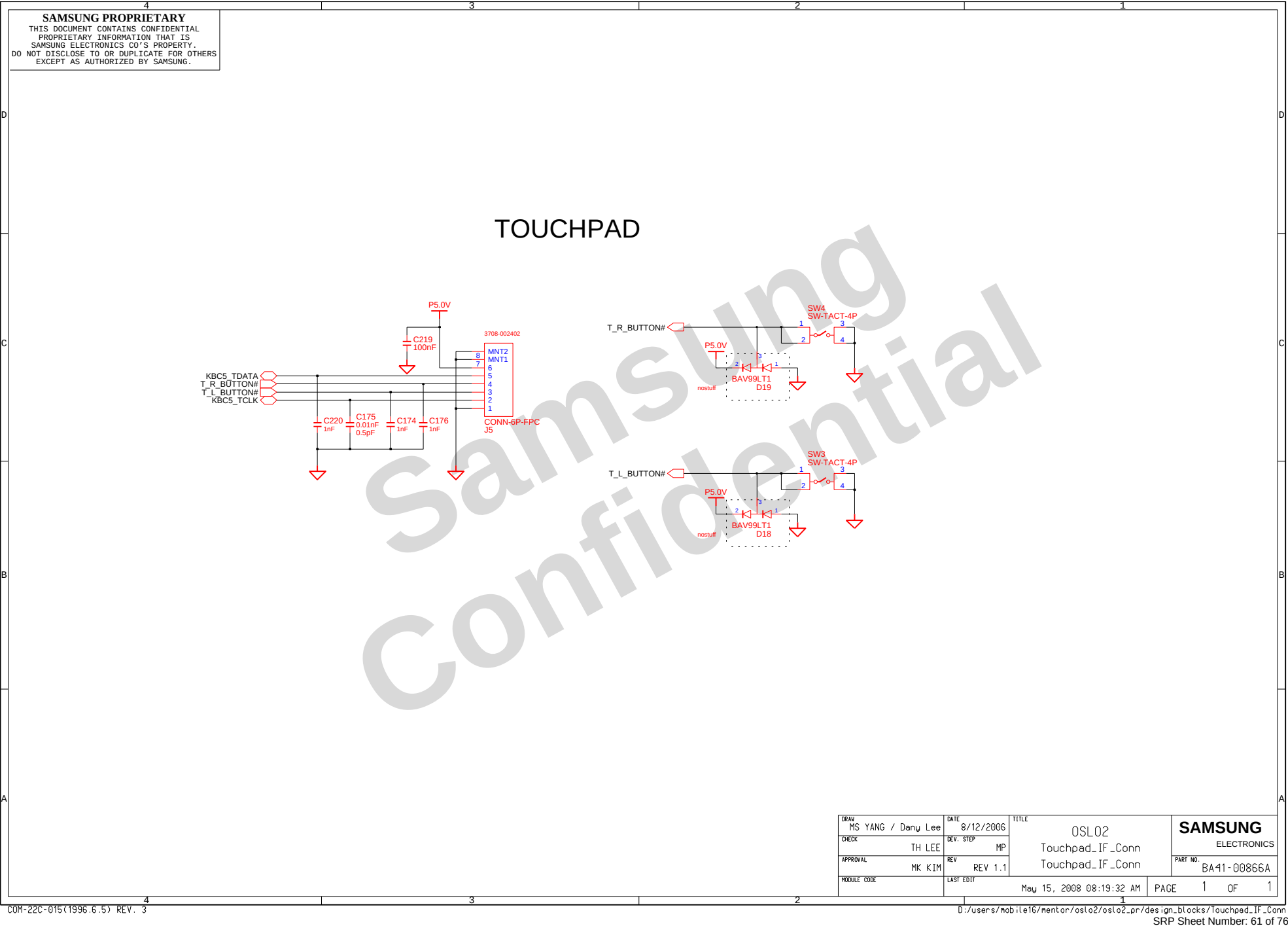
MICOM RESET

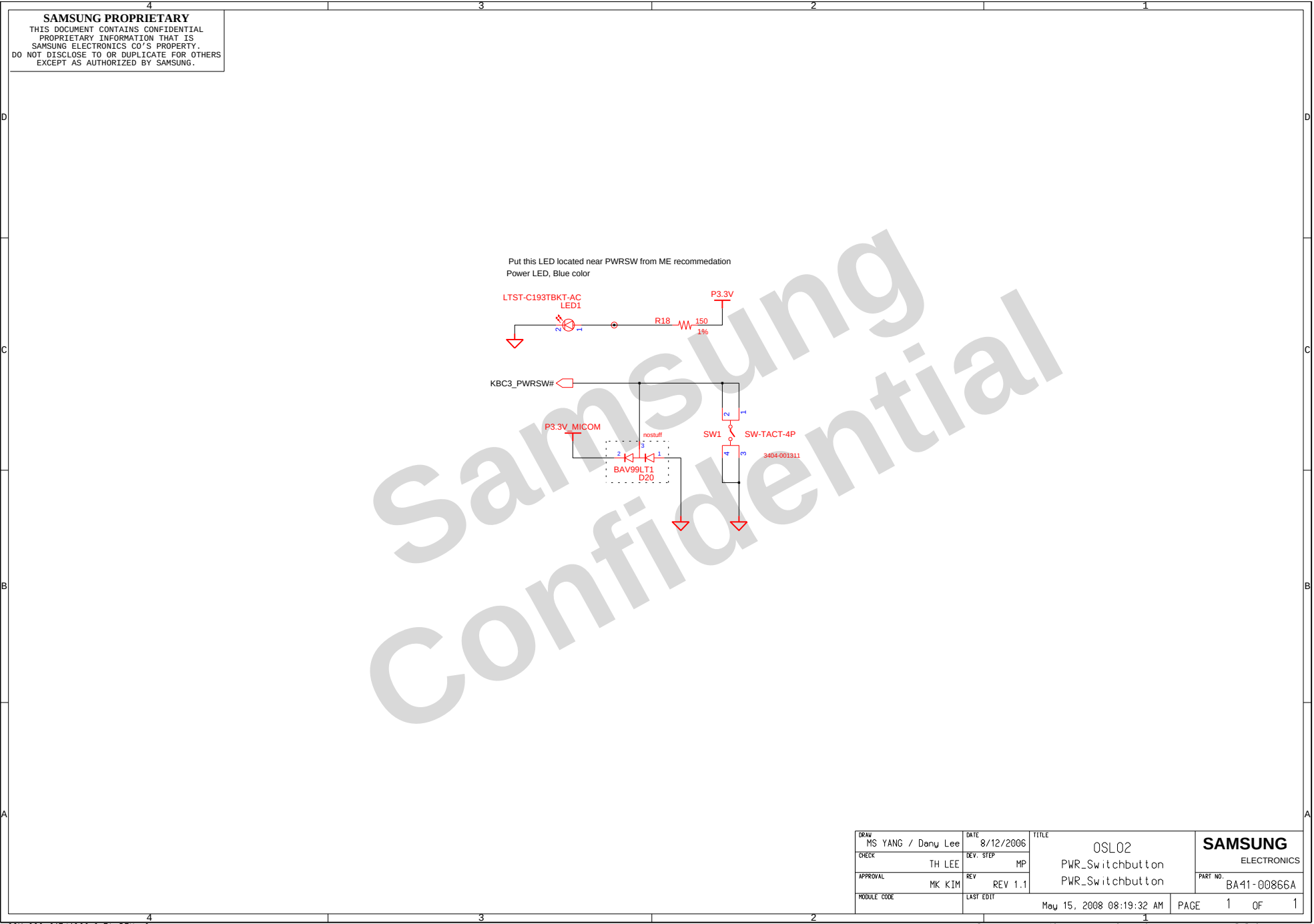


POWER SWITCH BLOCK WHILE MICOM UPDATE

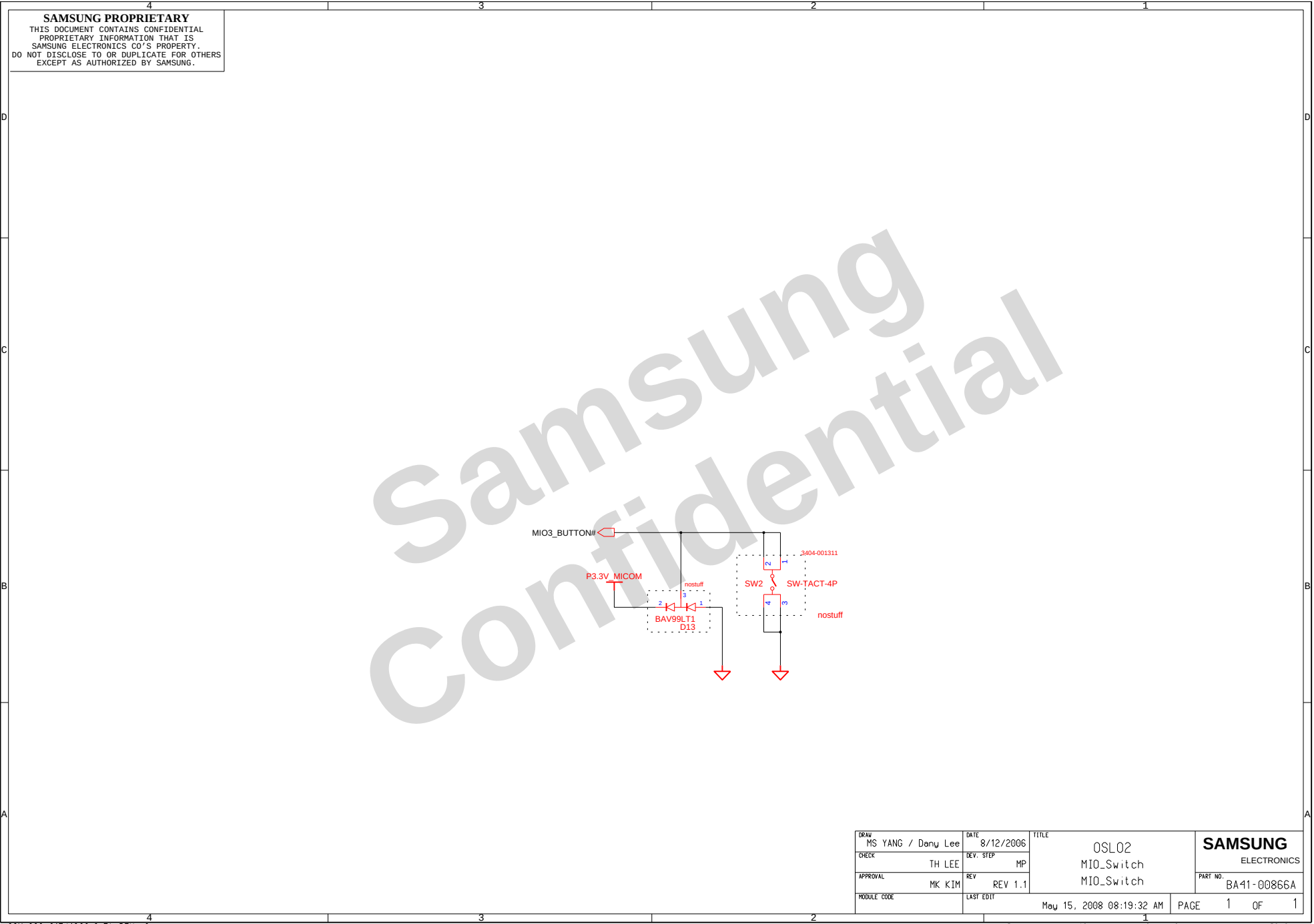
DRAWN BY MS YANG / Dany Lee		DATE 8/12/2006		TITLE OSL02			
CHECK TH LEE		REV. STEP MP		MICOM_Renesas2110-100p			
APPROVAL MK KIM		REV REV 1.1		MICOM_Renesas2110-100p		PART NO. BA41-00866A	
MODULE CODE		LAST EDIT		May 15, 2008 08:19:32 AM		PAGE 1 OF 1	







DRW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP	PWR_Switchbutton	
APPROVAL MK KIM	REV REV 1.1	PWR_Switchbutton	PART NO. BA41-00866A
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1



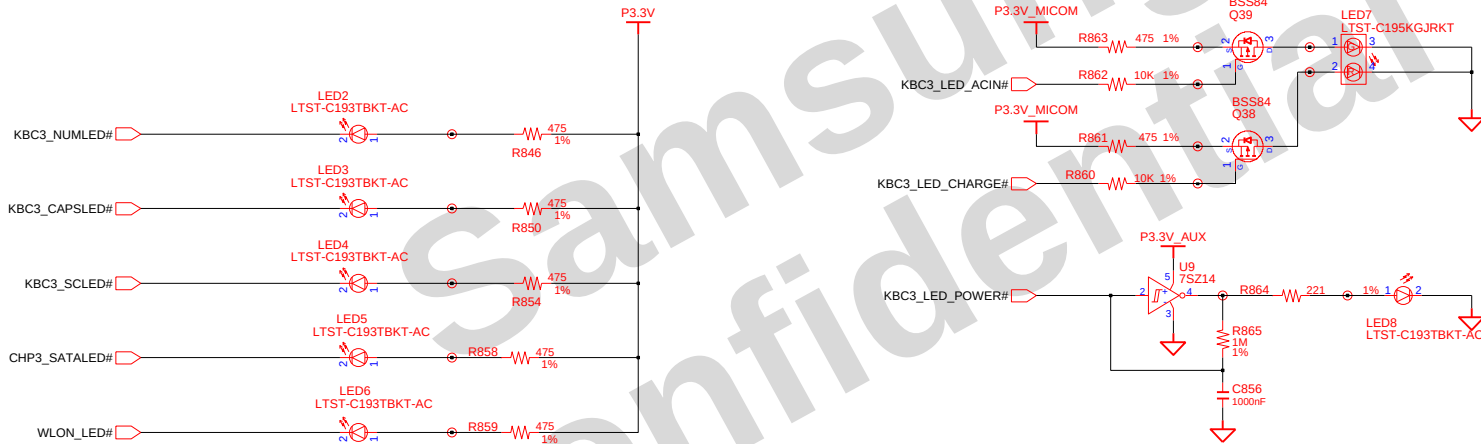
DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		MIO_Switch	
APPROVAL	MK KIM	REV	REV 1.1		MIO_Switch	PART NO. BA41-00866A
MODULE CODE		LAST EDIT				

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ADAPTERIN/CHARGING LED



DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA41-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1

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D

C

B

A

LID_SWITCH

P3.3V

C1 100nF

U1 A3212ELH/HED55XXU12

1 SUPPLY

3 OUTPUT

2

R2 20K 1%

LID3_SWITCH#

DRW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	LID_Switch	LID_Switch	
APPROVAL	MK KIM	REV	REV 1.1	LID_Switch	LID_Switch	
MODULE CODE	LAST EDIT			May 15, 2008 08:19:32 AM	PAGE	1 OF 1

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D:/users/nobile16/nentor/oslo2/oslo2.pr/design_blocks/LID_Switch
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D

C

B

A

LID_SWITCH

P3.3V

C1 100nF

U1 A3212ELH/HED55XXU12

1 SUPPLY

2 OUTPUT

3 GND

P3.3V

R2 20K 1%

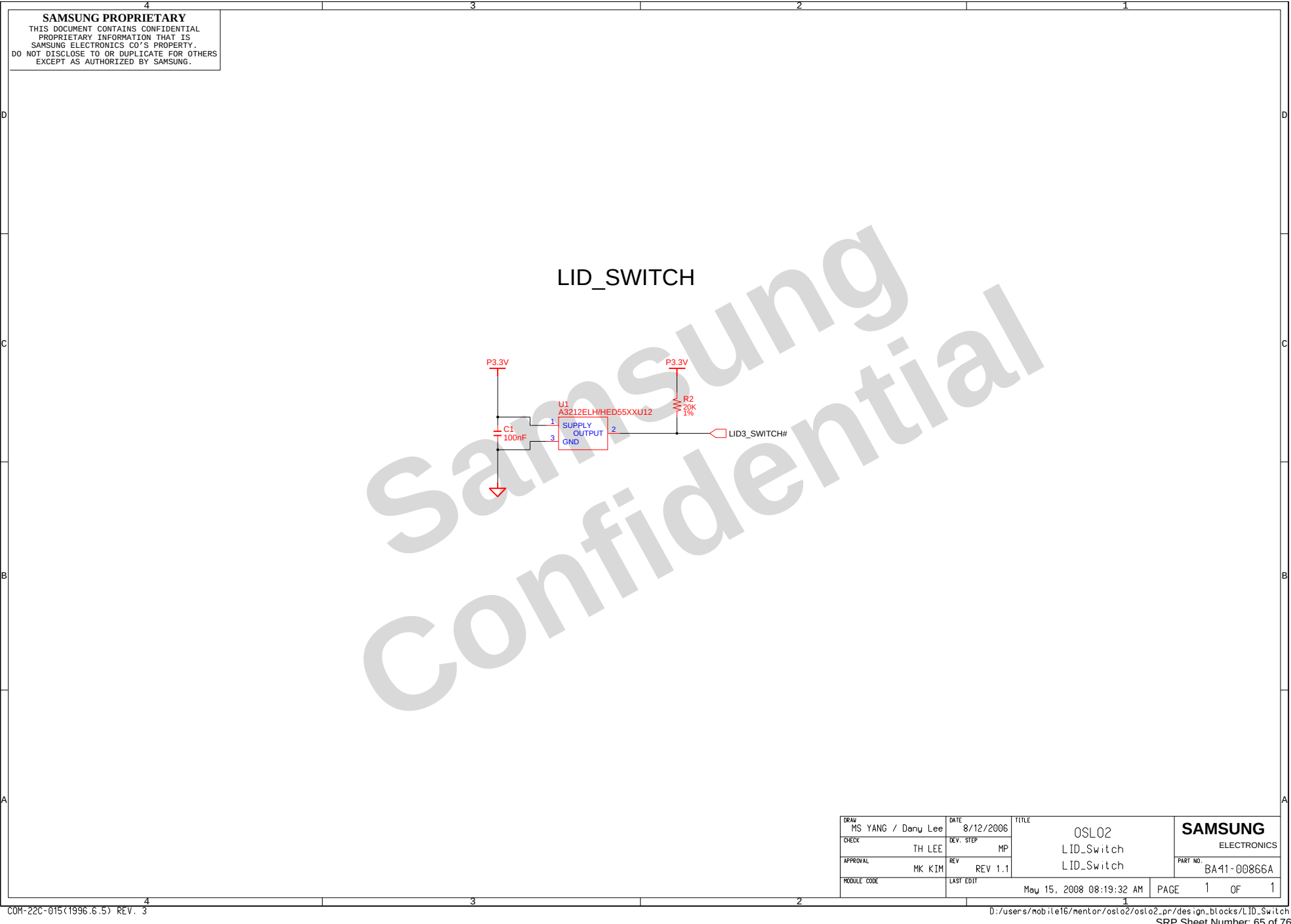
LID3_SWITCH#

DRW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	LID_Switch	LID_Switch	
APPROVAL	MK KIM	REV	REV 1.1			
MODULE CODE	LAST EDIT			May 15, 2008 08:19:32 AM	PAGE	1 OF 1

1

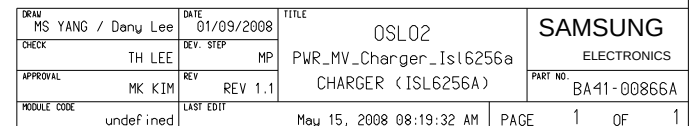
CON-22C-015(1996.6.5) REV. 3

D:/users/nobile16/nentor/oslo2/oslo2.pr/design_blocks/LID_Switch
SRP Sheet Number: 65 of 76



<

CHARGER & POWER MANAGEMENT

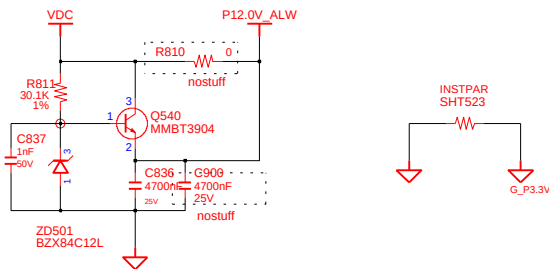


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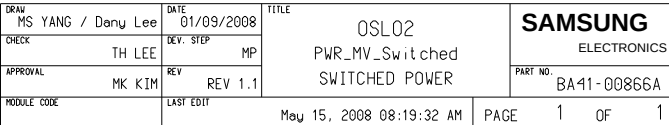
P3.3V_AUX & P5.0V_AUX

TONSEL VREF2
5V / 3.3V : 280KHz / 430KHz
(4.5A)

P12V ALW



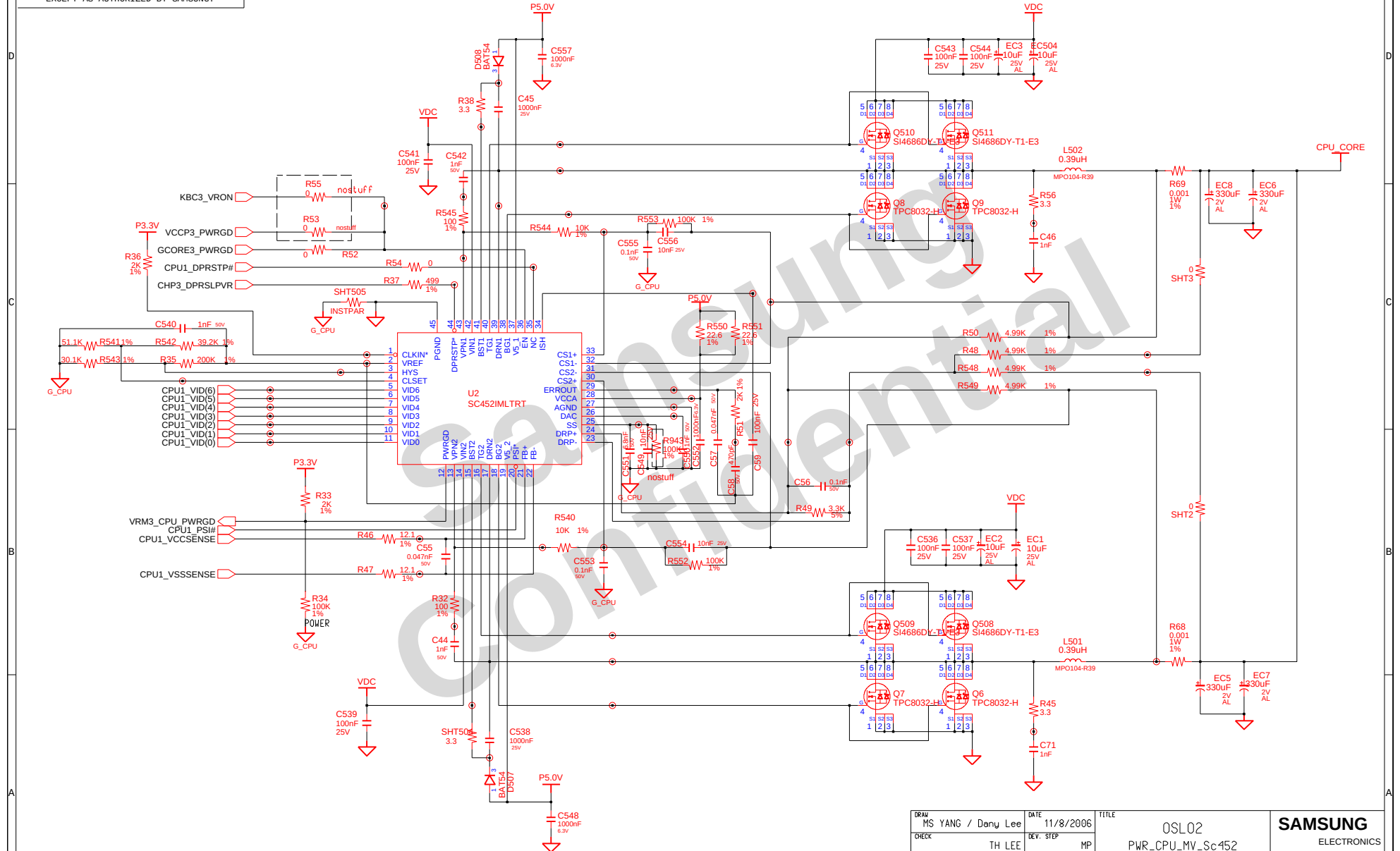
DRAW MS YANG / Dany Lee		DATE 11/8/2006		TITLE OSL02 PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX		 SAMSUNG ELECTRONICS	
CHECK TH LEE		DEV. STEP MP					
APPROVAL MK KIM		REV REV 1.1		PART NO.		BA41-00866A	
MODULE CODE undefined		LAST EDIT May 15, 2008 08:19:32 AM		PAGE 1		OF 1	



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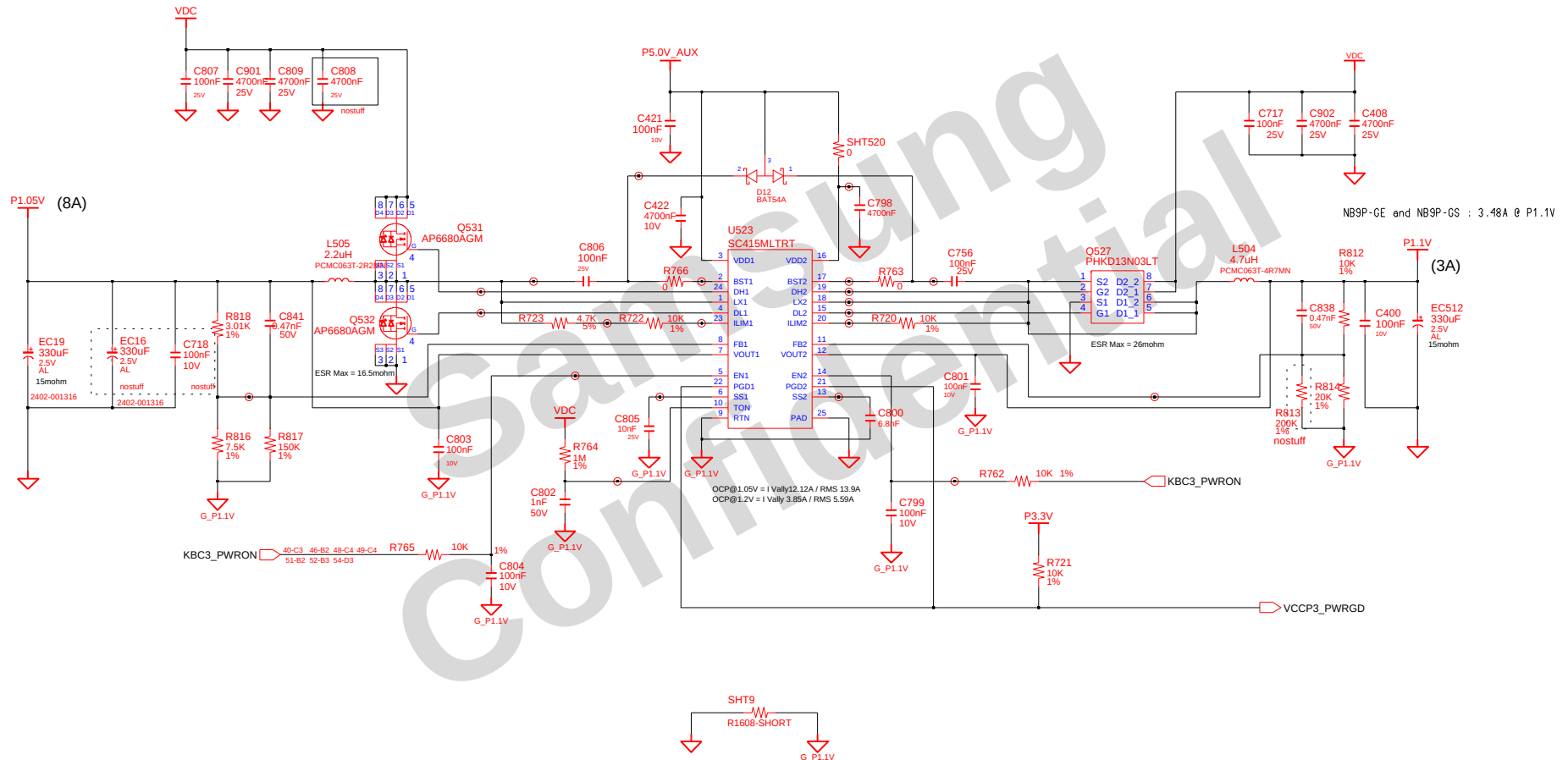
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CPU VRM [SEMTECH]



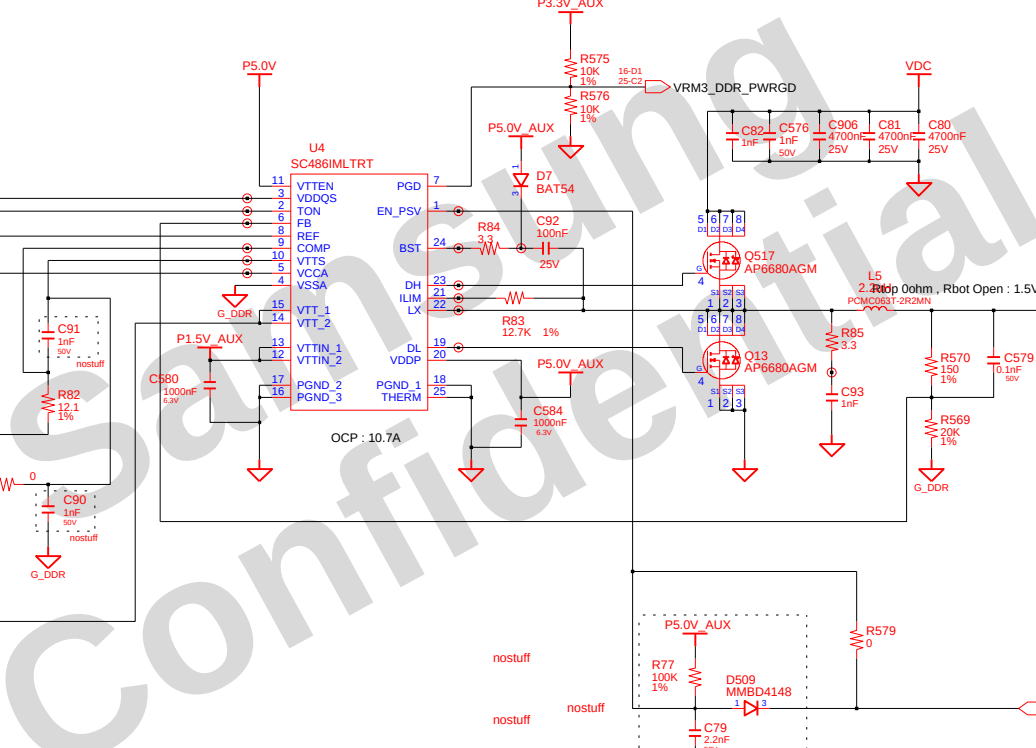
DRAW MS YANG / Dany Lee	DATE 11/8/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	PWR_CPU_MV_Sc452	
APPROVAL MK KIM	REV 1.1	CPU VRM (IMVP6+)	
MODULE CODE undefined	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

CHIPSET POWER(P1.05V & P1.1V)



DRAW	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02	SAMSUNG
CHECK	TH LEE	REV.	STEP	MP	PWR_MV_Cantiga	ELECTRONICS
APPROVAL	MK KIM	REV	1	Chipset Power (P1.05V-M, P1.1V)	BA41-00866A	
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	OF 1

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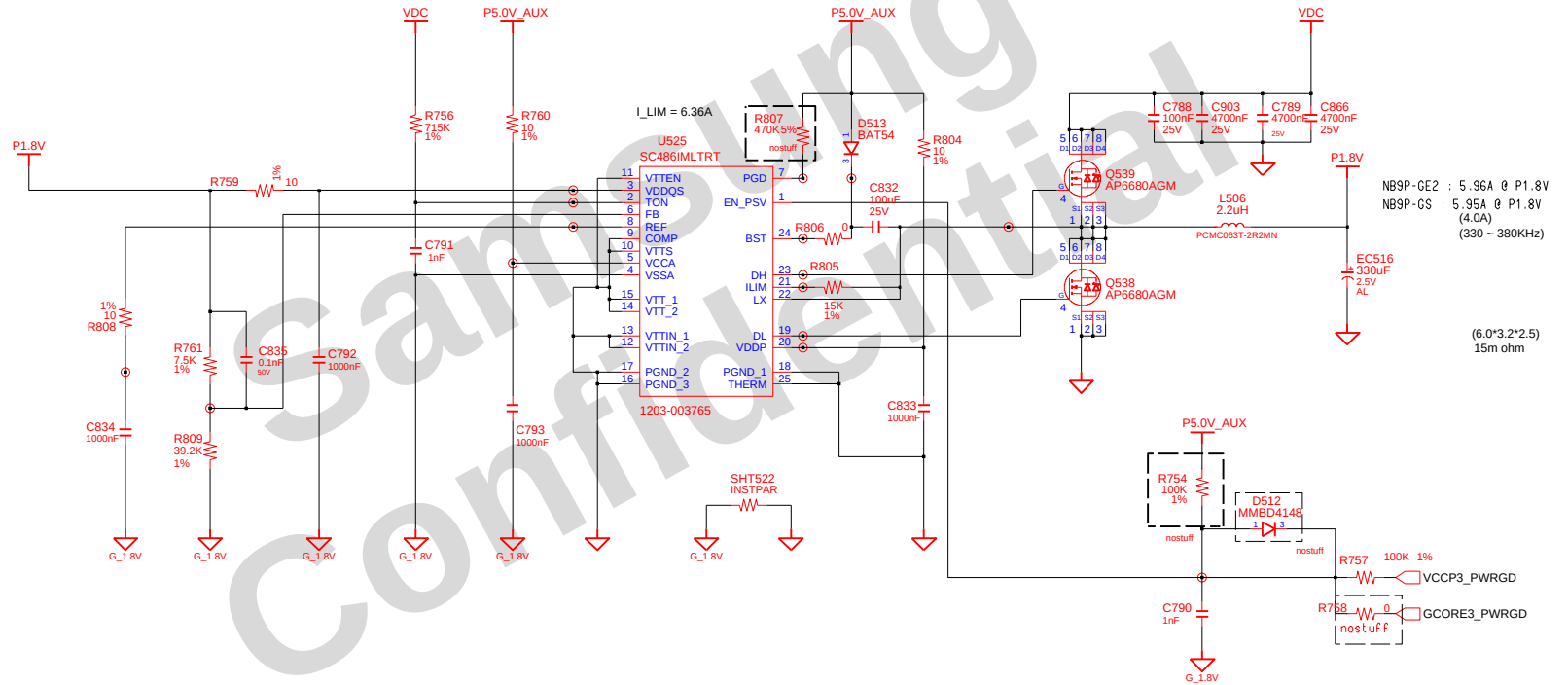


D:/users/mobile16/mentor/oslo2/oslo2_pr/design_blocks/PWR_MV_Memory

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P1.8V (External Gfx Memory)



NB9P-GE2 : 5.96A @ P1.8V
NB9P-GS : 5.95A @ P1.8V
(4.0A)
(330 ~ 380KHz)

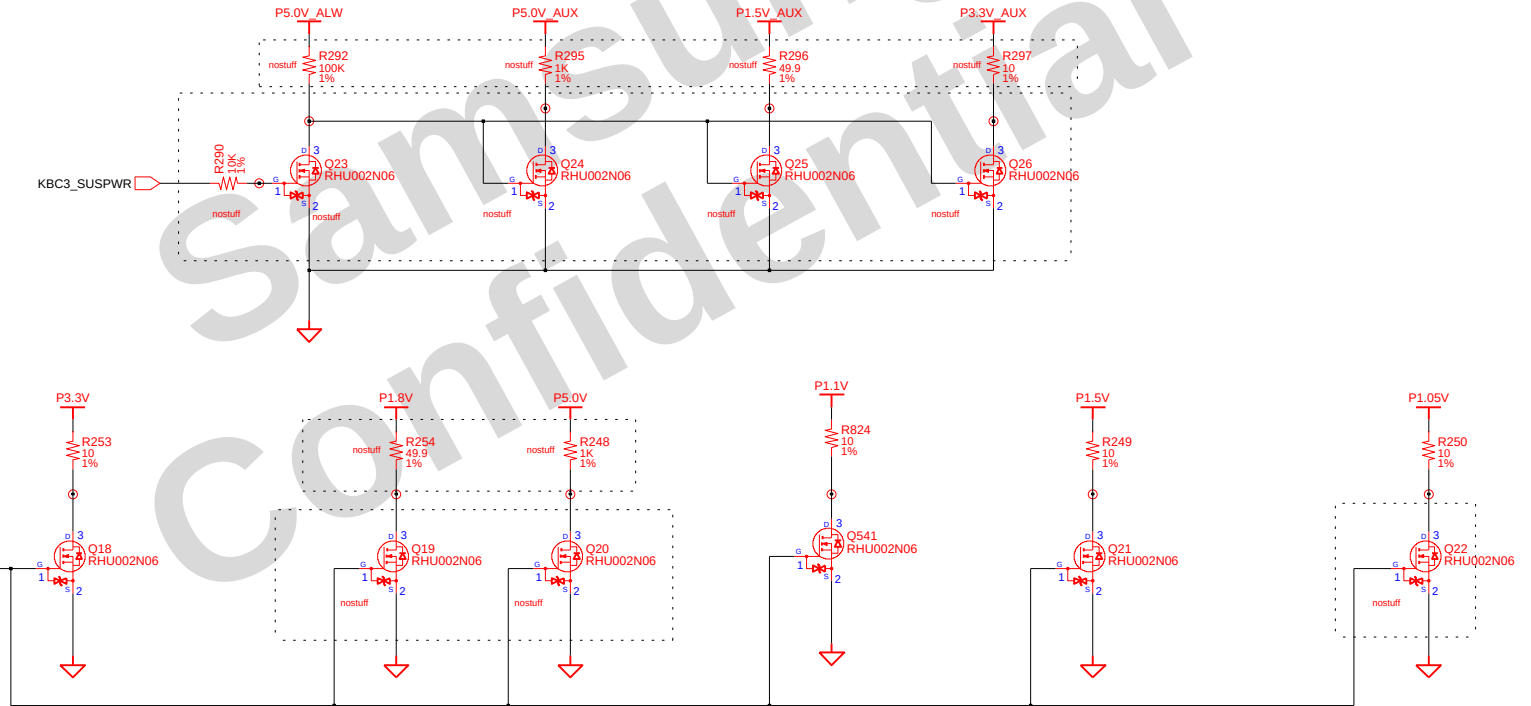
(6.0*3.2*2.5)
15m ohm

DRW MS YANG / Dany Lee	DATE 8/14/2007	TITLE OSL02 PWR_Gfx_MV_Ext Ext Gfx Memory(SC486)	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP	REV REV 1.1	PART NO. BA11-00866A
APPROVAL MK KIM	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 2
MODULE CODE			

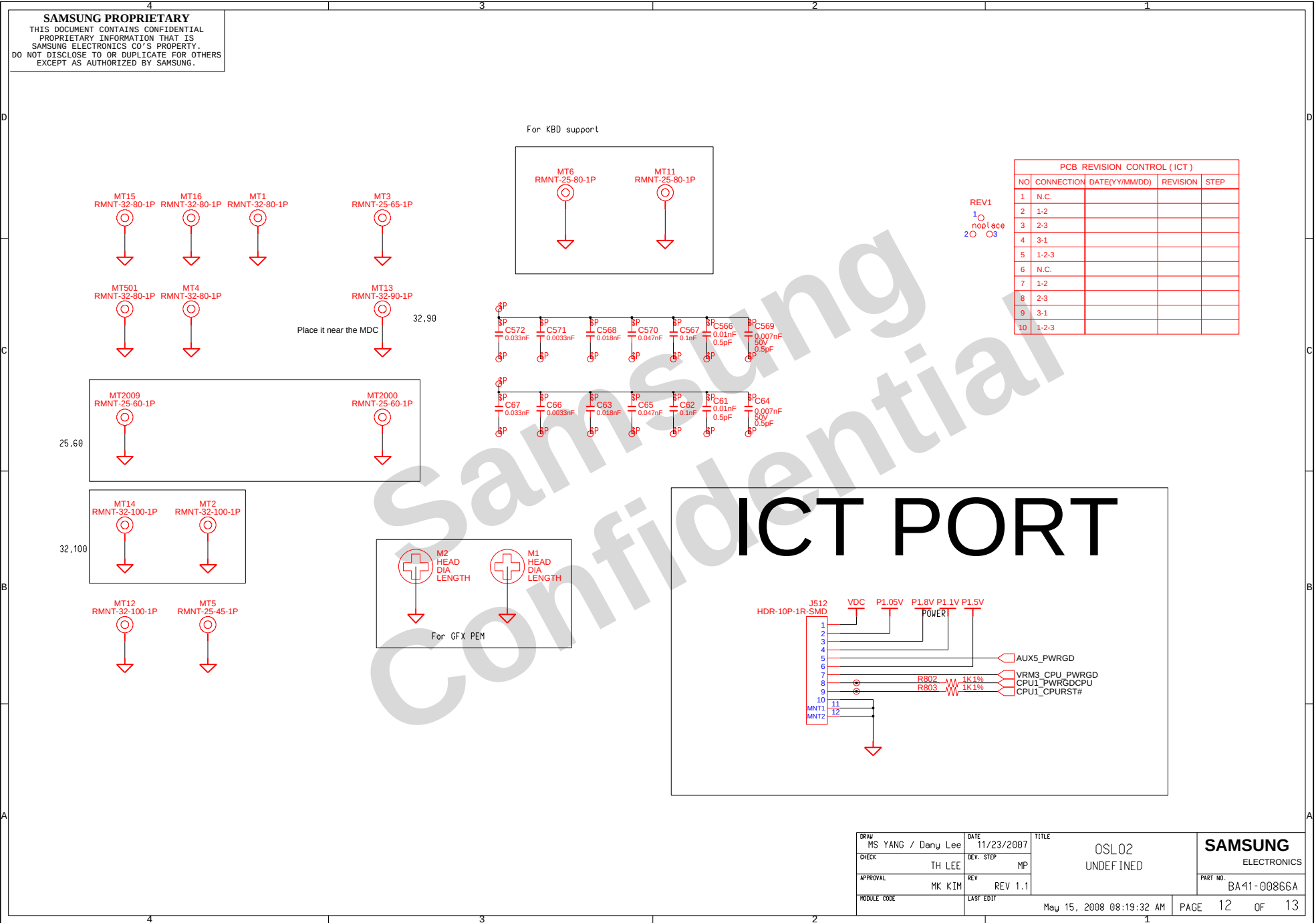
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POWER DISCHARGER



DRAW	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK	TH LEE	DEV. STEP	MP	PWR_MV_DisCharger	DISCHARGING LOGIC	
APPROVAL	MK KIM	REV	REV 1.1			
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1 OF 1	



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- ☐ CRT5_DDCDATA
- ☐ CRT5_HSYNC
- ☐ CRT5_VSYNC

- ☐ KBC5_KS1(1)
- ☐ KBC5_KS1(2)
- ☐ KBC5_KS1(3)
- ☐ KBC5_KS1(4)
- ☐ KBC5_KS1(5)
- ☐ KBC5_KS1(6)
- ☐ KBC5_KS1(7)
- ☐ KBC5_KS0(0)
- ☐ KBC5_KS0(1)
- ☐ KBC5_KS0(10)
- ☐ KBC5_KS0(11)
- ☐ KBC5_KS0(12)
- ☐ KBC5_KS0(13)
- ☐ KBC5_KS0(14)
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- ☐ KBC5_KS0(2)
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- ☐ KBC5_KS0(4)
- ☐ KBC5_KS0(5)
- ☐ KBC5_KS0(6)
- ☐ KBC5_KS0(7)

 P1.8V
 P1.8V
 P1.8V
 P1.8V
 P1.8V
 P1.8V_FBVDDQ
 P1.8V_FBVDDQ

GROUND
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D:/users/mobile16/mentor/oslo2/oslo2_pr
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Sheet66 ----- PWR_MV_Charger_Isl6256a[sheet1]
Sheet67 ----- PWR_MV_3V_5V[sheet1]
Sheet68 ----- PWR_MV_Switched[sheet1]
Sheet69 ----- PWR_CPU_MV_Sc452[sheet1]
Sheet70 ----- PWR_MV_Cantiga[sheet1]
Sheet71 ----- PWR_MV_MeMemory[sheet1]
Sheet72 ----- PWR_Gfx_MV_Ext[sheet1]
Sheet73 ----- PWR_Gfx_MV_Ext[sheet2]
Sheet74 ----- PWR_MV_DisCharger[sheet1]
Sheet75 ----- Root[sheet12]
Sheet76 ----- Root[sheet13]