

PALAU

CPU : Intel Merom-4M (800/667 MHz)
Chip Set : Intel Crestline & ICH8-M
Remarks : Mobility Platform

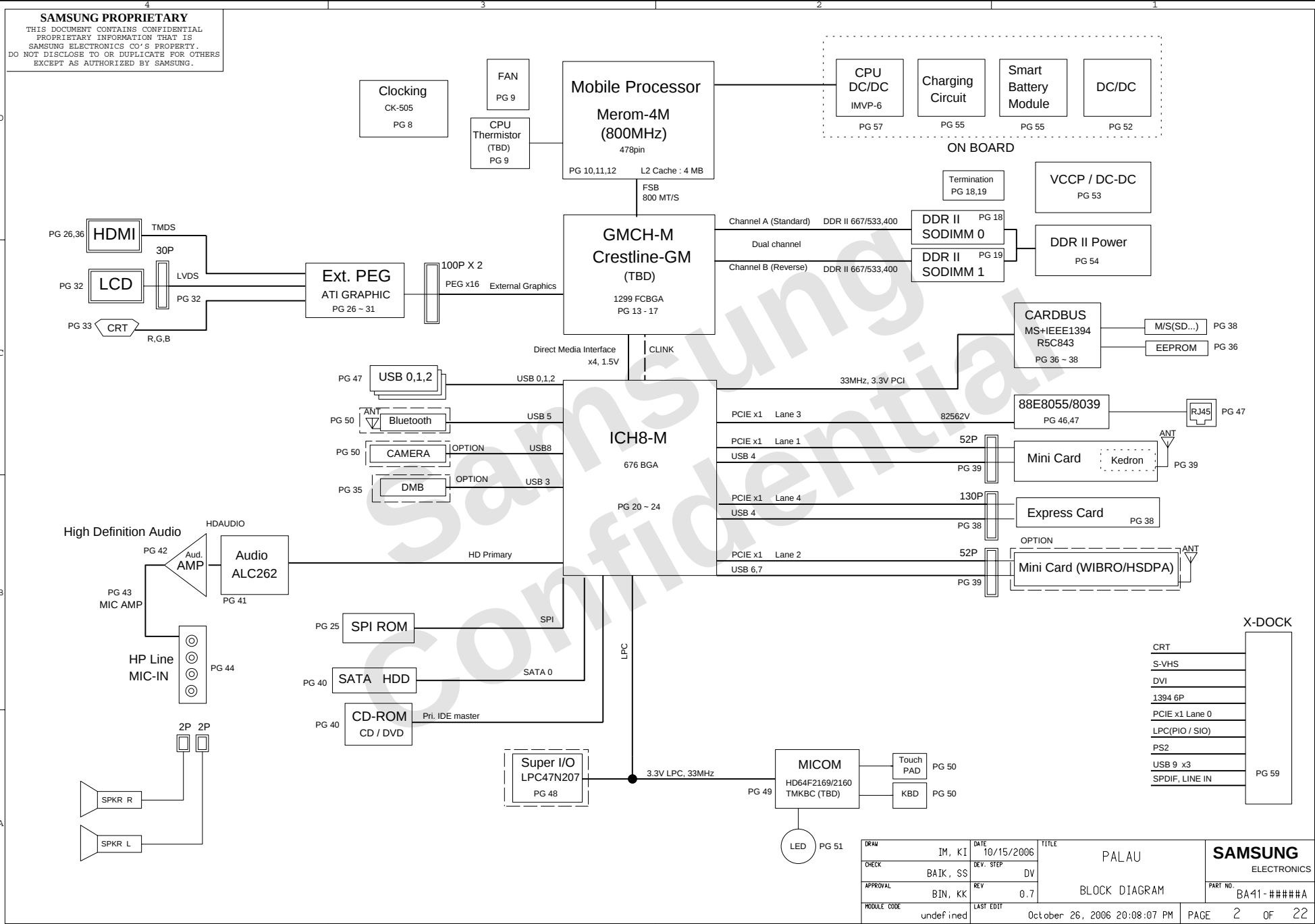
Model Name : SANTA ROSA STD
PBA Name : MAIN
PCB Code : BA41-00753A NANYA
PCB Code : BA41-00786A GCE
Dev. Step : PV - 2
Revision : 1.0
T.R. Date : 2007. 03.30

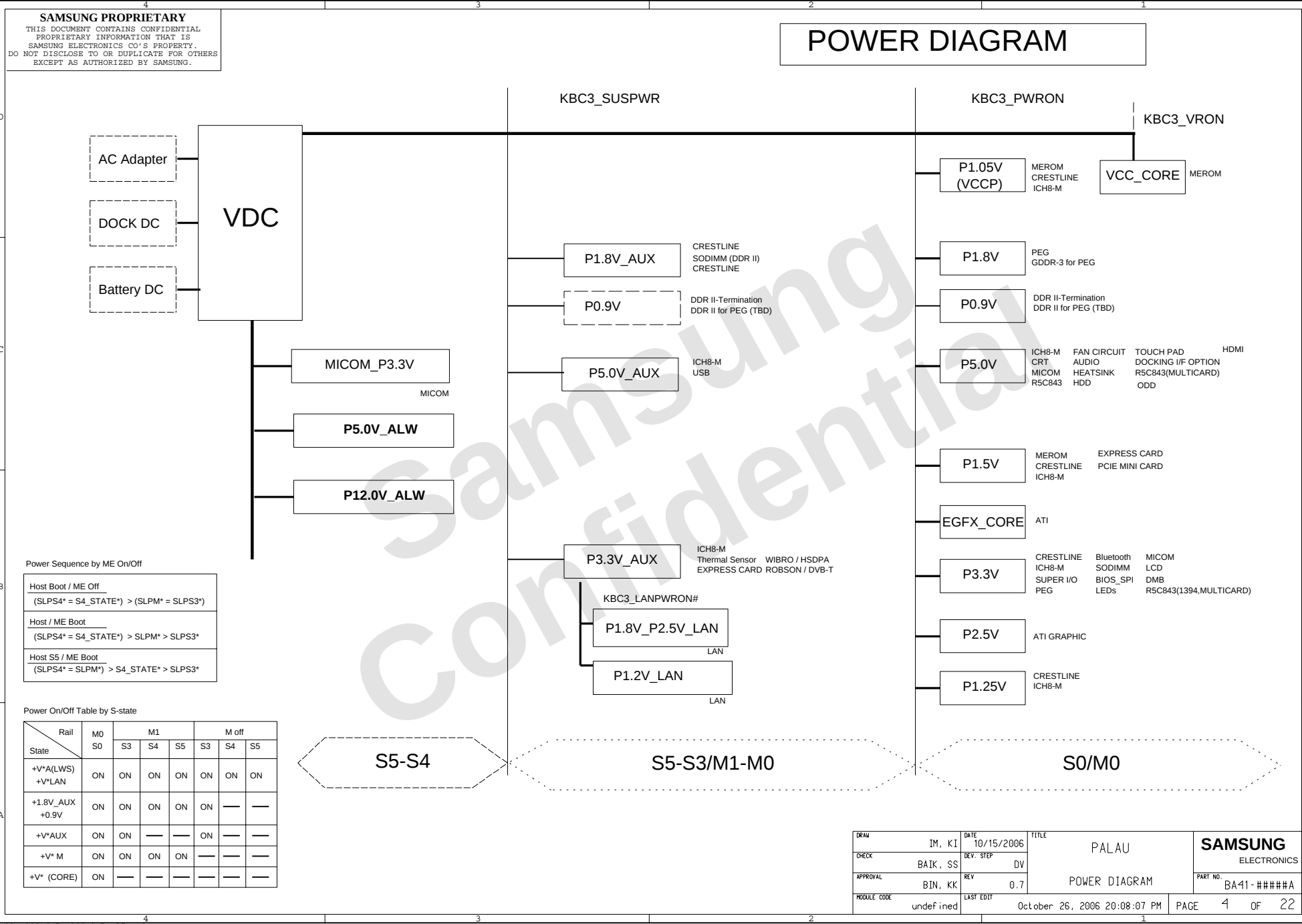
DRAW	CHECK	APPROVAL

Owner : SEC Mobile R & D Signature : X

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DRAW	IM, KI	DATE	10/15/2006	TITLE	PALAU	SAMSUNG ELECTRONICS
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MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	1 OF 22	

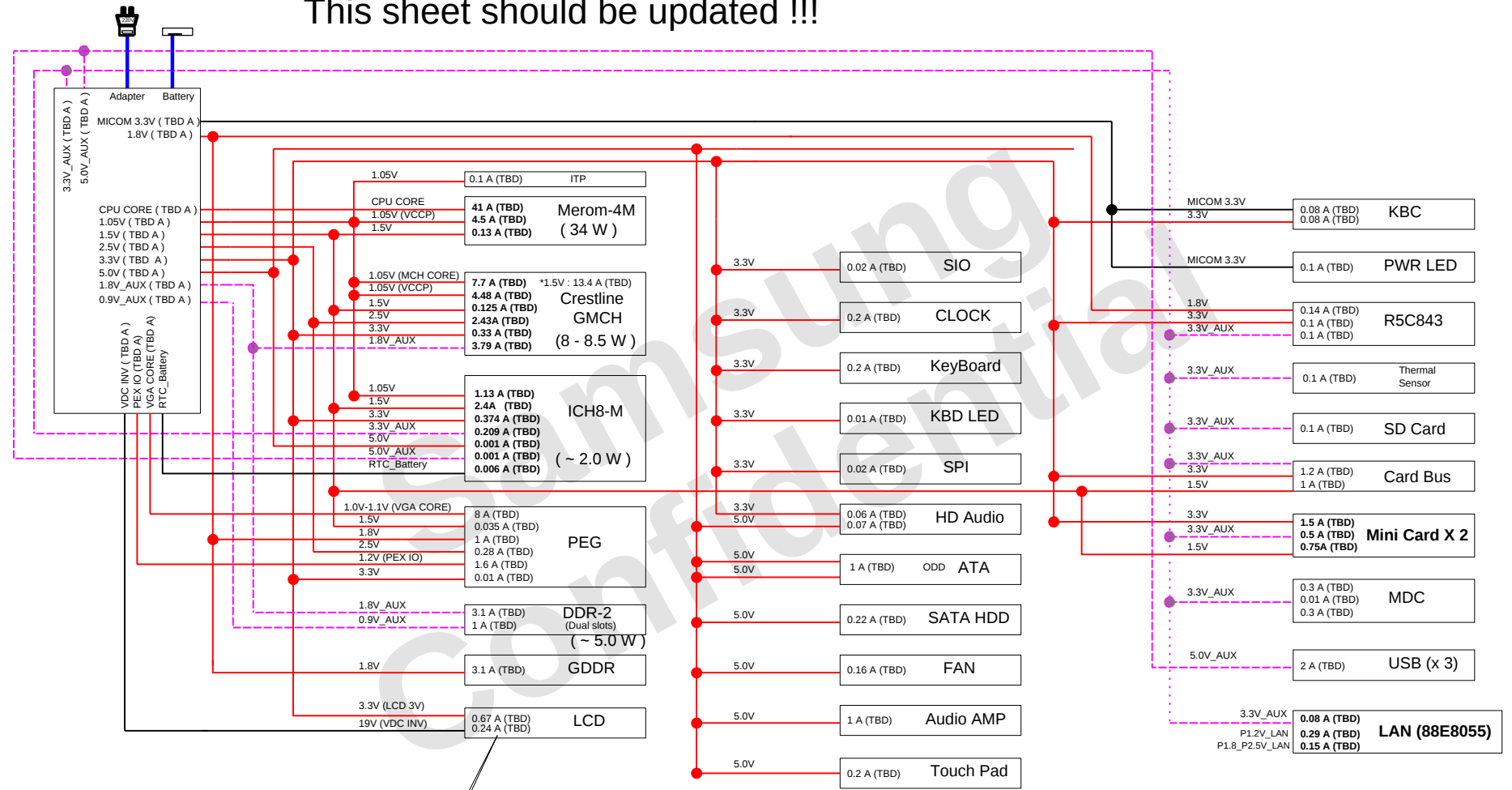




POWER RAILS ANALYSIS

Rev. 0.7

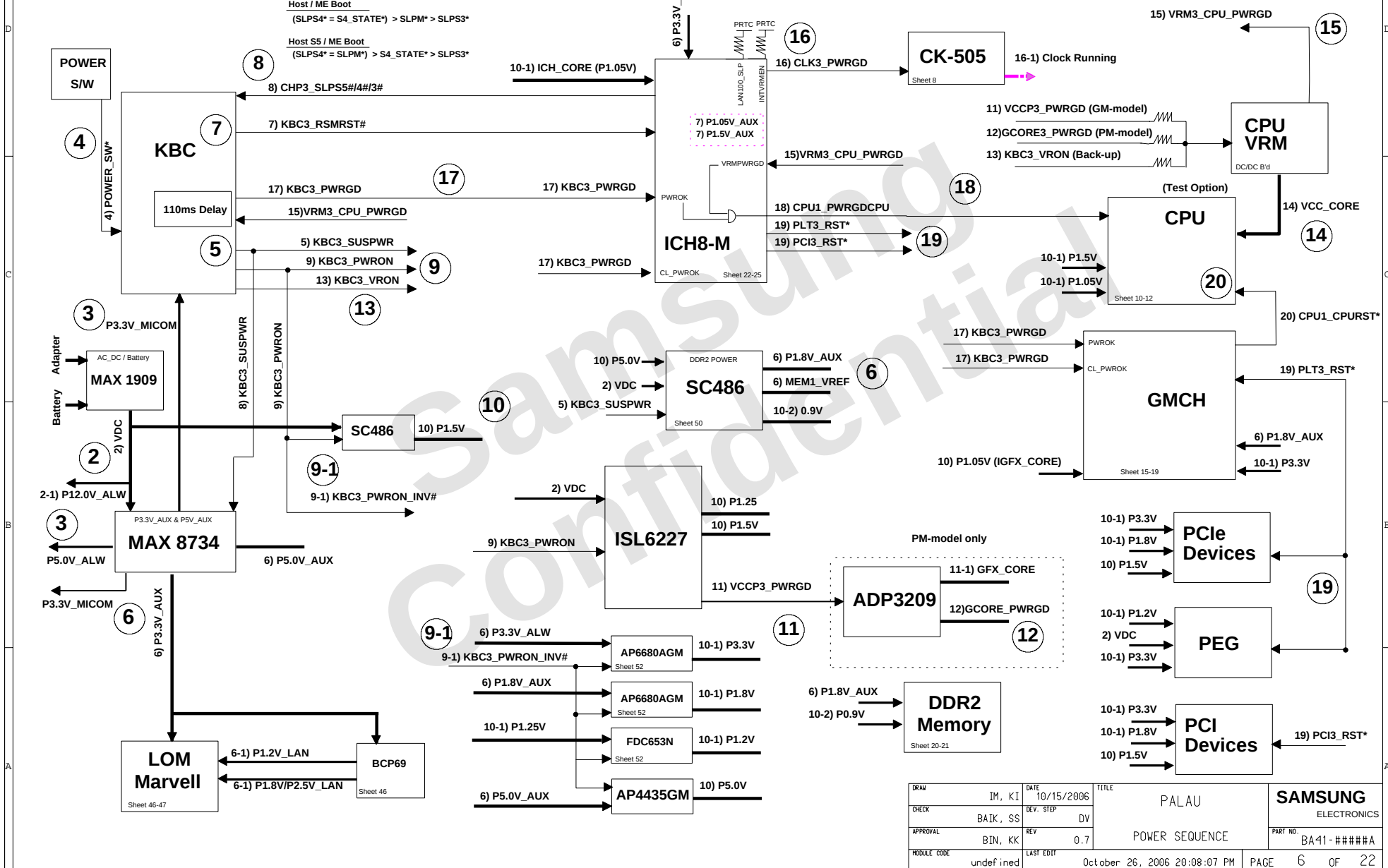
This sheet should be updated !!!

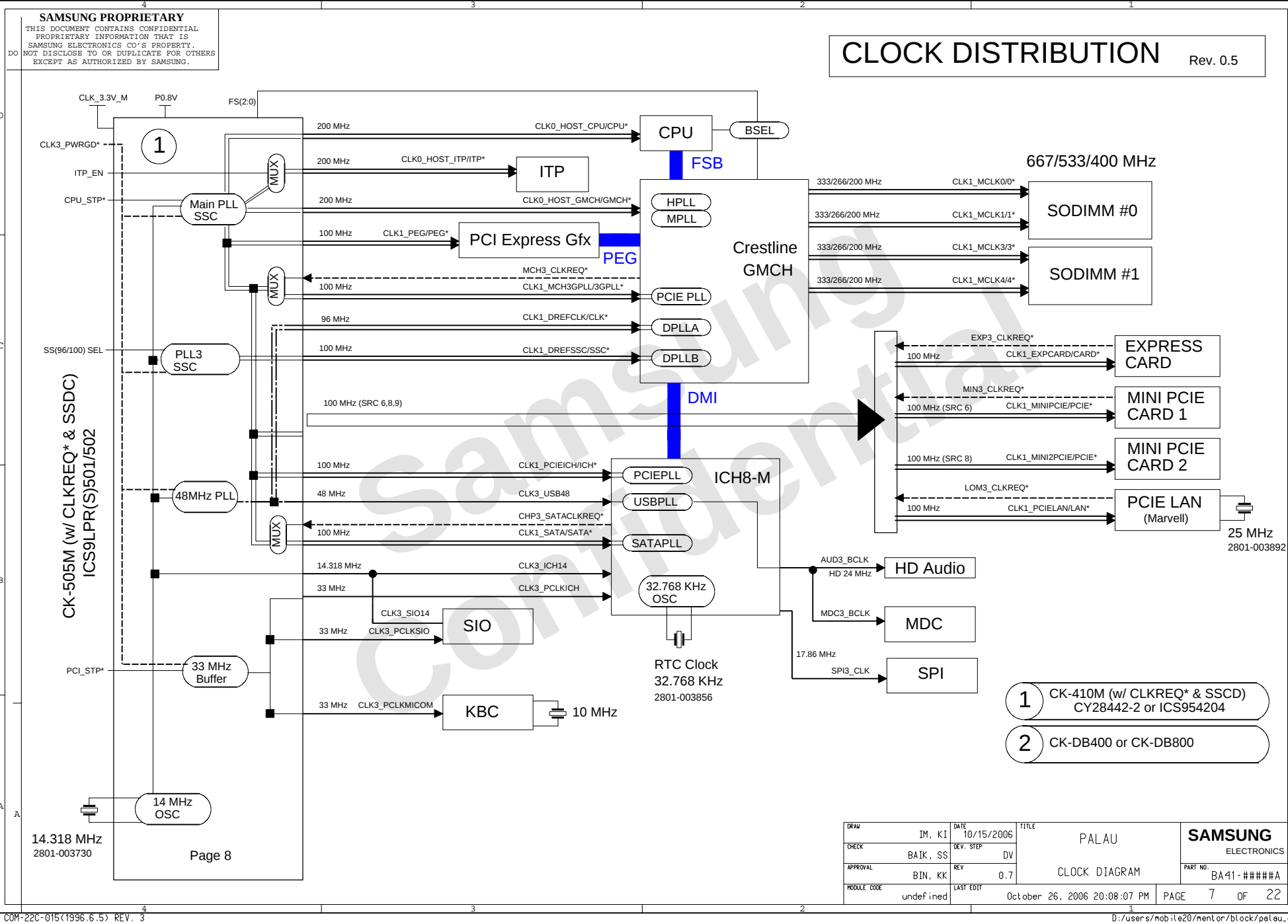


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				PAGE	5	OF 22

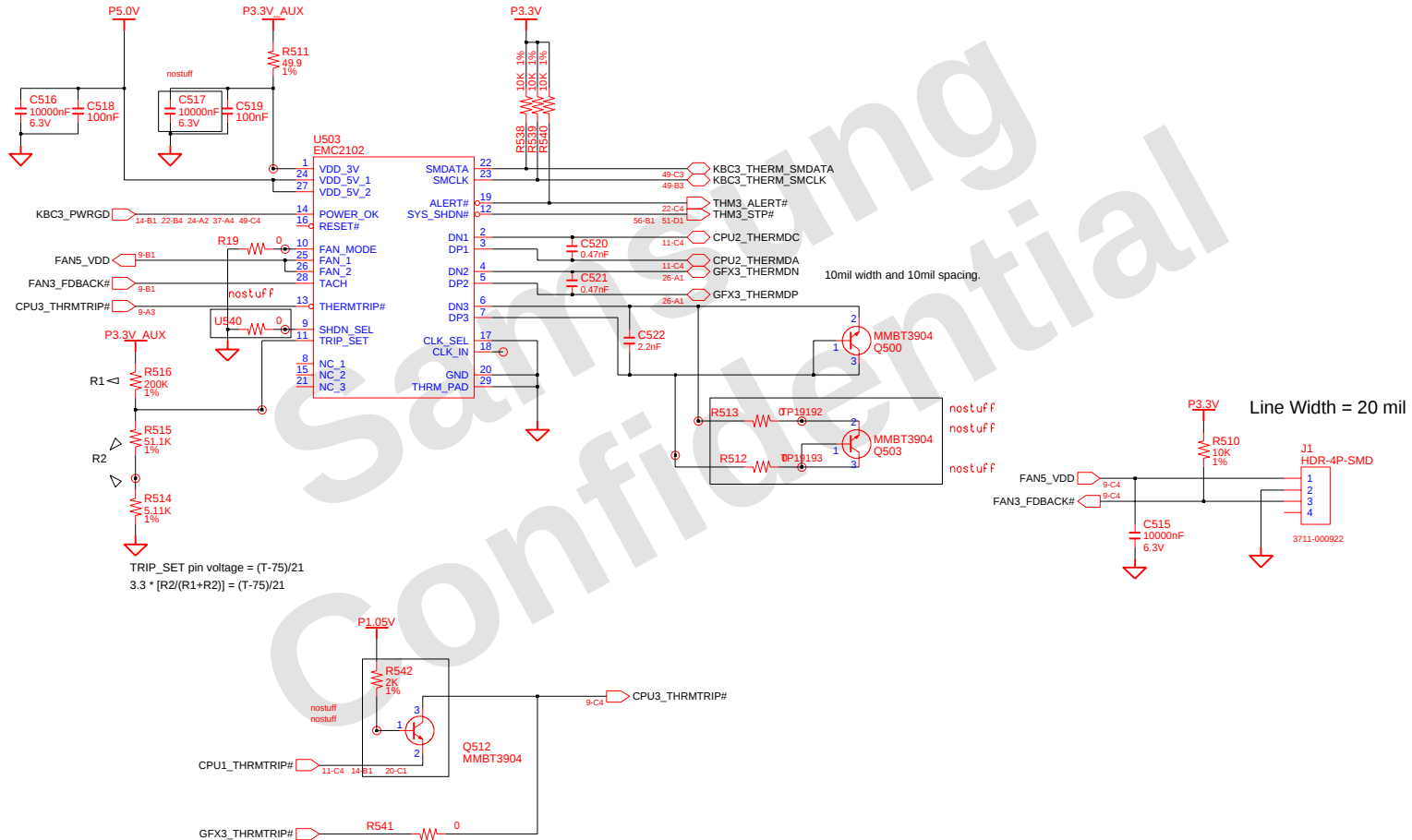
Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

POWER SEQUENCE Rev. 0.7

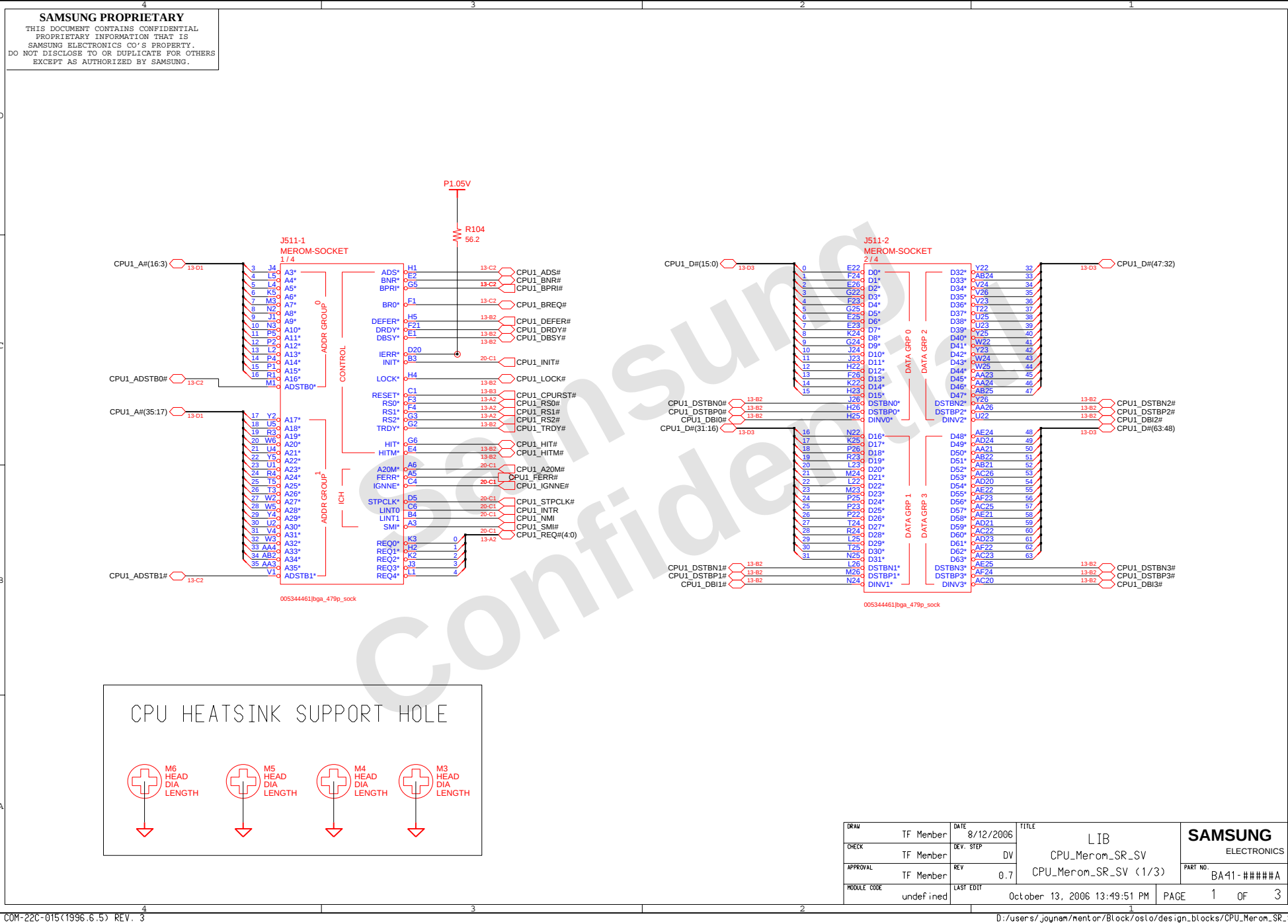


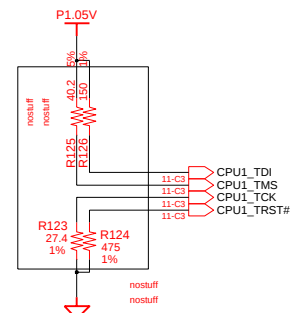


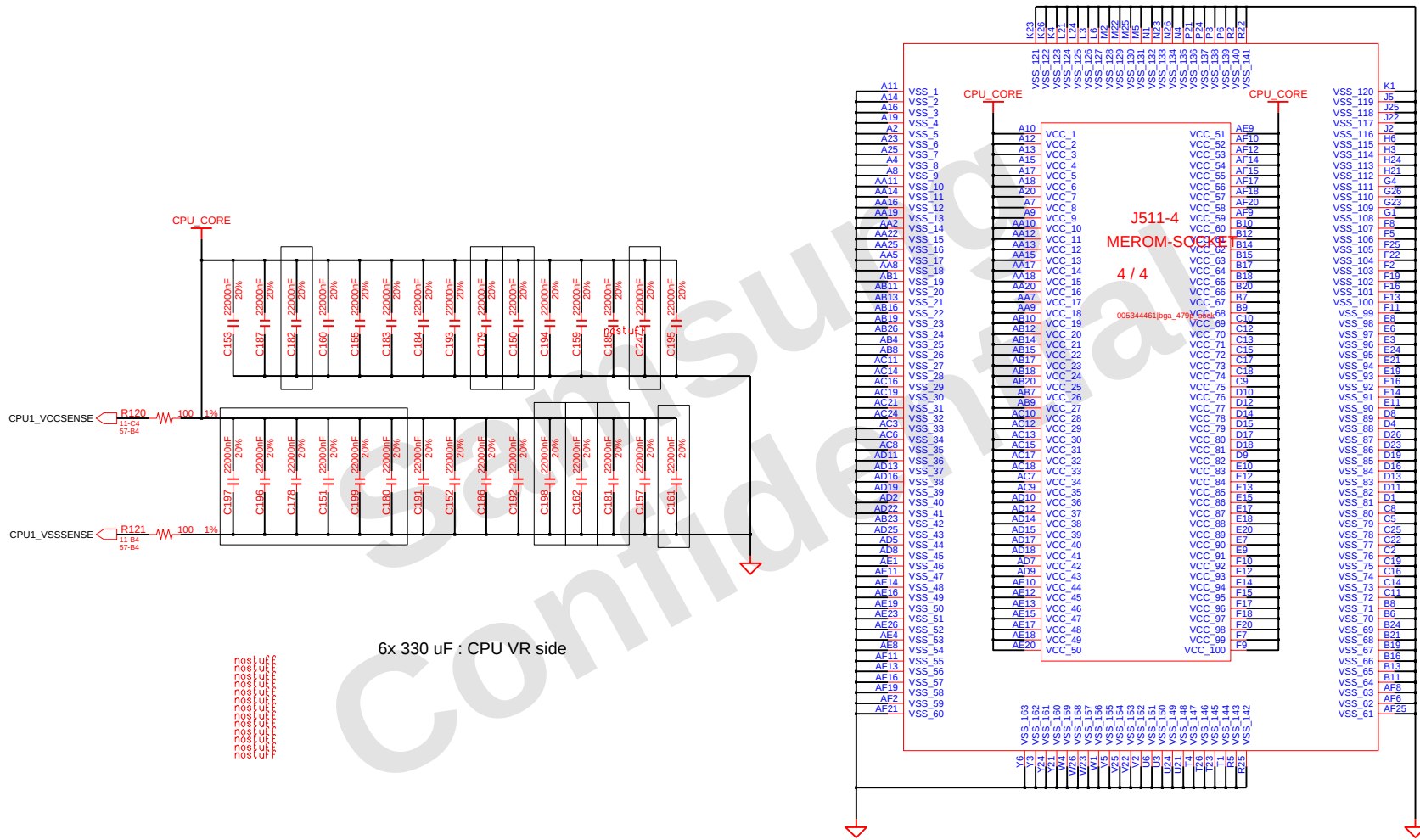
THERMAL SENSOR & FAN CONTROL



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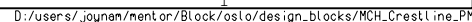




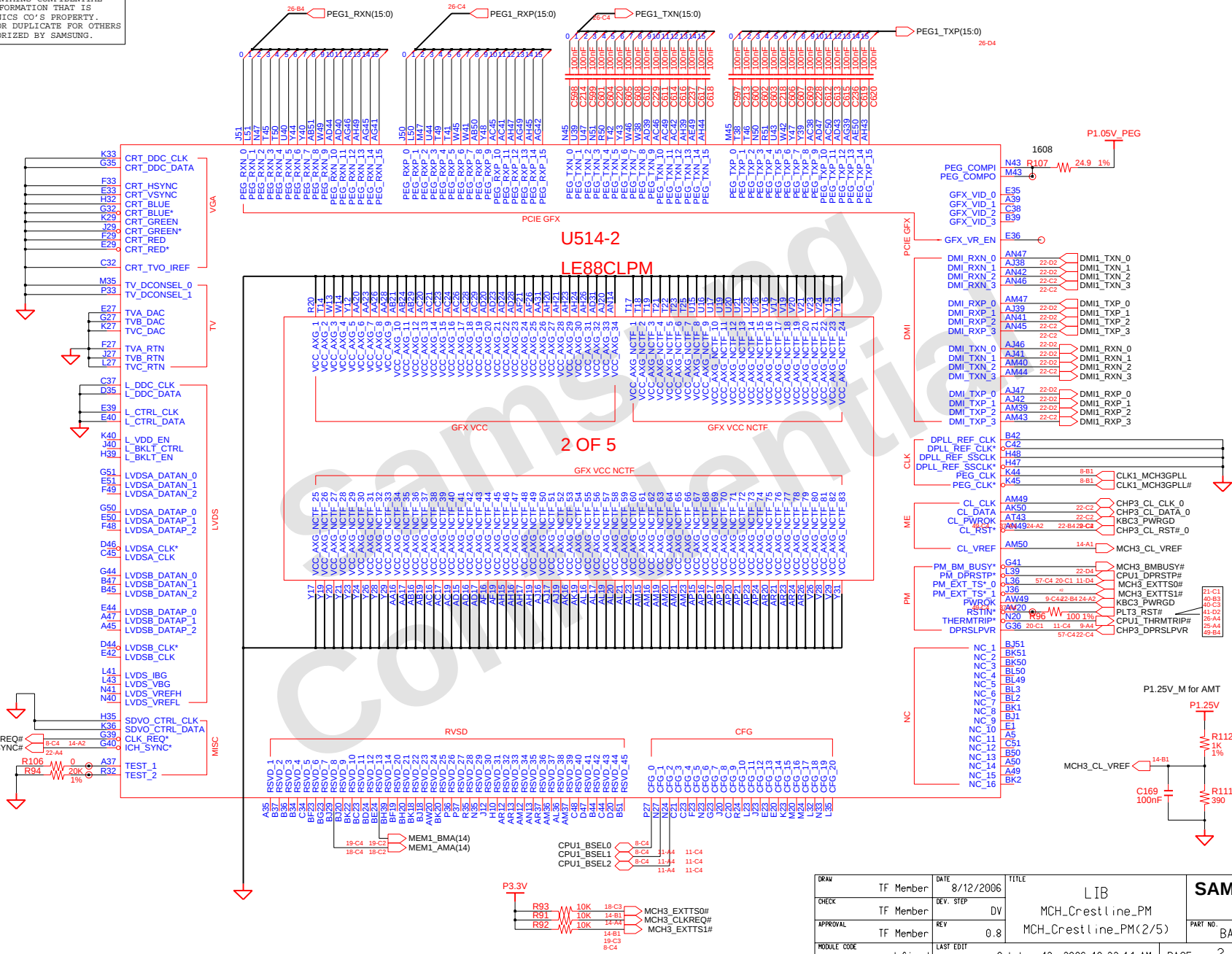


6x 330 uF : CPU VR side

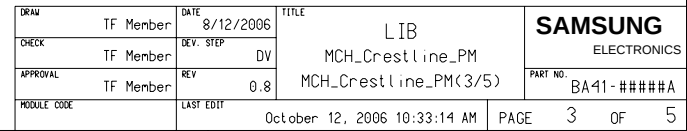
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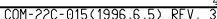


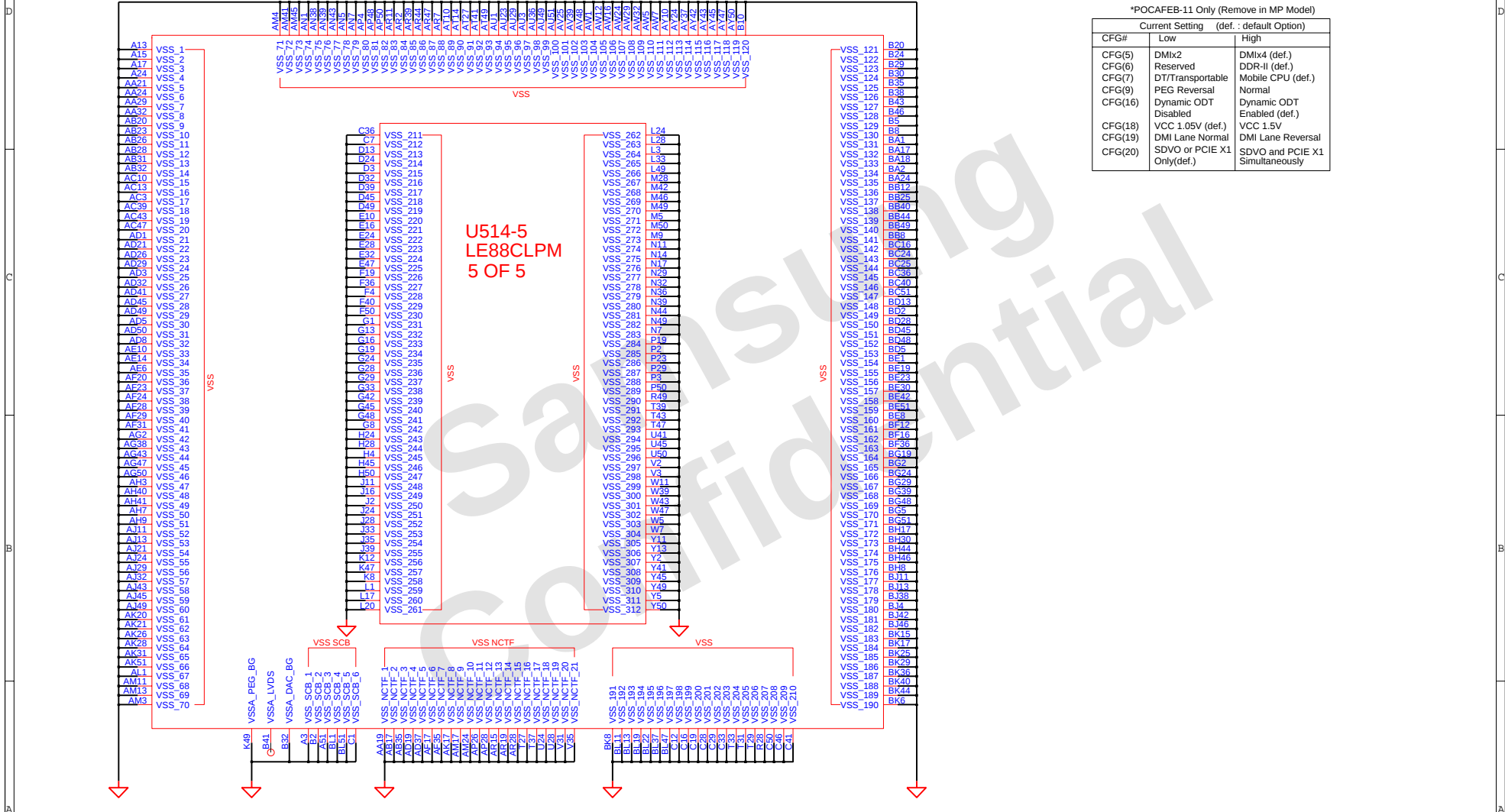
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APPROVAL	TF Member	REV	0.8			
PART NO.			BA41-#####			
MODULE CODE		LAST EDIT		October 12, 2006 10:33:14 AM	PAGE	1 OF 5



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D:/users/jounan/mentor/Block/oslo/design blocks/MCH Crestline PM

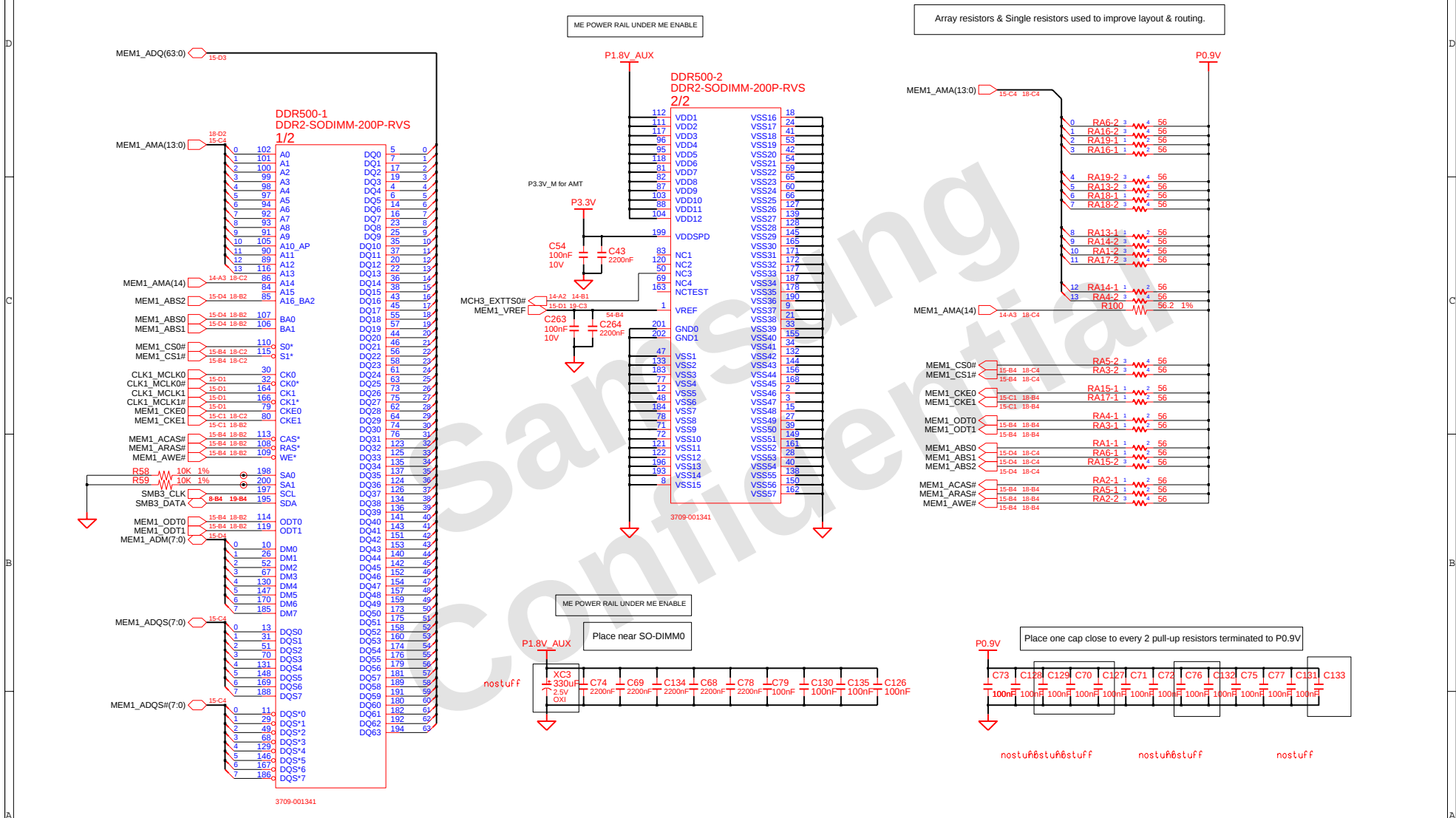


*POCAFE-11 Only (Remove in MP Model)

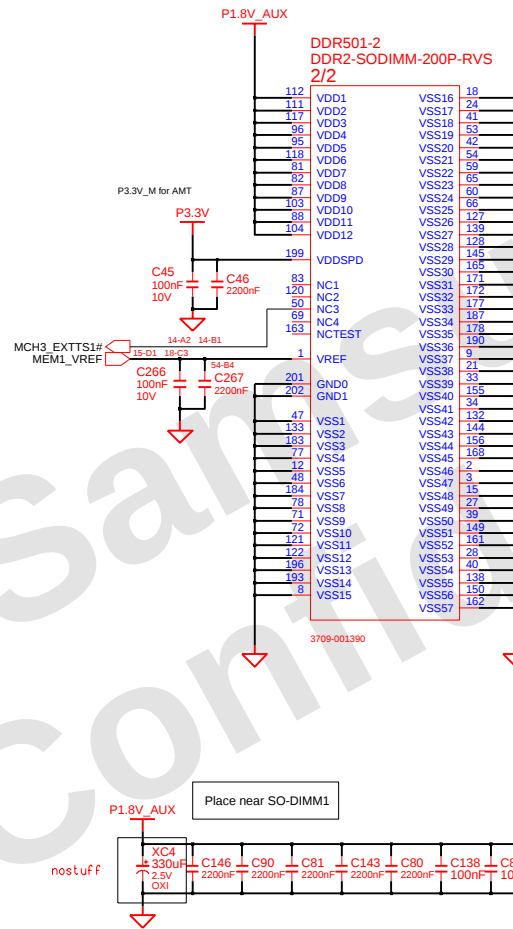
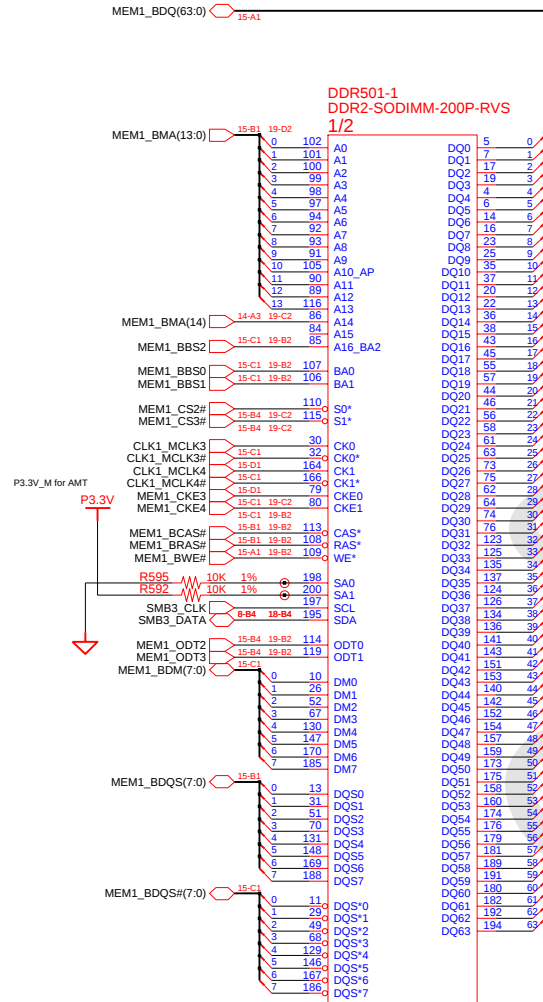
Current Setting (def.: default Option)		
CFG#	Low	High
CFG(5)	DMIX2	DMIX4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT	Dynamic ODT
	Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

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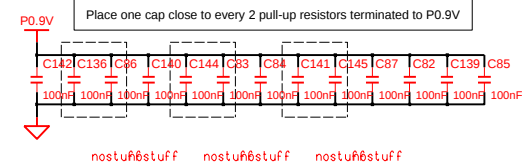
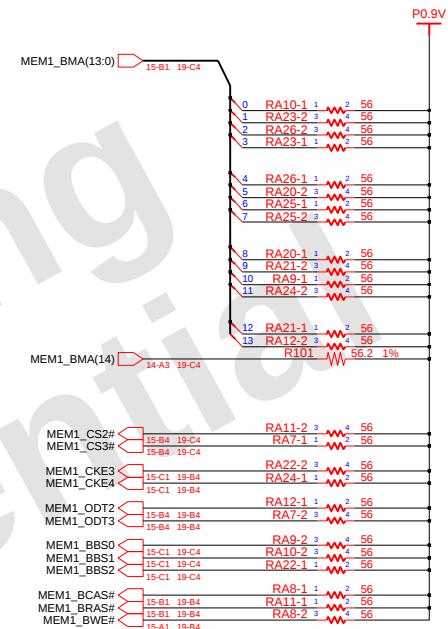
DDR SO-DIMM #0



DDR SO-DIMM #1

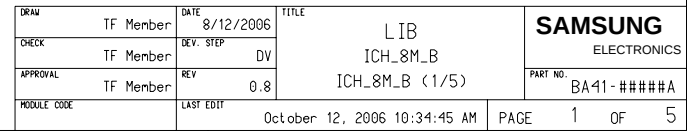


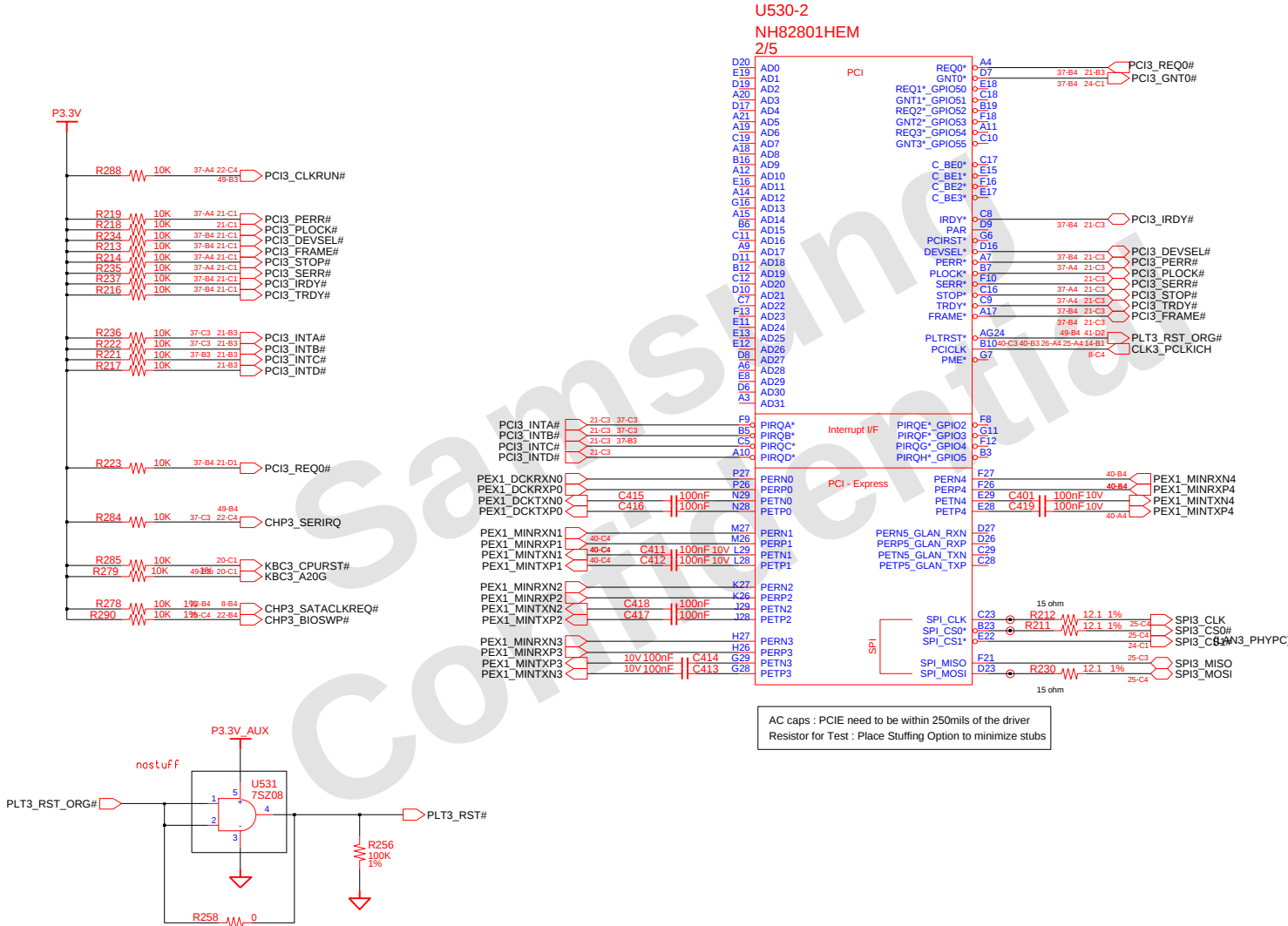
Array resistors & Single resistors used to improve layout & routing.



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MODULE CODE		LAST EDIT	October 10, 2006 20:55:25 PM	PAGE	2 OF 2	

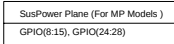
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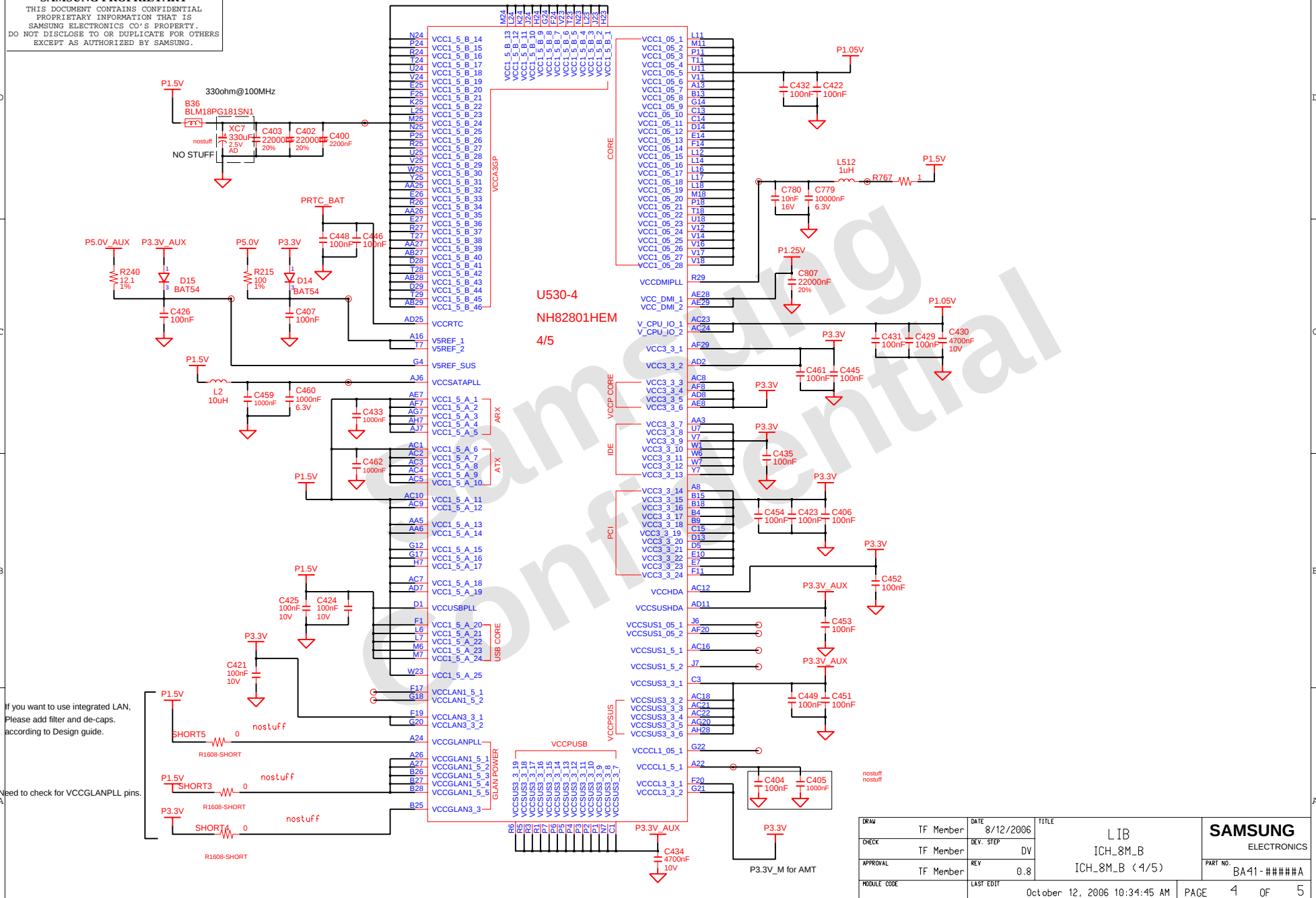
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MODULE CODE	undef ined	LAST EDIT	October 12, 2006 10:34:45 AM	PAGE	2 OF 5	

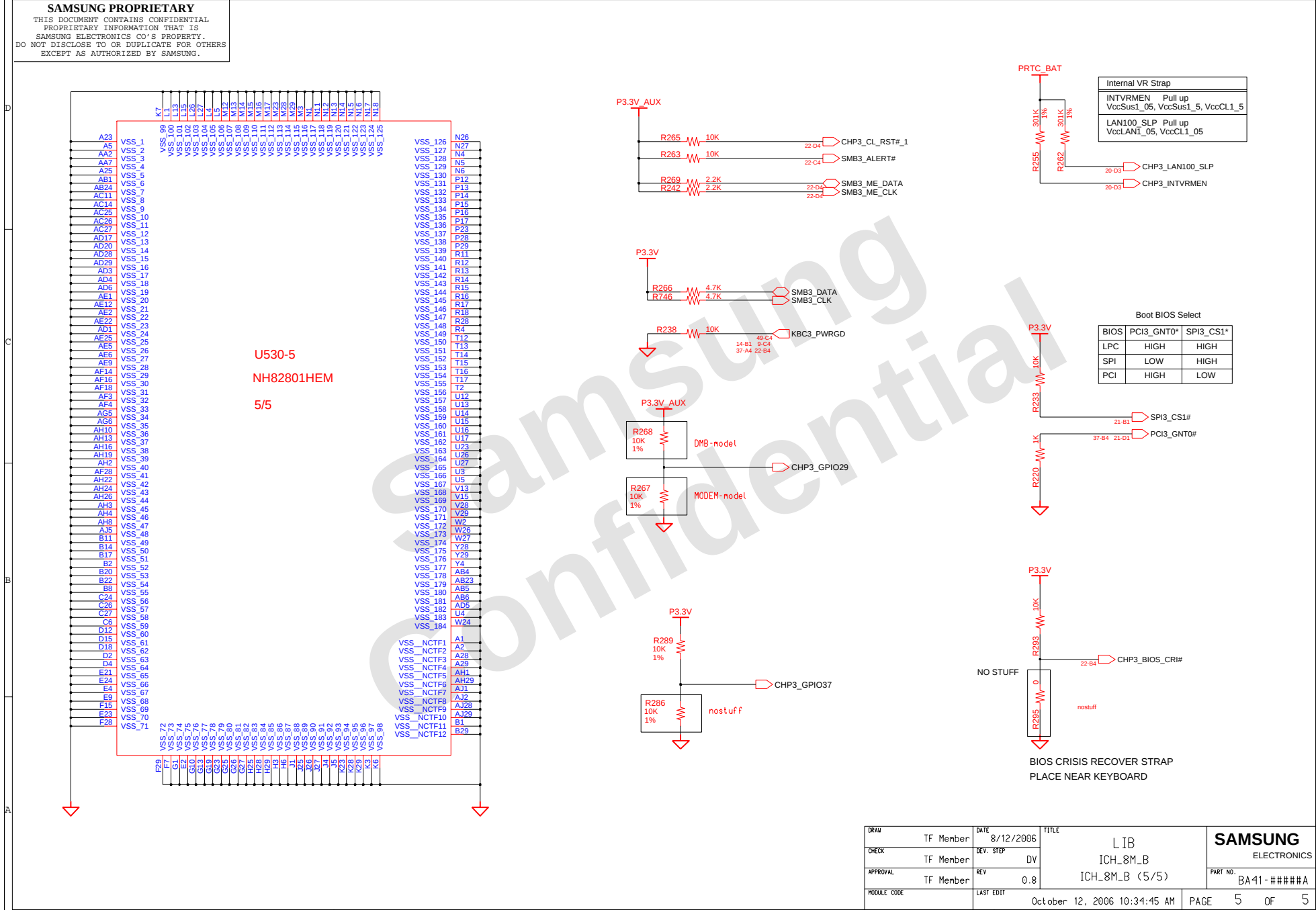
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DRAW	TF Member	DATE	8/12/2006	LIB ICH_8M_B ICH_8M_B (3/5)	SAMSUNG ELECTRONICS PART NO. BA14-#####
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APPROVAL	TF Member	REV	0.8		
MODULE CODE	LAST EDIT		October 12, 2006 10:34:45 AM		

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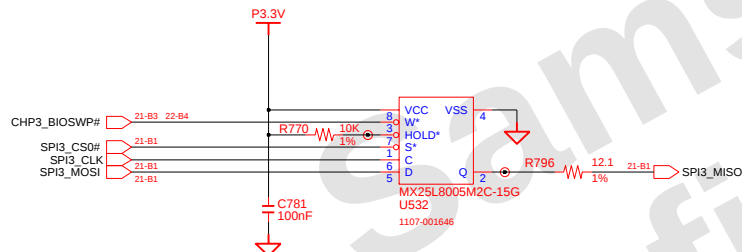
COM-22C-015(1996.6.5) REV. 3	3	2	1
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- SPI ROM LIST -

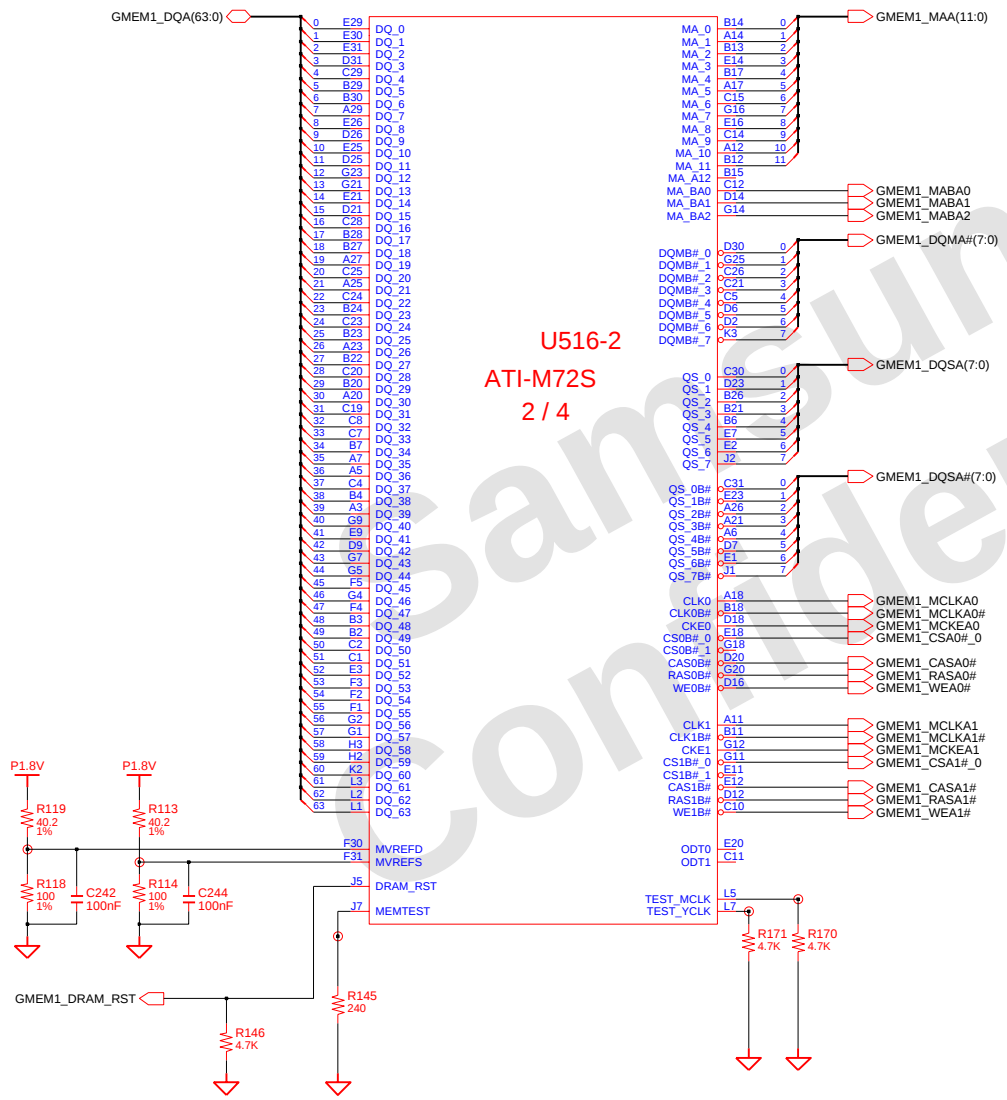
- Macronix - MX25L8005M2C-15G
- STM - M25PE80
- ATMEL - AT26DF081A-SU
- SST - 25VF080B-50-4C-S2AF
- WINBOND - W25X80-VSSI-G



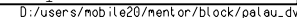
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPOMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY "PRESS SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

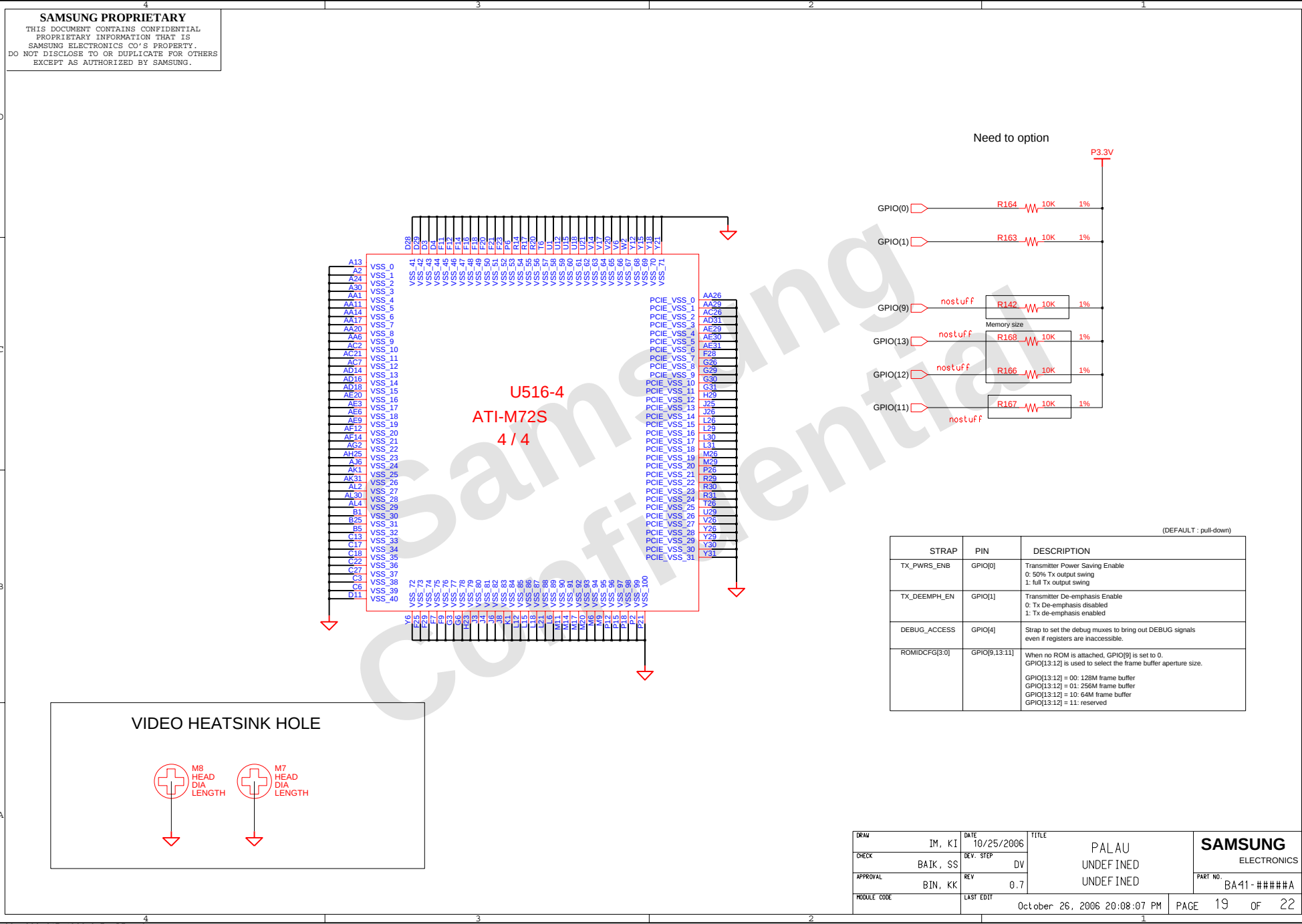
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MODULE CODE		LAST EDIT	October 10, 2006 20:56:20 PM	PAGE	1	BA41-####A
				OF	1	

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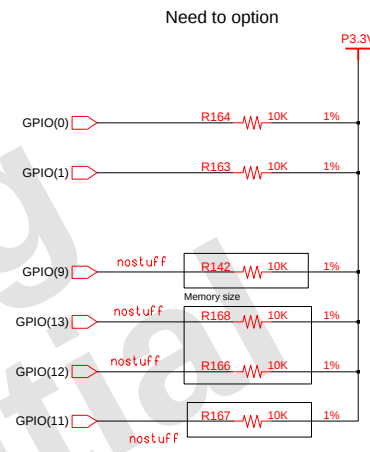
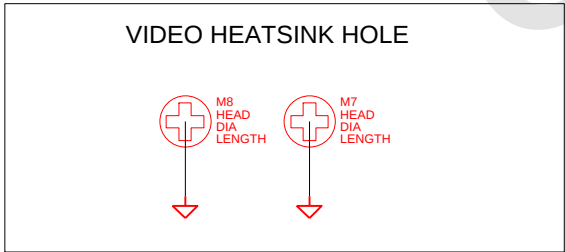


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APPROVAL	BIN, KK	LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	17	OF 22
MODULE CODE						



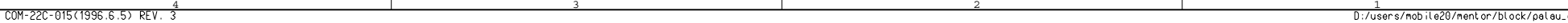


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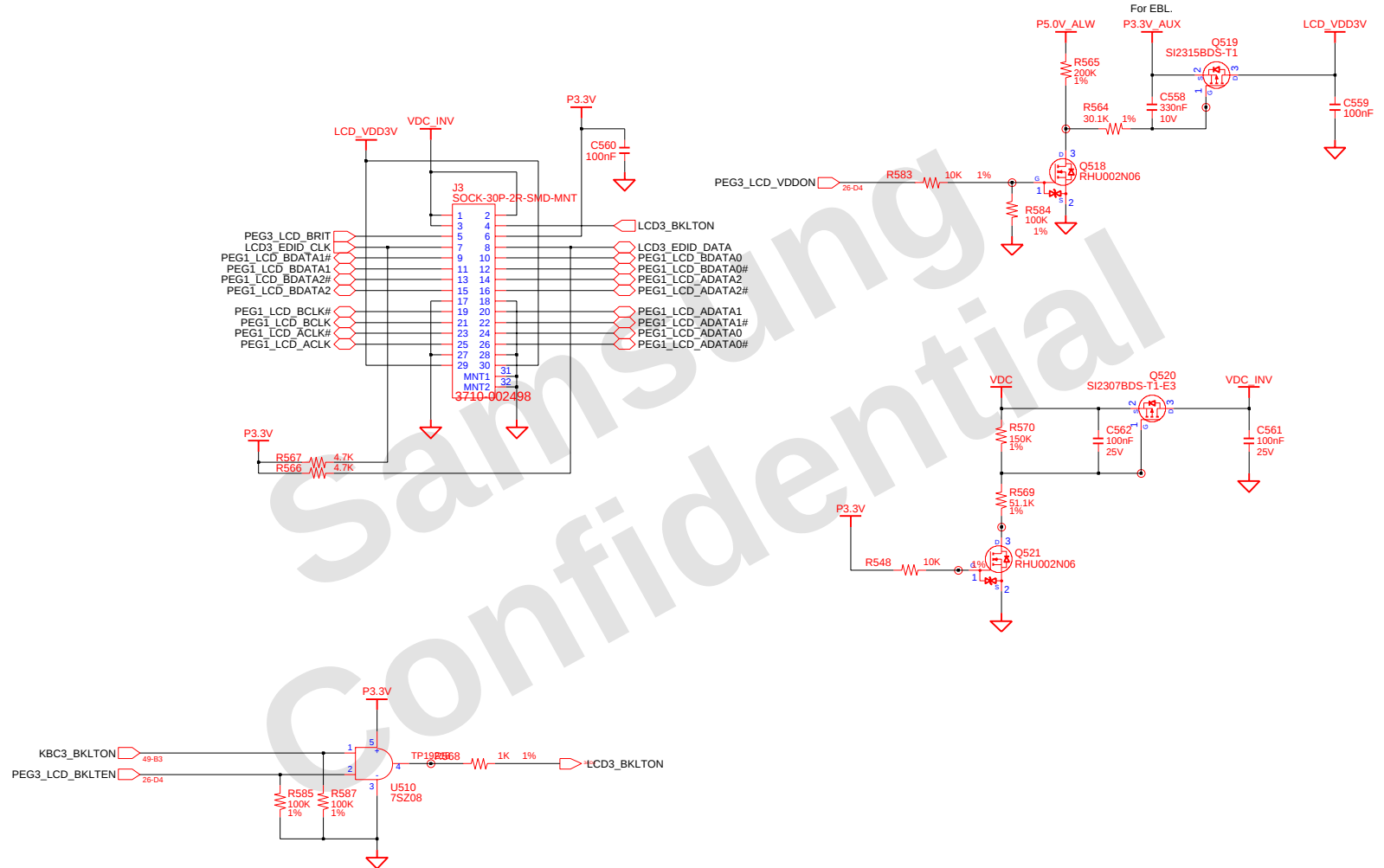
(DEFAULT : pull-down)		
STRAP	PIN	DESCRIPTION
TX_PWR5_ENB	GPIO[0]	Transmitter Power Saving Enable 0: 50% Tx output swing 1: full Tx output swing
TX_DEEMPH_EN	GPIO[1]	Transmitter De-emphasis Enable 0: Tx De-emphasis disabled 1: Tx de-emphasis enabled
DEBUG_ACCESS	GPIO[4]	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.
ROMIDCFG[3:0]	GPIO[9,13:11]	When no ROM is attached, GPIO[9] is set to 0. GPIO[13:12] is used to select the frame buffer aperture size. GPIO[13:12] = 00: 128M frame buffer GPIO[13:12] = 01: 256M frame buffer GPIO[13:12] = 10: 64M frame buffer GPIO[13:12] = 11: reserved

DRAW	IM, KI	DATE	10/25/2006	TITLE	PALAU UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS	
CHECK	BAIK, SS	DEV. STEP	DV				PART NO. BA41-#####
APPROVAL	BIN, KK	REV	0.7				
MODULE CODE	LAST EDIT		October 26, 2006 20:08:07 PM		PAGE	19 OF 22	

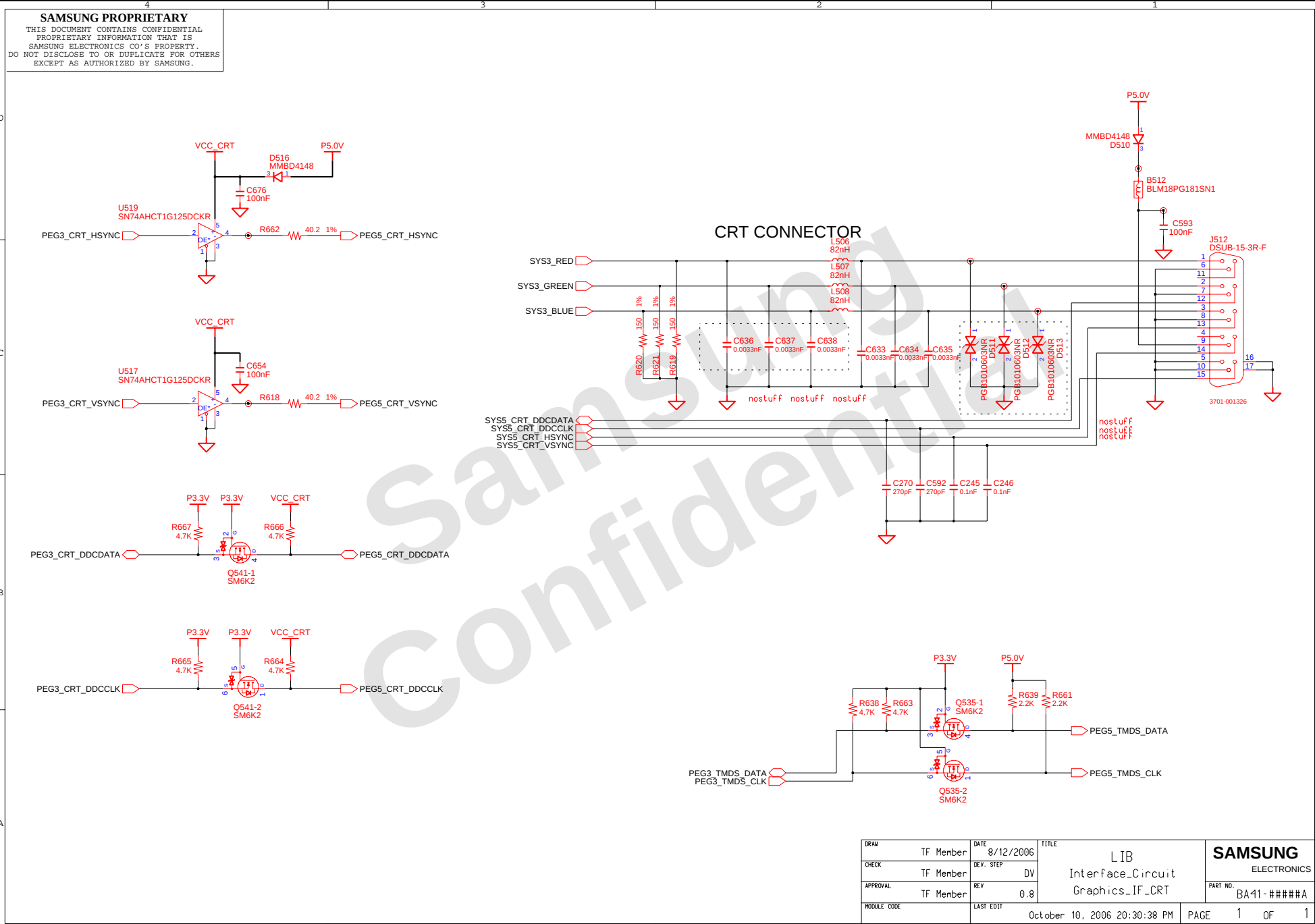


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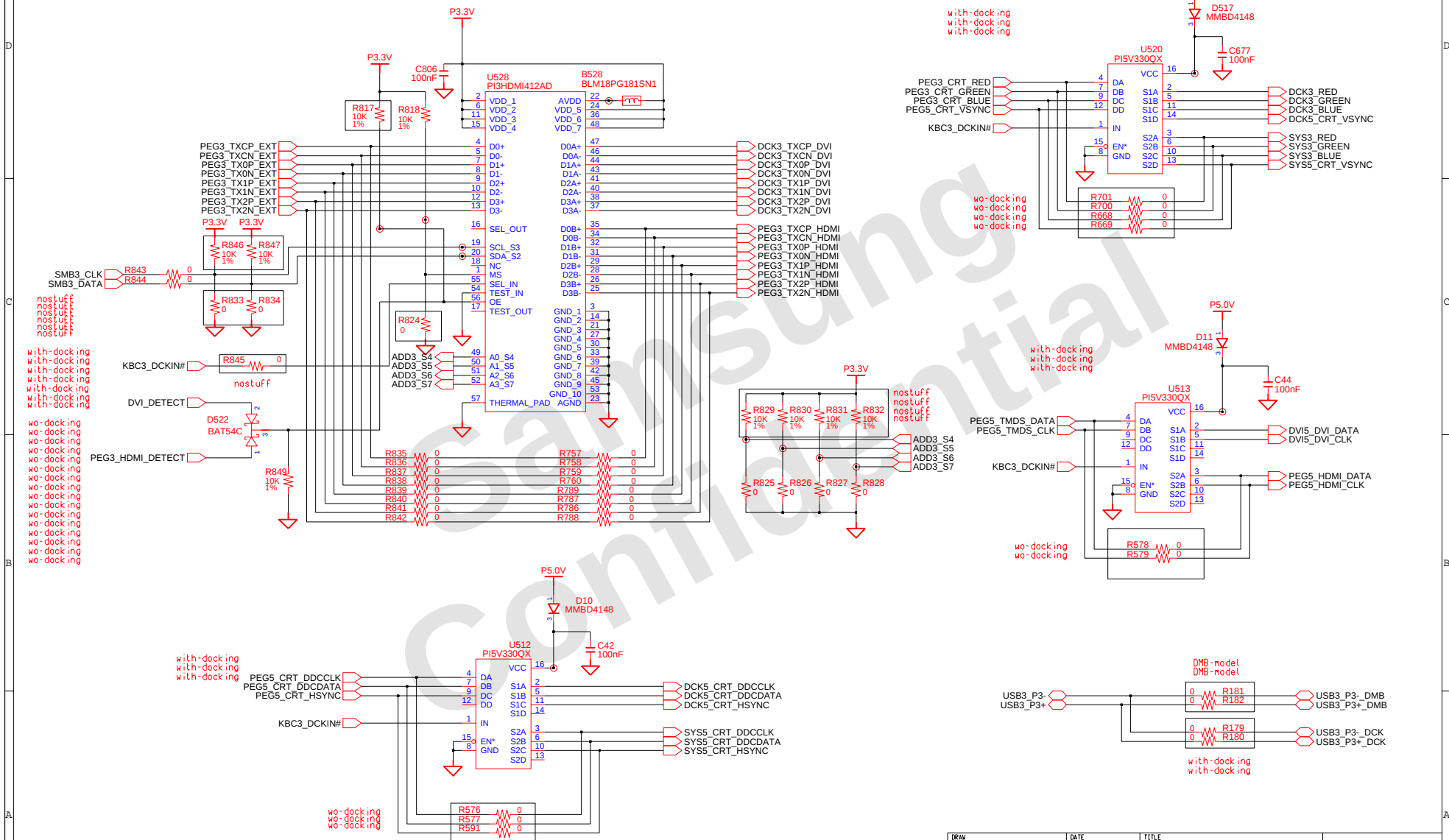


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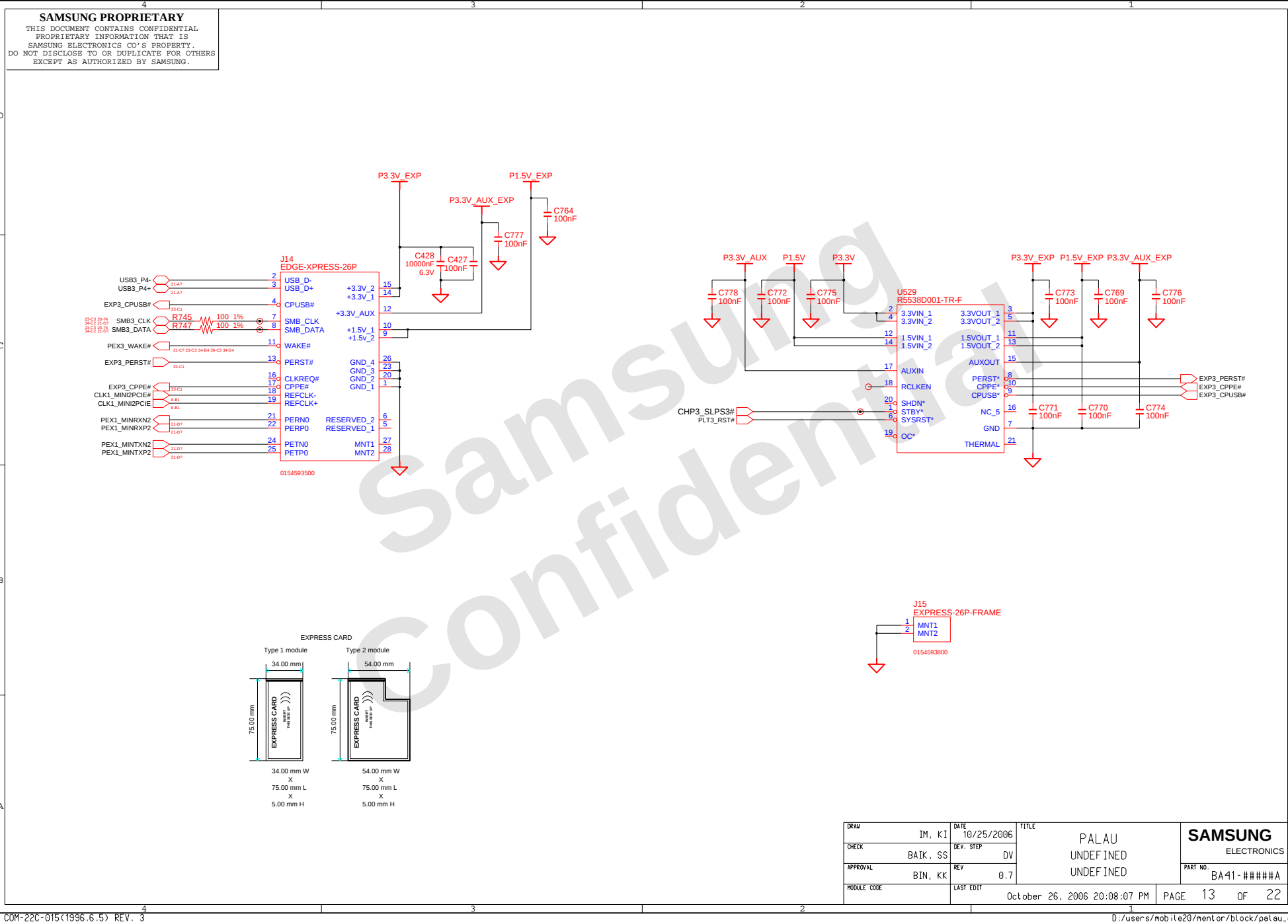


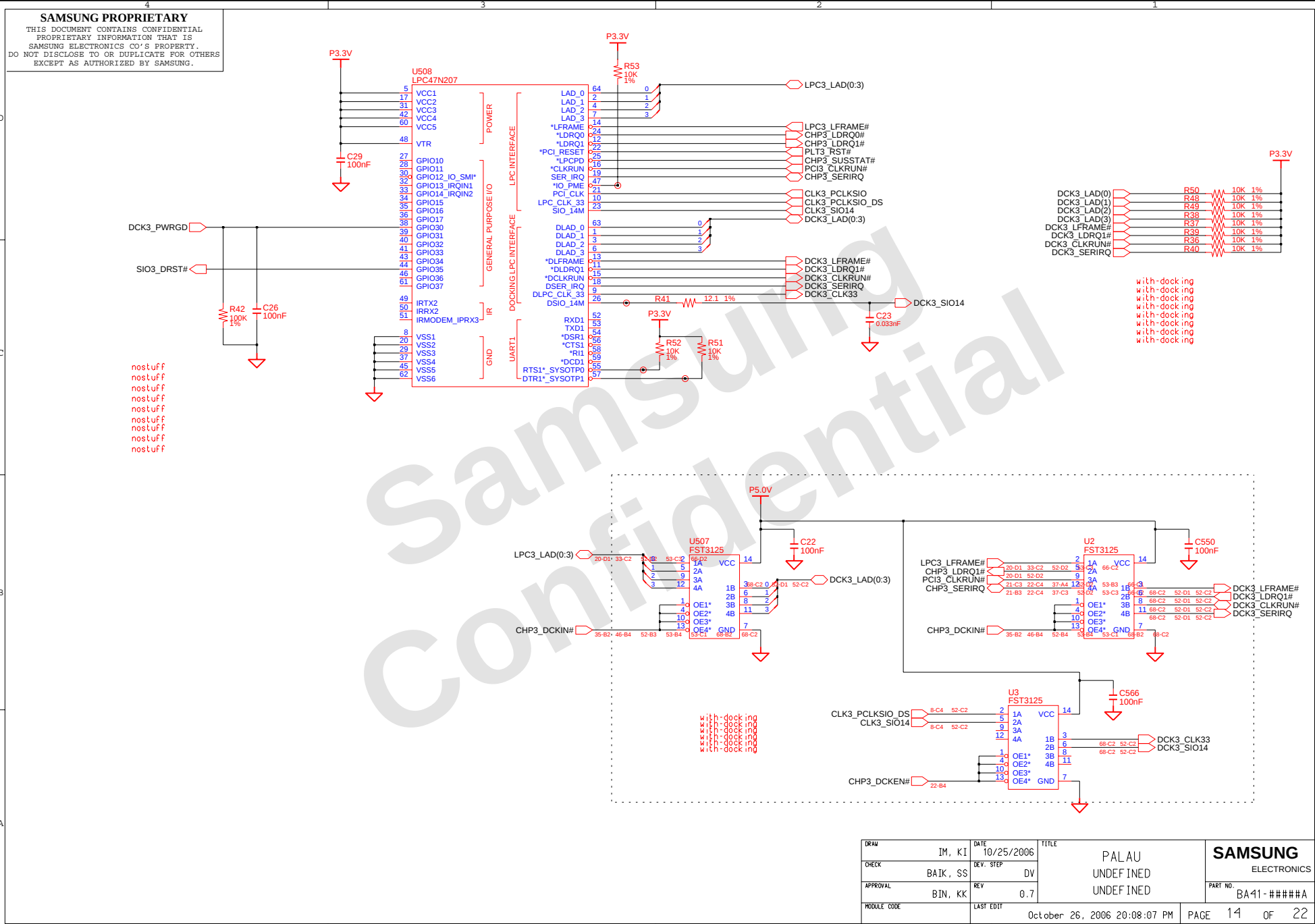
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DOCKING OPTION

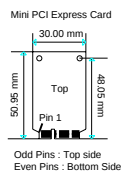
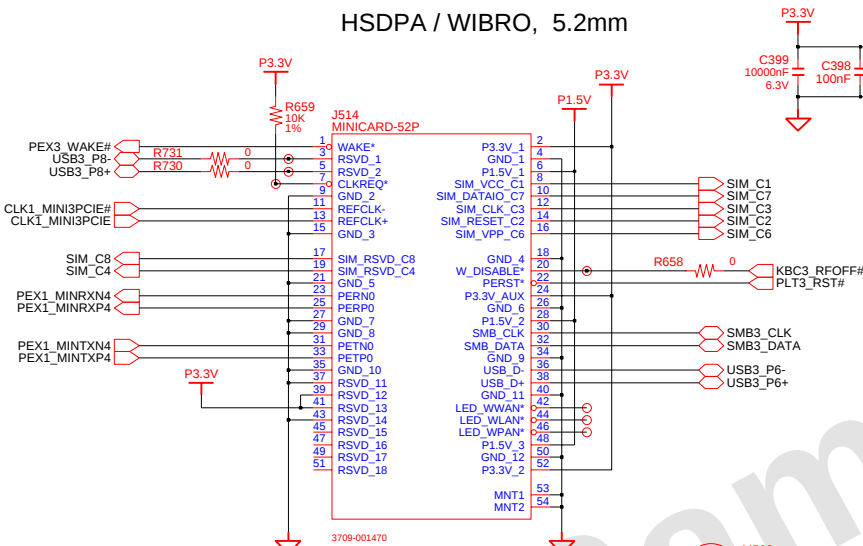


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MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	11	OF 22

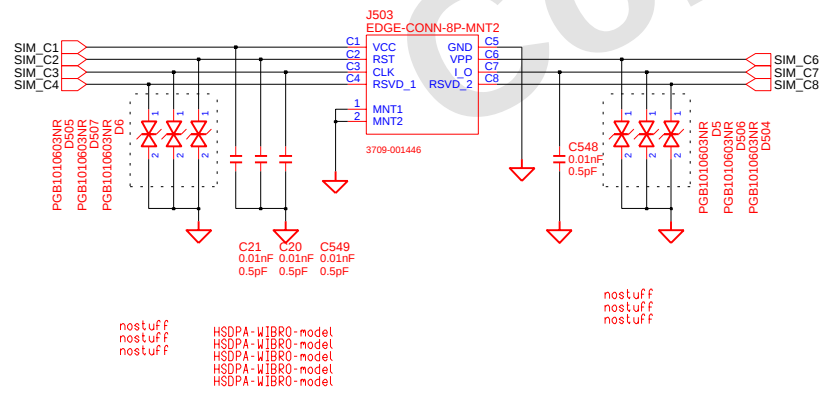




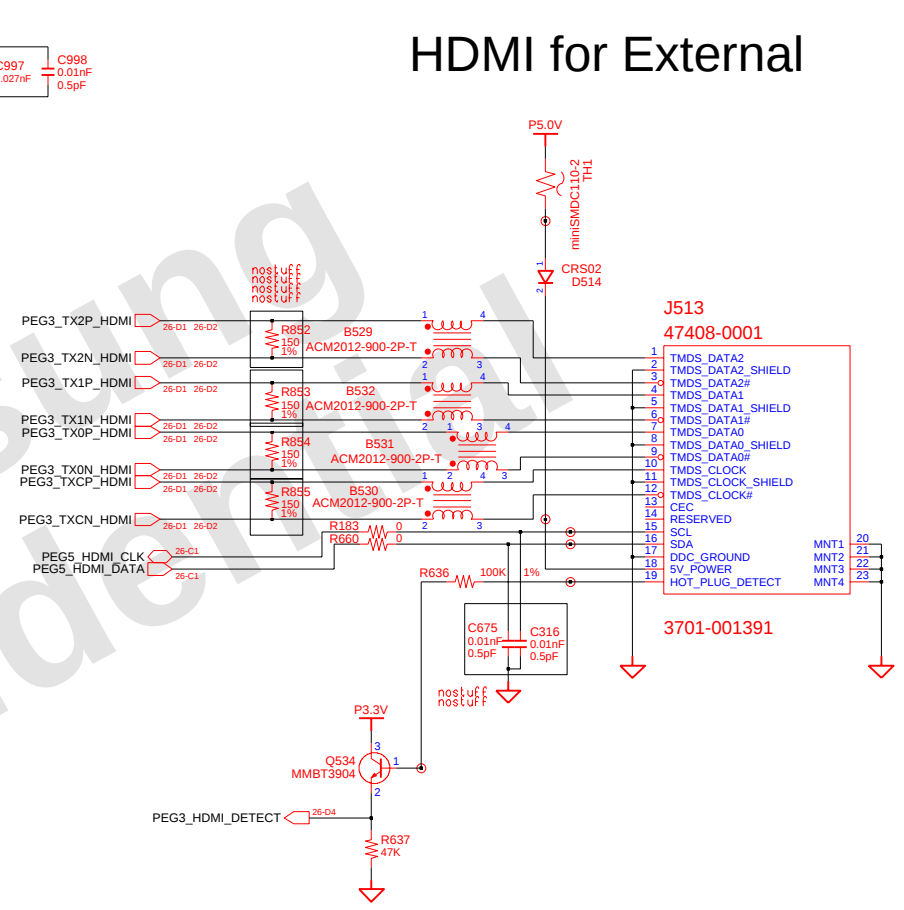
HSDPA / WIBRO, 5.2mm



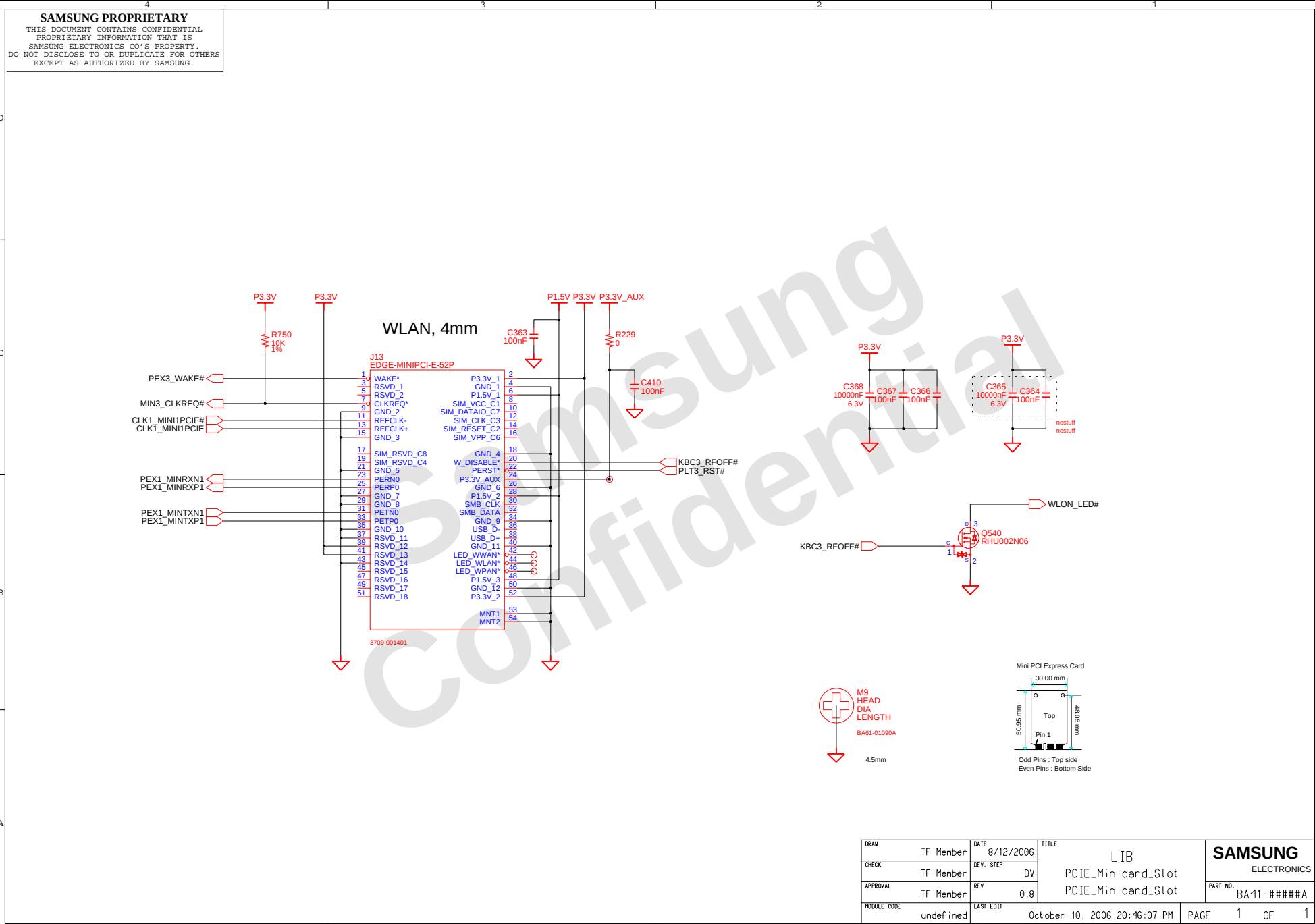
SIM CARD CONN.



HDMI for External

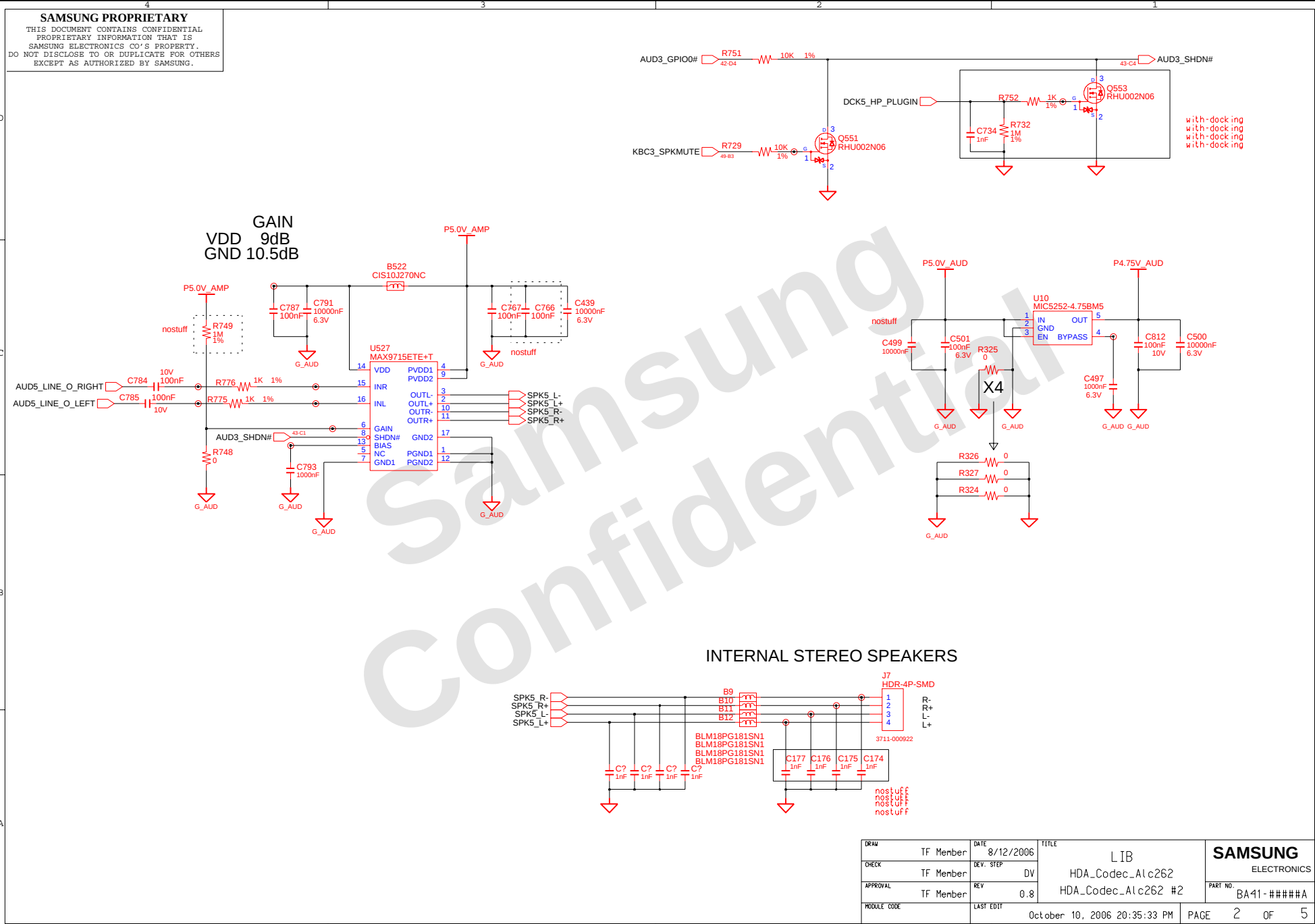


DRAW	IM, KI	DATE	10/25/2006	TITLE	PALAU	SAMSUNG
CHECK	BAIK, SS	DEV. STEP	DV	UNDEFINED	UNDEFINED	ELECTRONICS
APPROVAL	BIN, KK	REV	0.7	UNDEFINED	UNDEFINED	PART NO.
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	15	BA41-####A
				OF	22	

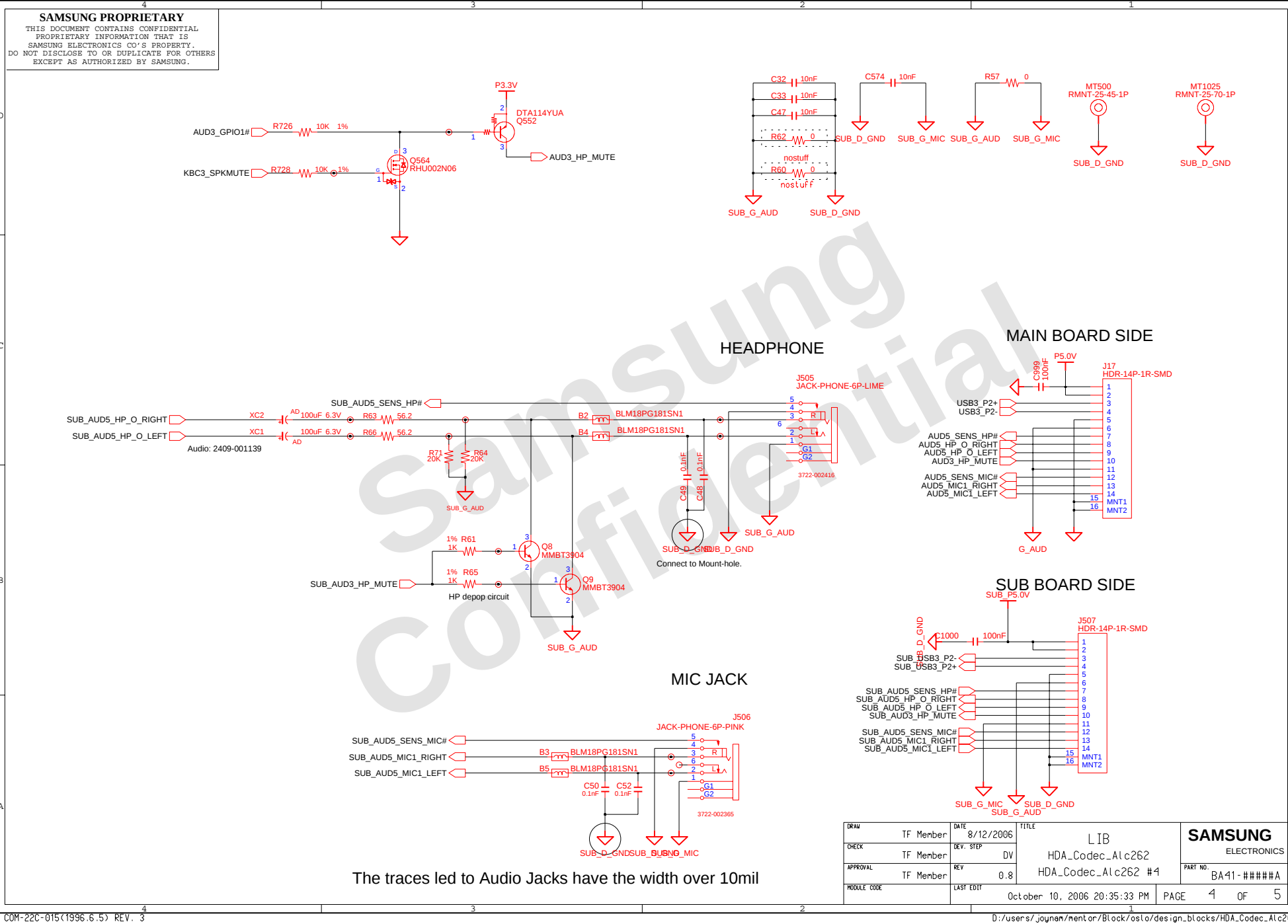


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CHECK	TF Member	DEV. STEP	DV	PCIE_Minicard_Slot		
APPROVAL	TF Member	REV	0.8	PCIE_Minicard_Slot		
MODULE CODE	undefined	LAST EDIT	October 10, 2006 20:46:07 PM	PAGE	1 OF 1	

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB		
CHECK	TF Member	DEV. STEP	DV	HDA_Codec_Alc262			
APPROVAL	TF Member	REV	0.8	HDA_Codec_Alc262 #1		PART NO.	BA41-#####A
MODULE CODE		LAST EDIT		October 10, 2006 20:35:33 PM	PAGE	1	OF 5



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	HDA_Codec_Alc262		
APPROVAL	TF Member	REV	0.8	HDA_Codec_Alc262 #2		
MODULE CODE		LAST EDIT	October 10, 2006 20:35:33 PM	PAGE	2 OF 5	

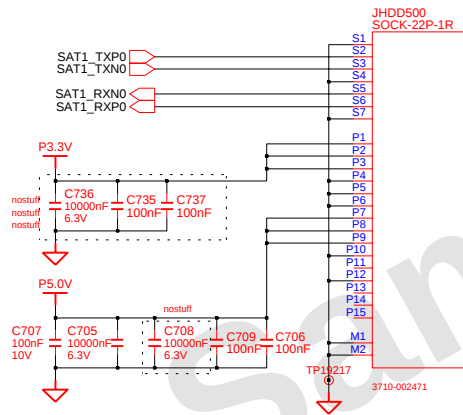


DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	HDA_Codec_Alc262		
APPROVAL	TF Member	REV	0.8	HDA_Codec_Alc262 #4		
MODULE CODE		LAST EDIT	October 10, 2006 20:35:33 PM	PAGE	4 OF 5	

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The schematic diagram illustrates the power management section of the SAM5D31 SoC. It shows the internal structure of the SAM5D31, including the PMIC (U8 MIC5159BM6), the DCDC1 (Q557 SI2315BDS-T1), and the LDO (Q20 EDG653N). The diagram details the connections for various power rails: P5.0V_AUD, P5.0V_AUX, P5.0V_AUD, P5.0V, P5.0V_AMP, and G_AUD. Key components include resistors (R245, R246, R247, R300, R301, R299, C437, C438, C436, C463, C464, C466), capacitors (C437, C438, C436, C463, C464, C466), and transistors (Q20, Q557, Q21). The diagram also shows the connection of the KBC3_PWRON signal to the PMIC and the DCDC1. The schematic is labeled 'Sam5d31' and 'Schematic'.

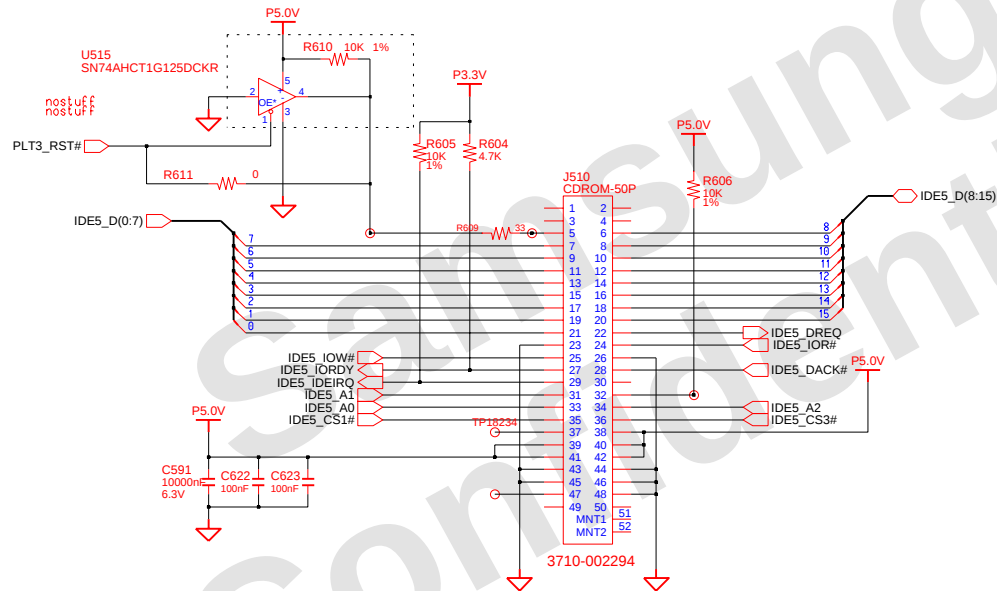
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CHECK	TF Member	DEV. STEP	DV			ELECTRONICS		
APPROVAL	TF Member	REV	0.8			PART NO.	BA11-####A	
MODULE CODE	undefined	LAST EDIT	October 10, 2006 20:35:33 PM			PAGE	5	OF 5



	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)

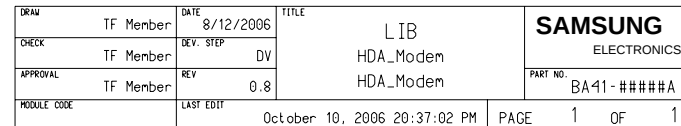
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CHECK	TF Member	DEV. STEP	DV		HDD_IF_Conn	
APPROVAL	TF Member	REV	0.8		HDD_IF_Conn	
MODULE CODE		LAST EDIT	October 12, 2006 12:18:59 PM	PAGE	1 OF 1	

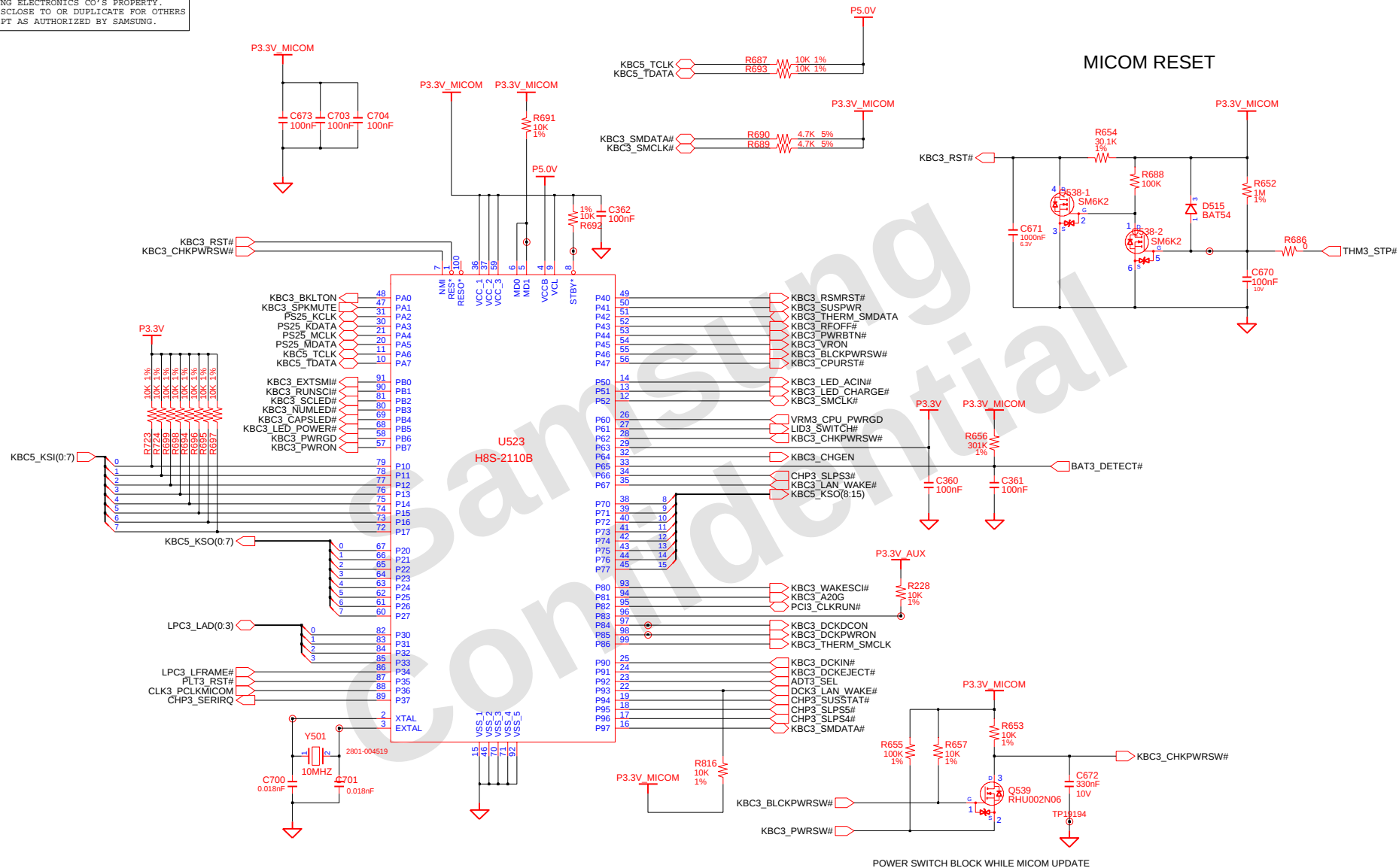
	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	ODD_IF_Conn	ODD_IF_Conn	
APPROVAL	TF Member	REV	0.8			
MODULE CODE		LAST EDIT	October 12, 2006 12:19:50 PM	PAGE	1 OF 1	

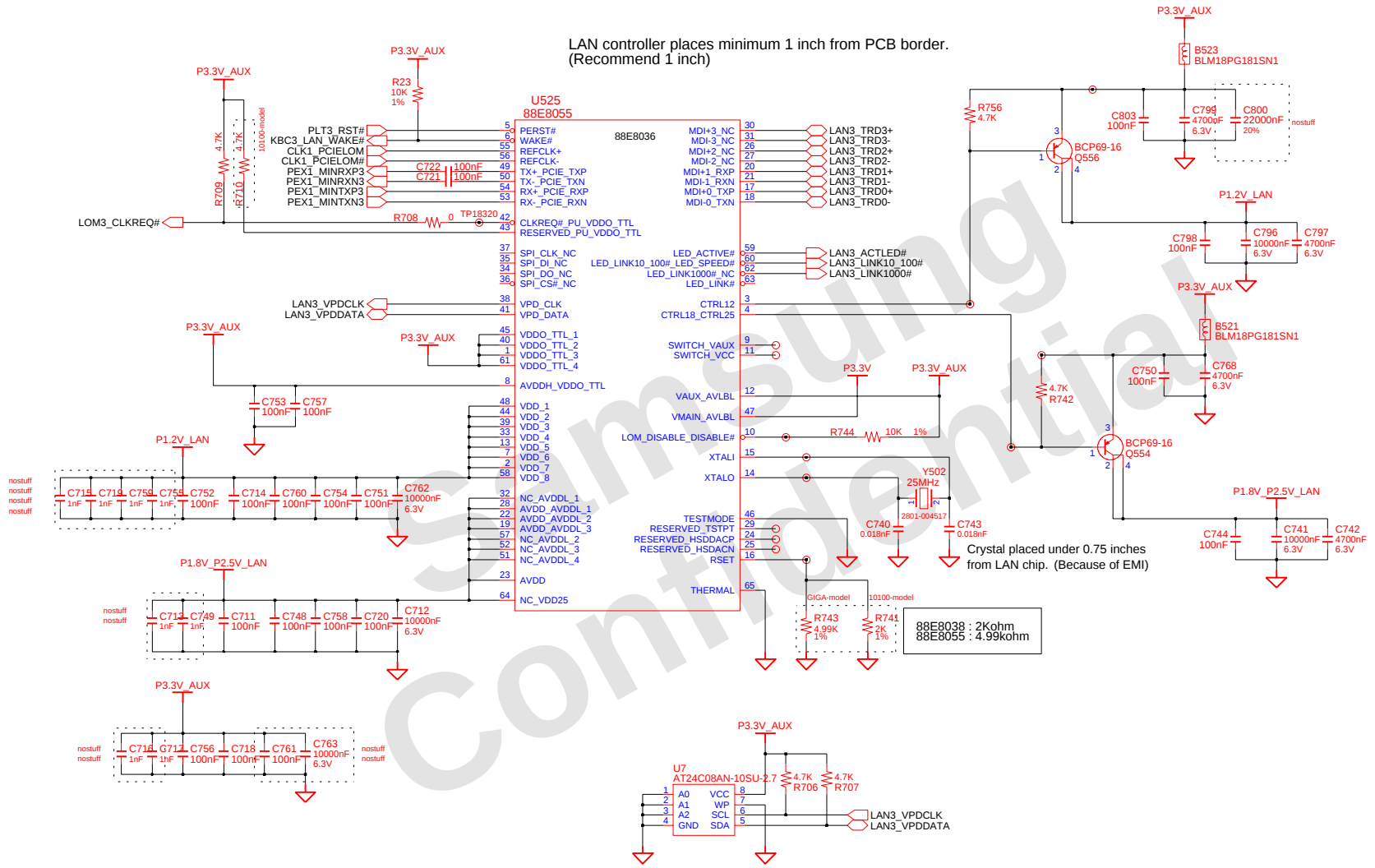
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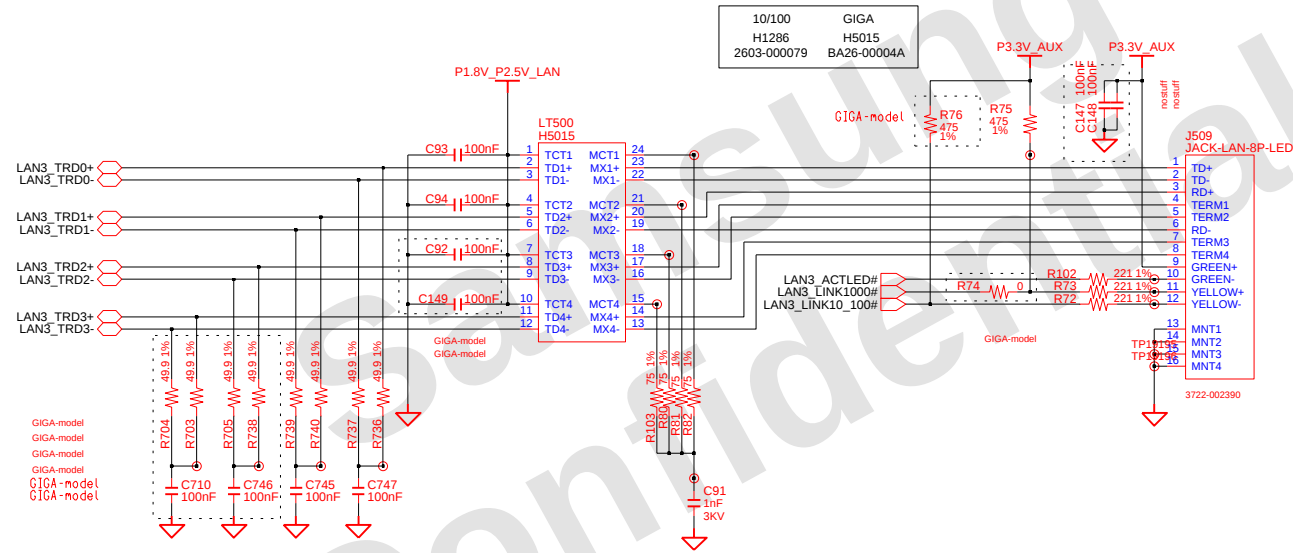
DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	MICOM_Renesas2110_100p		
APPROVAL	TF Member	REV	0.8	MICOM_Renesas2110_100p		
MODULE CODE		LAST EDIT	October 12, 2006 11:48:20 AM	PAGE	1 OF 1	

LAN controller places minimum 1 inch from PCB border.
(Recommend 1 inch)



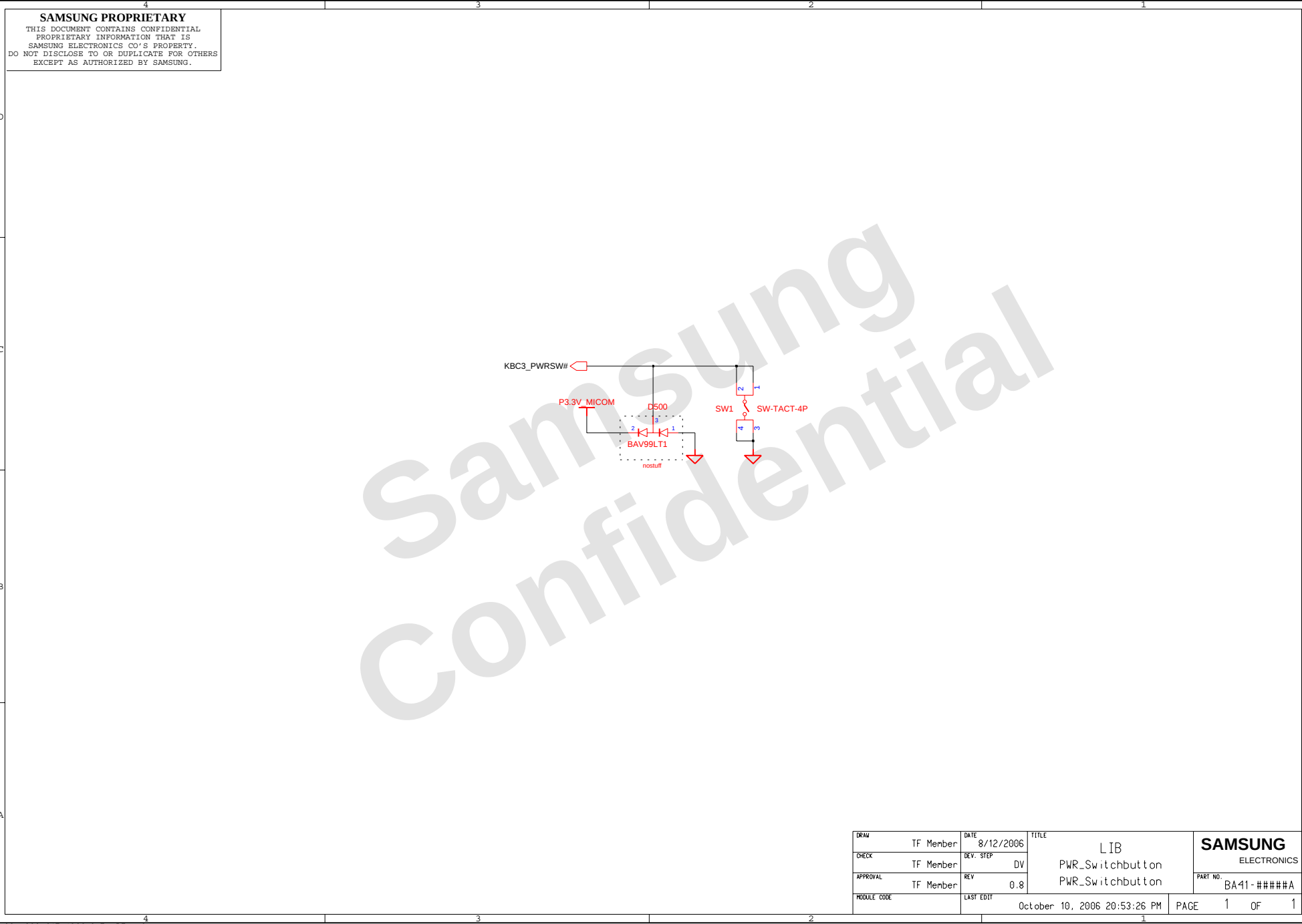
DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	LAN_Marvell_8055		
APPROVAL	TF Member	REV	0.8	LAN_Marvell_8055		
MODULE CODE		LAST EDIT	October 12, 2006 12:07:59 PM	PAGE	1 OF 2	

The distance between LAN controller
and transformer is designed to extend less than two inches.



Place near to the Marvell chip.

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	LAN_Marvell_8055		
APPROVAL	TF Member	REV	0.8	LAN_Marvell_8055		
MODULE CODE		LAST EDIT	October 12, 2006 12:07:59 PM	PAGE 2	OF 2	



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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	PWR_Switchbutton	PWR_Switchbutton	
APPROVAL	TF Member	REV	0.8			
MODULE CODE		LAST EDIT	October 10, 2006 20:53:26 PM	PAGE	1 OF 1	

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The diagram shows the electrical connections for the USB3_P5+ and USB3_P5- signals. The USB3_P5+ signal is connected to pin 1 of connector J9. The USB3_P5- signal is connected to pin 2 of connector J9. The connector J9 is labeled 'HDR-8P-1R-SMD'. The pins are numbered 1 through 10. Pins 1 and 2 are connected to the USB3_P5+ and USB3_P5- signals respectively. Pins 3 and 4 are connected to a common ground. Pins 5 and 6 are connected to a common ground. Pins 7 and 8 are connected to a common ground. Pins 9 and 10 are connected to a common ground. The connector J9 is also labeled with 'MNT1' and 'MNT2' for pins 9 and 10 respectively. The diagram includes a note 'Need to check' and a reference '3711-002127'.

DRAW	TF Member	DATE	8/12/2006	LIB Bluetooth_IF_Conn Bluetooth_IF_Conn	SAMSUNG	
CHECK	TF Member	DEV. STEP	DV		ELECTRONICS	
APPROVAL	TF Member	REV	0.1		PART NO.	BA41-#####
MODULE CODE	LAST EDIT				October 12, 2006 12:10:35 PM	PAGE 1 OF 1

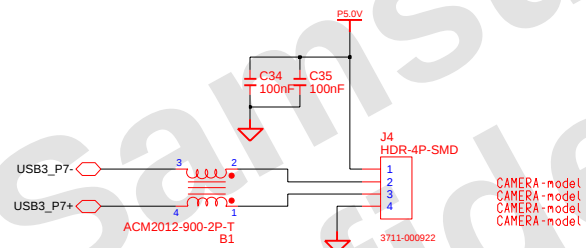
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CAMERA

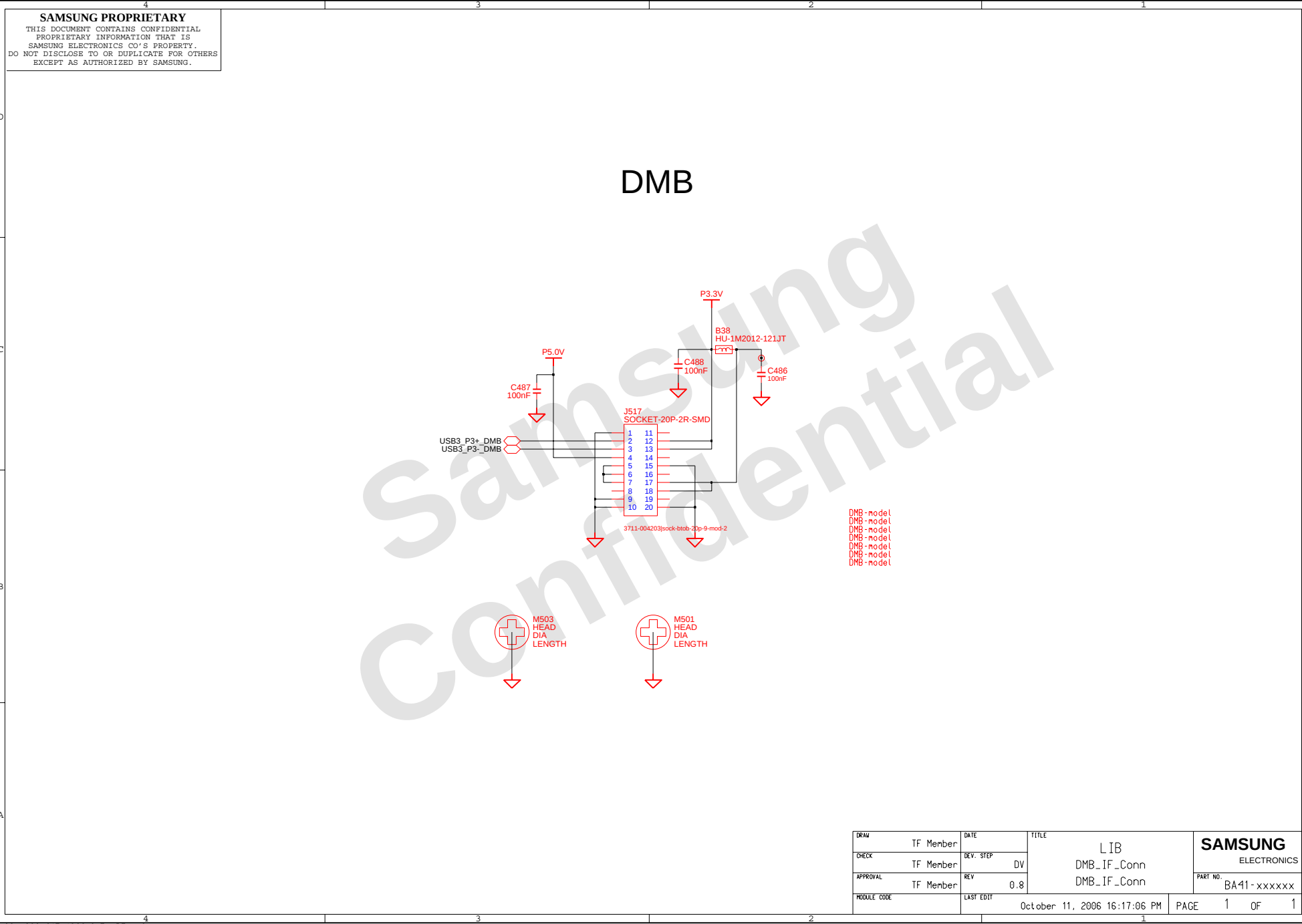
The schematic diagram for the CAMERA module shows the following components and connections:

- USB3_P7- and USB3_P7+:** Input signals connected to the primary of a transformer.
- ACM2012-900-2P-T B1:** A transformer with four pins labeled 1, 2, 3, and 4.
- C34 and C35:** 100nF capacitors connected to the secondary of the transformer.
- 5.0V:** A power supply connection point.
- J4 HDR-4P-SMD:** A 4-pin header with pins 1, 2, 3, and 4.
- 3711-000922:** A component connected to the ground of the header.

The diagram also includes a large diagonal watermark reading "SamSung Confidential".



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB Camera_IF_Conn	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV			
APPROVAL	TF Member	REV	0.8			
MODULE CODE				LAST EDIT	October 12, 2006 12:13:19 PM	PAGE 1 OF 1



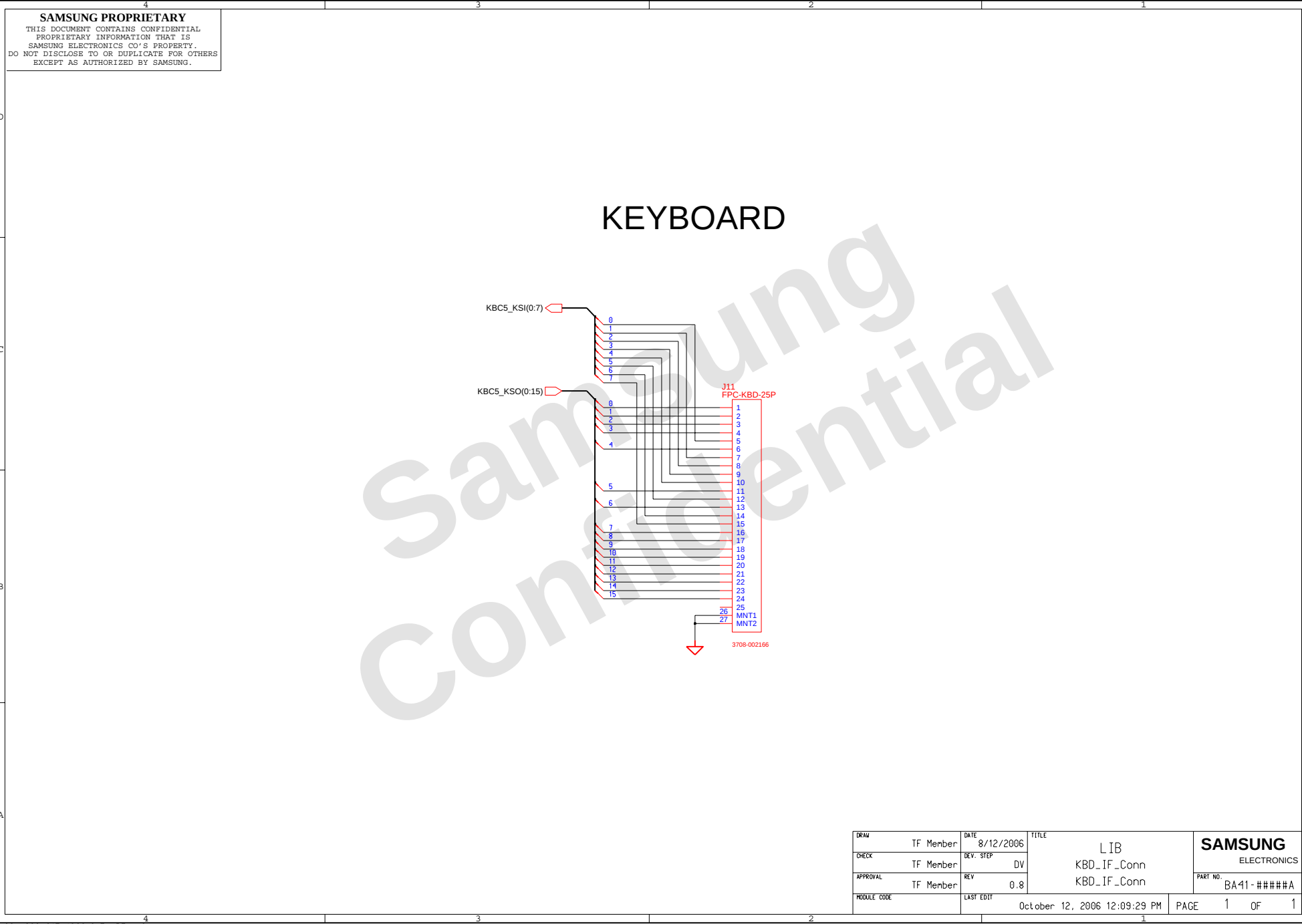
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TOUCHPAD



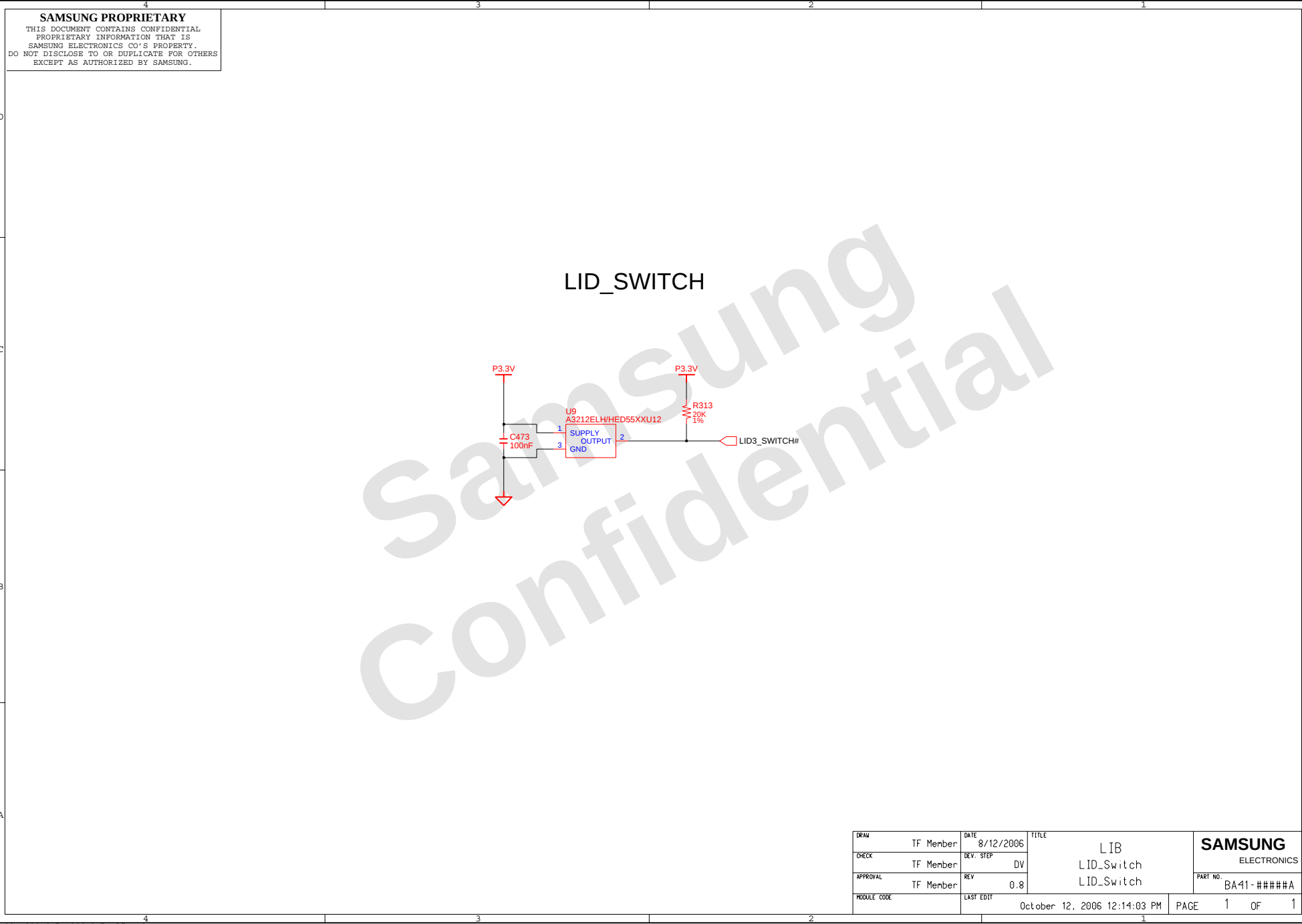
DRAW	TF Member	DATE	8/12/2006	LIB Touchpad_IF_Conn Touchpad_IF_Conn	SAMSUNG ELECTRONICS	
CHECK	TF Member	DEV. STEP	DV			
APPROVAL	TF Member	REV	0.8		PART NO.	BA41-####A
MODULE CODE	LAST EDIT				October 12, 2006 12:11:36 PM	PAGE 1 OF 1



KEYBOARD

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DRAW	TF Member	DATE	8/12/2006	TITLE	L IB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	KBD_IF_Conn		
APPROVAL	TF Member	REV	0.8	KBD_IF_Conn		
MODULE CODE	LAST EDIT			October 12, 2006 12:09:29 PM	PAGE	1 OF 1

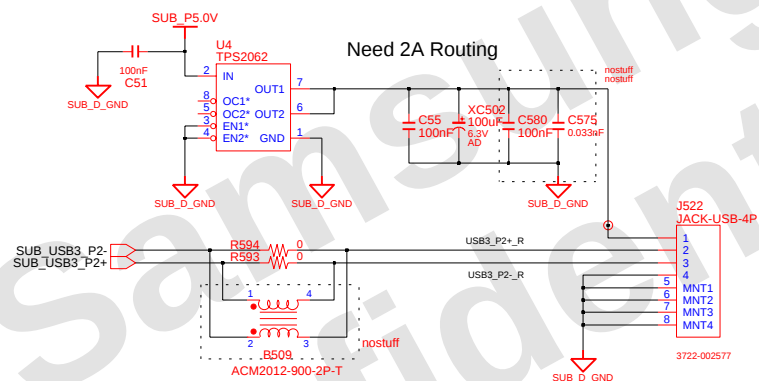


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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	LID_Switch		
APPROVAL	TF Member	REV	0.8	LID_Switch		
MODULE CODE	LAST EDIT			October 12, 2006 12:14:03 PM	PAGE	1 OF 1

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1 PORT USB CONNECTOR

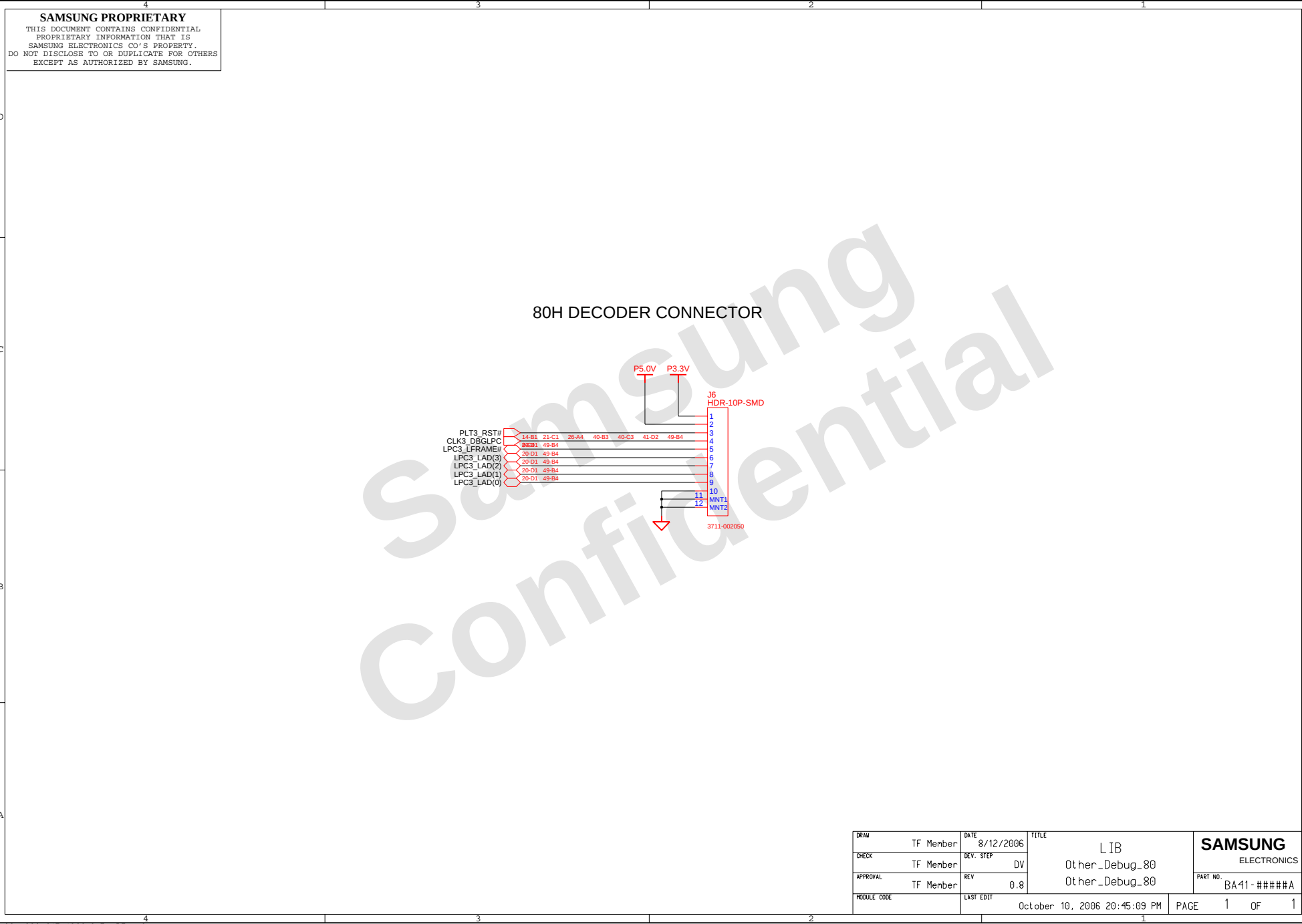


DRAW	TF Member	DATE	8/12/2006	LIB USB_1Port USB_1Port	SAMSUNG ELECTRONICS	
CHECK	TF Member	DEV. STEP	DV			
APPROVAL	TF Member	REV	0.8			
MODULE CODE			LAST EDIT	October 10, 2006 20:57:32 PM	PAGE	1 OF 1

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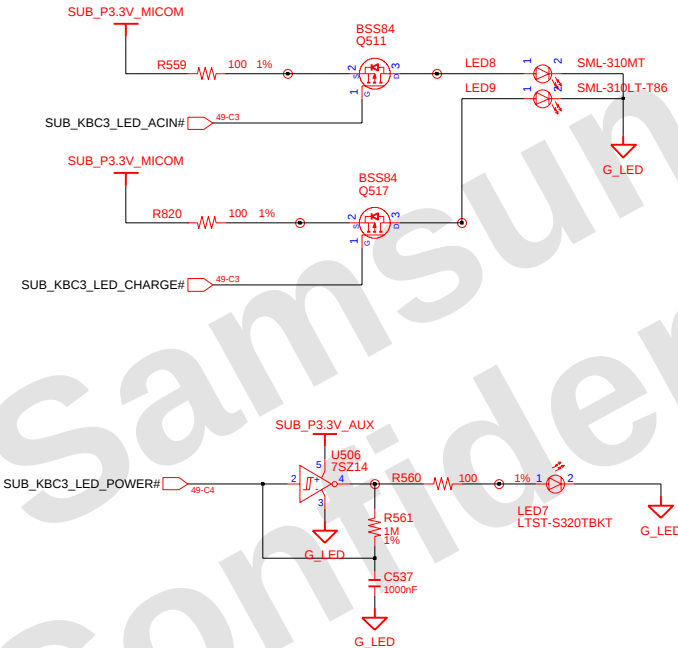
The schematic diagram illustrates the power and data connections for a USB3.0 module. The power section features a 5.0V regulator (U500 TPS2062) with input capacitors C505 (100nF) and C508 (100uF), and output capacitors U541 (100uF) and C830 (100nF). The data section shows USB3_P0- and USB3_P0+ connections to a transformer (B501 ACM2012-900-2P-T) and a USB3_P1- and USB3_P1+ connection to another transformer (B500 ACM2012-900-2P-T). The module is labeled "Need 4A Routing" and "3722-002382".

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB USB_2Port	SAMSUNG ELECTRONICS	PART NO.	BA41- #####	
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APPROVAL	TF Member	REV	0.8						USB_2Port
MODULE CODE	LAST EDIT								October 10, 2006 20:58:16 PM

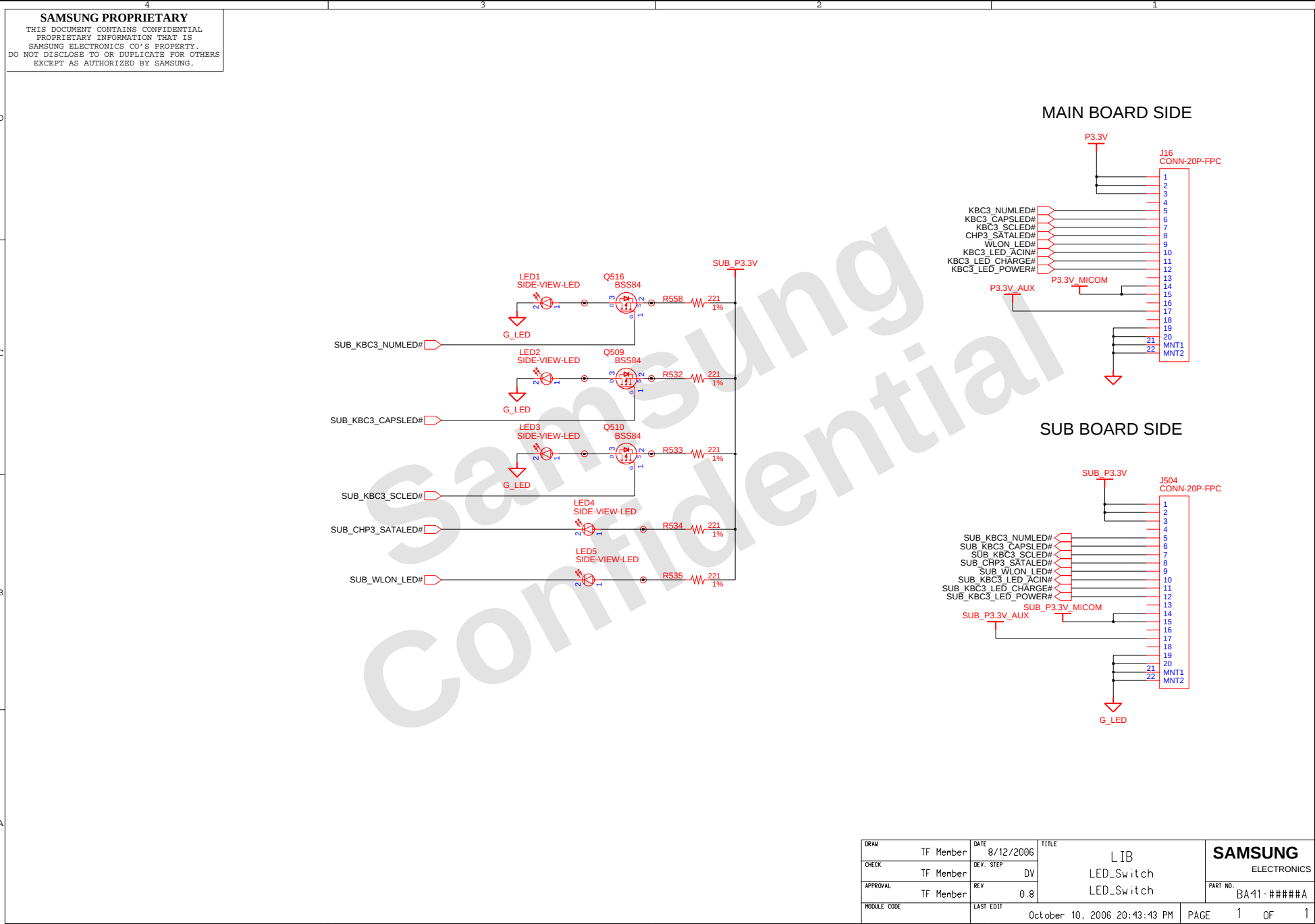


DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV	Other_Debug_80	Other_Debug_80	
APPROVAL	TF Member	REV	0.8			
MODULE CODE		LAST EDIT	October 10, 2006 20:45:09 PM	PAGE	1 OF 1	

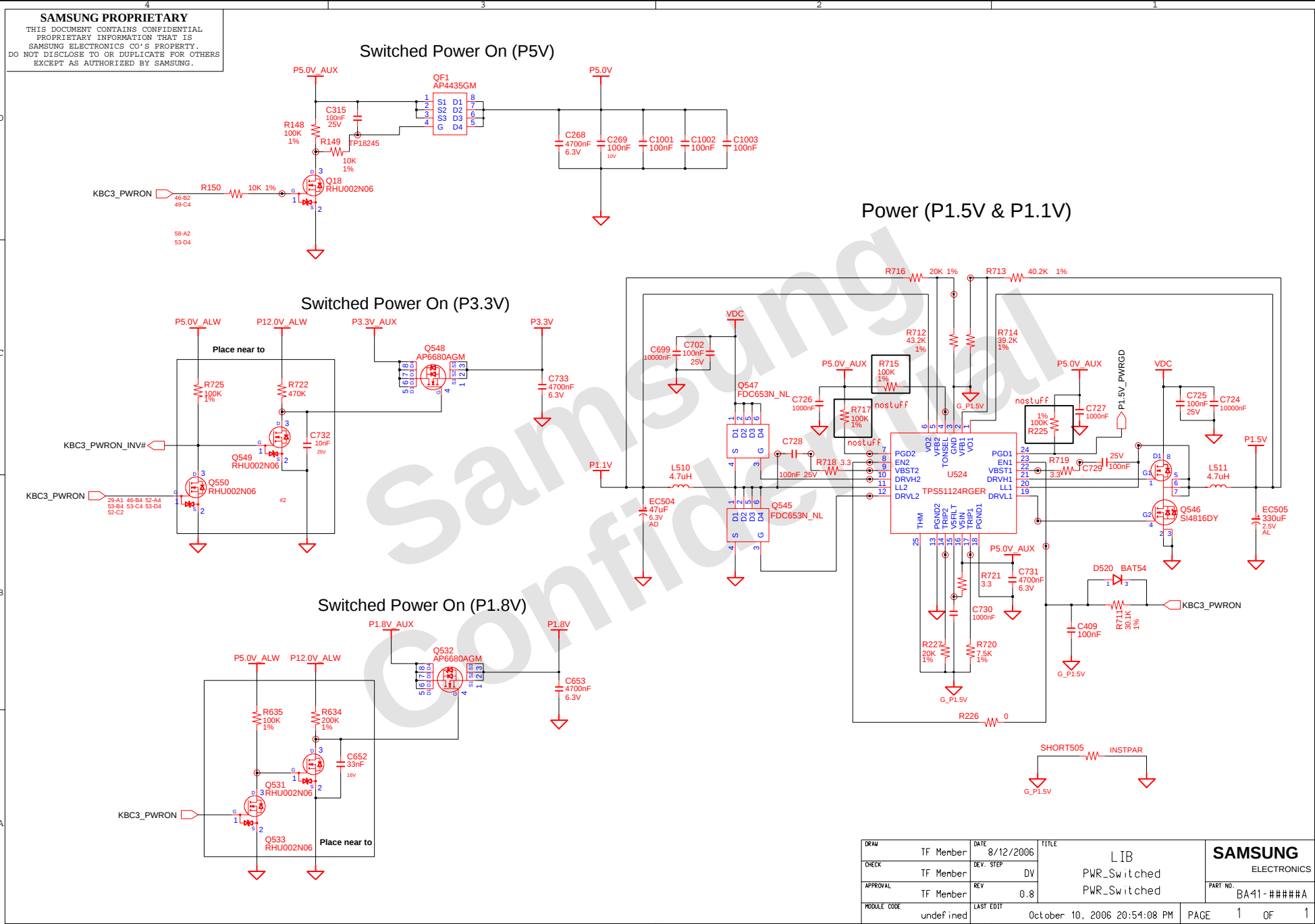
ADAPTERIN/CHARGING LED



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	PWR_Charger		
APPROVAL	TF Member	REV	0.8	PWR_Charger #1		
MODULE CODE	LAST EDIT		October 10, 2006 20:48:53 PM	PAGE	1 OF 2	PART NO. BA41-####A



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV			
APPROVAL	TF Member	REV	0.8			
				PART NO.	BA41-#####A	
MODULE CODE	LAST EDIT			October 10, 2006 20:43:43 PM	PAGE	1 OF 1



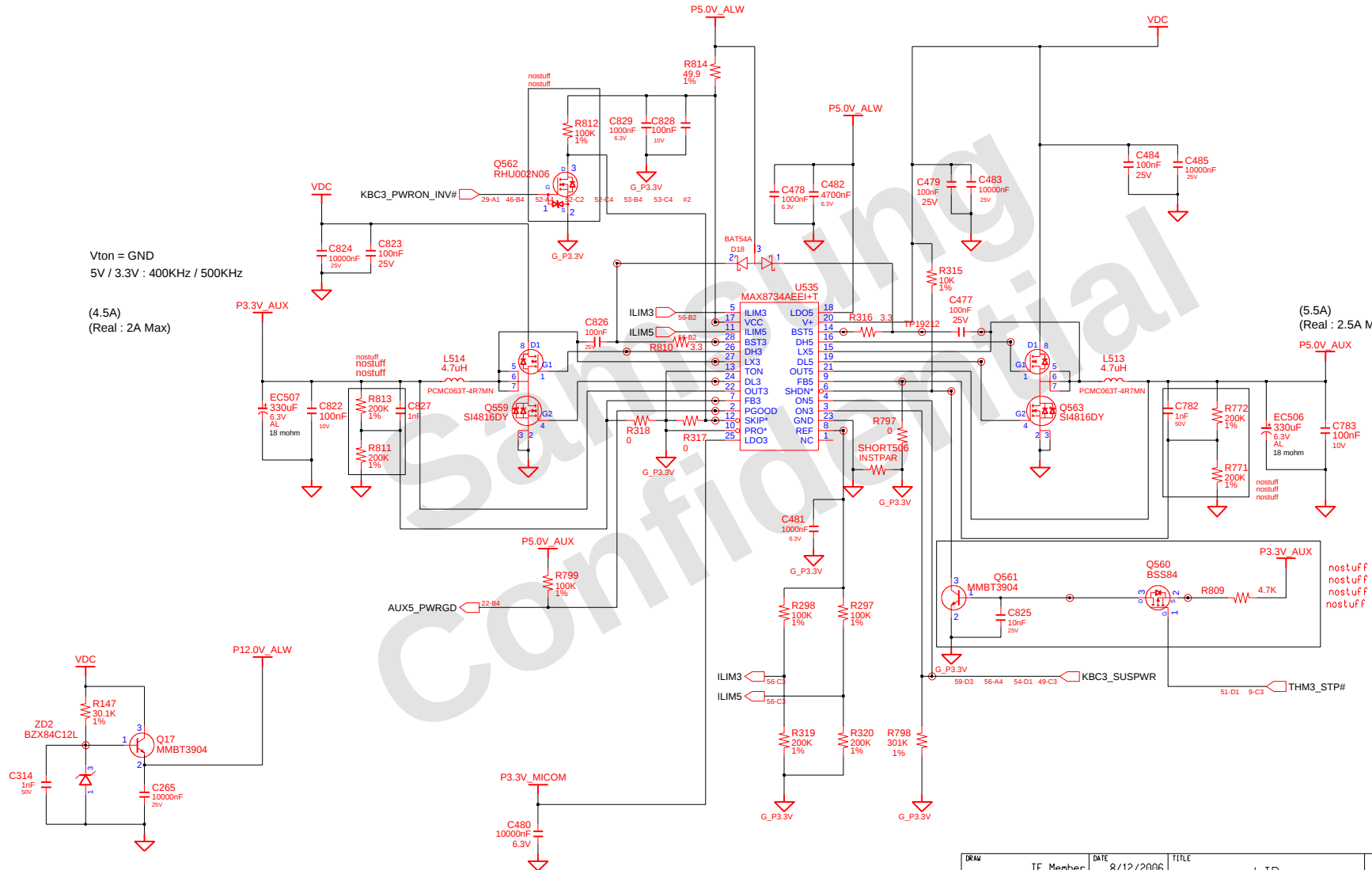
DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	TF Member	DEV. STEP	DV		PWR_Switched	
APPROVAL	TF Member	REV	0.8		PWR_Switched	
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:54:08 PM	PAGE	1	OF 1

P3.3V_ALW/AUX & P5V_AUX

V_{ton} = GND
5V / 3.3V : 400KHz / 500KHz

(4.5A)
(Real : 2A Max)

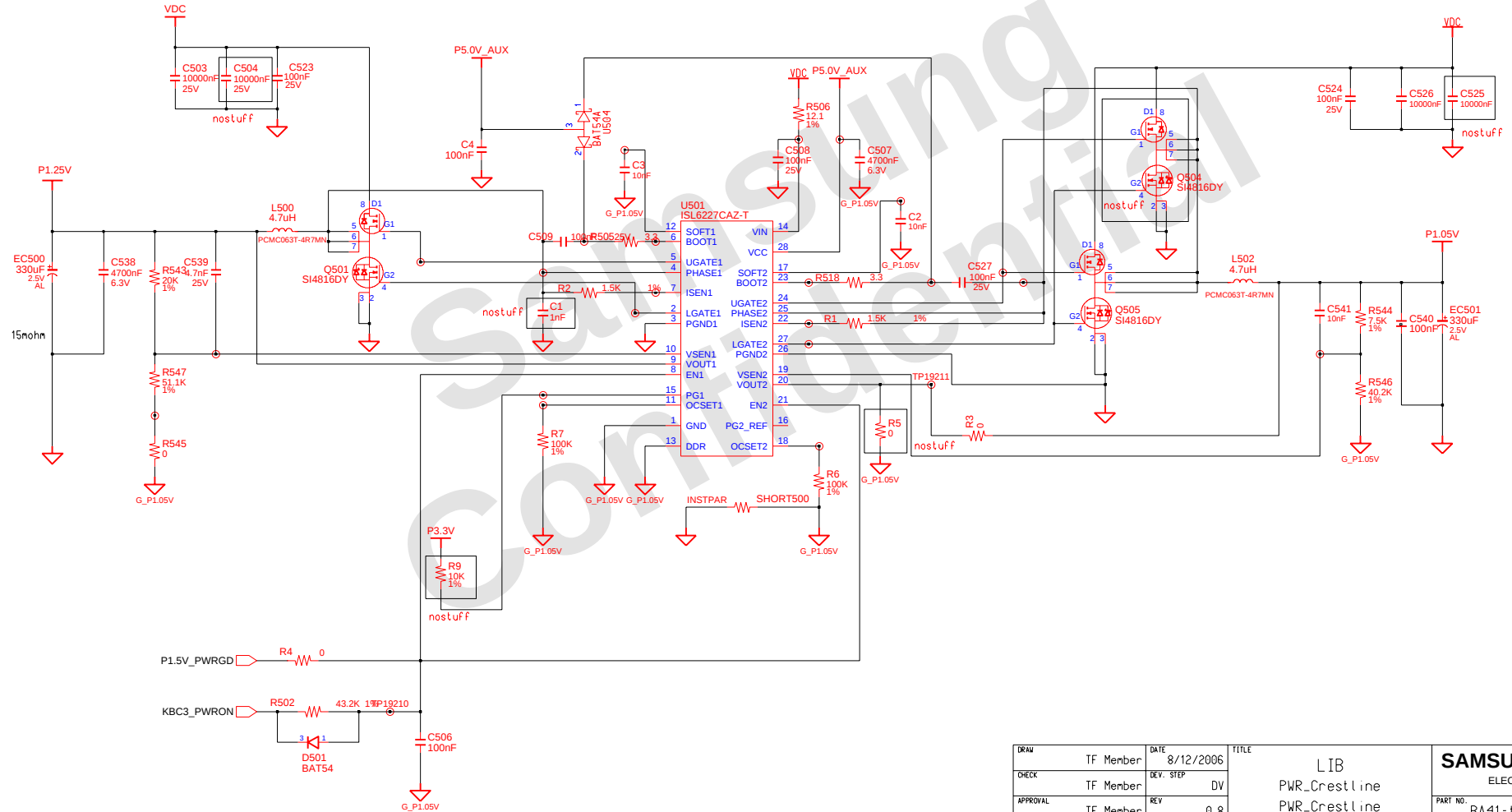
(5.5A)
(Real : 2.5A Max)



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG
CHECK	TF Member	DEV. STEP	DV		PWR_3V_5V	ELECTRONICS
APPROVAL	TF Member	REV	0.8		PWR_3V_5V	PART NO. BA41-####A
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:47:11 PM	PAGE	1 OF 1	

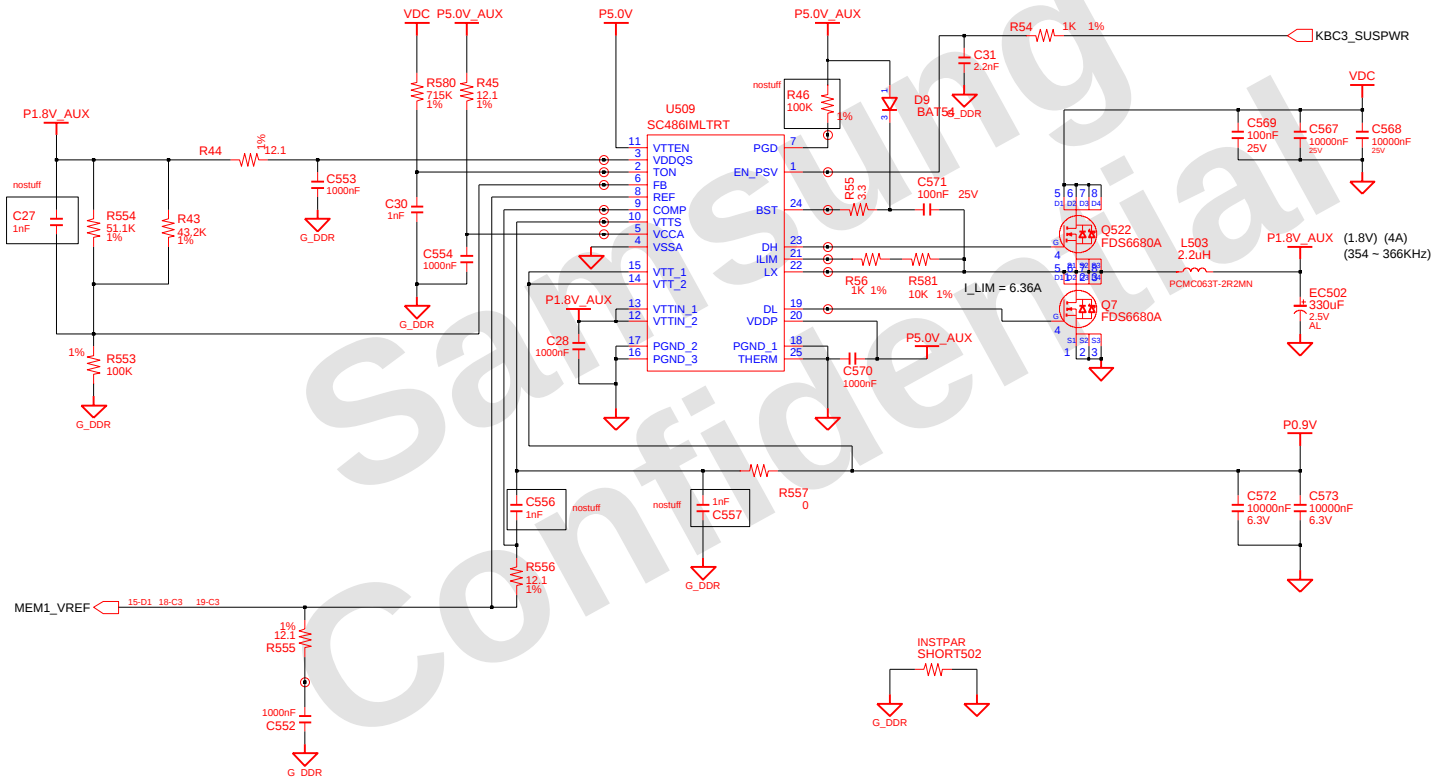
VCCP & P1.25V

LOCATION	PM-model	
	SEC P/N	VENDOR P/N
R2563	2007-007528	1.5Kohm, 1%, 1005
Q967	0505-001386	FDS6680A
Q968	0505-001386	FDS6680A
L815	2703-002530	IHLP2525CZ-01 2.2uH
EC845	2402-001168	2R5TPE330MF



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	TF Member	DEV. STEP	DV		PWR_Crestline	
APPROVAL	TF Member	REV	0.8		PWR_Crestline	
MODULE CODE		LAST EDIT	October 10, 2006 20:50:14 PM	PAGE	1 OF 1	

DDR2 Power



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG
CHECK	TF Member	DEV. STEP	DV	PWR_Memory	PWR_Memory	ELECTRONICS
APPROVAL	TF Member	REV	0.8	PWR_Memory	PWR_Memory	PART NO.
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:52:43 PM	PAGE	1 OF 1	BA41-####A

CPU VRM [SEMTECH]

