VBLE4 / VBLE5

Eureka

LA-8868P REV 1.0 Schematic

AMD Brazos 2.0 / Zacate APU / Hudson-M3L FCH
2012-07-12 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2012/05/18	Deciphered Date	2013/10/05

Compal Electronics, Inc.		
Title: SCHEMATIC, MB A8868		
Size: Custom	Document Number: 4019K4	Rev: B
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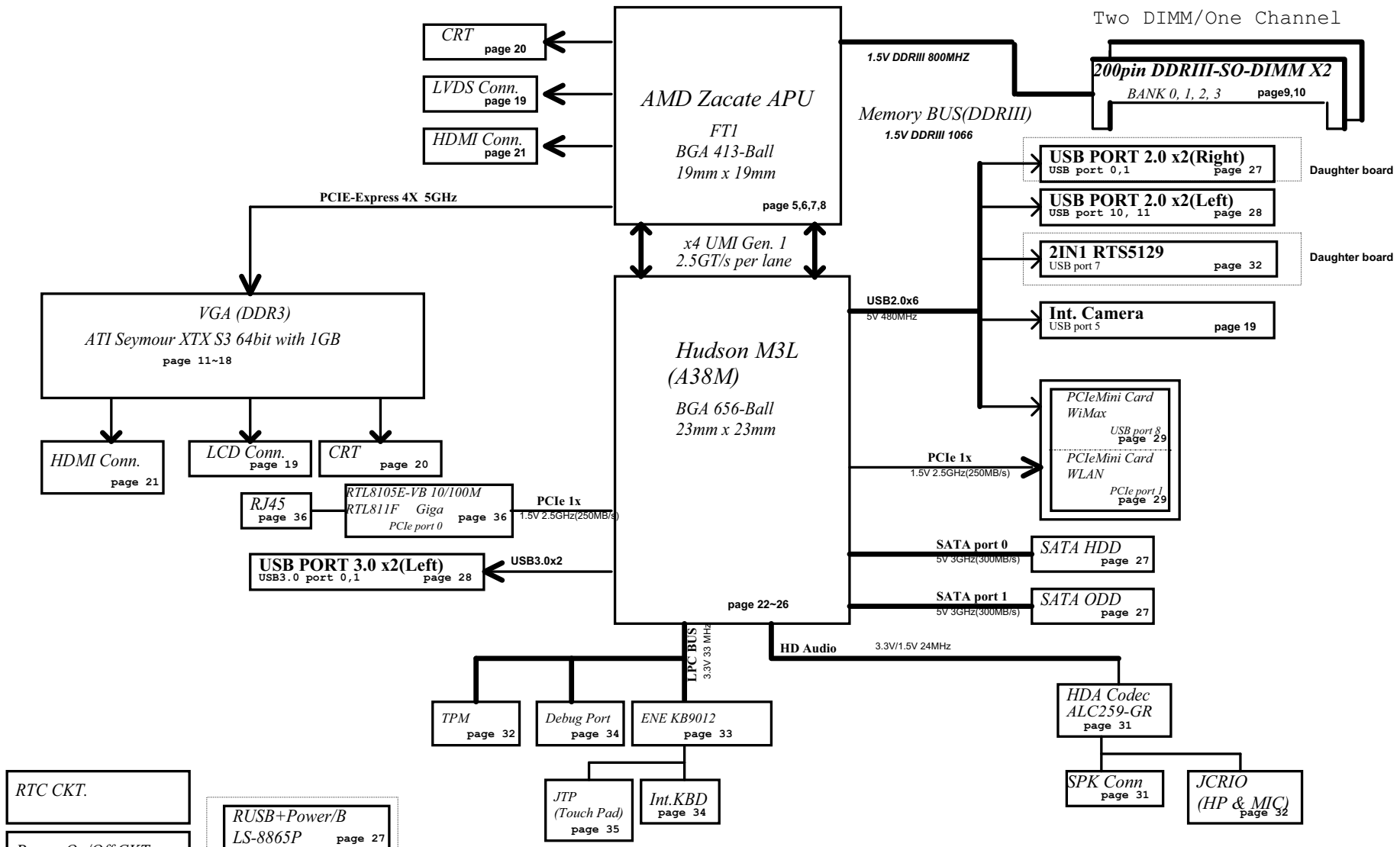

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Compal Electronics, Inc.

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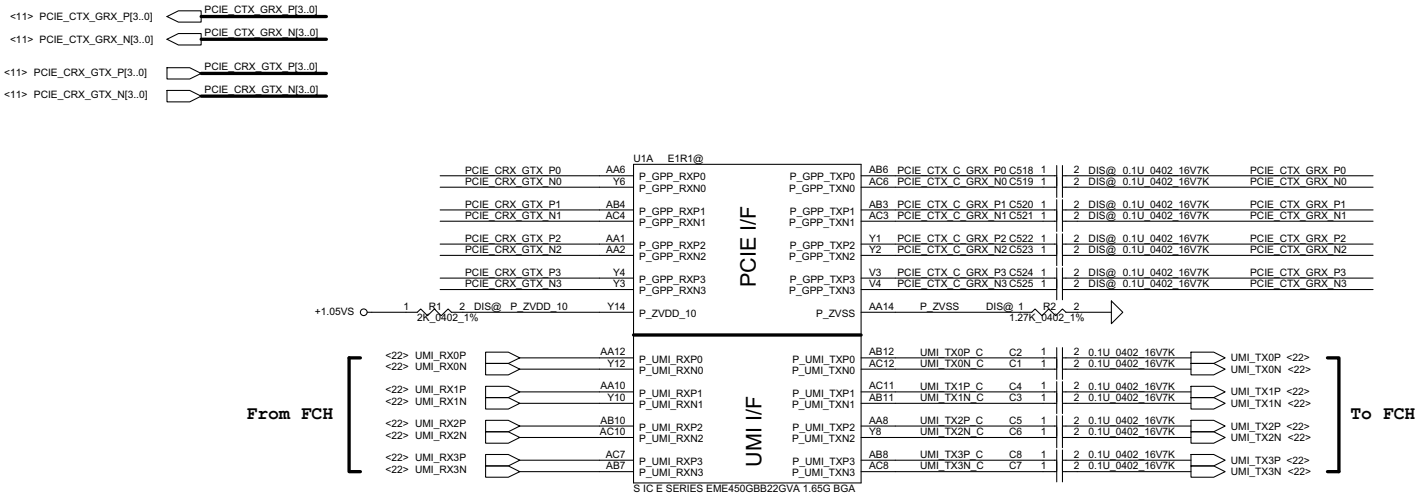
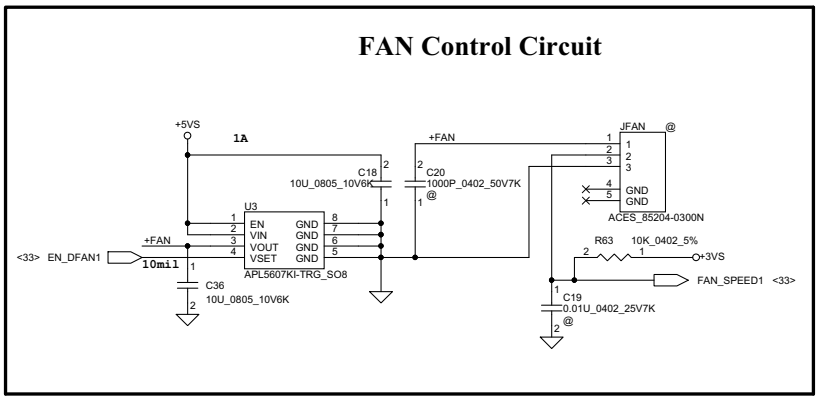


FAN Control Circuit



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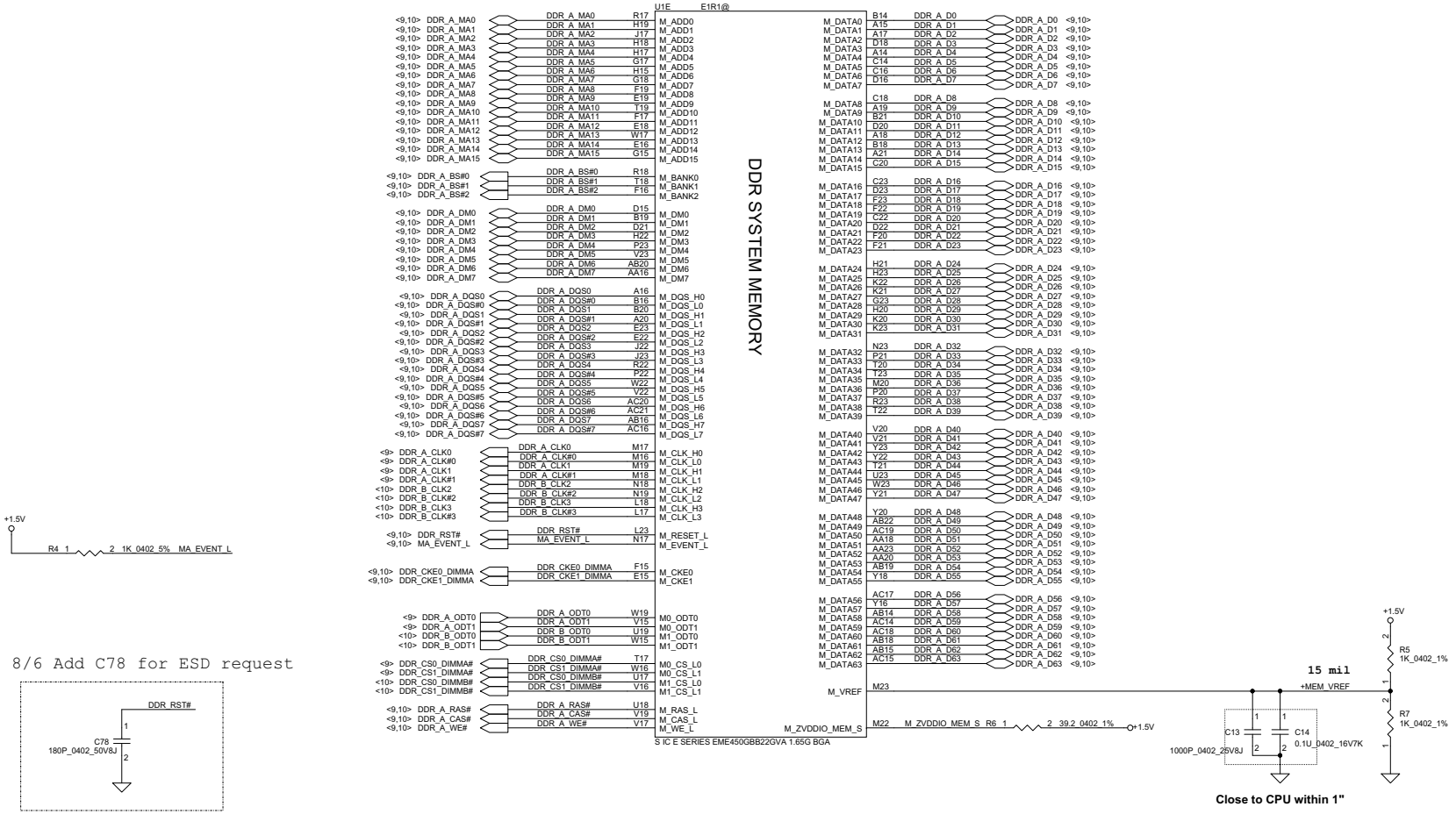

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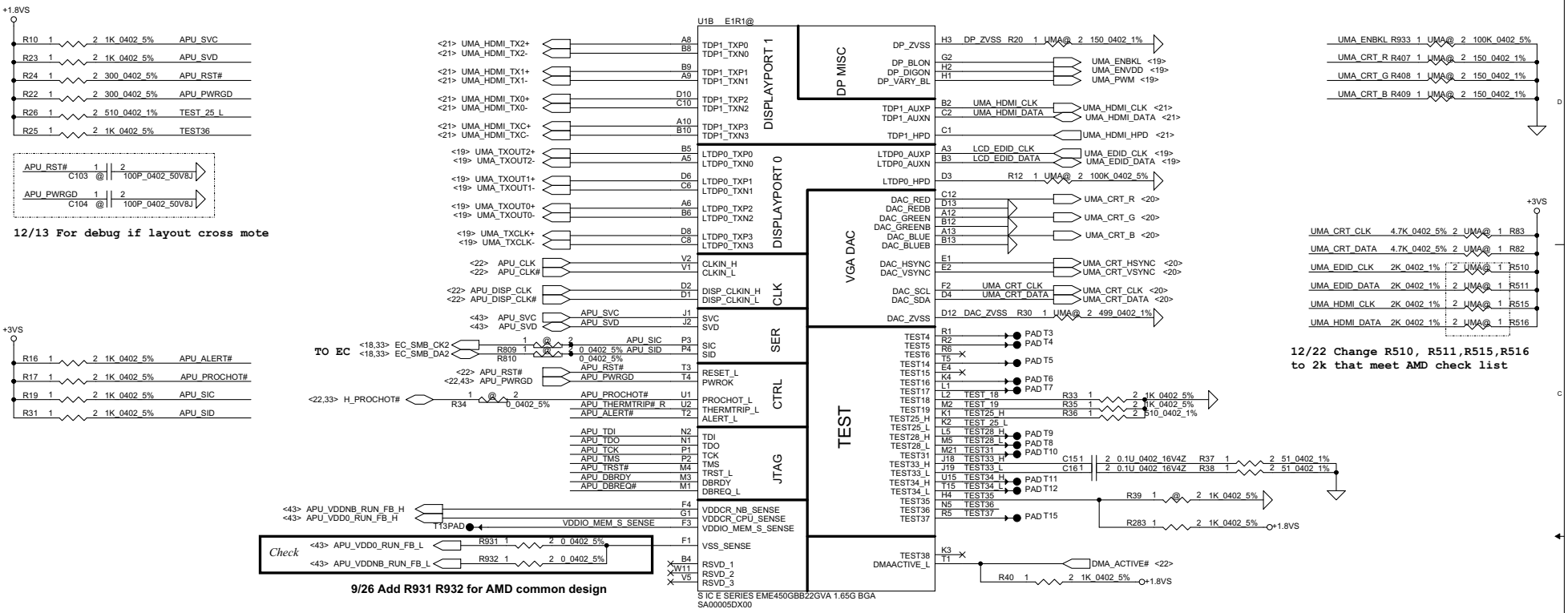
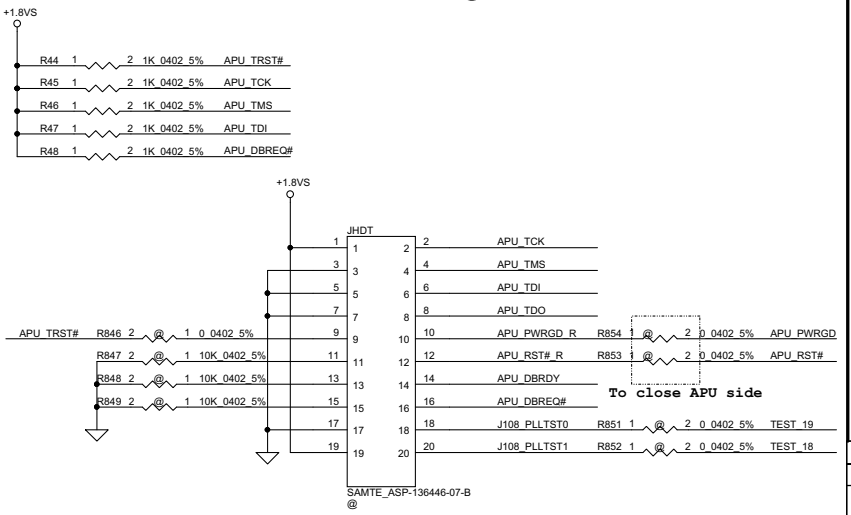
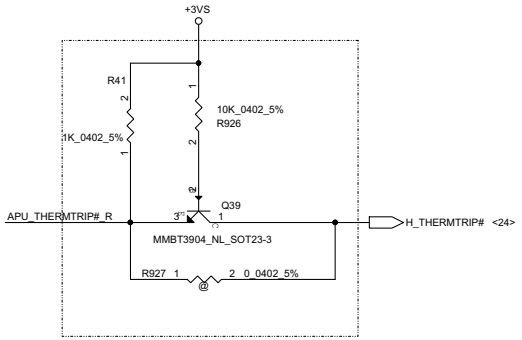


AMD HDT Debug Conn





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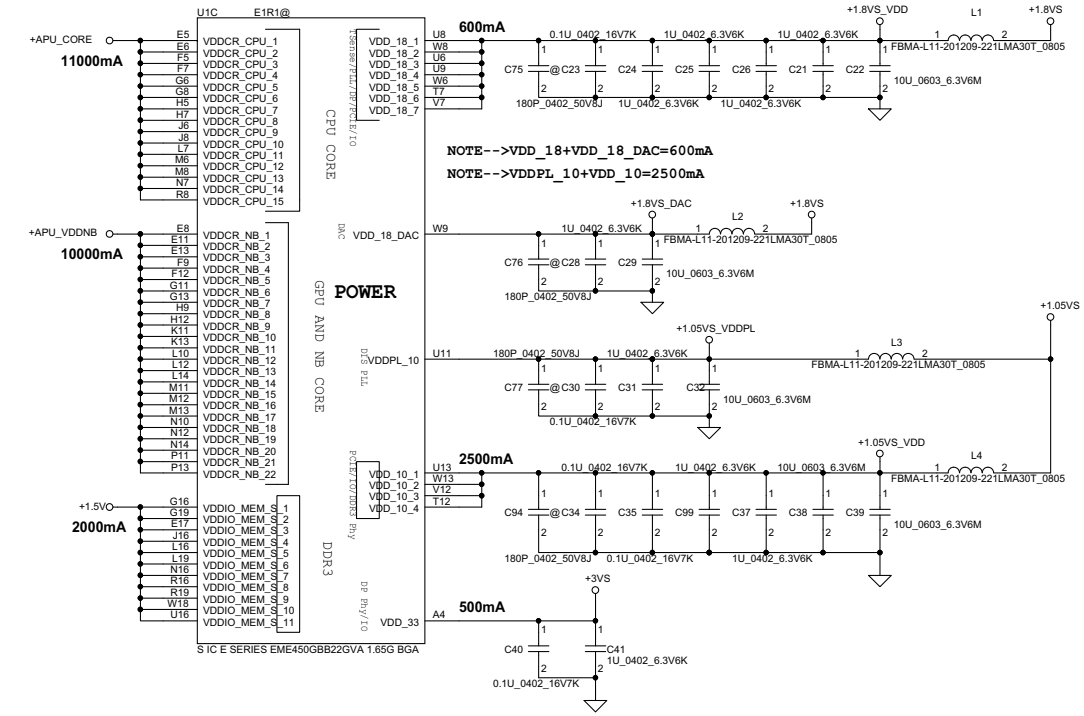
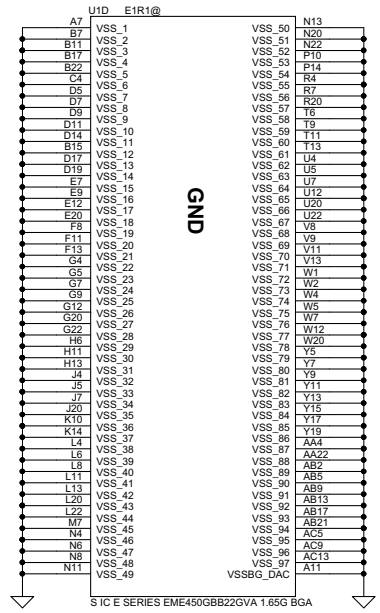
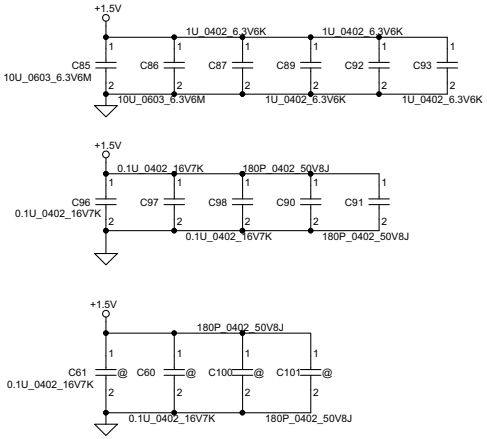
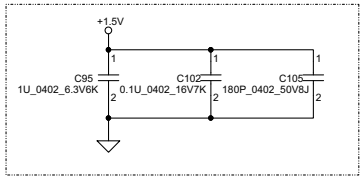






Add for EMI request on DVT



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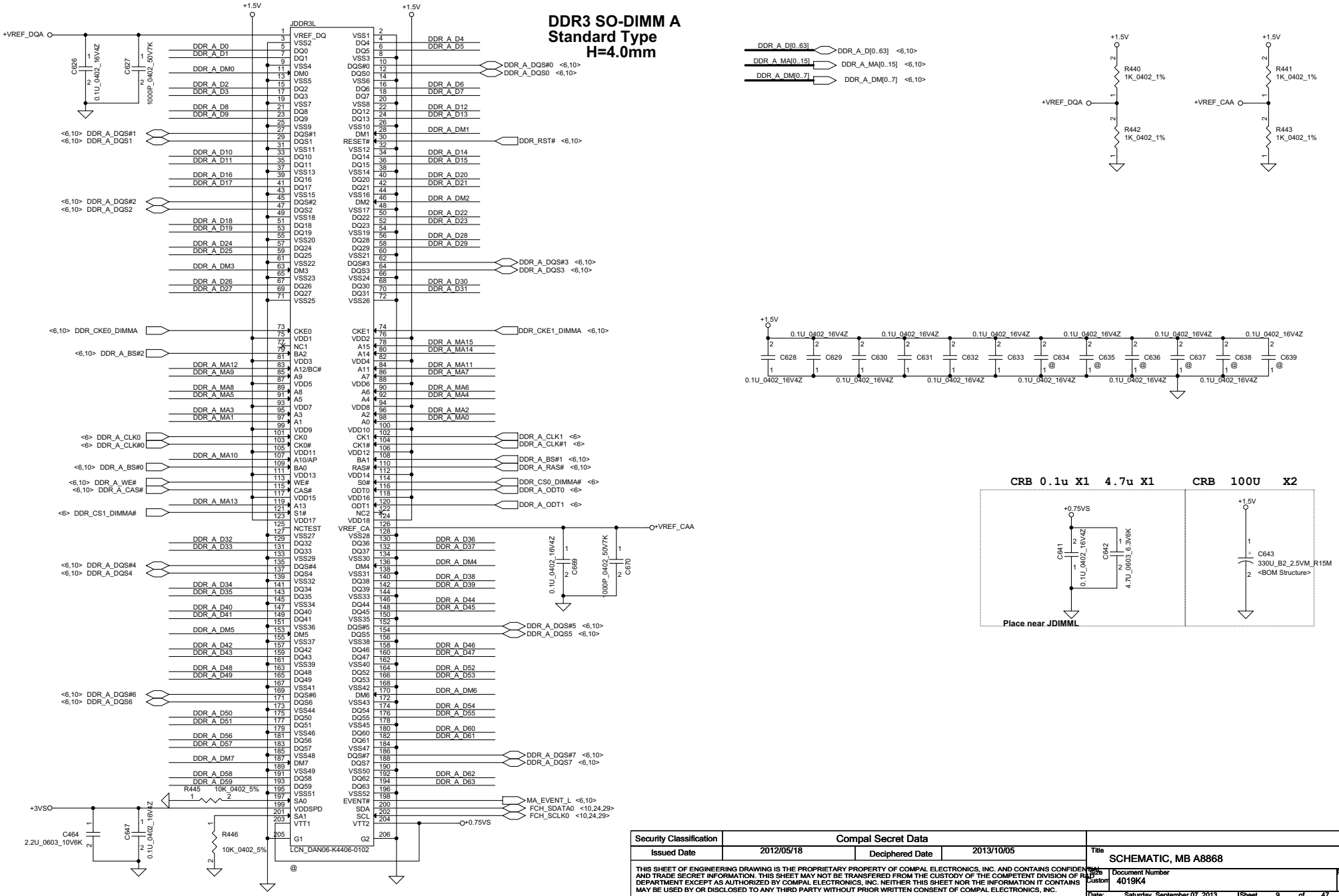
DDR3 SO-DIMM A
Standard Type
H=4.0mm



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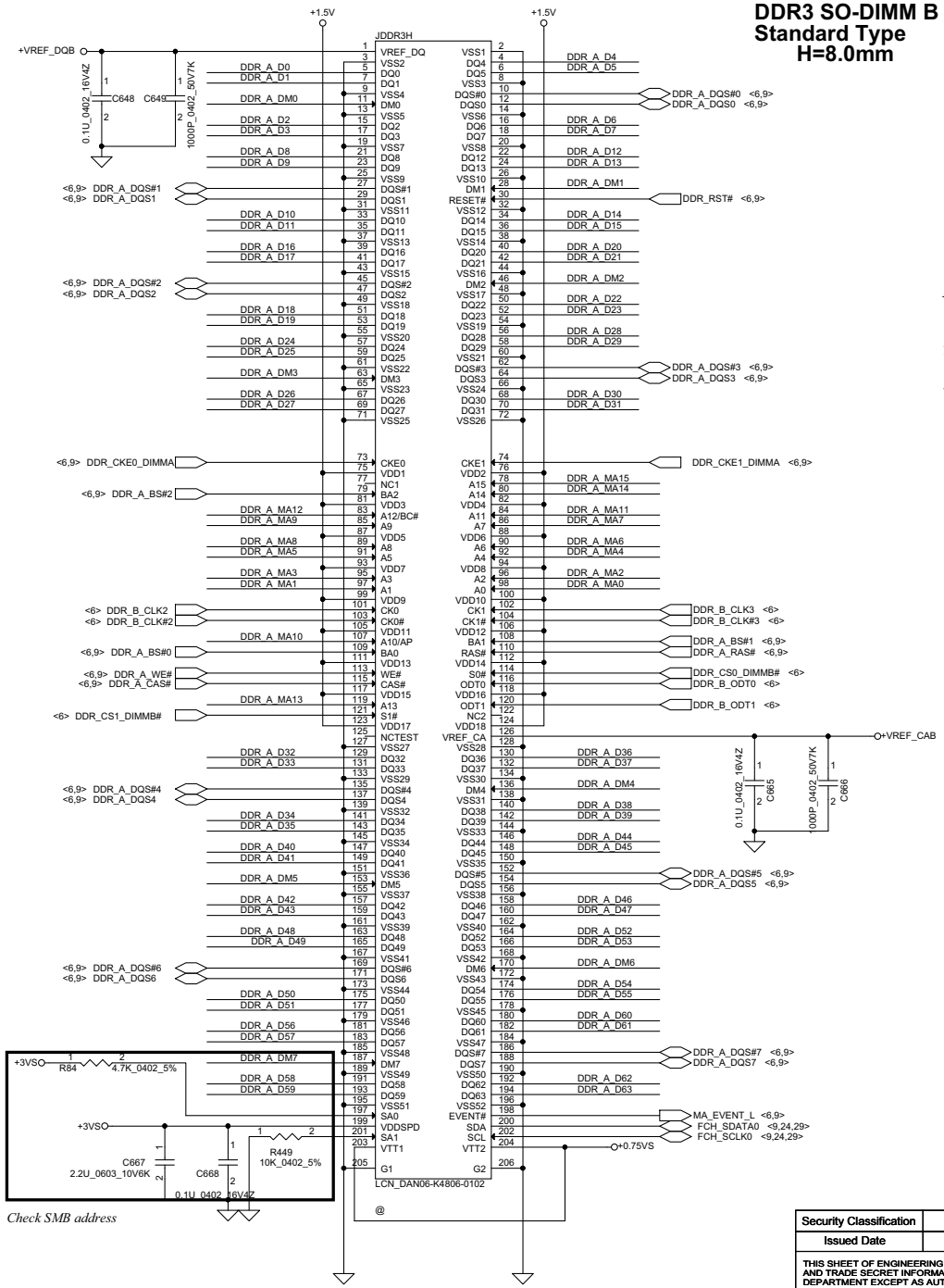
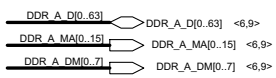
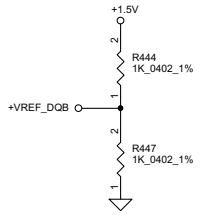
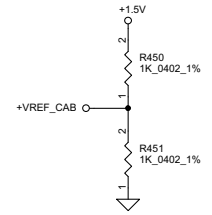
DDR3 SO-DIMM B
Standard Type
H=8.0mm

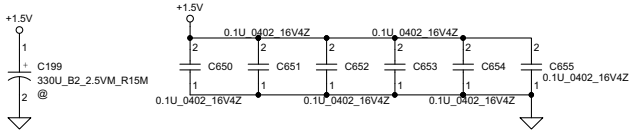


Check SMB address

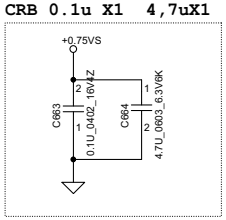








CRB 0.1u X1 4,7uX1



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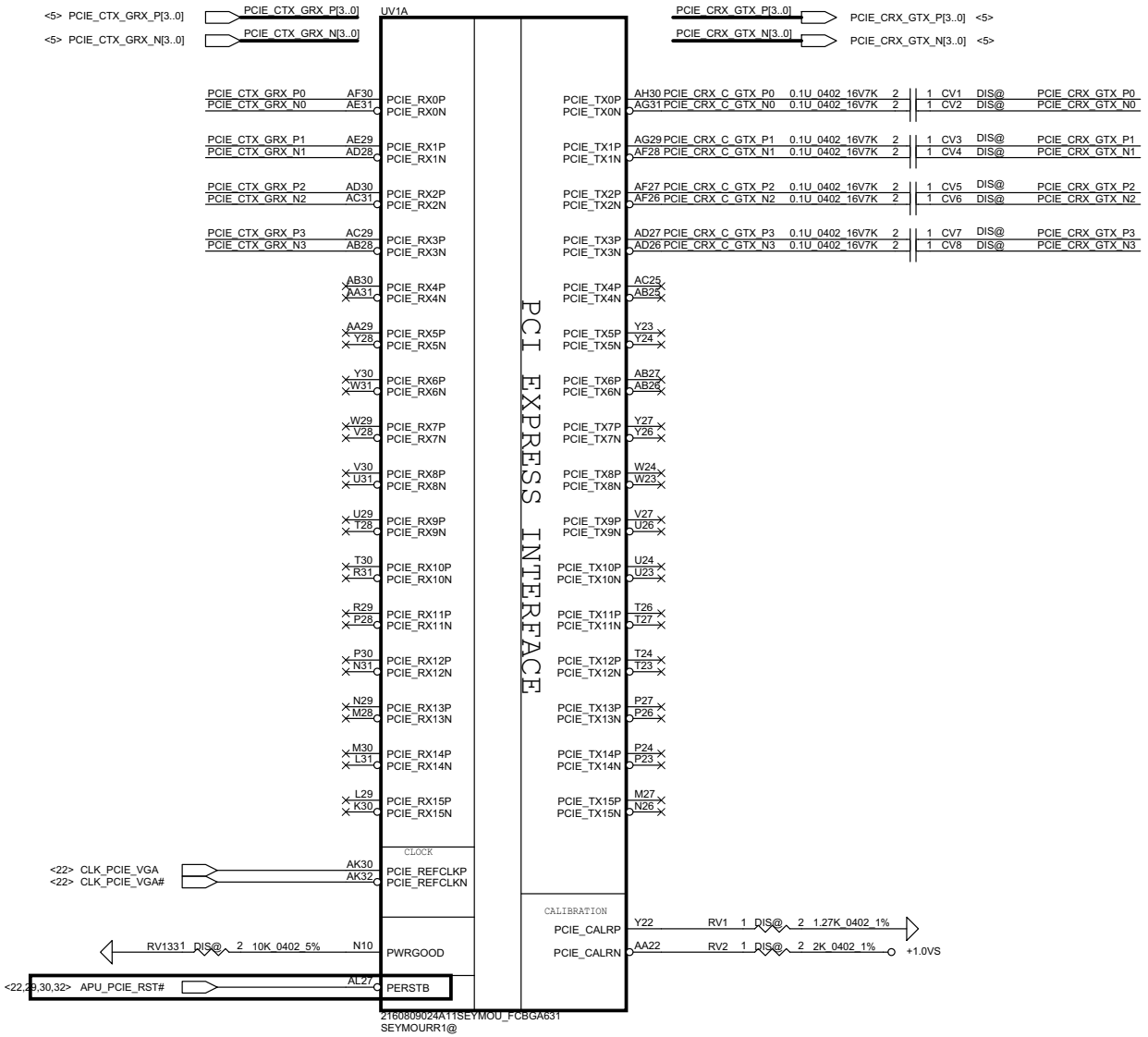

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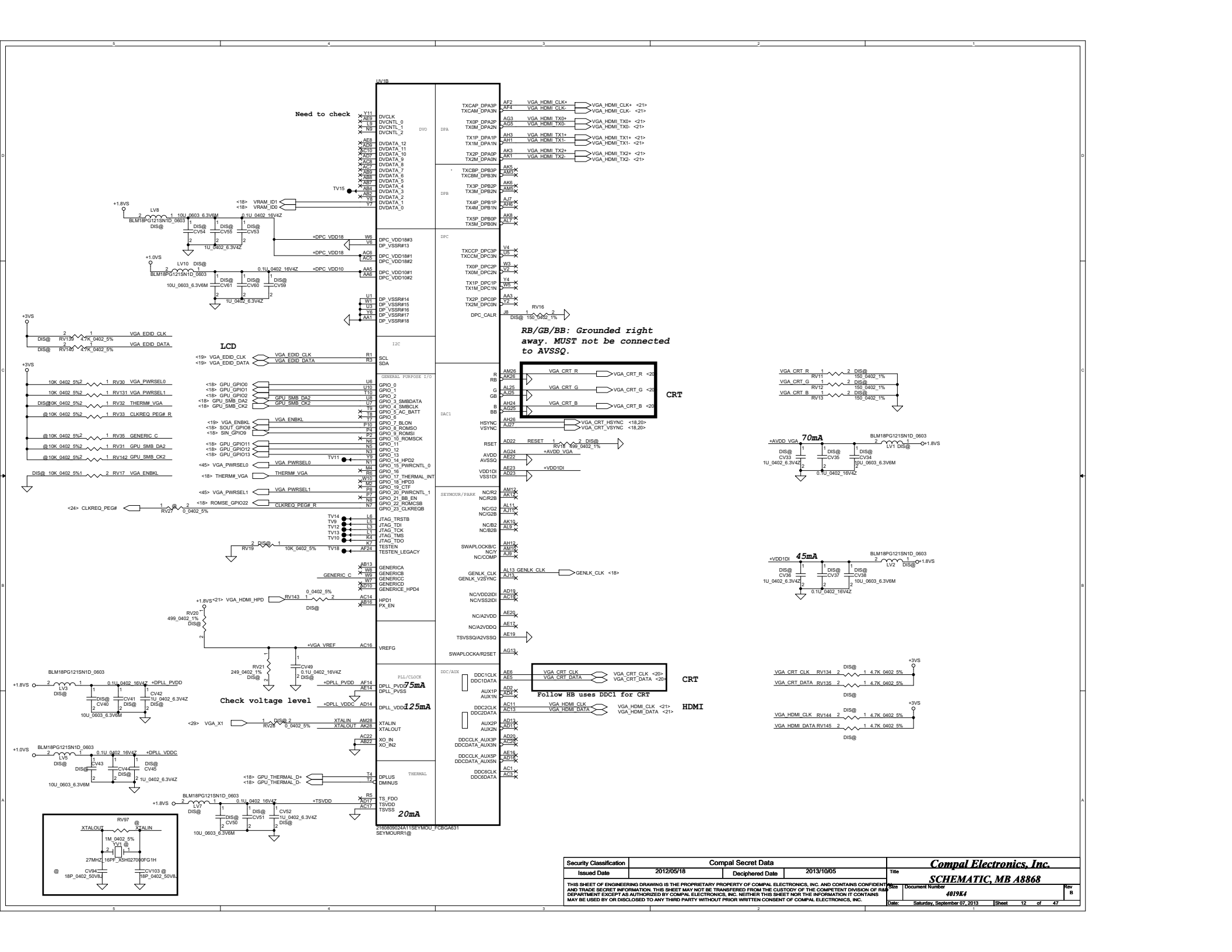

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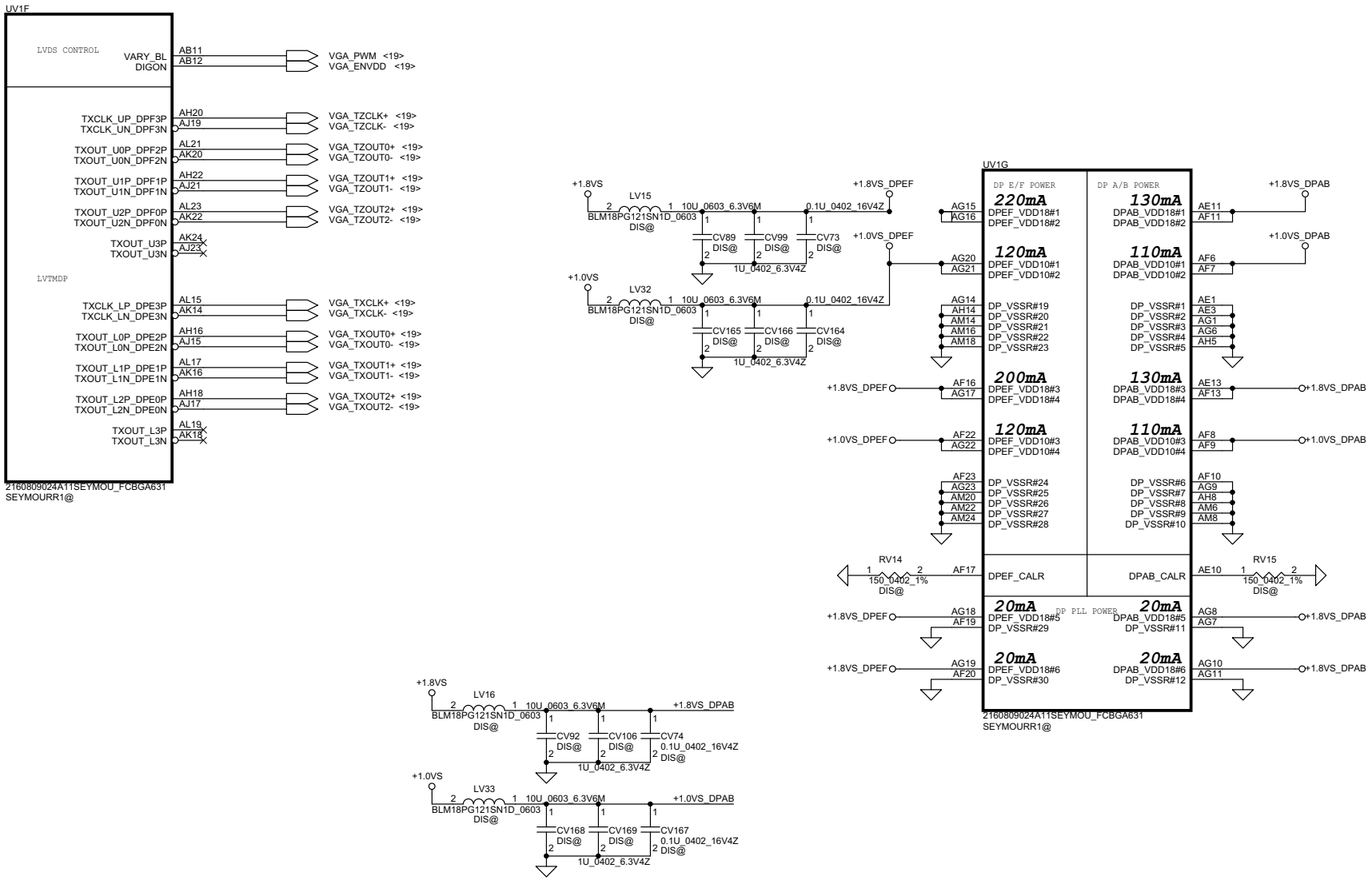

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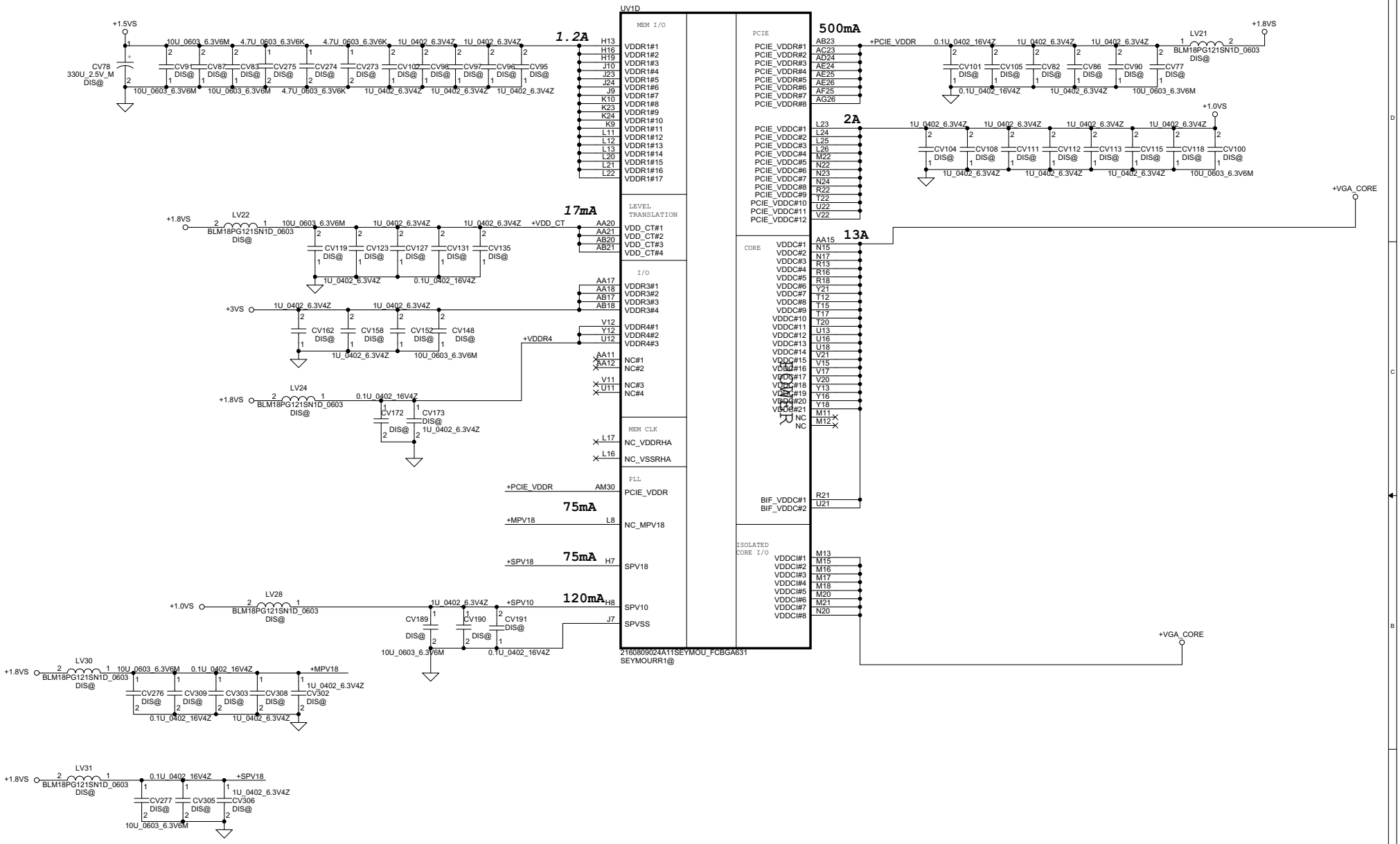

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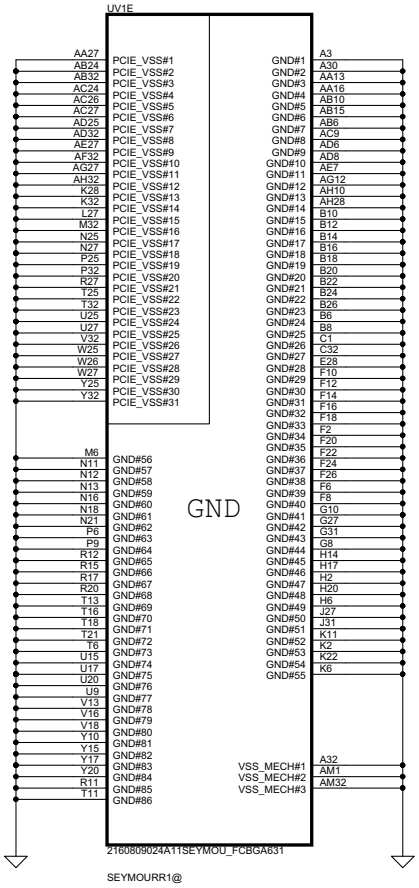

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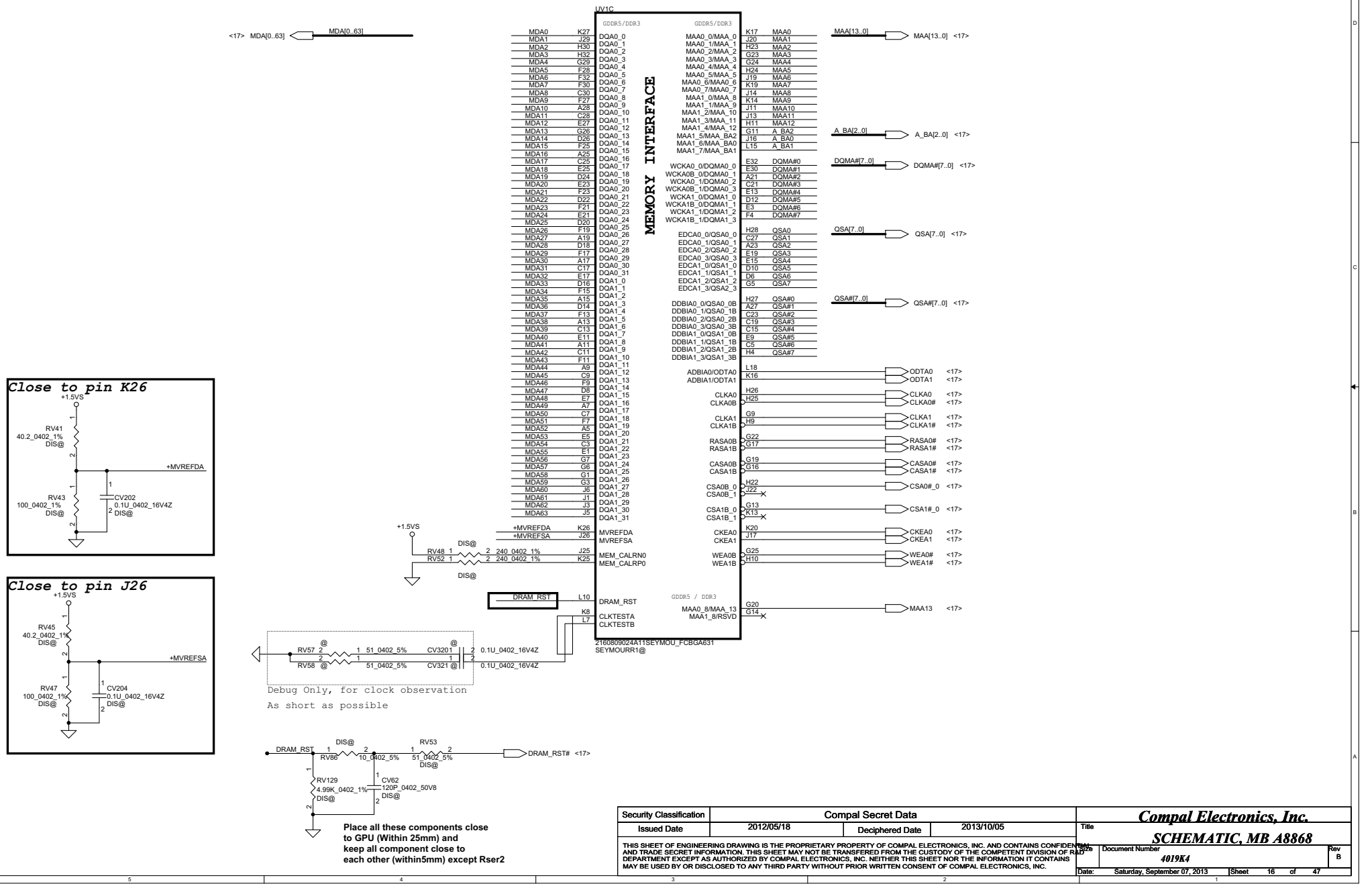

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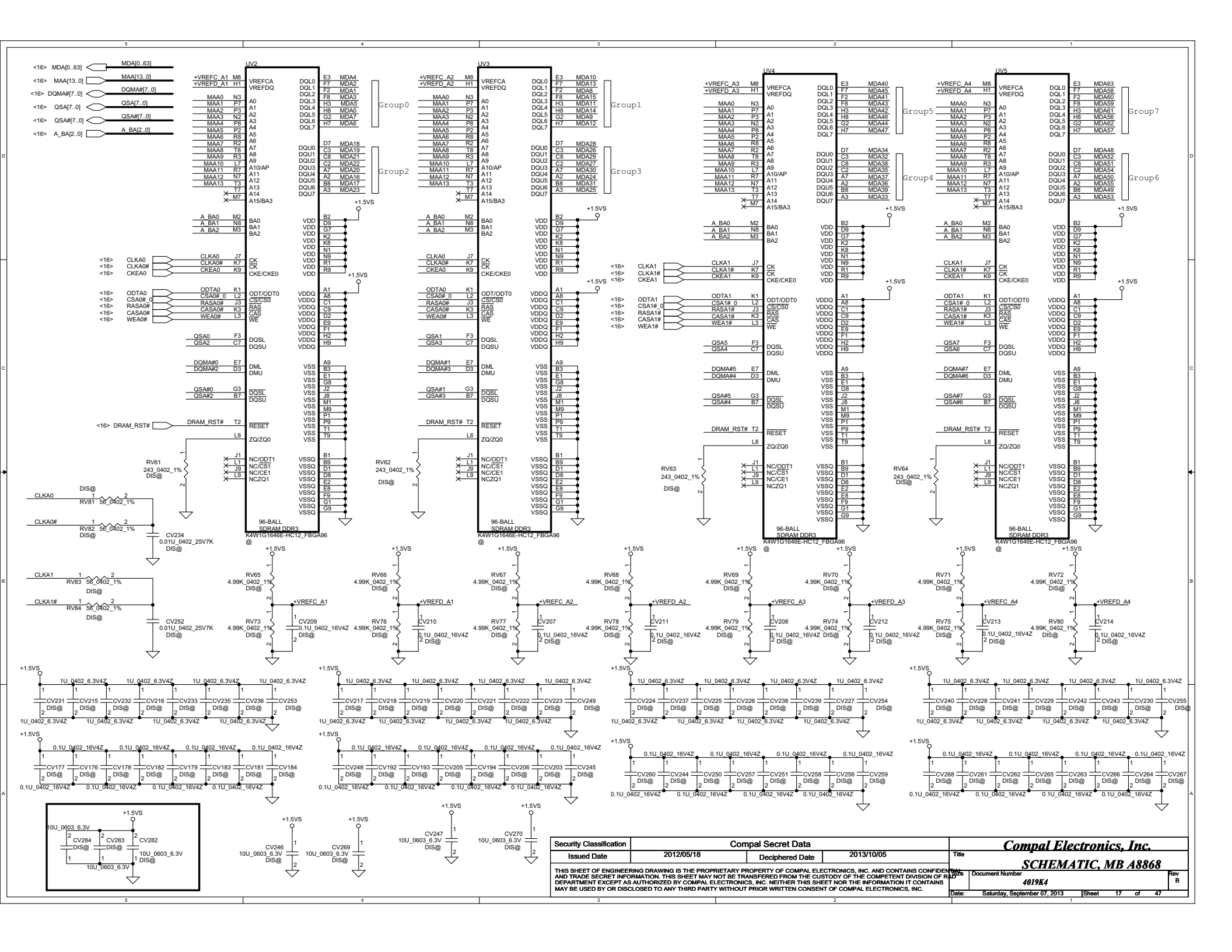
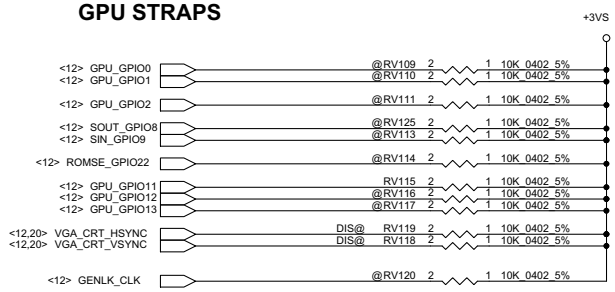
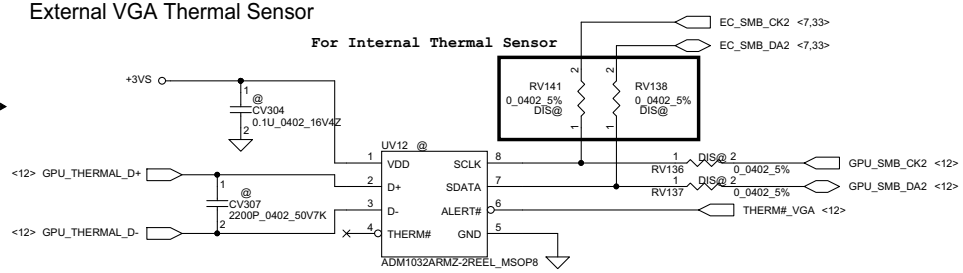


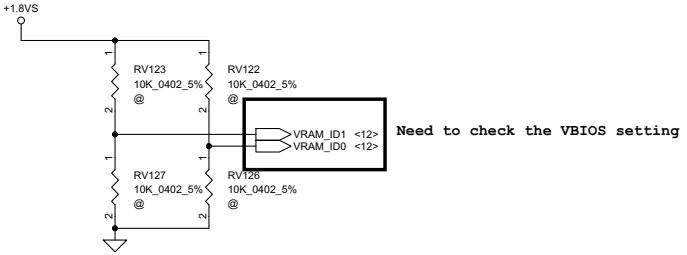
GPU STRAPS



GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0		GPIO22 = 1 (BIOS_ROM_EN = 1
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	*1 0 0*
0 0 1	256MB	*(M25P05A)*
0 1 0	64MB	

External VGA Thermal Sensor





Need to check the VBIOS setting

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 5.0 GT/s capability will be controlled by software
RESERVED	GPIO_8_ROMSO	SOUT_GPIO8	RESERVED	0
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (Internal pulldown)
VGA_DIS	GPIO_9_ROMSI	SIN_GPIO9	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
CONFIG(2:0)	GPIO[13:11]	GPU_GPIO11 GPU_GPIO12 GPU_GPIO13	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1 (256M)
RESERVED	GENLK_CLK	GENLK_CLK		0
AUD[1] AUD[0]	HSYNC VSYNC	VGA_CRT_HSYNC VGA_CRT_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	0 0

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 1,0
VRAM_ID[1:0]	DVDATA (1,0)	Seymour-S3	512M 64Mx16 (x4)	SAM K4W1G1646G-BC11	SA00004GS00	1 0
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC11	SA000047Q00	1 1

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UMA

<7> UMA_TXOUT0+ — R309 1 UMA@ 2 0_0402_5% — LCD_TXOUT0+
<7> UMA_TXOUT0- — R289 1 UMA@ 2 0_0402_5% — LCD_TXOUT0-
<7> UMA_TXOUT1+ — R293 1 UMA@ 2 0_0402_5% — LCD_TXOUT1+
<7> UMA_TXOUT1- — R291 1 UMA@ 2 0_0402_5% — LCD_TXOUT1-
<7> UMA_TXOUT2+ — R305 1 UMA@ 2 0_0402_5% — LCD_TXOUT2+
<7> UMA_TXOUT2- — R287 1 UMA@ 2 0_0402_5% — LCD_TXOUT2-
<7> UMA_TXCLK+ — R304 1 UMA@ 2 0_0402_5% — LCD_TXCLK+
<7> UMA_TXCLK- — R303 1 UMA@ 2 0_0402_5% — LCD_TXCLK-
<7> UMA_EDID_CLK — R308 1 UMA@ 2 0_0402_5% — LCD_EDID_CLK
<7> UMA_EDID_DATA — R307 1 UMA@ 2 0_0402_5% — LCD_EDID_DATA

<7> UMA_ENVDD — R358 1 UMA@ 2 0_0402_5% — LCD_ENVDD
<7> UMA_ENBKL — R359 1 UMA@ 2 0_0402_5% — EC_ENBKL — EC_ENBKL <33>

DISCRETE

<13> VGA_TXOUT0+ — R503 1 DIS@ 2 0_0402_5% — LCD_TXOUT0+
<13> VGA_TXOUT0- — R263 1 DIS@ 2 0_0402_5% — LCD_TXOUT0-
<13> VGA_TXOUT1+ — R265 1 DIS@ 2 0_0402_5% — LCD_TXOUT1+
<13> VGA_TXOUT1- — R264 1 DIS@ 2 0_0402_5% — LCD_TXOUT1-
<13> VGA_TXOUT2+ — R298 1 DIS@ 2 0_0402_5% — LCD_TXOUT2+
<13> VGA_TXOUT2- — R504 1 DIS@ 2 0_0402_5% — LCD_TXOUT2-
<13> VGA_TXCLK+ — R297 1 DIS@ 2 0_0402_5% — LCD_TXCLK+
<13> VGA_TXCLK- — R296 1 DIS@ 2 0_0402_5% — LCD_TXCLK-
<12> VGA_EDID_CLK — R300 1 DIS@ 2 0_0402_5% — LCD_EDID_CLK
<12> VGA_EDID_DATA — R299 1 DIS@ 2 0_0402_5% — LCD_EDID_DATA

<13> VGA_ENVDD — R350 1 DIS@ 2 0_0402_5% — LCD_ENVDD
<12> VGA_ENBKL — R357 1 DIS@ 2 0_0402_5% — EC_ENBKL

Close to LVDS Connector

<13> VGA_TZOUT0+ — R500 1 DIS@ 2 0_0402_5% — LCD_TZOUT0+
<13> VGA_TZOUT0- — R506 1 DIS@ 2 0_0402_5% — LCD_TZOUT0-
<13> VGA_TZOUT1+ — R507 1 DIS@ 2 0_0402_5% — LCD_TZOUT1+
<13> VGA_TZOUT1- — R508 1 DIS@ 2 0_0402_5% — LCD_TZOUT1-
<13> VGA_TZOUT2+ — R509 1 DIS@ 2 0_0402_5% — LCD_TZOUT2+
<13> VGA_TZOUT2- — R512 1 DIS@ 2 0_0402_5% — LCD_TZOUT2-
<13> VGA_TZCLK+ — R513 1 DIS@ 2 0_0402_5% — LCD_TZCLK+
<13> VGA_TZCLK- — R514 1 DIS@ 2 0_0402_5% — LCD_TZCLK-

4/23 Change R388 +3VS to +5VS

W=20mils

+5VS — R388 1 CAM@ 2 0_0603_5% — +5VS_LVDS_CAM — C257 1 2 CAM@ 0.1U_0402_10V7K

4/23 Change R388 +3VS_LVDS_CAM to +5VS_LVDS_CAM

JLVDS @

1,2	USB20_N5_R	
3,4	USB20_P5_R	
5,6	INT_MIC_CLK	INT_MIC_CLK <31>
7,8	INT_MIC_DATA	INT_MIC_DATA <31>
9,10	+3VS	
11,12	LCD_EDID_CLK	
13,14	LCD_EDID_DATA	
15,16	LCD_TXOUT0-	
17,18	LCD_TXOUT0+	
19,20	LCD_TXOUT1-	
21,22	LCD_TXOUT1+	
23,24	LCD_TXOUT2-	
25,26	LCD_TXOUT2+	
27,28	LCD_TXCLK-	
29,30	LCD_TXCLK+	
31,32	LED_PWM	
33,34	BKOFF#_R	
35,36	GND1,GND2,GND3,GND4,GND5,GND6	

D84 AZ5125-02S.R7G_SOT23-3 @ — INT_MIC_CLK <31>, INT_MIC_DATA <31>

2A +LCD_VDD — C252 0.1U_0402_10V7K — C235 4.7U_0805_10V4Z

For RF @ — C256 47P_0402_50V8J

+LCD_INV — For RF @ — C258 47P_0402_50V8J

D85 AZ5125-02S.R7G_SOT23-3 @

STARC_107K30-000001-G2

1.5A +LCD_INV — C270 47P_0402_50V8J @ For RF

JLVDS1 — ACES_87036-1001-CP @

GND,GND	
10,9	LCD_TZOUT0-, LCD_TZOUT0+
8,7	LCD_TZOUT1-, LCD_TZOUT1+
6,5	LCD_TZOUT2-, LCD_TZOUT2+
4,3	LCD_TZCLK-, LCD_TZCLK+
2,1	

4/23 Change R117 +3VS to +3VALW for LVDS power down sequence

+LCD_VDD — R110 100_0805_5% — +3VALW — R117 100K_0402_5%

Q1A 2N7002KDWH_SOT363-6 — +3VS — W=80mils — C265 0.047U_0402_25V7K — R133 2LCDPWR_GATE 68K_0402_5% — Q17 AO3413_SOT23 — C261 4700P_0402_25V7K — +LCD_VDD W=80mils — C260 0.1U_0402_10V7K

LCD_ENVDD — Q1B 2N7002KDWH_SOT363-6 — R116 100K_0402_5%

4/23 Change R110,R133,C265,C261 for LVDS power sequence

USB20_N5_R — R78 CAM@0_0402_5% — L55 @ — USB20_N5 <24>
USB20_P5_R — WCM-2012-900T_0805 — USB20_P5 <24>
R104CAM@0_0402_5%

Reserve for EMI request

R73 300_0402_5% @ — C300 10P_0402_50V8J @

Reserved for EHCI CRC errors

LED_PWM — RB751V40_SC76-2 D17 — 0_0402_5% DIS@ R333 — VGA_PWM <13>
R234 47K_0402_5%
0_0402_5% UMA@ R332 — UMA_PWM <7>

BKOFF#_R — RB751V40_SC76-2 D15 — BKOFF# <33>
R122 10K_0402_5%

Reserve for LVDS panel

1.5A +LCD_INV — L16 FBMA-L11-201209-221LMA30T_0805 — B+
C262 68P_0402_50V8J — C264 0.1U_0402_25V6

For EMI

B+ — C251 @, C281 @, C489 @, C490 @ — 0.1U_0402_25V6

Security Classification	Compal Secret Data		
Issued Date	2012/05/18	Deciphered Date	2013/10/05

Compal Electronics, Inc.

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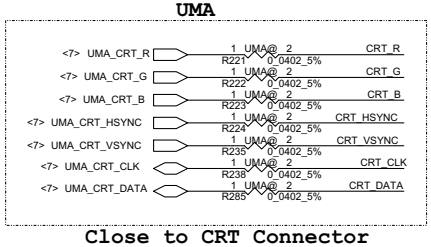
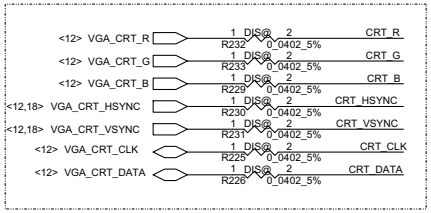
CRT CONNECTOR

UMA



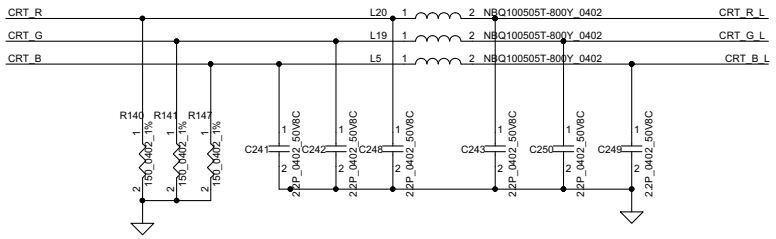
Close to CRT Connector

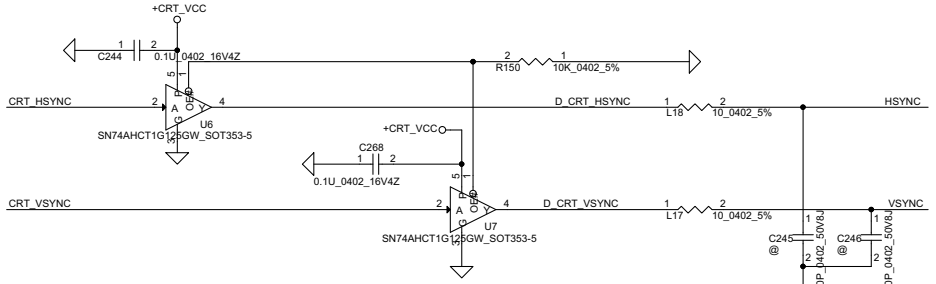
DISCRETE

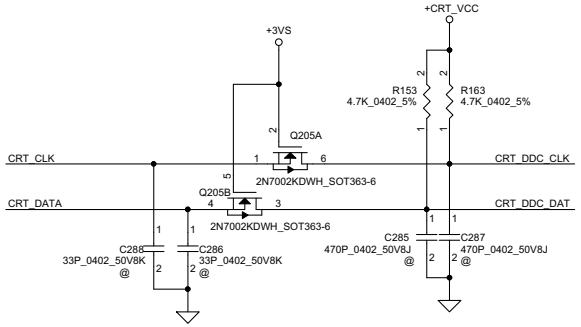


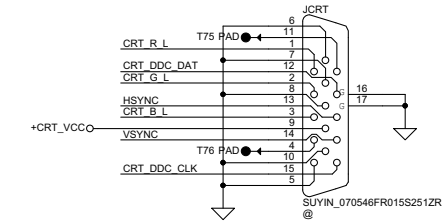
Close to CRT Connector

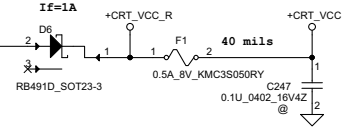
Remove D3~D5 on DVT

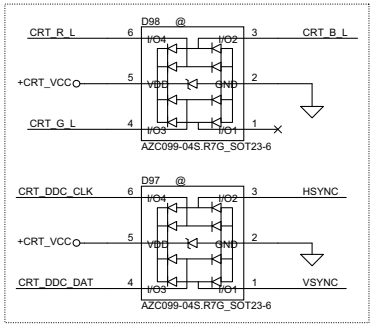












Reserve ESD for CRT connector on DVT

<Schematic Path> Security Classification	Compal Secret Data		
Issued Date	2012/05/18	Deciphered Date	2013/10/05

Compal Electronics, Inc.			
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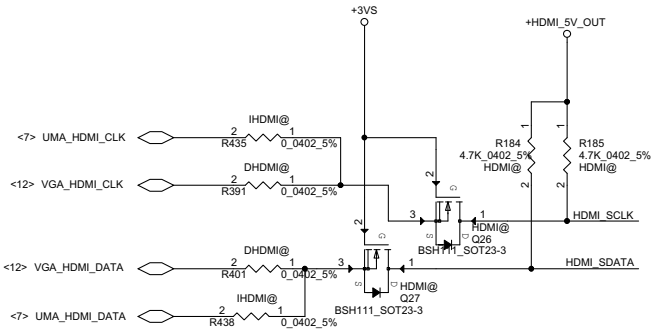
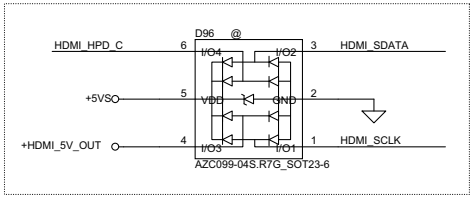


DISCRETE

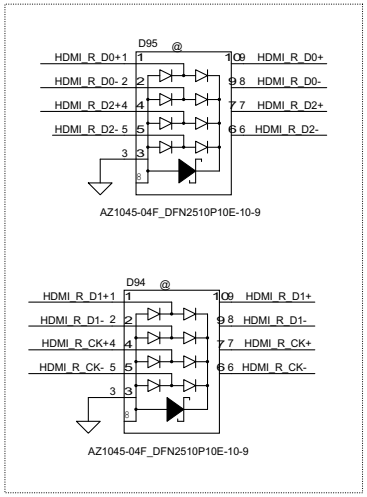
<12> VGA_HDMI_CLK+	CV296	1	2	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXC+
<12> VGA_HDMI_CLK-	CV293	1	2	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXC-
<12> VGA_HDMI_TX0+	CV294	1	2	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD0+
<12> VGA_HDMI_TX0-	CV297	1	2	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD0-
<12> VGA_HDMI_TX1+	CV299	1	2	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD1+
<12> VGA_HDMI_TX1-	CV298	1	2	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD1-
<12> VGA_HDMI_TX2+	CV295	1	2	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD2+
<12> VGA_HDMI_TX2-	CV300	1	2	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD2-

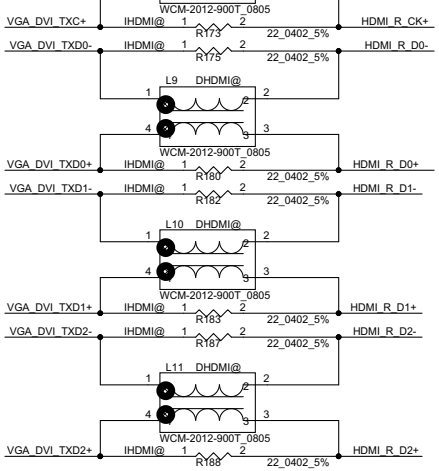
UMA

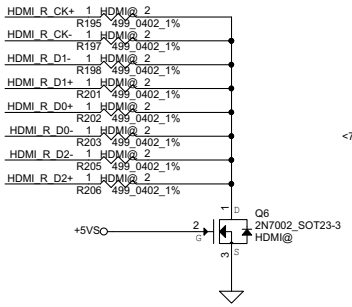
<7> UMA_HDMI_TXC+	C838	1	2	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXC+
<7> UMA_HDMI_TXC-	C837	1	2	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXC-
<7> UMA_HDMI_TX0+	C843	1	2	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD0+
<7> UMA_HDMI_TX0-	C844	1	2	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD0-
<7> UMA_HDMI_TX1+	C841	1	2	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD1+
<7> UMA_HDMI_TX1-	C842	1	2	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD1-
<7> UMA_HDMI_TX2+	C839	1	2	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD2+
<7> UMA_HDMI_TX2-	C840	1	2	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD2-

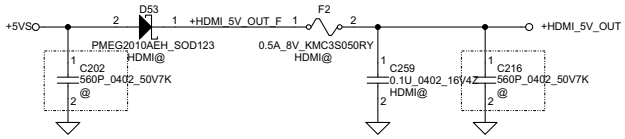


Reserve ESD for HDMI conn. on DVT



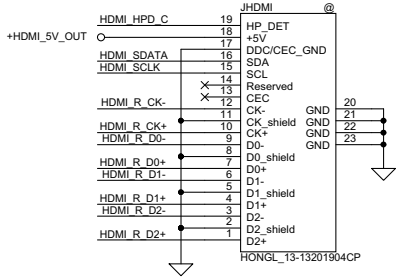


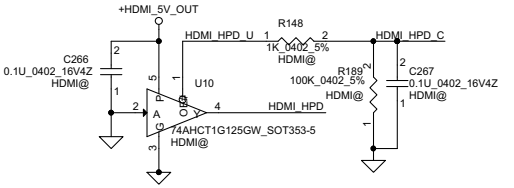


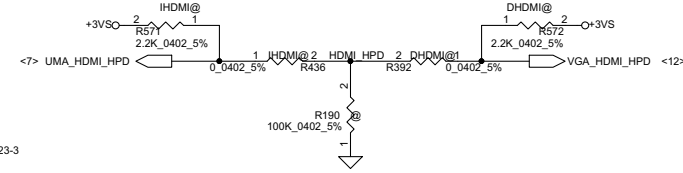


4/23 Add C202 and C216 for EMI request

HDMI Connector







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Compal Electronics, Inc.

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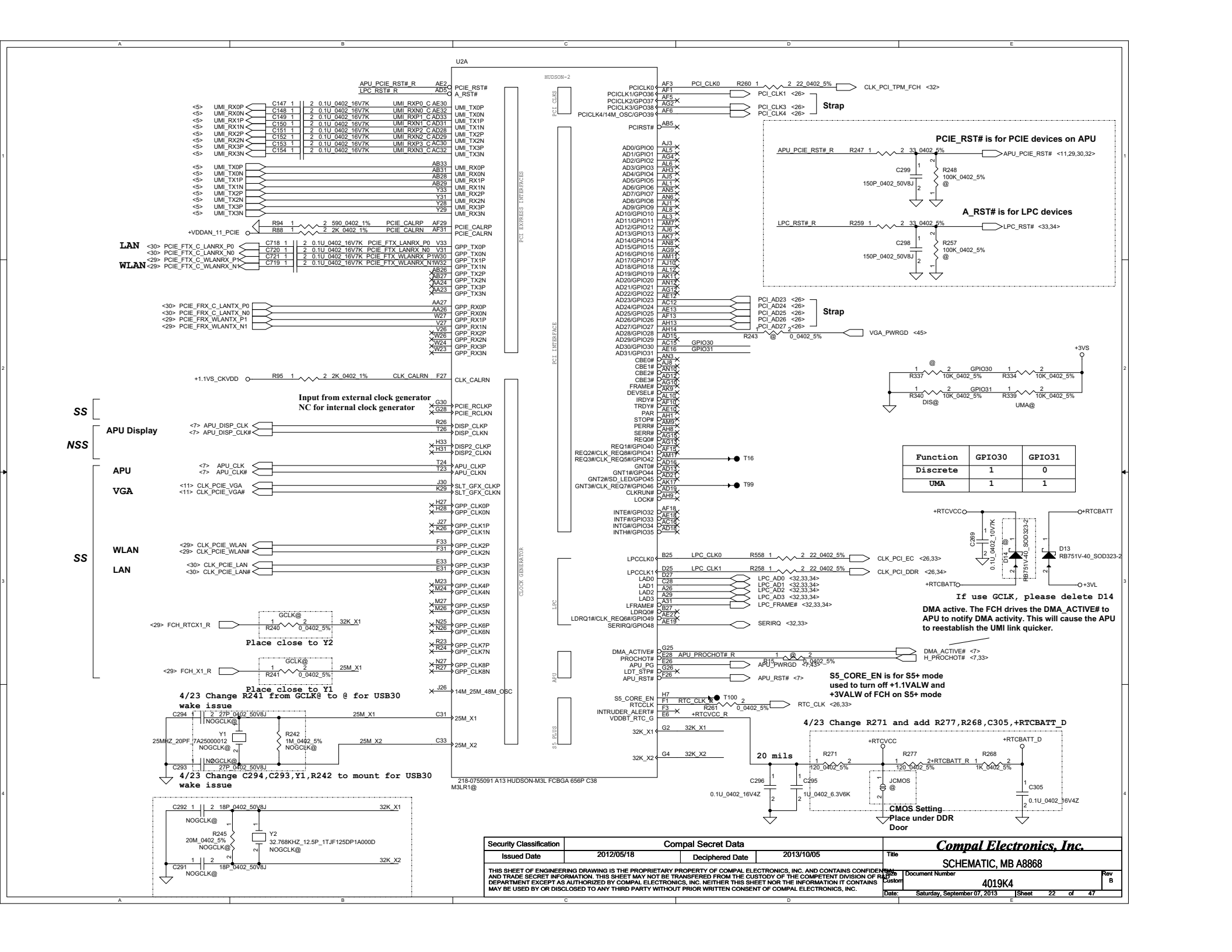

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HDMI_EN# (Internal 8.2K PU)

HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU

If an SPI ROM is shared between FCH and the Embedded Controller, a 10-k pull-up resistor to +3.3V_S5 is installed

Check

+3VALW_FCH

FCH_SPI_CS1# R115 @ 10K_0402_5%

from QMLE4

4MB SPI ROM & Non-shared ROM

SA00003K800

U13 W25Q32BVSSIG_SO8

FCH_SPI_CS1# FCH_SPI_MISO FCH_SPI_WP# FCH_SPI_HOLD# FCH_SPI_CLK_R FCH_SPI_MOSI

+3VALW_FCH C498 0.1U_0402_16V4Z

R112 2FCH_SPI_WP# 10K_0402_5%

R108 2FCH_SPI_HOLD# 10K_0402_5%

R111 33_0402_5% @

C160 22P_0402_50V8J @

Socket: SP07000F500/SP07000H900

HDD

ODD

<27> SATA_FTX_DRX_P0 AK19 SATA_TX0P

<27> SATA_FTX_DRX_N0 AM19 SATA_TX0N

<27> SATA_FRX_C_DTX_N0 AL20 SATA_RX0N

<27> SATA_FRX_C_DTX_P0 AN20 SATA_RX0P

<27> SATA_FTX_DRX_P1 AN22 SATA_TX1P

<27> SATA_FTX_DRX_N1 AL22 SATA_TX1N

<27> SATA_FRX_C_DTX_N1 AH20 SATA_RX1N

<27> SATA_FRX_C_DTX_P1 AJ20 SATA_RX1P

AJ22 SATA_TX2P

AH22 SATA_TX2N

AM23 SATA_RX2N

AK23 SATA_RX2P

AH24 SATA_TX3P

AJ24 SATA_TX3N

AN24 SATA_RX3N

AL24 SATA_RX3P

AL26 SATA_TX4P

AN26 SATA_TX4N

AJ26 SATA_RX4N

AH26 SATA_RX4P

AN29 SATA_TX5P

AL28 SATA_TX5N

AK27 SATA_RX5N

AM27 SATA_RX5P

AL29 NC6

AN31 NC7

AL31 NC8

AL33 NC9

AH33 NC10

AH31 NC11

AJ33 NC12

AJ31 NC13

FCH-M3L NC pin

To avoid LED flashing

+5VS R448 10K_0402_5% SATA_LED#

R454 20K_0402_5%

1K_0402_1% R128 SATA_CALRP AF28 SATA_CALRP

+AVDD_SATA 931_0402_1% R130 SATA_CALRN AF27 SATA_CALRN

<35> SATA_LED# SATA_LED# AD22 SATA_ACT#/GPIO67

AF21 SATA_X1

AG21 SATA_X2

T48 AH16 FANOUT0/GPIO52

<36> ODD_PWR AM15 FANOUT1/GPIO53

AJ16 FANOUT2/GPIO54

AK15 FANIN0/GPIO56

AN16 FANIN1/GPIO57

AL16 FANIN2/GPIO58

R151 10K_0402_5% K6 TEMPIN0/GPIO171

R146 10K_0402_5% K5 TEMPIN1/GPIO172

R149 10K_0402_5% K3 TEMPIN2/GPIO173

R152 10K_0402_5% M6 TEMPIN3/TALERT#/GPIO174

12/22 Follow the last Compal CRB board

U2B HUDSON-2

SD_CLK/SCLK_2/GPIO73 AL4 @ R455 1K_0402_1%

SD_CMD/SLOAD_2/GPIO74 AN4

SD_CD/GPIO75 AJ12

SD_WP/GPIO76 AH12

SD_DATA0/SDATI_2/GPIO77 AK13

SD_DATA1/SDATO_2/GPIO78 AM13

SD_DATA2/GPIO79 AH13

SD_DATA3/GPIO80 AJ14

SD CARD

GBE_COL AC4

GBE_CRS AD3

GBE_MDCK AD9

GBE_MDIO W10

GBE_RXCLK AB8

GBE_RXD3 AH7

GBE_RXD2 AF7

GBE_RXD1 AE7

GBE_RXD0 AD7

GBE_RXCTL/RXDV AG8

GBE_RXERR AD1

GBE_TXCLK AB7

GBE_TXD3 AF3

GBE_TXD2 AG6

GBE_TXD1 AE8

GBE_TXD0 AD8

GBE_TXCTL/TXEN AB9

GBE_PHY_PD AC2

GBE_PHY_RST# AA7

GBE_PHY_INTR W9 GBE_PHY_INTR

GBE LAN

SPI_DI/GPIO164 V6 FCH_SPI_MISO

SPI_DO/GPIO163 V5 FCH_SPI_MOSI

SPI_CLK/GPIO162 V3 FCH_SPI_CLK

SPI_CS1#/GPIO165 T6 FCH_SPI_CS1#

ROM_RST#/SPI_WP#/GPIO161 V1 FCH_SPI_WP#

SPI ROM

SERIAL ATA

VGA_RED L30

VGA_GREEN L32

VGA_BLUE M29

VGA_HSYNC/GPO68 M28

VGA_VSYNC/GPO69 N30

VGA_DDC_SDA/GPO70 M33

VGA_DDC_SCL/GPO71 N32

VGA_DAC_RSET K31

AUX_VGA_CH_P V28

AUX_VGA_CH_N V29

AUXCAL U28

ML_VGA_L0P T31

ML_VGA_L0N T33

ML_VGA_L1P T29

ML_VGA_L1N T28

ML_VGA_L2P R32

ML_VGA_L2N R30

ML_VGA_L3P P29

ML_VGA_L3N P28

ML_VGA_HPD/GPIO229 C29

VGA DAC

VGA MULTILINK

FCH-M3L NC pin

FCH_SPI_CLK_1 R113 0_0402_5% FCH_SPI_CLK_R

C161 22P_0402_50V8J @

5/17 Add R113 and reserve C161 for EMI request

+3VALW_FCH

GBE_PHY_INTR R121 10K_0402_5%

+3VALW_FCH

<28> SLP_CHG# SLP_CHG# R126 @ 10K_0402_5%

HW MONITOR

VIN0/GPIO175 N2 R137 10K_0402_5%

VIN1/GPIO176 M3 R138 10K_0402_5%

VIN2/SDATI_1/GPIO177 L2 R145 10K_0402_5%

VIN3/SDATO_1/GPIO178 N4 R139 10K_0402_5%

VIN4/SLOAD_1/GPIO179 P1 R142 10K_0402_5%

VIN5/SCLK_1/GPIO180 P3 SLP_CHG#1 R143 10K_0402_5%

VIN6/GBE_STAT3/GPIO181 M1 R144 10K_0402_5%

VIN7/GBE_LED3/GPIO182 M5 RF148 10K_0402_5%

NC1 AG16

NC2 AH10

NC3 A28

NC4 G27

NC5 L4

Need to enable internal pull down to leave unconnected

218-0755091 A13 HUDSON-M3L FCBGA 656P C38

M3LR1@

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PCIE_RST2 : Reset PCIE device on Hudson 3

For FCH internal debug use (Internal 10K pull-down)

+3VALW_FCH
R179 1 @ 2 2.2K_0402_5% TEST0
R181 1 @ 2 2.2K_0402_5% TEST1
RF1831 @ 2 2.2K_0402_5% TEST2

SM Bus 0-->S0 PWR domain==> SO-DIMM, WLAN
SM Bus 1-->S5 PWR domain==> no use

R282 2 1 100K_0402_5% EC_RSMRST#
R324 1 @ 2 10K_0402_5% HDA_BITCLK
R325 1 @ 2 10K_0402_5% AZ_SDIN0_HD
R326 1 @ 2 10K_0402_5% AZ_SDIN1_HD
R327 1 @ 2 10K_0402_5% AZ_SDIN2_HD
R329 1 @ 2 10K_0402_5% AZ_SDIN3_HD

12/22 Reserve R326,R327,R329 but AMD have internal pull down

USB_OC1# is for left USB3.0 ports
USB_OC0# is for right USB2.0 ports

+3VALW_FCH

Internal Pull-up

R278 1 @ 2 10K_0402_5% H_THERMTRIP#
R272 1 @ 2 10K_0402_5% EC_LID_OUT#
R276 1 @ 2 10K_0402_5% FCH_PCIE_WAKE#
R318 1 @ 2 10K_0402_5% USB_OC0#
R319 1 @ 2 10K_0402_5% USB_OC1#
R288 1 @ 2 10K_0402_5% FCH_SCLK1
RF289 1 @ 2 10K_0402_5% FCH_SDATA1

12/22 SMBus Not Implemented use 10k pull up to +3VALW_PCH

+3VS

RF287 1 @ 2 2.2K_0402_5% FCH_SCLK0
RF291 1 @ 2 2.2K_0402_5% FCH_SDATA0
R292 1 @ 2 8.2K_0402_5% CLKREQ_WLAN#
R290 1 @ 2 8.2K_0402_5% CLKREQ_LAN#
R320 1 @ 2 10K_0402_5% WD_PWRGD

Place R425 and C363 close to FCH for ESD

+3VALW_FCH
R312 2 1 10K_0402_5% @
+3VS
R311 2 1 10K_0402_5%
+3VS
Q32A
ODD_DA# FCH 1 R425 2 0_0402_5% @ 2ODD_DA# Q
6
1
ODD_DA# <27>
C363 1 0.1U_0402_16V4Z 2 @
2N7002KDWH_SOT363-6

Q32B in page14

U2D

HUDSON-2

T17 AB6 PCIE_RST2#/PCI_PME#/GEVENT4#
<33> EC_LID_OUT# R2 RI#/GEVENT22#
<27> ODD_PLUGIN# ODD_PLUGIN# W7 SPI_CS3#/GBE_STAT1/GEVENT21#
<33> SLP_S3# T3 SLP_S3#
<33> SLP_S5# W2 SLP_S5#
<33> PBTN_OUT# J4 PWR_BTN#
<33> FCH_PWRGD N7 PWR_GOOD
TEST0 T9 TEST0
TEST1 T10 TEST1/TMS
TEST2 V9 TEST2
<33> GATEA20 AE22 GA20IN/GEVENT0#
<33> KB_RST# AG19 KBRST#/GEVENT1#
<33> EC_SCI# R9 LPC_PME#/GEVENT3#
<33> EC_SMI# C26 LPC_SMI#/GEVENT23#
T5 LPC_PD#/GEVENT5#
U4 SYS_RESET#/GEVENT19#
<30> FCH_PCIE_WAKE# FCH_PCIE_WAKE# K1 WAKE#/GEVENT8#
V7 IR_RX1/GEVENT20#
<7> H_THERMTRIP# H_THERMTRIP# R10 THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD AF19 WD_PWRGD
<33> EC_RSMRST# U2 RSMRST#
AG24 CLK_REQ4#/SATA_IS0#/GPIO64
<30> CLKREQ_LAN# AE23 CLK_REQ3#/SATA_IS1#/GPIO63
AE26 SMARTVOLT1/SATA_IS2#/GPIO50
AF22 CLK_REQ0#/SATA_IS3#/GPIO60
AH17 SATA_IS4#/FANOUT3/GPIO55
AG18 SATA_IS5#/FANIN3/GPIO59
<31> FCH_SPKR AF24 SPKR/GPIO66
<9,10,29> FCH_SCLK0 FCH_SCLK0 AD26 SCL0/GPIO43
<9,10,29> FCH_SDATA0 FCH_SDATA0 AD25 SDA0/GPIO47
FCH_SCLK1 T7 SCL1/GPIO227
FCH_SDATA1 R7 SDA1/GPIO228
<29> CLKREQ_WLAN# AG25 CLK_REQ2#/FANIN4/GPIO62
AG22 CLK_REQ1#/FANOUT4/GPIO61
J2 IR_LED#/LLB#/GPIO184
AG26 SMARTVOLT2/SHUTDOWN#/GPIO51
V8 DDR3_RST#/GEVENT7#/VGA_PD
<30> LAN_EN LAN_EN W8 GBE_LED0/GPIO183
Y6 SPI_HOLD#/GBE_LED1/GEVENT9#
V10 GBE_LED2/GEVENT10#
AA8 GBE_STAT0/GEVENT11#
<12> CLKREQ_PEG# CLKREQ_PEG# AF25 CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
M7 BLINK/USB_OC7#/GEVENT18#
R8 USB_OC6#/IR_TX1/GEVENT6#
T59 T1 USB_OC5#/IR_TX0/GEVENT17#
ODD_DA# FCH F6 USB_OC4#/IR_RX0/GEVENT16#
T58 F5 USB_OC3#/AC_PRES/TDO/GEVENT15#
T56 P5 USB_OC2#/TCK/GEVENT14#
<28> USB_OC1# USB_OC1# J7 USB_OC1#/TDI/GEVENT13#
<27> USB_OC0# USB_OC0# T8 USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
<31> AZ_BITCLK_HD R159 1 2 33_0402_5% HDA_BITCLK AB3 AZ_BITCLK
<31> AZ_SDOUT_HD R160 1 2 33_0402_5% HDA_SDOUT AB1 AZ_SDOUT
<31> AZ_SDIN0_HD AZ_SDIN0_HD AA2 AZ_SDIN0/GPIO167
AZ_SDIN1_HD Y5 AZ_SDIN1/GPIO168
AZ_SDIN2_HD Y3 AZ_SDIN2/GPIO169
AZ_SDIN3_HD Y1 AZ_SDIN3/GPIO170
<31> AZ_SYNC_HD R161 1 2 33_0402_5% HDA_SYNC AD6 AZ_SYNC
<31> AZ_RST_HD# R162 1 2 33_0402_5% HDA_RST# AE4 AZ_RST#
T61 K19 PS2_DAT/SDA4/GPIO187
T19 J19 PS2_CLK/CEC/SCL4/GPIO188
J21 SPI_CS2#/GBE_STAT2/GPIO166
D21 PS2KB_DAT/GPIO189
(GPIO189/GPIO190) QMLE4: Detect UMA/PX C20 PS2KB_CLK/GPIO190
(GPIO191) QMLE4: PXS_RST# Y23 PS2M_DAT/GPIO191
(GPIO192) QMLE4: PXS_PWREN C22 PS2M_CLK/GPIO192
F21 KSO_0/GPIO209
E20 KSO_1/GPIO210
F20 KSO_2/GPIO211
A22 KSO_3/GPIO212
E18 KSO_4/GPIO213
A20 KSO_5/GPIO214
J18 KSO_6/GPIO215
H18 KSO_7/GPIO216
G18 KSO_8/GPIO217
B21 KSO_9/GPIO218
K18 KSO_10/GPIO219
D19 KSO_11/GPIO220
A18 KSO_12/GPIO221
C18 KSO_13/GPIO222
B19 KSO_14/GPIO223
B17 KSO_15/GPIO224
A24 KSO_16/GPIO225
D17 KSO_17/GPIO226

ACPI / WAKE UP EVENTS | USB 1.1 | GPIO | USB 2.0 | USB OC | HD AUDIO | USB 3.0 | EMBEDDED CTRL

218-0755091 A13 HUDSON-M3L FCBGA 656P C38

M3LR1@

USB MISC

USBCLK/14M_25M_48M_OSC G8
USB_RCOMP B9 USB_RCOMP R154 1 2 11.8K_0402_1%

USB_FSD1P/GPIO186 H1
USB_FSD1N H3
USB_FSD0P/GPIO185 H6
USB_FSD0N H5
USB_HSD13P H10
USB_HSD13N G10
USB_HSD12P K10
USB_HSD12N J12

FCH-M3L NC pin

USB_HSD11P G12 USB20_P11 <28>
USB_HSD11N F12 USB20_N11 <28> **USB 3.0-Left2**
USB_HSD10P K12 USB20_P10 <28>
USB_HSD10N K13 USB20_N10 <28> **USB 3.0-Left1**

Root

USB_HSD9P B11
USB_HSD9N D11

FCH-M3L NC pin

USB_HSD8P E10 USB20_P8 <29>
USB_HSD8N F10 USB20_N8 <29> **WLAN (BT)**
USB_HSD7P C10 USB20_P7 <32>
USB_HSD7N A10 USB20_N7 <32> **Cardreader**

Root

USB_HSD6P H9
USB_HSD6N G9
USB_HSD5P A8 USB20_P5 <19>
USB_HSD5N C8 USB20_N5 <19> **Int. Camera**

FCH-M3L NC pin

USB_HSD4P F8
USB_HSD4N E8
USB_HSD3P C6
USB_HSD3N A6
USB_HSD2P C5
USB_HSD2N A5

Root

USB_HSD1P C1 USB20_P1 <27>
USB_HSD1N C3 USB20_N1 <27>
USB_HSD0P E1 USB20_P0 <27>
USB_HSD0N E3 USB20_N0 <27>

USBSS_CALRP C16 USBSS_CALRP R864 1 2 1K_0402_1%
USBSS_CALRN A16 USBSS_CALRN R865 1 2 1K_0402_1% +FCH_VDD_11_SSUSB_S

USB_SS_TX3P A14
USB_SS_TX3N C14
USB_SS_RX3P C12
USB_SS_RX3N A12
USB_SS_TX2P D15
USB_SS_TX2N B15
USB_SS_RX2P E14
USB_SS_RX2N F14

FCH-M3L NC pin

USB_SS_TX1P F15 USB30_TX1P USB30_TX1P <28>
USB_SS_TX1N G15 USB30_TX1N USB30_TX1N <28>
USB_SS_RX1P H13 USB30_RX1P USB30_RX1P <28>
USB_SS_RX1N G13 USB30_RX1N USB30_RX1N <28>
USB_SS_TX0P J16 USB30_TX0P USB30_TX0P <28>
USB_SS_TX0N H16 USB30_TX0N USB30_TX0N <28>
USB_SS_RX0P J15 USB30_RX0P USB30_RX0P <28>
USB_SS_RX0N K15 USB30_RX0N USB30_RX0N <28>

LP2

LP1

SCL2/GPIO193 H19 R165 1 2 10K_0402_5%
SDA2/GPIO194 G19 R167 1 2 10K_0402_5%
SCL3_LV/GPIO195 G22 R227 1 2 10K_0402_5%
SDA3_LV/GPIO196 G21 R228 1 2 10K_0402_5%
EC_PWM0/EC_TIMER0/GPIO197 E22
EC_PWM1/EC_TIMER1/GPIO198 H22
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 J22 EC_PWM2
EC_PWM3/EC_TIMER3/GPIO200 H21
EC_PWM2 <26> strap pin

KSI_0/GPIO201 K21
KSI_1/GPIO202 K22
KSI_2/GPIO203 F22
KSI_3/GPIO204 F24
KSI_4/GPIO205 E24
KSI_5/GPIO206 B23
KSI_6/GPIO207 C24
KSI_7/GPIO208 F18

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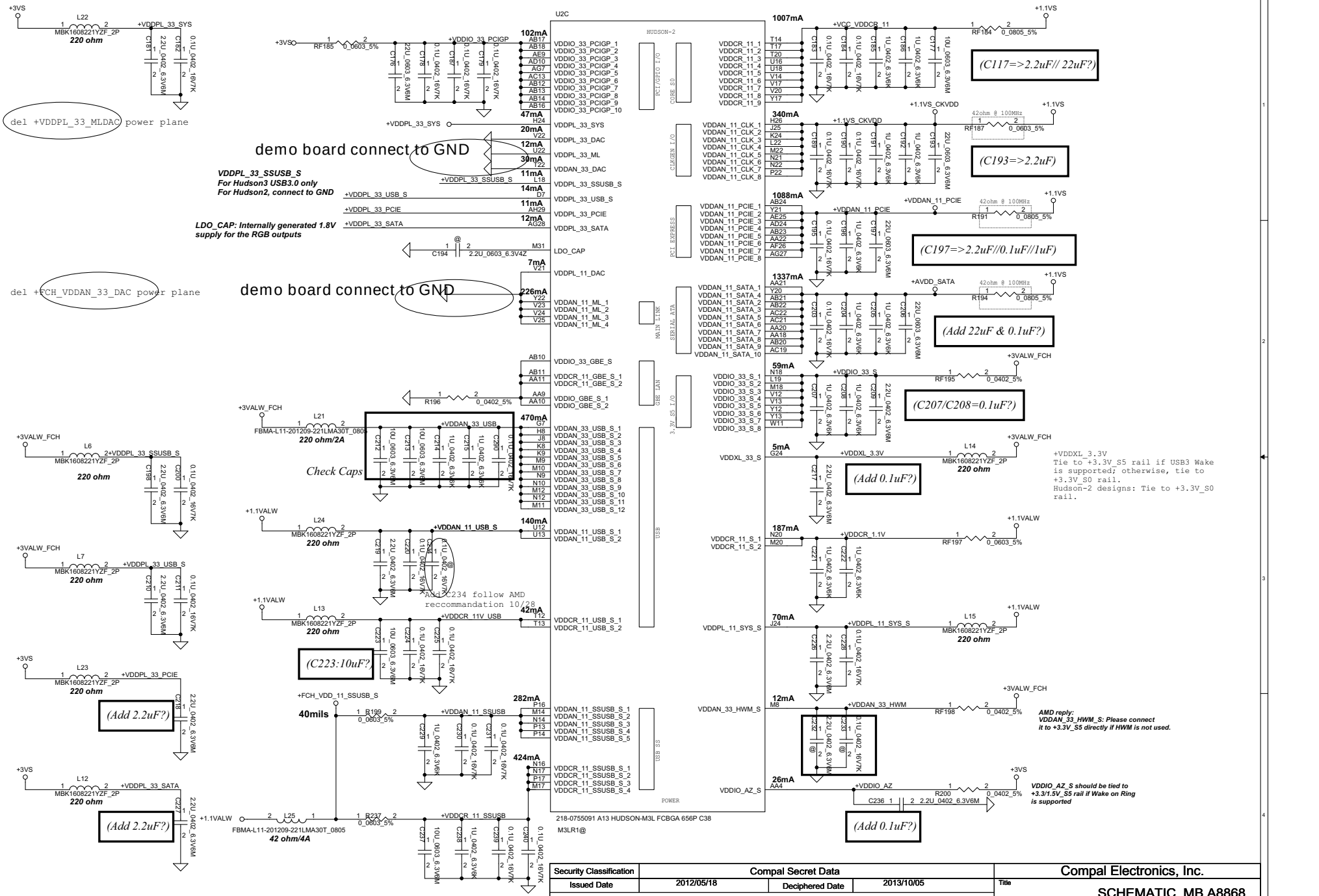
Date: Saturday, September 07, 2013 | Sheet 24 of 47



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Compal Electronics, Inc.

Title: SCHEMATIC, MB A8868

Size: Custom | Document Number: 4019K4 | Rev: B

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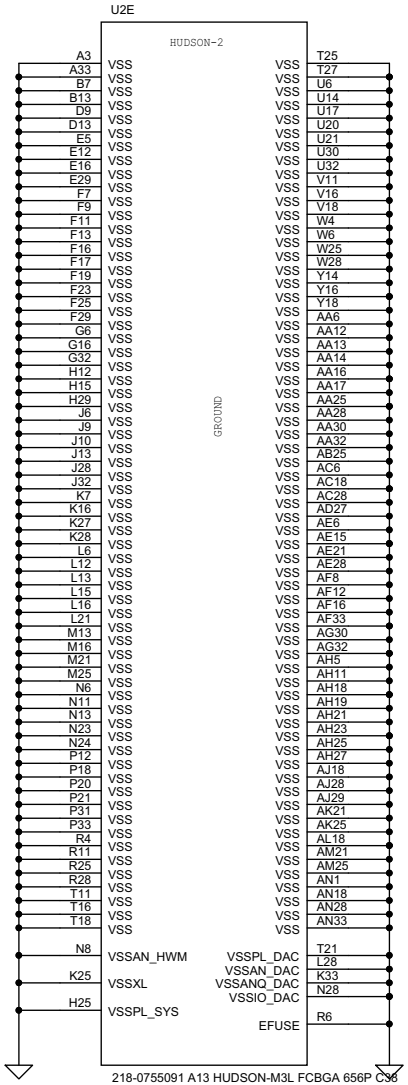


M3LR1@

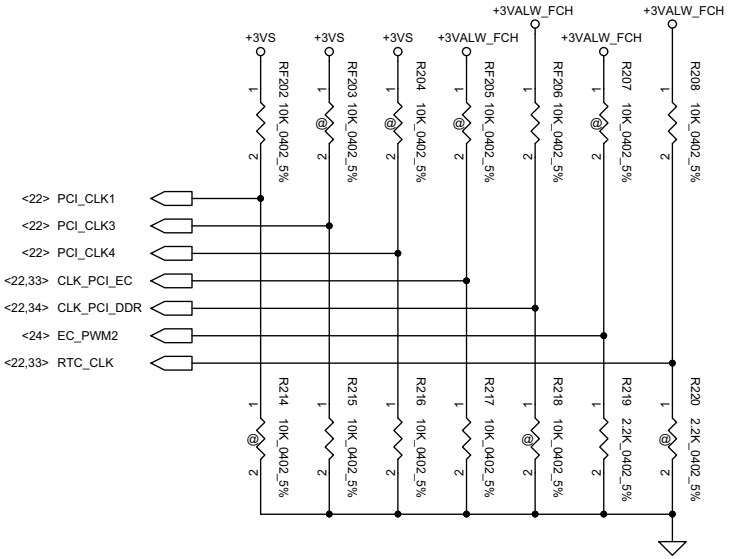
STRAP PINS

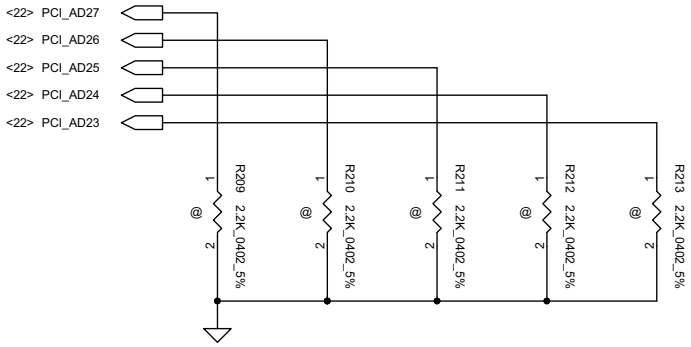
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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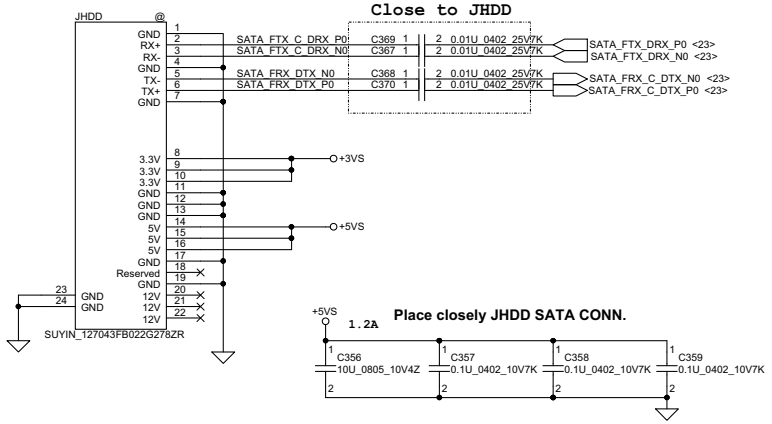
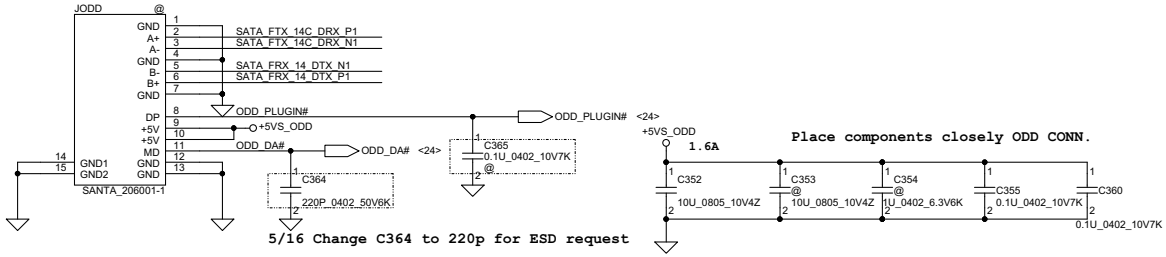
			Size: B; Document Number: 4019K4; Rev: B
			Date: Saturday, September 07, 2013; Sheet 26 of 47

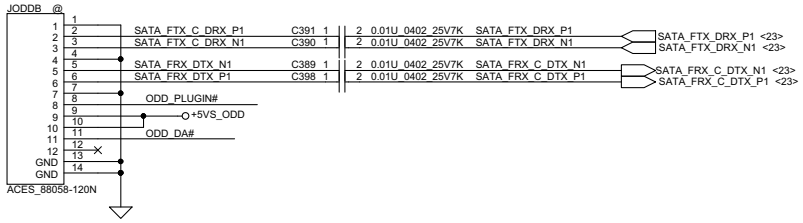
SATA HDD Conn.

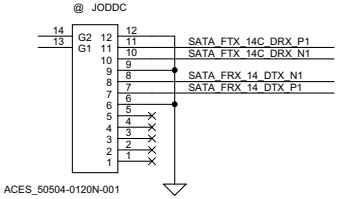


SATA ODD Conn (for 14")

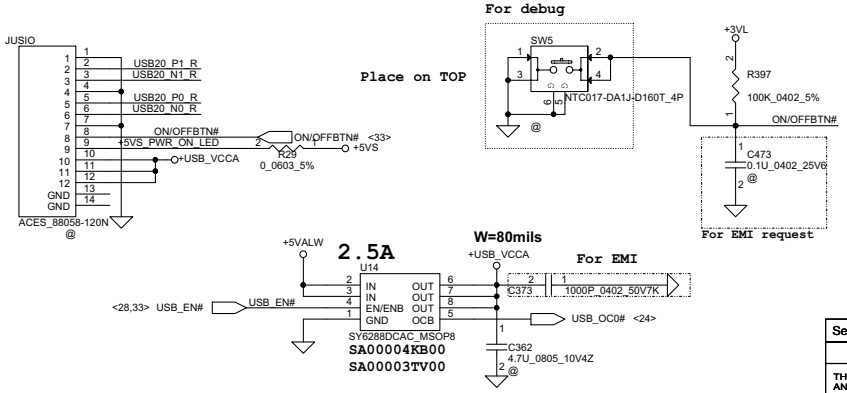


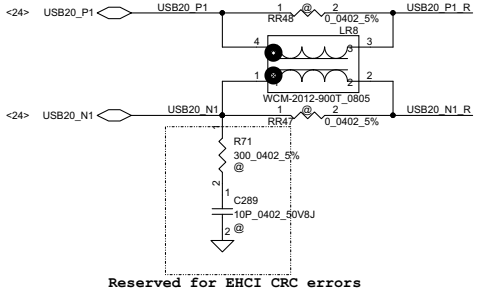
SATA ODD Conn (for 15")

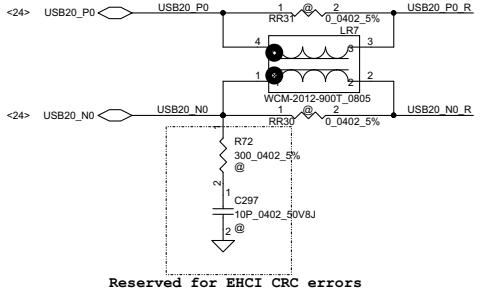




Power Button & RUSB connector







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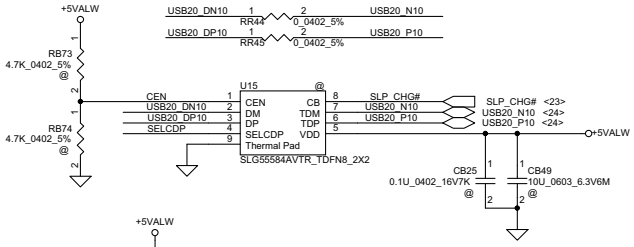
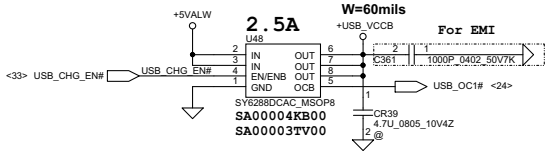
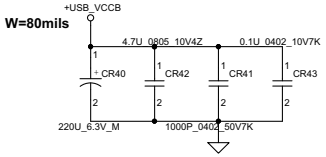
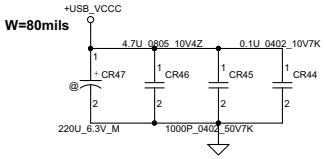
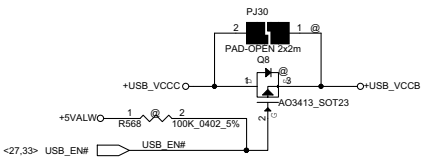
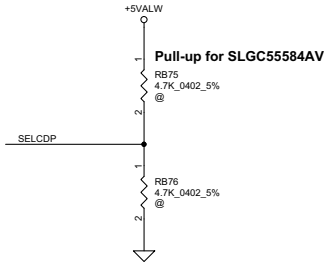




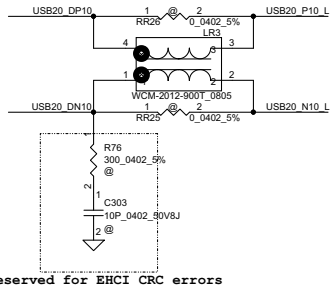




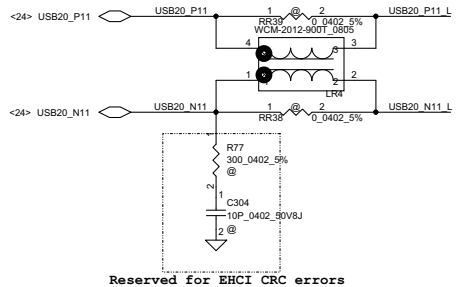




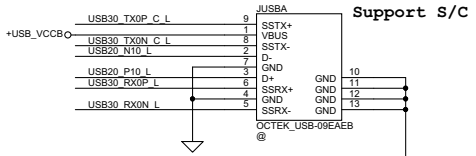
SLP_CHG#	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only

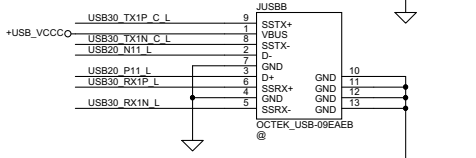


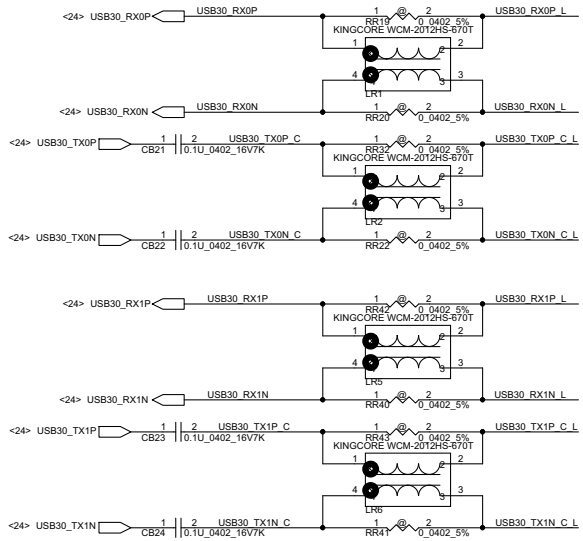
Reserved for EHCI CRC errors

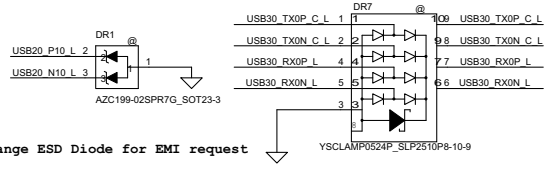


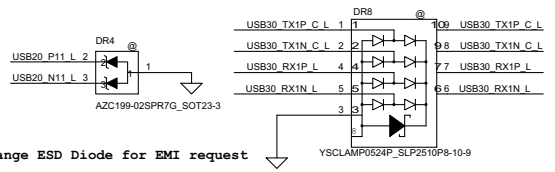
Reserved for EHCI CRC errors











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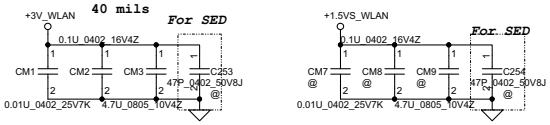
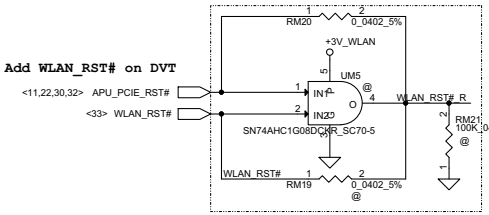
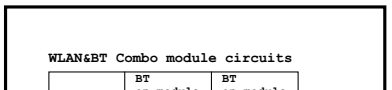
Slot 1 Half PCIe Mini Card-WLAN



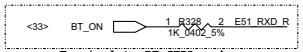


4/23 Add RM20 and change UM5,RM21 to @

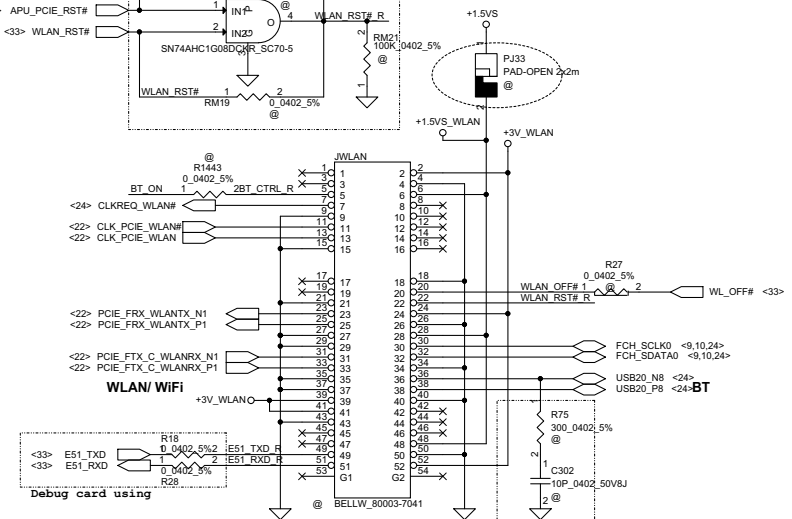


WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L



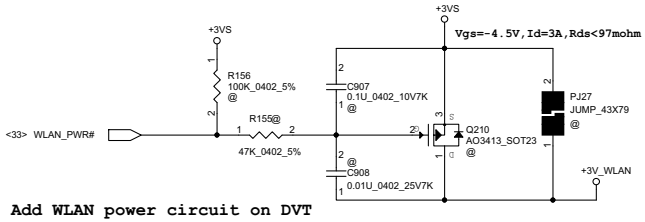
For isolate BT_CTRL and Compal Debug Card.



Change JWLAN symbol to SP07000TB00 on DVT

Reserved for EHCI CRC errors

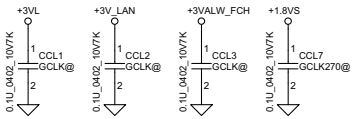
+3VALW TO +3V_WLAN

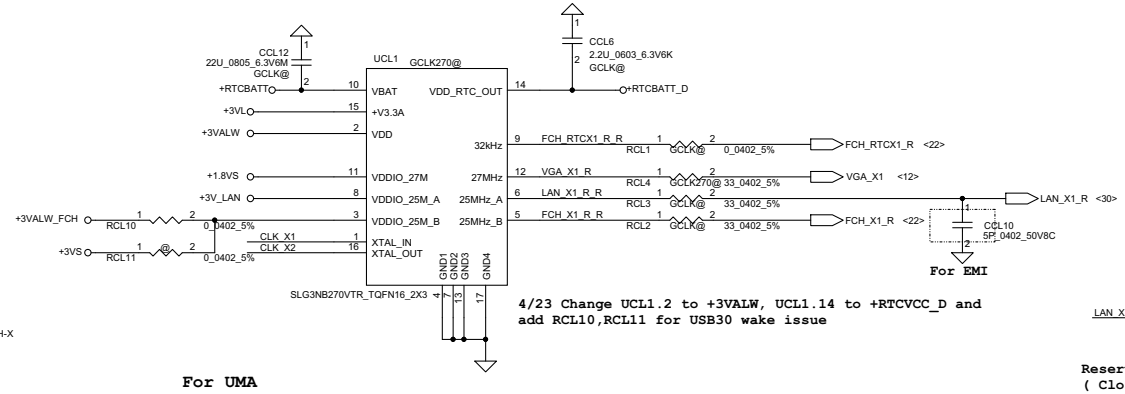


Add WLAN power circuit on DVT

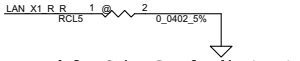
4/23 Change R156,R155,C907,C908,Q210 to @

Green Clock Generator

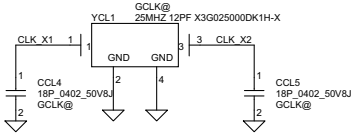




4/23 Change UCL1.2 to +3VALW, UCL1.14 to +RTCVCC_D and add RCL10,RCL11 for USB30 wake issue



Reserved for Swing Level adjustment (Close GCLK side)



For UMA

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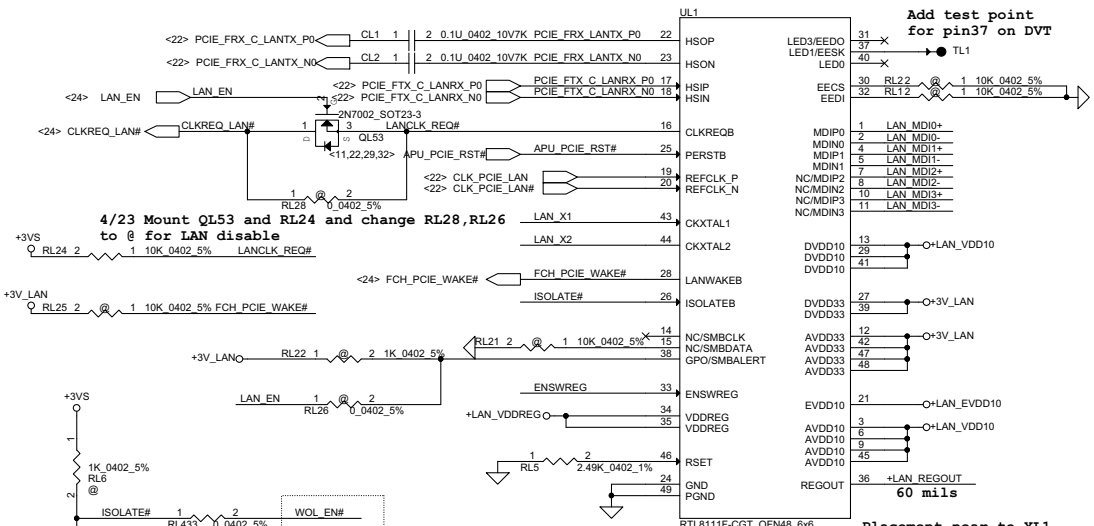
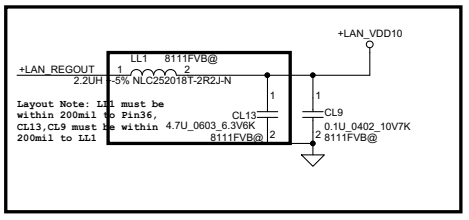
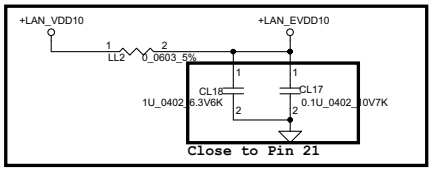
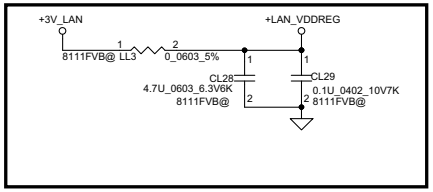
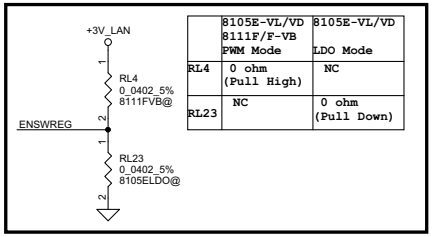


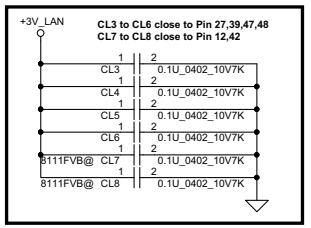


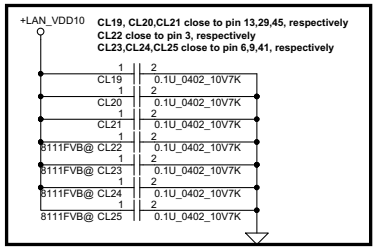




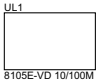


	8105E-VL/VD 8111F/F-VB PWM Mode	8105E-VL/VD LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)



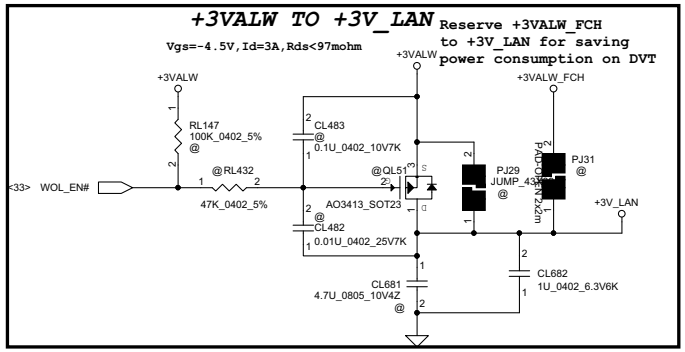


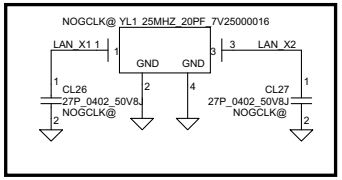
For P/N and footprint
Please place them to ISPD page



	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

	RTL8105E	RTL8111E/F
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	NC	1K ohm PH

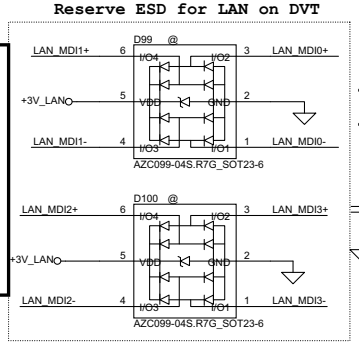


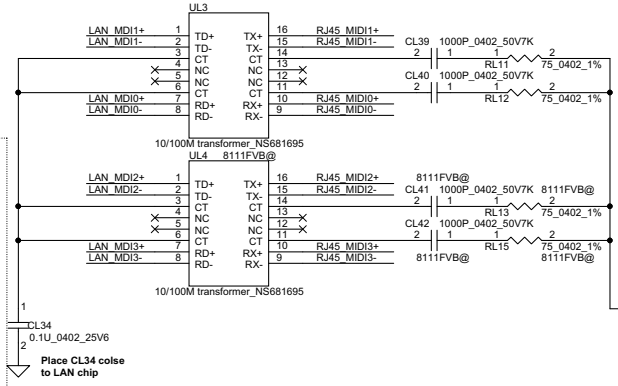


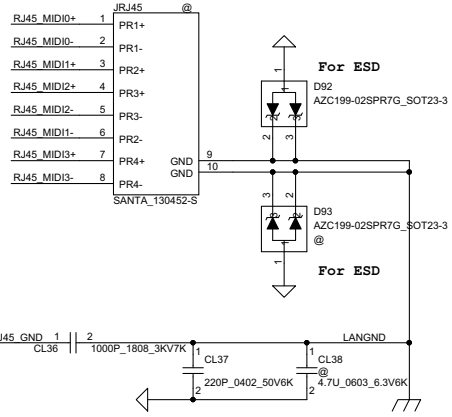
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN S0	LAN_EN Sx	ISOLATEB S0	ISOLATEB Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms







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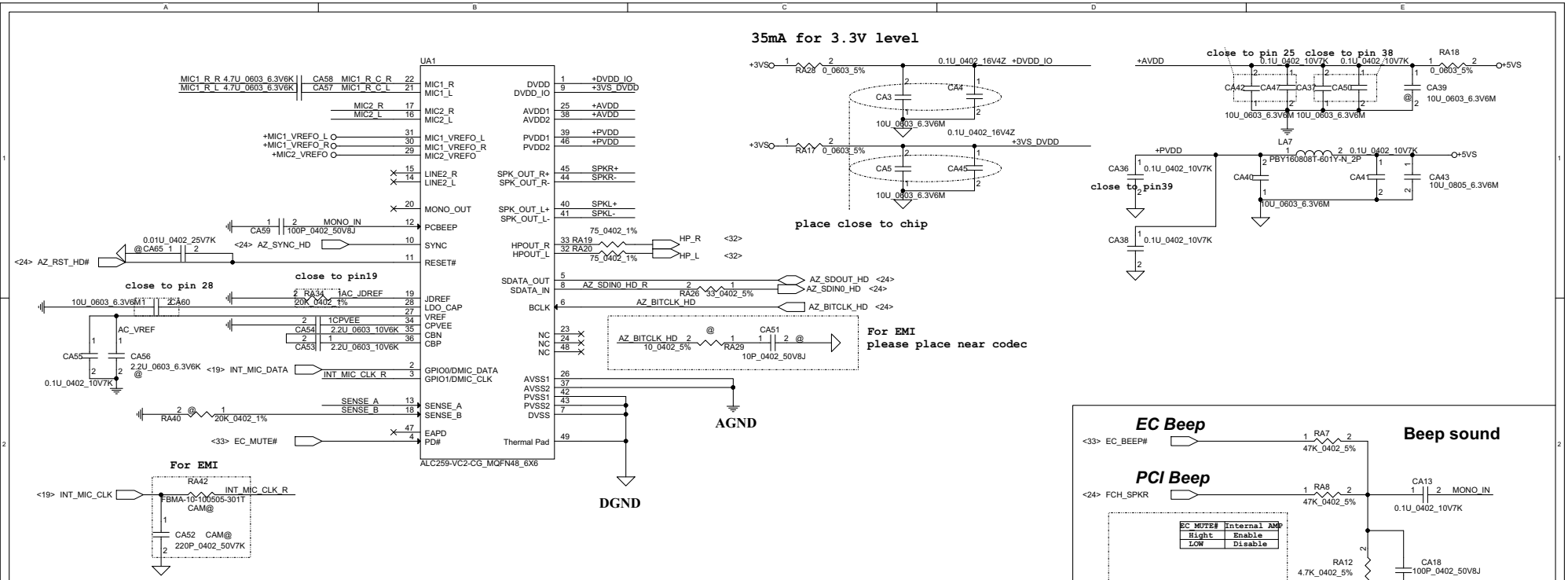
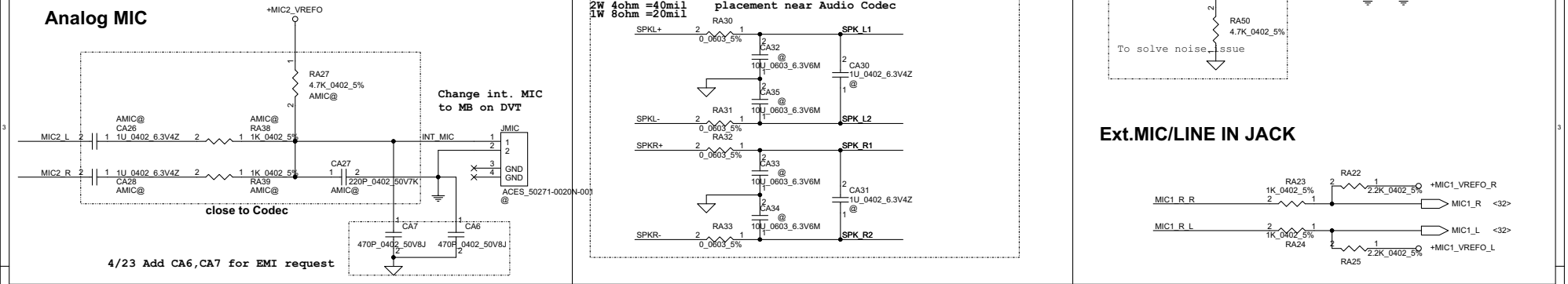
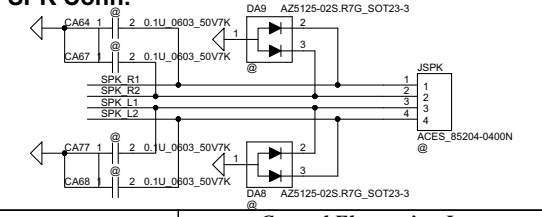
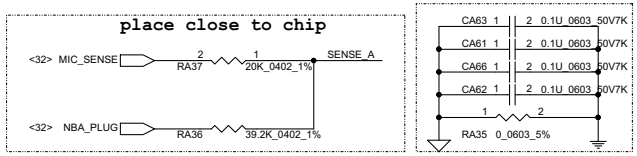






Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Analog MIC
	10K	PORT-H (PIN 20)	



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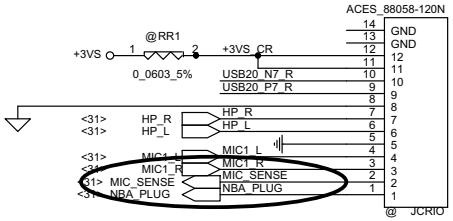
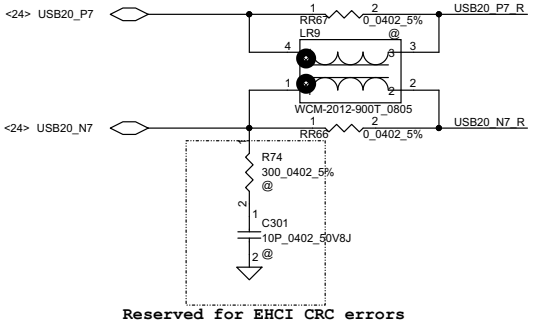
CardReader Conn.

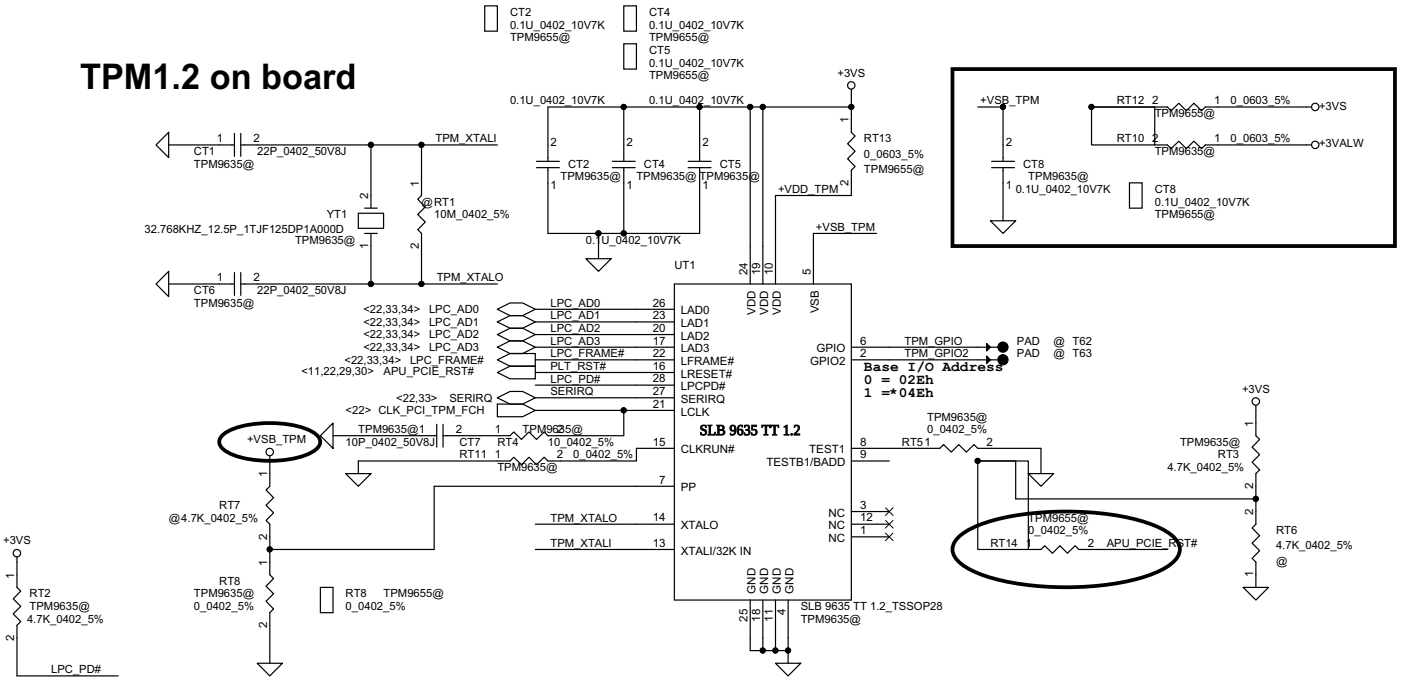


Update JCRIO pin definition on DVT



Reserved for EHCI CRC errors

TPM1.2 on board



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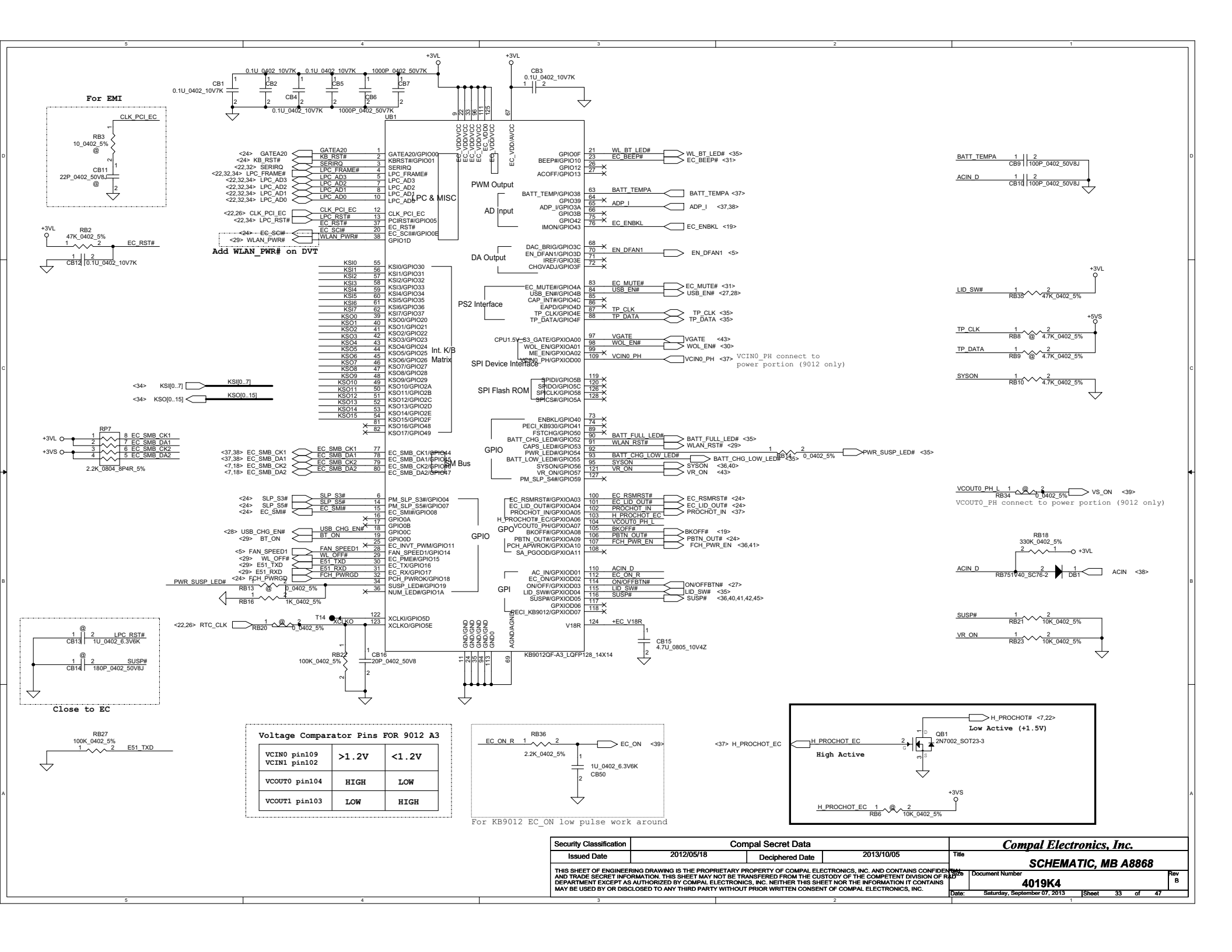

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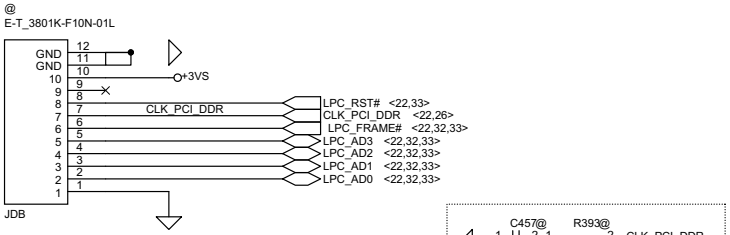
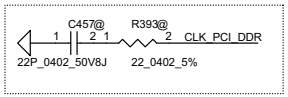
LPC Debug Port

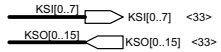
Place the PAD under DDR DIMM.

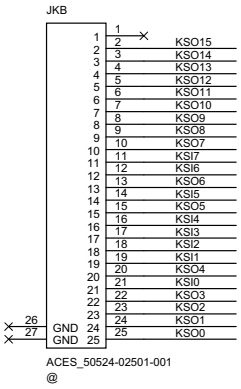




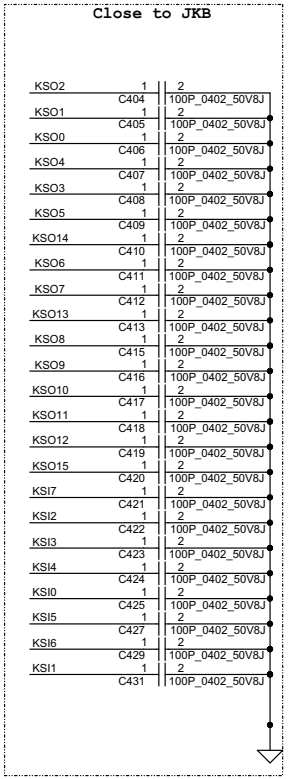
For EMI

KEYBOARD CONN.





For EMI
Close to JKB



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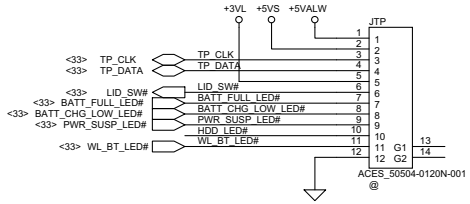
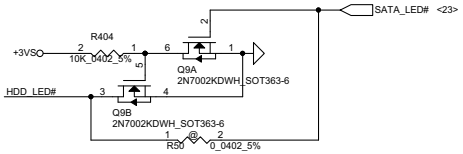
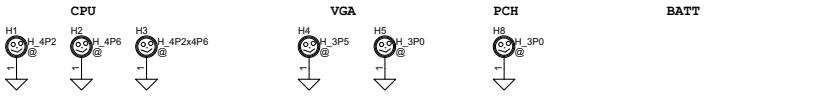
Touchpad Connector
(Reserve 7 pins for LED & Win8 TP)

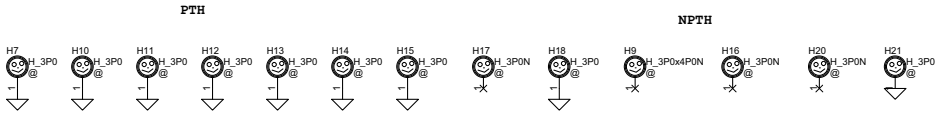


HDD LED



Screw Hole





PCB Fedical Mark PAD

ISPD

PCB ZZZ — PCB LA-8868P REV1

DC-IN PJP1 — PJP1 45@

FCH U2 — AMD A13 HUDSON-M3L R3 M3LR3@

CPU U1 — AMD E2-1800 R1_UNBW E2R1@

U1 — AMD E2-1800 R3 E2R3@

U1 — AMD E1-1200 R3 E1R3@

GPU UV1 — 2160809024A11SEYMOU_FCBGA631 SEYMOURR3@

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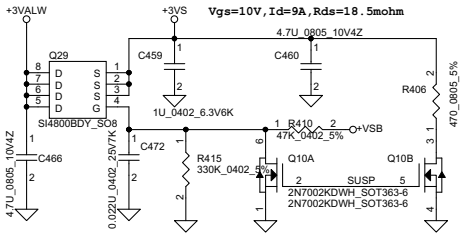
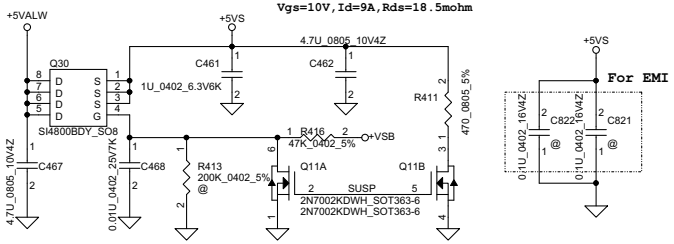
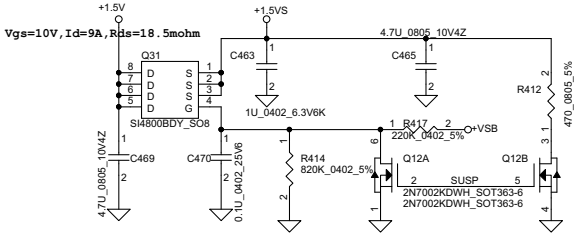
+3VALW TO +3VS

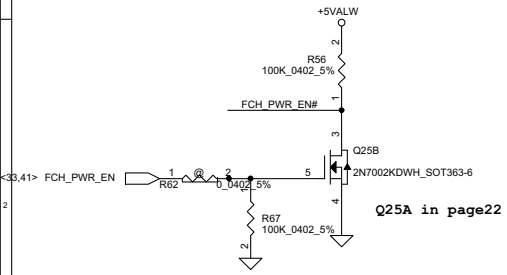


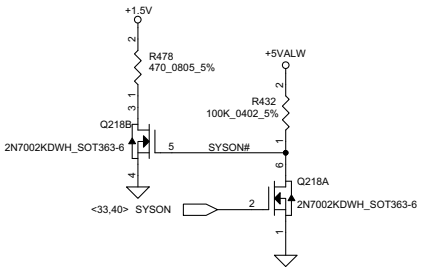
+5VALW TO +5VS

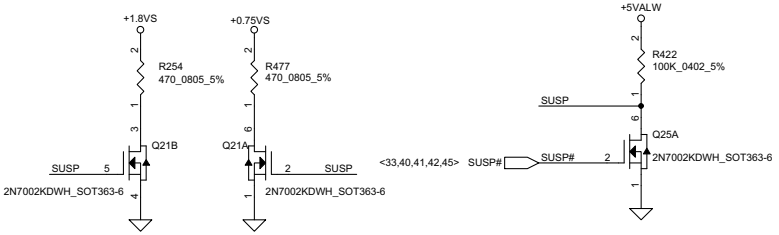


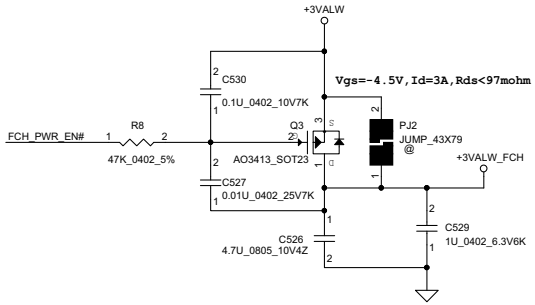
+1.5V to +1.5VS



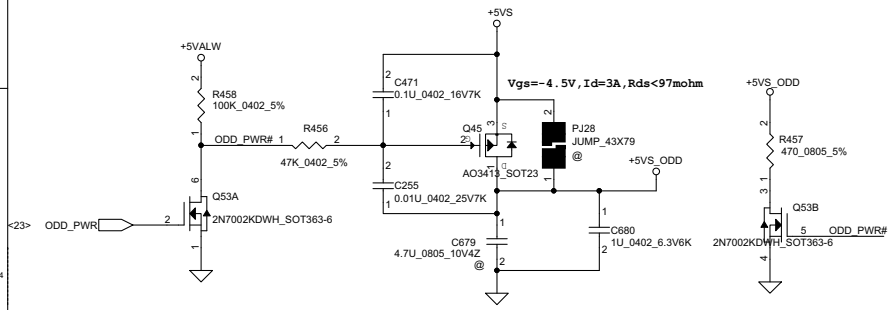




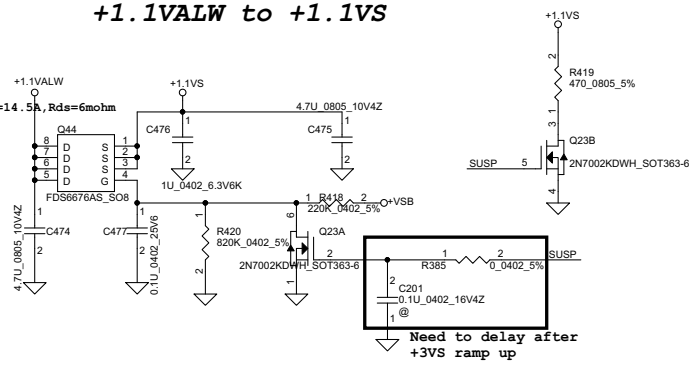




+5VS TO +5VS_ODD



+1.1VALW to +1.1VS



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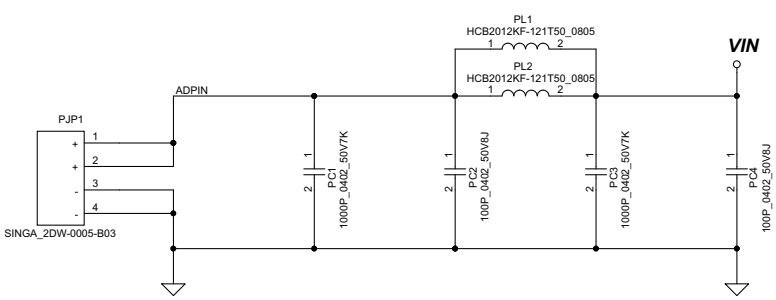
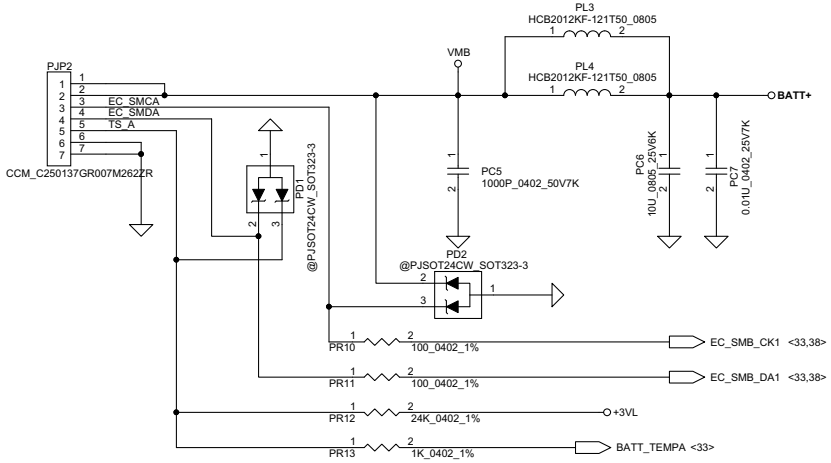
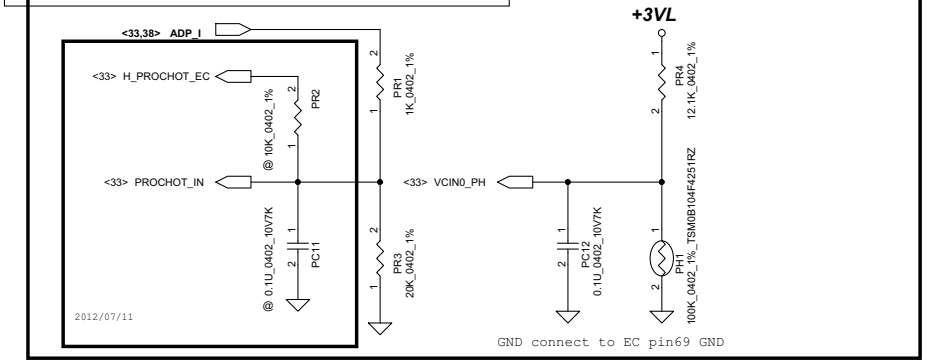
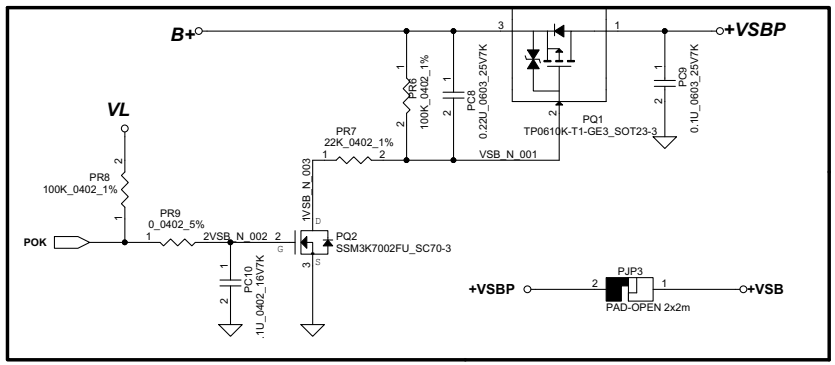




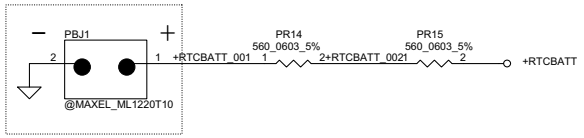
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

Please locate these parts
Near EC chip





RTC Battery



SP093MX0000

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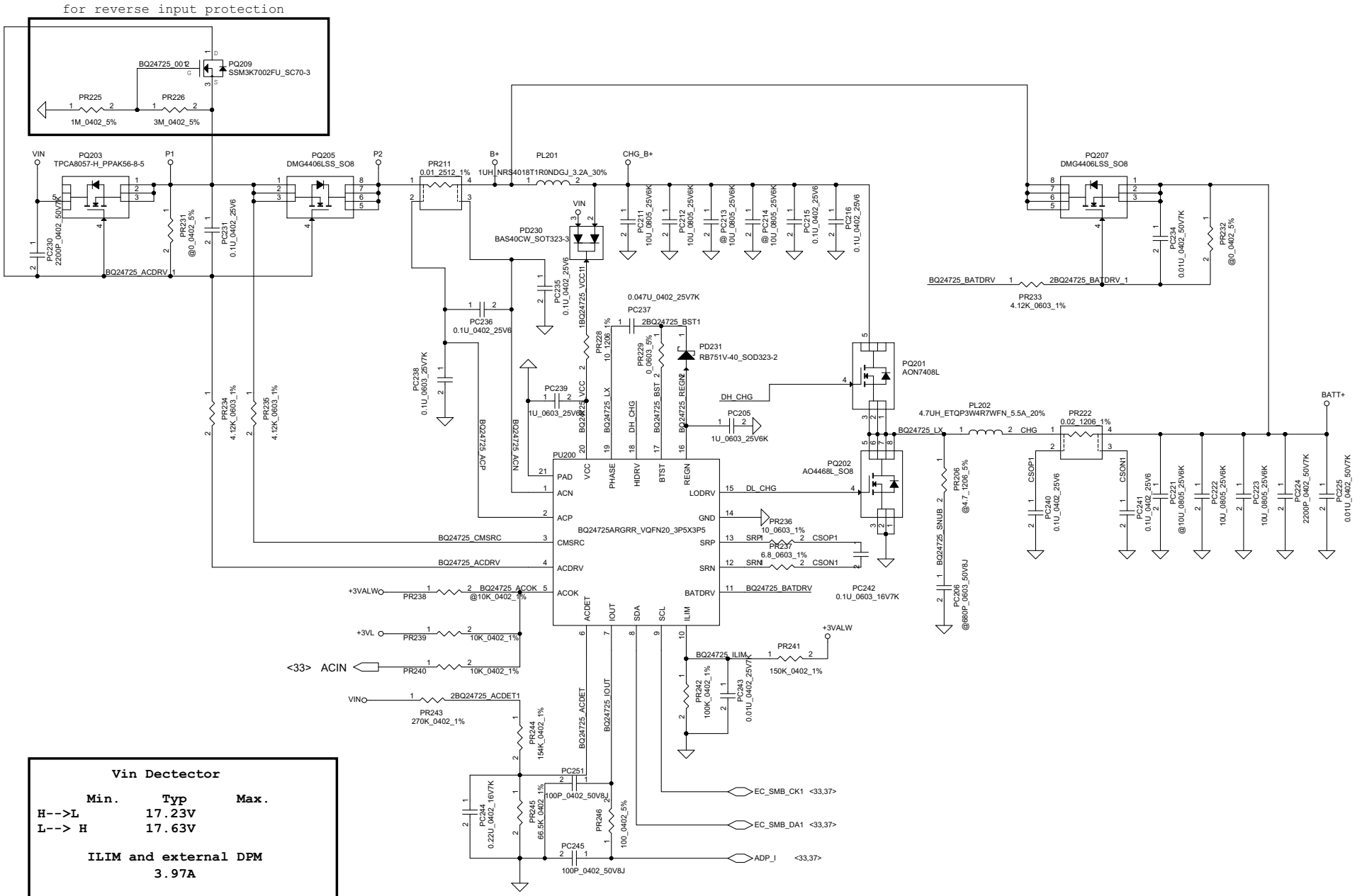

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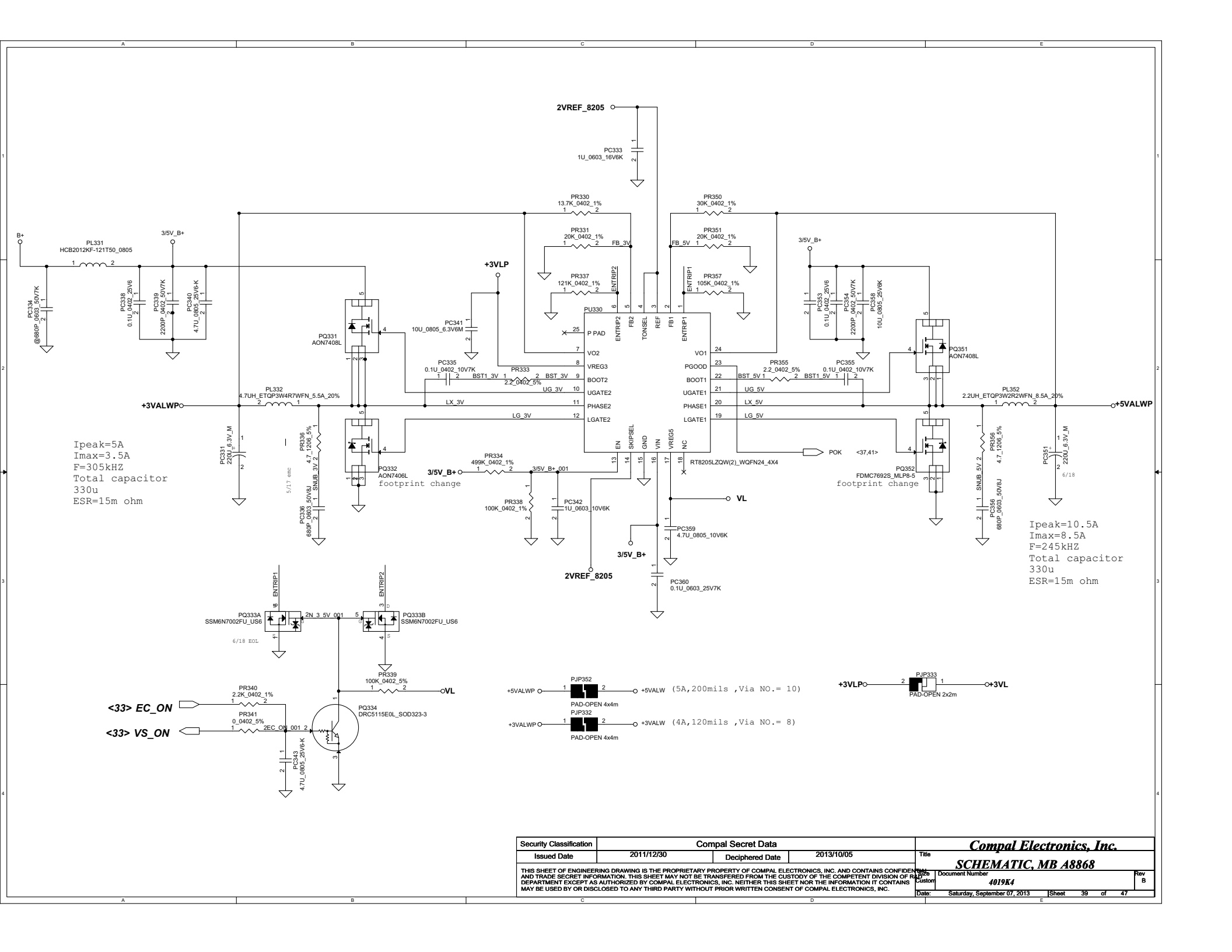

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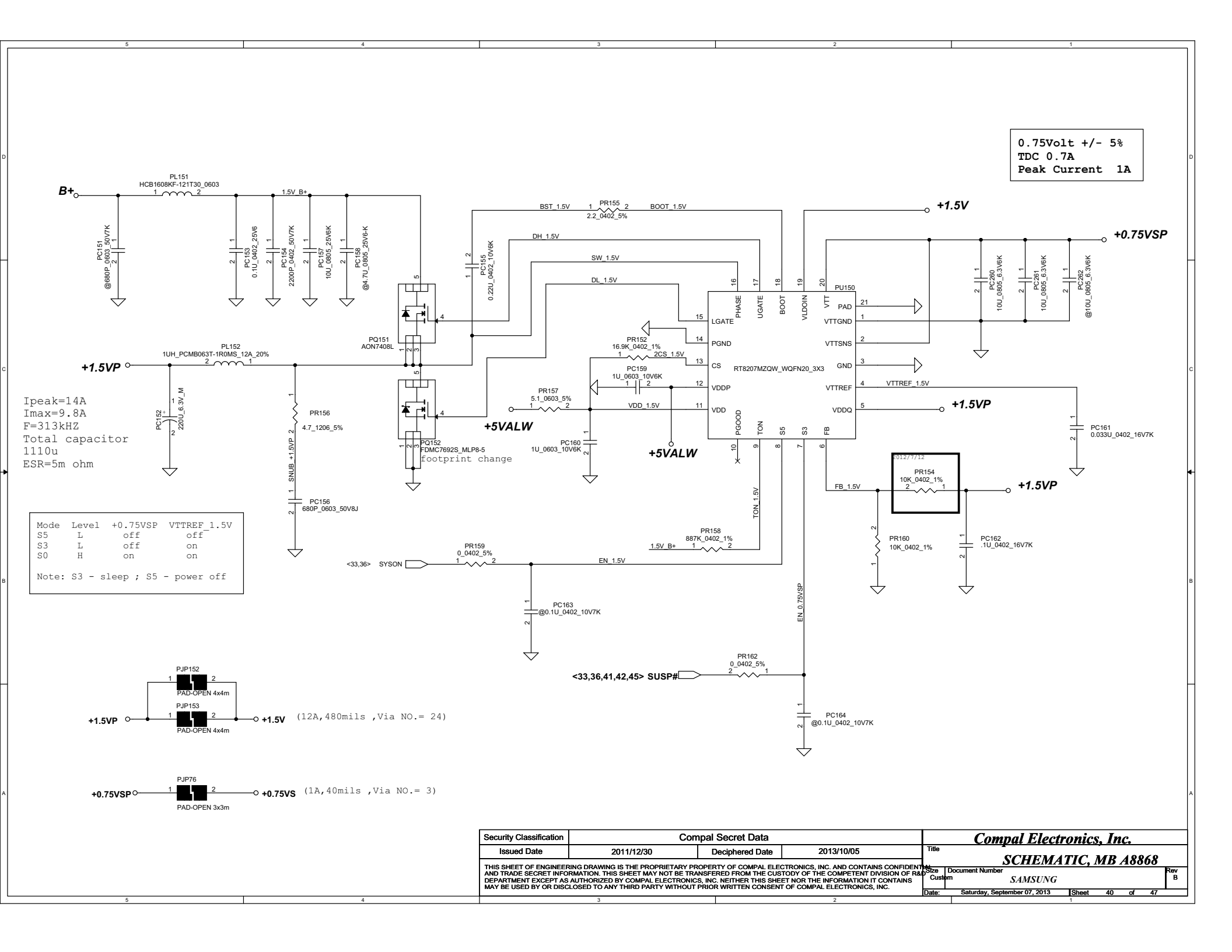

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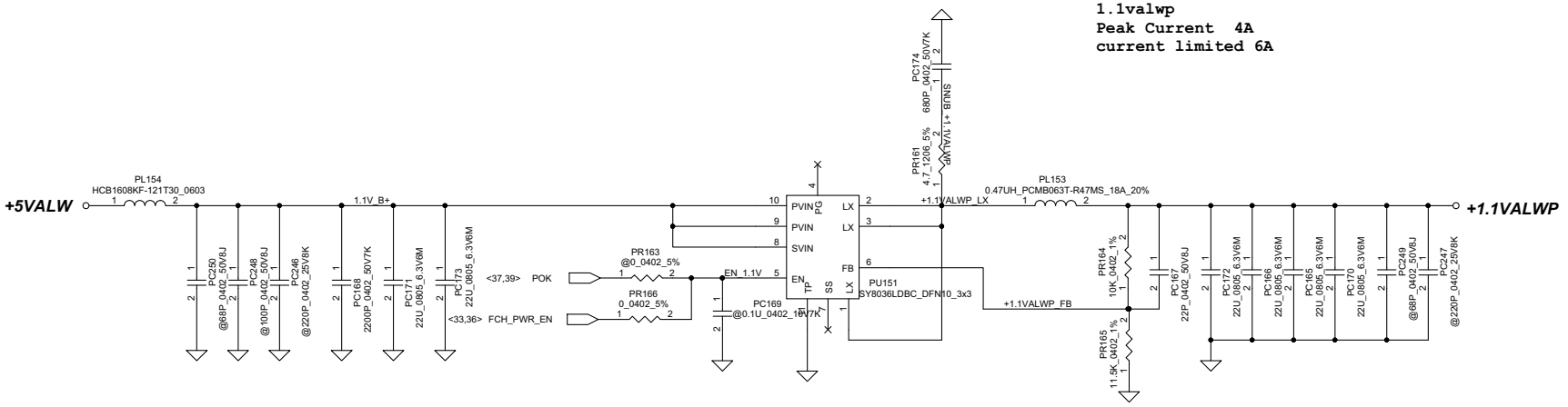
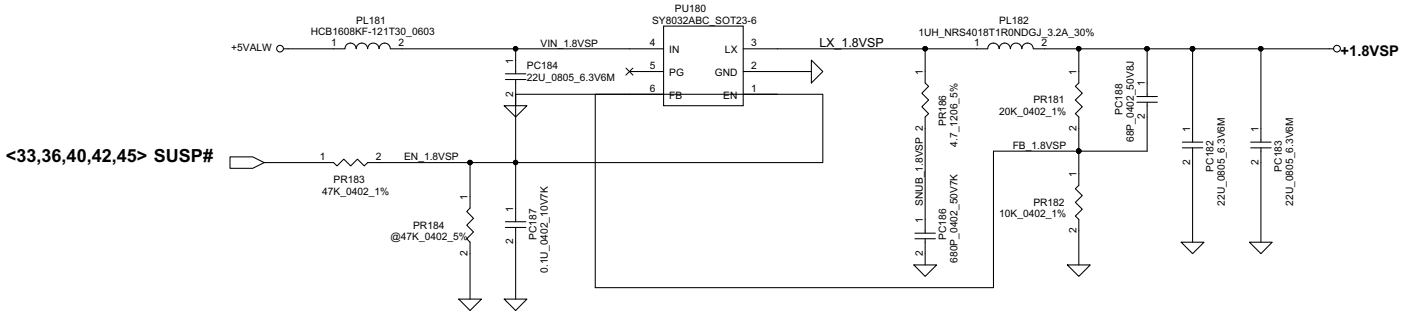
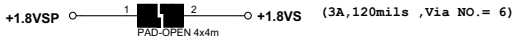
1.1valwp
Peak Current 4A
current limited 6A



(4A,240mils ,Via NO.= 8)





(3A,120mils ,Via NO.= 6)

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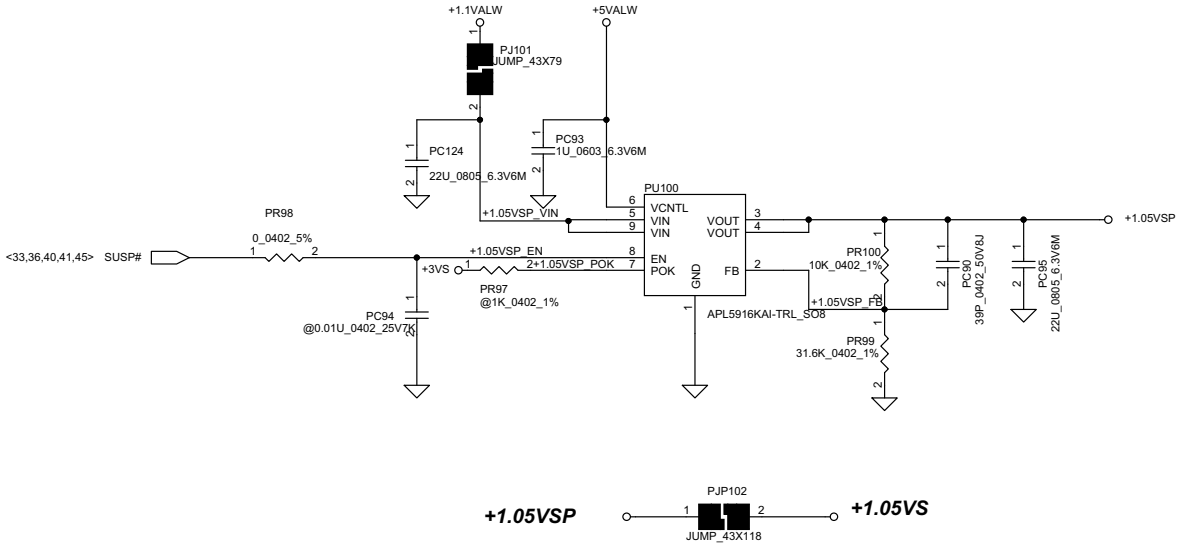

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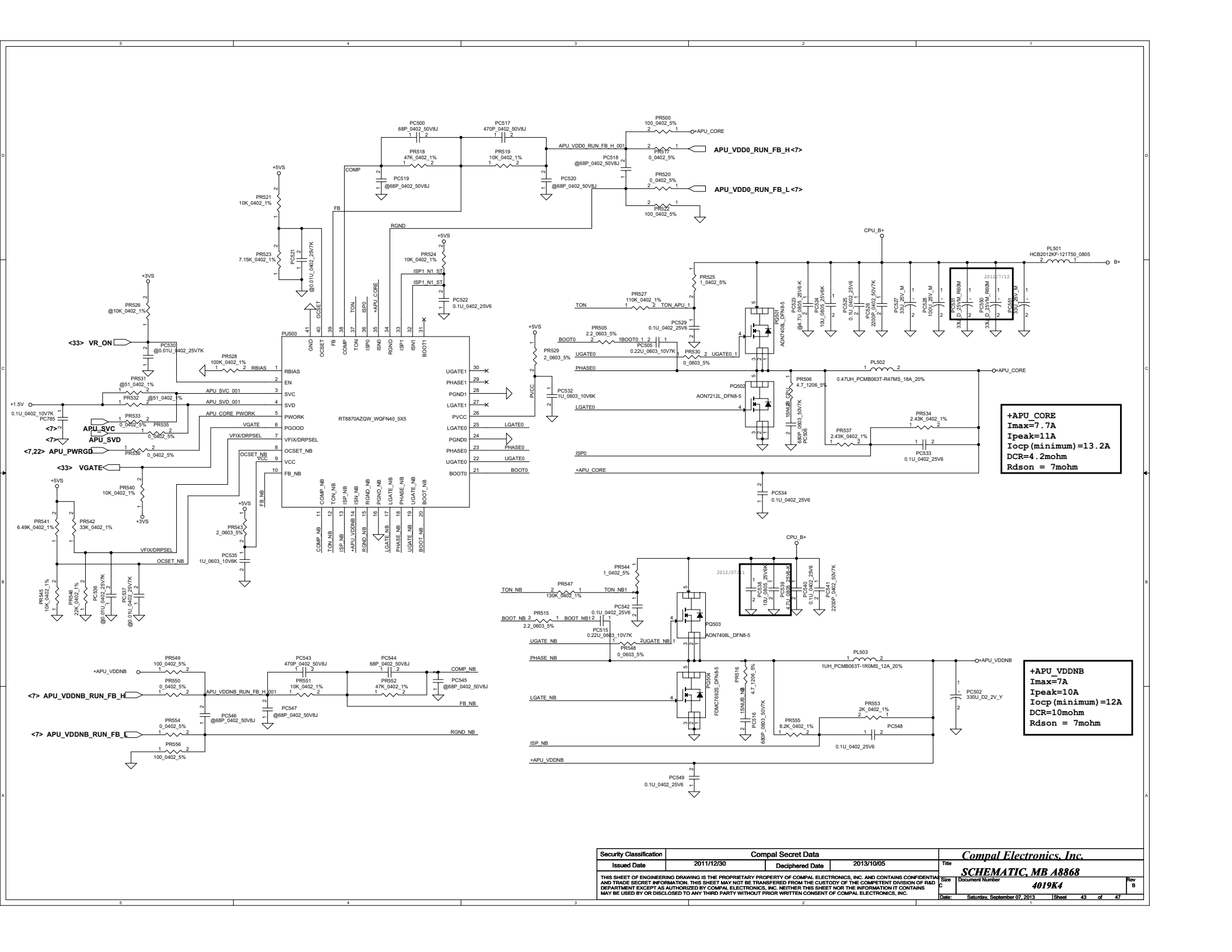

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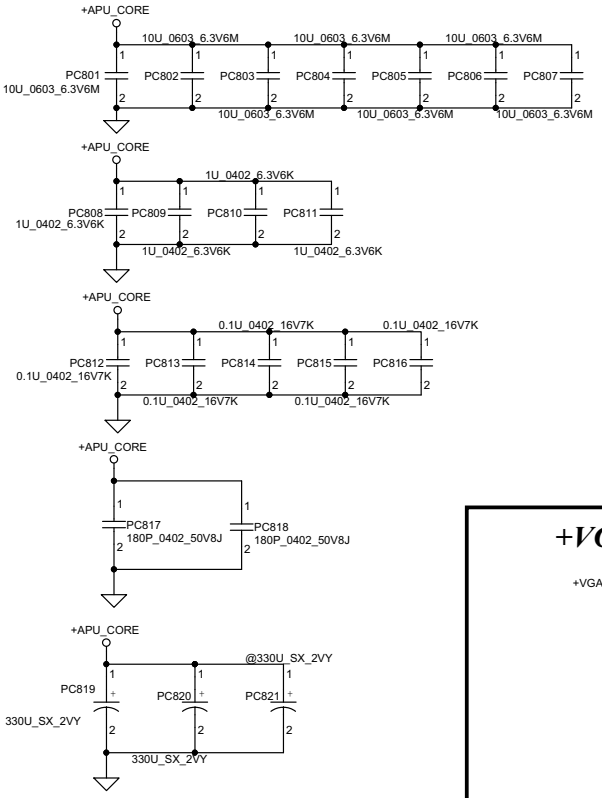
+APU_CORE



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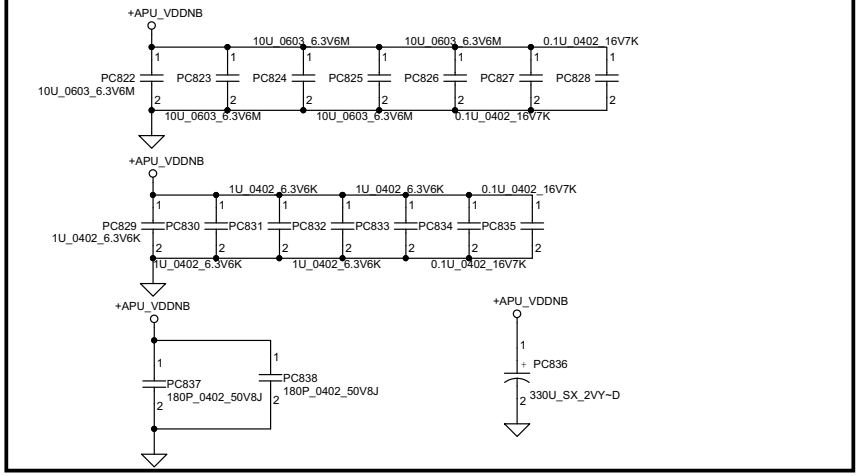

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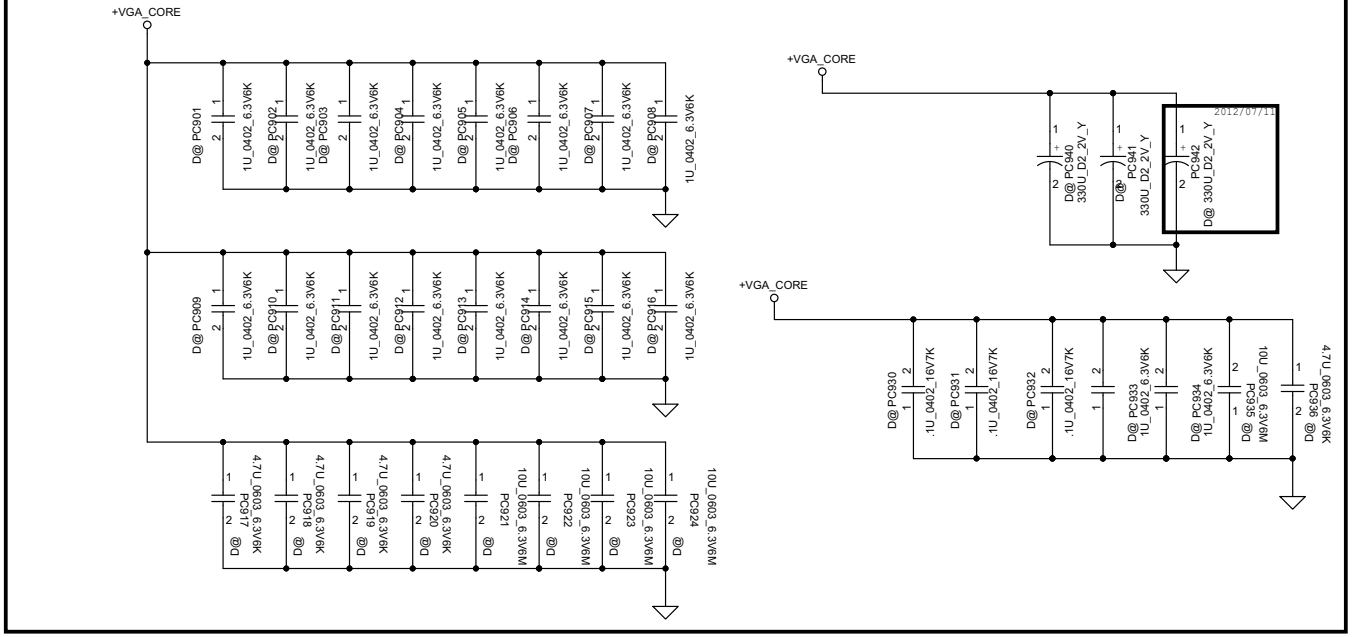

Security Classification	Compal Secret Data		
Issued Date	2011/12/30	Deciphered Date	

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Title: SCHEMATIC, MB A8868			
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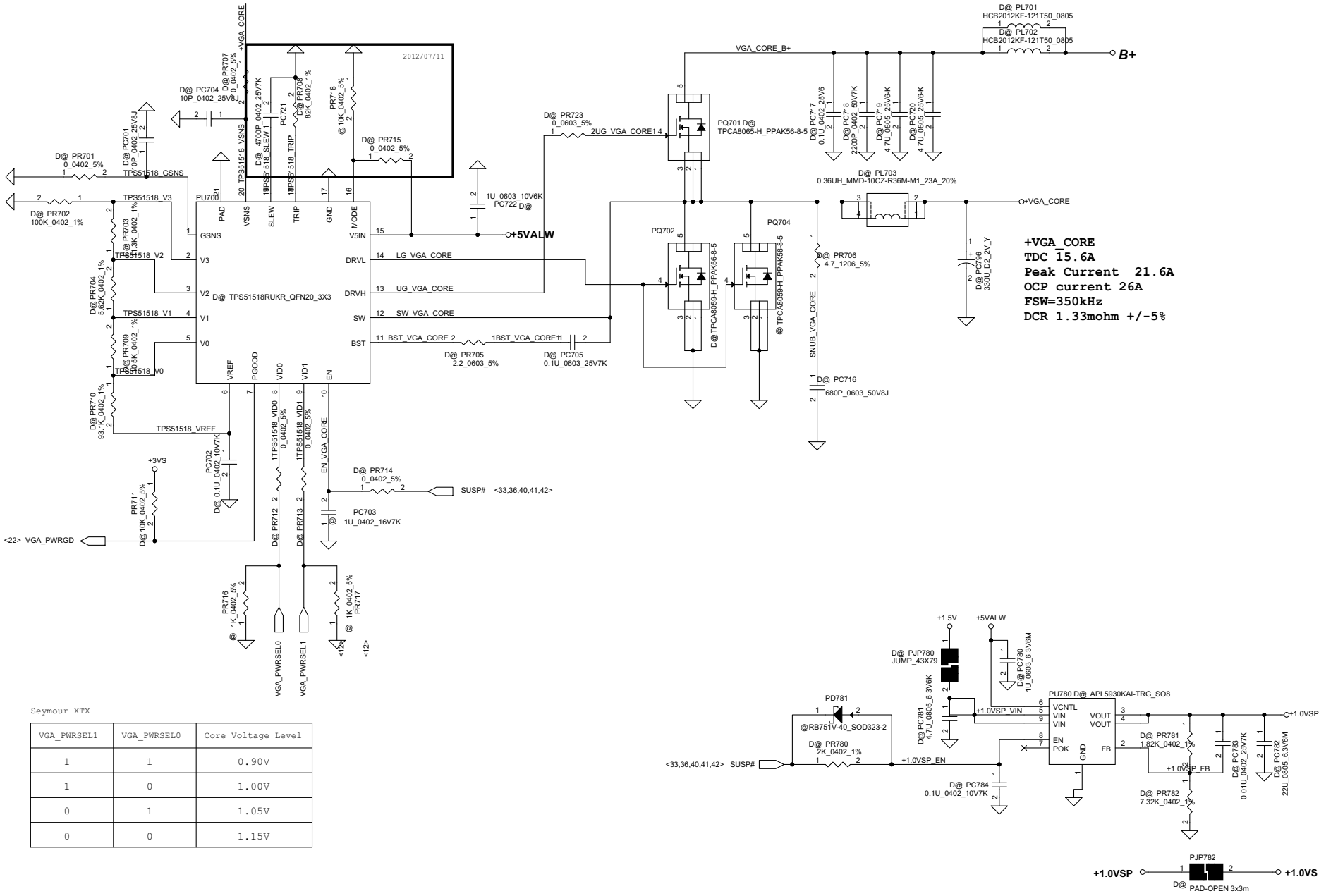
Date: Saturday, September 07, 2013	Sheet 44 of 47		



Seymour XTX

VGA_PWRSEL1	VGA_PWRSEL0	Core Voltage Level
1	1	0.90V
1	0	1.00V
0	1	1.05V
0	0	1.15V

Security Classification	Compal Secret Data		
Issued Date	2011/12/30	Deciphered Date	2013/10/05

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Size	Document Number: 4019K4
Rev	B
Date:	Saturday, September 07, 2013
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