QMLE4/5

Eureka Discrete

LA-8863P REV 0.3 Schematic

AMD Trinity APU / Hudson M3 FCH
Thames XT & Chelsea PRO
2012-03-13 Rev 0.3

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Issued Date	2011/11/28	Deciphered Date	2013/12/31

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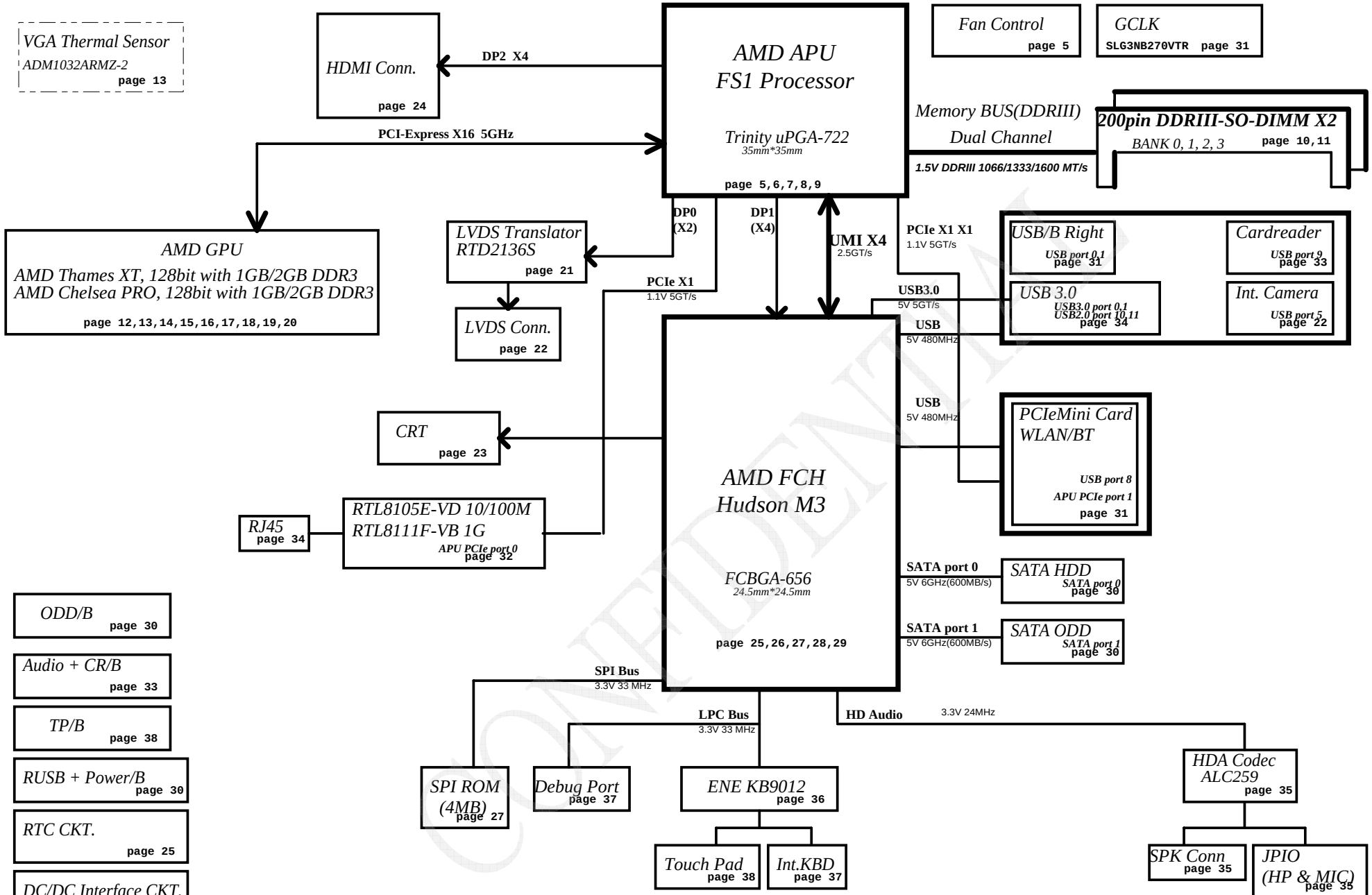

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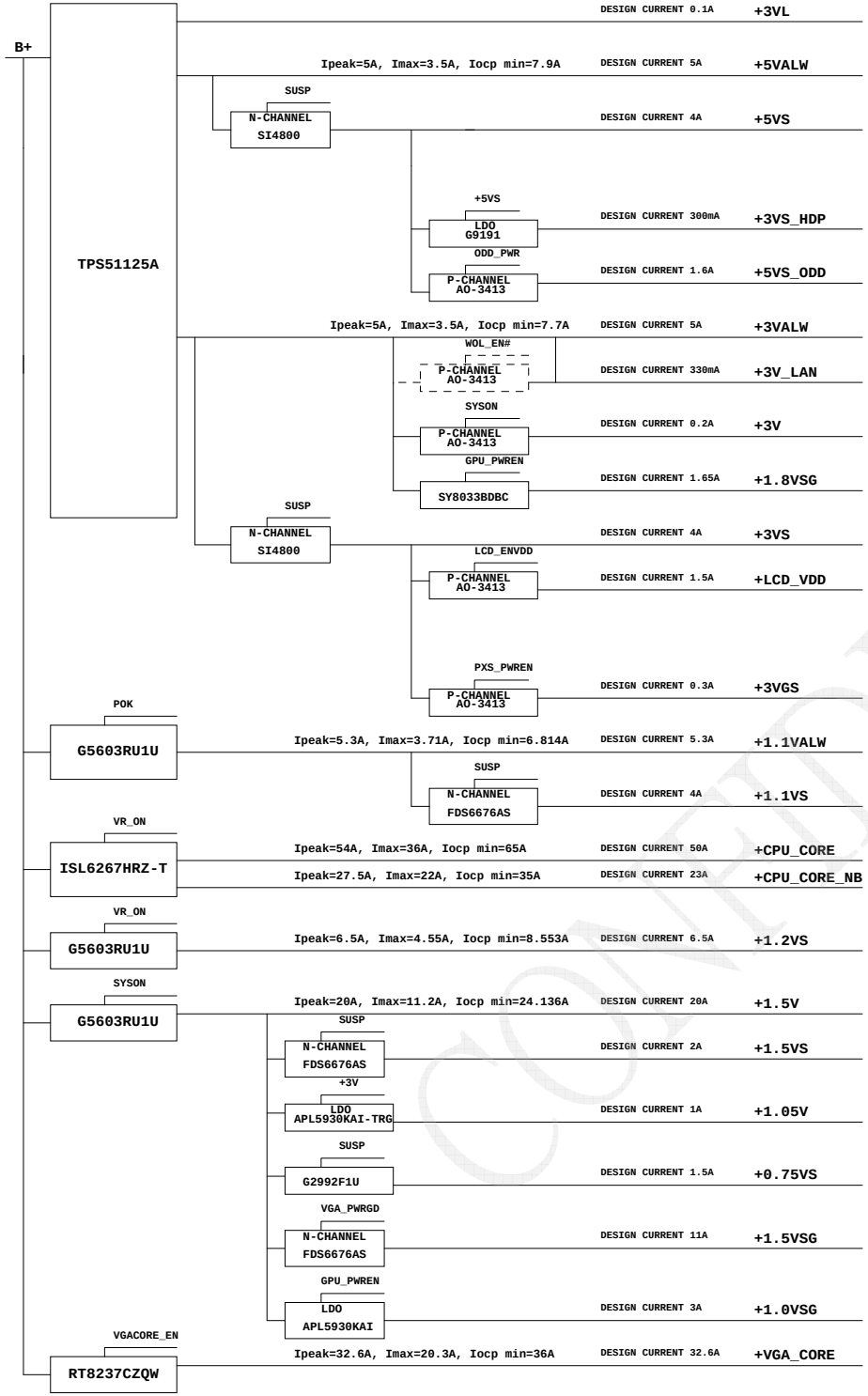

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB +VGA_CORE +3VGS +1.8VSG +1.5VSG +1.0VSG
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

BTO Option Table

Function	HDMI				SKU			
description	HDMI				SKU			
explain	UMA PowerXpress		COMMON		UMA	PowerXpress	Discrete	
BTO	IHDMI@		HDMI@		UMA@	UMA@+VGA@+PXS@	VGA@+DIS@	

Function	MINI PCI-E SLOT	LAN					
description		LAN					
explain		10/100M		GIGA			
BTO		8105ELDO@	8105ESWR@	8111E@			

Function			Cam & Mic	Panel		
description			Cam & Mic	Panel (DIS@)		
explain			Cam & Mic			
BTO			CAM@			

Function	GPIO for PowerXpress		Chipset			
description	PowerXpress (PXS@)		FCH		GPU	
explain	PowerXpress Enable	Crossfire Enable	Hudson-M3		Whistler Pro	
BTO	PXSEN@	CROSSEN@	HUDM3R1@	HUDM3R3@	WHPROR1@	WHPROR3@

Function	PowerXpress			FCH		
description	PowerXpress			FCH		
explain	BACO mode	Non-BACO		Hudson-M2	Hudson-M3	
BTO	BACO@	NOBACO@		M2@	M3@	

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	90 H	1001 000xb
+3VS	DDR SO-DIMM 1	92 H	1001 001xb
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011x b
+3VL	Charger IC	12 H	0001 001x b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	APU Thermal Sensor	98 H	1001 100x b
+3VS	GPU Internal Thermal	82 H	1000 001x b
+3VS	GPU External Thermal	9A H	1001 101x b
+3VS	GPU External Thermal	9A H	1001 101x b

EC SM Bus3 Address

+3VS	LVDS EEPROM	A8 H	1010 1000 b

STATE / SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

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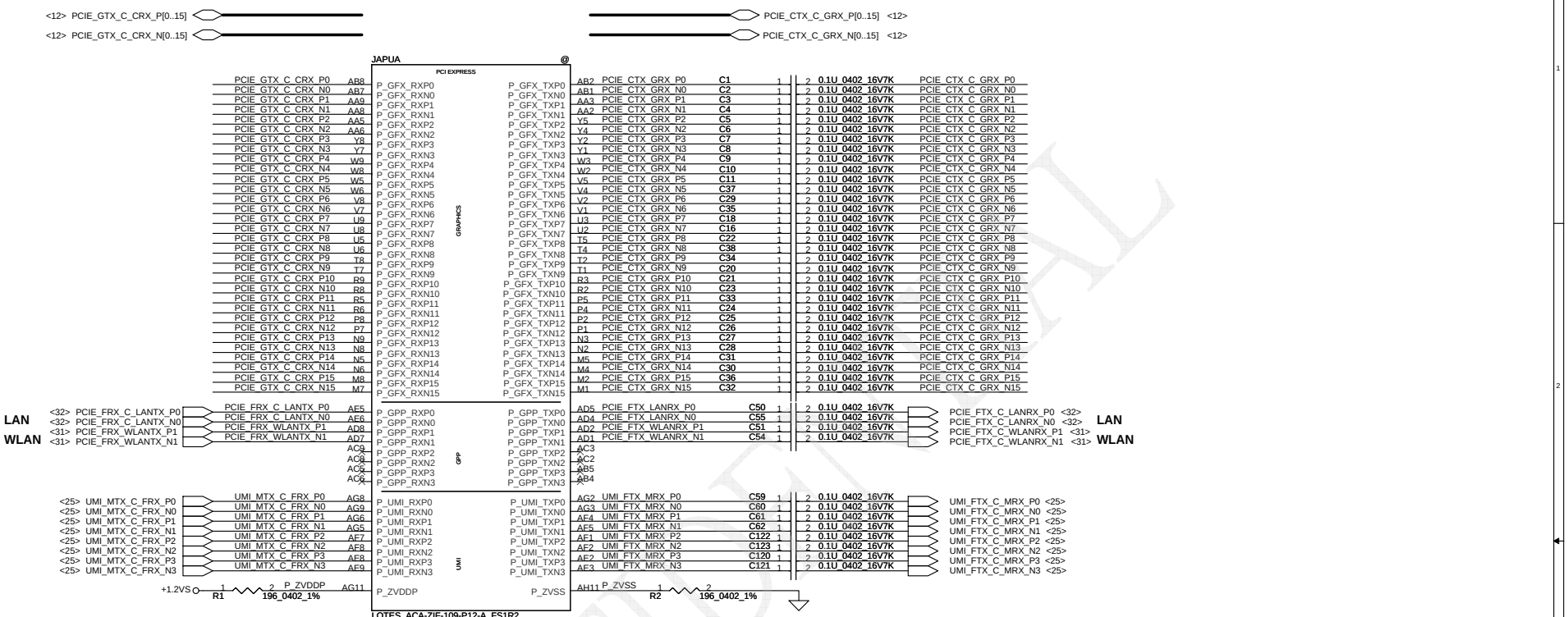

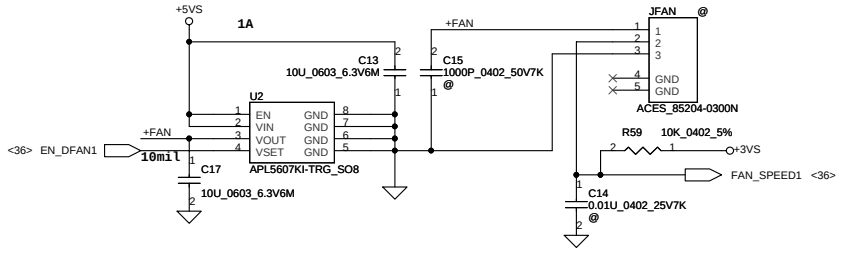

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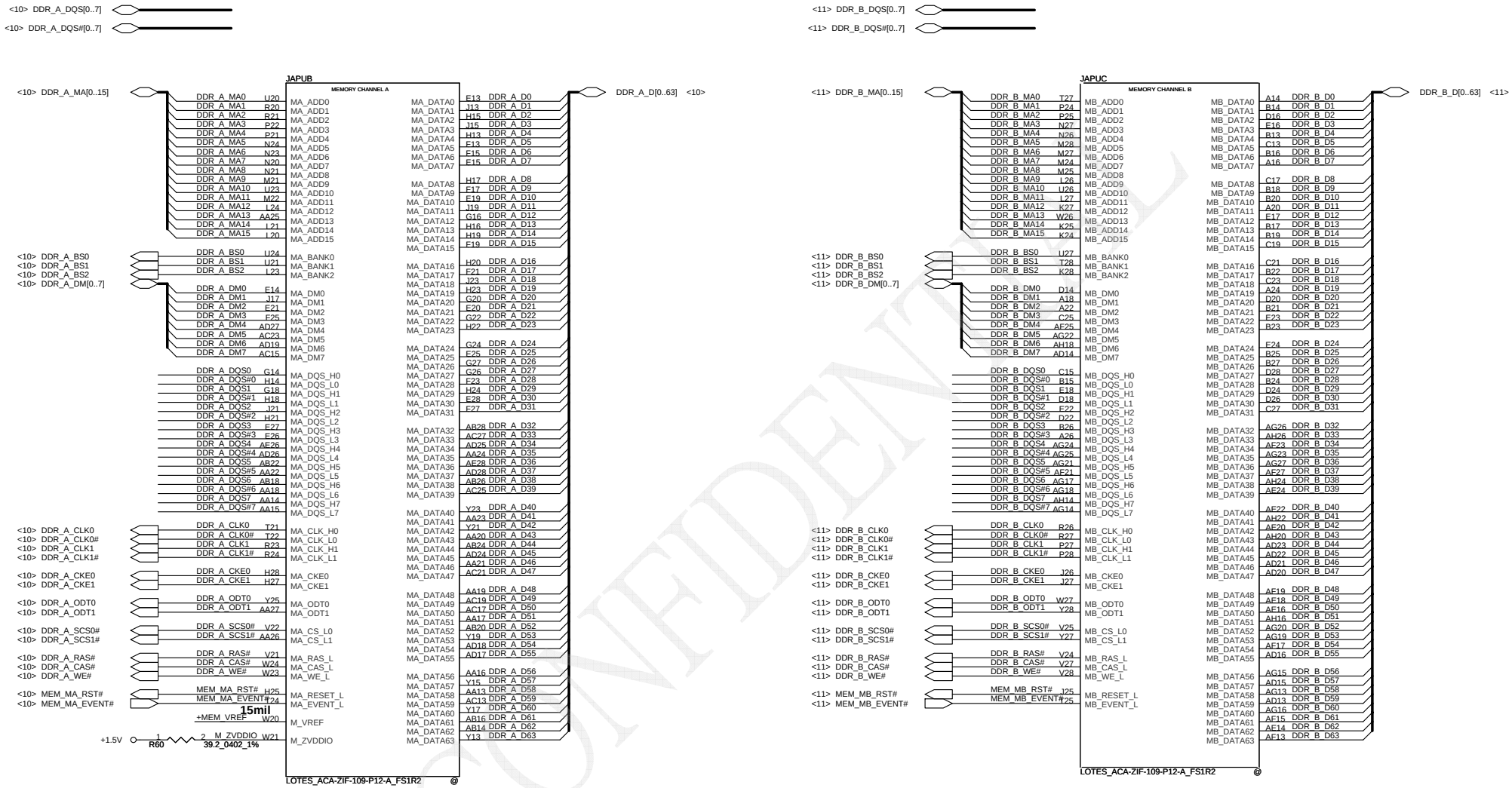
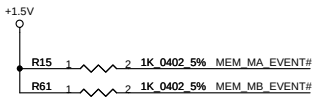
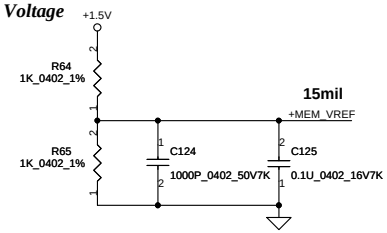


EVENT# pull high



0.75V Reference Voltage



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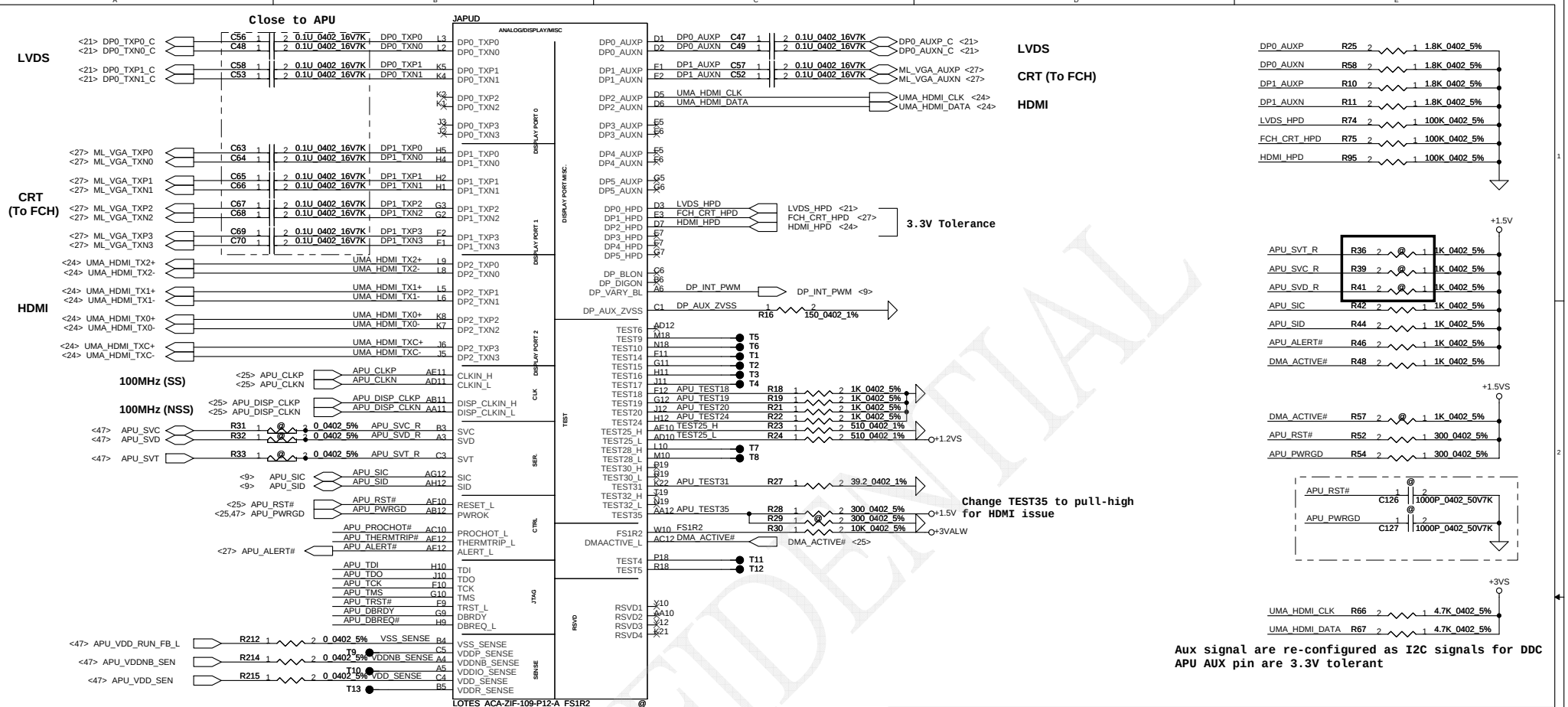

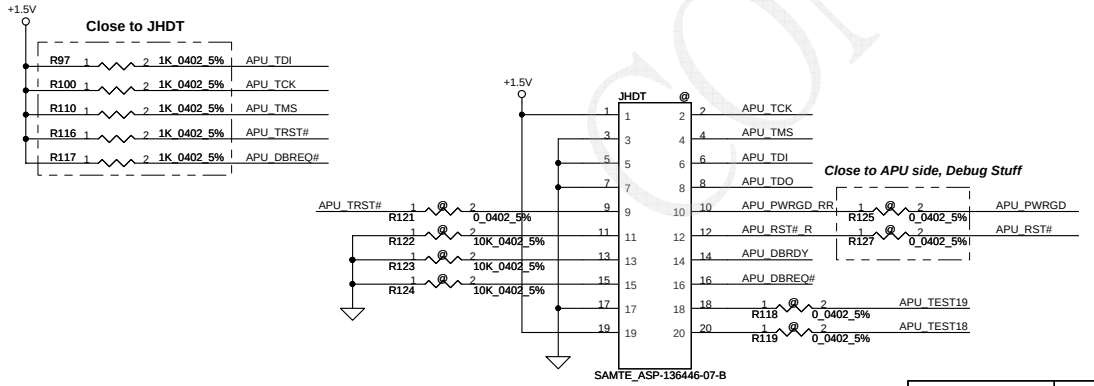

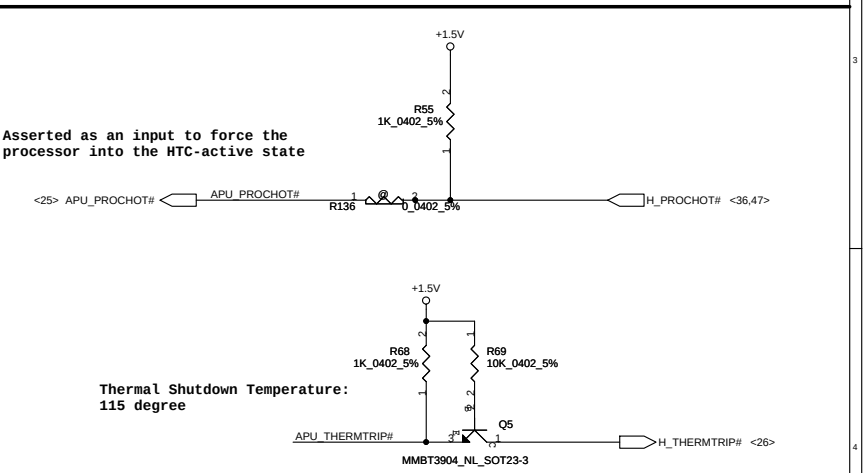

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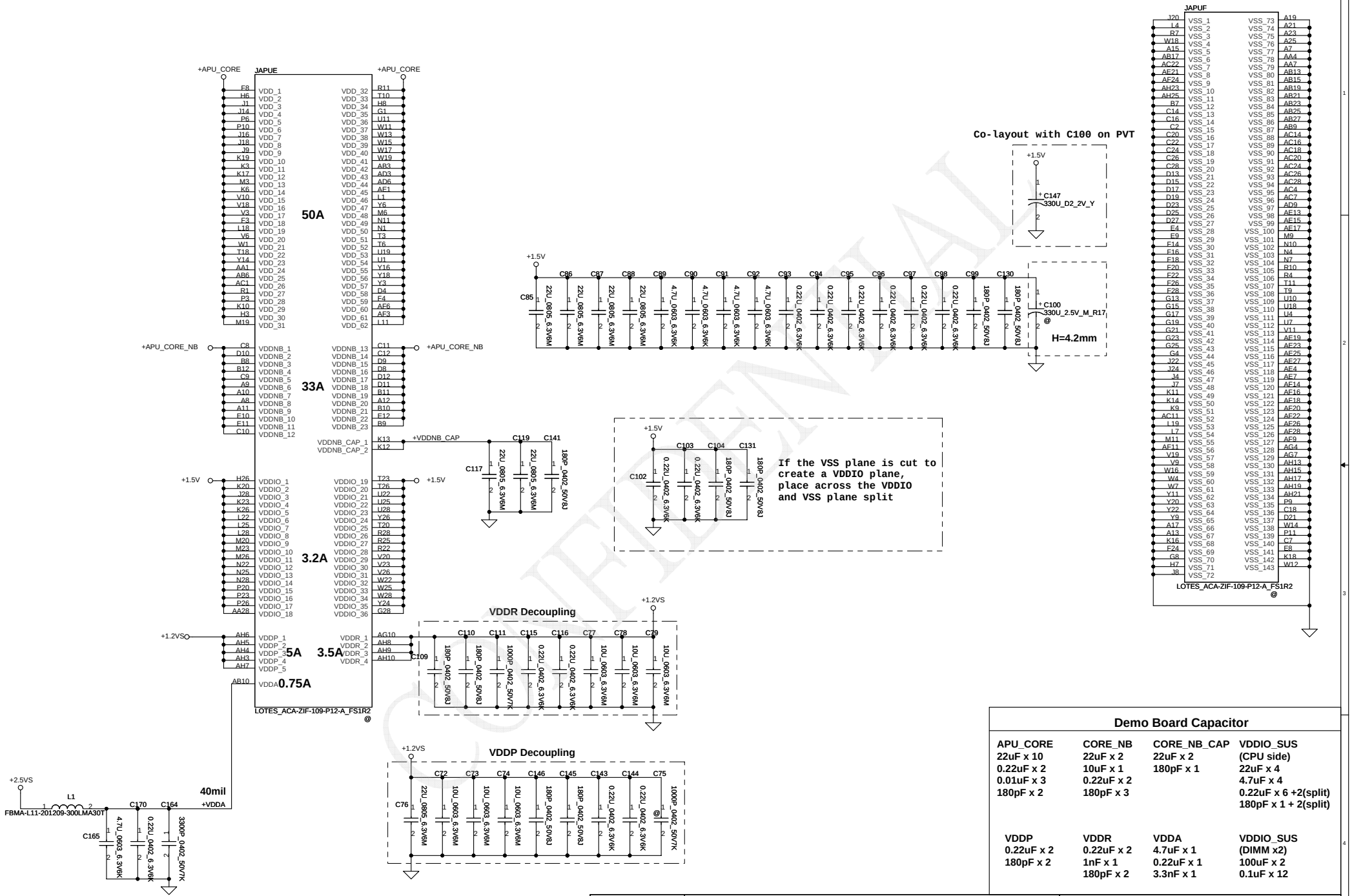

Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 1	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

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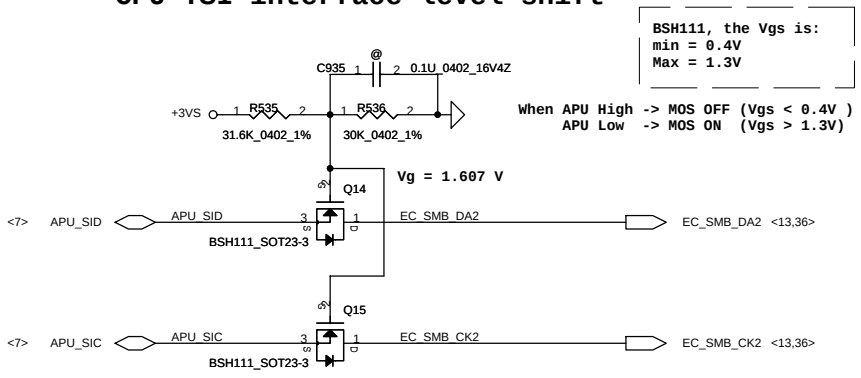
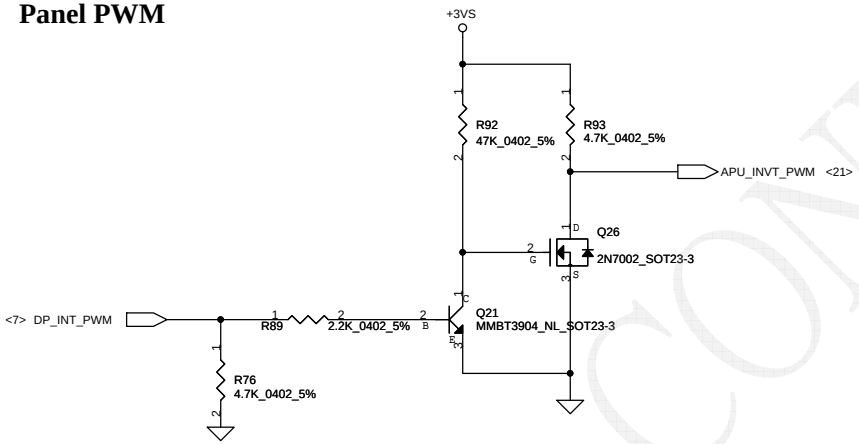
SB-TSI

CPU TSI interface level shift



Panel PWM



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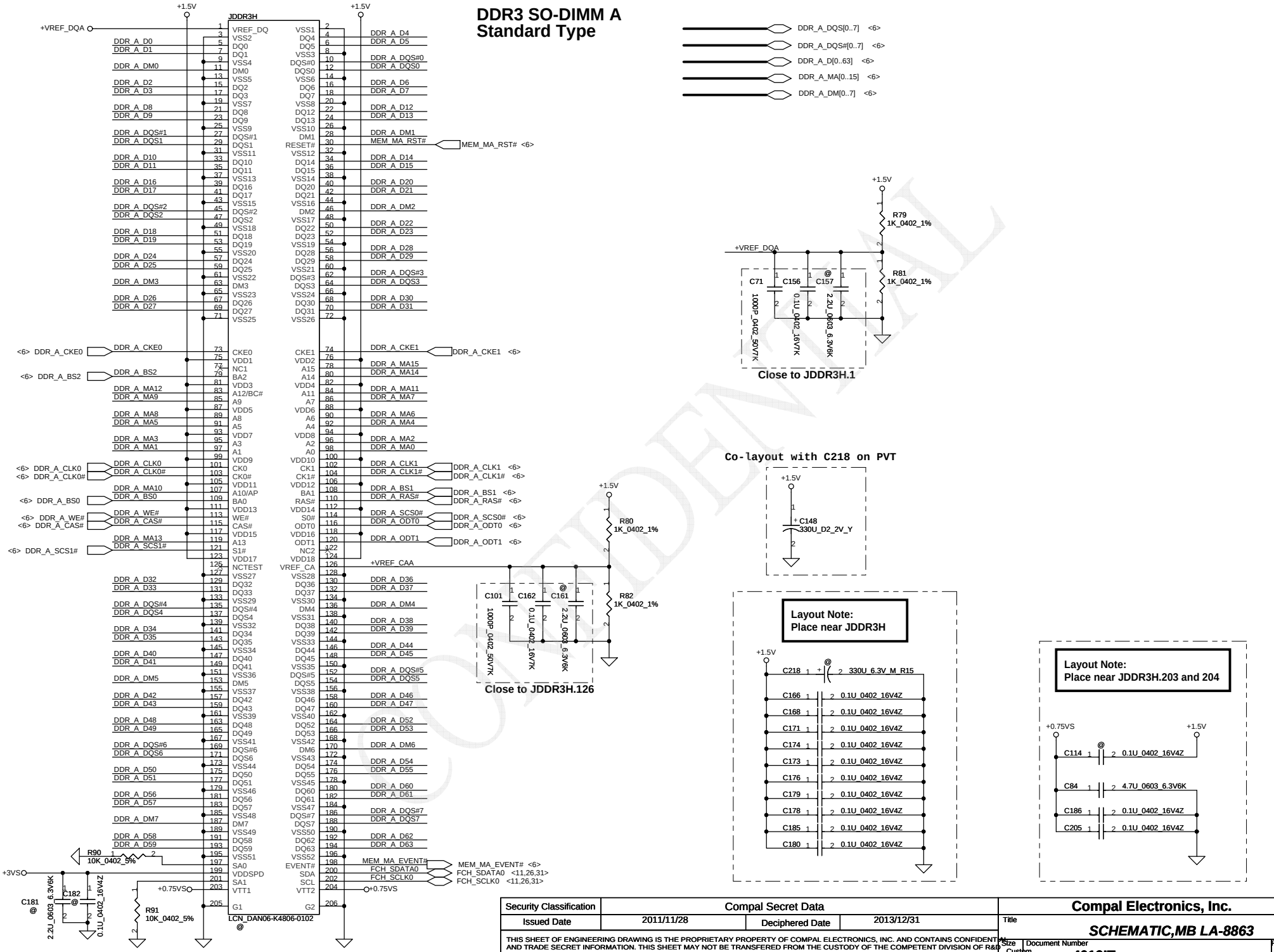
DDR3 SO-DIMM A
Standard Type



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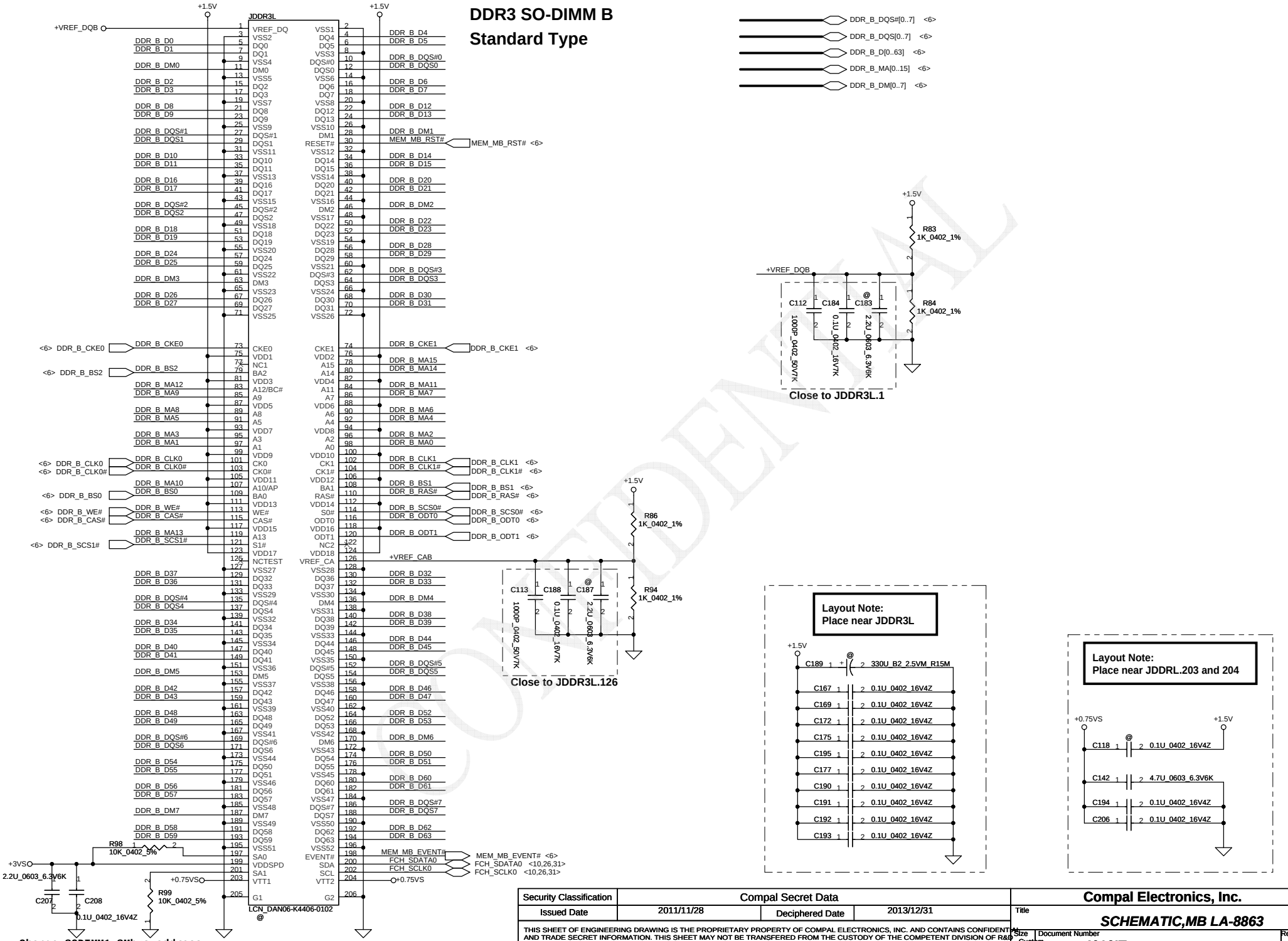
DDR3 SO-DIMM B
Standard Type



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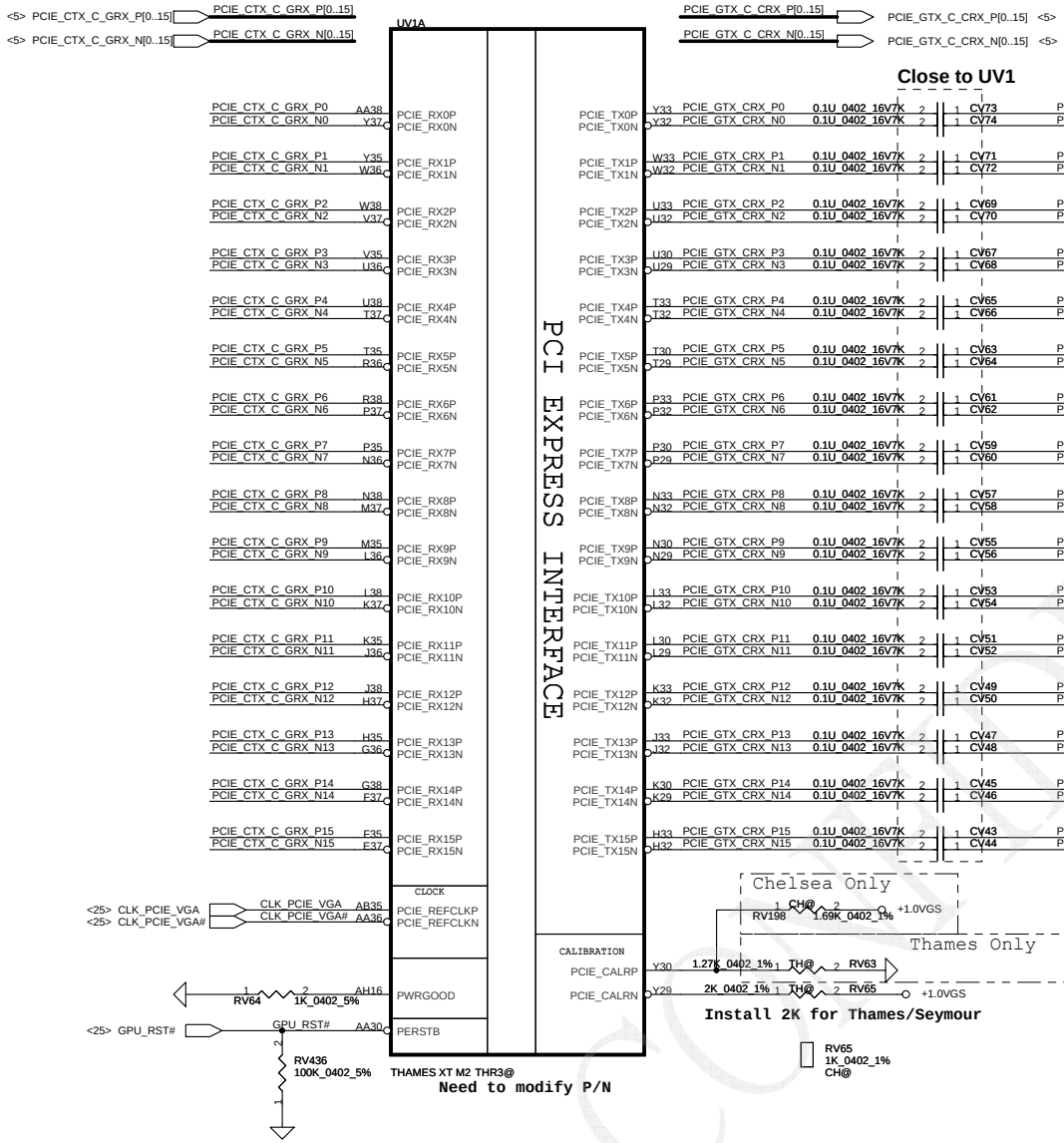
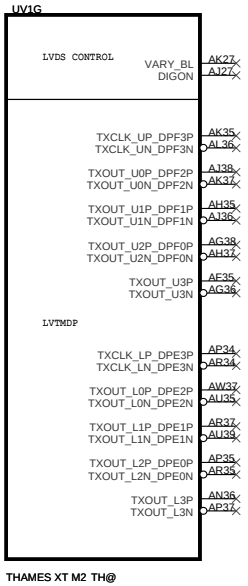


LVDS Interface



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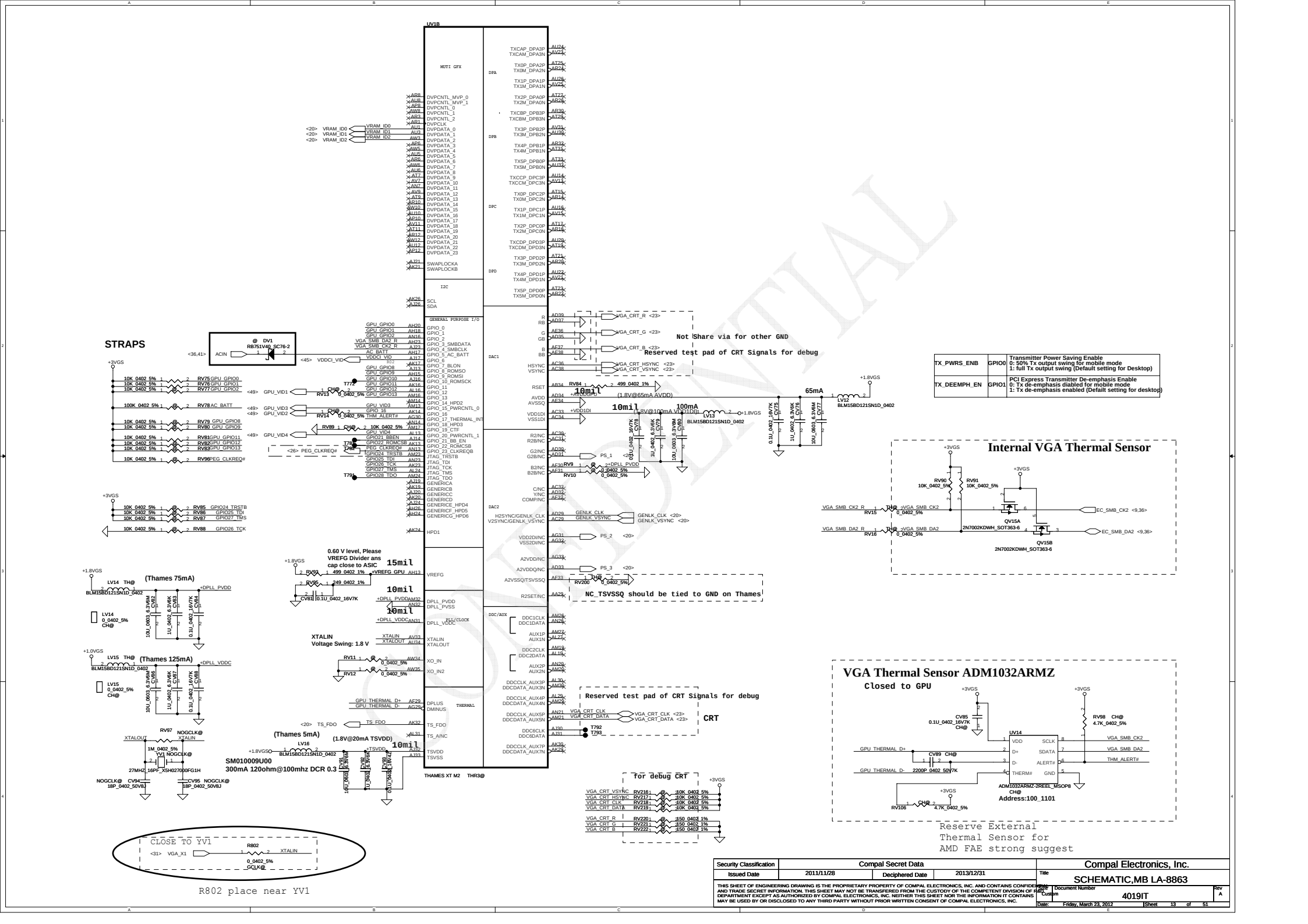

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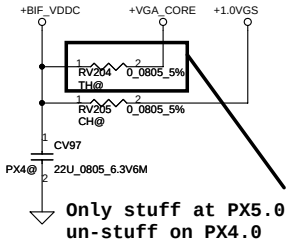
<25,26,44,49> PXS_PWREN — PXS_PWREN — RV102 1 @ 2 0_0402_5% — PX_MODE — PX_MODE <45,49>

for PX5.0

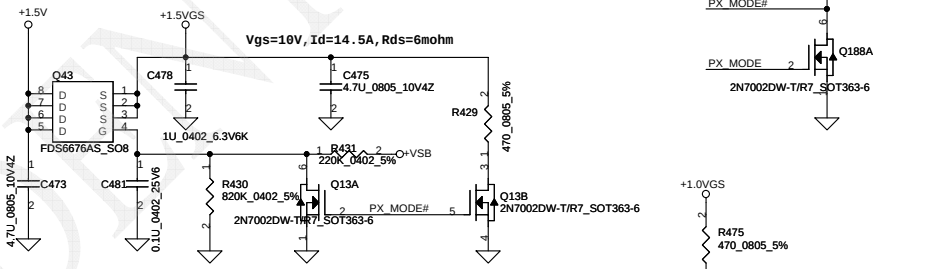
PX_MODE=1 for Normal Operation

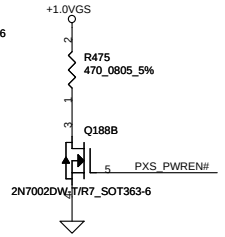
PX_MODE=0 to shut down VDDR3, PCIE_VDDC, 1.5VGS and 1.8VGS power rails



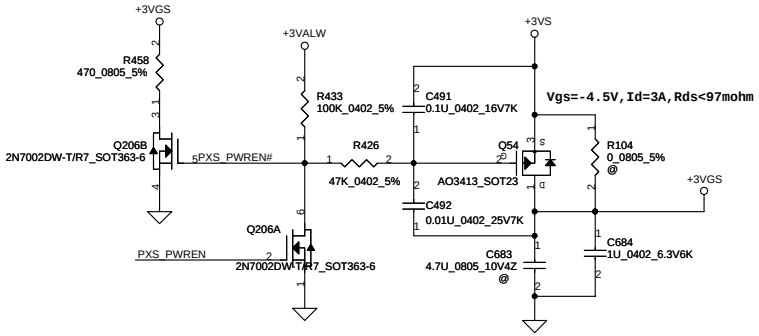
Only stuff at PX5.0 and Thames XT, un-stuff on PX4.0

+1.5V to +1.5VGS





+3VS to +3VGS



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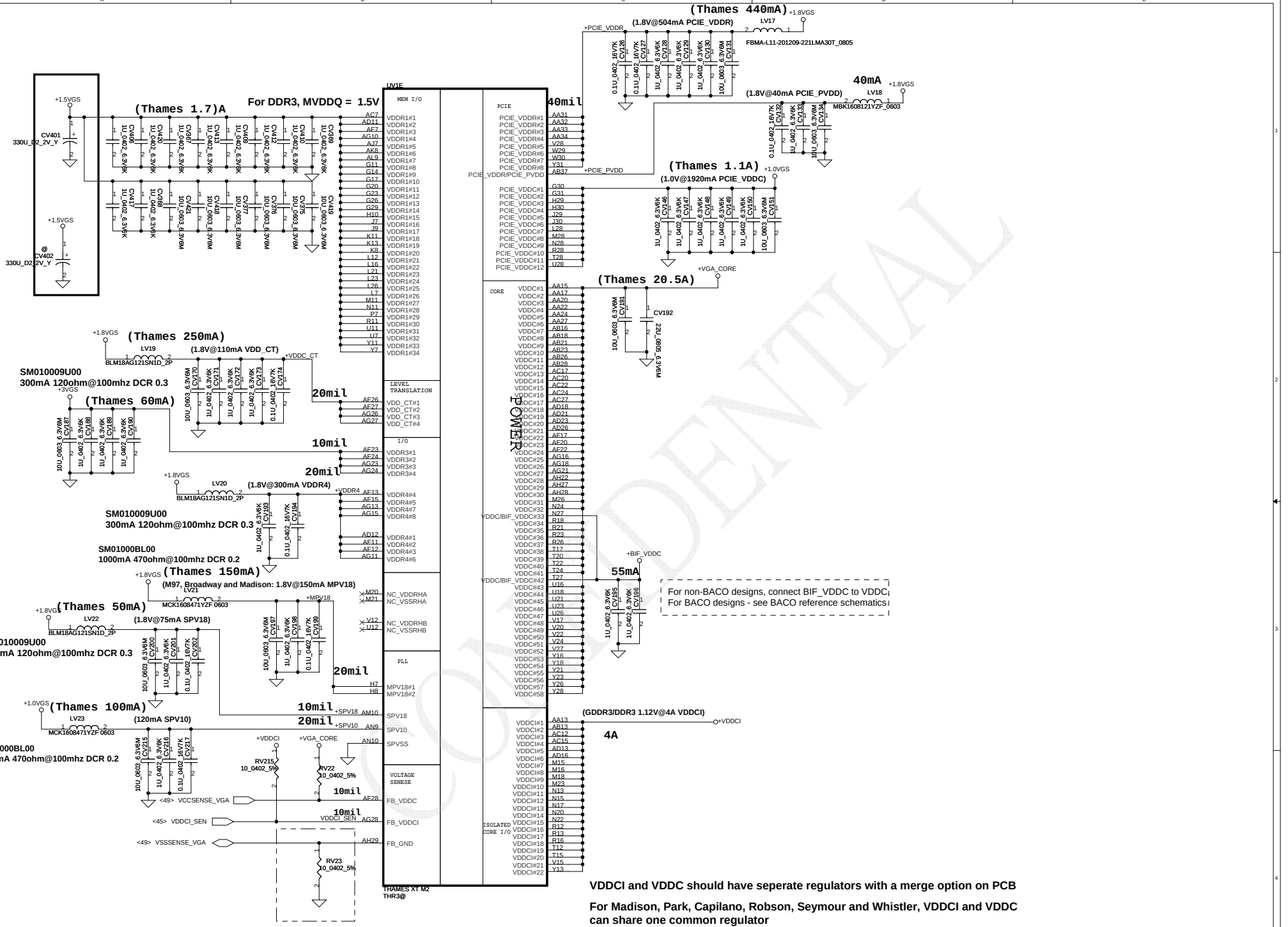

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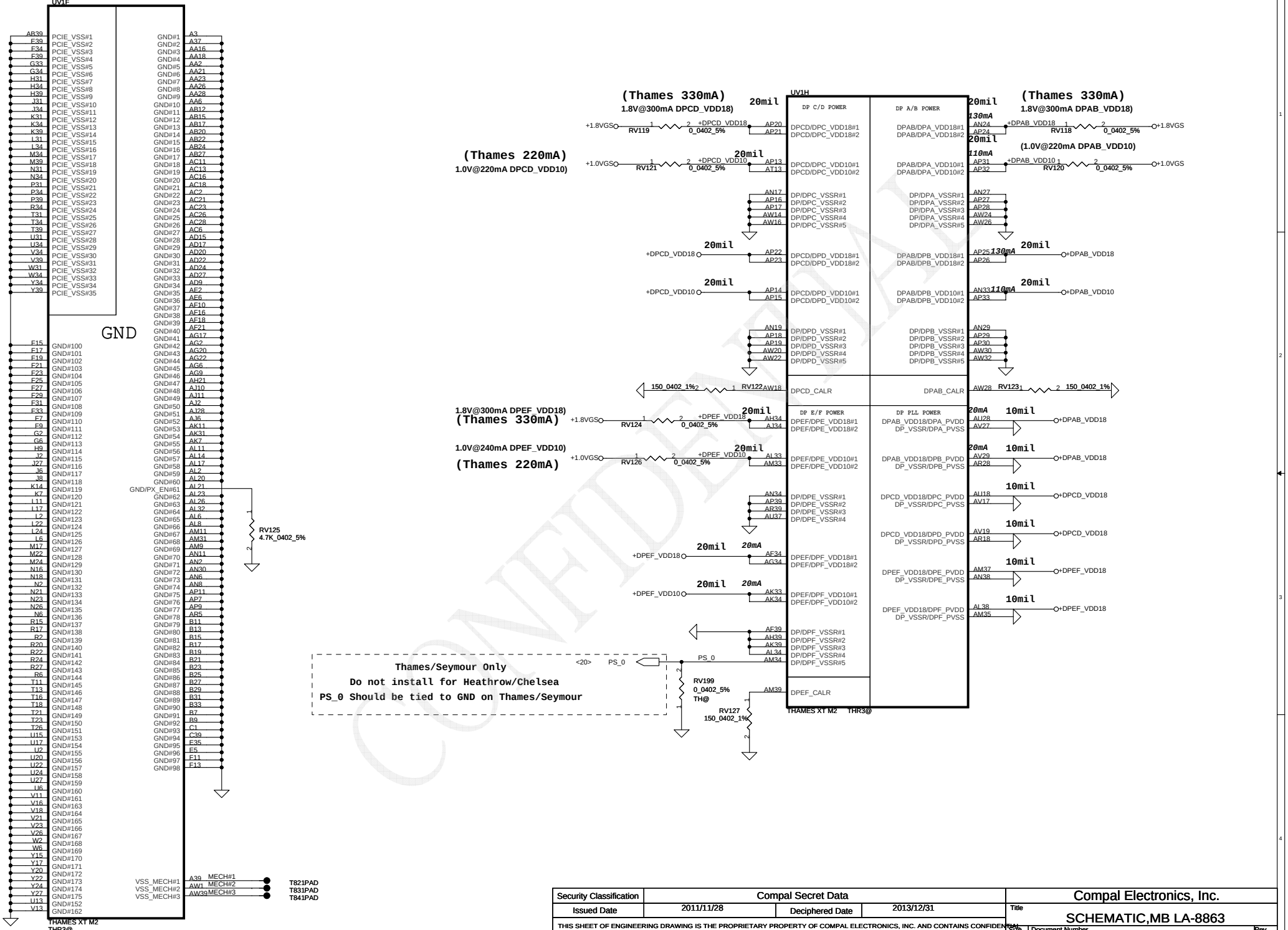

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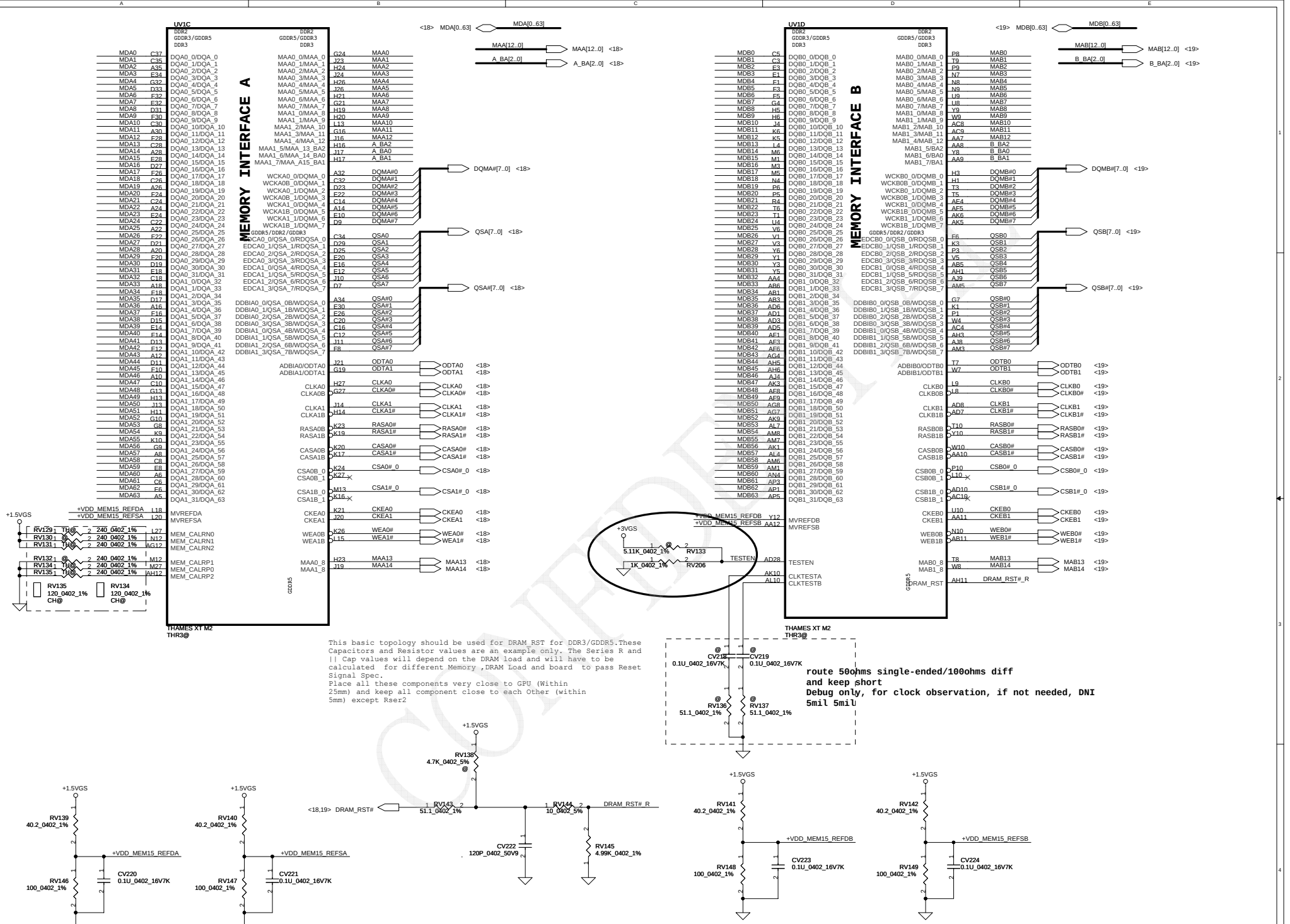

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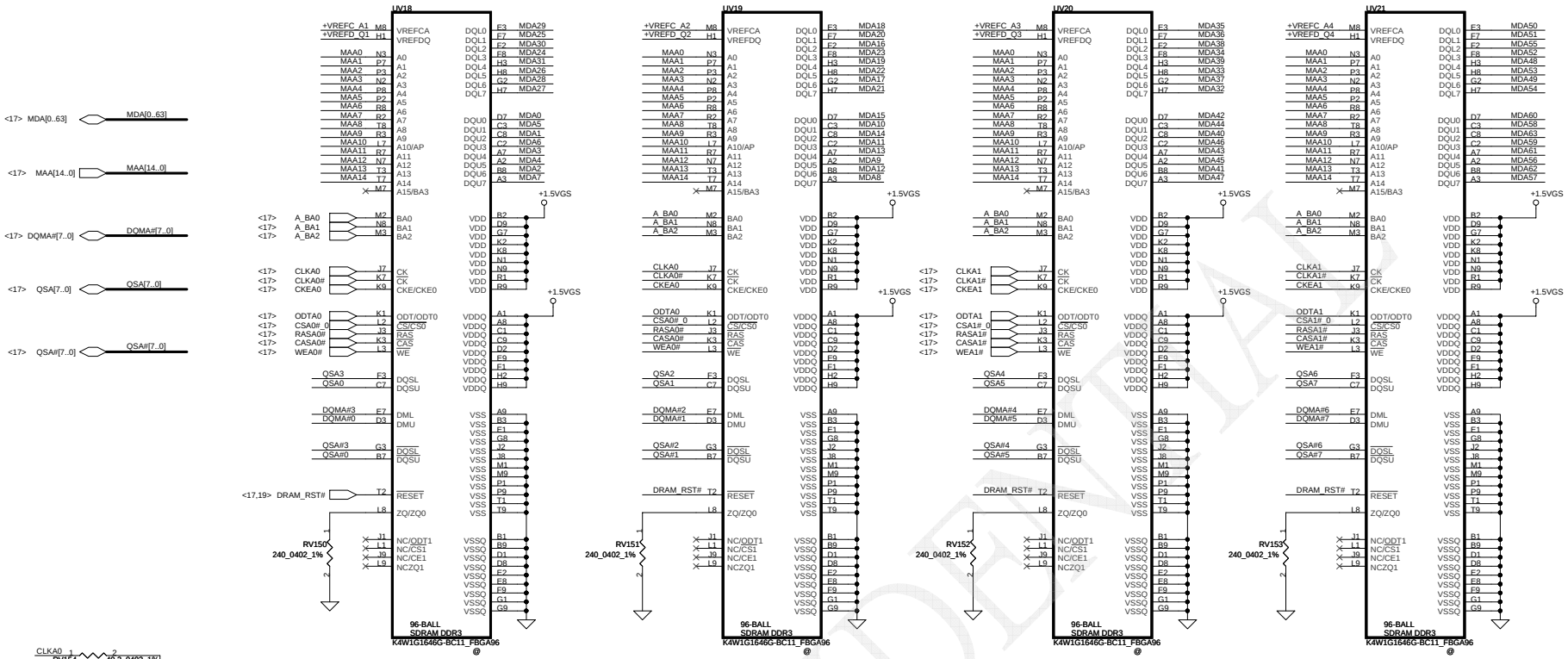
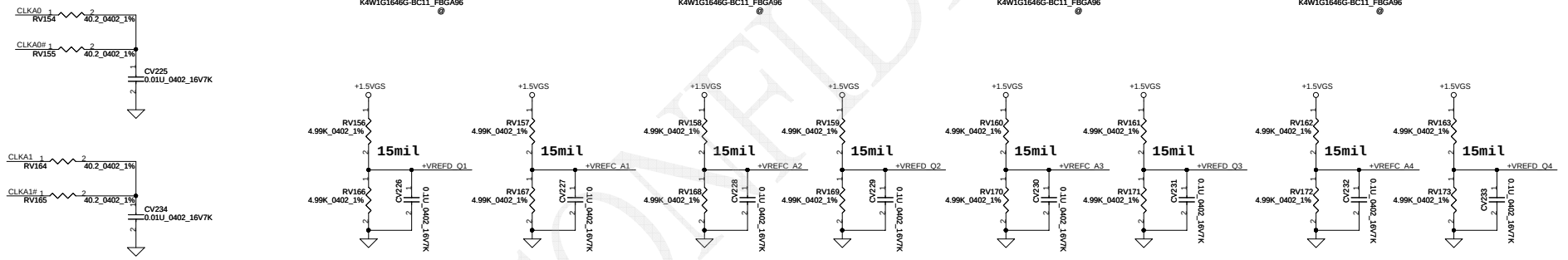
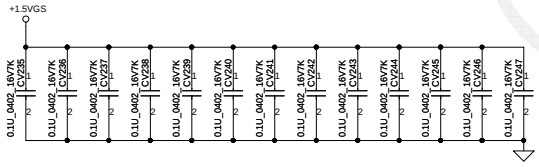
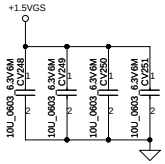
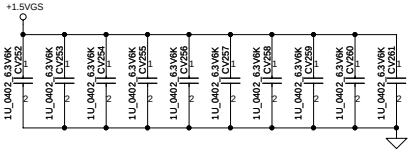
CHANNEL A: 512MB/1024MB DDR3

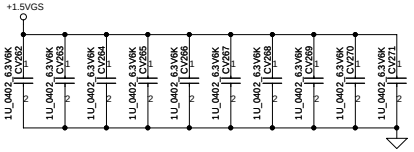












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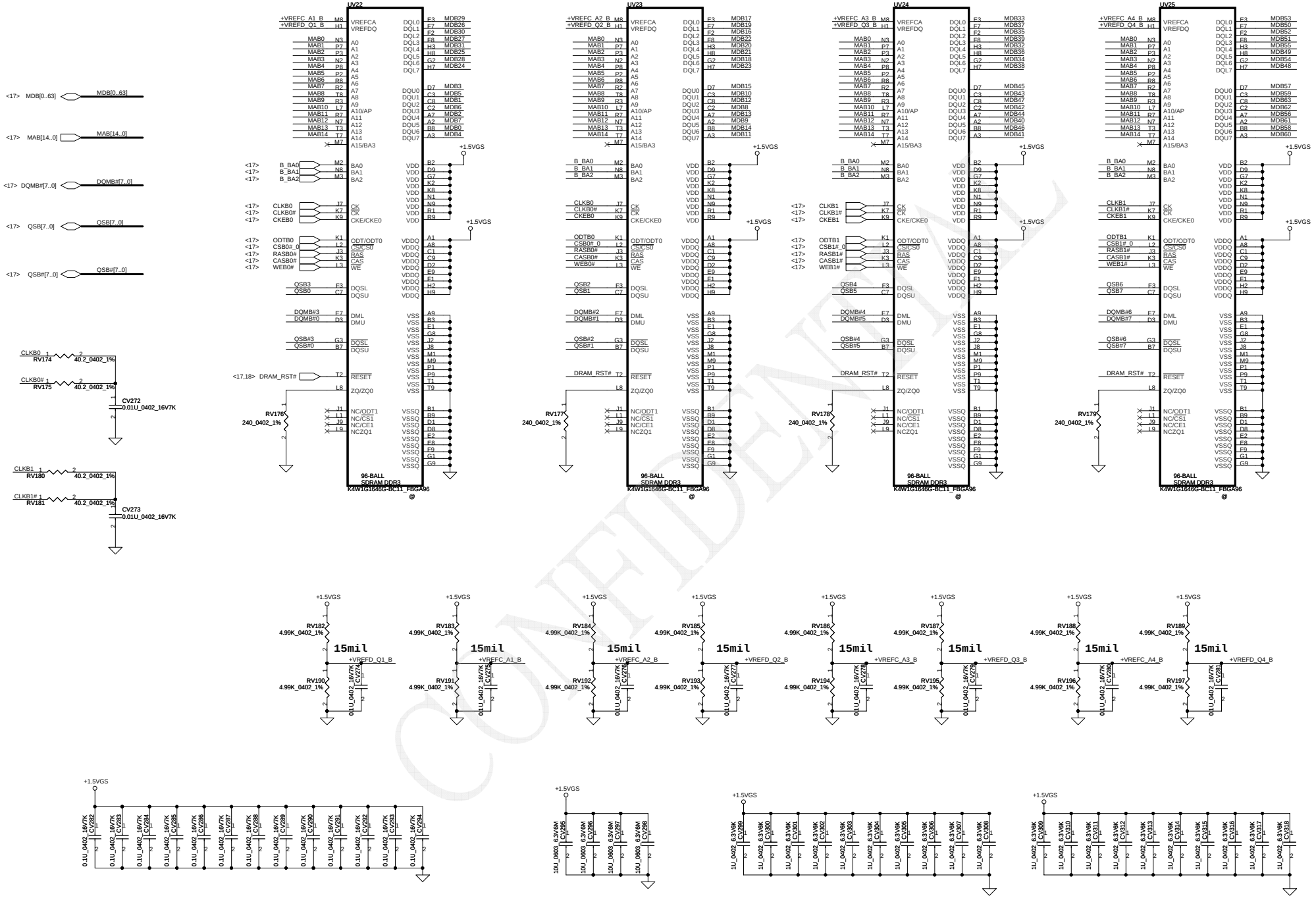
CHANNEL B: 512MB/1024MB DDR3



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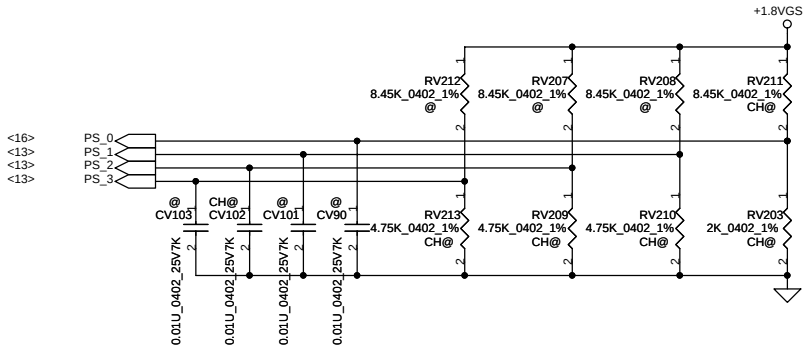
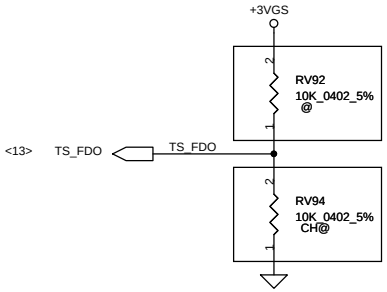
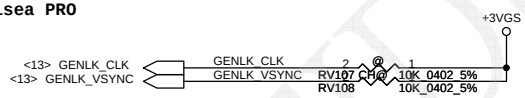
	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0	1 1	0 0 1	NC	8.45k	2k
PS_1	1 1	0 0 0	NC	NC	4.75k
PS_2	0 0	0 0 0	680 nF	NC	4.75k
PS_3	1 1	0 0 0	NC	NC	4.75k







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

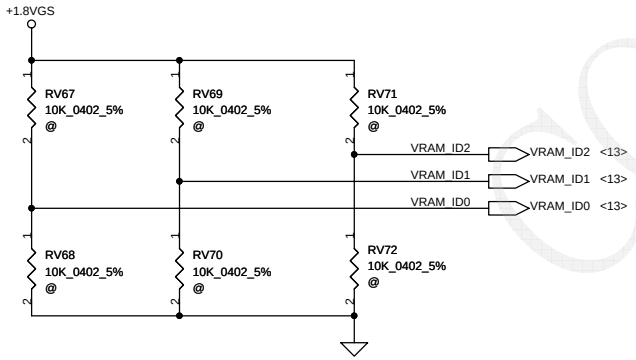
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	STRAPS	Conventional Pin Strap Equivalent	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
PS_0[3:1]	ROMIDCFG(2:0)	GPIO[13:11]	Memory aperture size select **256MB: 0 0 1**	0 0 1
PS_0[4]	N/A	GENLK_VSYNC	Must be 1 at rest. (Chelsea PRO)	1
PS_1[1]	STRAP_BIF_ GEN3_EN_A	GPIO2	PCIE Gen3 capability **0: 2.5GT/s** **1: 5GT/s**	0
PS_1[2]	STRAP_BIF_ CLK_PM_EN	GPIO8	PCIE clock power management capability.	0
PS_1[3]	N/A	GENLK_CLK	Must be 0 at rest. (Chelsea PRO)	0
PS_1[4]	TX_PWRS_ENB	GPIO0	PCIE full TX output swing **0: Half swing** **1: Full swing**	1
PS_1[5]	TX_DEEMPH_EN	GPIO1	PCIE transmitter de-emphsis enable **0: Disable** **1: Enable**	1
PS_2[1] PS_2[2]	N/A	N/A	Reserved	N/A
PS_2[3]	BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM **0: Disable** **1: Enable**	0
PS_2[4]	VGA DIS	GPIO9	VGA disable **0: Enable** **1: Disable**	0
PS_2[5] PS_3[3:1]	N/A	N/A	Reserved	N/A
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN _PINSTRAP[0] AUD_PORT_CONN _PINSTRAP[1] AUD_PORT_CONN _PINSTRAP[2]	N/A	Audio-capable display outputs 0 0 0 All endpoints are usable 1 1 1 No usable endpoints.	1 1 1
AUD[1] AUD[0]	HSYNC VSYNC		AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8



VRAM Straps

	Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
64MX16 (1G)	H5TQ1G63DFR-11C **Hynix 1GB SA000041S20**	**RV68** 0	**RV70** 0	**RV72** 0
*64MX16 (1G)	K4W1G1646G-BC11 **Samsung 1GB SA00004GS00**	**RV67** 1	**RV70** 0	**RV72** 0
128M16 (2G)	H5TQ2G63BFR-11C **Hynix 2GB SA00003YO00**	**RV68** 0	**RV69** 1	**RV72** 0
*128M16 (2G)	K4W2G1646C-HC11 **Samsung 2GB SA000047Q00**	**RV67** 1	**RV69** 1	**RV72** 0

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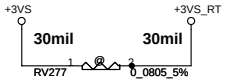
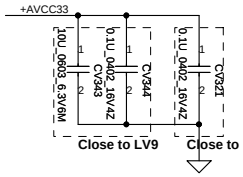
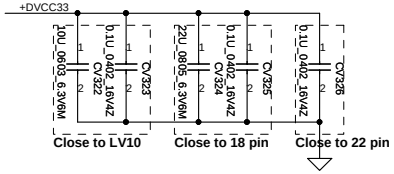
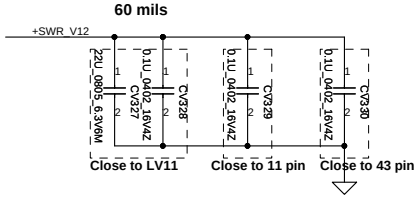
Power Consumption:

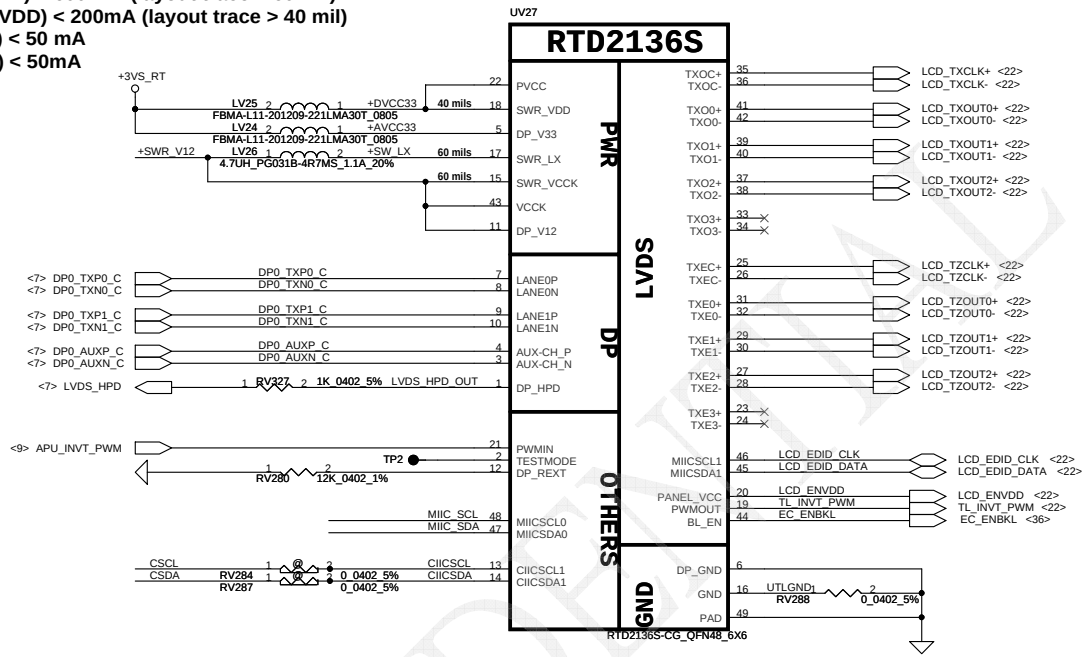
Pin5 (DPV33) < 20mA
Pin 11 (DPV12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA

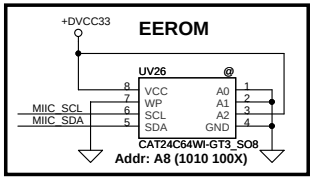


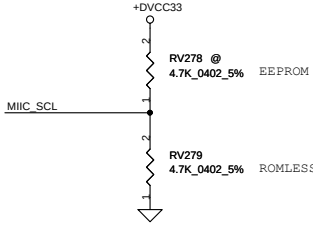


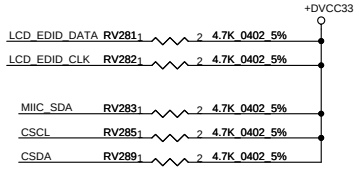


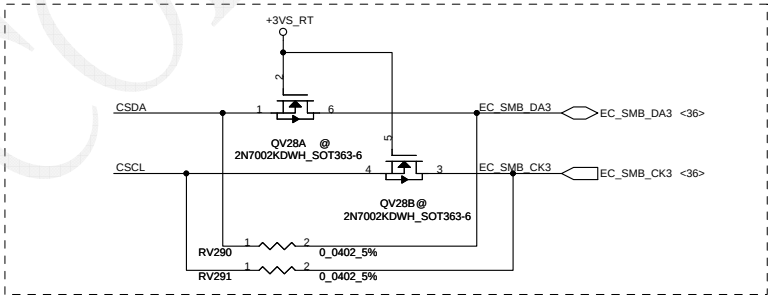


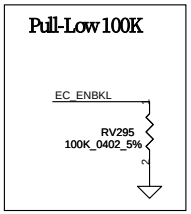












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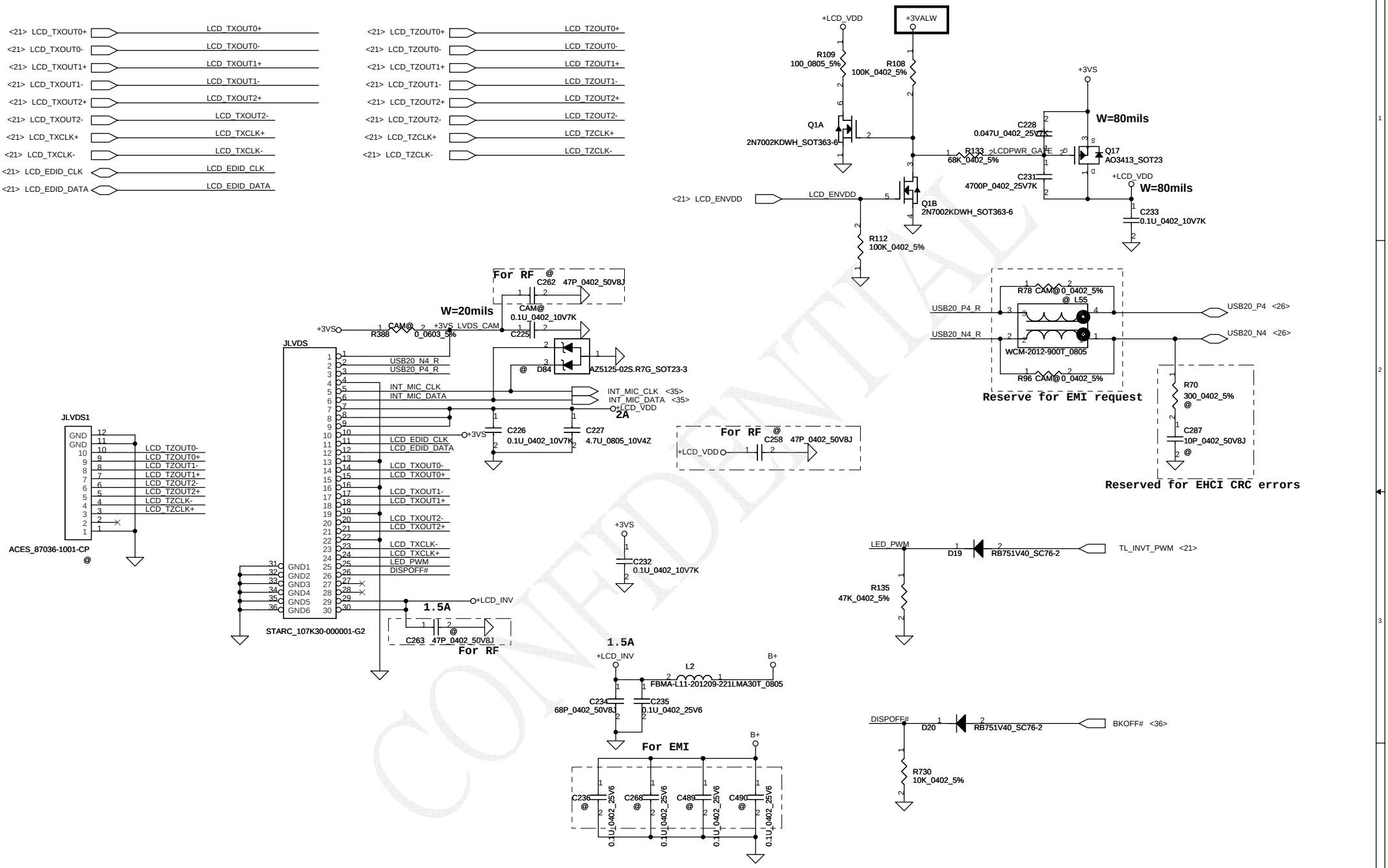

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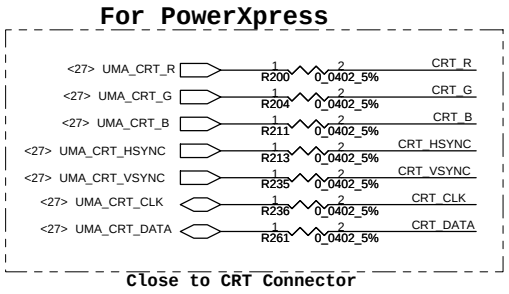
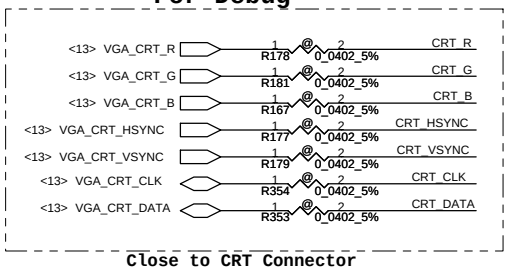
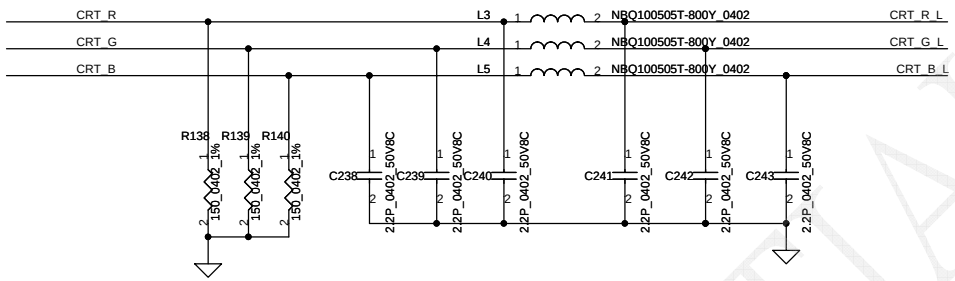
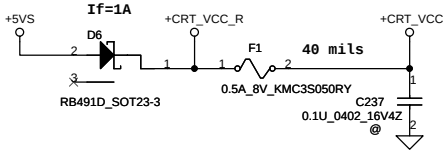
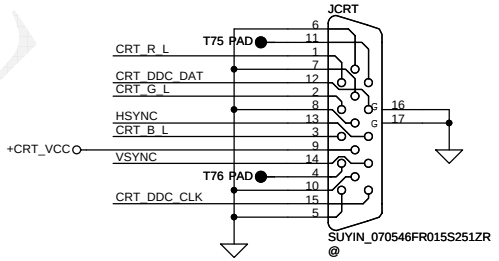
CRT CONNECTOR

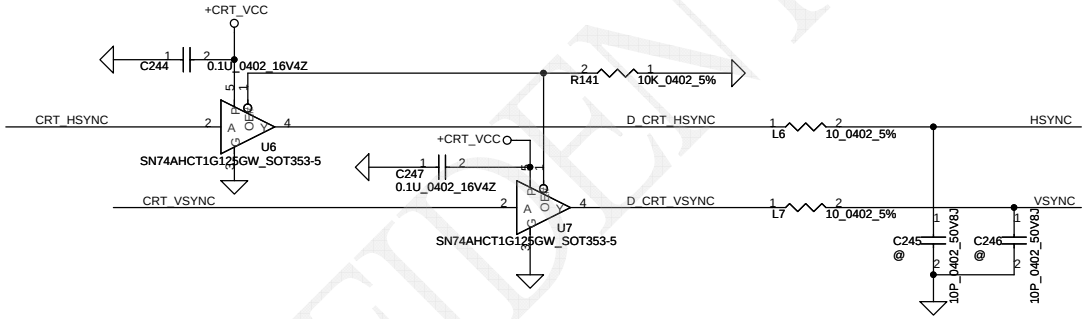


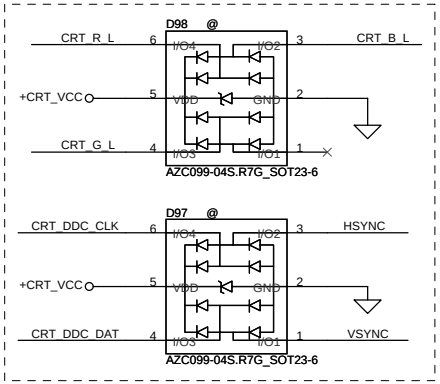




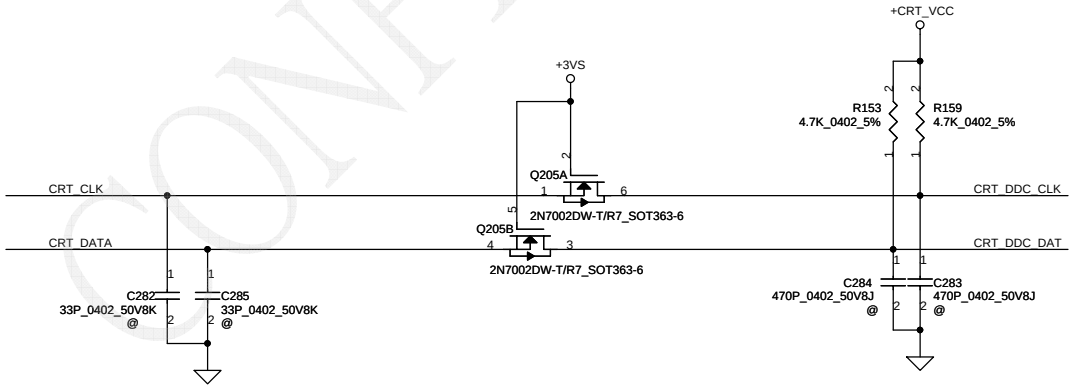








2/9: Add for ESD request



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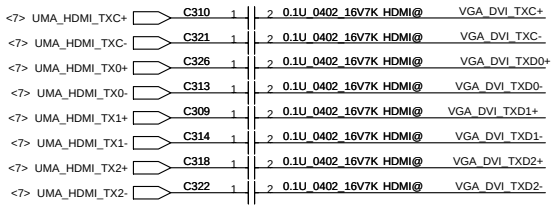
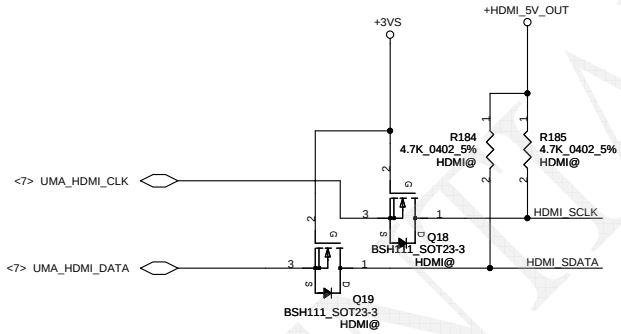
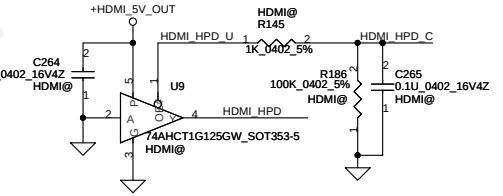
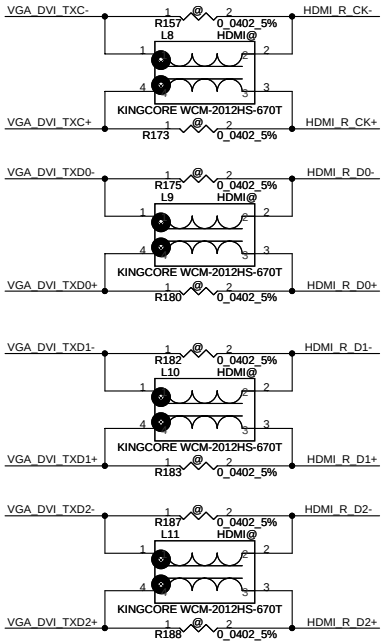
OE#	A	Y
L	L	L
L	H	H
H	X	Z

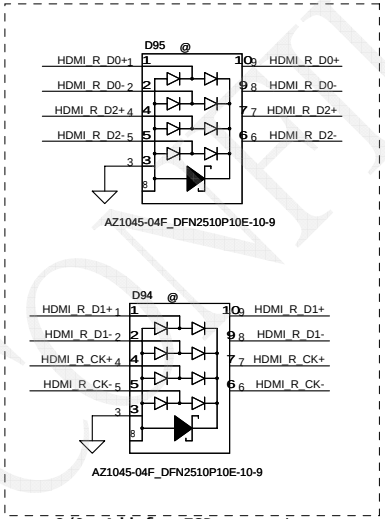
Change R184 and R185 from 2K to 4.7K for HDMI detect issue on preMP











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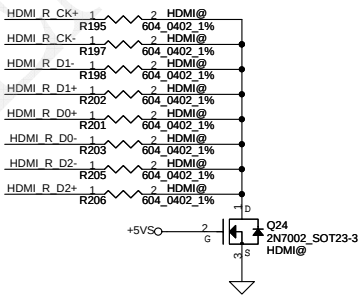
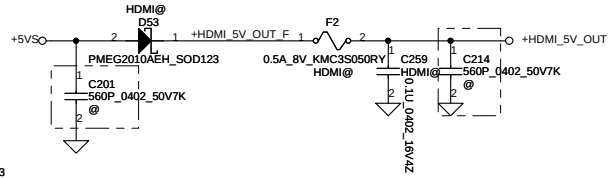
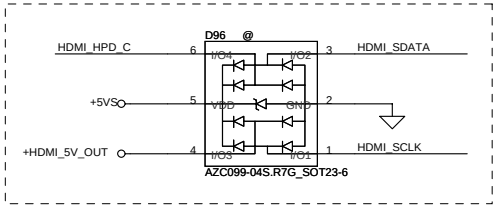


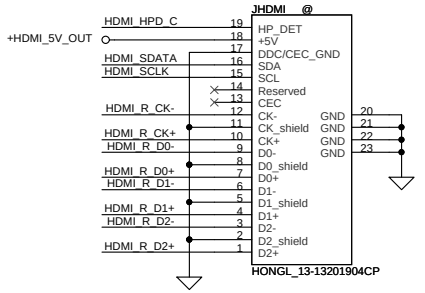
Add C201 and C214 for EMI request on PVT





2/9: Add for ESD request

HDMI Connector



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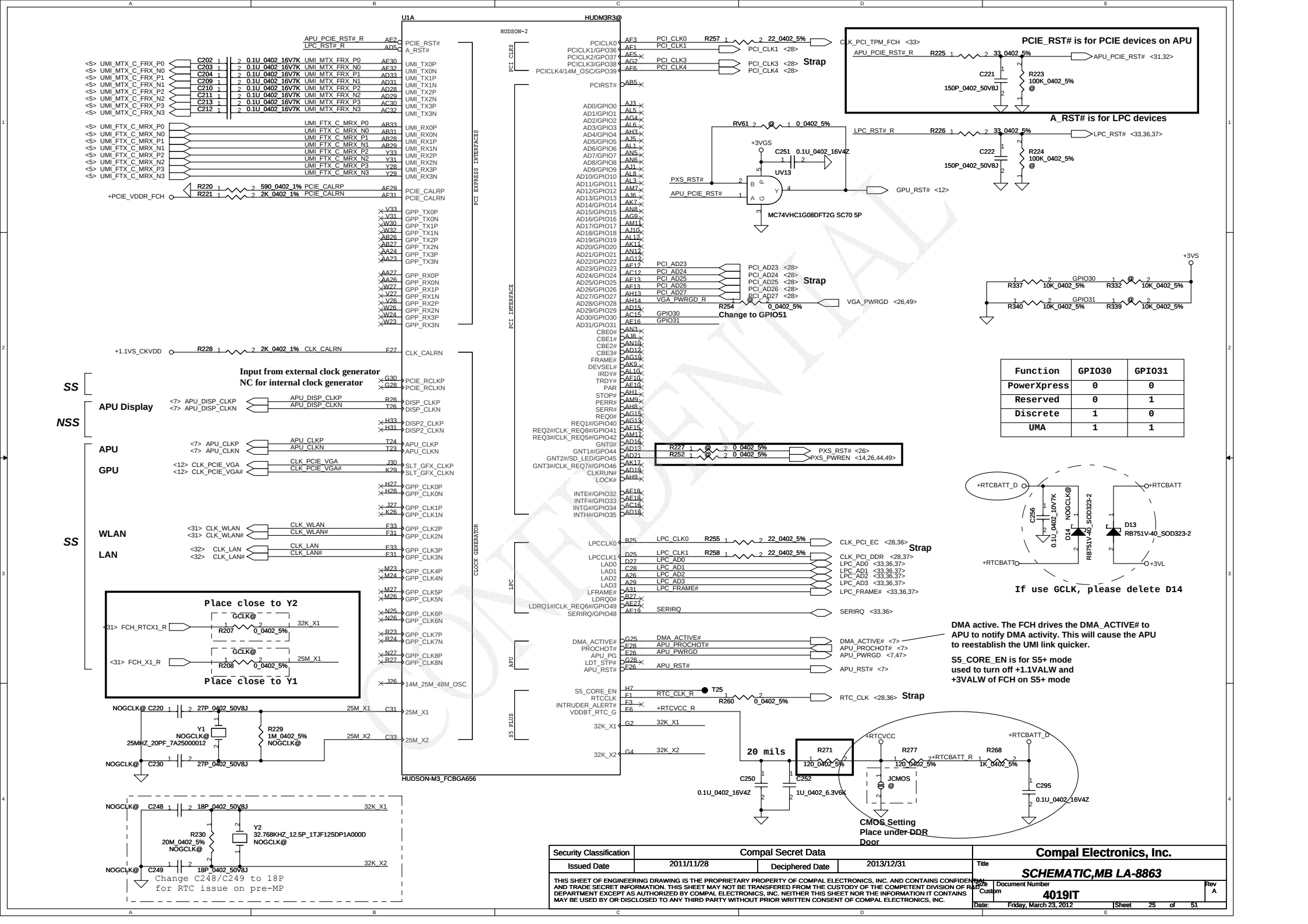

Function	GPIO30	GPIO31
PowerXpress	0	0
Reserved	0	1
Discrete	1	0
UMA	1	1

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PCIE_RST2# is for PCIE devices on FCH

U1D

HUDM3R3@

HUDSON-2

For FCH internal debug use
(Internal 10K pull-down)

+3VALW_FCH

R273 2.2K_0402_5% TEST0
R274 2.2K_0402_5% TEST1
R275 2.2K_0402_5% TEST2

SM Bus 0-->S0 PWR domain
SM Bus 1-->S5 PWR domain
(for ASF device only)

VGA_PD: Support CRT power saving
L: MLDAC power on
H: MLDAC power off

USB_OC1# is for left USB3.0 ports
USB_OC0# is for right USB2.0 ports

R295 0_0402_5%
R113 100K_0402_5%

R320 33_0402_5% HDA_BITCLK
R321 33_0402_5% HDA_SDOUT
R322 33_0402_5% HDA_SYNC
R323 33_0402_5% HDA_RST#

R326 10K_0402_5%
R328 10K_0402_5%
R338 10K_0402_5%
R343 10K_0402_5%

R329 11.8K_0402_1%

R330 1K_0402_1%
R334 1K_0402_1%

Hudson-M2/M3
OHCI (DEV-20, FUN-5)

Hudson-M2
OHCI (DEV-22, FUN-0)
EHCI (DEV-22, FUN-2)

Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)

USB 3.0-Left2
USB 3.0-Left1

Hudson-M2/M3
OHCI (DEV-19, FUN-0)
EHCI (DEV-19, FUN-2)

Int. Camera
WLAN (BT)
Cardreader
<Support Wakeup>
USB-Right2
USB-Right1
(Debug Port)

Hudson-M2/M3
OHCI (DEV-18, FUN-0)
EHCI (DEV-18, FUN-2)

Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)

SM Bus 2-->S5 PWR domain

Strap

Place R425 and C363
close to FCH for ESD

R425 0_0402_5%
C363 0.1U_0402_16V4Z

R312 10K_0402_5%
R311 10K_0402_5%

Q32A
2N7002DW-T/R7_SOT363-6

Q5530A
2N7002KDWH_SOT363-6

Q5530B
2N7002KDWH_SOT363-6

R216 10K_0402_5%

HUDSON-M3_FCBGA656

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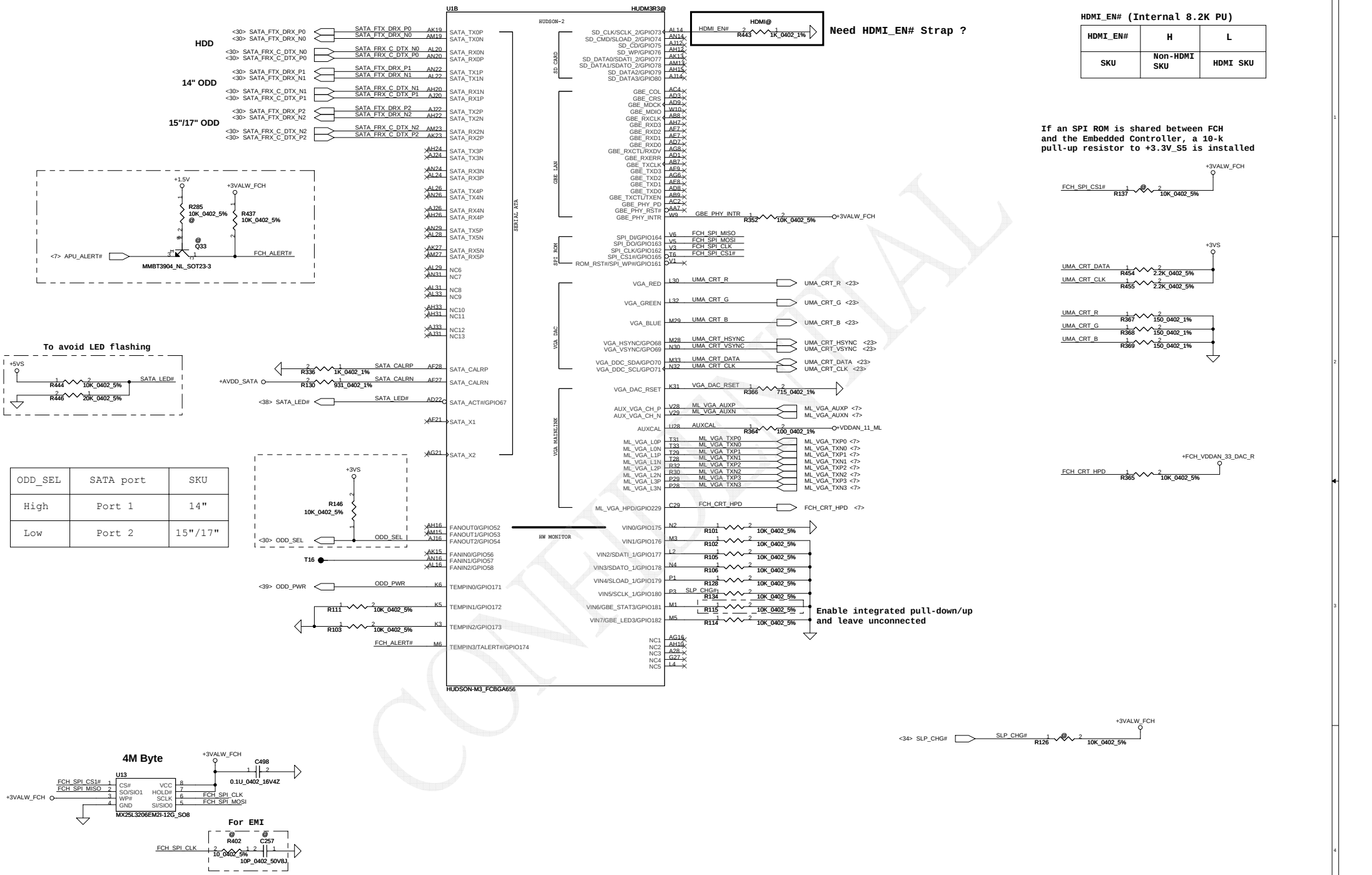

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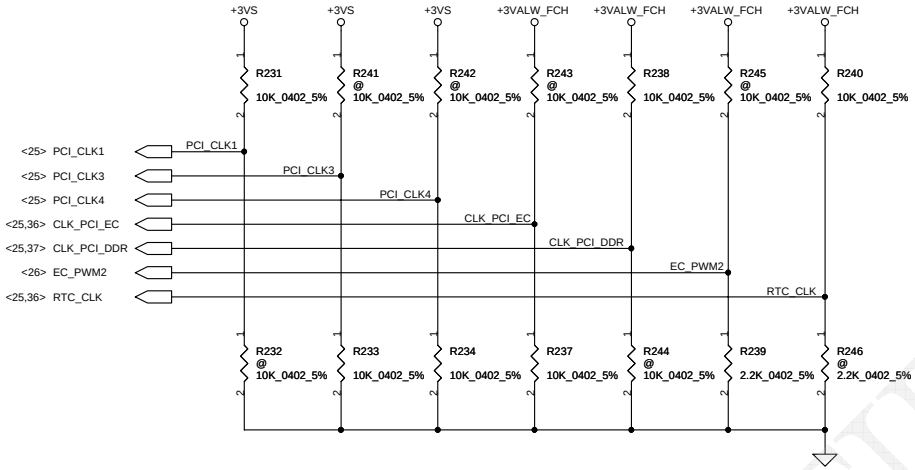
STRAP PINS

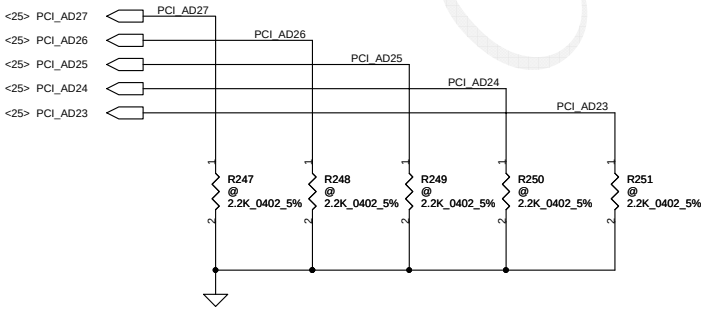
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



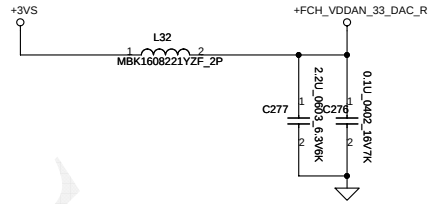
DEBUG STRAPS

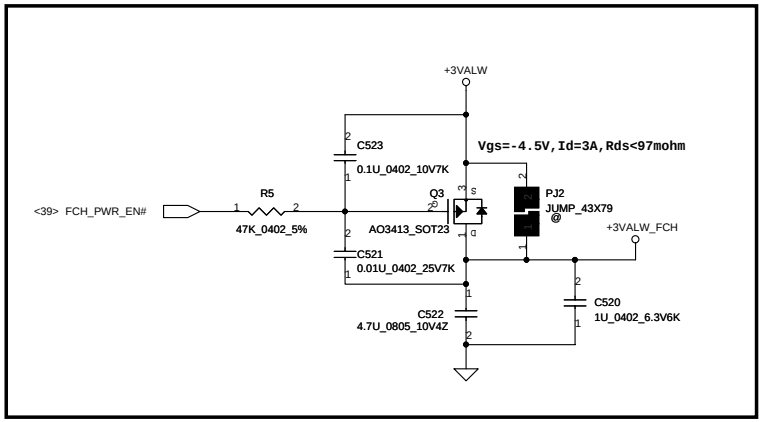
FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



CRT Power Down Circuit





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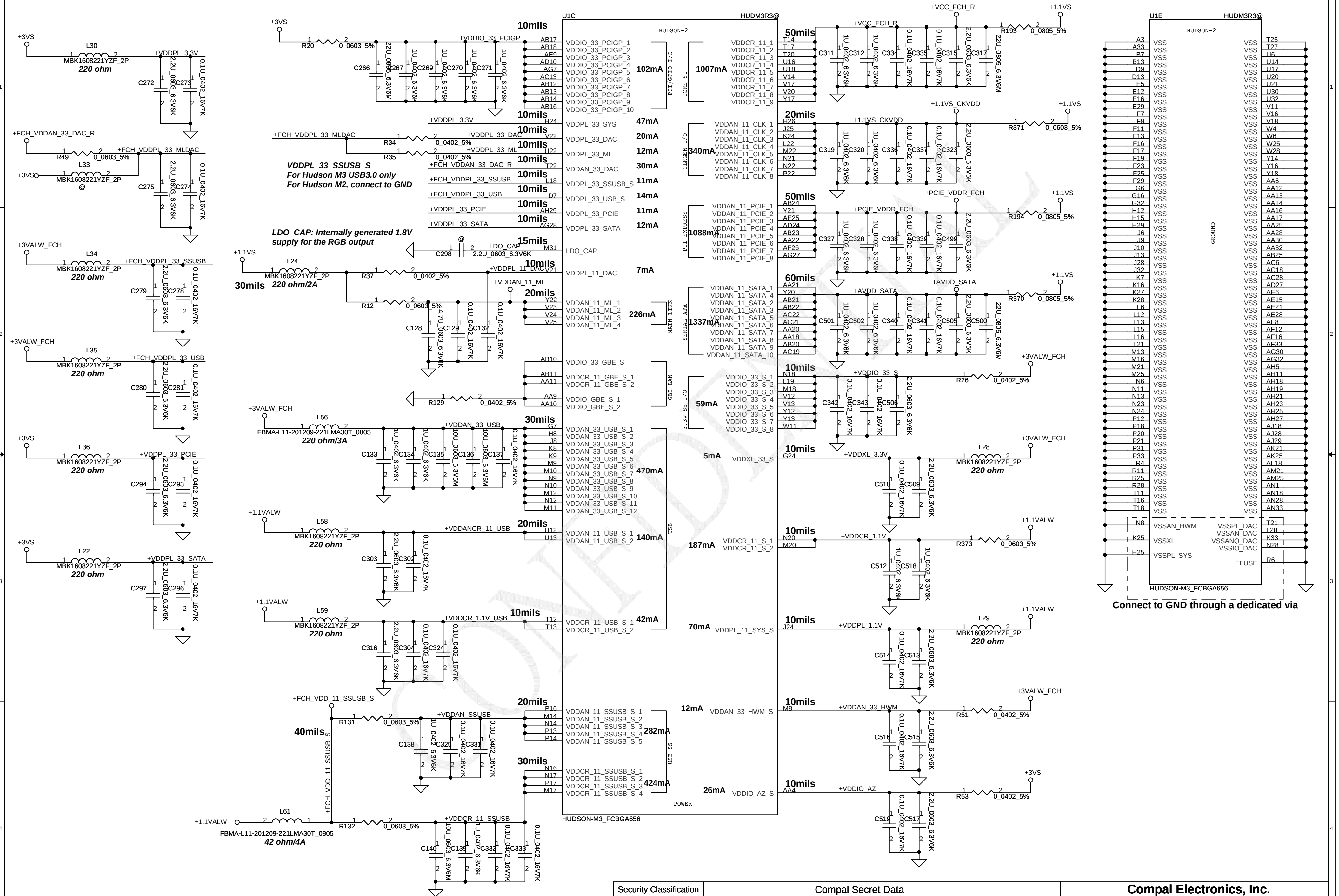

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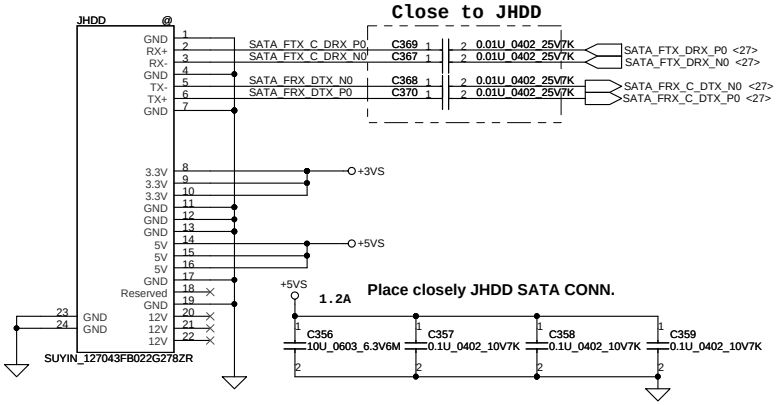
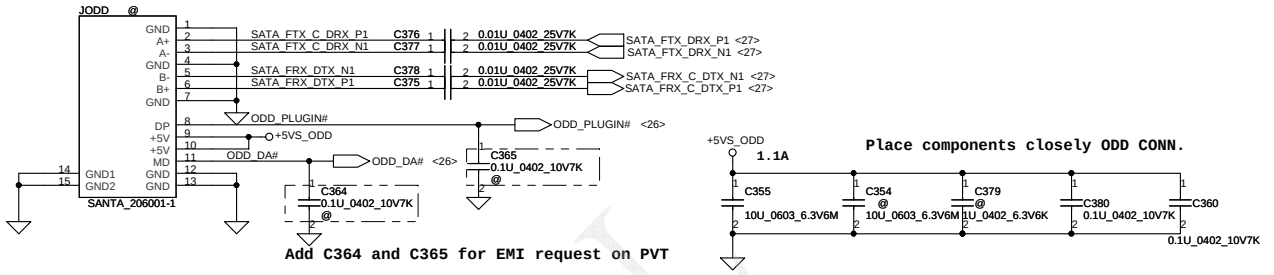
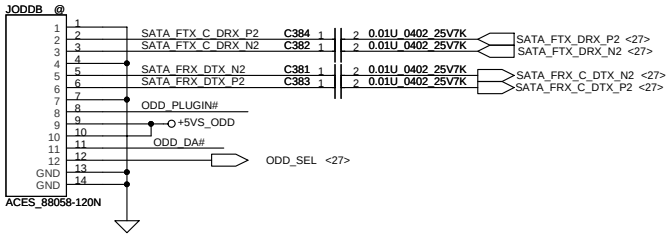
SATA HDD Conn.



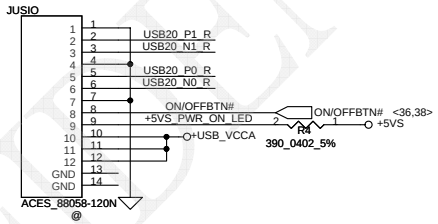
SATA ODD Conn

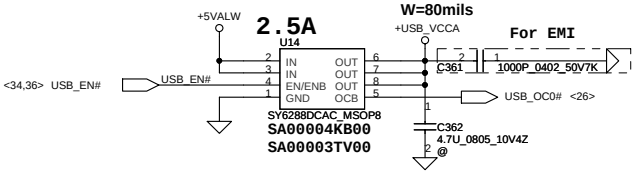


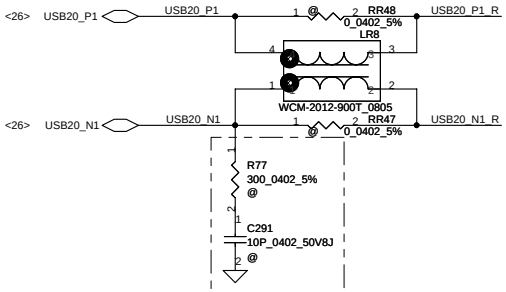
SATA ODD Conn (for 15"/17")

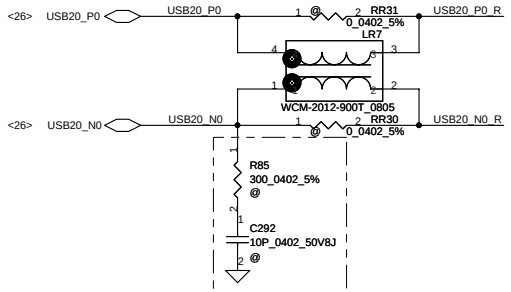


Power Button & RUSB connector









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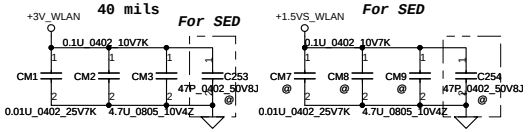
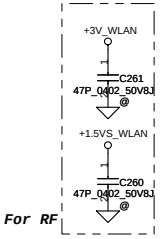
Slot 1 Half PCIe Mini Card-WLAN

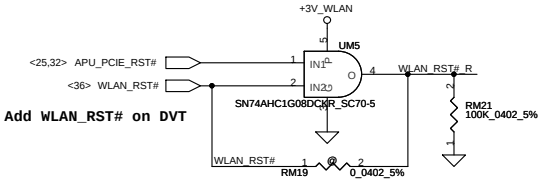




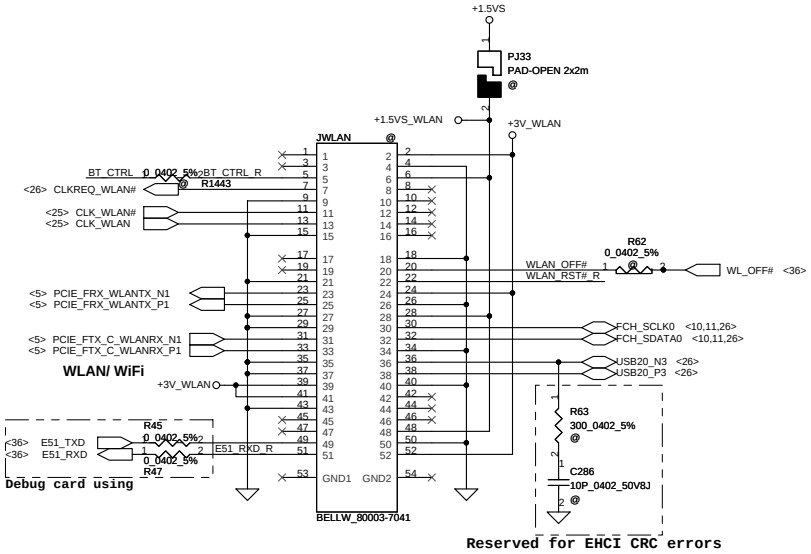
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L

For isolate BT_CTRL and Compal Debug Card.

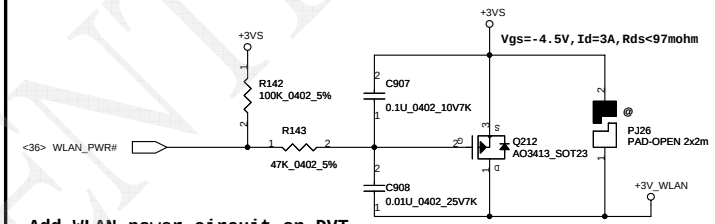


Add WLAN_RST# on DVT



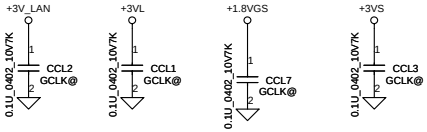
Reserved for EHCI CRC errors

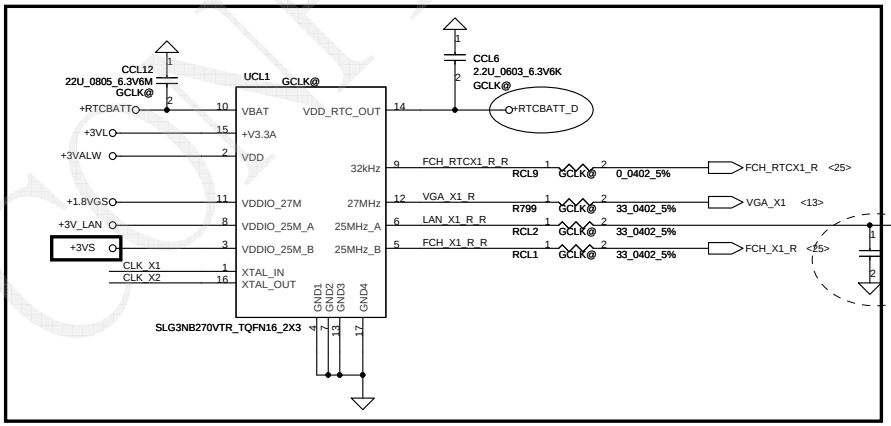
+3VALW TO +3V_WLAN



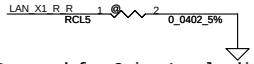
Add WLAN power circuit on DVT

Change to GCLK to SLG3NB270V
SA00005DP00 for 27MHz
for VGA



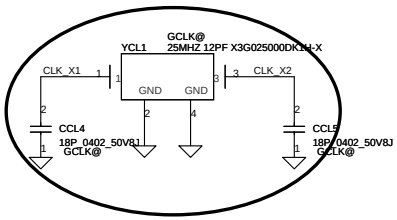


EMI request 11/06



Reserved for Swing Level adjustment
(Close GCLK side)

change part number to
SJ10000EF00



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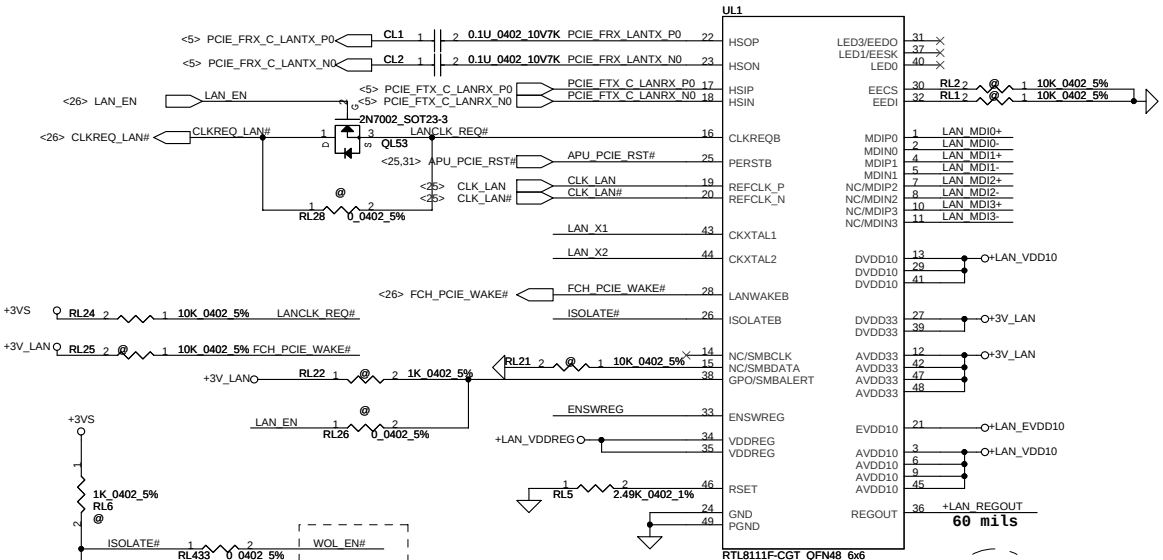
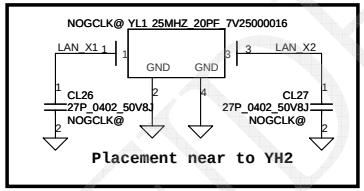
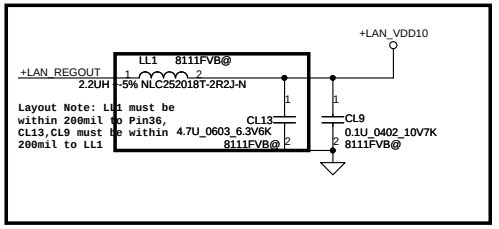
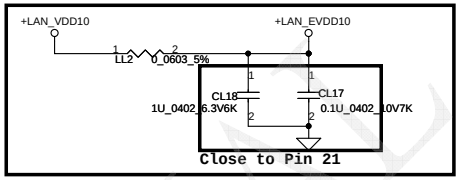


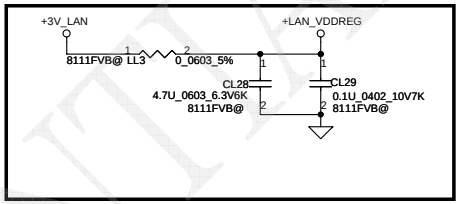
	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

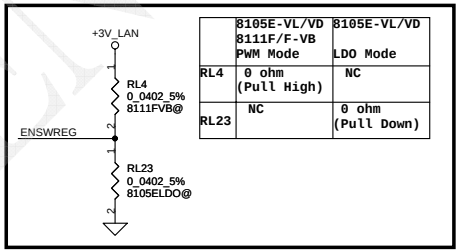
	RTL8105E	RTL8111E/F
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	NC	1K ohm PH



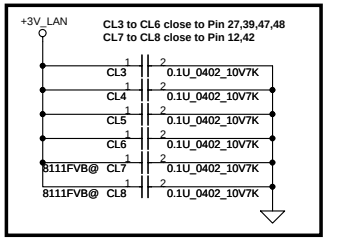


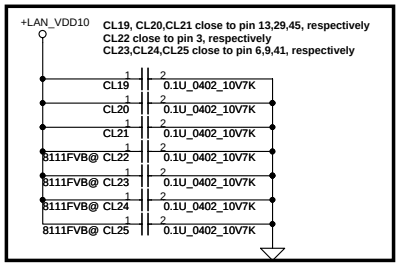




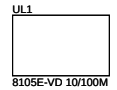


	8105E-VL/VD 8111F/F-VB PWM Mode	8105E-VL/VD LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)

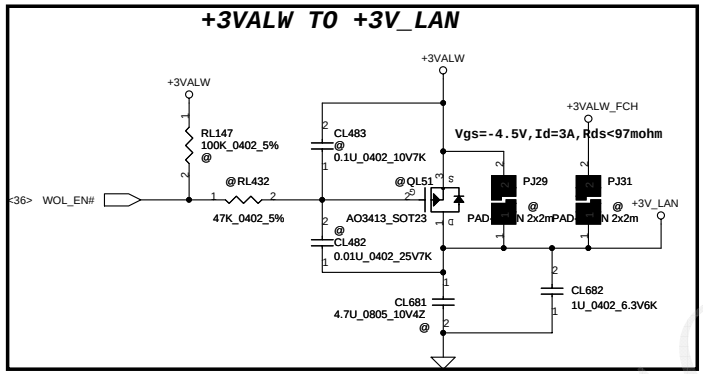




For P/N and footprint
Please place them to ISPD page



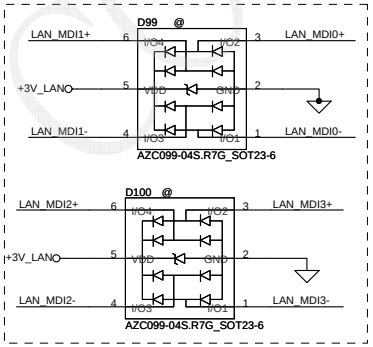
+3VALW TO +3V_LAN



+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

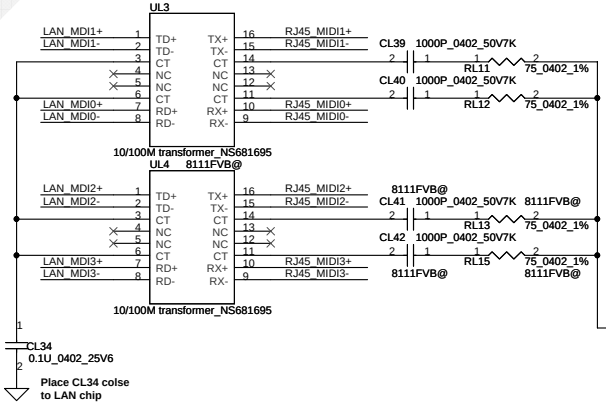
LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

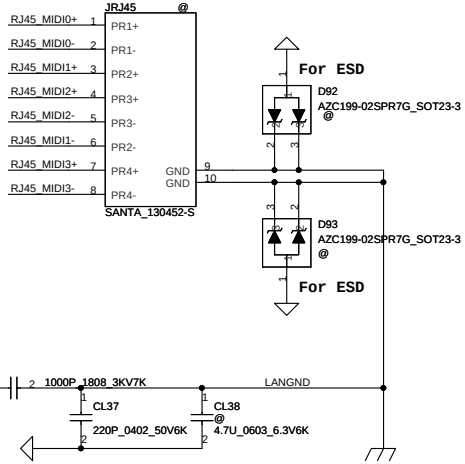


2/9: Add for ESD request

Main: SP050006N00
2nd: SP050005W00



LAN Conn.



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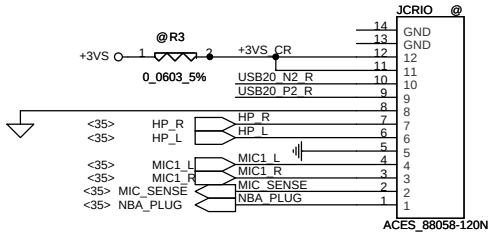
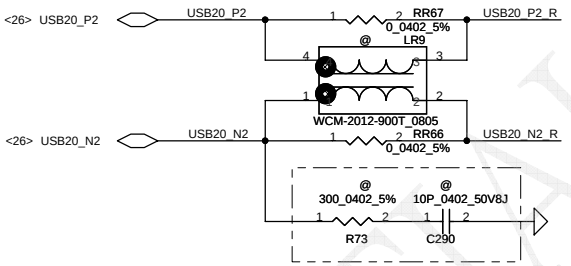
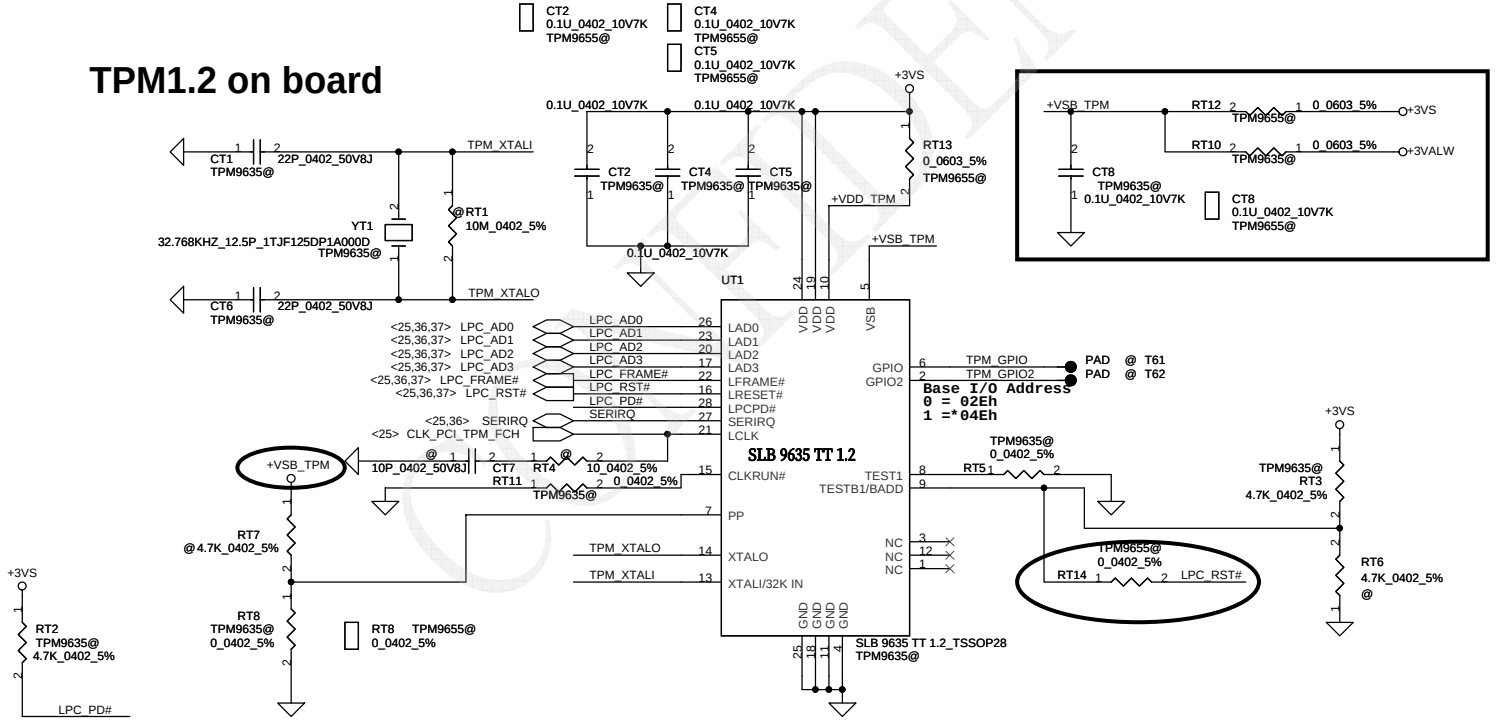
CardReader Conn.





Reserved for EHCI CRC errors

TPM1.2 on board



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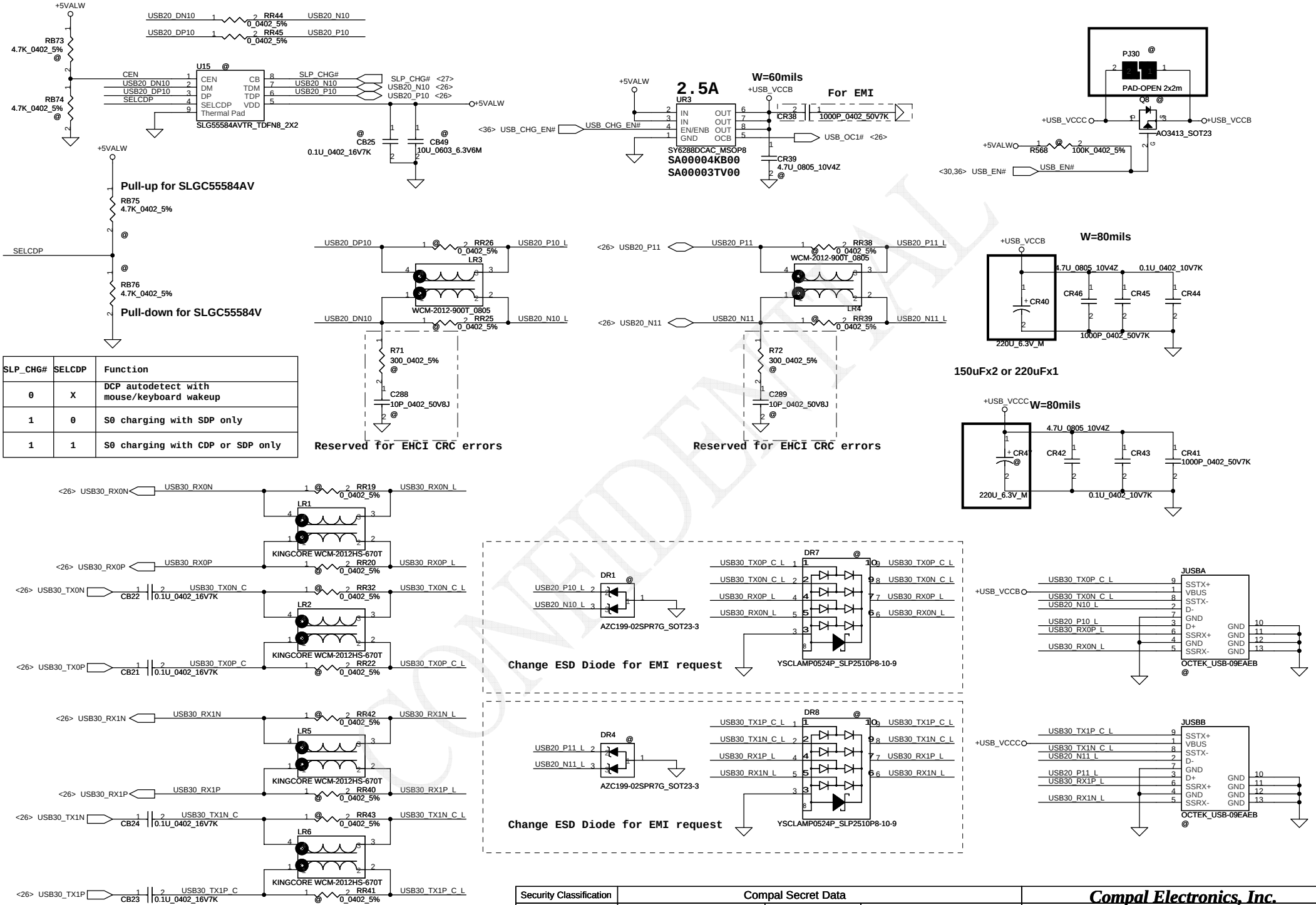

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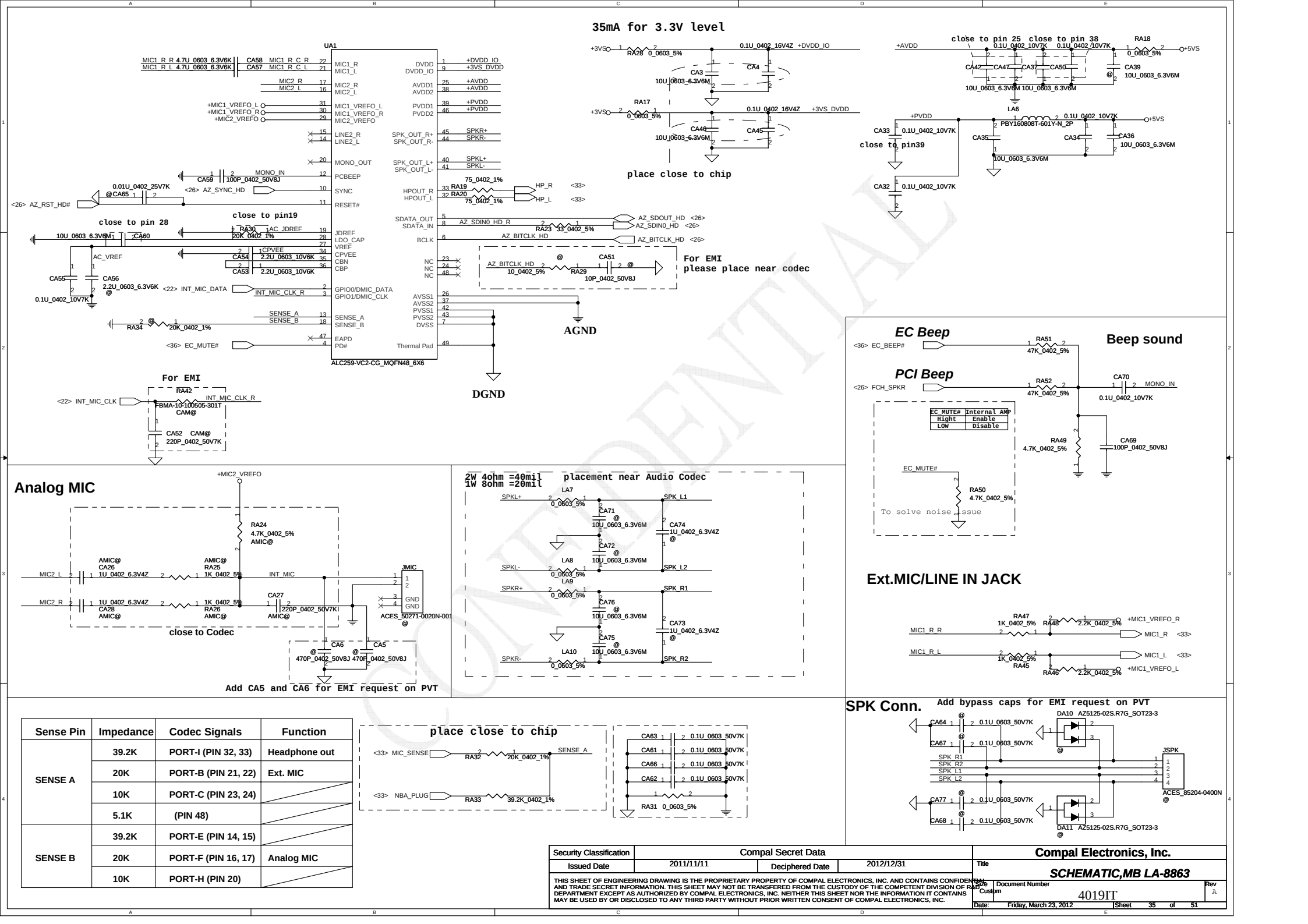

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Analog MIC
	10K	PORT-H (PIN 20)	

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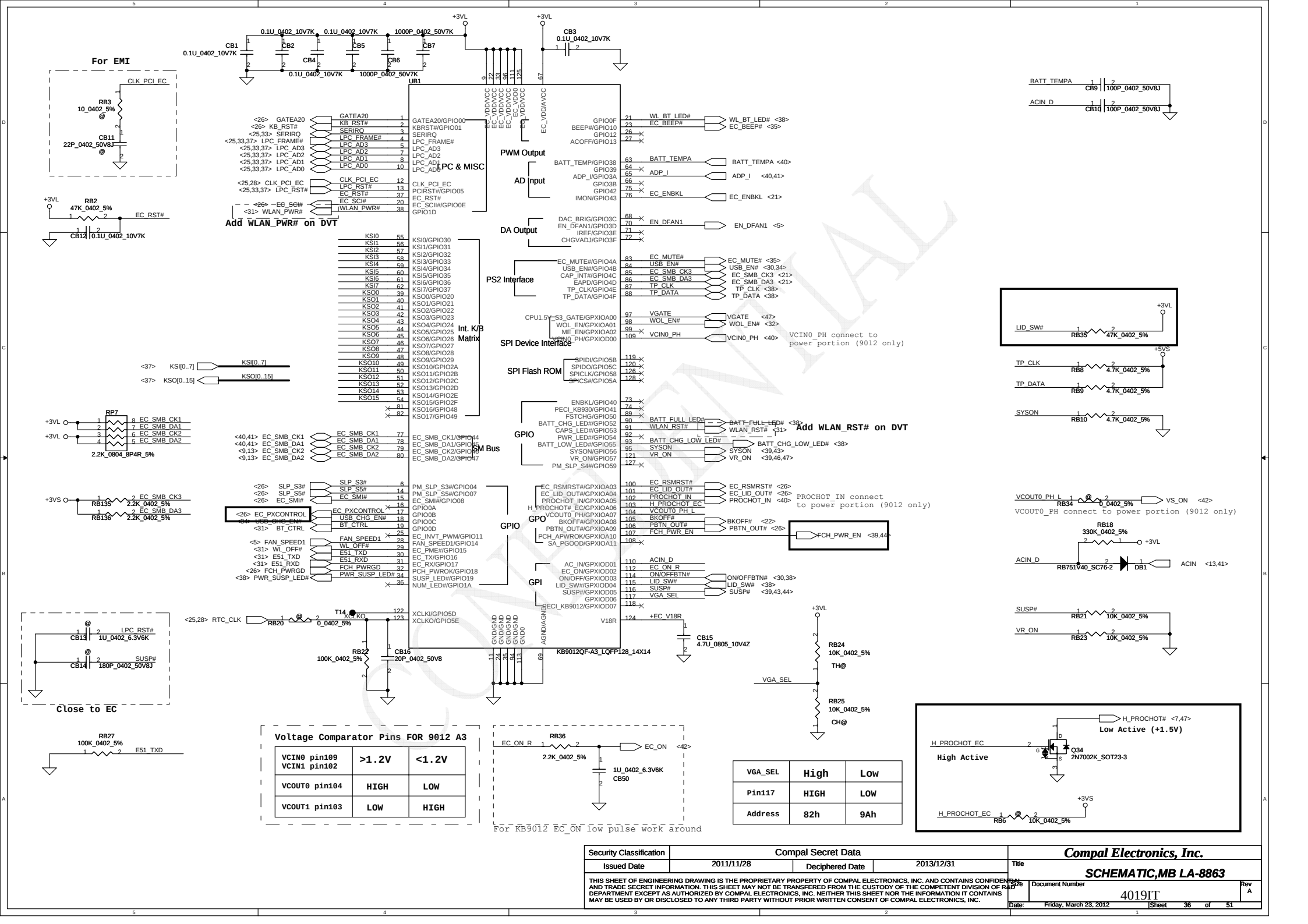

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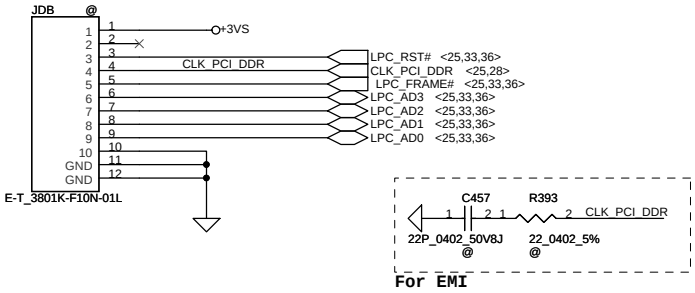
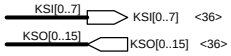
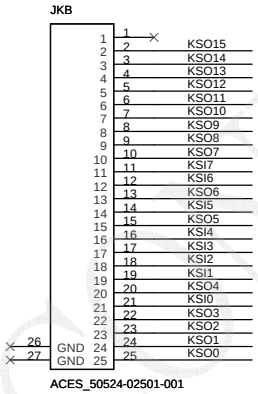
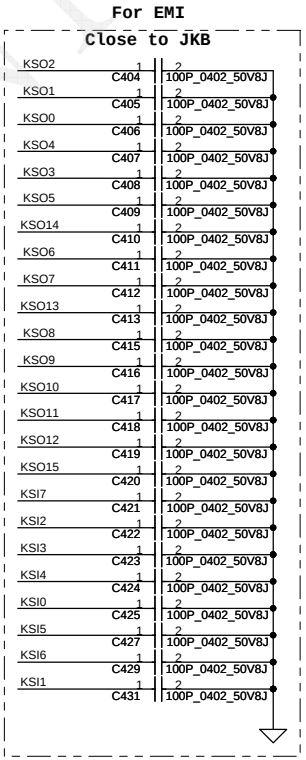
LPC Debug Port



KEYBOARD CONN.







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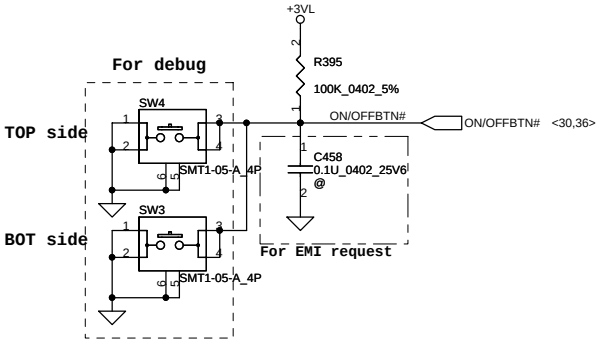
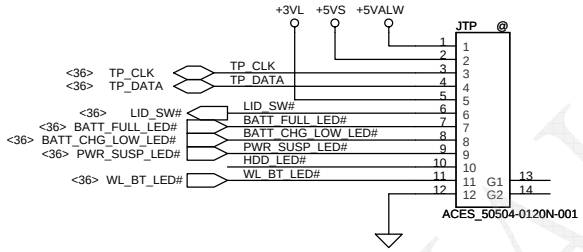
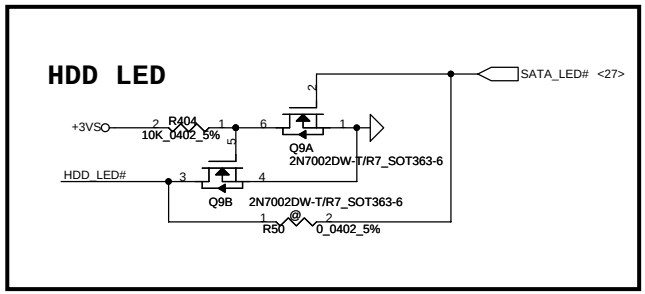
Power Button



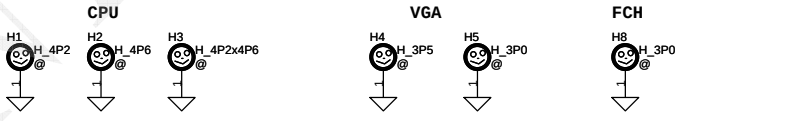
Touchpad Connector



HDD LED

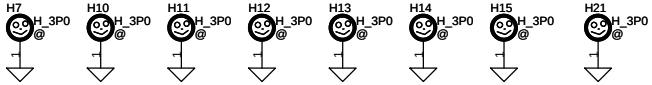


Screw Hole

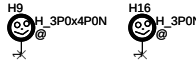


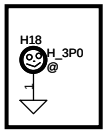
TP

PTH

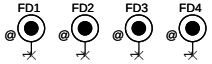


NPTH





PCB Fedical Mark PAD



ISPD

U1 HUDM3R1@
SA000043IN0
218-0755042 A13 HUDSON-M3

UV1 CHUNBW@
SA000056220
CHELSEA PRO

U1 HUDM3UNBW@
SA000043I00
218-0755042 A13 HUDSON-M3

UV1 THUNBW@
SA00004WI70
THAMES XT

ZZZ
DA80000ST00
PCB LA-7291P

PJP1 45@
PJP1

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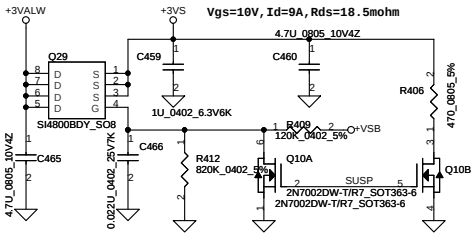
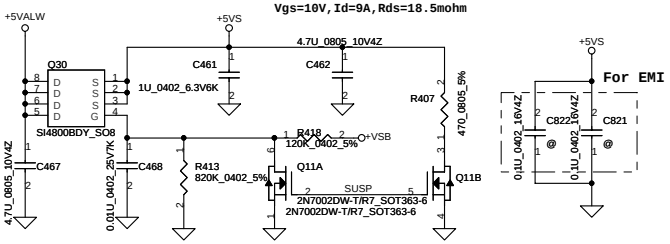
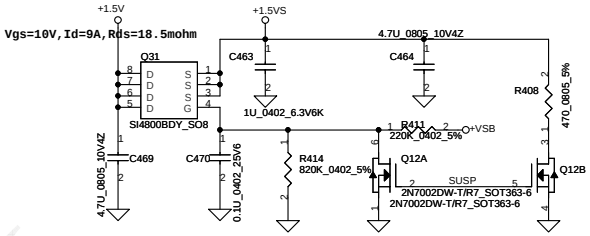
+3VALW TO +3VS



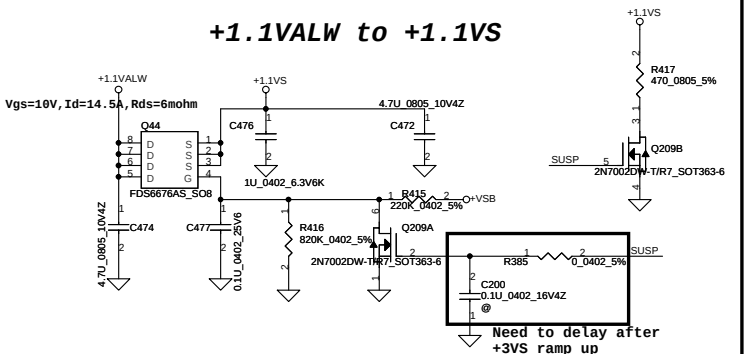
+5VALW TO +5VS

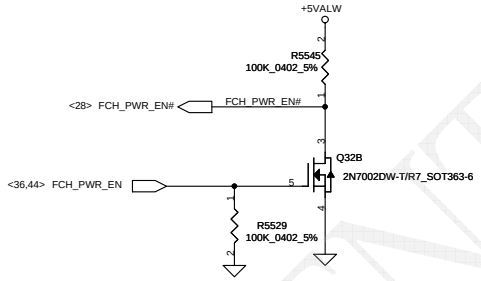


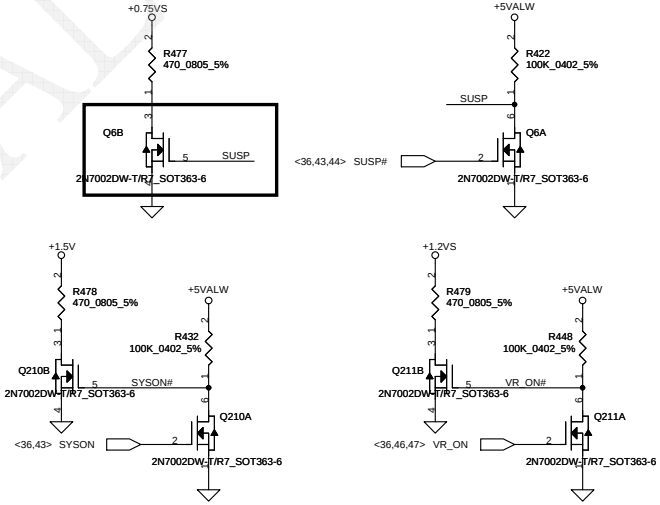
+1.5V to +1.5VS



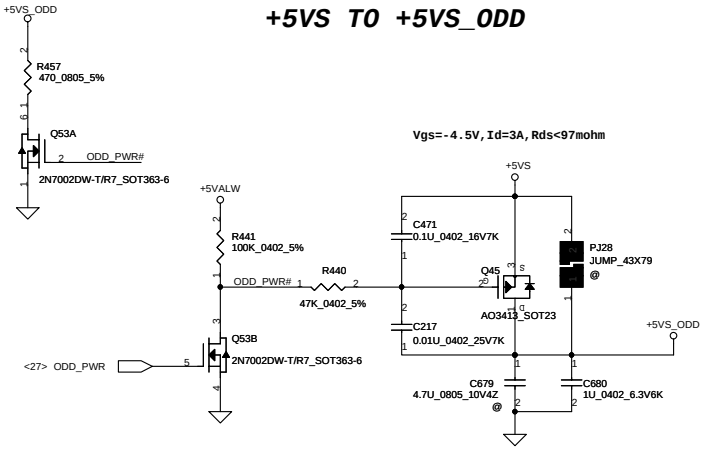
+1.1VALW to +1.1VS







+5VS TO +5VS_ODD



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Issued Date	2011/11/28	Deciphered Date	2013/12/31

Compal Electronics, Inc.			
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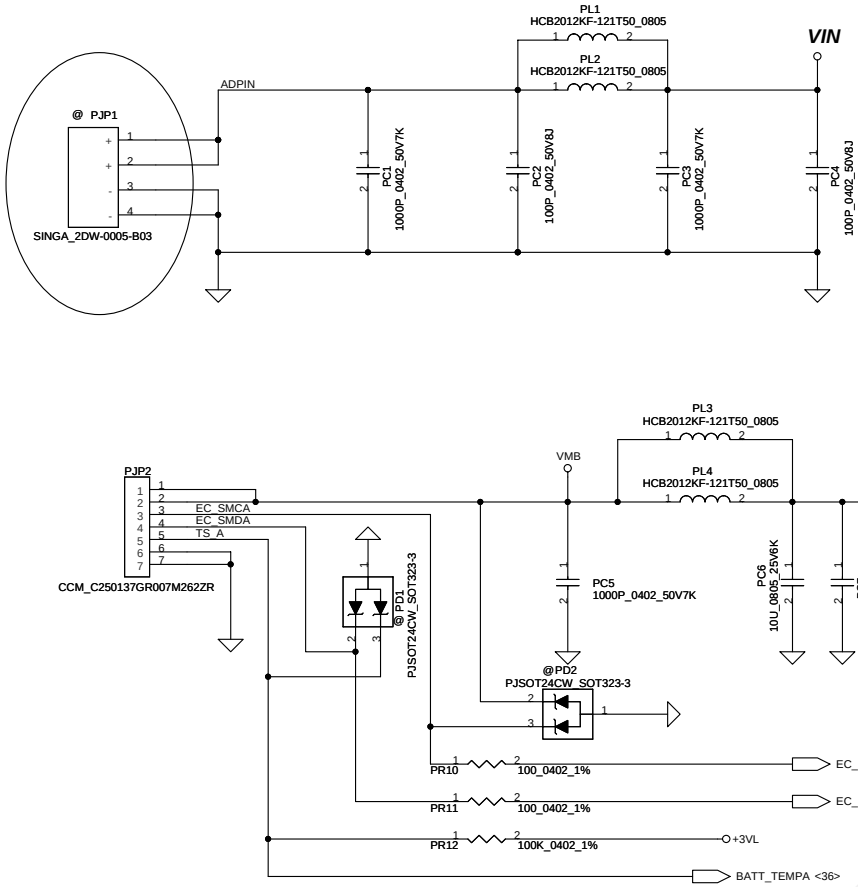
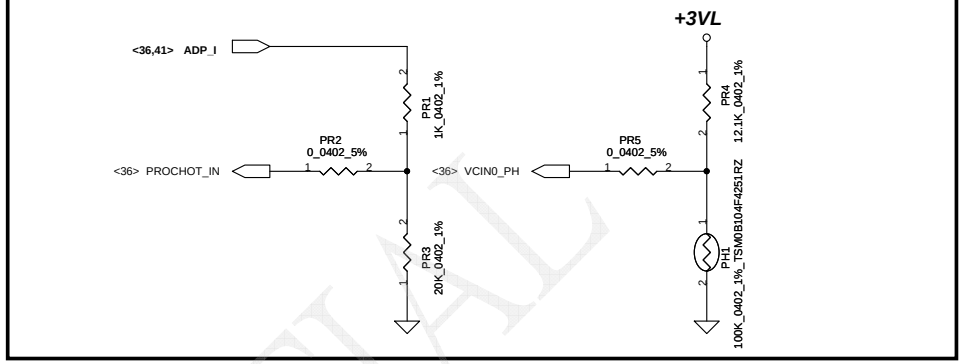
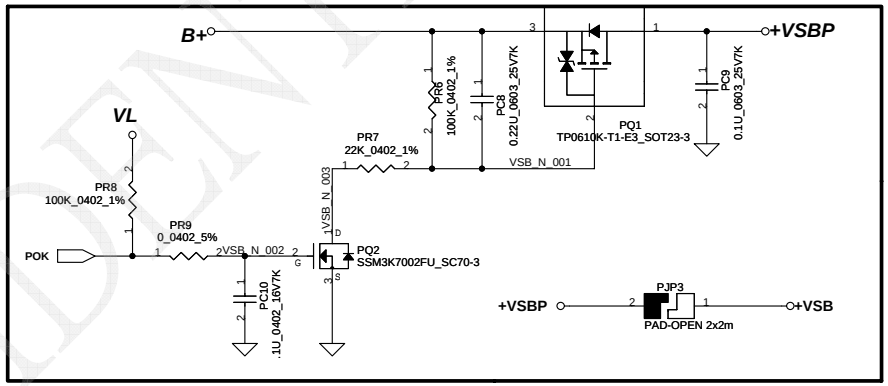


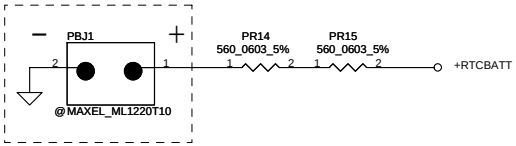
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

Please locate these parts
Near EC chip





RTC Battery



SP093MX0000

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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for reverse input protection

PQ209 SI1304BDL-T1-E3_SC70-3
PR225 1M_0402_5%
PR226 3M_0402_5%

VIN PQ203 TPCA8057-H_PPAK56-8-5 P1
PQ205 DMG4406LSS_SO8 P2
PR211 0.01_1206_1%
B+ 1UH_NRS4018T1R0NDGJ_3.2A_30% PL201
CHG_B+
PQ207 DMG4406LSS_SO8

PC230 2200P_0402_50V7K
PR231 @ 0_0402_5%
PC231 0.1U_0402_25V6
BQ24725_ACDRV
PC211 10U_0805_25V6K
@PC212 10U_0805_25V6K
PC213 10U_0805_25V6K
PC214 10U_0805_25V6K
@PC215 0.1U_0402_25V6
PC216 0.1U_0402_25V6
PC234 0.01U_0402_50V7K
PR232 @ 0_0402_5%
BQ24725_BATDRV PR233 4.12K_0603_1%

PD230 BAS40CW_SOT323-3
PC235 0.1U_0402_25V6
PC236 0.1U_0402_25V6
0.047U_0402_25V7K PC237
PR228 10_1206_1%
PR229 2.2_0603_5%
PD231 RB751V-40_SOD323-2
PC238 0.1U_0603_25V7K
PC239 1U_0603_25V6K
PC205 1U_0603_25V6K
PQ201 AON7408L
DH_CHG
PR234 4.12K_0603_1%
PR235 4.12K_0603_1%
PL202 4.7UH_ETQP3W4R7WFN_5.5A_20%
PR222 0.02_1206_1%
BATT+
PQ202 FDMC7692S_MLP8-5
PR206 @ 4.7_1206_5%
PC206 @ 680P_0402_50V7K
PC240 0.1U_0402_25V6
PC241 0.1U_0402_25V6
@ PC221 10U_0805_25V6K
PC222 10U_0805_25V6K
PC223 10U_0805_25V6K
PC224 2200P_0402_50V7K
PC225 0.01U_0402_50V7K

PU200 BQ24725RGRR_VQFN20_3P5X3P5
PAD ACN ACP CMSRC ACDRV ACOK VCC PHASE HIDRV BTST REGN LODRV GND SRP SRN BATDRV ACDET IOUT SDA SCL ILIM
BQ24725_CMSRC BQ24725_ACDRV BQ24725_ACOK BQ24725_BATDRV
PR236 10_0603_1%
PR237 6.8_0603_5%
PC242 0.1U_0603_16V7K

+3VALW @PR238 10K_0402_1%
+3VL PR239 10K_0402_1%
<13,36> ACIN PR240 10K_0402_1%
PR241 150K_0402_1%
PR242 100K_0402_1%
PC243 0.01U_0402_25V7K
VIN PR243 270K_0402_1%
PR244 154K_0402_1%
PC244 0.1U_0402_25V6
PR245 66.5K_0402_1%
PC246 100P_0402_50V8J
PR246 100_0402_5%
PC245 100P_0402_50V8J

EC_SMB_CK1 <36,40>
EC_SMB_DA1 <36,40>
ADP_I <36,40>

Please locate the RC
Near EC chip
2011-02-22

Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM 3.97A

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Issued Date	2009/01/23	Deciphered Date	2010/01/23

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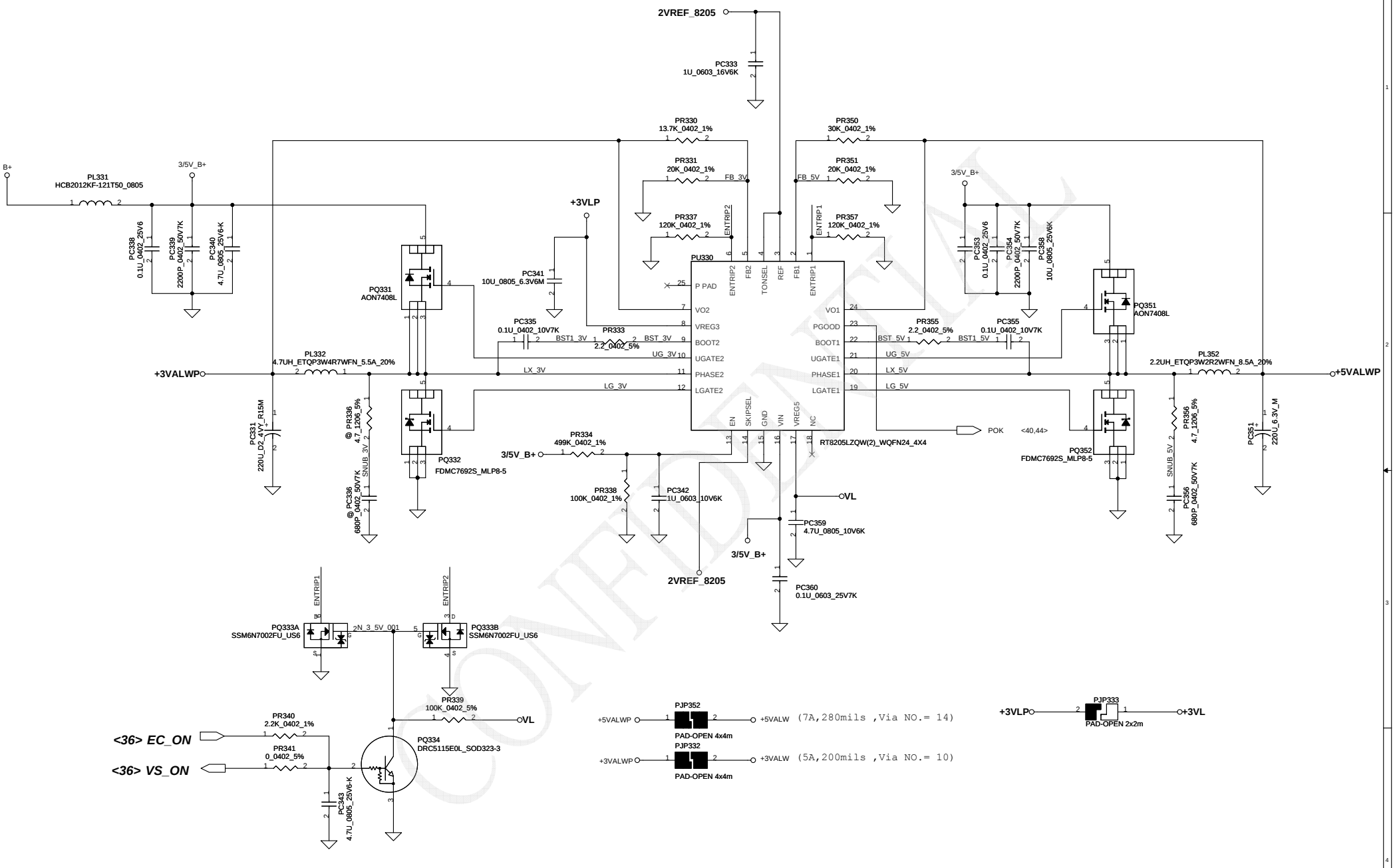

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.		
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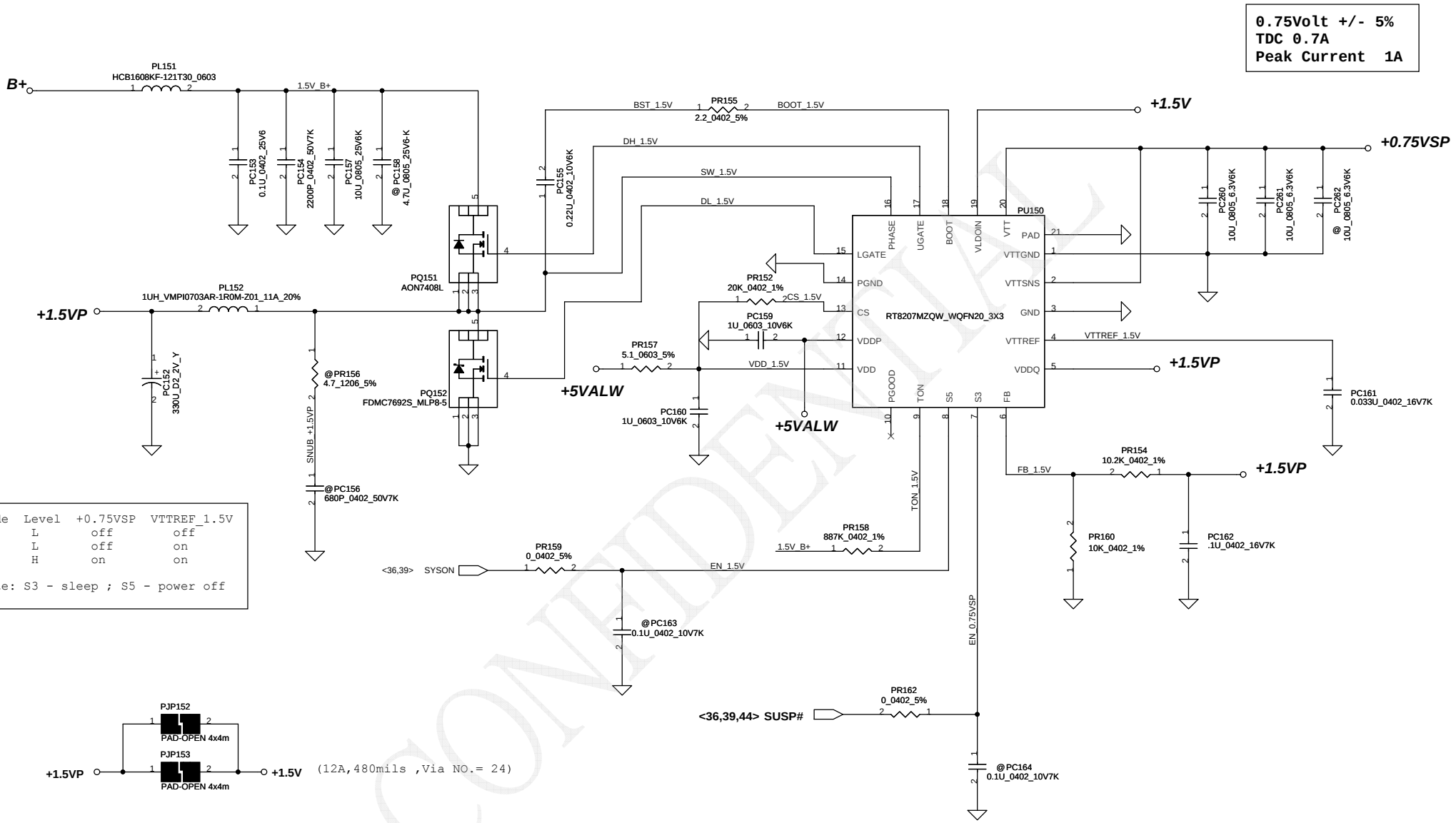

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

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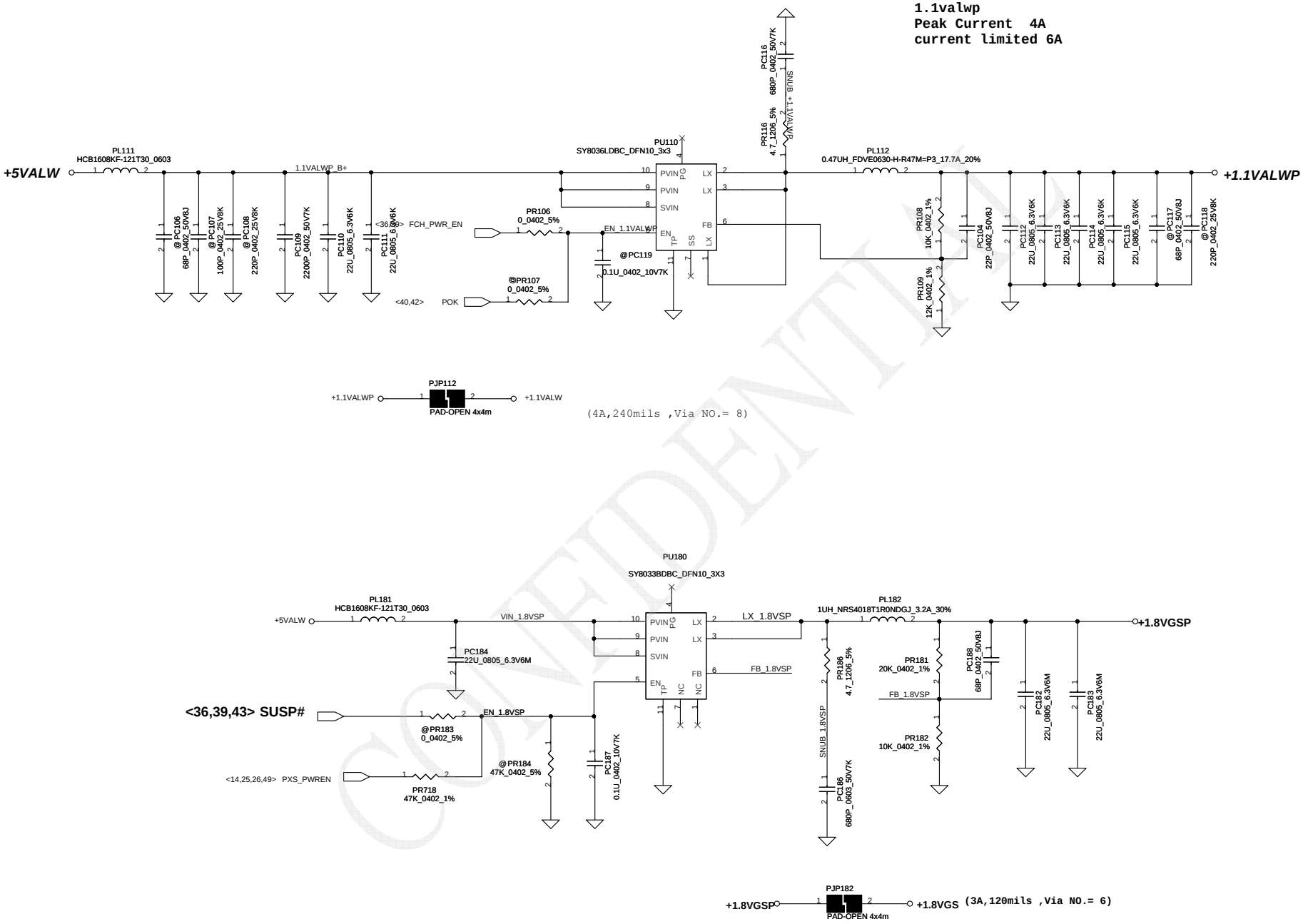

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

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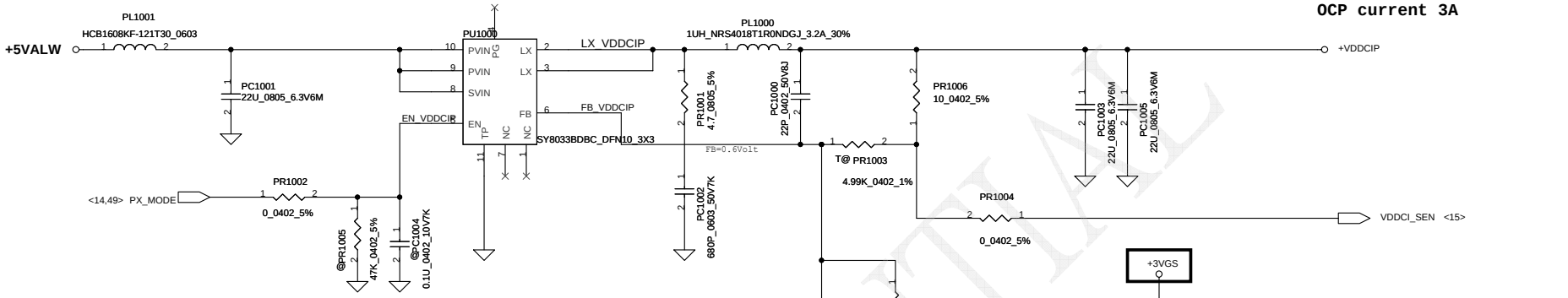
+VDDCI
TDC 2.2A

OCP current 3A

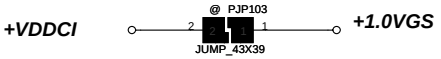


	VDDCI_VID	
High	1V PR1003 4.99K SD034499180 PR1007 29.4K SD034294280	0.95V PR1003 5.23K SD034523180 PR1007 86.6K SD034866280
Low	0.9V PR1003 4.99K SD034499180	0.91V PR1003 5.23K SD034523180
	Thames	Chelsea

PR1003 5.23K_0402_1% C@

PR1007 86.6K_0402_1% C@

(2.2A,100mils ,Via NO.= 5)



Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

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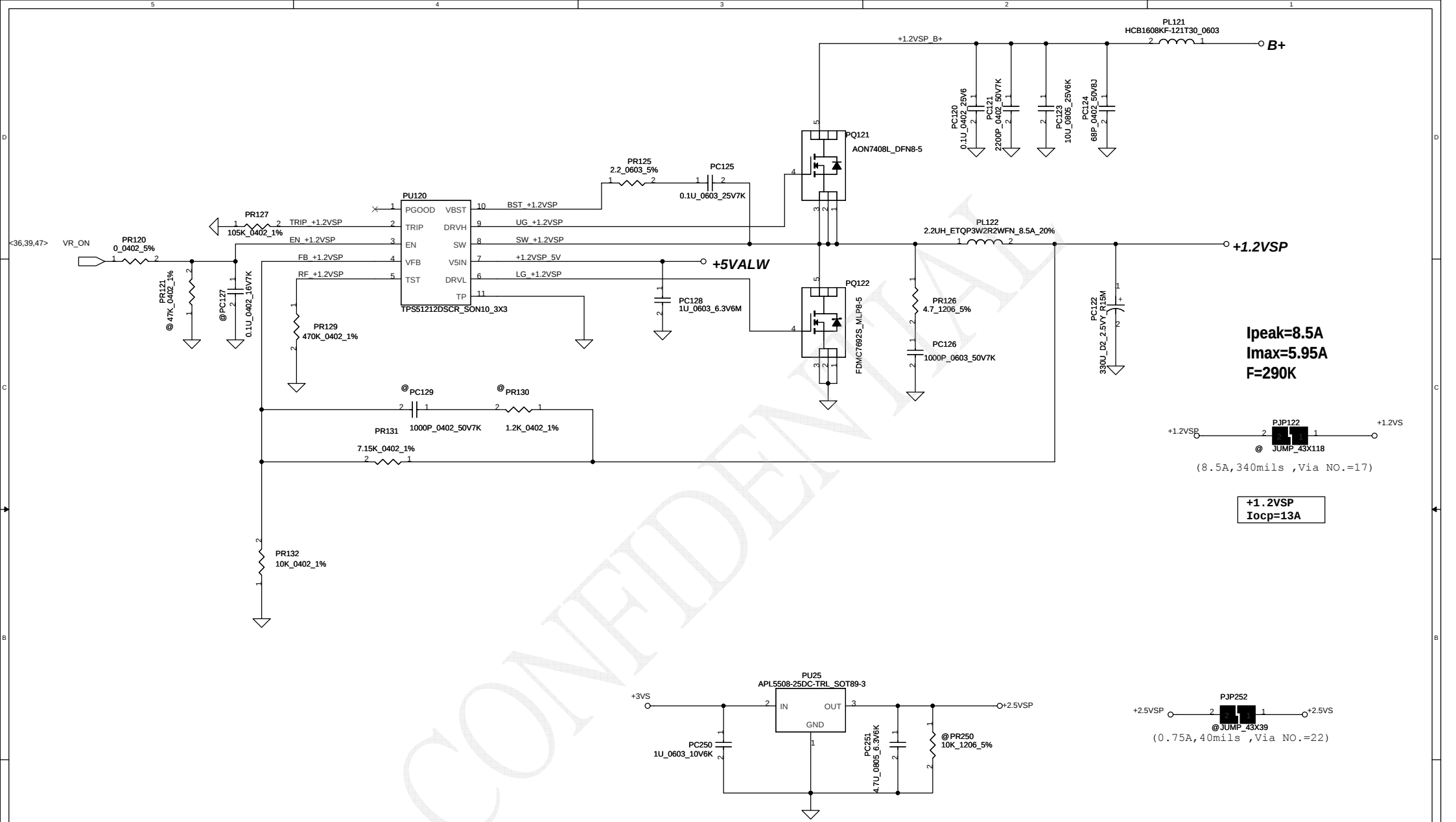

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.

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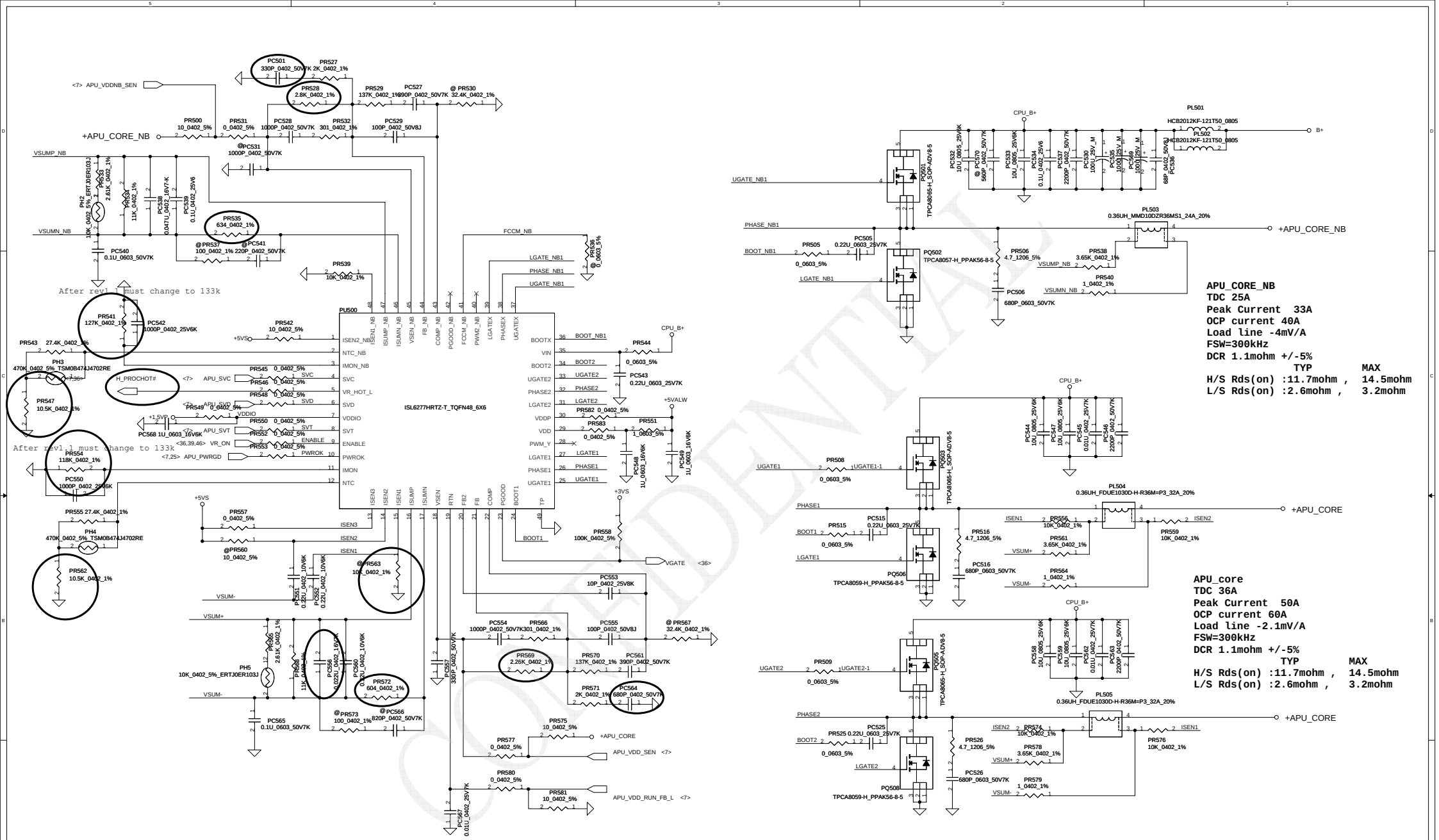

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.			
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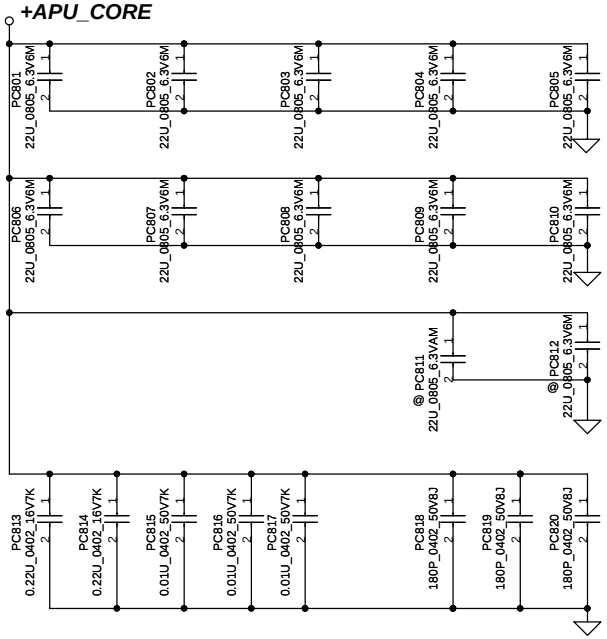
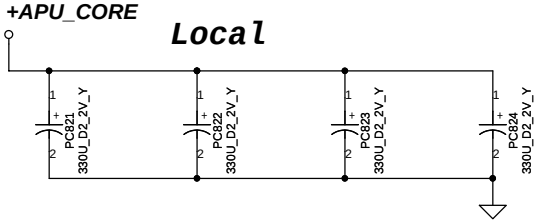
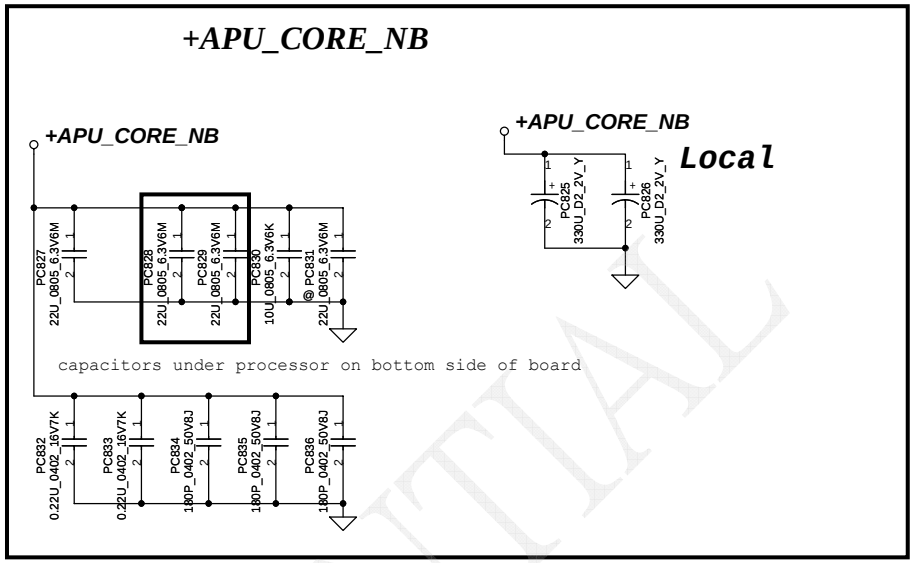
+APU_CORE

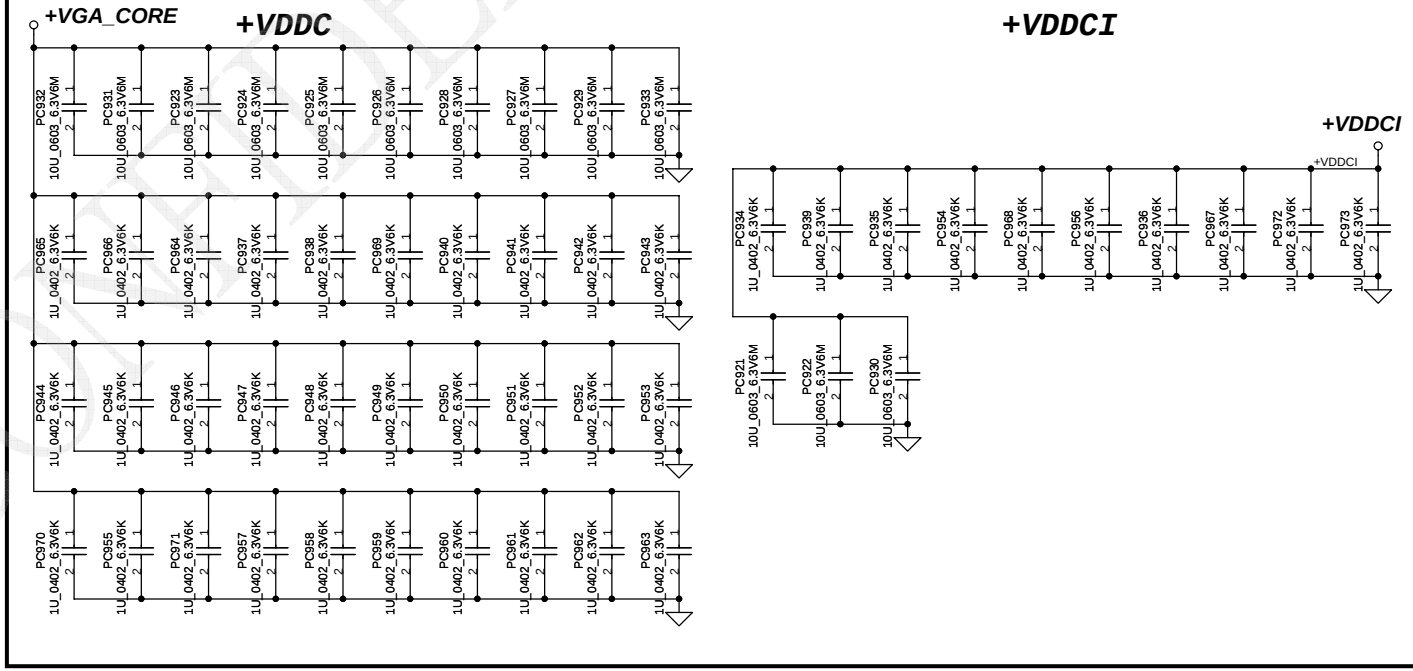




+APU_CORE_NB



+VGA_CORE



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Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.		
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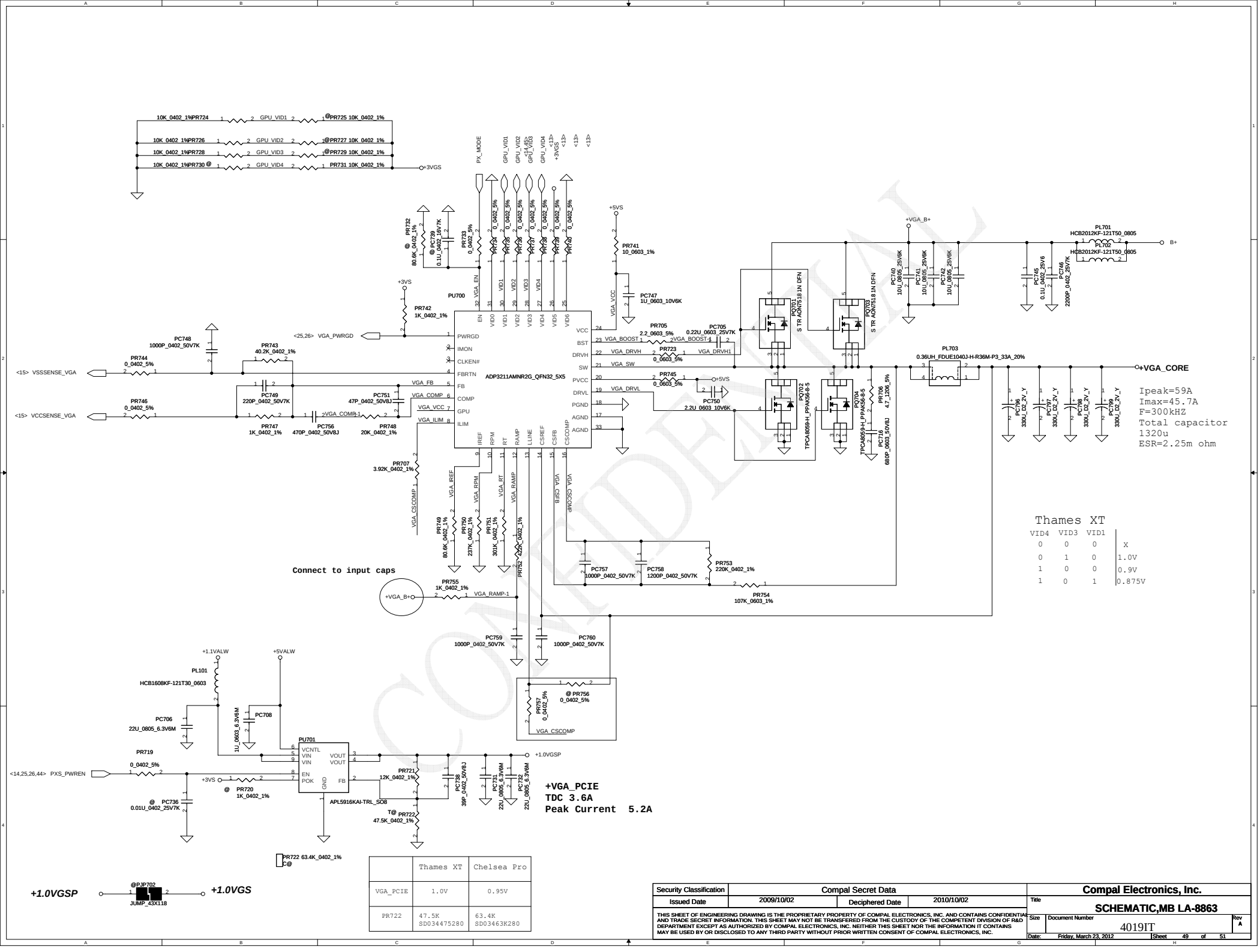

	Thames XT	Chelsea Pro
VGA_PCIE	1.0V	0.95V
PR722	47.5K SD034475280	63.4K SD03463K280

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HW PIR (Product Improve Record)

QMLE4 LA-8863P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2012/02/10

Item	Date	Page	Solution	Request
1.	1/10	P32	Add PJ31	For saving power consumption
2.	1/12	P38	Change JTP symbol to SP01001BF10	For ME request
3.	1/30	P35	Add internal MIC to MB	For customer request
4.	2/2	P14	Remove PX4.0 circuit	Support PX5.0
5.	2/2	P31	Add PJ26,PJ33, WLAN power circuit and reset pin	For customer request
6.	2/2	P33	Update JCRIO pin definition	Change int. MIC to MB
7.	2/2	P35	Remove CA64, add RA32 and RA33	Move sense resistors to MB
8.	2/3	P31	Change JWLAN symbol to SP07000TB00	For ME request
9.	2/3	P31	Add WLAN_PWR# and WLAN_RST#	For customer request
10.	2/7	P32	Change UL3 and UL4 PN to SP050005V00	For shortage

REVISION CHANGE: 0.2 TO 0.3
GERBER-OUT DATE: 2012/03/12

Item	Date	Page	Solution	Request
1.	3/1	P12	Update RTC scematic	For avoiding +3VL short to GND
2.	2/29	P22	Change R108 pull-high from +3VS to +3VALW	For LVDS sequence issue
3.	3/7	P26	Add R292 and reserve R293	To avoid PXS_PWREN floating
4.	3/7	P7	Unstuff R121~R124,R118,R119	For debug use
5.	3/7	P27	Update U13 footprint	
6.	3/7	P27/30	Connect SATA port2 to 15"ODD connector, and add GPIO54	To solve SATA EA fail issue
7.	3/8		Change RB20,RB34,R3,RV102,R425,R136,R31,R32,R33,RV284,RV287 R62,RV277 to short pad	
8.	3/12	P24	Add C201 and C214	For EMI request
9.	3/12	P30	Add C364 and C365	For EMI request
10.	3/12	P35	Add CA5, CA6, CA64, CA67, CA68 and CA77	For EMI request
11.	3/14	P8	Add C147 co-layout with C100	To avoid damage by SMT process
12.	3/14	P10	Add C148 co-layout with C218	To avoid damage by SMT process

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2012/02/14	P40-PWR-DCIN/BATT CONN/OTP	Delete PR12,PR13	Circuit modify
2.	2012/02/14	P41-PWR-CHARGER	Change PR211 to 0.01_1206_1%,PL201 to1UH 4*4*2 Add PC207,PC208,PC217,PC218,Delete PC232,PC233	Circuit modify
3.	2012/02/14	P43-PWR-1.5VP/+0.75VSP	Change PL152 to SH00000KS00	Circuit modify
4.	2012/02/14	P44-PWR-+1.1VALWP/+1.8VSP	Change PR718 to 47K,add PC187	HW request
5.	2012/02/14	P46-+1.2VSP/+2.5VSP PR127 to SD034105380	Change PL122 to 2.2uH(SH00000MR00),	Circuit modify
6.	2012/02/14	P37-PWR +CPU_CORE	Change PQ502 to TPCA8057	Circuit modify
7.	2012/03/06	P40-PWR-DCIN/BATT CONN/OTP	Add PR12(100KΩ)	Circuit modify

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