

QMLE4/5

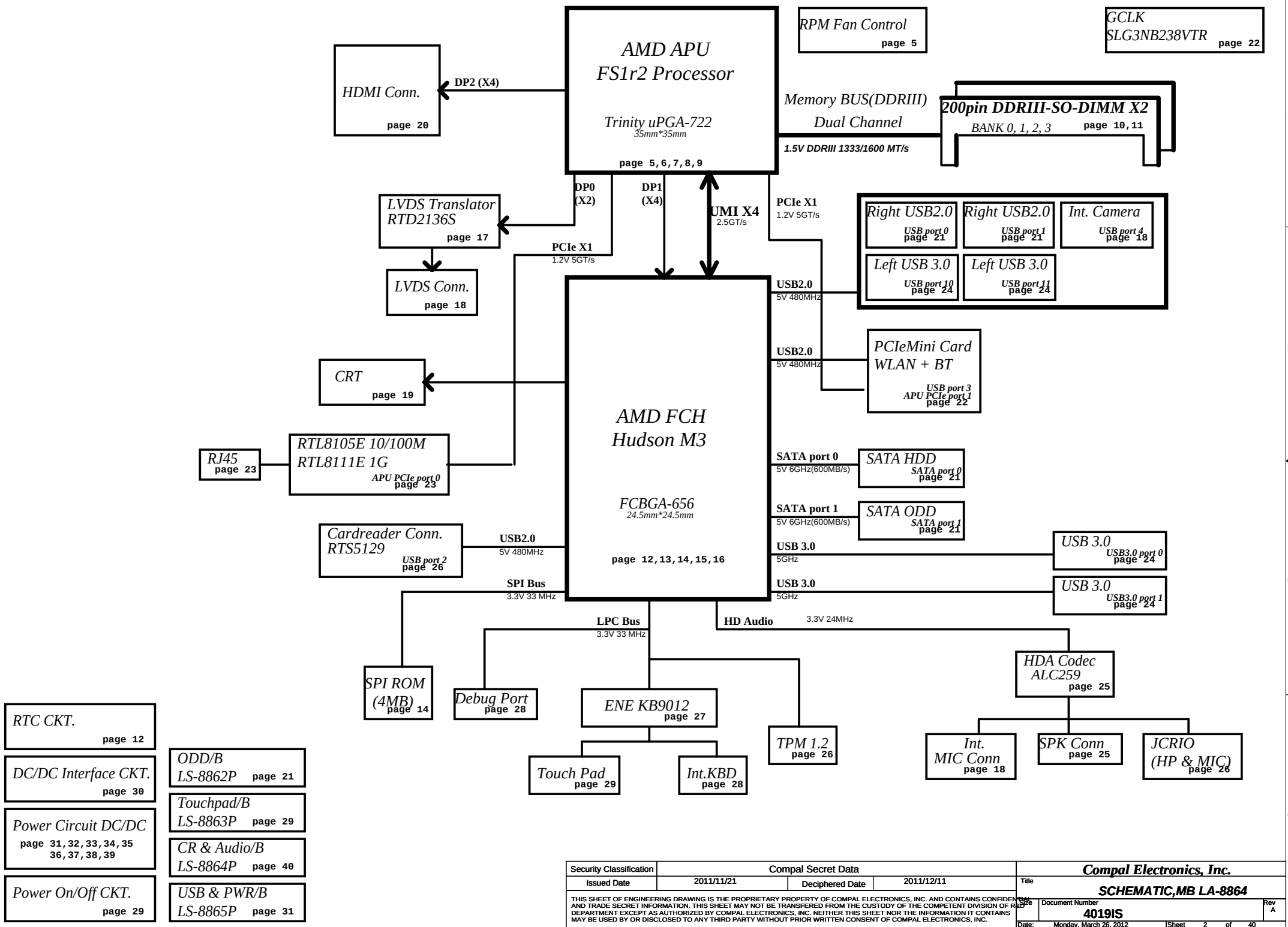
Eureka UMA

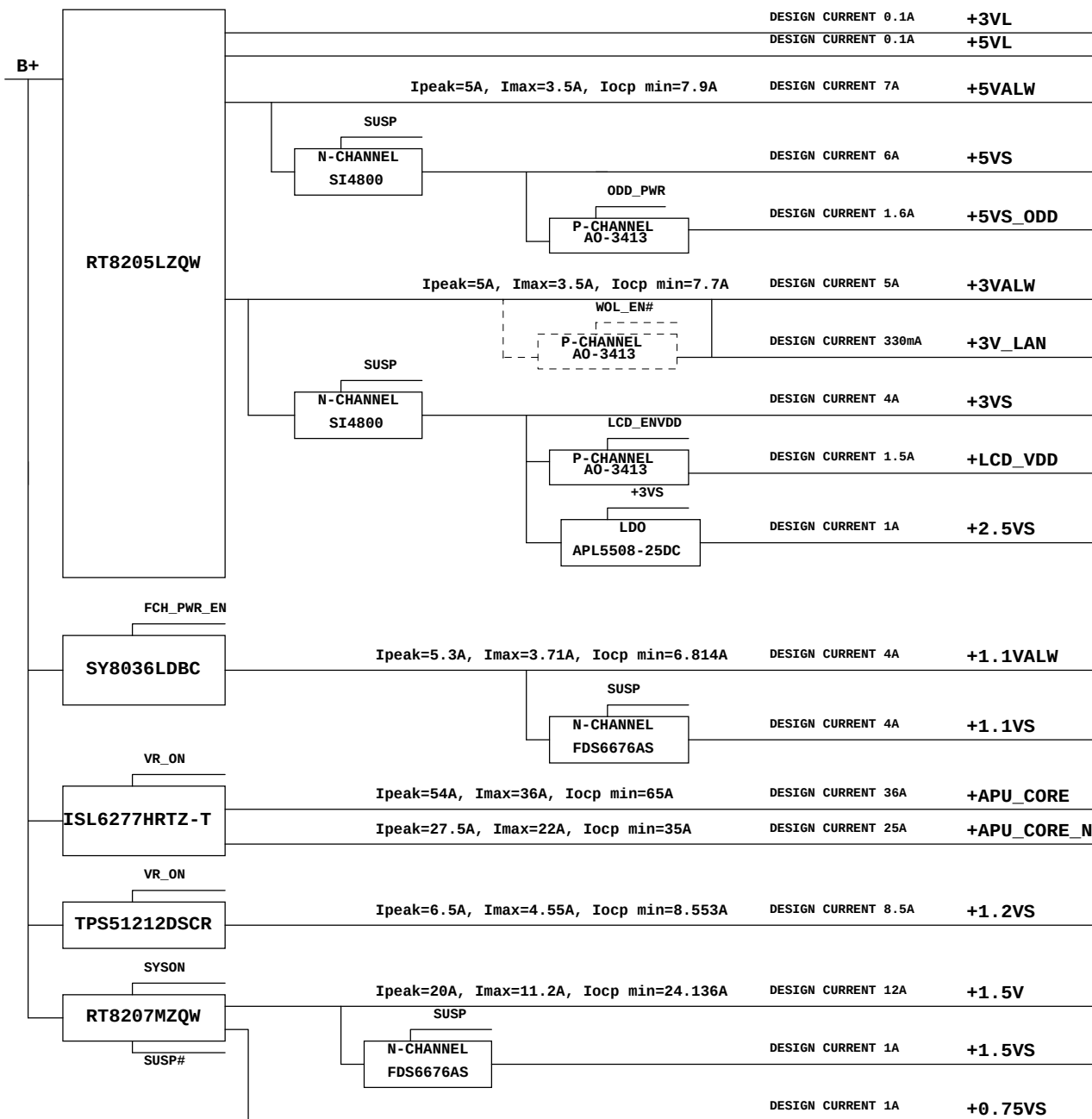
LA-8864P REV 0.3 Schematic

AMD Trinity FS1r2 APU / Hudson M3 FCH

2012-03-14 Rev 0.3

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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

BTO Option Table

Function	FCH			Clock	
description	Hudson-M3			Clock	
explain	R1	R3	UNBW	Green Clock	No Green Clock
BTO	HUDM3R1@	HUDM3R3@	HUDM3UNBW@	GCLK@	NOGCLK@

Function	LAN		Camera	Internal Analog MIC	TPM	
description	LAN		Camera	Internal Analog MIC	TPM	
explain	10/100M	GIGA	Camera	Internal Analog MIC	9635	9655
BTO	8105ELD0@	8111FVB@	CAM@	AMIC@	TPM9635@	TPM9655@

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 000X b
+3VS	DDR SO-DIMM 1	A2 H	1010 001X b
+3VS	WLAN		

EC SM Bus1 Address

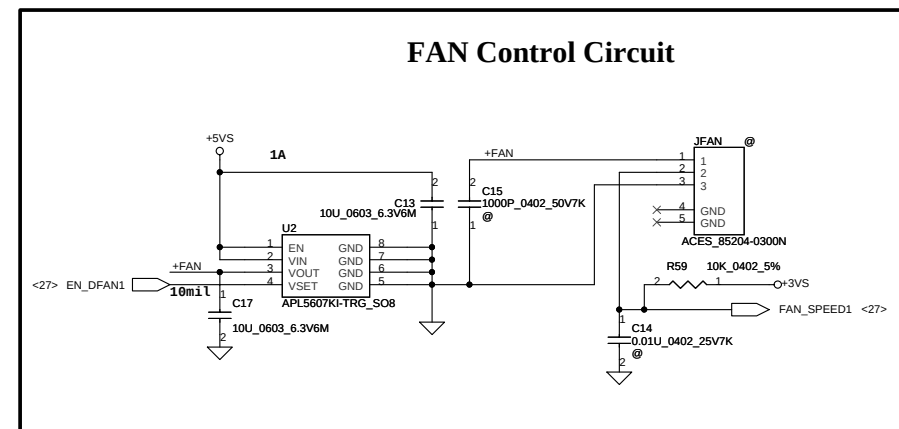
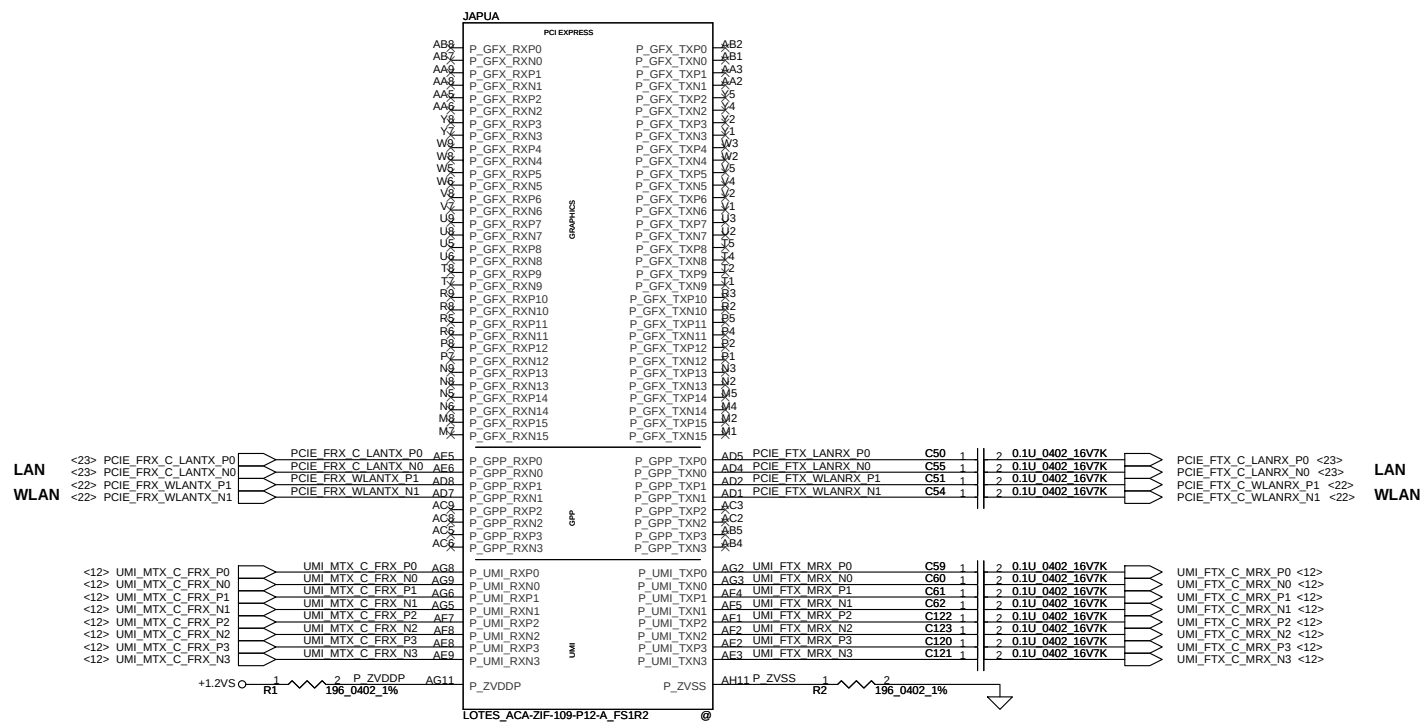
Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Charger	12 H	0001 0010 b
EC SM Bus2 Address			
Power	Device	HEX	Address
+3VL	SB-TSI	98 H	1001 1001 b

EC SM Bus3 Address

Power	Device	HEX	Address
+3VS	LVDS Translator	94 H	1001 0100 b

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

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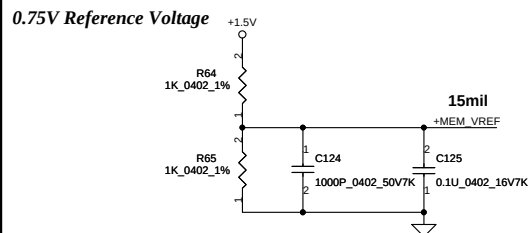
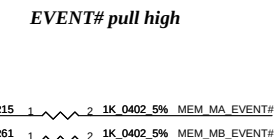
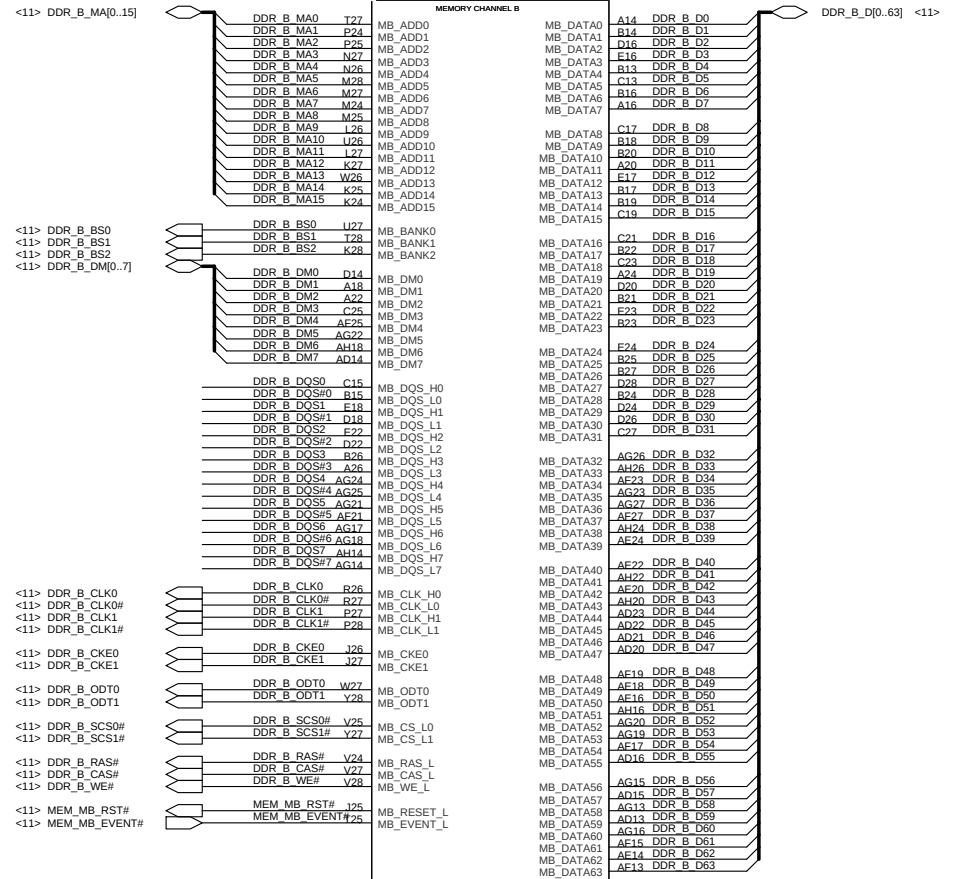
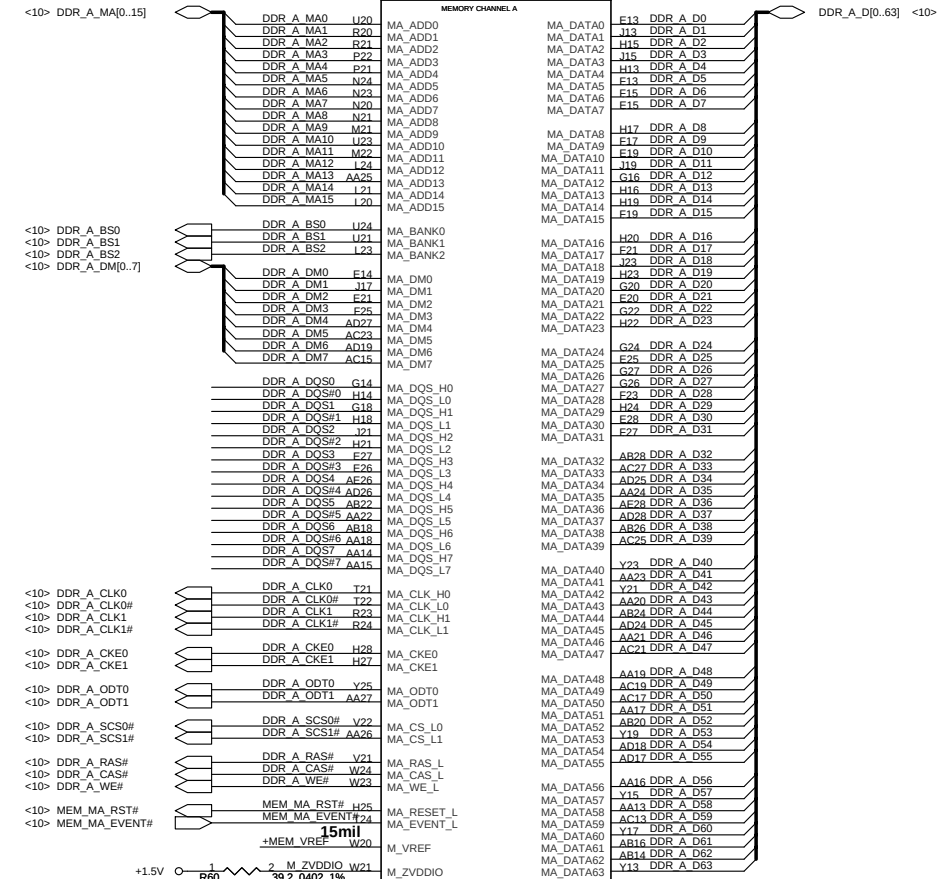
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<10> DDR_A_DQS[0..7]

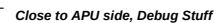
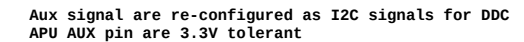
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<11> DDR_B_DQS[0..7]

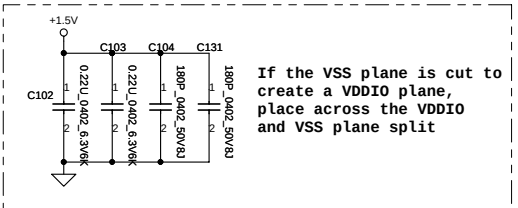
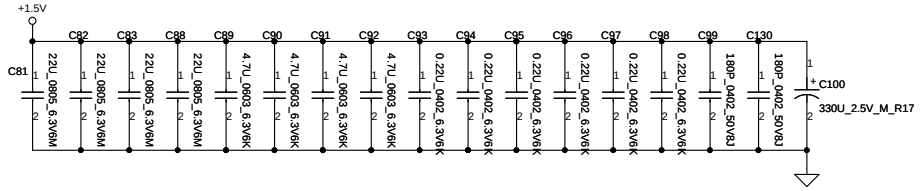
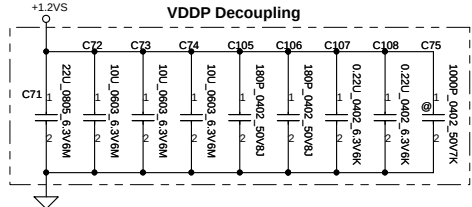
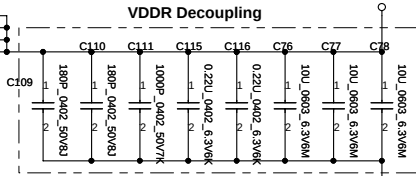
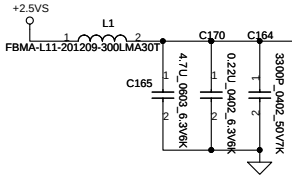
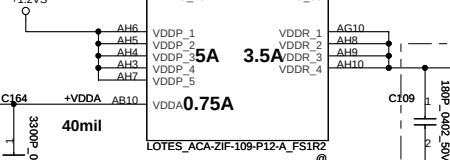
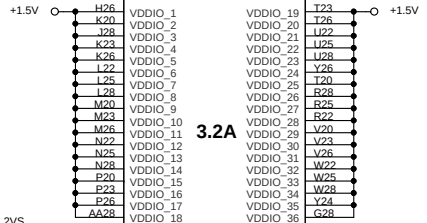
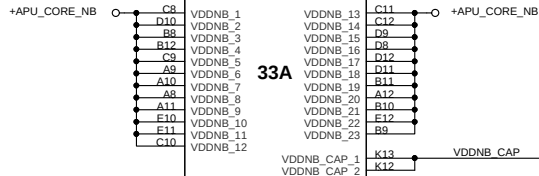
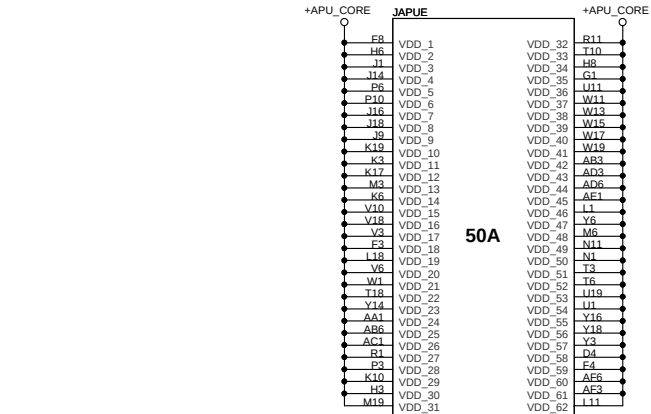
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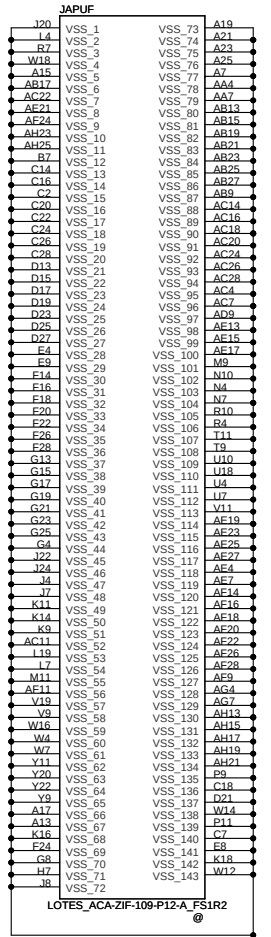
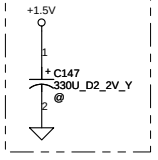
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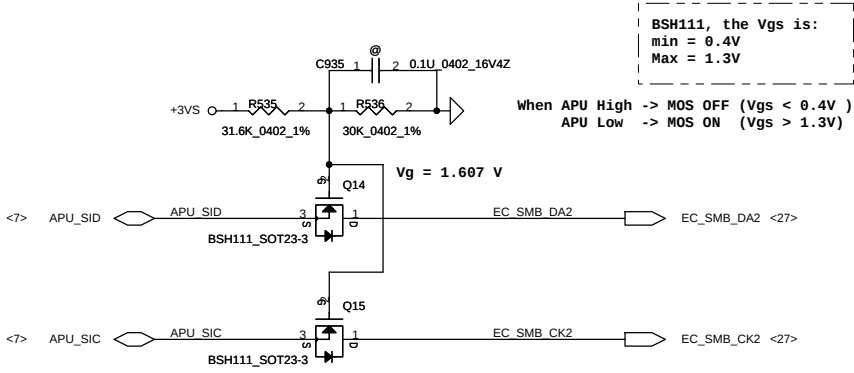


Co-layout with C100 on PVT

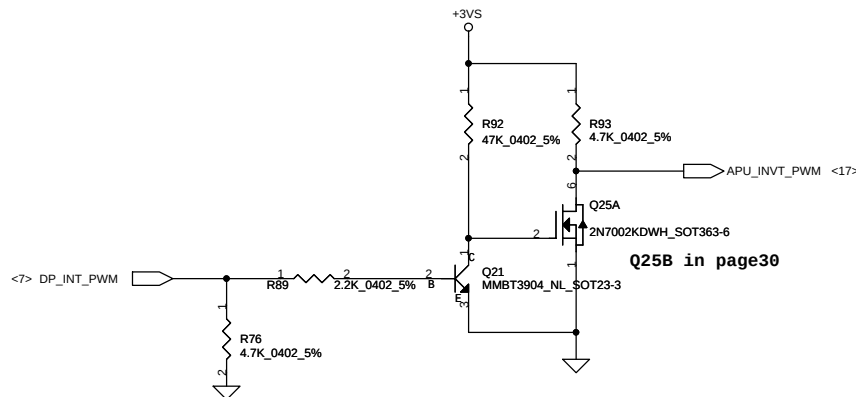


Demo Board Capacitor			
APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 + 2(split)
			180pF x 1 + 2(split)
VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 1	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

SB-TSI

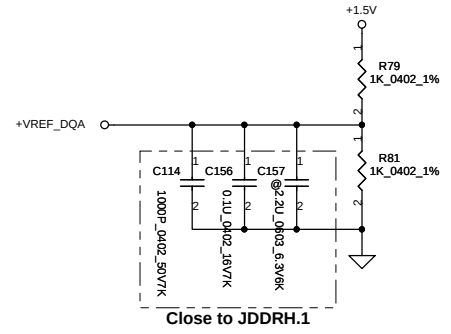
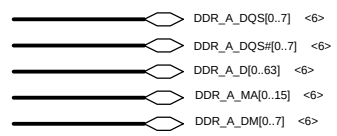
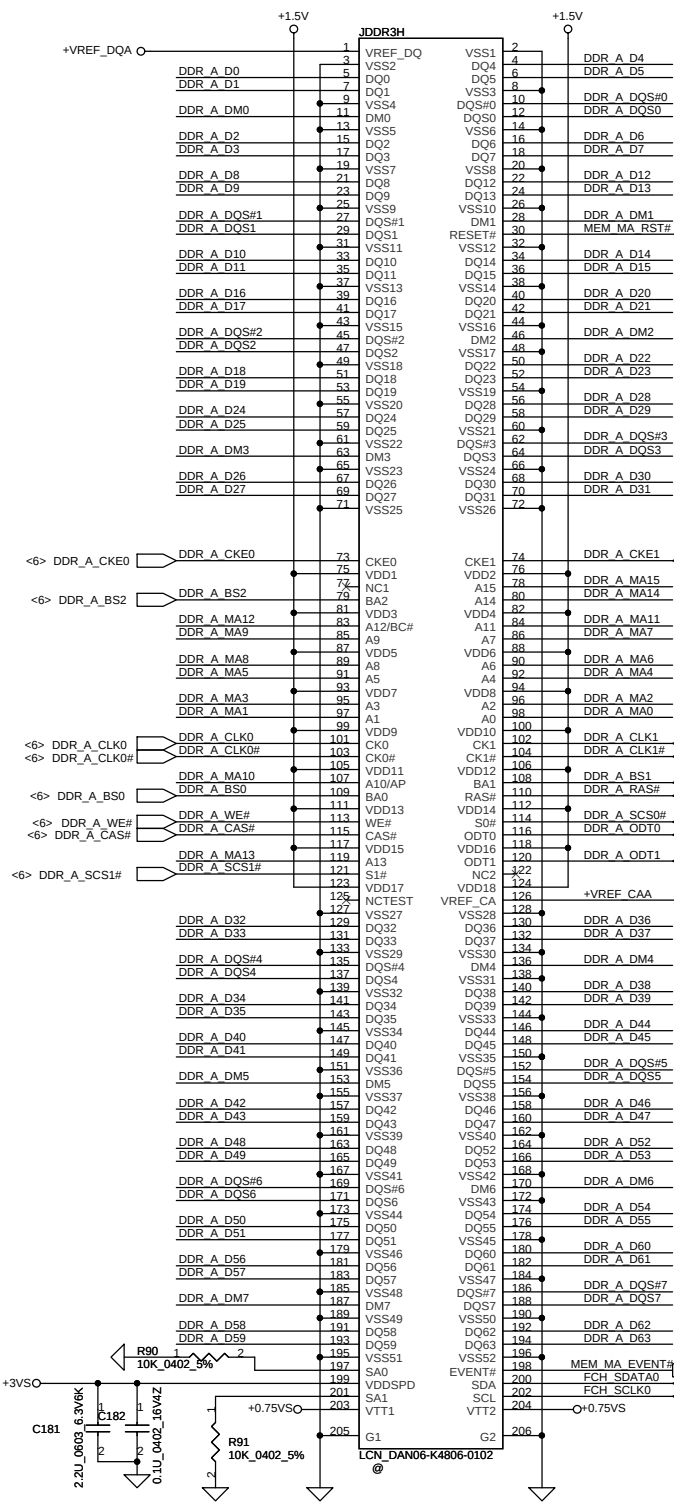


Panel PWM

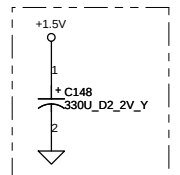


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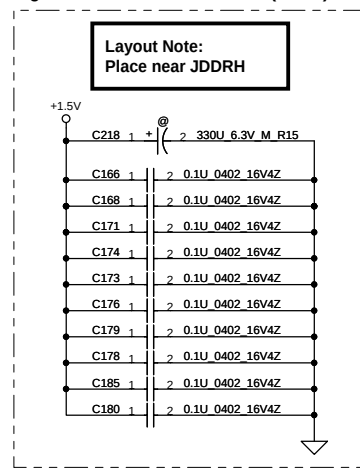
DDR3 SO-DIMM A Standard Type



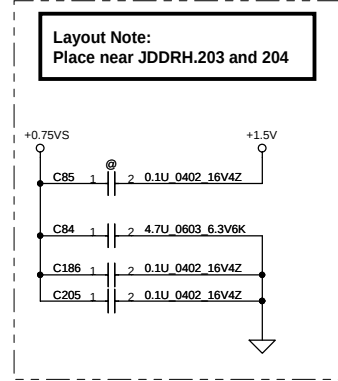
Co-layout with C218 on PVT



Change C218 to SF000002080 (330U) on DVT

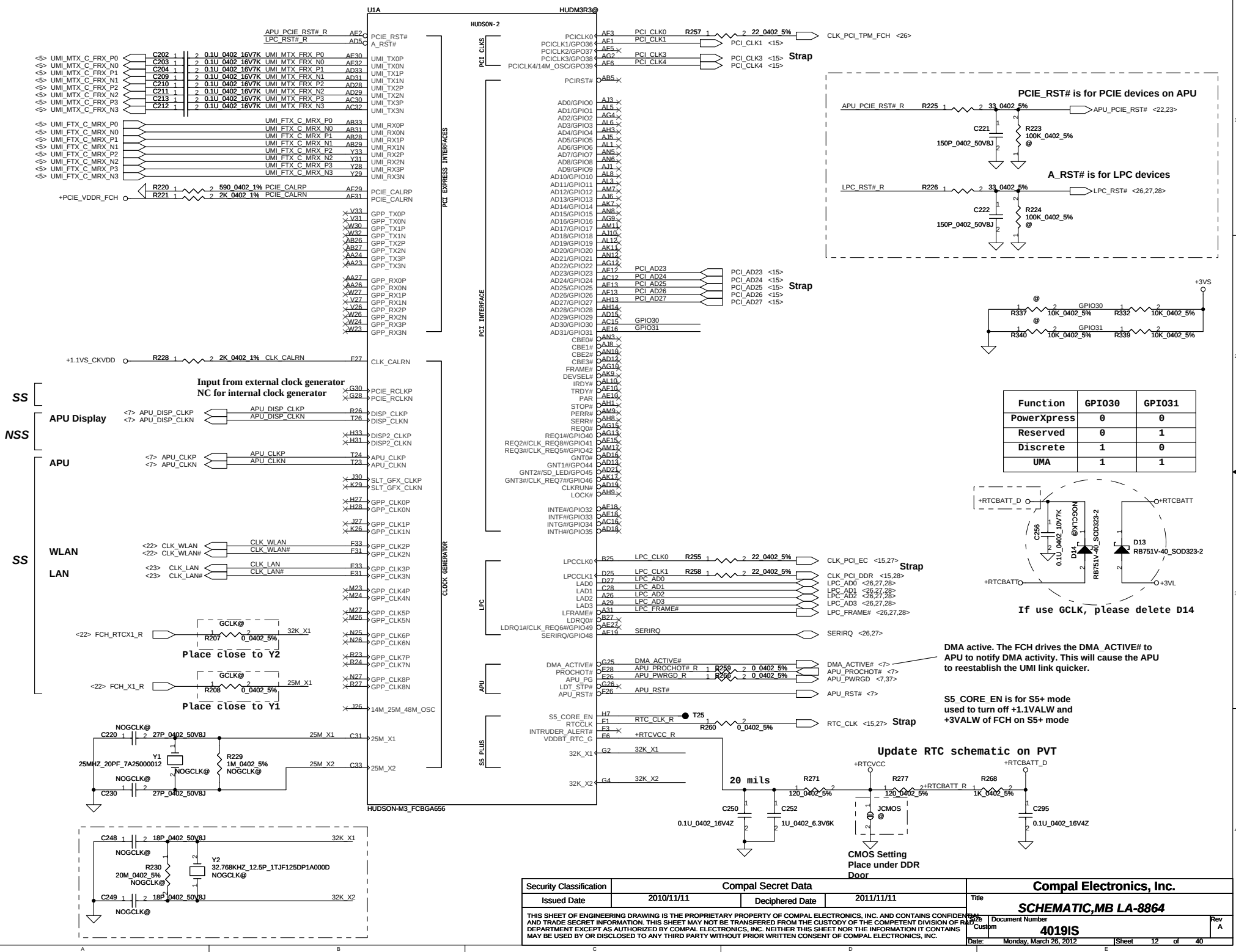


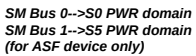
Layout Note:
Place near JDDRH



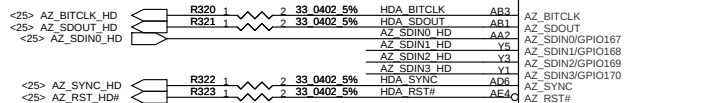
Layout Note:
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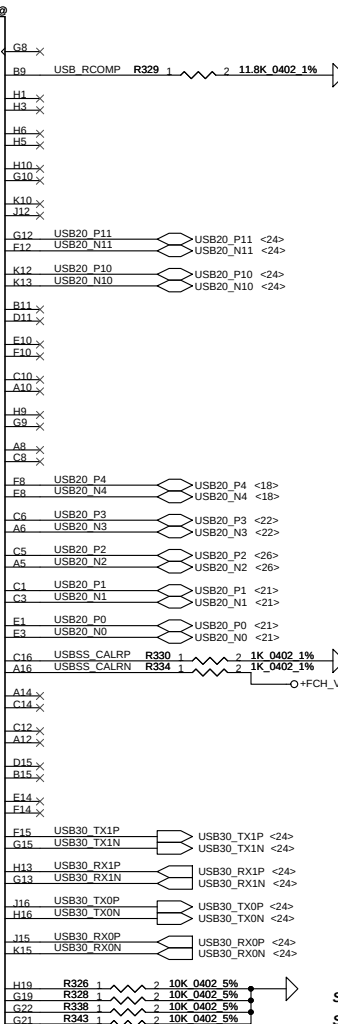
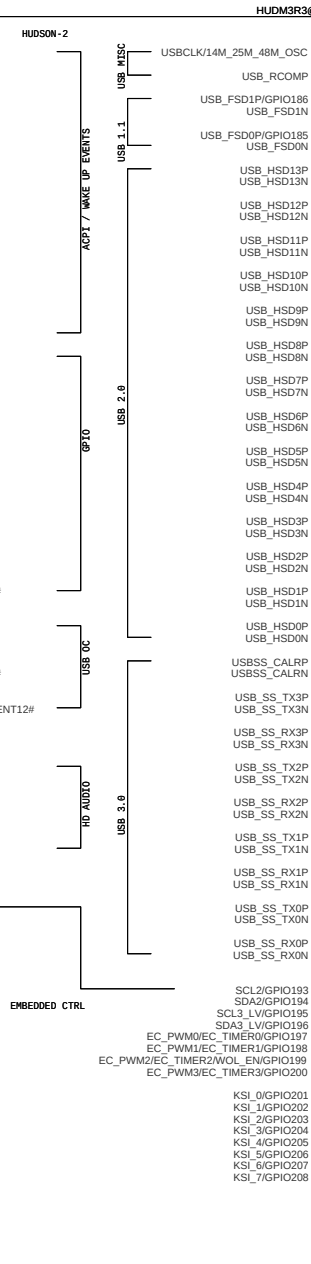
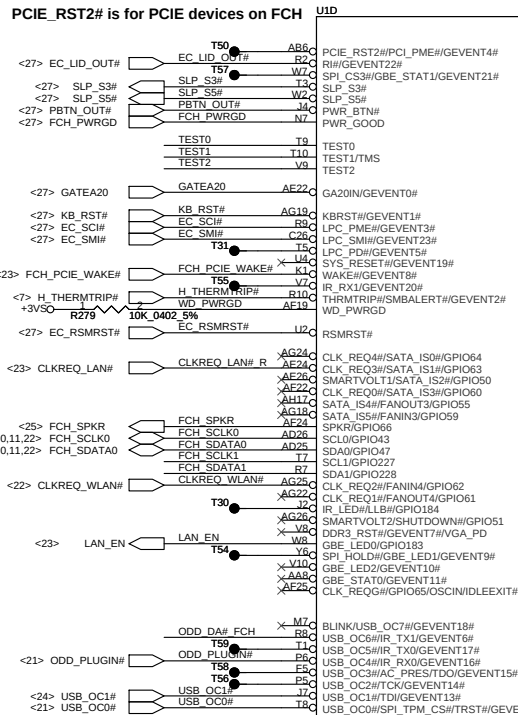
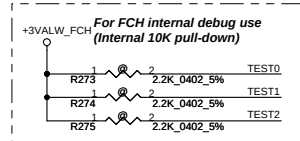
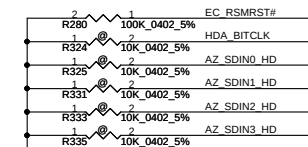
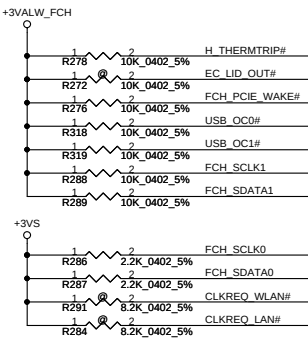




```
USB_OC1# is for left USB3.0 ports
USB_OC0# is for right USB2.0 ports
```



Internal Pull-up ?



**Hudson-M2/M3
OHCI (DEV-20, FUN-5)**

Hudson-M2
OHCI (DEV-22, FUN-0)
EHCI (DEV-22, FUN-2)

Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)

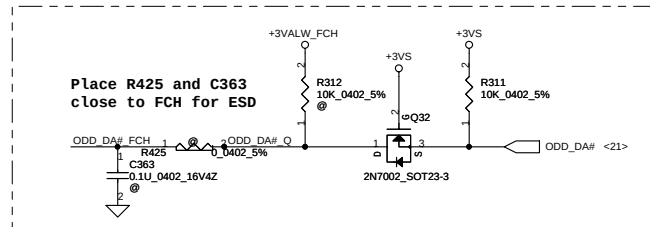
Hudson-M2/M3
OHCI (DEV-19, FUN-0)
EHCI (DEV-19, FUN-2)

Hudson-M2/M3
OHCI (DEV-18, FUN-0)
EHCI (DEV-18, FUN-2)

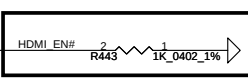
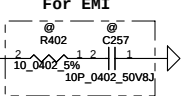
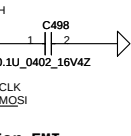
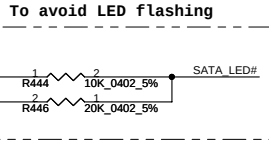
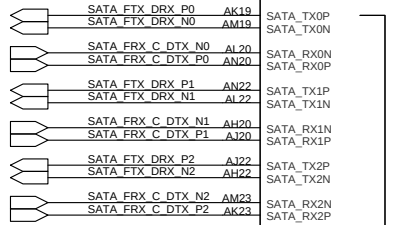
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Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)

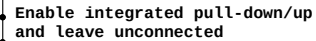
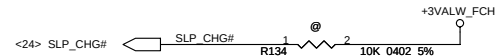
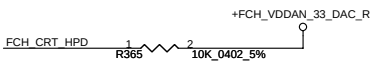
domain for SB-TSI



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If an SPI ROM is shared between FCH and the Embedded Controller, a 10-k pull-up resistor to +3.3V_S5 is installed

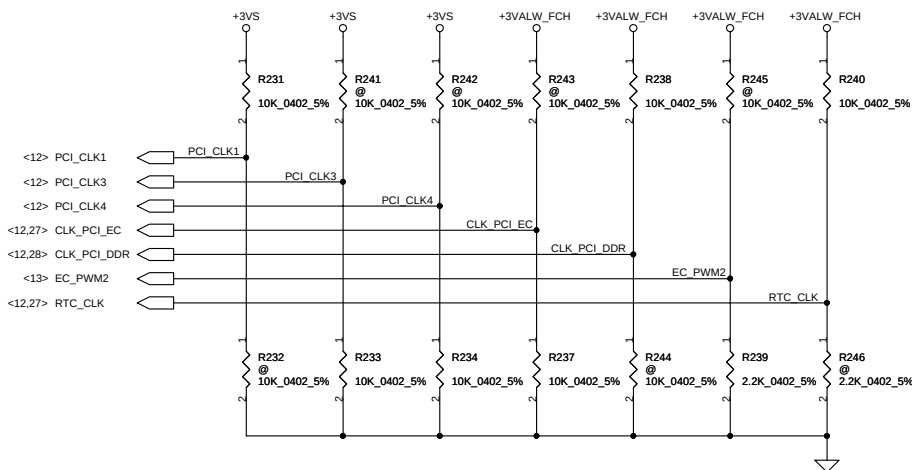
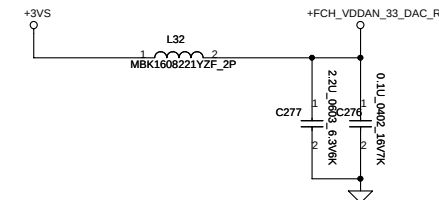


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STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

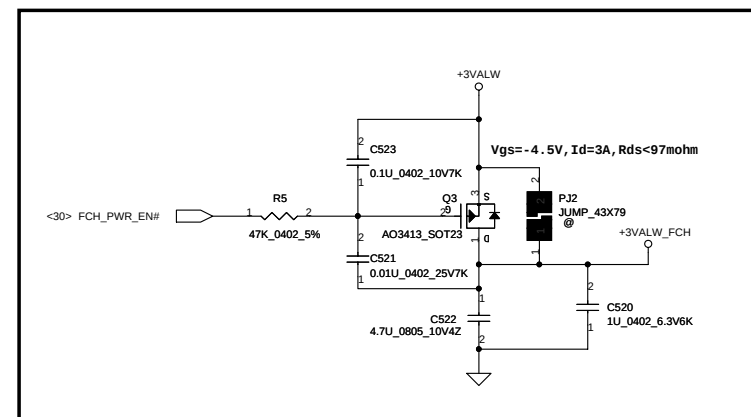
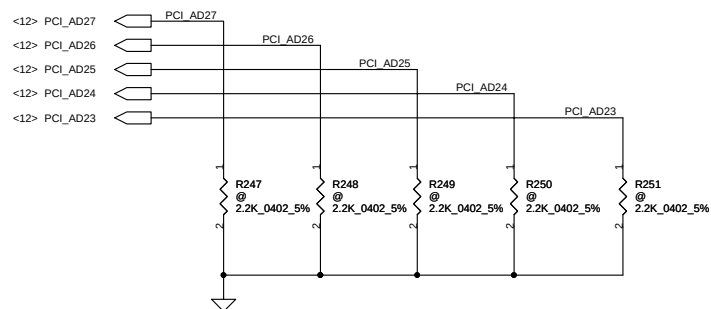
CRT Power Down Circuit



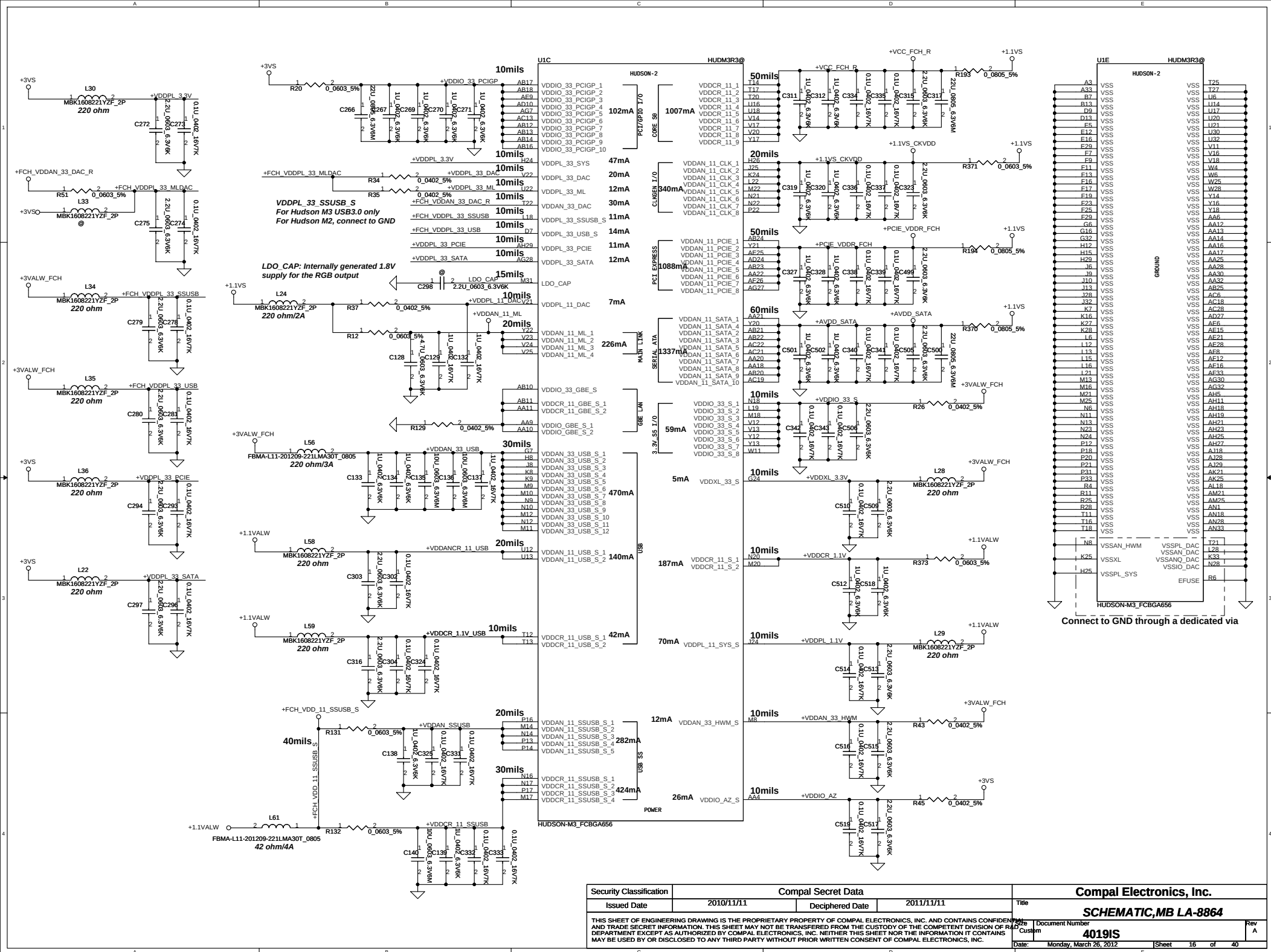
DEBUG STRAPS

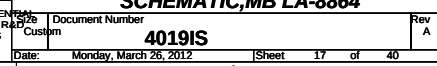
FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

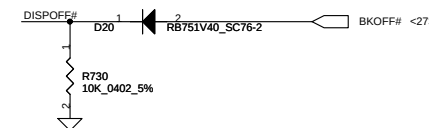
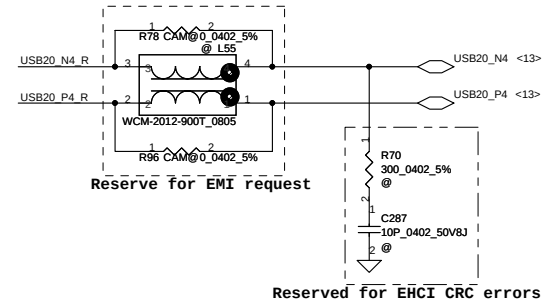
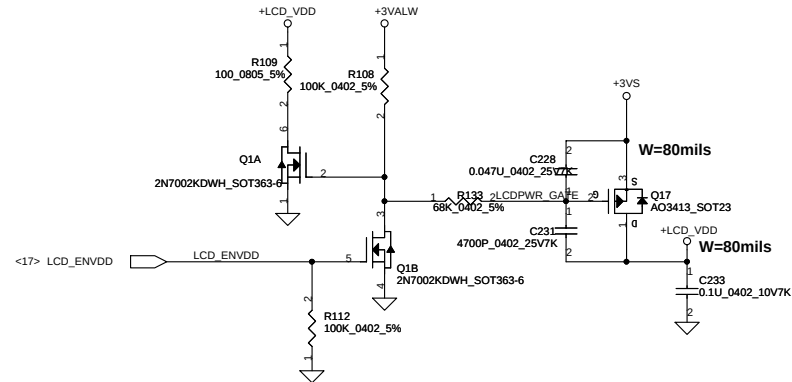
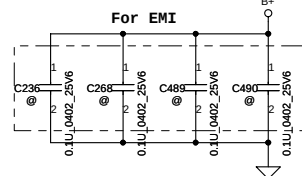
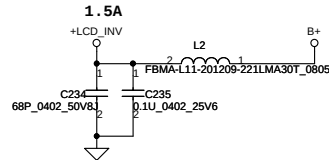
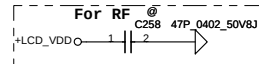
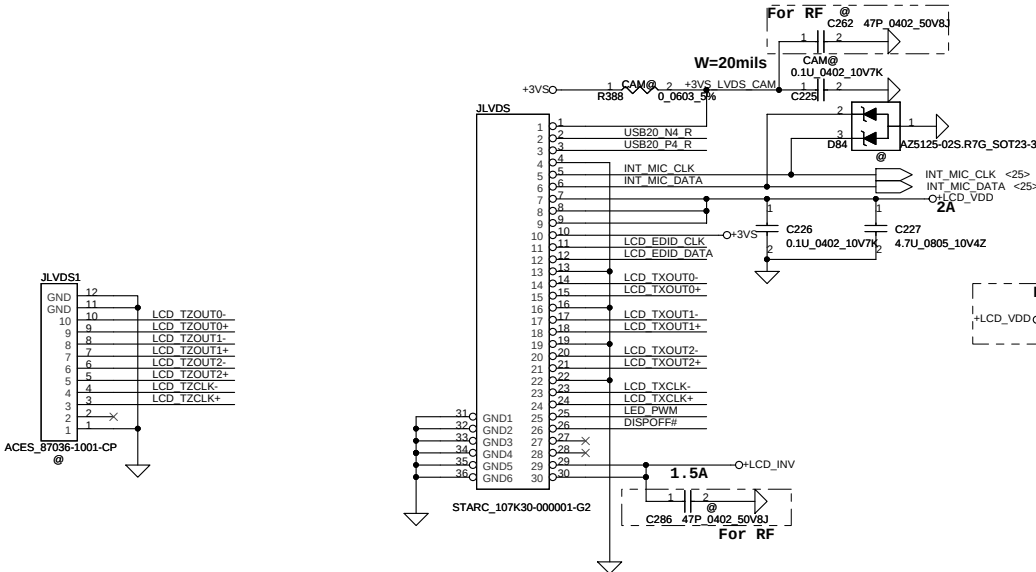
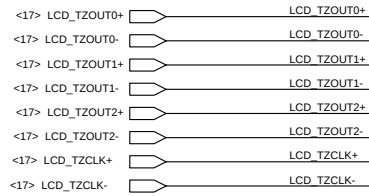
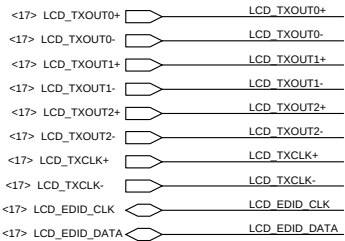
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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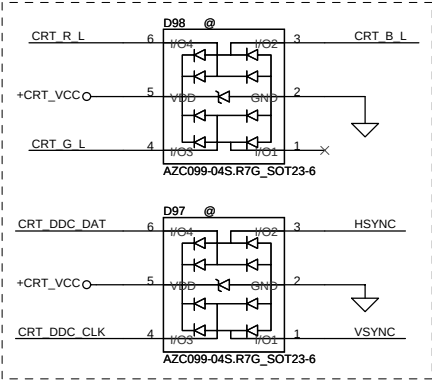
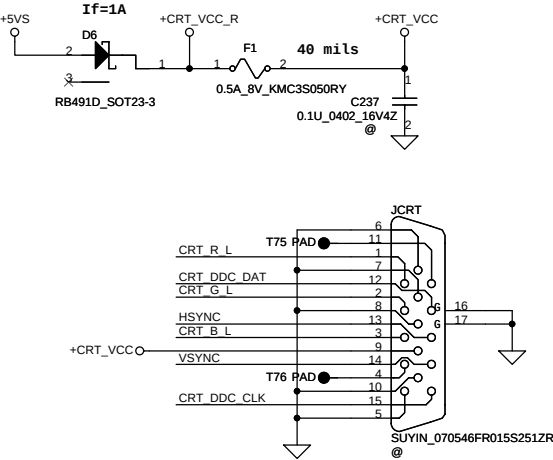
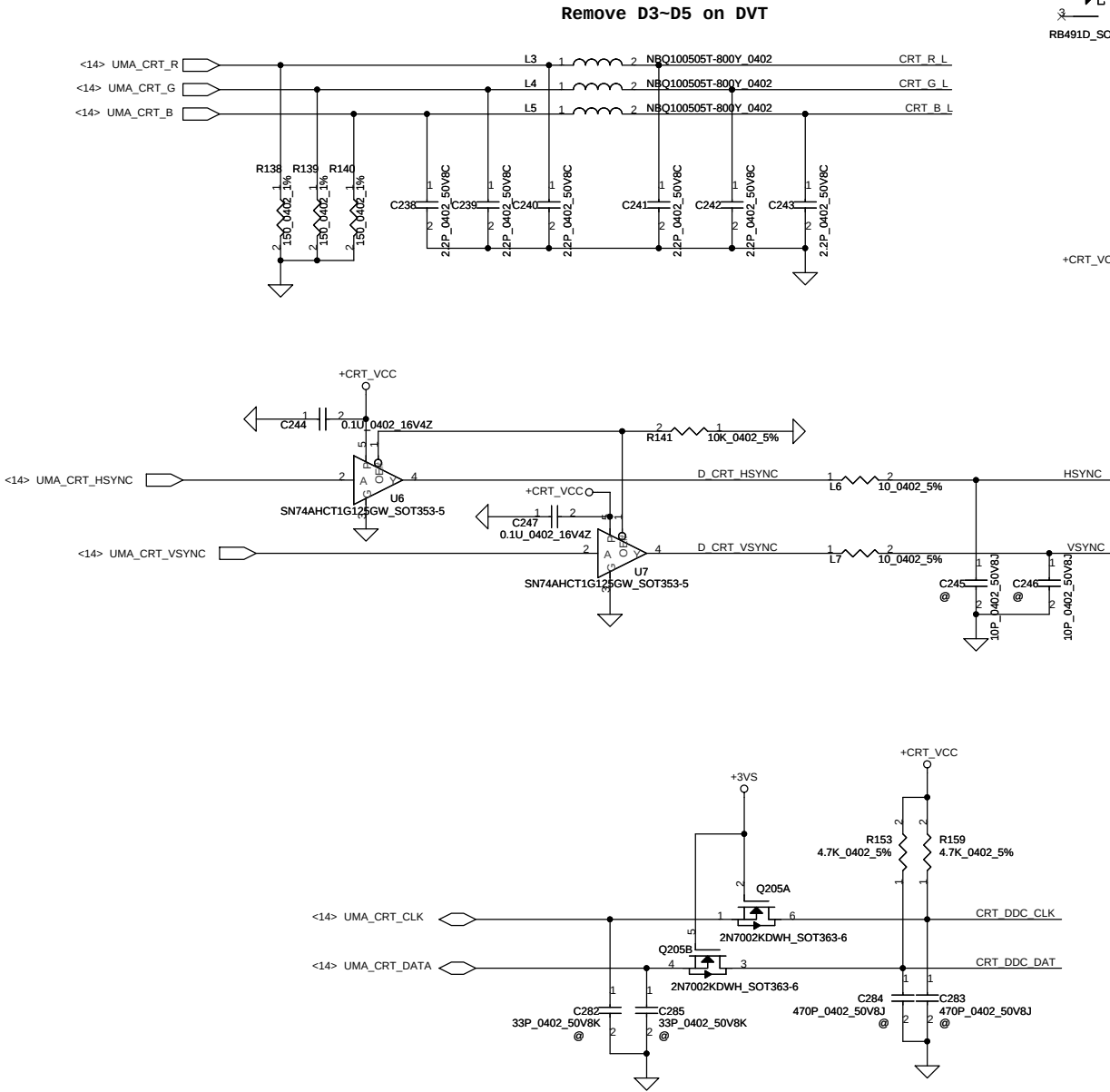






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								Document Number		4019IS	
								Date		Monday, March 26, 2012	
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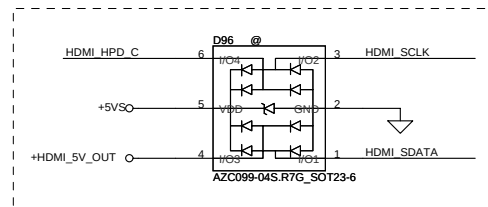
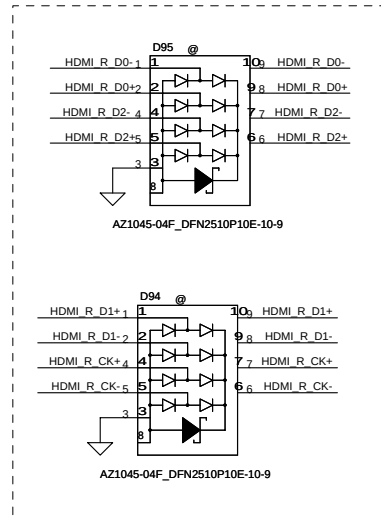
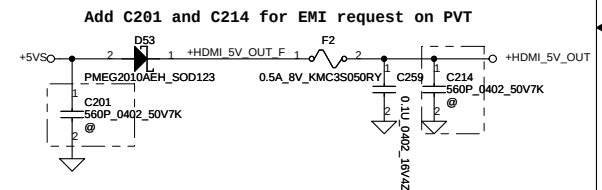
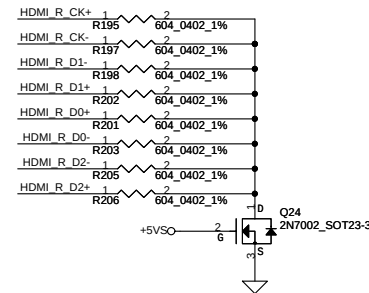
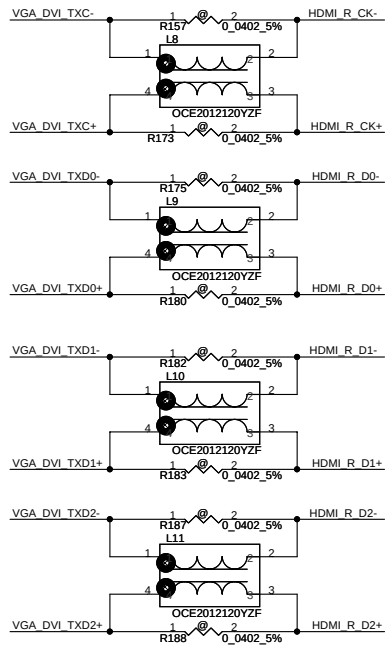
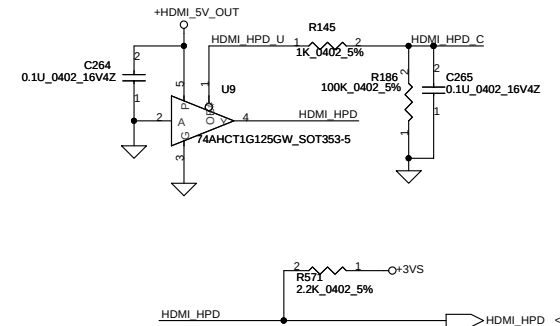
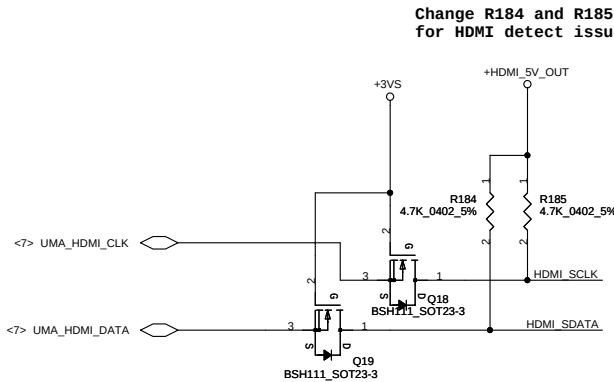
CRT CONNECTOR



Reserve ESD for CRT connector on DVT

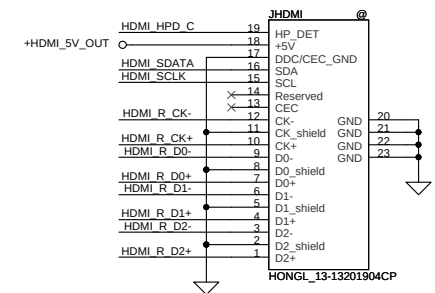
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<7> UMA_HDMI_TXC+	CV308	1	2	0.1U_0402_16V7K	VGA_DVI_TXC+
<7> UMA_HDMI_TXC-	CV304	1	2	0.1U_0402_16V7K	VGA_DVI_TXC-
<7> UMA_HDMI_TX0+	CV306	1	2	0.1U_0402_16V7K	VGA_DVI_TXD0+
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<7> UMA_HDMI_TX1+	CV303	1	2	0.1U_0402_16V7K	VGA_DVI_TXD1+
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<7> UMA_HDMI_TX2+	CV307	1	2	0.1U_0402_16V7K	VGA_DVI_TXD2+
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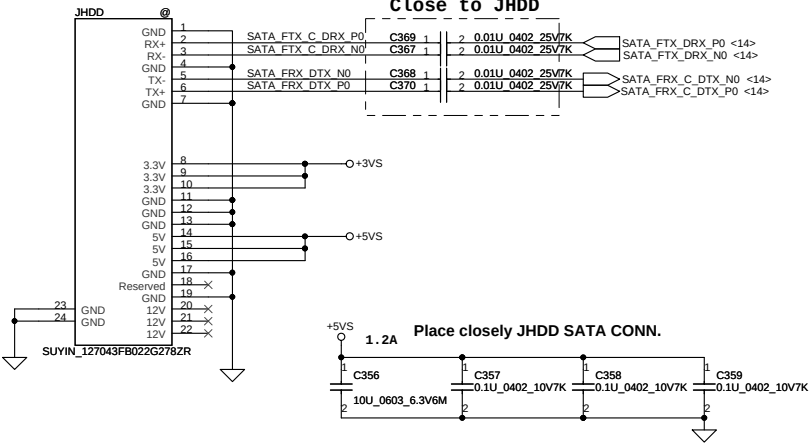
Reserve ESD for HDMI conn. on DVT

HDMI Connector

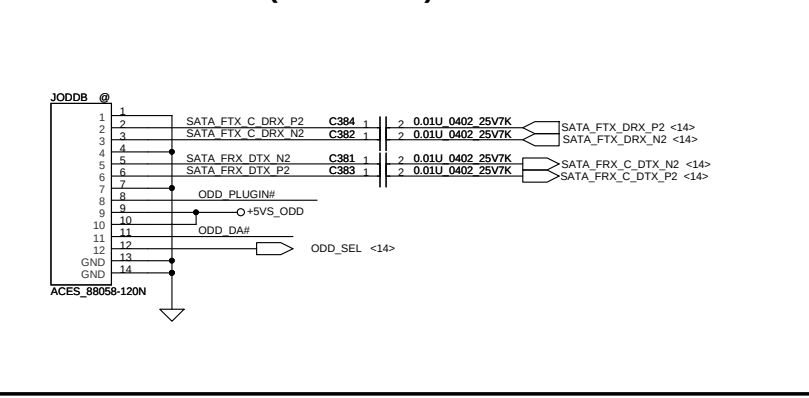


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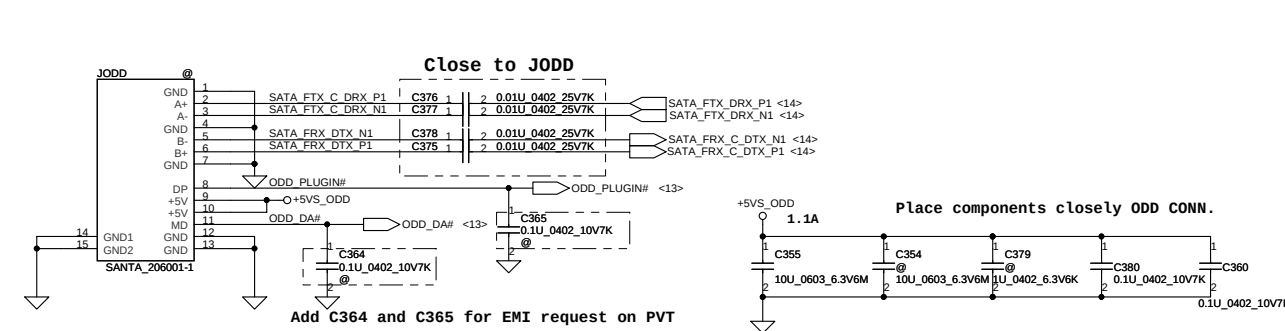
SATA HDD Conn.



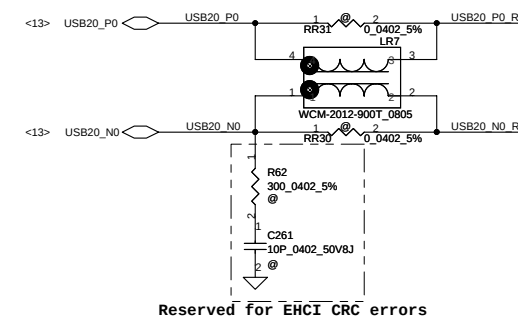
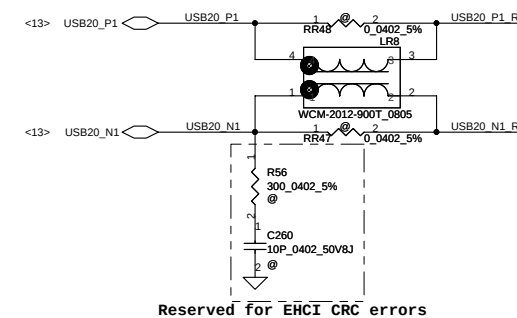
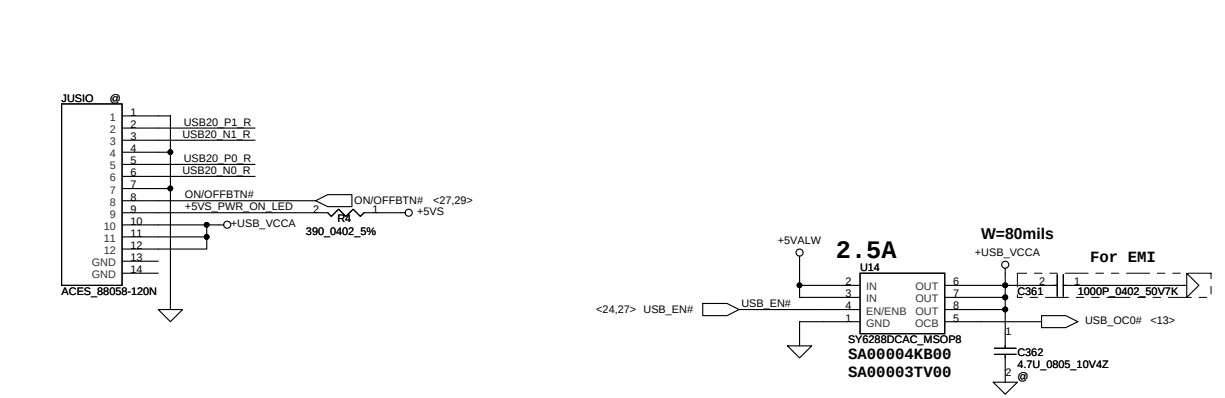
SATA ODD Conn (for 15"/17")



SATA ODD Conn (for 14")



Power Button & RUSB connector



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40 mils

For SED

16V4Z

CM2

CM3

CM5

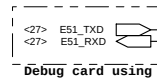
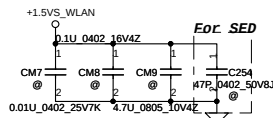
5V7K

4.7U_0805

10V4Z

47P

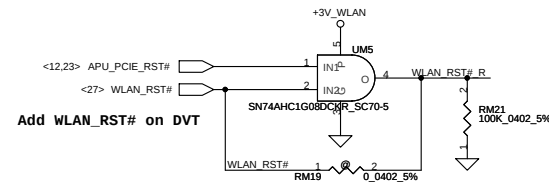
0402 50k



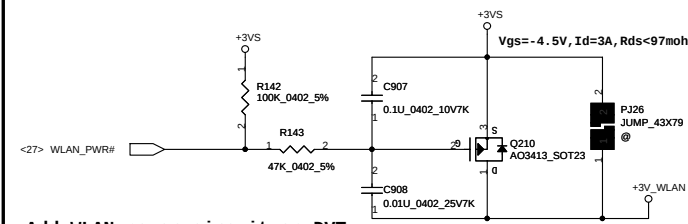
**Change JWLAN symbol to
SP07000TB00 on DVT**

Reserved for EHCI CRC errors

For isolate BT_CTRL and Compal Debug Card.

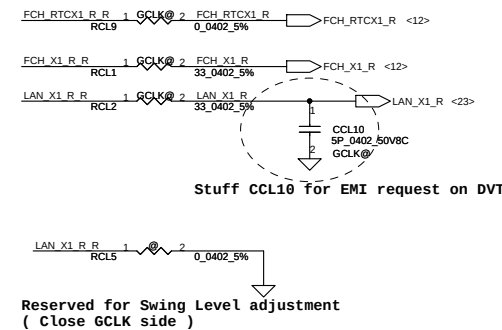
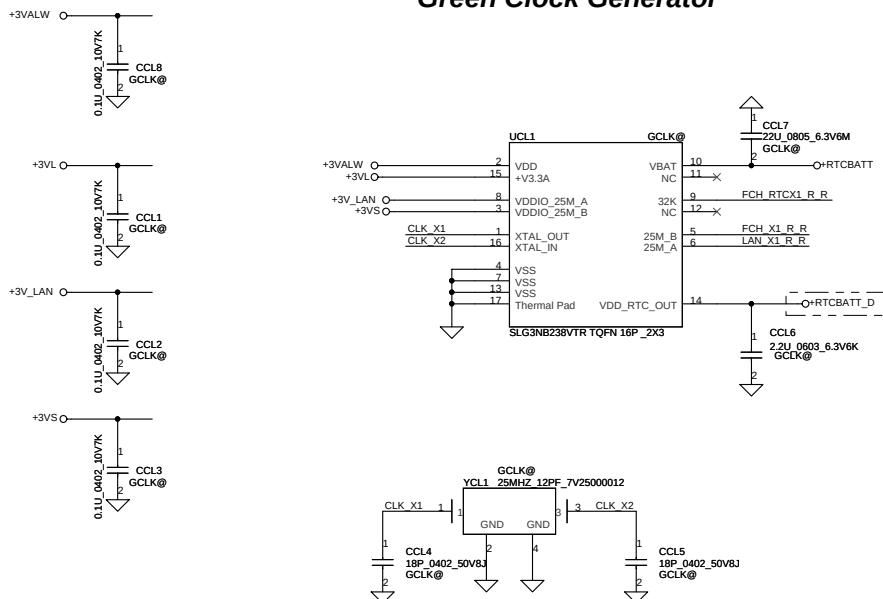


Add WLAN power circuit on DVT

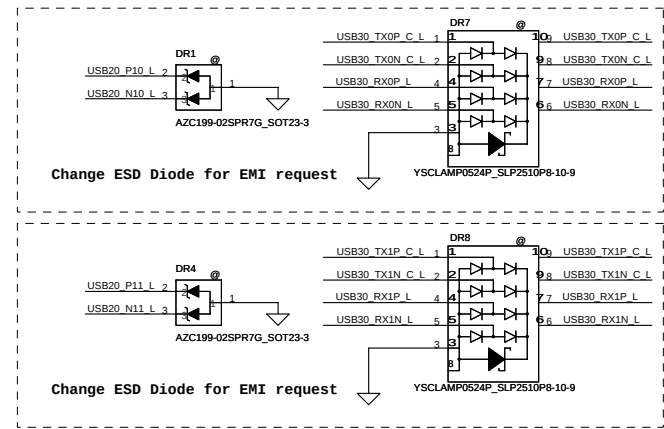
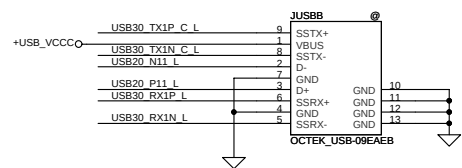
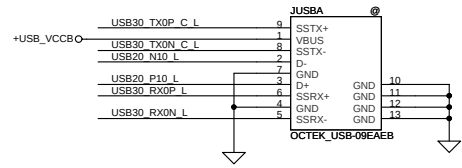
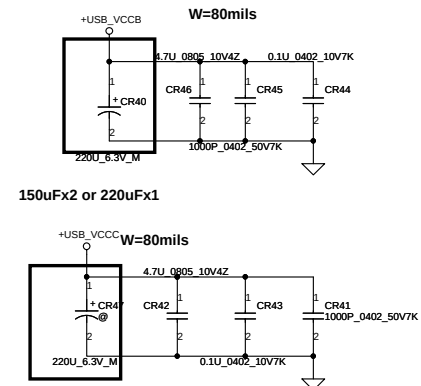
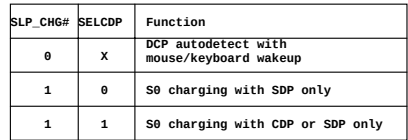


UCL1	
2	VDD
15	+V3.3A
8	VDDIO_25M_A
3	VDDIO_25M_B
CLK_X1	1 XTAL_OUT
CLK_X2	16 XTAL_IN
4	VSS
7	VSS
13	VSS
17	Thermal Pad
	VDD

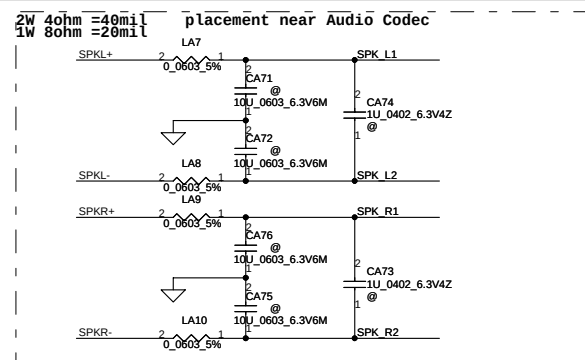
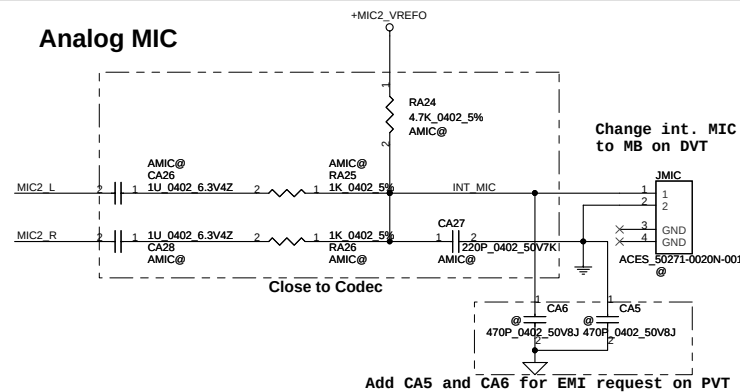
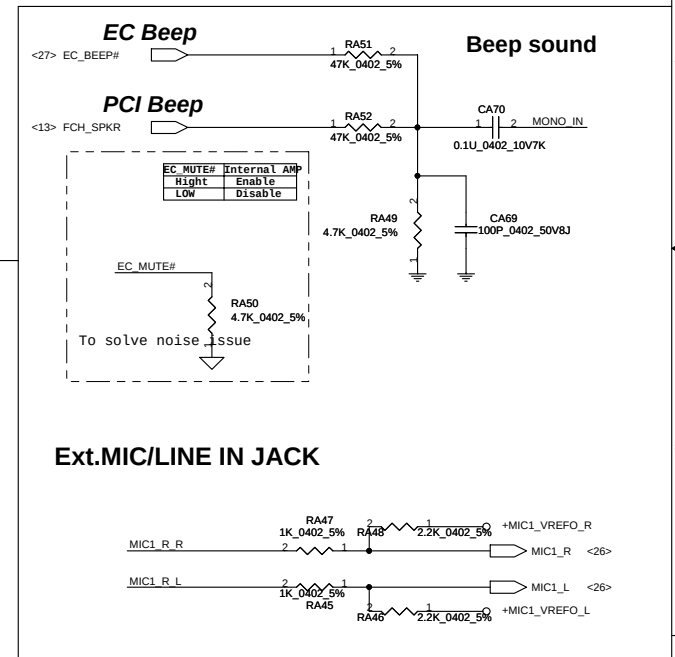
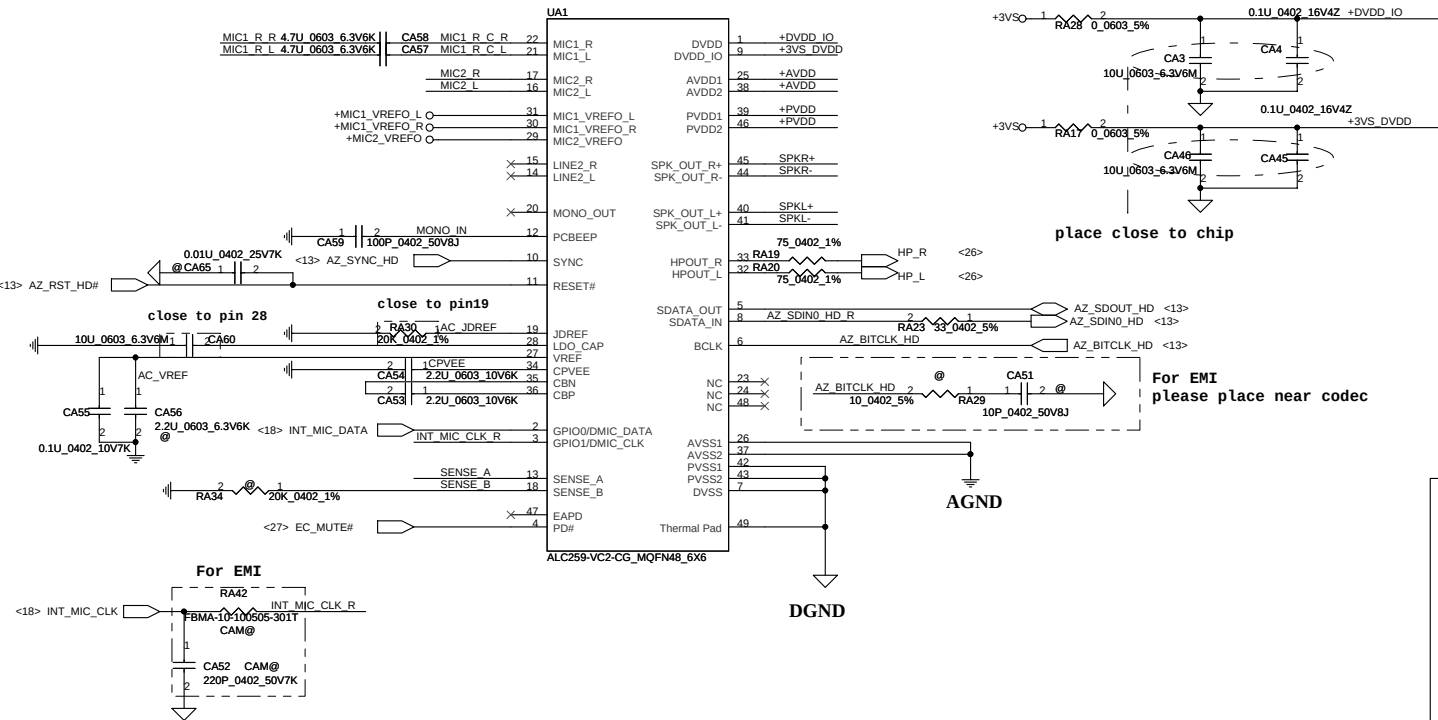
SLG3NB238VTR TQFN



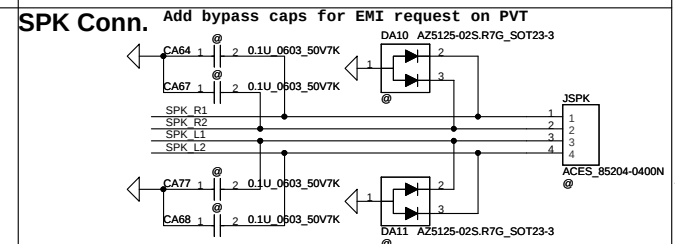
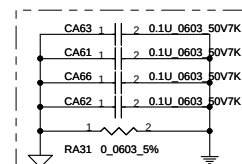
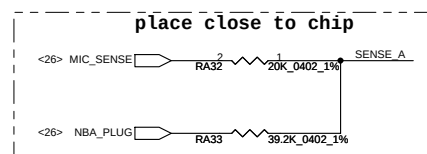
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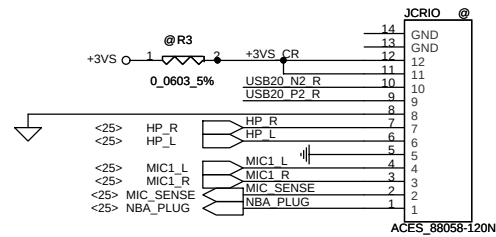
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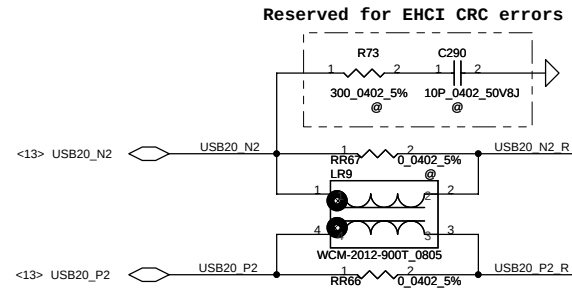
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



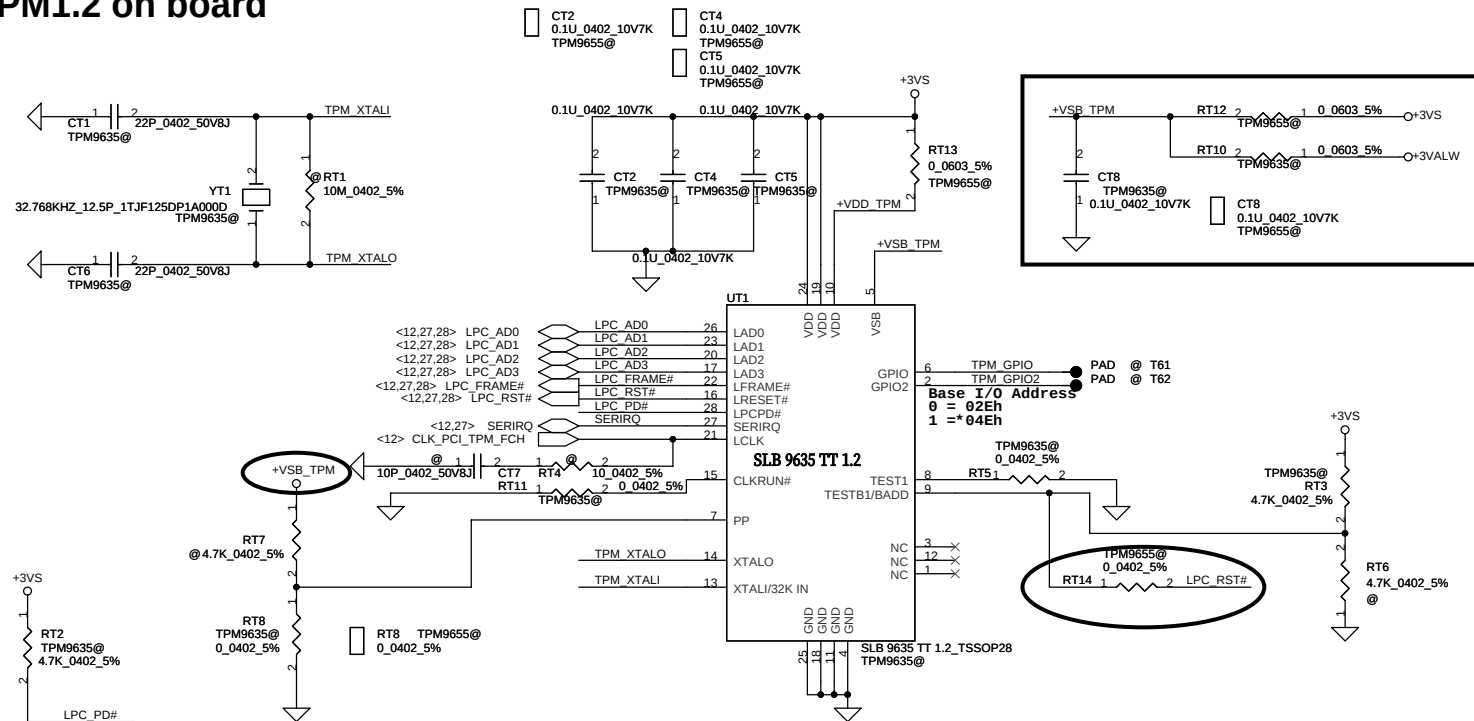
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CardReader & Audio Conn.

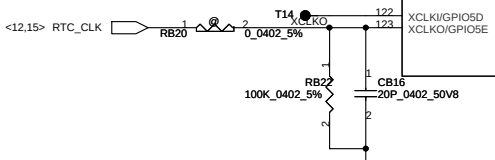
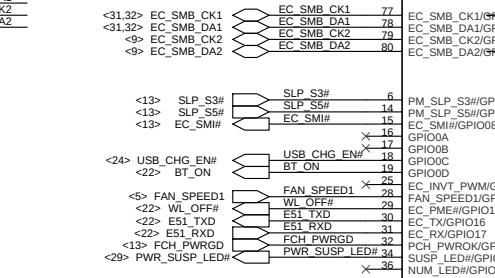
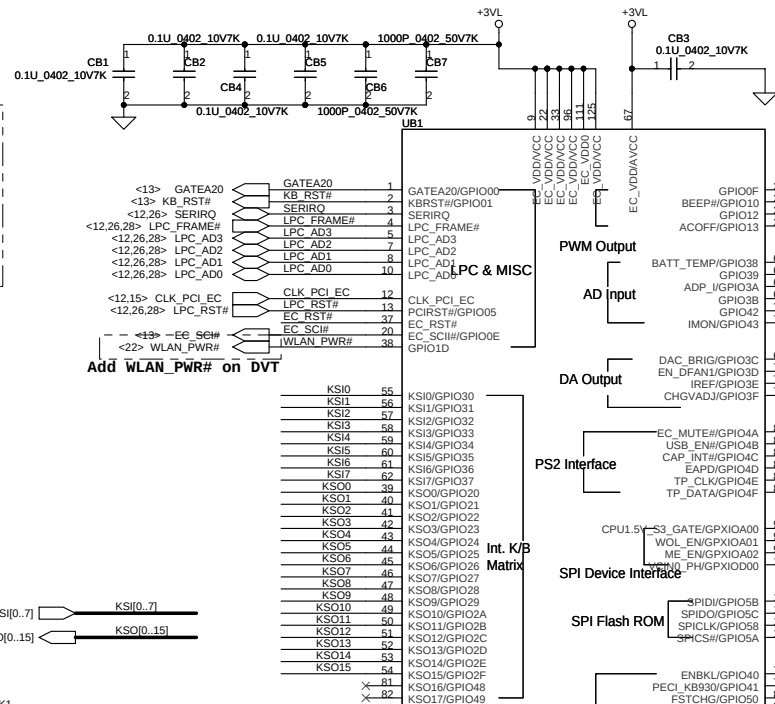
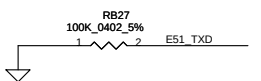
Update JCRI0 pin definition on DVT



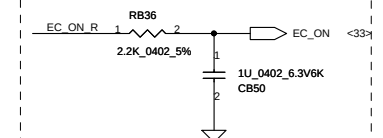
TPM1.2 on board



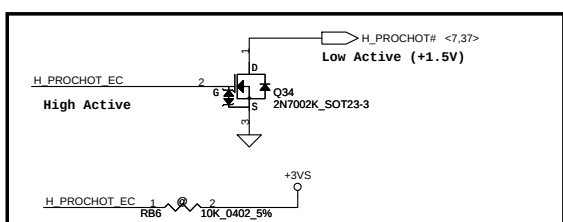
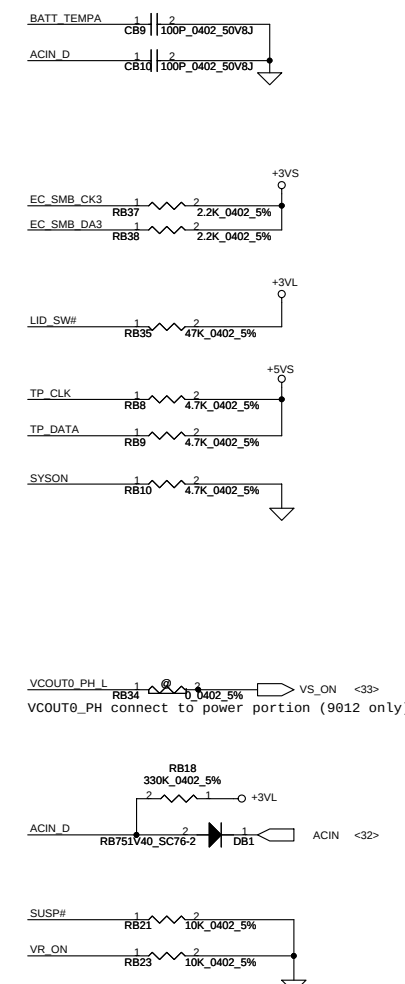
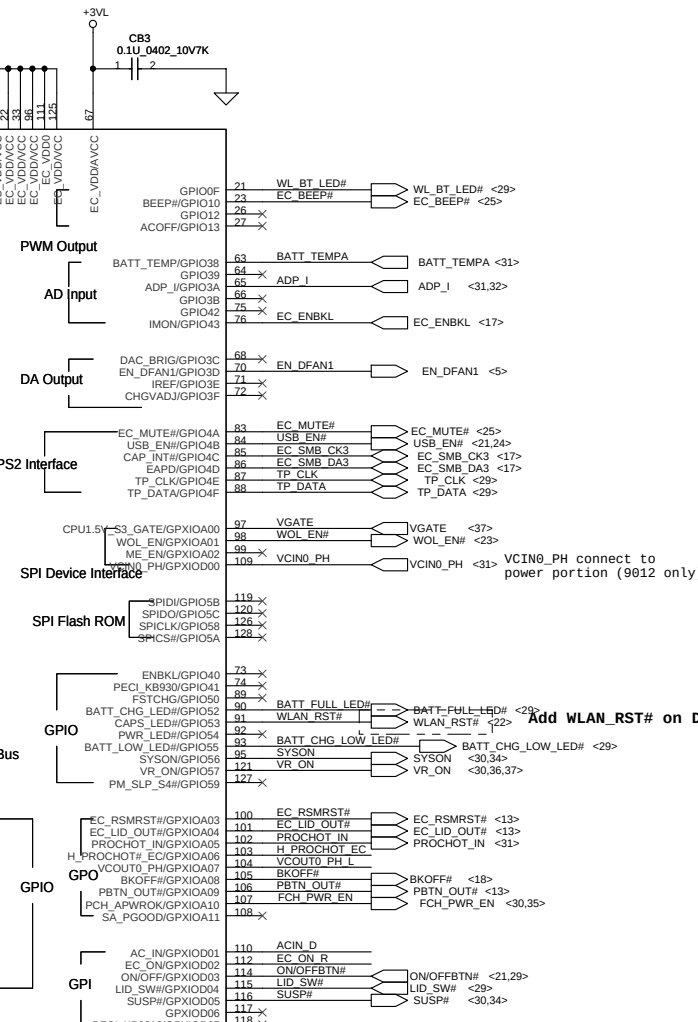
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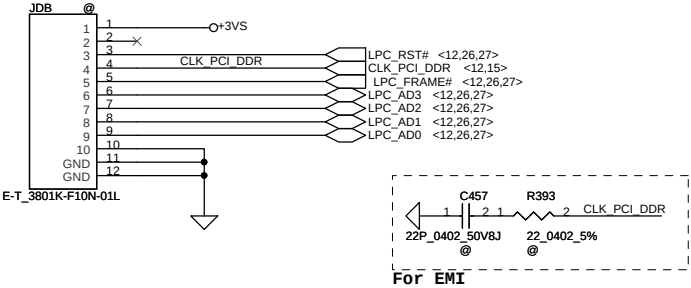
VCIN0 pin109 VCIN1 pin102	>1.2V	<1.2V
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



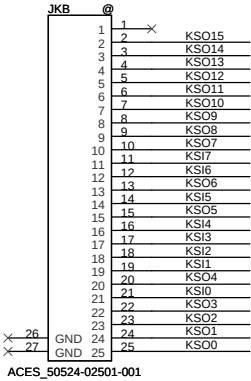
For KB9012-EC_ON low pulse work around



LPC Debug Port

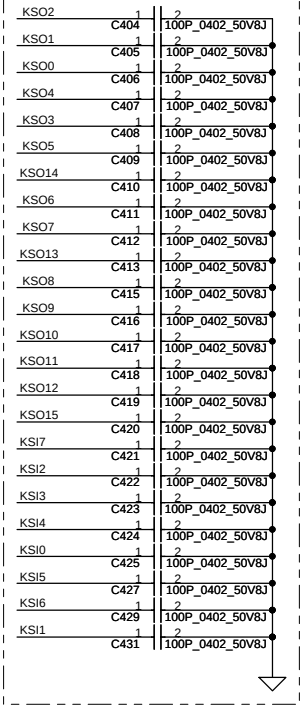


KEYBOARD CONN.



For EMI

close to JKB

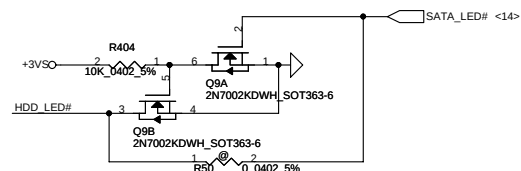


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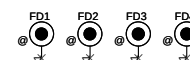


TP_DATA 2
TP_CLK 3
D89 @
YSDA0502C_SOT23-3
1

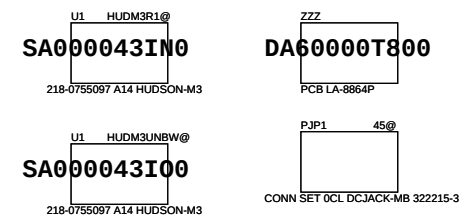
Place close to JT



PCB Federal Mark PAD

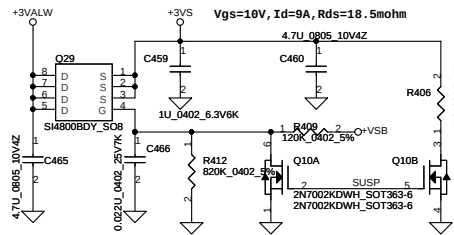


ISPD

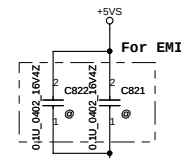
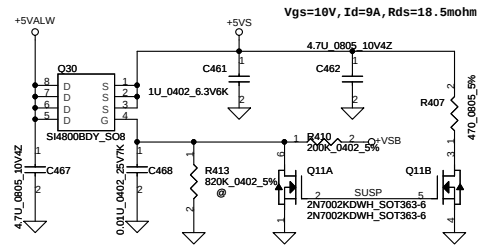


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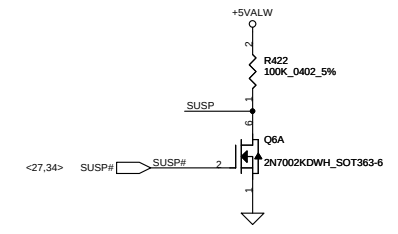
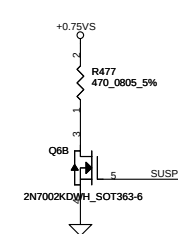
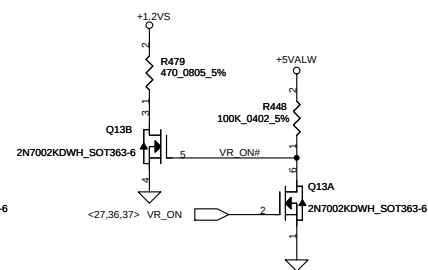
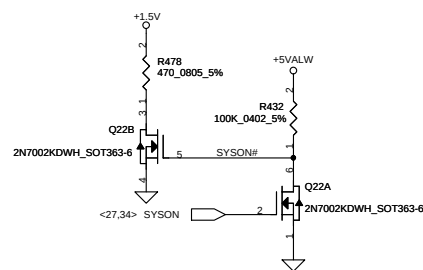
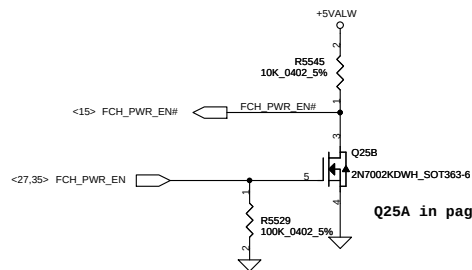
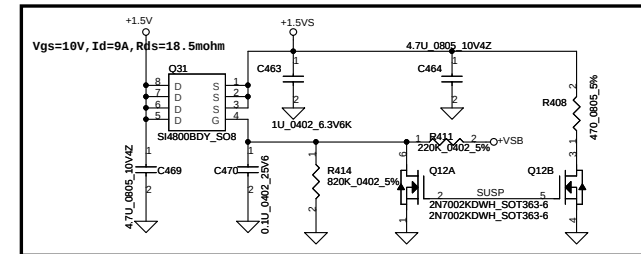
+3VALW T0 +3VS



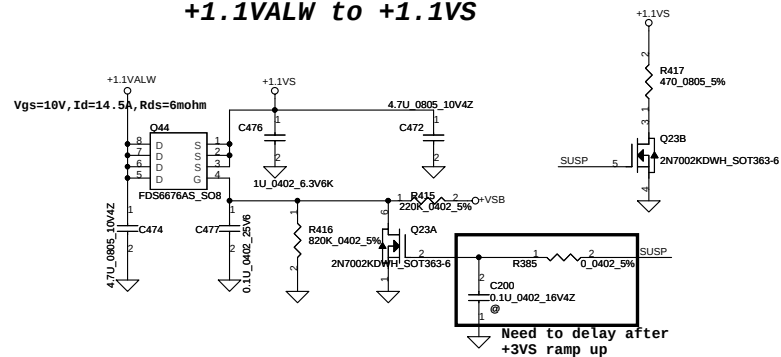
+5VALW TO +5VS



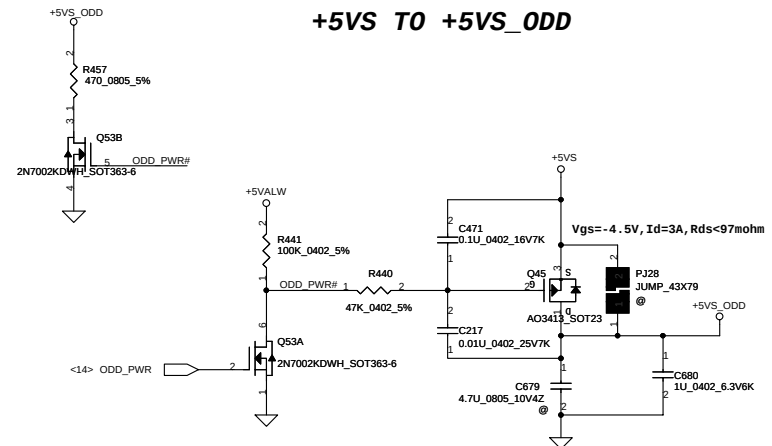
+1.5V to +1.5VS Change +1.5VS MOS
to Smaller Current ?



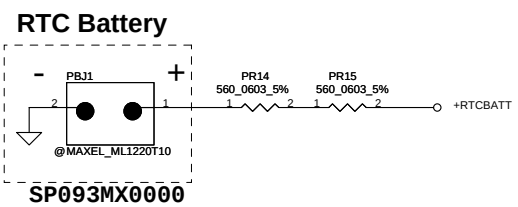
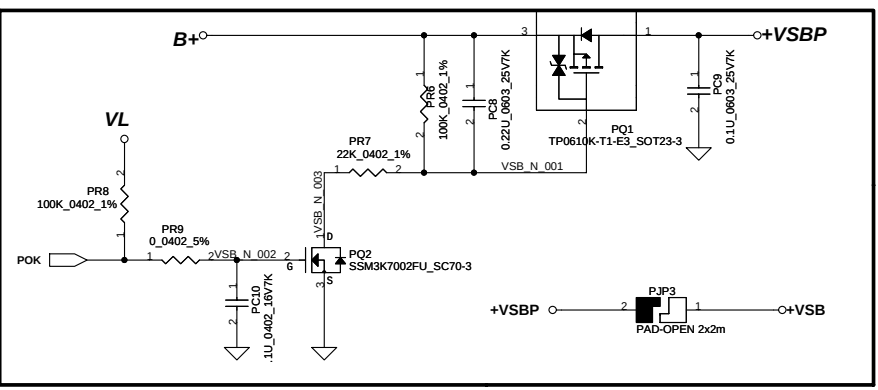
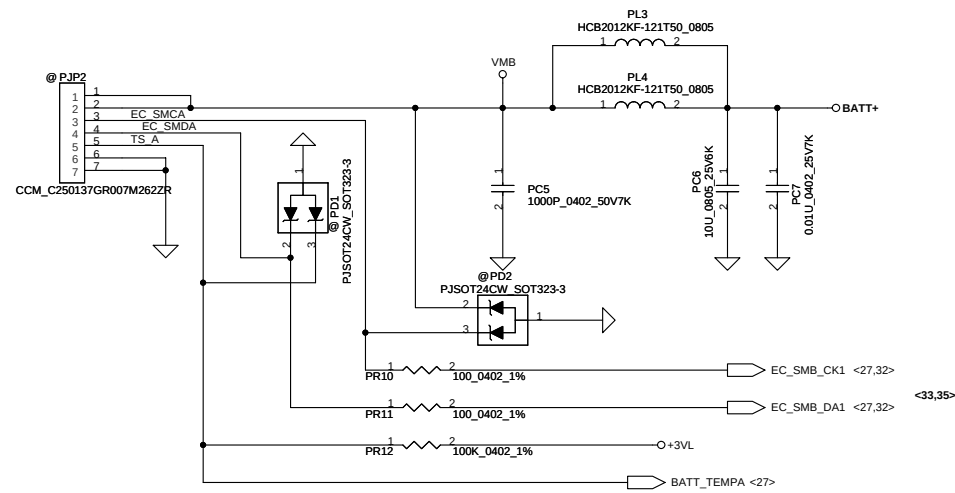
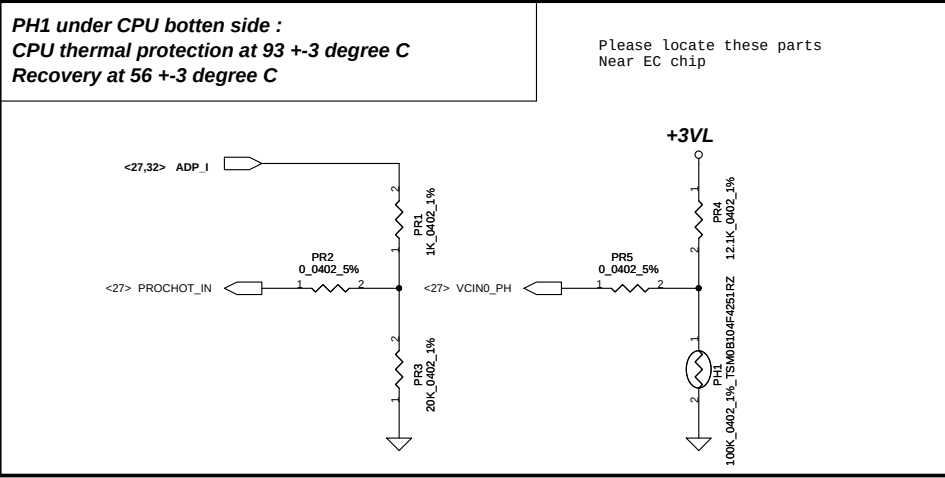
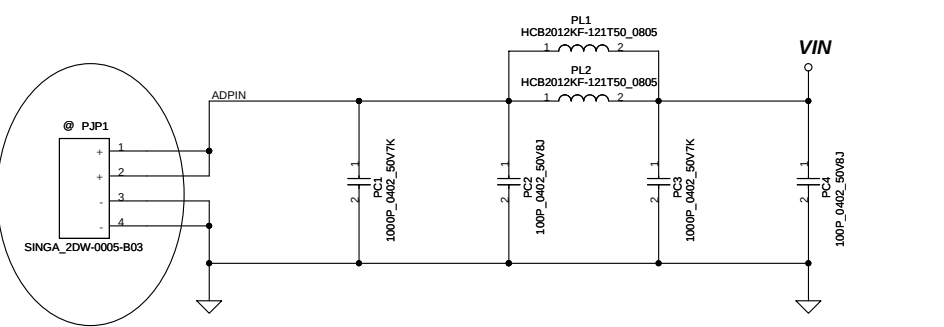
+1.1VALW to +1.1VS



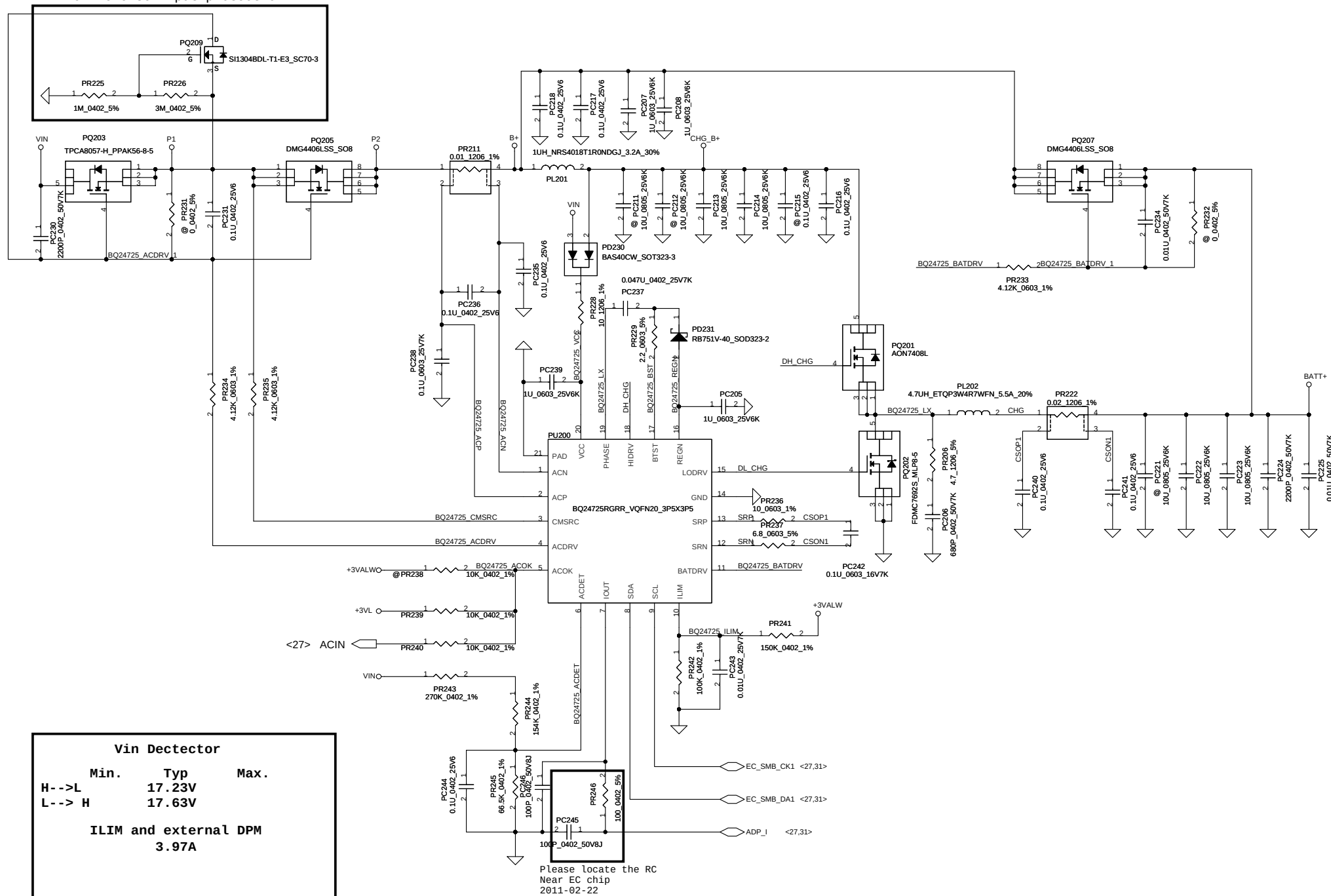
+5VS T0 +5VS_ODD

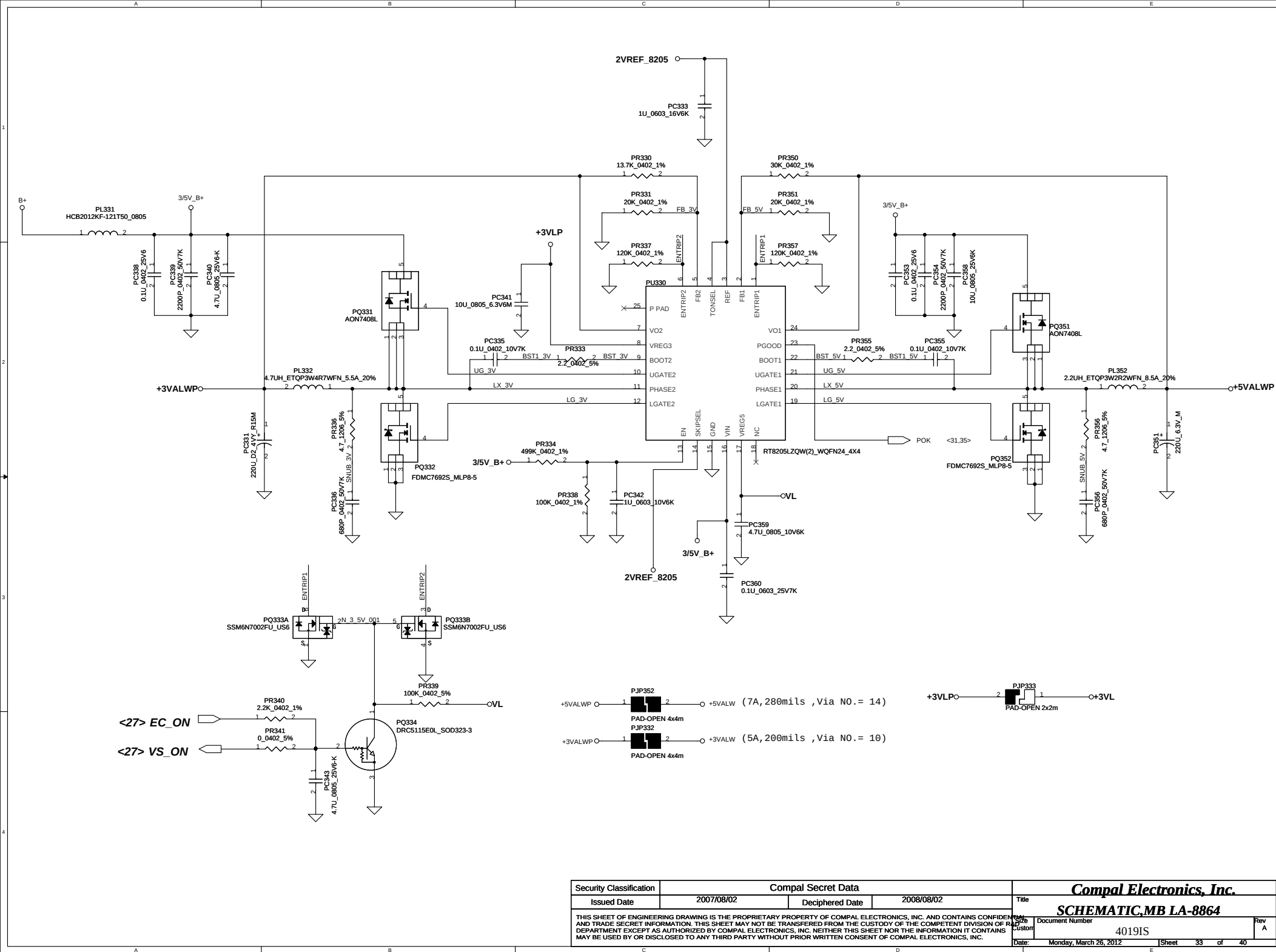


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for reverse input protection

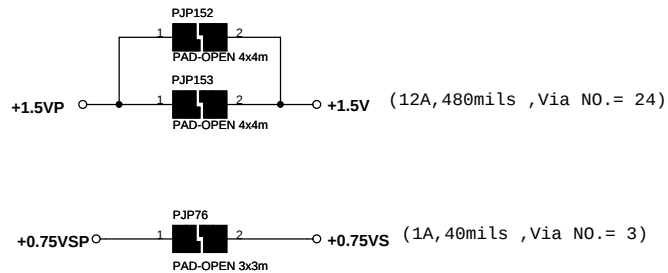




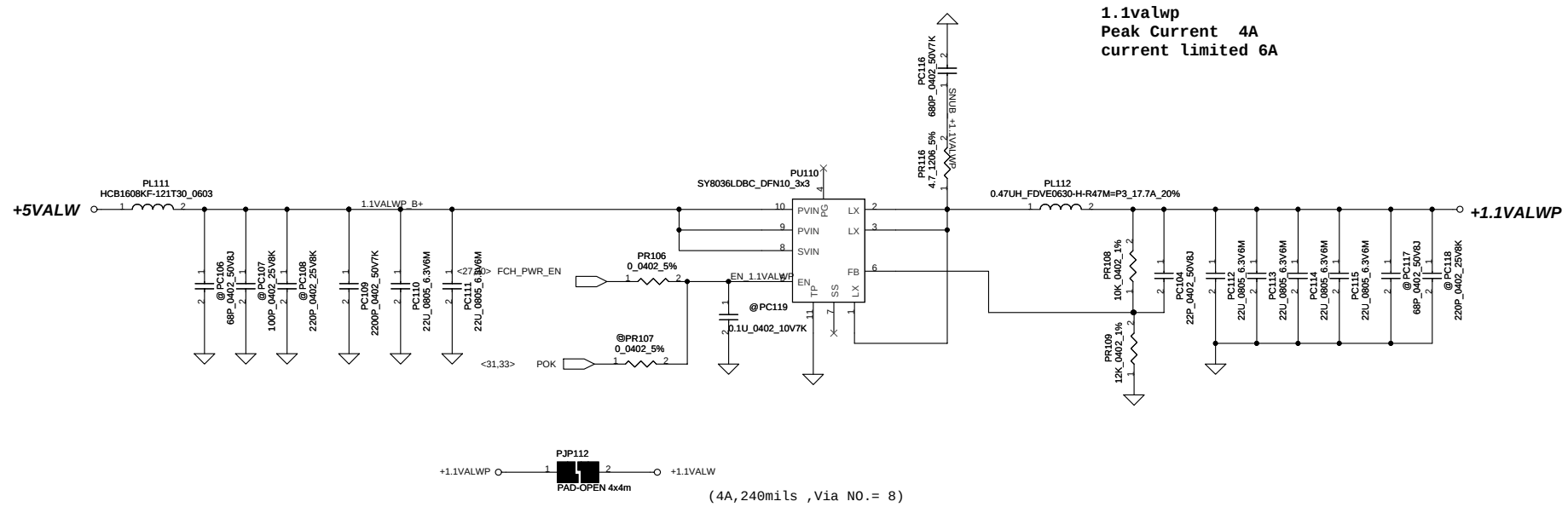
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Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

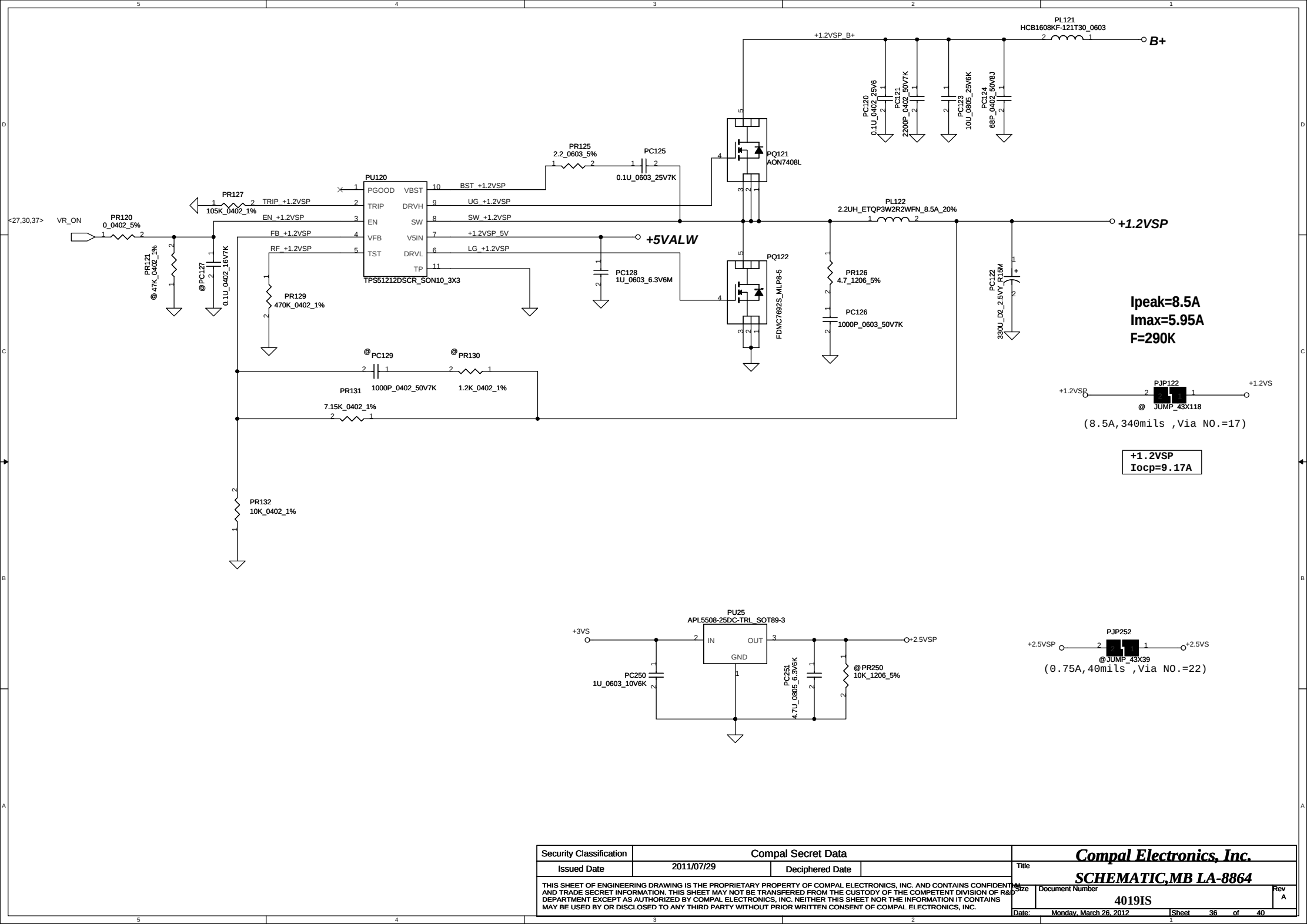
Note: S3 - sleep ; S5 - power off



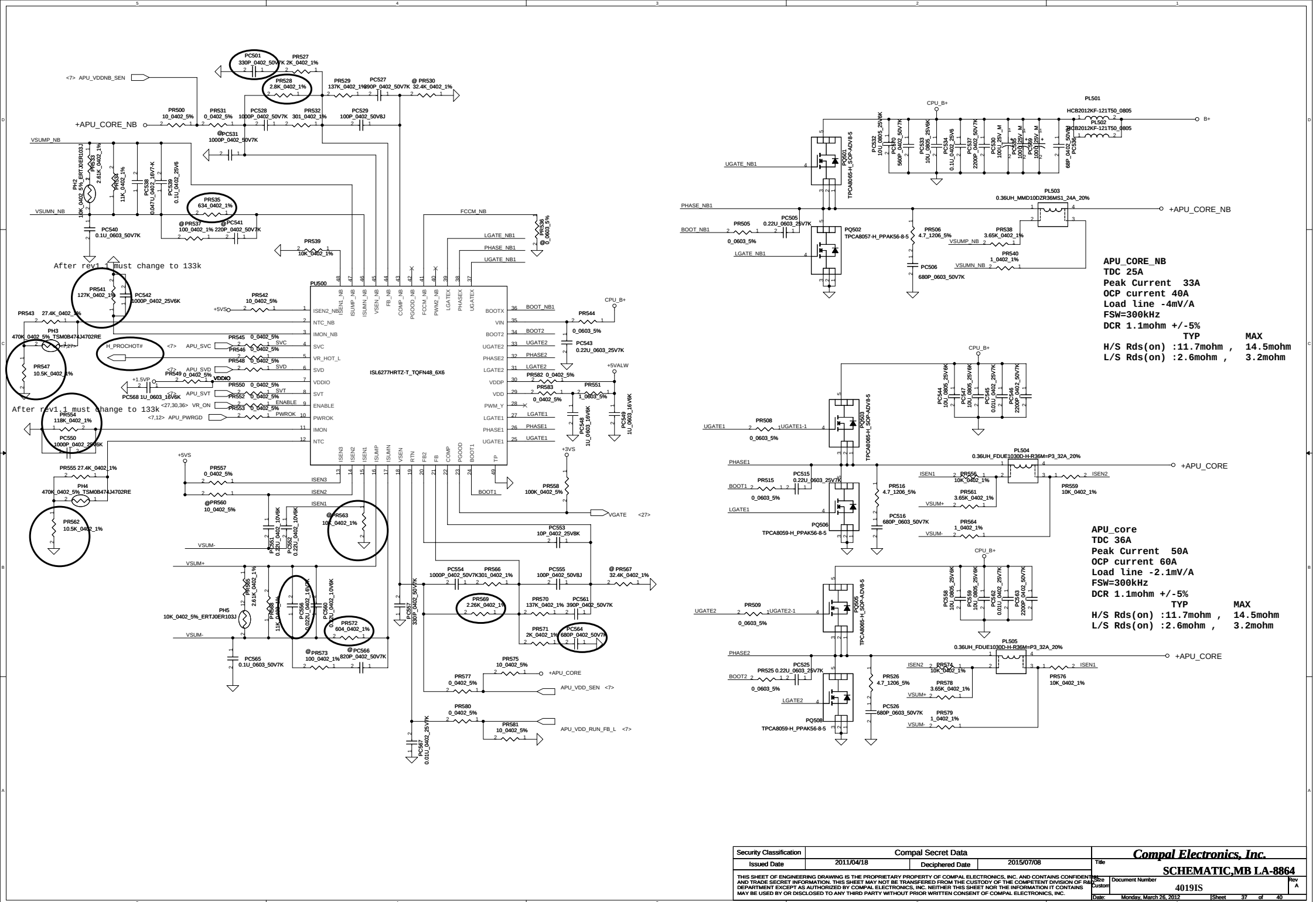
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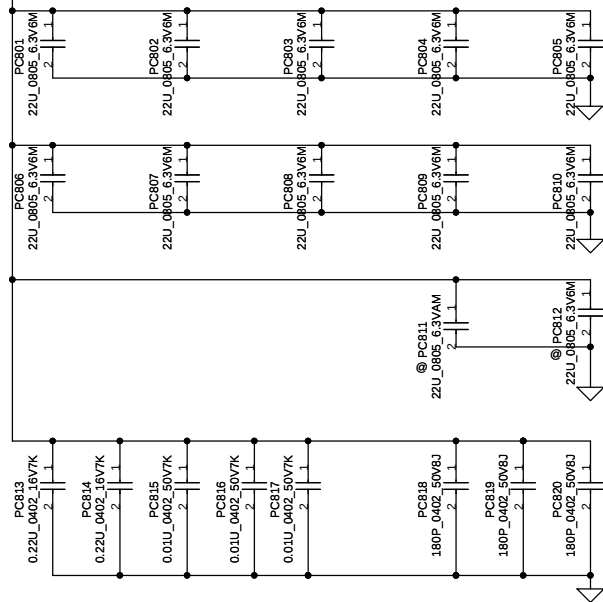
APU_CORE_NB
TDC 25A
Peak Current 33A
OCP current 40A
Load line -4mV/A
FSW=300kHz
DCR 1.1mohm +/-5%
TYP
H/S Rds(on) :11.7mohm , 14.5mohm
L/S Rds(on) :2.6mohm , 3.2mohm

APU_core
TDC 36A
Peak Current 50A
OCP current 60A
Load line -2.1mV/A
FSW=300kHz
DCR 1.1mohm +/-5%
TYP
H/S Rds(on) :11.7mohm , 14.5mohm
L/S Rds(on) :2.6mohm , 3.2mohm

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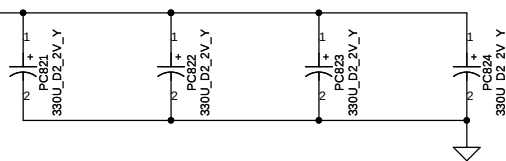
+APU_CORE

+APU_CORE



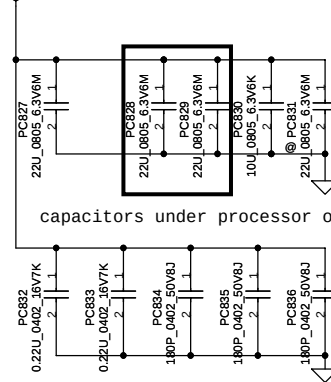
+APU_CORE

Local



+APU_CORE_NB

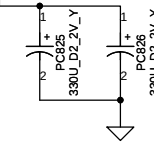
+APU_CORE_NB



capacitors under processor on bottom side of board

+APU_CORE_NB

Local



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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2012/01/04	P31-PWR-DCIN/BATT CONN/OTP	Change PQ1 to SB9006100280	Change source
2.	2012/01/04	P32-PWR-CHARGER	Change PQ209 to SB00000GC10,PQ203 to PCA8057 PQ202 to FDMC7692,PR241 to150K,PR243 to 270K Change PC211,PC212 to unmount ,add PC206,PR206	Change source Circuit modify
3.	2012/01/04	P33-PWR-3.3VALWP/5VALWP	Change PR350 to 30K,PR351 to 20K,PR337,PR357 to120K add PC336,PR336,PC356,PR356	Circuit modify
4.	2012/01/04	P34-PWR-1.5VP/+0.75VSP	Add PR156,PC156	
5.	2012/01/04	P37-PWR +CPU_CORE	Change PL503 to SH00000HD00,PQ502 to TPCA8057	Change source

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HW PIR (Product Improve Record)

QMLE4 LA-8864P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2012/02/13

Item	Date	Page	Solution	Request
1.	1/10	P23	Add PJ31	For saving power consumption
2.	1/12	P29	Change JTP symbol to SP01001BF10	For ME request
3.	1/30	P25	Add internal MIC to MB	For customer request
4.	1/31	P23	Swap UL3 MDI0 and MDI1	For LAN trace routing
5.	2/1	P22	Add PJ33, WLAN power circuit and reset pin	For customer request
6.	2/2	P26	Update JCRI0 pin definition	Change int. MIC to MB
7.	2/2	P25	Remove CA64, add RA32 and RA33	Move sense resistors to MB
8.	2/3	P22	Change JWLAN symbol to SP07000TB00	For ME request
9.	2/3	P27	Add WLAN_PWR# and WLAN_RST#	For customer request
10.	2/8	P23	Add test point TL1 for pin37	For vendor request
11.	2/8	P29	Add screw H17, H20 and H21	For ME request
12.	2/9	P10	Change C218 from 390U to 330U (SF000002080)	For cost down
13.	2/9	P20	Reserve ESD D94-D96 for HDMI	For ESD request
14.	2/9	P19	Remove D3-D5 and add D97 and D98	For ESD request
15.	2/9	P23	Reserve ESD D99 and D100 for LAN	For ESD request
16.	2/9	P21	Add resistors to improve SATA signal quality	For SATA ODD co-layout
17.	2/10	P7	Stuff C126 and C127	For EMI request
18.	2/10	P22	Stuff CCL10	For EMI request
19.	2/10	P7	Reserve R77 and R85	For DeepS3 leakage
20.	2/21	P23	Change UL3 and UL4 PN to SP050006N00	For EMI request

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2012/03/12

Item	Date	Page	Solution	
1.	3/1	P12	Update RTC scematic	For avoiding +3VL short to GND
2.	2/29	P22	Change R108 pull-high from +3VS to +3VALW	For LVDS sequence issue
3.	3/7	P26	Add R292 and reserve R293	To avoid PXS_PWREN floating
4.	3/7	P7	Unstuff R121-R124,R118,R119	For debug use
5.	3/7	P27	Update U13 footprint	
6.	3/7	P27/30	Connect SATA port2 to 15"ODD connector, and add GPIO54	To solve SATA EA fail issue
7.	3/8		Change RB20, RB34, R3, RV102, R425, R136, R31, R32, R33, RV284, RV287 R62, RV277 to short pad	
8.	3/12	P20	Add C201 and C214	For EMI request
9.	3/12	P21	Add C364 and C365	For EMI request
10.	3/12	P25	Add CA5, CA6, CA64, CA67, CA68 and CA77	For EMI request
11.	3/14	P8	Add C147 co-layout with C100	To avoid damage by SMT process
12.	3/14	P10	Add C148 co-layout with C218	To avoid damage by SMT process