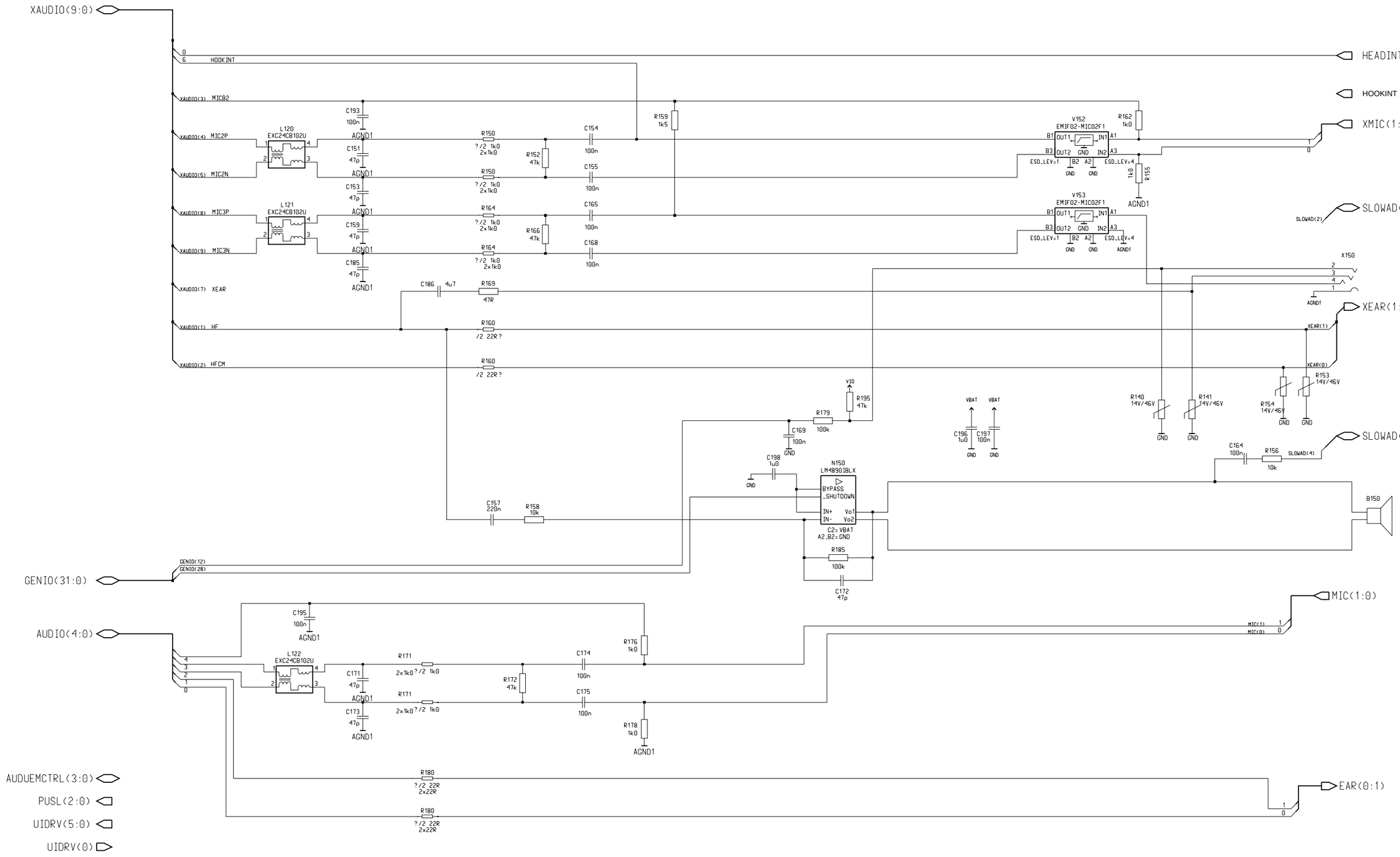
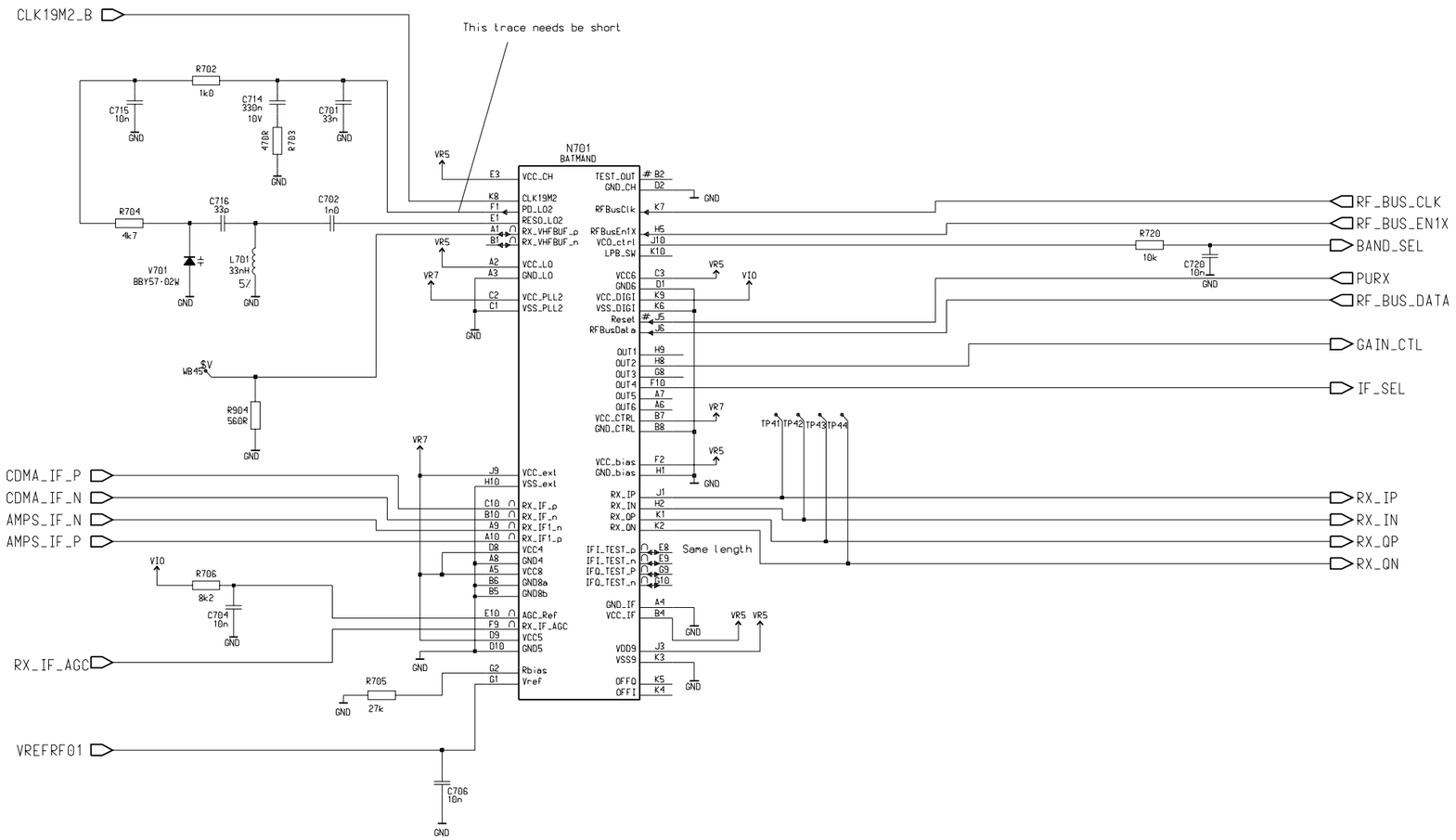
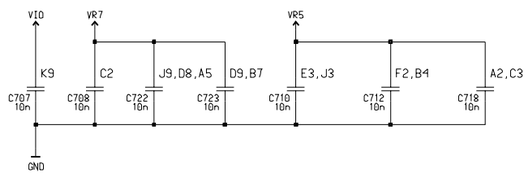
Audio

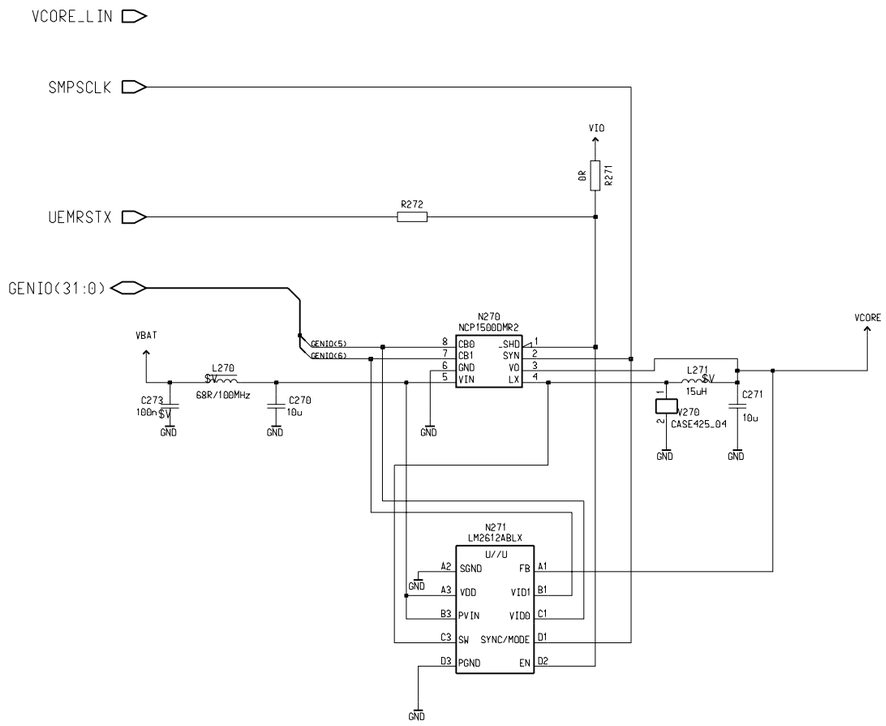

XAUDIO(9:0)
HEADINT
HOOKINT
XMIC(1:0)
SLOWAD(6:0)
XEAR(1:0)
SLOWAD(6:0)
MIC(1:0)
EAR(0:1)
GENIO(31:0)
AUDIO(4:0)
AUDUEMCTRL(3:0)
PUSL(2:0)
UIDRV(5:0)
UIDRV(0)
L120 EXC24CB102U
L121 EXC24CB102U
L122 EXC24CB102U
V152 EMIF02-MIC02F1
V153 EMIF02-MIC02F1
N150 LM4890IBLX
BYPASS
SHUTDOWN
IN+ Vo1
IN- Vo2
C2=VBAT
A2,B2=GND
B150
X150
AGND1
GND
VBAT
V10
HF
HFCM
XEAR
MIC2P
MIC2N
MIC3P
MIC3N
MICB2
HOOKINT

Circuit Diagram of RX (Batman)



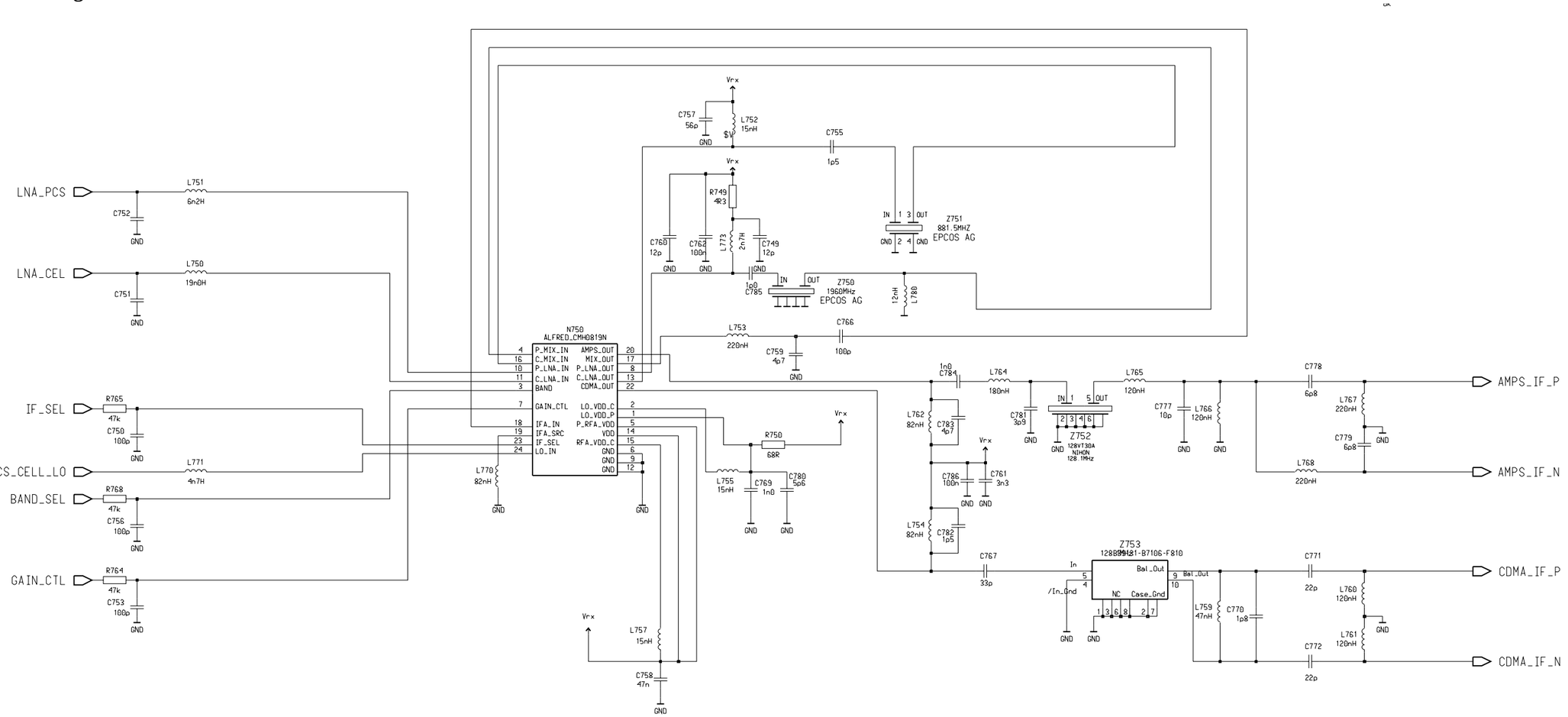


DC-DC Converter



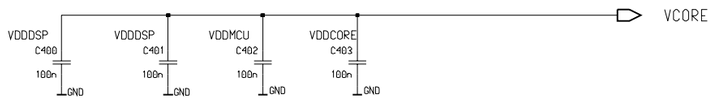
Circuit Diagram of Test and Emulator Interface

Circuit Diagram of RX front end

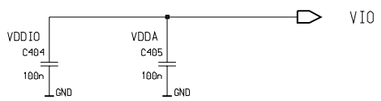


	LOGIC INPUTS		
MODES	BAND	GAIN_CTL	IF_SEL
CEL CDMA Hi Gain	0	1	0
CEL CDMA Lo Gain	0	0	0
PCS CDMA Hi Gain	1	1	0
PCS CDMA Lo Gain	1	0	0
AMPS Hi Gain	0	1	1
AMPS Lo Gain	0	0	1

UPP Decoupling Diagram

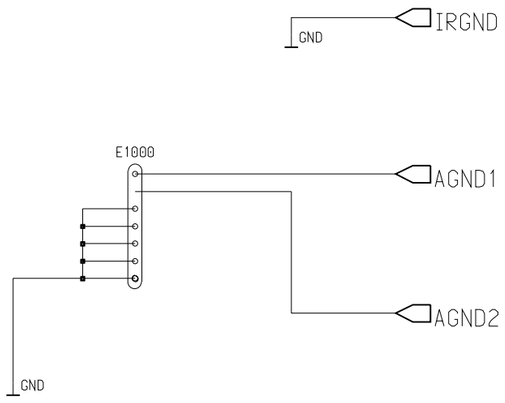


Place caps near UPP

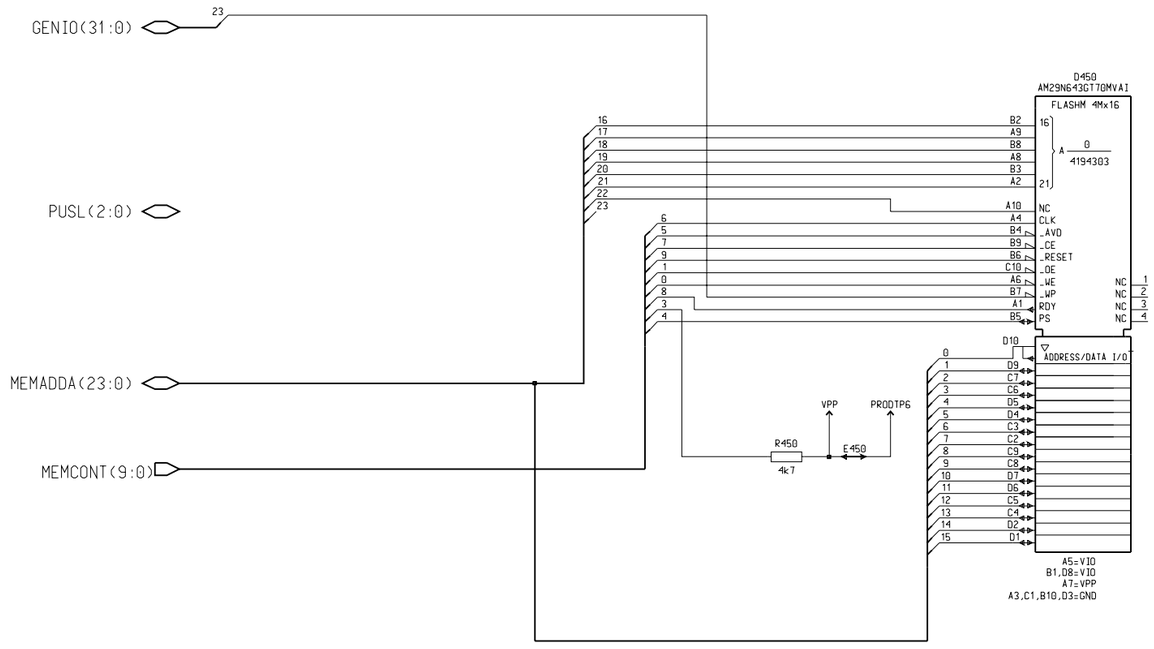


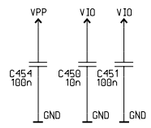
JTAG Emulator Connector and Buffers

MultiGND Connecting Audio GNDs to Global GNDs

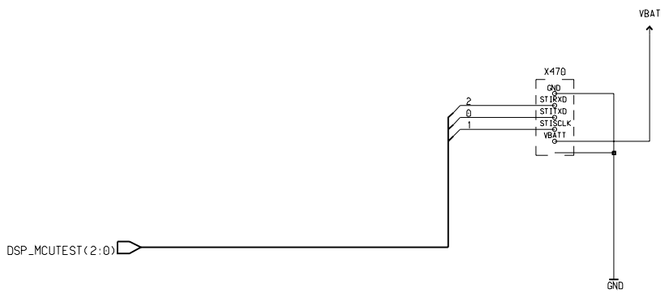


Circuit Diagram of Memory Configuration

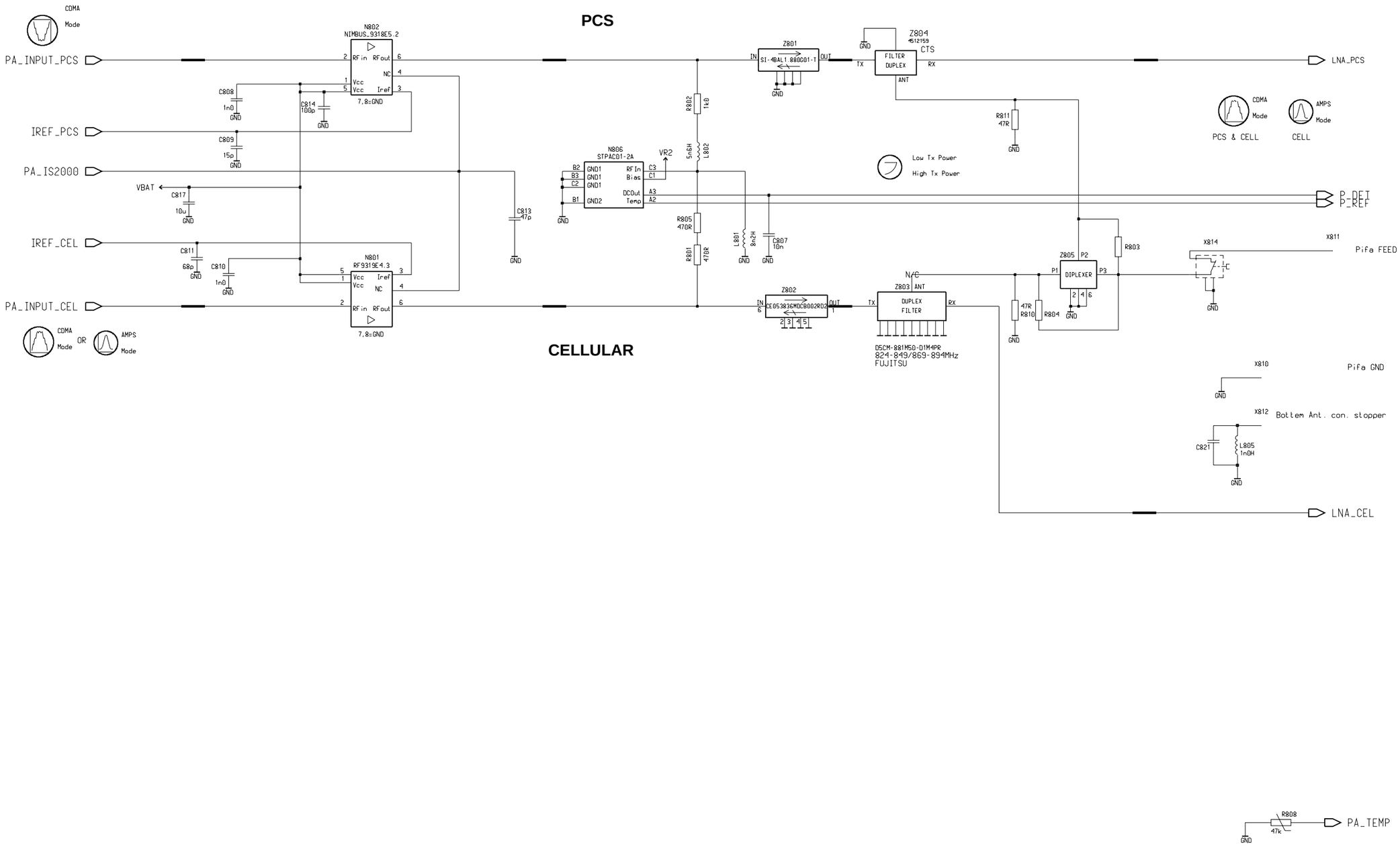




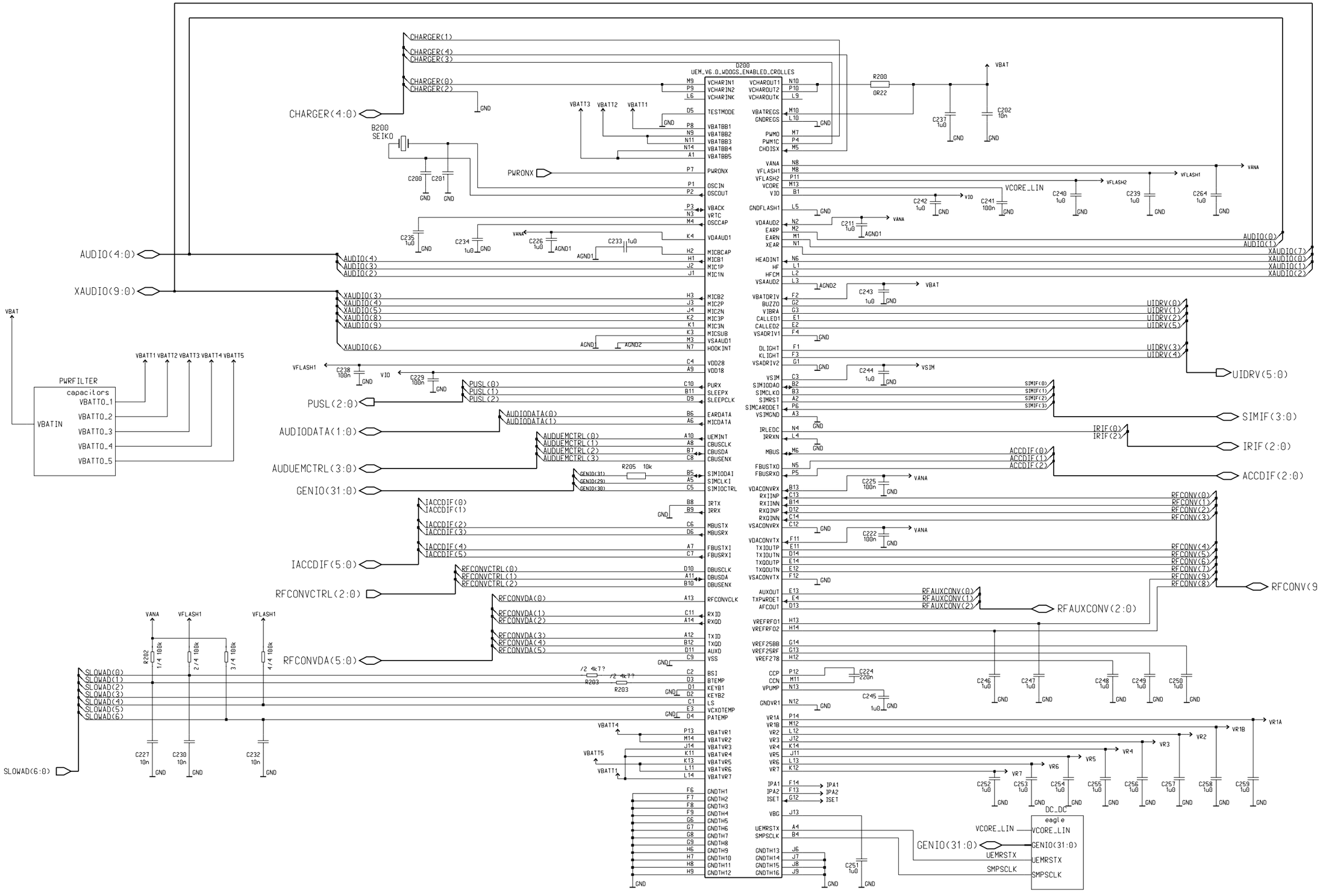
Circuit Diagram of Ostrich Test Interface



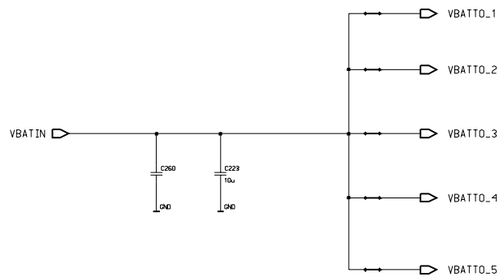
Circuit Diagram of PA



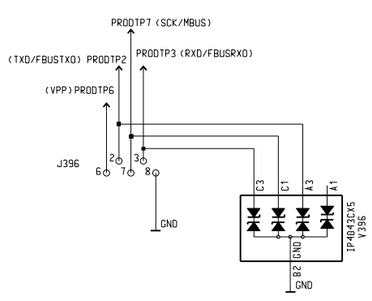
Circuit Diagram of Common Baseband



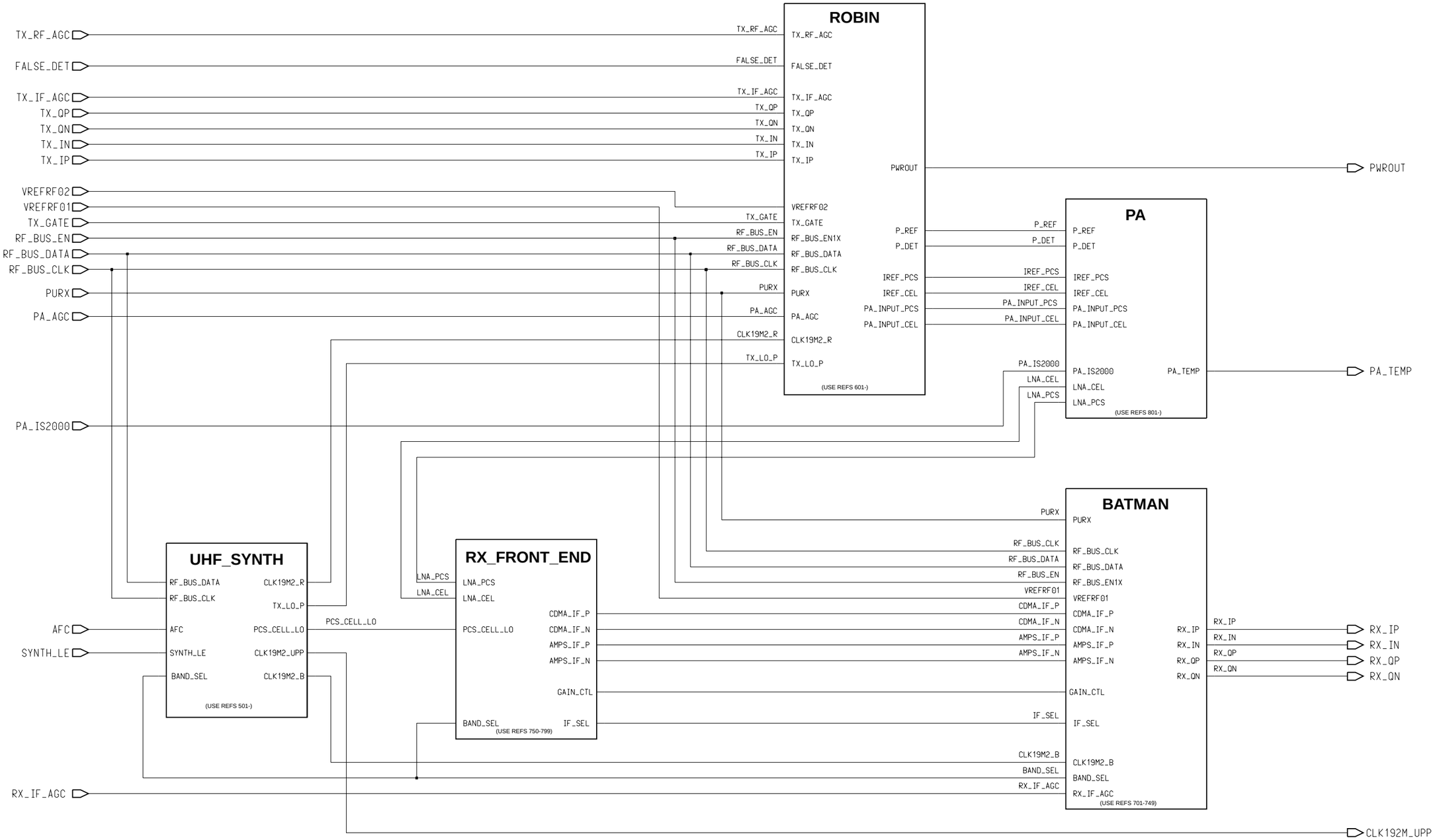
Circuit Diagram of DCT4 Power Supply



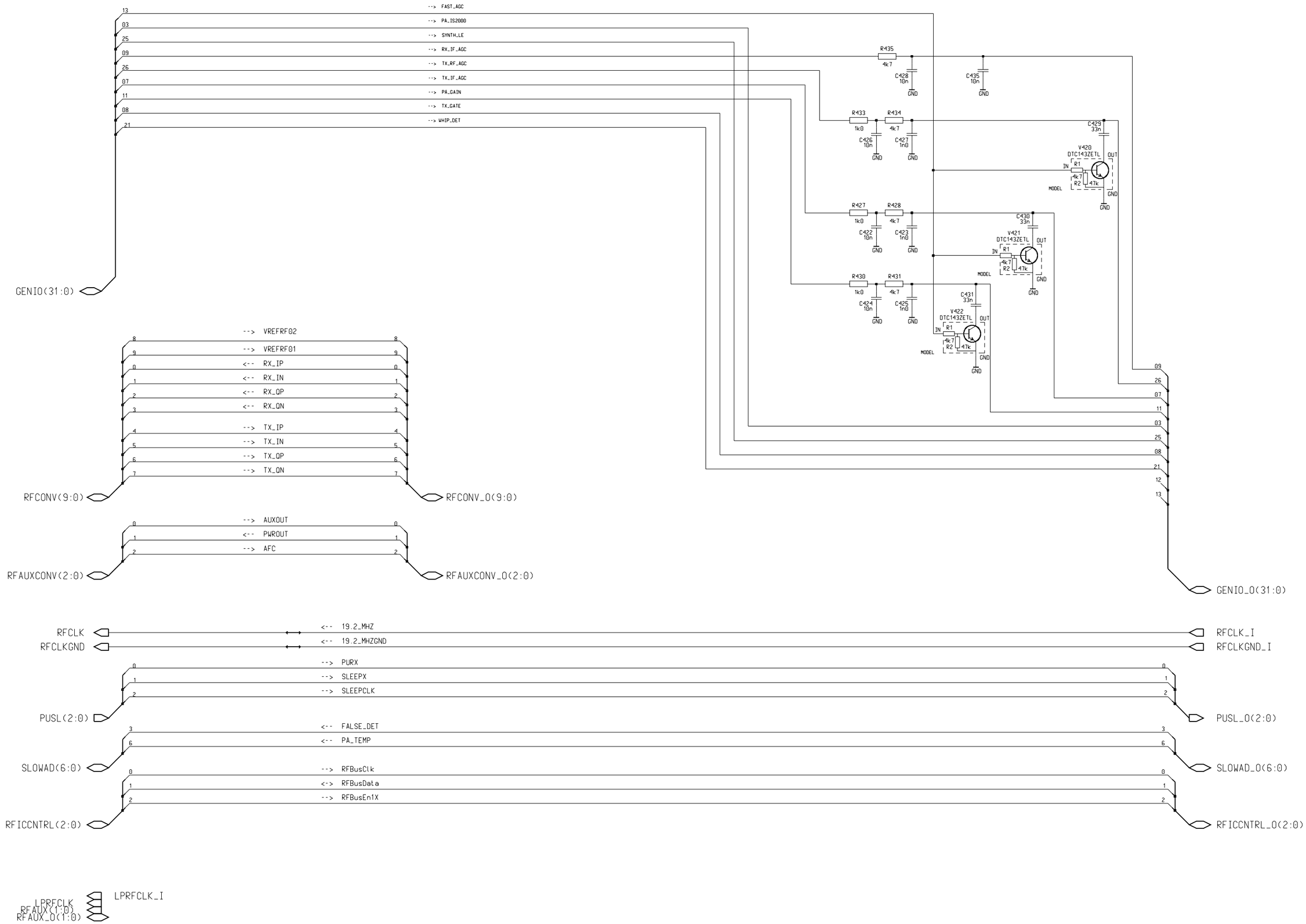
5-pin Production Test Pattern



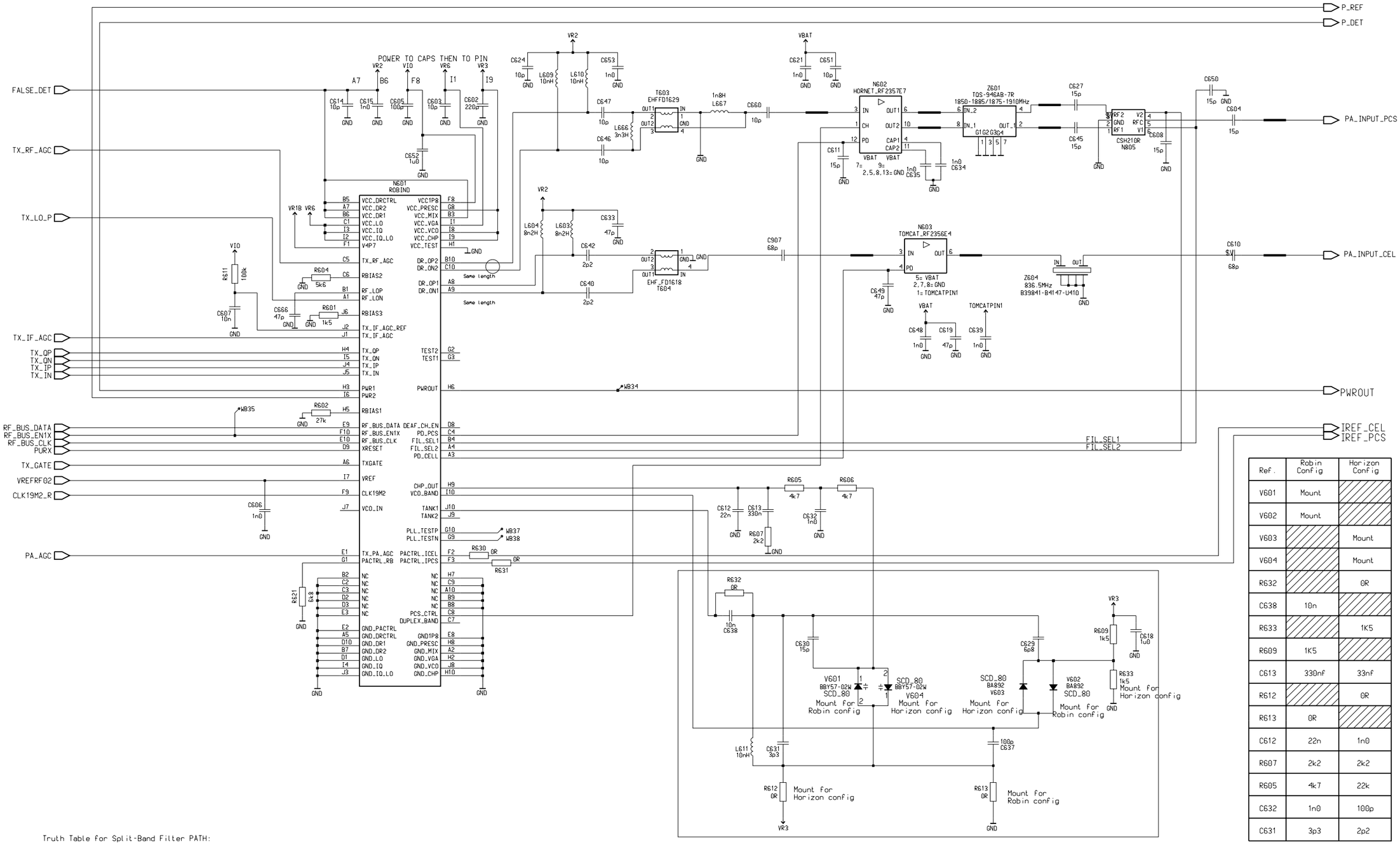
Circuit Diagram of RF



Circuit Diagram of RF-BB Interface



Circuit Diagram of Robin



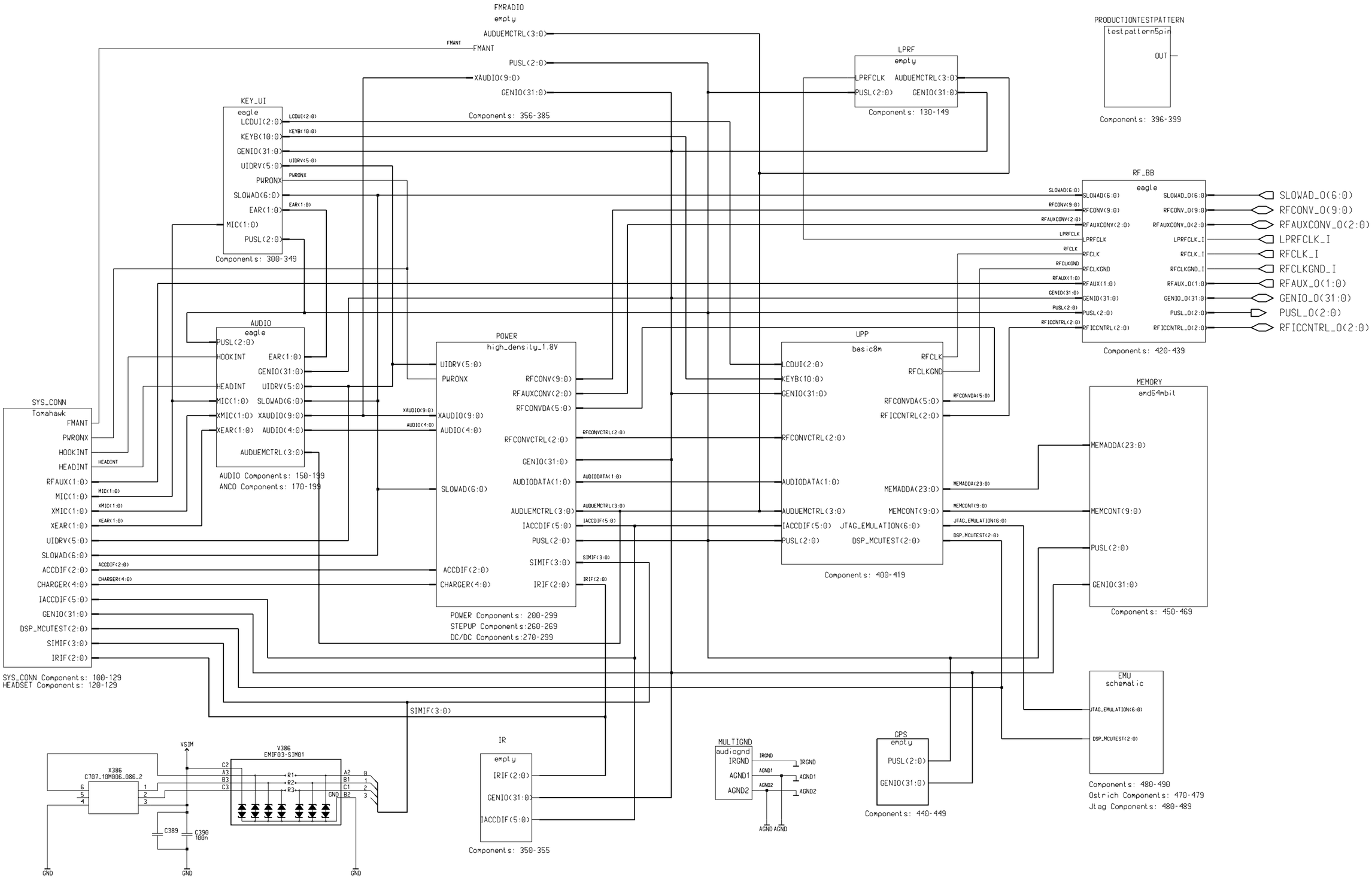
Ref.	Robin Config	Horizon Config
V601	Mount	
V602	Mount	
V603		Mount
V604		Mount
R632		0R
C638	10n	
R633		1K5
R609	1K5	
C613	330nf	33nf
R612		0R
R613	0R	
C612	22n	1n0
R607	2k2	2k2
R605	4k7	22k
C632	1n0	100p
C631	3p3	2p2

Truth Table for Split-Band Filter PATH:

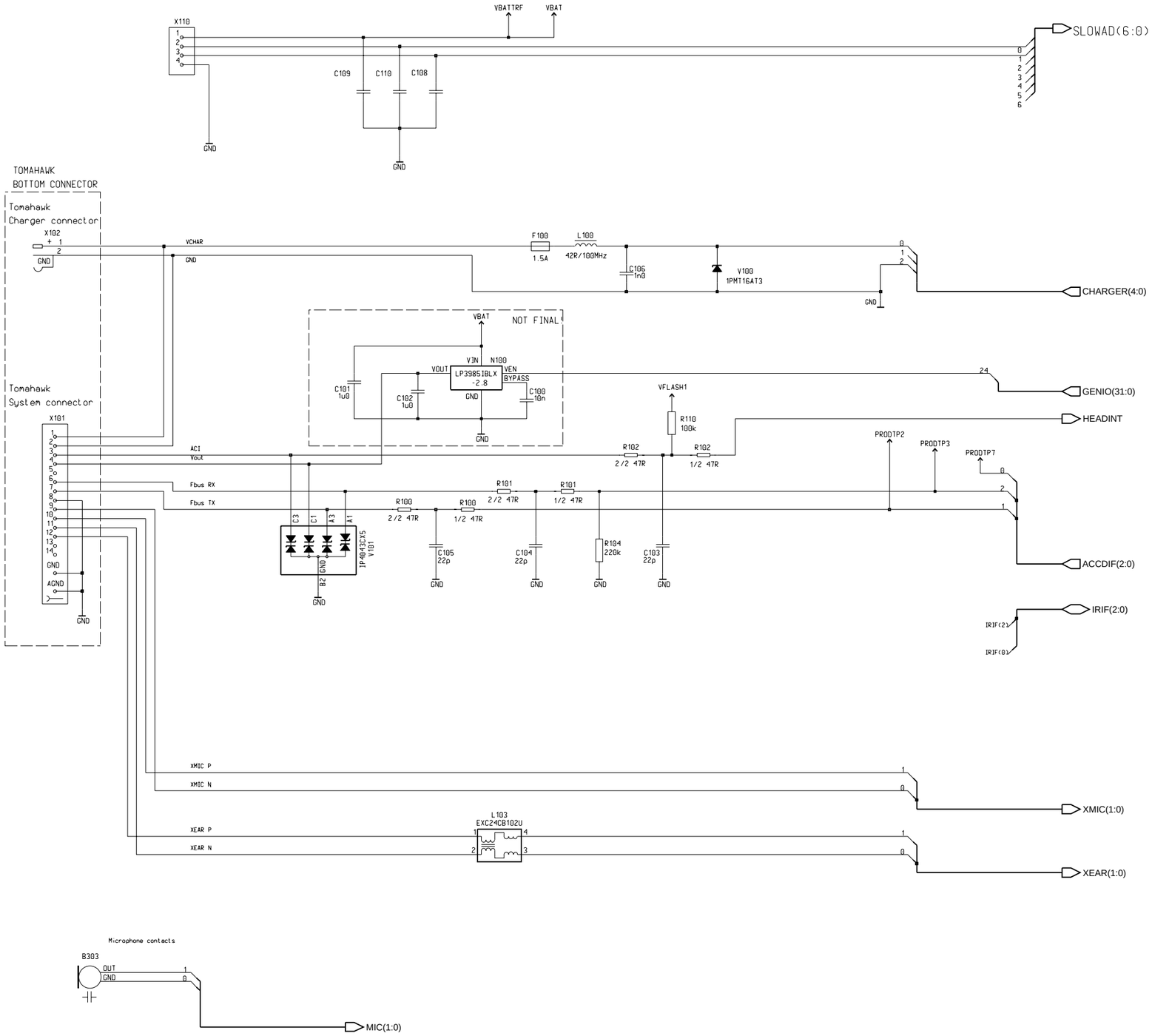
DRV CNTL	DRV OUT STATE	VCONT1	VCONT2	SWITCH IN STATE
0 volt	RFOUT1	0 volt	2.7 volt	RFI1
2.7 volt	RFOUT2	2.7 volt	0 volt	RFI2

	VCO_BAND
Cell band	low (shorted to ground)
PCS band	tri-stated (open circuit)

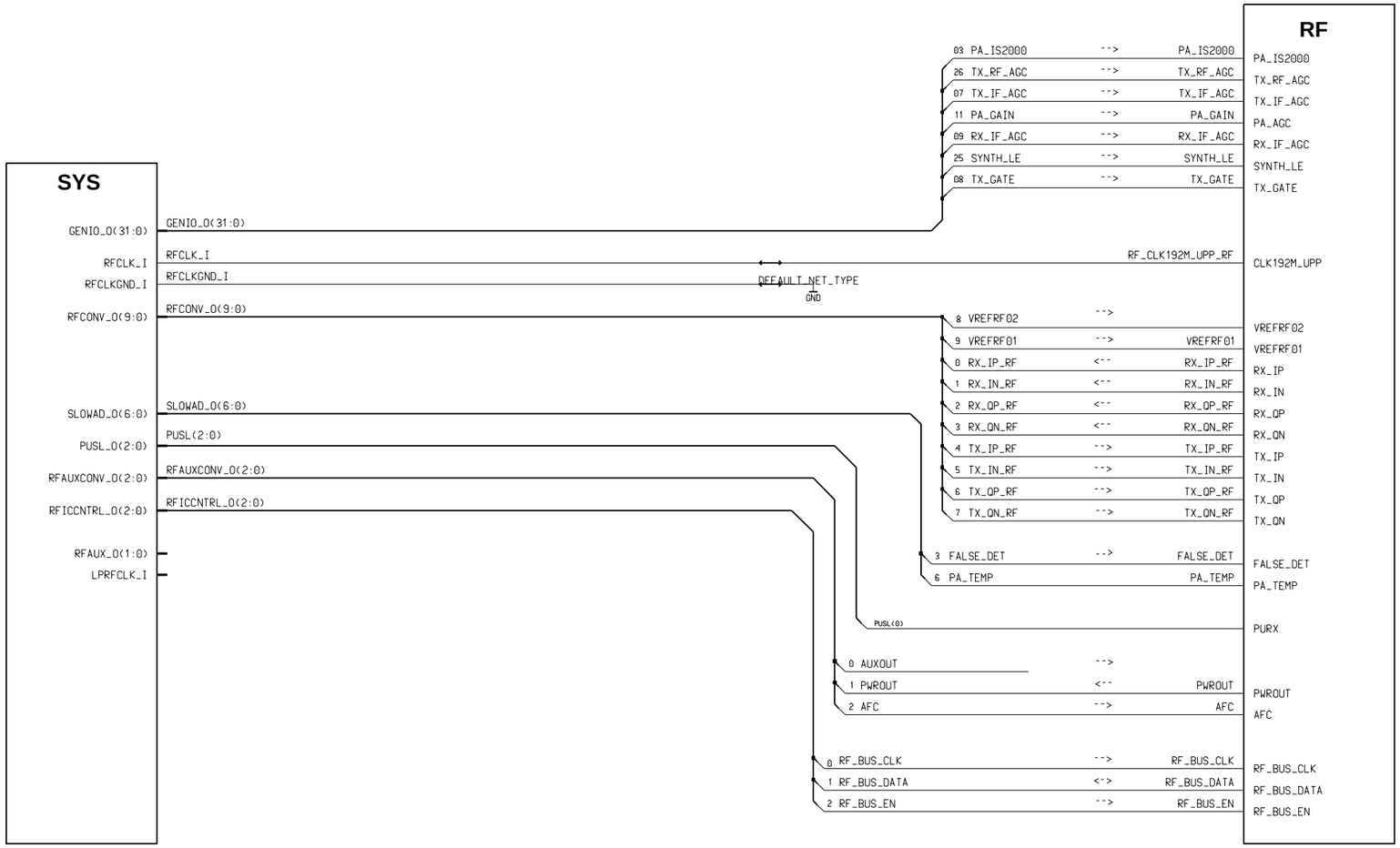
DCT4 Common Baseband Schematic (top level)



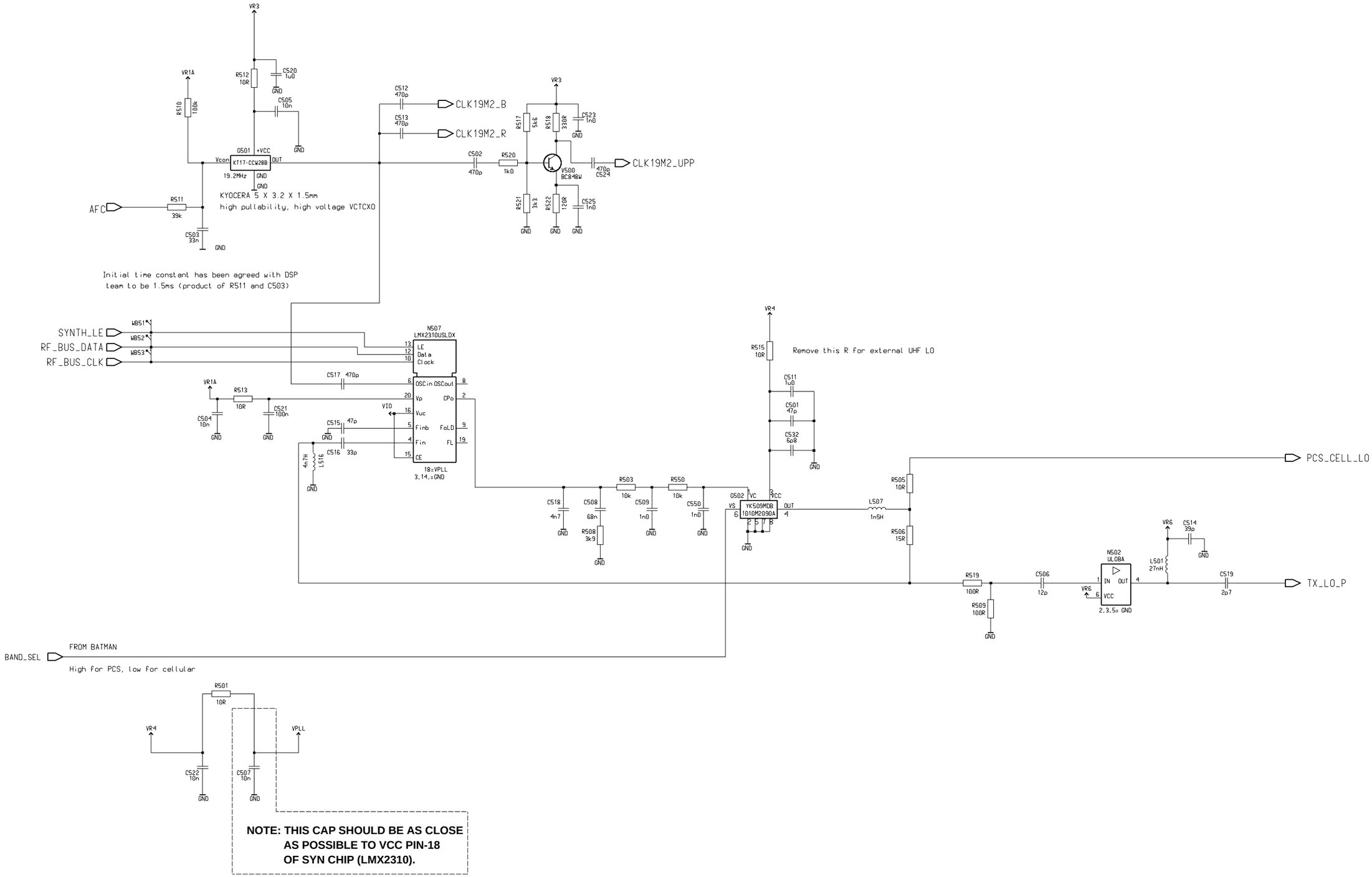
Circuit Diagram of System Connector



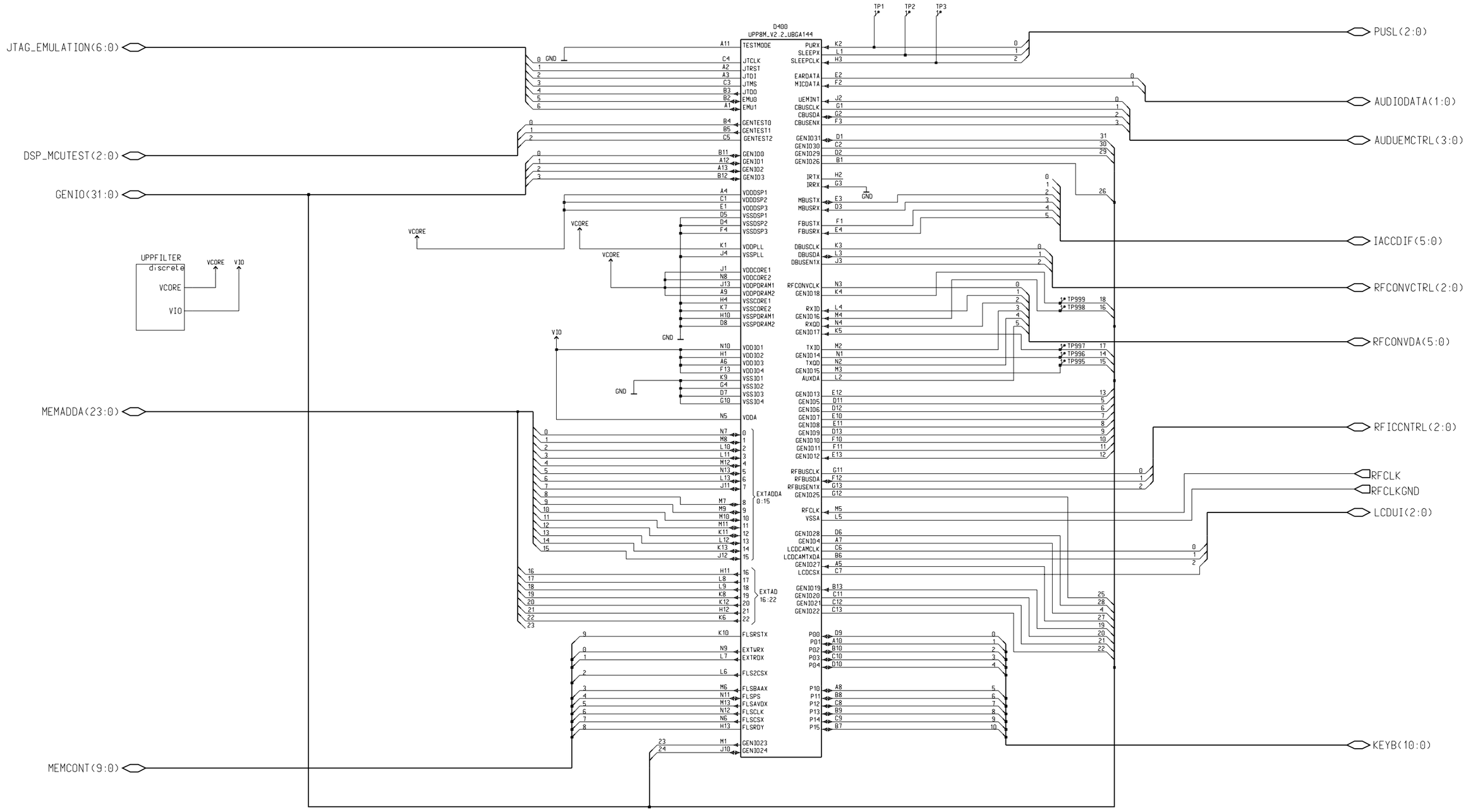
Circuit Diagram of Top Level



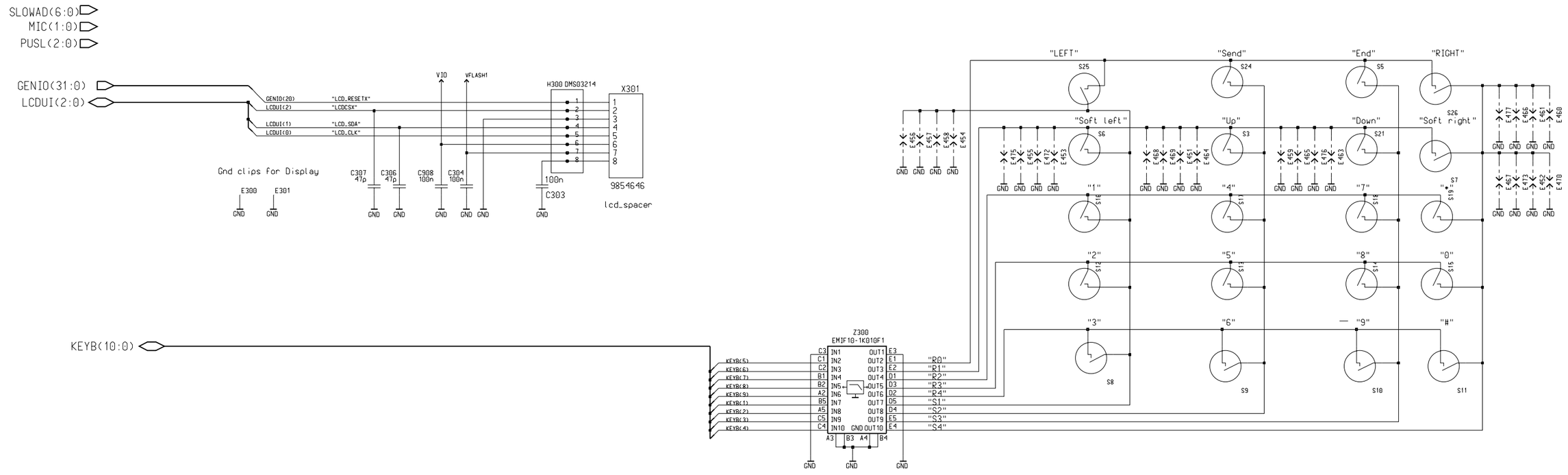
Circuit Diagram of UHF Synthesizer



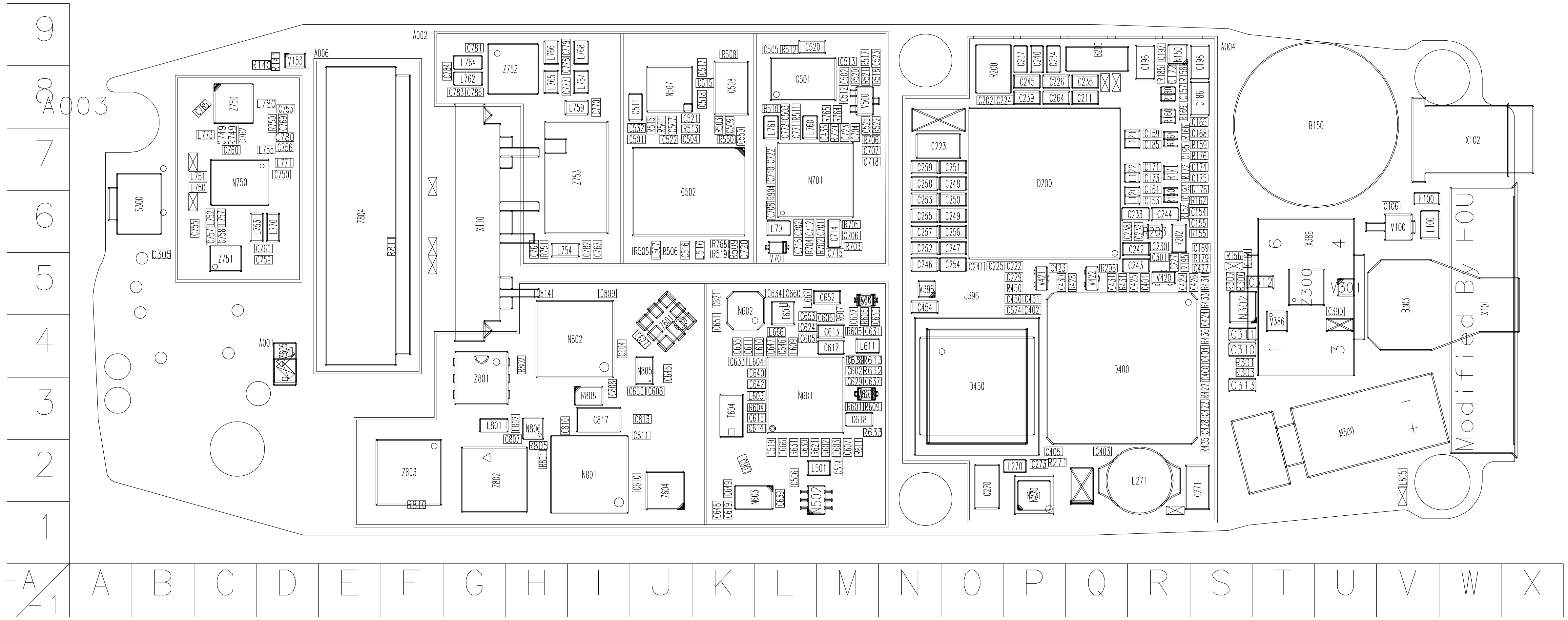
Circuit Diagram of DCT4 UPP



User Interface



Component Layout - Top



Component Layout - Bottom