

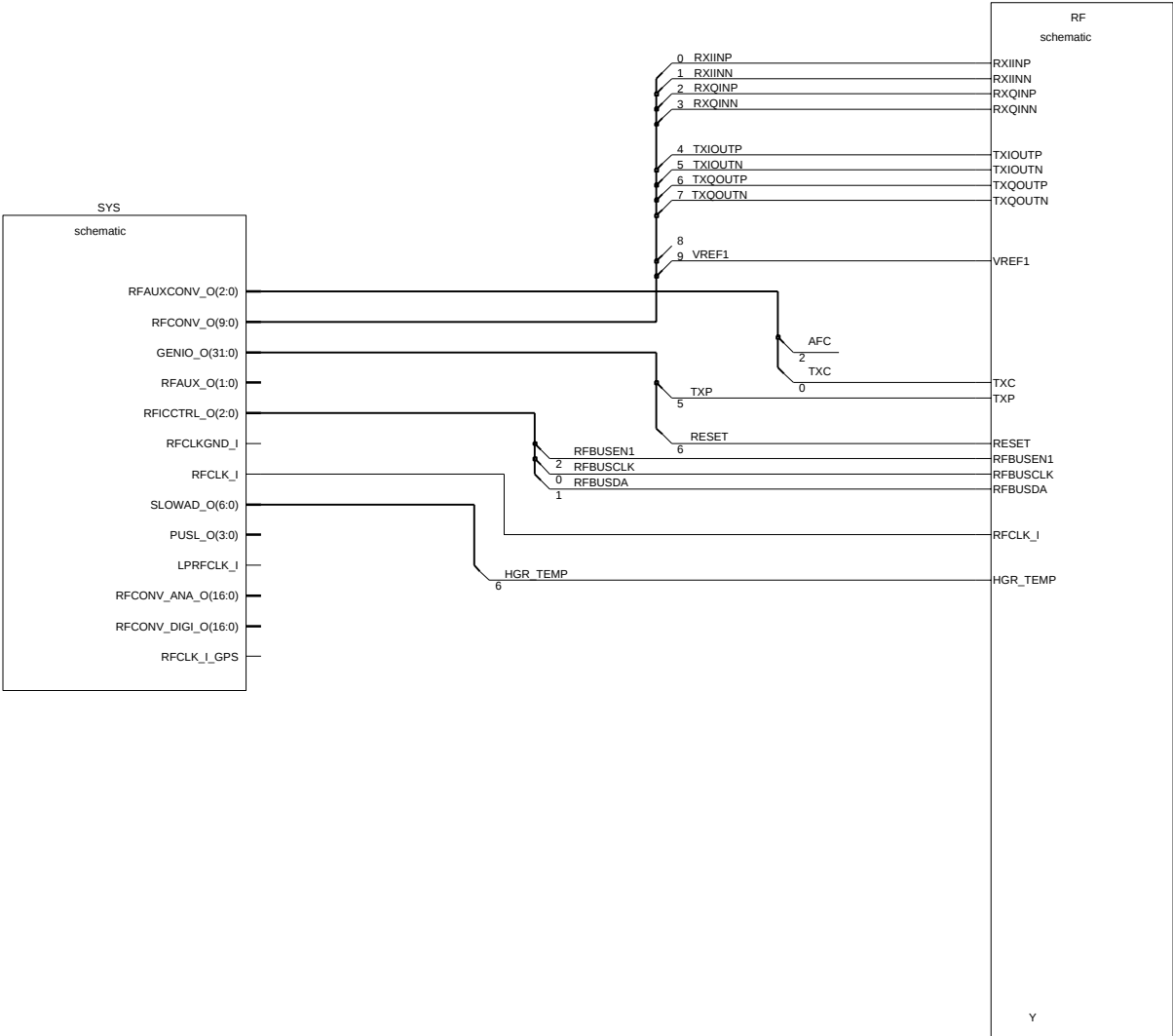
8 – SCHEMATICS

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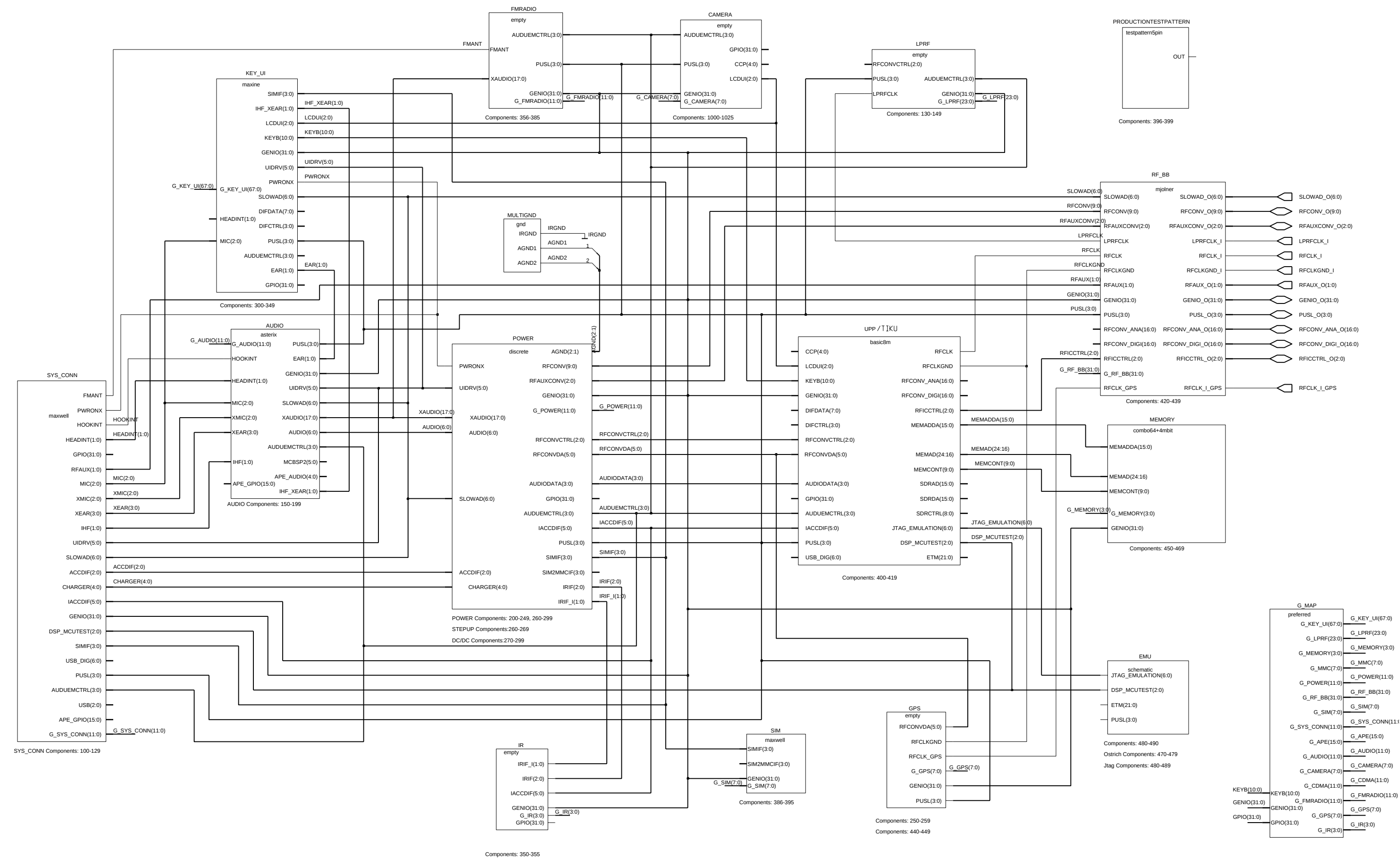
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Title: Top Sheet

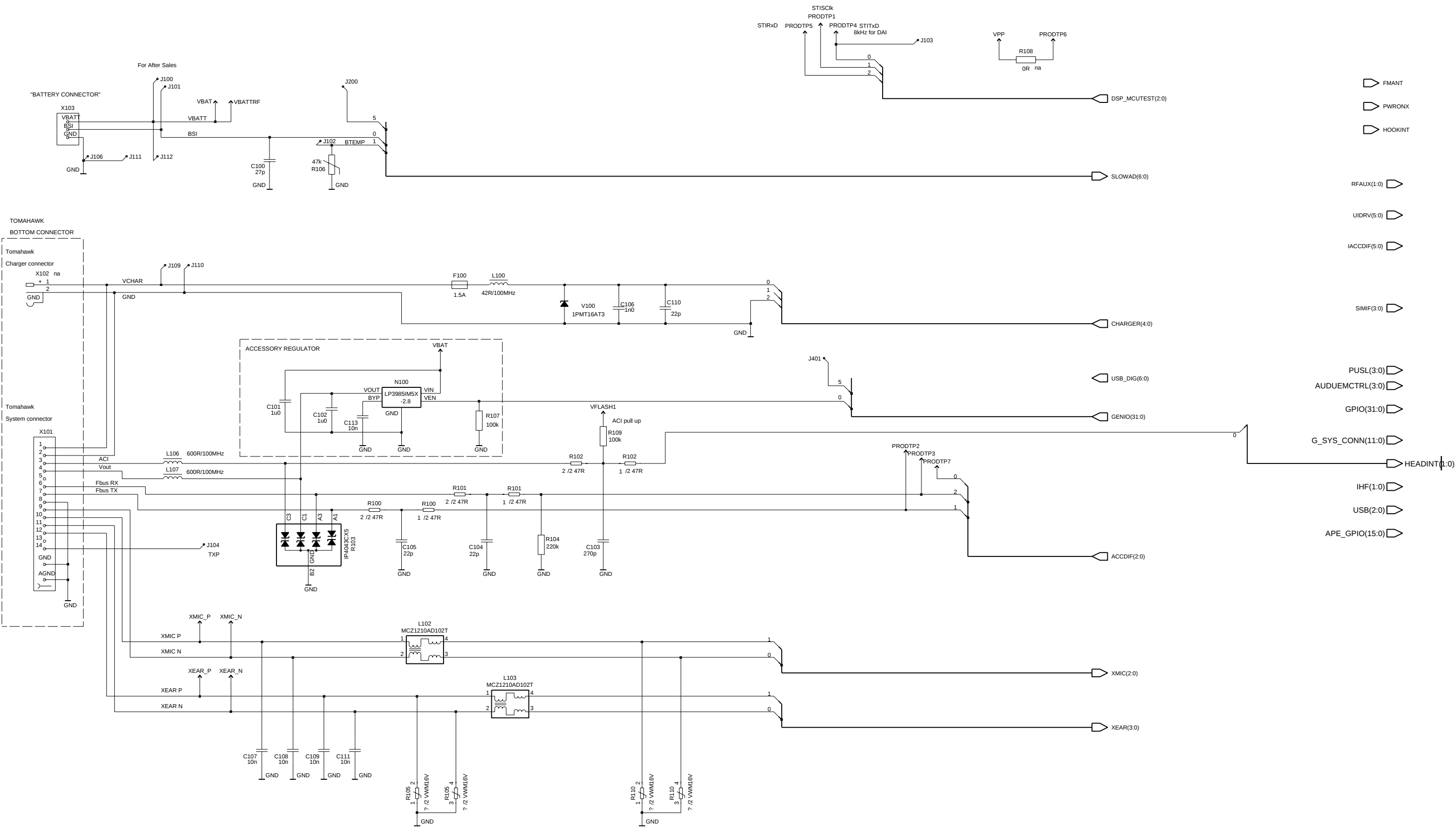
CBB_OVERVIEW		MODEL	CBB_VERSION
SYS_CONN		MAXWELL	SYS_6.1
KEY_UI		MAXINE	SYS_6.1
AUDIO		MAXWELL	SYS_6.1
FMRADIO		EMPTY	SYS_6.1
MULTIGND		GND	SYS_6.1
POWER	PWRFILTER	DISCRETE	SYS_6.1
	DC_DC	LIGHT	SYS_6.1
	REG_CAP	EMPTY	SYS_6.1
	PWR_RES	MAXWELL	SYS_6.1
		THERM1	SYS_6.1
IR		EMPTY	SYS_6.1
CAMERA		EMPTY	SYS_6.1
LPRF		EMPTY	SYS_6.1
UPP	UPPFILTER	BASIC8M	SYS_6.1
		DISCRETE	SYS_6.1
SIM		MAXWELL	SYS_6.1
GPS		EMPTY	SYS_6.1
PRODUCTIONS PATTERN	MODULE_ID	TESTPATTERN 5PIN	SYS_6.1
		MODULE_ID	SYS_6.1
RF_BB		MJOLNER	SYS_6.1
MEMORY	MEMFILTER	COMBO64*4MBIT	SYS_6.1
	MEMWING	NOVFLASH1CAP	SYS_6.1
	MEMEXTENSION	EMPTY	SYS_6.1
		EMPTY	SYS_6.1
EMU	JTAG	SCHEMATIC	SYS_6.1
	OSTRICH	TESTPOINT	SYS_6.1
	ETM	TESTPOINT	SYS_6.1



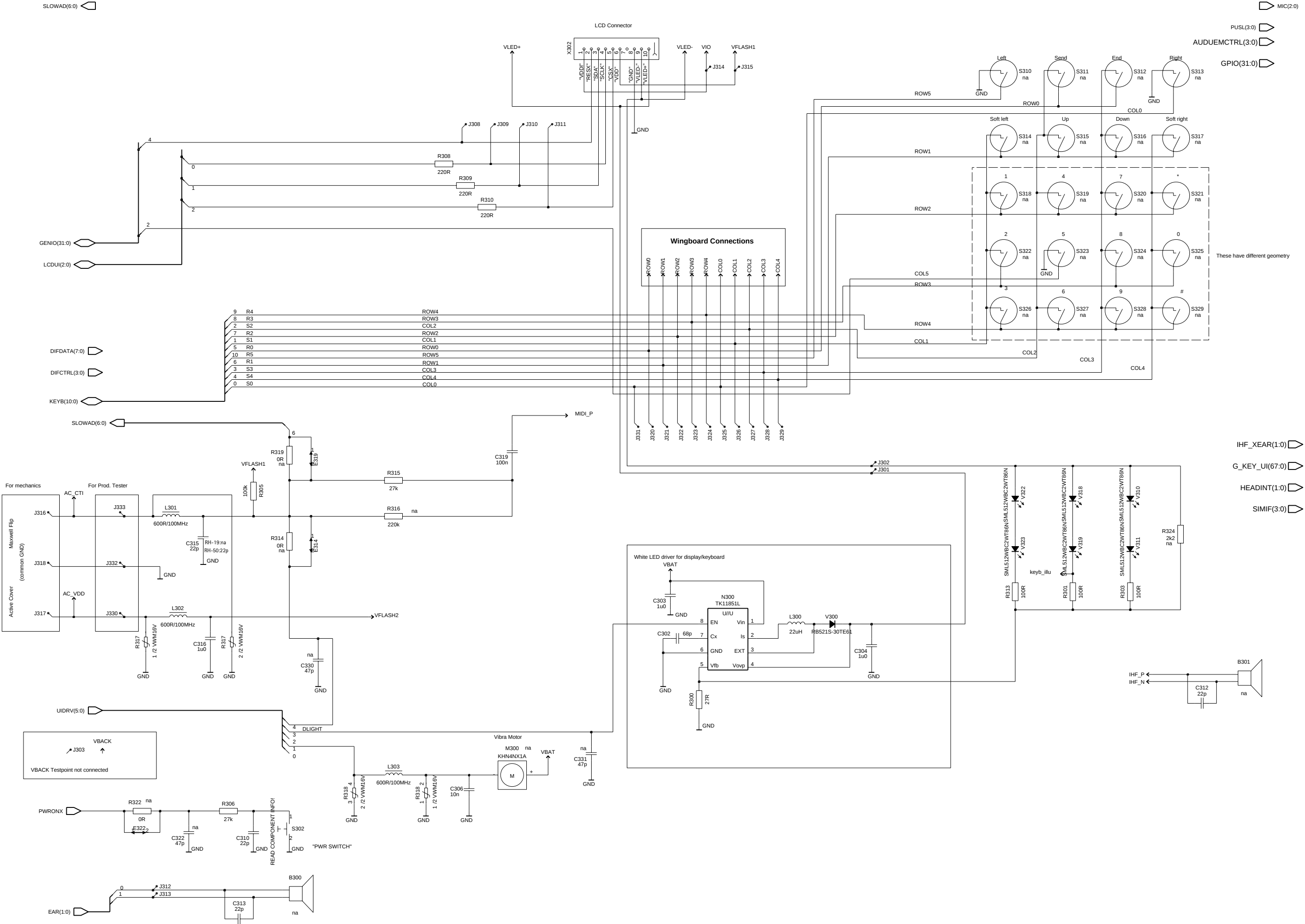
Title: DCT4 Common Baseband Schematic (Top Level)



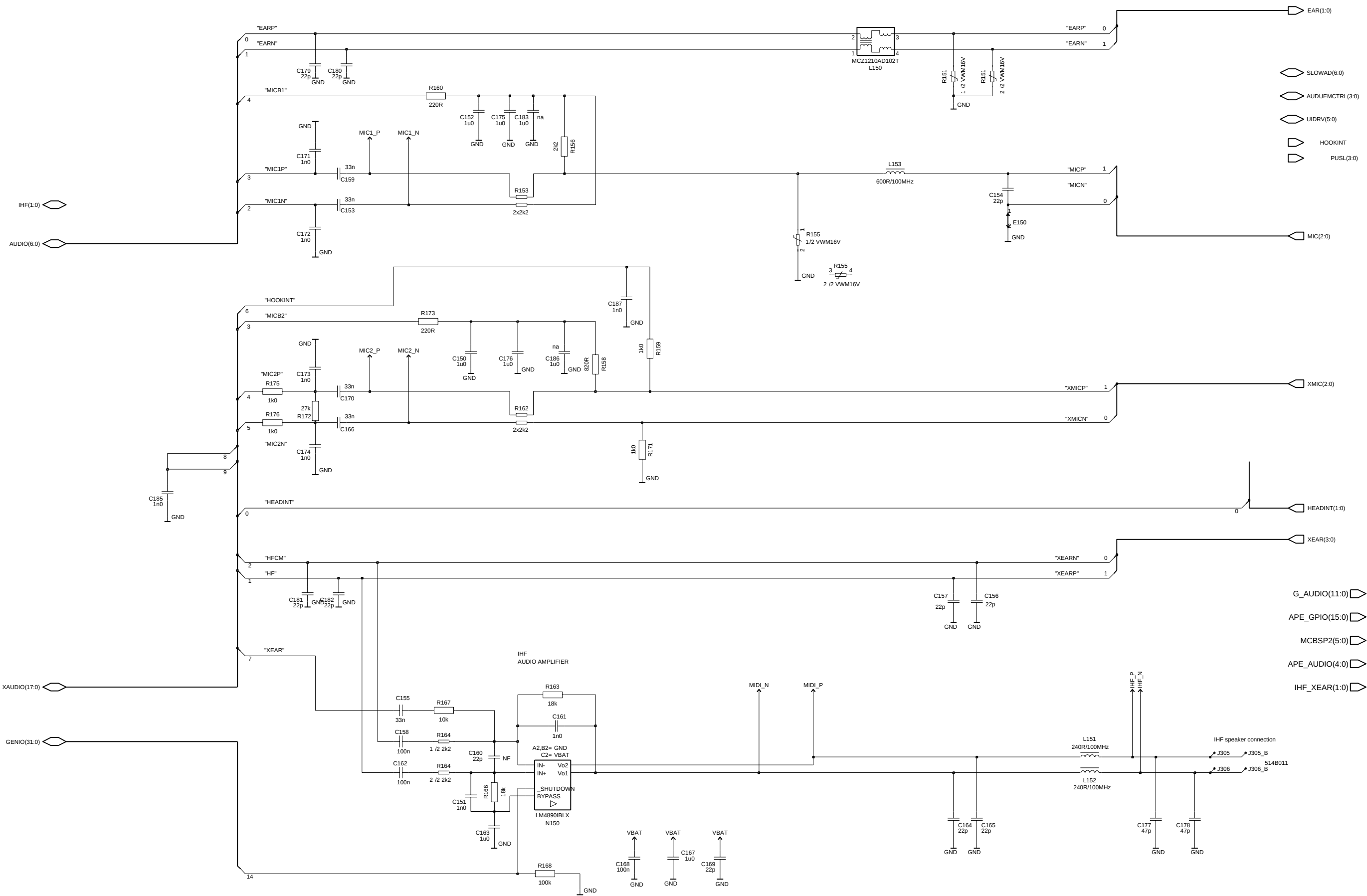
Title: RH-19/RH-50 System Connector



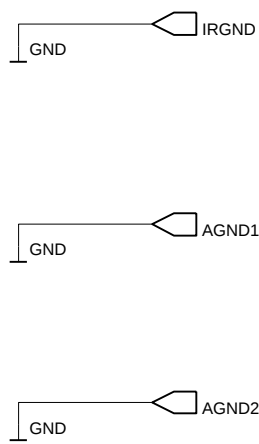
Title: RH-19/RH-50 User Interface



Title: RH-19/RH-50 Audio



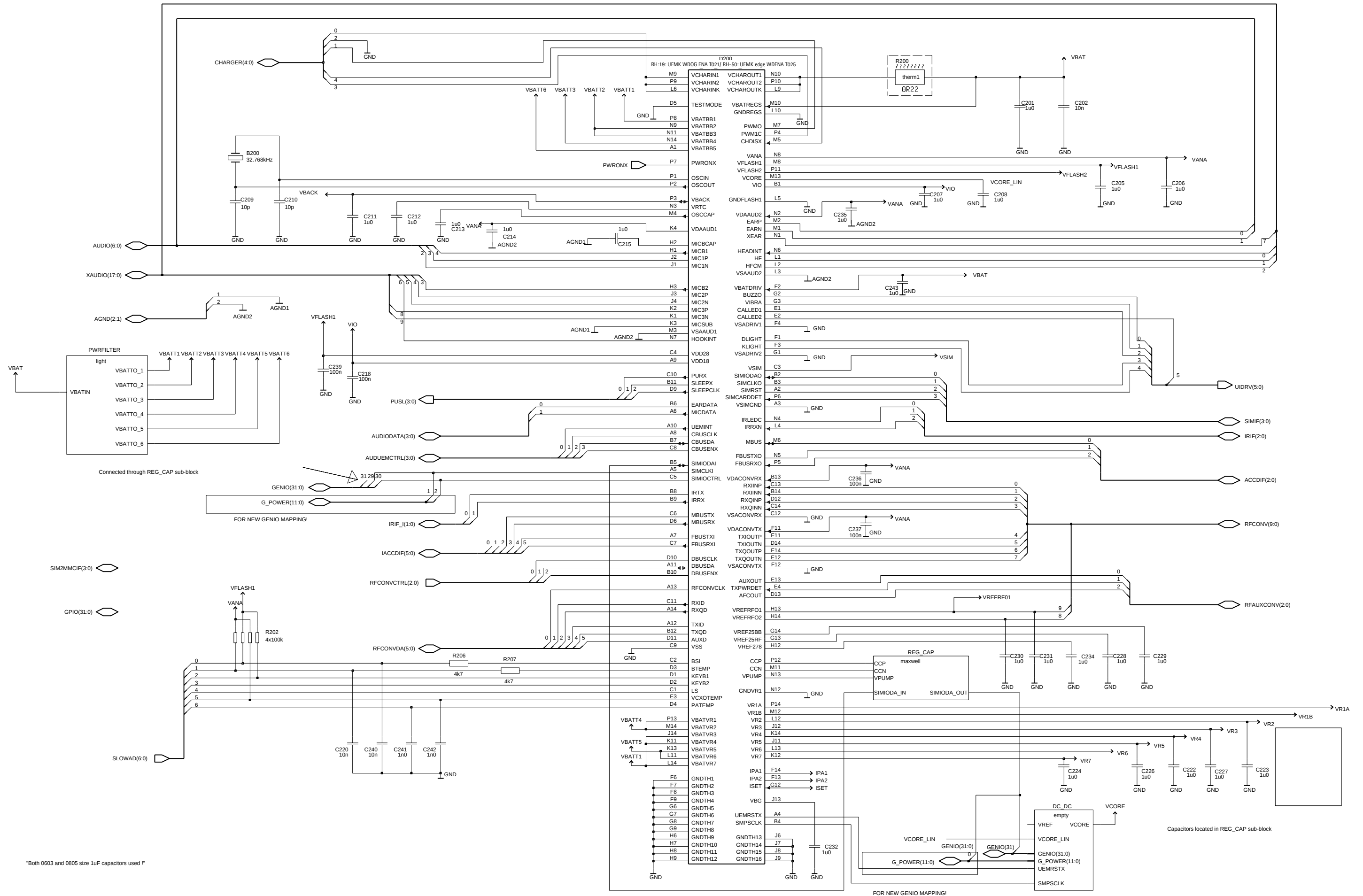
Title: MultiGND Symbol Bypass



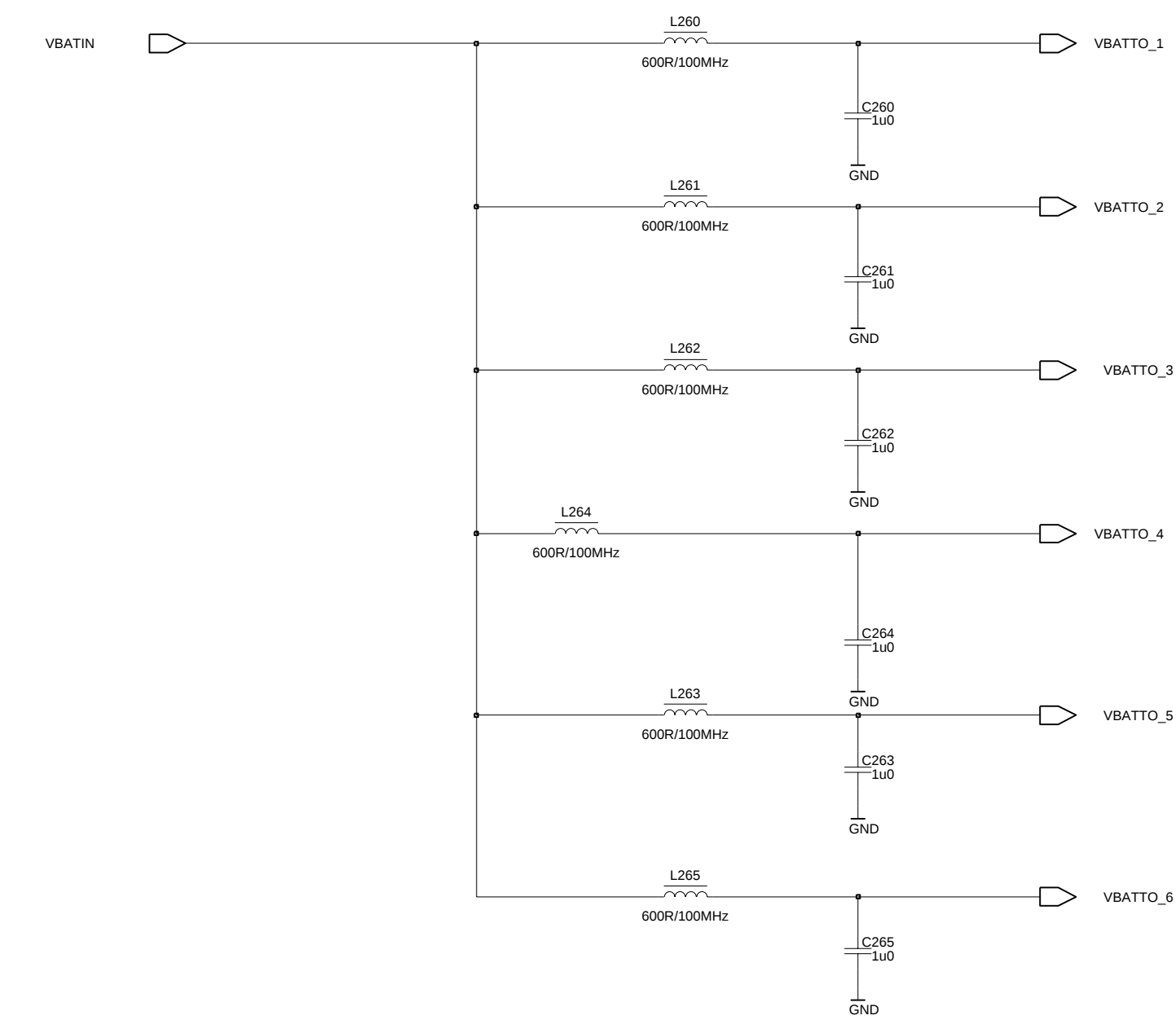
Title: 5 pin Production Test Pattern



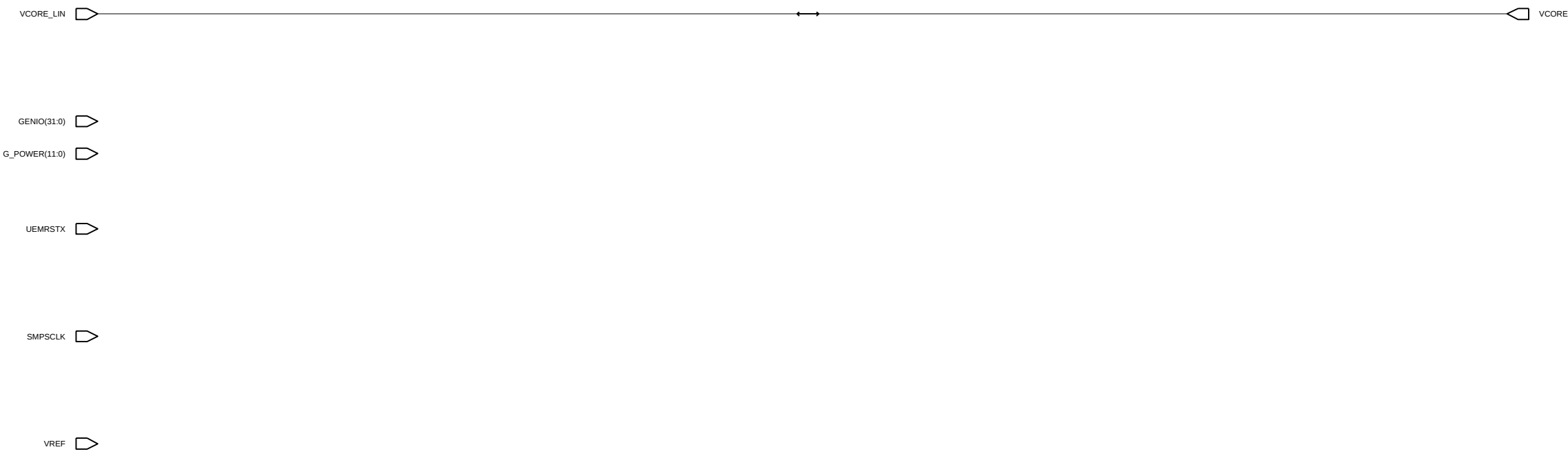
Title: Discrete Power Management



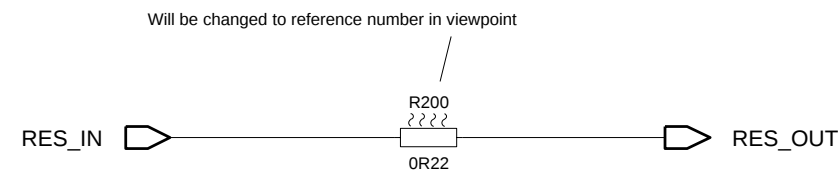
Title: Light Filtering



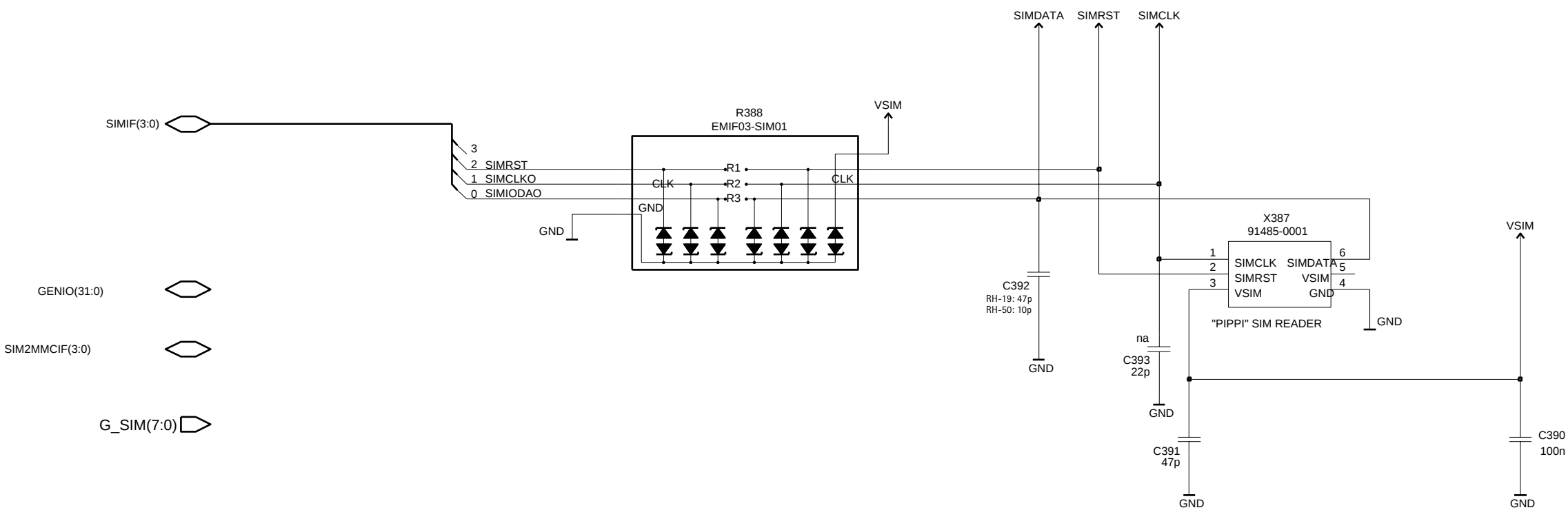
Title: DC/DC Convertor



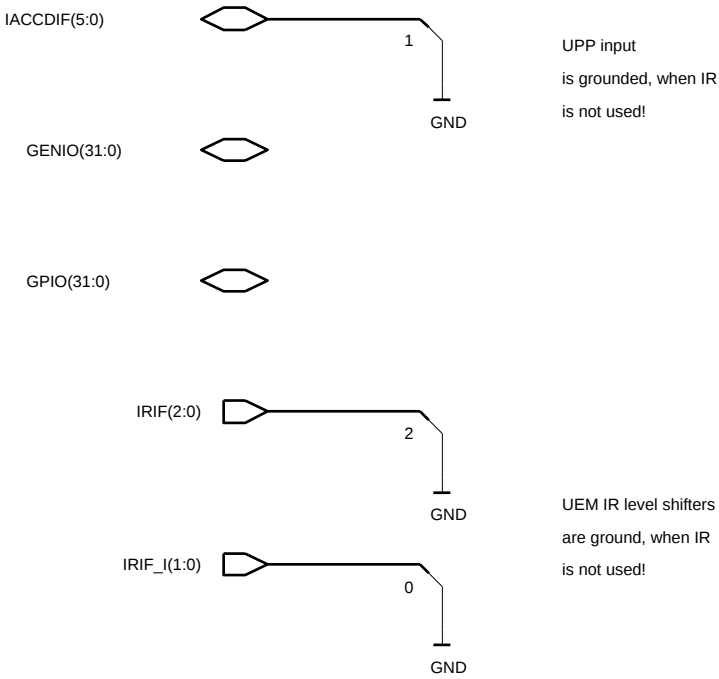
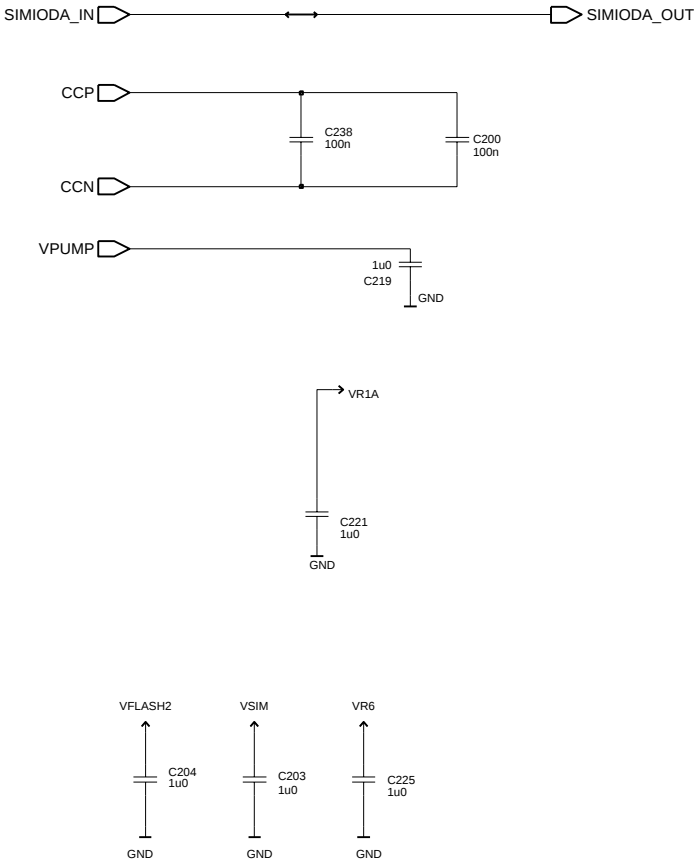
Title: PWR Resistor 0805 thermal1



Title: SIM Reader for RH-19/RH-50

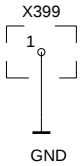


Title: RH-19/RH-50 Filters / No IR Interface present in this project

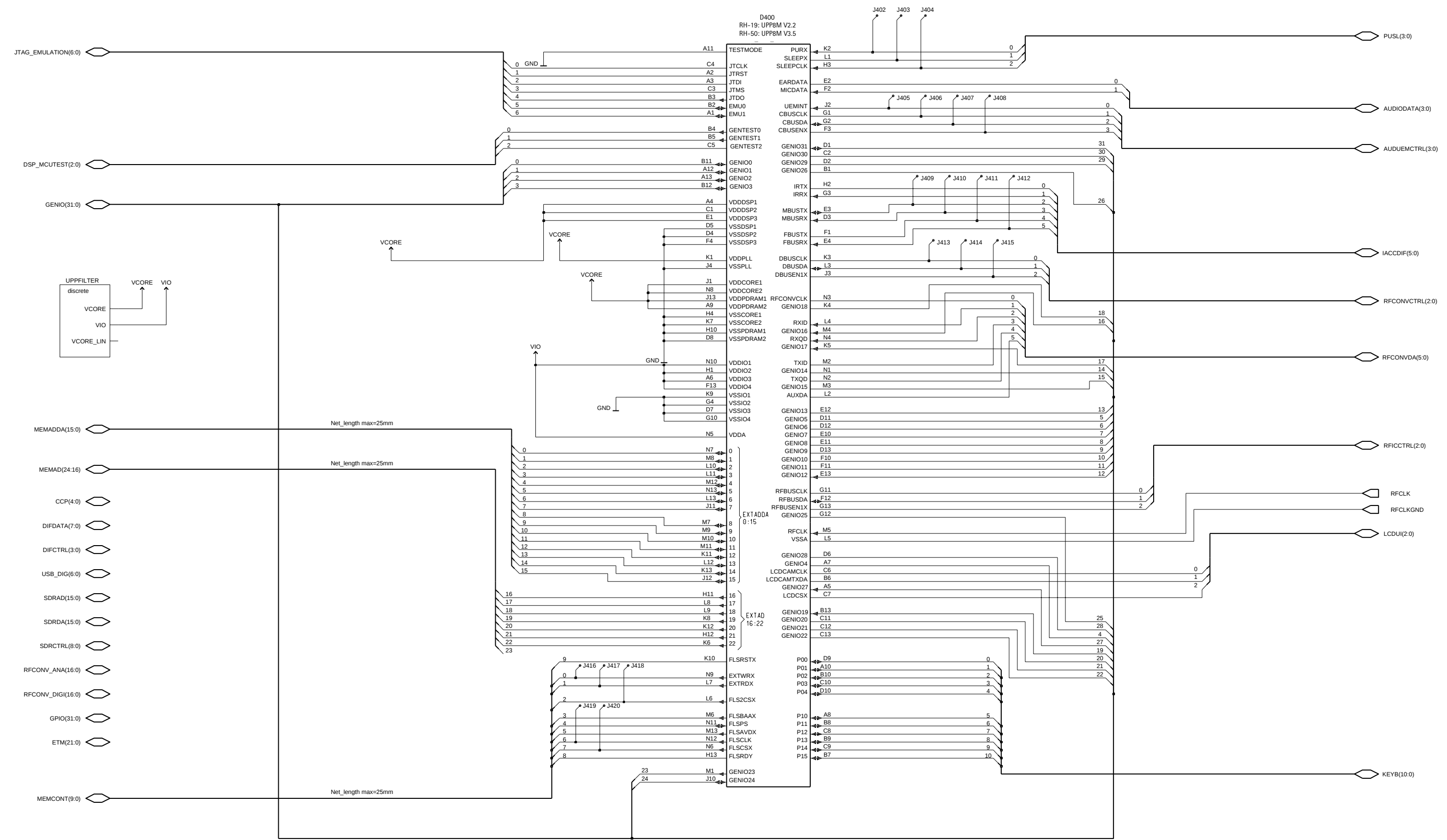


Title: Module ID

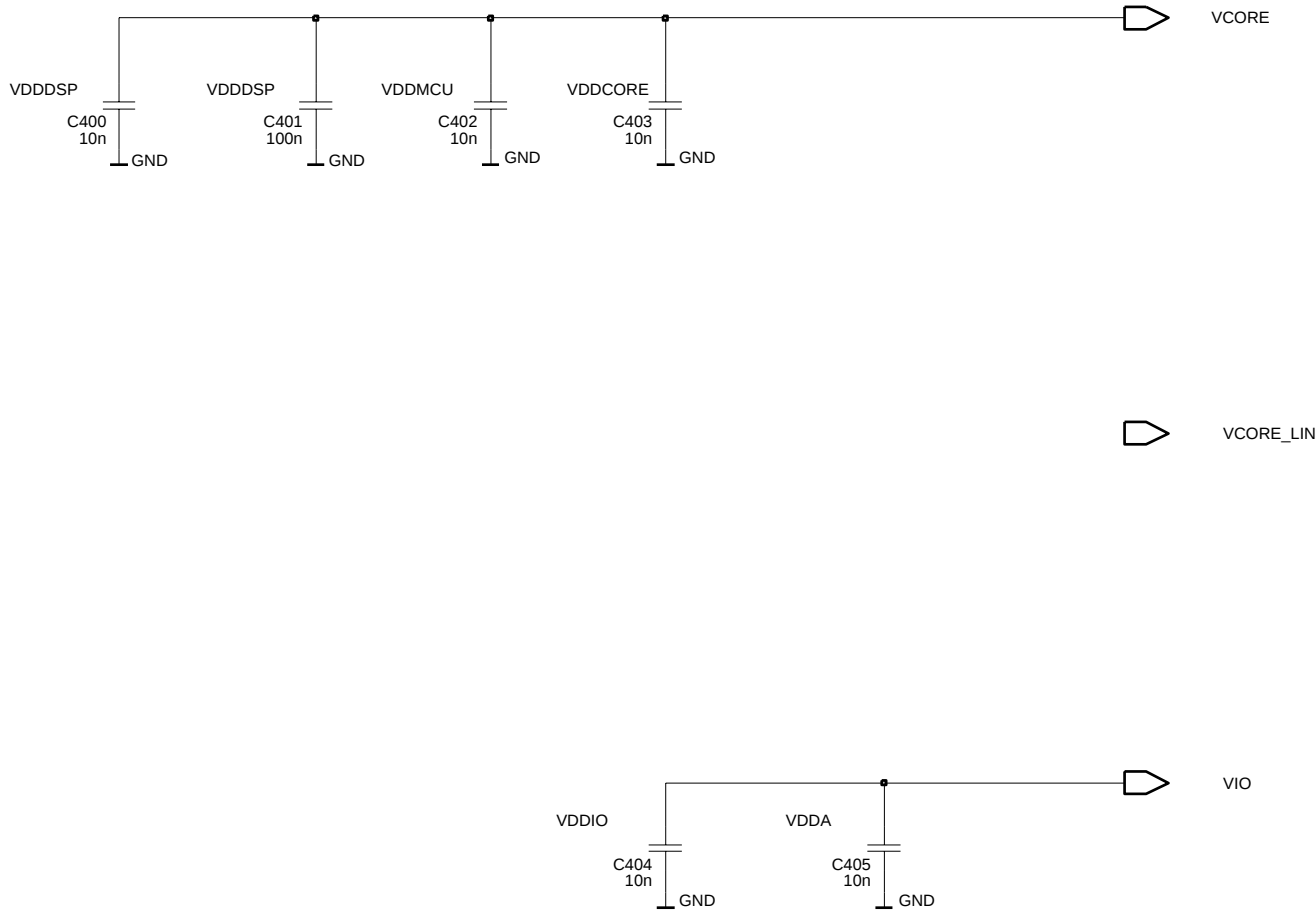
OUTPUT



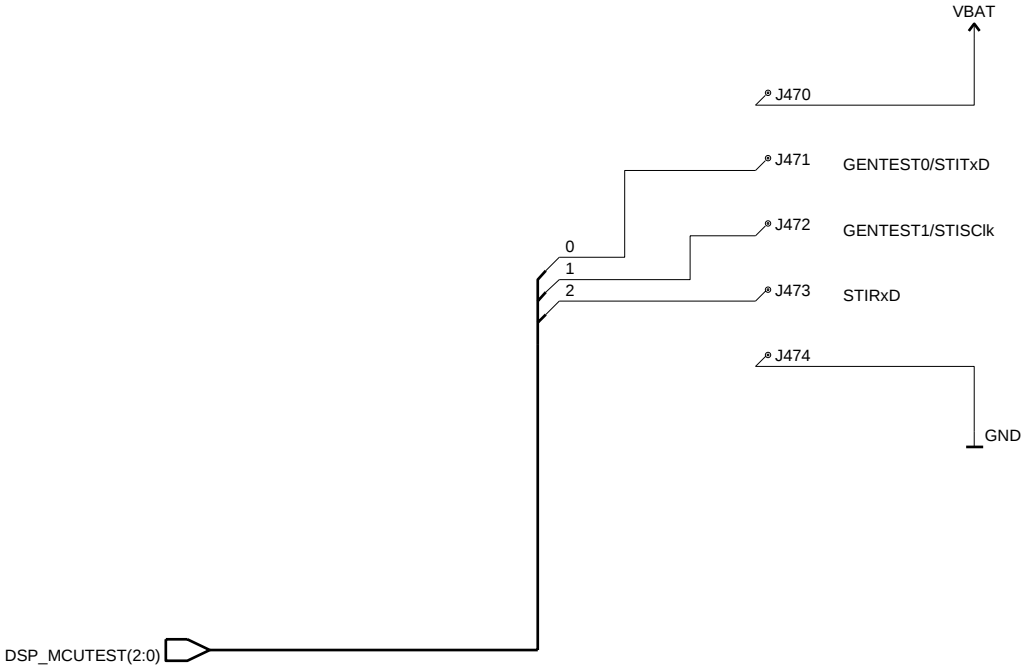
Title: UPP 8M Implementation



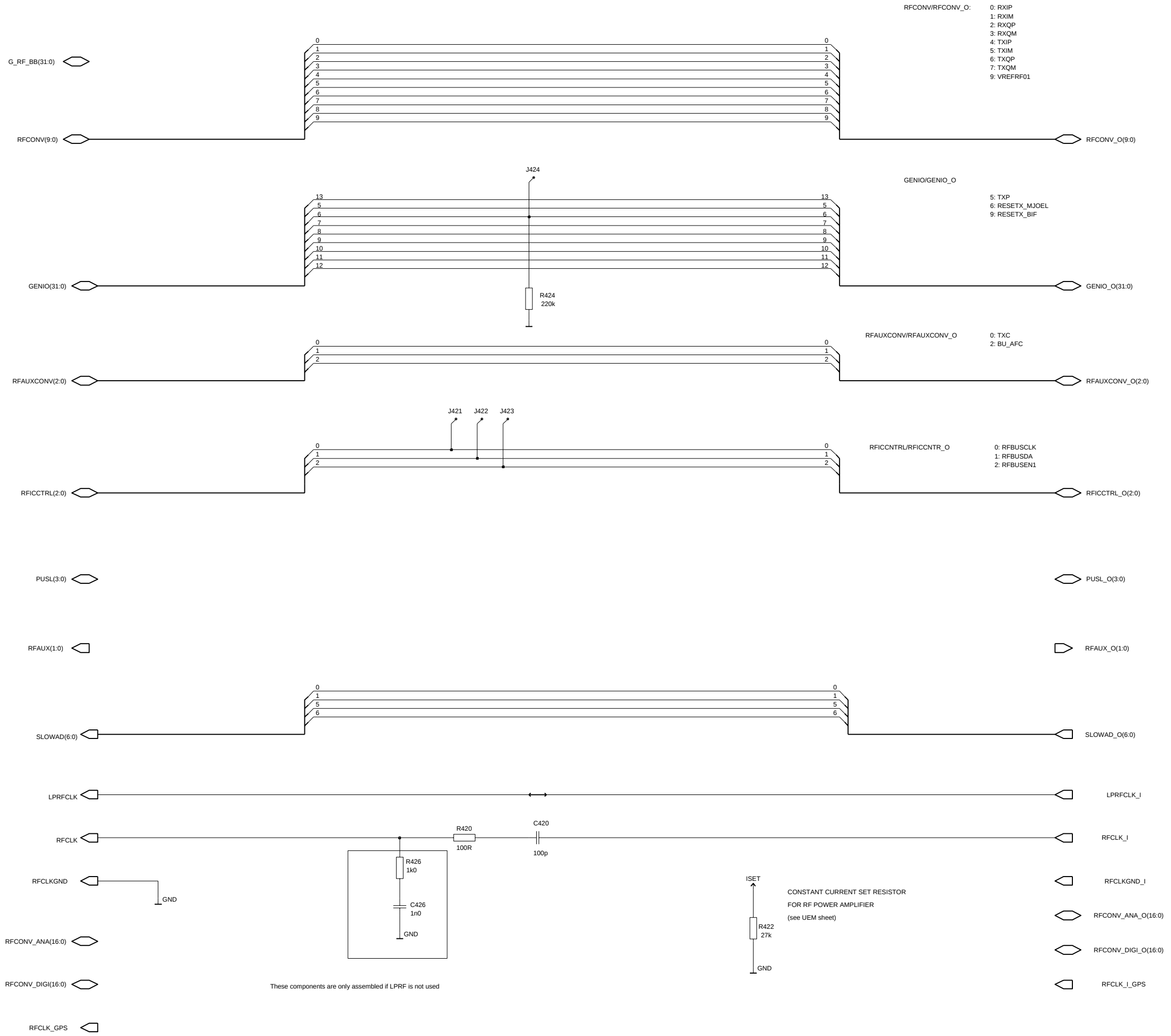
Title: Discrete Decoupling Capacitors for UPP



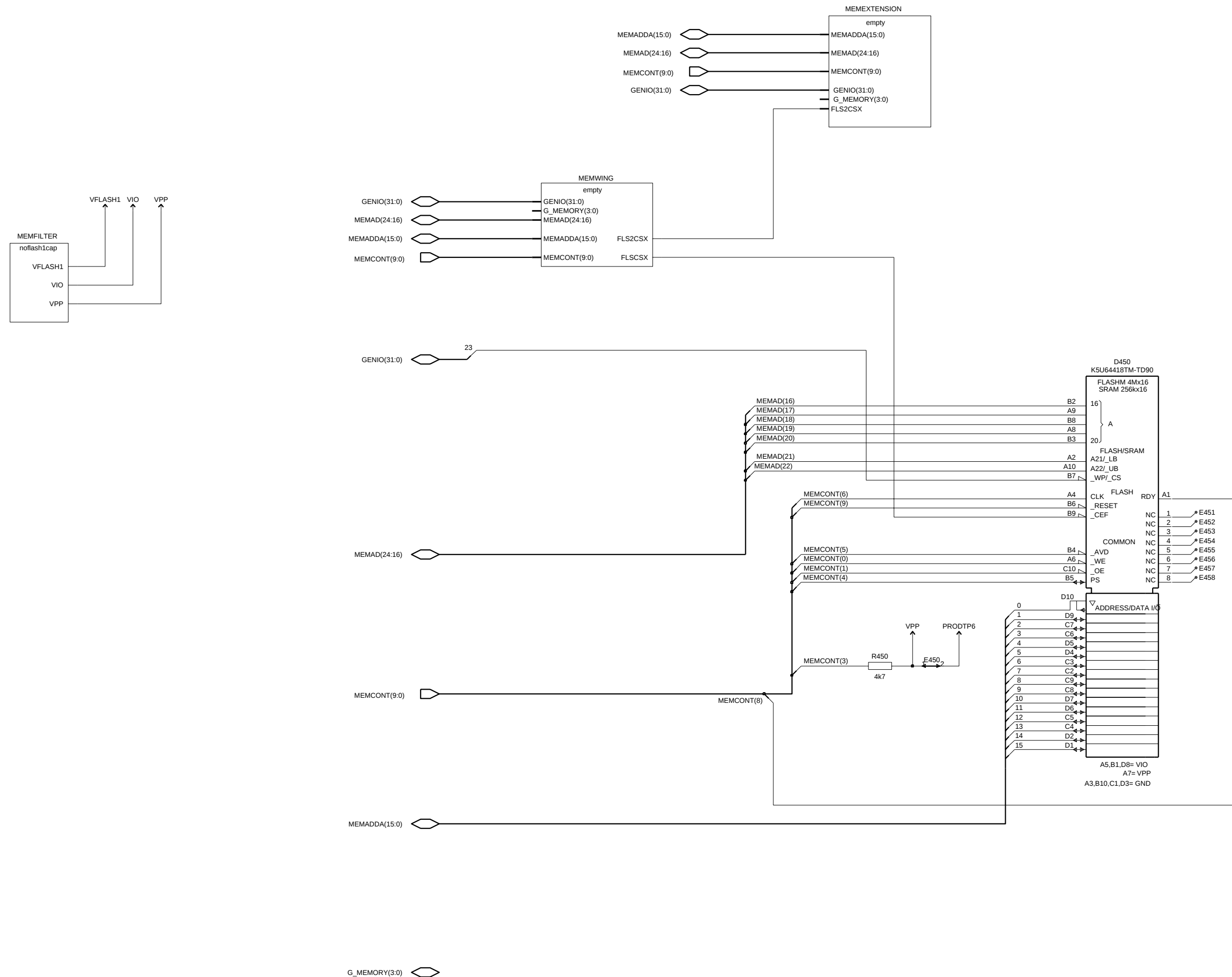
Title: Testpoints based Ostrich Inteface



Title: GSM RF - Baseband Interface



Title: Combo Memory 64 + 4 Mbit



Title: Discrete Capacitors for Memory without VFlash1



Title: Empty Wing Sheet

MEMADDA(15:0)

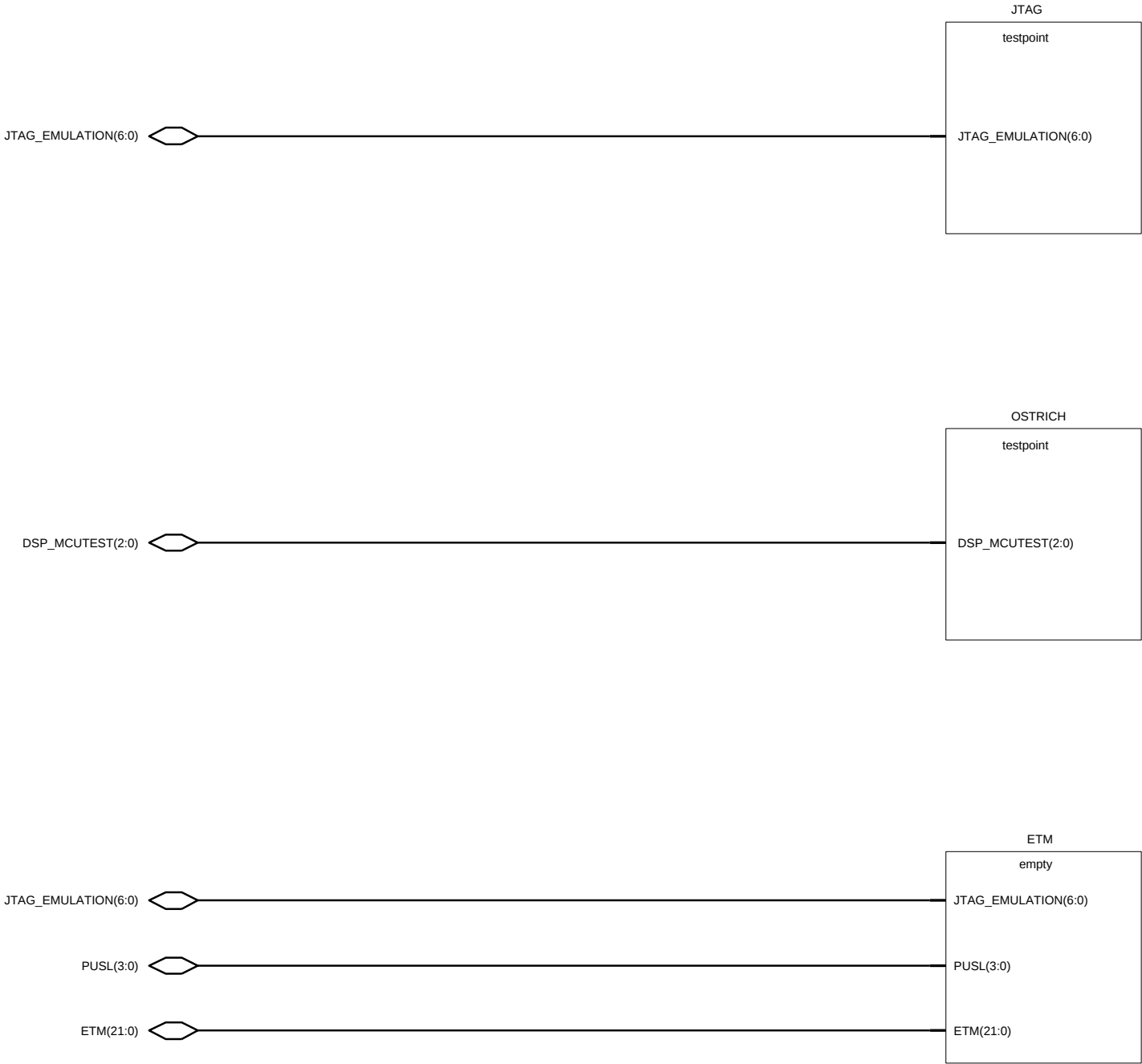
MEMAD(24:16)

GENIO(31:0)

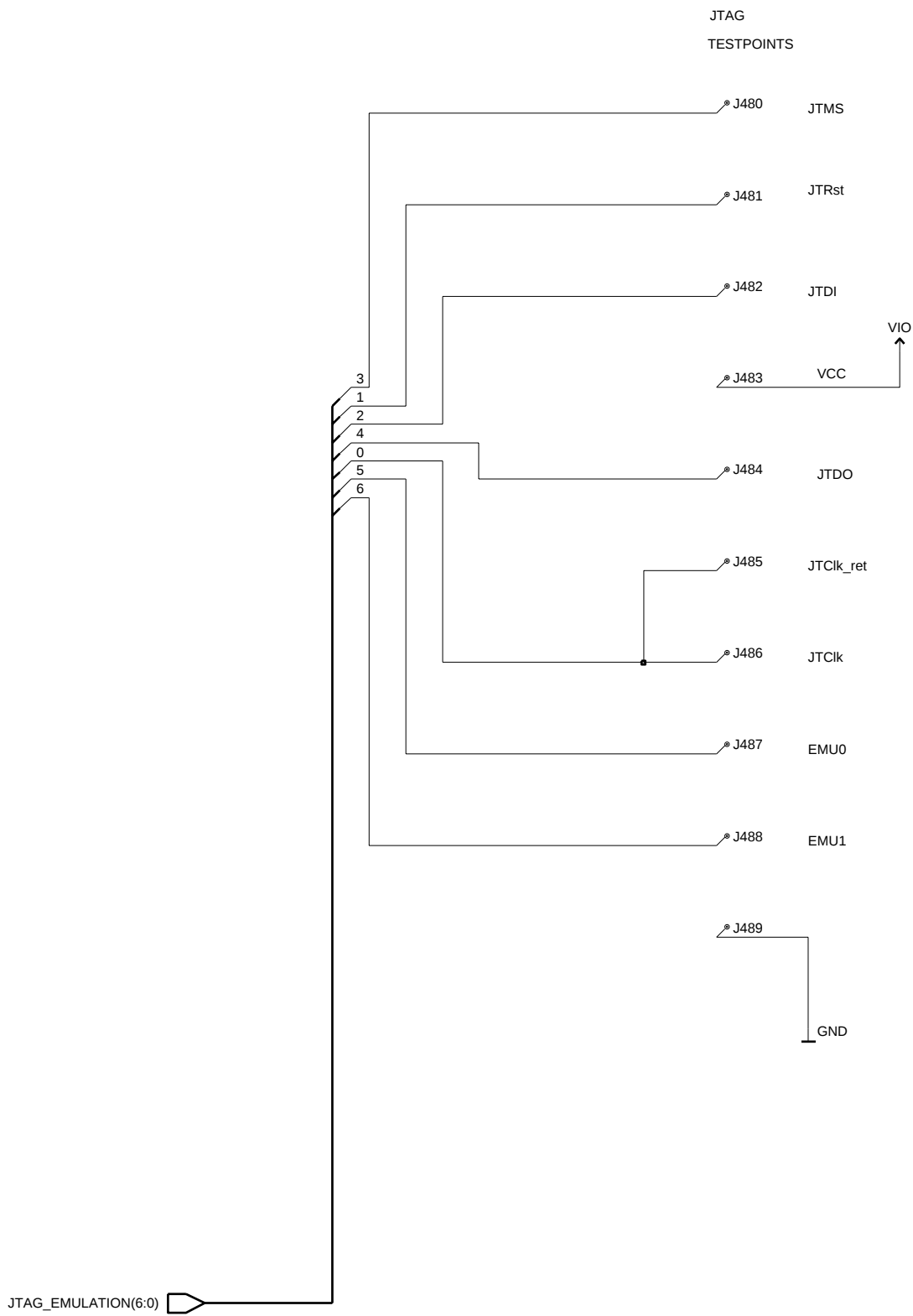
G_MEMORY(3:0)



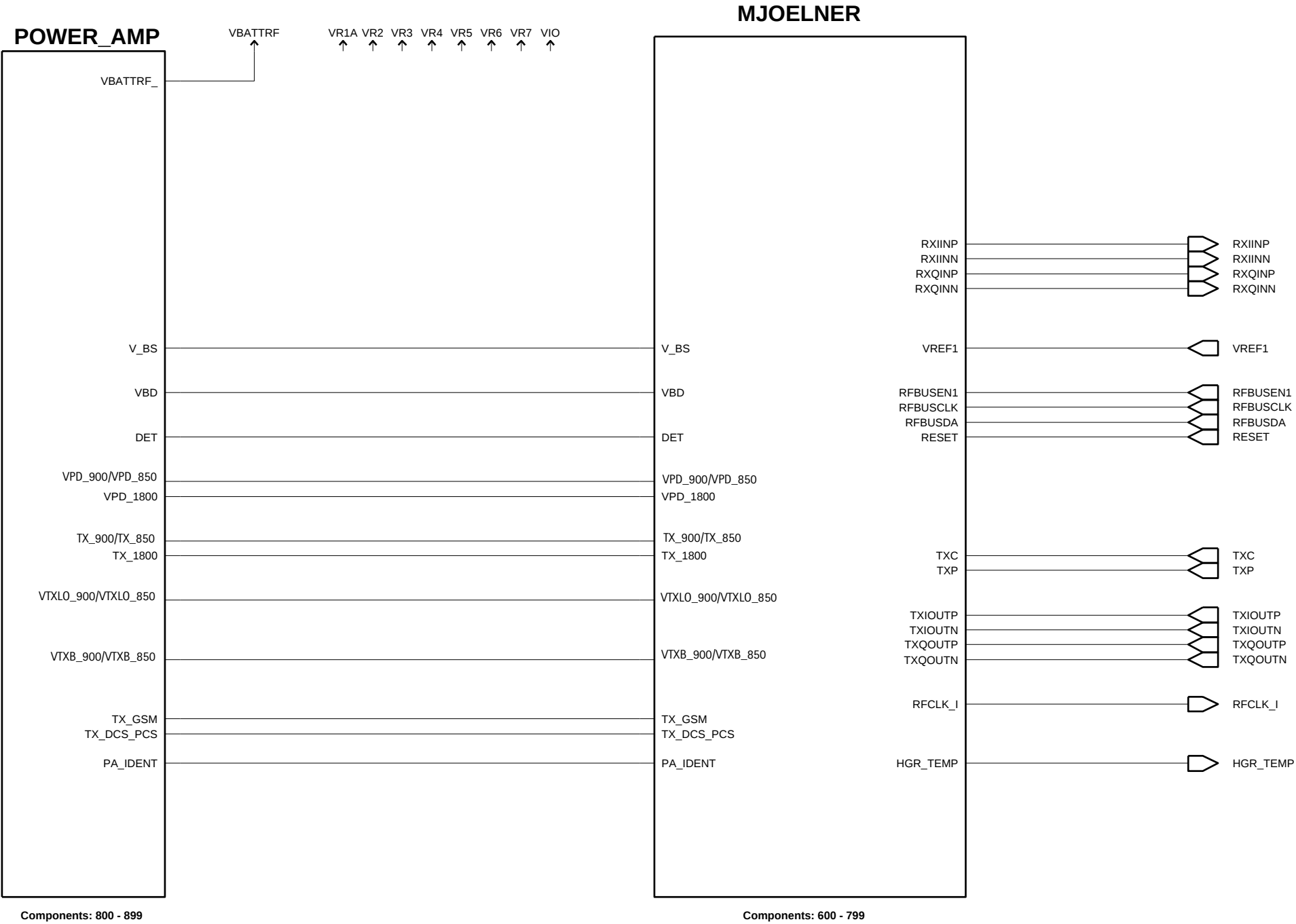
Title: Test and Emulator Inteface



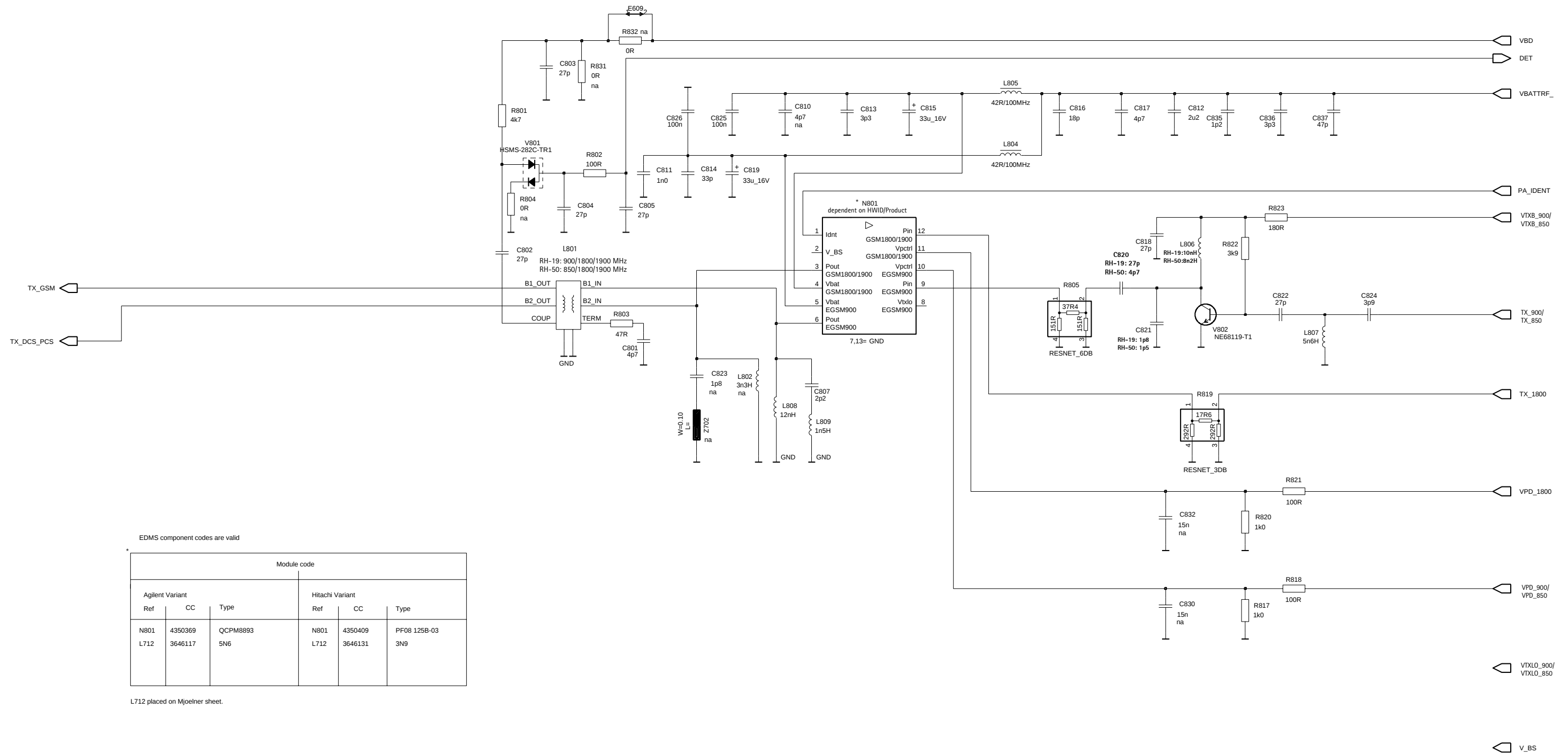
Title: Testpoints for JTAG Emulator



Title: RF Top Sheet



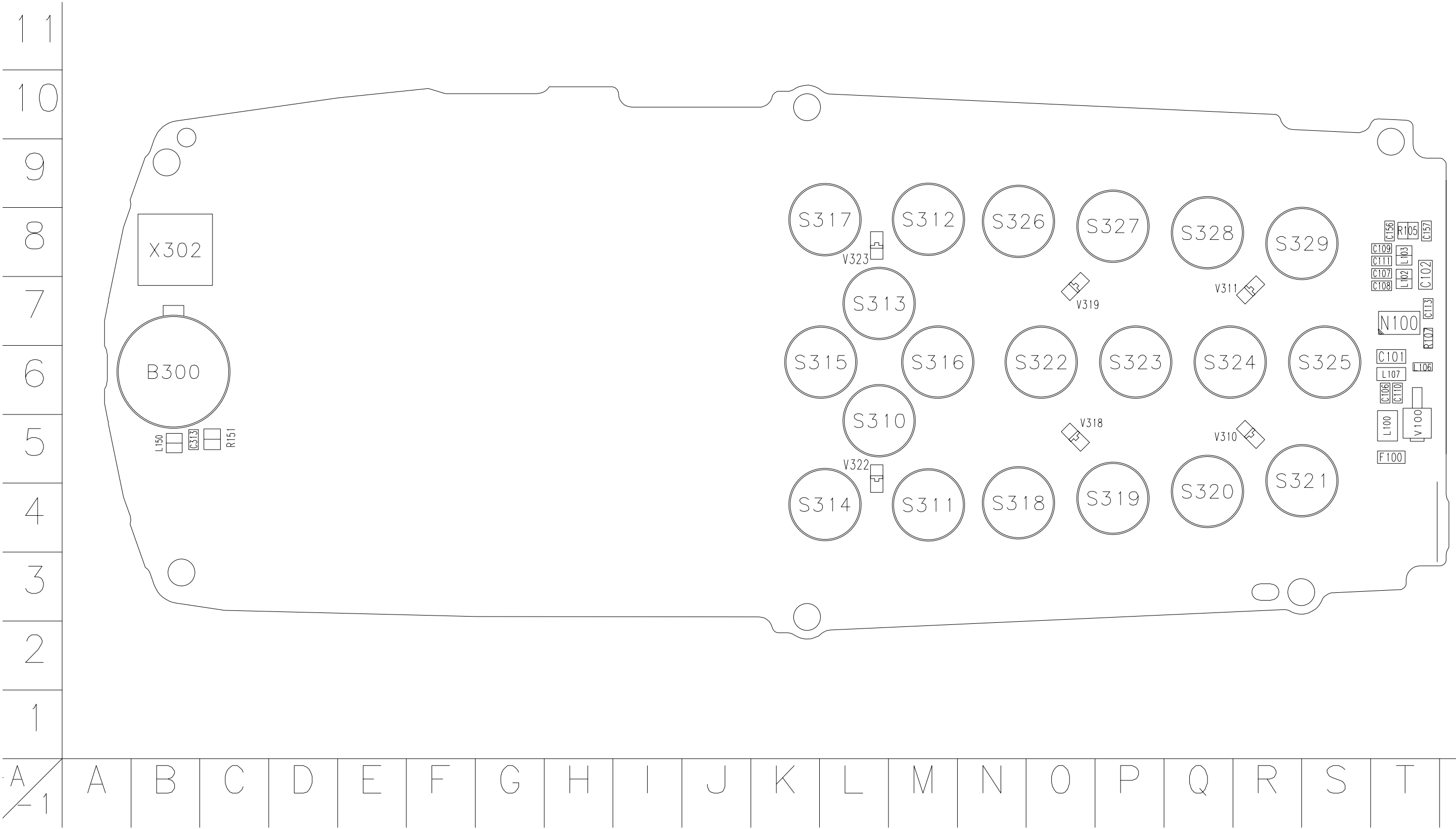
Title: Power Amplifier



EDMS component codes are valid					
			Module code		
Agilent Variant			Hitachi Variant		
Ref	CC	Type	Ref	CC	Type
N801	4350369	QCPM8893	N801	4350409	PF08 125B-03
L712	3646117	5N6	L712	3646131	3N9

L712 placed on Mjoelner sheet.

Component layout diagram, top



Component layout diagram, bottom

(Components in red = not assembled)

