ZZZ1	ZZZ3	ZZZ4	ZZZ5	ZZZ6	ZZZ7	ZZZ8	ZZZ9
LA-9902P DAG1@	LA-9902P DAG2@	LS-9901P DA2@	LS-9902P DA2@	LS-9903P DAG1@	LS-9904P DAG1@	LA-9901P DA2G1@	LA-9901P DA2G2@

Compal Confidential

G400S/G500S UMA M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

LA-9902P

2013-05-06

REV:1.0

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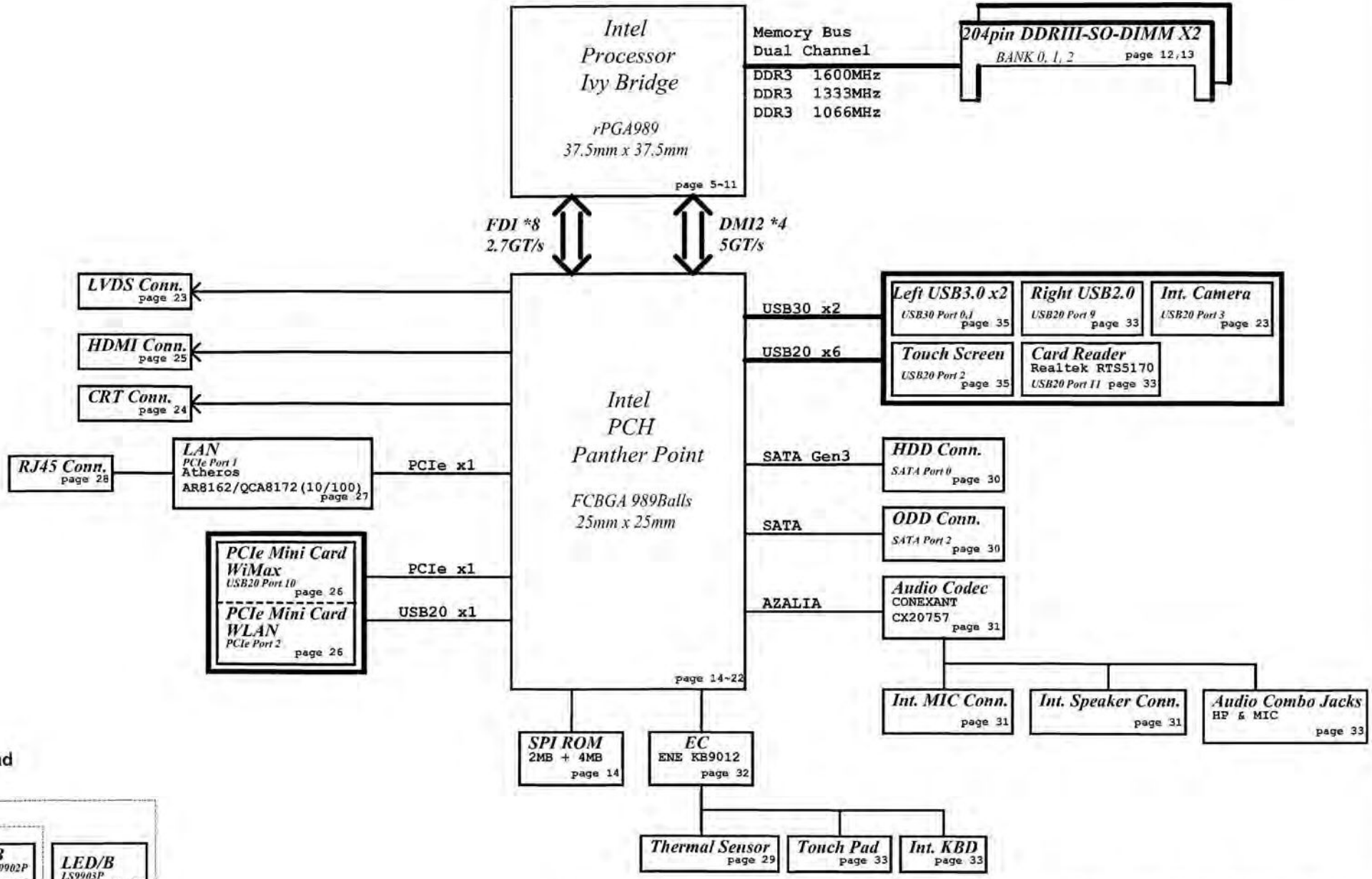
Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 1 of 52

Compal confidential
File Name :LA-9902P

Chief River



Sub-borad

15"

14"

Power/B LS9902P page 33	LED/B LS9903P page 33
IO/B LS9901P page 33	ODD/B LS9904P page 30

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SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 2 of 52

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID table for AD channel

Vcc	3.3V
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001 100xb

PCH SM Bus address

Device	Address
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	USB Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB/B (Right Side USB2.0)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
45 LEVEL	45@
Connector	ME@
For VILG2 (14")	14@
For VILG1 (15")	15@
HDMI	HDMI@
Camera	CMOS@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
10/100 LAN(AR8162L)	8162@
10/100 LAN(QCA8172)	8172@
Green clock(DIS sku)	GCLK304@
Green clock(UMA sku)	GCLK244@
Green clk support	GCLK@
No Green clk support	NOGCLK@
Touch Screen SKU	TS@
Optimus SKU	OPT@
UMA SKU	UMA@
PCH(NM70 sku)	NM70@
PCH(HM70 sku)	HM70@
PCH(HM76 sku)	HM76@
VRAM(1000MHz)	1000M@
VRAM(900MHz)	900M@
Unpop	@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	V +3VS_VGA	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS_VGA	X	V +3VS	X	X	V +3VS	X

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Title: SCHEMATIC M/B LA-9902

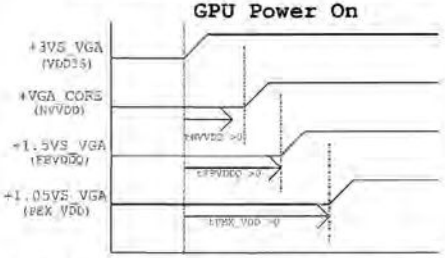
Size: B | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 2 of 52

N14x GPIO Pin Definition Table

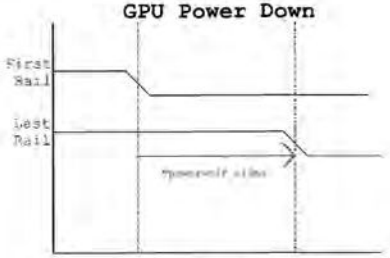
Pin Name	Normal Function	I/O	Functional Description	Default PU/PD
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID:Strap to boot FBVDD/Q
GPIO2~4	Non-support for LCD	O	Panel	100k PD
GPIO5	Reserve			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100k PD
GPIO8	OVERT	IO	Active Low Thermal Catastrophic Over Temperature	100k PU
GPIO9	ALERT	IO	Active Low Thermal Alert	100k PU
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100k PD
GPIO11	PWM_VID	O	GPU Core VDD PWM control supply overdraw input	
GPIO12	PWR_LEVEL	I	AC power detact or control signal	100k PU
GPIO13	PSI	O	Phase Shedding	PSI:100k PU to enable two phase
GPIO14~19	Non-support for HDA	I	Hot Plug	
GPIO20~21	Reserve			

GPU Power On



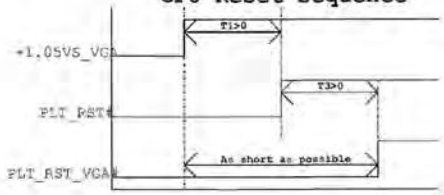
1. All power rail ramp up time should be larger than 400s
2. The total time for all rails to rise should be within 8ms
3. A power rail has to ramp up 90% before the next power rail in sequence can start ramping up
4. No signal should be applied to the GPU before the power rail are fully ramped.

GPU Power Down

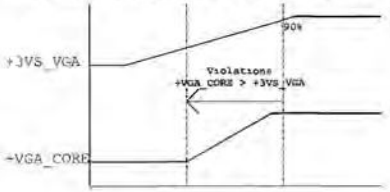


1.All GPU power rails should be turned off within 10ms

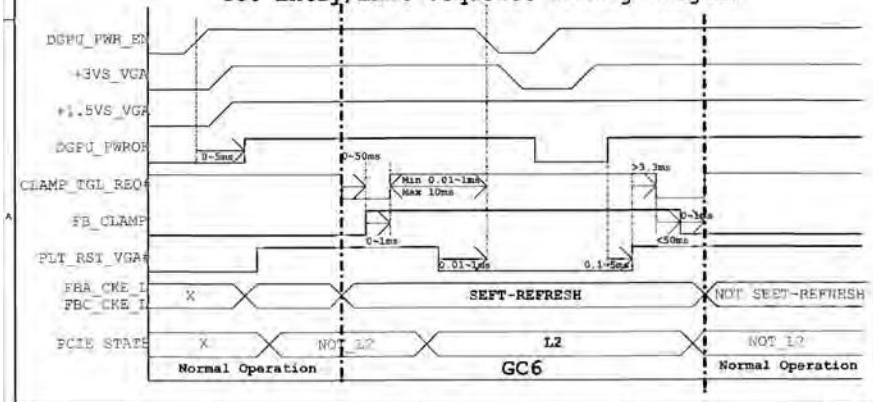
GPU Reset Sequence



Power sequencing violations



GC6 Entry/Exit Sequence Timing Diagram



For N14P-GV2 strap table

X76

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	1 GHz	128M* 16* 4 1GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M* 16* 4 1GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M* 16* 4 1GB	Hynix H5TQ2G63DFR-N0C	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 35K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M* 16* 4 2GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M* 16* 4 2GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PU 5K

For N14P-GS strap table

X76

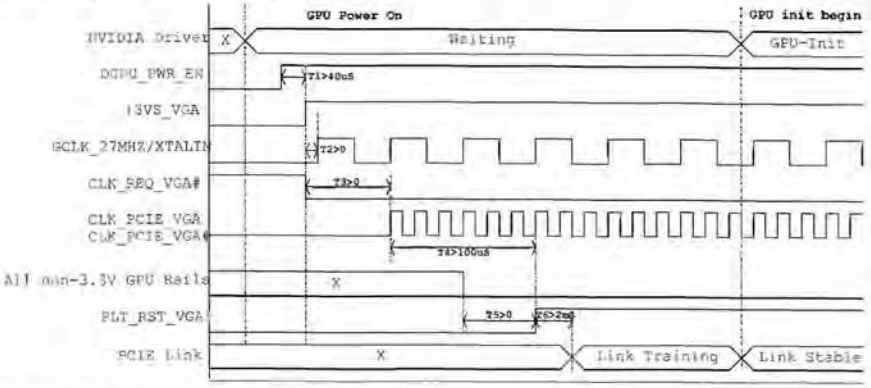
GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GS	1 GHz	128M* 16* 8 2GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M* 16* 8 2GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M* 16* 8 2GB	Hynix H5TQ2G63DFR-N0C	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 35K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M* 16* 8 4GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M* 16* 8 4GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PD 15K

For N14M-GE strap table

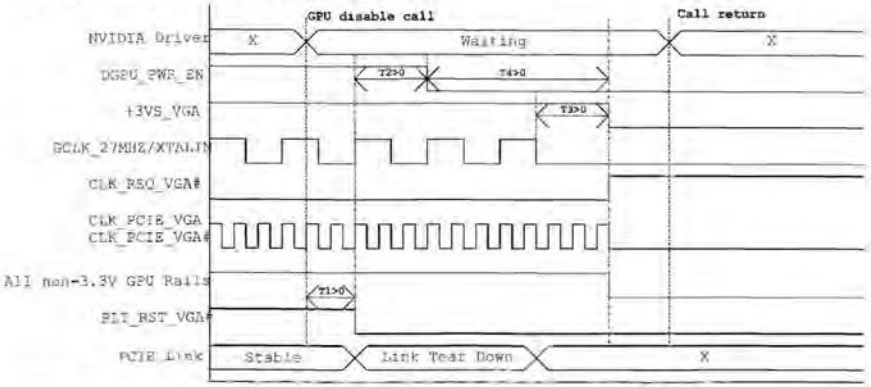
X76

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14M-GE	1 GHz	128M* 16* 4 1GB	Samsung K4W2G1646E-BC1A	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M* 16* 4 1GB	Micron MT41J128M16JT-093G:K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M* 16* 4 1GB	Hynix H5TQ2G63DFR-N0C	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M* 16* 4 2GB	Samsung K4W4G1646B-HC11	R PU 10K	R PD 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M* 16* 4 2GB	Micron MT41K256M16HA-107G:E	R PU 10K	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K

Optimus Typical Power-Up Sequence



Optimus Typical Power-Down Sequence



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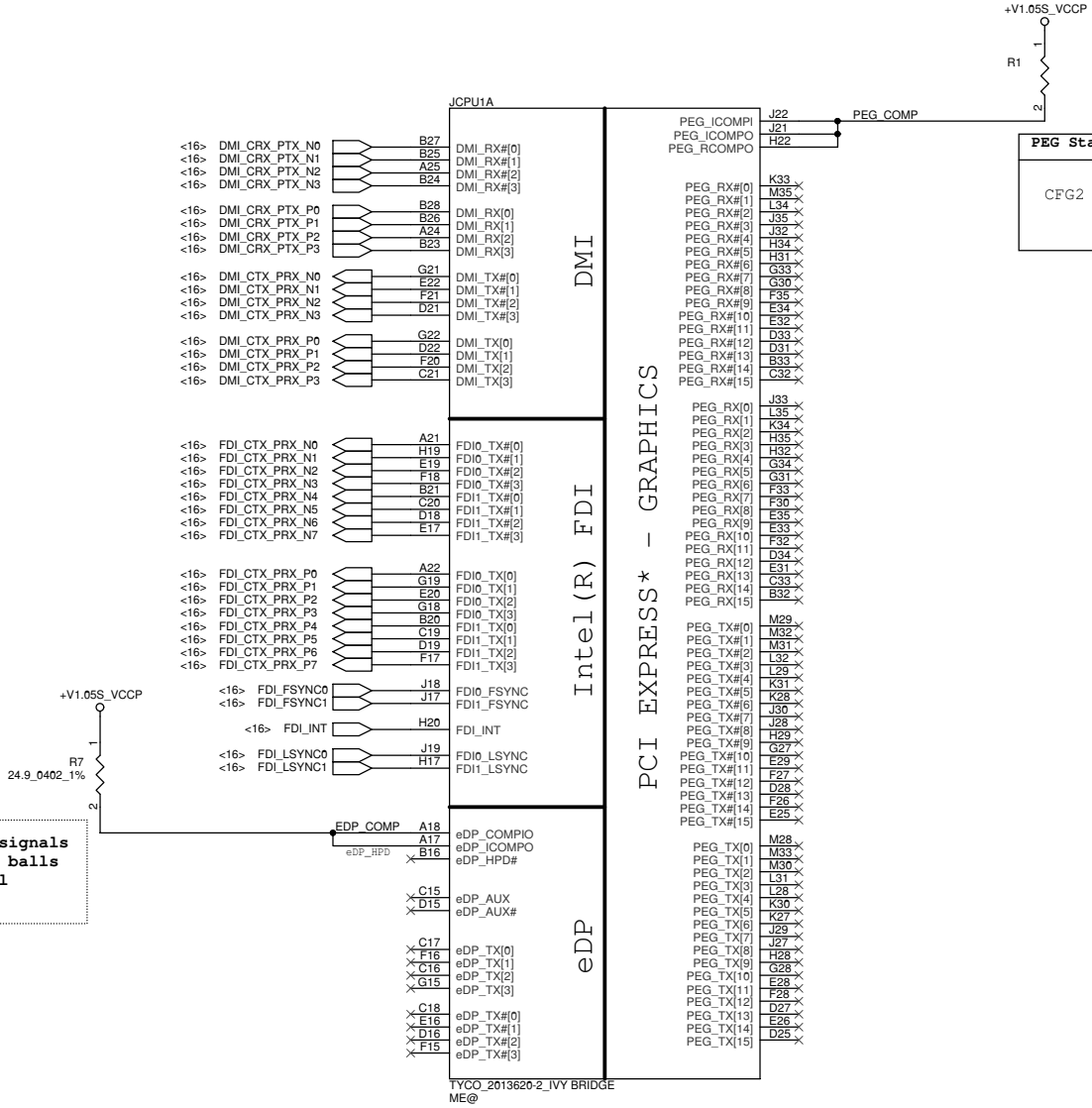
Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 4 of 52

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

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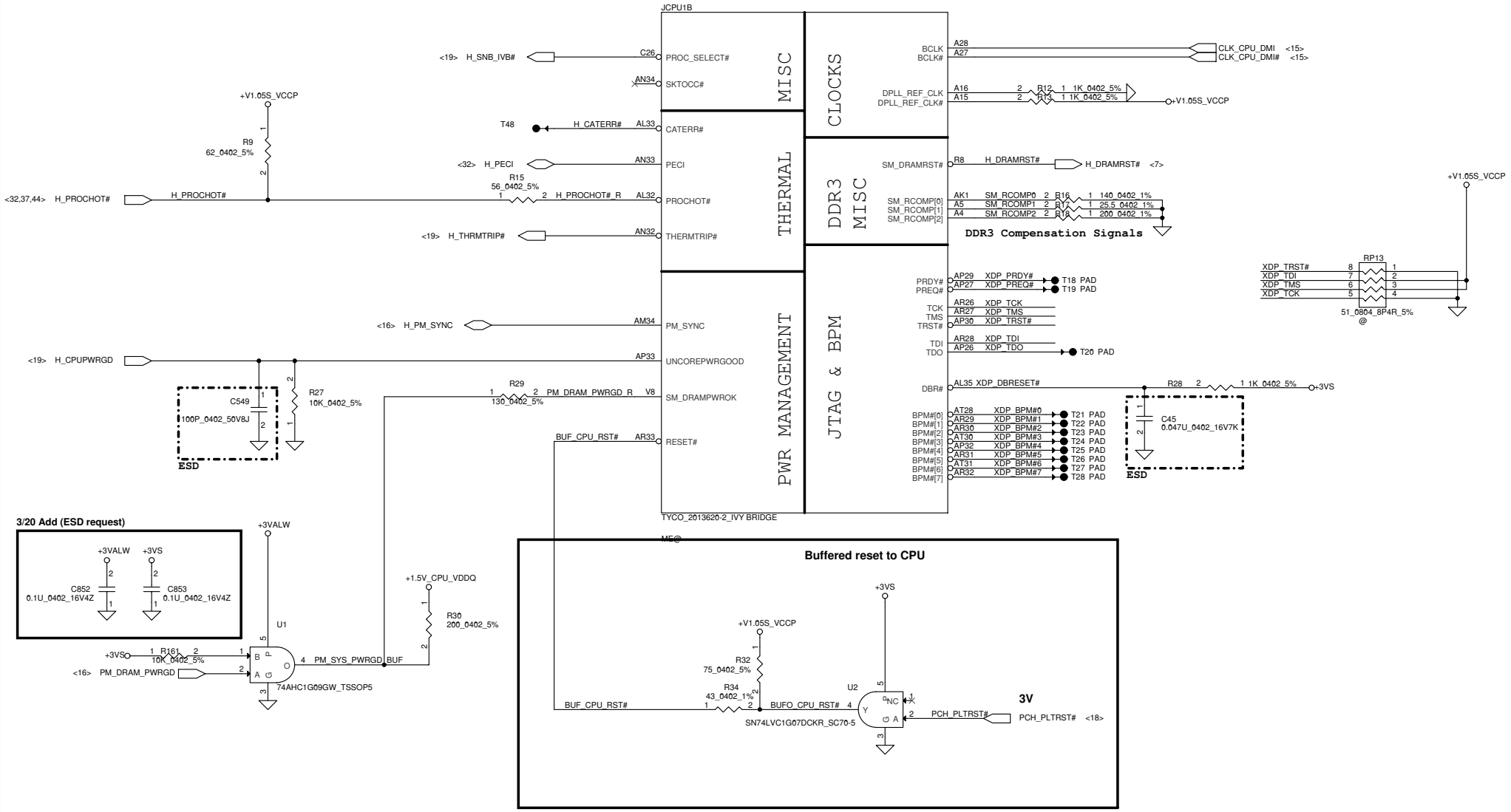
Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 5 of 52



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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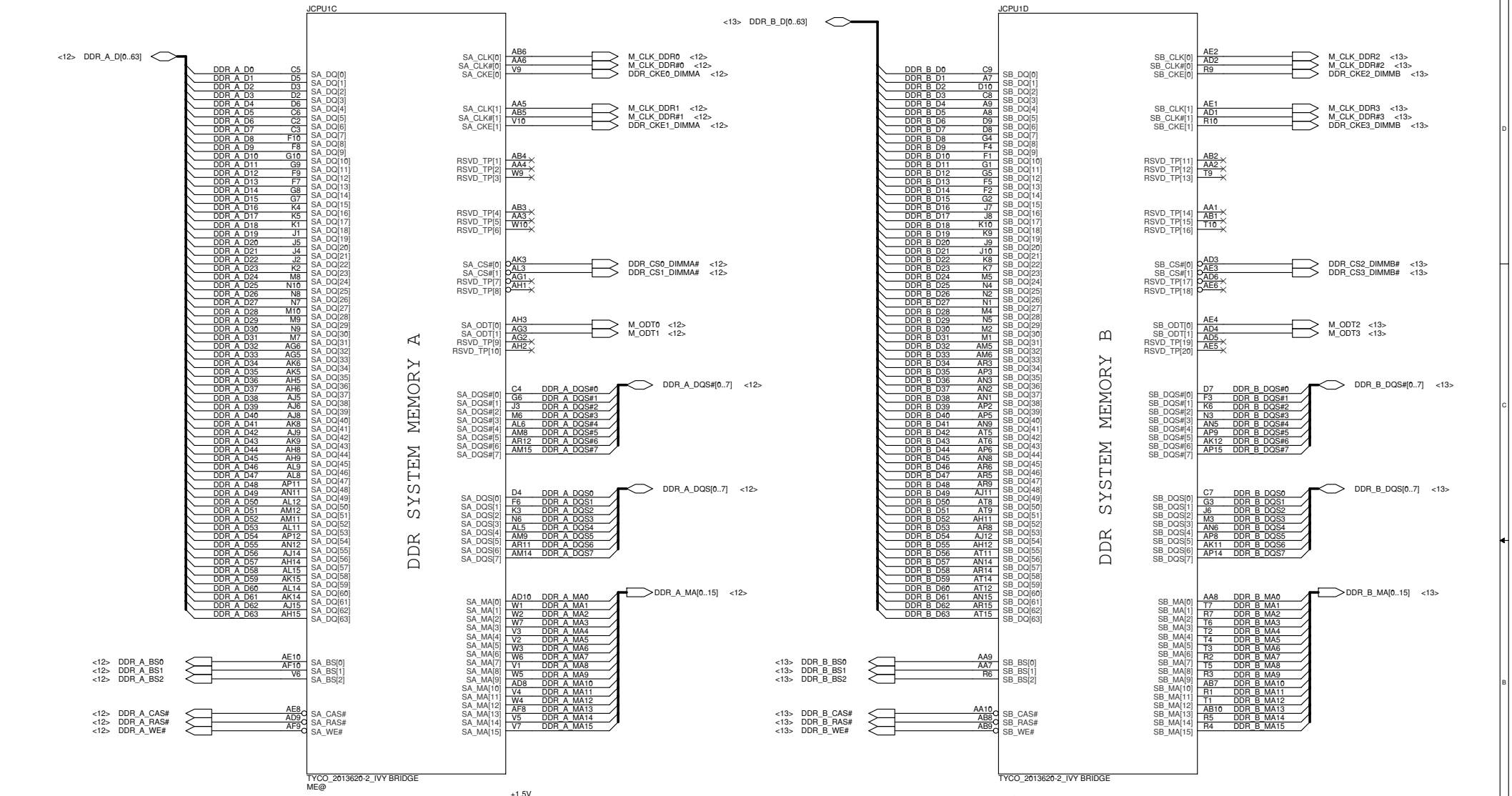
Date: Wednesday, May 08, 2013 | Sheet 6 of 52



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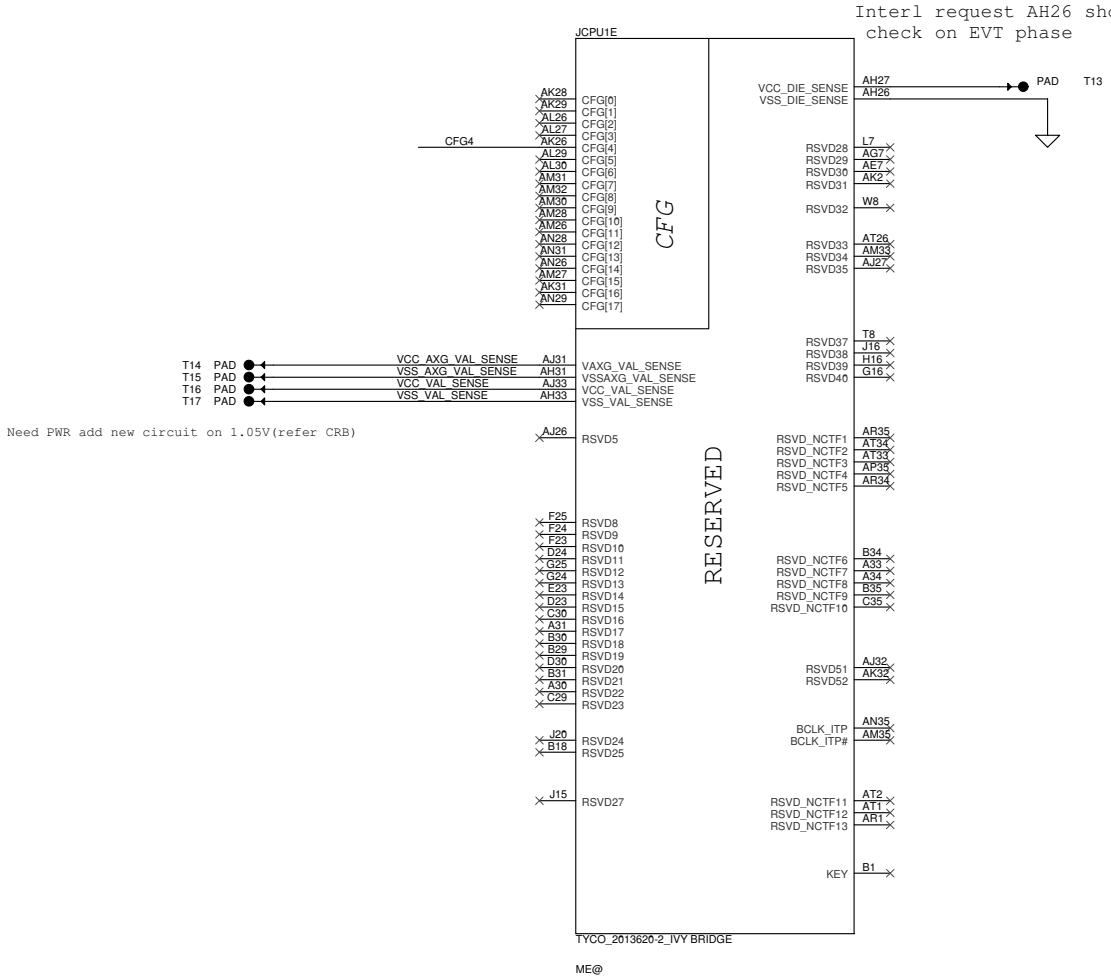
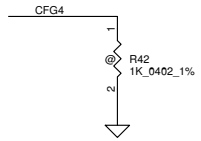
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: SCHEMATIC M/B LA-9902
				Size: Custom; Document Number: 4019N1; Rev: B
				Date: Wednesday, May 08, 2013; Sheet 7 of 52

CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled *10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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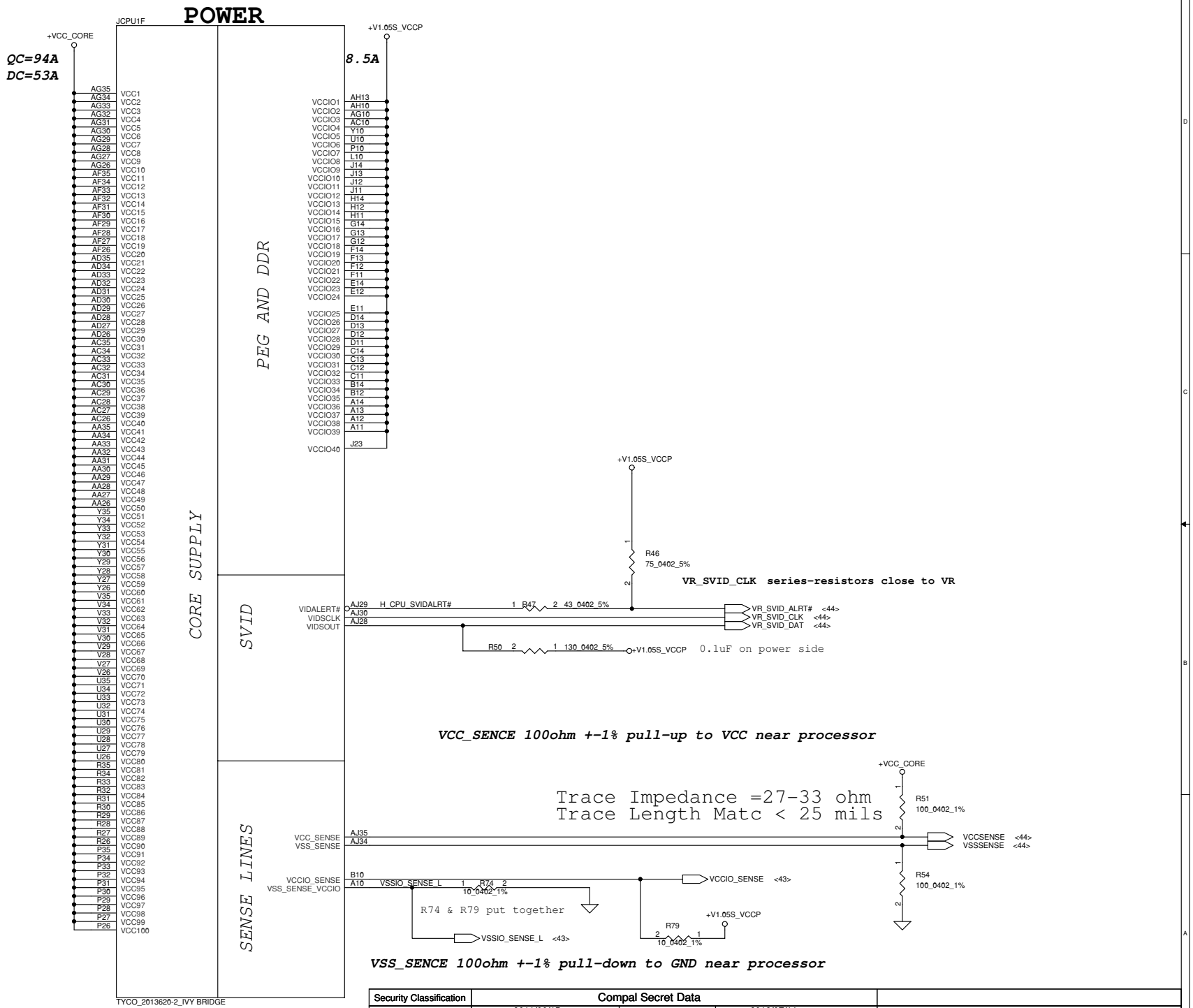
Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 8 of 52

POWER



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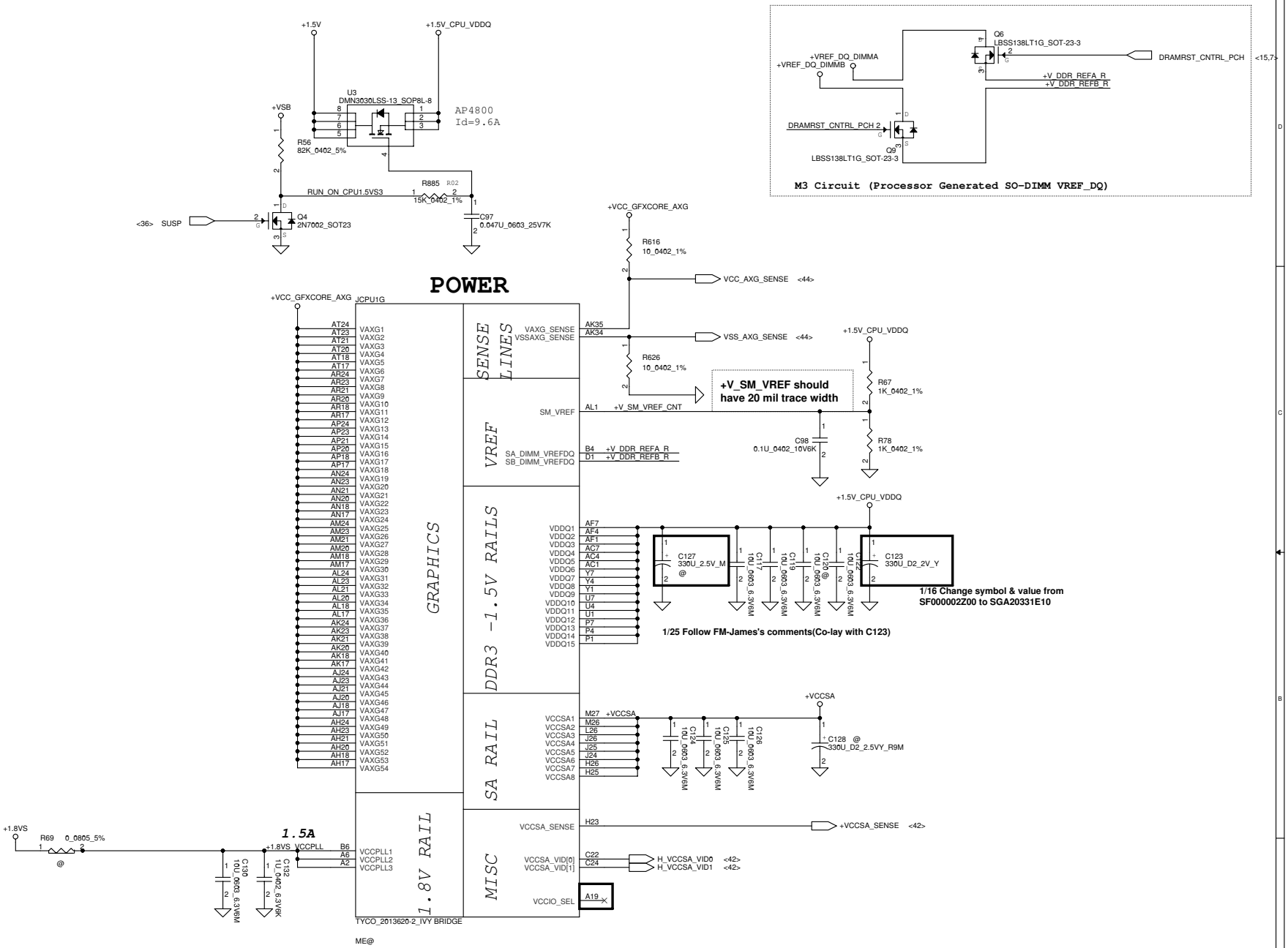
Size: Custom | Document Number: **4019N1** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 9 of 52



IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0
Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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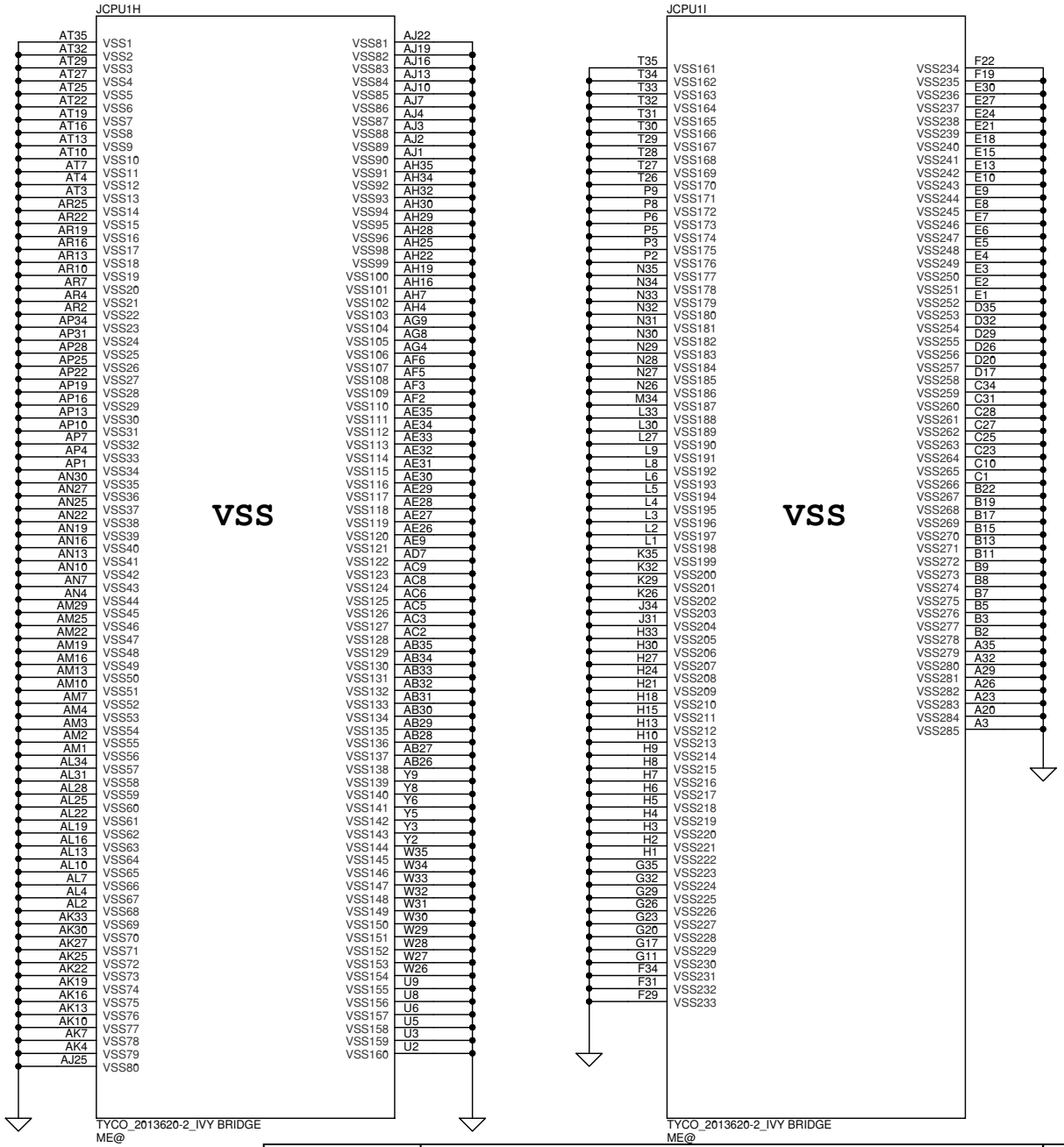
Size: Custom | Document Number: **4019N1** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 10 of 52



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Title: **SCHEMATIC M/B LA-9902**

Size: Custom | Document Number: **4019N1** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 11 of 52

DDR3 SO-DIMM A

3401.5V

JDIMM1

Pin	Signal	Pin	Signal
1	VREF_DQ	2	VSS1
3	VSS2	4	DQ4
5	DQ0	6	DQ5
7	DQ1	8	VSS3
9	VSS4	10	DQS#0
11	DM0	12	DQS0
13	VSS5	14	VSS6
15	DQ2	16	DQ6
17	DQ3	18	DQ7
19	VSS7	20	VSS8
21	DQ8	22	DQ12
23	DQ9	24	DQ13
25	VSS9	26	VSS10
27	DQS#1	28	DM1
29	DQS1	30	RESET#
31	VSS11	32	VSS12
33	DQ10	34	DQ14
35	DQ11	36	DQ15
37	VSS13	38	VSS14
39	DQ16	40	DQ20
41	DQ17	42	DQ21
43	VSS15	44	VSS16
45	DQS#2	46	DM2
47	DQS2	48	VSS17
49	VSS18	50	DQ22
51	DQ18	52	DQ23
53	DQ19	54	VSS19
55	VSS20	56	DQ28
57	DQ24	58	DQ29
59	DQ25	60	VSS21
61	VSS22	62	DQS#3
63	DM3	64	DQS3
65	VSS23	66	VSS24
67	DQ26	68	DQ30
69	DQ27	70	DQ31
71	VSS25	72	VSS26
73	CKE0	74	CKE1
75	VDD1	76	VDD2
77	NC1	78	A15
79	BA2	80	A14
81	VDD3	82	VDD4
83	A12/BC#	84	A11
85	A9	86	A7
87	VDD5	88	VDD6
89	A8	90	A6
91	A5	92	A4
93	VDD7	94	VDD8
95	A3	96	A2
97	A1	98	A0
99	VDD9	100	VDD10
101	CK0	102	CK1
103	CK0#	104	CK1#
105	VDD11	106	VDD12
107	A10/AP	108	BA1
109	BA0	110	RAS#
111	VDD13	112	VDD14
113	WE#	114	S0#
115	CAS#	116	ODT0
117	VDD15	118	VDD16
119	A13	120	ODT1
121	S1#	122	NC2
123	VDD17	124	VDD18
125	NCTEST	126	VREF_CA
127	VSS27	128	VSS28
129	DQ32	130	DQ36
131	DQ33	132	DQ37
133	VSS29	134	VSS30
135	DQS#4	136	DM4
137	DQS4	138	VSS31
139	VSS32	140	DQ38
141	DQ34	142	DQ39
143	DQ35	144	VSS33
145	VSS34	146	DQ44
147	DQ40	148	DQ45
149	DQ41	150	VSS35
151	VSS36	152	DQS#5
153	DQS#5	154	DQS5
155	DM5	156	VSS38
157	VSS37	158	DQ46
159	DQ42	160	DQ47
161	DQ43	162	VSS40
163	VSS39	164	DQ52
165	DQ48	166	DQ53
167	DQ49	168	VSS42
169	VSS41	170	DM6
171	DQS#6	172	VSS43
173	DQS6	174	DQ54
175	VSS44	176	DQ55
177	DQ50	178	VSS45
179	DQ51	180	DQ60
181	VSS46	182	DQ61
183	DQ56	184	VSS47
185	DQ57	186	DQS#7
187	VSS48	188	DQS7
189	DM7	190	VSS50
191	VSS49	192	DQ62
193	DQ58	194	DQ63
195	DQ59	196	VSS52
197	VSS51	198	EVENT#
199	SA0	200	SDA
201	VDDSPD	202	SCL
203	SA1	204	VTT2
205	VTT1	206	G2
	G1		

LCN_DAN06-K4806-0103
ME@

+VREF_DQ_DIMMA
+1.5V
+3V_DIMM
+3VS
+VREF_CA
+0.75VS

0.65A@0.75V

DDR_A_D0, DDR_A_D1, DDR_A_D2, DDR_A_D3, DDR_A_D8, DDR_A_D9, DDR_A_DQS#1, DDR_A_DQS1, DDR_A_D10, DDR_A_D11, DDR_A_D16, DDR_A_D17, DDR_A_DQS#2, DDR_A_DQS2, DDR_A_D18, DDR_A_D19, DDR_A_D24, DDR_A_D25, DDR_A_D26, DDR_A_D27, DDR_A_D32, DDR_A_D33, DDR_A_DQS#4, DDR_A_DQS4, DDR_A_D34, DDR_A_D35, DDR_A_D40, DDR_A_D41, DDR_A_D42, DDR_A_D43, DDR_A_D48, DDR_A_D49, DDR_A_DQS#6, DDR_A_DQS6, DDR_A_D50, DDR_A_D51, DDR_A_D56, DDR_A_D57, DDR_A_D58, DDR_A_D59

DDR_A_D4, DDR_A_D5, DDR_A_DQS#0, DDR_A_DQS0, DDR_A_D6, DDR_A_D7, DDR_A_D12, DDR_A_D13, DDR_A_D14, DDR_A_D15, DDR_A_D20, DDR_A_D21, DDR_A_D22, DDR_A_D23, DDR_A_D28, DDR_A_D29, DDR_A_DQS#3, DDR_A_DQS3, DDR_A_D30, DDR_A_D31, DDR_A_D36, DDR_A_D37, DDR_A_D38, DDR_A_D39, DDR_A_D44, DDR_A_D45, DDR_A_DQS#5, DDR_A_DQS5, DDR_A_D46, DDR_A_D47, DDR_A_D52, DDR_A_D53, DDR_A_D54, DDR_A_D55, DDR_A_D60, DDR_A_D61, DDR_A_DQS#7, DDR_A_DQS7, DDR_A_D62, DDR_A_D63

<7> DDR_CKE0_DIMMA — DDR_CKE0_DIMMA
DDR_CKE1_DIMMA — DDR_CKE1_DIMMA <7>
<7> DDR_A_BS2 — DDR_A_BS2
DDR_A_MA12, DDR_A_MA9, DDR_A_MA8, DDR_A_MA5, DDR_A_MA3, DDR_A_MA1
DDR_A_MA15, DDR_A_MA14, DDR_A_MA11, DDR_A_MA7, DDR_A_MA6, DDR_A_MA4, DDR_A_MA2, DDR_A_MA0
<7> M_CLK_DDR0, <7> M_CLK_DDR#0 — M_CLK_DDR0, M_CLK_DDR#0
M_CLK_DDR1 <7>, M_CLK_DDR#1 <7>
<7> DDR_A_BS0 — DDR_A_MA10, DDR_A_BS0
DDR_A_BS1 <7>, DDR_A_RAS# <7>
<7> DDR_A_WE#, <7> DDR_A_CAS# — DDR_A_WE#, DDR_A_CAS#
DDR_CS0_DIMMA# — DDR_CS0_DIMMA# <7>, M_ODT0 <7>
<7> DDR_CS1_DIMMA# — DDR_A_MA13, DDR_CS1_DIMMA#
M_ODT1 <7>
SMB_DATA_S3 — SMB_DATA_S3 <13,15,26>
SMB_CLK_S3 — SMB_CLK_S3 <13,15,26>

<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

DDR3_DRAMRST# — DDR3_DRAMRST# <13,7>

RP15: +VREF_DQ_DIMMA, +VREF_DQ_DIMMB, +1.5V, 1K_0804_8P4R_1%
RP16: +VREF_CA, +VREF_CB, +1.5V, 1K_0804_8P4R_1%

C133 0.1U_0402_10V6K
C135 0.1U_0402_10V6K
C156 0.1U_0402_10V6K
R136 0_0402_5%

```
VDDQ(1.5V) =
   3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
   6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
   3*0805 10uf  4*0402 1uf
VREF =
   1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
   1*0402 0.1uf  1*0402 2.2uf
```

Layout Note:
Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

C139 10U_0603_6.3V6M, C140 10U_0603_6.3V6M, C141 10U_0603_6.3V6M, C142 10U_0603_6.3V6M, C143 10U_0603_6.3V6M, C144 10U_0603_6.3V6M, C145 @ 0.1U_0402_10V6K, C146 0.1U_0402_10V6K, C147 0.1U_0402_10V6K, C148 0.1U_0402_10V6K, C149 @ 220U_6.3V_M

Layout Note:
Place near DIMM

+0.75VS
C150 1U_0402_6.3V6K, C152 1U_0402_6.3V6K

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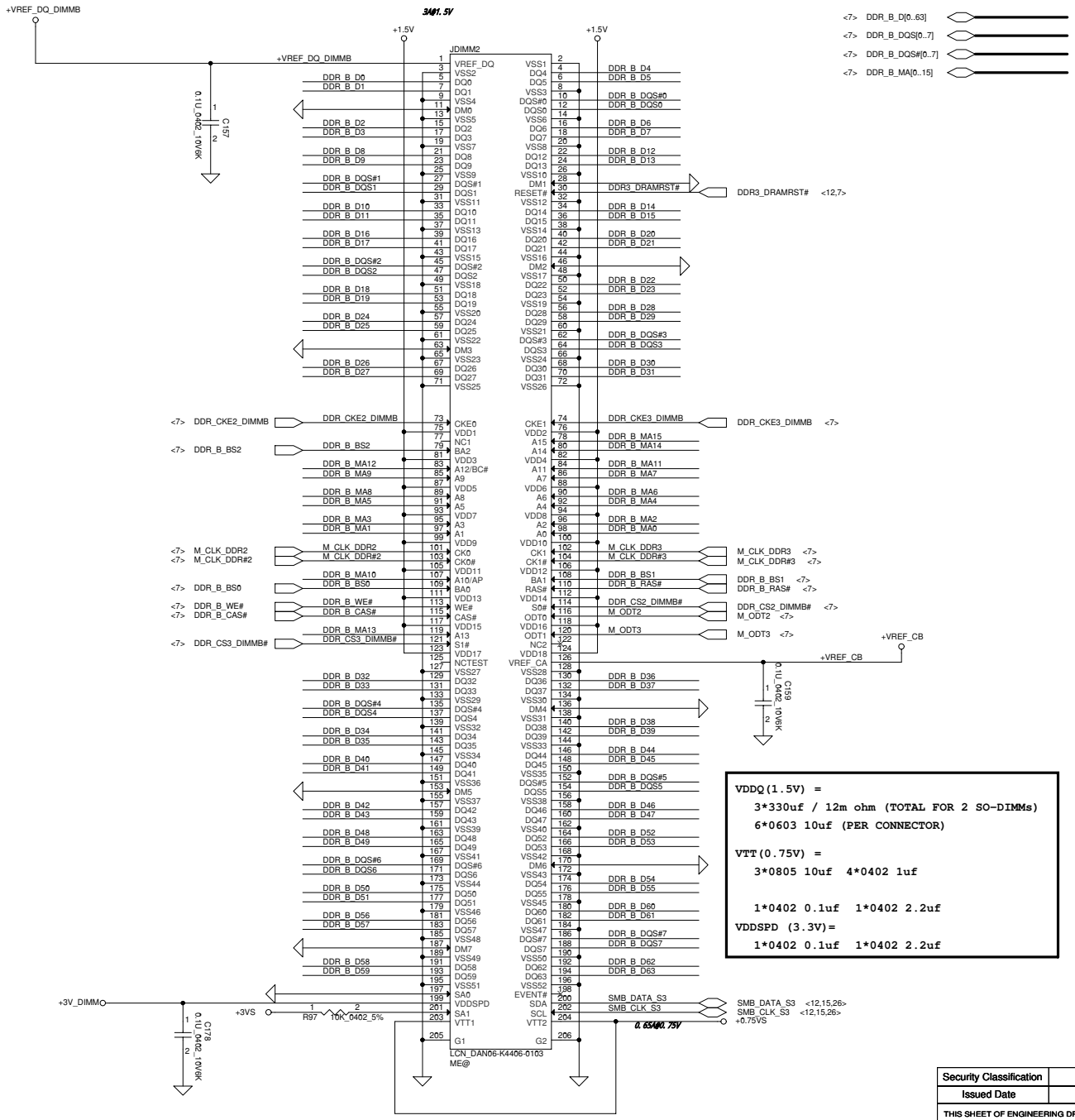
Size: Custom | Document Number: 4019N1 | Rev: B

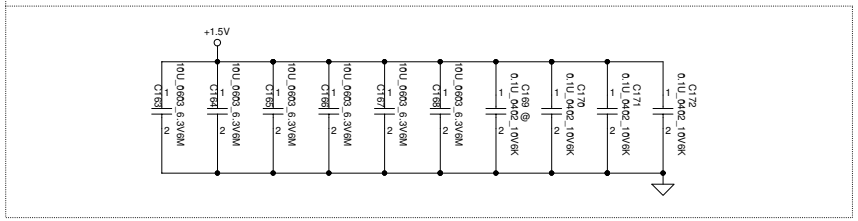
Date: Wednesday, May 08, 2013 | Sheet 12 of 52



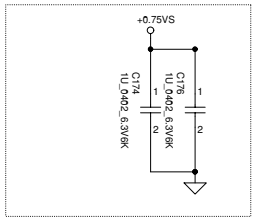
Layout Note:
Place near DIMM

*(10uF_0603_6.3V)*8*

*(0.1uF_402_10V)*4*



Layout Note:
Place near DIMM




```
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   6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
   3*0805 10uf  4*0402 1uf

   1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
   1*0402 0.1uf  1*0402 2.2uf
```

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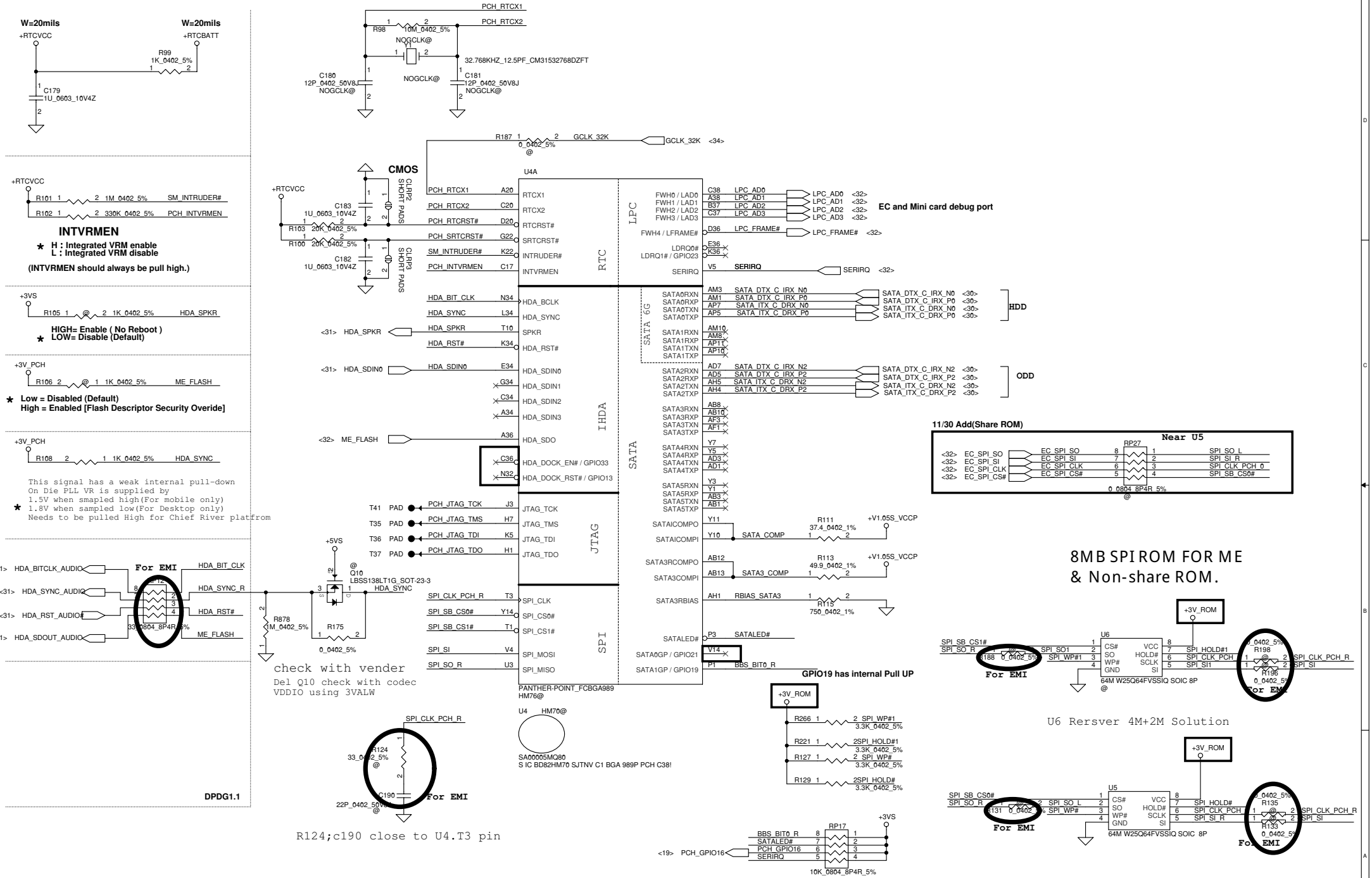
Size | Document Number: **4019N1** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 13 of 52



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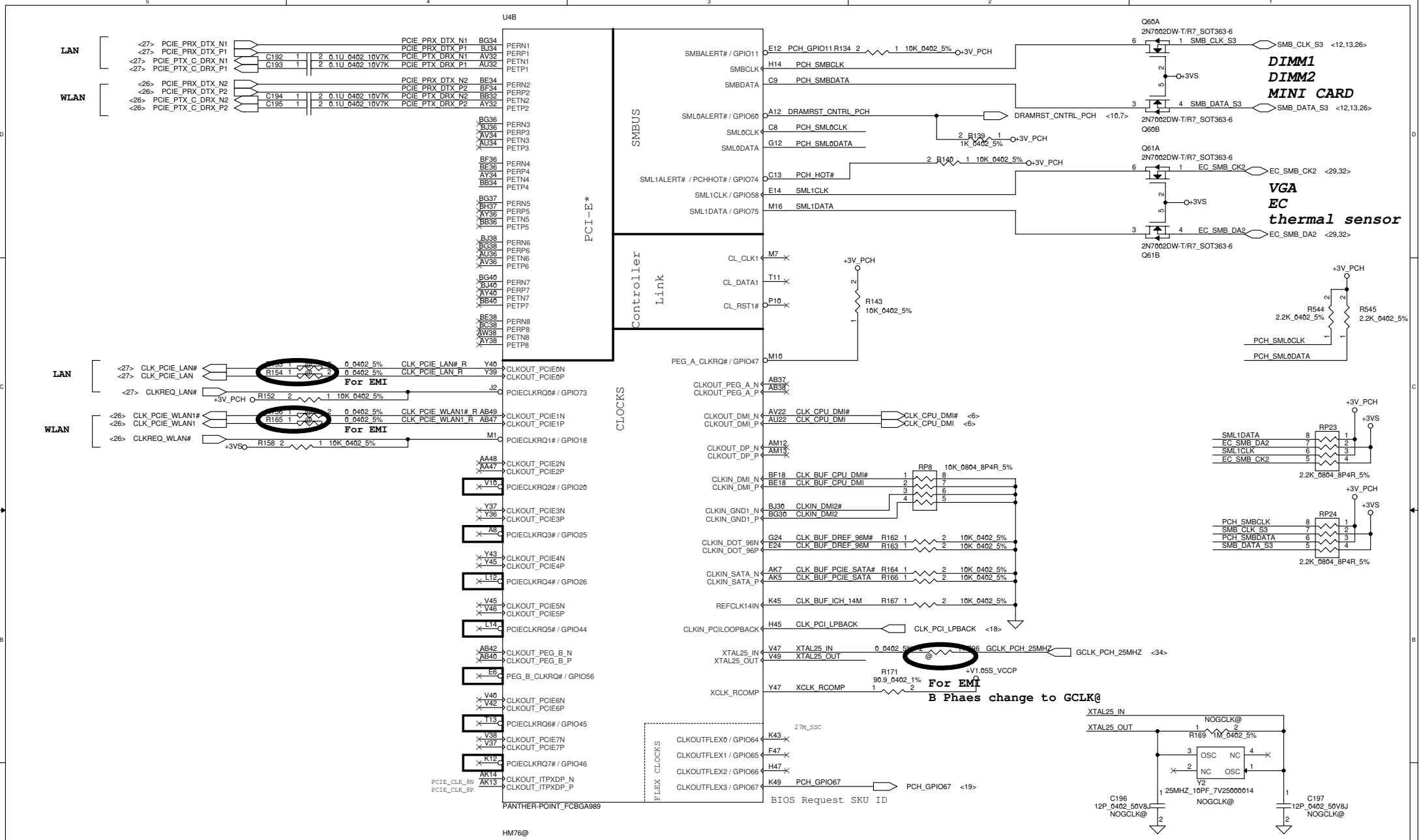
Date: Wednesday, May 08, 2013 | Sheet 14 of 52



Security Classification	Compal Secret Data		
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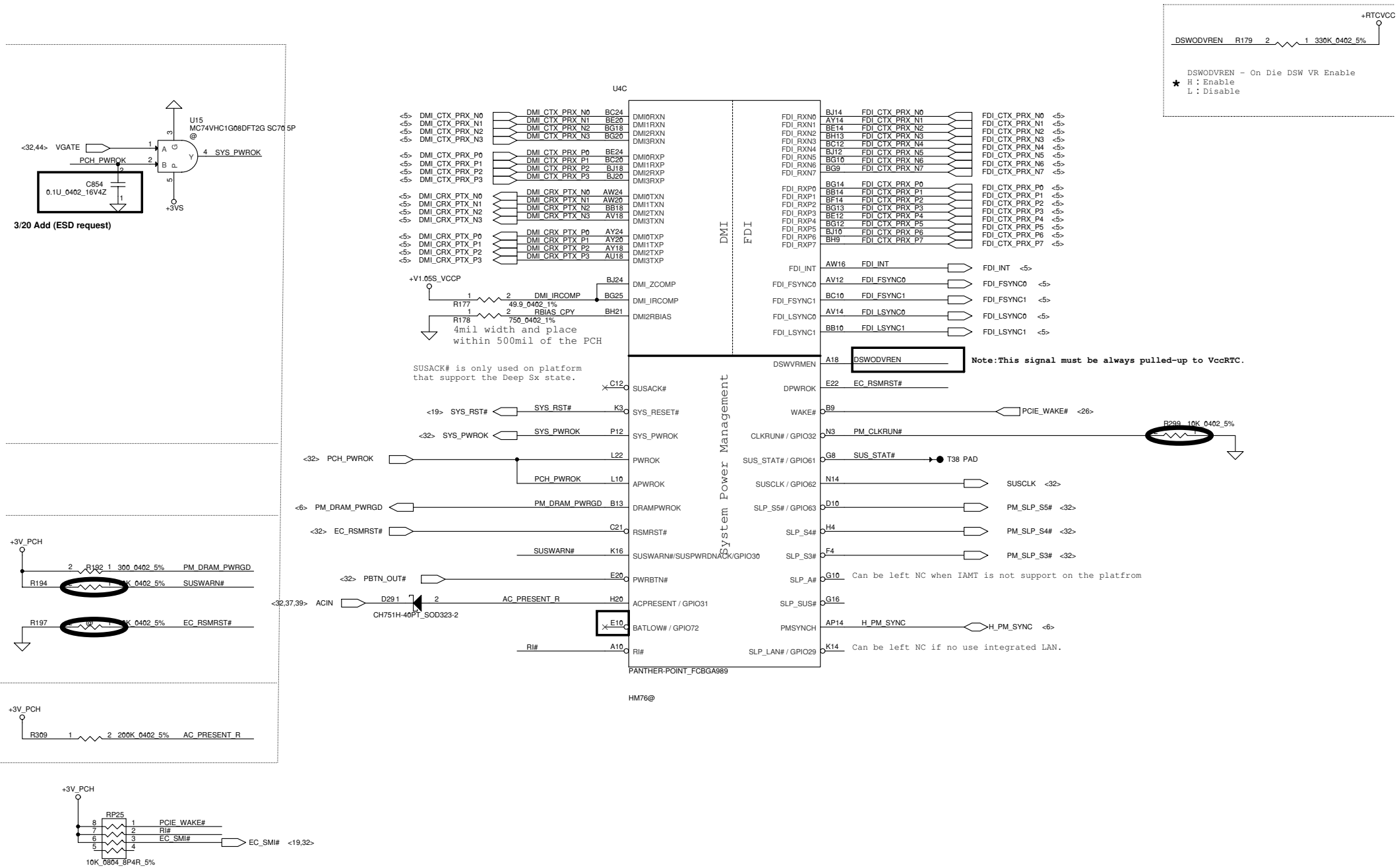
Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 15 of 52



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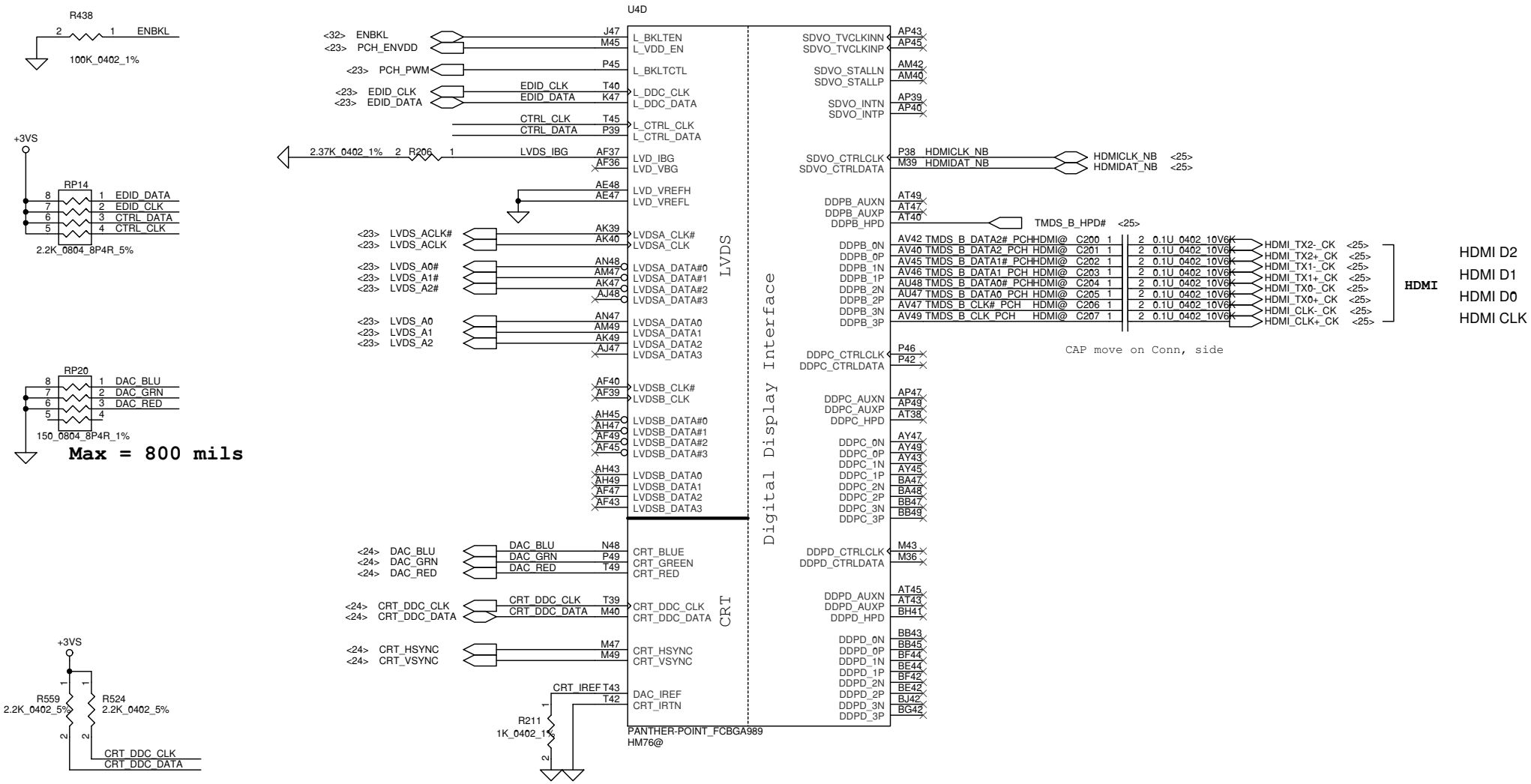
Date: Wednesday, May 08, 2013 | Sheet 16 of 52



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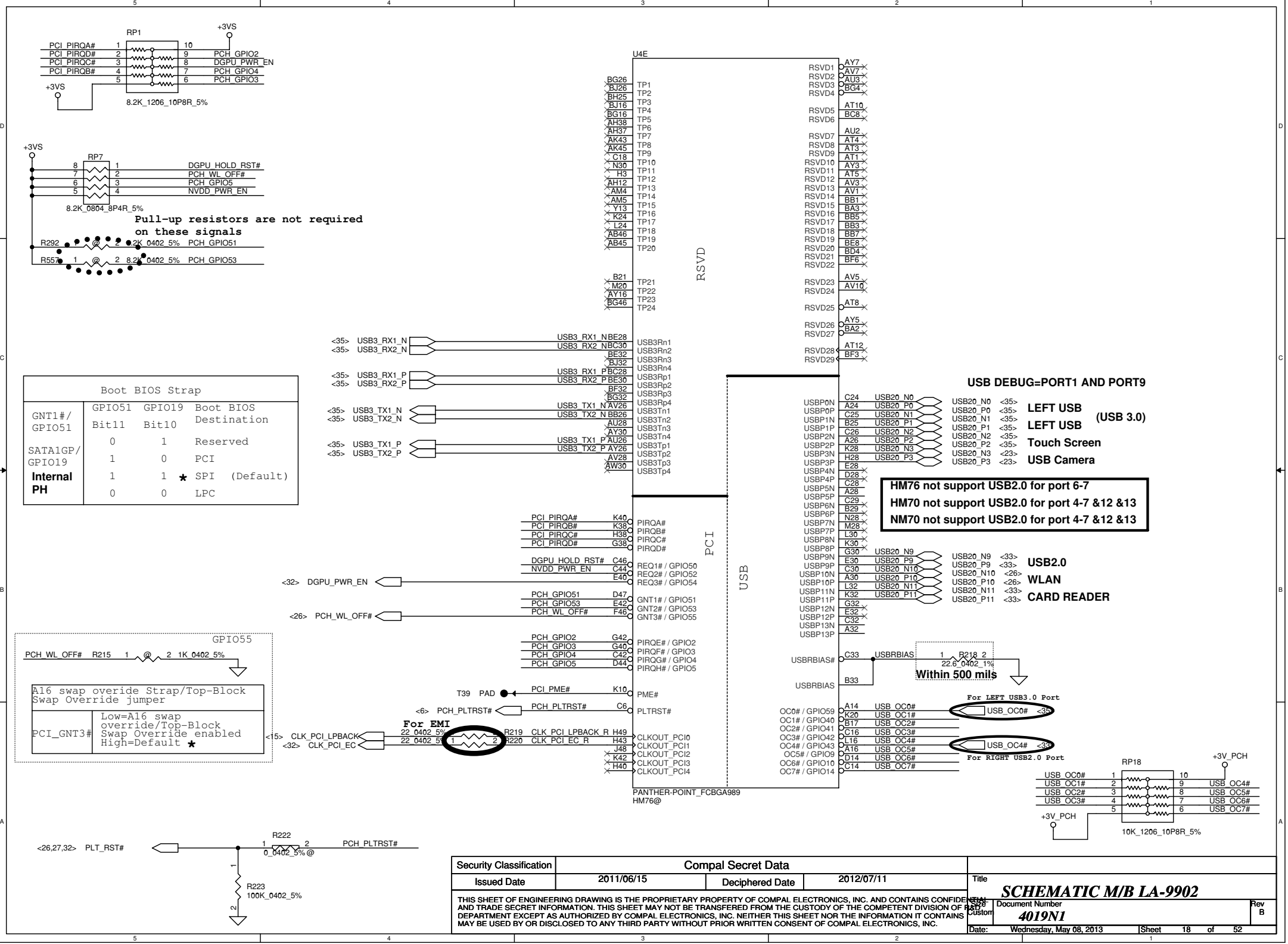
Size: B | Document Number: **4019N1** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 17 of 52



Boot BIOS Strap			
GNT1#/ GPIO51	GPIO51 Bit11	GPIO19 Bit10	Boot BIOS Destination
SATA1GP/ GPIO19	0	1	Reserved
	1	0	PCI
Internal PH	1	1 ★	SPI (Default)
	0	0	LPC

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

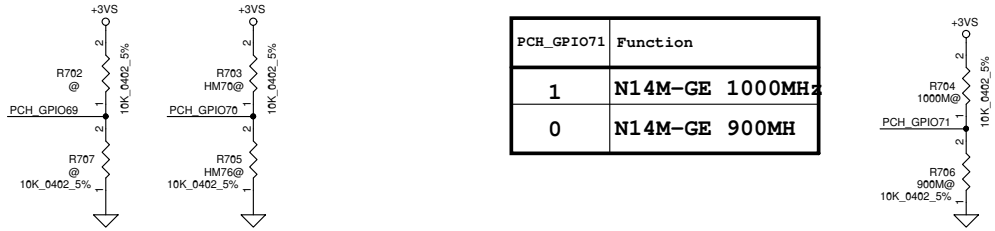
Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 18 of 52

PCH_GPIO69	PCH_GPIO70	Function
-	-	NM70
-	-	Reserved
-	1	HM70
-	0	HM76

PCH_GPIO71	Function
1	N14M-GE 1000MHz
0	N14M-GE 900MH



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

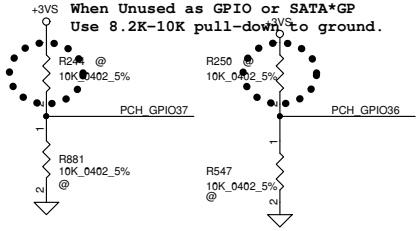
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

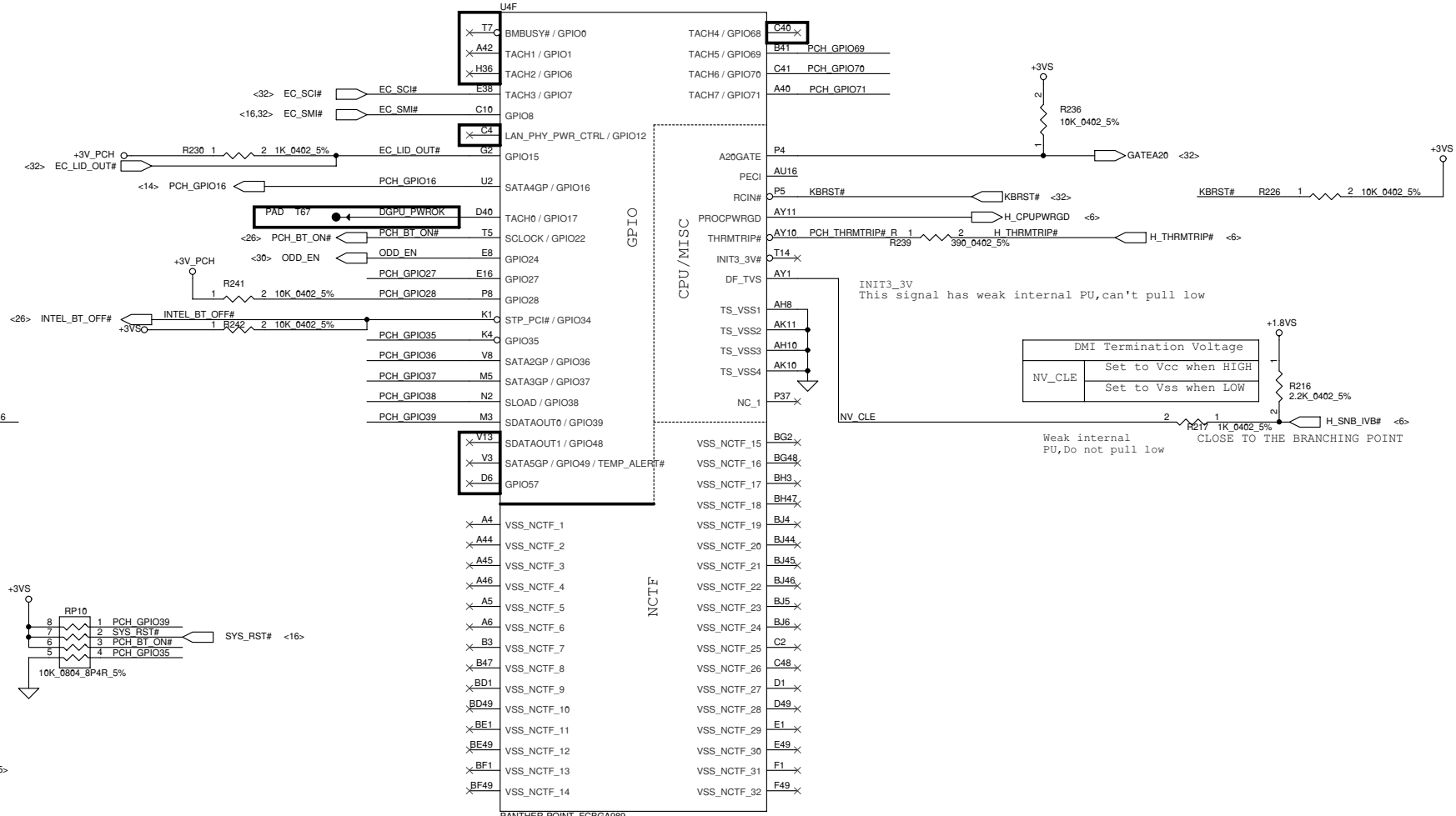
R240 1 @ 2 1K_0402_5% PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 1 @ 2 10K_0402_5% PCH_GPIO27

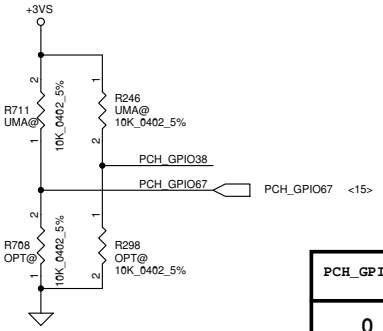
GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.





DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

BIOS Request SKU ID



PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

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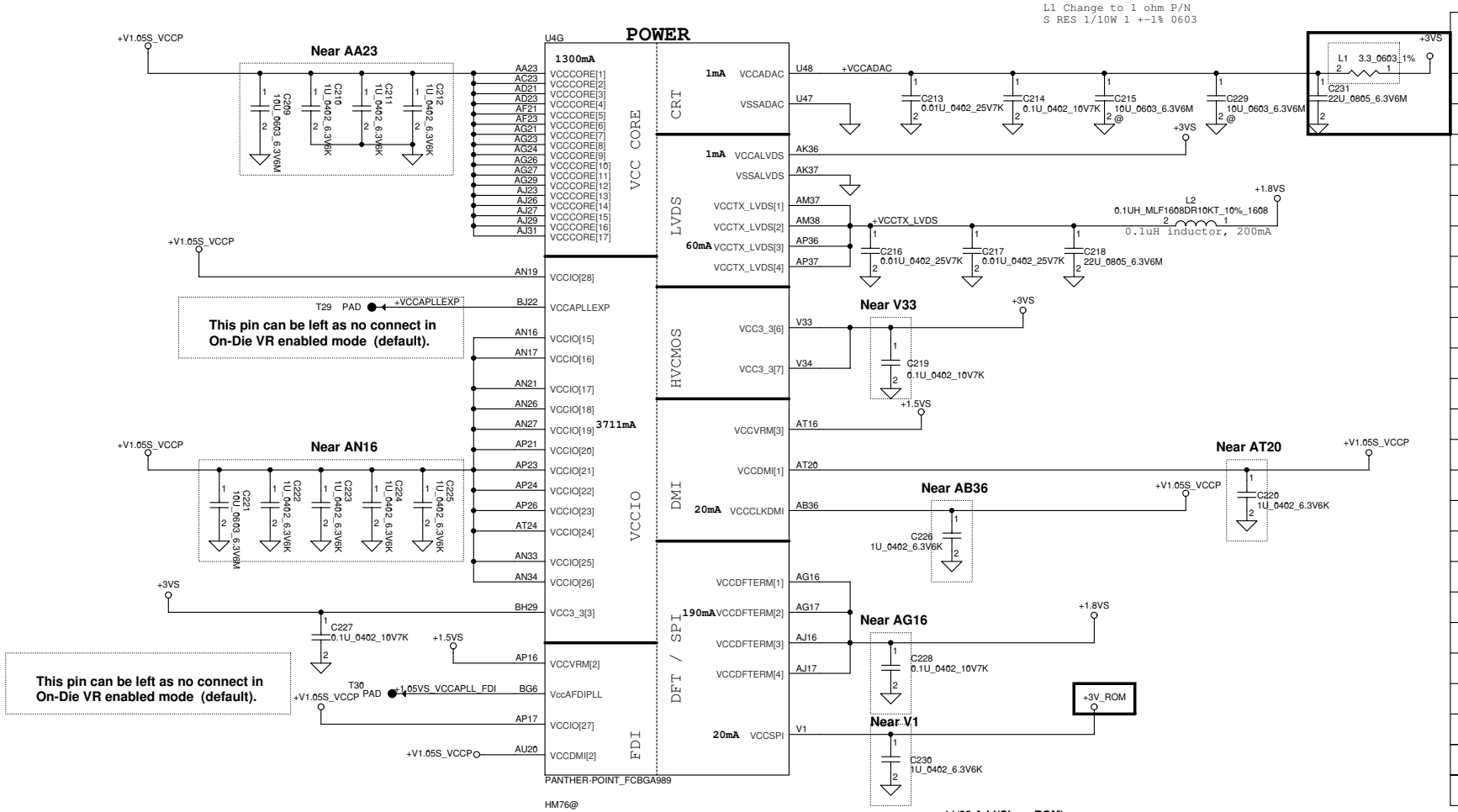
Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 19 of 52



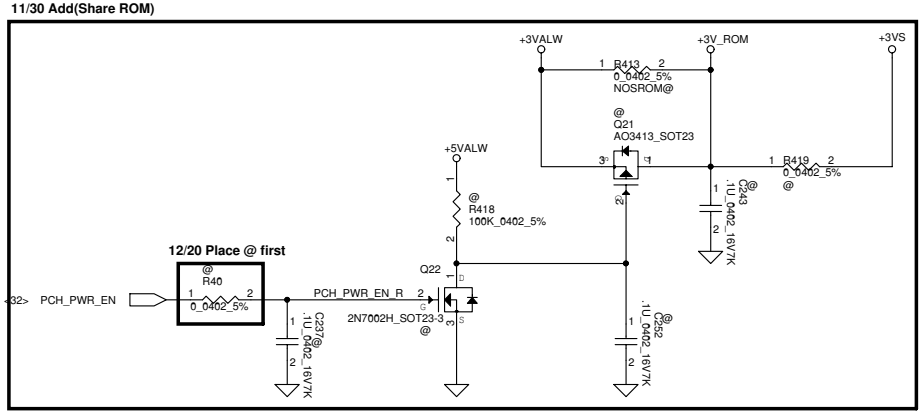
PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Intel recommand VCCVRM==>1.5V FOR MOBILE
stuff R265 and unstuff R266 VCCVRM==>1.8V FOR DESKTOP

VCCVRM = 160mA detal waiting for newest spec

11/30 Add(Share ROM)



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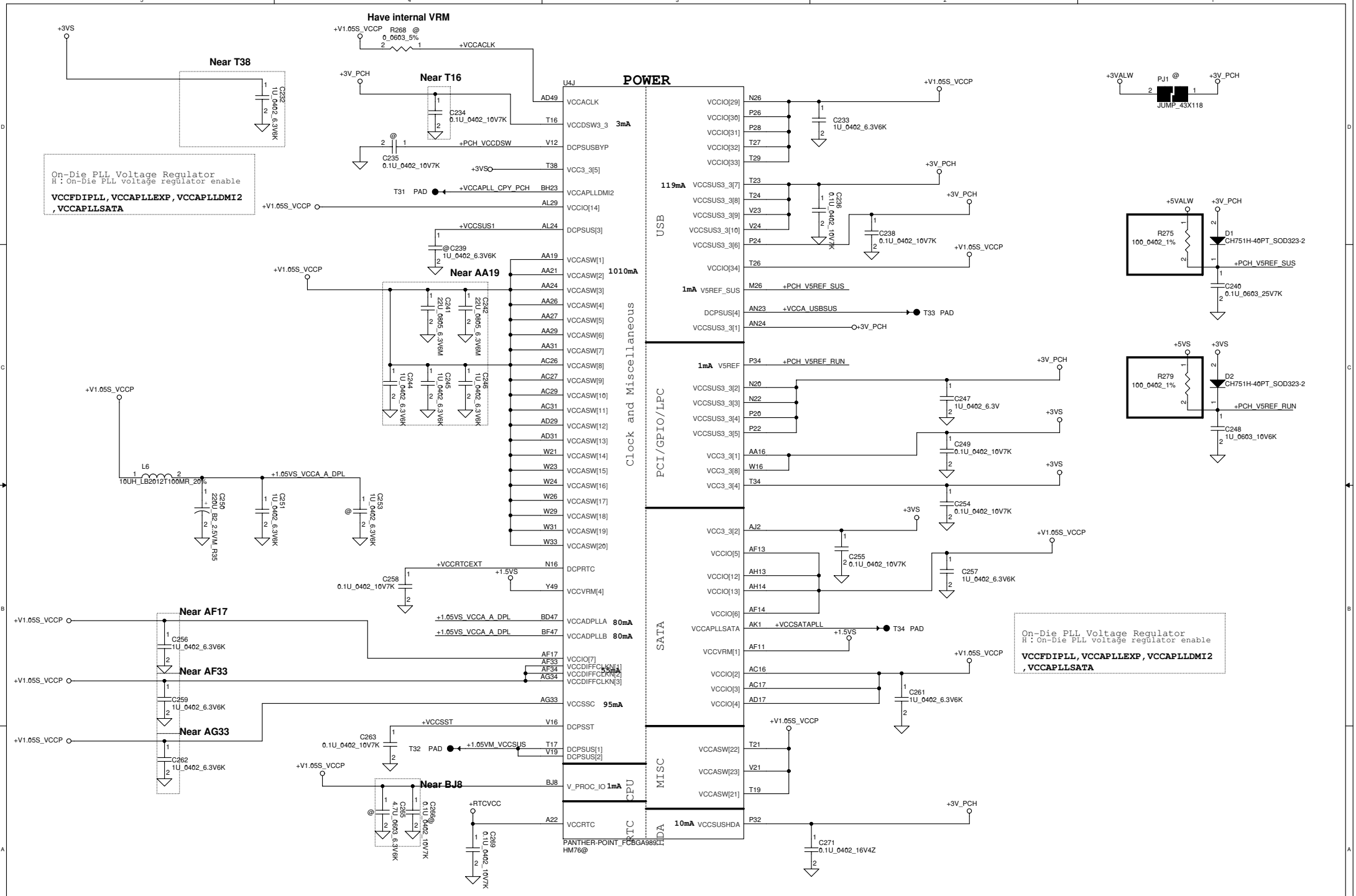
Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 20 of 52



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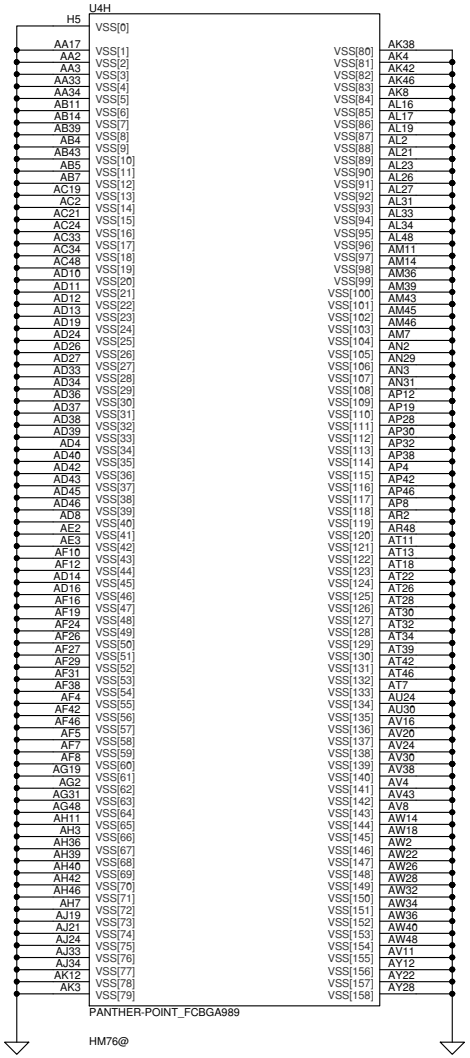
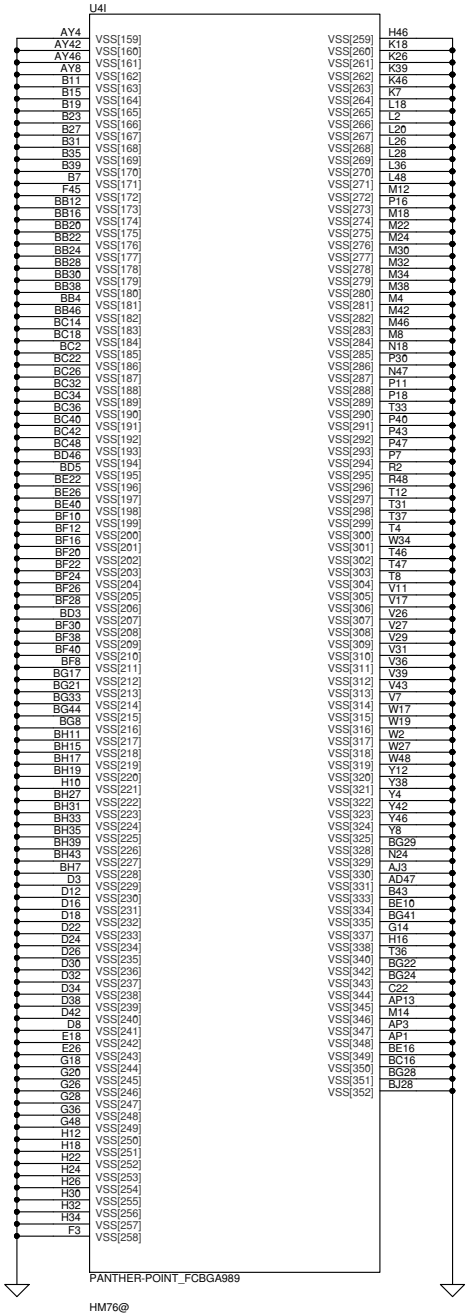
Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 21 of 52





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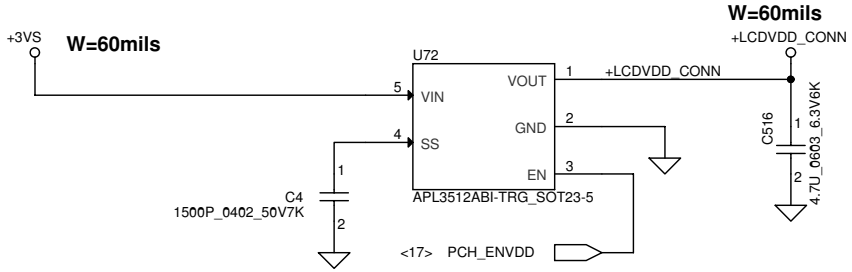
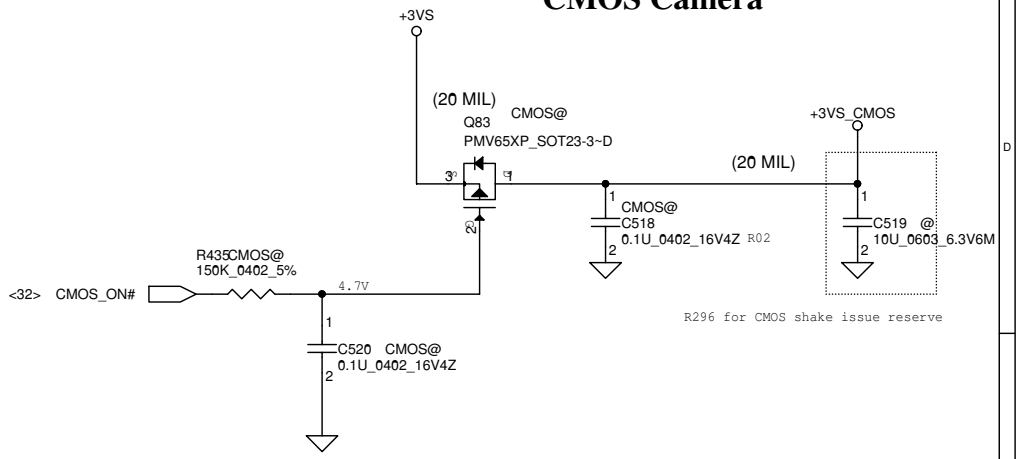
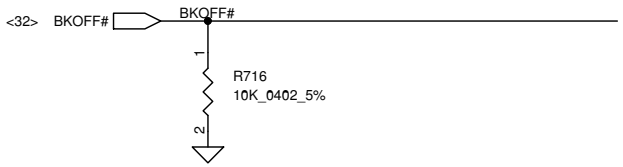
LCD POWER CIRCUIT

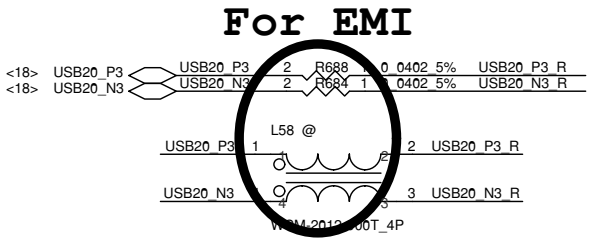


CMOS Camera

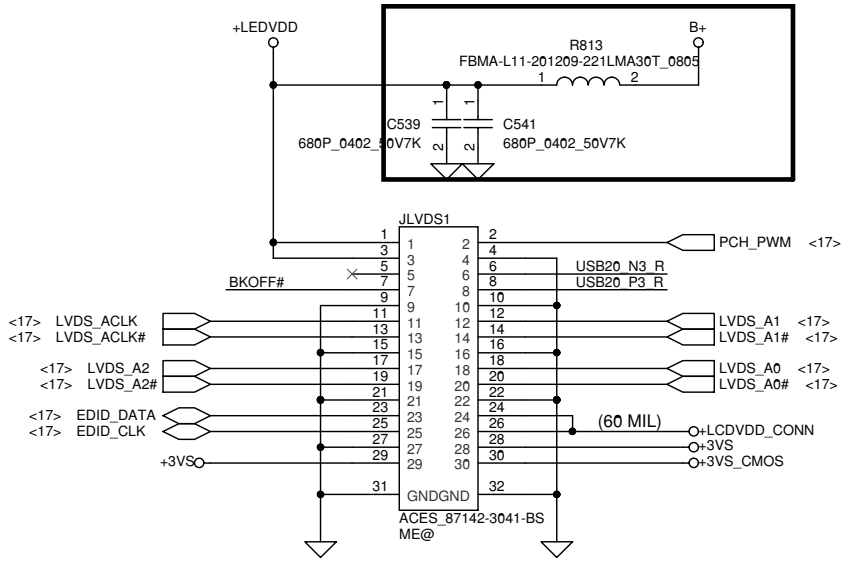


VGA LCD/PANEL BD. Conn.





12/12 Mount C539/C541 of 680pF,Chanage R813 to 220 ohm bead.(For EMI request)



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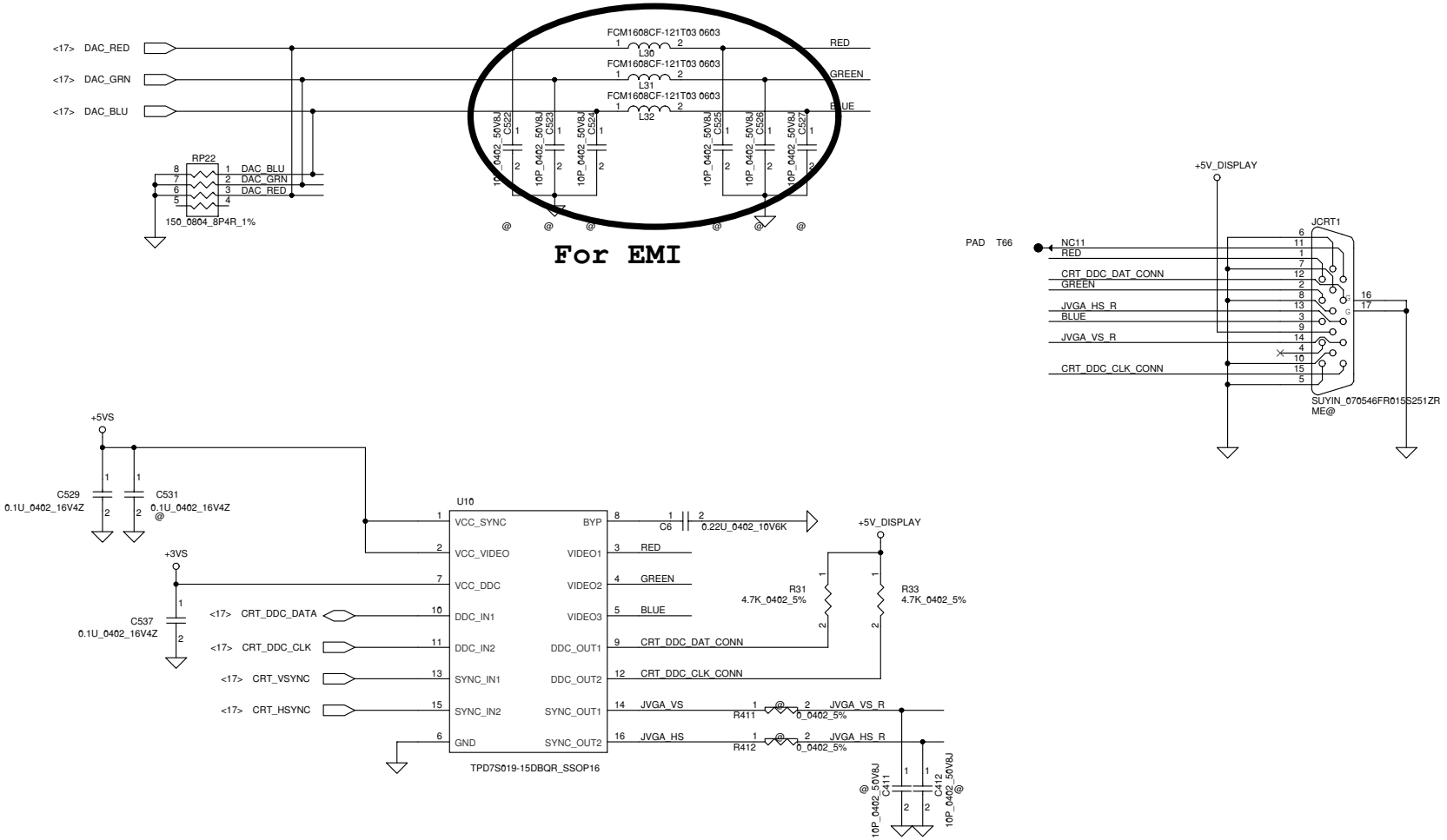
Title: **SCHEMATIC M/B LA-9902**

Size: Custom | Document Number: **4019N1** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 23 of 52



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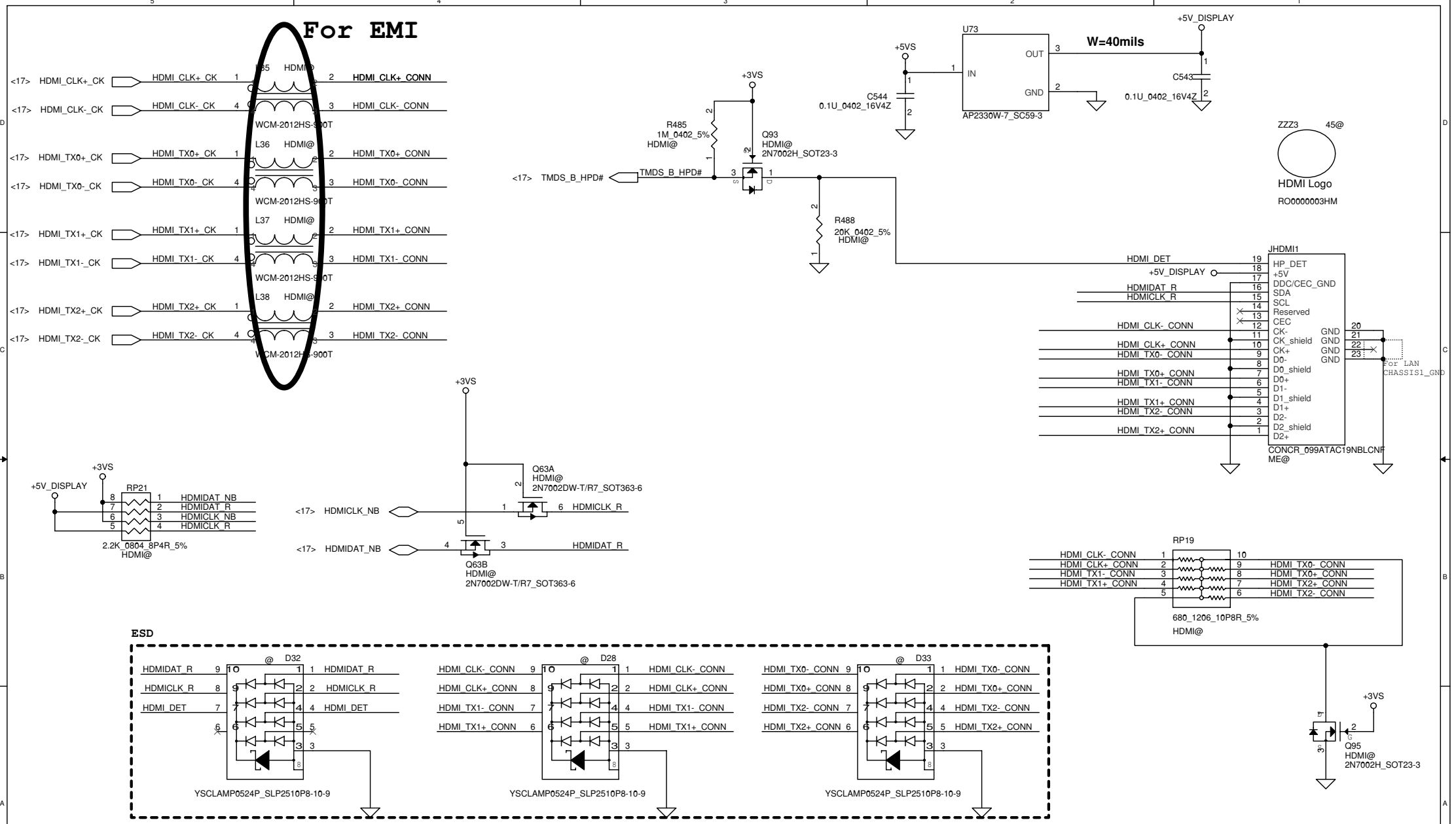
Size	Document Number	Rev
Custom	4019N1	B

Date: Wednesday, May 08, 2013 Sheet 24 of 52



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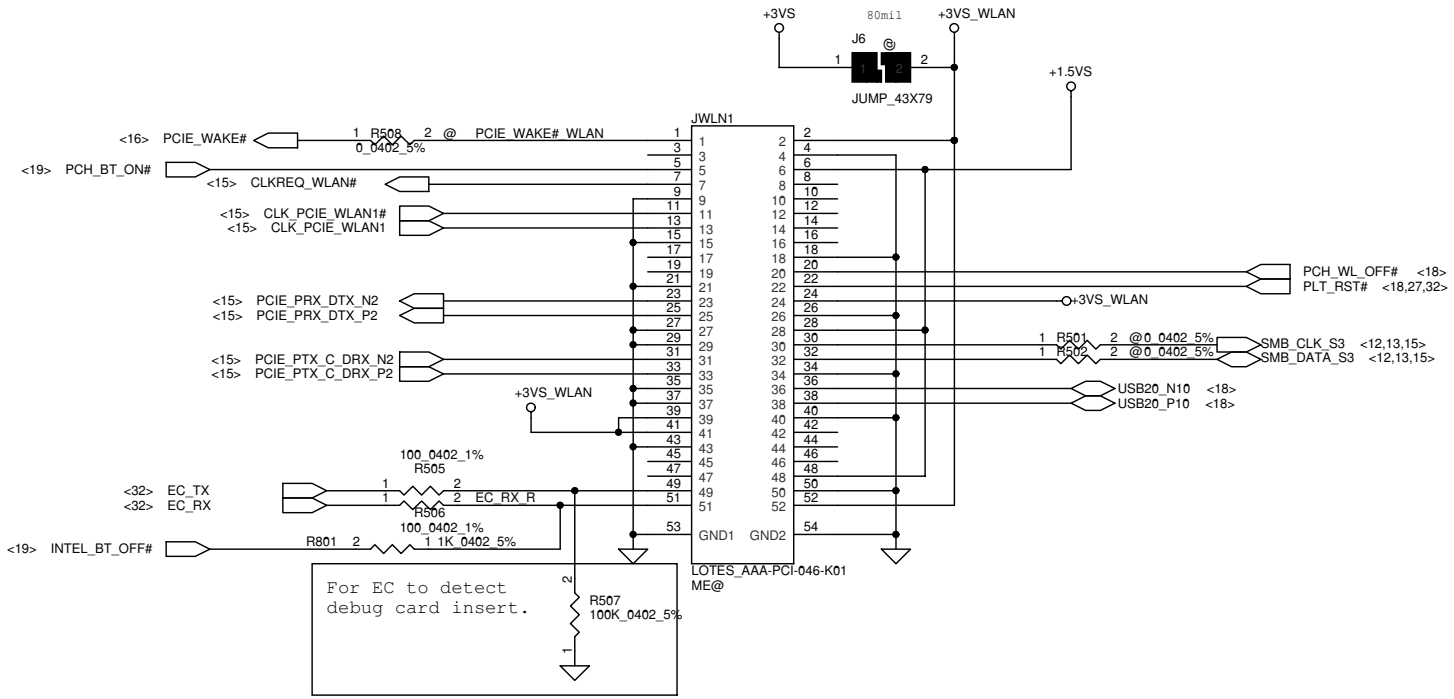
Title: **SCHEMATIC M/B LA-9902**

Size: B | Document Number: **4019N1** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 25 of 52

Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

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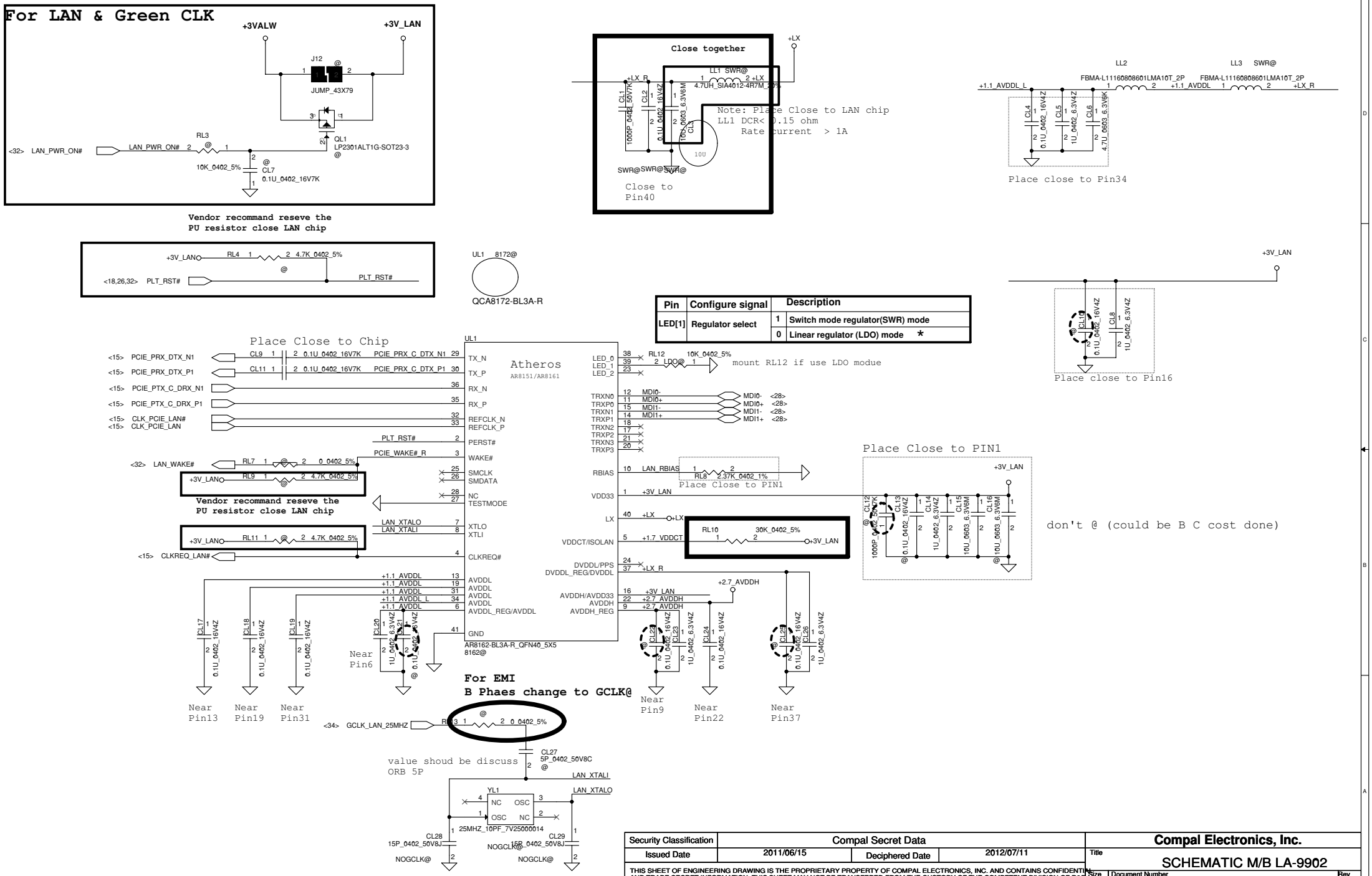
				Size: Document Number: 4019N1 — Rev: B
				Date: Wednesday, May 08, 2013 — Sheet 26 of 52



Pin	Configure signal	Description	
LED[1]	Regulator select	1	Switch mode regulator(SWR) mode
		0	Linear regulator (LDO) mode *

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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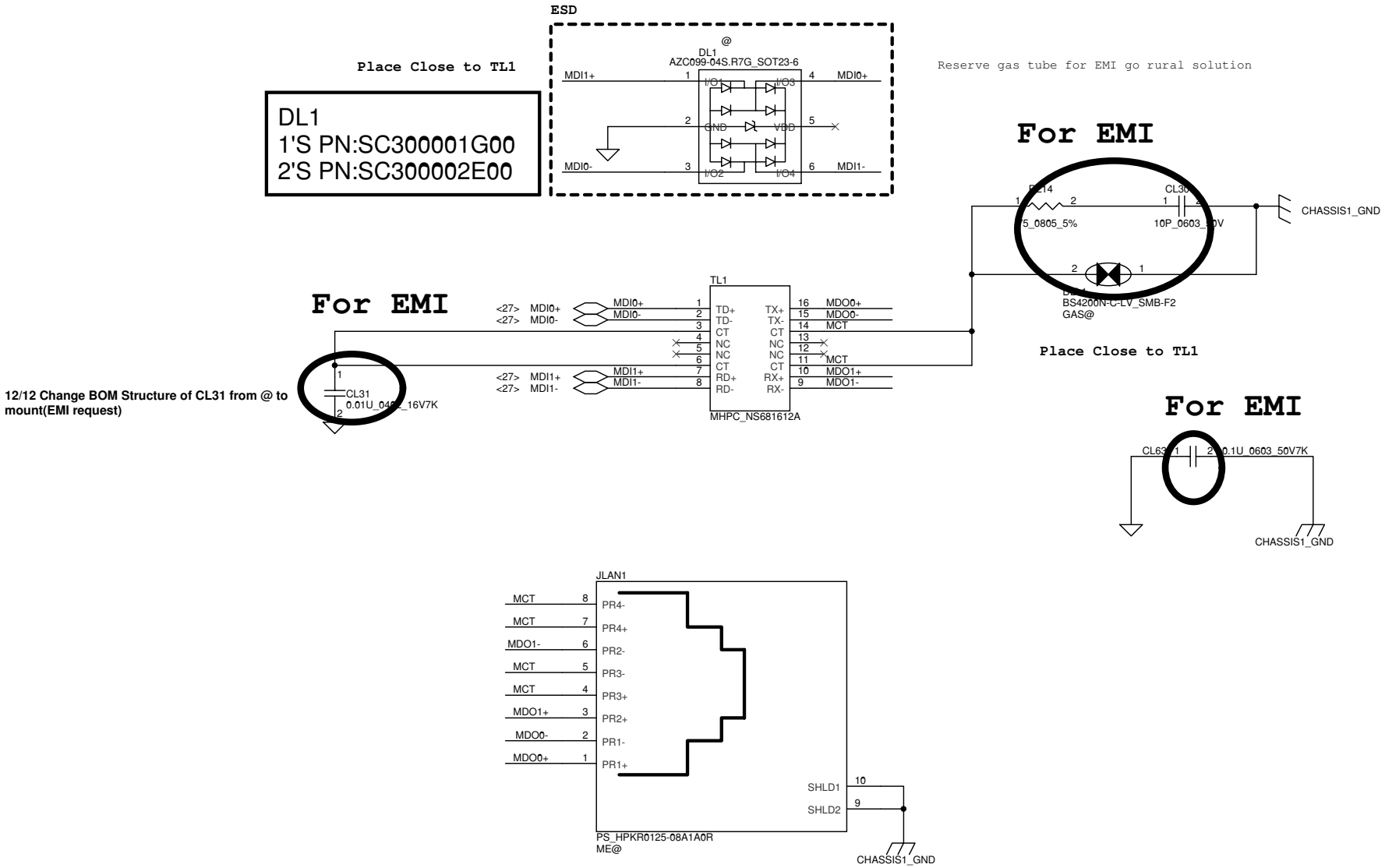

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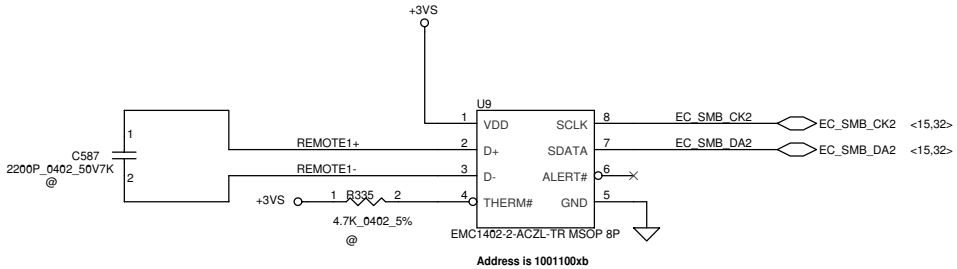
				Size: B; Document Number: 4019N1; Rev: B
				Date: Wednesday, May 08, 2013; Sheet 28 of 52

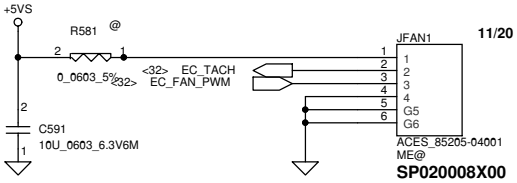
2 Channel

SMSC thermal sensor placed near VRAM

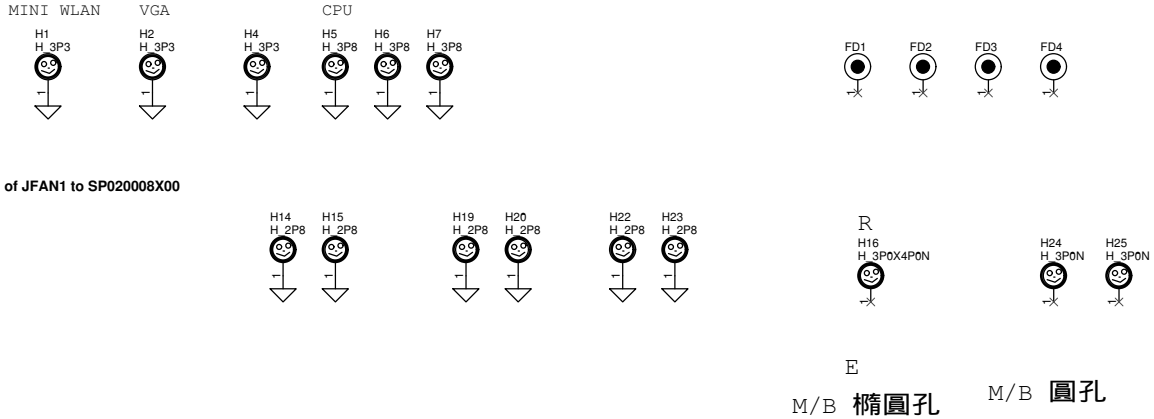


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



11/20 Change symbol of JFAN1 to SP020008X00



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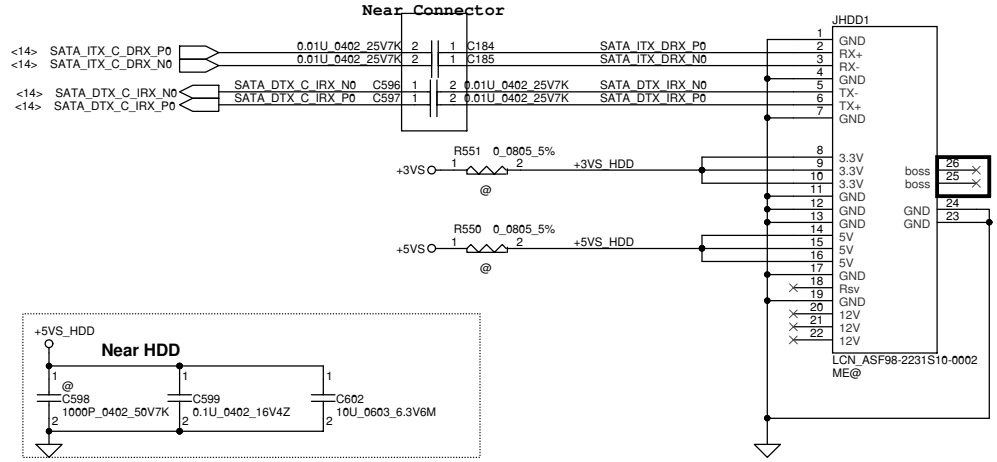
Title: **SCHEMATIC M/B LA-9902**

Size: Custom | Document Number: **4019N1** | Rev: B

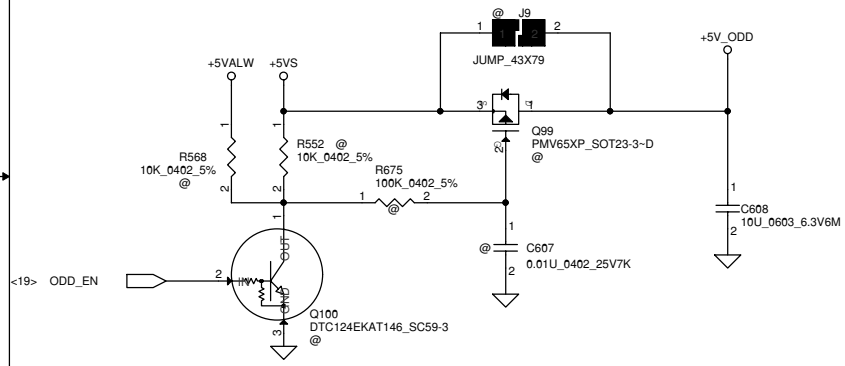
Date: Wednesday, May 08, 2013 | Sheet 29 of 52

SATA HDD Conn.



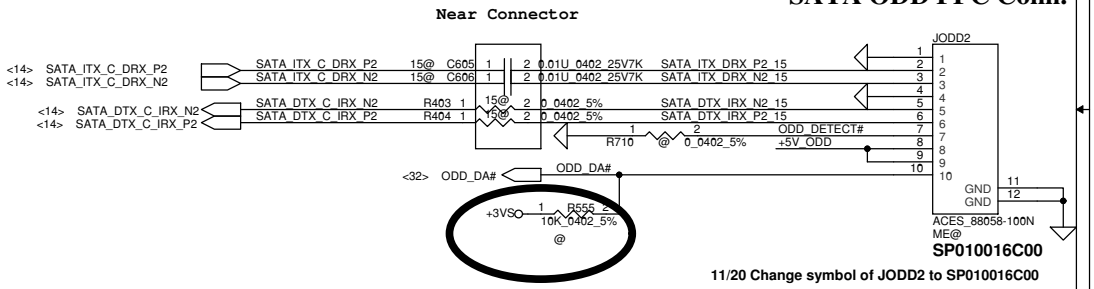
1/16 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_ASF98-2231S10-0002_22P (DC010005W00 toDC010009C00)

ODD Power Control



FOR 15"

SATA ODD FFC Conn.

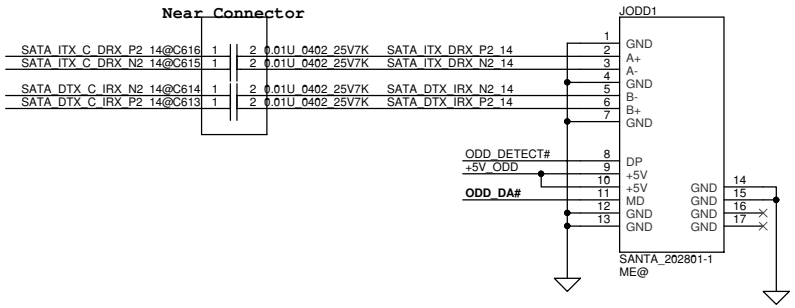


11/20 Change symbol of JODD2 to SP010016C00

Co-lay

FOR 14"

SATA ODD Conn.



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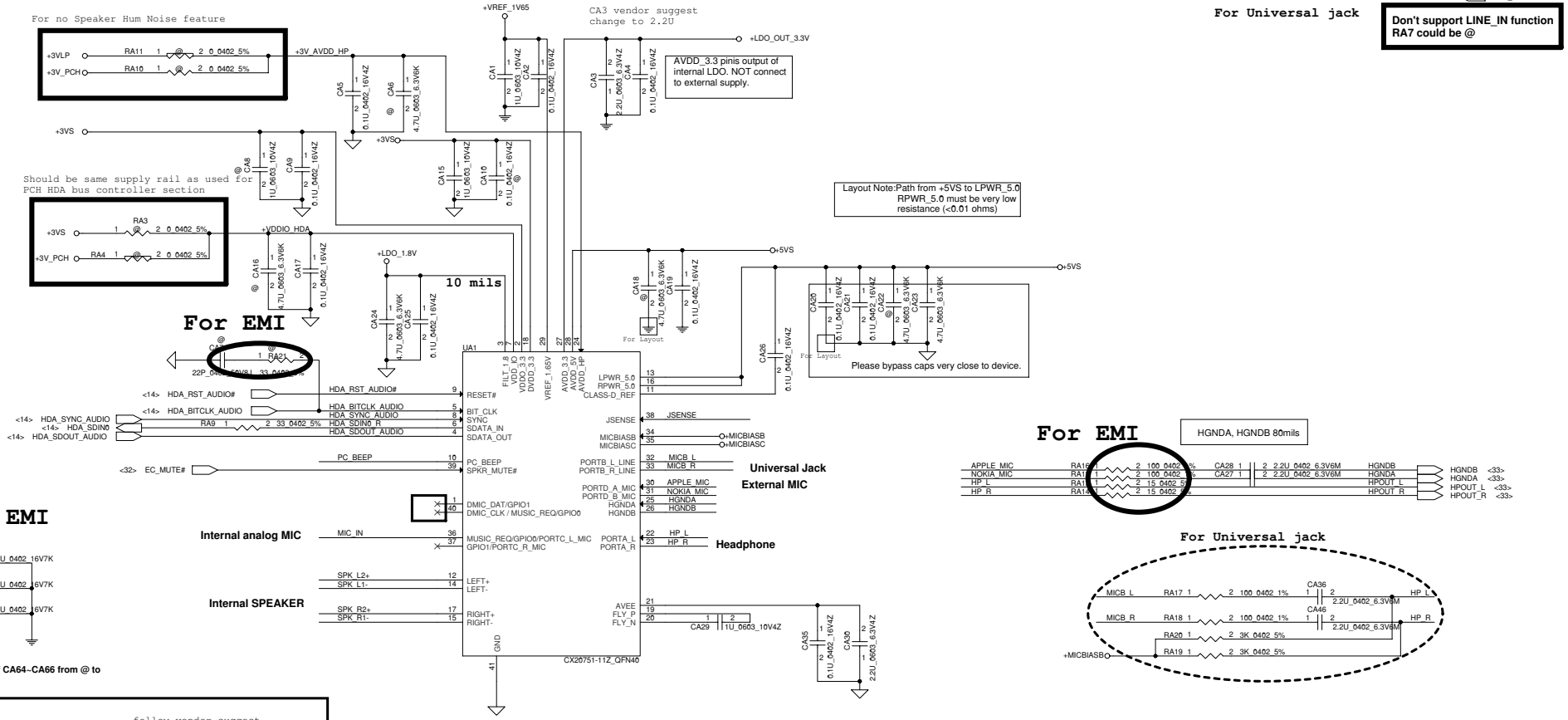
				Date: Wednesday, May 08, 2013; Sheet 30 of 52

CX20757
High Definition Audio Codec SoC With Integrated Class-D Stereo Amplifier.
An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



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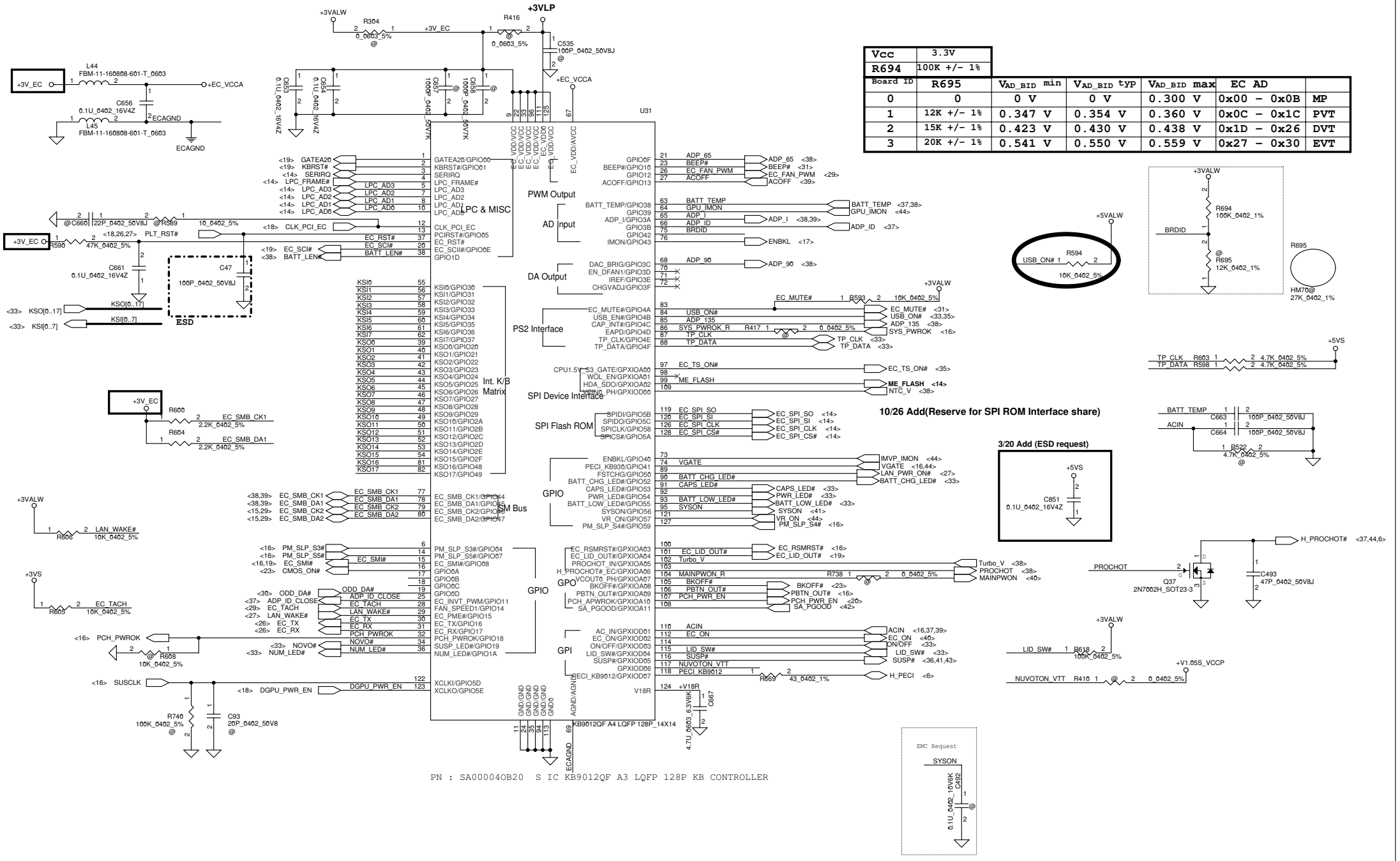
Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 31 of 52



Vcc	3.3V					
R694	100K +/- 1%					
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT

PN : SA00004OB20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER

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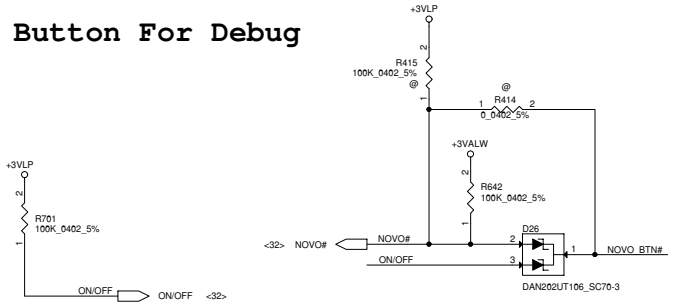
Title: **SCHEMATIC M/B LA-9902**

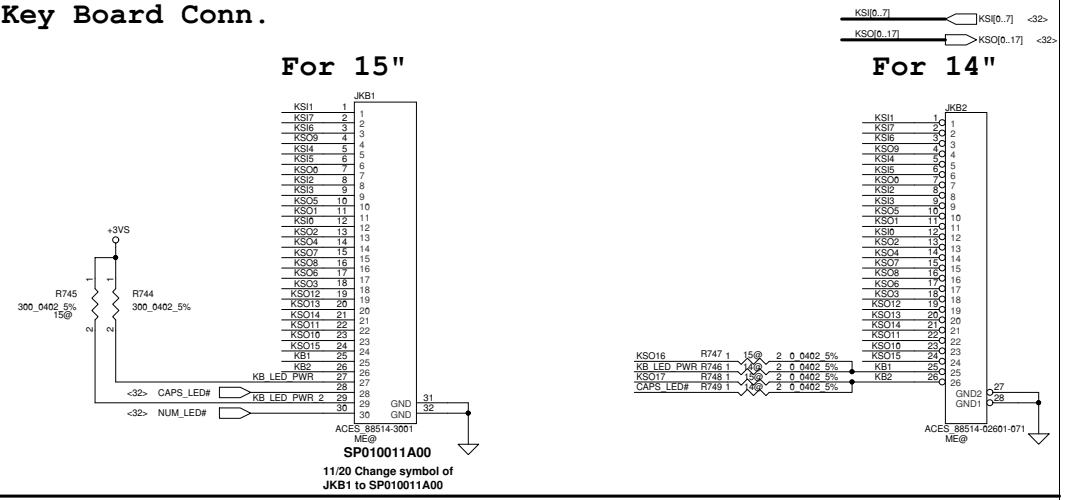
Size: Custom | Document Number: **4019N1** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 32 of 52

PWR Button For Debug



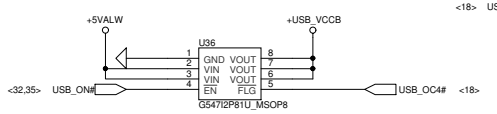
Key Board Conn.



11/20 Change symbol of JKB1 to SP010011A00

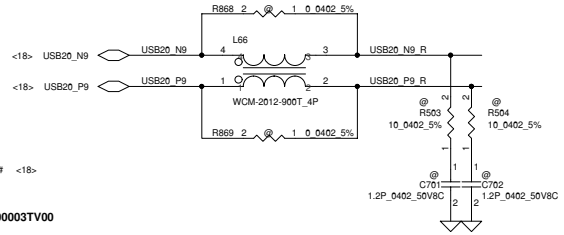
IO/B Conn.

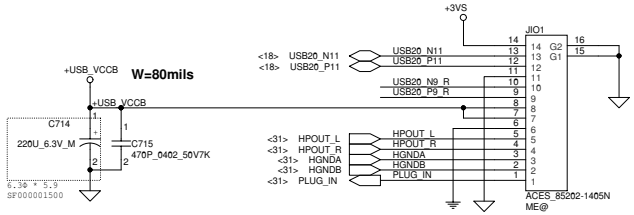
Ext. USB2.0



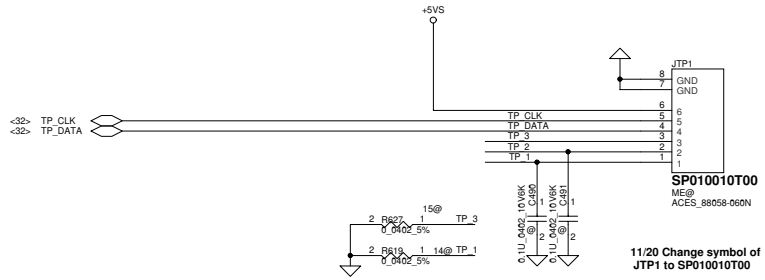
11/30 Change U36 symbol & PN from SA00003XM00 to SA00003TV00

For EMI



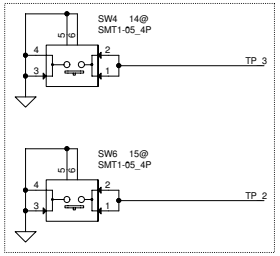


TP Switch & TP Conn.

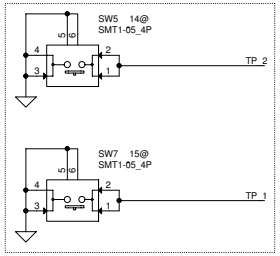


11/20 Change symbol of JTP1 to SP010010T00

L



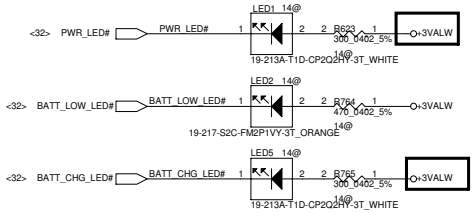
R



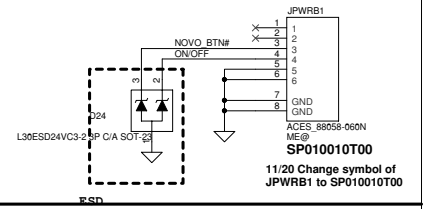
15"	
1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

14"	
1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

LED

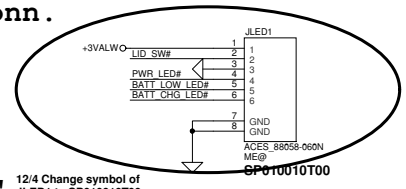


PWR/B Conn.



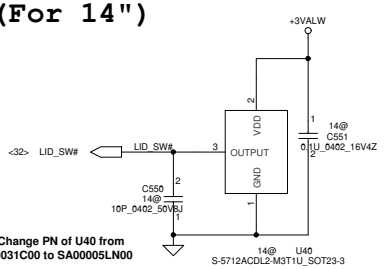
11/20 Change symbol of JPWRB1 to SP010010T00

LED/B Conn.



For 15" 12/4 Change symbol of JLED1 to SP010010T00

Lid SW(For 14")



11/30 Change PN of U40 from SA000031C00 to SA00005LN00

Security Classification	Compal Secret Data		
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Title: SCHEMATIC M/B LA-9902

Size: C | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 33 of 52

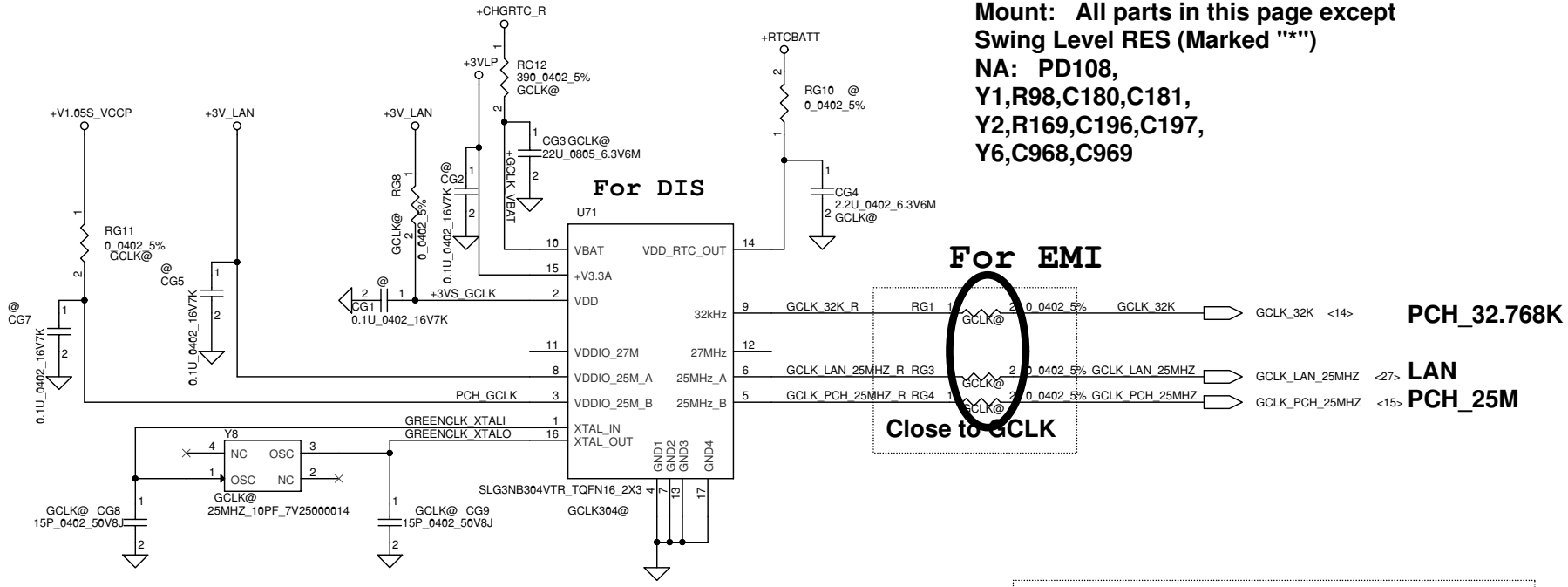
For UMA

U71 GCLK244@

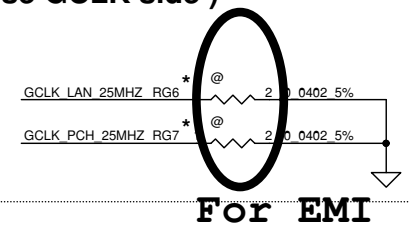
SLG3NB244VTR_TQFN16_2X3

Every power trace need:
W=20mils

For GreenCLK generate CLK:
Mount: All parts in this page except Swing Level RES (Marked "*")
NA: PD108,
Y1,R98,C180,C181,
Y2,R169,C196,C197,
Y6,C968,C969



Reserved for Swing Level adjustment
(Close GCLK side)



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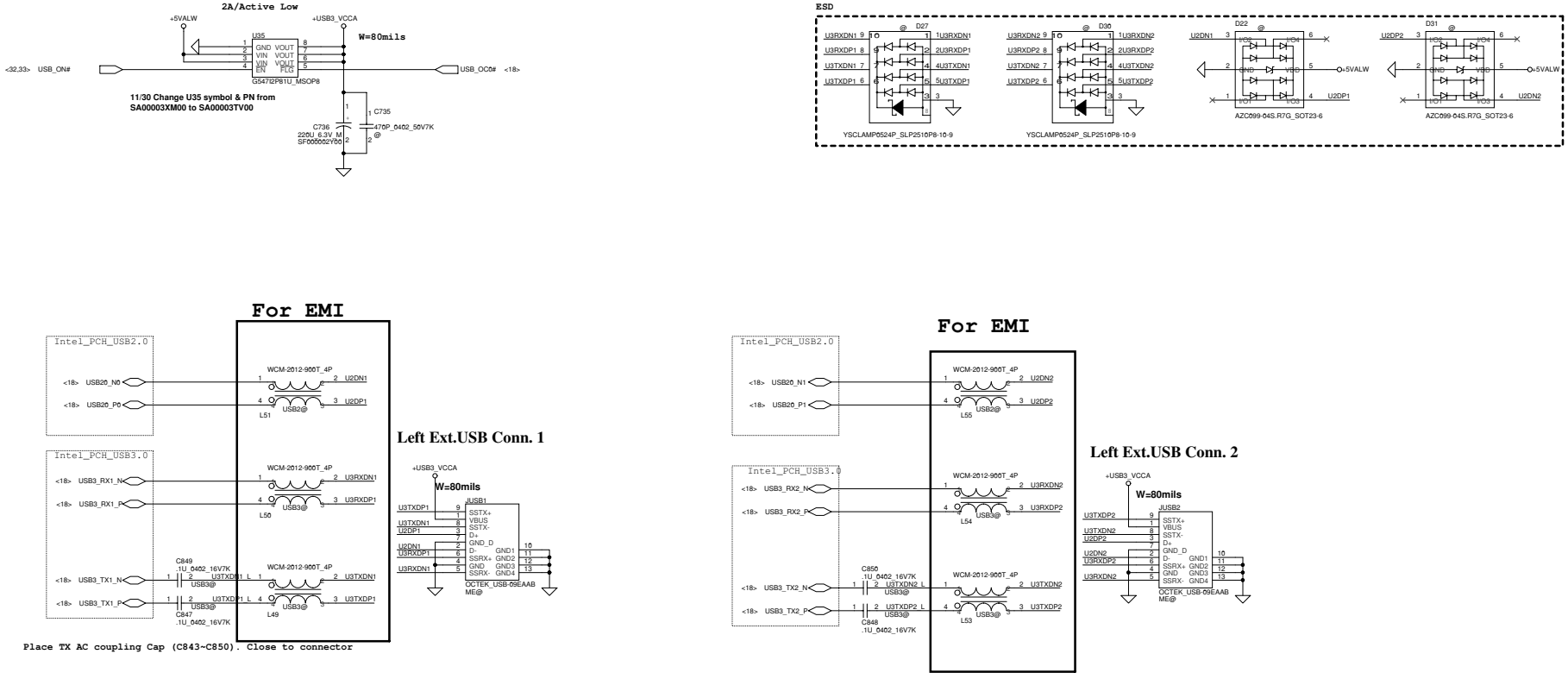
				Size: B; Document Number: 4019N1; Rev: B
				Date: Wednesday, May 08, 2013; Sheet 34 of 52

Touch Screen

USB3.0



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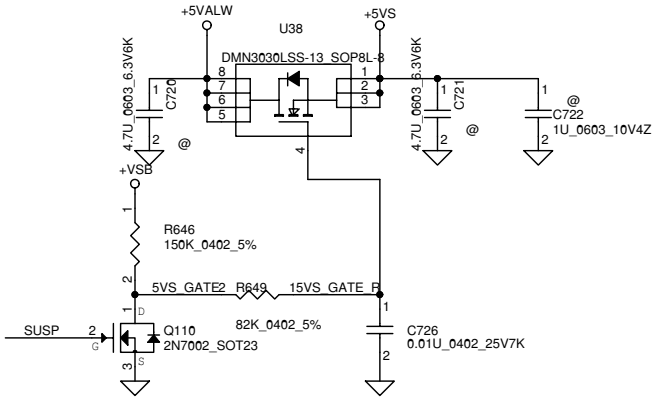
Title: ***SCHEMATIC M/B LA-9902***

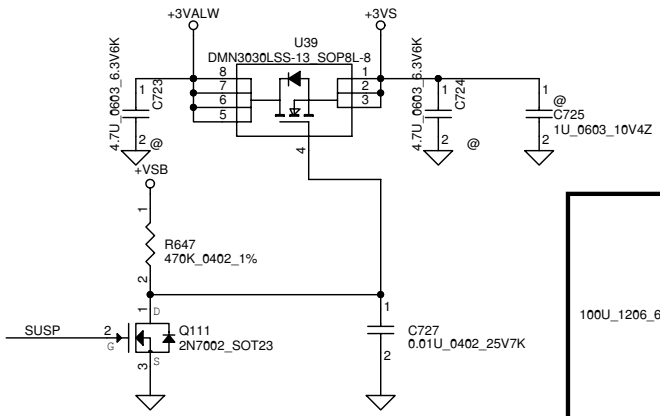
Size: Custom | Document Number: 4019N1 | Rev: B

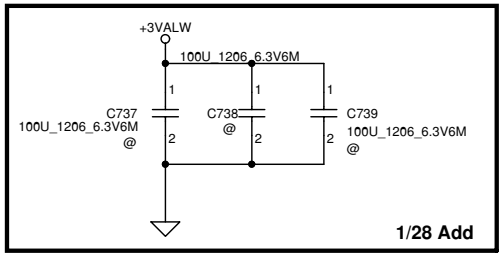
Date: Wednesday, May 08, 2013 | Sheet 35 of 52

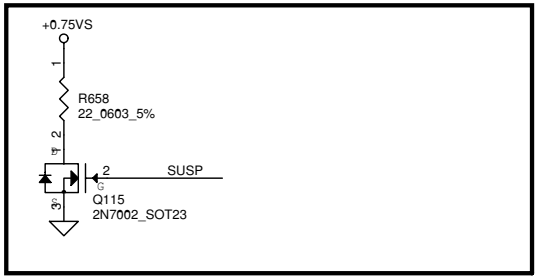
+5VALW to +5VS



+3VALW to +3VS

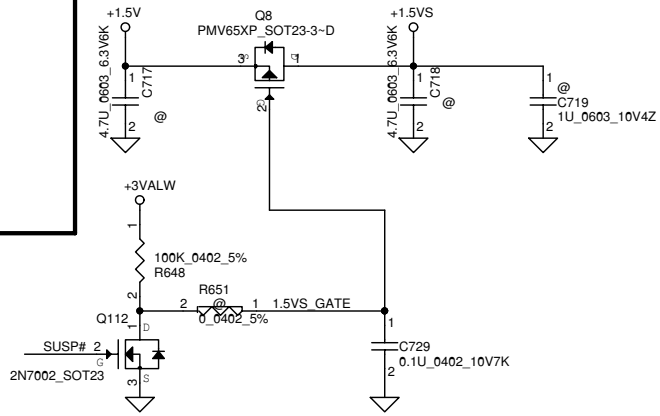


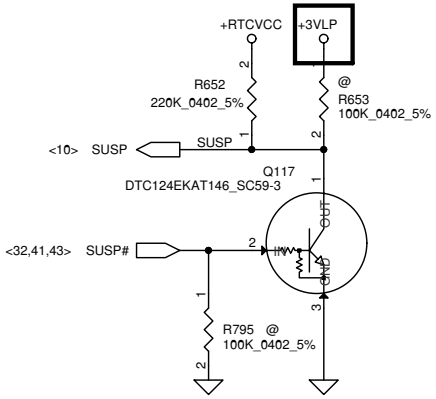




For Intel S3 Power Reduction.

+1.5V to +1.5VS





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Compal Electronics, Inc.

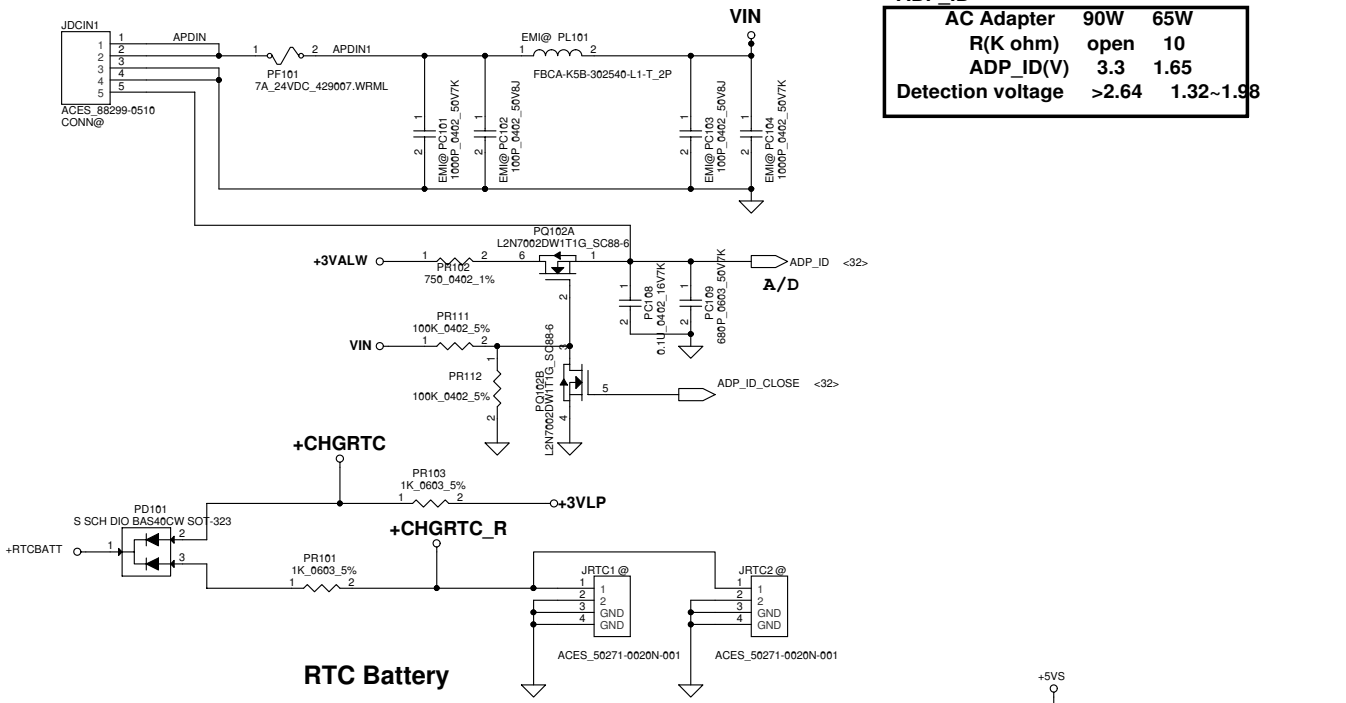
Title: SCHEMATIC M/B LA-9902

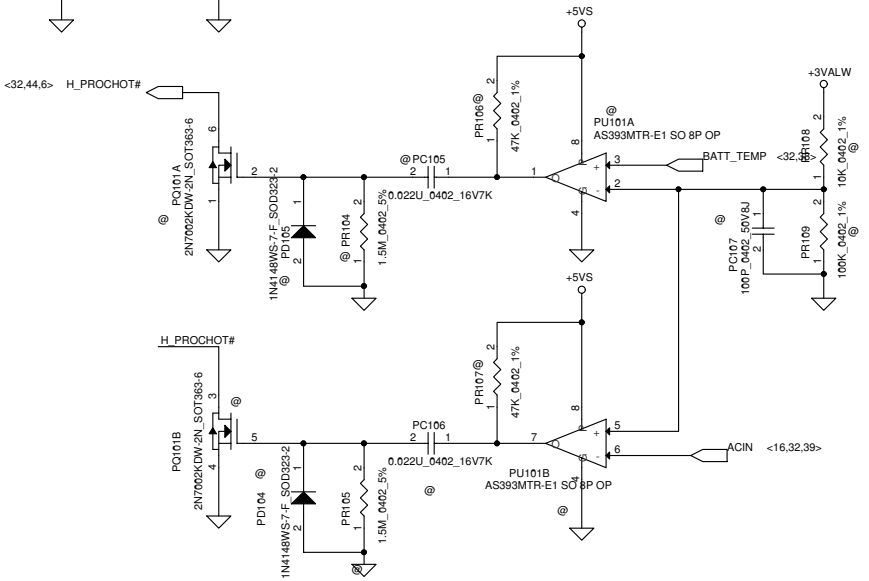
Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 36 of 52

ADP_ID

AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98





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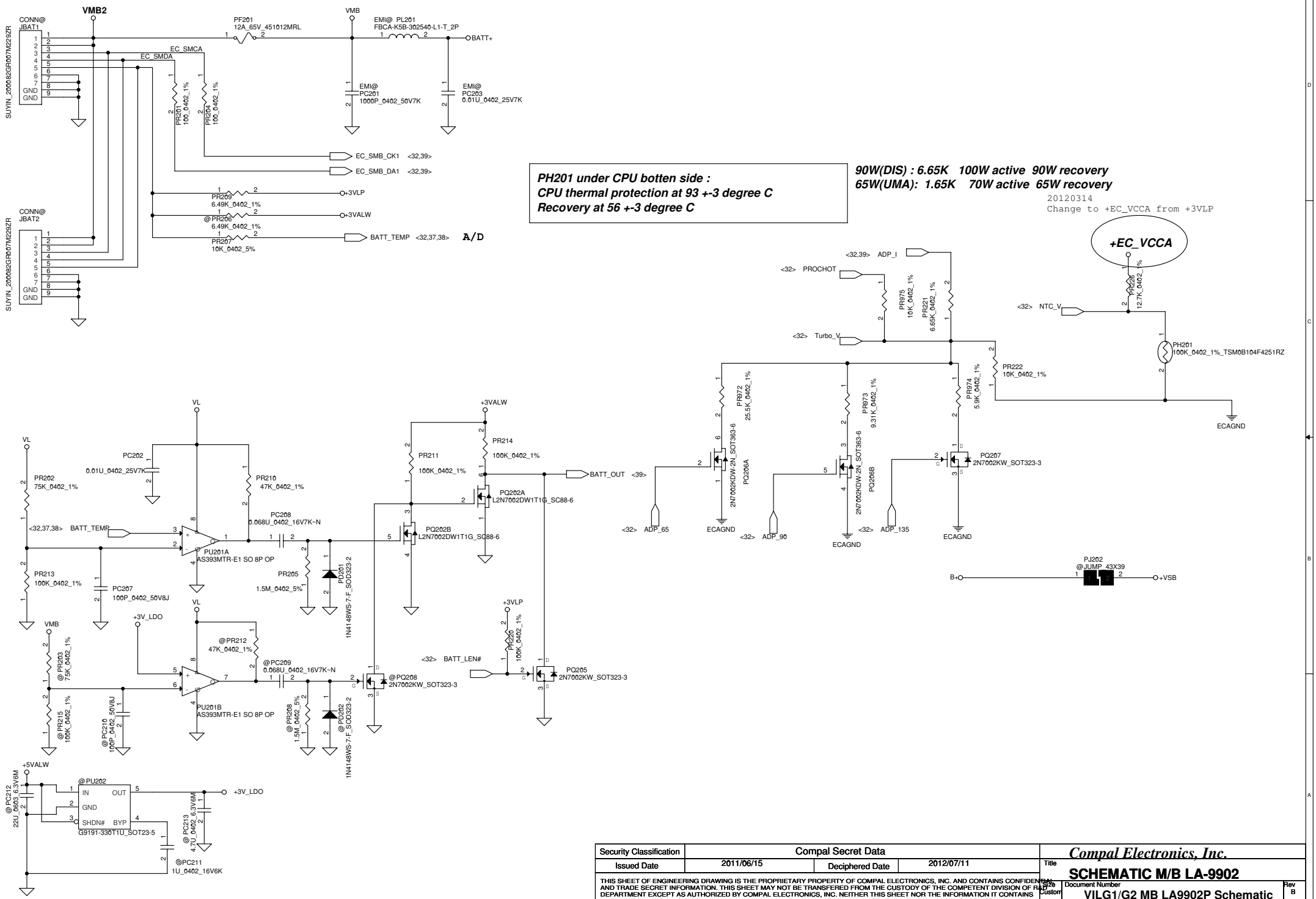
Title: **SCHEMATIC M/B LA-9902**

Size: Custom | Document Number: **VILG1/G2 MB LA9902P Schematic** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 37 of 52



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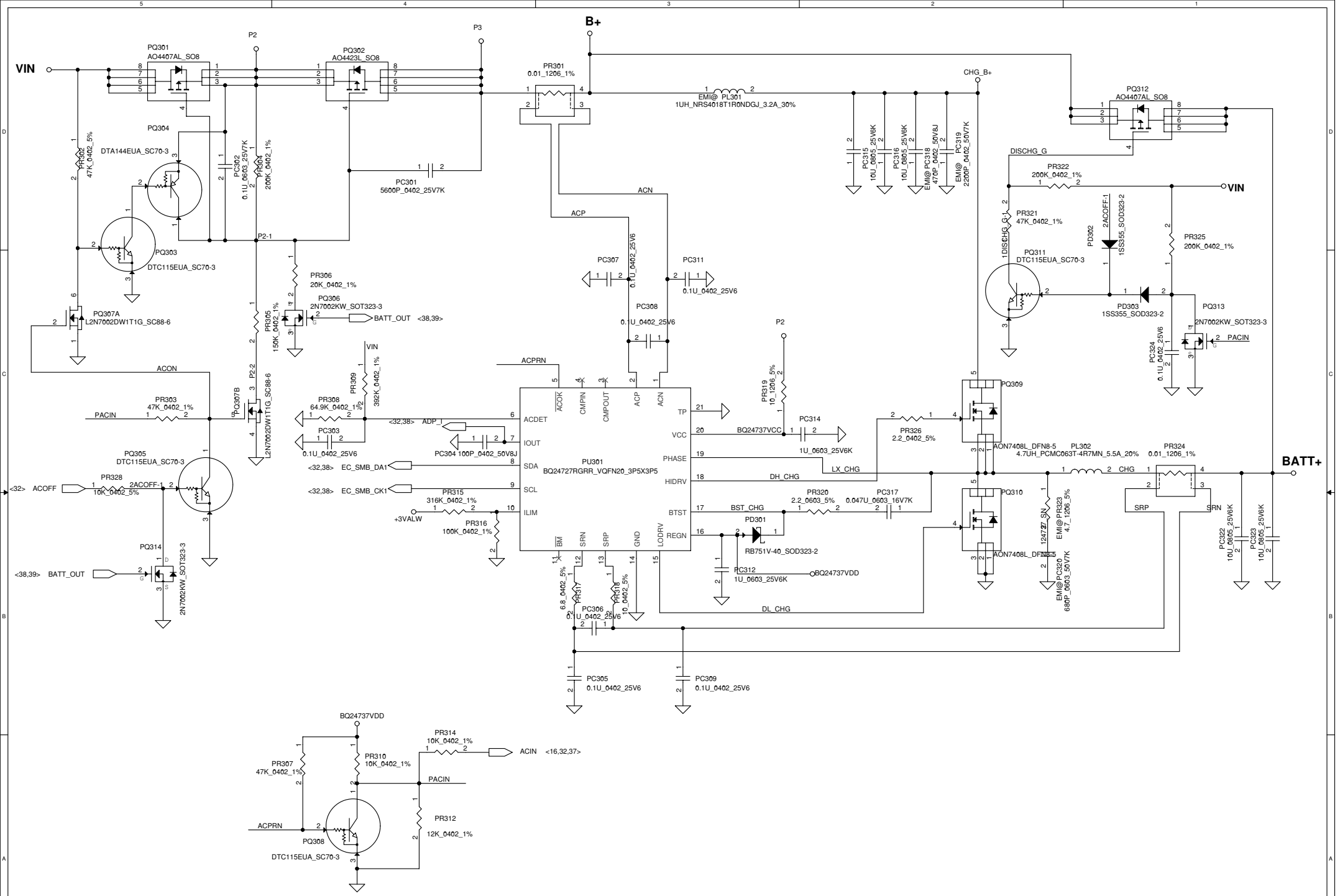
Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 38 of 52



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Compal Electronics, Inc.

Title: **CHARGER**

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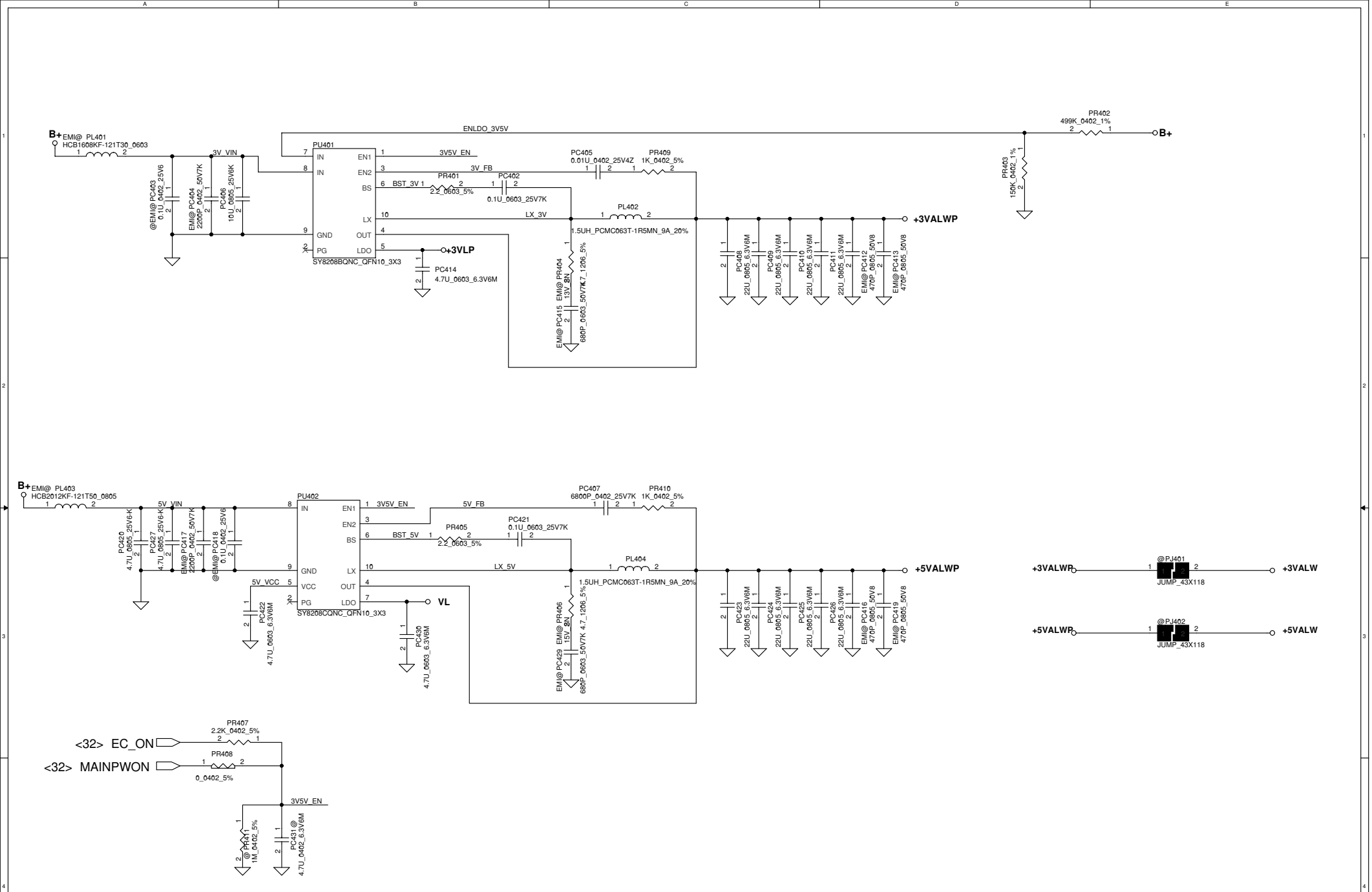
Date: Wednesday, May 08, 2013 | Sheet 39 of 52



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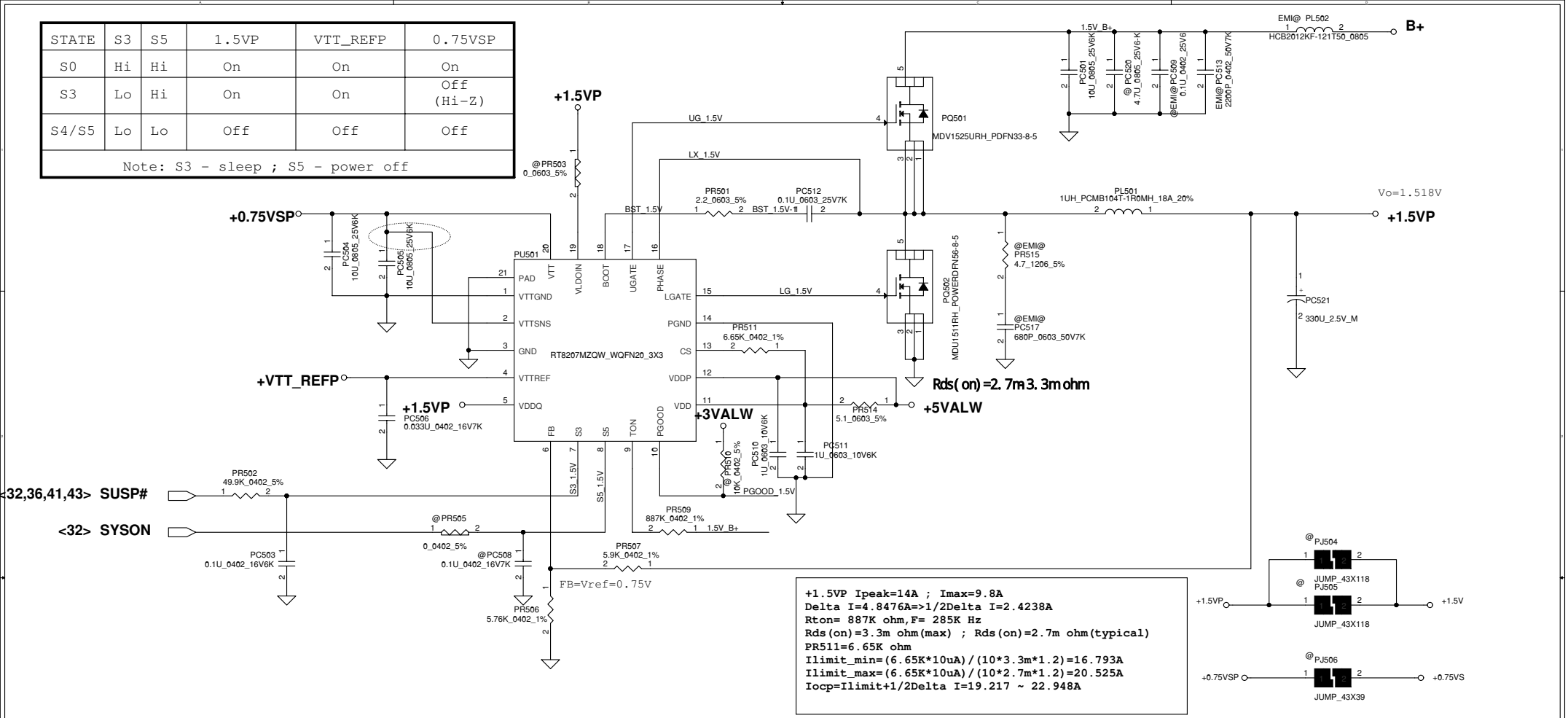
Title: **SCHEMATIC M/B LA-9902**

Size: Custom | Document Number: **VILG1/G2 MB LA9902P Schematic** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 40 of 52

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



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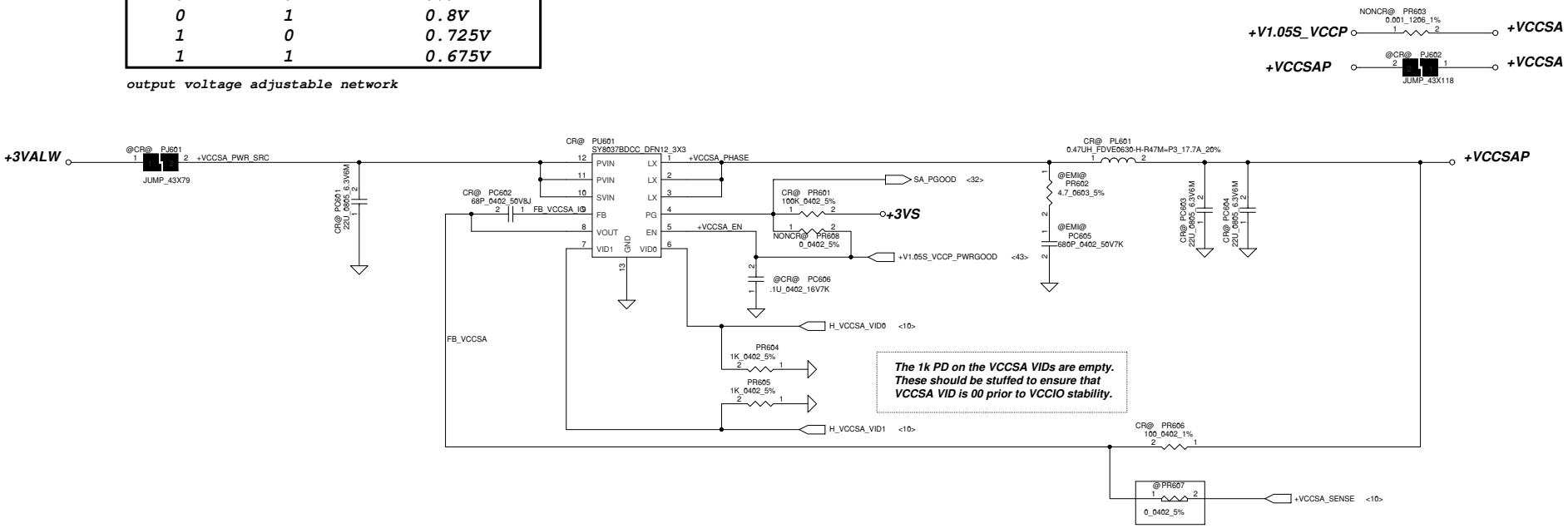
Title: **SCHEMATIC M/B LA-9902**

Size: A3 | Custom | Document Number: **VILG1/G2 MB LA9902P Schematic** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 41 of 52

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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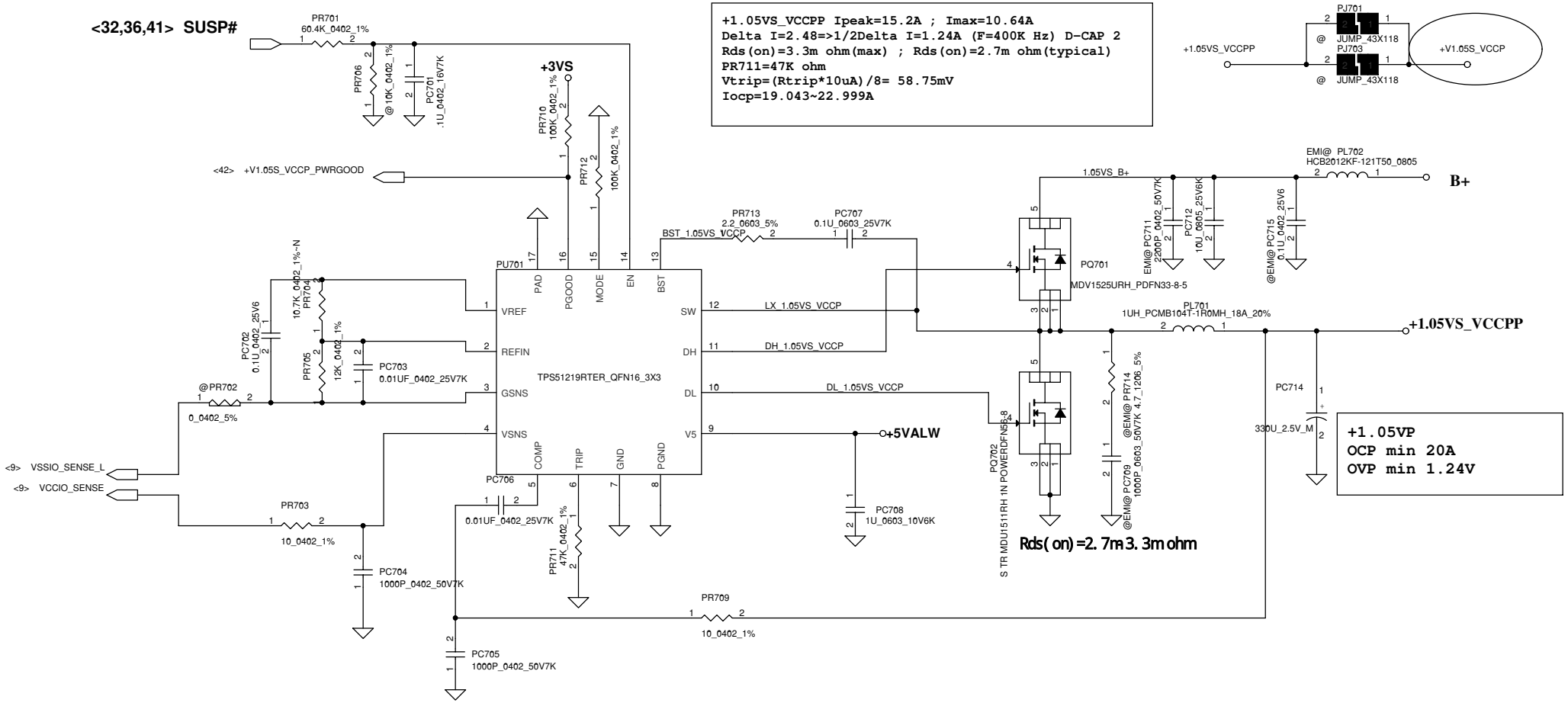
Title: SCHEMATIC M/B LA-9902

Size: C | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 42 of 52



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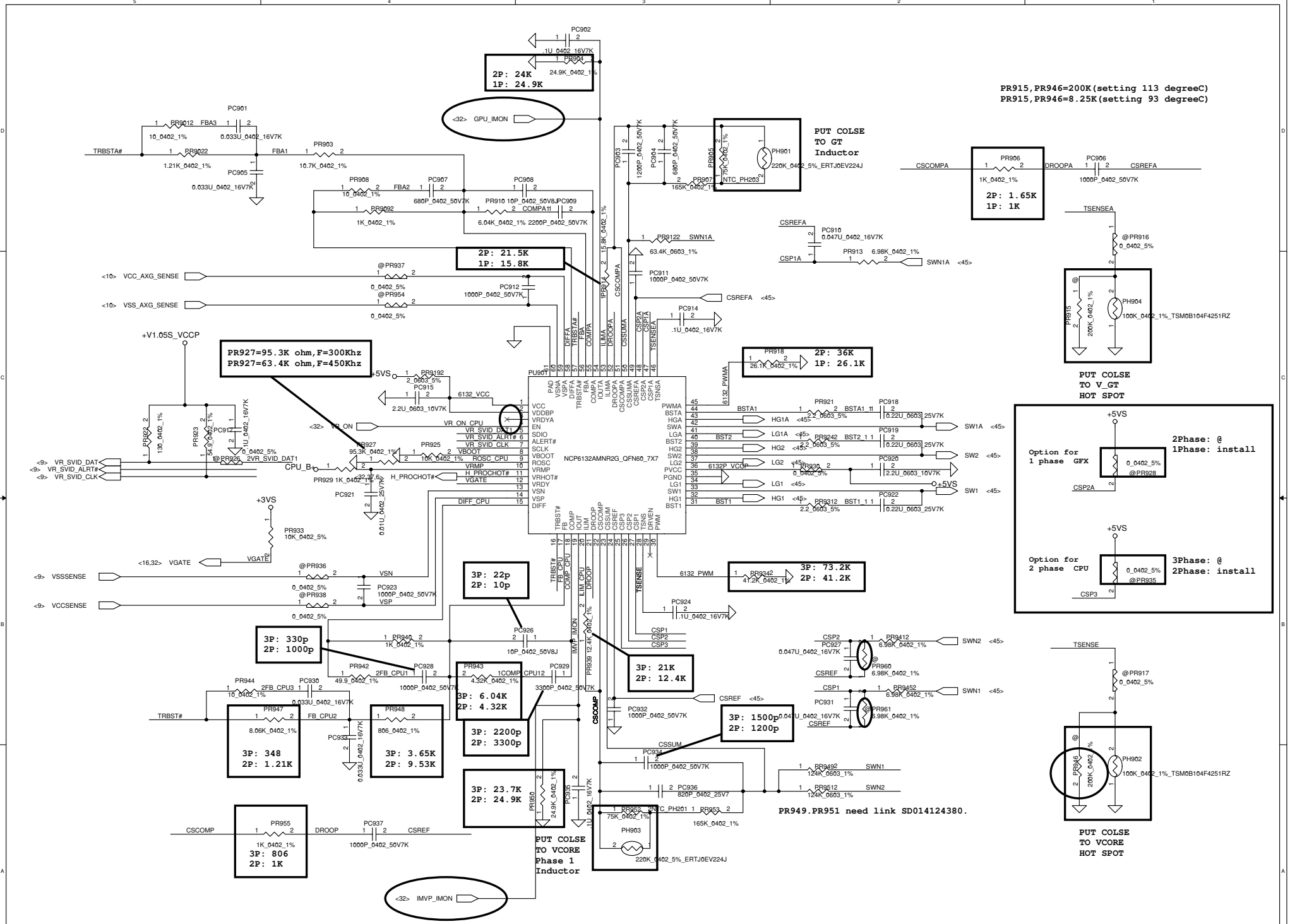
Title: **SCHEMATIC M/B LA-9902**

Size: Custom | Document Number: **VILG1/G2 MB LA9902P Schematic** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 43 of 52



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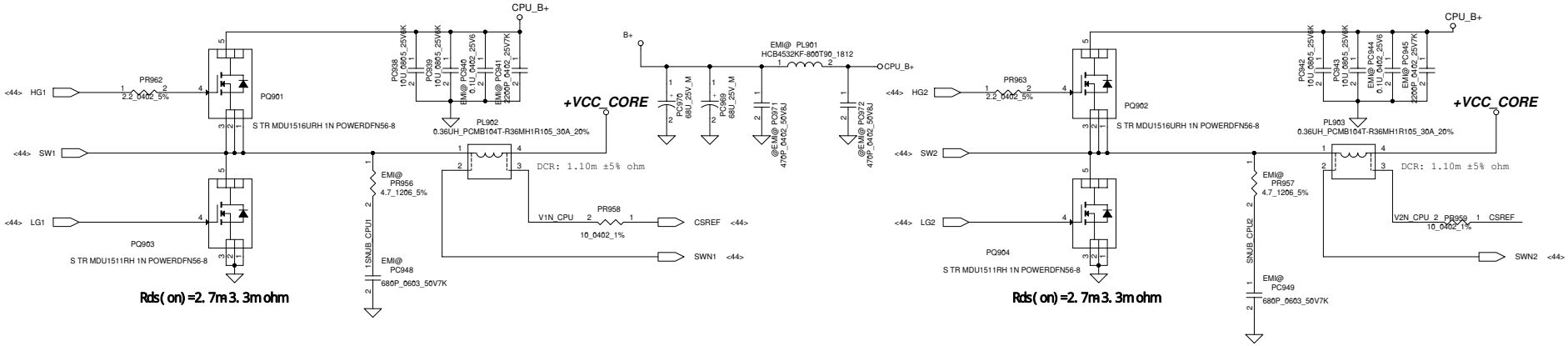
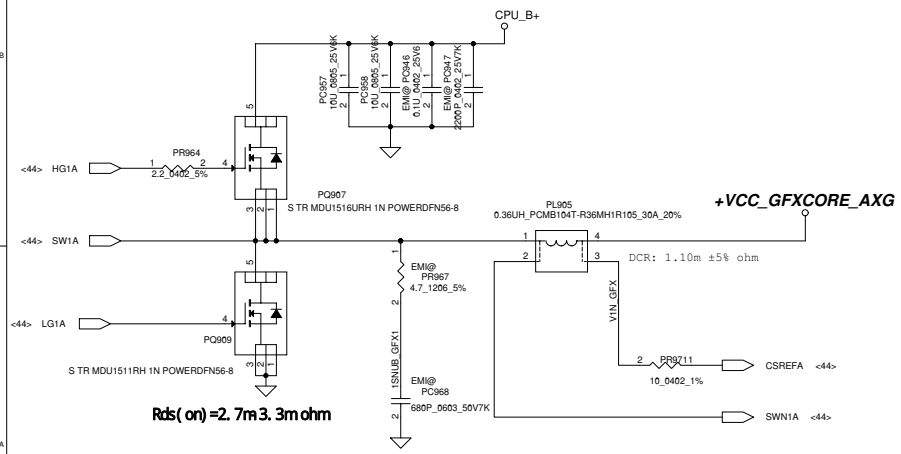
Title: ***SCHEMATIC M/B LA-9902***

Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 44 of 52



QC 45W CPU	DC 35W CPU
VID1=0.9V	VID1=1.05V
IccMax=94A	IccMax=53A
Icc_Dyn=66A	Icc_Dyn=43A
Icc_TDC=52A	Icc_TDC=36A
R_LL=1.9m ohm	R_LL=1.9m ohm
OCP~110A	OCP~65A



QC 45W GT2	DC 35W GT2
VID1=1.23V	VID1=1.23V
IccMax=46A	IccMax=33A
Icc_Dyn=37A	Icc_Dyn=20.2A
Icc_TDC=38A	Icc_TDC=21.5A
R_LL=3.9m ohm	R_LL=3.9m ohm
OCP~55A	OCP~40A

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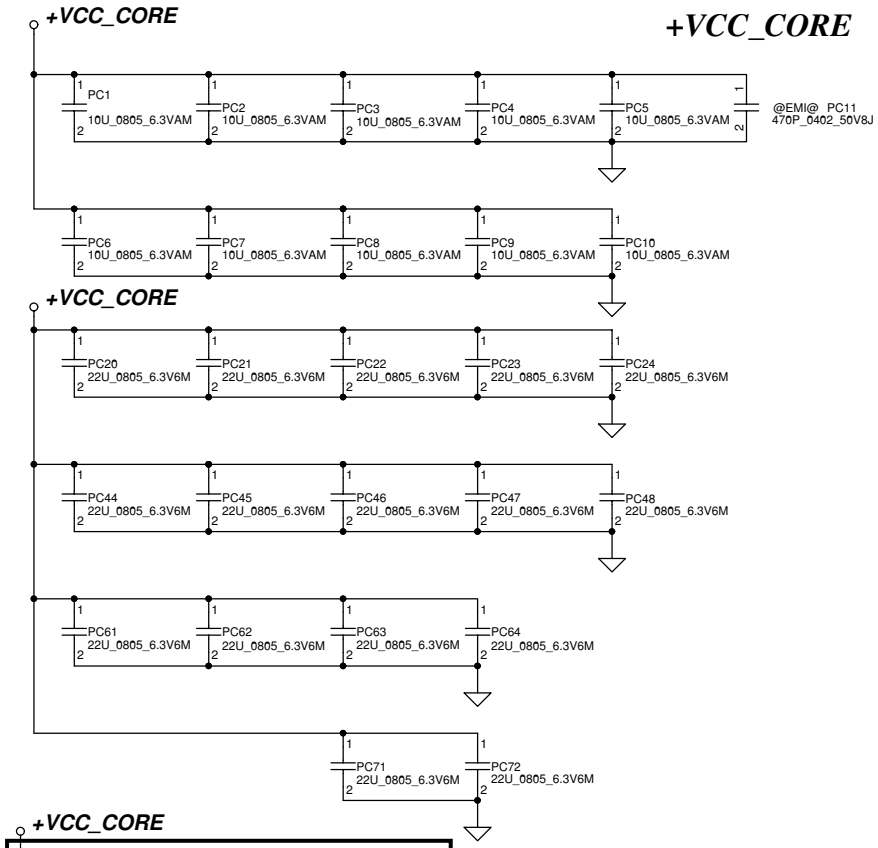
Issued Date	2011/06/15	Deciphered Date	2012/07/11

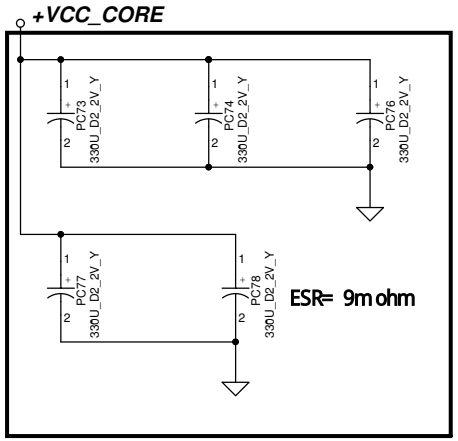
Compal Electronics, Inc.

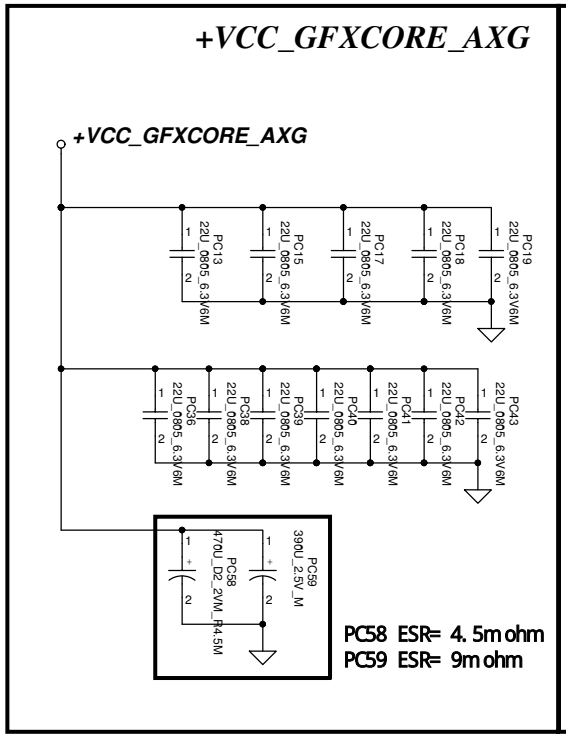
Title: SCHEMATIC M/B LA-9902

Size: C | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 45 of 52

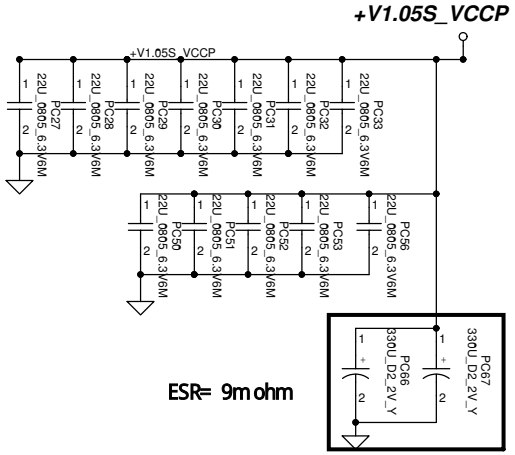






Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



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Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 46 of 52

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Design Change of IC Package.	40	Change PU401 to SA000061M00(S IC SY8208BQNC QFN 10P PWM)	2012/11/22	DVT
2	Design Change of IC Package.	40	Change PU402 to SA000061N00(S IC SY8208CQNC QFN 10P PWM)	2012/11/22	DVT
3	Add ADP_ID Circuit.	37	Add PQ102 to SB00000EO10(S TR 2N7002KDW 2N SOT-363-6 PANJIT) Add PR111.PR112 to SD028100380(S RES 1/16W 100K +-5% 0402)	2012/12/03	DVT
4	Factory lack of material.	41	Change PC521 to SF000003H00(S_A-P_CAP 330U 2.5V M 6.3X4.2 LESR16M SL)	2012/12/06	DVT
5	Factory lack of material.	45	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2012/12/06	DVT
6	EMI request adjust +3VALWP/+5VALWP snubber function.	40	Change @PR404.@PC415.@PR406.@PC429 to PR404.PC415.PR406.PC429.	2012/12/06	DVT
7	EMI request adjust +3VALWP/+5VALWP boost resistor.	40	Change PR401.PR405 to SD013220B80(S RES 1/10W 2.2 +-5% 0603).	2012/12/06	DVT
8	EMI request add bypass capacitor.	40	Add PC412.PC413.PC416.PC419 to SE001471J80(S CER CAP 470P 50V J NPO 0805 H0.6)	2012/12/06	DVT
9	EMI request adjust CPU/GFX CORE snubber function.	45	Change @PR956.@PC948.@PR957.@PC949.@PR967.@PC968 to PR956.PC948.PR957.PC949.PR967.PC968.	2012/12/06	DVT
10	EMI request adjust bypass capacitor.	45	Change @PC940 to PC940.	2012/12/06	DVT
11	EMI request add bypass capacitor.	45	Add PC944.PC946 to SE00000G880(S CER CAP 0.1U 25V K X5R 0402) Add PC945.PC947 to SE075222K80(S CER CAP 2200P 25V K X7R 0402)	2012/12/06	DVT
12	Design Change of input capacitor.	40	Change PC420 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25) Add PC427 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25)	2012/12/07	DVT
13	Design Change of IC Application.	40	Add @PR409.@PR410 to SD028100180(S RES 1/16W 1K +-5% 0402) Add @PC405 to SE075472K80(S CER CAP 4700P 25V K X7R 0402) Add @PC407 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402) Add PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/12/10	DVT
14	Design Change of IC Application.	44	Change PC936 to SE000008980(S CER CAP 820P 25V K X7R 0402) Change PC929 to SE074332K80(S CER CAP 3300P 50V K X7R 0402) Change PC926 to SE071100J80(S CER CAP 10P 50V J NPO 0402) Change PC928 to SE074102K80(S CER CAP 1000P 50V K X7R 0402) Change PR943 to SD00000J280(S RES 1/16W 4.32K +-1% 0402) Change PR949.PR951 to SD014124380(S RES 1/10W 124K +-1% 0603 YAGEO)	2012/12/17	DVT
15	Design Change of CPU/GFX CORE Choke.	45	Change PL902.PL903.PL905 to SH00000NM00(S COIL 0.22UH +-20% PCMB104T-R22MS 35A)	2012/12/21	DVT
16	Design Change of VCCSA(LDO).	42	Delete PC607.PC608.PC609.PC610.PC611.PC612.PC613.PC614.PJ603.PJ604.PR608.PR609.PR610.PR611.PU602	2012/12/21	DVT
17	Reduction Part Count.	37	Delete PR110.	2013/01/18	PVT
18	Reduction Part Count.	42	Delete PR603.	2013/01/18	PVT
19	Reduction Part Count.	44	Delete PC916.	2013/01/18	PVT
20	Design Change of IC Application.	40	Change @PC405.@PR490.@PC407.@PR410 to PC405.PR490.PC407.PR410. Change PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 47 of 52

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
21	Reduction Part Count.	41	Change PR505.PR516 to SD028000080(S RES 1/16W 0 +-5% 0402) Change PR503 to SD013000080(S RES 1/10W 0 +-5% 0603)	2013/01/18	PVT
22	Design Change of Thermal Application.	41	Change PC521 to SGA20331E10(S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2013/01/18	PVT
23	Reduction Part Count.	43	Change PR702 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
24	Reduction Part Count.	44	Change PR926.PR916.PR917 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
25	Design Change of CPU/GFX CORE Choke.	45	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2013/01/18	PVT
26	Design Change of CPU/GFX CORE Frequence.	44	Change PR927 to SD034953280(S RES 1/16W 95.3K +-1% 0402)	2013/01/18	PVT
27	Factory lack of material.	40	Change PC420.PC427 to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	2013/01/18	PVT
28	Reduction Part Count.	40	Delete PR411.	2013/01/21	PVT
29	Design Change of Power Circuit Application.	38	Change PC208 to SE000003J80(S CER CAP 0.068U 16V K X7R 0402)	2013/01/23	PVT
30	Design Change of Power Circuit Application.	39	Add PR328 to SD028100280(S RES 1/16W 0 +-5% 0402) Add PQ314 to SB000009Q80(S TR 2N7002KW 1N SOT323-3)	2013/01/23	PVT
31	Design Change of Power Circuit Application.	40	Change PC405 to SE072103Z80(S CER CAP .01U 25V Z Y5V 0402) Change PC407 to SE075682K80(S CER CAP 6800P 25V K X7R 0402)	2013/03/04	PVT
32	Design Change of Power Circuit Application.	42	Add PR608 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/03/14	Pre-MP

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 48 of 52

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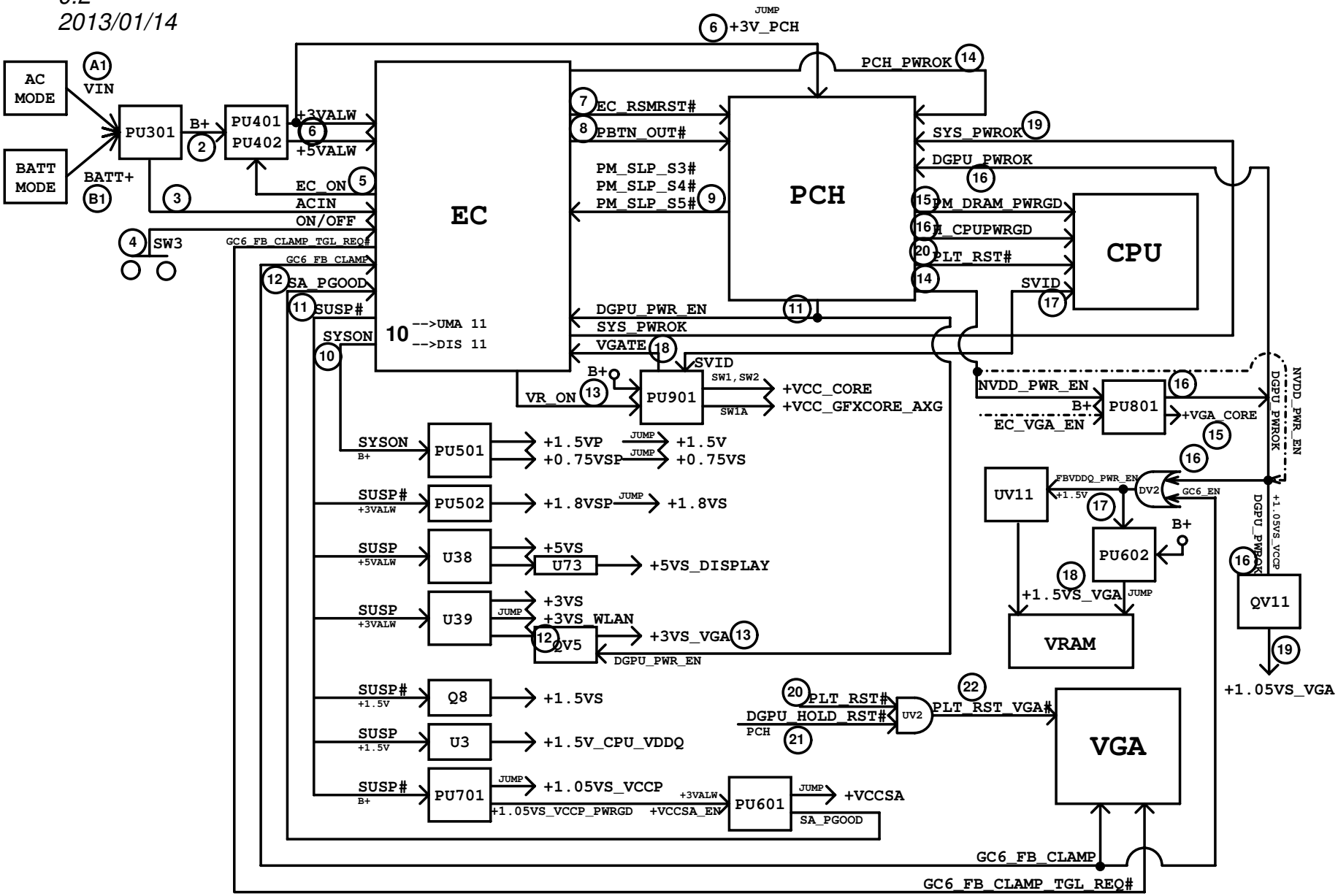
MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-9901P*
REVISION: *0.2*
DATE: *2013/01/14*



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: **SCHEMATIC M/B LA-9902**

Size: Custom | Document Number: **4019N1** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 49 of 52

VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.5~11	Change footprint of JCPU1	For Lenovo rule
2	P.14	Add R406, R407, R408, R409	Reserve for improvement factory processes
3	P.42	Add EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
4	P.42	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
5	P.42	Reserve R410	Reserve Pull-high for GPIO use
6	P.42	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design
7	P.42	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
8	P.42	Change ENBKL from EC Pin.73 to EC Pin.76	For common design
9	P.42	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
10	P.42	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
11	P.34	Add R411, R412, C411, C412	Reserve for EMI
12	P.20	Add Q21, R40, C237, Q22, R418, C243, C252, R413	Reserve for power consumption
13	P.25	Del Q12/R806	For Change Audio Jack type from Normal close to Normal open

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Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 50 of 52

VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			DVT TO PVT
1	P.26	Reserve R508	For leakage current issue of Atheros WLAN
2	P.31	Change RA22 to reserve	For PC Beep issue(can't heard sound of "di" on BIOS setup menu)
3	P.31	Reserve RA10/RA11	For solve Codec speaker Hum noise issue(Zizi)
4	P.32	Reserve R416	Reserve +3VLP power rail to EC
5	P.32	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC
6	P.32	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC
7	P.14	Change U5 from 4MB to 8MB ROM	Follow common design
			PVT TO Pre-MP
1	P.32	Chagne R416 to shortpad	
2	P.42	Reserve +1.05S_VCCP_PWRGOOD of +V1.05S_VCCP to connect to SA_PGOOD	For Celeron/Pentium CPU

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Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 51 of 52

Item	Reason for change	PG#	Modify List	Date	Phase
44					
45					
46					
47					
48					
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51					
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52					
53					

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 52 of 52