

MODEL NAME :VAW03

PCB NO : LA-9103P

BOM P/N : DA60000UT00 LA-9103P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

Inspiron Value OAK(Essentials) 15 UMA (Comal Richland)
Inspiron Value OAK(Essentials) 15 Discrete#1 (Comal Richland, AMD Mars Pro)
Inspiron MainStream OAK(Essentials) 15 UMA (Comal Richland)
Inspiron MainStream OAK(Essentials) 15 Discrete#2 (Comal Richland, AMD Mars Pro)
Vostro Value OAK(Essentials) 15 UMA (Comal Richland)

Dell / Compal Confidential

Schematic Document

AMD FP2 Richland Processor with DDRIII + Bolton M3 FCH
AMD VGA Sun XT

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
UMA@ : Only for UMA
DIS@ : Only for Discrete
GCLK@ : Green CLK implemented
NGCLK@ : Non Green CLK implemented
@3221: ALC 3221
@3223 : ALC 3223
EMC@ : EMC Parts
2nd@ : for APL3512 2nd source control
(RN9, RV32, RL22)

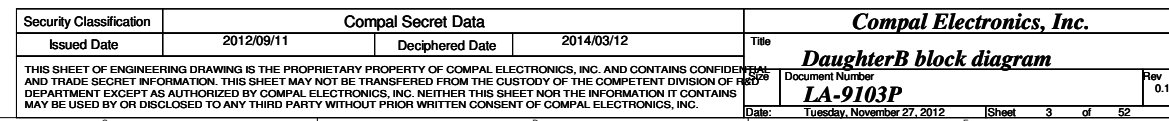
2012-11-26

Rev: 0.2

R1@ : R1 P/N for PCB
R3@ : R3 P/N for PCB
THR1@ : Thames-XT R1 P/N
THR3@ : Thames-XT R3 P/N
CHR1@ : Chelsea-Pro R1 P/N
CHR3@ : Chelsea-Pro R3 P/N
R@ : RTD2132-R
S@ : RTD2132-S

X76@ : VRAM Group
CH@ : Chelsea M2
SE@ : Seymour M2
TH@ : Thames-XT
Mars@ : Mars Pro M2
A4R1@ : A4 APU-R1
A6R1@ : A6 APU-R1
A8R1@ : A8 APU-R1
A8@ : A8 APU Symbol
Hud@ : HUDSON-M3
Bol@ : BOLTON-M3

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				Sheet	1 of 52
				Rev	0.1



Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	000 1011	11h 0x16	ADM1032ARMZ	100 1101	4Dh 0x9A
Charger IC	000 1001	09h 0x12	SB-TSI	100 1100	4Ch 0x98
			RTD2132	100 1010	4Ah 0x94
			GPU	100 0001	41h 0x82

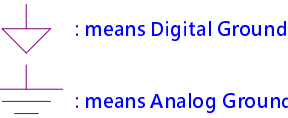
SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

Symbol Note :



FCH

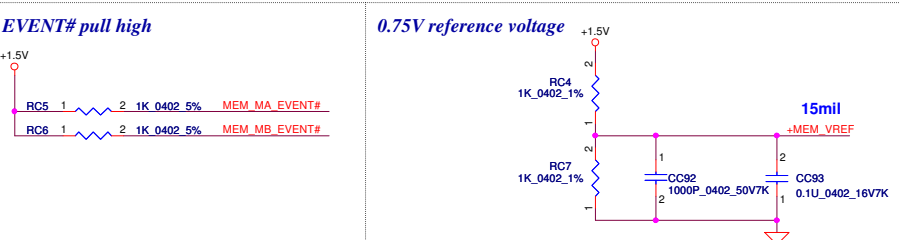
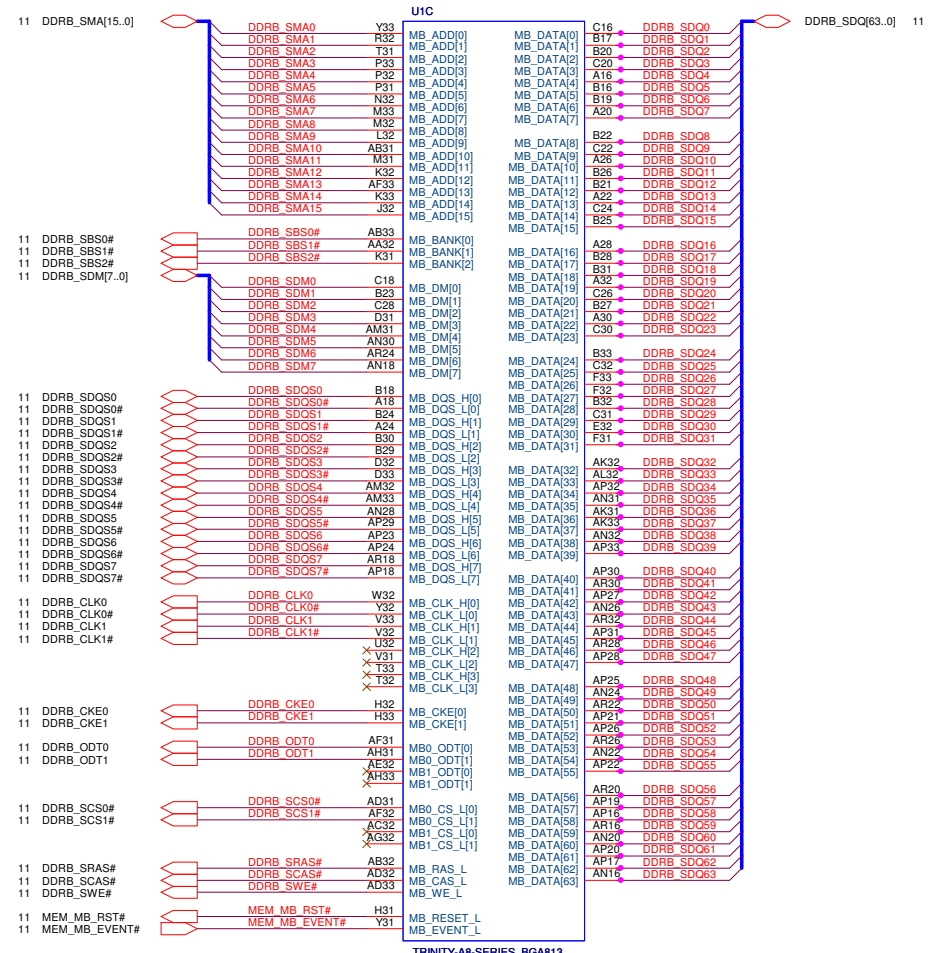
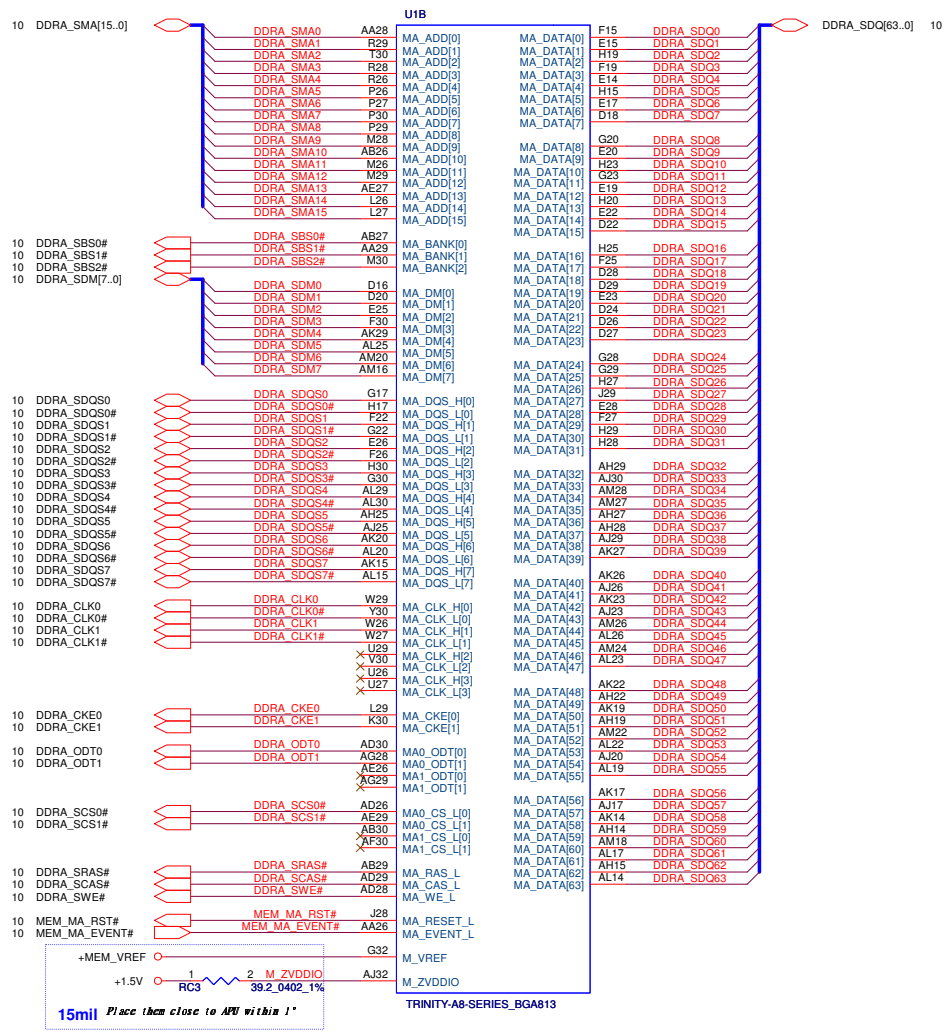
USB PORT#	DESTINATION
0	USB conn.3 DEBUG PORT
1	MINI CARD (WLAN)
2	USB conn.4
3	NC
4	NC
5	NC
6	Card Reader
7	NC
8	NC
9	Camera
10	USB conn.2
11	NC
12	NC
13	USB conn.1

CLK

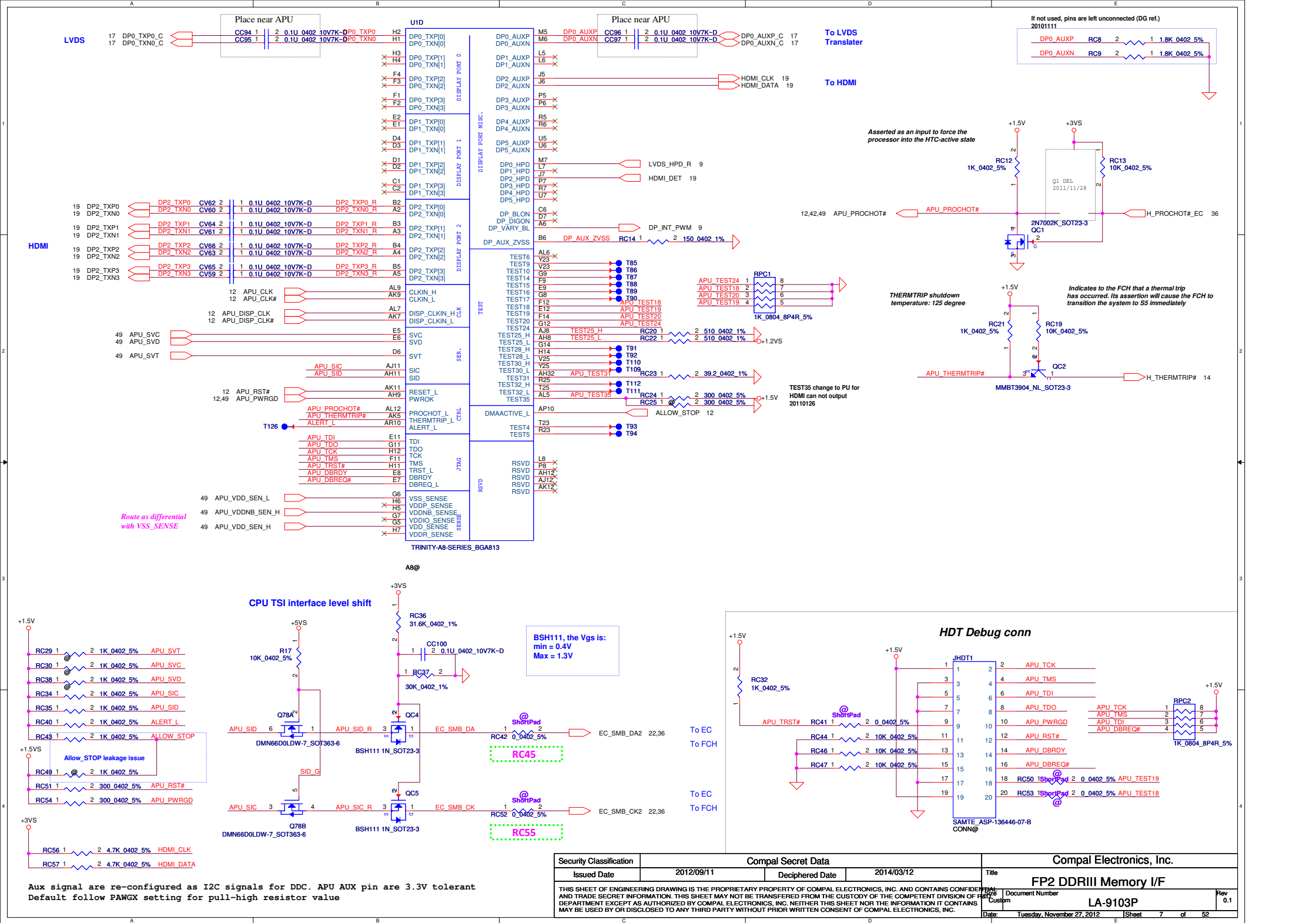
DIFFERENTIAL	DESTINATION
CLKOUT_PCIE0	None
CLKOUT_PCIE1	None
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI CARD WLAN
CLKOUT_PCIE4	None
CLKOUT_PCIE5	None
CLKOUT_PCIE6	None
CLKOUT_PCIE7	None
CLKOUT_PEG_B	None

SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

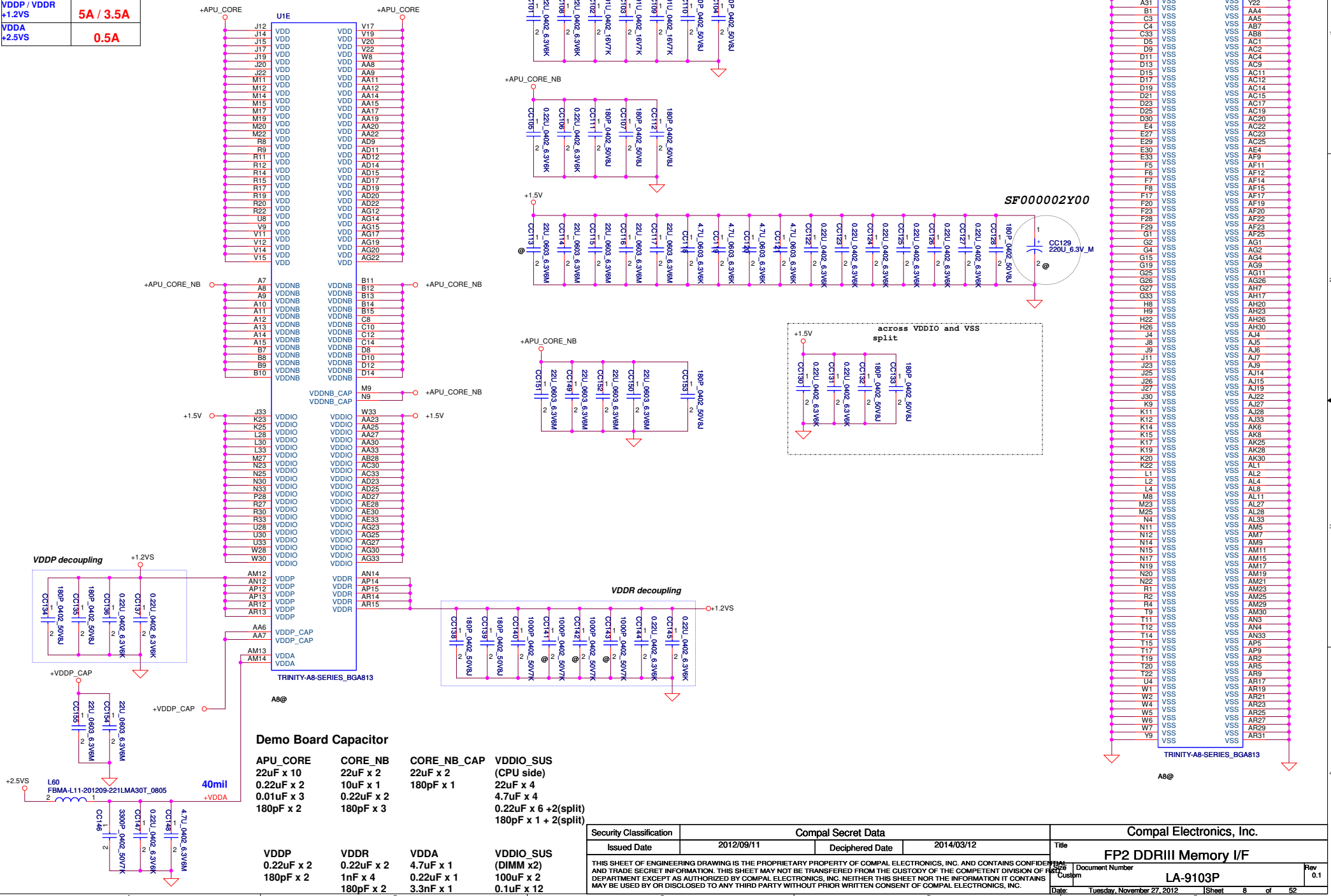


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						Document Number		LA-9103P		Rev	
						Custom				0.1	
						Date		Tuesday, November 27, 2012		Sheet 6 of 52	



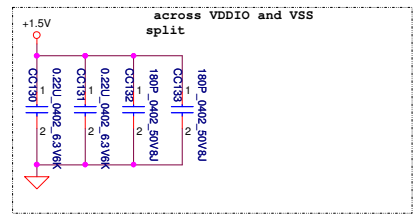
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title FP2 DDRIII Memory I/F		
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Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



U1F		
A17	VSS	Y11
A19	VSS	Y12
A21	VSS	Y14
A23	VSS	Y15
A25	VSS	Y17
A27	VSS	Y19
A29	VSS	Y20
A31	VSS	Y22
B1	VSS	AA4
C3	VSS	AA5
C4	VSS	AB7
C33	VSS	AB8
D5	VSS	AC1
D9	VSS	AC2
D11	VSS	AC4
D13	VSS	AC9
D15	VSS	AC11
D17	VSS	AC12
D19	VSS	AC14
D21	VSS	AC15
D23	VSS	AC17
D25	VSS	AC19
D30	VSS	AC20
E4	VSS	AC22
E27	VSS	AC23
E29	VSS	AC25
E30	VSS	AE4
E33	VSS	AF9
F5	VSS	AF11
F6	VSS	AF12
F7	VSS	AF14
F8	VSS	AF15
F17	VSS	AF17
F20	VSS	AF19
F23	VSS	AF20
F28	VSS	AF22
F29	VSS	AF23
G1	VSS	AG5
G2	VSS	AG1
G4	VSS	AG2
G15	VSS	AG4
G19	VSS	AG9
G26	VSS	AG11
G26	VSS	AG26
G27	VSS	AH7
G33	VSS	AH17
H6	VSS	AH20
H6	VSS	AH23
H22	VSS	AH26
H26	VSS	AH30
J4	VSS	AJ4
J8	VSS	AJ5
J9	VSS	AJ6
J11	VSS	AJ7
J23	VSS	AJ8
J25	VSS	AJ14
J26	VSS	AJ15
J27	VSS	AJ19
J30	VSS	AJ22
K9	VSS	AJ27
K11	VSS	AJ28
K12	VSS	AJ33
K14	VSS	AK6
K15	VSS	AK8
K17	VSS	AK25
K19	VSS	AK28
K20	VSS	AK30
K22	VSS	AL1
L1	VSS	AL2
L2	VSS	AL4
L4	VSS	AL8
M6	VSS	AL11
M23	VSS	AL27
M25	VSS	AL28
N4	VSS	AL33
N11	VSS	AM5
N12	VSS	AM7
N14	VSS	AM9
N15	VSS	AM11
N17	VSS	AM15
N19	VSS	AM17
N20	VSS	AM19
N22	VSS	AM21
R1	VSS	AM23
R2	VSS	AM25
R4	VSS	AM29
T9	VSS	AM30
T11	VSS	AN3
T12	VSS	AN4
T14	VSS	AN33
T15	VSS	AP5
T17	VSS	AP9
T19	VSS	AR2
T20	VSS	AR5
T22	VSS	AR9
U4	VSS	AR17
W1	VSS	AR19
W2	VSS	AR21
W4	VSS	AR23
W5	VSS	AR25
W6	VSS	AR27
W7	VSS	AR29
Y9	VSS	AR31

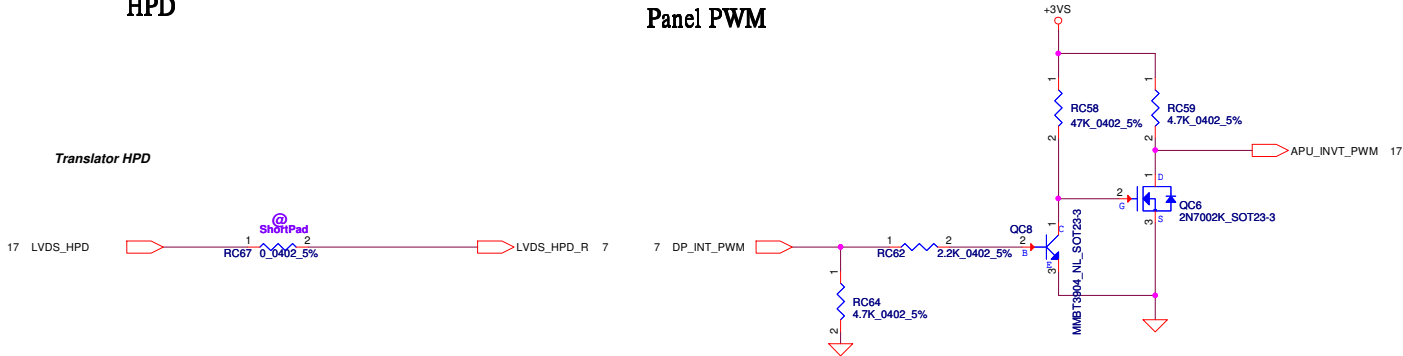
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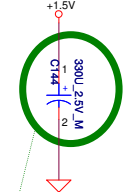
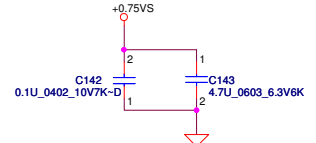
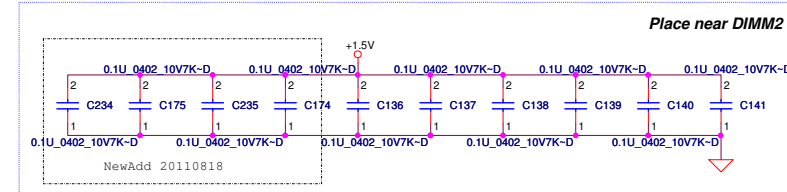
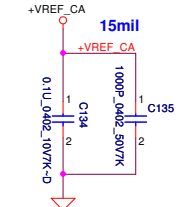
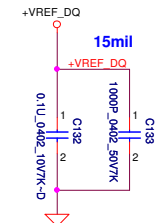
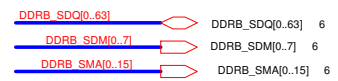
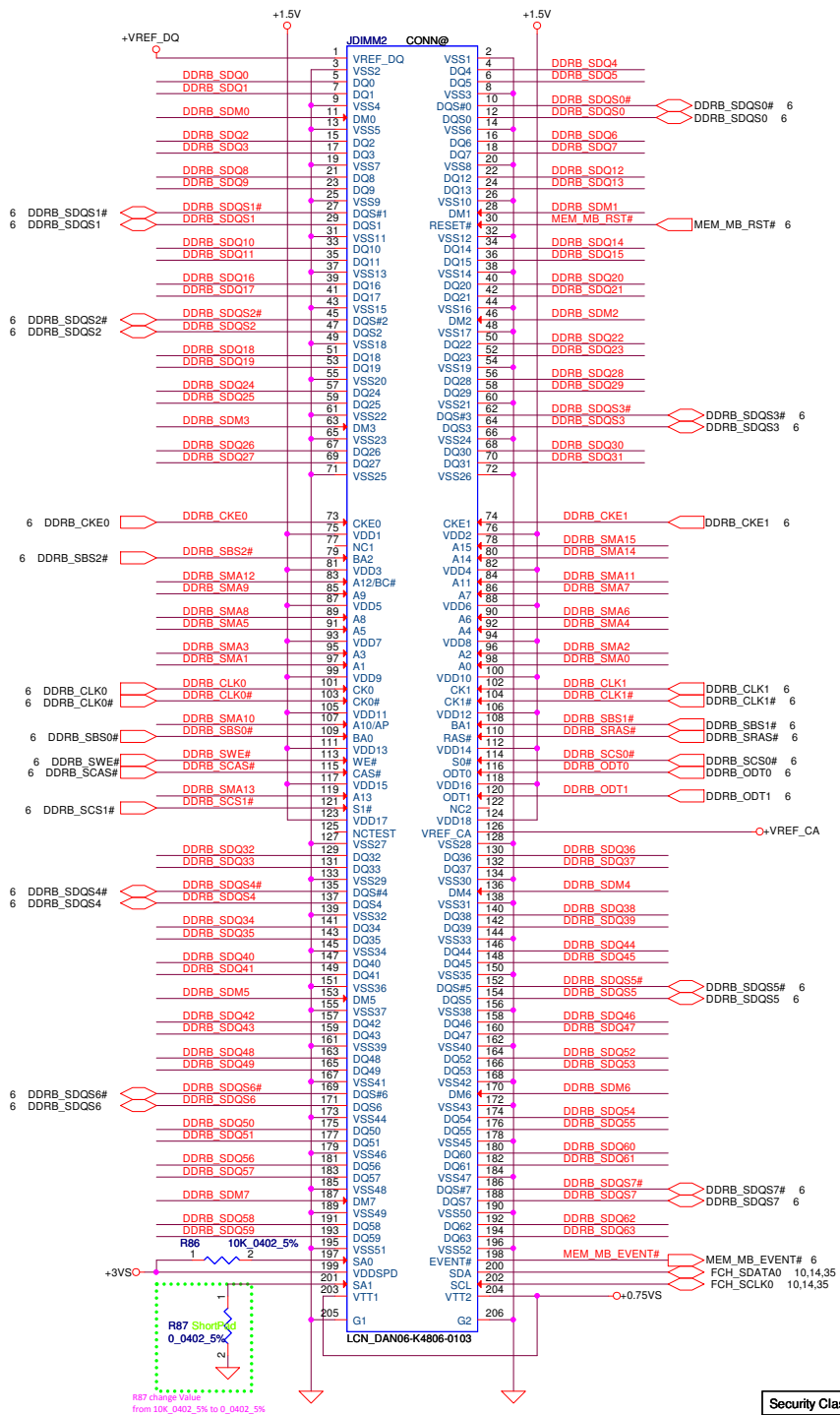


HPD

Panel PWM

Translator HPD

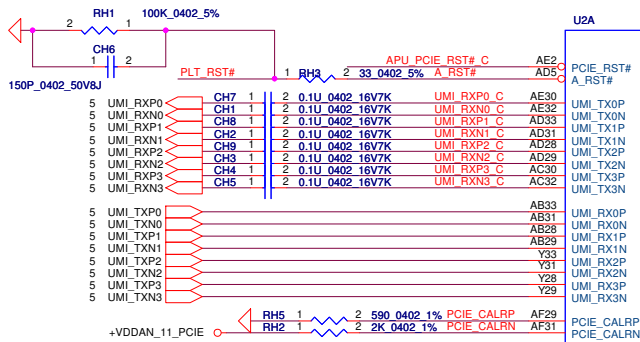




(330uF_6.3V_4.2L_ESR17m)*1=(SF000002Z00)

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R90/ C146 close to FCH



Move PCIe device to APU. 20110819

SS

APU DISP

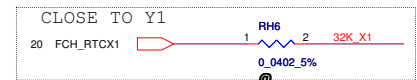
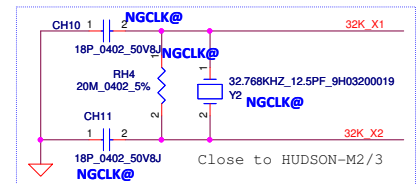
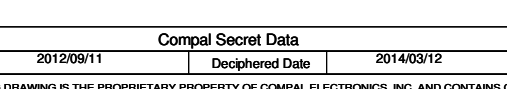
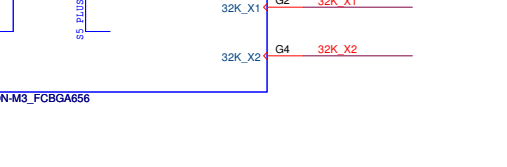
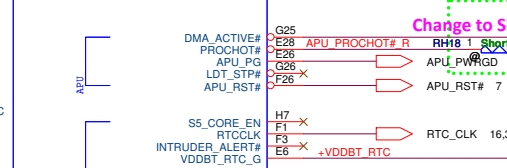
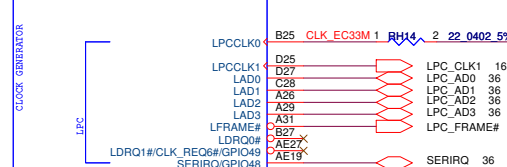
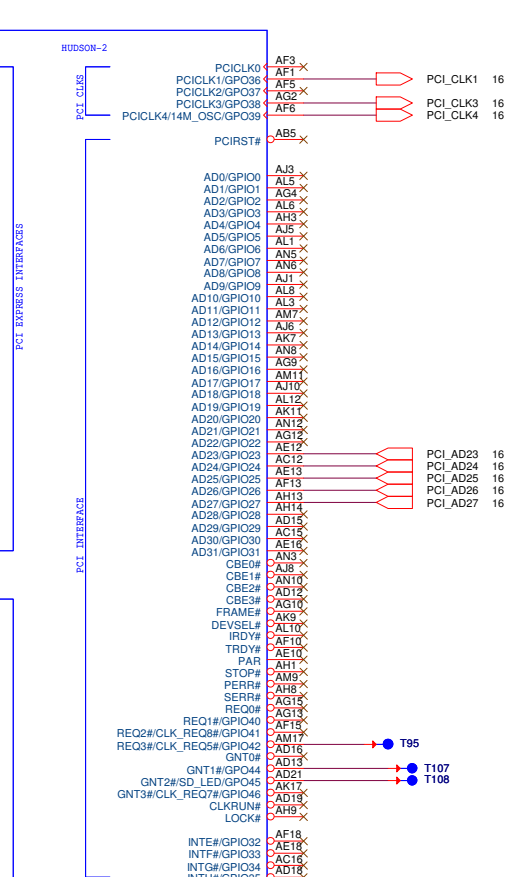
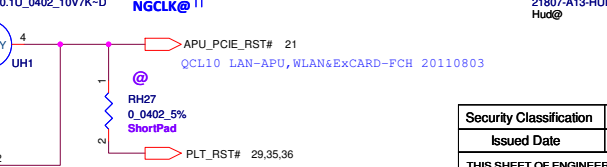
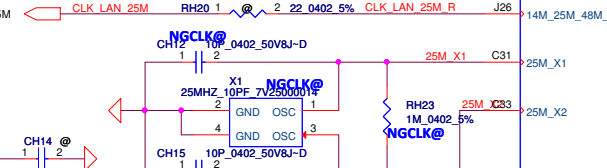
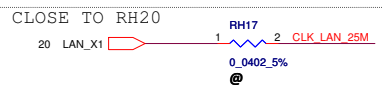
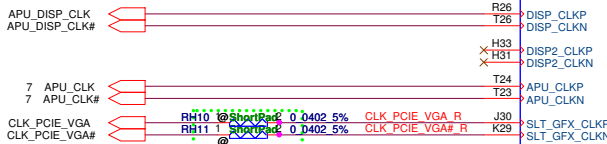
APU

VGA

WLAN

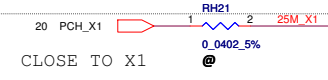
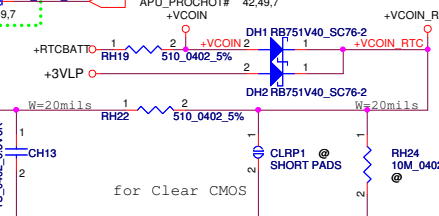
LAN

For "EXT" CLK mode, input to PCIe,

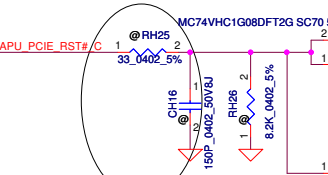


APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

Change to Short Pad



For PCIe device reset on FS1 (GFX, LAN, WLAN, LVDS, Travis)
APU_PCIE_RST# : Reset PCIe device on APU

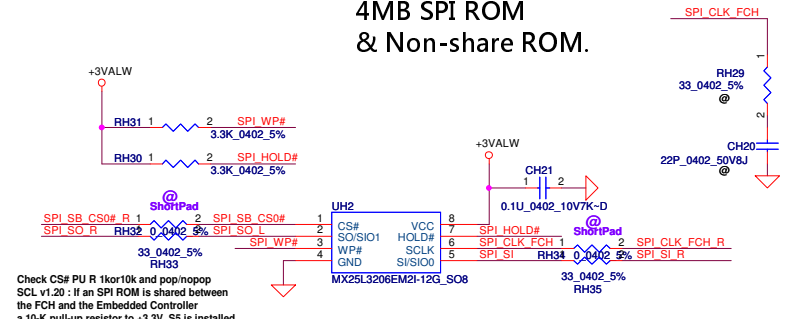
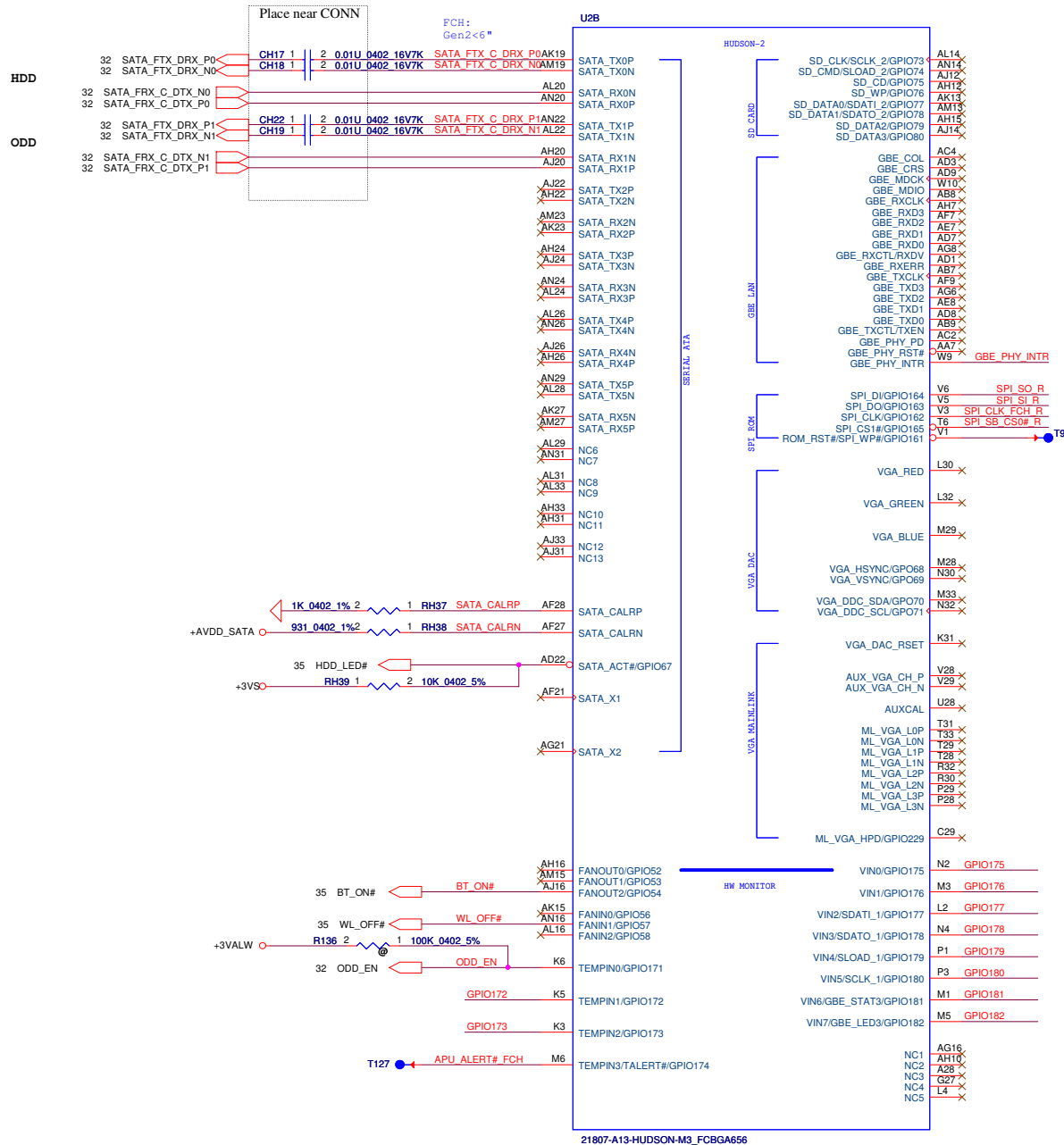


R692/ C790 close to FCH

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				2014/03/12				Document Number			
								LA-9103P			
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								0.1			

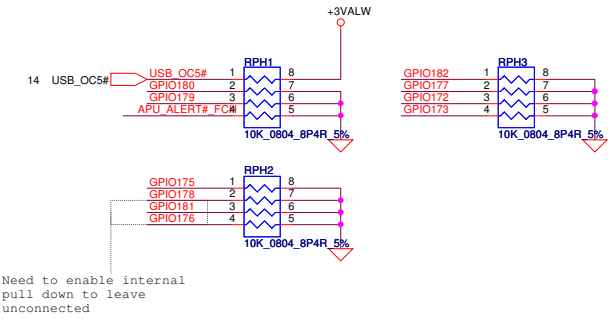
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4MB SPI ROM & Non-share ROM.



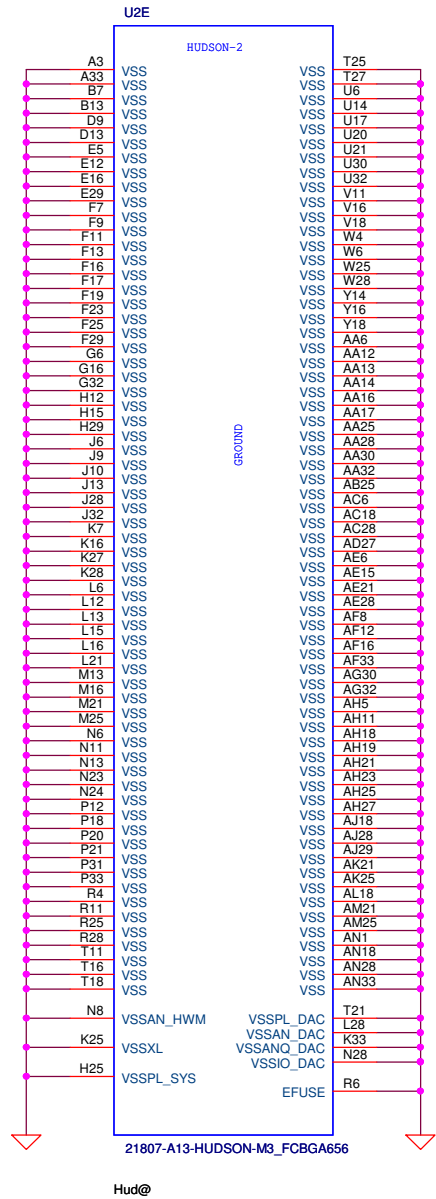
GBE_PHY_INTR
Pulled-up to +3.3V_S5 with a 10-K 5% resistor.
FCH SCL v1.20 #19-85

Removed RGMII/MII support and updated termination requirements for GBE_COL, GBE_CRD, GBE_RXERR and GBE_MDIO when RGMII/MII interface is not used.
FCH DGv1.20 / SCL v1.20



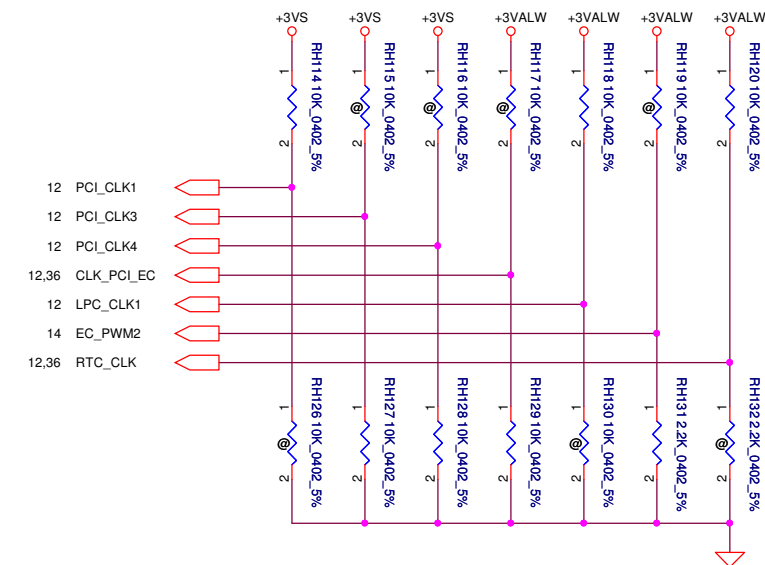
Hud@

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								Custom		LA-9103P	0.1
Date: Tuesday, November 27, 2012								Sheet		13 of 52	



STRAP PINS

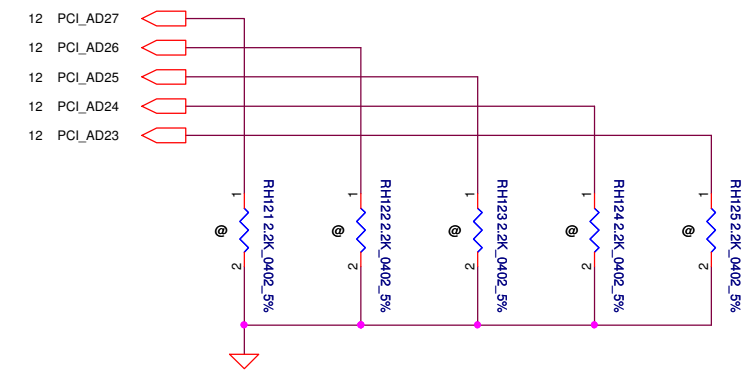
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



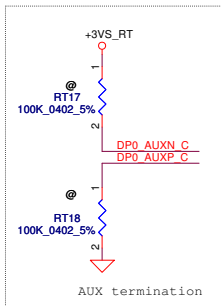
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

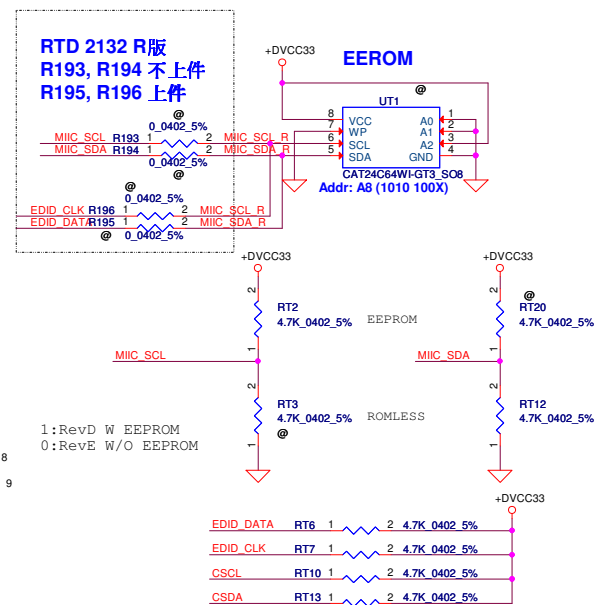
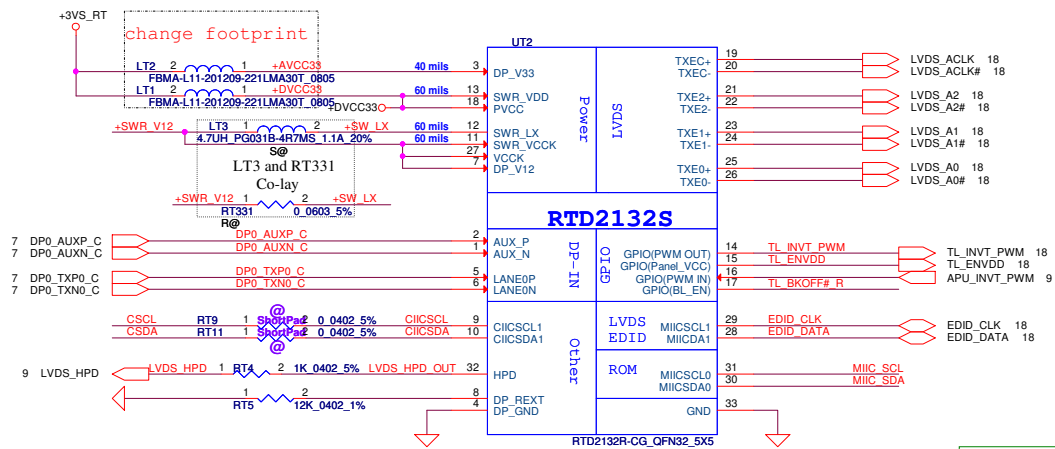


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								Size B	Document Number			LA-9103P		Rev	0.1
								Date: Tuesday, November 27, 2012							
		3		2		Sheet		16	of 52						

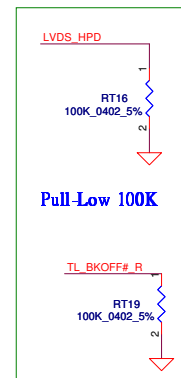


Power Consumption:

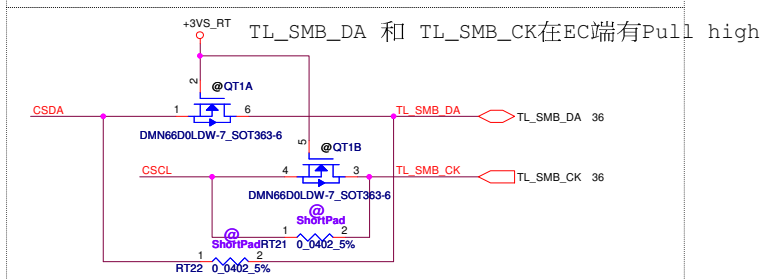
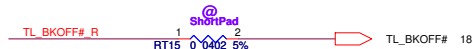
- Pin3 (DPV33) < 20mA
- Pin 7 (DP_V12) < 100mA
- Pin 11 (SWR_VCKK) < 100mA (layout trace > 60 mil)
- Pin 12 (SWR_LX) < 600mA (layout trace > 60 mil)
- Pin 13 (SWR_VDD) < 200mA (layout trace > 40 mil)
- Pin 18 (PVCC) < 50 mA
- Pin 27 (VCKK) < 50mA



		Pin30	
		0	1
Pin31	0	x	EP MODE
	1	ROM	EEPROM

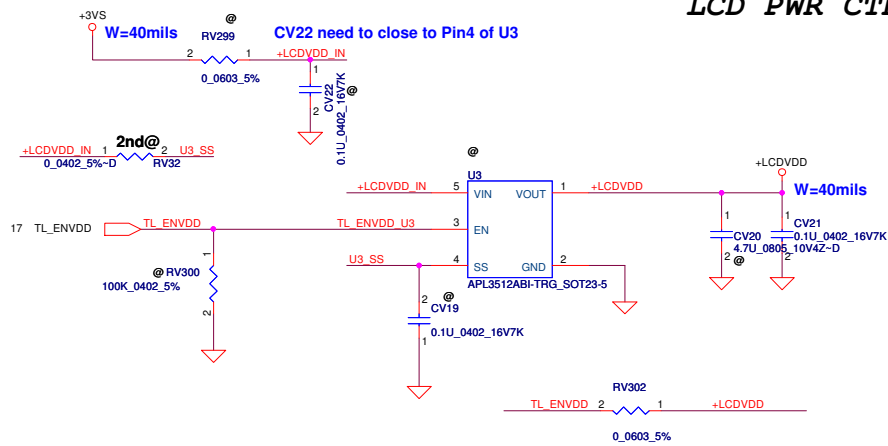


Vendor advise reserve it

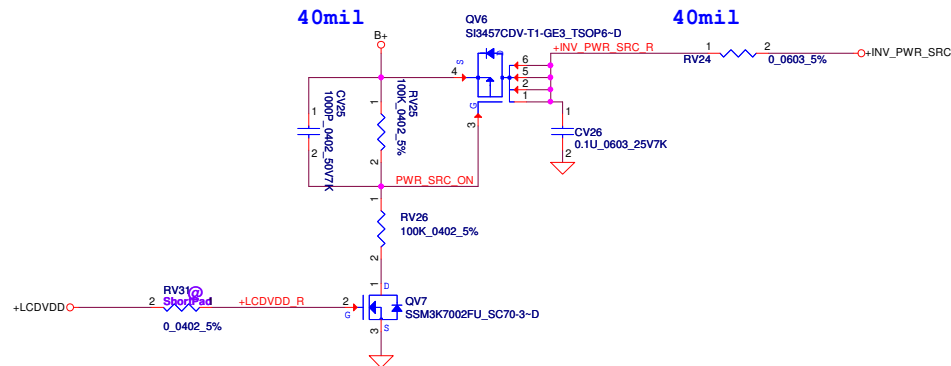


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				Doc Number	LA-9103P
				Date:	Tuesday, November 27, 2012
				Sheet	17 of 52

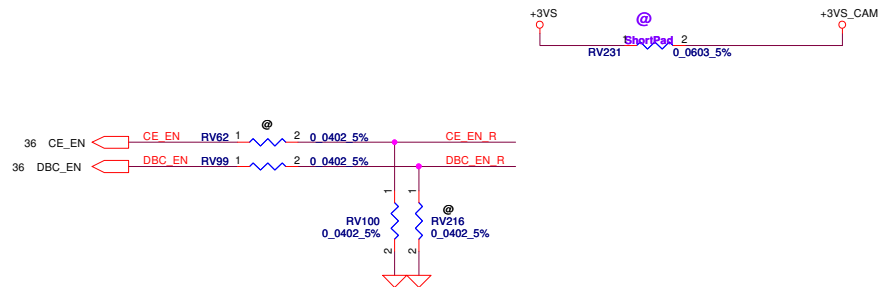
LCD PWR CTRL



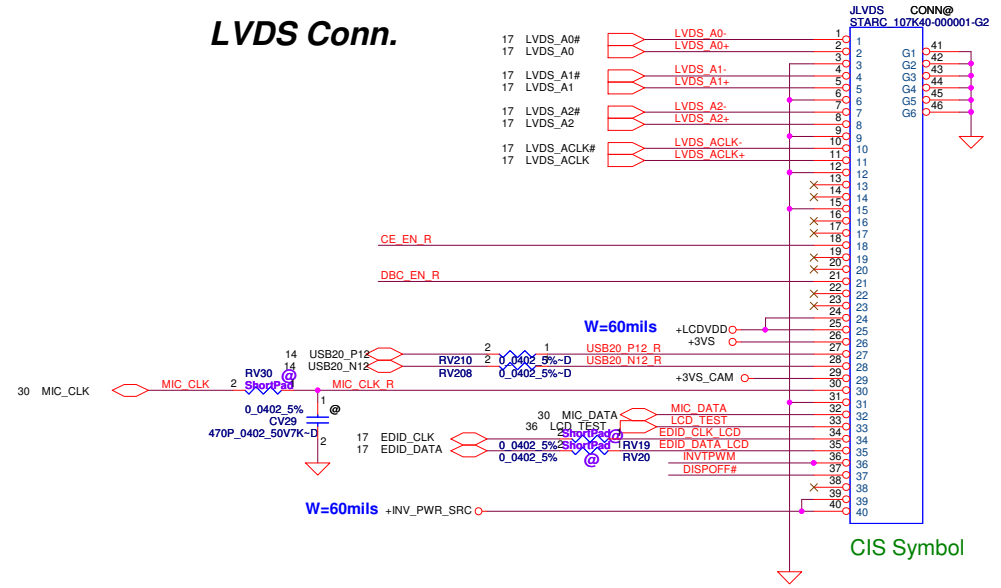
LCD backlight PWR CTRL



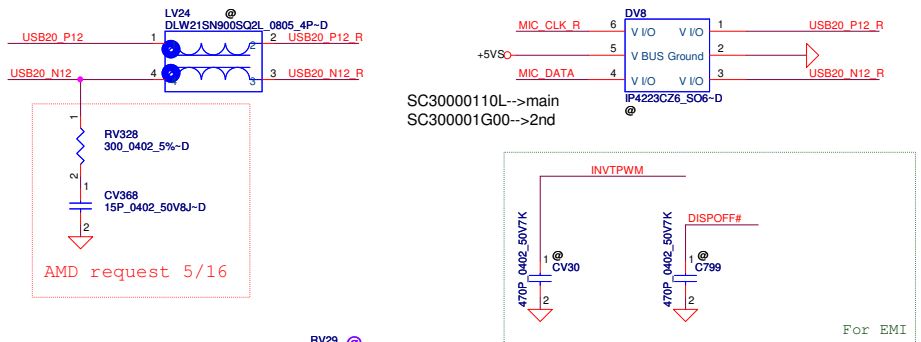
Wedcam PWR CTRL



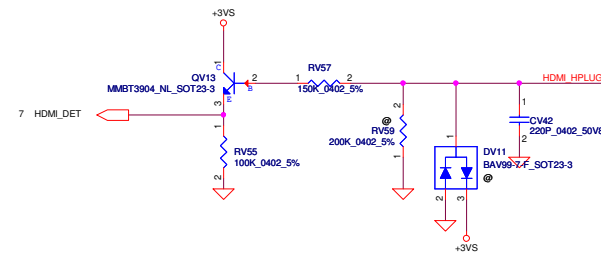
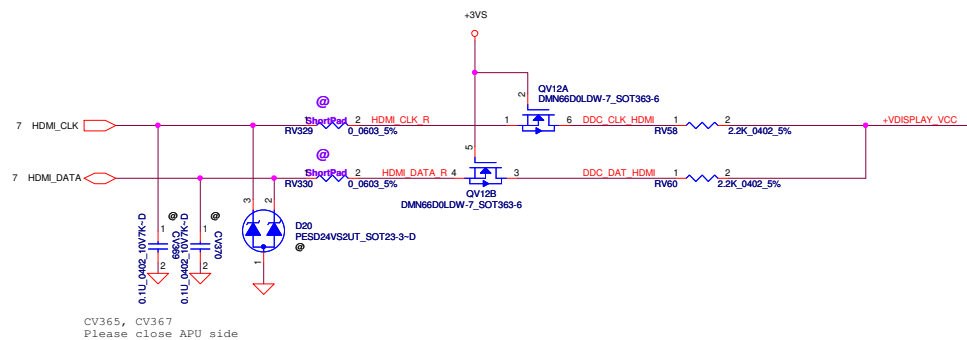
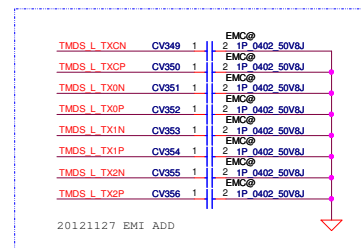
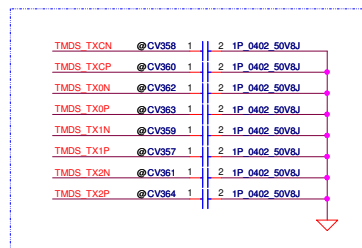
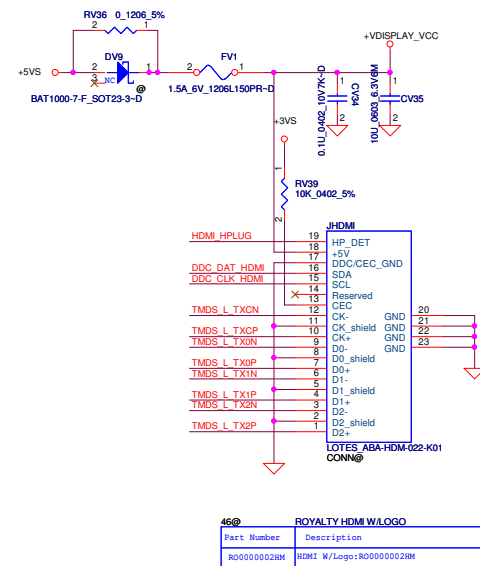
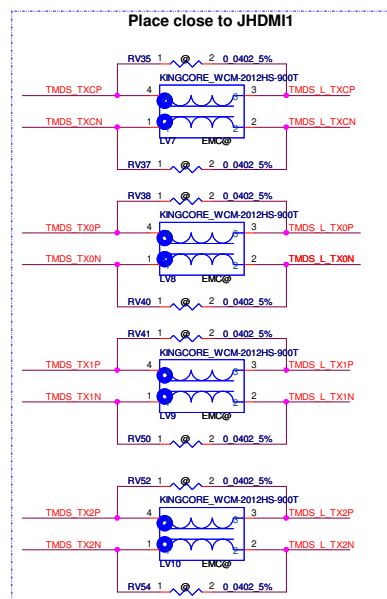
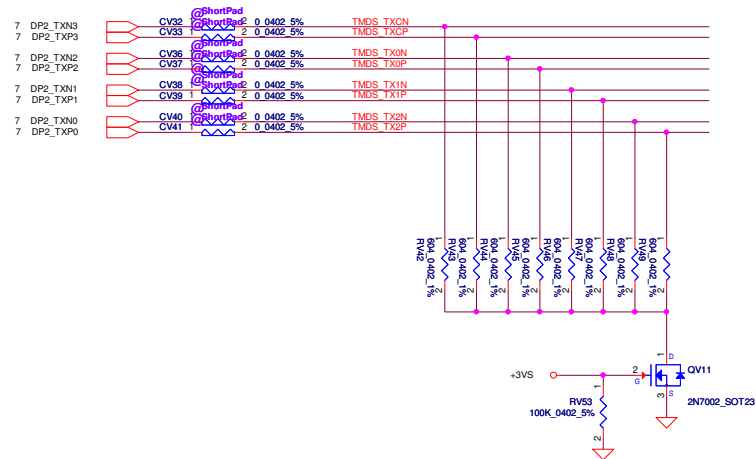
LVDS Conn.



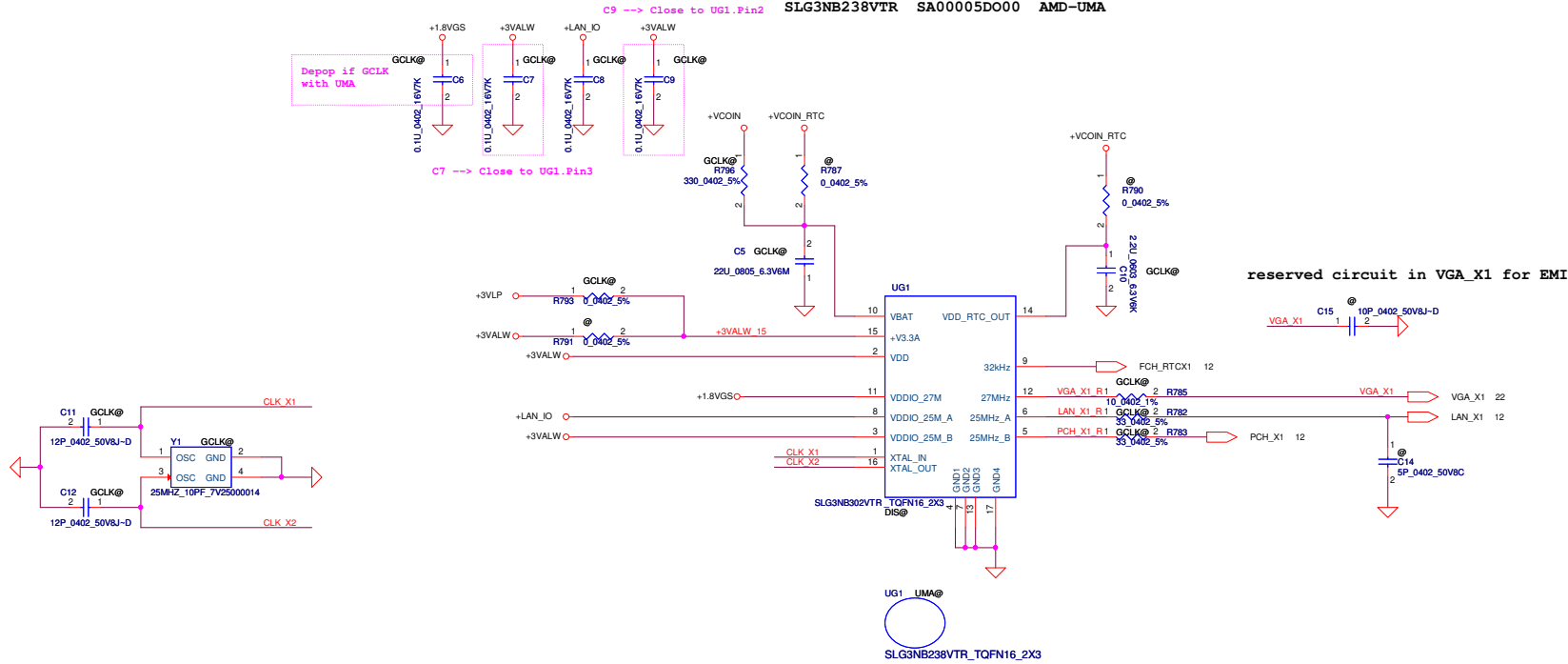
*** Reserved for EMI/ESD/RF
need to close to JLVDS**

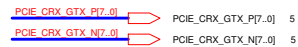


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						Date	Sheet
						Tuesday, November 27, 2012	18 of 52

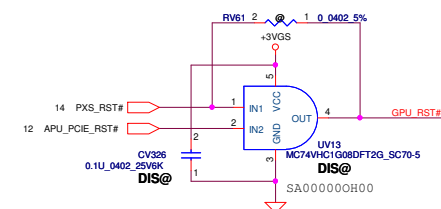


SLG3NB244VTR SA000057I00 Intel-UMA
SLG3NB300VTR SA00005RS00 Intel-DIS
SLG3NB302VTR SA00006D500 AMD-DIS
SLG3NB238VTR SA00005D000 AMD-UMA



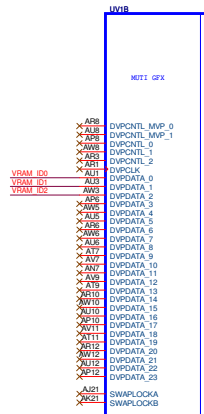
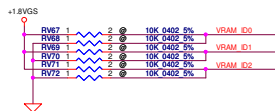


PCI EXPRESS INTERFACE



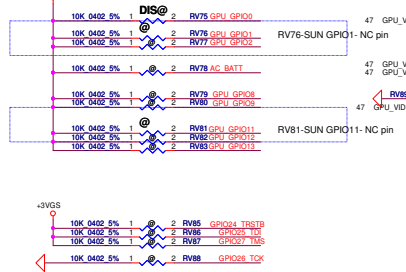
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OPTIONAL FOR MEMORY ID ON HEATHROW/CHELSEA/VENUS/THAMES/SEYMOUR ONLY
No DVO or GPIO function on Mars



SUN GPU GPIO1, 2, 7, 11, 12, 13, 14, 18 - NC pin

STRAPS



0.60 V level, Please
VREFG Divider ans
cap close to ASIC

20mil

0.935V@Mars Pro

0.935V@Mars Pro

0.935V@Mars Pro

0.935V@Mars Pro

0.935V@Mars Pro

0.935V@Mars Pro

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0.935V@Mars Pro

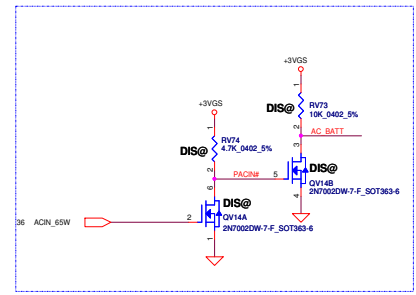
0.935V@Mars Pro

0.935V@Mars Pro

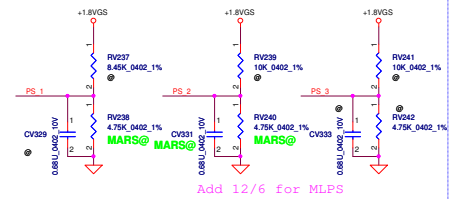
0.935V@Mars Pro

CONFIGURATION STRAPS				RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE				0= DO NOT INSTALL RESISTOR	
GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				1= INSTALL 10K RESISTOR	
				X= DESIGN DEPENDANT	
				NA= NOT APPLICABLE	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS		
TX_PWR_EN	GPIO0	POE FULL TX OUTPUT SWING	0: 50% swing 1: Pull-up swing	X	
TX_DEEMPH_EN	GPIO1	POE TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X	
REVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.5GT/s 1: 5.0GT/s	0	
REVD	GPIO8	RESERVED		0	
BIF_VGA_DIS	GPIO9	VGA ENABLED		0	
REVD	GPIO21	RESERVED		0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X	
ROMCFG(2:0)	GPIO(3:1)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX	
VP_DEVICE_STRAP_ENA	VSYNCC	IGNORE VP DEVICE STRAPS		0	
REVD	HSSYNCC			0	
REVD	GENERICC			0	
AUD(1)	HSYNCC	AUD(1) AUD(0) 0: 0 No audio function 0: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI		11	
AUD(0)	VSYNCC				
GPIO21	HSSYNCC				
GPIO2	GENERICC				
GPIO8					

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL
RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND
NOT CONFLICT DURING RESET



MLPS Setting please refer Page 24



TX_PWR_EN	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

MLPS Bit	strap	AMD recommended setting	R_FU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC	
PS1:	10000	RV237=NC	RV238=8.475K	CV329=NC	
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u	

[] Via call back function:

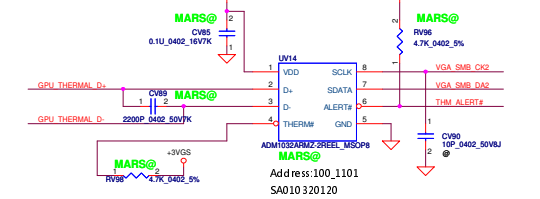
[V] Reading from GPIO/LCD/ATA pins: PS_3

ID	Memory Type	Configuration	Row x Col x Bank bits	Channel Size	VPN	DPN
0	Samsung K4W2G1646E-BC11	128Mx16x8PCS	14"10"8	2G	K4W2G1646E-BC11	2488G
1	Samsung K4W2G1646E-BC11	128Mx16x4PCS	14"10"8	1G	K4W2G1646E-BC11	
2	Micron MT41K128M16JT-107G-K	128Mx16x4PCS	14"10"8	1G	MT41K128M16JT-107G-K	
3	Hynix H5TC2G63FFR-11C	128Mx16x4PCS	14"10"8	1G	H5TC2G63FFR-11C	
4	Samsung K4W4G1646B-HC11	256Mx16x4PCS	15"10"8	2G	K4W4G1646B-HC11	
5	Micron MT41K256M16HA-107G-E	256Mx16x4PCS	15"10"8	2G	MT41K256M16HA-107G-E	
6	Hynix H5TC4G63AFR-11C	256Mx16x4PCS	15"10"8	2G	H5TC4G63AFR-11C	
7						

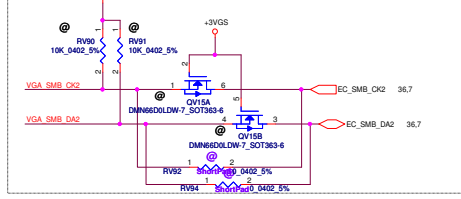
P5_3 CONFIG [2:0]		Memory Configuration					
ID	RV241	RV242	Bits[3:1]	Memory Type	Configuration	Row x Col x Bank bits	Channel Size
0	NC	4750	000	Samsung-DDR3	128M x 16 8PCS	14 x 10 x 8	2G
1	8450	2000	001	Samsung-DDR3	128M x 16 4PCS	14 x 10 x 8	1G
2	4530	2000	010	Micron-DDR3	128M x 16 4PCS	14 x 10 x 8	1G
3	6980	4990	011	Hynix-DDR3	128M x 16 4PCS	14 x 10 x 8	1G
4	4530	4990	100	Samsung-DDR3	256M x 16 4PCS	15 x 10 x 8	2G
5	3240	5620	101	Micron-DDR3	256M x 16 4PCS	15 x 10 x 8	2G
6	3400	10000	110	Hynix-DDR3	256M x 16 4PCS	15 x 10 x 8	2G
7	4750	NC	111				

VGA Thermal Sensor ADM1032ARMZ

Close to GPU



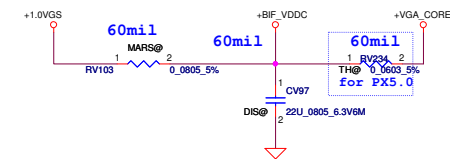
Internal VGA Thermal Sensor



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Switch circuits in BACO desings for Thanes/Seymour only

for PX4.0 and PX5.0

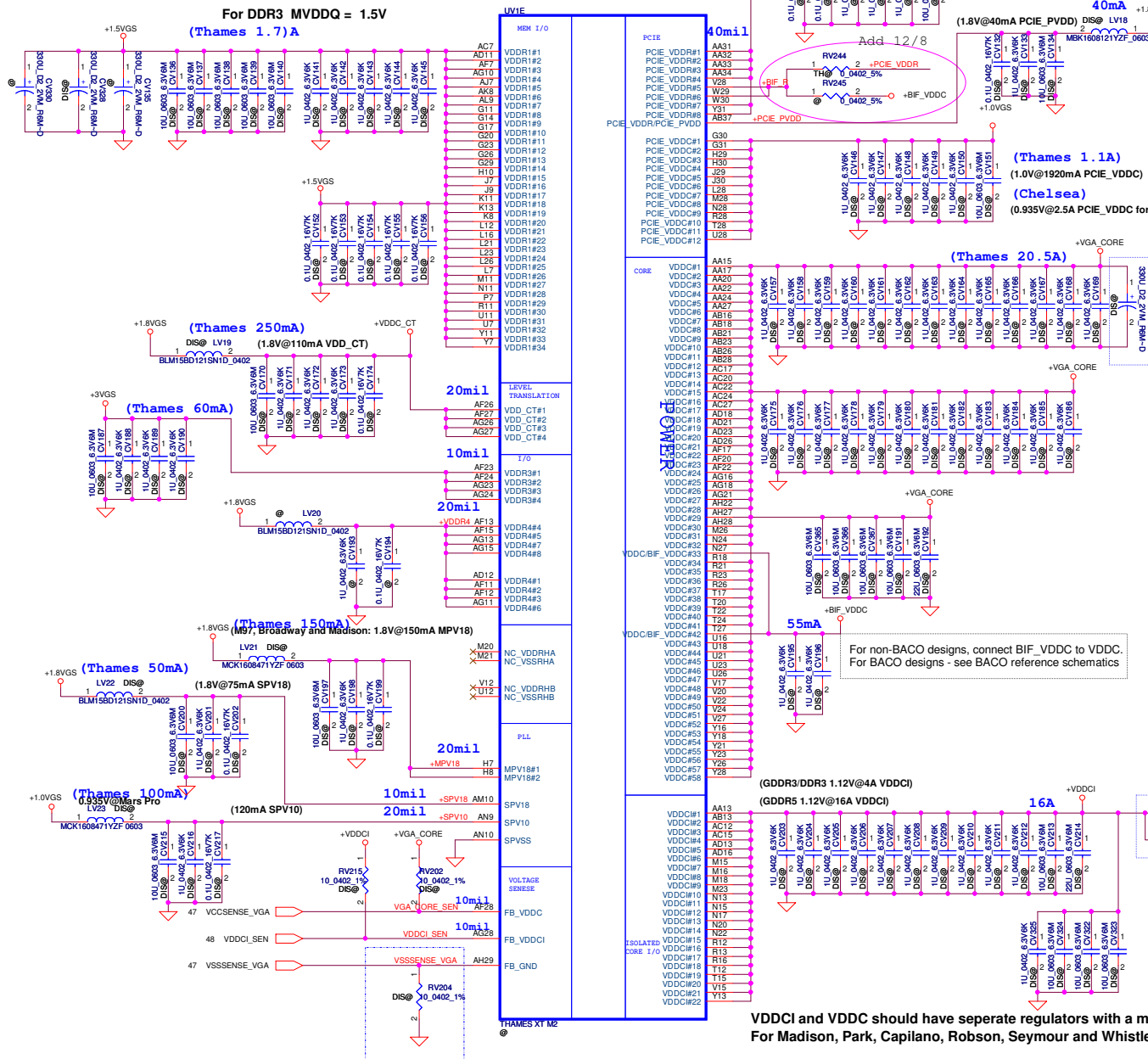


+1.5VGPU 2 JP10 1 +1.5VGS
JUMP_43X118

+1.5VGPU直接由Power線路Control

```
PX4.0 +VGA_CORE,VDDCI,+1.5VGS OFF
PX4.0 +3VGS, +1.0VGS,+1.8VGS ON
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF
```

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				LA-9103P	
Date:	Tuesday November 27, 2012	ISheet	23	of	50



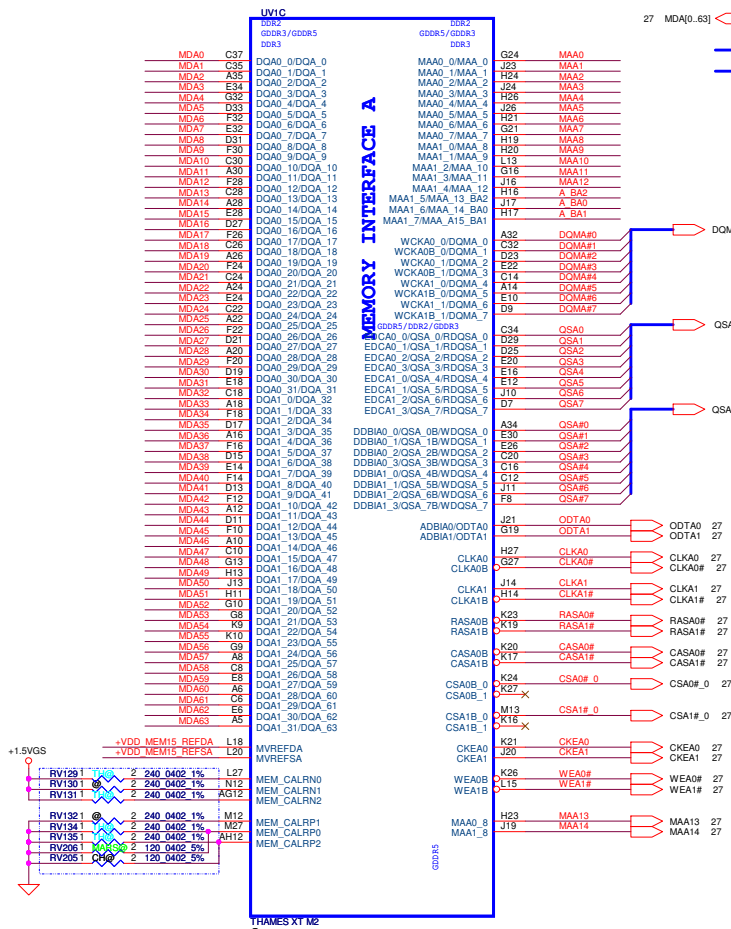
For Thames/Seymour
BIF_VDDC is connected to VDDC in non BACO designs
BACO designs, switch circuits is required so that
when GPU is operating, BIF_VDDC is connected to VDDC,
while in BACO mode, BIF_VDDC is connected to +1.0V

For MARS/VENUS/HEATHROW/CHELSEA
BIF_VDDC should be connected with 0.95V

On Heathrow/Chelsea/Venus/Mars only
PCI_VDDC : 0.95V @ 1.3A (GEN3.0)

VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

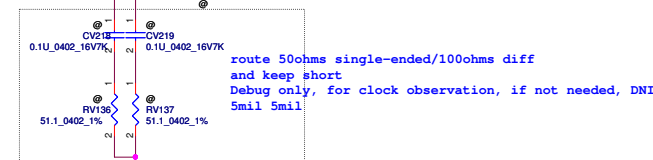
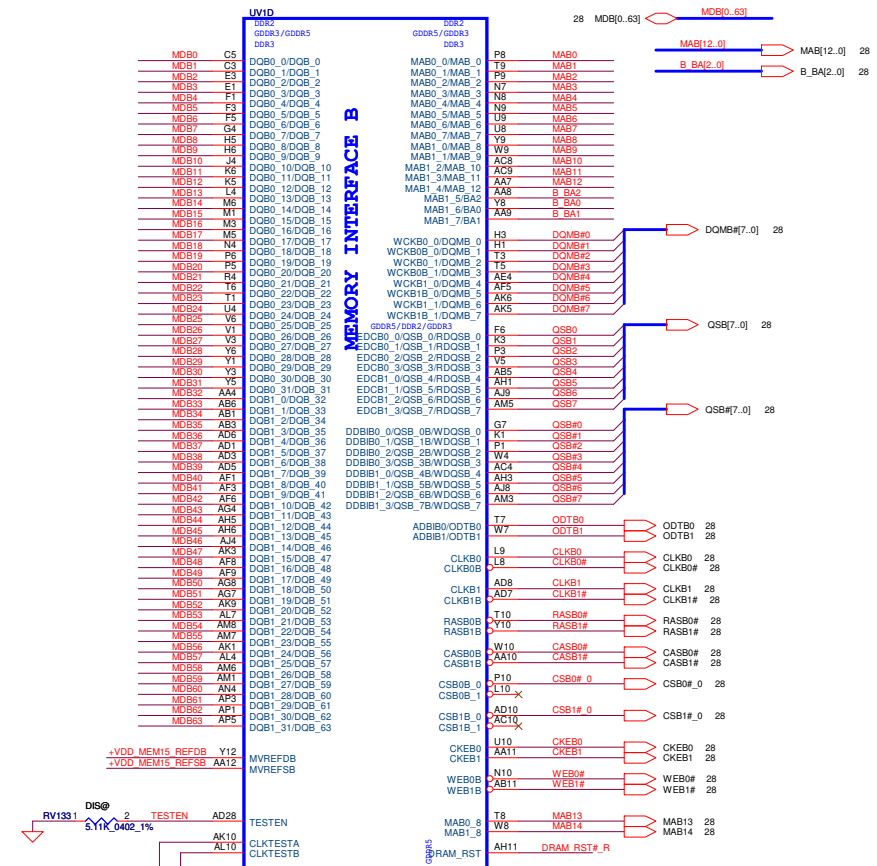
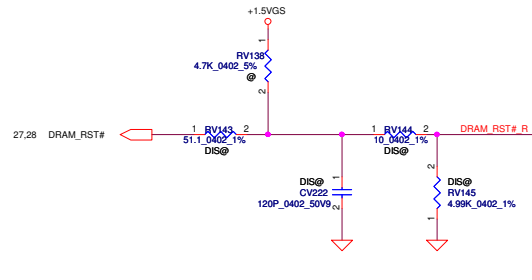
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Rev	1
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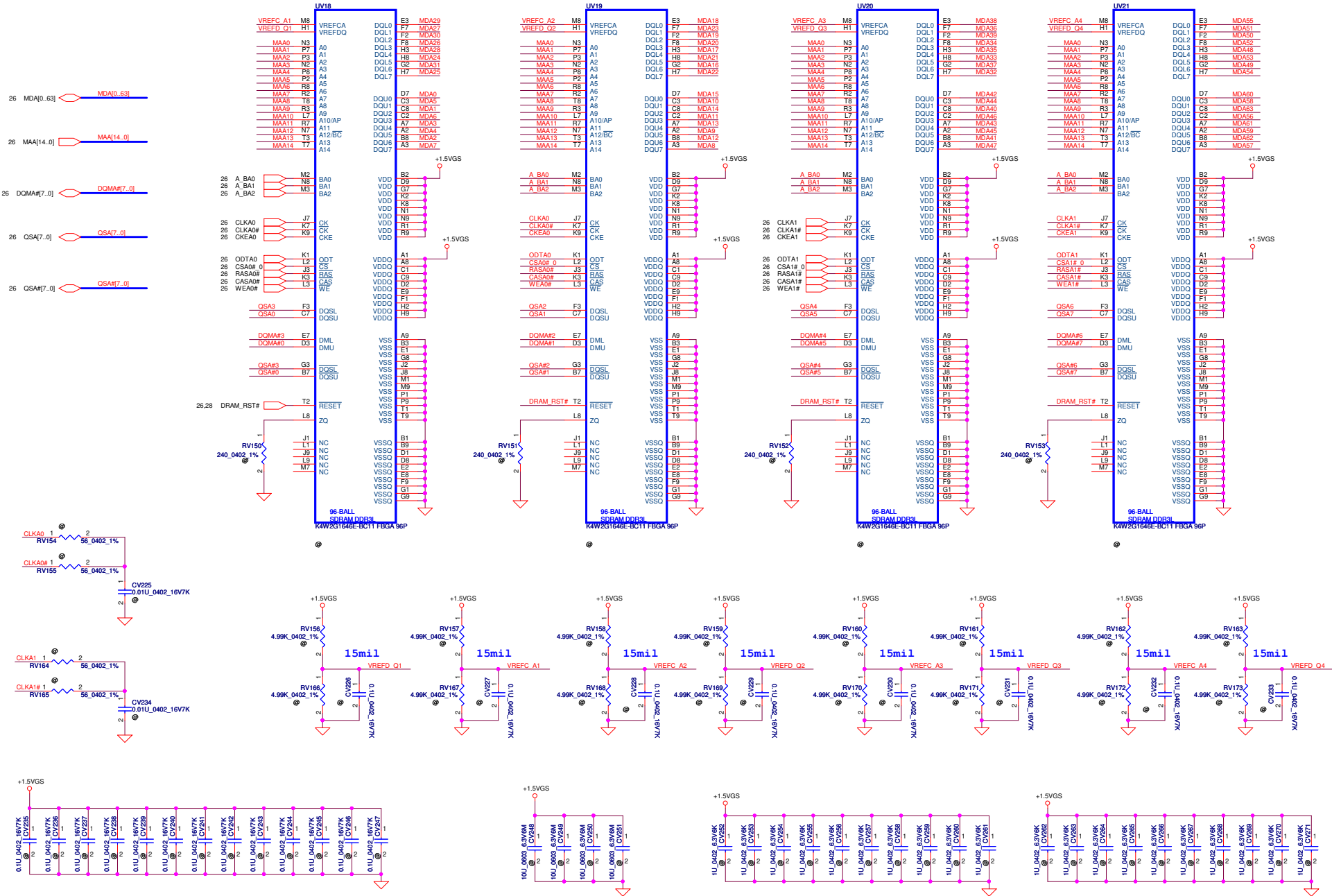
Co-lay Thames/Mars Pro/Chelsea

	Thames M2	Mars Pro	Chelsea M2
RV129	POP	@	@
RV130	@	@	@
RV131	POP	@	@
RV132	@	@	@
RV134	POP	@	@
RV135	POP	@	@
RV206	@	MARS@	@
RV205	@	@	POP

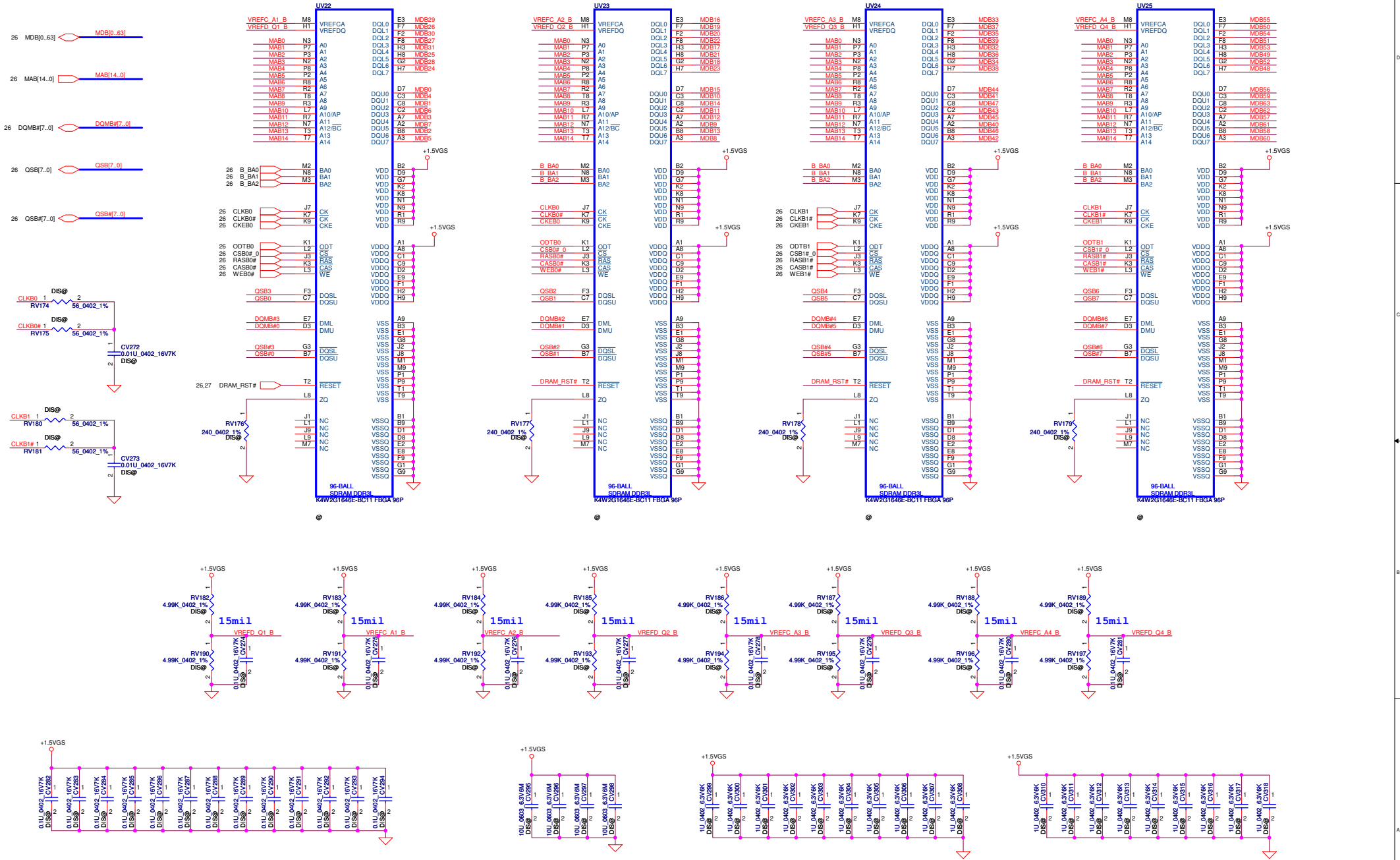
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and I Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

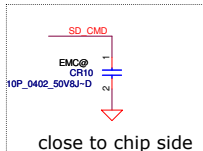
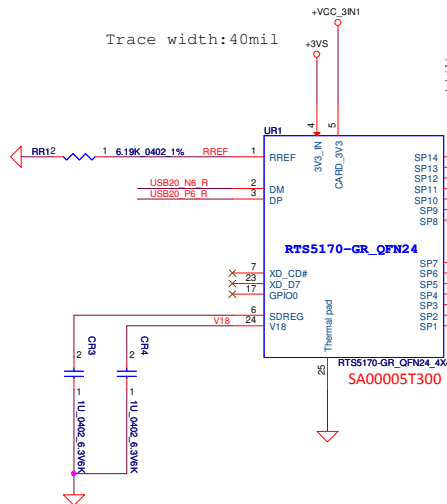
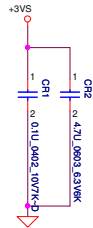
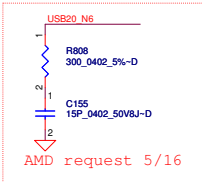
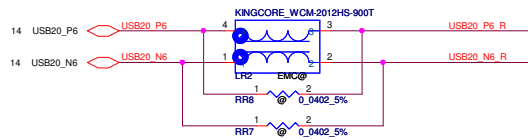


CHANNEL A: 256MB/512MB DDR3



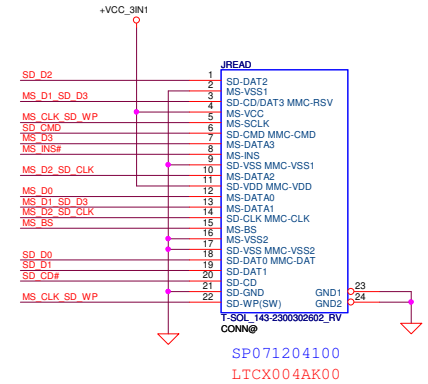
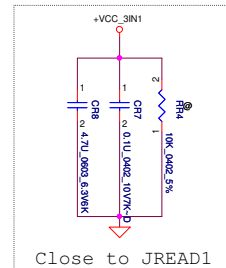
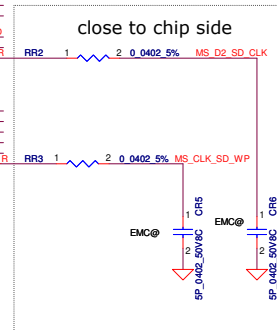
CHANNEL B: 256MB/512MB DDR3





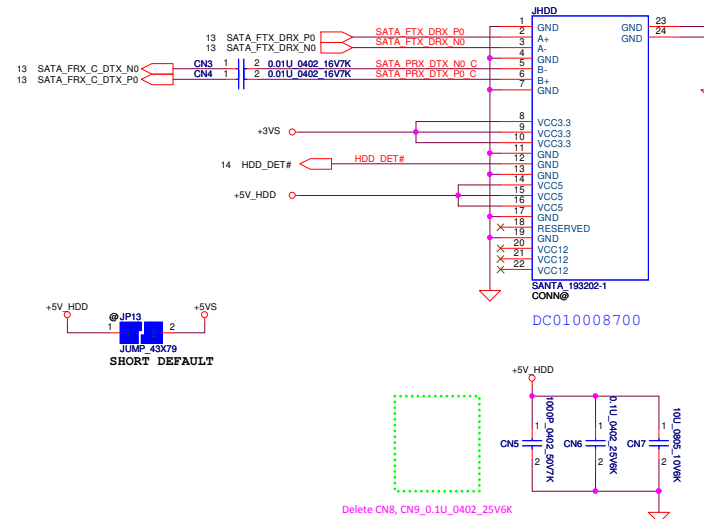
拉MS_D2_SD_CLK到Conn pin 14 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 22 SD_W



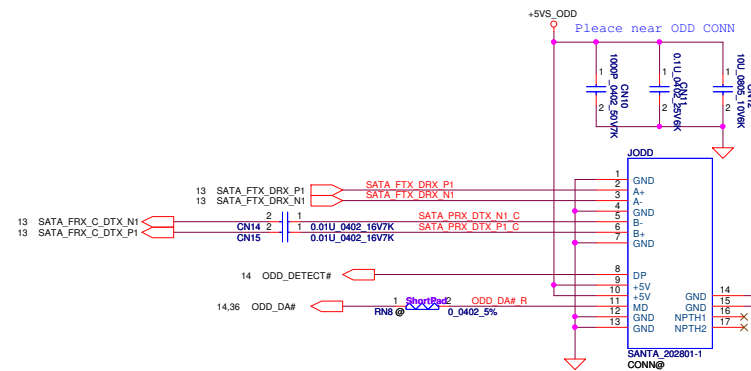
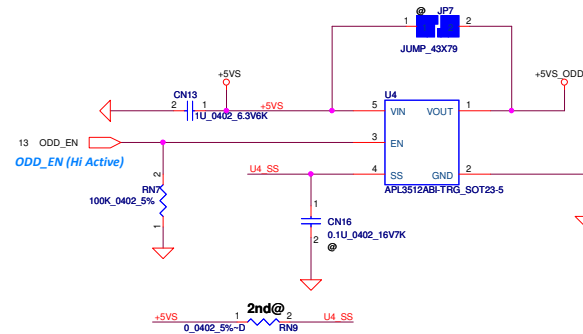
SATA HDD Conn.

+5V_HDD Source



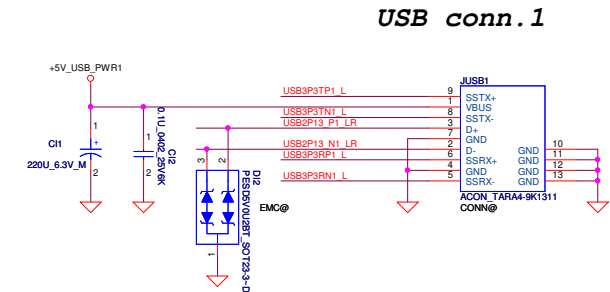
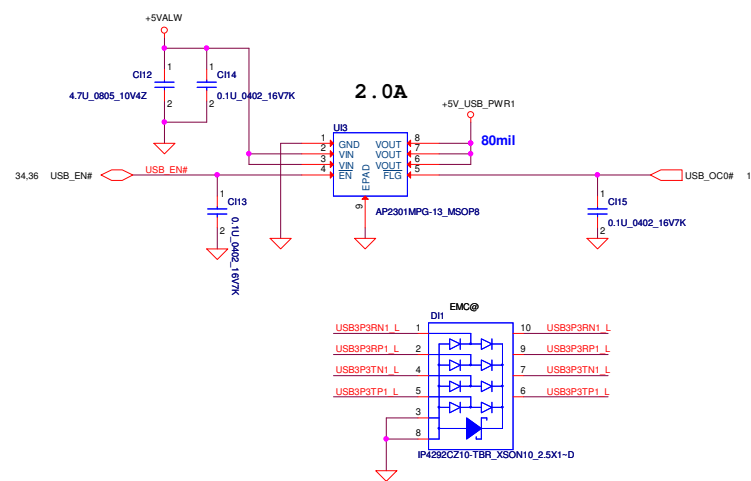
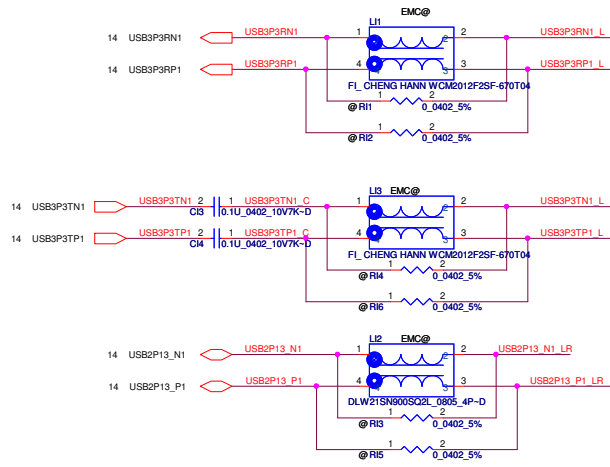
SATA ODD Conn.

ODD Power Control

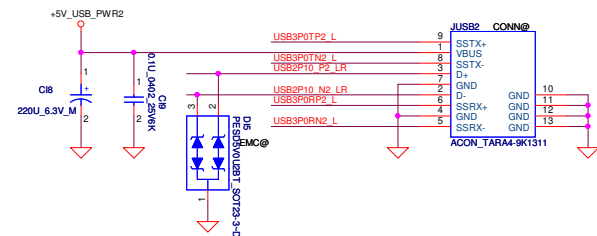
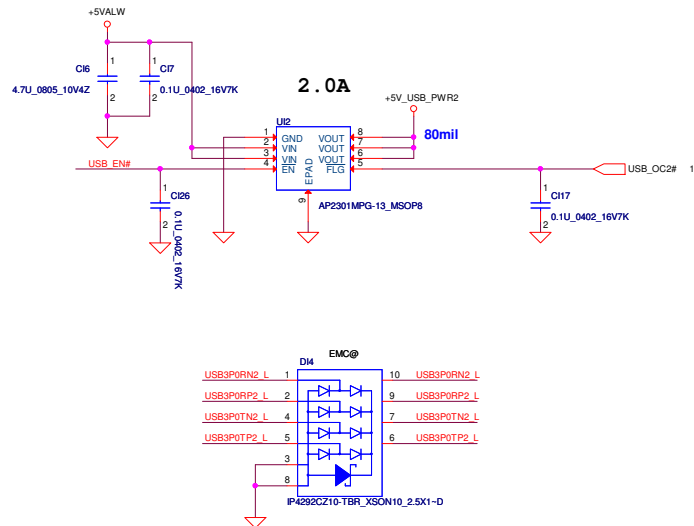
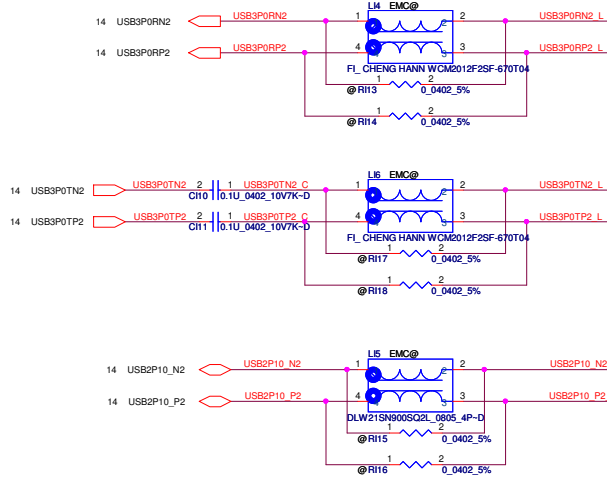


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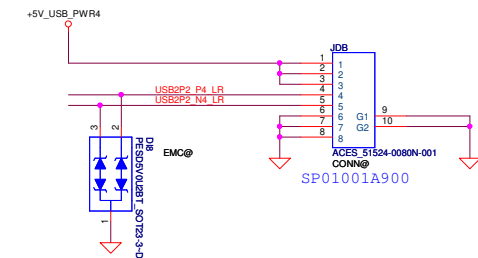
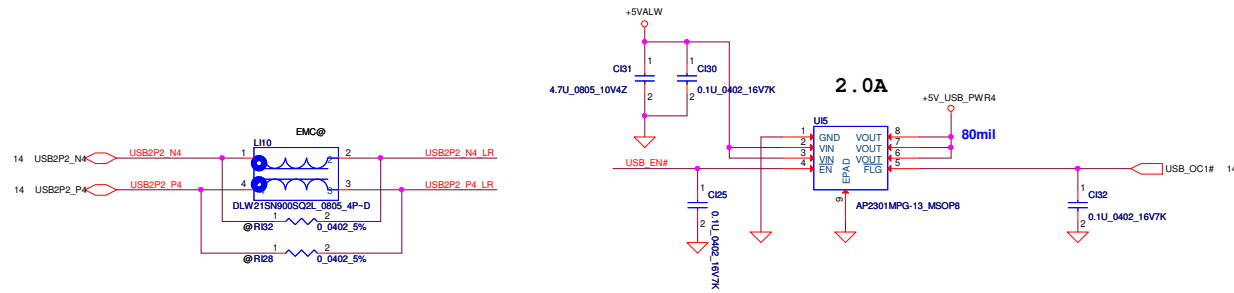
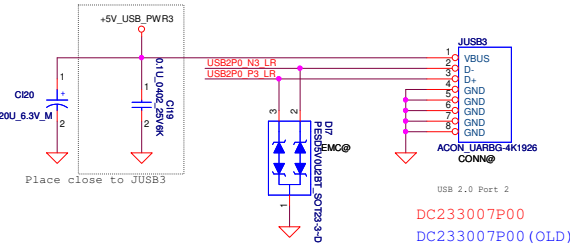
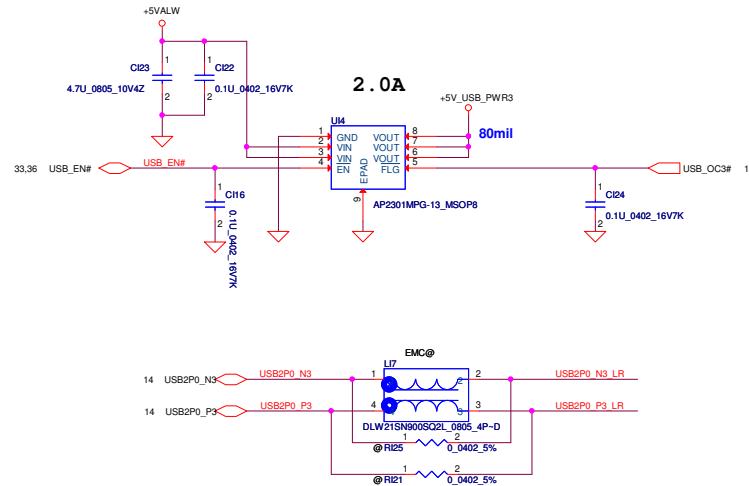
9/20 OAK Intel USB3.0 issue
 Change LI1, LI3, LI4, LI6 Part
 PN: from SM01002080L (\$ SUPPRE_ MURATA DLW21SN900SQ2L 0805)
 To SM070000580 (\$ COM FL_ CHENG HANN WCM2012F25F-670T04)



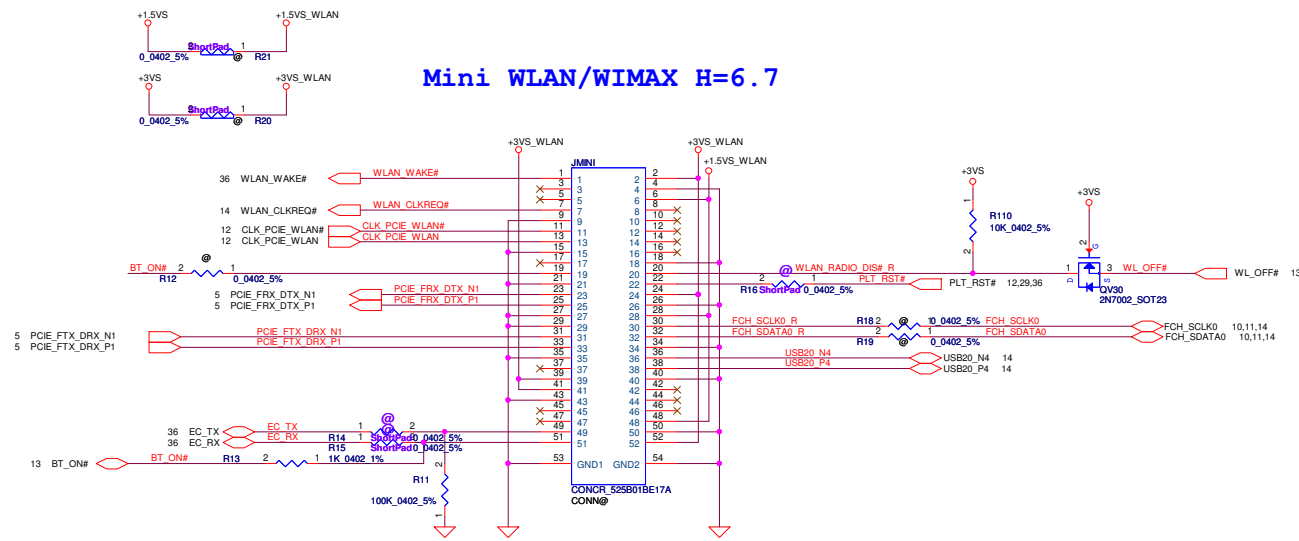
USB conn.1



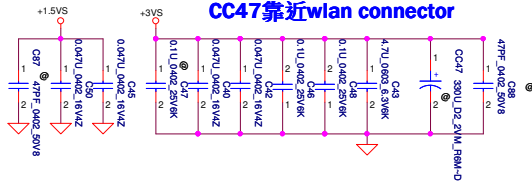
USB conn.2



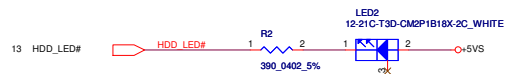
Security Classification		Compal Secret Data		Title	
Issued Date	2012/09/11	Deciphered Date	2014/03/12	MB to USB2.0 DB	
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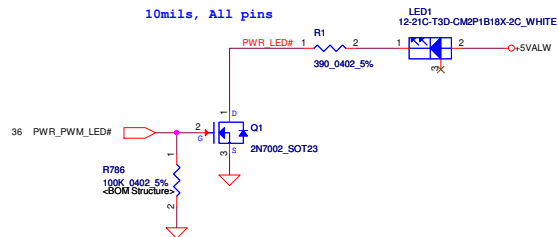
CC47靠近wlan connector



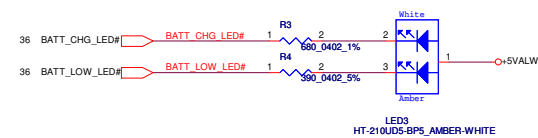
HDD LED



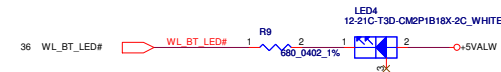
Power LED



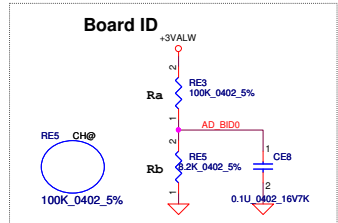
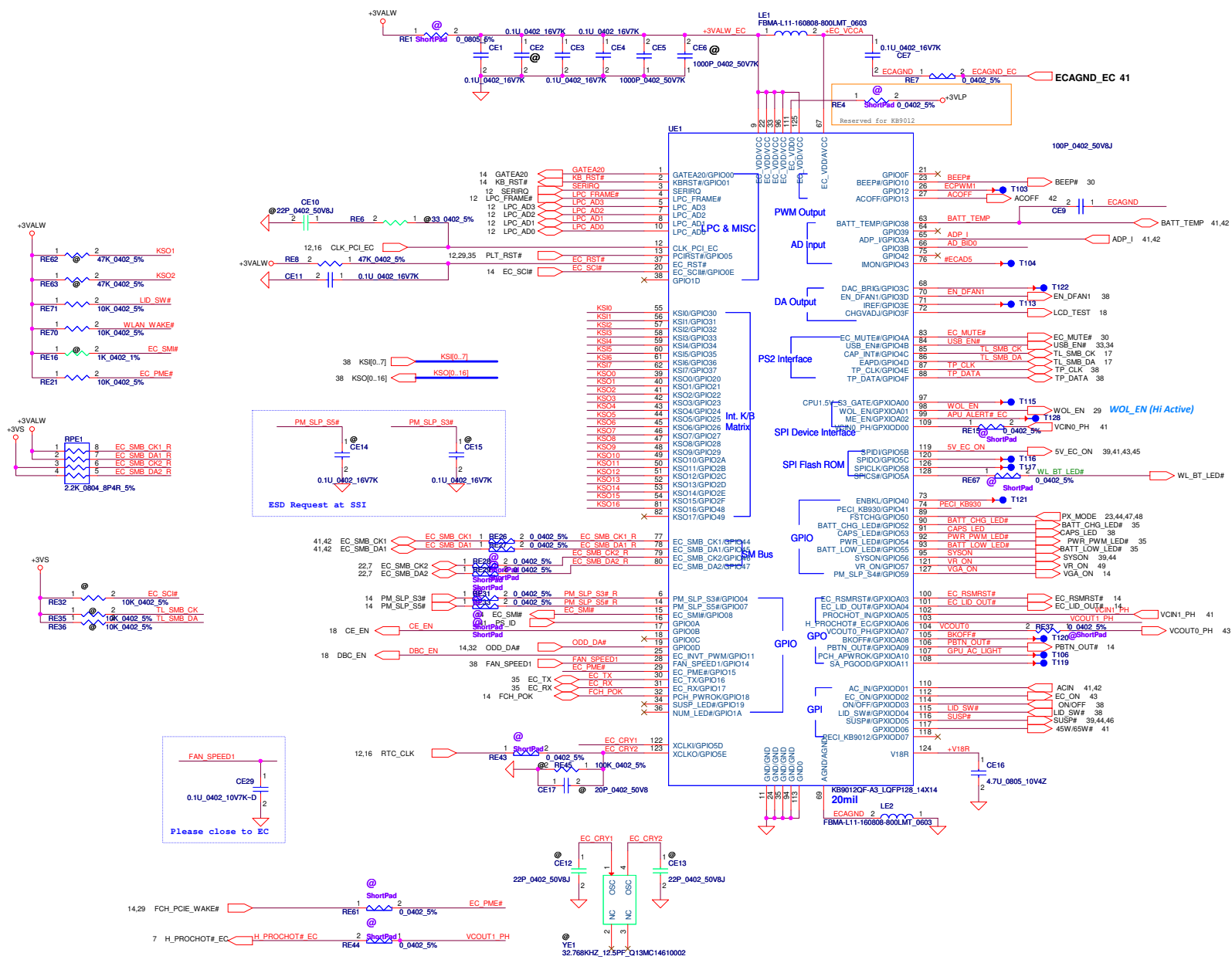
Battery LED



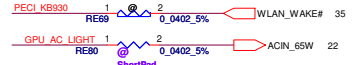
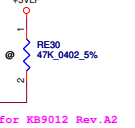
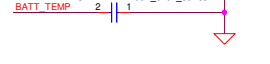
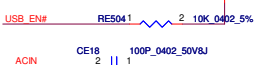
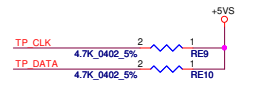
Wireless LED



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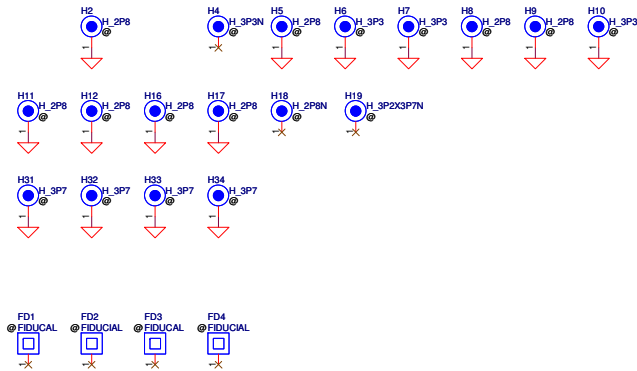


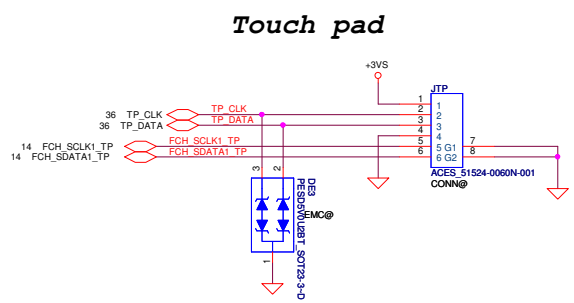
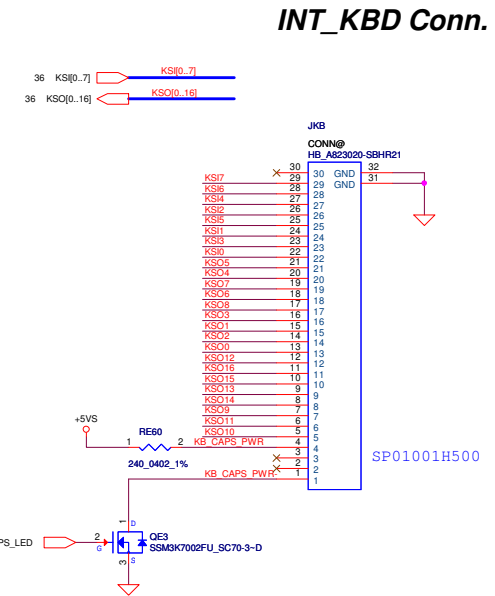
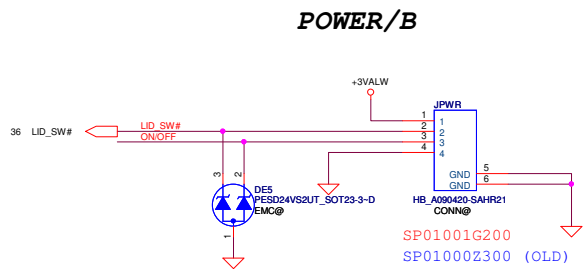
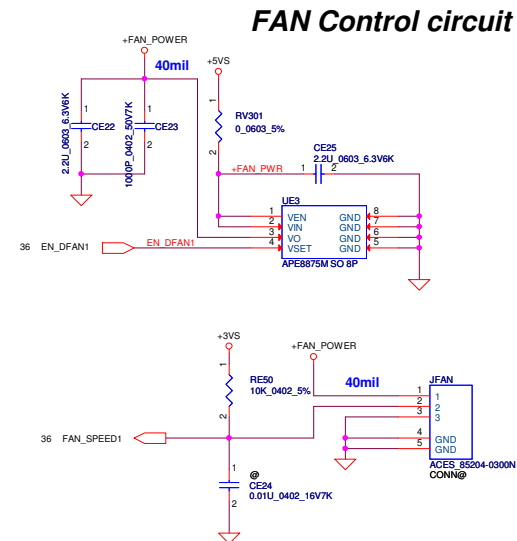
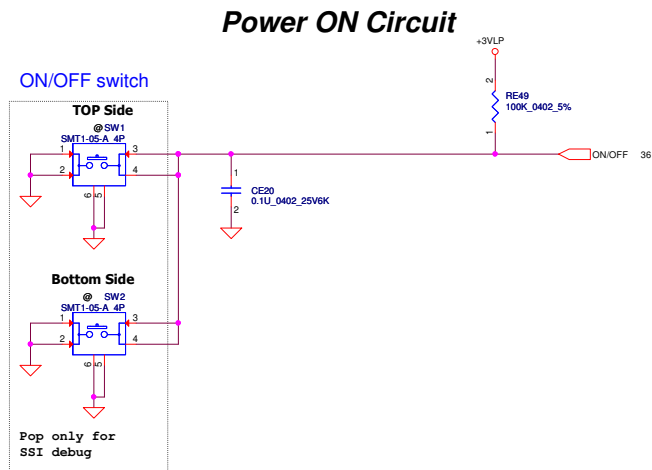
Analog Board ID definition,
Please see page 4.



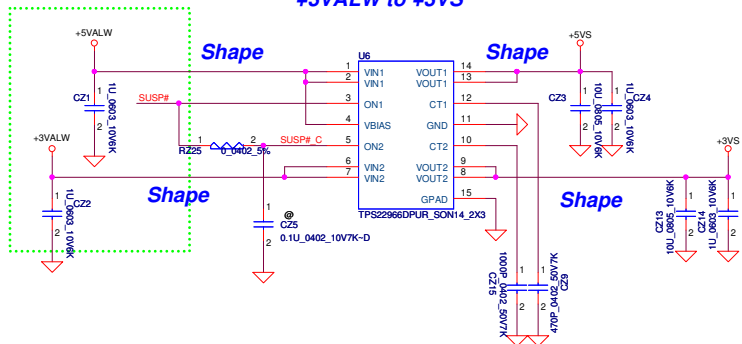
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Screw Hole

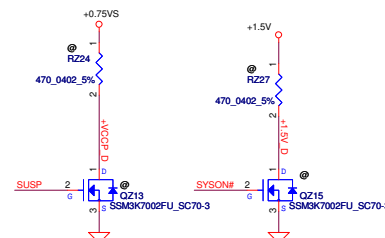
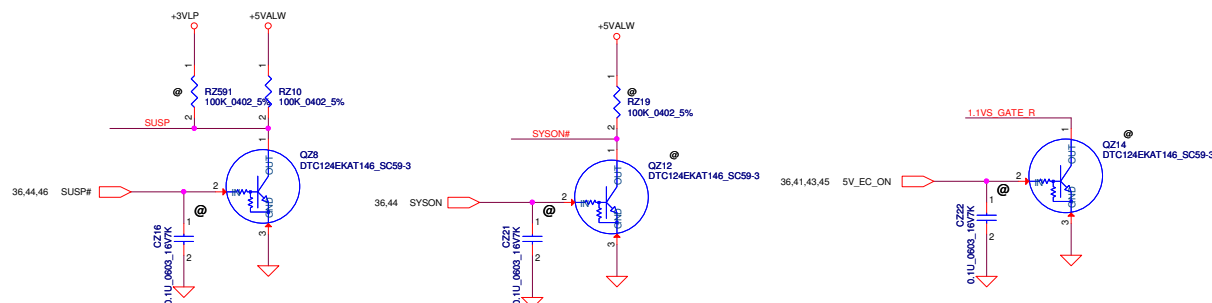
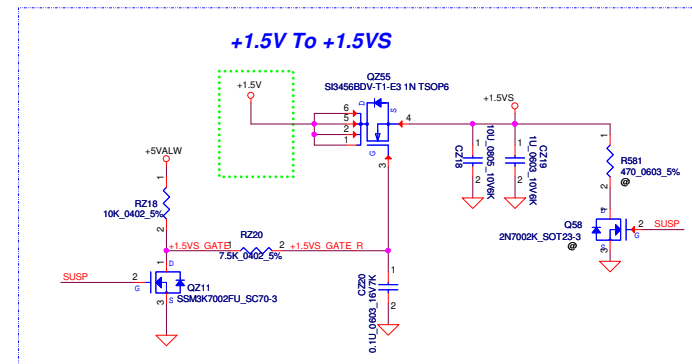
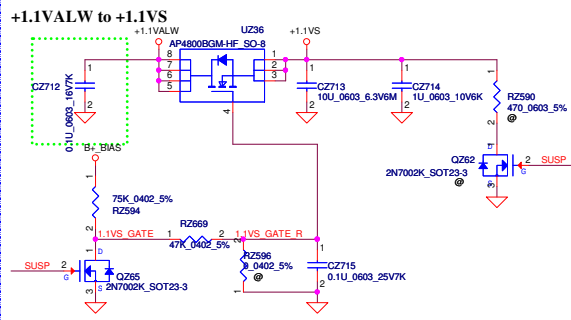




+5VALW to +5VS
+3VALW to +3VS

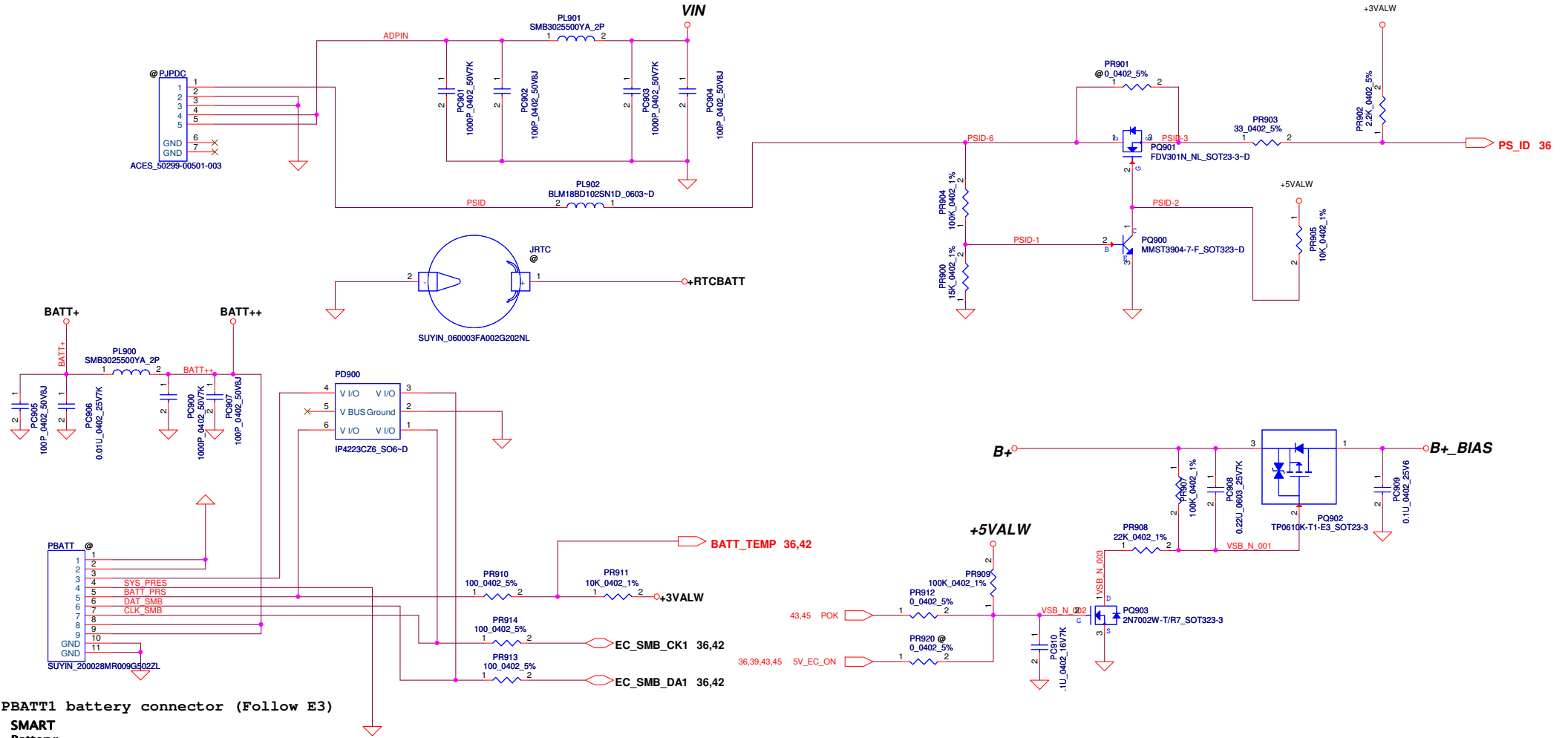


CTx (pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835



Page 1

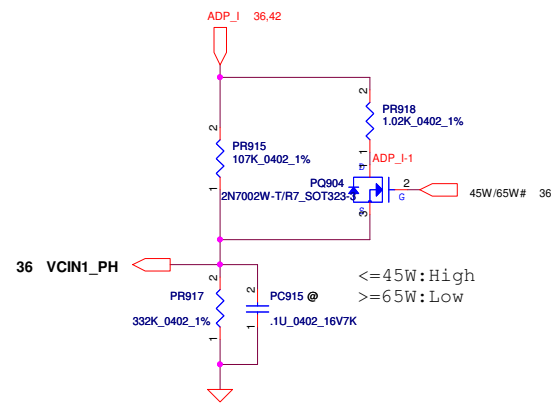
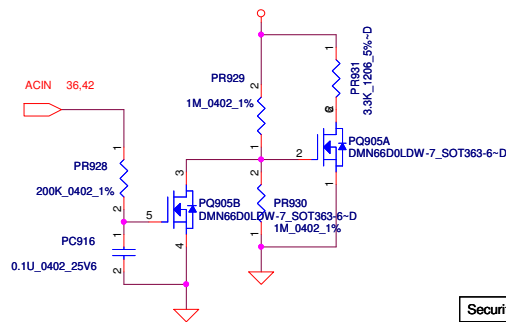
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	HW-PIR	
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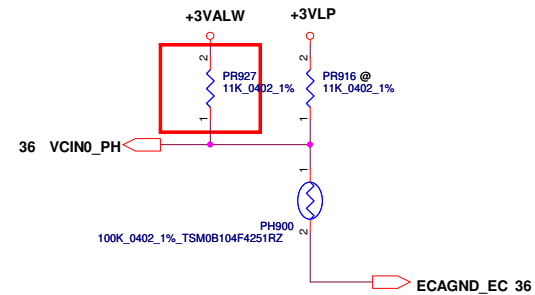
PBATT1 battery connector (Follow E3)

- SMART Battery:**
- 01.GND1
 - 02.GND2
 - 03.BAT_ALERT
 - 04.SYS_PRES
 - 05.BATT_PRS
 - 06.DAT_SMB
 - 07.CLK_SMB
 - 08.BATT1 +
 - 09.BATT2 +

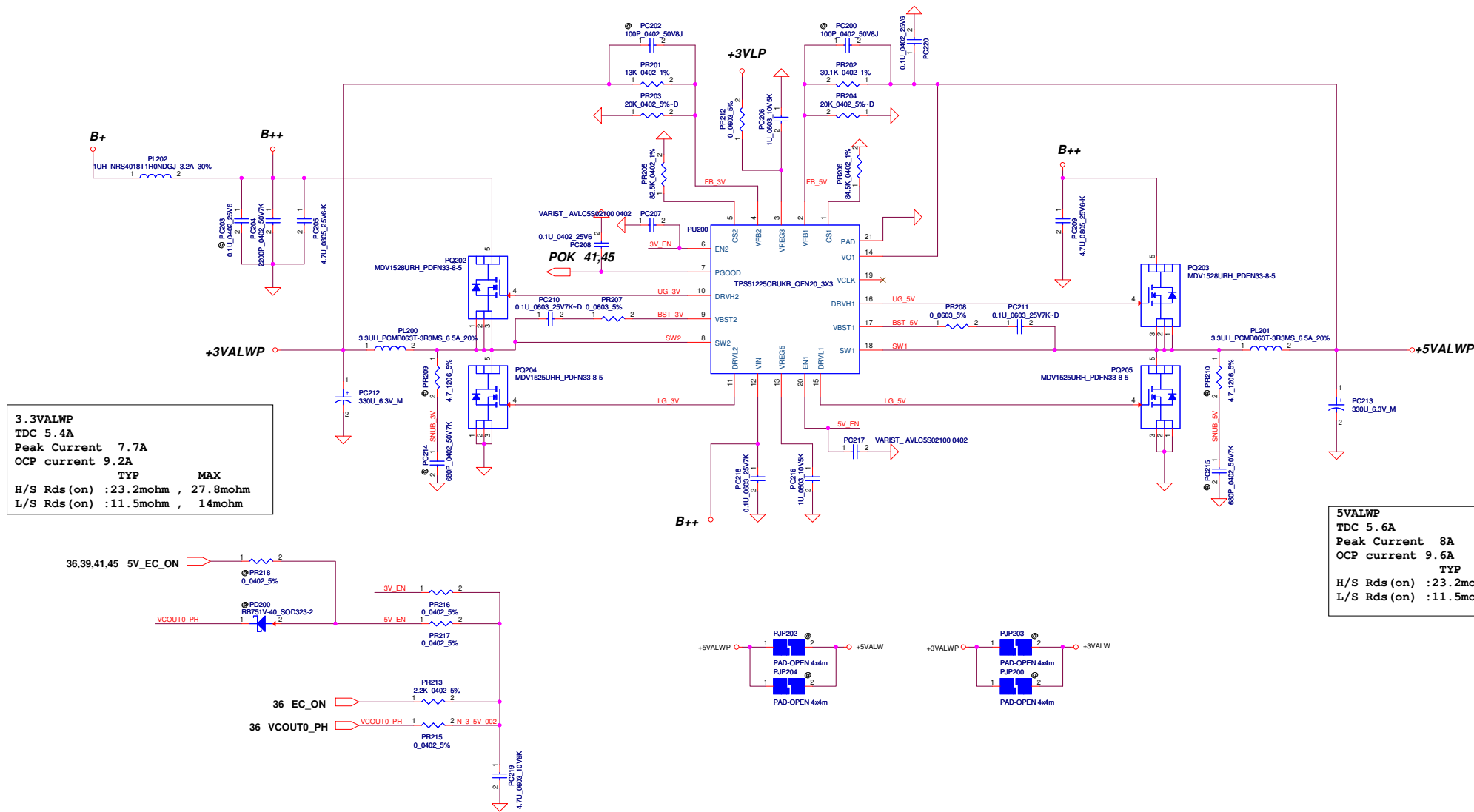
Exp lot6 Circuit



PH900 under CPU bottom side :
CPU thermal protection at 96 degree C



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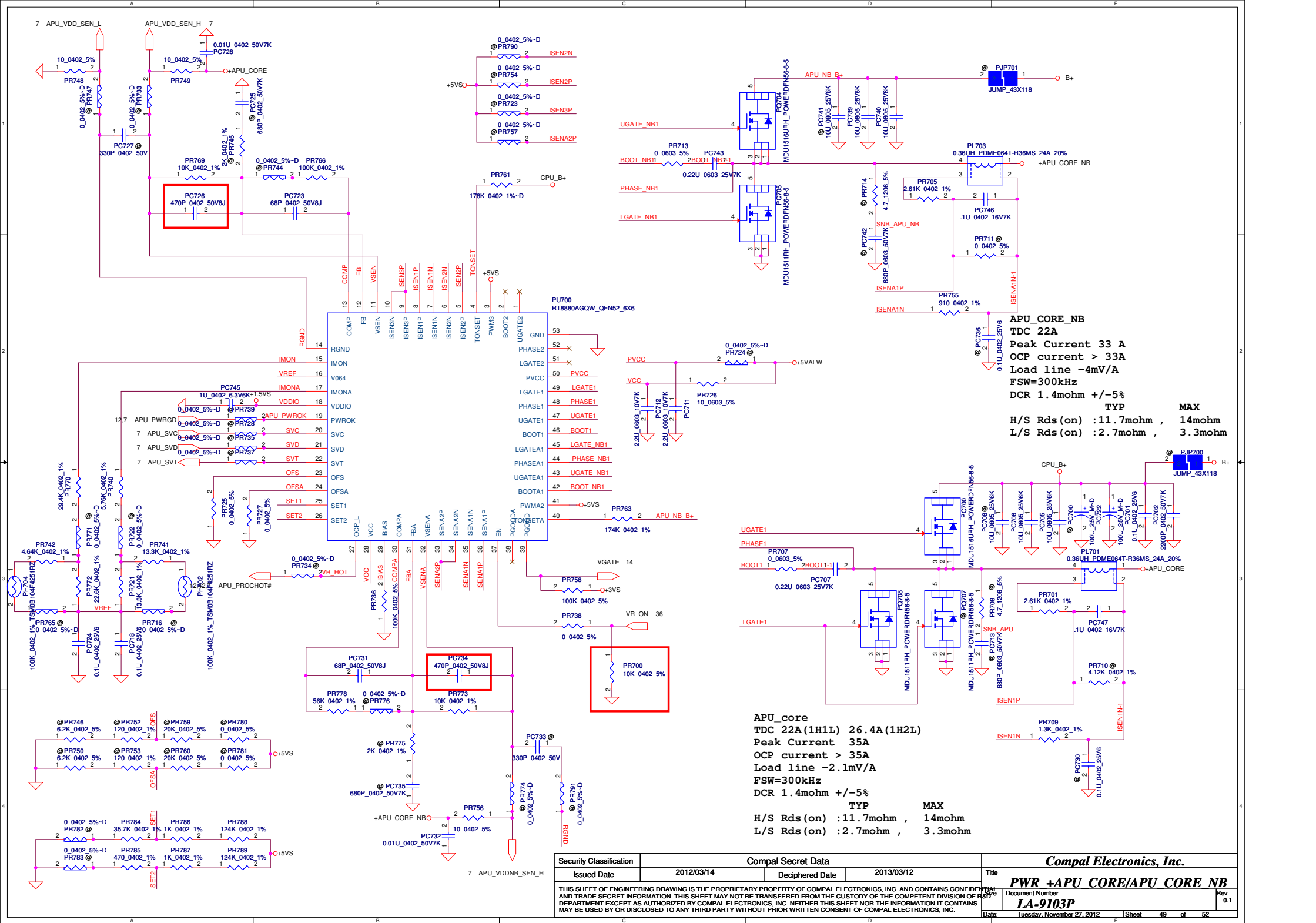


1.5VP
TDC 11A
Peak Current 16A
OCP current 19A

	TYP	MAX
H/S Rds (on)	: 23.2mohm	27.8mohm
L/S Rds (on)	: 7mohm	8.4mohm

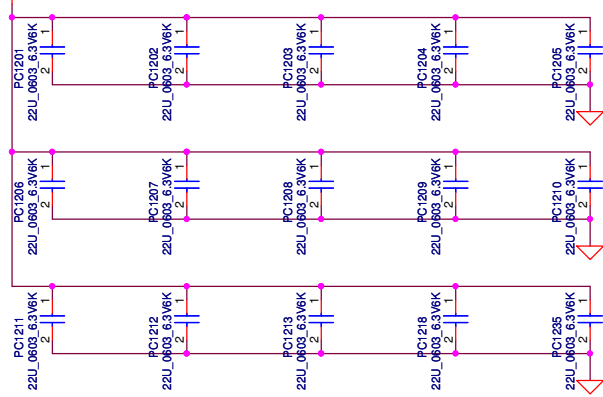
0.75VSP
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

+1.5VGPU
TDC 5.6A
Peak Current 8A
OCP current 9.6A

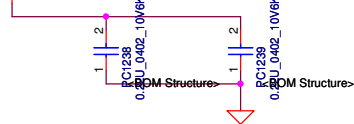


+APU_CORE

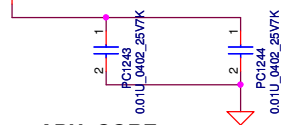
+APU_CORE



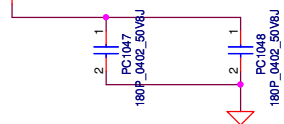
+APU_CORE



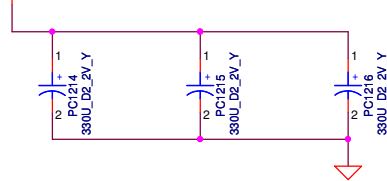
+APU_CORE



+APU_CORE

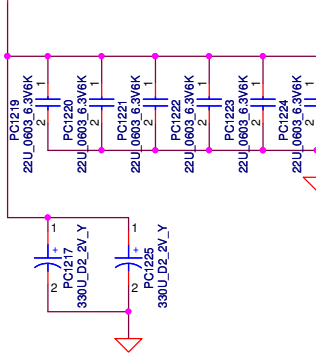


+APU_CORE



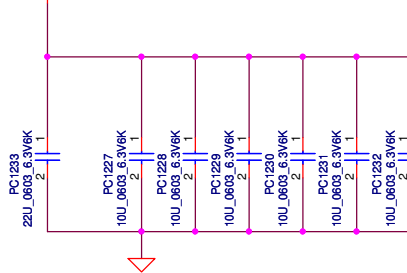
+APU_CORE_NB

+APU_CORE_NB



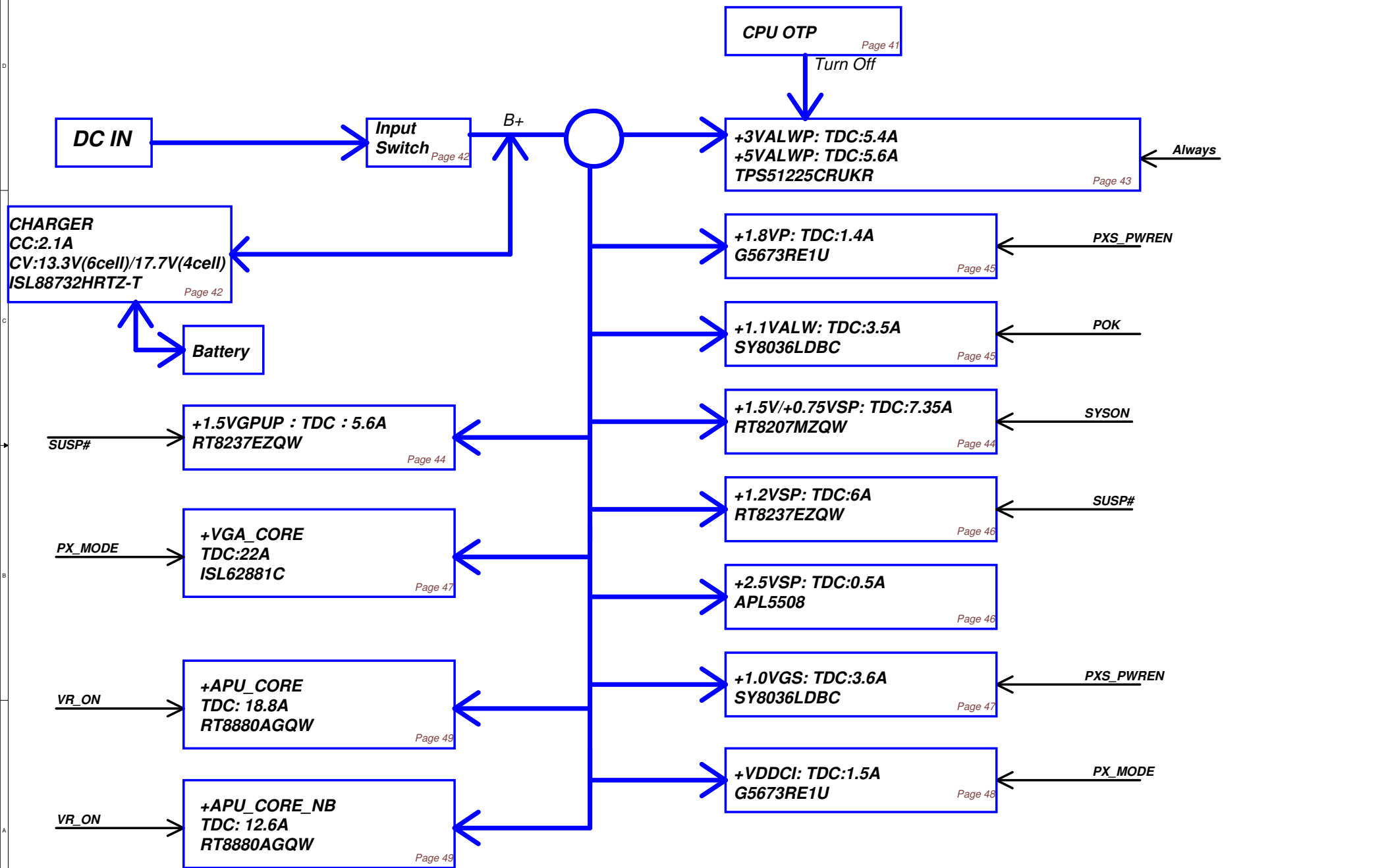
+1.2VS

+1.2VS



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Power block



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