Compal Confidential

Model Name : ZIPS1

File Name : LA-A341P

BOM P/N:

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Stella M/B Schematics Document

Intel Shark Bay ULT Processor with DDR3L

Rev. 1A_20130902A

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Issued Date	2013/03/08	Deciphered Date	2015/03/08

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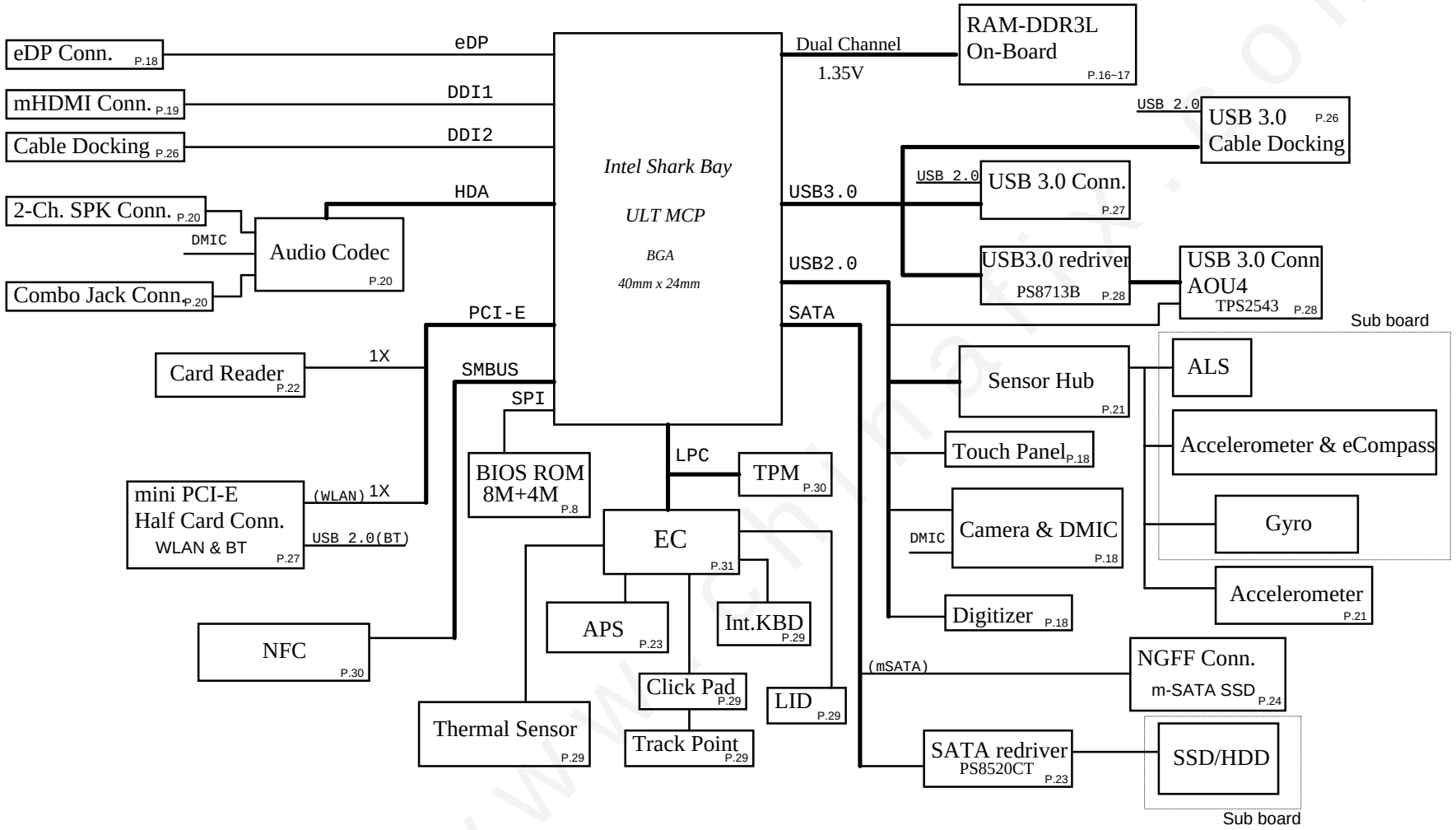
Model Name : ST-Note
File Name : Block Diagram



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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +0.675VS +1.05VS	+3VM +1.05VM
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only (AOU Disable)	X	X	X	X	
S5 S4/AC & Battery don't exist (AOU Disable)	X	X	X	X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
EMI Mount	EMI@
dGPU	DIS@
Intel UMA	UMA@
AOAC	AOAC@
TPM	TPM@
SBA	SBA@
Non-SBA	NOSBA@
DRAM Option	DDR1@
Unpop	@
EMI Un-Mount	@EMI@

USB 2.0 Port Table

	USB 2.0	Port	3 External USB Port
		0	USB 3.0 Port + AOU (Left)
		1	USB 3.0 Port (Right)
		2	USB 3.0 Port (Docking)
		3	Mini Card (WLAN/BT)
		4	Touch Screen
		5	Camera
		6	Sensor Hub
		7	Digitizer

USB 3.0 Port Table

Port	
1	USB 3.0 Port (Left)
2	USB 3.0 Port (Right)
3	USB 3.0 Port (Docking)
4	

PCIE Port Table

Port	Lane	
1		
2		
3		WLAN
4		Cardreader
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

SATA Port Table

Port	
0	HDD
1	NGFF SSD
2	
3	

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H
Charger	0001 011X b	12H

EC SM Bus2 address

Device	Address	HEX
Thermal Sensor Fintek F75303M	1001_101xb	9AH
Synaptics Inter Touch Click Pad	0010_110xb	2CH

PCH SM Bus address

Device	Address	HEX
Security Rom	1010 100xb	A8H

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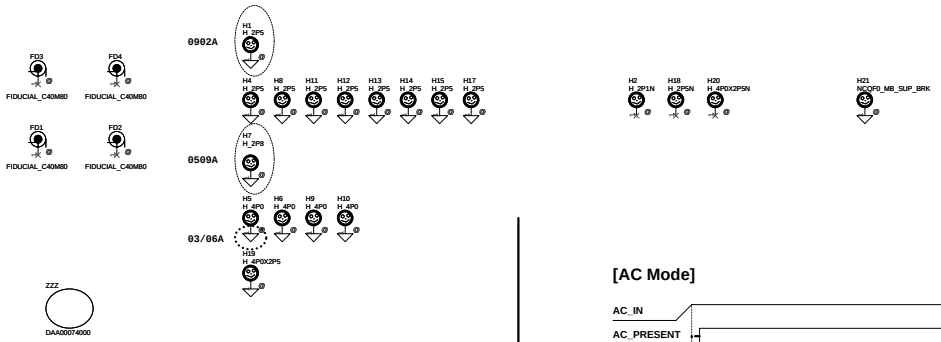
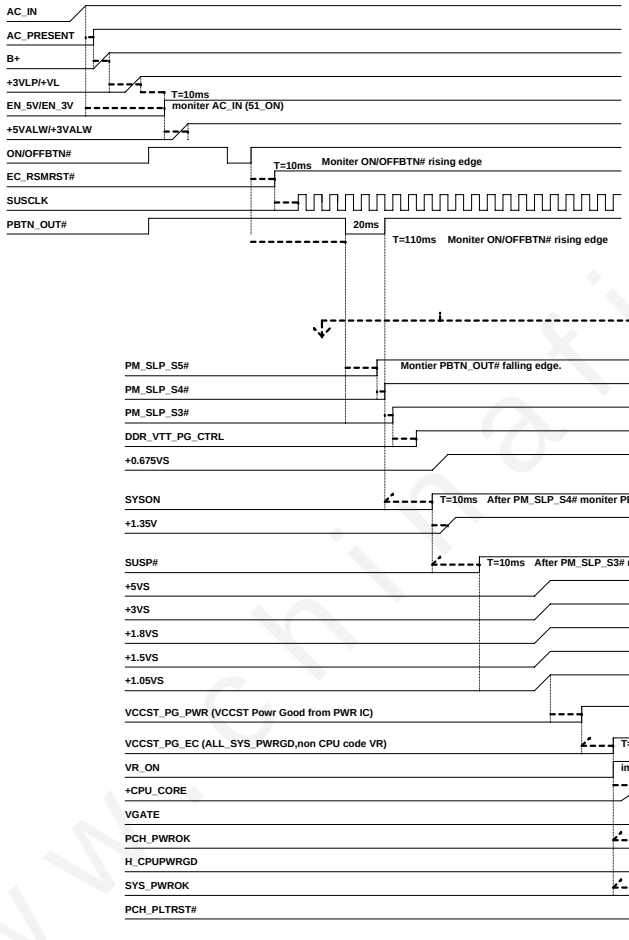


RAM_ID3 GPIO46	RAM_ID2 GPIO47	RAM_ID1 GPIO48	RAM_ID0 GPIO49	RAM
0	0	0	0	HYNIX 4GB
0	0	0	1	SAMSUNG 4GB
0	0	1	0	MICRON 4GB
0	0	1	1	ELPIDA 4GB
0	1	0	0	SAMSUNG 8GB
0	1	0	1	ELPIDA 8GB
0	1	1	0	MICRON 8GB
0	1	1	1	HYNIX 8GB
1	0	0	0	TBD
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD

[AC Mode]



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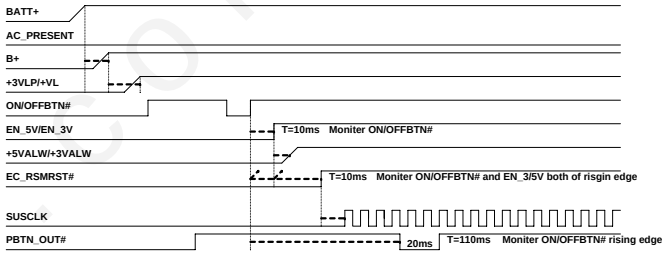

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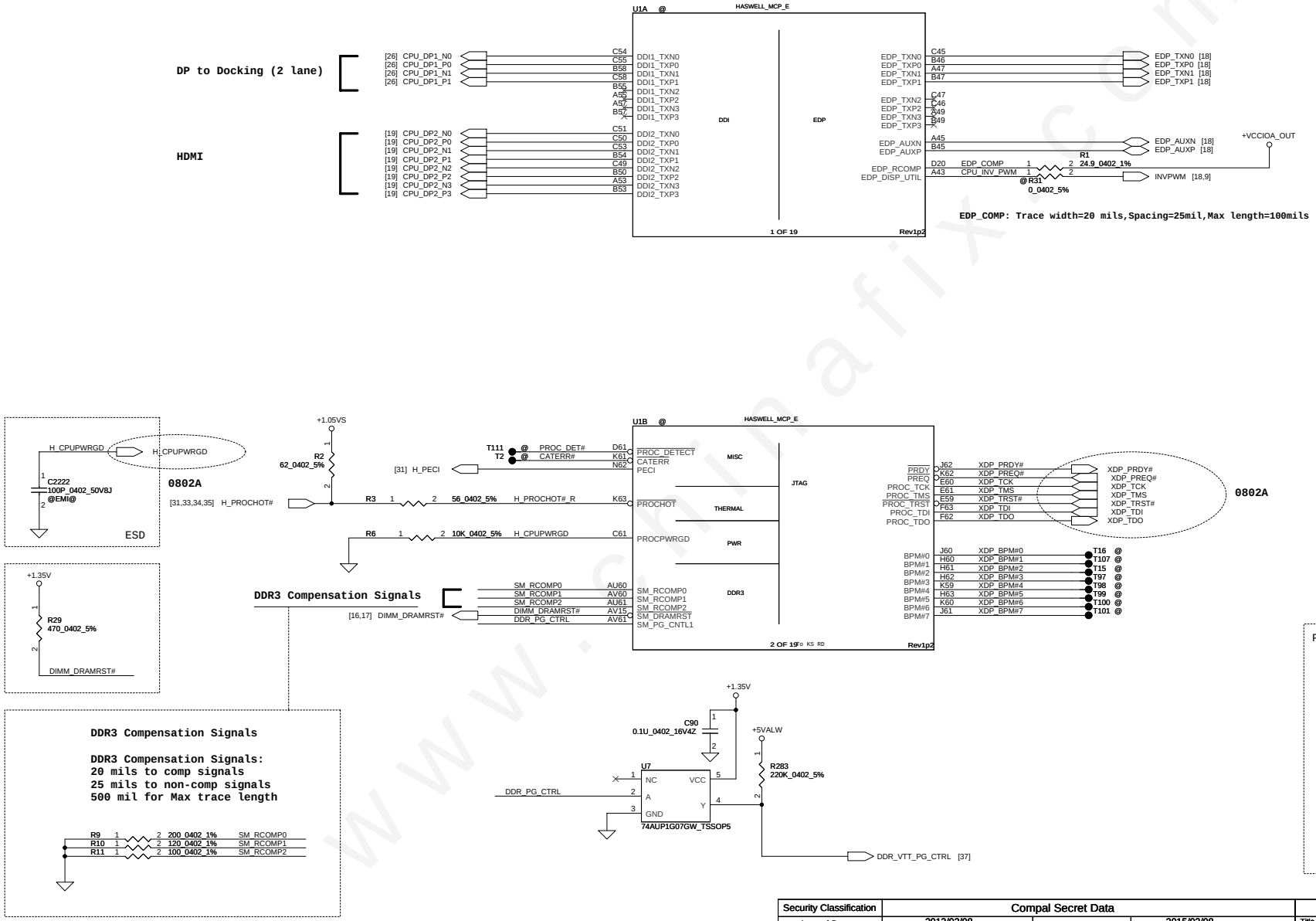
DDI/ MSIC/ XDP



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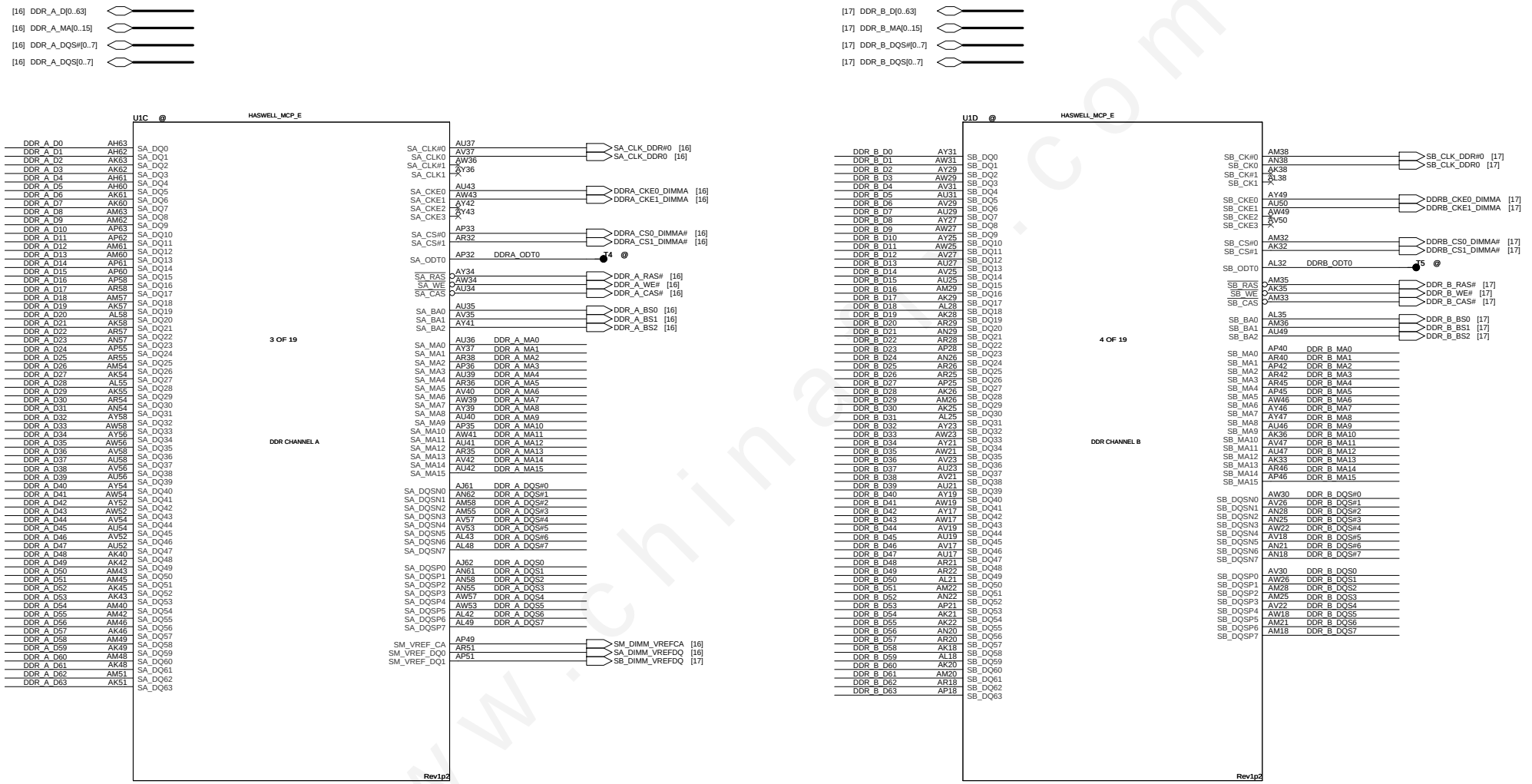
Memory I/F



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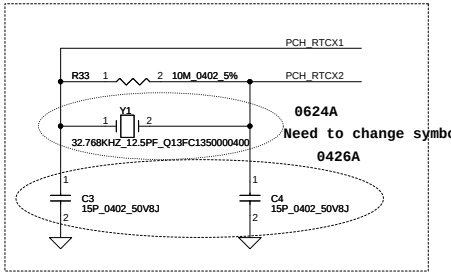
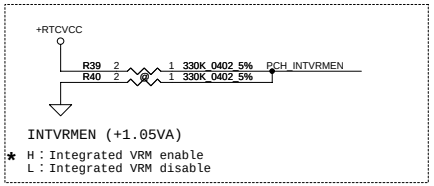
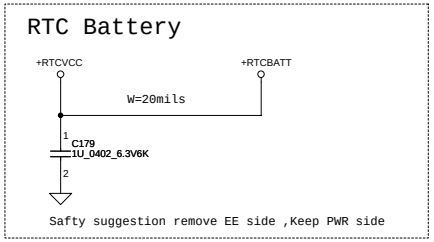
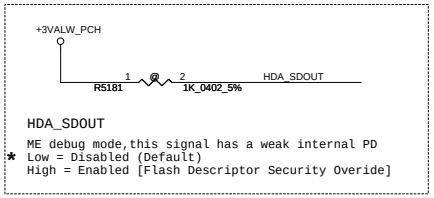
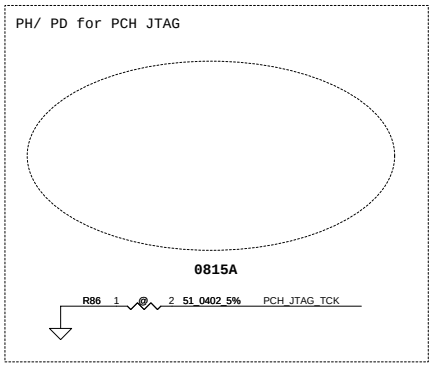
RTC/ SATA/ XDP

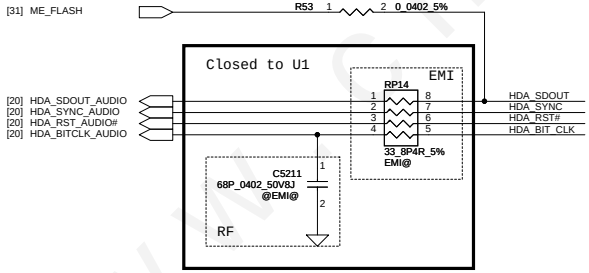


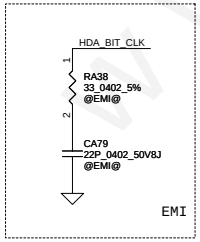












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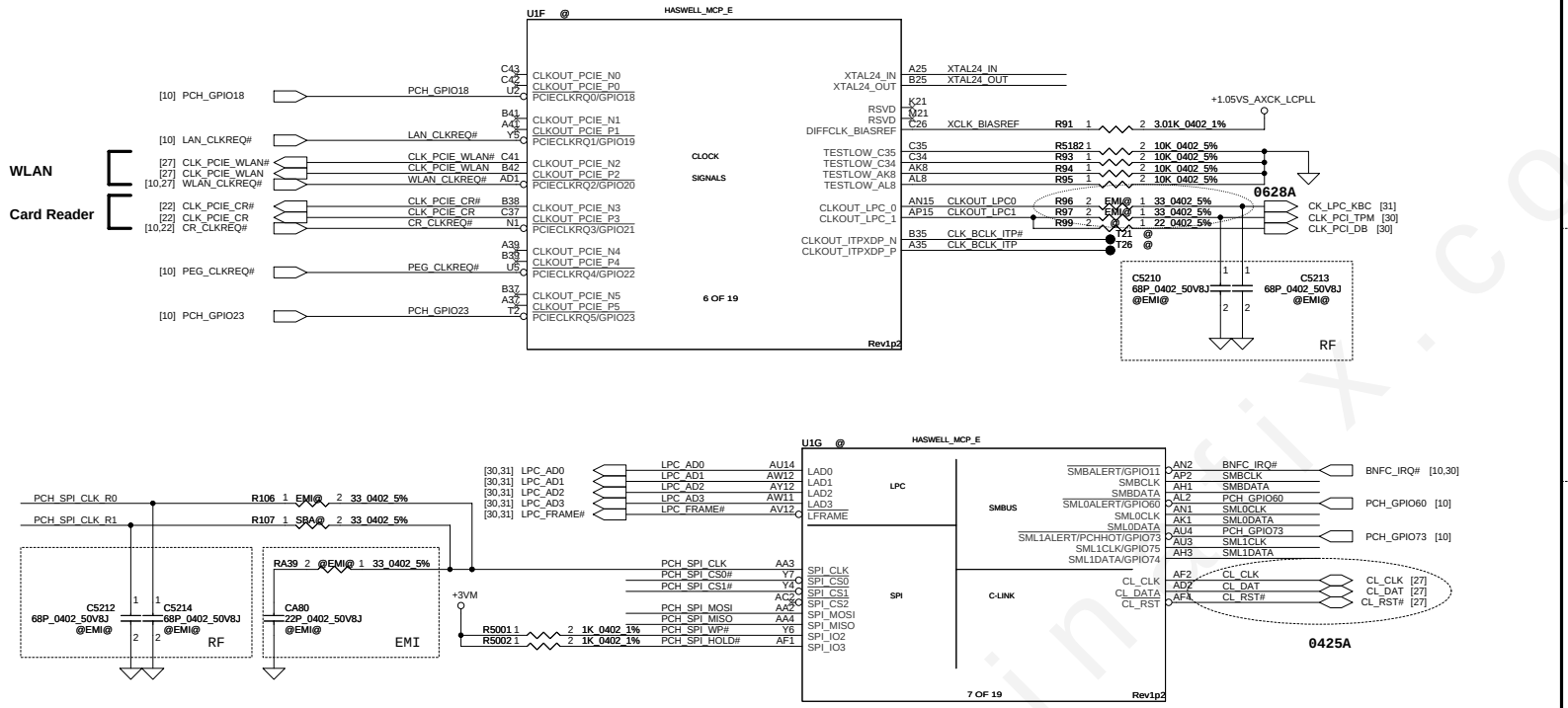
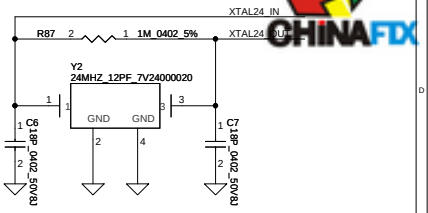
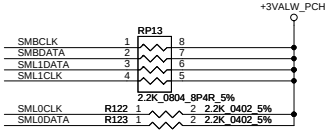
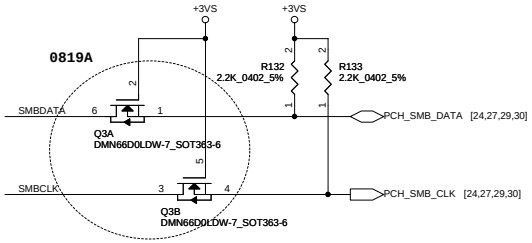
CLK/ SPI/ SMBUS





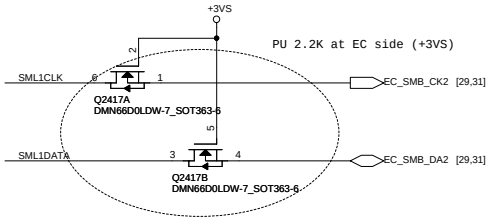


SMBus :SPD/PCIe/Security/TP/NFC



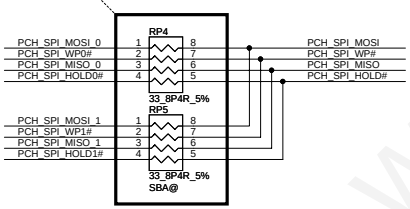
Change Symbol

SML1 Bus :EC/Sensors

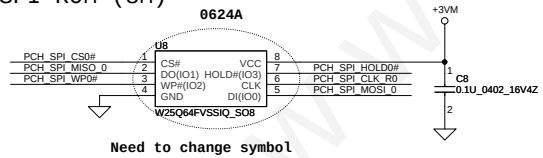


Change Symbol 0819A

SBA - 2 SPI Device = 33 ohm - P/N: SD309330A80
Non-SBA - 1 SPI Device = 15 ohm - P/N: SD300001P00



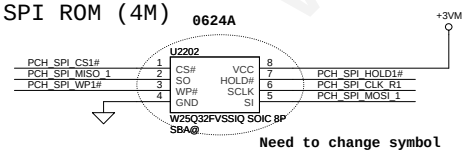
SPI ROM (8M)



Need to change symbol

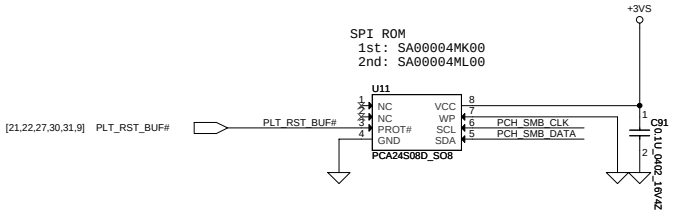
SPI ROM 8MB
1st: SA000039A30 - Winbond
2nd: SA000046400 - E-ON
SPI ROM 4MB
1st: SA00003K820 - Winbond
2nd: SA00004LI00 - E-ON

SPI ROM (4M)



Need to change symbol

Security ROM



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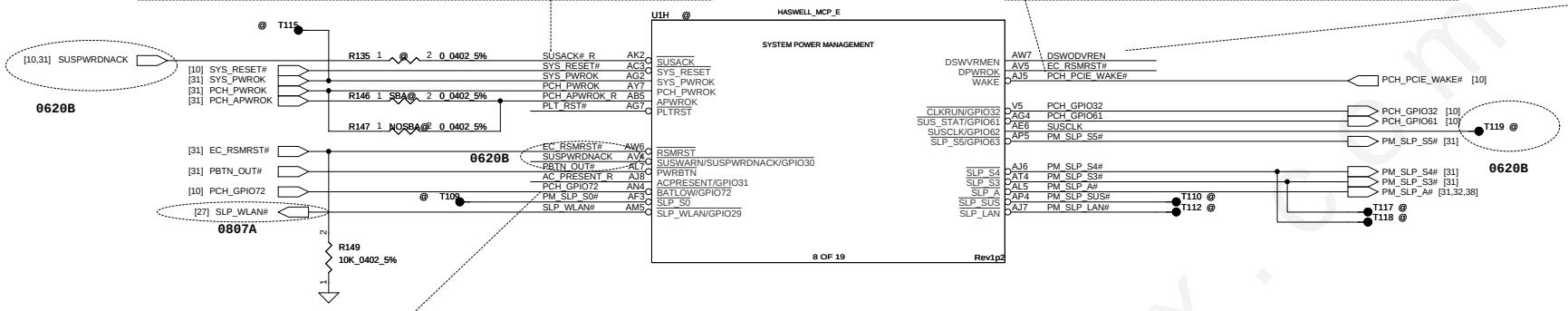
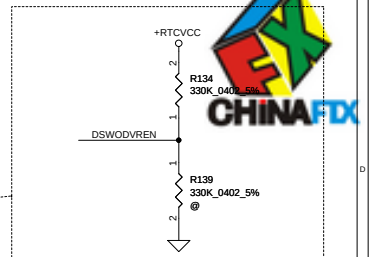
PM/ GPIO/ DDI

Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.
CAN be NC ,if not support Deep Sx

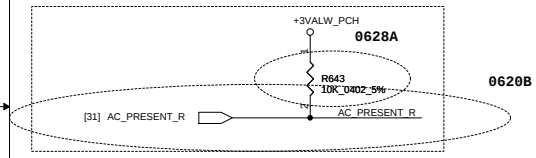
DPWROK: Tired toghter with RSMRST# that do not support Deep Sx

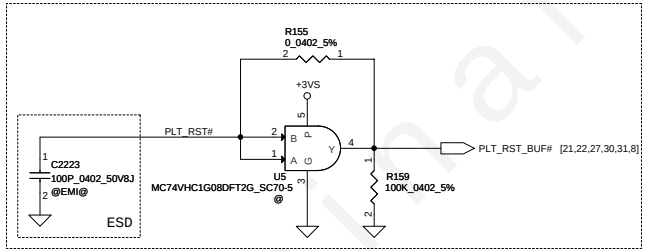


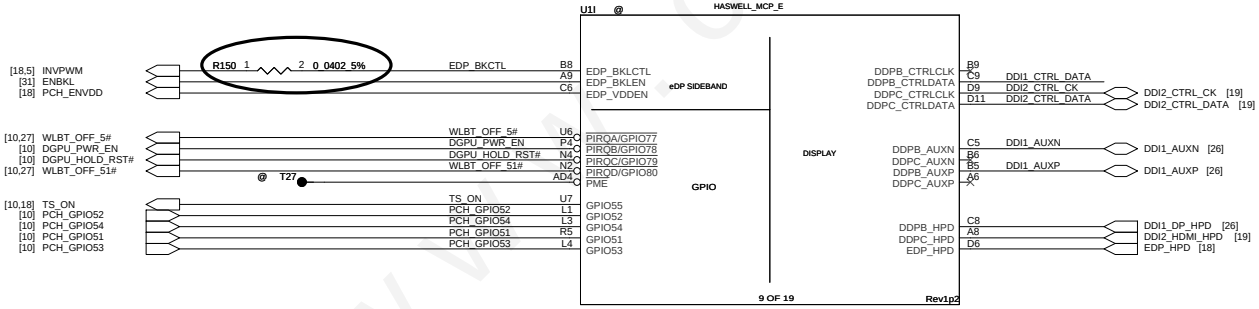


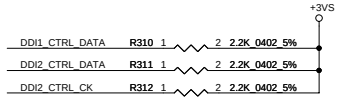
DSWODVREN - On Die DSW VR Enable
* H : Enable (default)
L : Disable

PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx , connect to VCCSUS3_3)









DDPB_CTRLDATA: Port B Detected
DDPC_CTRLDATA: Port C Detected
* 1: Port B or C is detected
0: Port B or C is not detected
Port have internal PD

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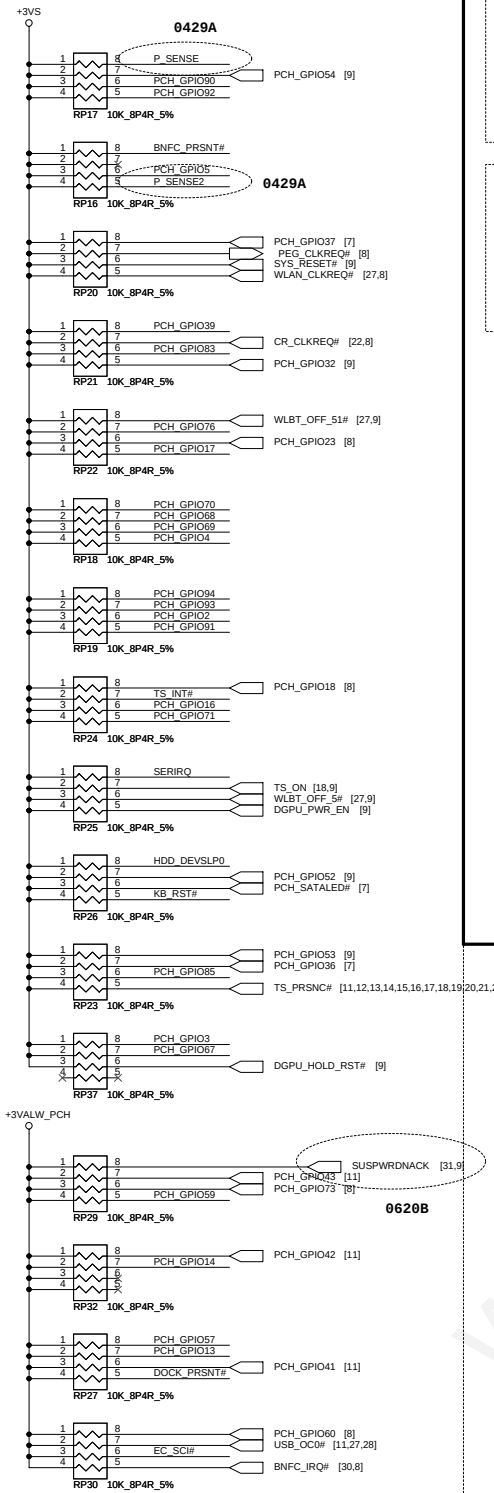
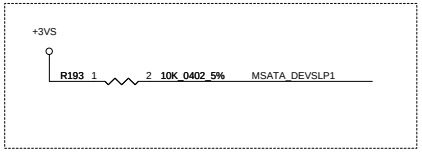
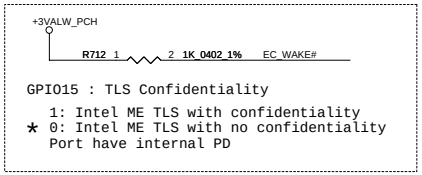
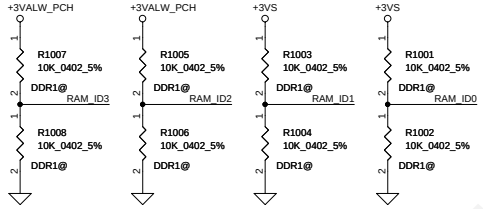
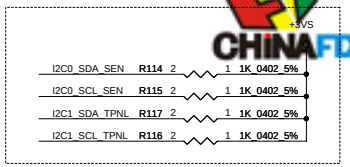
GPIO/ LPIO

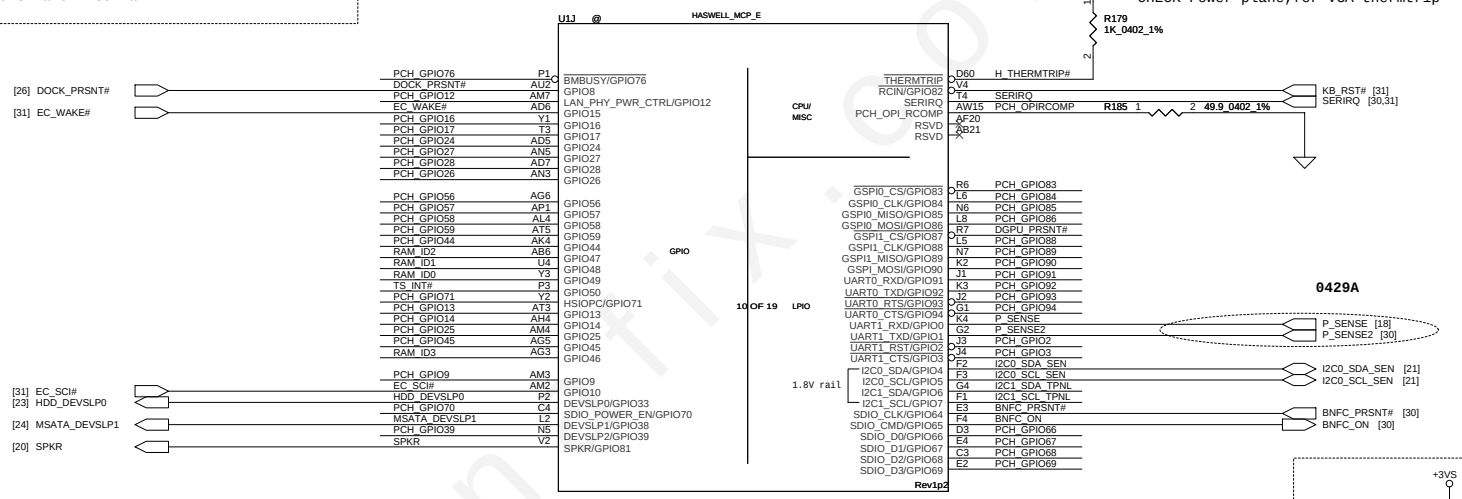


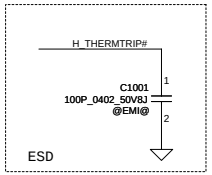


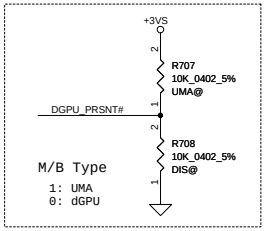


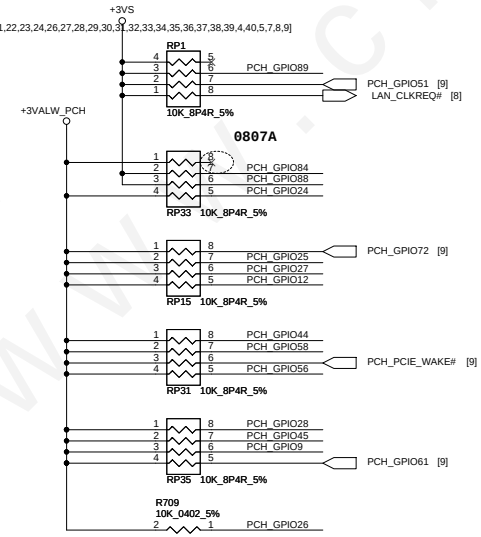




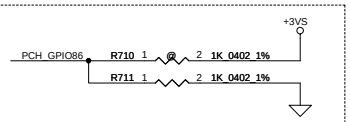


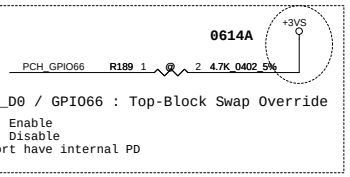






RAM_ID3 GPIO46	RAM_ID2 GPIO47	RAM_ID1 GPIO48	RAM_ID0 GPIO49	RAM
0	0	0	0	HYNIX 4GB
0	0	0	1	SAMSUNG 4GB
0	0	1	0	MICRON 4GB
0	0	1	1	ELPIDA 4GB
0	1	0	0	SAMSUNG 8GB
0	1	0	1	ELPIDA 8GB
0	1	1	0	MICRON 8GB
0	1	1	1	HYNIX 8GB
1	0	0	0	TBD
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD





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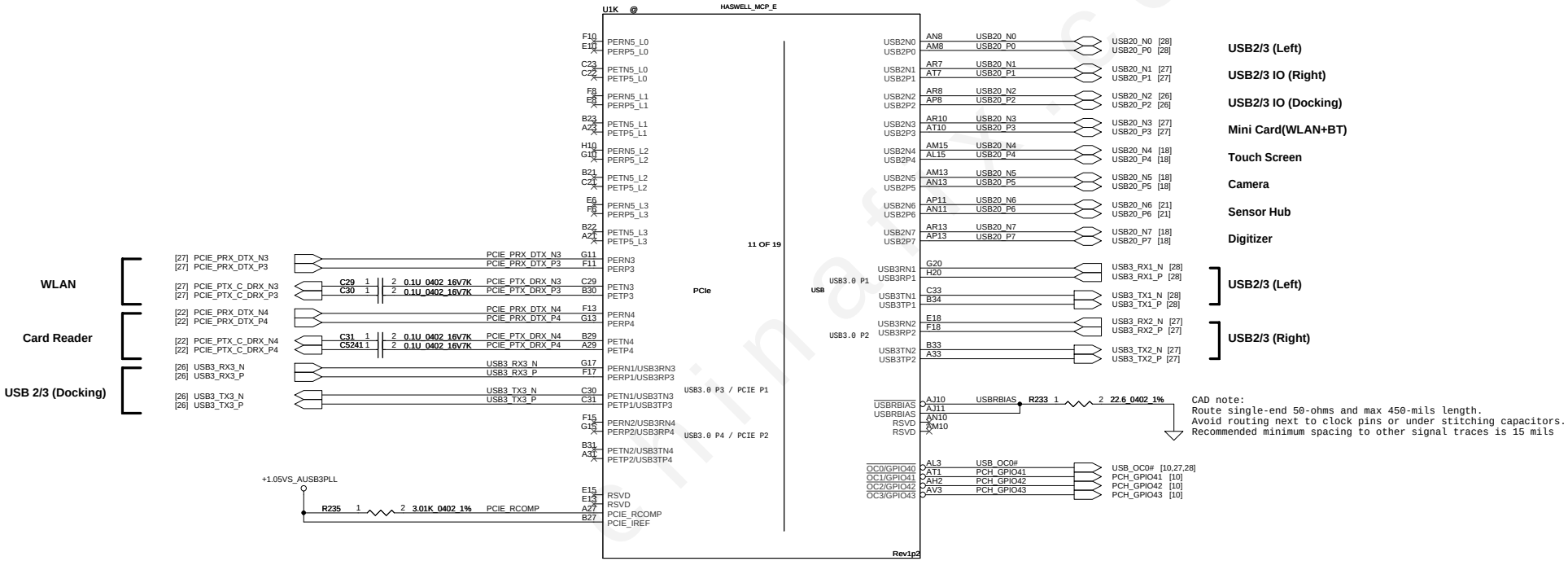
PCIE/ USB



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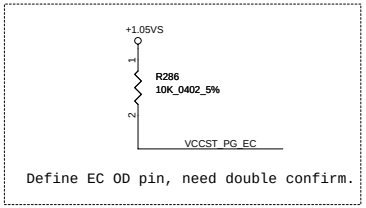
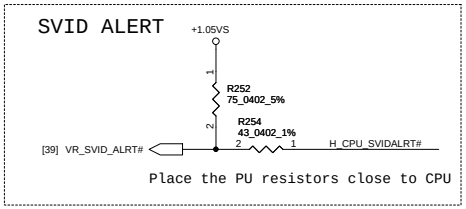
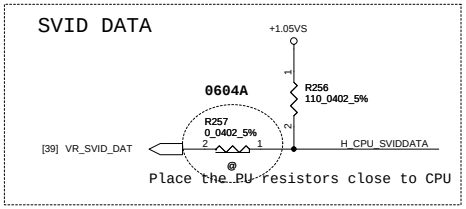
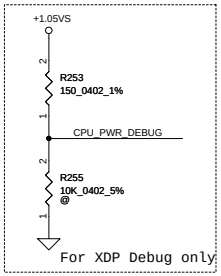
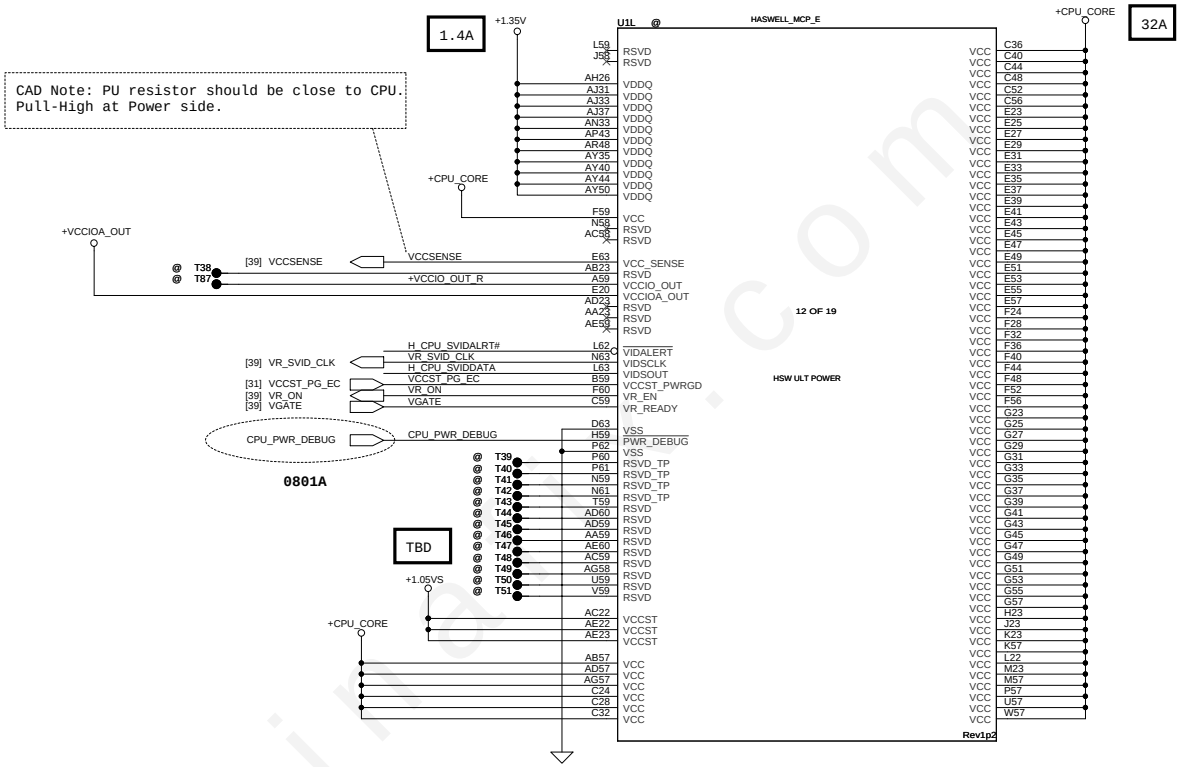


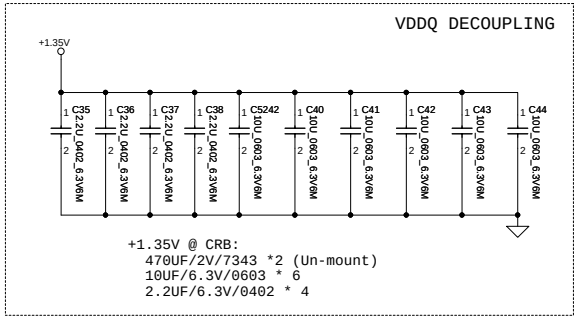






CAD Note: PU resistor should be close to CPU.
Pull-High at Power side.





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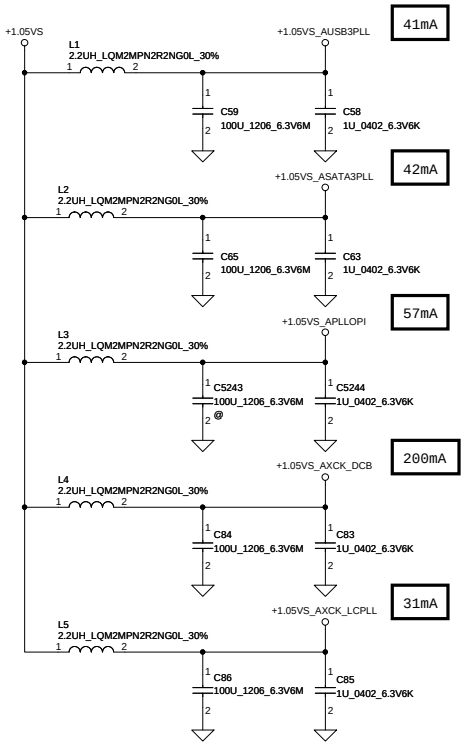
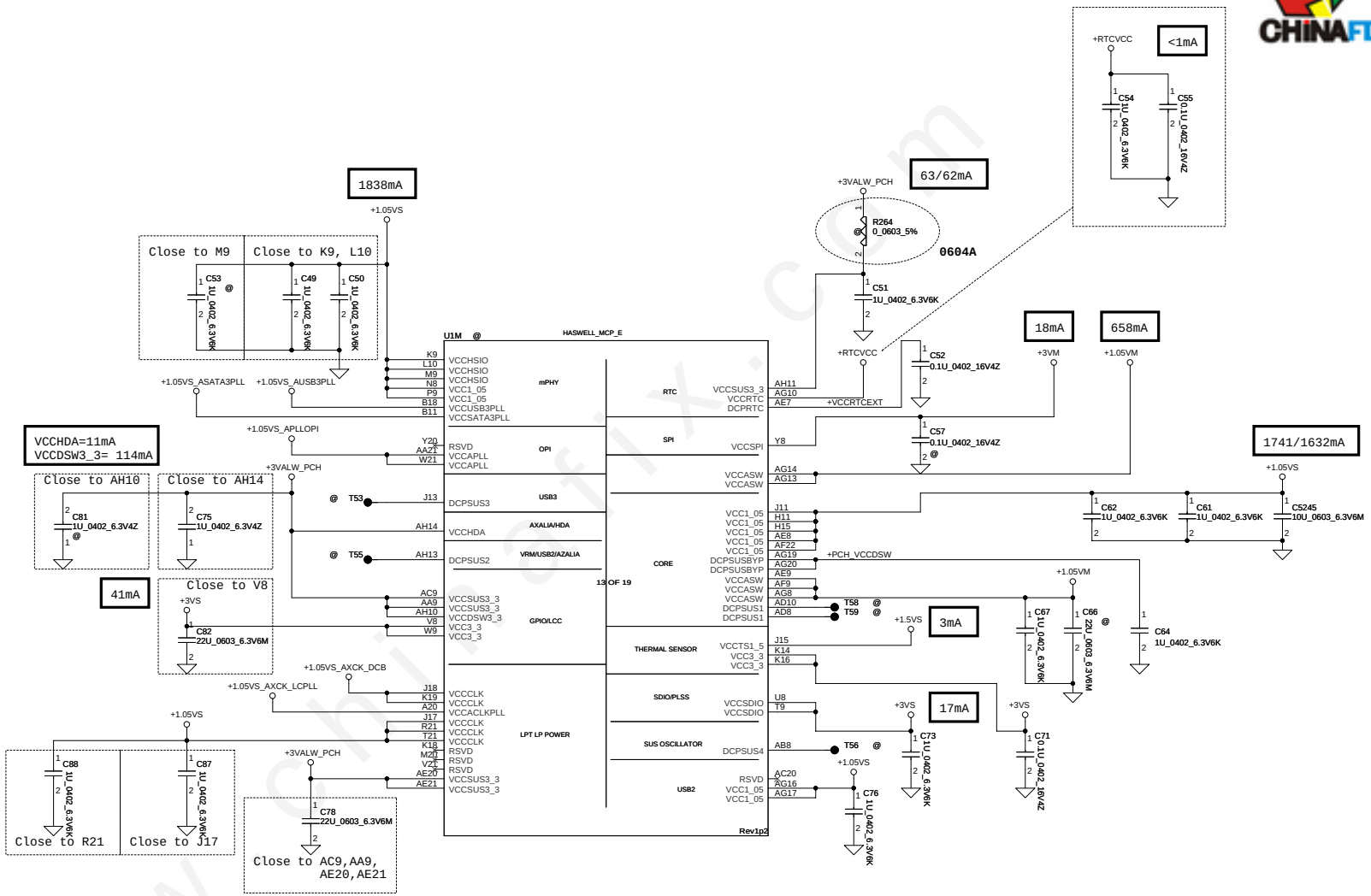
Power





Only availible on External Suspend VR powered.
DcpSus1= 109mA
DcpSus2= 25mA
DcpSus3= 10mA
DcpSus4= 1mA

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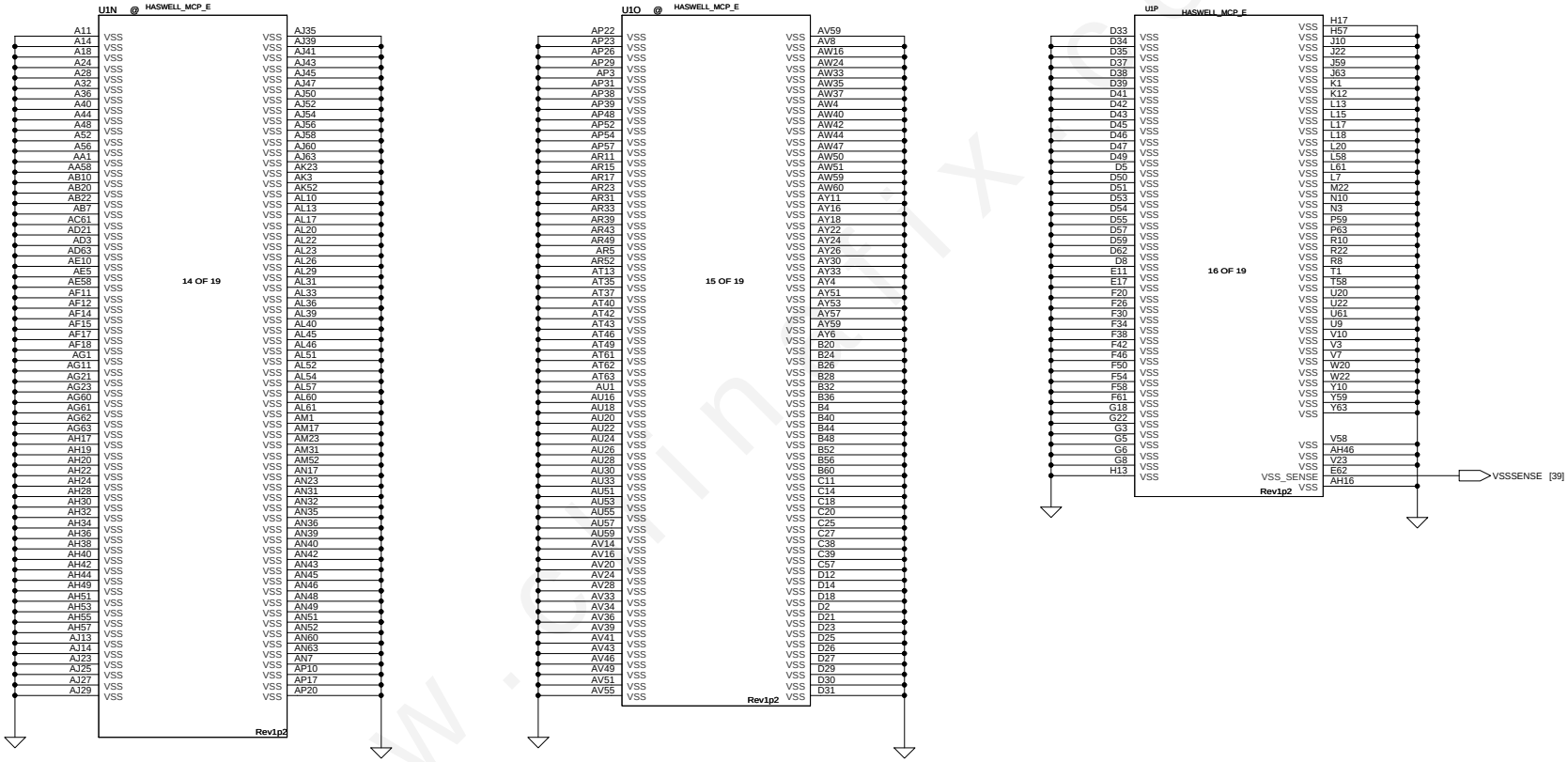
GND



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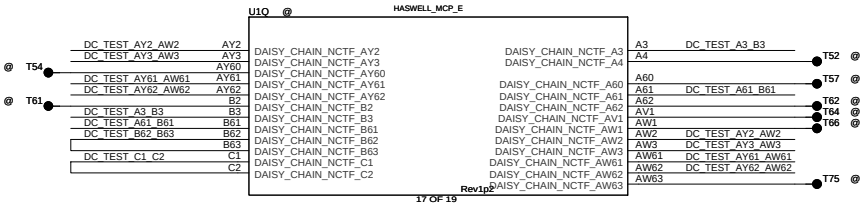
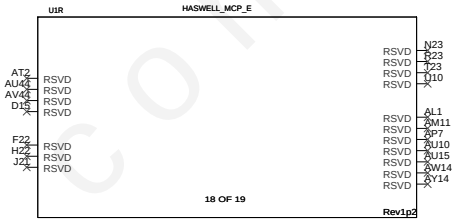
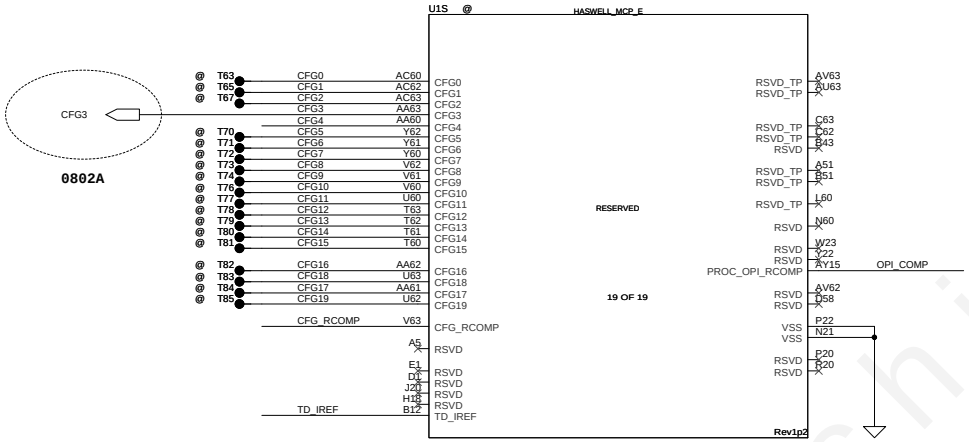
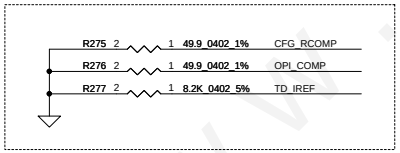
RSVD

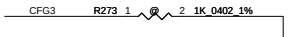






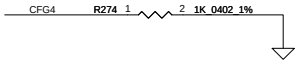


CFG Straps for Processor



CFG3 - Physical Debug Enable (DFX Privacy)

1: DISABLED
0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR.
CFG3 have internal PU.



CFG4 - Display Port Presence Strap

1 : Disabled; No Physical Display Port attached to Embedded Display Port
0 : Enabled; An external Display Port device is connected to the Embedded Display Port
CFG4 have internal PH.

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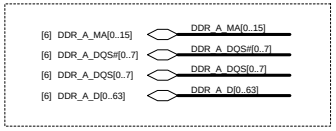

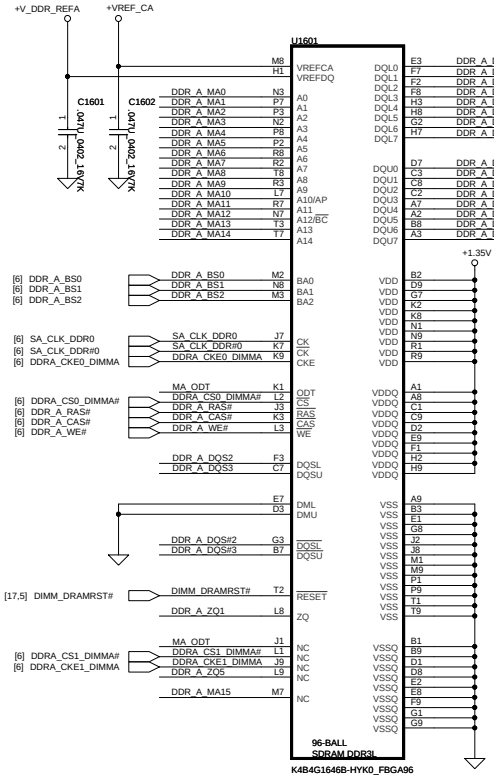

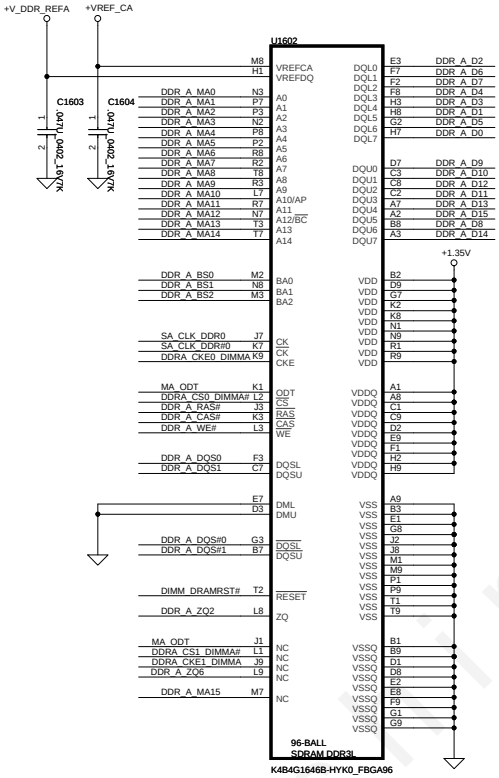

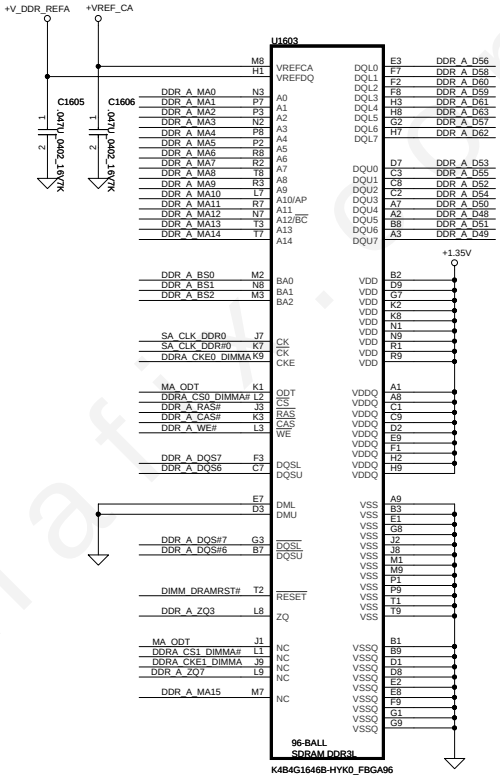

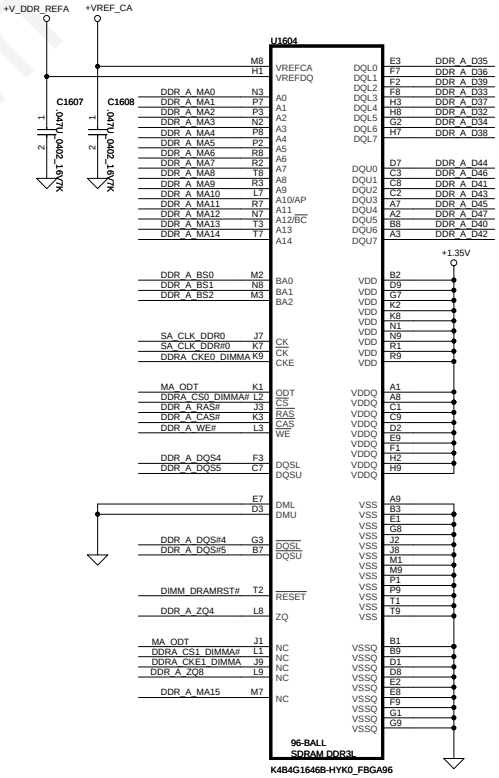

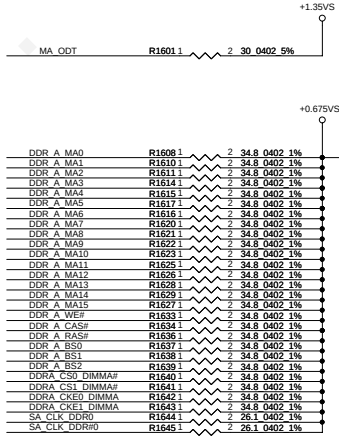

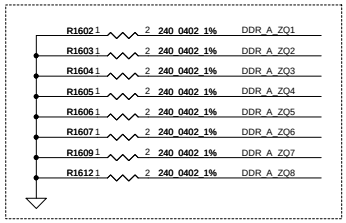

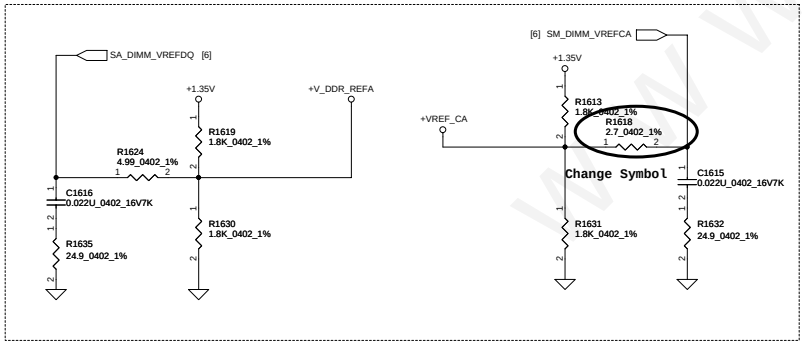

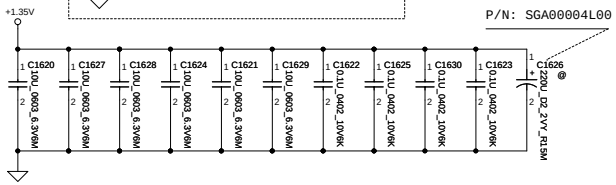

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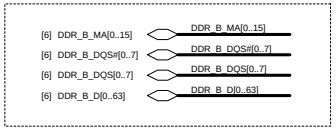
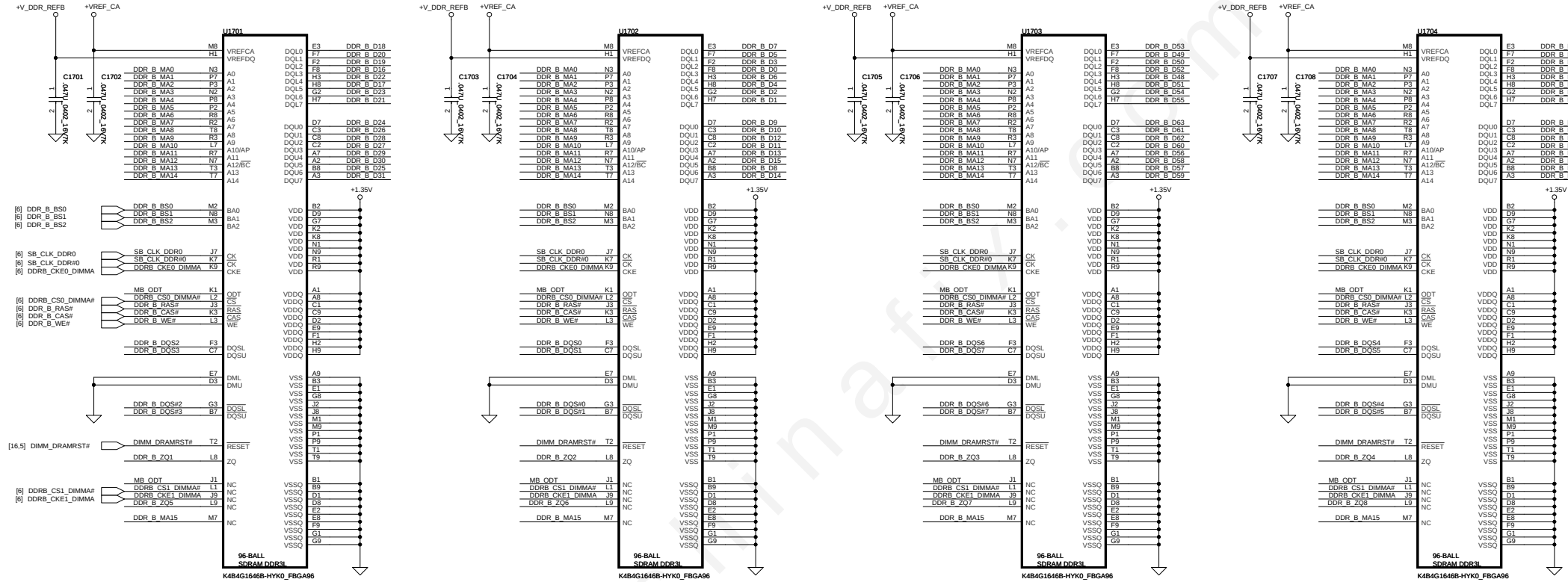
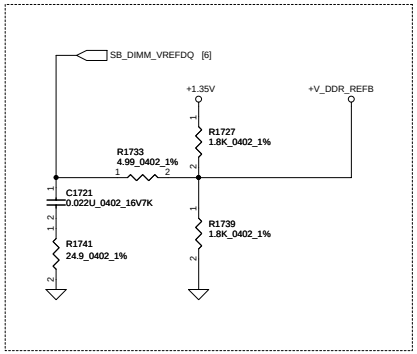
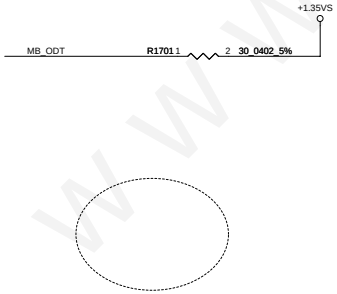
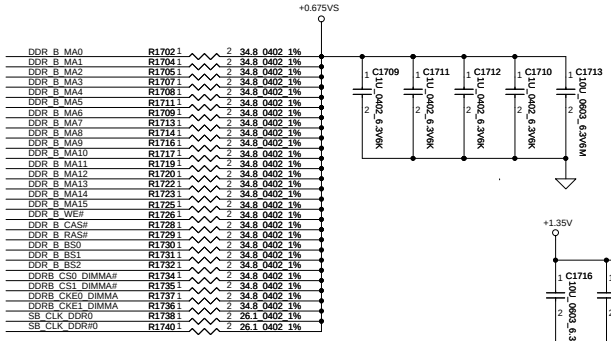
On Board B

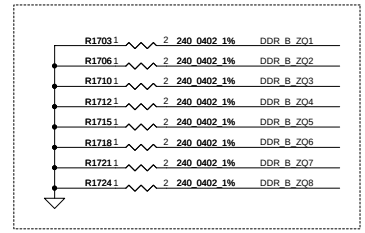


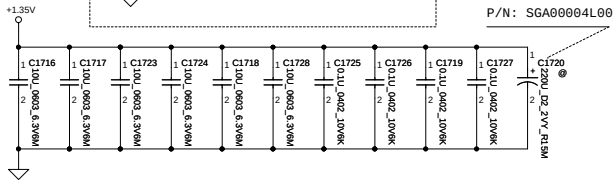












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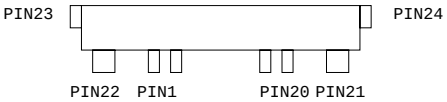
Digitizer & CMOS Conn

DMIC & CAMERA
module pin define

No	SIGNAL
1	VCC (3.3V)
2	D-
3	D+
4	GND_CAM
5	GND_DMIC
6	MIC_C
7	MIC_D
8	MIC_VCC



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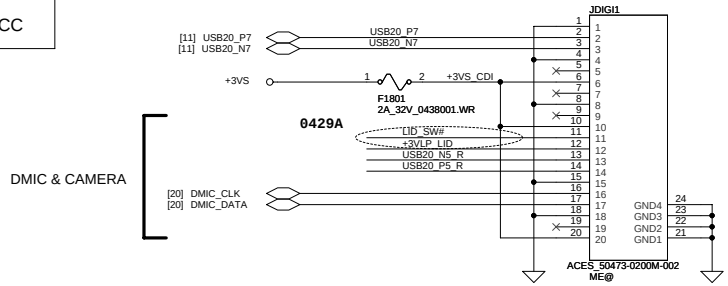
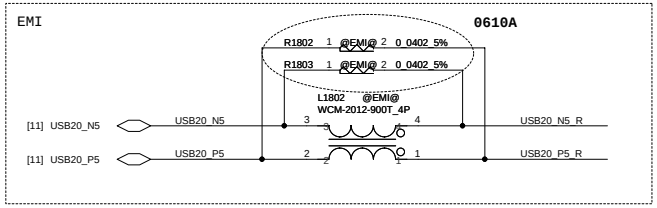
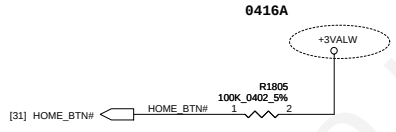
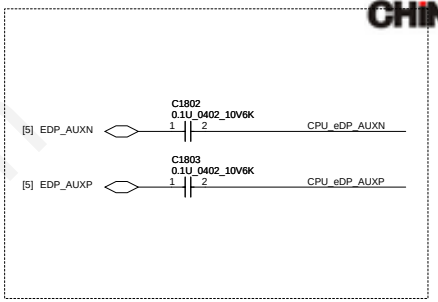
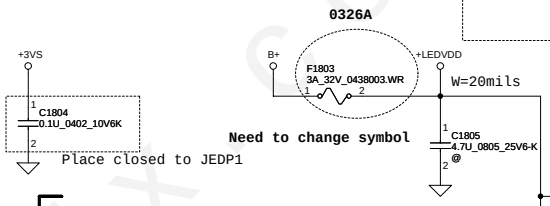


eDP Panel Conn









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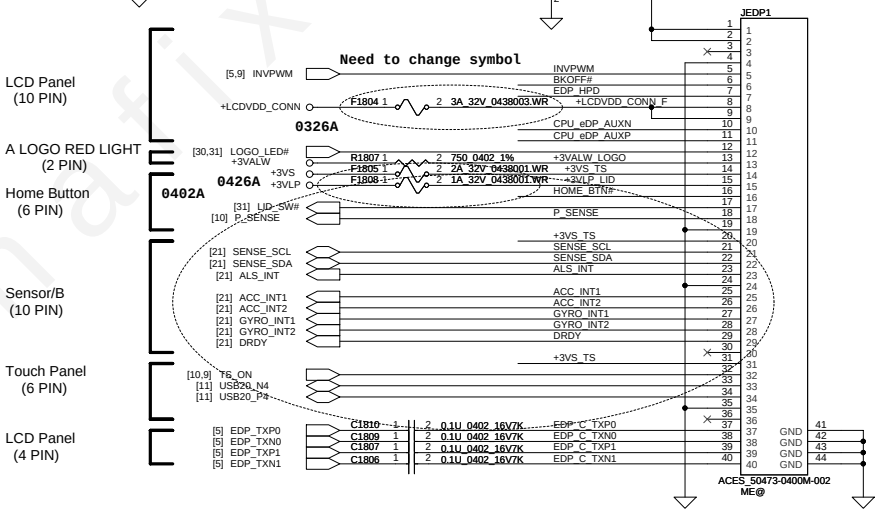

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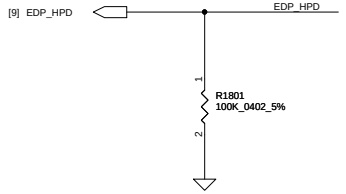
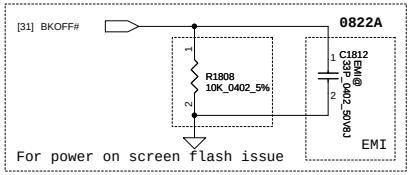
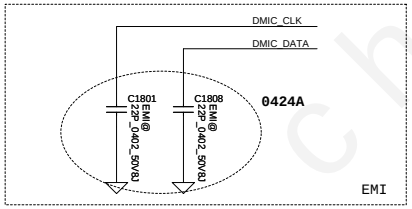


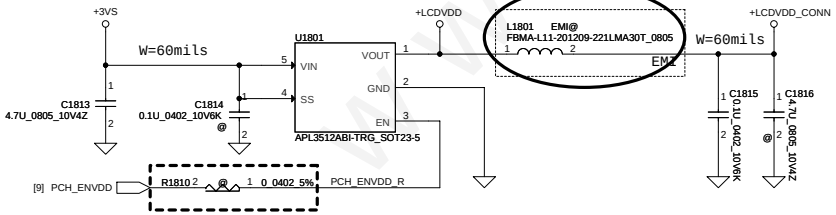




LCD POWER CIRCUIT

SS table

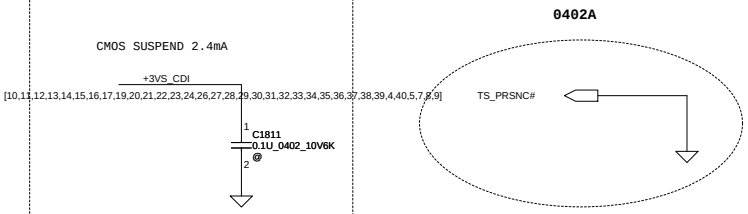
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS



0109 Remove after test.

Camera Modual POWER CIRCUIT

CMOS SUSPEND 2.4mA



Touch PANEL
module pin define

No	USB/I2C
1	VCC (3.3V)
2	Reset
3	GND
4	D-
5	D+
6	GND
7	SCL
8	SDA
9	INT
10	PRSENT

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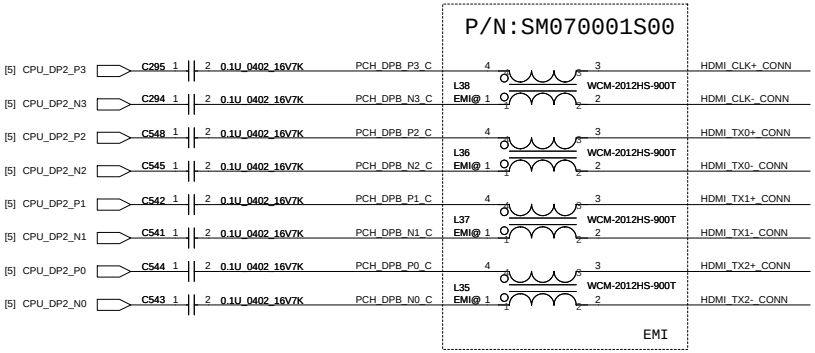
HDMI



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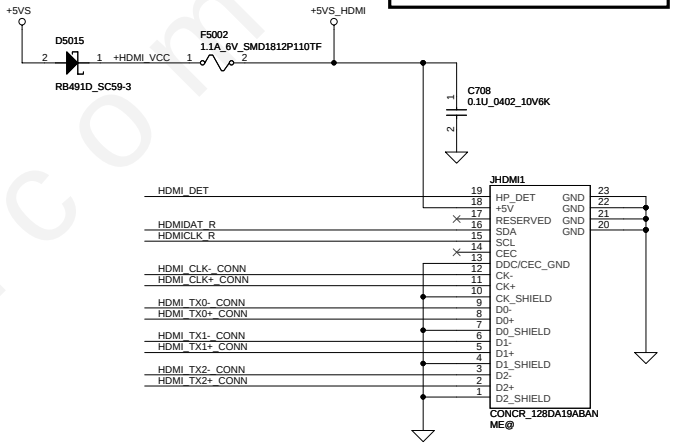
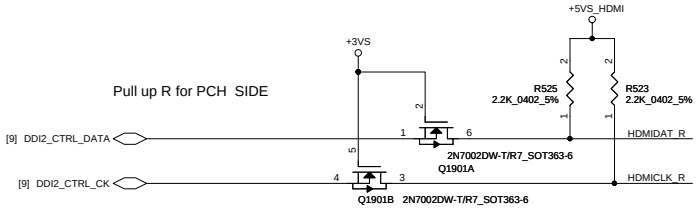
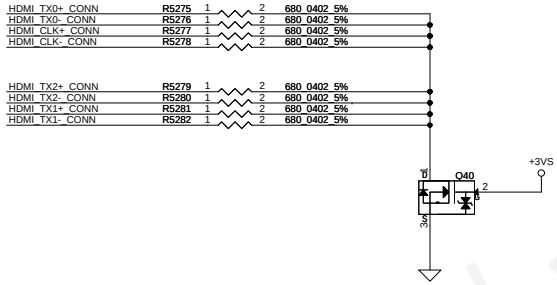
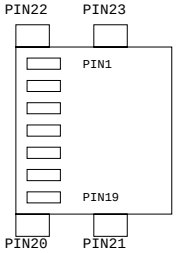
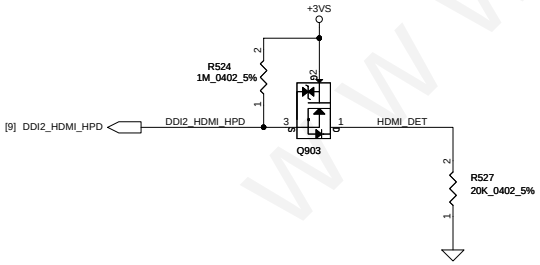
TYPE C Connector

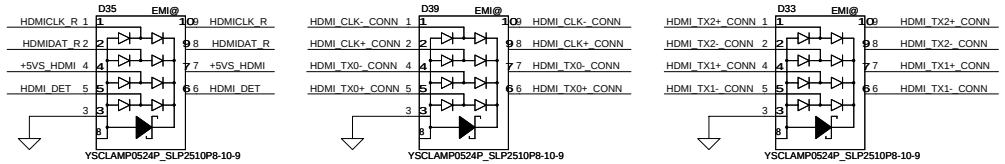












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ESD

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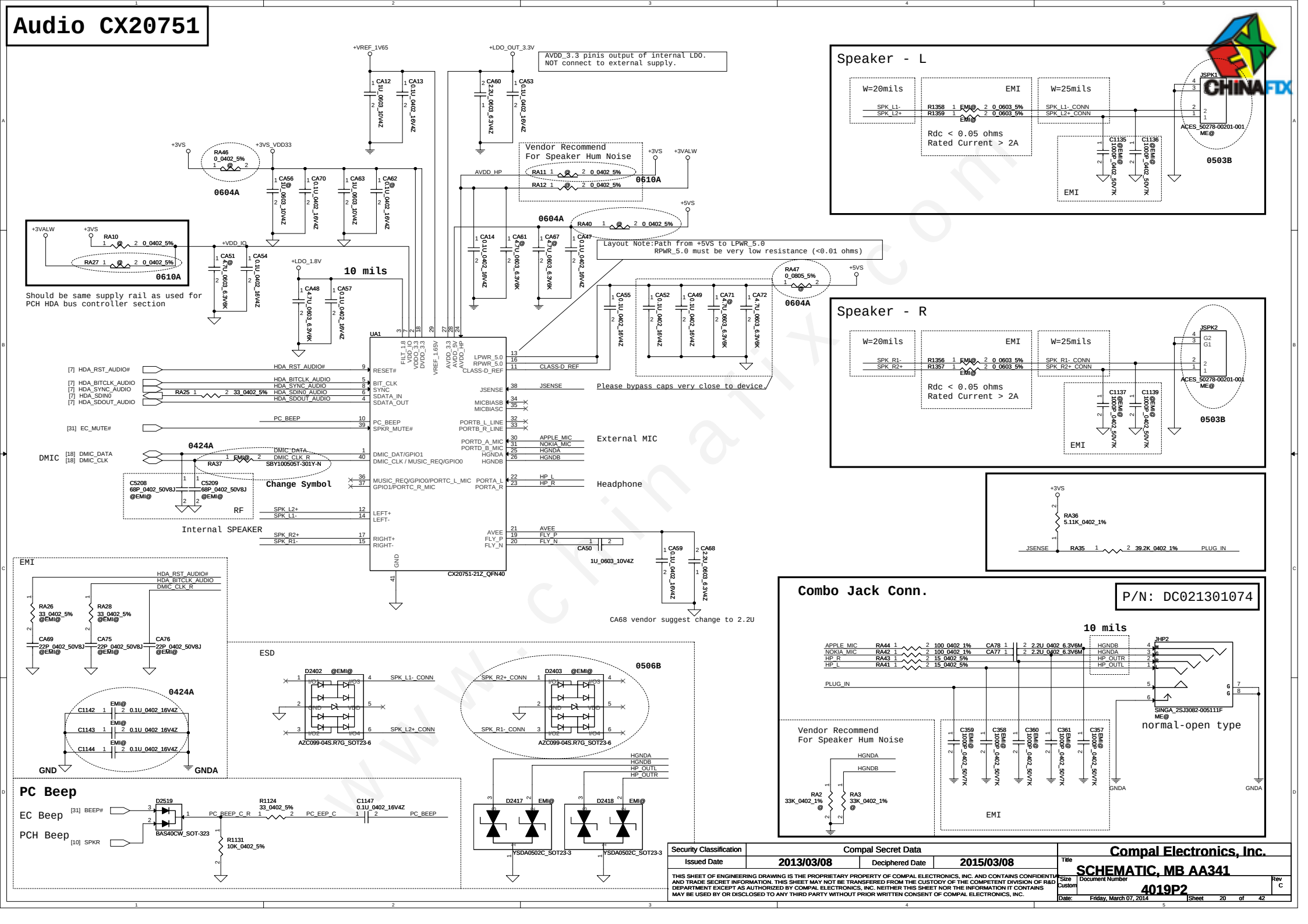
Audio CX20751



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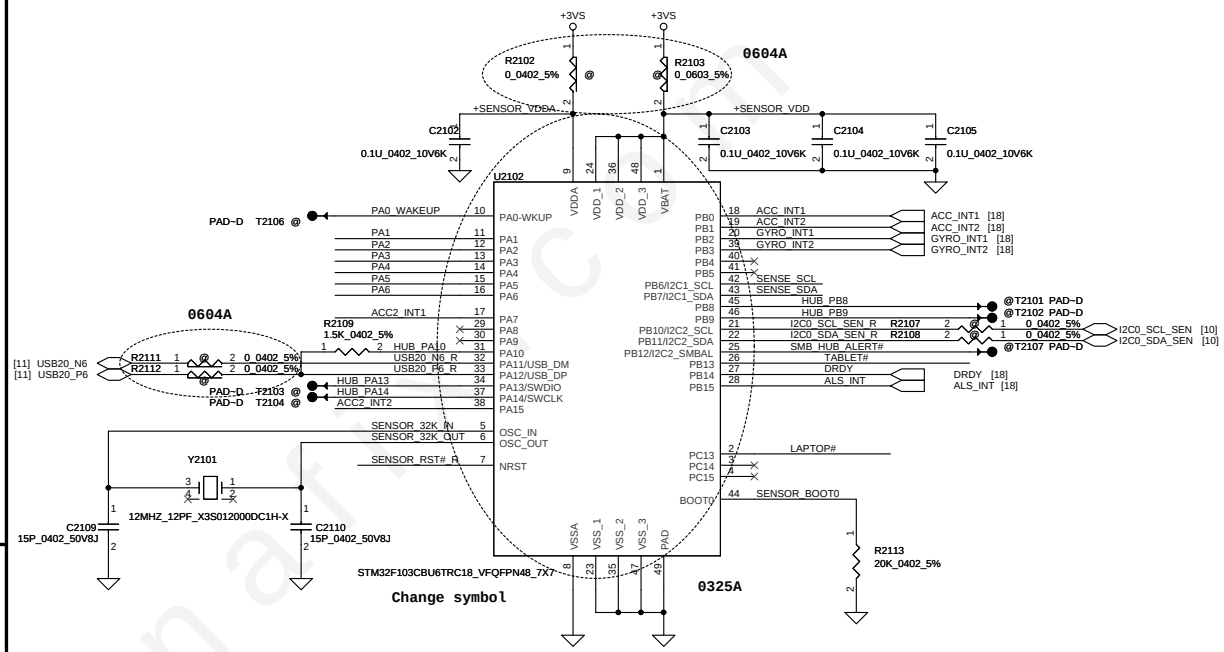
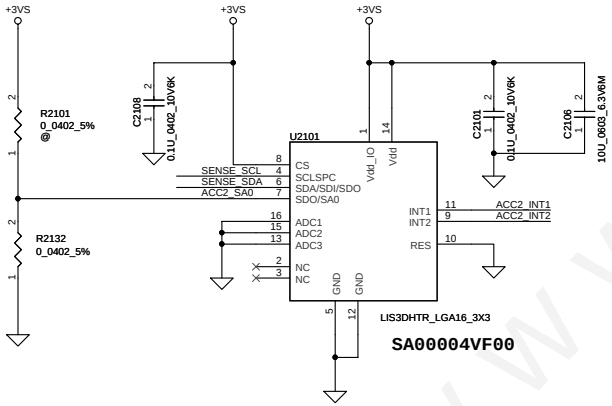
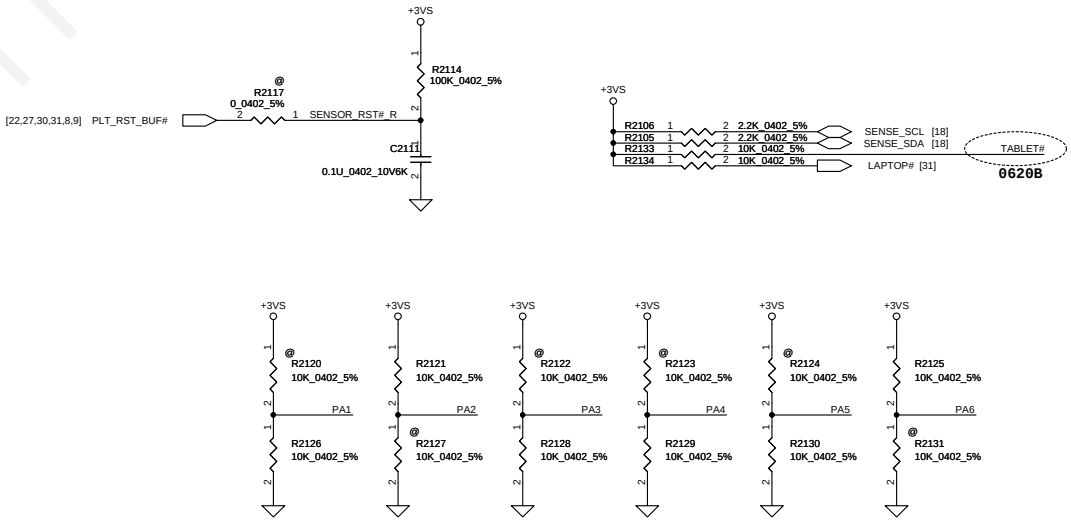
Sensor Hub



2nd G-sensor



	ACC2_SA0
H	0x33h 0x32h
L	0x31h 0x30h



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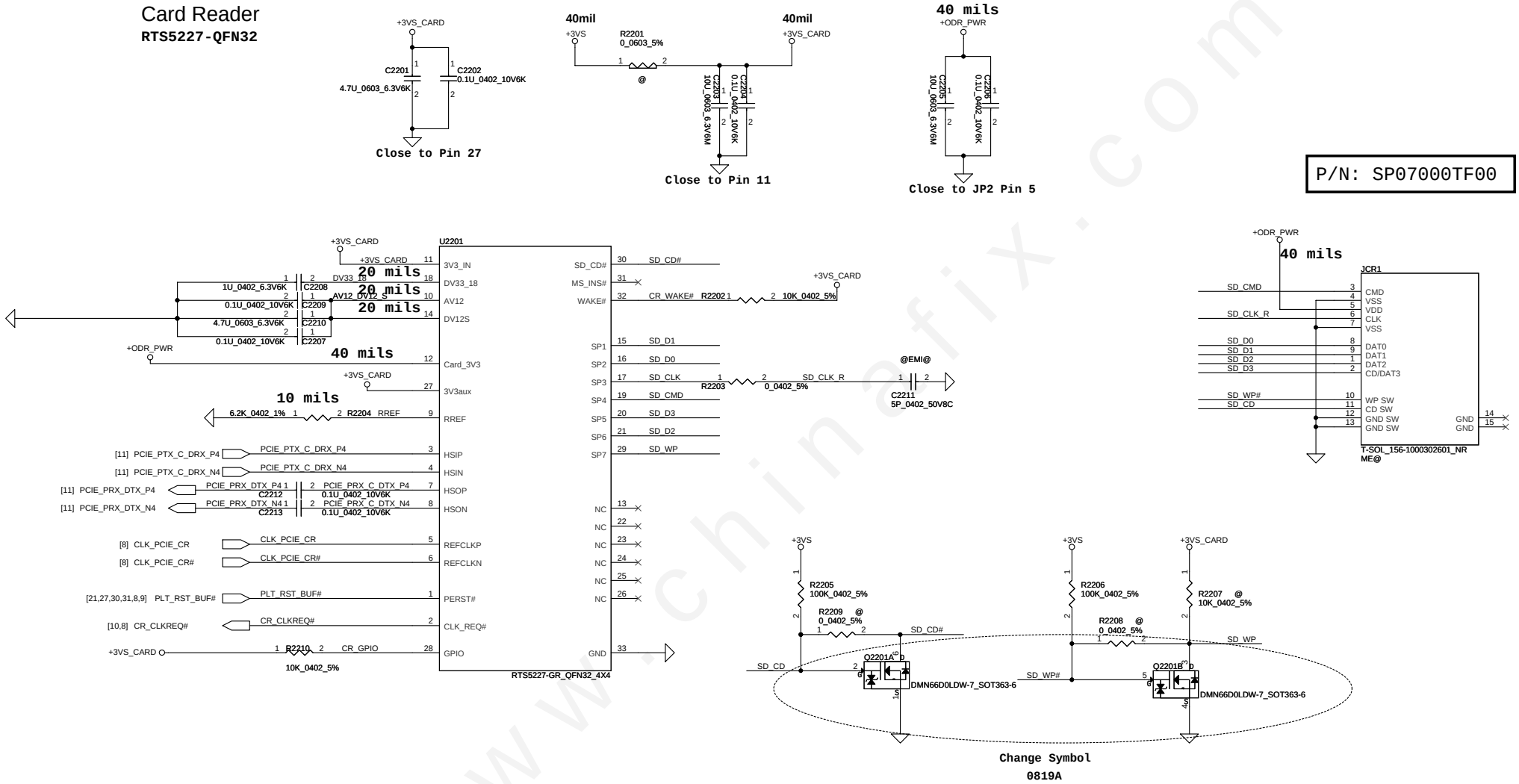
Card Reader

RTS5227-QFN32



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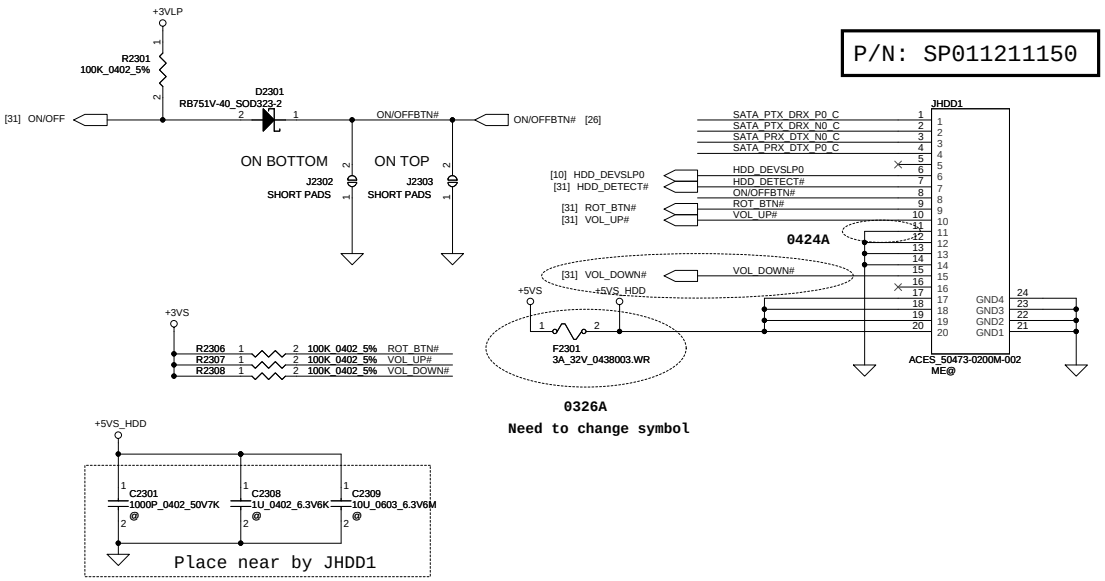
SATA HDD WTB Conn

P/N: SP011211150



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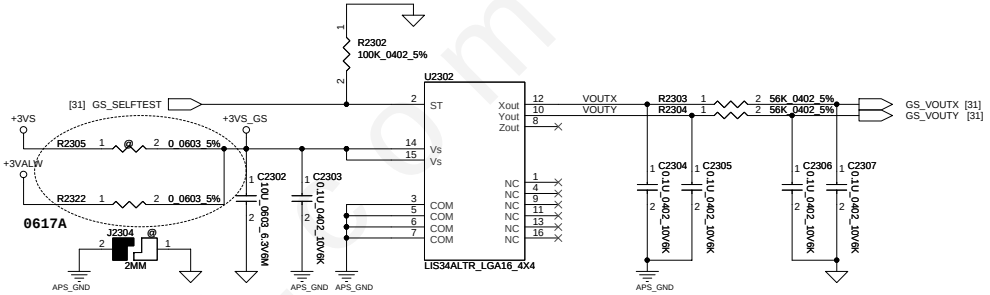
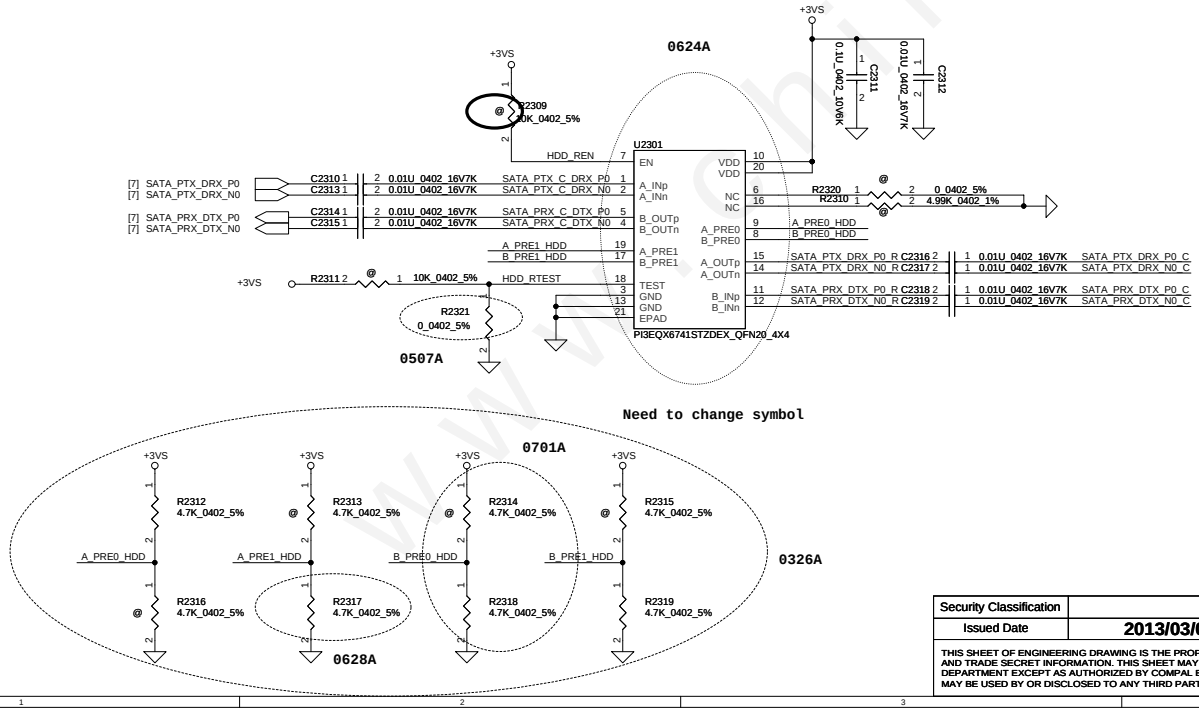


HDD SATA Redriver



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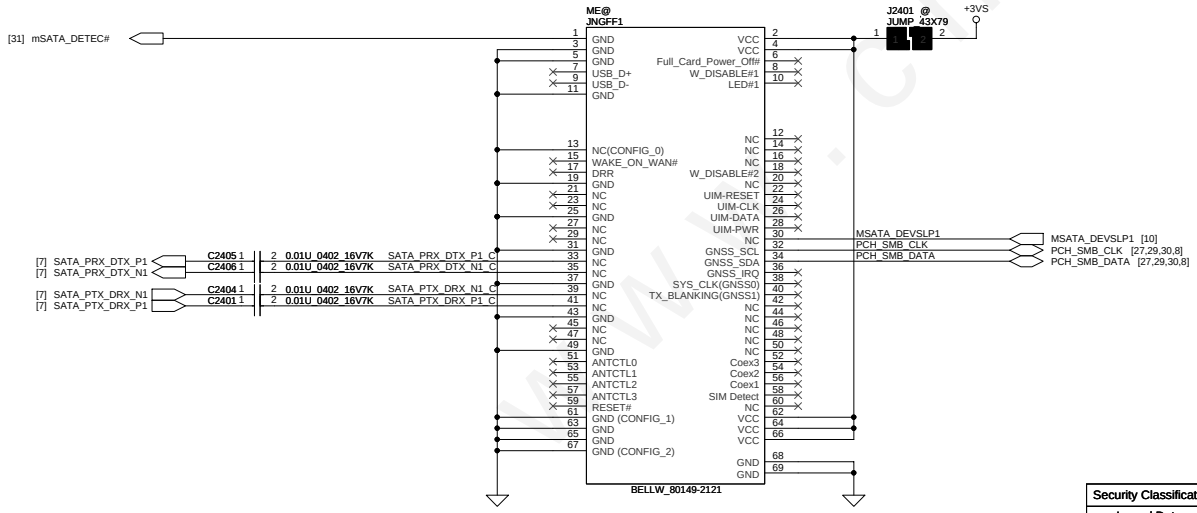
NGFF SATA Redriver

NGFF mSATA Conn

P/N:SP071212280



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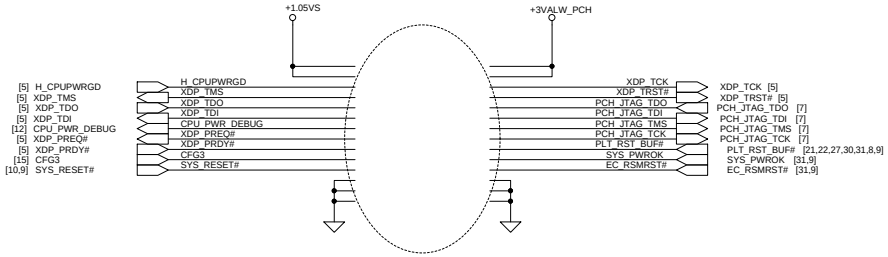
Remove XDP conn. for non-vPro



0815A

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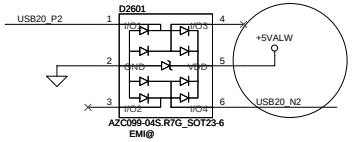
Docking (USB3.0)



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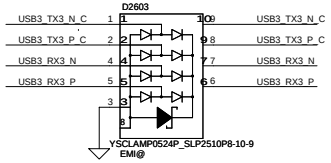

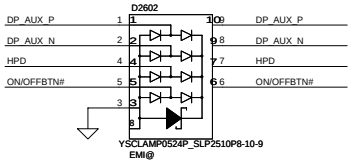

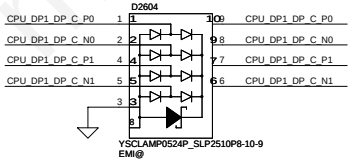

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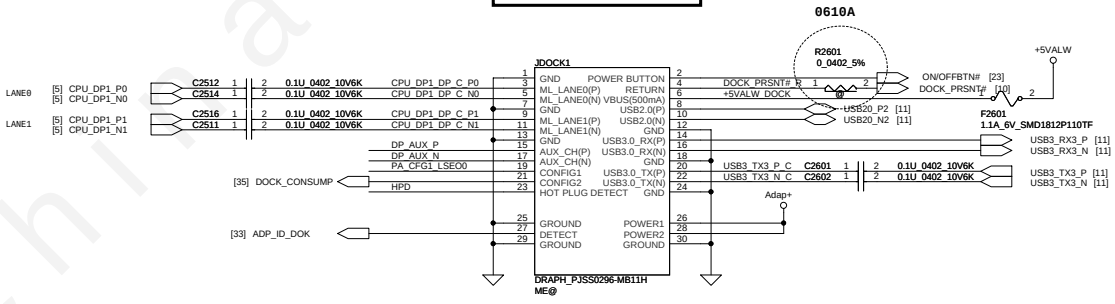

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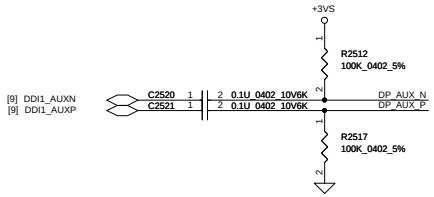

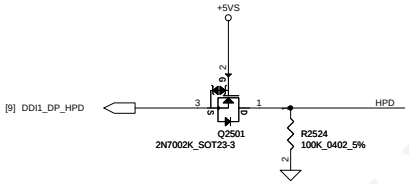

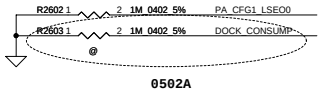

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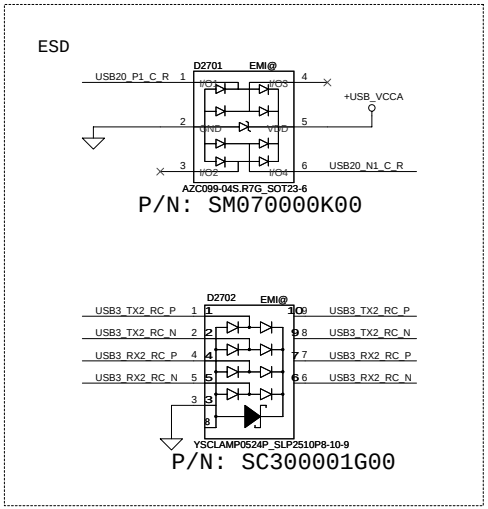
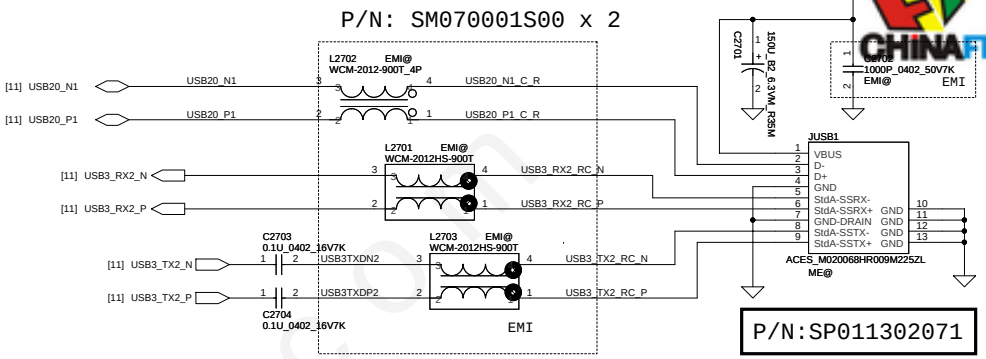
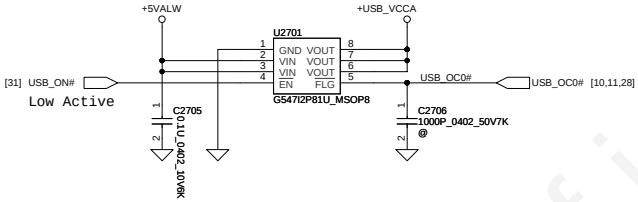
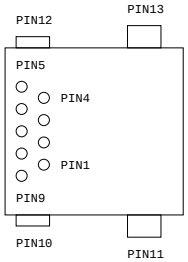
USB30 Conn









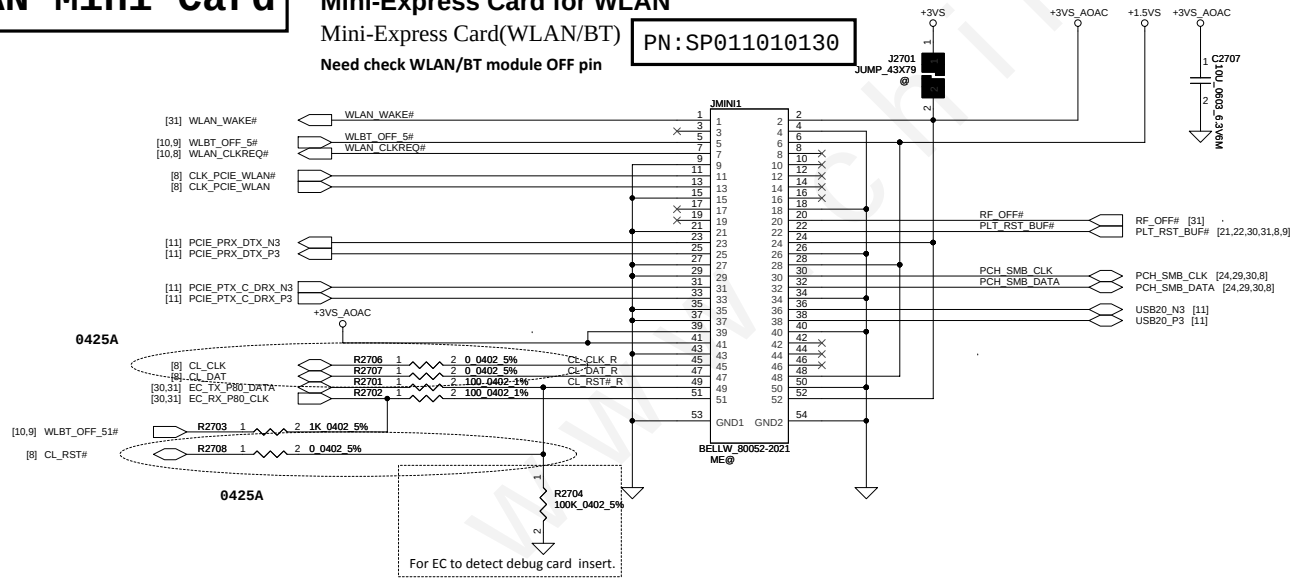
WLAN Mini Card

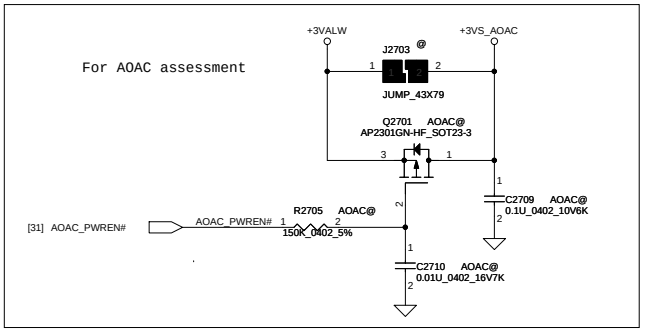
Mini-Express Card for WLAN

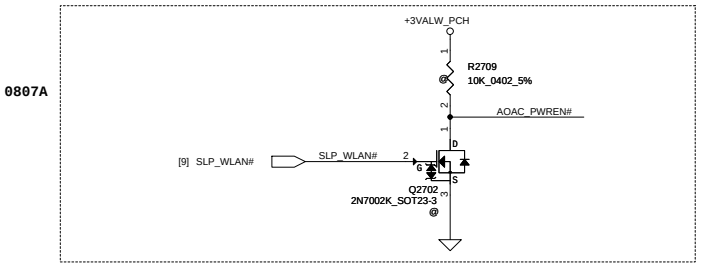
Mini-Express Card(WLAN/BT)

Need check WLAN/BT module OFF pin

PN:SP011010130







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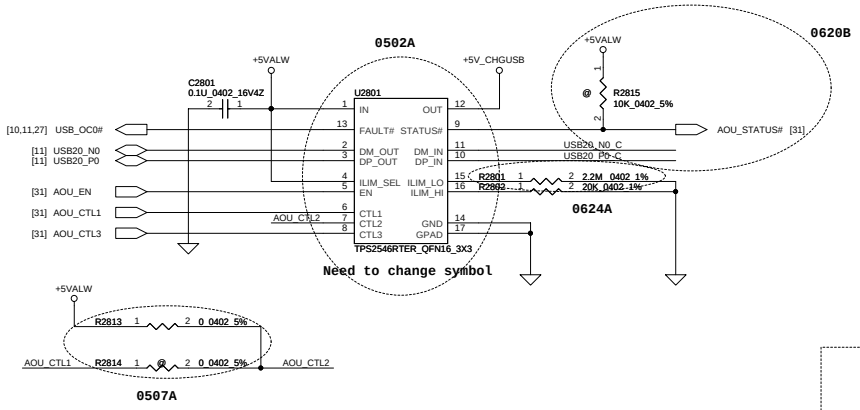
USB 3.0 Charger & Conn.



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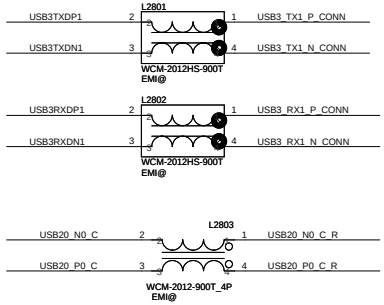

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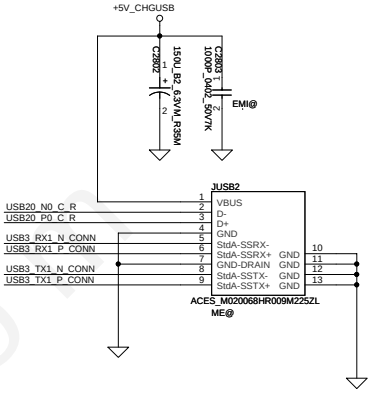

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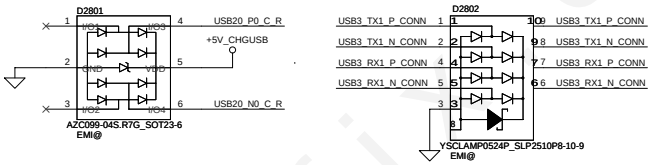

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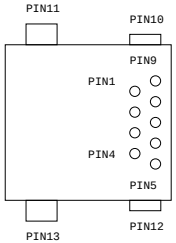

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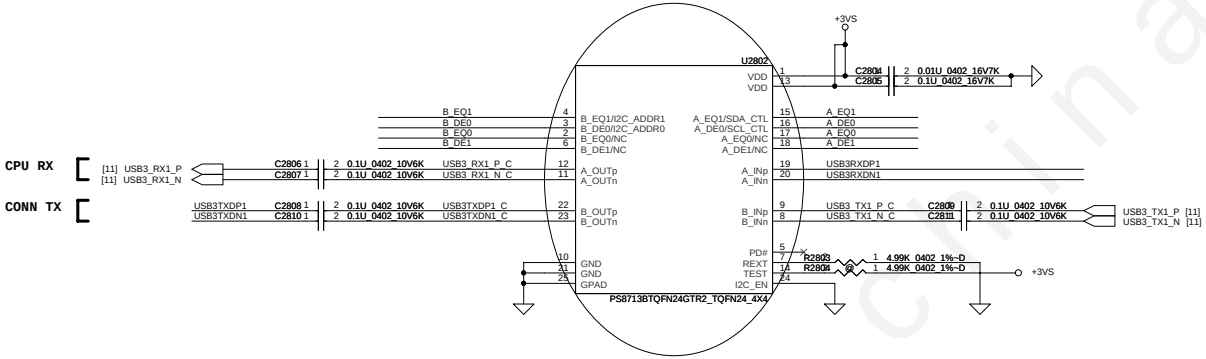
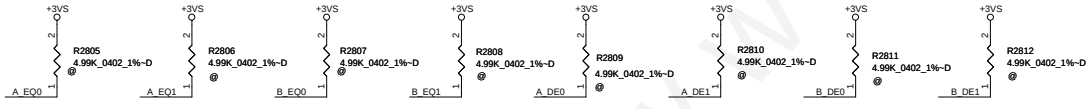
6/25



	A_EQ1/B_EQ1 (Internal pull Low)	A_EQ0/B_EQ0 (Internal pull Low)
reserved	Low	Low
program EQ for channel loss up to 7dB	Low	High
program EQ for channel loss up to 14.5dB	High	Low
program EQ for channel loss up to 11.5dB	High	High



	TEST (Internal pull Low)
Normal operation (default)	Low
Test mode enable	High

	A_DE1/B_DE1 (Internal pull Low)	A_DE0/B_DE0 (Internal pull Low)
3.5dB de-emphasis	Low	Low
No de-emphasis	Low	High
2.7dB de-emphasis	High	Low
5dB with boost output swing	High	High

PN:SA000059H00

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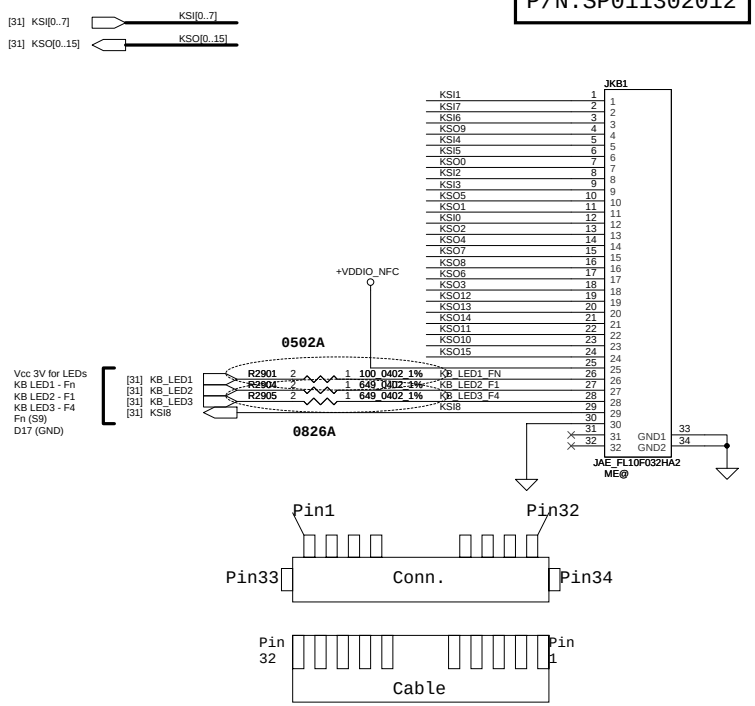
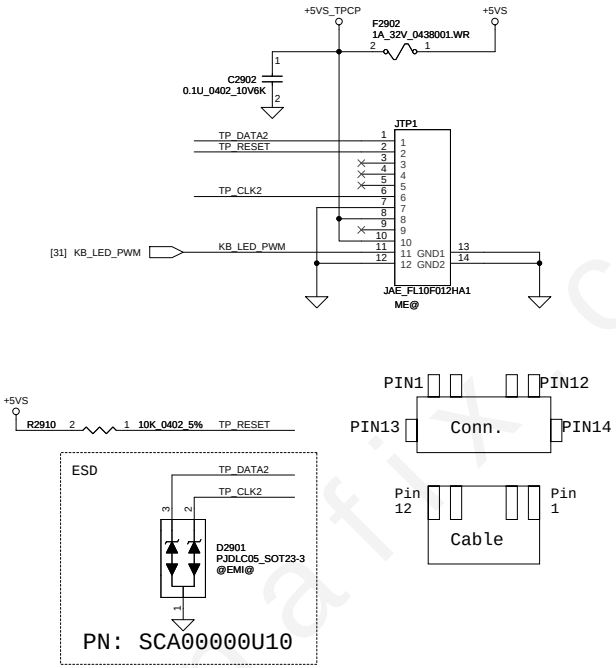
Int KB Conn

P/N:SP011302012



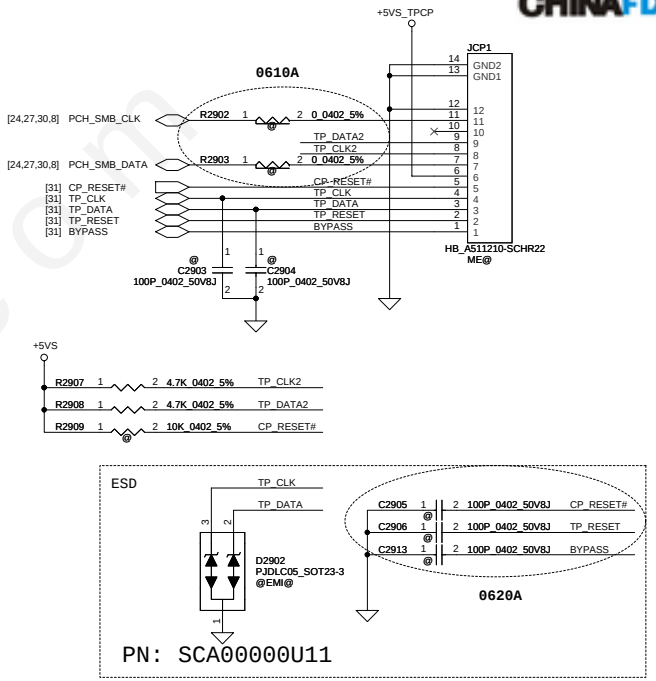
Track Point

P/N:SP011302013

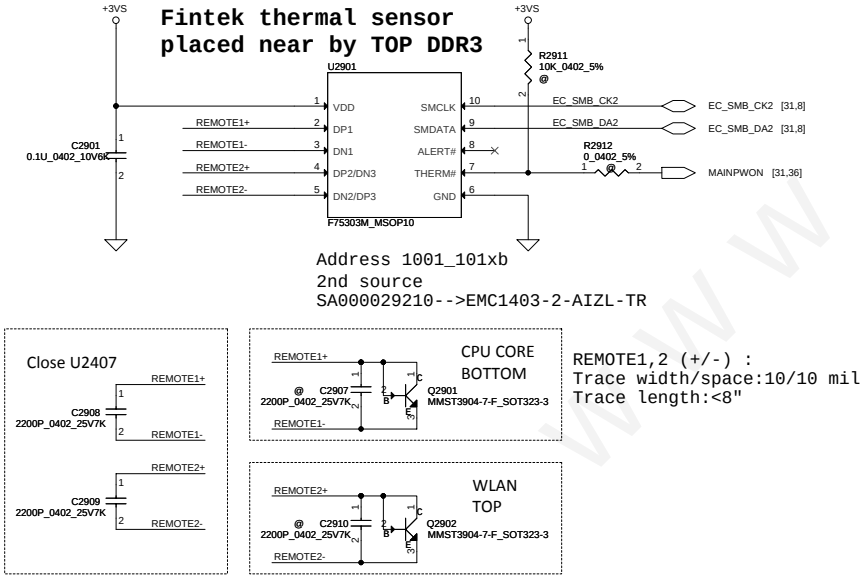


Click PAD

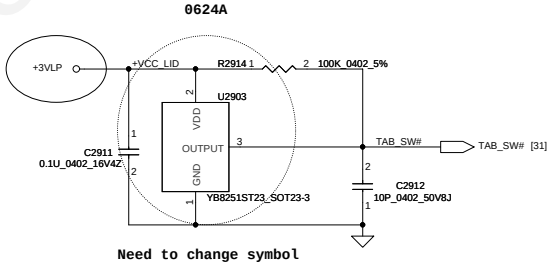
P/N:DC02120109 0



THRM Sensor



Tablet Switch



Track Point pin define

NO	Signal
1	IPD DATA
2	IPD RST
3	NC
4	NC
5	NC
6	IPD CLK
7	GND
8	VCC5
9	BKLITE DEC
10	LED VCC5
11	LED PWM
12	LED GND

Click PAD pin define

NO	Signal
1	GND
2	SMB CLK
3	NC
4	DATA-TP
5	CLK-TP
6	SMB-DATA
7	VDD
8	RESET
9	CLK
10	DATA
11	TP4RST
12	BYPASS

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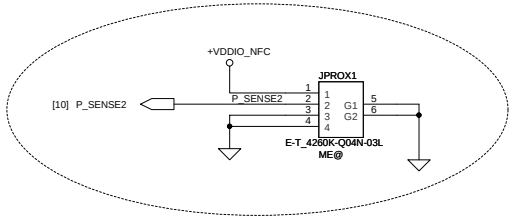
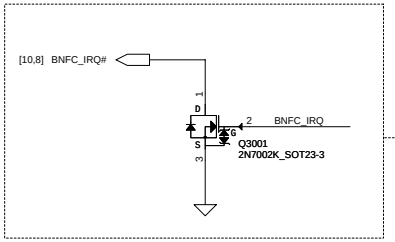
P-Sensor Conn



0507A

NFC

Module Pin define
1.IP/VBAT
2.IP/VDDIO
3.IO/I2C-SDA
4.I/I2C-SCL
5.G/GND
6.O/IRQ-NFC
7.O/NFC_Presence#
8.I/REG_UP
9.OP/VDD_Ext_SE
10.IP/UIM_PWR
11.IO/SWP



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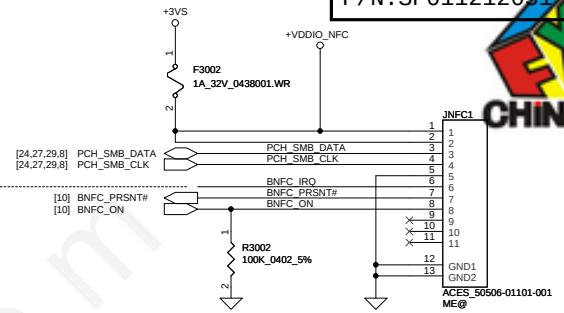
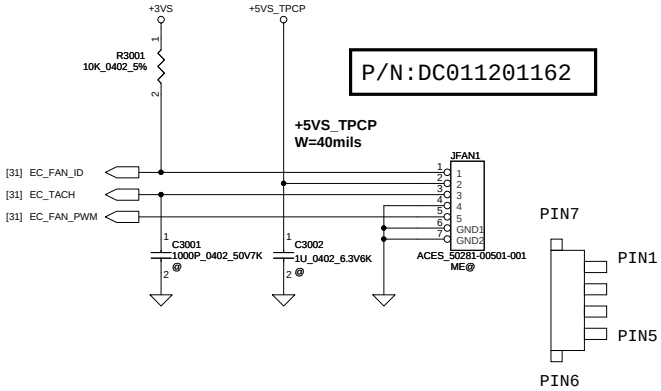
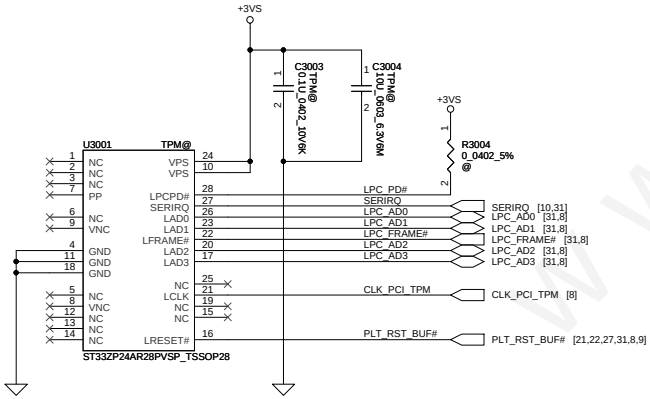


Conn

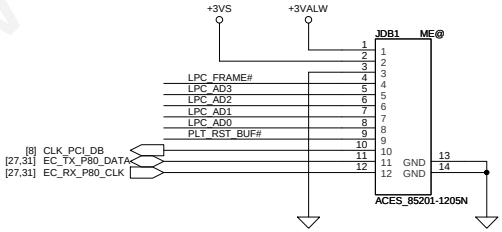
FAN Conn



TPM

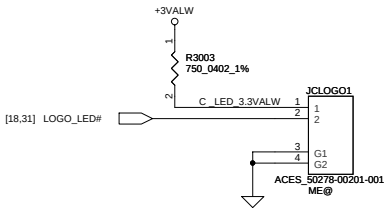


Debug Conn



C-logo Conn

PN:SP02000EZ10



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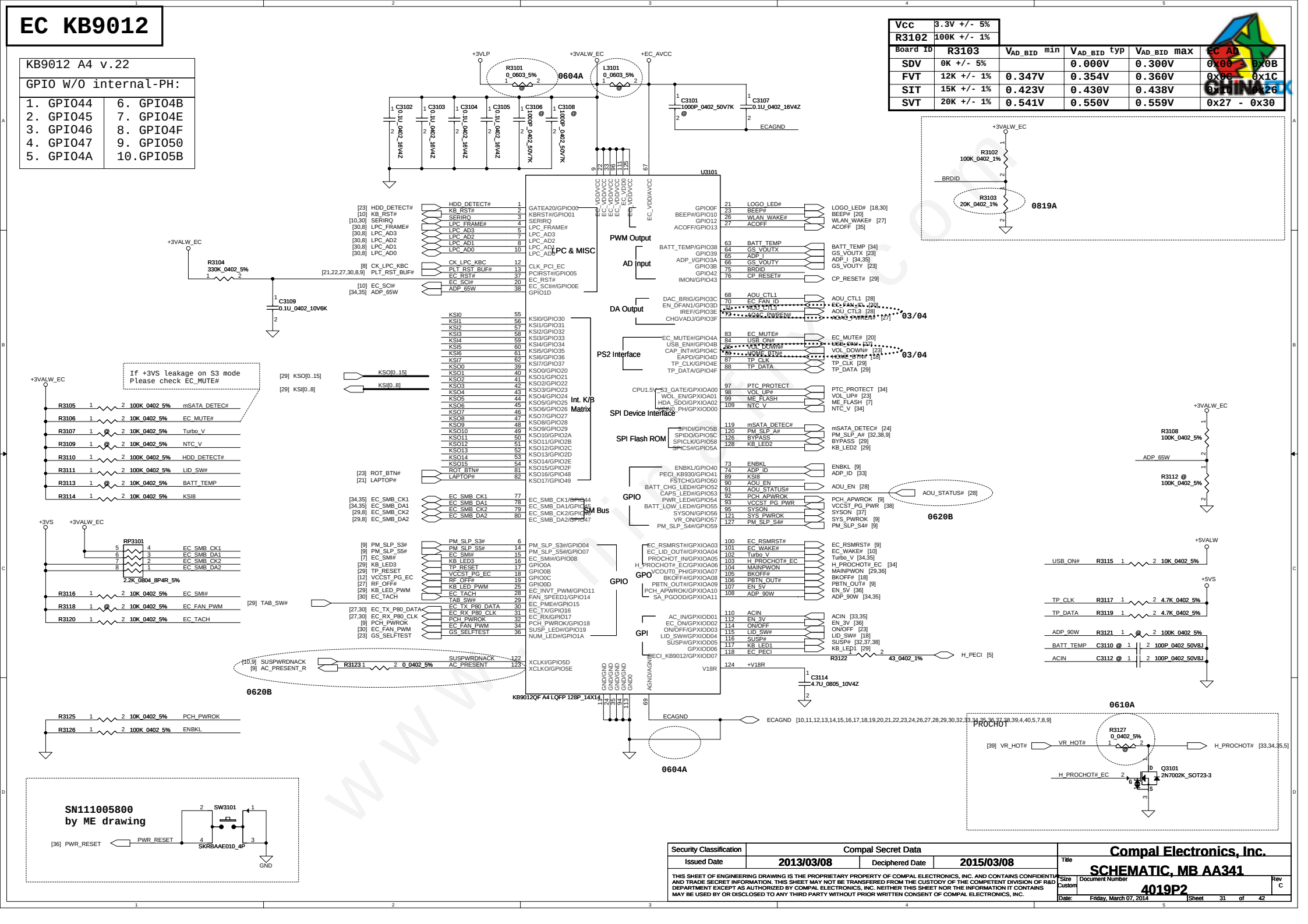
EC KB9012

KB9012 A4 v.22	
GPIO W/O internal-PH:	
1. GPIO44	6. GPIO4B
2. GPIO45	7. GPIO4E
3. GPIO46	8. GPIO4F
4. GPIO47	9. GPIO50
5. GPIO4A	10.GPIO5B

Vcc	3.3V +/- 5%				
R3102	100K +/- 1%				
Board ID	R3103	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD
SDV	0K +/- 5%		0.000V	0.300V	0x00 - 0x0B
FVT	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
SIT	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
SVT	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30



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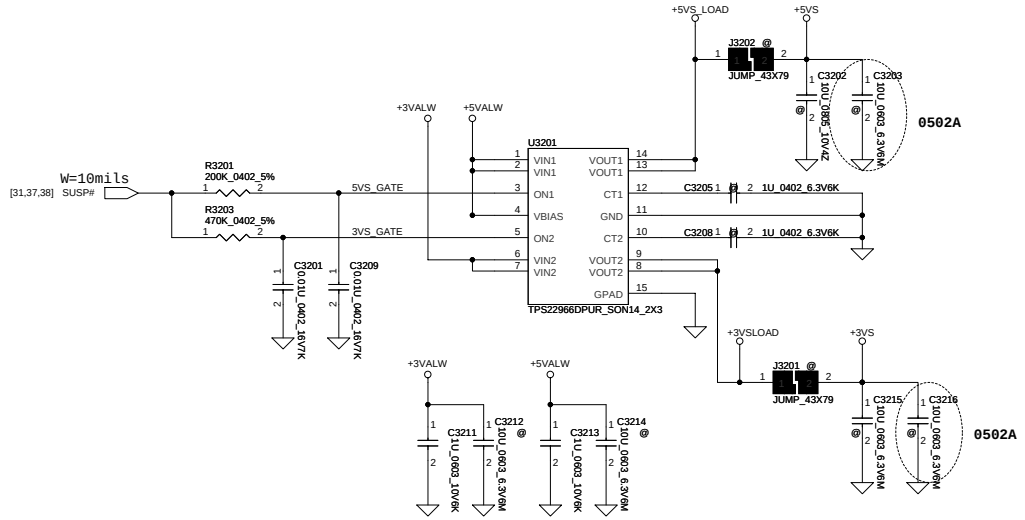
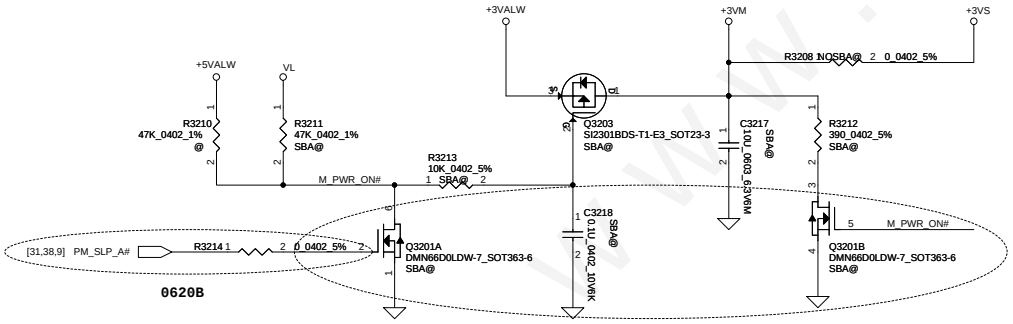
DC/DC I/F

+5VALW TO +5VS
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)

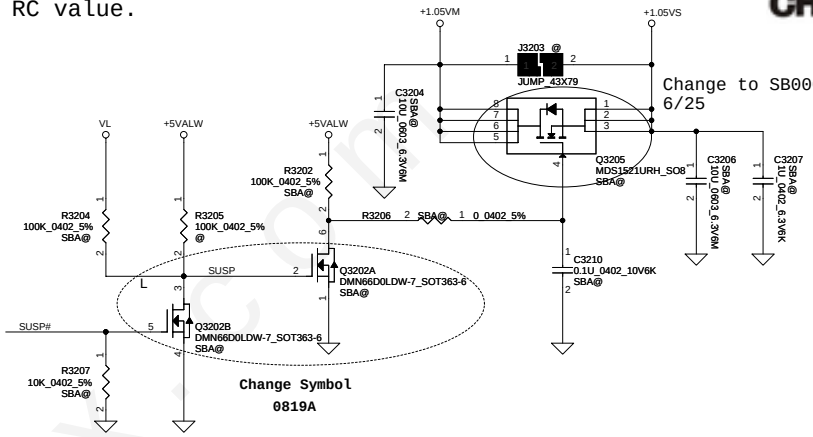
+3VALW TO +3VM (SBA)

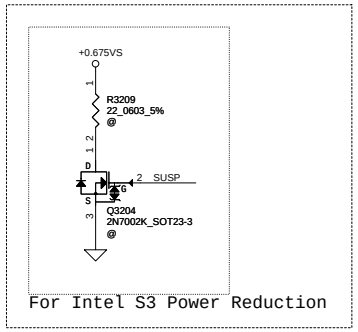


PJ703 Short => NOSBA
PJ703 Open => SBA

Rds(on) VGS=4.5V,ID=8.5A,7mOhm(Max)

Check RC value.





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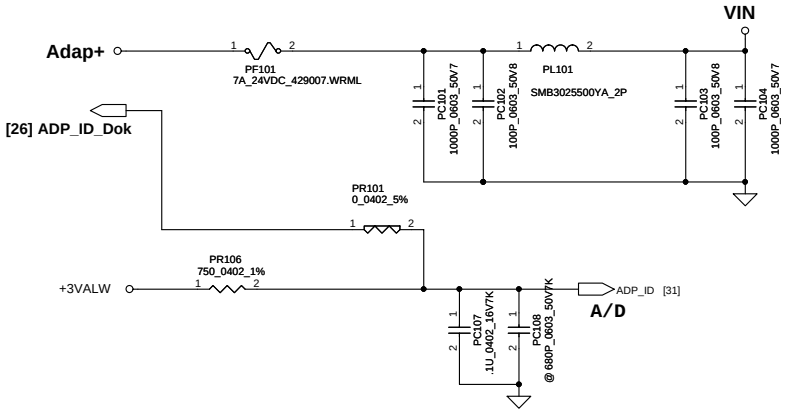
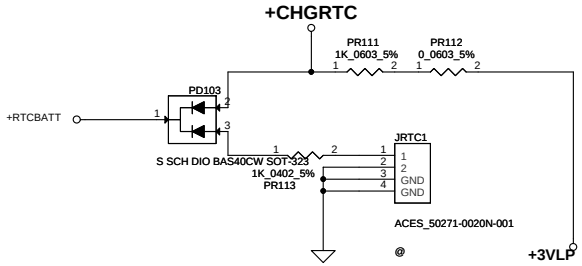
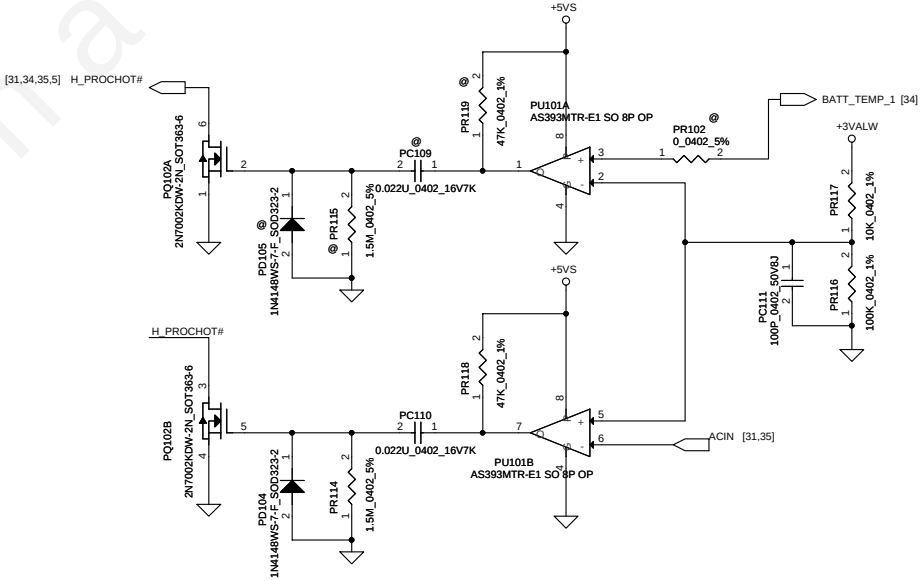


ADP_ID

AC Adapter	45W	65W	90W
R(ohm)	118	287	549
ADP_ID(V)	0.449	0.913	1.395
Detection -Voltage(V)	<=0.663, >0.234	<=1.134, >0.693	<=1.618 >1.172





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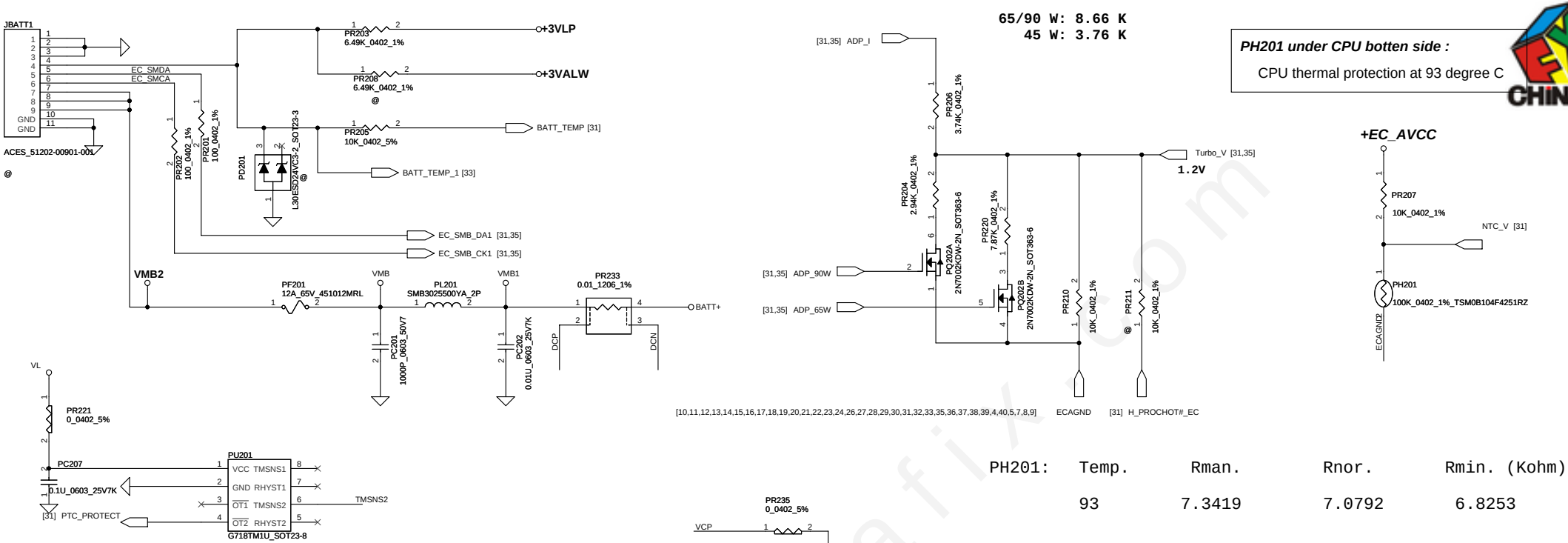
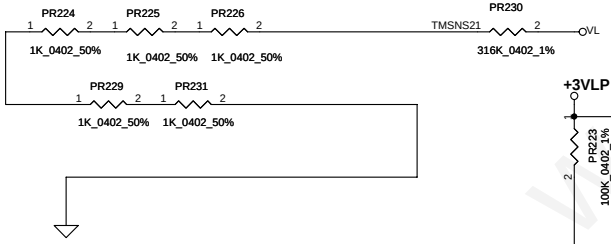


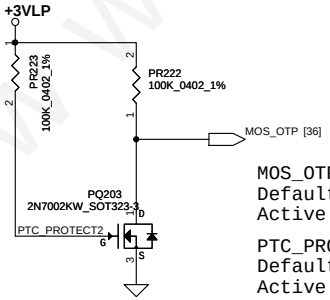
PH201 under CPU botten side :

CPU thermal protection at 93 degree C

PH201:	Temp.	Rman.	Rnor.	Rmin. (Kohm)
	93	7.3419	7.0792	6.8253

Posestor





MOS_OTP:
Default:High
Active :Low

PTC_PROTECT:
Default:Low
Active :High

Battery Protection Circuit for Turbo Mode

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

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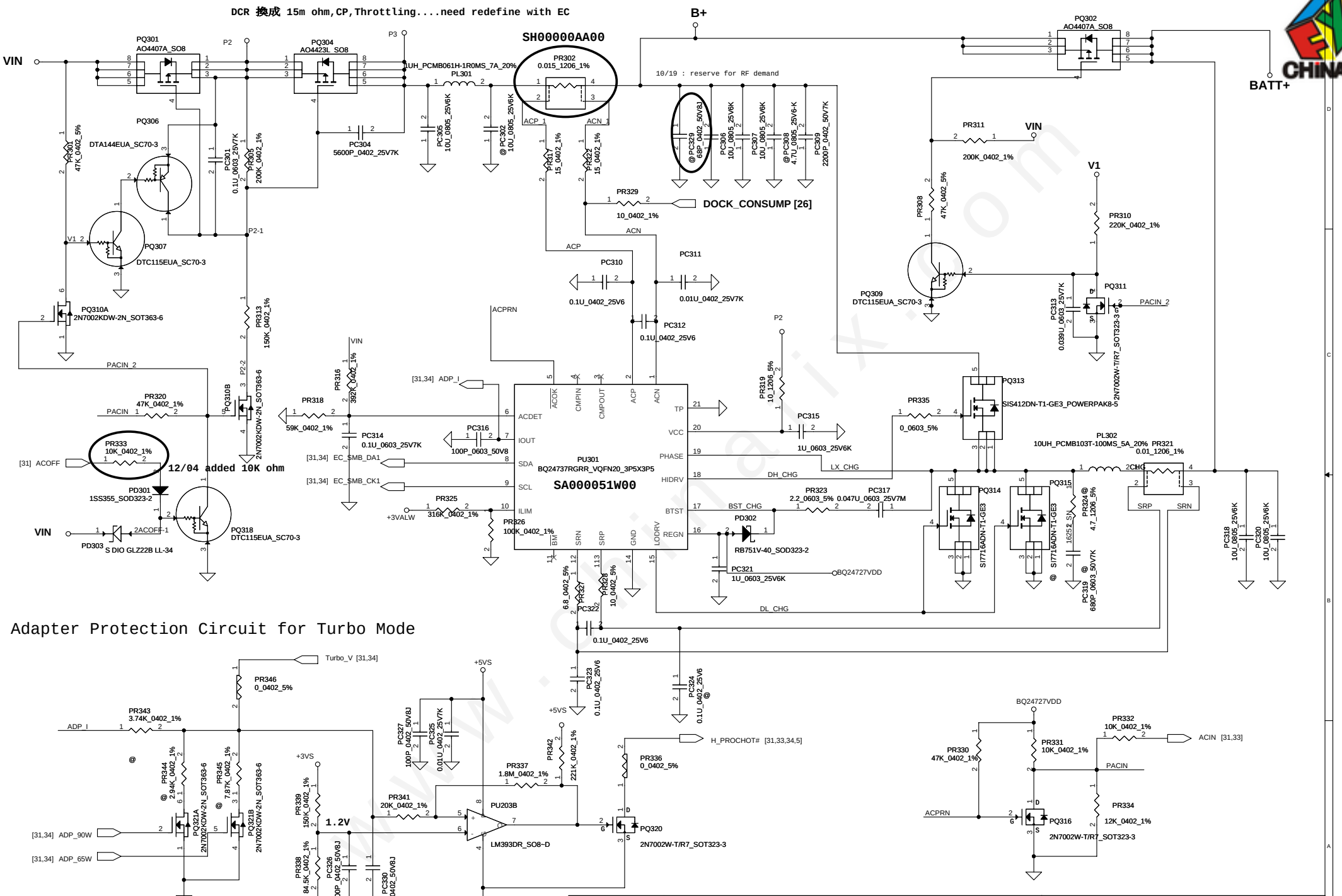

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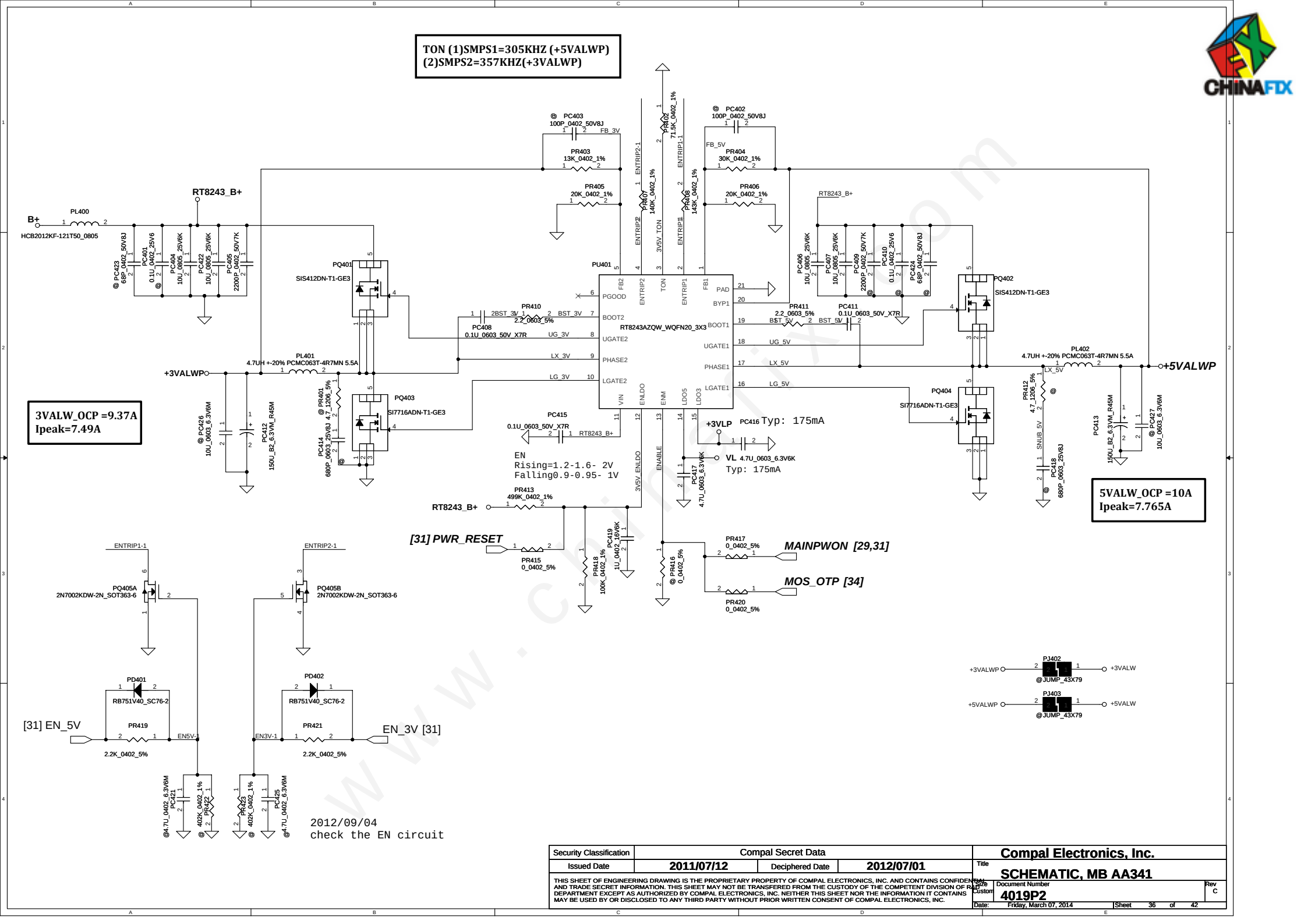

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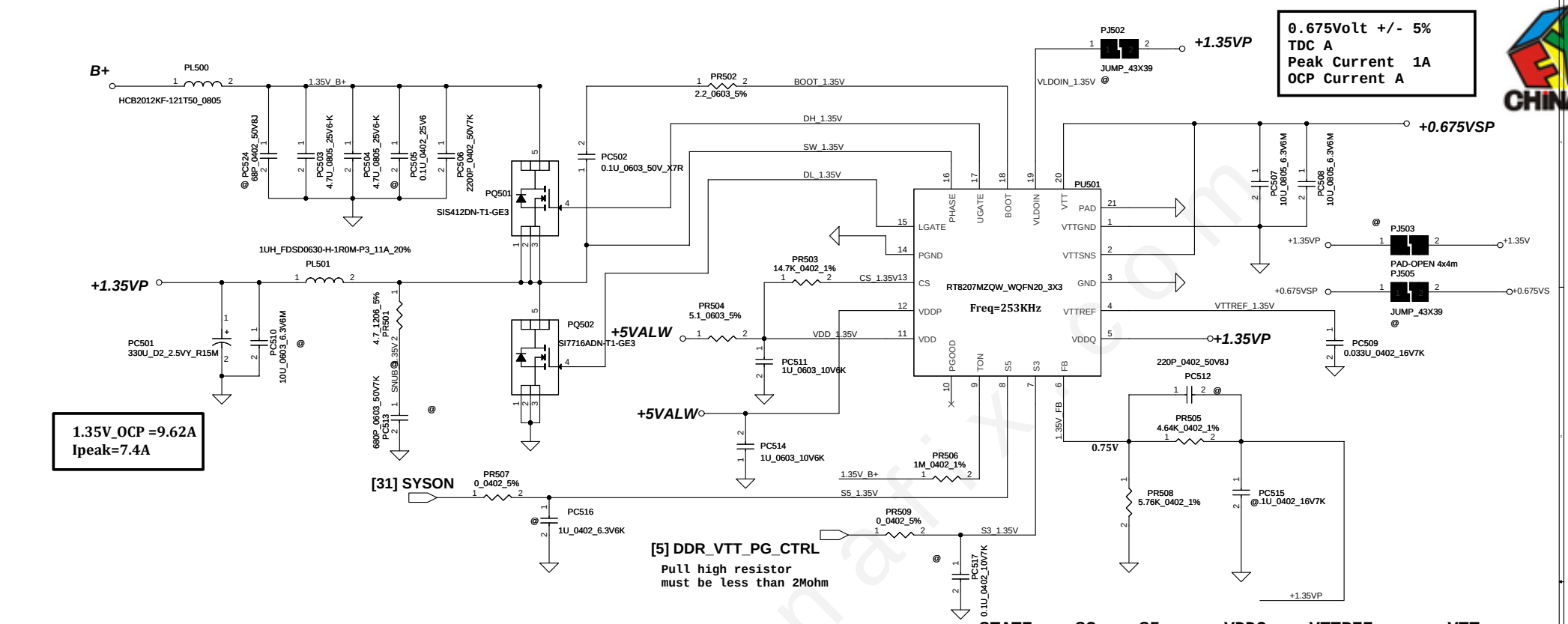
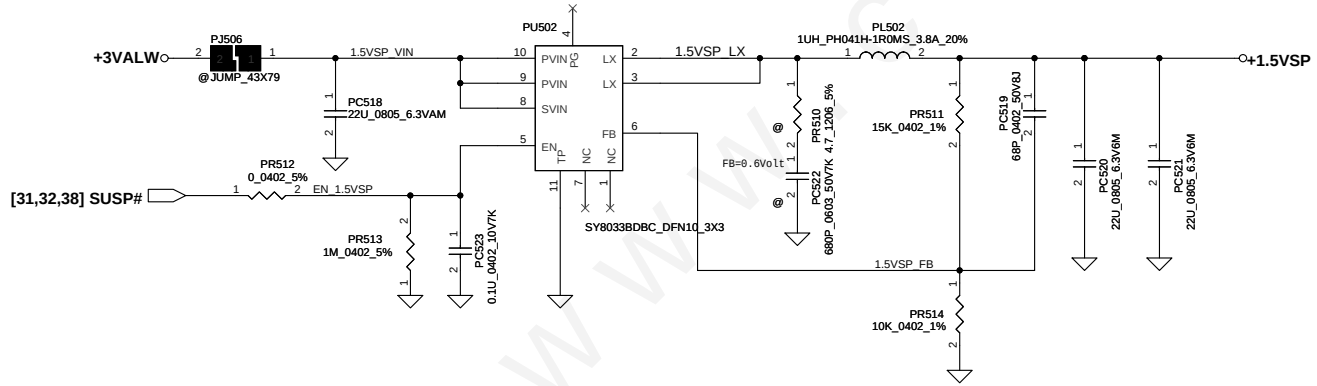
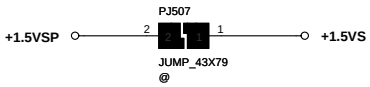


STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)





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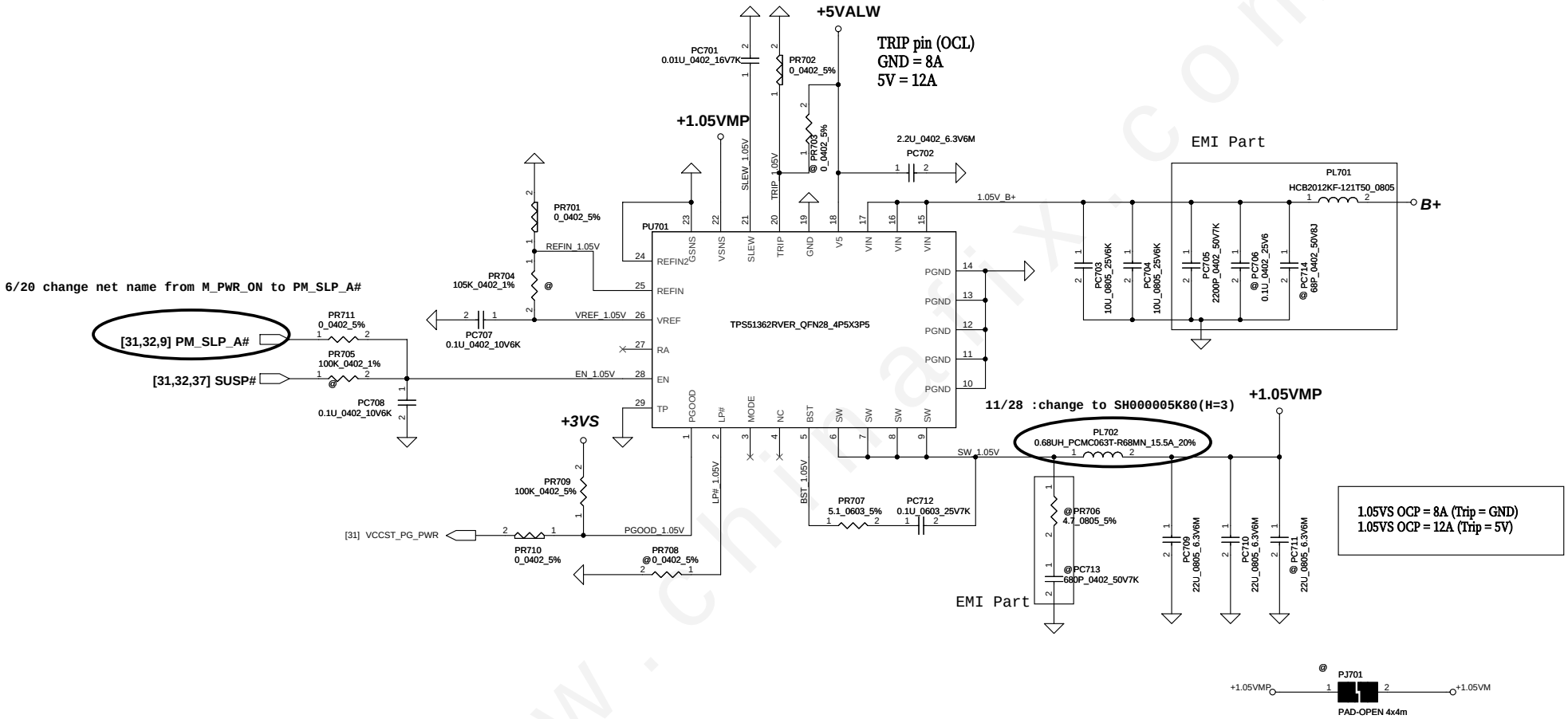

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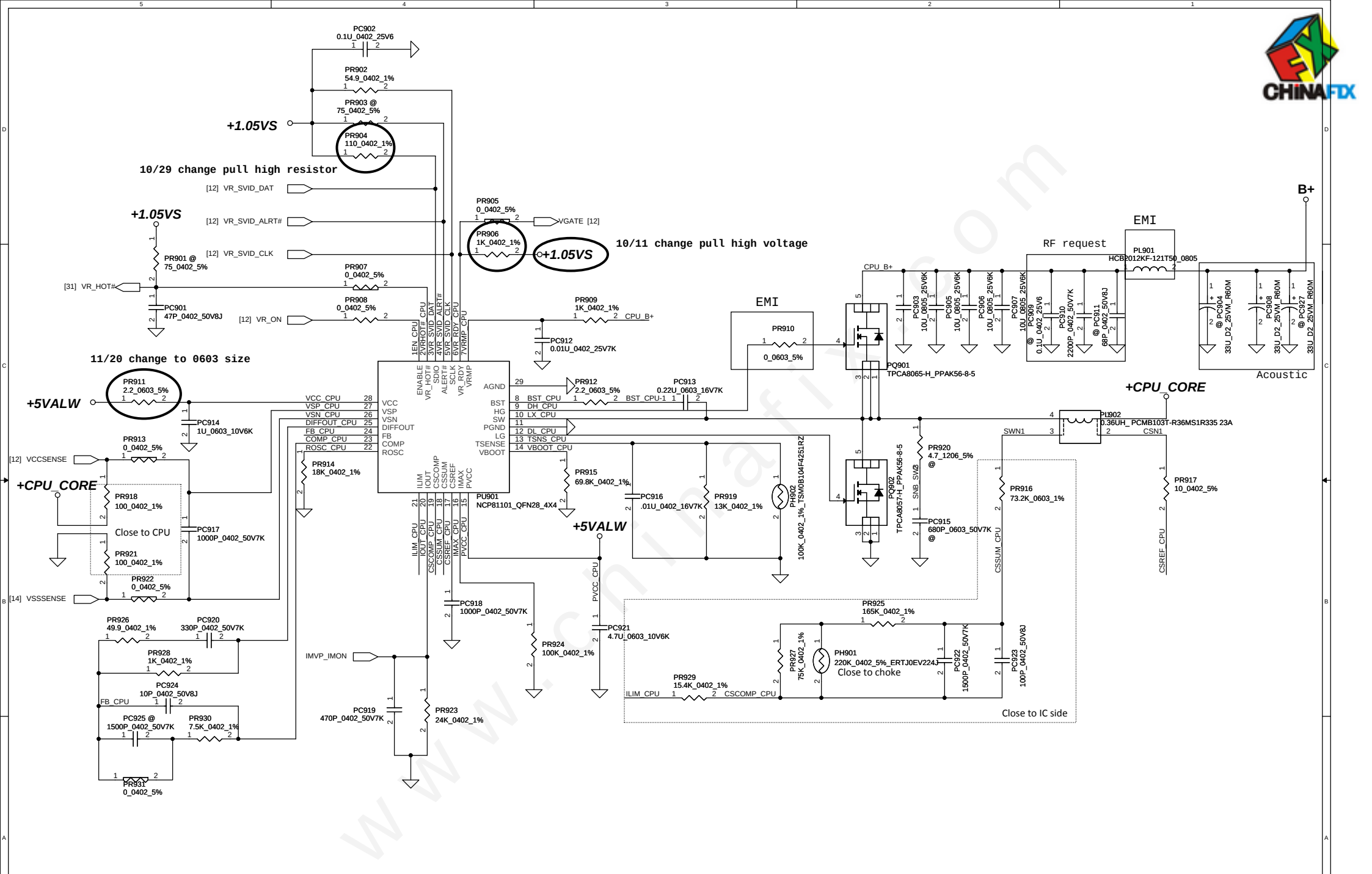

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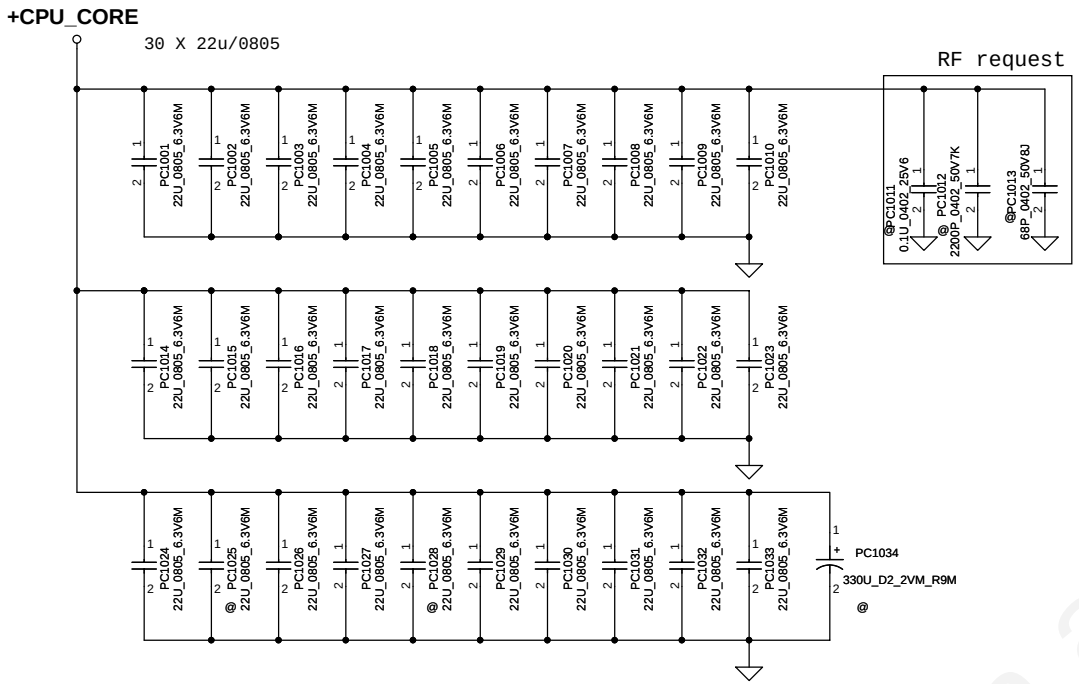

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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title: SCHEMATIC, MB AA341
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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	We just have adpter over-load protection circuit to replace the one-shot circuit, so we can reserve the one-shot circuit.	P33	Un-mount PR119, PC109, PR115, PD105.	2013.04.24	SDV
2	We want to tune the switching ring to meet the derating spec.	P37	Change PC502 from 0.22u to 0.1u.	2013.04.24	SDV
3	For fine tune LL & trainsient of CPU core, we must to change R/C value to meet Intel's spec.	P39	Change PR916 from 47k to 73.2k and PC923 from 560p to 100p, PC1025, PC1028, PC1034 to un-mount.	2013.04.24	SDV
4	For aviod EMI/EMI to damage OP or other components through the loop of BATT_TEMP.	P34	Reserve PD201	2013.04.30	SDV
5					
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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function

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Security Classification	Compal Secret Data		
Issued Date	2013/03/08	Deciphered Date	2015/03/08

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