ZZZ1 PCB DAZ@

PJP1 45@DCIN

ZZZ2 LA-5981P DA2@

ZZZ3 LS-5981P DA2@

ZZZ4 LS-5982P DA2@

ZZZ5 LS-5983P DA2@

ZZZ6 LS-5984P DA2@

ZZZ7 LS-5986P DA2@

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NCQF0 M/B Schematics Document

Intel Arrandale/Clarksfield Processor with DDRIII + Ibex Peak-M

2010-04-18

REV:1.A

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

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Title: Cover Page

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 1 of 63

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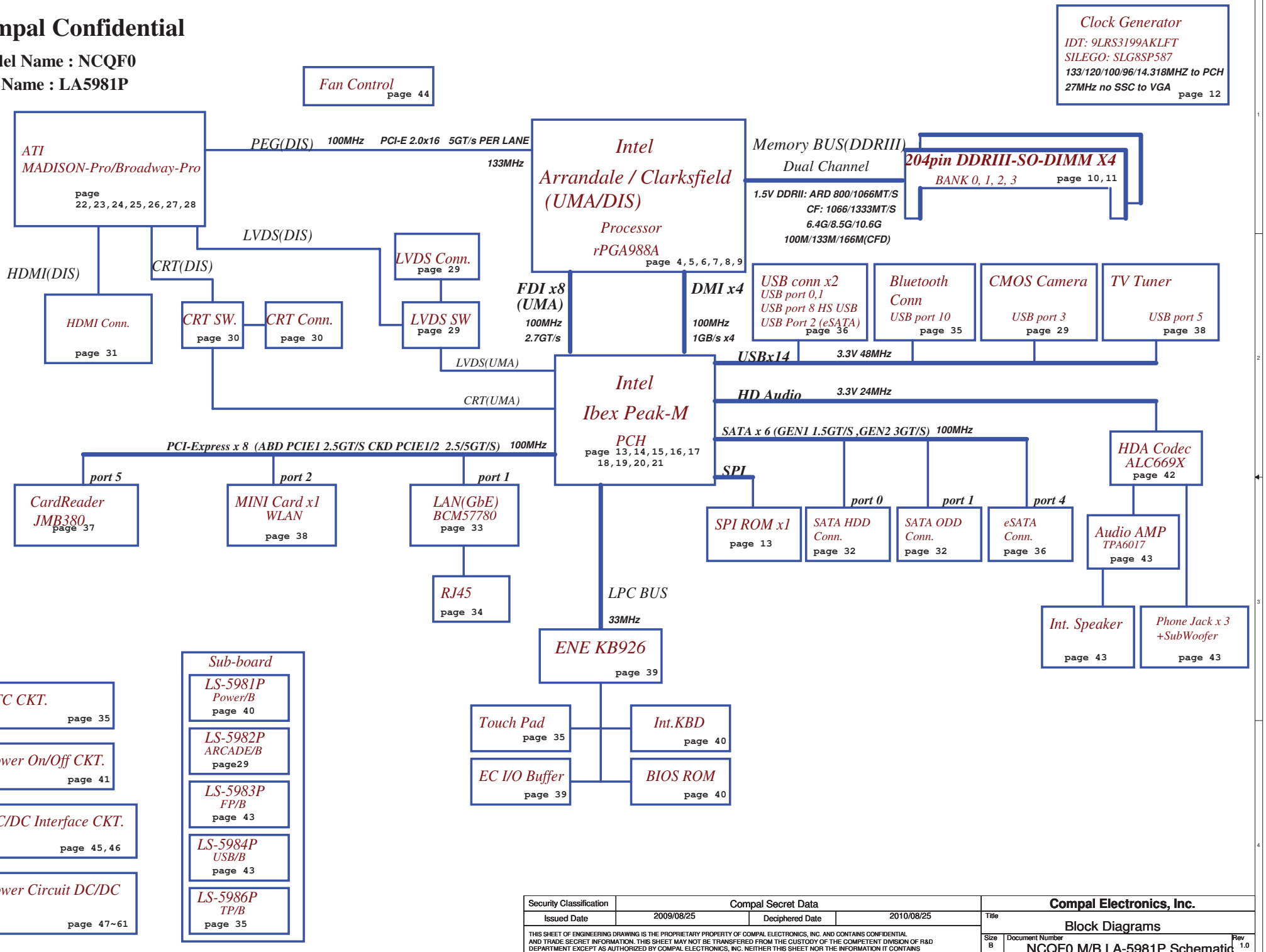
Model Name : NCQF0
File Name : LA5981P



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Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title	Block Diagrams	
Size B	Document Number NCQF0 M/B LA-5981P Schematic	Rev 1.0
Date: Sunday, April 18, 2010	Sheet 2 of 63	

Voltage Rails

Power Plane	Description	S1	S3	S5	DGPU (UMA)	DGPU (DIS)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	ON	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF		
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3V	3.3V power rail for PCH	ON	ON	ON		
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+5V	5V power rail for PCH	ON	ON	ON		
+VSB	VSB always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+5VSDGPU	5V power rail for GPU				OFF	ON
+1.5VSDGPU	1.5V power rail for VRAM				OFF	ON
+1.8VSDGPU	1.8V switched power rail for GPU				OFF	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727 ISL90728	0101 1100b 0111 1100b

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
DIS Only	DIS@
DGPU	VGA@
Broadway	WAY@
Madison	MAD@
Park	PAR@
Switchable Graphics	SG@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB/B
	UHCI1	2	eSATA USB
		3	CMOS Camera
	UHCI2	4	Mini Card 1
		5	Mini Card 2
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Conn.
		9	
	UHCI5	10	Blue Tooth
		11	Finger Print
	UHCI6	12	
		13	

BOM Config
Switchable Graphics (PARK) SKU: SG@/VGA@/PAR@
Switchable Graphics (MADISON) SKU: SG@/VGA@/MAD@
DIS ONLY (BROADWAY): DIS@/VGA@/WAY@

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Title: Notes List

Size: B | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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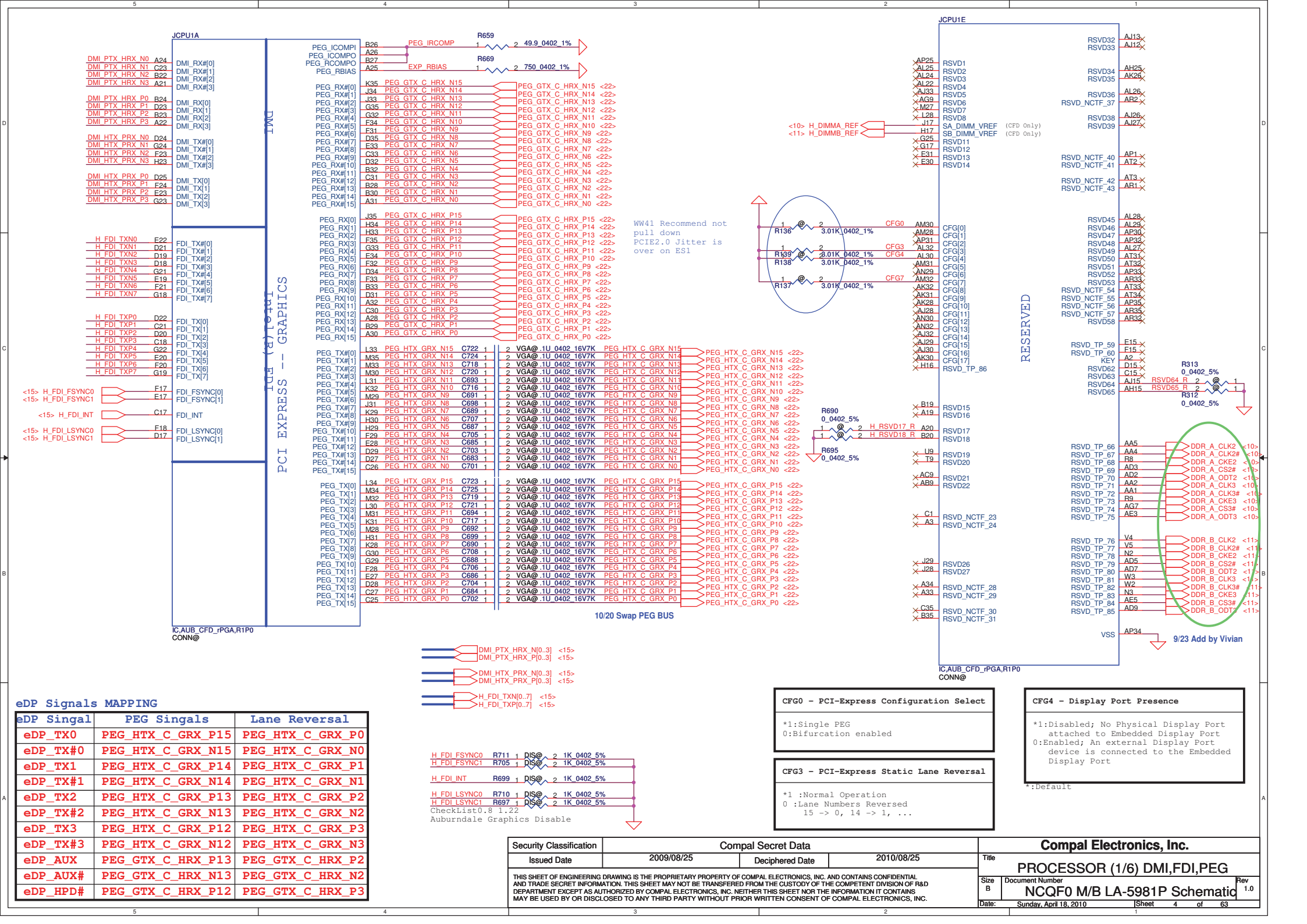

eDP Signals MAPPING

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Title	PROCESSOR (1/6) DMI,FDI,PEG	
Size B	Document Number NCQF0 M/B LA-5981P Schematic	Rev 1.0
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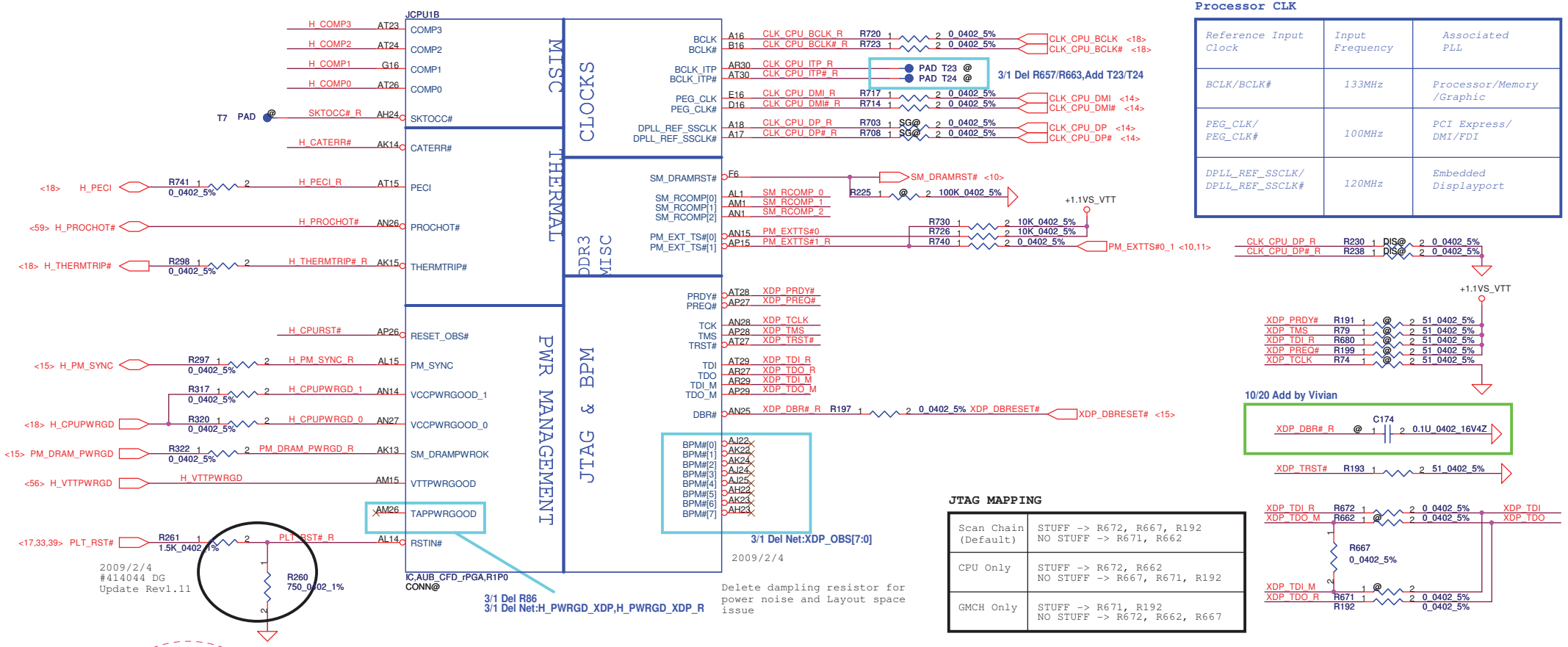
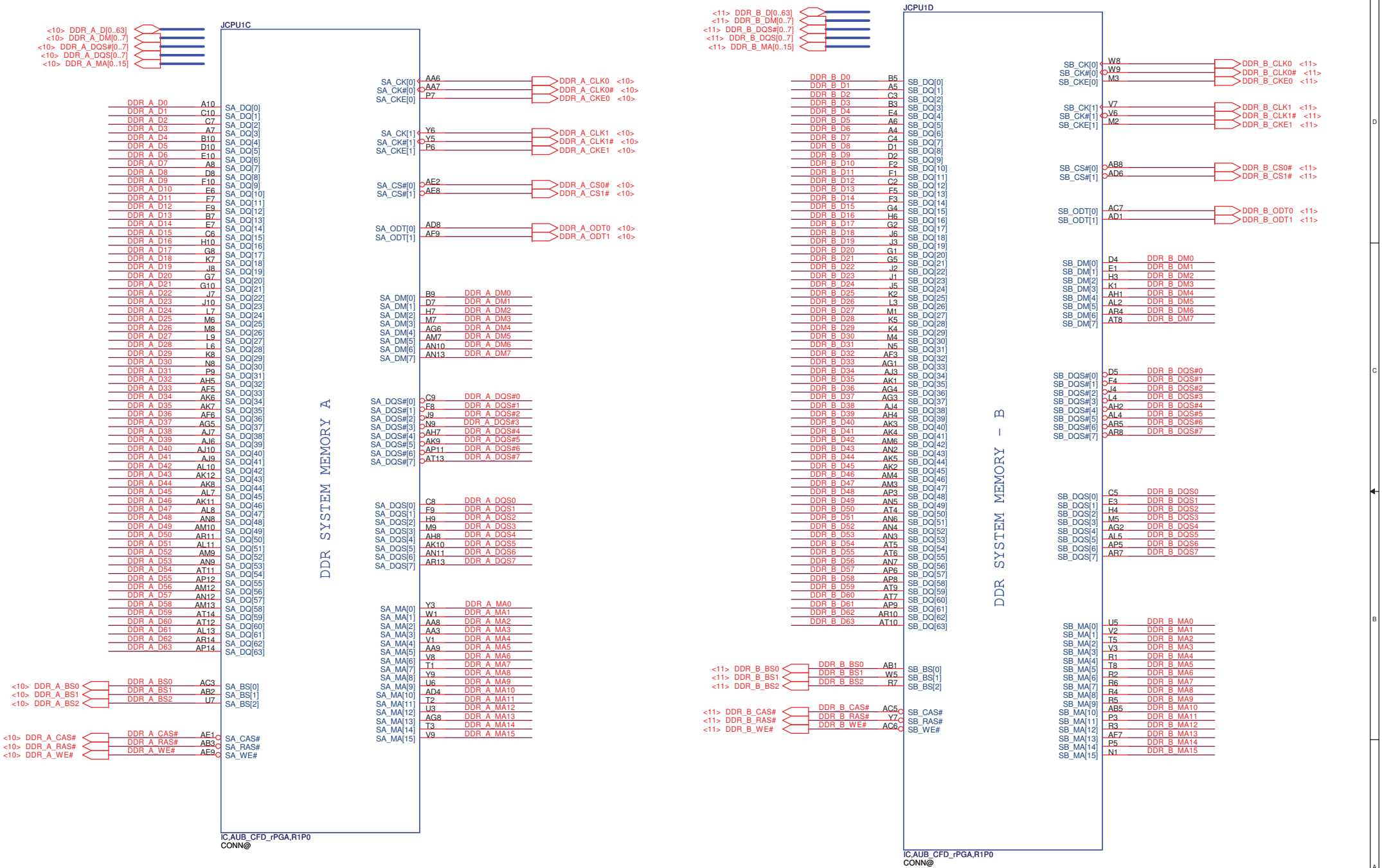


Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	PROCESSOR (2/6) CLK,JTAG		
Size B	Document Number NCQF0 M/B LA-5981P Schematic		Rev 1.0
Date: Sunday, April 18, 2010		Sheet 5 of 63	



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NCQF0 M/B LA-5981P Schematic	1.0

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JCPU1F

+CPU_CORE

WW15 MOW
Peak 21A
Continuous 18A

48A

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

IC,AUB_CFD_rPGA,R1P0
CONN@

+1.1VS_VTT

10U_0805_6.3V6M

22U_0805_6.3V6M

330U_D2E_2VM_R6M

11/13 Change symbol of C799/C800/C802 from SGA00002380 to SGA00002U00(Due to EOL)

CSC (Current Sense Configuration)
8/25

H_VTTVID1 = low, 1.1V
H_VTTVID1 = high, 1.05V

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

Note:CRB has the VTT_SENSE connected through a "no-stuff" 0- series resistor and VSS_SENSE_VTT floating.

(Place these capacitors between inductor and socket on Bottom)

(Place these capacitors under CPU socket, top layer)

(Place these capacitors on CPU cavity, Bottom Layer)

(Place these capacitors on CPU cavity, Bottom Layer)

4 x 330uF(6m ohm@100kHz)

TOP side (under inductor)

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X330uF	6m ohm/4	2X330uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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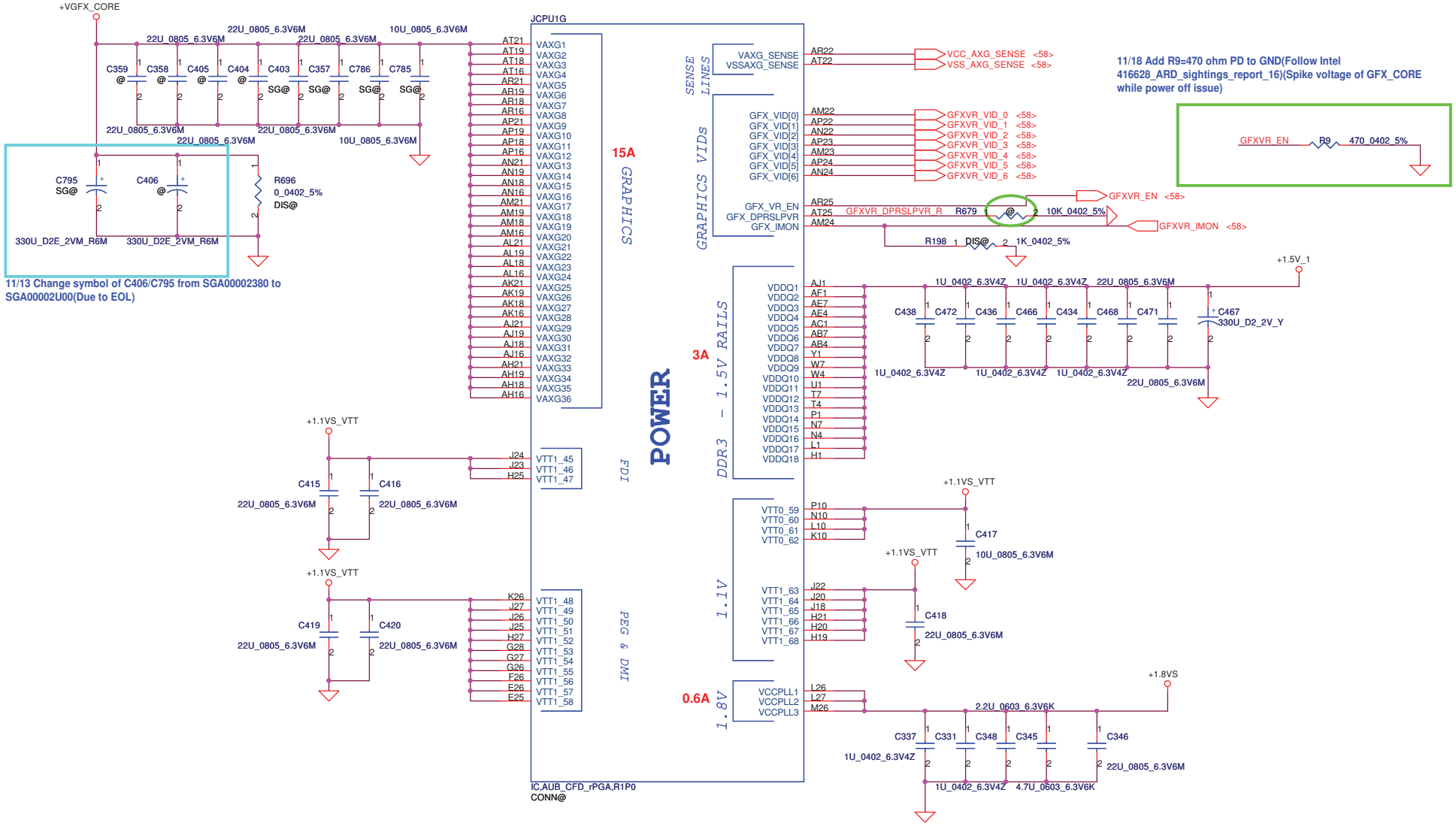

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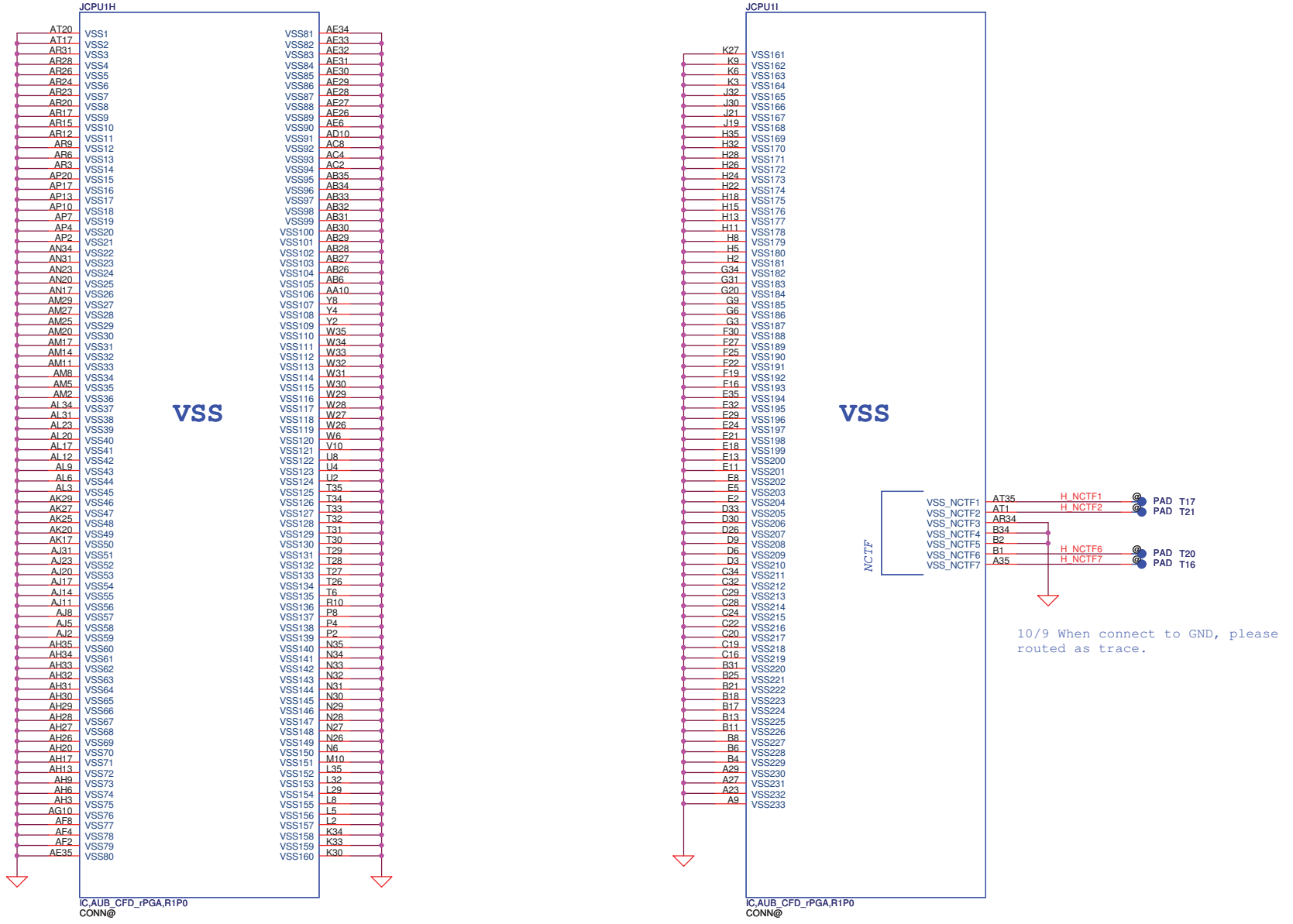
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 Sheet 8 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0

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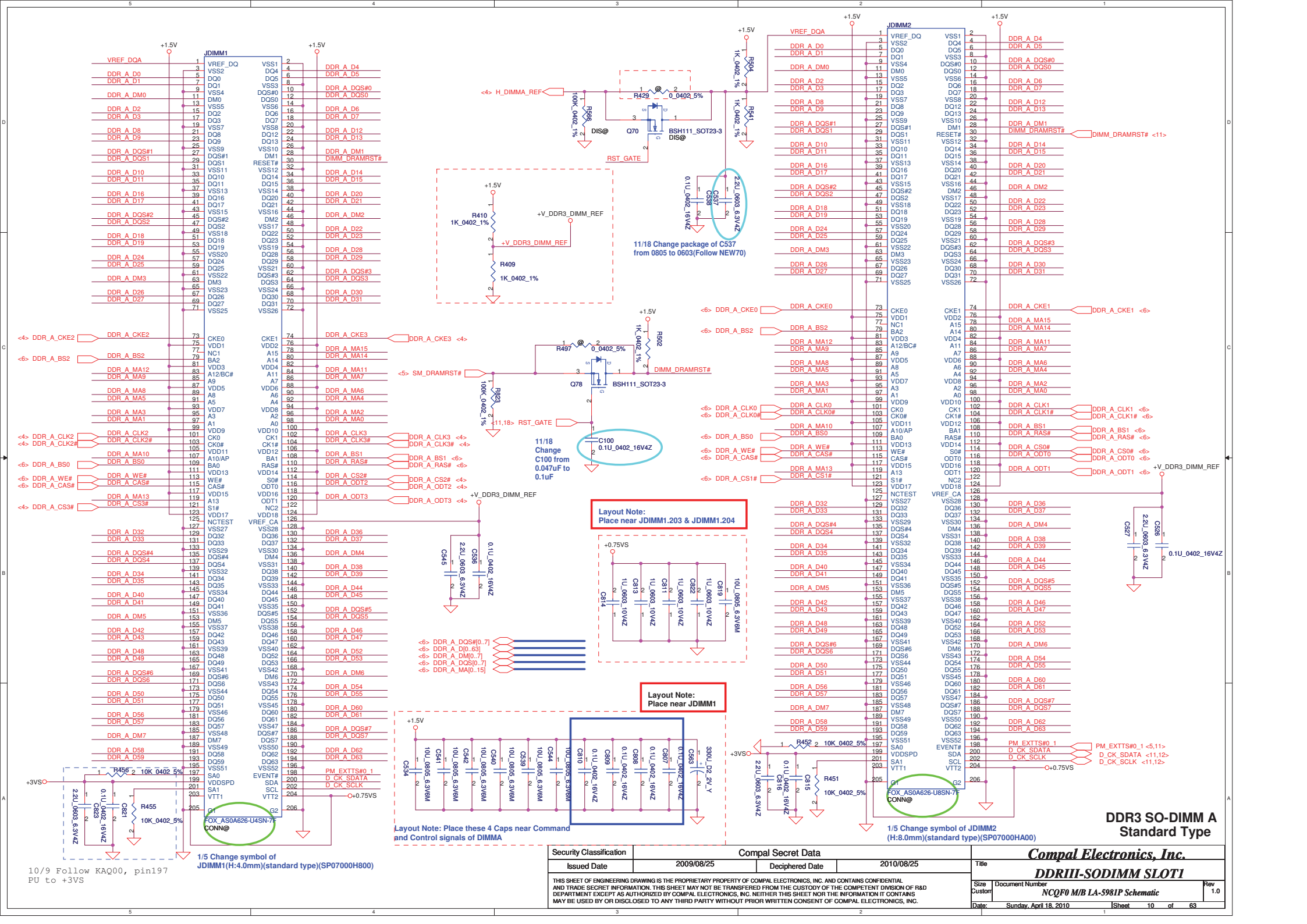

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT1			
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 1.0
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2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

JDIMM4

JDIMM3

Layout Note:
Place near JDIMM2.203 & JDIMM2.204

Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

11/18 Change package of C553 from 0805 to 0603(Follow NEW70)

11/09 Change symbol of JDIMM4 by Vivian(H:8.0mm)(Reverse type)(SP07000M300)

11/09 Change symbol of JDIMM3 by Vivian(H:4.0mm)(Reverse type)(SP07000J500)

10/9 Follow KAQ00, pin197 PU to +3VS

DDR3 SO-DIMM B
Reverse Type

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

Size	Document Number	Rev
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10/9 Change L34 part number
from SM010014520 to SM01000AX00

10/9 Change L39 part number
from SM010014520 to SM01000AX00

10/9 Change L37 part number
from SM010014520 to SM01000AX00

Clock Generator

Integrated 33ohm Resistor

10/19 Add

Integrated 33ohm Resistor

Integrated 33ohm Resistor

12/11 Change PN of U35 to SA00003HR00

LOW Power:
Realtek: RTM890N-631-VB-GRT, SA00003HQ10
*IDT: ICS9LVS3199AKLFT, SA00003HR00

10/27 Place C497/C485/C488 on pin1/pin17/pin24 side(U35)

Silego Have Internal Pull-Up

IDT Have Internal Pull-Down

9/10 Change symbol of Q31/Q32 to SC70-3

9/10 Change symbol of Q29 to SC70-3

9/23 Change C495 to 22pF

update PCB footprint

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

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Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Clock Generator (CK505)

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+RTCVCC R222 20K_0402_1% PCH_RTCRST# RC Delay 18~25mS close to RAM door J4 10K_0603_5% @ C369 1U_0603_10V6K

+RTCVCC R221 20K_0402_1% PCH_SRTCRST# RC Delay 18~25mS close to RAM door J5 10K_0603_5% @ C370 1U_0603_10V6K

C768 18P_0402_50V8J PCH_RTCX1 X2 NC OSC NC OSC R692 10M_0402_5% 32.768KHZ_12.5PF_Q13MC14610002 C766 18P_0402_50V8J PCH_RTCX2

U60A REV1.0 IBEXPEAK-M_FCBGA107

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14

R220 1M_0402_5% SM_INTRUDER#

R223 330K_0402_1% PCH_INTVRMEN

10/5 Change R223 to 330K ohm

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

LPC: FWH0 / LAD0 D33 LPC_AD0, FWH1 / LAD1 B33 LPC_AD1, FWH2 / LAD2 C32 LPC_AD2, FWH3 / LAD3 A32 LPC_AD3, FWH4 / LFRAME# C34 LPC_FRAME#, LDRQ0# A34, LDRQ1# / GPIO23 E34 DCR_R R743 0_0402_5% DCR, SERIRQ AB9 SERIRQ

9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

11/23 Add +3VS R569 20K_0402_5% @ DCR

HDA for AUDIO

<42> HDA_BITCLK_AUDIO R655 33_0402_5% HDA_BITCLK_PCH
<42> HDA_SYNC_AUDIO R660 33_0402_5% HDA_SYNC_PCH
<42> HDA_RST#_AUDIO R653 33_0402_5% HDA_RST#_PCH
<42> HDA_SDOUT_AUDIO R665 33_0402_5% HDA_SDOUT_PCH

If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull under door.

IHDA: HDA_BITCLK_PCH A30, HDA_SYNC_PCH D29, PCH_SPKR P1, HDA_RST#_PCH C30, HDA_SDIN0 G30, HDA_SDIN1 F30, HDA_SDIN2 E32, HDA_SDIN3 F32, HDA_SDO B29

<39,42> PCH_SPKR

SATA for HDD1: SATA0RXN AK7 SATA_DTX_C_PRX_N0, SATA0RXP AK6 SATA_DTX_C_PRX_P0, SATA0TXN AK11 SATA_PTX_DRX_N0, SATA0TXP AK9 SATA_PTX_DRX_P0

SATA for ODD: SATA1RXN AH6 SATA_DTX_C_PRX_N1, SATA1RXP AH5 SATA_DTX_C_PRX_P1, SATA1TXN AH9 SATA_PTX_DRX_N1, SATA1TXP AH8 SATA_PTX_DRX_P1

2/10 SATA2, SATA3 not support on HM55

SATA2RXN AE11, SATA2RXP AE9, SATA2TXN AE7, SATA2TXP AE6

SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1

SATA for eSATA: SATA4RXN AD9 SATA_DTX_C_PRX_N4, SATA4RXP AD8 SATA_DTX_C_PRX_P4, SATA4TXN AD6 SATA_PTX_DRX_N4, SATA4TXP AD5 SATA_PTX_DRX_P4

SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1

GPIO33 can not pull down (manufacturing environments)

HDA_DOCK_EN# / GPIO33 H32, HDA_DOCK_RST# / GPIO13 J30

JTAG: PCH_JTAG_TCK M3, PCH_JTAG_TMS K3, PCH_JTAG_TDI K1, PCH_JTAG_TDO J2, PCH_JTAG_RST# J4

SATAICOMPO AF16, SATAICOMPI AF15, SATA_COMP R208 37.4_0402_1%, +1.05VS

+3VS R319 100K_0402_5% ME_EN# <39> ME_EN SSM3K7002FU_SC70-3 Q22 R321 100K_0402_5%

9/10 Change symbol of Q22 to SC70-3

10/5 Change R287 to 10K ohm

+3VS R287 10K_0402_5% @ PCH_SPKR Have internal PD

R295 10K_0402_5% SERIRQ

SPI: PCH_SPI_CLK_1 R739 0_0402_5% PCH_SPI_CLK BA2, PCH_SPI_CS0# R735 15_0402_5% PCH_SPI_CS0#_R AV3, SPI_CS1# AY3, PCH_SPI_MOSI_1 R736 15_0402_5% PCH_SPI_MOSI AY1, PCH_SPI_MISO_1 R734 0_0402_5% PCH_SPI_MISO AV1

9/3 Remove R738

10/5 Change R734 to 0 ohm

SATALED# T3, SATA0GP / GPIO21 Y9, SATA1GP / GPIO19 V1

+3VS R272 10K_0402_5% PCH_SATALED# PCH_SATALED# <40>

PCH_GPIO21 R292 @ 10K_0402_5%

PCH_GPIO19 R268 @ 10K_0402_5%

+3VS R269 10K_0402_5% R307 10K_0402_5%

PCH Pin	RefDes	PCH JTAG Pre-Production ES1	PCH JTAG Pre-Production ES2	PCH JTAG Production * MP
PCH_JTAG_TDO	R716	No Install	200ohm	No Install
	R713	No Install	100ohm	No Install
PCH_JTAG_TMS	R722	200ohm	200ohm	No Install
	R725	100ohm	100ohm	No Install
PCH_JTAG_TDI	R715	200ohm	200ohm	No Install
	R712	100ohm	100ohm	No Install
PCH_JTAG_TCK	R277	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R304	20Kohm	20Kohm	No Install
	R303	10Kohm	10Kohm	No Install

11/11 Del R278/R718/R719/R728

11/11 Change Bom structure of R303/R304/R712/R713/R715/R716/R722/R725 from mount to @

+3VALW
PCH_JTAG_TMS R722 @ 200_0402_5% R725 @ 100_0402_5%
PCH_JTAG_TDO R716 @ 200_0402_5% R713 @ 100_0402_5%
PCH_JTAG_TDI R715 @ 200_0402_5% R712 @ 100_0402_5%
PCH_JTAG_RST# R304 @ 20K_0402_5% R303 @ 10K_0402_5%

+3VS PCH_SPI_MOSI R732 @ 1K_0402_5%
enable iTPM: SPI_MOSI High

11/11 Change R277 from 4.7K ohm to 51 ohm(Follow 385422 Debug port design guide Rev1.8)

PCH_JTAG_TCK R277 51_0402_5%

+3VS R328 3.3K_0402_5% SPI_WP1# R329 3.3K_0402_5% SPI_HOLD1#
PCH_SPI_CS0# U32 CS# WP# HOLD# GND VCC SCLK SI SO
PCH_SPI_CLK_1 PCH_SPI_MOSI_1 PCH_SPI_MISO_1
S IC FL 32M MX25L3205DM2I-12G SOP 8P

SPI ROM Footprint 150mil

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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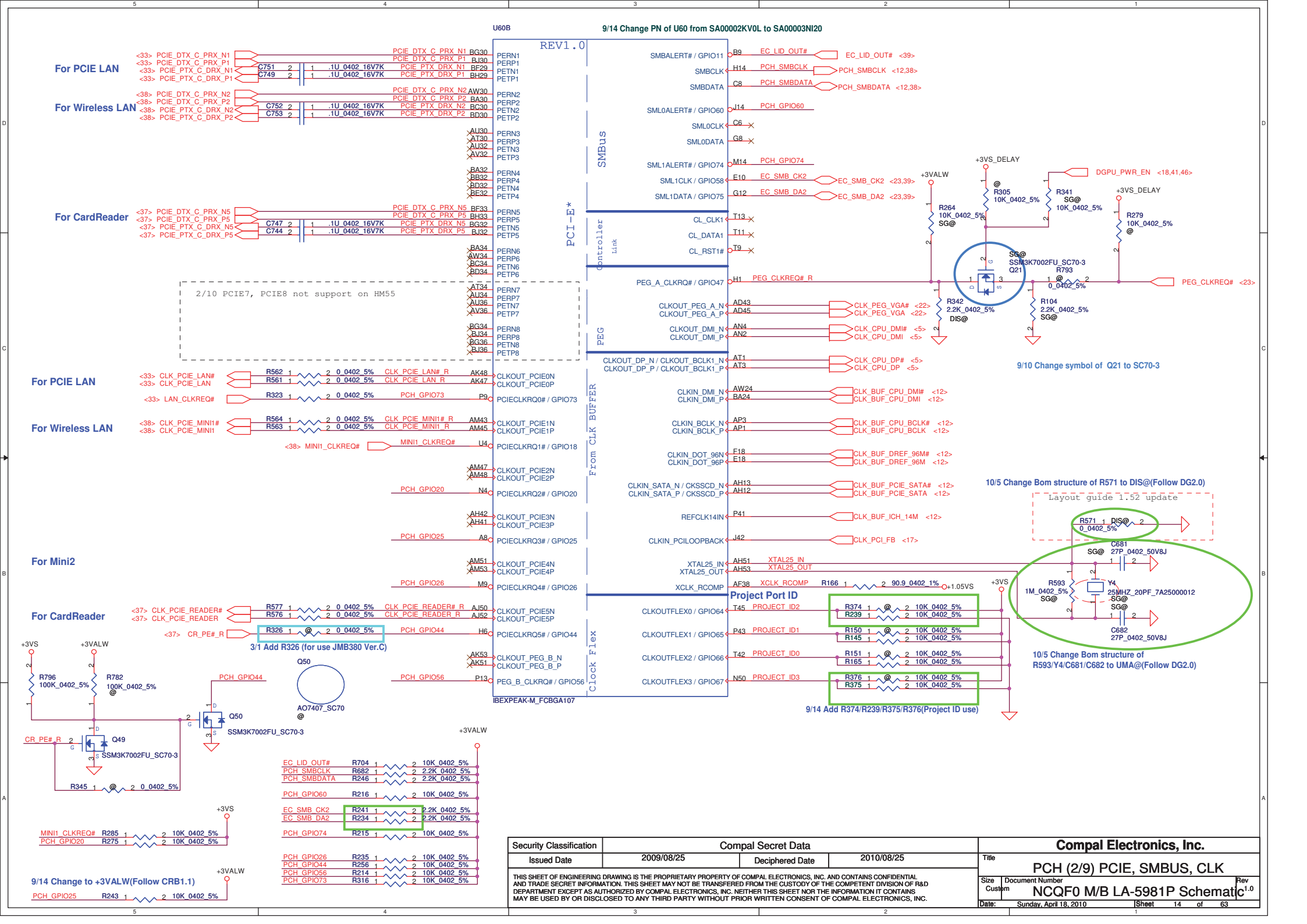

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

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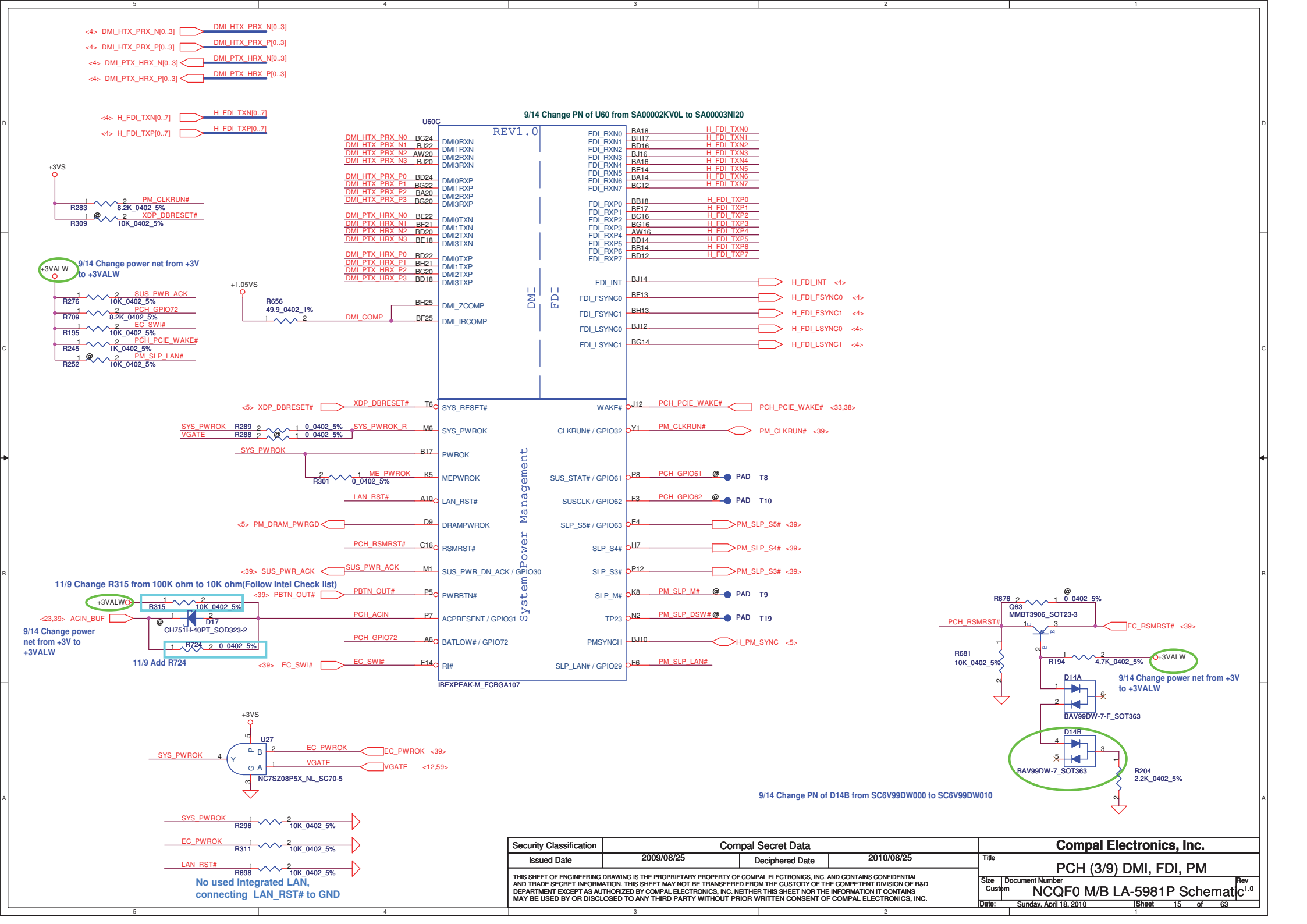

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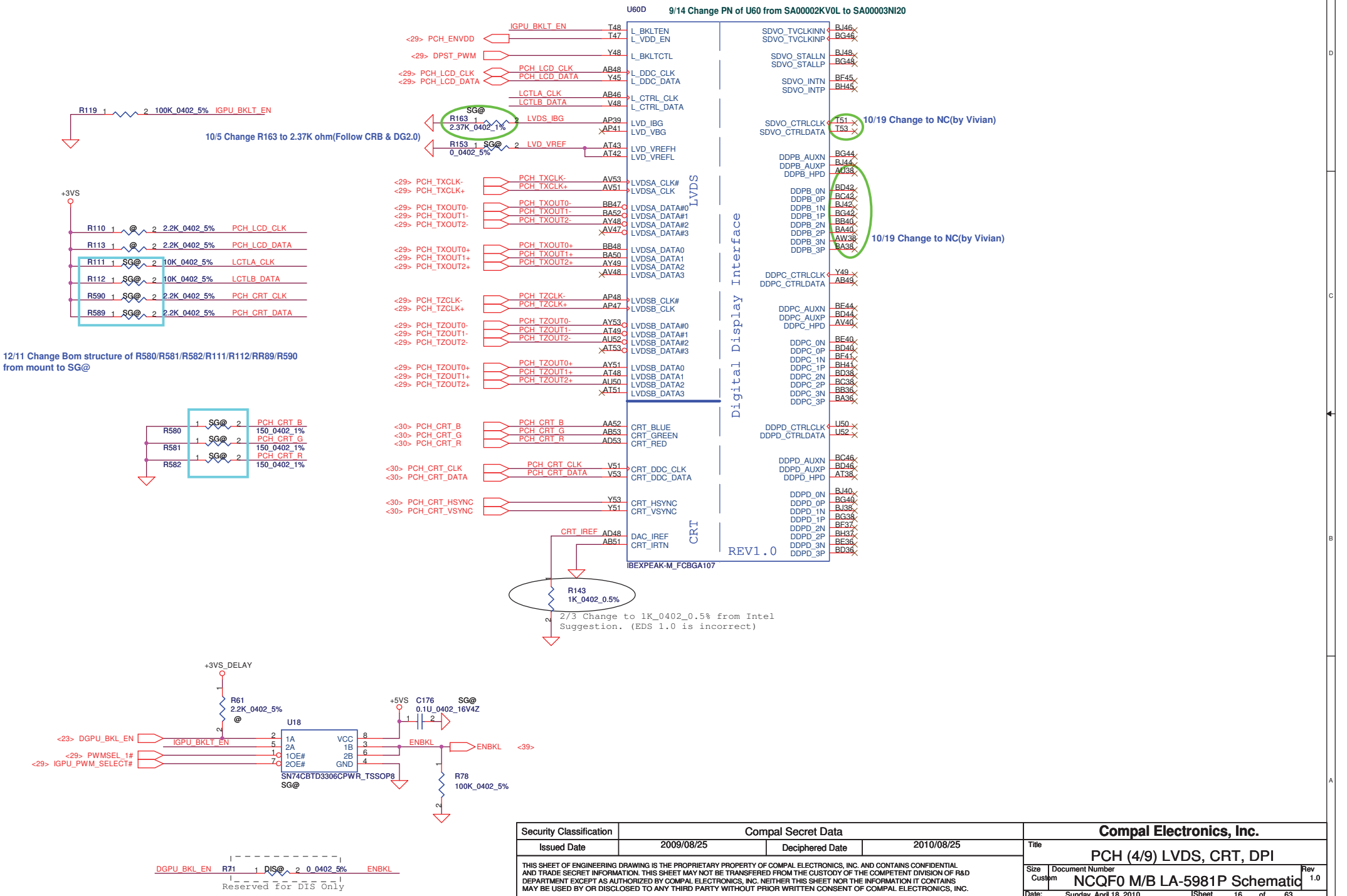


Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 Sheet 16 of 63

9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

11/13 Add RP1~RP5

RP1: DGPU_SELECT#, PCI_PIRQD#, PCI_STOP#, PCI_IRDY# — 8.2K_1206_8P4R_5%

RP2: PCI_PERR#, PCI_DEVSEL#, PCI_PLOCK#, PCI_SERR# — 8.2K_1206_8P4R_5%

RP3: PCI_REQ3#, PCI_PIRQF#, PCI_PIRQB#, PCI_REQ0# — 8.2K_1206_8P4R_5%

RP4: PCI_PIRQH#, PCI_TRDY#, PCI_FRAME#, PCI_REQ1# — 8.2K_1206_8P4R_5%

RP5: PCI_PIRQE#, PCI_PIRQA#, PCI_PIRQC#, PCI_PIRQG# — 8.2K_1206_8P4R_5%

U60E — REV1.0 — IBEXPEAK-M_FCBGA107

PCI: AD0–AD31, C/BE0#–C/BE3#, PIRQA#–PIRQD#, REQ0#, REQ1# / GPIO50, REQ2# / GPIO52, REQ3# / GPIO54, GNT0#, GNT1# / GPIO51, GNT2# / GPIO53, GNT3# / GPIO55, PIRQE# / GPIO2, PIRQF# / GPIO3, PIRQG# / GPIO4, PIRQH# / GPIO5, PCIRST#, SERR#, PERR#, IRDY#, PAR, DEVSEL#, FRAME#, PLOCK#, STOP#, TRDY#, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4

NVRAM: NV_CE#0–NV_CE#3, NV_DQS0, NV_DQS1, NV_DQ0 / NV_IO0 – NV_DQ15 / NV_IO15, NV_ALE, NV_CLE, NV_RCOMP, NV_RB#, NV_WR#0_RE#, NV_WR#1_RE#, NV_WE#_CK0, NV_WE#_CK1

9/4 NC

USB: USBP0N/P – USBP5N/P, USBP6N/P, USBP7N/P, USBP8N/P, USBP9N/P, USBP10N/P – USBP13N/P, USBRBIAS#, USBRBIAS, OC0# / GPIO59 – OC7# / GPIO14

USB Conn.(HS) JUSB1 — USB/B — eSATA USB Conn. — CMOS Camera (LVDS) — Mini Card(WLAN) — Mini Card(Mini2) — EHCI 1

USB Conn.(HS) JUSB2 — Bluetooth — Fingerprint — EHCI 2

R188 22.6_0402_1%

(For USB Port0)
(For USB Port1)
(For eSATA USB Port)
(For USB Port8)

OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

R588 22_0402_5% CLK_PCI_LPC_R
R141 22_0402_5% CLK_PCI_FB_R

2008/1/6 2009MOW01 change to 22 ohm

PCI_GNT0# R123 1K_0402_5% Have internal PU
PCI_GNT1# R149 1K_0402_5% Have internal PU
PCI_GNT3# R585 1K_0402_5% Have internal PU

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

+VCCQ_NAND

NV_ALE R721 1K_0402_5%
NV_CLE R240 1K_0402_5%

U30 NC7SZ08P5X_NL_SC70-5: PLT_RST# → PLT_RST_BUF# <37,38>
R338 100K_0402_5%

U29 NC7SZ08P5X_NL_SC70-5 VGA@: <18> DGPU_HOLD_RST#, R765 0_0402_5% DIS@ → PLTRST_VGA# <22>
R340 100_0402_5% VGA@
R339 100K_0402_5% VGA@

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

11/18 Del RP13
11/18 Add R168/R172/R174/R176(For Layout request)

USB_OC#3_R R168 10K_0402_5%
USB_OC#5_R R172 10K_0402_5%
USB_OC#7_R R174 10K_0402_5%
USB_OC#6_R R176 10K_0402_5%
→ +3VALW

10/27 Change power net from +3V to +3VALW

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 17 of 63

9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

U60F

IBEXPEAK-M_FCBGA107

REV1.0

+3VS

R267 1 2 10K_0402_5% COLOR_ENG_EN_R
R565 1 CIR@ 2 20K_0402_5% CIR_DETECT
R644 1 2 10K_0402_5% DGPU_EDIDSEL#
R271 1 2 10K_0402_5% DGPU_HOLD_RST#_R
R314 1 2 10K_0402_5% CR_CPPE#
R274 1 2 10K_0402_5% CR_WAKE#
R290 1 2 10K_0402_5% DGPU_PWR_EN
R293 1 @ 2 10K_0402_5% DGPU_PRSNT
R294 1 2 10K_0402_5% PCH_GPIO48
R270 1 2 10K_0402_5% PCH_TEMP_ALERT#
R302 1 2 10K_0402_5% PCH_GPIO34
R173 1 2 10K_0402_5% EC_SCI#

+3VALW

R306 1 2 10K_0402_5% PCH_GPIO57
R247 1 2 10K_0402_5% EC_SMI#
R308 1 2 10K_0402_5% PCH_GPIO28
R244 1 2 10K_0402_5% PCH_GPIO12
R262 1 2 10K_0402_5% RST_GATE
R258 1 2 10K_0402_5% PCH_GPIO45

9/14 Change power net from +3V to +3VALW

10/9 DGPU_PRSNT represent VGA exist indicator.

11/23 Add R572

R333 1 VGA@ 2 10K_0402_5% DGPU_PRSNT
R155 1 @ 2 10K_0402_5% DGPU_PWROK_BUF_R
R291 1 2 10K_0402_5% PCH_GPIO35
R371 1 2 1K_0402_5% CIR_DETECT
NON_CIR@

+3VS
R266 10K_0402_5%
High: CRT Plugged
CRT_DET
<30> CRT_DET#
SSM3K7002FU_SC70-3 Q20

10/26 Change R371 from 10k ohm to 1K ohm

9/10 Change symbol of Q20 to SC70-3

+3VALW
R310 1K_0402_5%
VGA_HDMI_DET#
<31> HDMI_HPD
HDMI_HPD
SSM3K7002FU_SC70-3 Q23

1/11 Change net name from VGA_HDMI_DET to HDMI_HPD

10/5 Add Q23

CRT_DET Y3 BMBUSY# / GPIO0
<29> DGPU_EDIDSEL# DGPU_EDIDSEL# C38 TACH1 / GPIO1
CIR_DETECT D37 TACH2 / GPIO6
<39> EC_SCI# EC_SCI# J32 TACH3 / GPIO7
<39> EC_SMI# EC_SMI# F10 GPIO8
(GPIO8 Should not be Pull-Low)
PCH_GPIO12 K9 LAN_PHY_PWR_CTRL / GPIO12
VGA_HDMI_DET# T7 GPIO15
<17> DGPU_HOLD_RST# R224 0_0402_5% SG@ DGPU_HOLD_RST#_R AA2 SATA4GP / GPIO16
<41> VGA_PWROK_BUF R152 0_0402_5% DGPU_PWROK_BUF_R F38 TACH0 / GPIO17
<37> CR_CPPE# CR_CPPE# Y7 SCLOCK / GPIO22
(Rev:1.0 GPIO24 Only)
H10 GPIO24
11/9 Remove
AB12 GPIO27
PCH_GPIO28 V13 GPIO28
PCH_GPIO34 M11 STP_PCI# / GPIO34
PCH_GPIO35 V6 SATACLKREQ# / GPIO35
<14,41,46> DGPU_PWR_EN DGPU_PWR_EN AB7 SATA2GP / GPIO36
DGPU_PRSNT AB13 SATA3GP / GPIO37
<29> COLOR_ENG_EN R572 0_0402_5% COLOR_ENG_EN_R V3 SLOAD / GPIO38
<37> CR_WAKE# CR_WAKE# P3 SDATAOUT0 / GPIO39
PCH_GPIO45 H3 PCIECLKRQ6# / GPIO45
<10,11> RST_GATE RST_GATE F1 PCIECLKRQ7# / GPIO46
PCH_GPIO48 AB6 SDATAOUT1 / GPIO48
<39> PCH_TEMP_ALERT# PCH_TEMP_ALERT# AA4 SATA5GP / GPIO49
PCH_GPIO57 F8 GPIO57

GPIO

CLKOUT_PCIE6N AH45
CLKOUT_PCIE6P AH46
CLKOUT_PCIE7N AF48
CLKOUT_PCIE7P AF47
A20GATE U2 EC_GA20 <39>
CLKOUT_BCLK0_N / CLKOUT_PCIE8N AM3 CLK_CPU_BCLK# <5>
CLKOUT_BCLK0_P / CLKOUT_PCIE8P AM1 CLK_CPU_BCLK <5>
PECI BG10 H_PECI <5>
RCIN# T1 EC_KBRST# EC_KBRST# <39>
PROCPWRGD BE10 H_CPUPWRGD <5>
THRMTRIP# BD10 THRMTRIP_PCH# 2 R233 1 56_0402_5% H_THERMTRIP# H_THERMTRIP# <5>
2 R232 1 56_0402_5% +1.1VS_VTT

CPU

MISC

EC_GA20 R286 1 2 10K_0402_5%
EC_KBRST# R284 1 2 10K_0402_5%

WW46 Platform/Design Updates
2008/11/17 54.9 1% ->56 5%

TP1 BA22
TP2 AW22
TP3 BB22
TP4 AY45
TP5 AY46
TP6 AV43
TP7 AV45
TP8 AF13
TP9 M18
TP10 N18
TP11 AJ24
TP12 AK41
TP13 AK42
TP14 M32
TP15 N32
TP16 M30
TP17 N30
TP18 H12
TP19 AA23
NC_1 AB45
NC_2 AB38
NC_3 AB42
NC_4 AB41
NC_5 T39
INIT3_3V# P6
TP24 C10 TP24_SST @ PAD T18

(Have internal PD, Do not pull high)

NCTF

RSVD

VSS_NCTF_1 A4
VSS_NCTF_2 A49
VSS_NCTF_3 A5
VSS_NCTF_4 A50
VSS_NCTF_5 A52
VSS_NCTF_6 A53
VSS_NCTF_7 B2
VSS_NCTF_8 B4
VSS_NCTF_9 B52
VSS_NCTF_10 B53
VSS_NCTF_11 BE1
VSS_NCTF_12 BE53
VSS_NCTF_13 BF1
VSS_NCTF_14 BF53
VSS_NCTF_15 BH1
VSS_NCTF_16 BH2
VSS_NCTF_17 BH52
VSS_NCTF_18 BH53
VSS_NCTF_19 BJ1
VSS_NCTF_20 BJ2
VSS_NCTF_21 BJ4
VSS_NCTF_22 BJ49
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ50
VSS_NCTF_25 BJ52
VSS_NCTF_26 BJ53
VSS_NCTF_27 D1
VSS_NCTF_28 D2
VSS_NCTF_29 D53
VSS_NCTF_30 E1
VSS_NCTF_31 E53

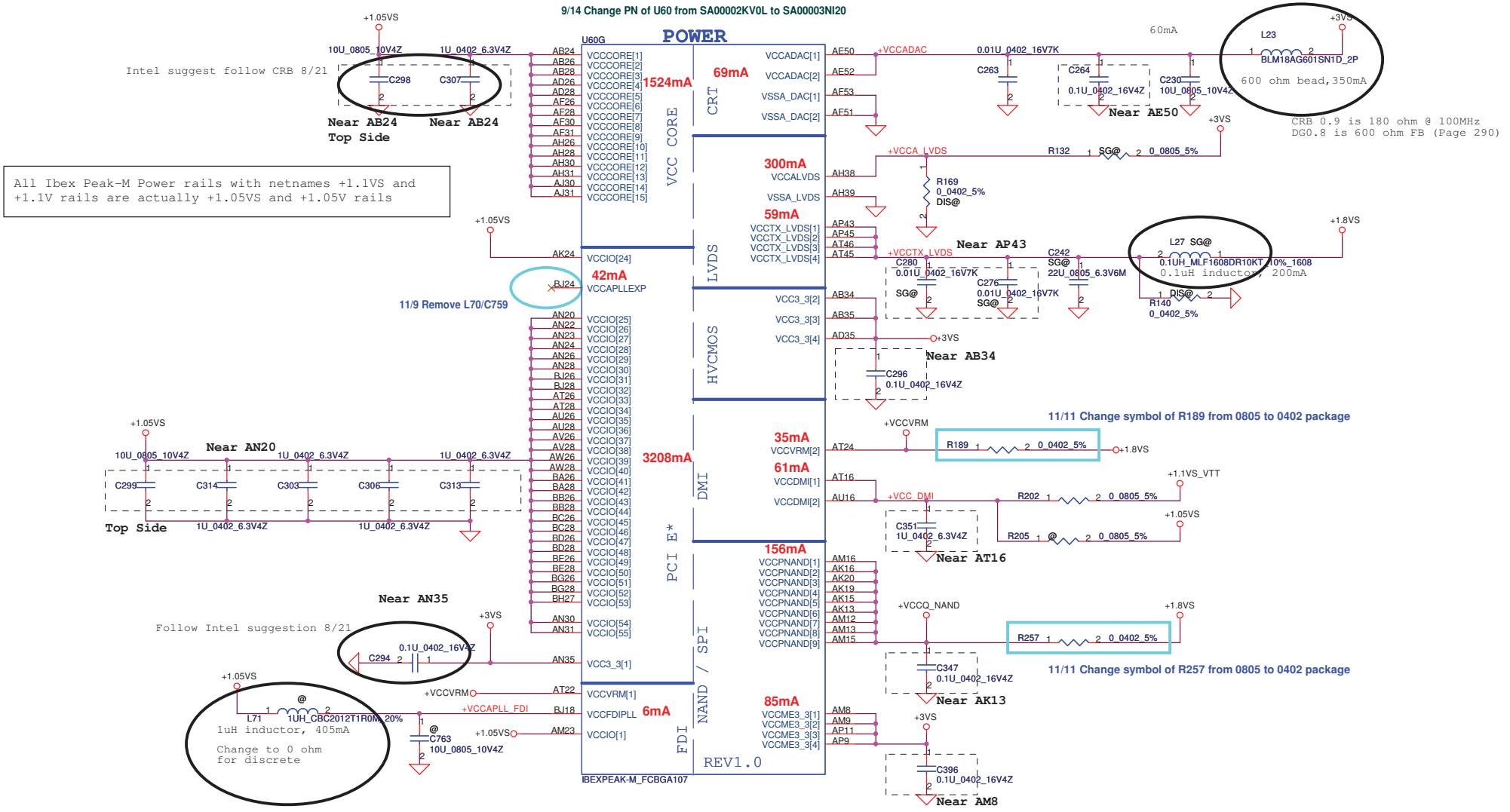
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

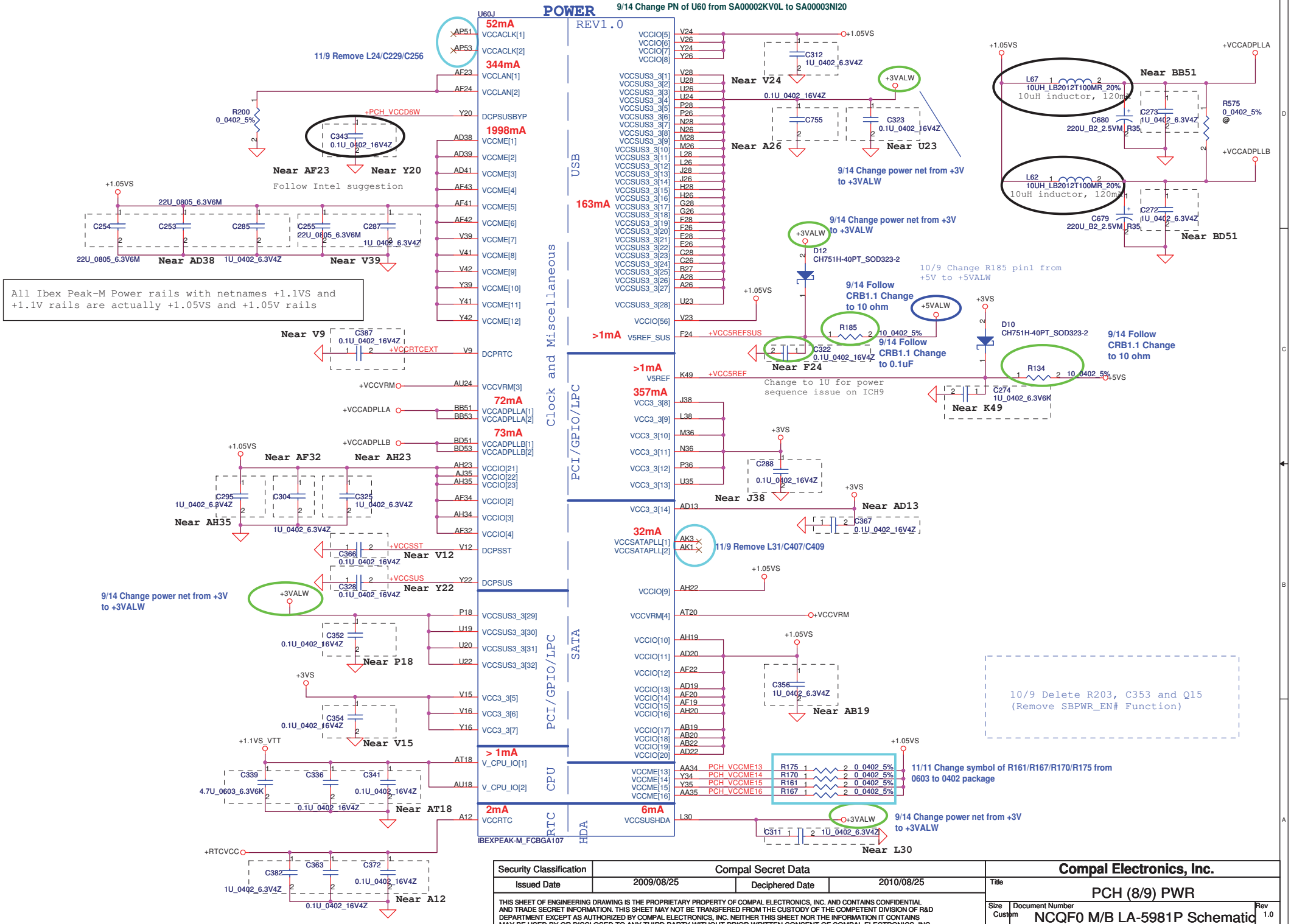
Date: Sunday, April 18, 2010 | Sheet 18 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title	PCH (7/9) PWR
Size / Document Number	Custom / NCQF0 M/B LA-5981P Schematic
Rev	1.0
Date:	Sunday, April 18, 2010
Sheet	19 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 20 of 63

U60I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BE6	VSS[206]	VSS[306]	U34
BE8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
E6	VSS[238]	VSS[338]	Y38
E8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AF39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK39
H38	VSS[257]	VSS[366]	AV14
H42	VSS[258]		

REV1.0

IBEXPEAK-M_FCBGA107

9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

U60H

AB16	VSS[0]		
AA19	VSS[1]	VSS[80]	AK30
AA20	VSS[2]	VSS[81]	AK31
AA22	VSS[3]	VSS[82]	AK32
AM19	VSS[4]	VSS[83]	AK34
AA24	VSS[5]	VSS[84]	AK35
AA26	VSS[6]	VSS[85]	AK38
AA28	VSS[7]	VSS[86]	AK43
AA30	VSS[8]	VSS[87]	AK46
AA31	VSS[9]	VSS[88]	AK49
AA32	VSS[10]	VSS[89]	AK5
AB11	VSS[11]	VSS[90]	AK8
AB15	VSS[12]	VSS[91]	AL2
AB23	VSS[13]	VSS[92]	AL52
AB30	VSS[14]	VSS[93]	AM11
AB31	VSS[15]	VSS[94]	BB44
AB32	VSS[16]	VSS[95]	AD24
AB39	VSS[17]	VSS[96]	AM20
AB43	VSS[18]	VSS[97]	AM22
AB47	VSS[19]	VSS[98]	AM24
AB5	VSS[20]	VSS[99]	AM26
AB8	VSS[21]	VSS[100]	AM28
AC2	VSS[22]	VSS[101]	BA42
AC52	VSS[23]	VSS[102]	AM30
AD11	VSS[24]	VSS[103]	AM31
AD12	VSS[25]	VSS[104]	AM32
AD16	VSS[26]	VSS[105]	AM34
AD23	VSS[27]	VSS[106]	AM35
AD30	VSS[28]	VSS[107]	AM38
AD31	VSS[29]	VSS[108]	AM39
AD32	VSS[30]	VSS[109]	AM42
AD34	VSS[31]	VSS[110]	AU20
AU22	VSS[32]	VSS[111]	AM46
AD42	VSS[33]	VSS[112]	AV22
AD46	VSS[34]	VSS[113]	AM49
AD49	VSS[35]	VSS[114]	AM7
AD7	VSS[36]	VSS[115]	AA50
AE2	VSS[37]	VSS[116]	BB10
AE4	VSS[38]	VSS[117]	AN32
AF12	VSS[39]	VSS[118]	AN50
Y13	VSS[40]	VSS[119]	AN52
AH49	VSS[41]	VSS[120]	AP12
AU4	VSS[42]	VSS[121]	AP42
AF35	VSS[43]	VSS[122]	AP46
AP13	VSS[44]	VSS[123]	AP49
AN34	VSS[45]	VSS[124]	AP5
AF45	VSS[46]	VSS[125]	AP8
AF46	VSS[47]	VSS[126]	AR2
AF49	VSS[48]	VSS[127]	AR52
AF5	VSS[49]	VSS[128]	AT11
AF8	VSS[50]	VSS[129]	BA12
AG2	VSS[51]	VSS[130]	AH48
AG52	VSS[52]	VSS[131]	AT32
AH11	VSS[53]	VSS[132]	AT36
AH15	VSS[54]	VSS[133]	AT41
AH16	VSS[55]	VSS[134]	AT47
AH24	VSS[56]	VSS[135]	AT7
AH32	VSS[57]	VSS[136]	AV12
AV18	VSS[58]	VSS[137]	AV16
AH43	VSS[59]	VSS[138]	AV20
AH47	VSS[60]	VSS[139]	AV24
AH7	VSS[61]	VSS[140]	AV30
AJ19	VSS[62]	VSS[141]	AV34
AJ2	VSS[63]	VSS[142]	AV38
AJ20	VSS[64]	VSS[143]	AV42
AJ22	VSS[65]	VSS[144]	AV46
AJ23	VSS[66]	VSS[145]	AV49
AJ26	VSS[67]	VSS[146]	AV5
AJ28	VSS[68]	VSS[147]	AV8
AJ32	VSS[69]	VSS[148]	AW14
AJ34	VSS[70]	VSS[149]	AW18
AT5	VSS[71]	VSS[150]	AW2
AJ4	VSS[72]	VSS[151]	BF9
AK12	VSS[73]	VSS[152]	AW32
AM41	VSS[74]	VSS[153]	AW36
AN19	VSS[75]	VSS[154]	AW40
AK26	VSS[76]	VSS[155]	AW52
AK22	VSS[77]	VSS[156]	AY11
AK23	VSS[78]	VSS[157]	AY43
AK28	VSS[79]	VSS[158]	AY47

REV1.0

IBEXPEAK-M_FCBGA107

9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

1. dGPU Power On at Post

(1) Check DGPU_PRSNT (GPIO37) is low

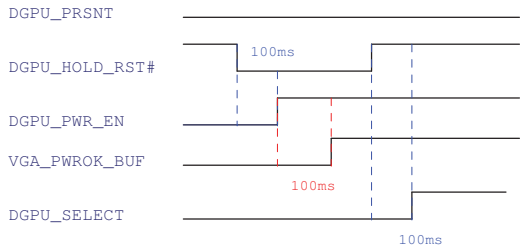
(2) Hold DGPU_HOLD_RST# (GPIO16) low, and wait for 100ms

(3) Set DGPU_PWR_EN (GPIO36) high, and wait for 100ms

(4) If, after 100 ms, VGA_PWROK_BUF (GPIO17) is not asserted high, then it is a fatal error

(5) Set DGPU_HOLD_RST# pin high and wait 100ms

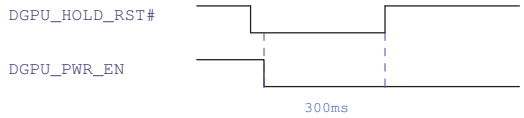
(6) DGPU_SELECT is high



2. dGPU Power On at Runtime

(1) 3 interposer
- Ⅰ. DGPU_HOLD_RST# held low
- Ⅱ. DGPU_PWR_EN held high to turn on DGPU
- Ⅲ. Delay 300ms

(2) DGPU_HOLD_RST# held high



3. dGPU Power OFF at Runtime

(1) Set DGPU_HOLD_RST# low

(2) Set DGPU_PWR_EN low

DGPU_PWR_EN:
-Driven by BIOS to turn on/off discrete graphic power.

VGA_PWROK_BUF:
-Driven by dGPU VR to indicate the power status to PCH.
-Used to enable clocks to dGPU.

DGPU_HOLD_RST#:
-Discrete Graphic Enable signal. Controlled by BIOS and driven by PCH GPIO.
-Used to gate with Platform Reset to enable the Reset for DGPU.

DGPU_SELECT:
-Select line for MUX to control the Display from iGPU or dGPU
-Needs to be controlled by BIOS.

DGPU_PWM_SELECT#
-Select line for MUX to control Backlight Inverter from iGPU or dGPU.

EDID_SELECT#
-Select line for MUX to control EDID from iGPU or dGPU.

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 21 of 63

10/14 Add By Vivian

U54 — 216-0769010 BROADWAY WAY@

U54 — 216-0774007 PARK PAR@

U54A

PCI EXPRESS INTERFACE

<4> PEG_HTX_C_GRX_P0	PEG_HTX_C_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_GTX_HRX_P0	C66	2 VGA@.1U_0402_16V7K	PEG_GTX_C_HRX_P0 <4>
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CLOCK

<14> CLK_PEG_VGA	CLK_PEG_VGA	AB35	PCIE_REFCLKP
<14> CLK_PEG_VGA#	CLK_PEG_VGA#	AA36	PCIE_REFCLKN

	AJ21		NC#1
	AK21		NC#2
<41,57> VGA_PWROK	VGA_PWROK	AH16	PWRGOOD
<17> PLTRST_VGA#	PLTRST_VGA#	AA30	PERSTB

CALIBRATION

PCIE_CALRP	Y30	PCIE_CALRP	R75 1 VGA@ 2	1.27K_0402_1%
PCIE_CALRN	Y29	PCIE_CALRN	R82 1 VGA@ 2	2K_0402_1%

VGA_PWROK — R517 @ 1 2 — VGA_PWROK_R — 0_0402_5%

VGA_PWROK_R — R766 10K_0402_1% VGA@

+1.0VSDGPU

216-0772000 MADISON — MAD@

10/6 Change symbol of U54 to Madison-M2

M96 P/N : SA00002UQ50 (S IC 216-0729042-00 A13 M96 FCBGA962 0FA)

9/14 Change poewr net to +1.0VSDGPU

ENVDD — R88 10K_0402_5% VGA@

VGA_PNL_PWM — R84 10K_0402_5% VGA@

add for DPST support.

U54G

LVDS CONTROL

VARY_BL	AK27	VGA_PNL_PWM	VGA_PNL_PWM <29>
DIGON	AJ27	ENVDD	ENVDD <29>

TXCLK_UP_DPF3P	AK35	VGA_TZCLK+	VGA_TZCLK+ <29>
TXCLK_UN_DPF3N	AL36	VGA_TZCLK-	VGA_TZCLK- <29>
TXOUT_U0P_DPF2P	AJ38	VGA_TZOUT0+	VGA_TZOUT0+ <29>
TXOUT_U0N_DPF2N	AK37	VGA_TZOUT0-	VGA_TZOUT0- <29>
TXOUT_U1P_DPF1P	AH35	VGA_TZOUT1+	VGA_TZOUT1+ <29>
TXOUT_U1N_DPF1N	AJ36	VGA_TZOUT1-	VGA_TZOUT1- <29>
TXOUT_U2P_DPF0P	AG38	VGA_TZOUT2+	VGA_TZOUT2+ <29>
TXOUT_U2N_DPF0N	AH37	VGA_TZOUT2-	VGA_TZOUT2- <29>
TXOUT_U3P	AF35	T12	
TXOUT_U3N	AG36	T13	

LVTMDP

@ @

TXCLK_LP_DPE3P	AP34	VGA_TXCLK+	VGA_TXCLK+ <29>
TXCLK_LN_DPE3N	AR34	VGA_TXCLK-	VGA_TXCLK- <29>
TXOUT_L0P_DPE2P	AW37	VGA_TXOUT0+	VGA_TXOUT0+ <29>
TXOUT_L0N_DPE2N	AU35	VGA_TXOUT0-	VGA_TXOUT0- <29>
TXOUT_L1P_DPE1P	AR37	VGA_TXOUT1+	VGA_TXOUT1+ <29>
TXOUT_L1N_DPE1N	AU39	VGA_TXOUT1-	VGA_TXOUT1- <29>
TXOUT_L2P_DPE0P	AP35	VGA_TXOUT2+	VGA_TXOUT2+ <29>
TXOUT_L2N_DPE0N	AR35	VGA_TXOUT2-	VGA_TXOUT2- <29>
TXOUT_L3P	AN36	T15	
TXOUT_L3N	AP37	T14	

@ @

216-0772000 MADISON — MAD@

10/6 Change symbol of U54 to Madison-M2

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Mannhatton_ PCIE / LVDS

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 22 of 63

Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
CONFIG[1] CONFIG[2] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
SMS_EN_HARD	H2SYNC	Can be unconnected if not used.	0
VIP_DEVICE _STRAP_DIS	V2SYNC	Can be unconnected if not used.	0

Madison Pro

Location / VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
ATI(8pcs)1GB	O	1	O	O
* Samsung(8pcs) 1GB	O	1	O	1
Hynix(8pcs) 1GB	O	1	1	O
Samsung(8pcs) 128*16	1	1	O	1
Hynix(8pcs) 128*16	1	1	1	O

Broadway Pro

Location / VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
ATI(8pcs)1GB	O	1	O	O
Samsung(8pcs) 1GB	O	1	O	1
* Hynix(8pcs) 1GB	O	1	1	O
Samsung(8pcs) 128*16	1	1	O	1
Hynix(8pcs) 128*16	1	1	1	O

11/2 Add R648

10/5 Add

8/25 ATI suggest

8/25 Modify by Vivian

10/19 Add by Vivian

9/14 Change poewr net to +1.0VSDGPU

9/21 Add R378 PU to +3VS_DELAY(Slove system boot up hangs issue)

9/21 Add R666 PD to GND(Slove system boot up hangs issue)

12/7 Add C567=@100pF(Avoid noise)

Do not PU R177 for GPIO22 if not implement external flash ROM

10/6 Change symbol of U54 to Madison-M2

External VGA Thermal Sensor

U15 ADM1032ARMZ-2REEL_MSOP8

1/14 Change PN of Q9 from SB00000AR00 to SB00000D900(material issue)

3/2 Change Bom structure of C120 to mount,Change value of R525 to 24k ohm(1%)

Use boradway GPU, R28 change to 0 Ohm(SD028000080)

9/10 Change symbol of Q76 to SC70-3

9/14 Change part of C72 to 10uF(ATI suggest)

9/14 Modify PWR Seq

8/25 ATI suggest

PWR Sequence

+3VS_DELAY

VGA_CORE (VDDC)

+1.8VS

M96 only

CRT

HDMI

10/27 Add R670/R678/R685/R691
10/27 Place R670 Close to U22,R678/R685/R691 close to U54

FLASH ROM

U22 AT25F512B-SSH-T_SOP8

1/6 Change PN of U22 from SA00001O100 to SA00003NH00

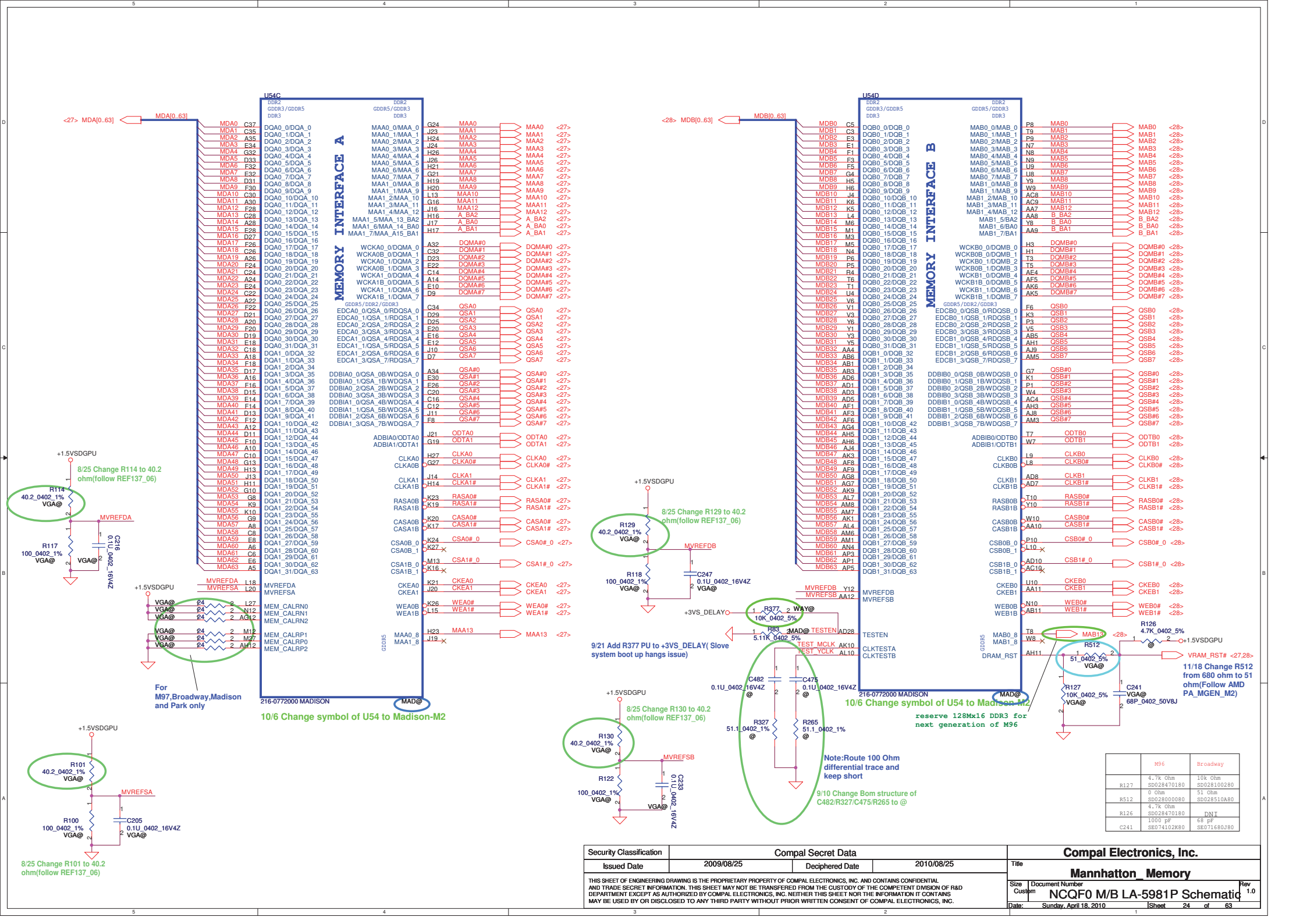
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Mannhatton_Strape/DP/HDMI//CRT

Size: C | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 23 of 63



	M96	Broadway
R127	4.7k Ohm SD028470180	10k Ohm SD028100280
R512	0 Ohm SD028000080	51 Ohm SD028510A80
R126	4.7k Ohm SD028470180	DNI
C241	1000 pF SE074102K80	68 pF SE071680J80

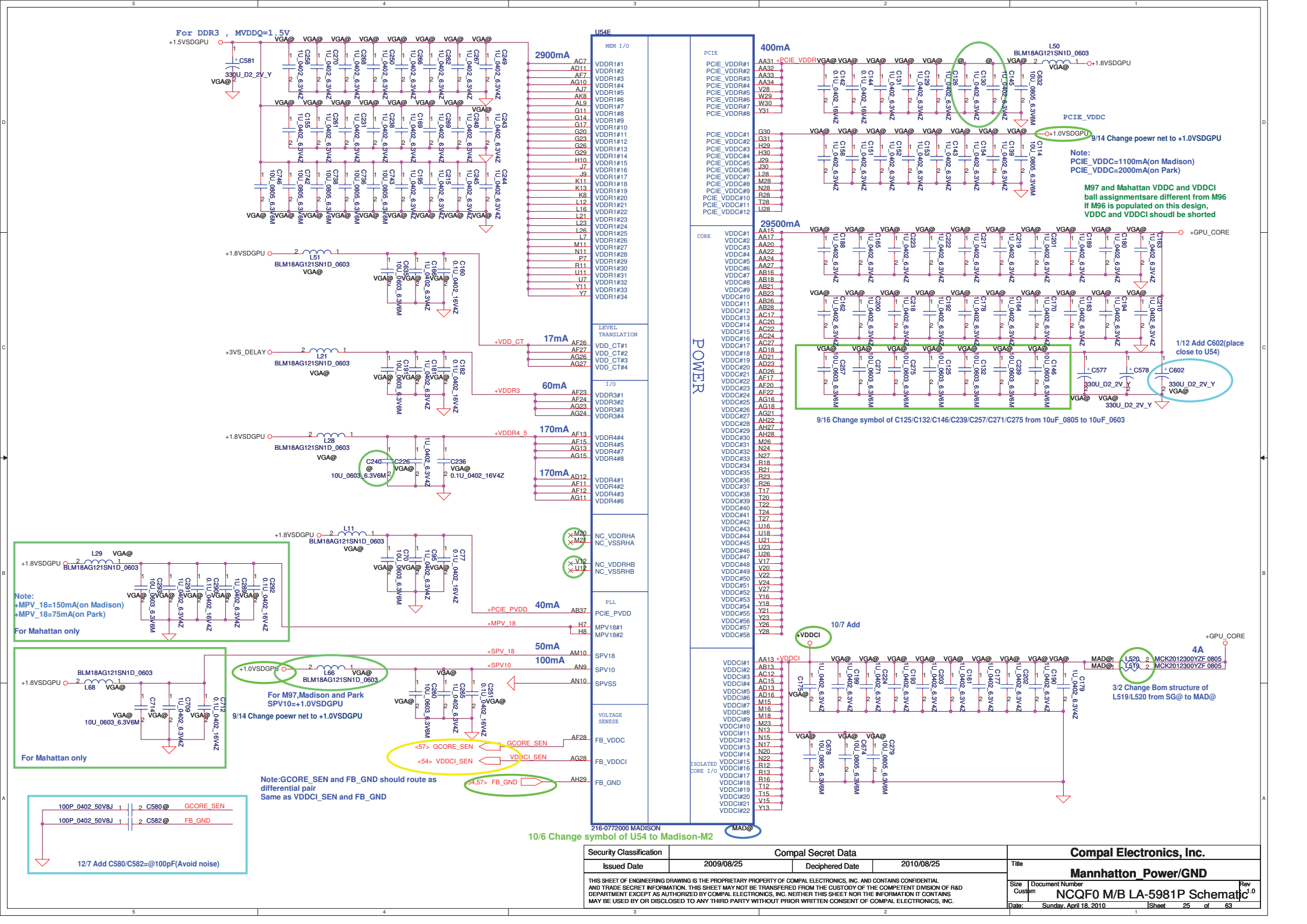
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_ Memory**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 Sheet 24 of 63



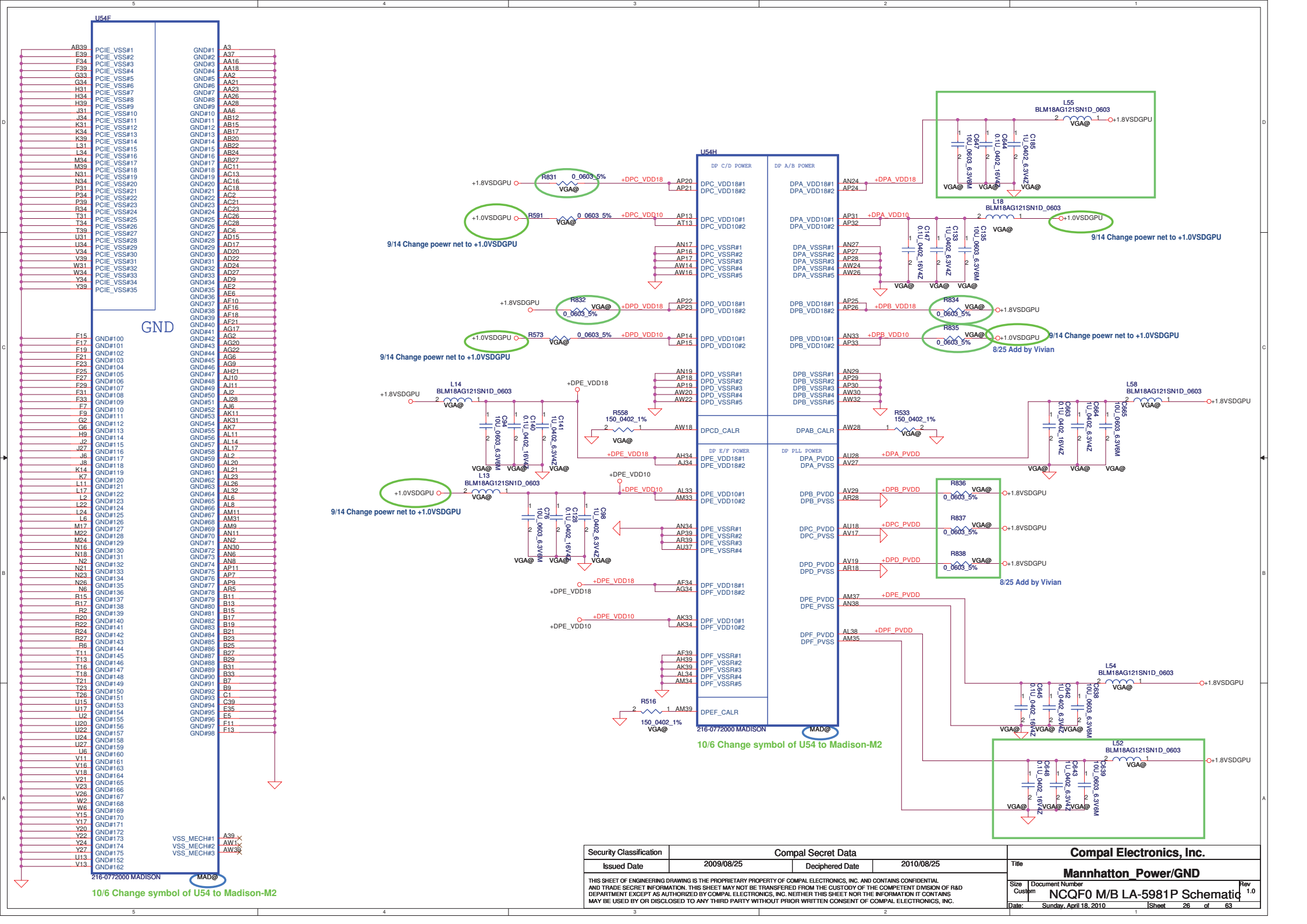
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_Power/GND**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 Sheet 25 of 63



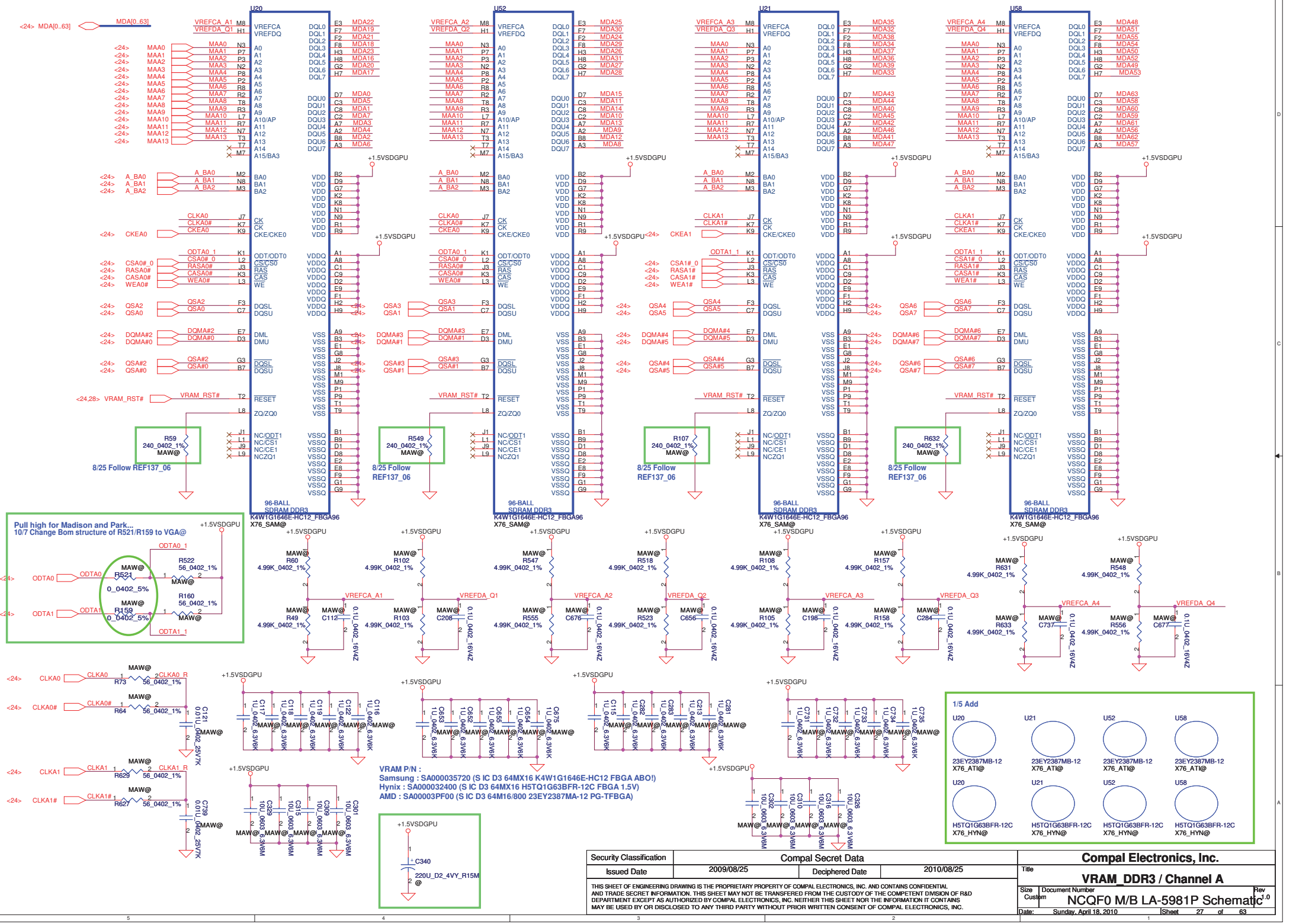
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_Power/GND**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 | Sheet 26 of 63



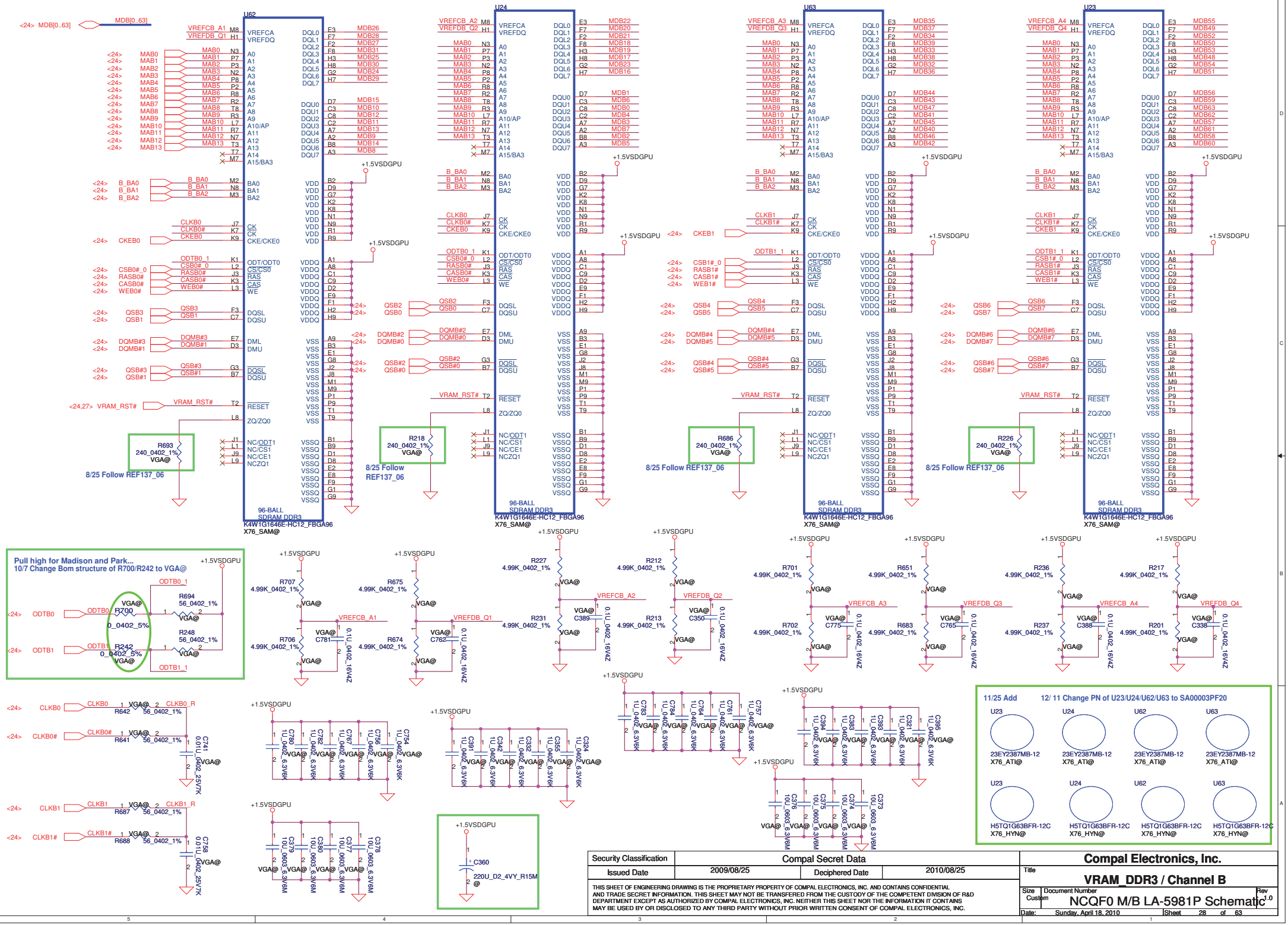
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **VRAM_DDR3 / Channel A**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 Sheet 27 of 63


U62
U24
U63
U23
96-BALL SDRAM DDR3
K4W1G1646E-HC12_FBGA96
X76_SAM@
+1.5VSDGPU
MDB[0..63]
8/25 Follow REF137_06
Pull high for Madison and Park...
10/7 Change Bom structure of R700/R242 to VGA@
11/25 Add
12/ 11 Change PN of U23/U24/U62/U63 to SA00003PF20
23EY2387MB-12 X76_ATI@
H5TQ1G63BFR-12C X76_HYN@
Security Classification
Compal Secret Data
Issued Date
2009/08/25
Deciphered Date
2010/08/25
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Compal Electronics, Inc.
Title
VRAM_DDR3 / Channel B
Size
Custom
Document Number
NCQF0 M/B LA-5981P Schematic
Rev
1.0
Date:
Sunday, April 18, 2010
Sheet
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of
63

LCD POWER CIRCUIT

1/14 Change PN of Q6 from SB00000AR00 to SB00000D900(material issue)

9/14 Change power net from +3V to +3VALW

W=60mils

4/17 Add D22

Reserved for DIS Only

GPU Support DPST for DIS Only

4/16 Add

4/16 Add R46

SN74CBTD3306CPWR_TSSOP8

NC7SZ14P5X_NL_SC70-5

SG For LVDS

SEL=LOW, B1
SEL=High, B2

PI3LVD1012BE_BQSOP80

9/1 Del D5/R22(BKOFF# not need to pull high)

LED PANEL Conn.

W=40mils

10/14 Change R16/R17 to 2.2K ohm

1/14 Change PN of Q80 from SB00000AR00 to SB00000D900(material issue)

11/11 Change R65/R91 to 2.2K ohm

1/14 Change PN of Q81 from SB00000AR00 to SB00000D900(material issue)

I-PEX_20143-040E-20F

9/1 Add L7(EMI Suggest)

WCM2012F2S-900T04_0805

9/14 Add R777(by Vivian)

9/16 Add D25(by Vivian)

DAN202UT106_SC70-3

DIS ONLY

CM1293-04SO_SOT23-6

SSM3K7002FU_SC70-3

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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CRT Connector

10/14 Change PN of L40/L43/L48 to SM01000AX00

L48 MBK1608221YZF_2P @
L43 MBK1608221YZF_2P @
L40 MBK1608221YZF_2P @

W=40mils

+5VS → D2 RB491D_SC59-3 → F1 1.1A_6V_SMD1812P110TF W=40mils → +CRT_VCC
+R_CRT_VCC
C17 0.1U_0402_16V4Z

10/14 Change to 0 ohm for DIS

CRT_R → L48 0_0603_5% → CRT_R_1 → L49 FCM2012CF-800T06_2P → CRT_R_2
CRT_G → L43 0_0603_5% → CRT_G_1 → L44 FCM2012CF-800T06_2P → CRT_G_2
CRT_B → L40 0_0603_5% → CRT_B_1 → L41 FCM2012CF-800T06_2P → CRT_B_2

R508 150_0402_1%
R503 150_0402_1%
R501 150_0402_1%
C631 12P_0402_50V8J
C623 12P_0402_50V8J
C611 12P_0402_50V8J
Change to 15pF for DIS
C630 @ 22P_0402_50V8J
C615 @ 22P_0402_50V8J
C610 @ 22P_0402_50V8J
C50 15P_0402_50V8J
C41 15P_0402_50V8J
C24 15P_0402_50V8J
Change to 12pf for DIS

9/14 Change description and value of L2/L3.

L3 BLM18AG121SN1D_0603
L2 BLM18AG121SN1D_0603
CRT_HSYNC_2
CRT_VSYNC_2
C37 10P_0402_50V8J
C19 10P_0402_50V8J

C18 100P_0402_50V8J
C40 68P_0402_50V8J
C14 68P_0402_50V8J
DSUB_12
DSUB_15
R13 100K_0402_5%
+CRT_VCC

JCRT1 SUYIN_070546FR015S263ZR @
RGND, ID0, Red, GGND, SDA, Green, BGND, Hsync, Blue, +5V, Vsync, res, SGND, SCL, GND, GND, GND
CRT_DET# <18>

11/13 Change symbol of JCRT1 from DC060003O00 to DC060003N00

C49 0.1U_0402_16V4Z
+CRT_VCC
R21 10K_0402_5%
U12 74AHCT1G125GW_SOT353-5
CRT_HSYNC → CRT_HSYNC_1

C29 0.1U_0402_16V4Z
+CRT_VCC
U4 74AHCT1G125GW_SOT353-5
CRT_VSYNC → CRT_VSYNC_1

+3VS
C113 0.1U_0402_16V4Z SG@
C173 0.1U_0402_16V4Z SG@
C172 0.1U_0402_16V4Z SG@
C171 0.1U_0402_16V4Z SG@

U17 SG@
PI3V712-AZLEX_TQFN32_6X3~D

VDD	A0	CRT_R
VDD	A1	CRT_G
VDD	A2	CRT_B
VDD	A3	CRT_HSYNC
VDD	A4	CRT_VSYNC
0B1	SEL1	DGPU_SELECT# → DGPU_SELECT# <17,29>
1B1		
2B1		
3B1	A5	DSUB_12_R
4B1	A6	DSUB_15_R
5B1		
6B1	SEL2	DGPU_EDIDSEL_R# → DGPU_EDIDSEL_R# <29>
0B2		
1B2		
2B2	GND	
3B2	GND	
4B2	GND	
5B2	GND	
6B2	GPAD	

<23> VGA_CRT_R, VGA_CRT_G, VGA_CRT_B, VGA_CRT_HSYNC, VGA_CRT_VSYNC, VGA_DDC_DATA, VGA_DDC_CLK
<16> PCH_CRT_R, PCH_CRT_G, PCH_CRT_B, PCH_CRT_HSYNC, PCH_CRT_VSYNC, PCH_CRT_DATA, PCH_CRT_CLK

10/14 Change net name

L	B1	DIS
H	B2	UMA

9/10 Change U17 from SA000026Y00 to SA00003B300
Michael

VGA DDC PU 4.7K on Page 23
Reserved for DIS only

10/14 Add R55/R56= 0 ohm

+3VS
+CRT_VCC
R15 2.2K_0402_5%
R14 2.2K_0402_5%
VGA_DDC_DATA → R55 DIS@ → DSUB_12_R 0_0402_5% → Q84A DMN66D0LDW-7 2N_SOT363-6 VGA@ → DSUB_12
VGA_DDC_CLK → R56 DIS@ → DSUB_15_R 0_0402_5% → Q84B DMN66D0LDW-7 2N_SOT363-6 VGA@ → DSUB_15

4/2 Change PN of Q84 from SB00000D900 to SB00000DH00(ESD issue)

Reserved for DIS only

VGA_CRT_G, VGA_CRT_R → RP11 DIS@ 0_0404_4P2R_5% → CRT_G, CRT_R
VGA_CRT_HSYNC, VGA_CRT_B → RP12 DIS@ 0_0404_4P2R_5% → CRT_HSYNC, CRT_B
VGA_CRT_VSYNC → R53 DIS@ 0_0402_5% → CRT_VSYNC

9/14 Change to RP for layout request
Michael

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2009/08/25

Compal Electronics, Inc.
Title: CRT Connector
Size: B
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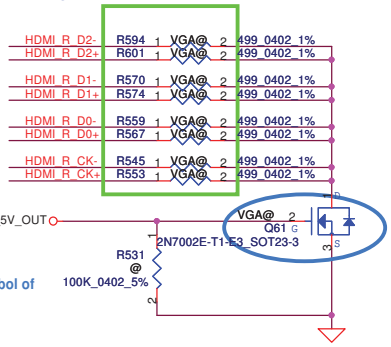
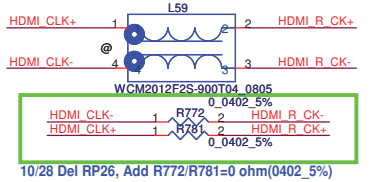
Place closed to JHDMI1

9/14 Change Bom structure from DIS @ to VGA@

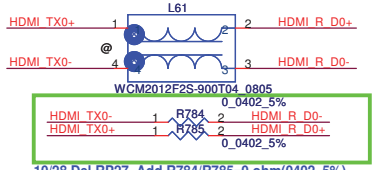


9/23 Change symbol of Q61 to SOT23-3

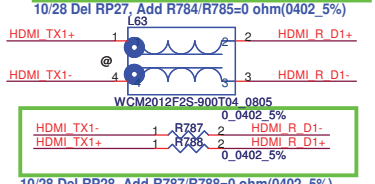
4/2 Change PN of Q61 from SB570020110 to SB000008J10



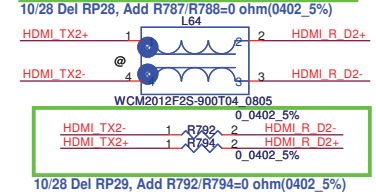
10/28 Del RP26, Add R772/R781=0 ohm(0402_5%)



10/28 Del RP27, Add R784/R785=0 ohm(0402_5%)

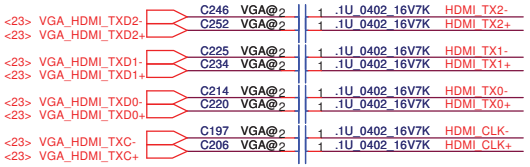


10/28 Del RP28, Add R787/R788=0 ohm(0402_5%)

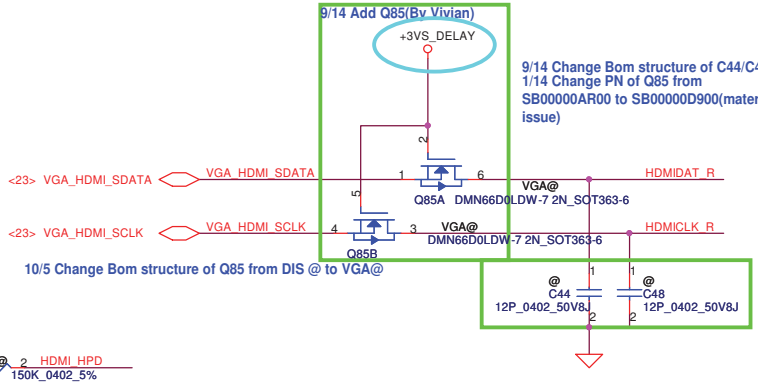


10/28 Del RP29, Add R792/R794=0 ohm(0402_5%)

0914 Change to RP
Michael

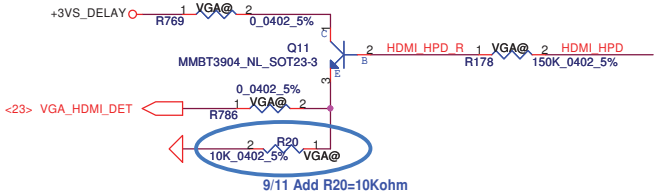


9/14 Add Q85(By Vivian)

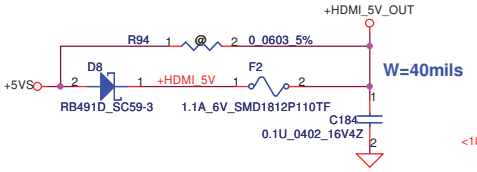


9/14 Change Bom structure of C44/C48 from DIS @ to @
1/14 Change PN of Q85 from SB00000AR00 to SB00000D900(material issue)

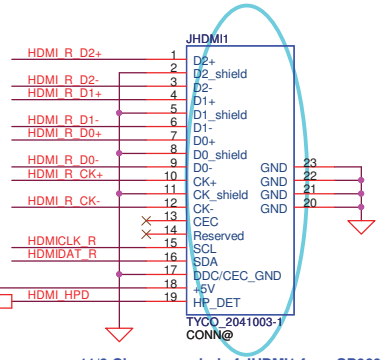
10/5 Change Bom structure of Q85 from DIS @ to VGA@



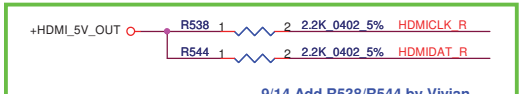
9/11 Add R20=10Kohm



W=40mils



11/9 Change symbol of JHDMI1 from SP060003Z00 to DC232000A00



9/14 Add R538/R544 by Vivian

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: HDMI Level Shife & Conn

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

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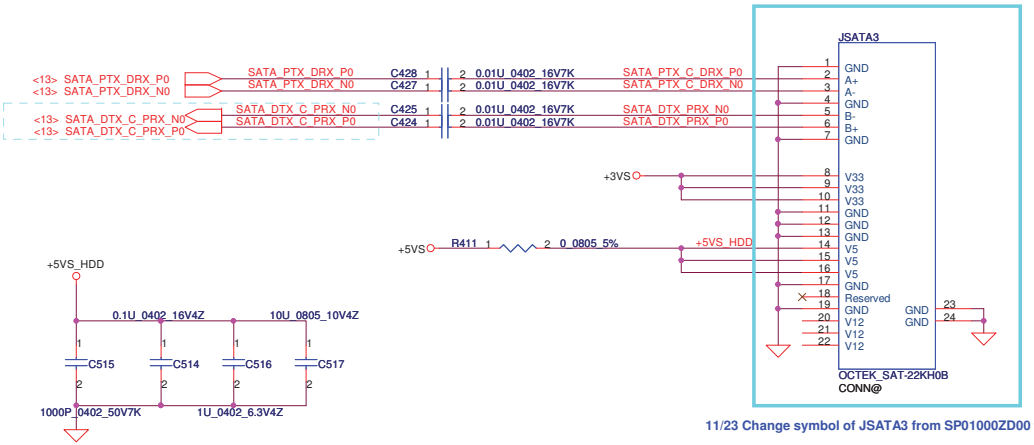
HDD

SATA HDD Conn.



11/23 Change symbol of JSATA3 from SP01000ZD00 to SP01000ZE00

ODD

SATA ODD Conn.

12/1 Change symbol of JSATA2 to SUYIN_127382FB013S102ZR_13P(SP01000QJ00)

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **HDD & ODD Connector**

Size	Document Number	Rev
B	NCQF0 M/B LA-5981P Schematic	1.0

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11/13 Change symbol of R800 from 1206 package to 0805 package

60mil

+3VALW — R800 1 2 0_0805_5% — +3V_LAN

C901 4.7U_0603_6.3V6K

C902 0.1U_0402_16V4Z

U70

BCM57780A0KMLG_QFN48_7X7

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

U71 @ AT24C02_SO8

R802 1K_0402_1% @

R803 1K_0402_1%

R811 1K_0402_1%

R812 1K_0402_1% @

C906 0.1U_0402_16V4Z @

SPROM_CLK

SPROM_DOUT

20mil

L100 BLM18AG601SN1D_2P — +LAN_XTALVDDH — +3V_LAN

L101 BLM18AG601SN1D_2P — +LAN_BIASVDDH

L102 BLM18AG601SN1D_2P — +LAN_AVDDH

L104 BLM18AG601SN1D_2P — +LAN_PCIEPLLVDD — +1.2V_LAN

L105 BLM18AG601SN1D_2P — +LAN_GPHYPLLVDDL — +1.2V_LAN

L106 BLM18AG601SN1D_2P — +LAN_AVDDL — +1.2V_LAN

C909 0.1U_0402_16V4Z

C910 0.1U_0402_16V4Z

C911 0.1U_0402_16V4Z

C912 0.1U_0402_16V4Z

C915 0.1U_0402_16V4Z

C916 4.7U_0603_6.3V6K

C919 0.1U_0402_16V4Z

C920 4.7U_0603_6.3V6K

C921 0.1U_0402_16V4Z

C922 4.7U_0603_6.3V6K

L103 4.7UH_PG031B-4R7MS_1.1A_20%

+1.2V_LAN_OUT — +1.2V_LAN

C913 0.1U_0402_16V4Z

C914 10U_0805_10V4Z

C917 4.7U_0603_6.3V6K

C918 0.1U_0402_16V4Z

+3V_LAN

+1.2V_LAN

+3VS

LAN_XTALI

LAN_XTALO_R

R815 200_0402_1%

Y10 25MHZ_20PF_7A25000012

C923 27P_0402_50V8J

C924 27P_0402_50V8J

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Broadcom BCM57780

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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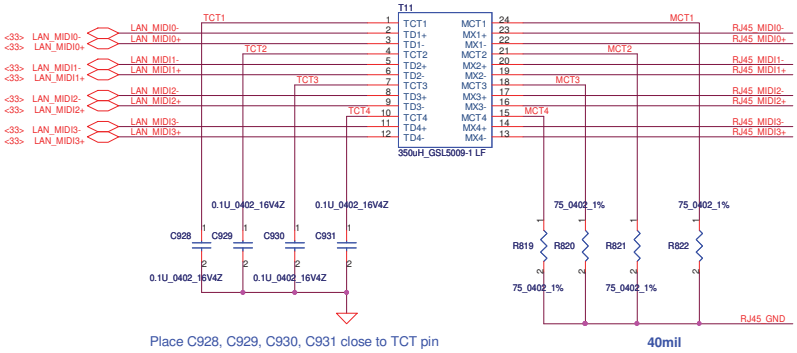
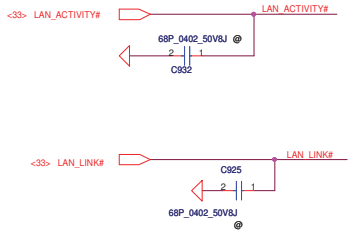
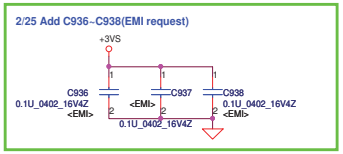
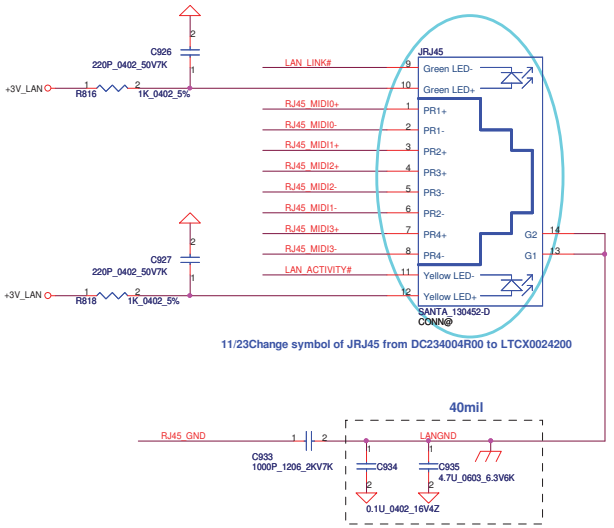
LAN Connector









Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size	Document Number	Rev
	NCQF0 M/B LA-5981P Schematic	1.0

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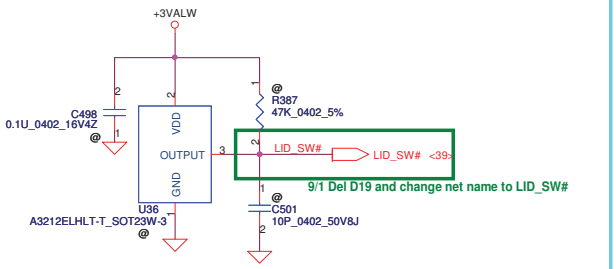
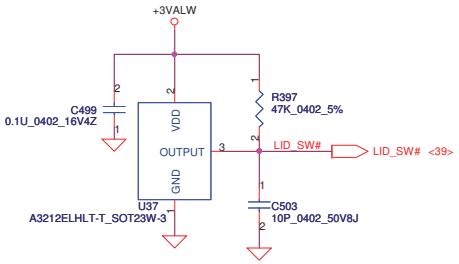
Lid Switch

(Hall Effect Switch)

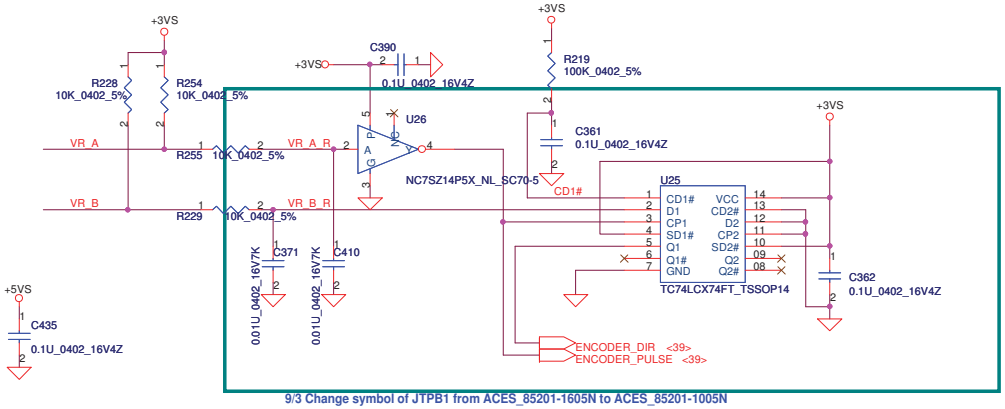


9/1 Del D19 and change net name to LID_SW#

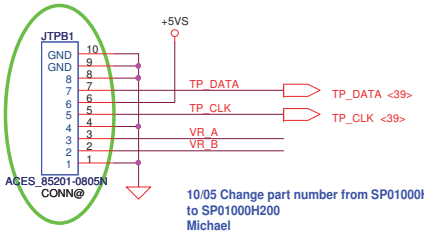


1/6 Add U37/R397/C503/C499=(ME request)

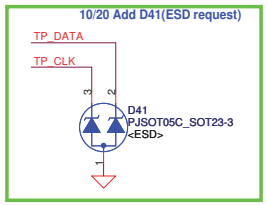
Touch Pad



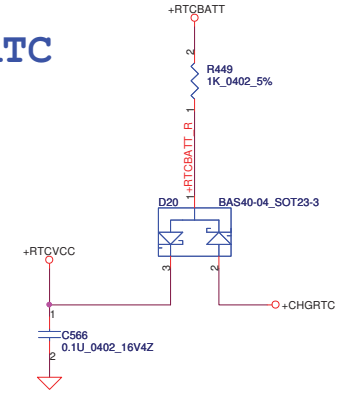
9/3 Change symbol of JTPB1 from ACES_85201-1605N to ACES_85201-1005N



10/05 Change part number from SP01000H400 to SP01000H200
Michael

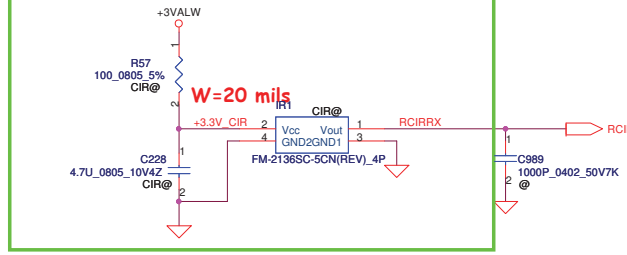


RTC



CIR

1/5 Change BOM Structure of R57/C228/IR1 from mount to CIR@



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: LID/RTC/CIR			
Size	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 1.0
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eSATA

+USB_VCCD
150U_B2_6.3VM_R35M
C794
C793
470P_0402_50V7K

10/28 Add symbol of D16 of SC300000P00
+USB_VCCD
D16 <ESD>
PWR GND
IO2 IO1
USB20_P2_1
USB20_N2_1
CM1293A-02SR_SOT143-4

2/23 Change symbol of C286 from 150uF to 220uF
220U_6.3V_M
C286
C297
470P_0402_50V7K
+USB_VCCD
R654 @ 0_0402_5%
L69
<17> USB20_P2
USB20_P2
USB20_P2_1
<17> USB20_N2
USB20_N2
USB20_N2_1
WCM-2012-900T_4P
R658 @ 0_0402_5%
JSATA1
USB
VBUS
D-
D+
GND
ESATA
A+
A-
B-
B+
FOXCONN-3Q318111-RB1021-7F
CONN@
<13> SATA_PTX_DRX_P4
<13> SATA_PTX_DRX_N4
SATA_PTX_DRX_P4
SATA_PTX_DRX_N4
C318 0.01U_0402_25V7K
C317 0.01U_0402_25V7K
SATA_PTX_C_DRX_P4
SATA_PTX_C_DRX_N4
<13> SATA_DTX_C_PRX_N4
<13> SATA_DTX_C_PRX_P4
SATA_DTX_C_PRX_N4
SATA_DTX_C_PRX_P4
C308 0.01U_0402_25V7K
C305 0.01U_0402_25V7K
SATA_DTX_PRX_N4
SATA_DTX_PRX_P4
11/9 Change symbol of JSATA1 from DC230711060 to DC233004B00

9/14 Change power net from +3V to +3VALW
+3VALW
+5VALW
+USB_VCCD
U59
GND VOUT
VIN VOUT
VIN VOUT
EN FLG
SYSON#
RT9715BGS_SO8
R643
100K_0402_5%
R635
10K_0402_5%
C728
4.7U_0603_6.3V6K
C730
0.1U_0402_16V4Z
USB_OC#02 <17>
9/14 Change symbol of U59

10/28 Change symbol of D13 from SC300000O00 to SC300000P00
+USB_VCCD
D13 <ESD>
PWR GND
IO2 IO1
USB20_N0_1
USB20_P0_1
CM1293A-02SR_SOT143-4

+USB_VCCD
R280 @ 0_0402_5%
L32
<17> USB20_N0
USB20_N0
USB20_N0_1
<17> USB20_P0
USB20_P0
USB20_P0_1
WCM-2012-900T_4P
R281 @ 0_0402_5%
JUSB1
VBUS
D-
D+
GND
SUYIN_020133GB004M51PZR
CONN@
11/9 Change symbol of JUSB1 from SP01000F100 to SP060004200

HS USB Port

9/14 Change power net from +3V to +3VALW
+3VALW
+5VALW
+USB_VCCA
U64
GND VOUT
VIN VOUT
VIN VOUT
EN FLG
RT9715BGS_SO8
R750
100K_0402_5%
R751
10K_0402_5%
C798
4.7U_0603_6.3V6K
C801
0.1U_0402_16V4Z
USB_OC#4 <17>
<43,45> SYSON#
9/14 Change symbol of U64

+USB_VCCA
150U_B2_6.3VM_R35M
1/6 Add C319/320
C319
C320
470P_0402_50V7K
R324 @ 0_0402_5%
L33
<17> USB20_N8
USB20_N8
USB20_N8_1
<17> USB20_P8
USB20_P8
USB20_P8_1
WCM-2012-900T_4P
R331 @ 0_0402_5%
JUSB2
VBUS
D-
D+
GND
SUYIN_020133GB004M51PZR
CONN@
11/9 Change symbol of JUSB2 from SP01000B000 to SP060004200

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: USB / eSATA

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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SD,MMC,MS, xD muti-function pin define

MDIO PIN Name	SD/MMC PIN Name	MS Card PIN Name	xD Card PIN Name
MDIO00	SD7-DAT0	MS4-DATA0	XD10-D0
MDIO01	SD8-DAT1	MS3-DATA1	XD11-D1
MDIO02	SD9-DAT2	MS5-DATA2	XD12-D2
MDIO03	SD1-DAT3	MS7-DATA3	XD13-D3
MDIO04	SD2-CMD	MS2-BS	XD07-WE
MDIO05	SD5-CLK	MS8-SCLK	XD04-CE
MDIO06	SD-WP		XD08-WP
MDIO07			XD05-CLE
MDIO08			XD14-D4
MDIO09			XD15-D5
MDIO10			XD16-D6
MDIO11			XD17-D7
MDIO12			XD03-RE
MDIO13			XD02-R/B
MDIO14			XD06-ALE
CR1_LEDN			
CR1_PCTLN			
CR1_CD0N	SD-CD		XD01-CD
CR1_CD1N		MS6-INS	XD01-CD

NOTE

12/2 JMB380B--Mount D7/R24/R30,R849 use 8.2K ohm
12/2 JMB380C--Del D7/R24/R30,mount R853;R849 use 12K ohm

3/2 Add R718/C168 for RESET

12/2 Add R853= 0 ohm(co-layout JMB380 revisonC)

12/2 Add C104(Follow Spec)

12/2 Place C73/C68/C104 close to pin5 of U2

3/2 Change R849 to 12K ohm

3/3 Change PN of U2 from SA000023A10 to SA000023A20(JMB380 Ver.B to Ver.C)

12/2 Add R95(Place R95 close to pin24 of U2)

10/15 Change symbol of J1394A from SUYIN_020115FR004S550ZL_4P-T to SUYIN_020115FB004S512ZL_4P by Vivian

Close to Chip

9/1 1394 Differential Pairs=110 ohm

5 IN 1 CardRead

Memory Card Power

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Card Reader JMB380

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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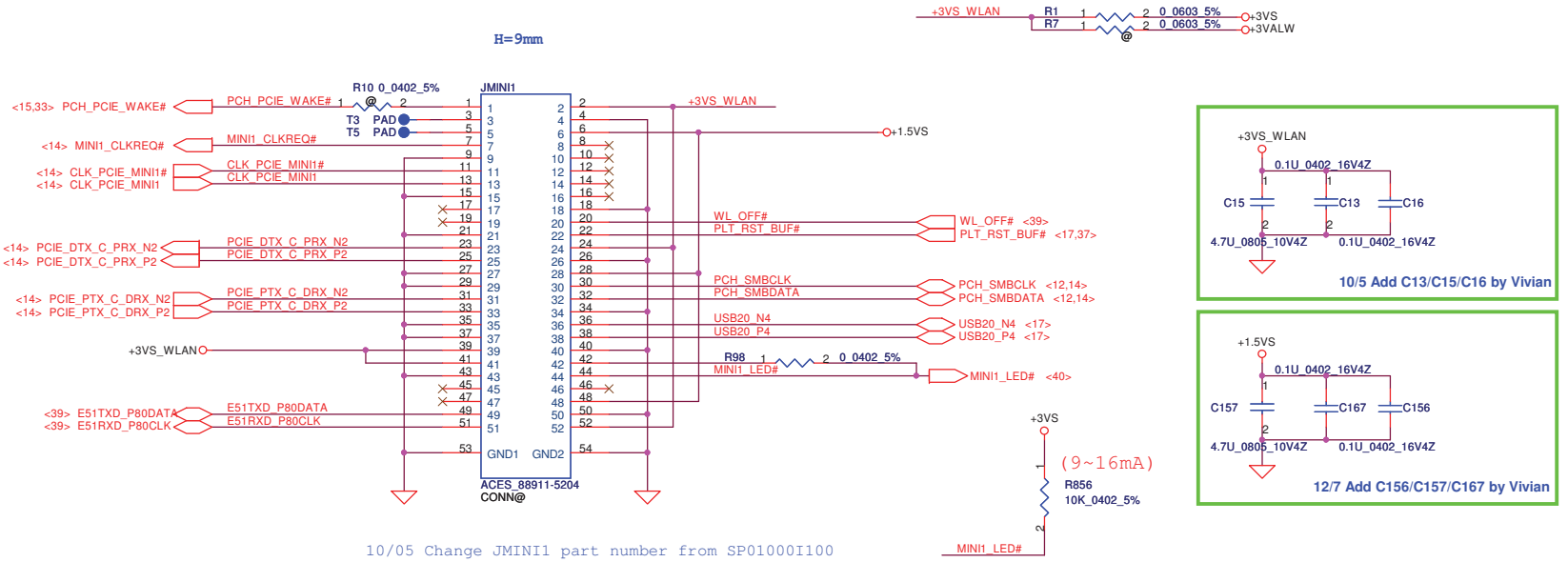
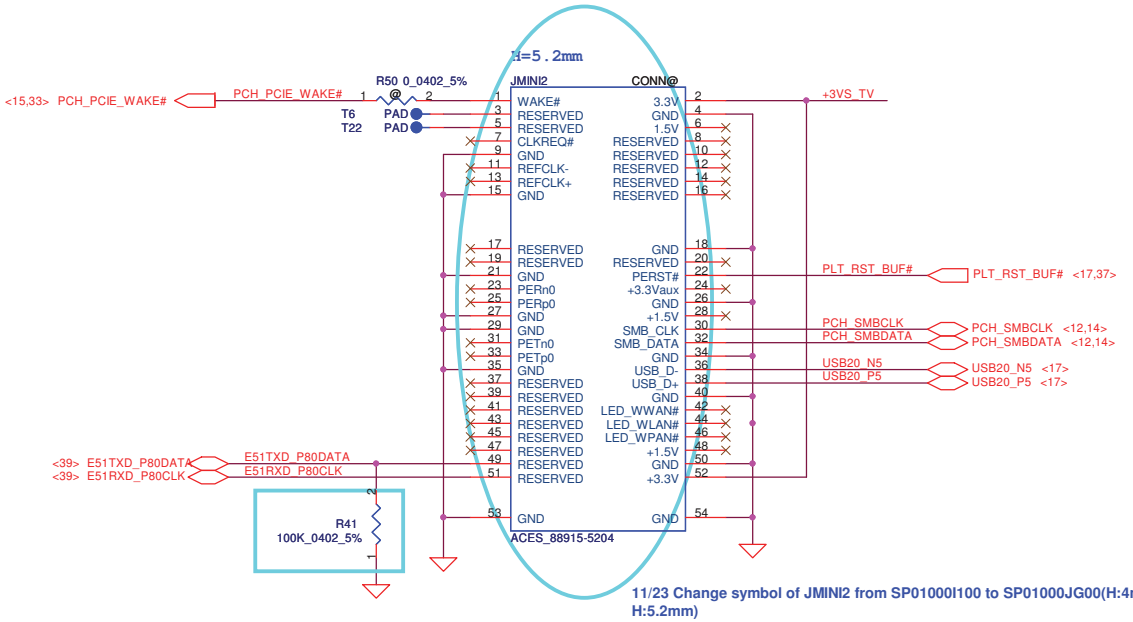
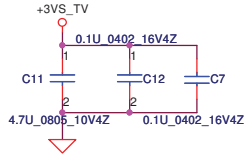
WLAN



10/05 Change JMINI1 part number from SP01000I100
to SP01000FP00
Michael

MINI





11/23 Change symbol of JMINI2 from SP01000I100 to SP01000JG00(H:4mm to H:5.2mm)

11/9 Change symbol of R41 from SD028100280 to SD028100380(10k ohm to 100k ohm)

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **WLAN&MINI**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

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For EC Tools

9/14 Change description and value of L36.

9/14 Add By Vivian(EMI suggest)

11/11 Add R273=@ 0 ohm(Follow NAU00)

10/1 ENE Recommand

2/25 Add R430/R442/R446

2/25 Change Bom structure of R421/R422/R431 from mount to @

11/9 Add R459

4/15 Change PN of SW2/SW3 from SN100001C00 to SN100003R00

4/1 Change footprint of SW2/SW3 from SW_SKRELGE010_2P to SW_NTC317-AB1G-C220C_2P

12/11 Change PN of U38 from SA00001J580 to SA00001J5A0(Rev:D3 to E0)

12/ 11 Change R365 from 100K to 0 ohm(Follow EC request)

9/1 Change net to ENCODER_DIR

10/1 EC Recommand

Analog Board ID definition, Please see page 3.

1/14 Change value of C518/C519 from 15pF to 18pF

12/8 Add C548/C550/C562/C595~C601=@ 100pF(Avoid switching noise)

9/14 Change description and value of L35.

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: EC ENE KB926

Size: B | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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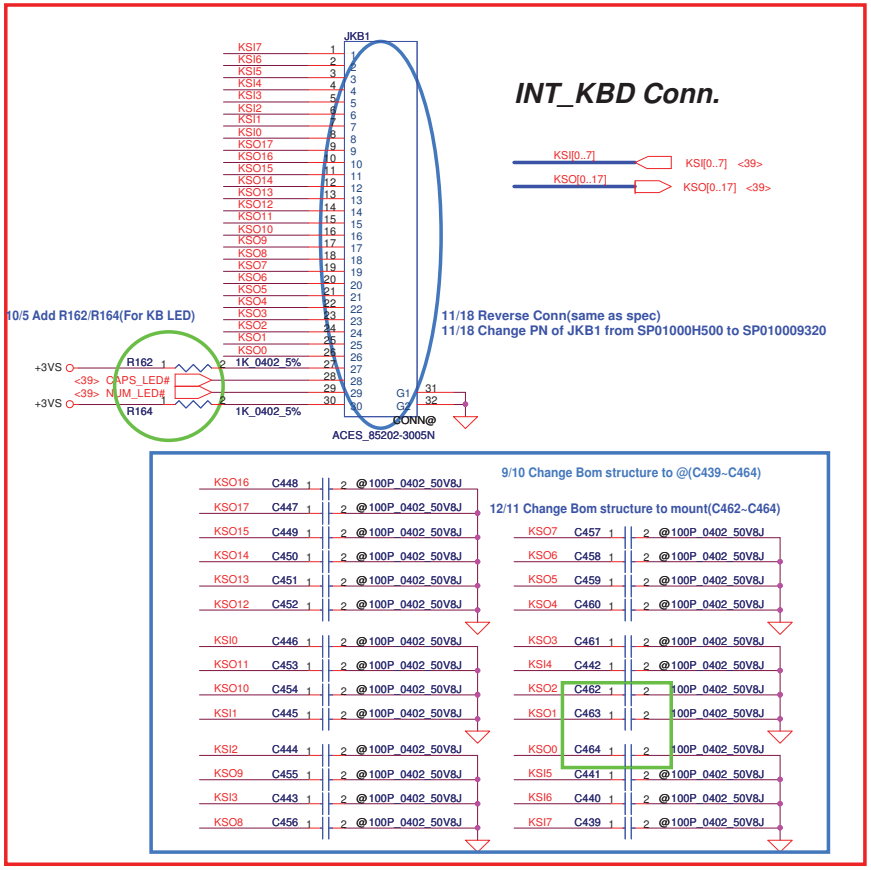

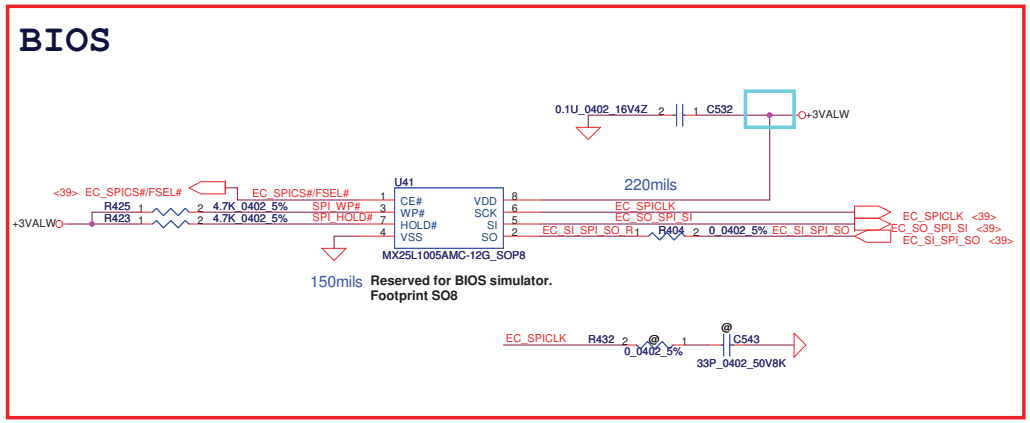

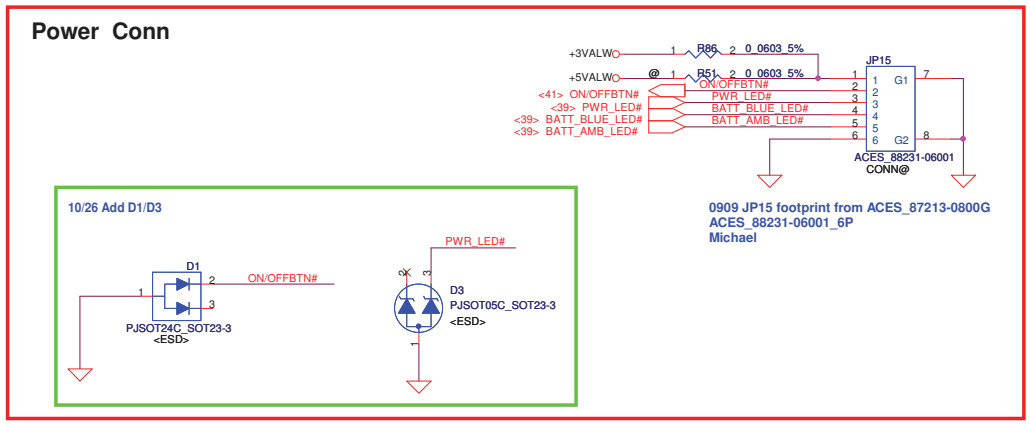

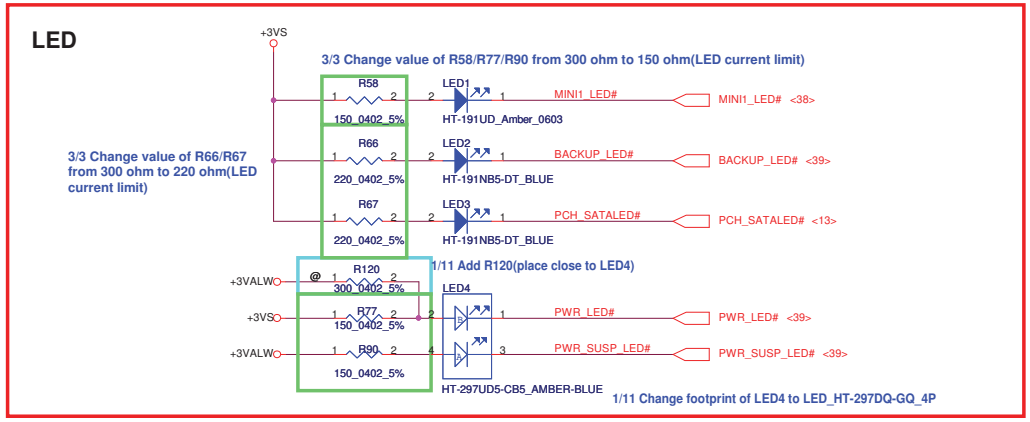

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
B	NCQF0 M/B LA-5981P Schematic	1.0

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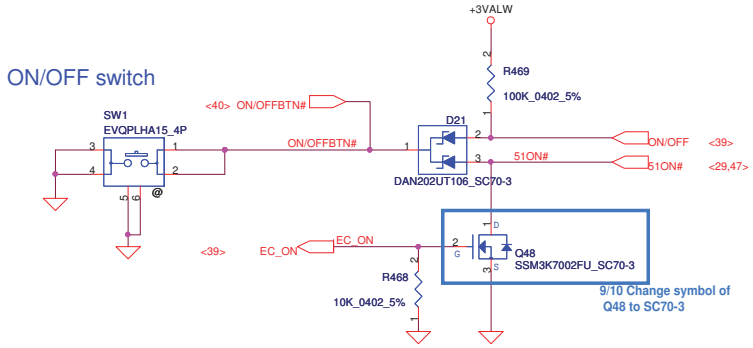
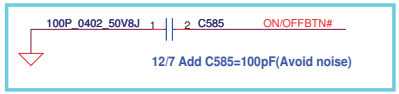
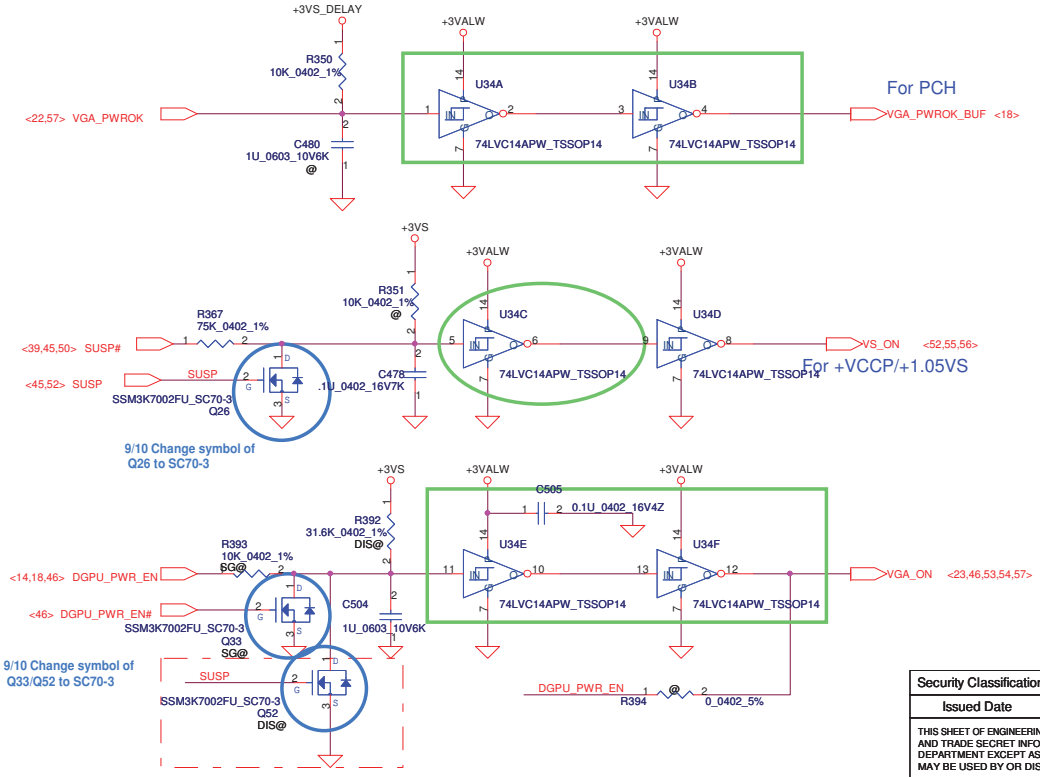
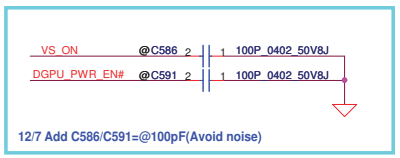
Power Button





Power ON Circuit





Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Power OK/PBN/TP Lock/LED

Size: B | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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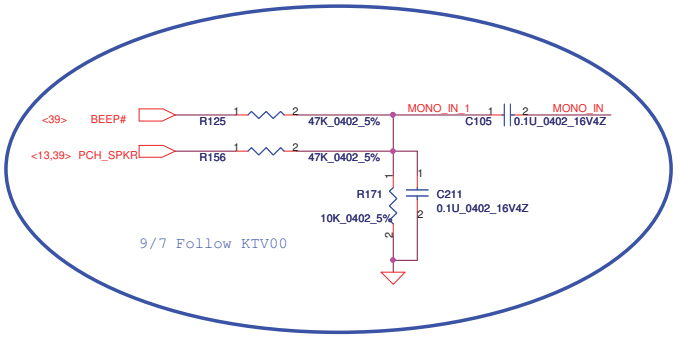
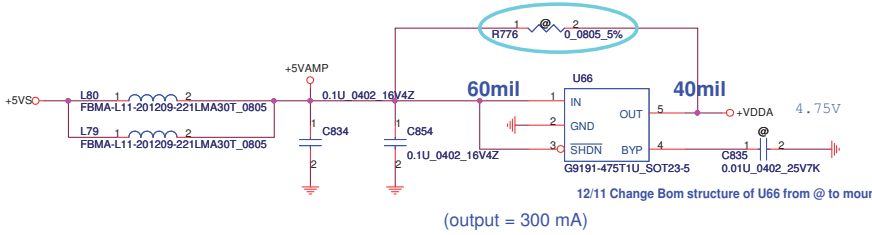
HD Audio Codec

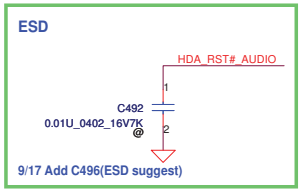


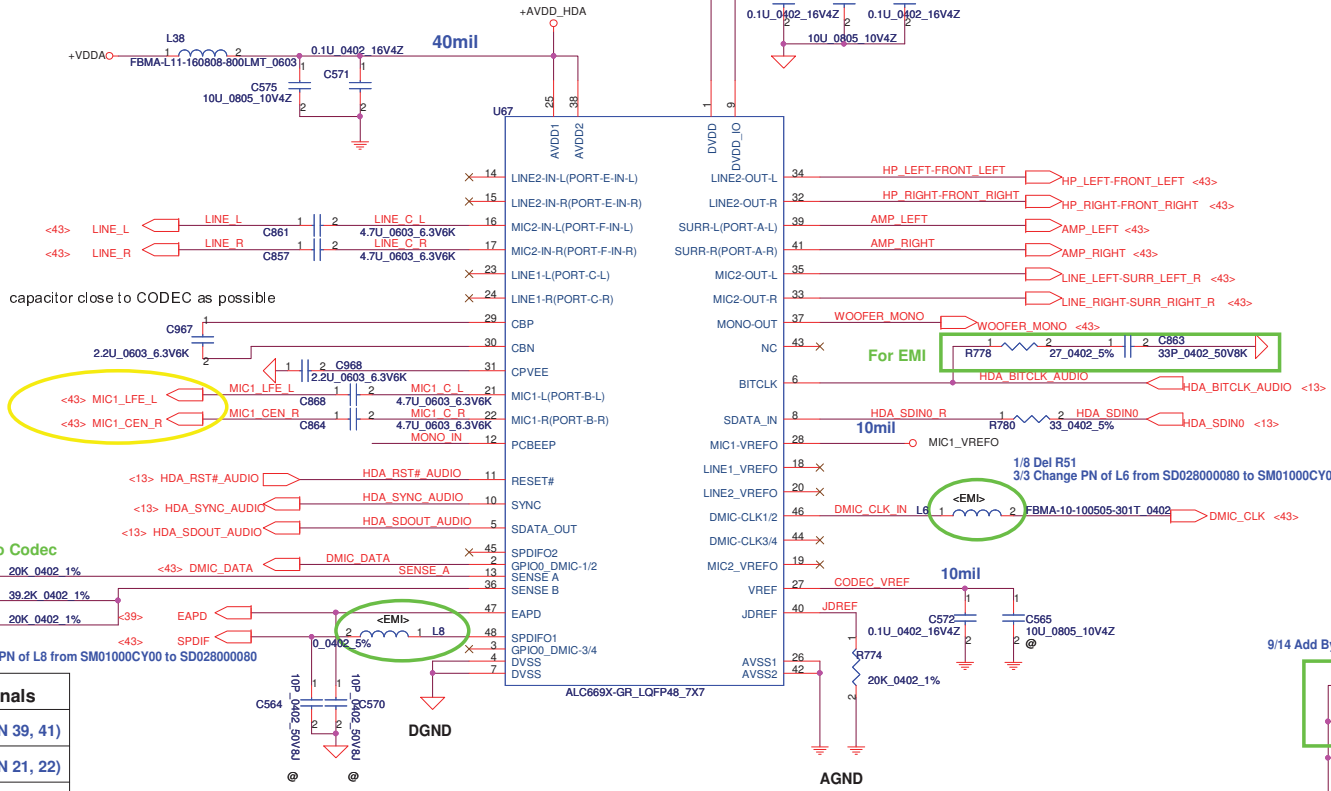
12/11 Change Bom structure of R776 from mount to @



12/11 Change Bom structure of U66 from @ to mount

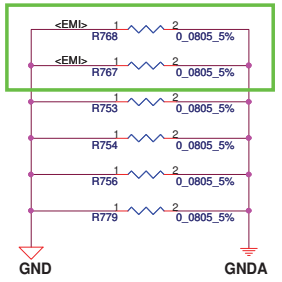
(output = 300 mA)





Sense Pin	Impedance	Codec Signals
SENSE A		PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
		PORT-C (PIN 23, 24)
SENSE B	39.2K	PORT-E (PIN 32, 34)
	20K	PORT-F (PIN 33, 35)
		PORT-H (PIN 37)

9/14 Add By Vivian(EMI suggest)



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: HD Audio Codec ALC669X

Size	Document Number	Rev
B	NCQF0 M/B LA-5981P Schematic	1.0

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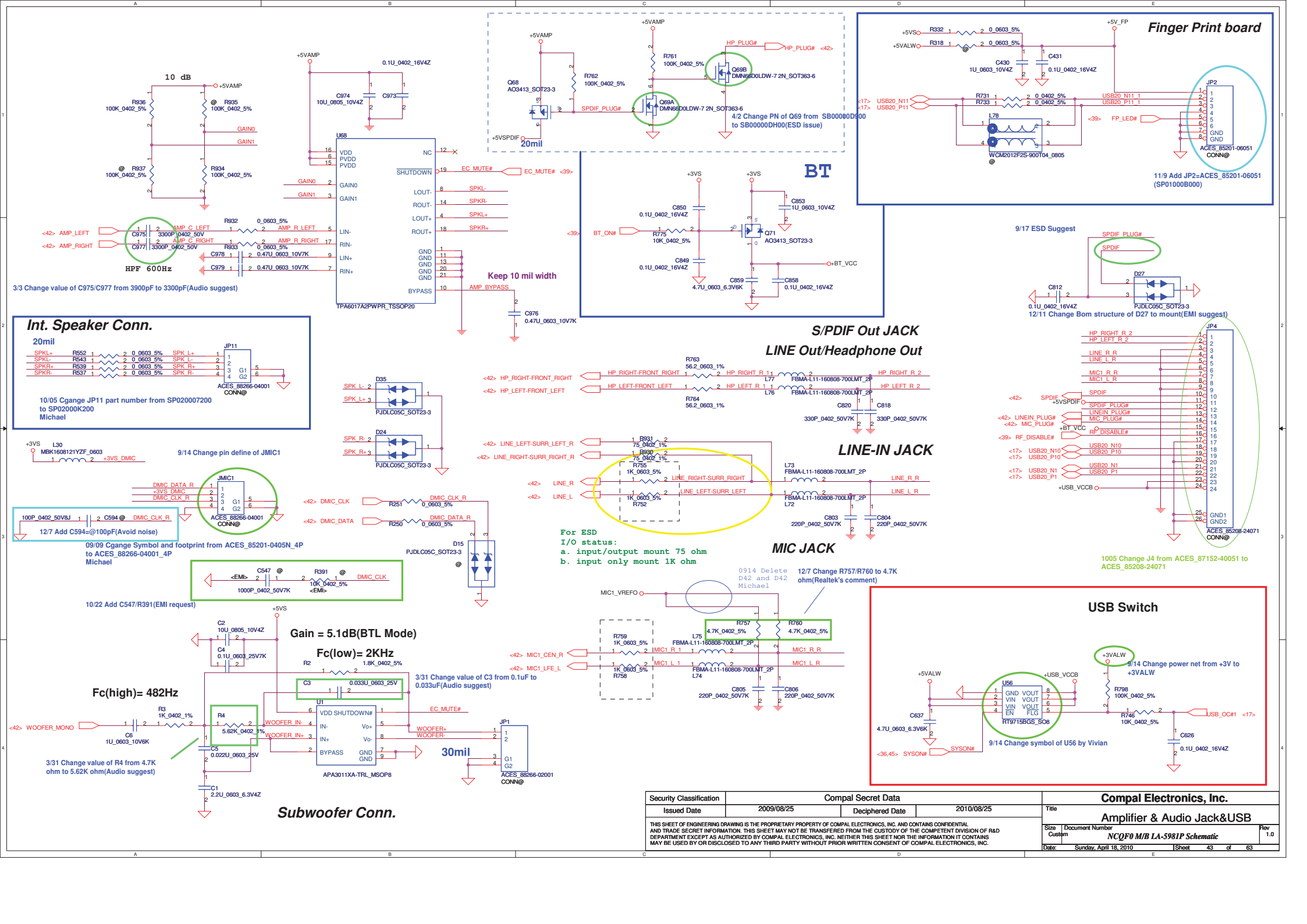

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Amplifier & Audio Jack&USB

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

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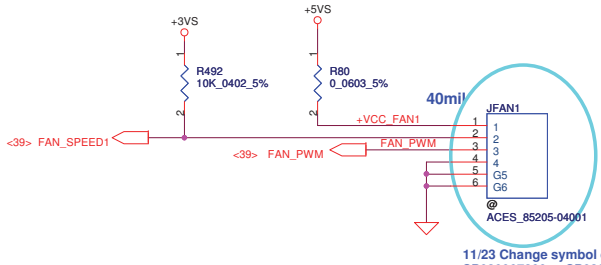
FAN1 Conn



11/23 Change symbol of JFAN1 from SP020007200 to SP020008X00

Screw

H1 H_3P0 · H2 H_3P0 · H3 H_3P0 · H4 H_3P0 · H5 H_3P0 · H6 H_3P0 · H7 H_3P0 · H8 H_3P0 · H9 H_3P0 · H10 H_3P0

H11 H_3P2 · H12 H_3P2 · H19 H_3P2

H15 H_3P8 · H16 H_3P8 · H17 H_3P8 · H18 H_3P8 · H13 H_3P8 · H14 H_3P8

H23 H_2P3X0P6 · H24 H_2P3X0P6

NON-PDH

2/25 Change footprint of H22

H21 H_5P0X3P0N · H20 H_6P0X3P0N · H22 H_2P8N

FD3 FIDUCIAL_C40M80 · FD1 FIDUCIAL_C40M80 · FD4 FIDUCIAL_C40M80 · FD2 FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size: B | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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+5VALW TO +5VS

For EMI Require 1/21
Put near Right side of DIMM

+5VALW, +5VS
U44 SI4800BDY-T1-E3_SO8
C555 1U_0603_10V4Z
R443 470_0603_5%
0.1U_0402_16V4Z C556
9/1 Del C574/C562/567
+VSB R444 200K_0402_5%
5VS_GATE
DMN66D0LDW-7 2N_SOT363-6
Q42B SUSP
C561 0.1U_0603_25V7K
SUSP Q42A DMN66D0LDW-7 2N_SOT363-6
4/2 Change PN of Q42 from SB00000D900 to SB00000DH00(ESD issue)

+3VALW TO +3VS

+3VALW, +3VS
U42 SI4800BDY-T1-E3_SO8
C549 1U_0603_10V4Z
R440 470_0603_5%
9/1 Del C547/C548/C545
+VSB R447 200K_0402_5%
3VS_GATE
DMN66D0LDW-7 2N_SOT363-6
Q43B SUSP
C560 0.1U_0603_25V7K
SUSP Q43A DMN66D0LDW-7 2N_SOT363-6
12/7 Add C579
C579 100P_0402_50V8J @
4/2 Change PN of Q43 from SB00000D900 to SB00000DH00(ESD issue)

+1.5V to +1.5VS

Optional, if +1.5VS can combine with +1.5V_1

+1.5V, +1.5VS
U43 SI4800BDY-T1-E3_SO8
J3 JUMP_43X118@ +1.5V_1
C557 1U_0603_10V4Z
R441 470_0603_5%
9/1 Del C550/C558/C559
+VSB R436 510K_0402_5%
1.5VS_GATE
DMN66D0LDW-7 2N_SOT363-6
Q41B SUSP
C546 0.1U_0603_25V7K
R435 @ 510K_0402_5%
SUSP Q41A DMN66D0LDW-7 2N_SOT363-6
4/2 Change PN of Q41 from SB00000D900 to SB00000DH00(ESD issue)
<39,47> ACIN
ACIN @ SSM3K7002FU_SC70-3 Q39
9/10 Change symbol of Q39 to SC70-3

11/26 Change R448 from 470 ohm to 22 ohm

+0.75VS R448 22_0603_5%
+1.05VS R661 470_0603_5% @
+1.1VS_VTT R729 470_0603_5% @
+1.8VS R424 470_0603_5% @
+1.5V R437 470_0603_5% @
SSM3K7002FU_SC70-3 Q44 SUSP
SSM3K7002FU_SC70-3 Q64 SUSP @
SSM3K7002FU_SC70-3 Q66 SUSP @
SSM3K7002FU_SC70-3 Q37 SUSP @
SSM3K7002FU_SC70-3 Q38 SYSON# @
9/10 Change symbol of Q37/Q38/Q44/Q64/Q66 to SC70-3
11/13 Change Bom structure of R424/R448/R661/R729/Q37/Q44/Q64/Q66 from mount to @

10/9 Delete R428, R431 and Q36
(Remove SBPWR_EN# Function)

+5VALW
R439 100K_0402_5%
<36,43> SYSON#
SYSON#
<39,55> SYSON
SYSON
Q40A DMN66D0LDW-7 2N_SOT363-6
R434 100K_0402_5%
4/2 Change PN of Q40 from SB00000D900 to SB00000DH00(ESD issue)

+5VALW
R433 100K_0402_5%
<41,52> SUSP
SUSP
<39,41,50> SUSP#
Q40B DMN66D0LDW-7 2N_SOT363-6
R438 10K_0402_5%
4/2 Change PN of Q40 from SB00000D900 to SB00000DH00(ESD issue)

For Calpella CPU S3 DRAM Power

(1.5V_CPU VDDQ)

+1.5V, +1.5V_1
C969 0.1U_0402_16V4Z
C970 0.1U_0402_16V4Z
C971 0.1U_0402_16V4Z
C972 0.1U_0402_16V4Z
U48 SI4856ADY_SO8
250mil(6A)
C592 0.1U_0402_16V4Z
R495 470_0603_5%
12/7 Add R325=20K ohm(For Capella S3 resume become shutdown issue
R496 100K_0402_1%
+VSB
1.5V_1_GATE
R325 20K_0402_5%
C593 0.1U_0603_25V7K
SUSP SSM3K7002FU_SC70-3 Q79
9/10 Change symbol of Q79 to SC70-3
SUSP SSM3K7002FU_SC70-3 Q55
9/10 Change symbol of Q55 to SC70-3

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	NCQF0 M/B LA-5981P Schematic	1.0

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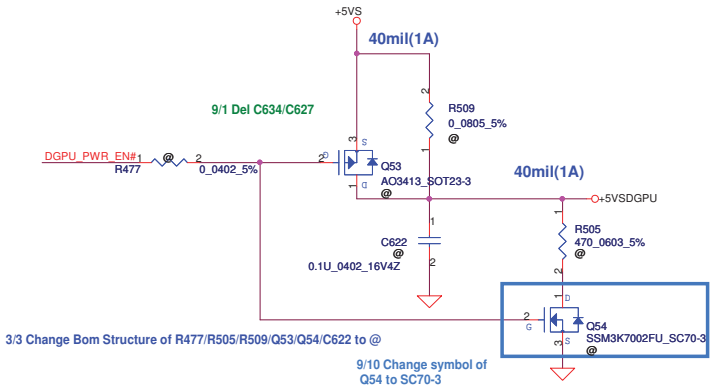
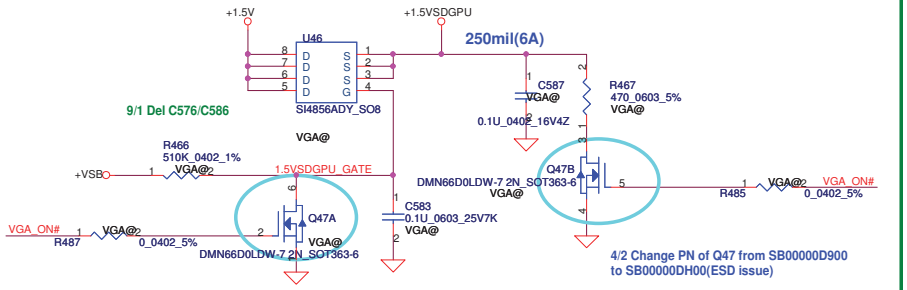
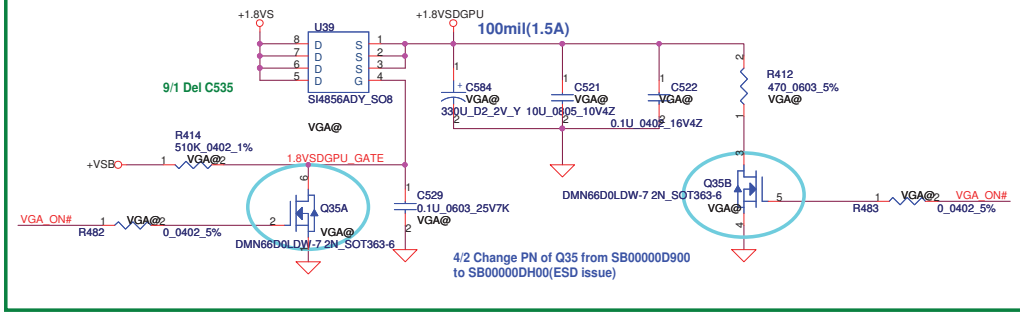
+5VS to +5VSDGPU

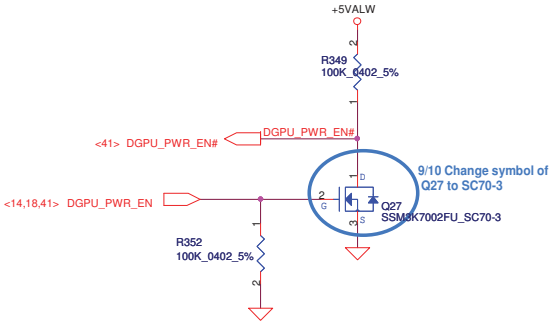


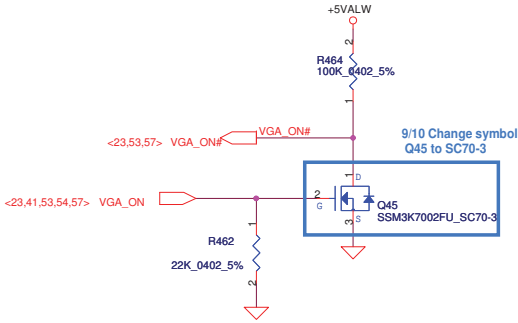
+1.5V to +1.5VSDGPU Transfer



+1.8VS to +1.8VSDGPU Transfer







Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: VGA DC Interface

Size	Document Number	Rev
B	NCQF0 M/B LA-5981P Schematic	1.0

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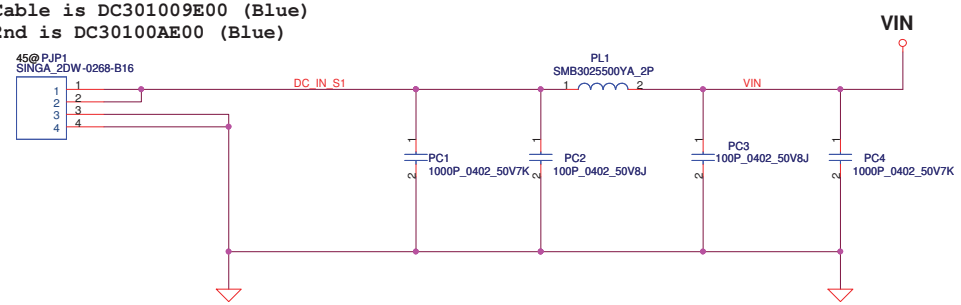
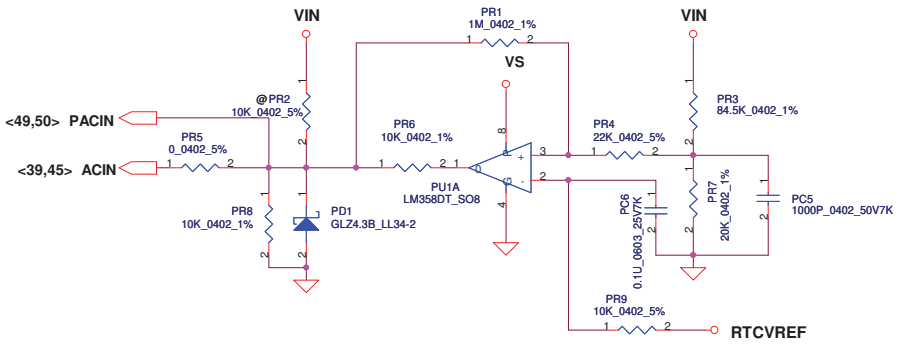
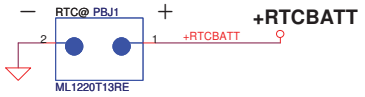
On board conn is DC301001Y00
Cable is DC301009E00 (Blue)
2nd is DC30100AE00 (Blue)

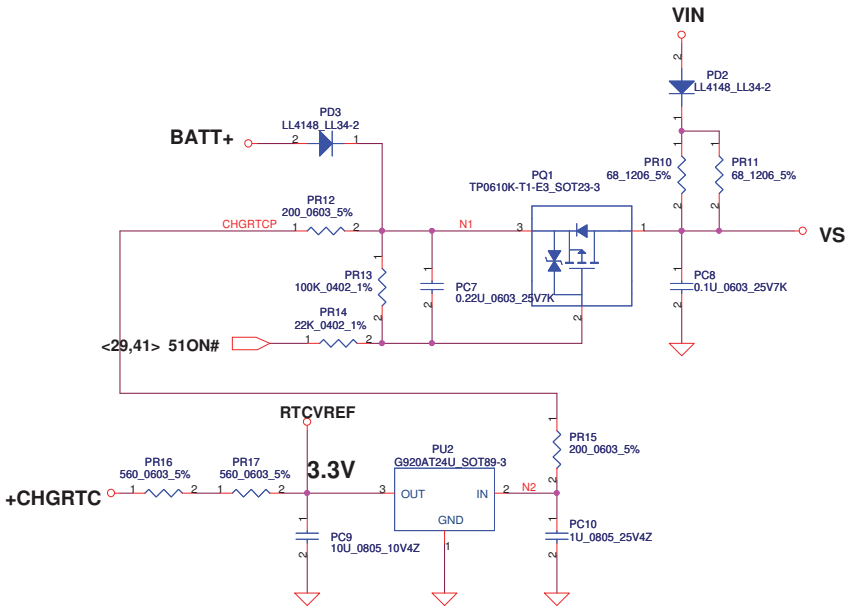


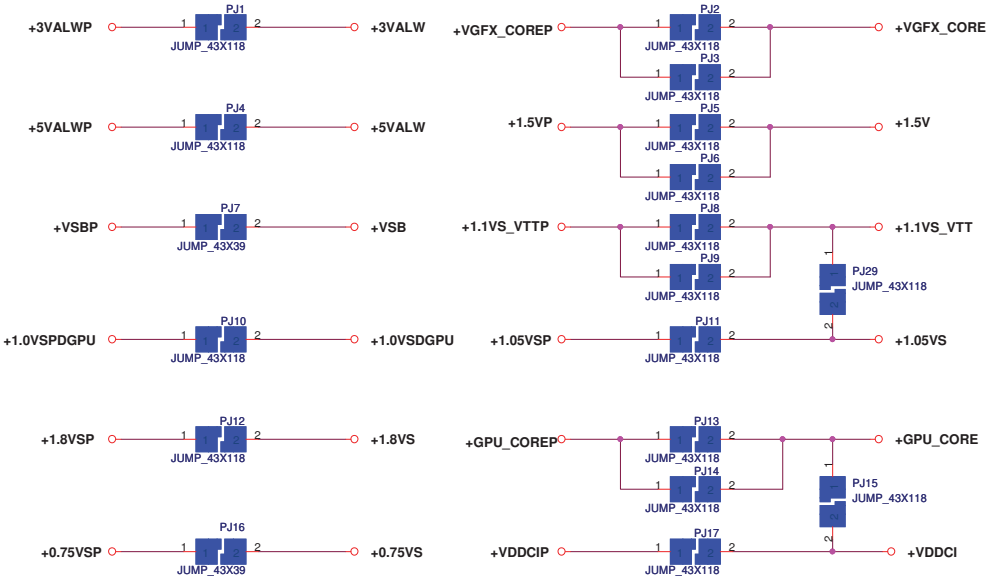




Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **DCIN & DETECTOR**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1
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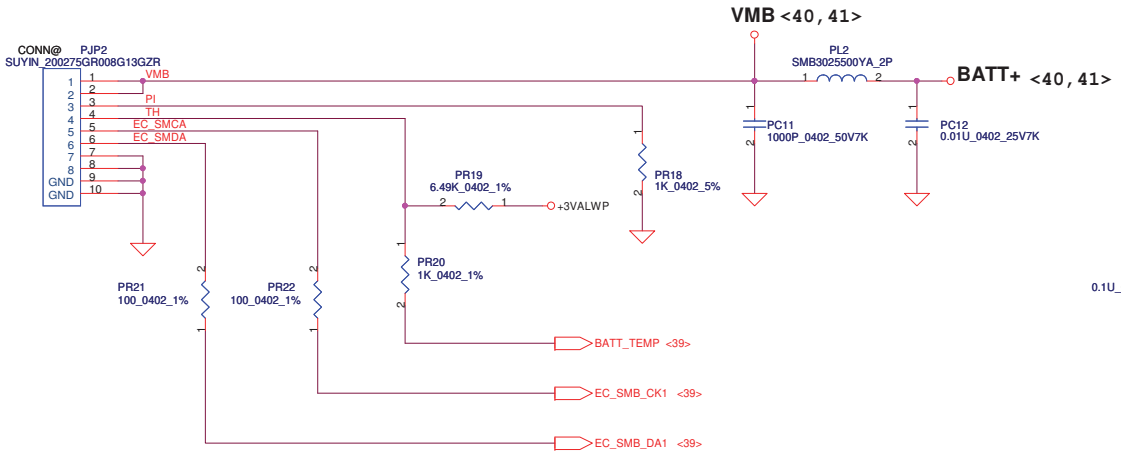


Reference only!! Not SPEC

PH1 under CPU botten side :

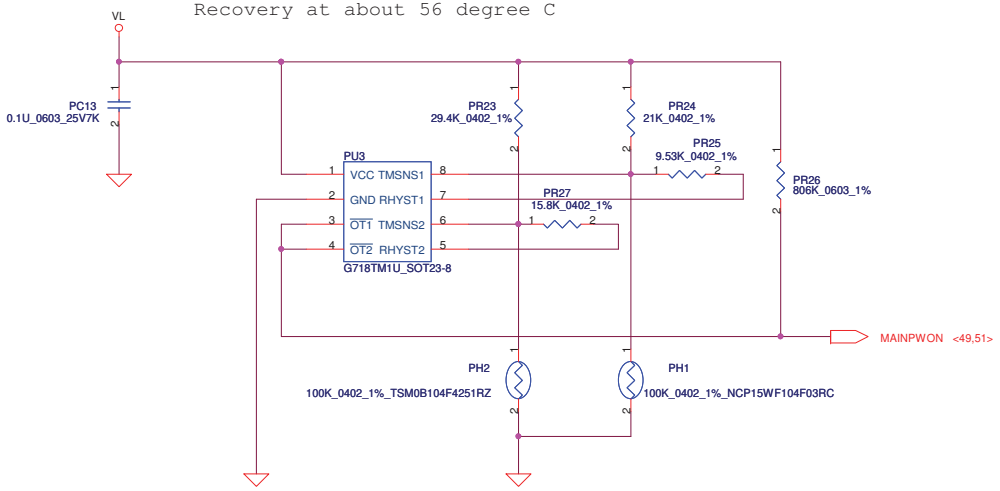
CPU thermal protection at about 92 degree C

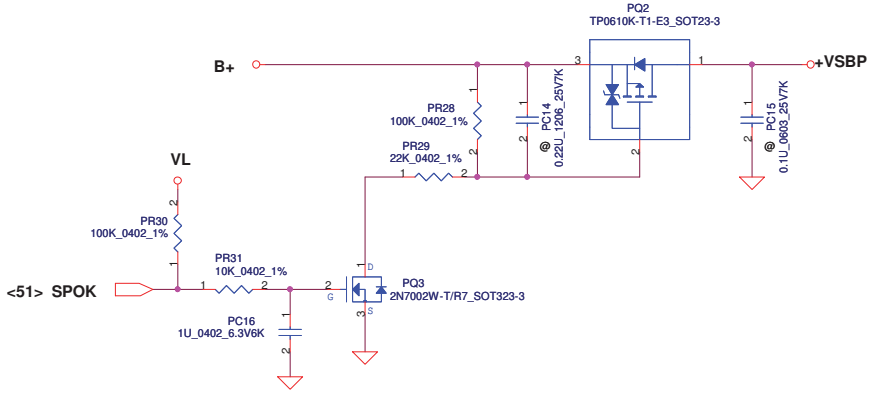
Recovery at about 56 degree C

PH2 under FAN down side :

CPU thermal protection at about 82 degree C

Recovery at about 56 degree C





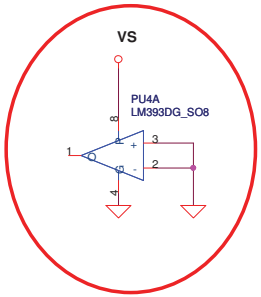
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

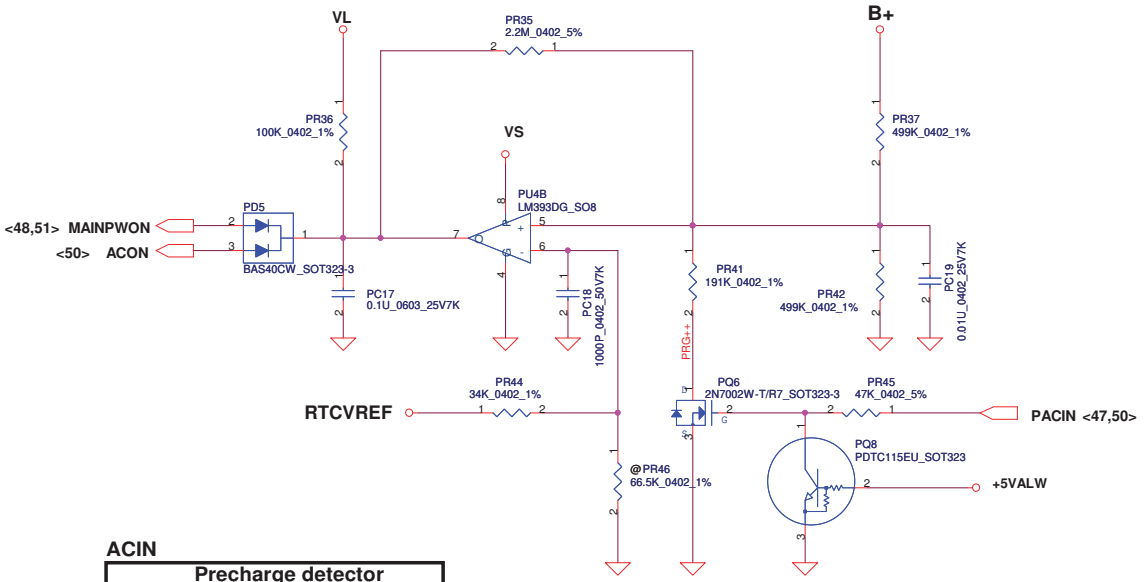
Compal Electronics, Inc.

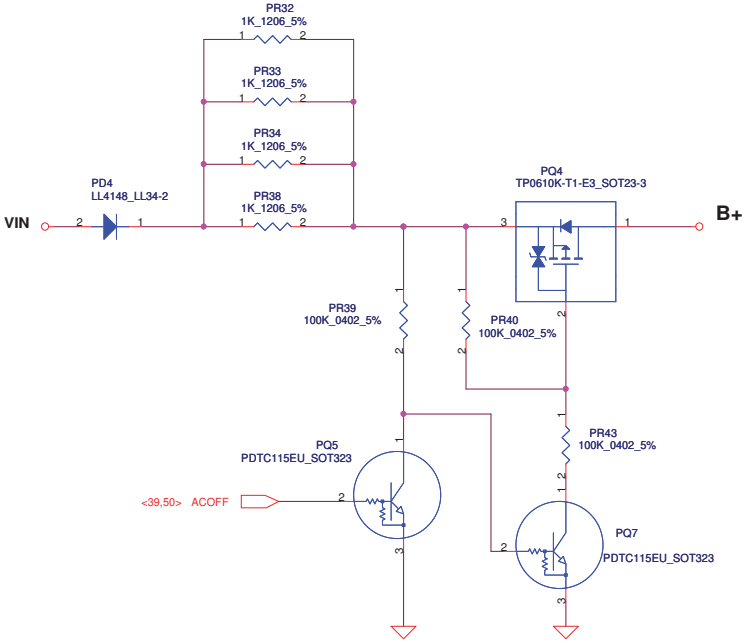
Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 Sheet 48 of 62







ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

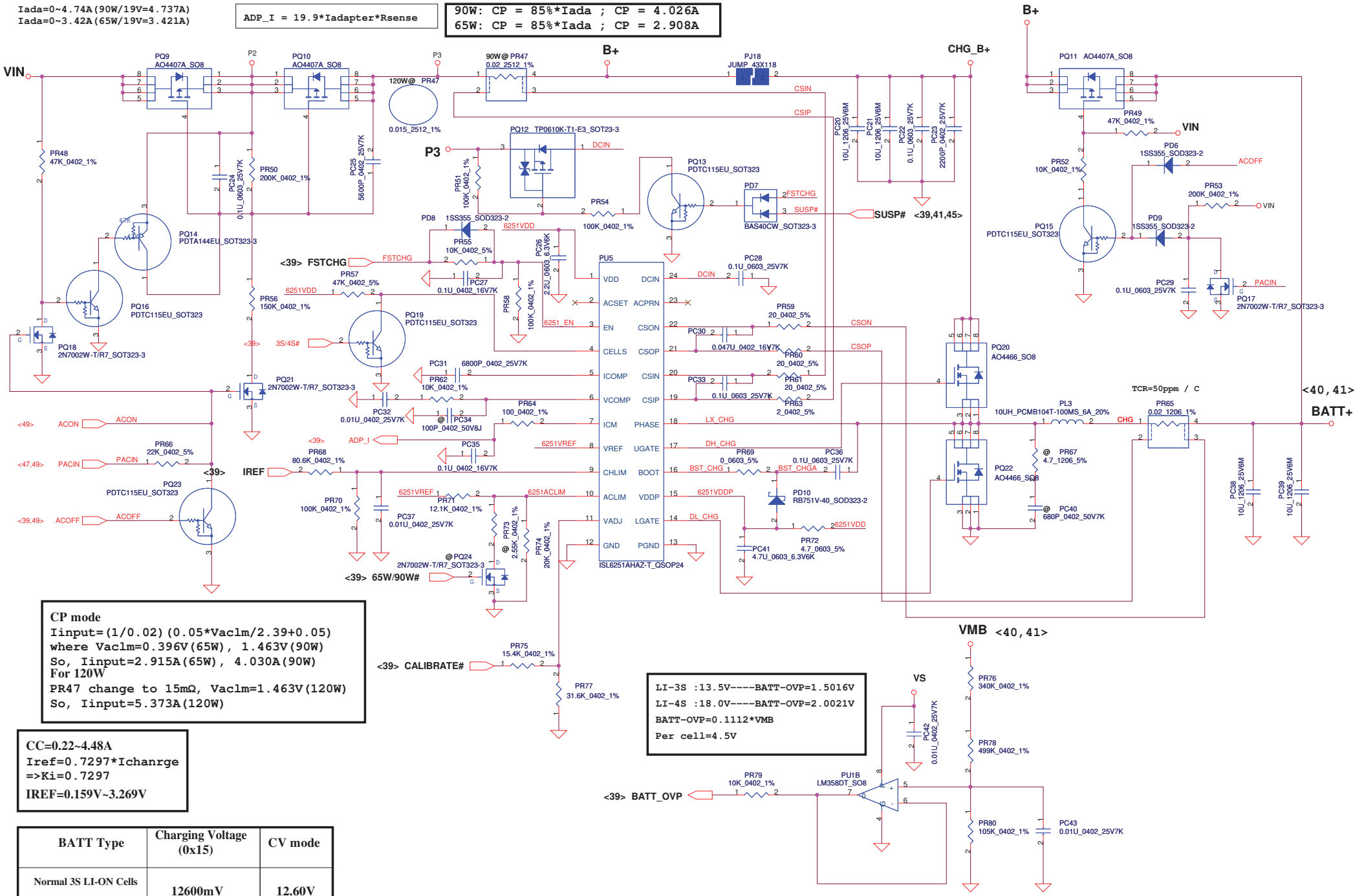
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	PRECHARGE		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 0.1
Date: Sunday, April 18, 2010	Sheet 49 of 62		

Iada=0~4.74A(90W/19V=4.737A)
Iada=0~3.42A(65W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

90W: CP = 85%*Iada ; CP = 4.026A
65W: CP = 85%*Iada ; CP = 2.908A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=0.396V(65W), 1.463V(90W)
So, Iinput=2.915A(65W), 4.030A(90W)
For 120W
PR47 change to 15mΩ, Vaclm=1.463V(120W)
So, Iinput=5.373A(120W)

CC=0.22~4.48A
Iref=0.7297*Ichanrge
=>Ki=0.7297
IREF=0.159V~3.269V

LI-3S :13.5V----BATT-OVP=1.5016V
LI-4S :18.0V----BATT-OVP=2.0021V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

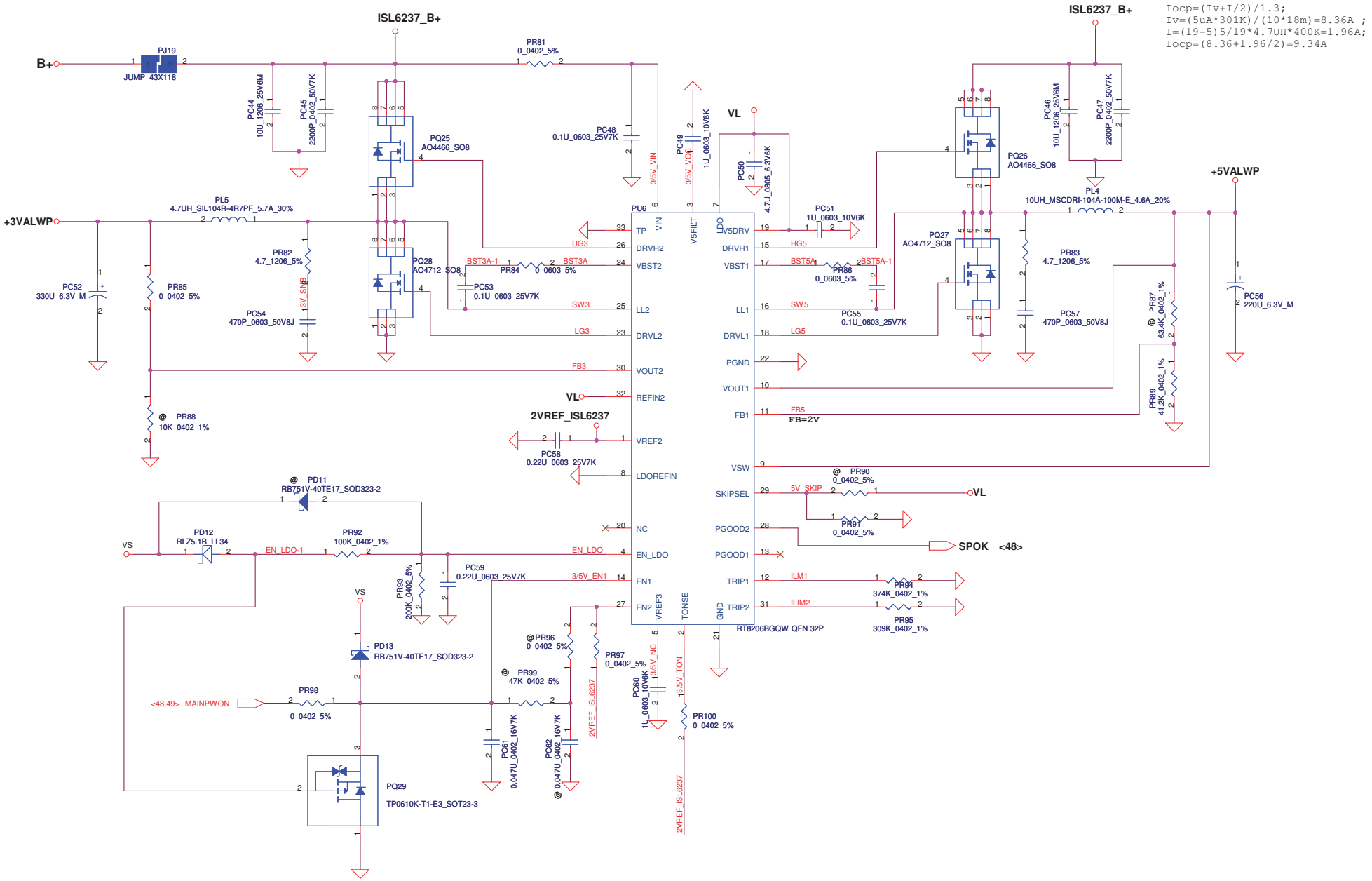
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 0.1

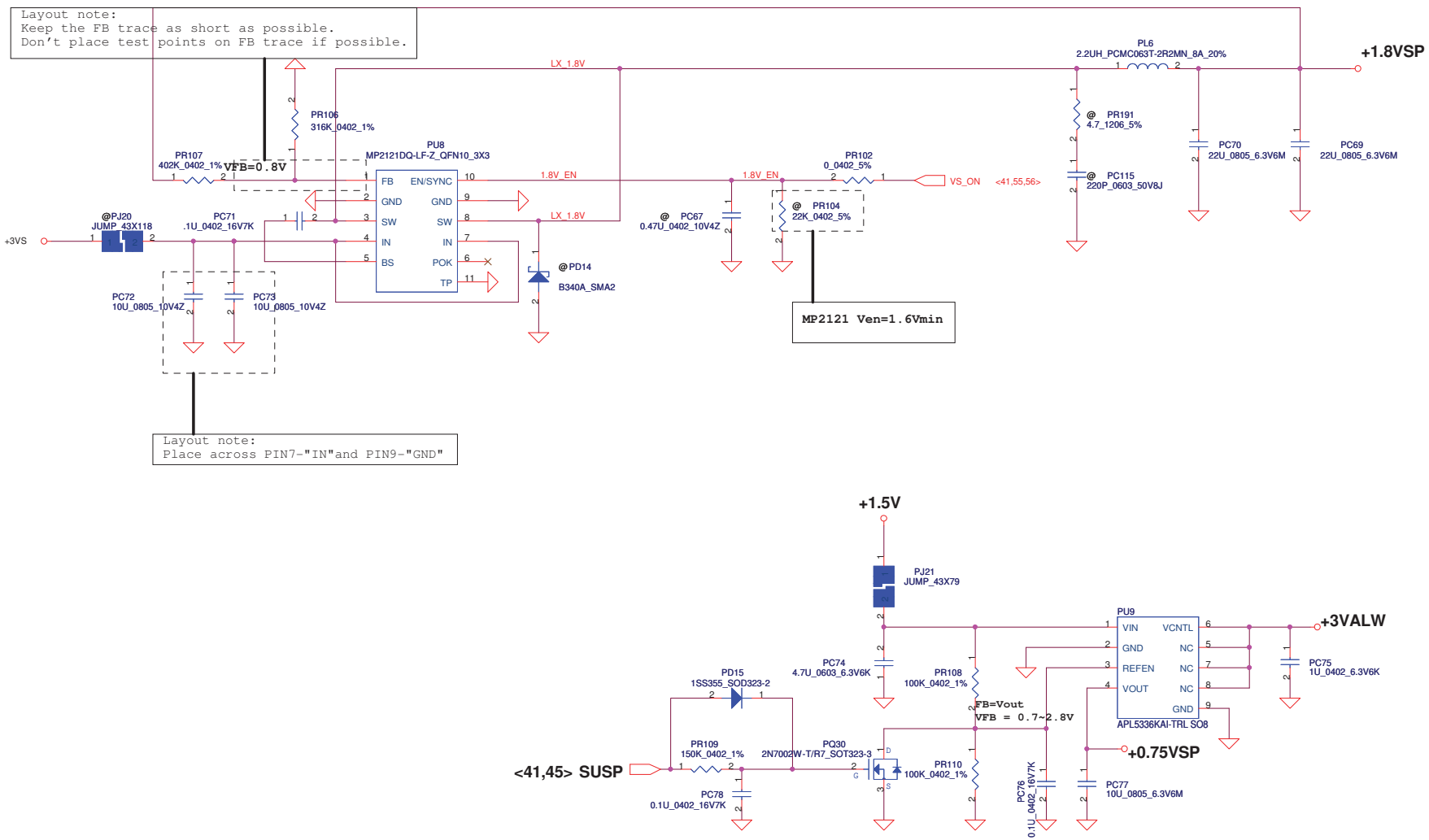
Date: Sunday, April 18, 2010 | Sheet 50 of 62



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title	3VALW/5VALW	
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic	Rev: 0.1
Date: Sunday, April 18, 2010	Sheet 51 of 62	



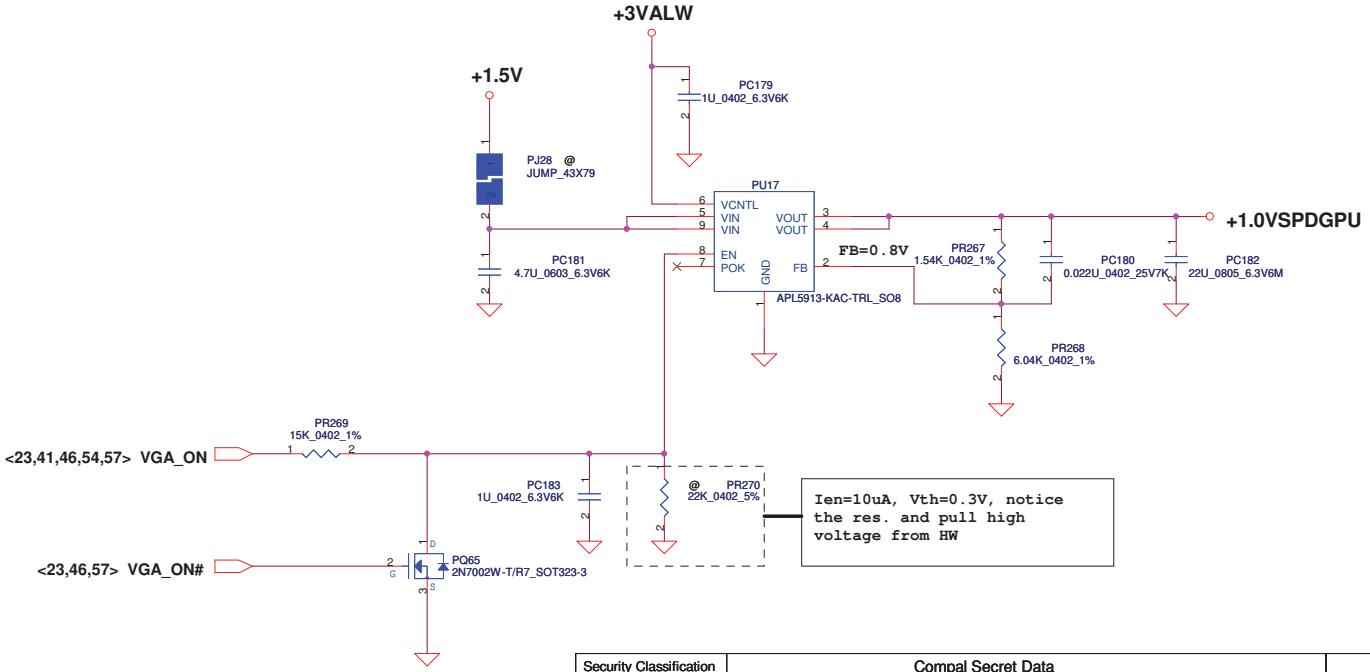
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **+1.8VSP/+0.75VSP**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 52 of 62



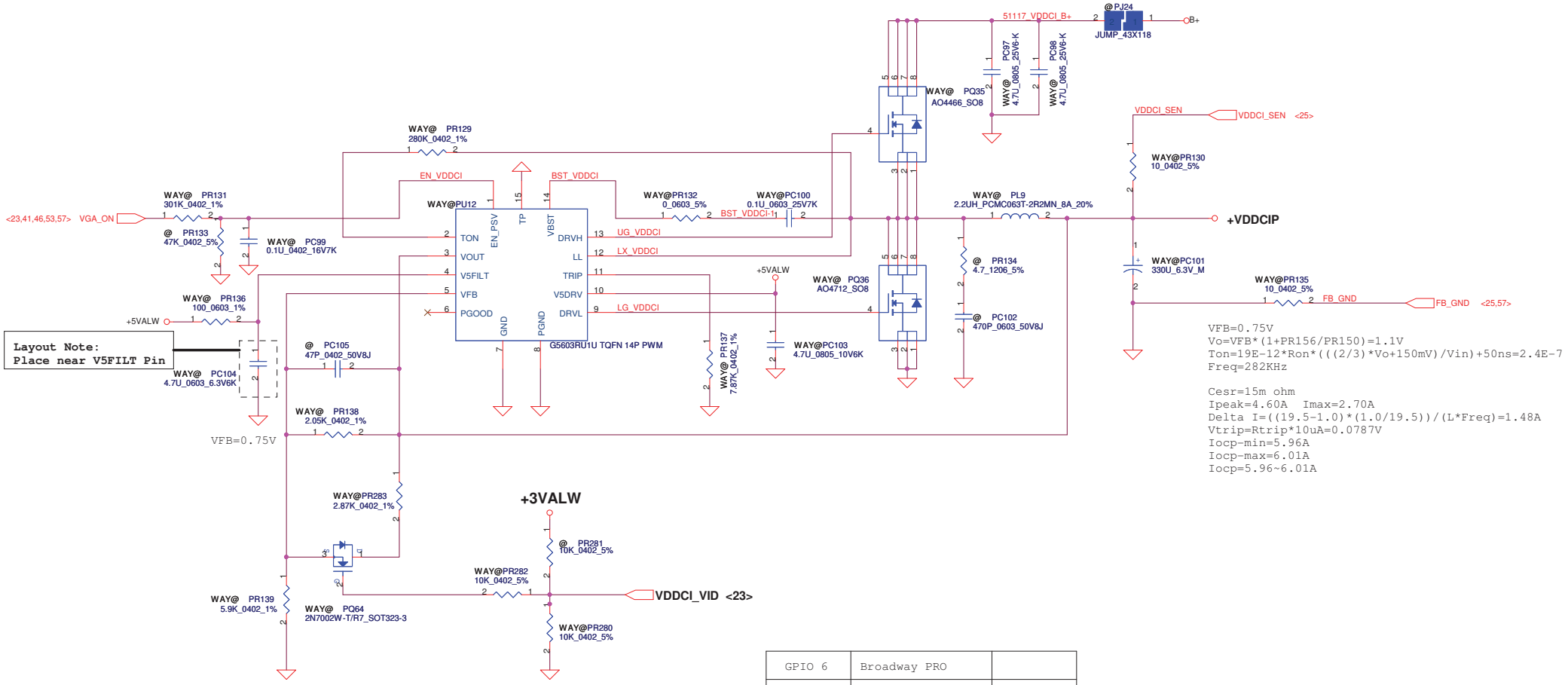
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **+1.0VSDGPU**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 53 of 62



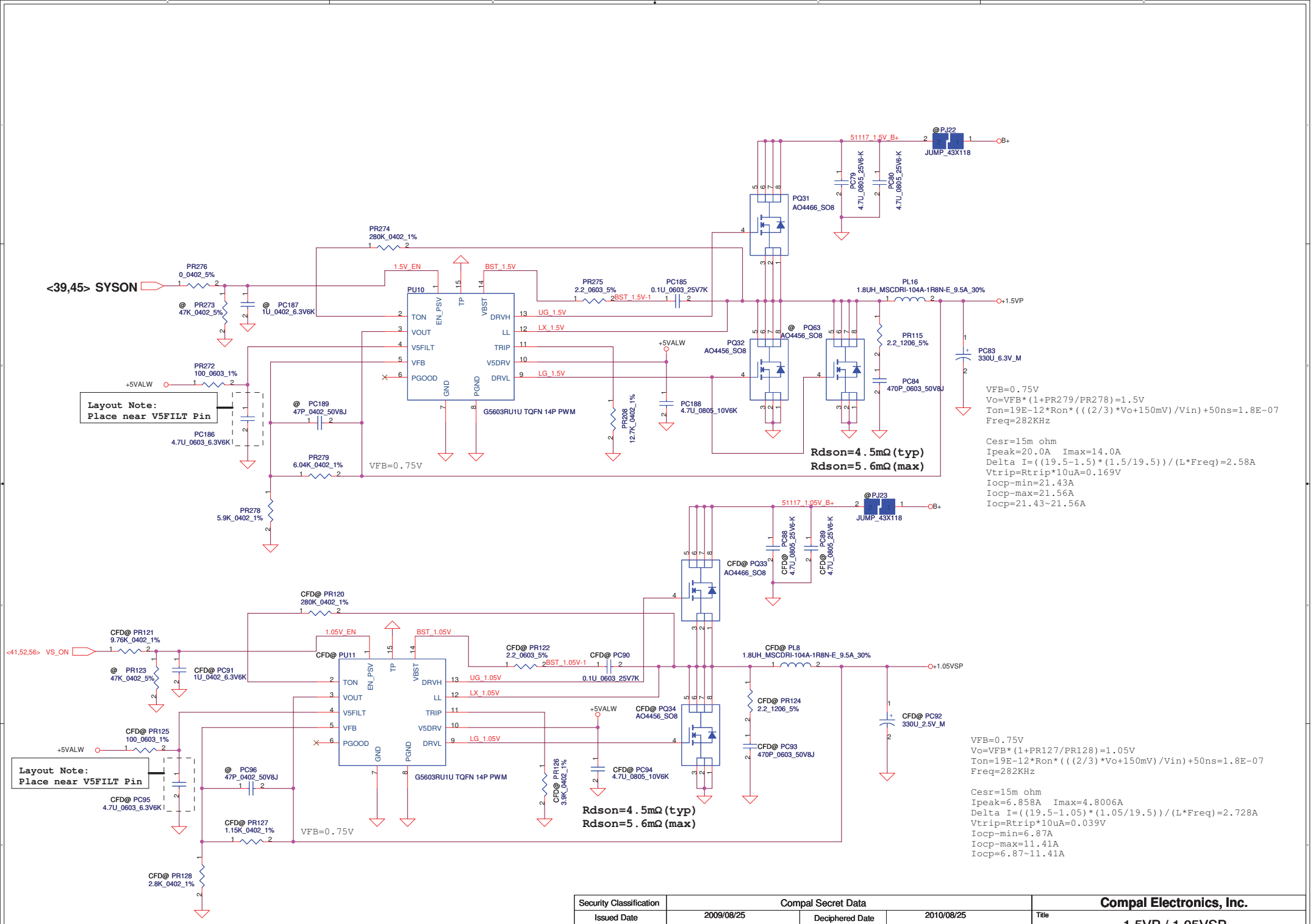
GPIO 6	Broadway PRO	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	

Compal Electronics, Inc.

Title: **VDDCIP**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 54 of 62



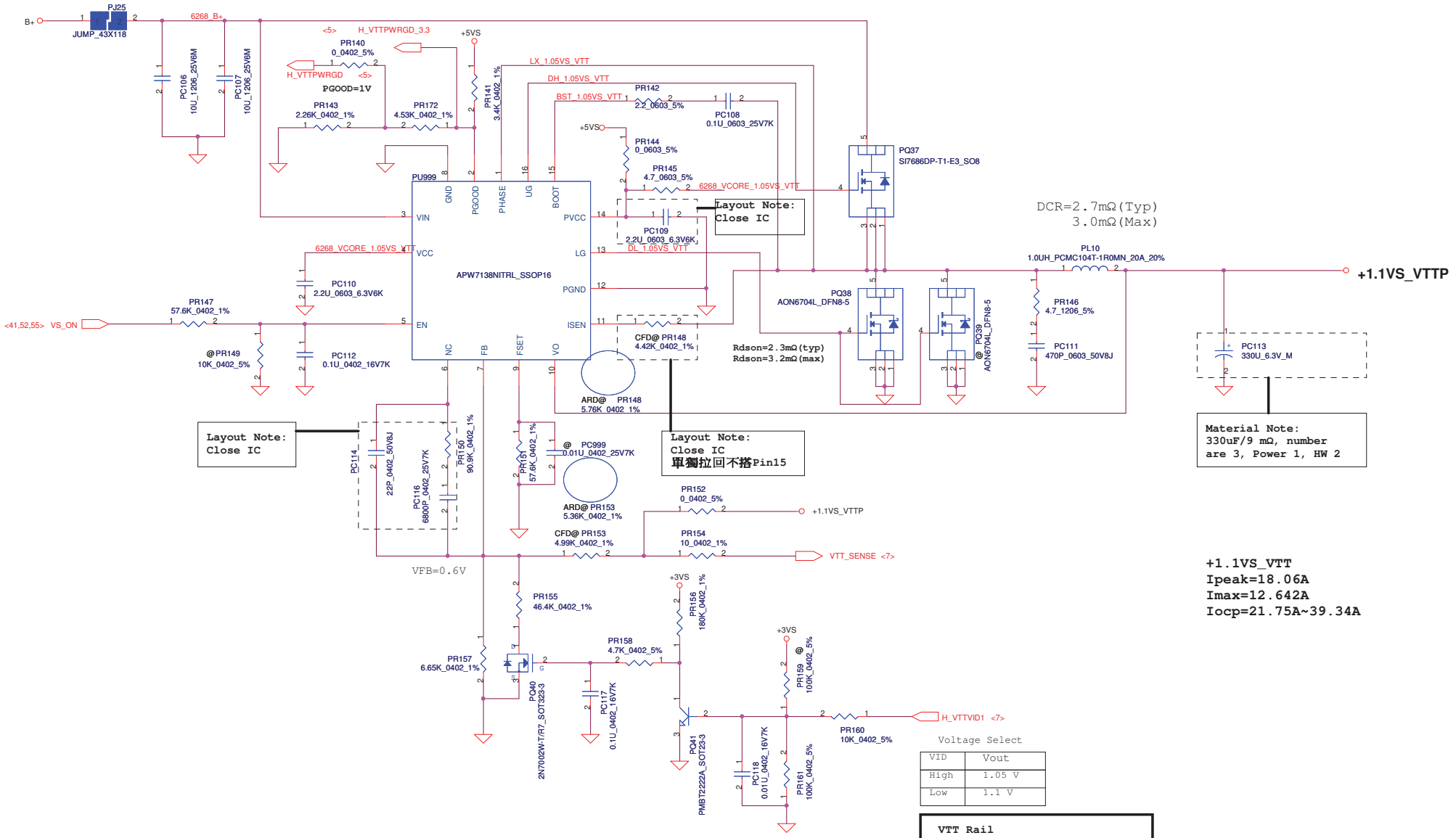
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: 1.5VP / 1.05VSP

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 Sheet 55 of 62



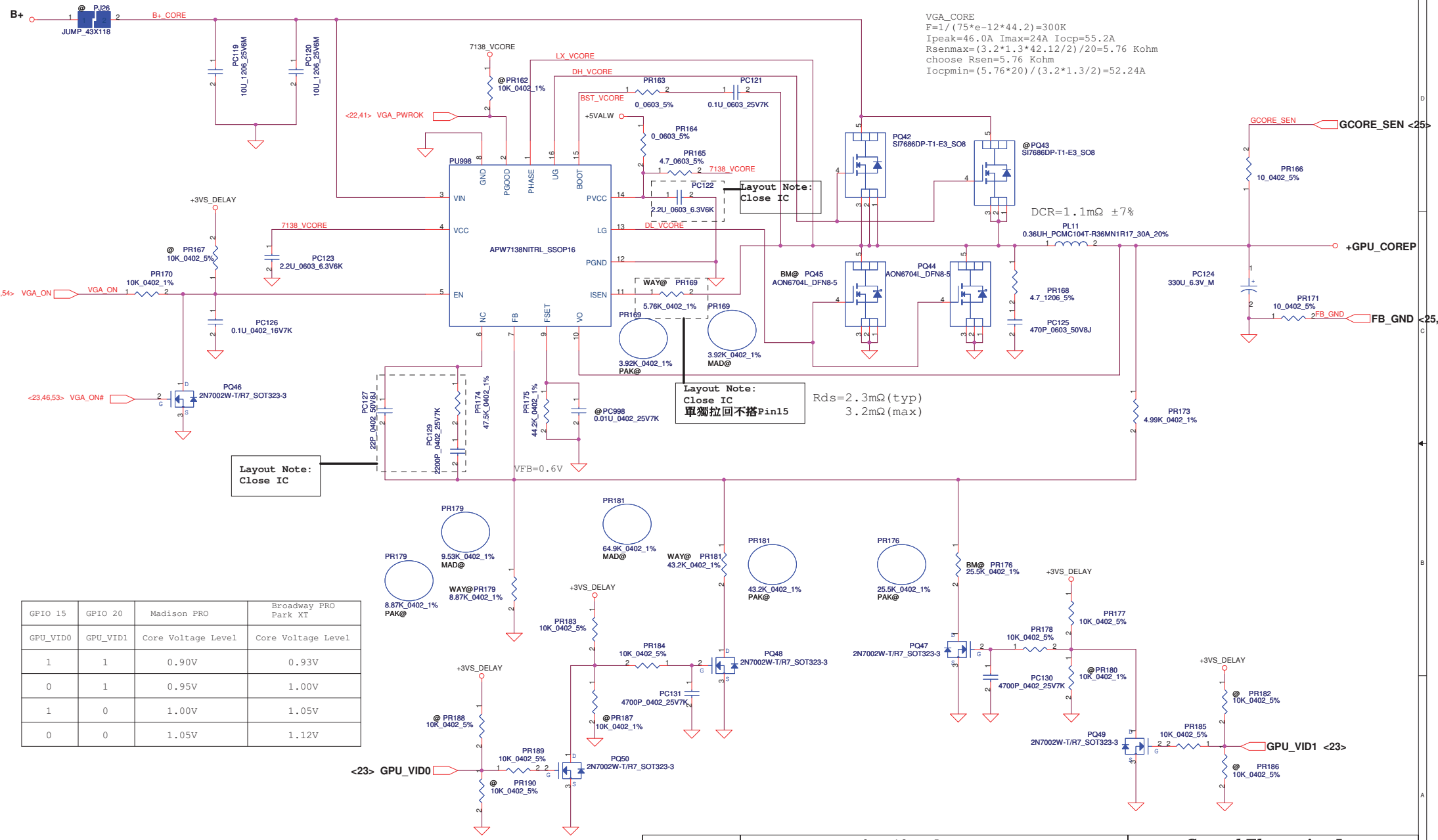
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: +1.1VS_VTTP

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 0.1

Date: Sunday, April 18, 2010 | Sheet 56 of 62



VGA_CORE
F=1/(75*e-12*44.2)=300K
Ipeak=46.0A Imax=24A Iocp=55.2A
Rsenmax=(3.2*1.3*42.12/2)/20=5.76 Kohm
choose Rsen=5.76 Kohm
Iocpmin=(5.76*20)/(3.2*1.3/2)=52.24A

GPIO 15	GPIO 20	Madison PRO	Broadway PRO Park XT
GPU_VID0	GPU_VID1	Core Voltage Level	Core Voltage Level
1	1	0.90V	0.93V
0	1	0.95V	1.00V
1	0	1.00V	1.05V
0	0	1.05V	1.12V

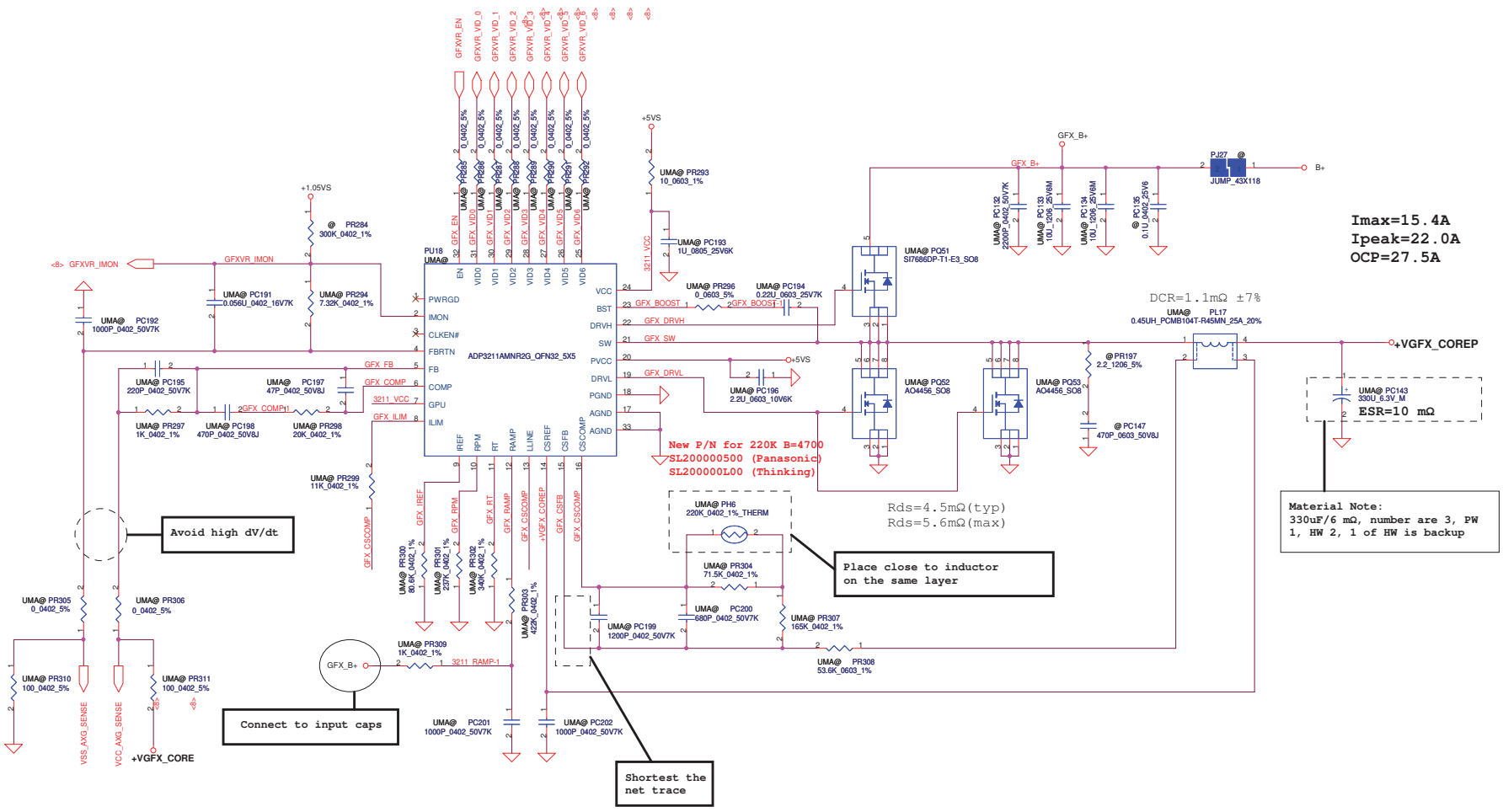
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: GPU_COREP

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 Sheet 57 of 62



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

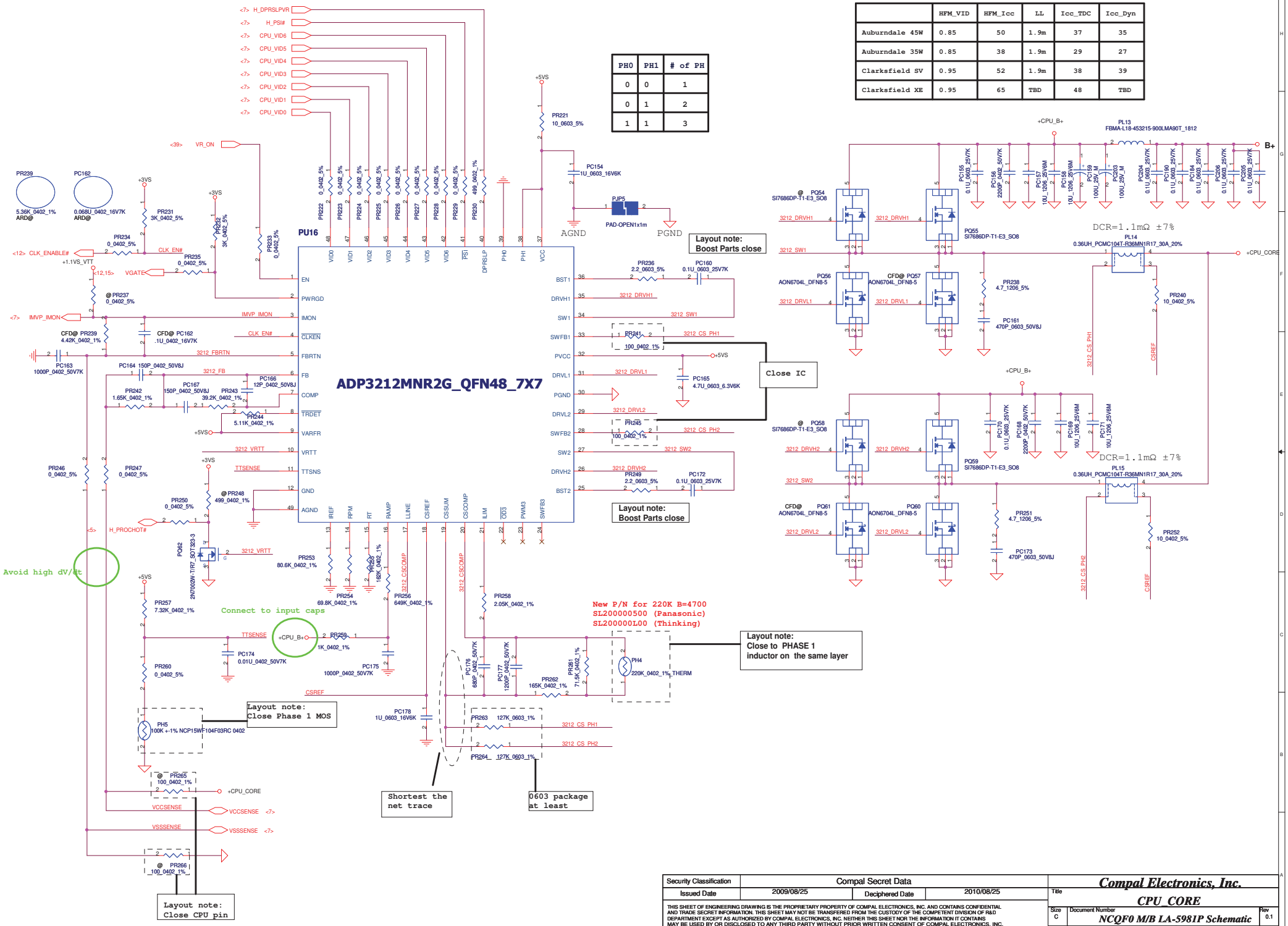
Title: +GFX_COREP

Size	Document Number	Rev
C	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 58 of 62

PH0	PH1	# of PH
0	0	1
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	0.85	50	1.9m	37	35
Auburndale 35W	0.85	38	1.9m	29	27
Clarksfield SV	0.95	52	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	CPU_CORE		
Size C	Document Number NCQF0 M/B LA-5981P Schematic		Rev 0.1
Date: Sunday, April 18, 2010		Sheet 59 of 62	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify chager circuit	Design change	0.1	48	Change BQ24751 to ISL6251	2009 10/07	EVT
2	During shutdown, GFX has a pulse	Make GFX_EN pull down quickly	0.1	58	~~Add PD15 to connect GFX_EN and VS_ON~~	~~2009~~ 11/02	EVT
3	Park XT SPEC change	More display performance	0.1	57	Change PR176 from 31.6KΩ to 43.2KΩ(SD034432280) Change PR179 from 9.53KΩ to 8.87KΩ(SD034887180) Change PR181 from 64.9KΩ to 25.5KΩ(SD034255280)	2009 11/05	EVT
4	ME height not enough	Prevent EL-cap. to knock the door	0.1	51	Change PC56 from 330uF 6L to 220uF 4.5L(SF000002Y00)	2009 11/11	EVT
5	Cost review	Cost down	0.1	57	Change PC124 from 6mΩ to 10mΩ(SF000002O00)	2009 11/11	EVT
6		Tune OCP	0.1	58	Change PR294 from 6.98KΩ to 7.15KΩ(SD034715180) Change PR299 from 10.7KΩ to 11KΩ(SD034110280)	2009 11/11	EVT
7		Tune OCP & Imon	0.1	59	Change PR239 from 499KΩ to 4.53KΩ(SD034453180) Change PC162 from 0.082uF to 0.1uF(SE076104KM8) Change PR258 from 1.91KΩ to 2.05KΩ(SD034205180) ~~Change PR261 from 73.2KΩ to 71.5KΩ(SD034715280)~~ Change PR263, PR264 from 120KΩ to 127KΩ(SD014127380) Change PR258 from 1.91KΩ to 2.05KΩ(SD034205180)	2009 11/11	EVT
8							
9	Not enough space	Not enough space	0.1	52	Change PL6 from 10x10 to 7x7(SH000006I80)	2009 11/12	EVT
10	HW Jason request	Add new VGA voltage table	0.1	57	Add PR176,PR179,PR181 virtual parts	2009 11/19	EVT
11	Design review	1.5V change APW7138 to TPS51117	0.1	55		2009 11/19	EVT
12	Design review	Provide GFX output a reference	0.1	58	Add PR310,PR311	2009 12/03	EVT
13	S3 resume shutdown	Make sure 0.75V high later than 1.5V and low earlier than 1.5V	0.1	52	Add PD15	2009 12/08	EVT
14	Design review	1.5V tune output voltage	0.2	55	Change PR278 from 59KΩ to 124KΩ(SD034124380) Change PR279 from 24KΩ to 124KΩ(SD034124380) Change PR208 from 9.09KΩ to 16.9KΩ(SD034169280)	2009 12/15	DVT
15	Power OFF sequence	+1.0vsdgpu need power down within 20ms	0.2	53	Add PQ65	2010 01/05	DVT
16	HW request raise 1% voltage	1.5V tune output voltage	0.2	55	Change PR279 from 124KΩ to 127KΩ(SD034127380)	2010 01/07	DVT
17	OTP activity	Have a pull high	0.2	48	Enable PR23	2010 01/07	DVT
18	EMI solution	Add bypass cap from B+ to Gnd	0.2	59	Add PC184,PC190,PC204,PC205,PC206	2010 01/08	DVT
19	GFX character	Improve Imon, Loadline	0.2	58	Change PR294 from 7.15KΩ to 7.32KΩ(SD034732180) Change PR308 from 43.2KΩ to 53.6KΩ(SD034536380)	2010 01/08	DVT
20	CPU character	Improve Imon, Loadline, Transient	0.2	59	Change PR239 from 4.53KΩ to 4.42KΩ(SD000004J80) Change PC176 from 390pF to 680pF(SE074681K80)	2010 01/08	DVT
21	Costdown	Change pack from 1206 to 0805	0.2		Change PC79,PC80,PC88,PC89,PC97,PC98 from 1206 to 0805(SE000006R80)	2010 01/08	DVT
22	Tune sequence	GPU_core need ramp up before VDDCIP	0.2	54	Change PR131 from 10KΩ to 57.6KΩ(SD034576280)	2010 01/08	DVT
23	Run 3D Mark hang	Improve GPU character	0.2	57	Change PL11 from 0.56uH to 0.36uH(SH000005680) Change PR169 from 2.43KΩ to 3.92KΩ(SD034392180) Change PR176 from 31.6KΩ to 25.5KΩ(SD034255280) ~~Change PR181 from 68.1KΩ to 64.9KΩ(SD034649280)~~ Change PR137 from 6.65KΩ to 7.87KΩ(SD034787180)	2010 01/13	DVT

Delete 2009 11/05

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	01/05	P.40	PWR_LED# connect from +3VALW to +3VS; PWR_SUSP_LED# conector from +3VS to +3VALW	
	01/05	P.10	JDIMM1 and JDIMM2 location swap	
	01/05	P.47~60	upgrade PWR schematic	
	01/06	P.31	Change net name of Q85.pin2/5 from +3VS to +3VS_DELAY	
	01/06	P.35	Add one Lid Switch schematic for reserve	
	01/08	P.47~60	upgrade PWR schematic	
	01/08	P.42	Add two of 300 ohm bead for DMIC_CLK and SPDIF signal(L6/L8)	
	01/11	P.47~60	upgrade PWR schematic	
	01/11	P.40	Reserve R120=300 ohm pull-high to +3VALW	
	01/11	P.18	Change net name of Q23.pin2 from VGA_HDMI_DET to HDMI_HPD	
	01/12	P.25	Add C602=330uF to decrease ripple of +GPU_CORE	
	02/25	P.23	Change net connection(from R45.2 to Q7.1)	
	02/25	P.29	Add R37=SG@ 0 ohm connect between DPST_PWM_1 and INVTPWM	
	02/25	P.34	Add C936~C938=mount 0.1uF for slove EMI issue	
	02/25	P.39	Add R430/R442/R446=mount 10k ohm pull-high to +3VALW	
	02/25	P.39	Change Bom structure of R421/R422/R431 from mount to reserve	
	02/25	P.47~63	upgrade PWR schematic	
	03/01	P.5	Del XDP schematic(JP5/R89/R92/R93/R96/C168/R86/R657/R663)	
	03/01	P.14	Add R326/R345/R782/R796(for use JMB380 Ver.C)	
	03/01	P.14	Add Q49/Q50(for use JMB380 Ver.C)	
	03/01	P.47~63	upgrade PWR schematic	
	03/02	P.37	Add R718/C168 (for reset)	
	03/31	P.23	Add Update VRAM Table	
	03/31	P.43	Change value of R4 from 4.7K ohm to 5.62K ohm	
	03/31	P.43	Change value of C3 from 0.1uF to 0.033uF	
	03/31	P.36	Change Bom structure of R654/R658/R280/R281/R324/R331 from mount to @	
	03/31	P.36	Change Bom structure of L32/L33/L69 from @ to mount	
	03/31	P.36	Change symbol and PN of L32/L33/L39 from SM070001310 to SM070000K00	
	03/31	P.24	Change Bom structure of R83 from SG@ to MAD@	
	04/01	P.39	Change footprint of SW2/SW3 from SW_SKRELGE010_2P to SW_NTC317-AB1G-C220C_2P	
	04/02	P.23	Change PN of Q9 from SB00000D900 to SB00000DH00	
	04/02	P.29	Change PN of Q6/Q80/Q81 from SB00000D900 to SB00000DH00	
	04/02	P.30	Change PN of Q84 from SB00000D900 to SB00000DH00	
	04/02	P.31	Change PN of Q85 from SB00000D900 to SB00000DH00	
	04/02	P.31	Change PN of Q61 from SB570020110 to SB000008J10	
	04/02	P.43	Change PN of Q69 from SB00000D900 to SB00000DH00	
	04/02	P.45	Change PN of Q40/Q41/Q42/Q43 from SB00000D900 to SB00000DH00	
	04/02	P.46	Change PN of Q35/Q47 from SB00000D900 to SB00000DH00	
	04/15	P.39	Change PN of SW2/SW3 from SN100001C00 to SN100003R00	
	04/15	P.41	Change Bom structure of SW1 from mount to @	
	04/18	P.29	Add LVDS schematic(U13/U31/C204/C187=@)	
	04/18	P.40	Add R51=@ 0 ohm	
	04/18	P.47~63	upgrade PWR schematic	

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

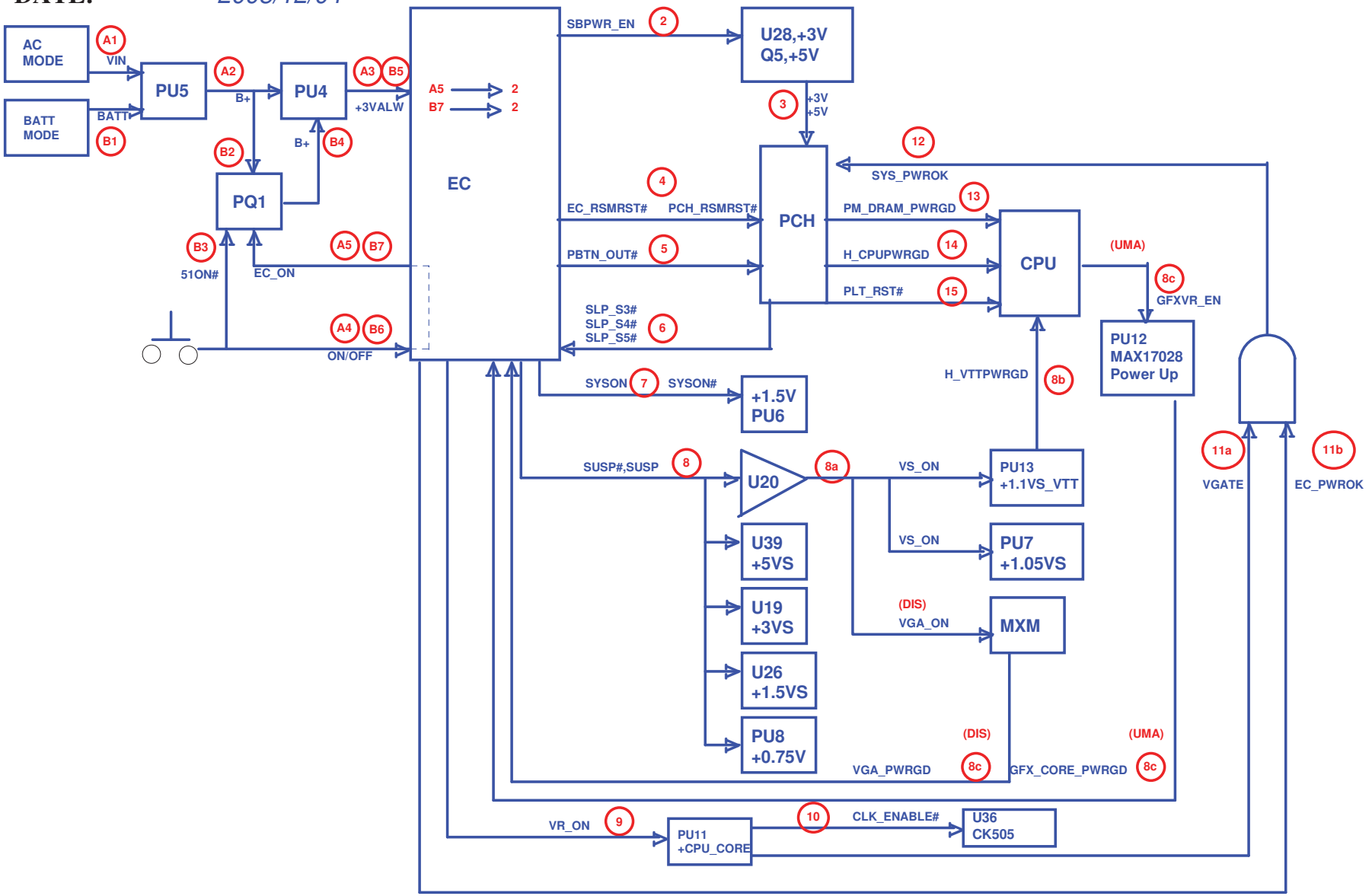
Title: HW PIR

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 61 of 63

COMPAL CONFIDENTIAL

MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Power Sequence Block Diagram

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 0.1

Date: Sunday, April 18, 2010 | Sheet 62 of 62

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	EMI request	Cut-in snubber and couple cap on B+	0.2		Enable 3V/5V/1.5V/1.05V/VTT/GPU snubber	2010 01/13	DVT
25	Buyer request	Costdown	0.2		Change PU10,PU11,PU12 from TPS51117 to G5603(SA00003HM00)	2010 01/14	DVT
26	HW/Ivan request	Raise voltage 2%(Arrendale only)	0.3	56	Change PR153 from 4.99KΩ to 5.36KΩ(SD034536180)	2010 02/11	PVT
27	The same setting for 2nd source	Fix 5V for all IC	0.3	51	Disable PR87	2010 02/23	PVT
28	GPU output cap add 330uF for hang issue	Tune VDDCIP sequence and Power common design	0.3	54	Change PR131 from 57.6KΩ to 301KΩ(SD034301380) Net +5VALW instead of +5VSDGPU	2010 02/23	PVT
29	EMI request	Cut-in snubber and boost res.	0.3		Change PR122,PR142,PR236,PR249,PR275 from 0Ω to 2.2Ω(SD013220B80) Add PR238,PR251 to 4.7Ω Add PC161,PC173 to 470pF	2010 02/25	PVT
30	65/90# only low signal	Fix adapter mode	0.4	50	Disable PR73, PQ24	2010 03/23	Pre-MP
8	Protect logic deformation	Add PH2 function	0.4	48	Change PR23 from 0Ω to 29.4Ω(SD034294280) Add PR27, PH2	2010 03/23	Pre-MP
9	Improve anti-noise	Reduce voltage divider	0.4	54	Change PR138 from 43K to 2.05K(SD034205180) Change PR139 from 124K to 5.9K(SD034590180) Change PR283 from 60.4K to 2.87K(SD034287180)	2010 03/26	Pre-MP
10	Improve anti-noise	Reduce voltage divider	0.4	55	~~Change PR278 from 124K to 5.9K(SD034590180)~~ Change PR279 from 127K to 6.04K(SD034604180) Change PR127 from 24K to 1.15K(SD034115180) ~~Change PR128 from 59K to 2.8K(SD034280180)~~	2010 03/26	Pre-MP
11							
12	Cut-in 120W adapter	Tune a CP setting for 120W adapter	0.4	50	Change PR47 from 0.02 to 0.015(SD000001E00)	2010 03/26	Pre-MP
13	Modify VGA voltage table	Rise Broadway voltage to the same to Park	0.4	57	Change PR179 from 9.53 to 8.87 Change PR181 from 64.9 to 43.2	2010 04/16	Pre-MP
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 0.1

Date: Sunday, April 18, 2010 | Sheet 63 of 63