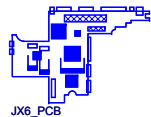
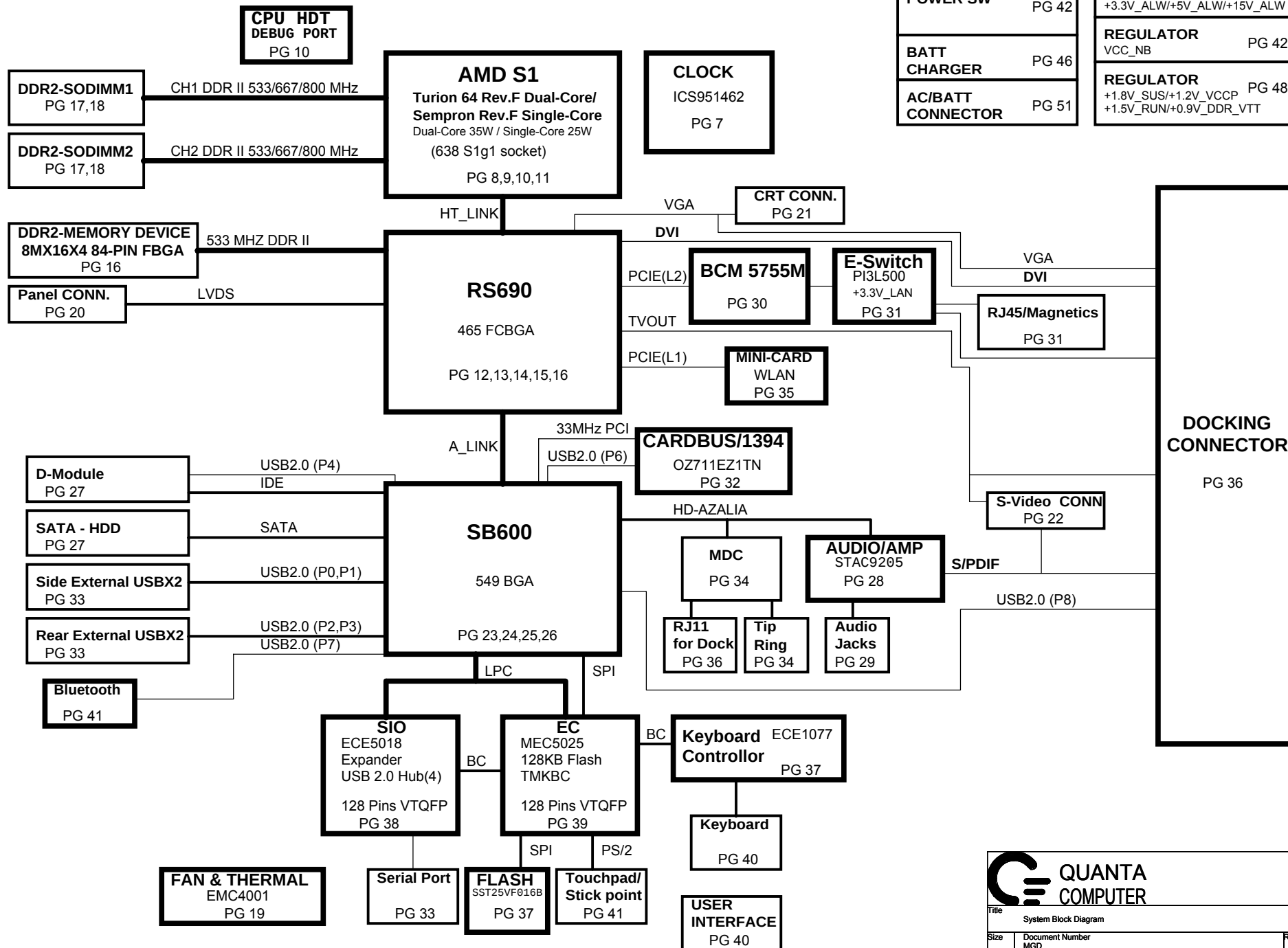


Quanta Project Name: JX6
Dell Project Name: MGD Lite
2007-03-01
REV : D3B
A00/X-Build Stage

 QUANTA COMPUTER			
Title: COVER PAGE			
Size:	Document Number:	Rev:	
	MGD	3A	
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JX6 MGD-INTEGRATED



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31	SIO (MEC5025)
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35	TP,BT & FIR
36	Switch,Keyboard & LED
37	FAN & Thermal
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44	System Reset Circuit
45-46	Battery Selector & Charger
47	DDR2_1.8VSUS, 0.9V
48	1.5VSUS,1.05V(VTT)
49	VGA DC/DC,1.25V,1.05V
50	CPU_MAX8786(3phase)
51	D/D Power
52	RUN Power Switch
53	DCIN,Batt
54	PAD& SCREW
55	EMI CAP
56	SMBUS BLOCK

Power States

Power Rail	Control Signal	S0/M0	S3/M1	S3/M1	S4/M1	S3/M-off	S4/M-off	S5/M-off
+3.3V_ALW								
+5V_ALW								
+3.3V_LAN								
+1.8V_SUS								
+0.9V_DDR_VTT								
+5V_SUS								
+3.3V_SUS								
+5V_RUN								
+3.3V_RUN								
+1.8V_RUN								
+1.25V_RUN								
+1.5V_RUN								
+1.05V_VCCP								
VCC_VCRE								
+LCDVCC								
+5V_MOD								

POWER STATES

State \ Signal	SLP S3#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF)	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

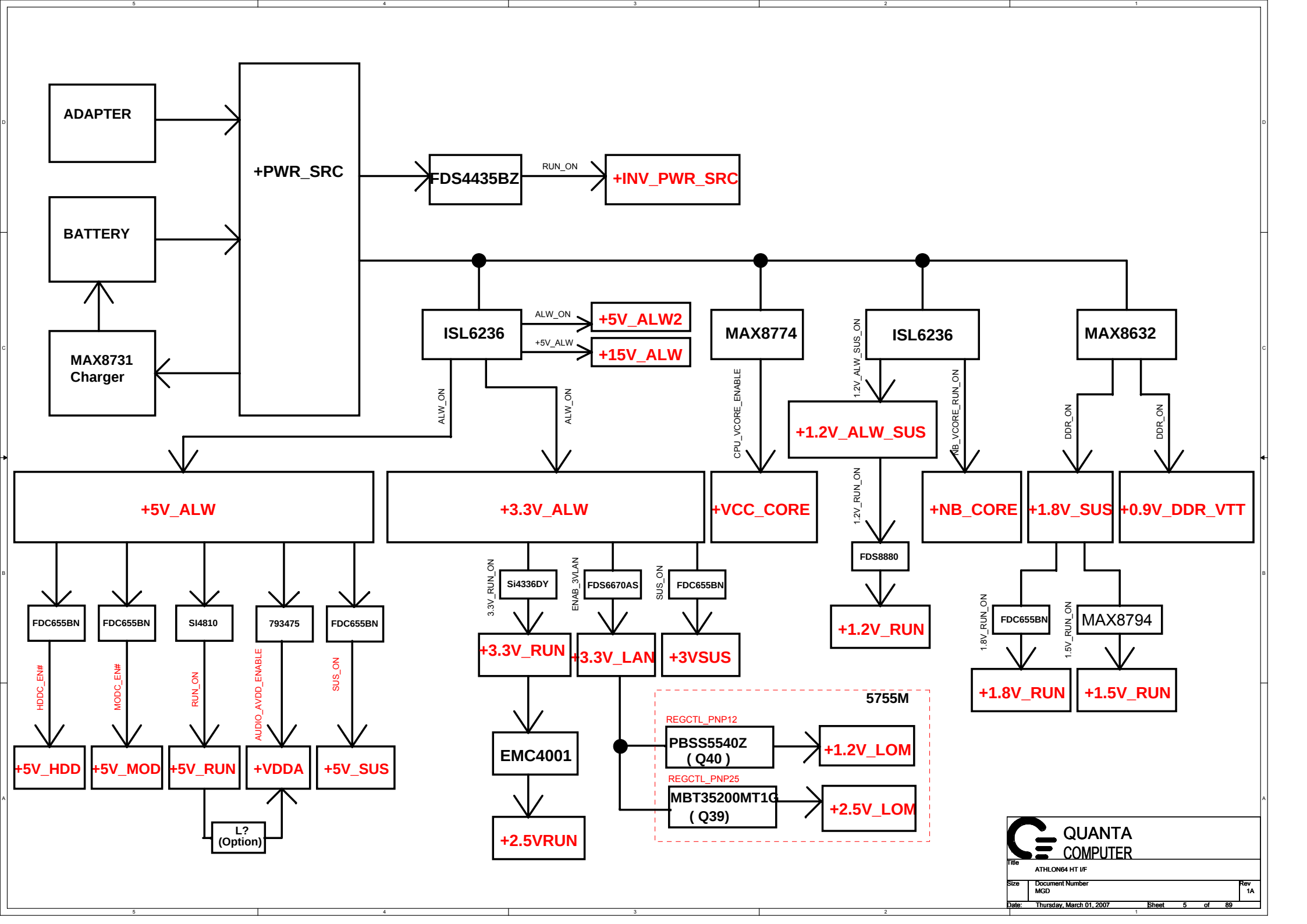
State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW +1.2V_ALW_SUS	+5V_SUS +3.3V_SUS +1.8V_SUS +0.9V_DDR_VTT	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.2V_RUN +1.5V_RUN +VCC_CORE +NB_CORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4 on Battery	OFF	OFF	OFF

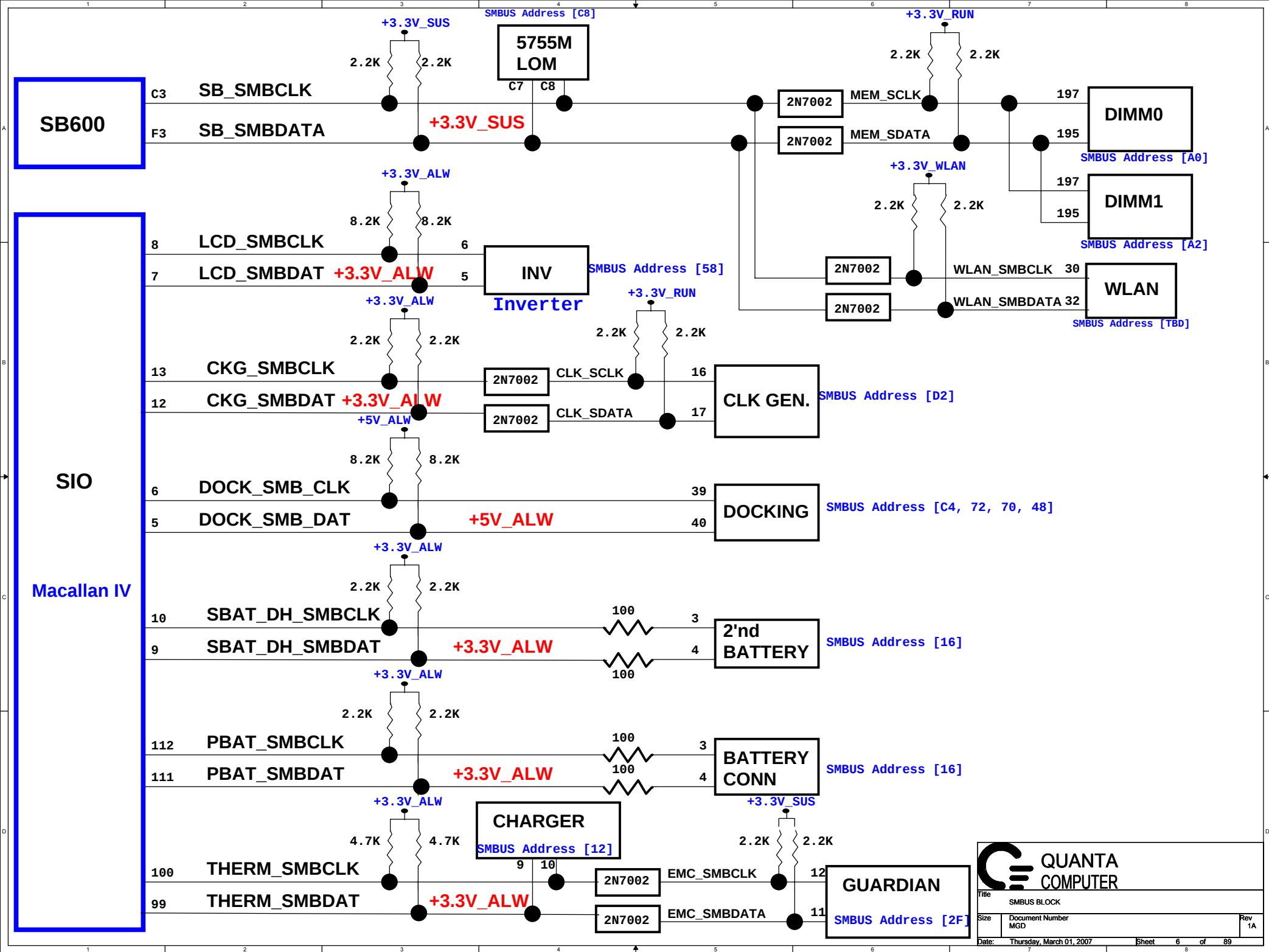
PCI TABLE

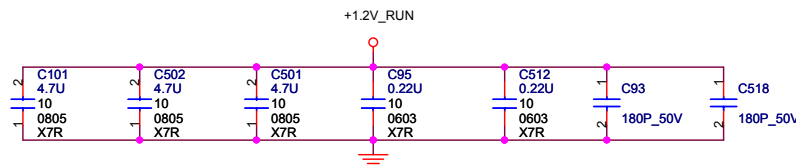
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CardBus	AD17	REQ#1/GNT#1	IRQ_SERIRQ IRQD
Docking	AD24	REQ#0/GNT#0	PIRQA

	USB PORT#	DESTINATION
SB600	0	Side Pair Top
	1	Side Pair Bottom
	2	Rear Bottom as viewed from the back
	3	Rear Top as viewed from the back
	4	Floppy Disk
	5	
	6	Cardbus
	7	BT
	8	Dock
	9	
ECE5018	1	NC
	2	NC
	3	NC
	4	NC

PCI EXPRESS	DESTINATION
Lane 0	MINI CARD-1 WWAN
Lane 1	MINI CARD-2 WLAN
Lane 2	LOM
Lane 3	None







LAYOUT: Place bypass cap on topside of board

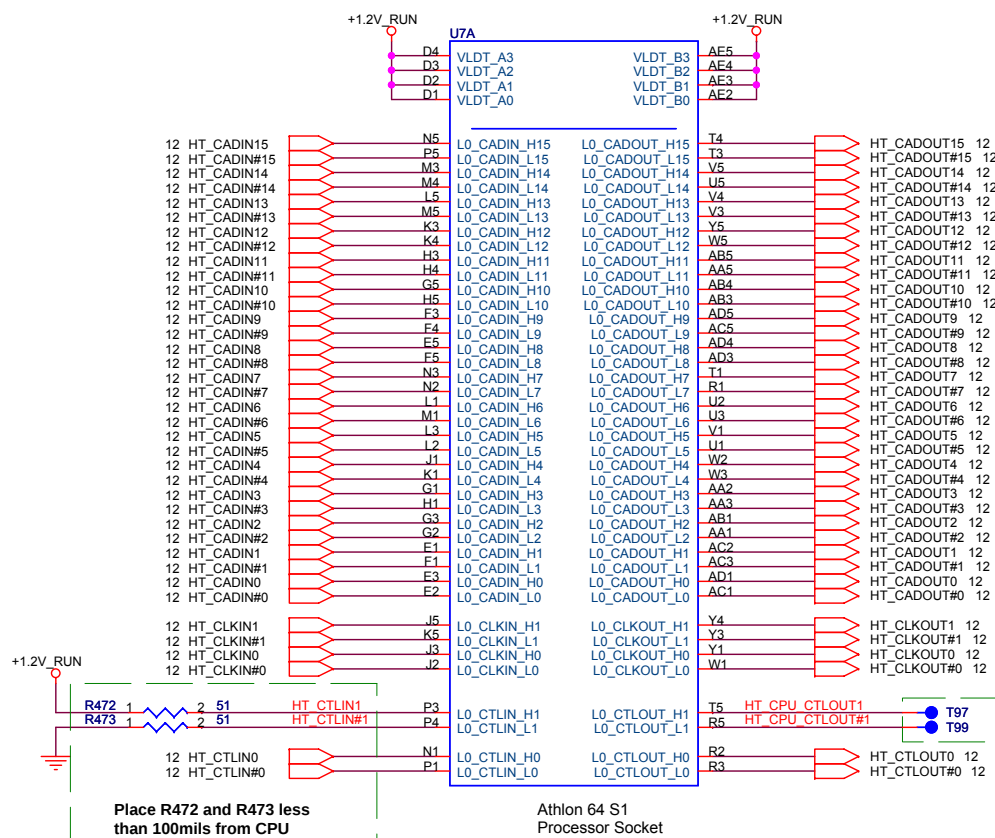


NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

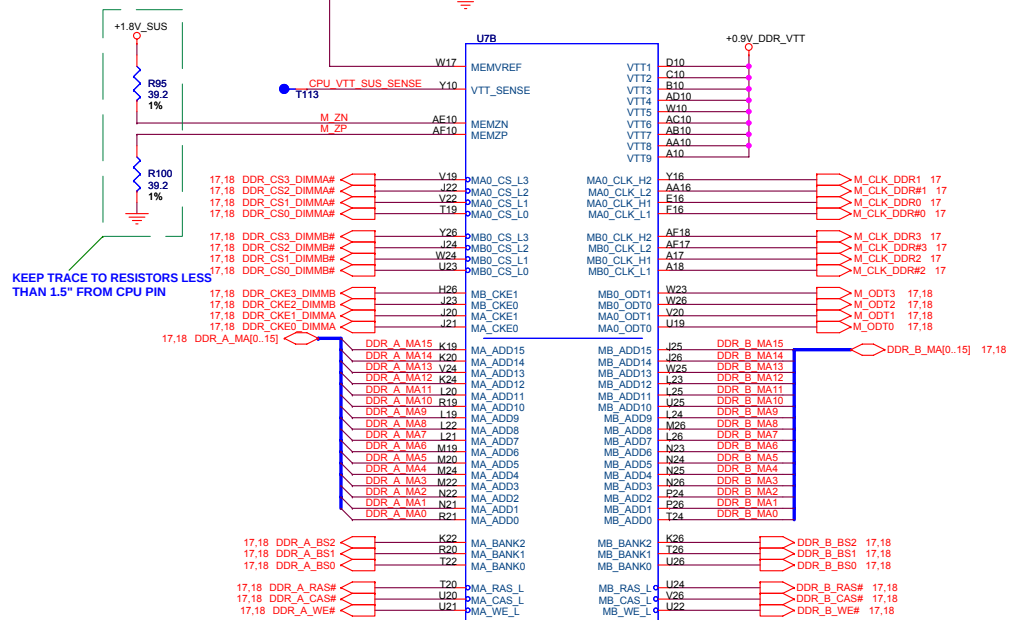


Title		
ATHLON64 HT I/F		
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Date:	Thursday, March 01, 2007	Sheet 8 of 89

CPU_VTT_SUS_SENSE
should be routed as 10mils
and 10mils spacing from any
adjacent signals in X, Y, Z
directions.

CPU_VTT_SUS_SENSE
should be routed as 10mils
and 10mils spacing from any
adjacent signals in X, Y, Z
directions.

Place Capacitors for +0.9V_CPU_M_VREF_SUS < 1" from RS690.
+0.9V_CPU_M_VREF_SUS trace length < 6", trace width > 15mils and
20mils spacing from any adjacent signals in X, Y, Z directions.



DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket

Notes for the SODIMM locations:
DIMMA = Far = Bottom
DIMMB = Near = Top

Athlon 64 S1 Processor Socket

To SODIMM socket B (Near/Top)

To SODIMM socket A (Far/Bottom)

DDR B DQ[0..7]

DDR B DQ[8..15]

DDR B DQ[16..23]

DDR B DQ[24..31]

DDR B DQ[32..39]

DDR B DQ[40..47]

DDR B DQ[48..55]

DDR B DQ[56..63]

DDR B DQ[64..71]

DDR B DQ[72..79]

DDR B DQ[80..87]

DDR B DQ[88..95]

DDR B DQ[96..103]

DDR B DQ[104..111]

DDR B DQ[112..119]

DDR B DQ[120..127]

DDR B DQ[128..135]

DDR B DQ[136..143]

DDR B DQ[144..151]

DDR B DQ[152..159]

DDR B DQ[160..167]

DDR B DQ[168..175]

DDR B DQ[176..183]

DDR B DQ[184..191]

DDR B DQ[192..199]

DDR B DQ[200..207]

DDR B DQ[208..215]

DDR B DQ[216..223]

DDR B DQ[224..231]

DDR B DQ[232..239]

DDR B DQ[240..247]

DDR B DQ[248..255]

DDR B DQ[256..263]

DDR B DQ[264..271]

DDR B DQ[272..279]

DDR B DQ[280..287]

DDR B DQ[288..295]

DDR B DQ[296..303]

DDR B DQ[304..311]

DDR B DQ[312..319]

DDR B DQ[320..327]

DDR B DQ[328..335]

DDR B DQ[336..343]

DDR B DQ[344..351]

DDR B DQ[352..359]

DDR B DQ[360..367]

DDR B DQ[368..375]

DDR B DQ[376..383]

DDR B DQ[384..391]

DDR B DQ[392..399]

DDR B DQ[400..407]

DDR B DQ[408..415]

DDR B DQ[416..423]

DDR B DQ[424..431]

DDR B DQ[432..439]

DDR B DQ[440..447]

DDR B DQ[448..455]

DDR B DQ[456..463]

DDR B DQ[464..471]

DDR B DQ[472..479]

DDR B DQ[480..487]

DDR B DQ[488..495]

DDR B DQ[496..503]

DDR B DQ[504..511]

DDR B DQ[512..519]

DDR B DQ[520..527]

DDR B DQ[528..535]

DDR B DQ[536..543]

DDR B DQ[544..551]

DDR B DQ[552..559]

DDR B DQ[560..567]

DDR B DQ[568..575]

DDR B DQ[576..583]

DDR B DQ[584..591]

DDR B DQ[592..599]

DDR B DQ[600..607]

DDR B DQ[608..615]

DDR B DQ[616..623]

DDR B DQ[624..631]

DDR B DQ[632..639]

DDR B DQ[640..647]

DDR B DQ[648..655]

DDR B DQ[656..663]

DDR B DQ[664..671]

DDR B DQ[672..679]

DDR B DQ[680..687]

DDR B DQ[688..695]

DDR B DQ[696..703]

DDR B DQ[704..711]

DDR B DQ[712..719]

DDR B DQ[720..727]

DDR B DQ[728..735]

DDR B DQ[736..743]

DDR B DQ[744..751]

DDR B DQ[752..759]

DDR B DQ[760..767]

DDR B DQ[768..775]

DDR B DQ[776..783]

DDR B DQ[784..791]

DDR B DQ[792..799]

DDR B DQ[800..807]

DDR B DQ[808..815]

DDR B DQ[816..823]

DDR B DQ[824..831]

DDR B DQ[832..839]

DDR B DQ[840..847]

DDR B DQ[848..855]

DDR B DQ[856..863]

DDR B DQ[864..871]

DDR B DQ[872..879]

DDR B DQ[880..887]

DDR B DQ[888..895]

DDR B DQ[896..903]

DDR B DQ[904..911]

DDR B DQ[912..919]

DDR B DQ[920..927]

DDR B DQ[928..935]

DDR B DQ[936..943]

DDR B DQ[944..951]

DDR B DQ[952..959]

DDR B DQ[960..967]

DDR B DQ[968..975]

DDR B DQ[976..983]

DDR B DQ[984..991]

DDR B DQ[992..999]

DDR B DQ[1000..1007]

DDR B DQ[1008..1015]

DDR B DQ[1016..1023]

DDR B DQ[1024..1031]

DDR B DQ[1032..1039]

DDR B DQ[1040..1047]

DDR B DQ[1048..1055]

DDR B DQ[1056..1063]

DDR B DQ[1064..1071]

DDR B DQ[1072..1079]

DDR B DQ[1080..1087]

DDR B DQ[1088..1095]

DDR B DQ[1096..1103]

DDR B DQ[1104..1111]

DDR B DQ[1112..1119]

DDR B DQ[1120..1127]

DDR B DQ[1128..1135]

DDR B DQ[1136..1143]

DDR B DQ[1144..1151]

DDR B DQ[1152..1159]

DDR B DQ[1160..1167]

DDR B DQ[1168..1175]

DDR B DQ[1176..1183]

DDR B DQ[1184..1191]

DDR B DQ[1192..1199]

DDR B DQ[1200..1207]

DDR B DQ[1208..1215]

DDR B DQ[1216..1223]

DDR B DQ[1224..1231]

DDR B DQ[1232..1239]

DDR B DQ[1240..1247]

DDR B DQ[1248..1255]

DDR B DQ[1256..1263]

DDR B DQ[1264..1271]

DDR B DQ[1272..1279]

DDR B DQ[1280..1287]

DDR B DQ[1288..1295]

DDR B DQ[1296..1303]

DDR B DQ[1304..1311]

DDR B DQ[1312..1319]

DDR B DQ[1320..1327]

DDR B DQ[1328..1335]

DDR B DQ[1336..1343]

DDR B DQ[1344..1351]

DDR B DQ[1352..1359]

DDR B DQ[1360..1367]

DDR B DQ[1368..1375]

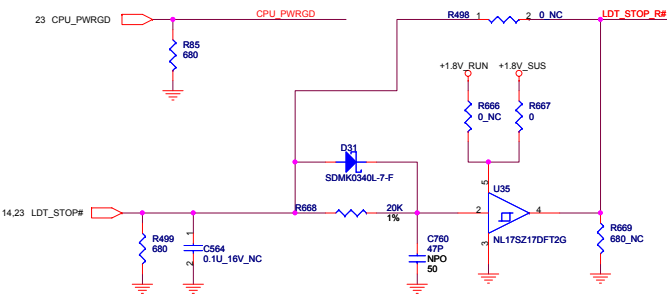
DDR B DQ[1376..1383]

DDR B DQ[1384..1391]

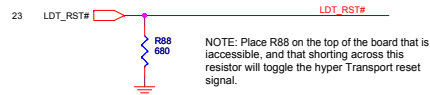
DDR B DQ[1392..1399]

<

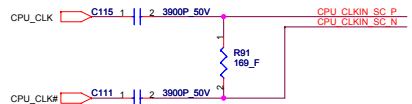
SB600 ONLY



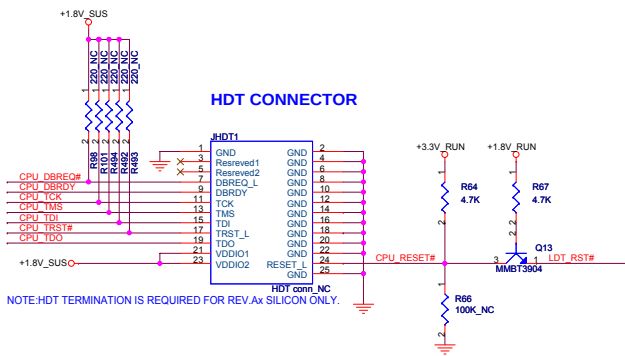
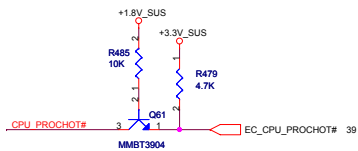
NOTE: R499 and C564 close to JCPU pin F10



NOTE: Place R88 on the top of the board that is accessible, and that shorting across this resistor will toggle the hyper Transport reset signal.



- 1.KEEP TRACE TO RESISTOR LESS THAN 600MILS FROM CPU PIN AND TRACE TO AC CAPS LESS THAN 1250MILS.
2. CPUCLK and CPUCLK# mismatch < 35 mils.



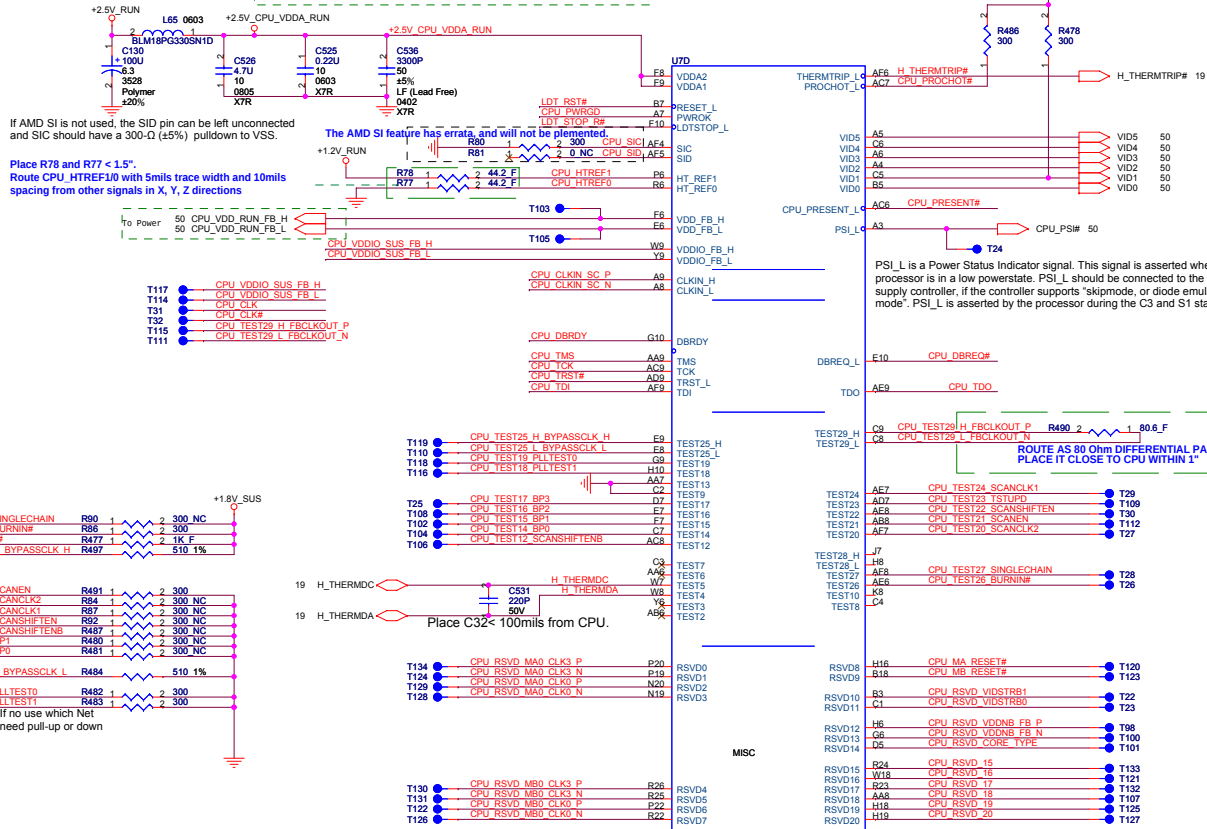
NOTE:HDT TERMINATION IS REQUIRED FOR REV.Ax SILICON ONLY.

LAYOUT: ROUTE VDDA TRACE APPROX.

50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

This trace should be kept at least 20 mils away from all other signals.

+2.5V CPU VDDA RUN



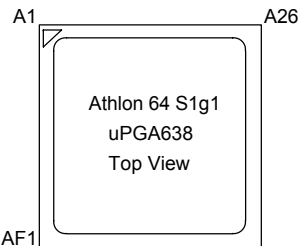
AMD NPT S1 SOCKET
Processor Socket

Title
ATHLON64 CTRL. & DEBUG

Size	Document Number
	MGD

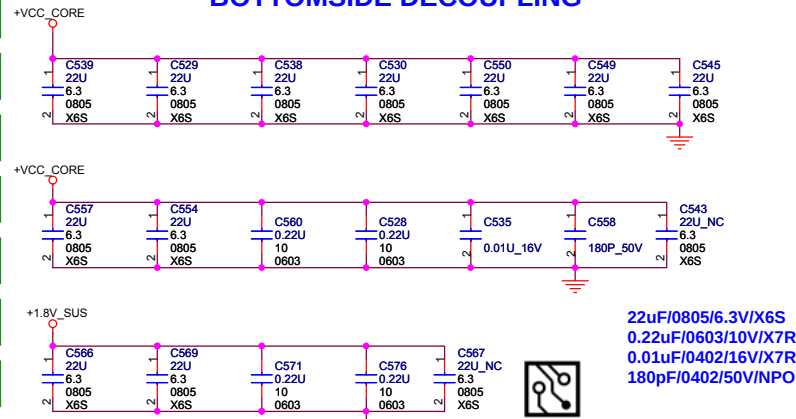
Date: Thursday, March 01, 2007 Sheet 10 of 89

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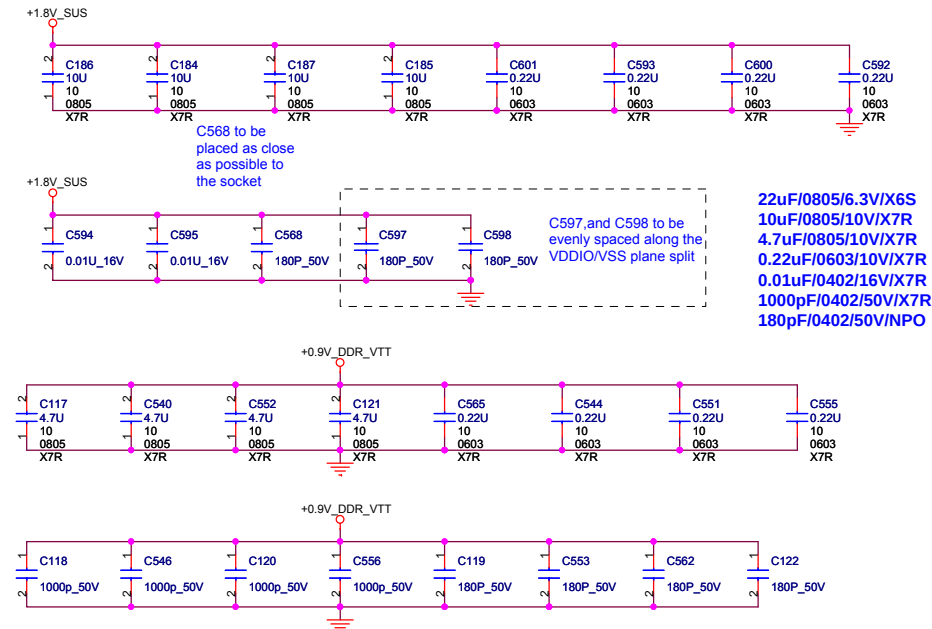


PROCESSOR POWER AND GROUND

BOTTOMSIDE DECOUPLING

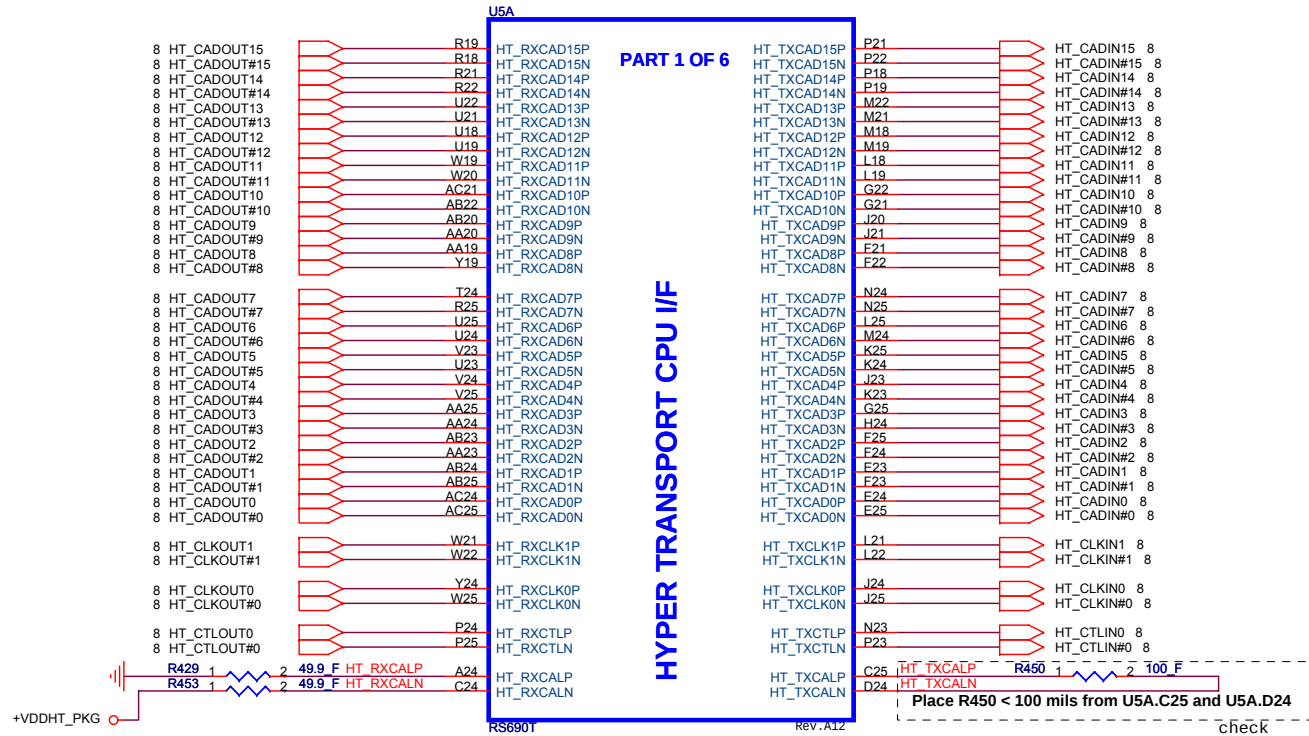


DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



Title ATHLON64 PWR & GND		
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Change Part Number



Title
RS690T-HT LINK0 I/F

Size
Document Number
MGD

Rev
2A

Date: Thursday, March 01, 2007

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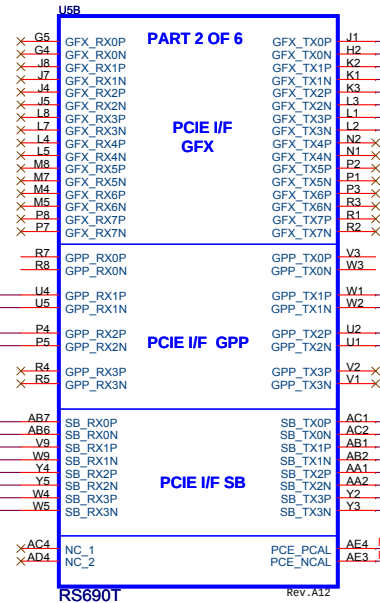
WLAN <-----

GIGA LAN <-----

35 PCIE_NBRX_WLANTX_P1
35 PCIE_NBRX_WLANTX_N1

30 PCIE_NBRX_LOMTX_P2
30 PCIE_NBRX_LOMTX_N2

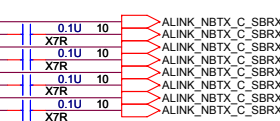
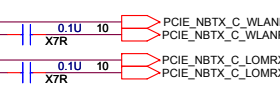
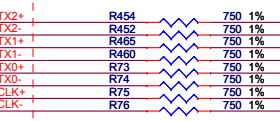
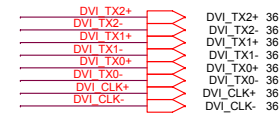
23 ALINK_NBRX_SBTX_P0
23 ALINK_NBRX_SBTX_N0
23 ALINK_NBRX_SBTX_P1
23 ALINK_NBRX_SBTX_N1
23 ALINK_NBRX_SBTX_P2
23 ALINK_NBRX_SBTX_N2
23 ALINK_NBRX_SBTX_P3
23 ALINK_NBRX_SBTX_N3

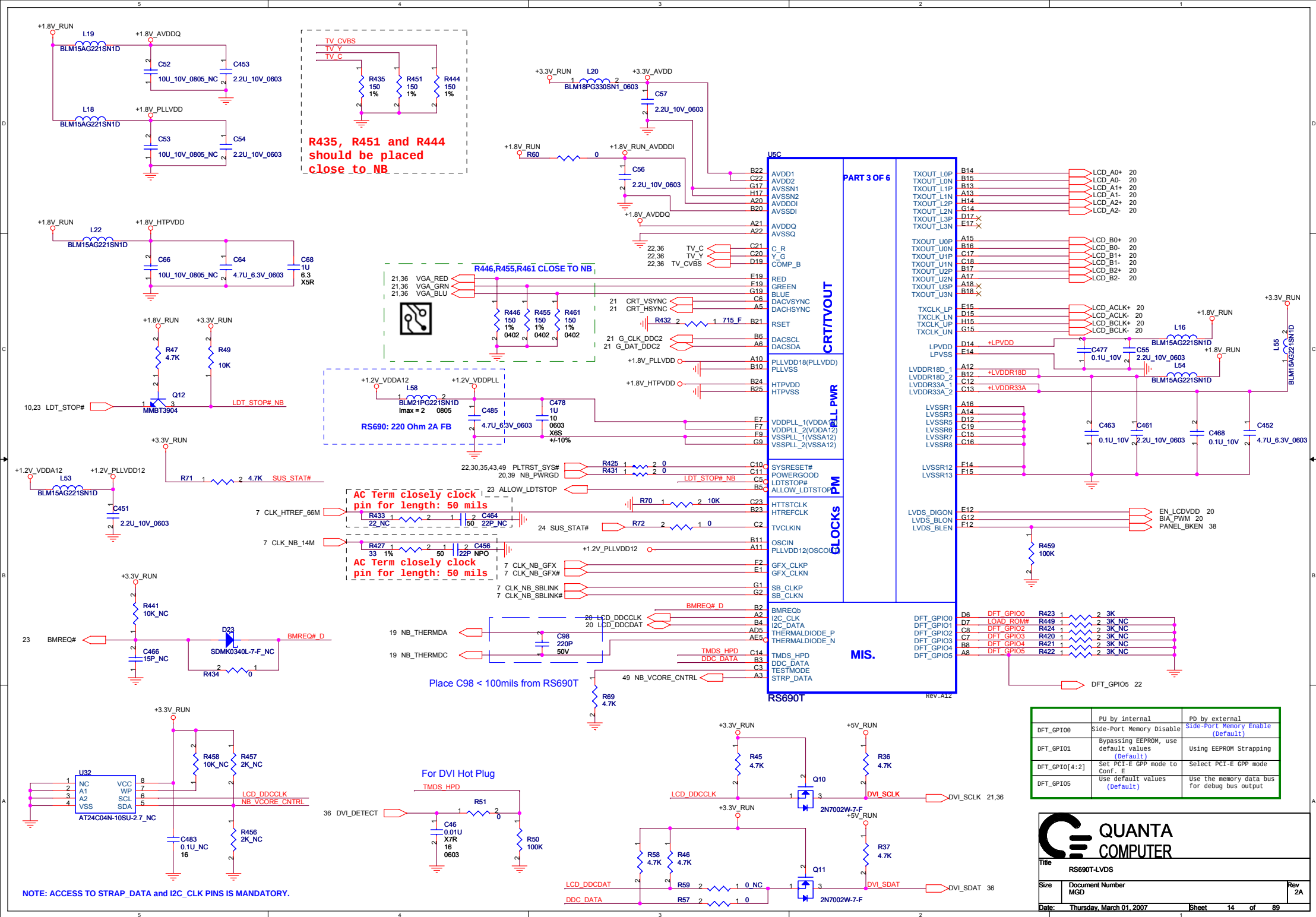


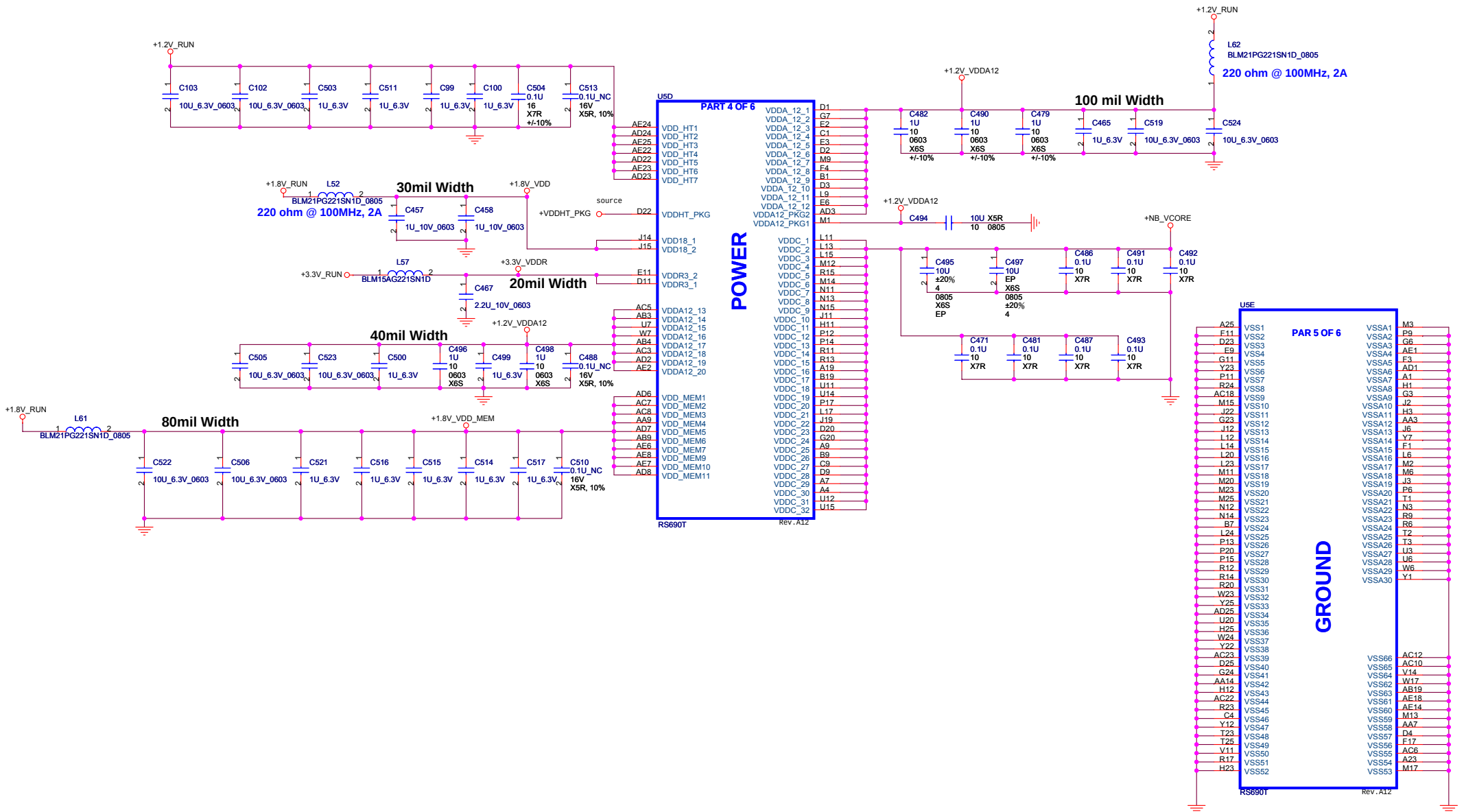
Place near RS690T

No placement limitation,
minimum stub

Layout Note :750 ohm
resistors
are placed at the same
via as
the series capacitors

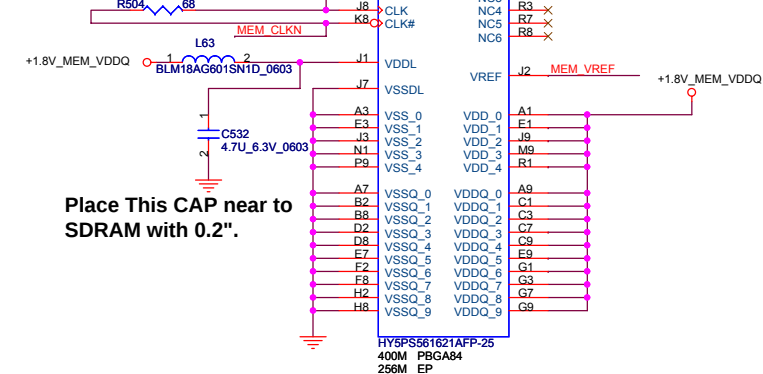






Bit Swap

Place R504 to close to U5.

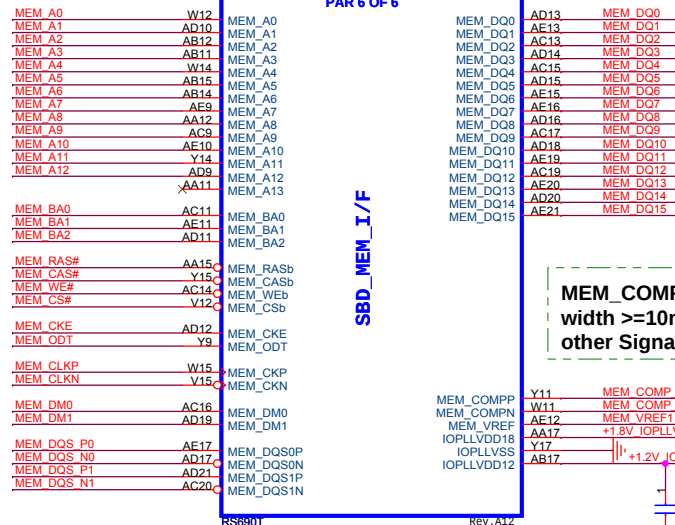


Place This CAP near to SDRAM with 0.2".

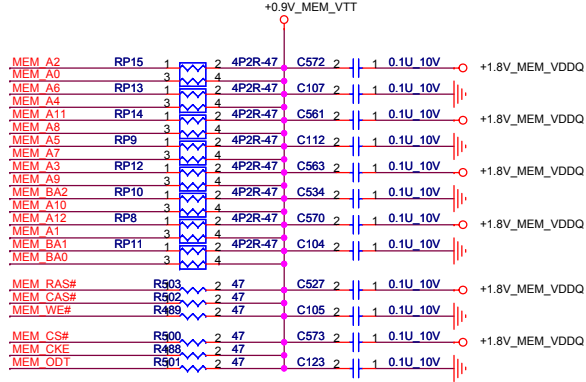
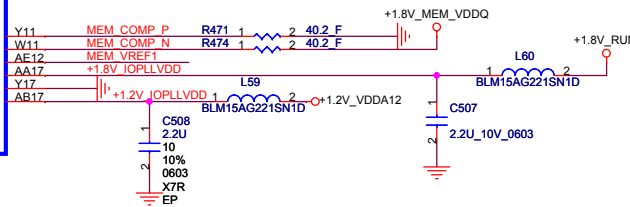
256-Mbit DDR2 16Mbit*16(4bank)

SBD_MEM_I/F

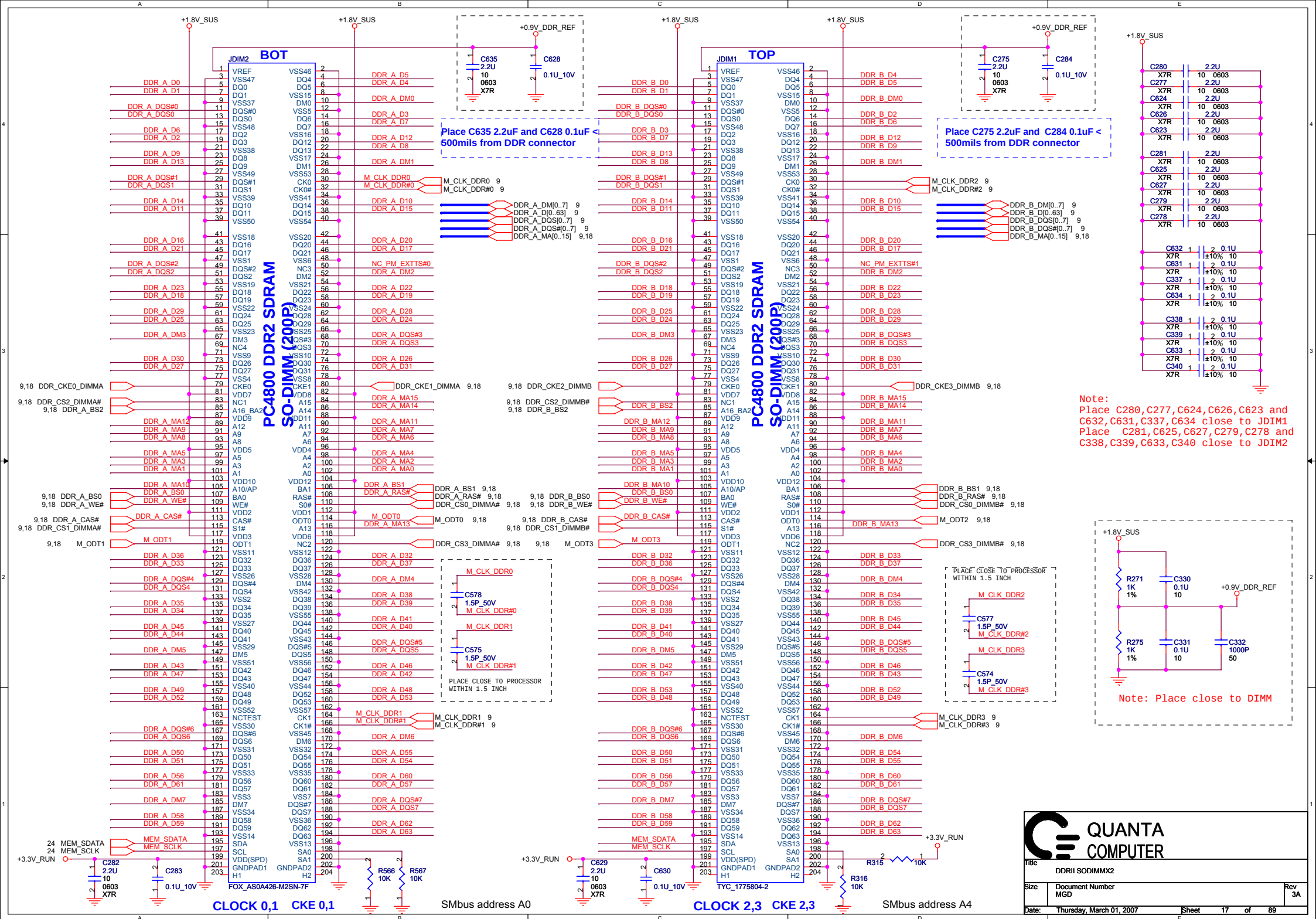
PAR 6 OF 6



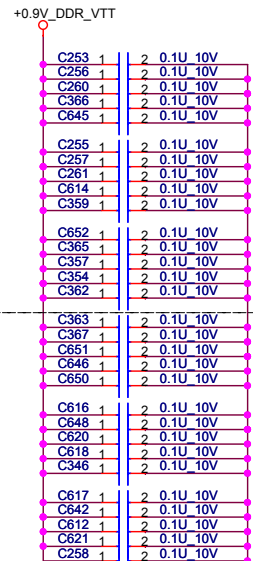
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions



Local Frame Buffer(64MB) DDRII Power



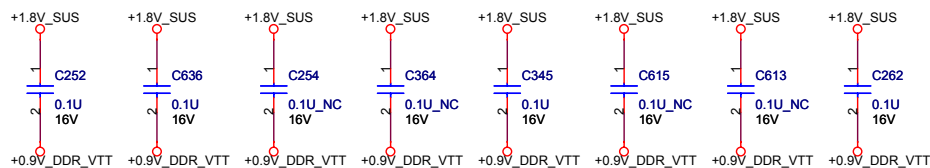
Note:
please close to DIMMA



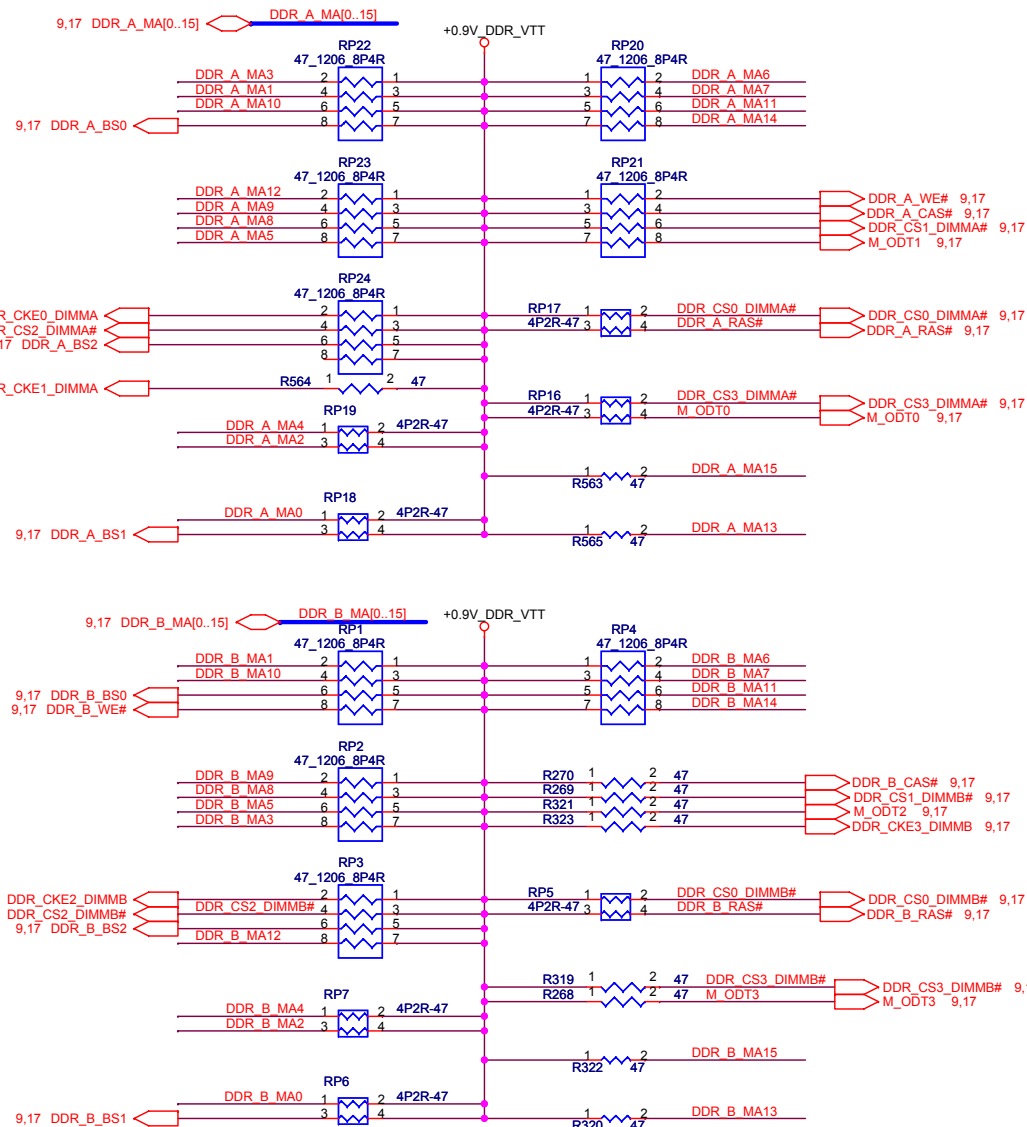
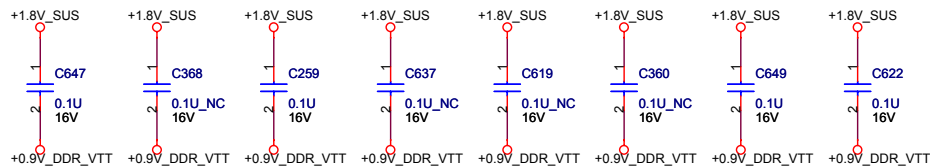
Note:
please close to DIMMB

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT

Note: Reserve stitching function for JDIM1.



Note: Reserve stitching function for JDIM2.





QUANTA

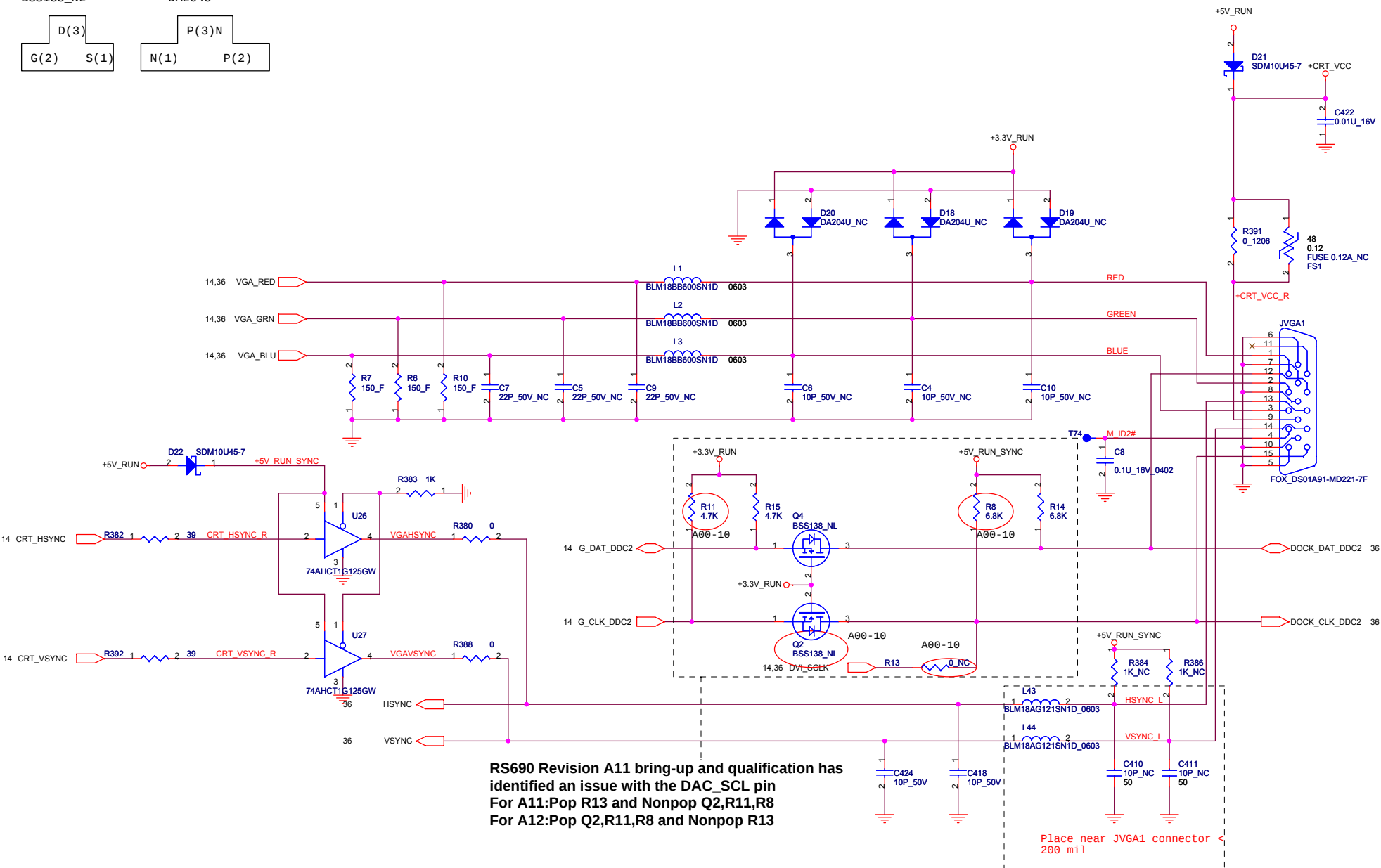
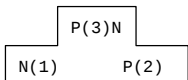
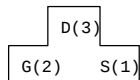
COMPUTER

Title DDRII TERMINATION		
Size MGD	Document Number	Rev 2A
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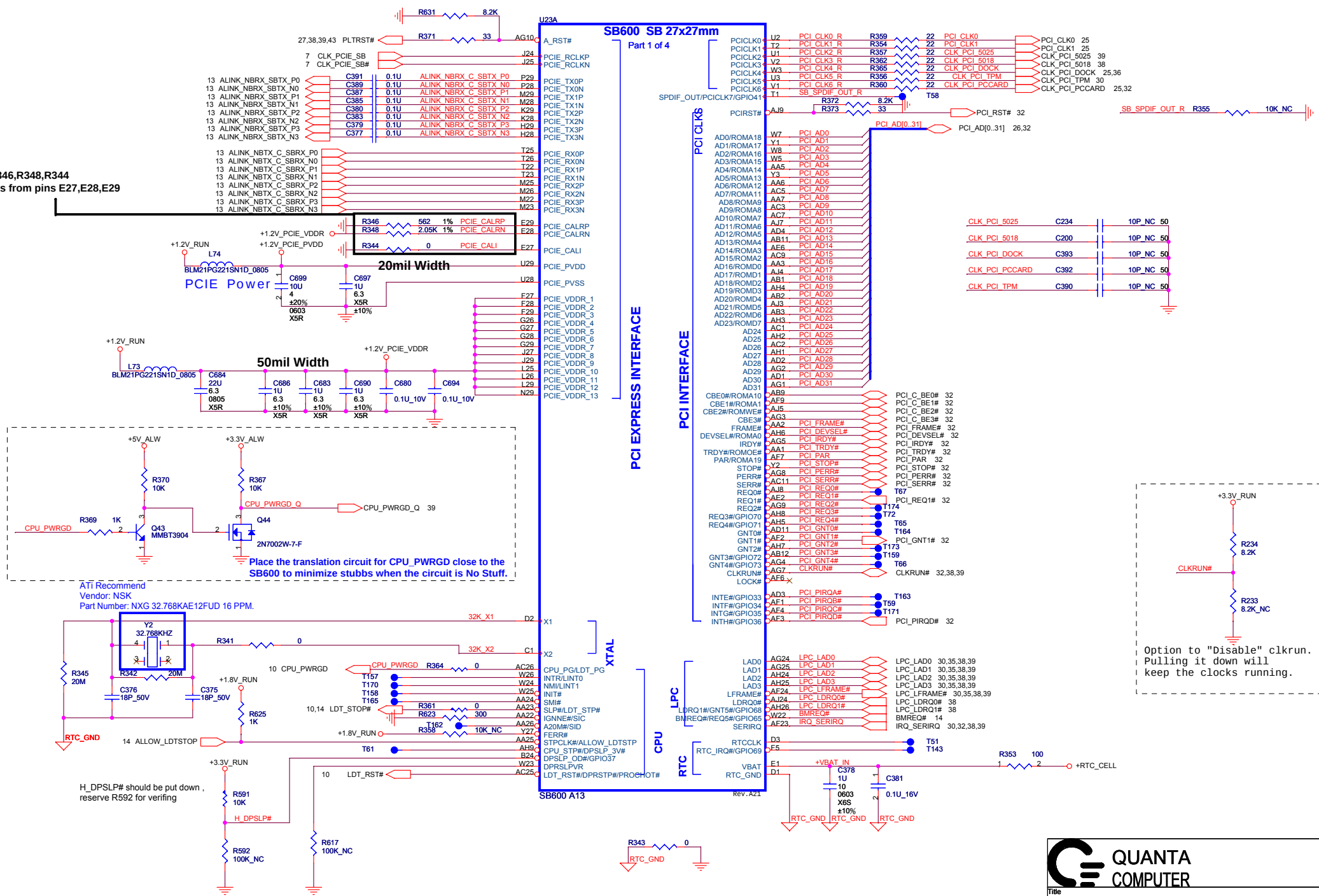
Symbol:
BSS138_NL

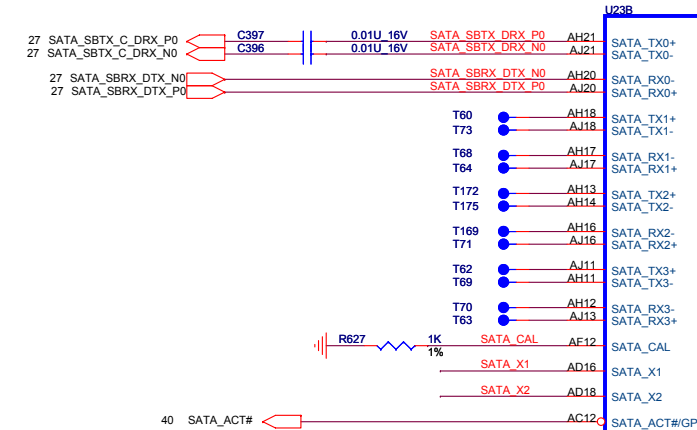
Symbol:
DA204U



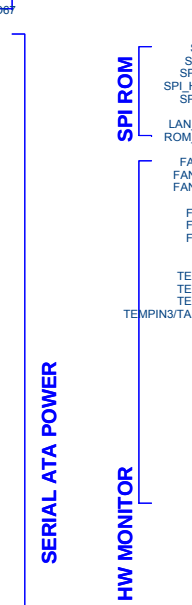
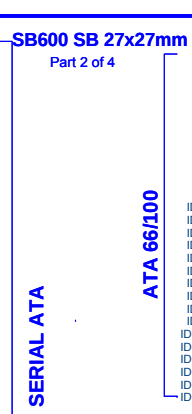
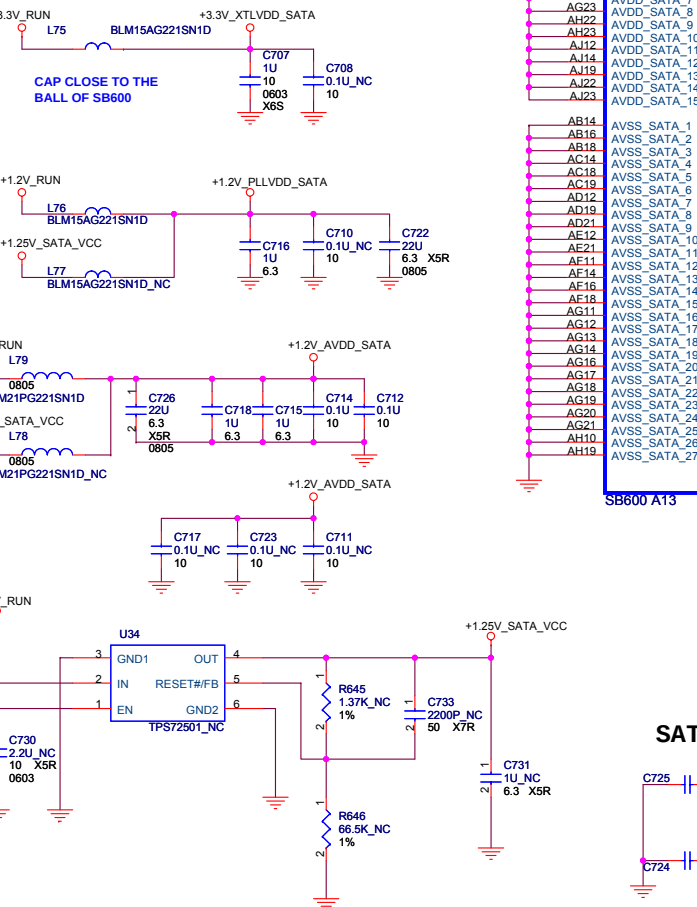
Title CRT CONN		
Size MGD	Document Number	Rev 3A
Date: Thursday, March 01, 2007	Sheet 21	of 89

Place R346,R348,R344
< 100mils from pins E27,E28,E29

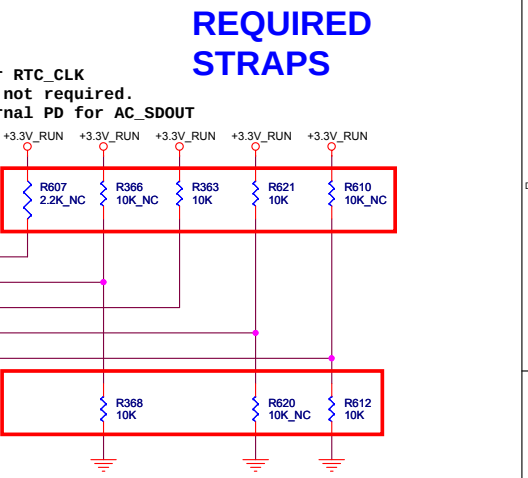
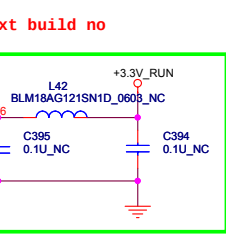
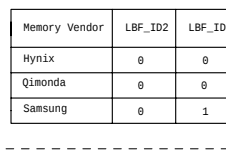
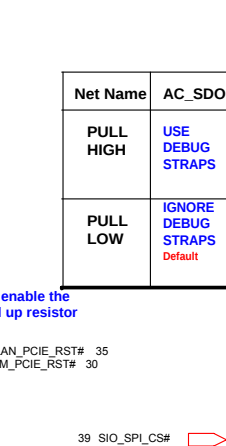
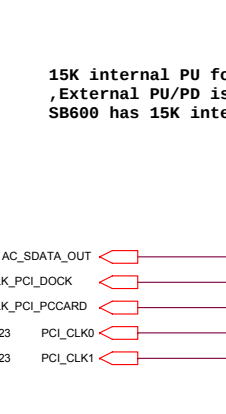
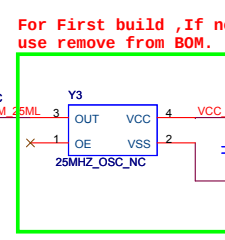
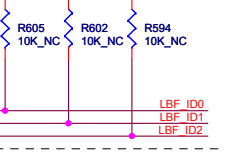
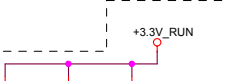
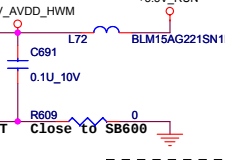
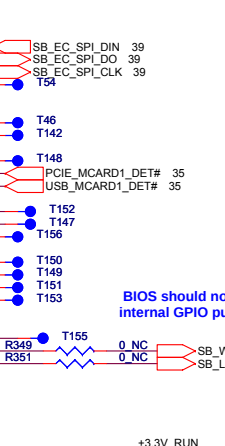
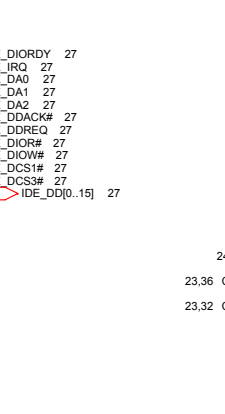
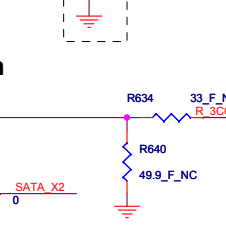
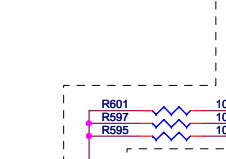
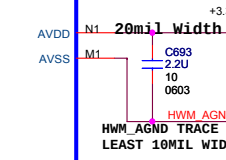
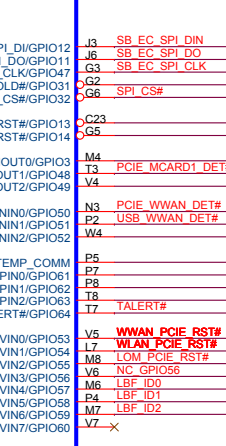
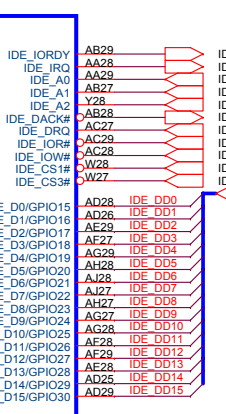
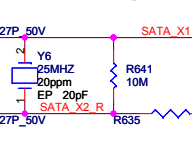




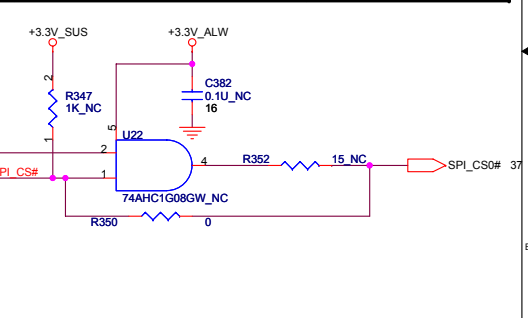
SATA Power



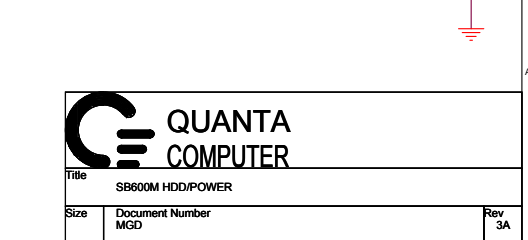
SATA clock Option



Net Name	AC_SDOUT	CLK_PCI_DOCK	CLK_PCI_PCCARD	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8	H, H = PCI ROM H, L = SPI ROM	Default
PULL LOW	IGNORE DEBUG STRAPS Default	USE EXT. 48MHZ	CPU IF=P4	L, H = LPC ROM L, L = FWH ROM	



Memory Vendor	LBF_ID2	LBF_ID1	LBF_ID0
Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0



QUANTA
COMPUTER

Title: SB600M HDD/POWER

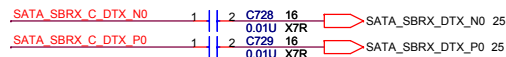
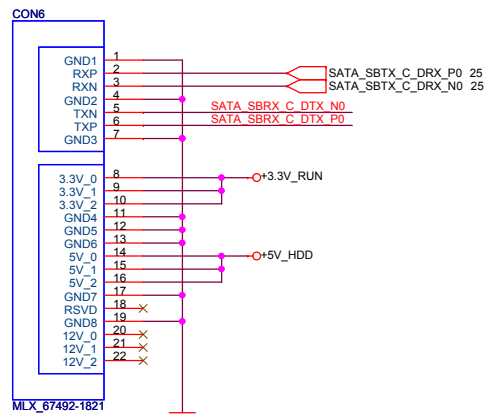
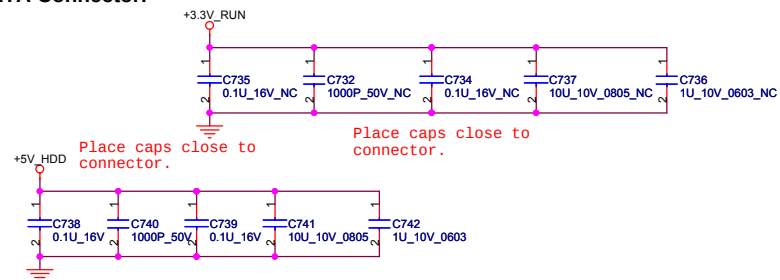
Size: Document Number MGD

Date: Thursday, March 01, 2007

Sheet: 25 of 89

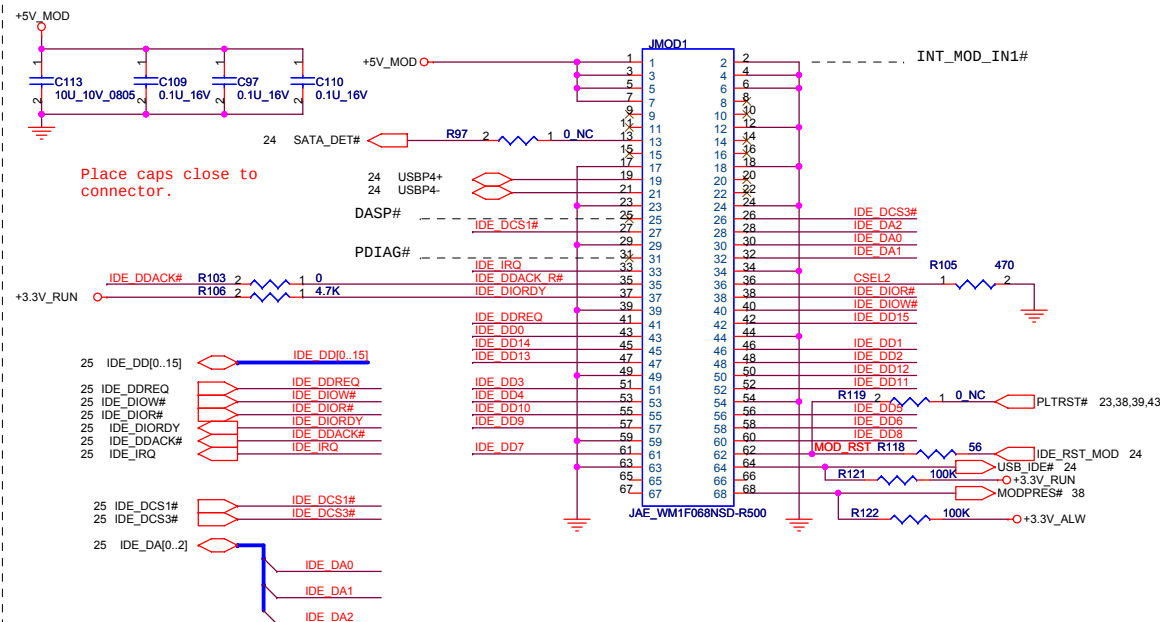
Rev: 3A

SATA Connector.

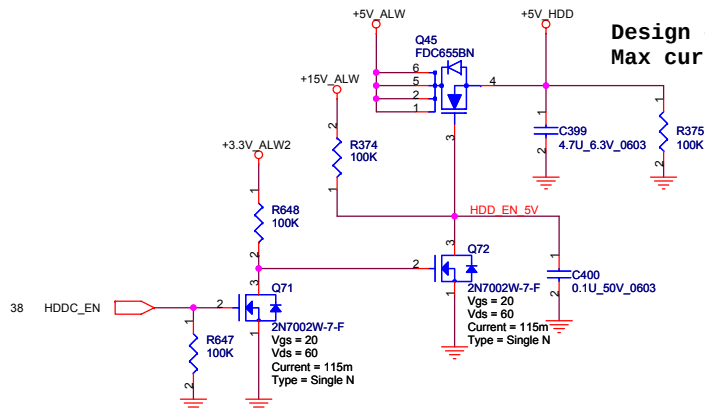


NOTE:
C728,C729 Close to CON6

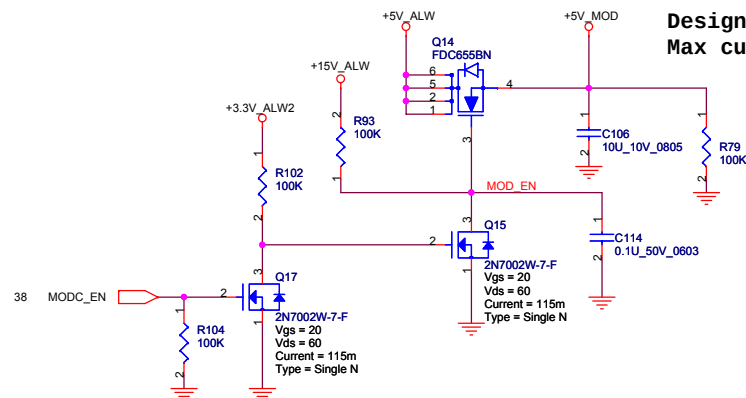
ODD Connector.



Design current: 700mA
Max current: 1000mA



Design current: 1050mA
Max current: 1500mA

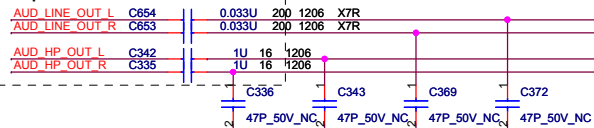


Symbol:
2N7002W-7-F
D(3)
G(2) S(1)



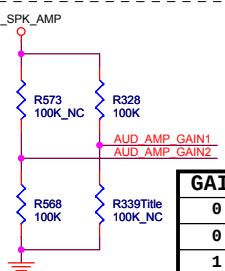
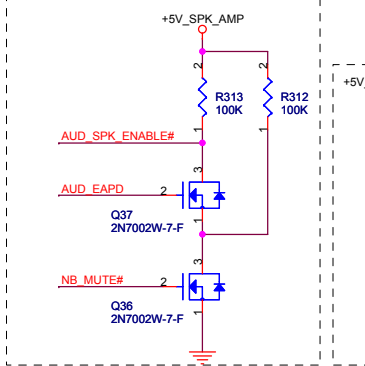
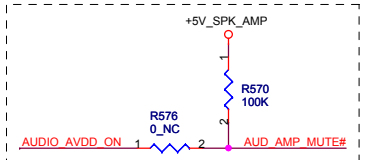
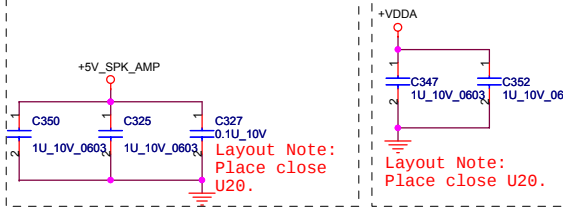
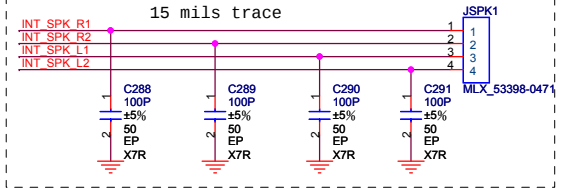
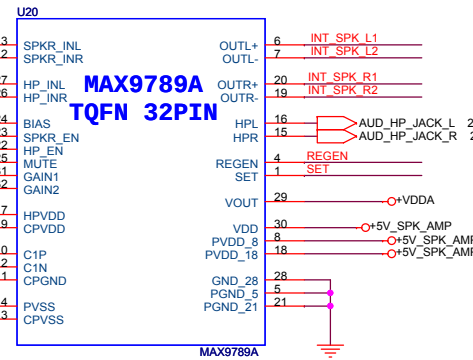
Title SATA (HDD&CD_ROM)		
Size MGD	Document Number	Rev 2A
Date: Thursday, March 01, 2007	Sheet 27	of 89

Package 1206 for THD+N performance for Vista Logo requirements.

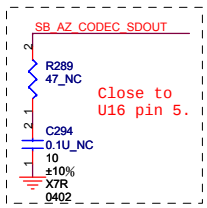
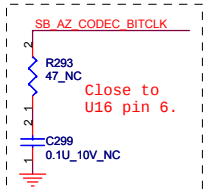
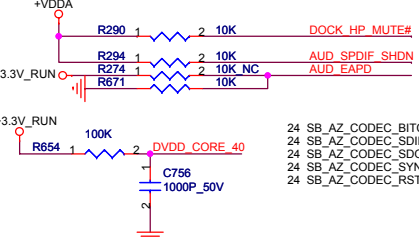
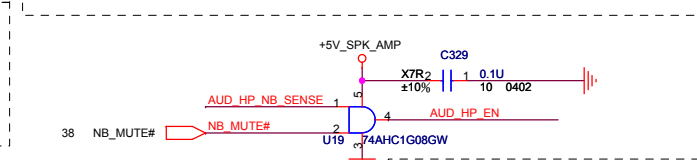
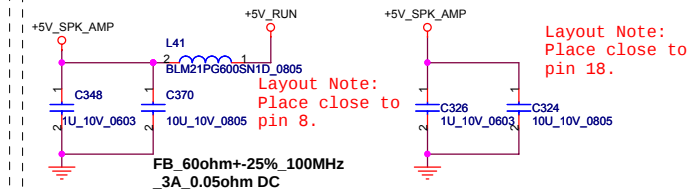
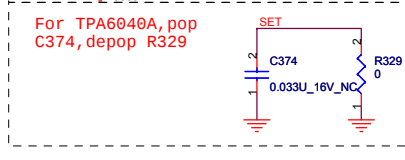
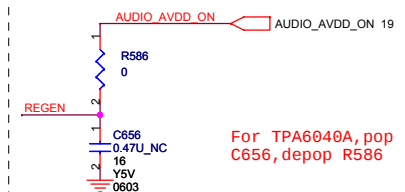


INTERNAL SPEAKER AMP

MAX9789A
TQFN 32PIN

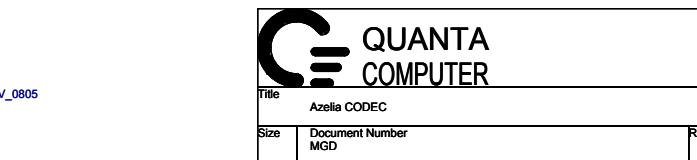
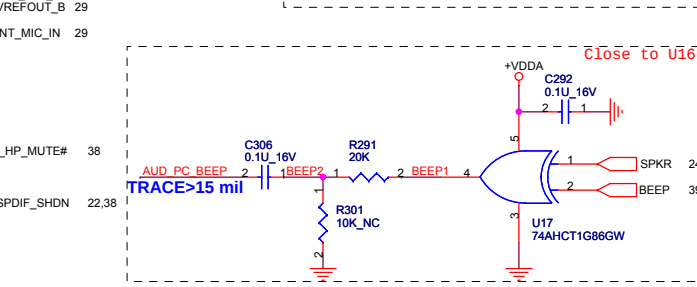
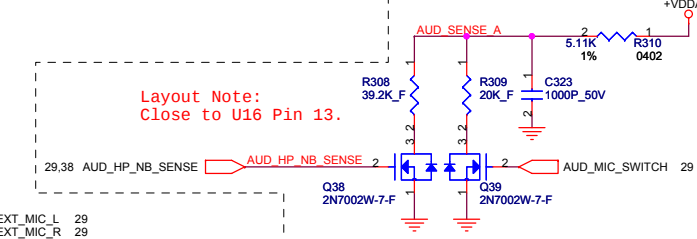
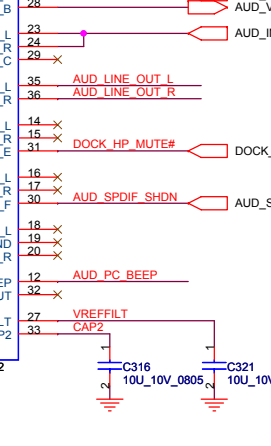
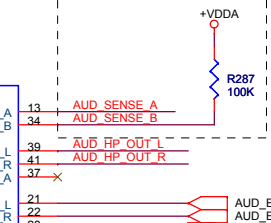
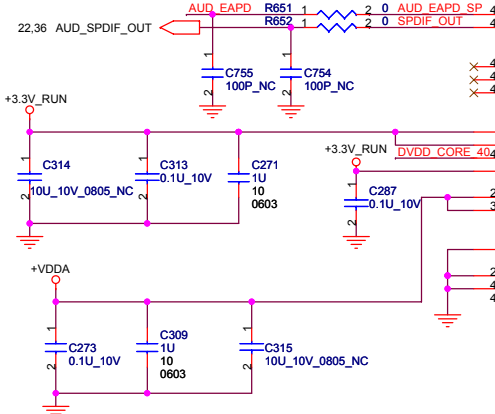
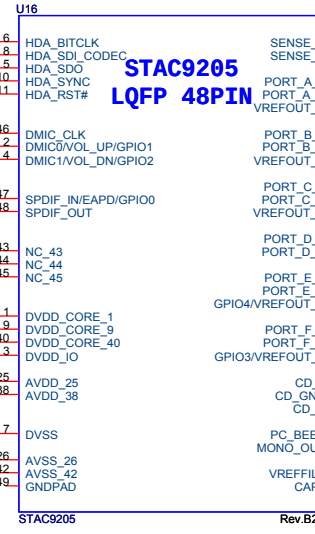


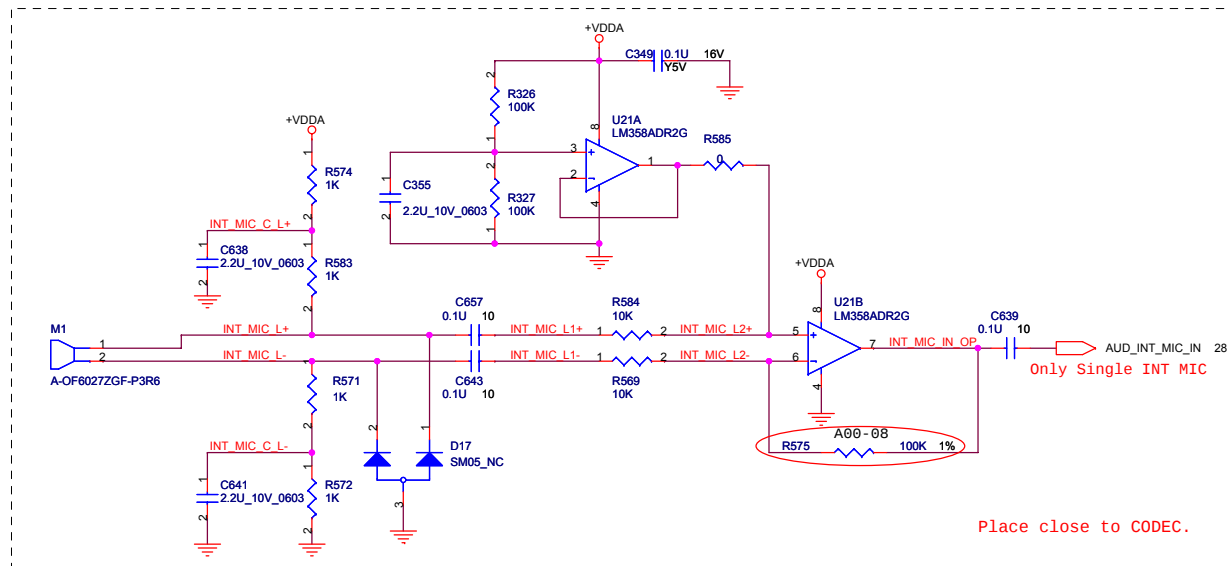
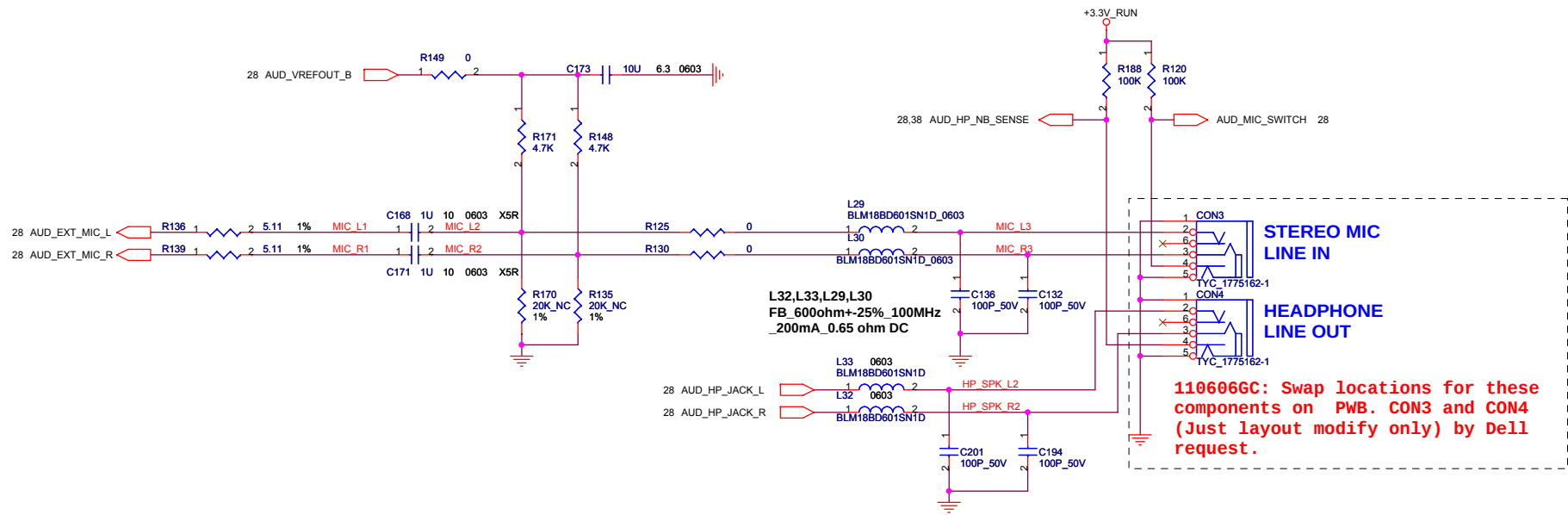
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB Default
1	1	21.6dB

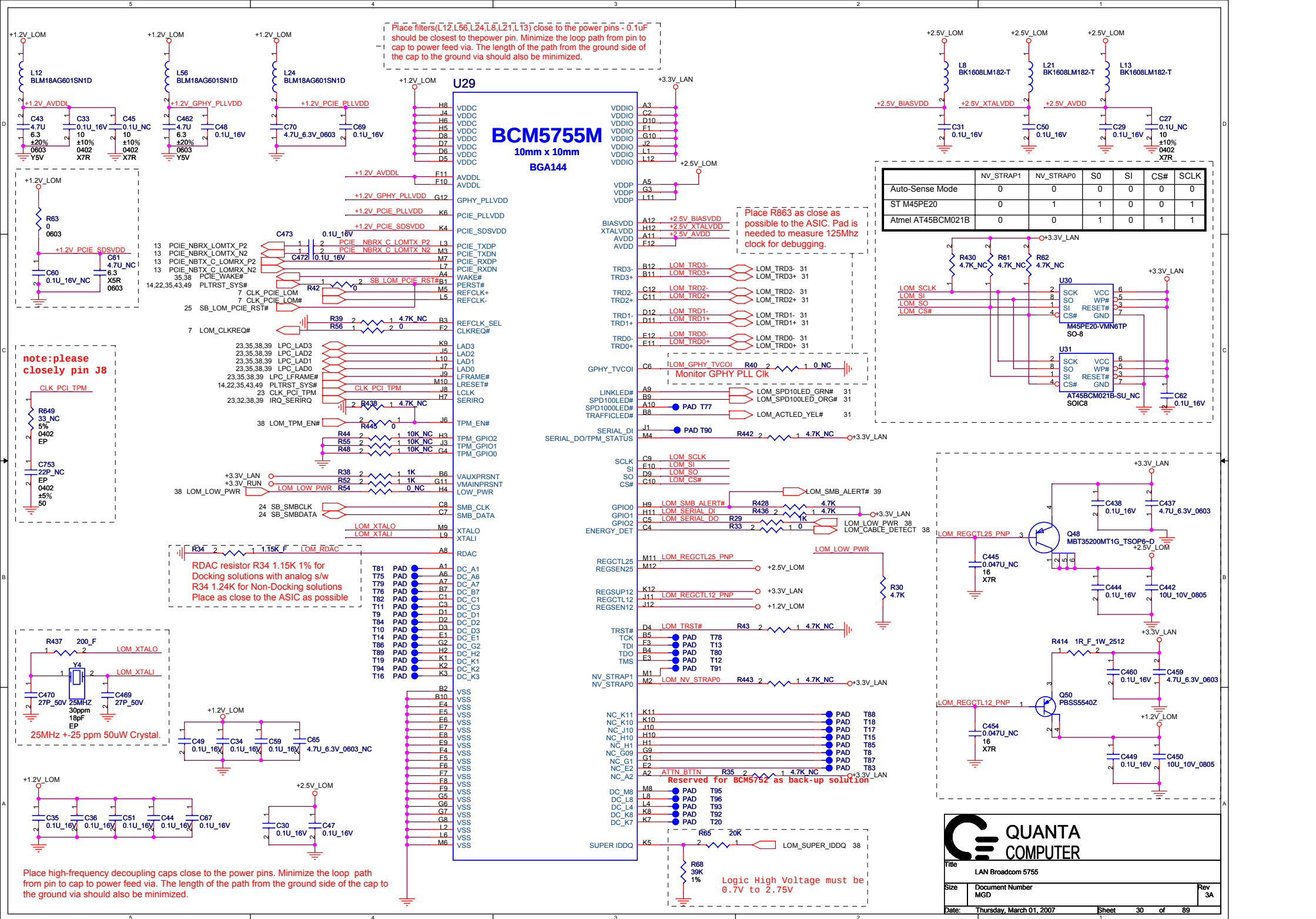


AZALIA (HD) CODEC

STAC9205
LQFP 48PIN

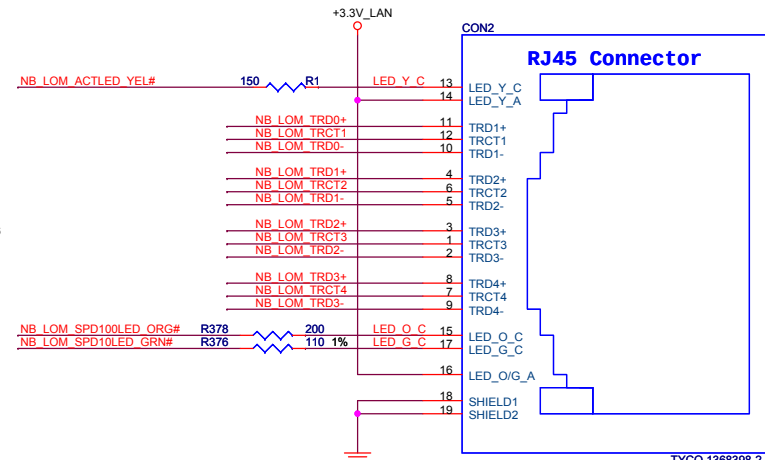
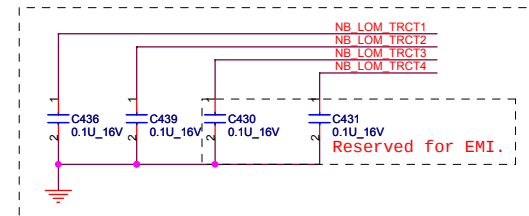
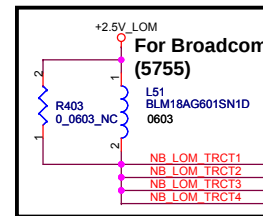
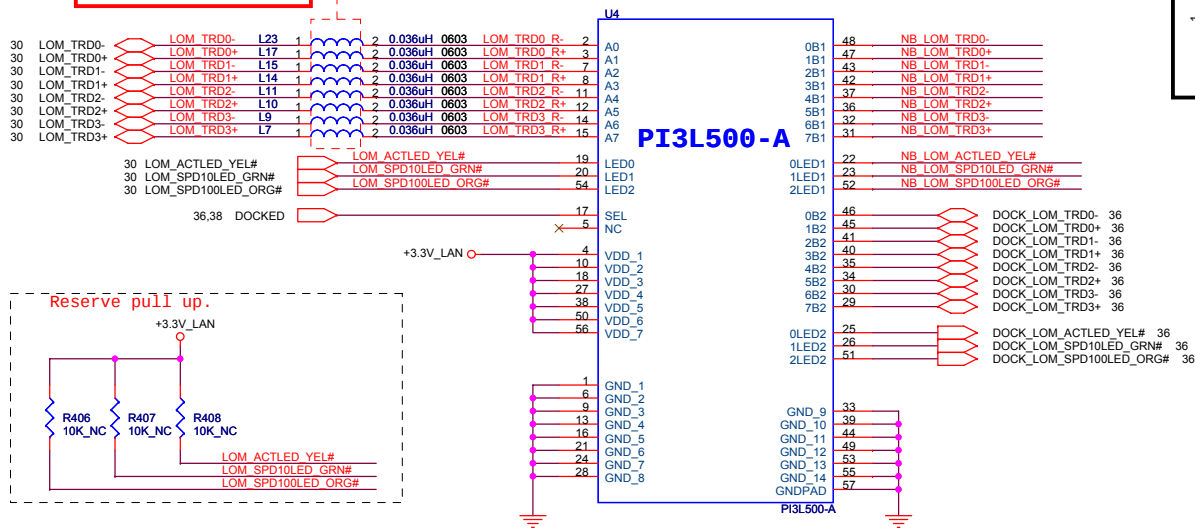




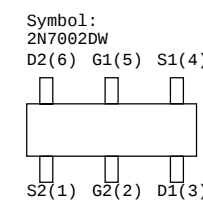
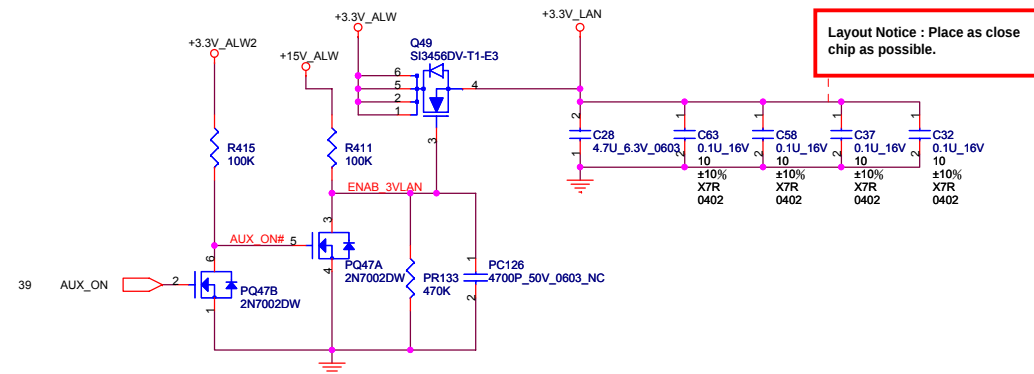
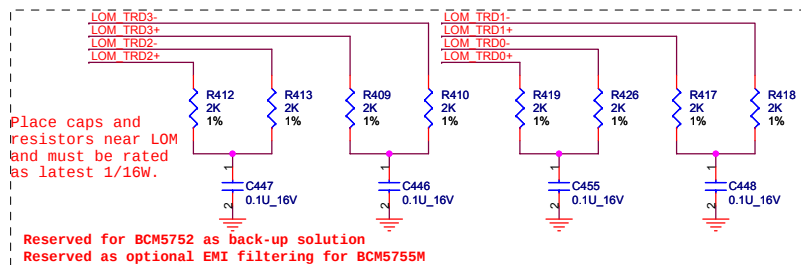


TRANSFORM+RJ45

Layout Notice : Place bead as close PI3L500 as possible



Design Current: 640.15 mA,
 Max Current: 914.5 mA.

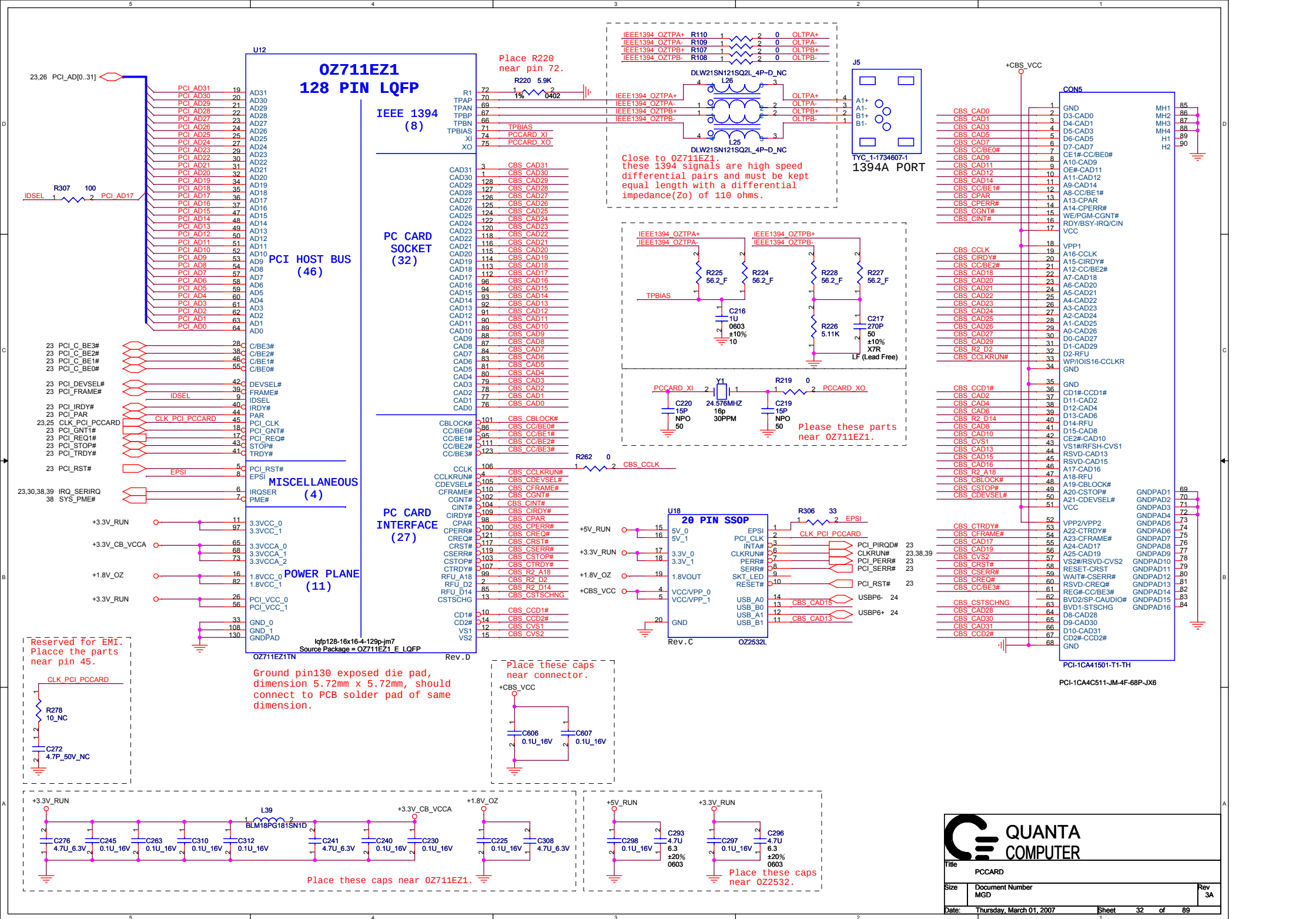


QUANTA COMPUTER

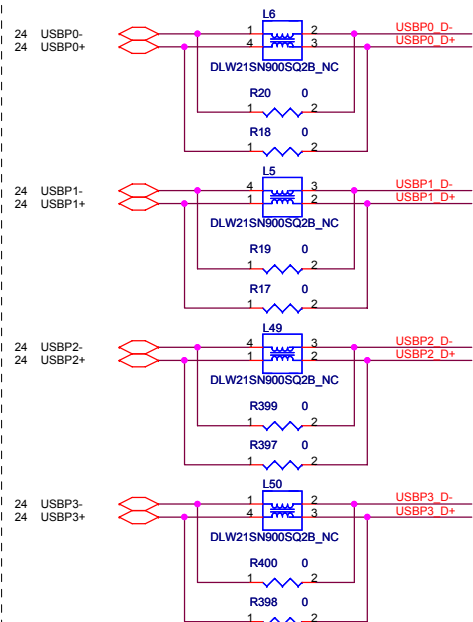
Title: LAN SWITCH

Size: Document Number MGD Rev 3A

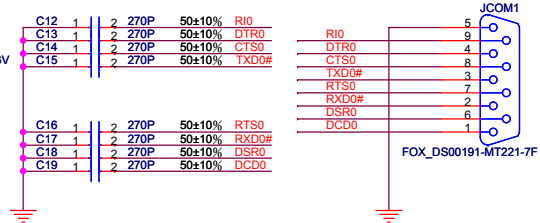
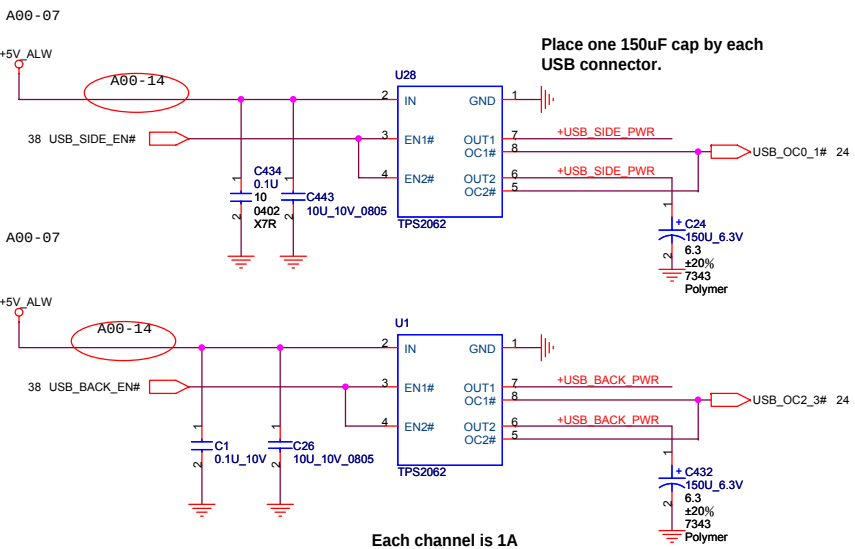
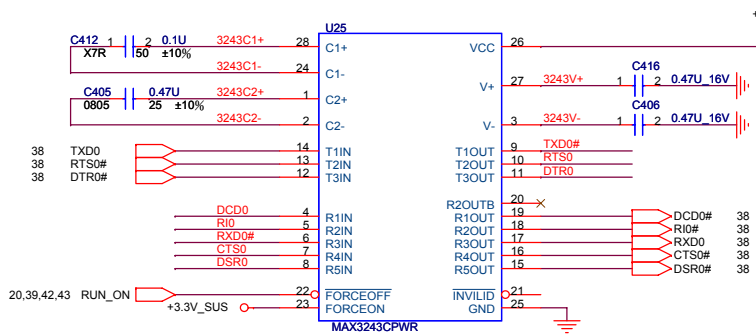
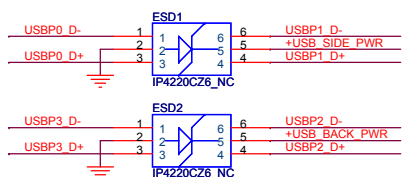
Date: Thursday, March 01, 2007 Sheet 31 of 89



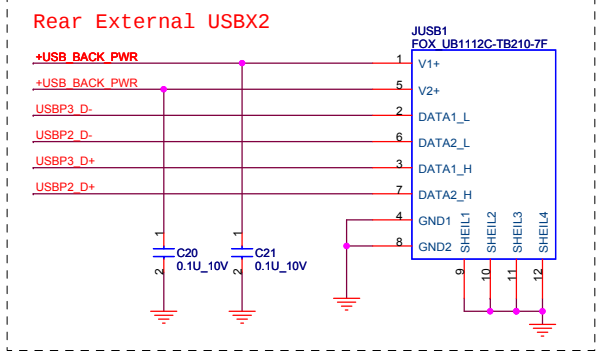
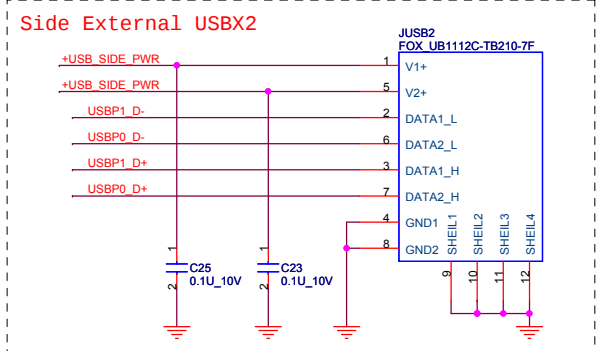
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

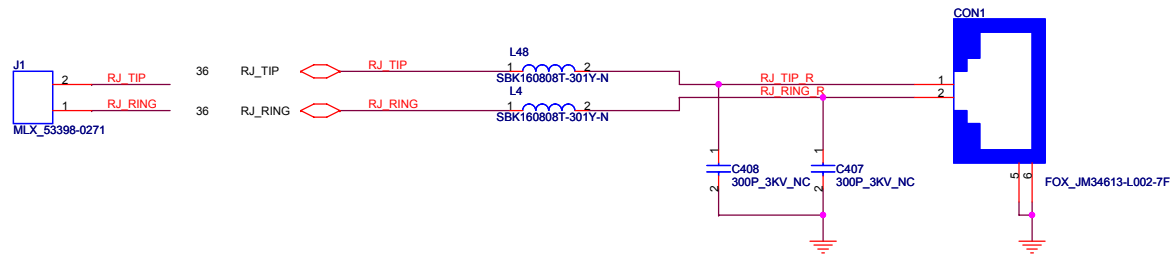


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

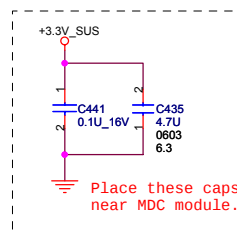
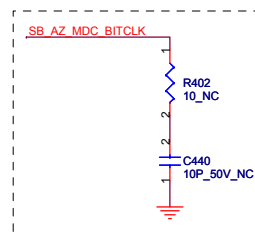
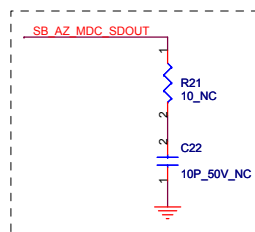
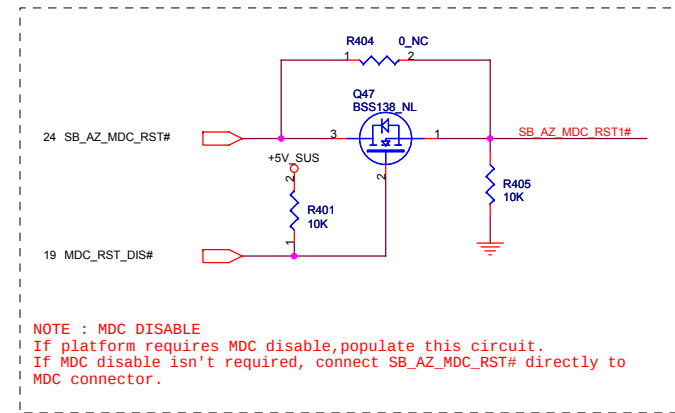
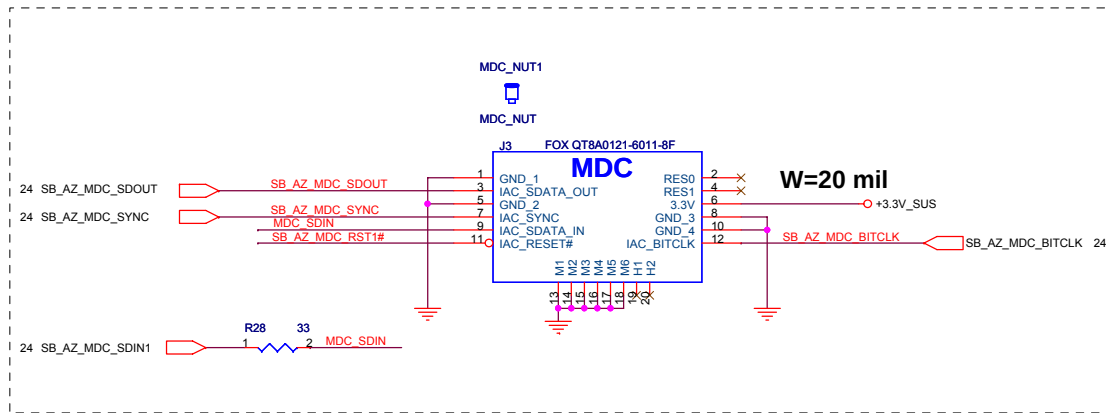
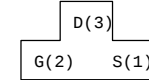


Place these beads close to JCOM1 as soon as possible
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out

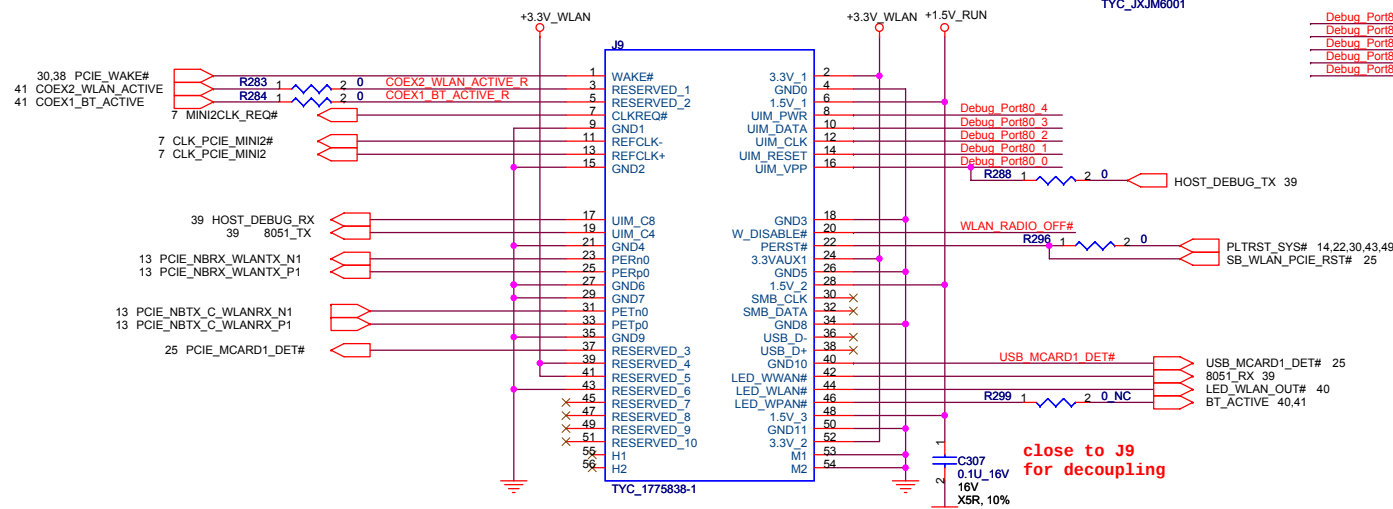
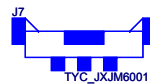




Symbol:
BSS138_NL



MiniCard WLAN connector

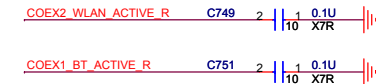


Reserve for Port 80 Debug I/F

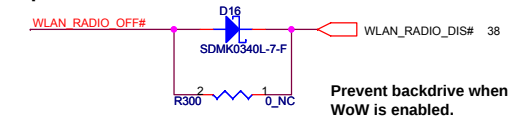
Debug_Port80_4	R302	1	2	0	NC	LPC_LFRAME#	23,30,38,39
Debug_Port80_3	R303	1	2	0	NC	LPC_LAD3	23,30,38,39
Debug_Port80_2	R304	1	2	0	NC	LPC_LAD2	23,30,38,39
Debug_Port80_1	R305	1	2	0	NC	LPC_LAD1	23,30,38,39
Debug_Port80_0	R292	1	2	0	NC	LPC_LAD0	23,30,38,39

EMI solution

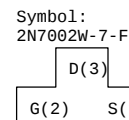
please as close as possible to the WLAN connector (J9.3 & J9.5)



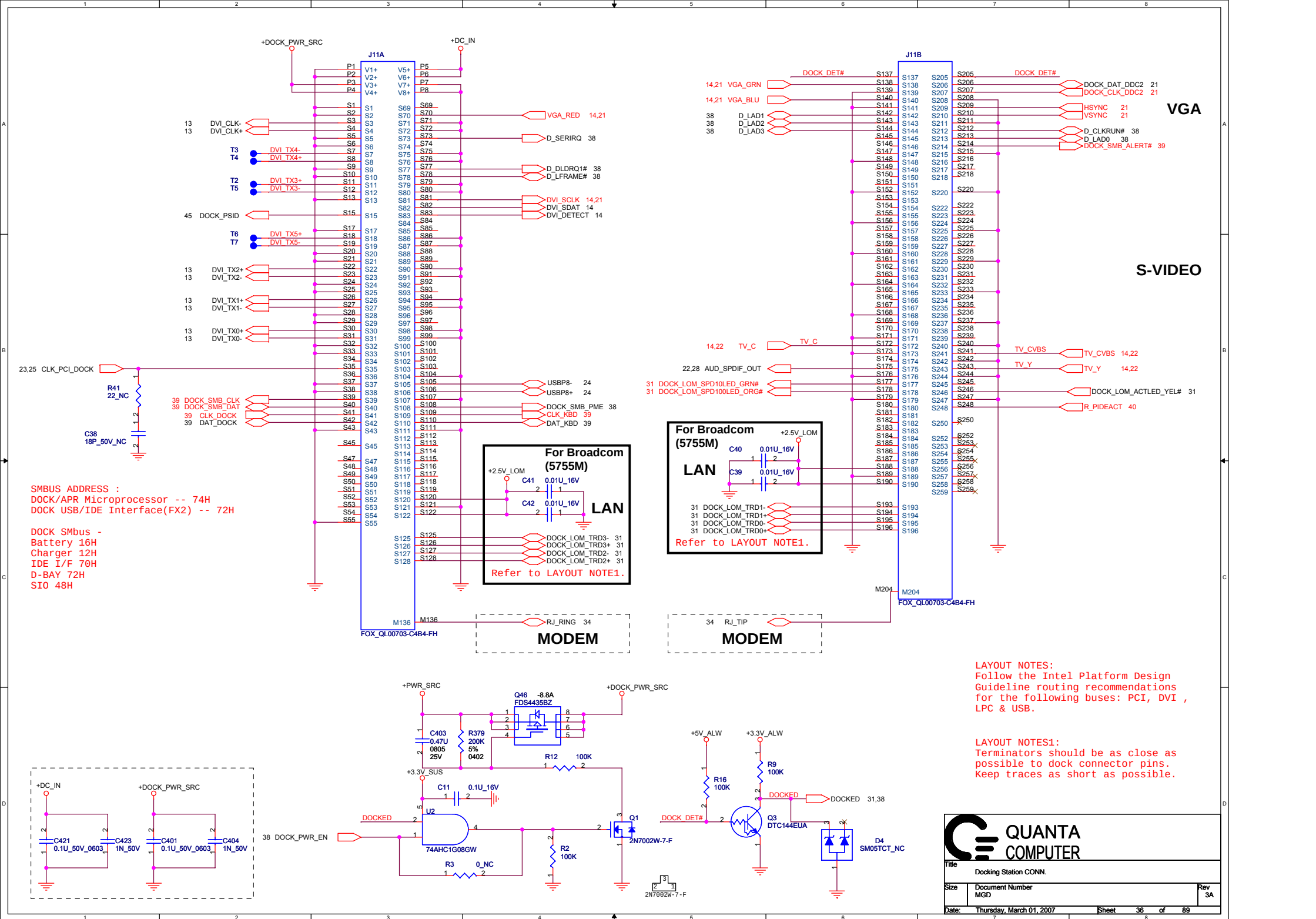
Support for WoW



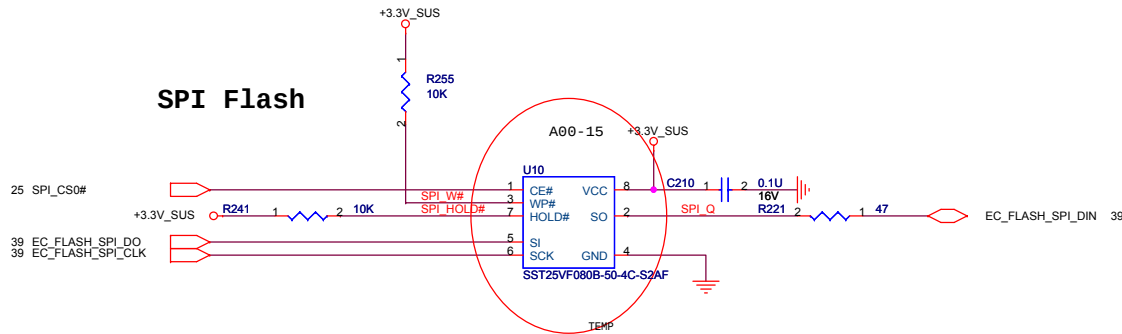
Place caps close to connector.



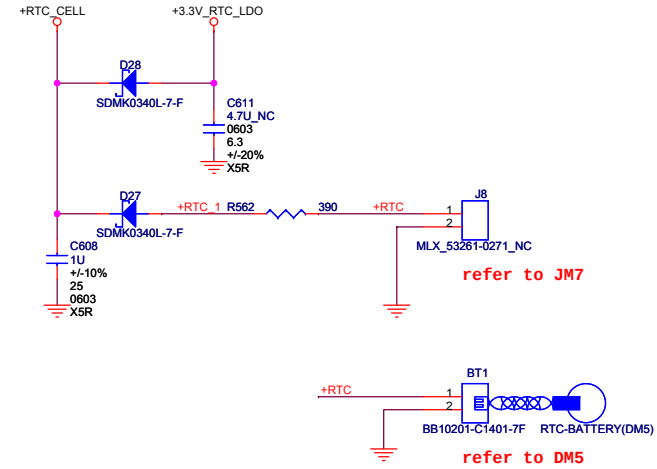
QUANTA COMPUTER	
Title: MINI-PCI	
Size: MGD	Document Number: Rev 3A
Date: Thursday, March 01, 2007	Sheet: 35 of 89



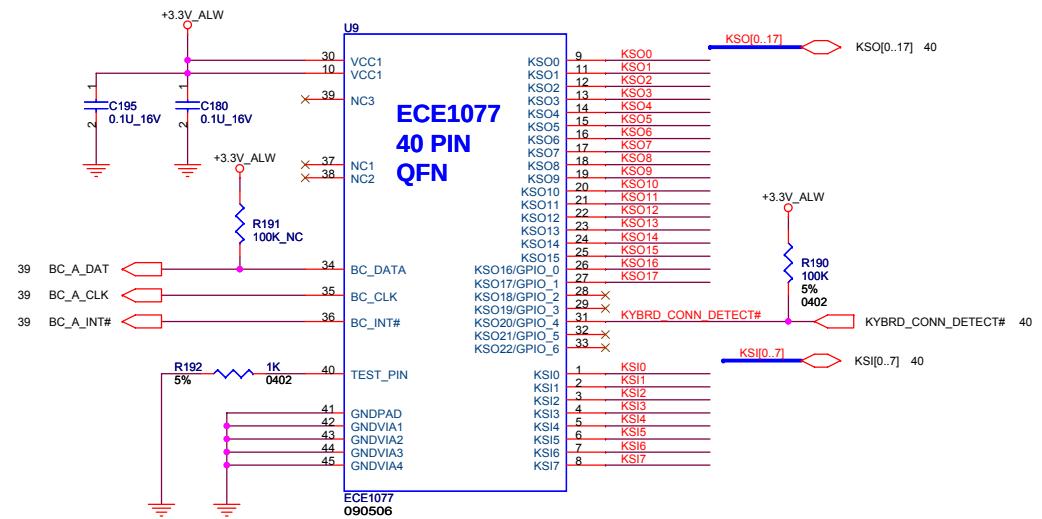
SPI Flash



RTC BATTERY



Keyboard Scan Extension



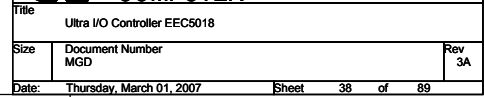
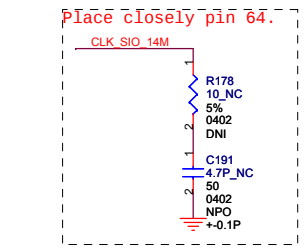
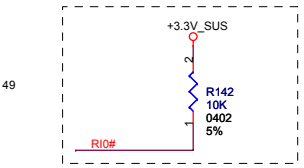
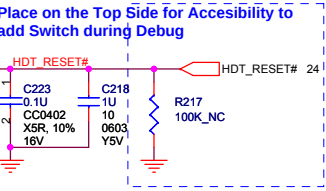
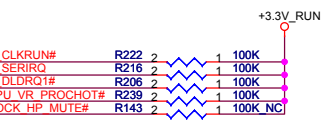
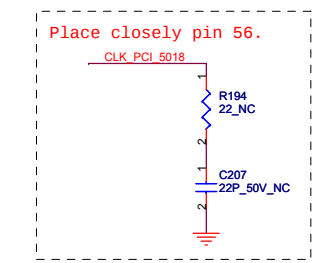
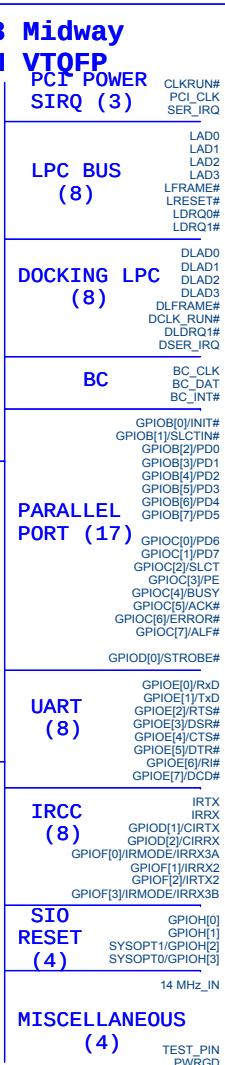
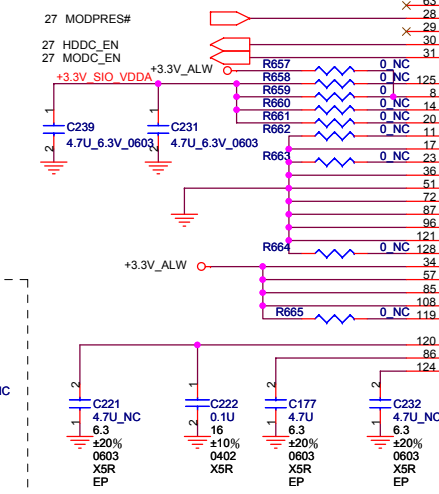
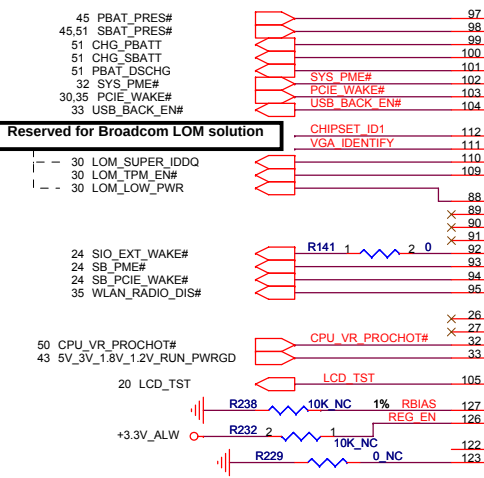
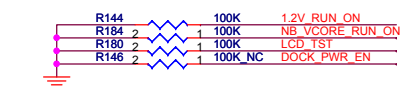
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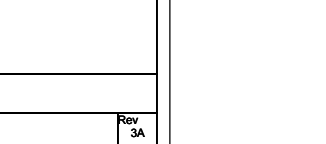
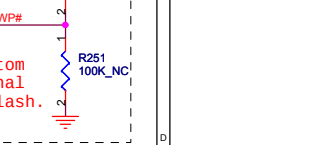
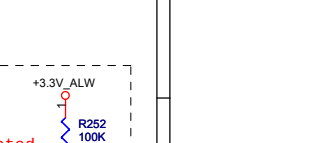
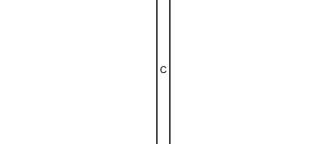
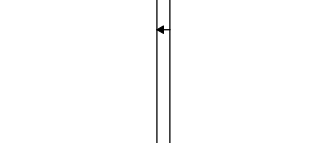
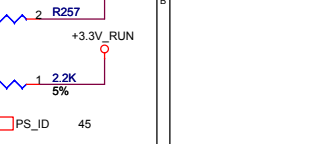
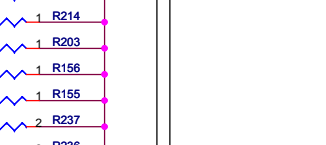
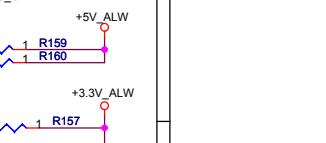
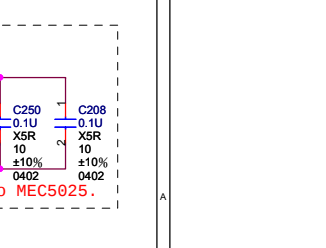
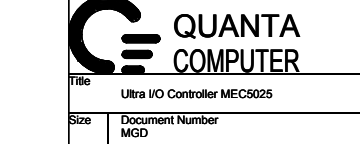
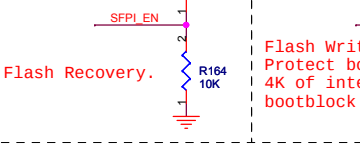
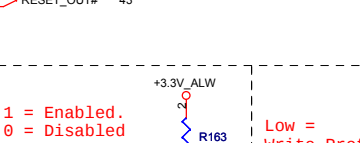
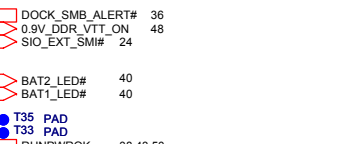
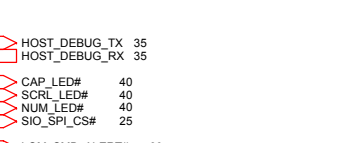
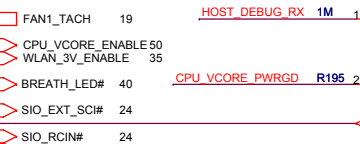
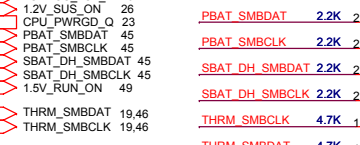
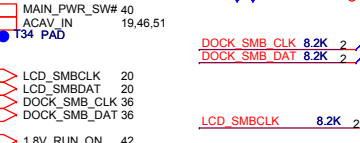
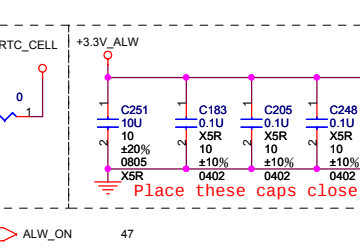
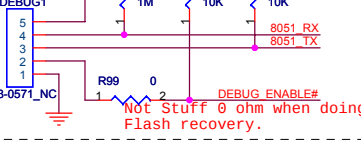
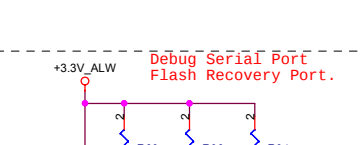
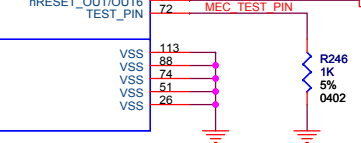
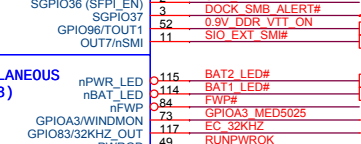
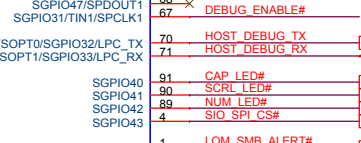
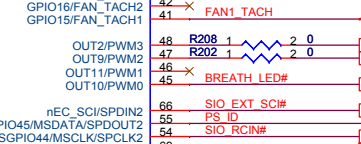
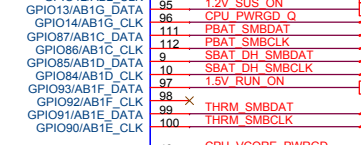
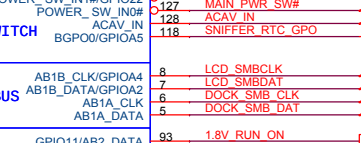
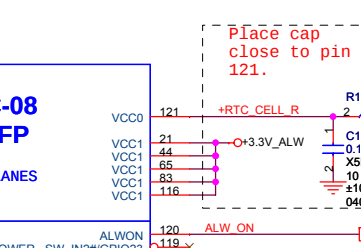
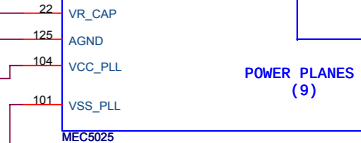
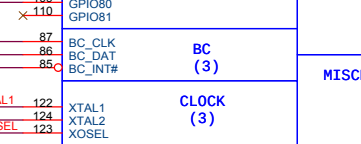
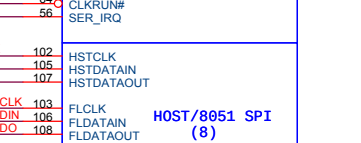
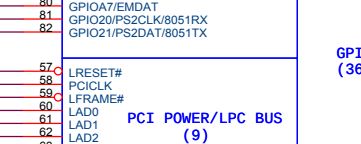
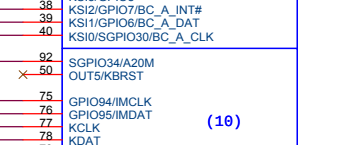
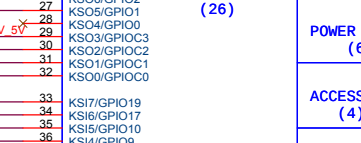
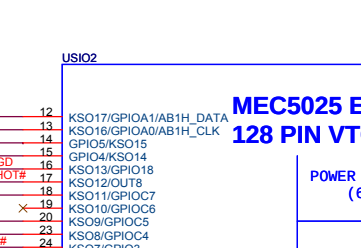
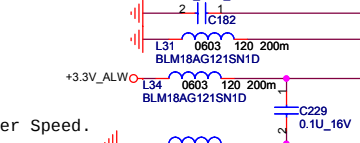
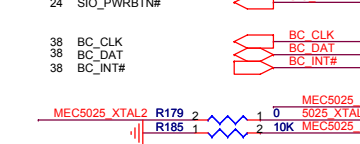
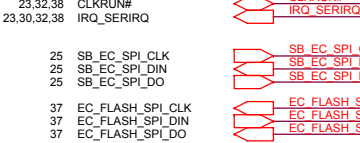
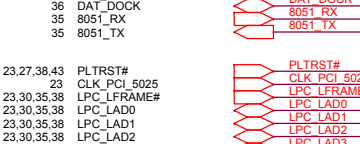
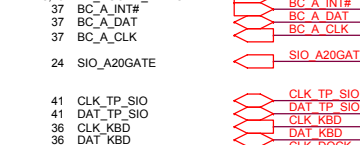
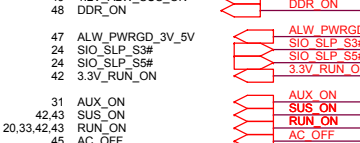
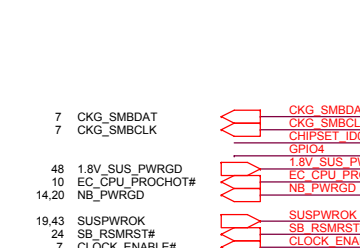
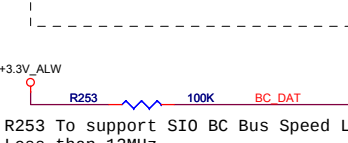
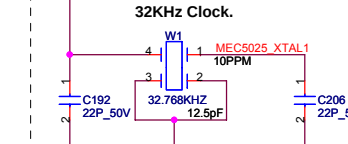
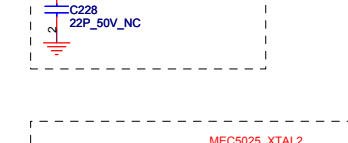
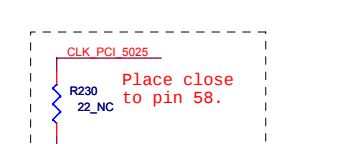
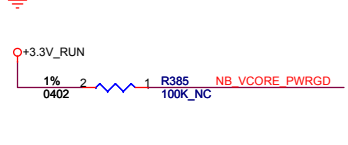
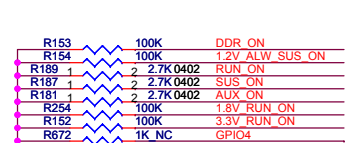
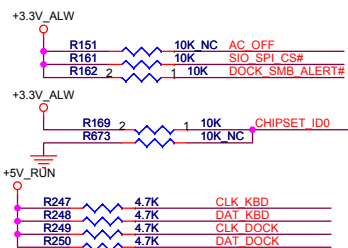
 R147 2 1 100K USB_SIDE_EN#

 R176 2 1 100K USB_BACK_EN#

 R166 2 1 10K SYS_PME#

 R173 2 1 10K PCIE_WAKE#





MEC5025 EC-08 128 PIN VTQFP

POWER PLANES (6)

POWER SWITCH (6)

ACCESS BUS (4)

GPIO (36)

MISCELLANEOUS (8)

POWER PLANES (9)

KEYBOARD/MOUSE (26)

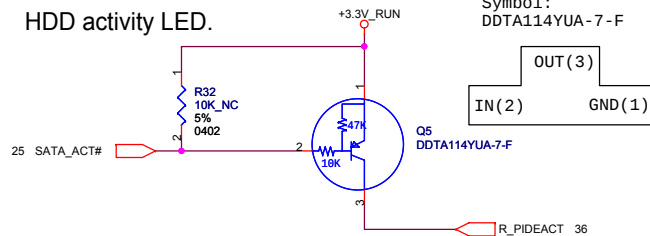
PCI POWER/LPC BUS (9)

HOST/8051 SPI (8)

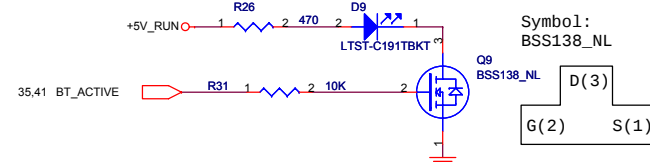
BC (3)

CLOCK (3)

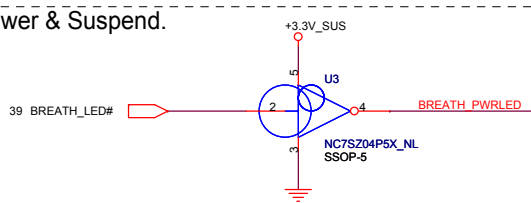
HDD activity LED.



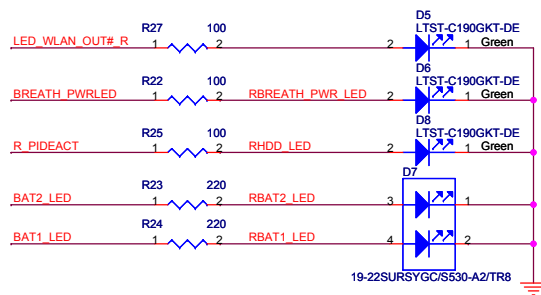
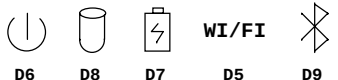
Blue tooth LED.



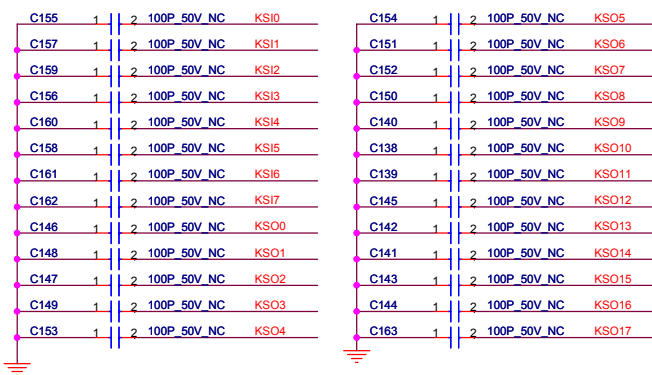
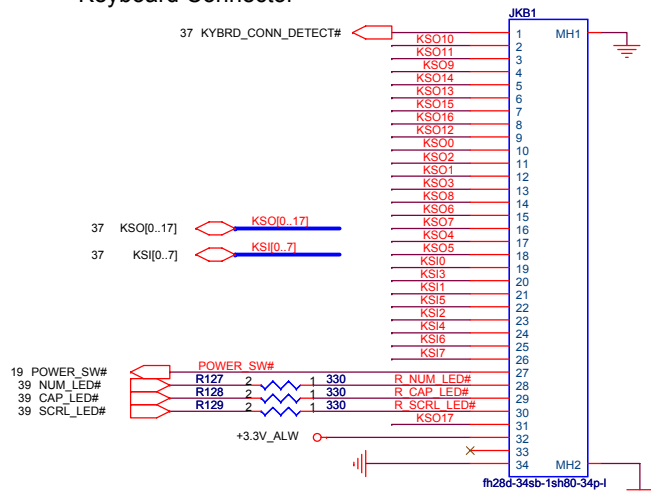
Power & Suspend.



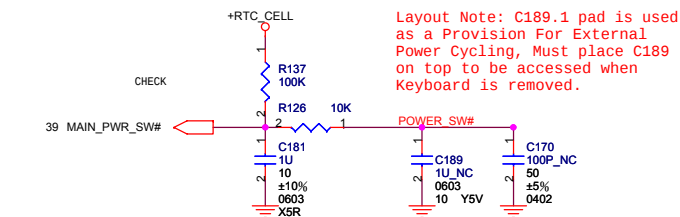
NOTE: LED layout location
Please refer to this location to layout



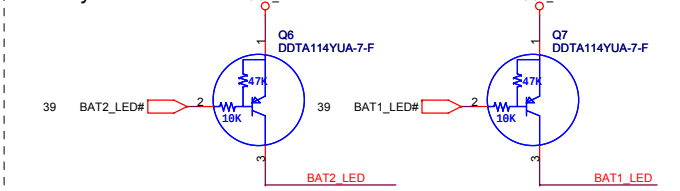
Keyboard Connector



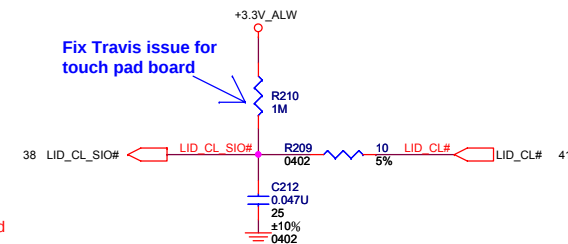
Layout Note: C189.1 pad is used
as a Provision For External
Power Cycling, Must place C189
on top to be accessed when
Keyboard is removed.



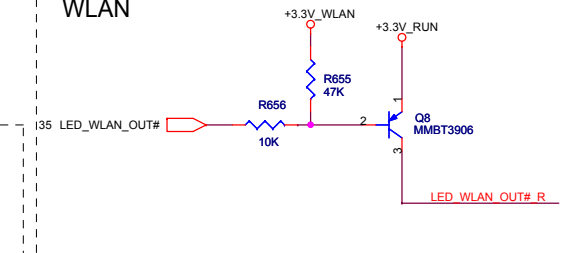
Battery status.



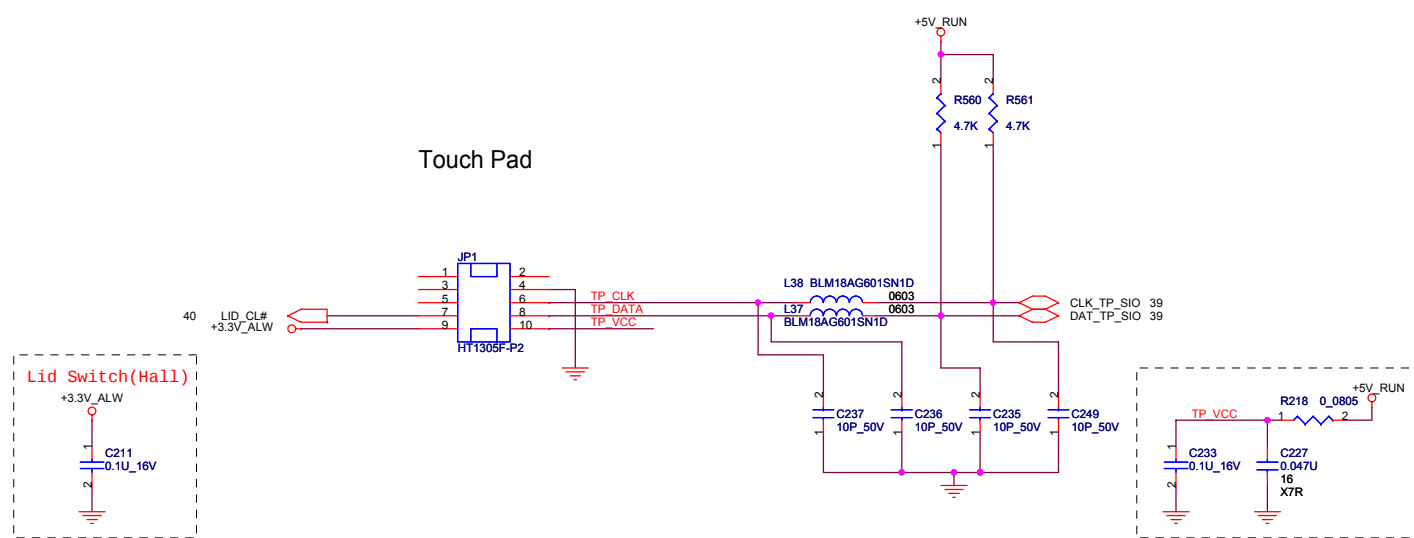
Hall Switch



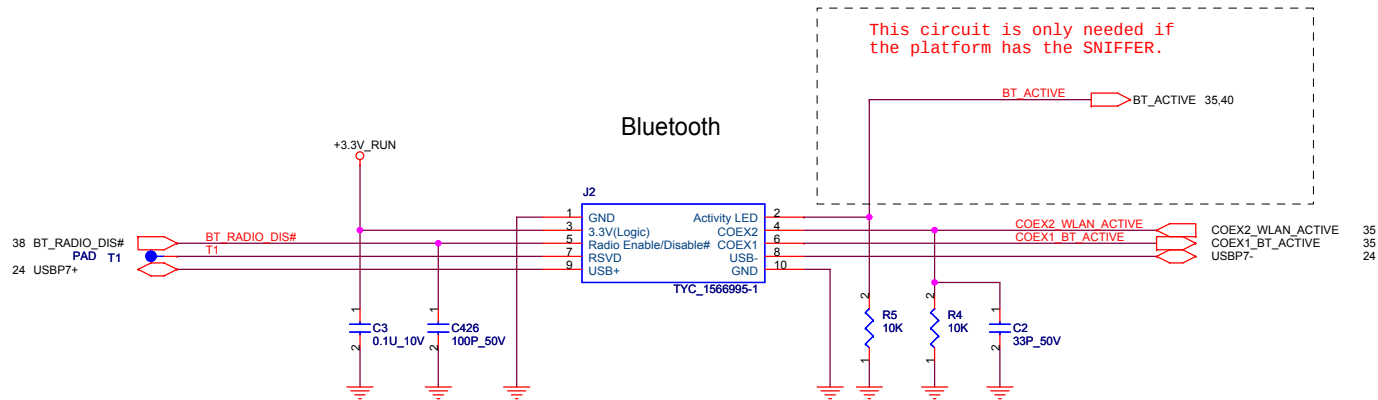
WLAN



Touch Pad

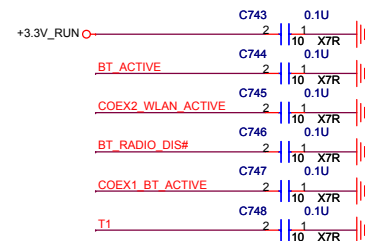


Bluetooth



EMI solution

please as close as possible to the connector (J2.1-J2.7) on these traces



Title TOUCH PAD, BULE TOOTH & FIR

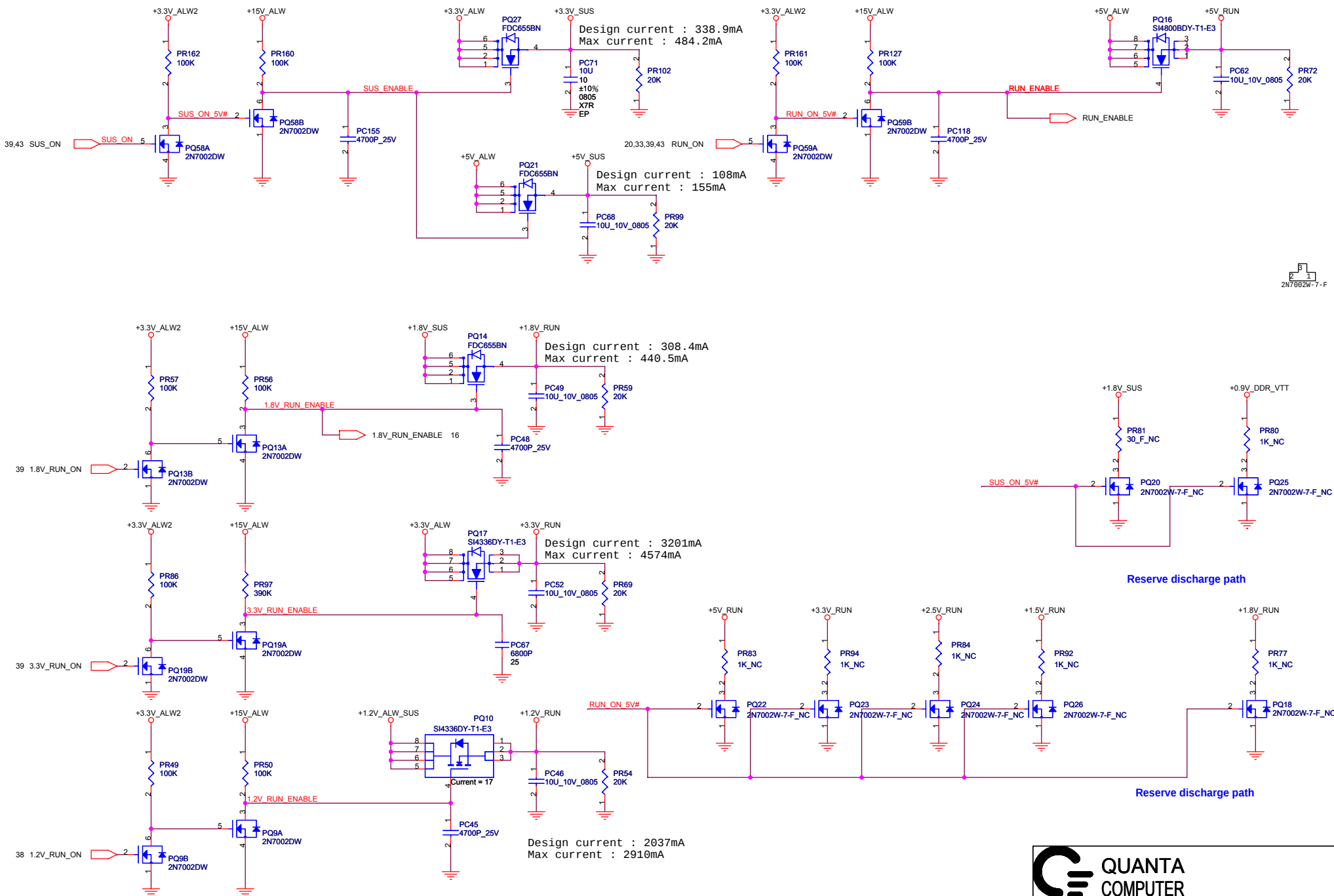
Size Document Number MGD

Rev 2A

Date: Thursday, March 01, 2007

Sheet 41 of 89

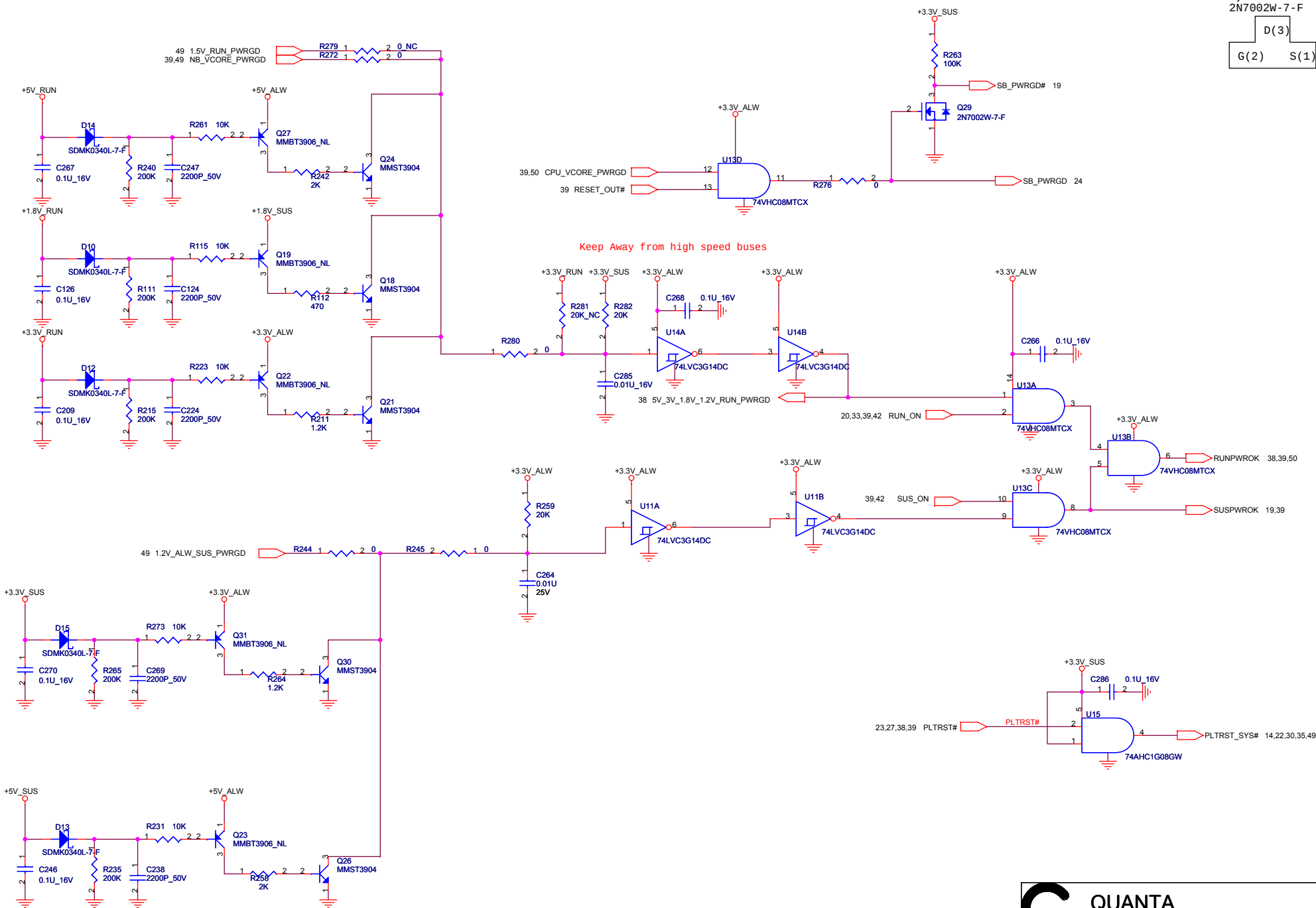
Design current : 1888mA
Max current : 2697mA



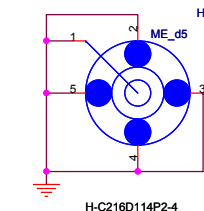
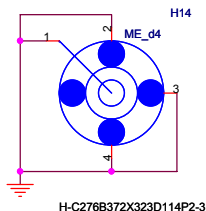
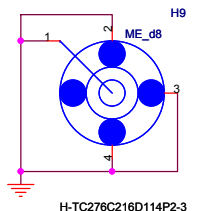
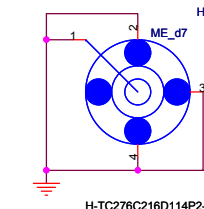
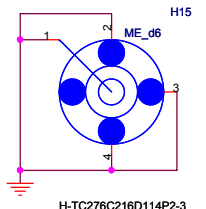
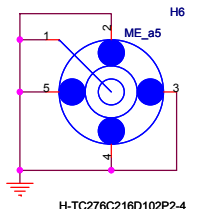
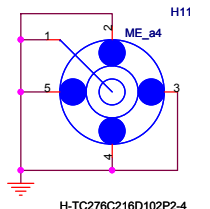
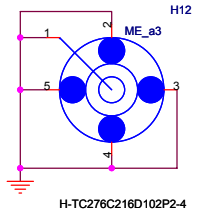
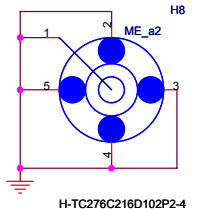
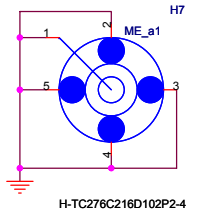
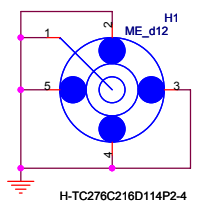
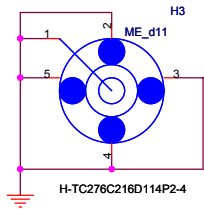
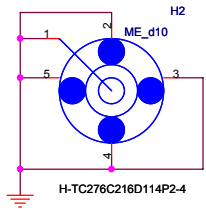
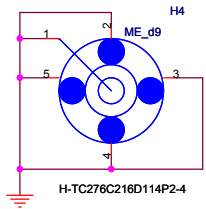
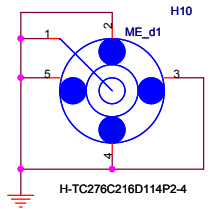
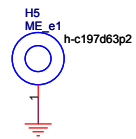
Symbol:
2N7002W-7-F

D(3)

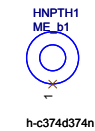
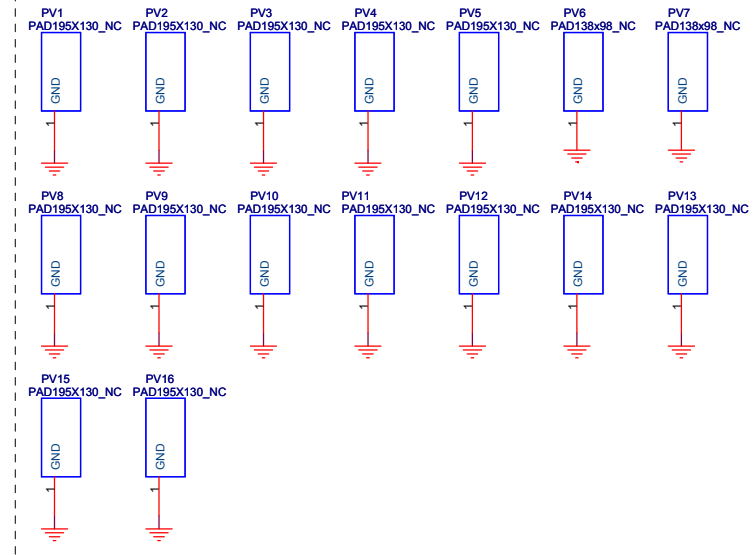
G(2) S(1)



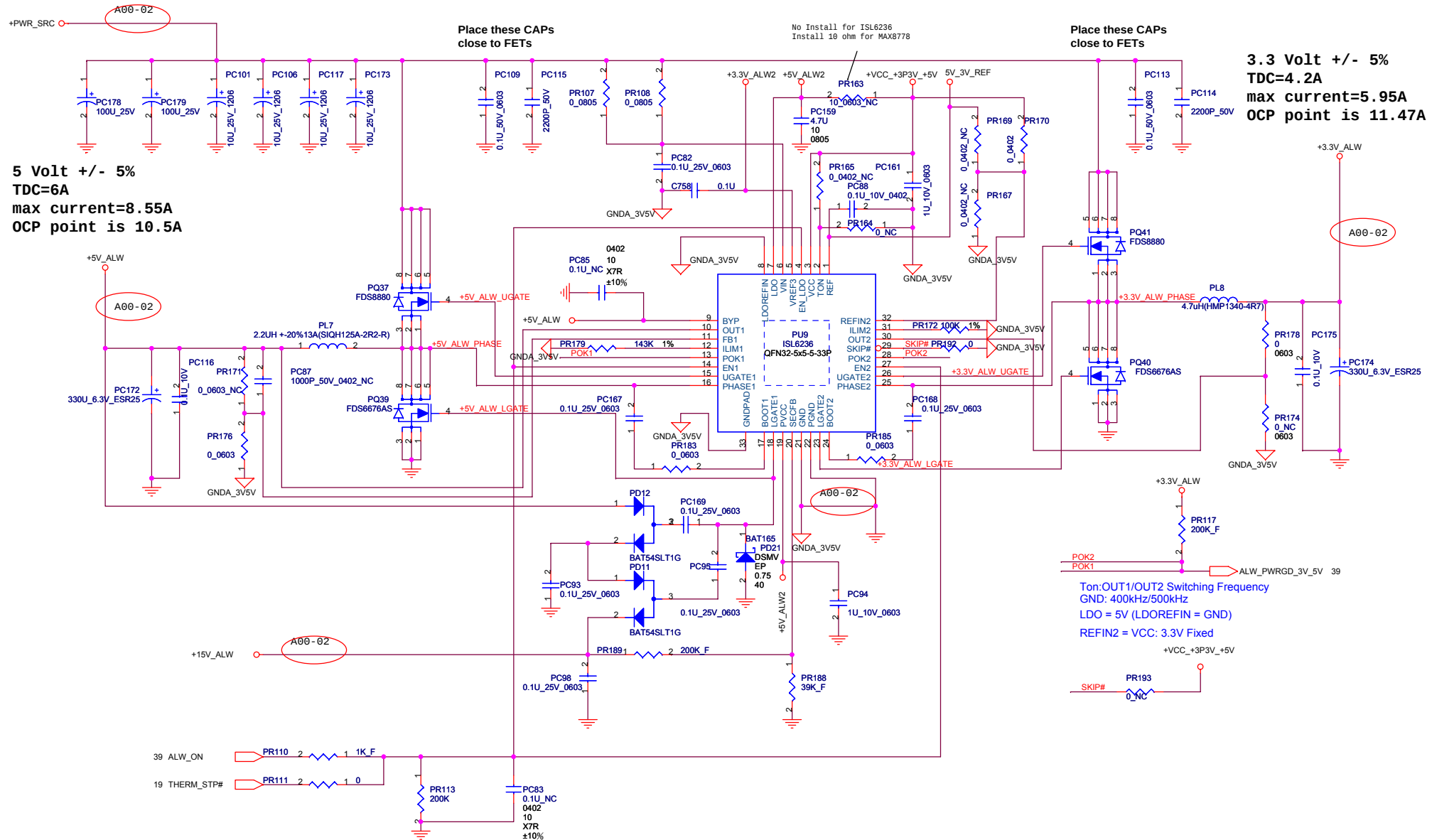
MDC



Reserved for EMI.

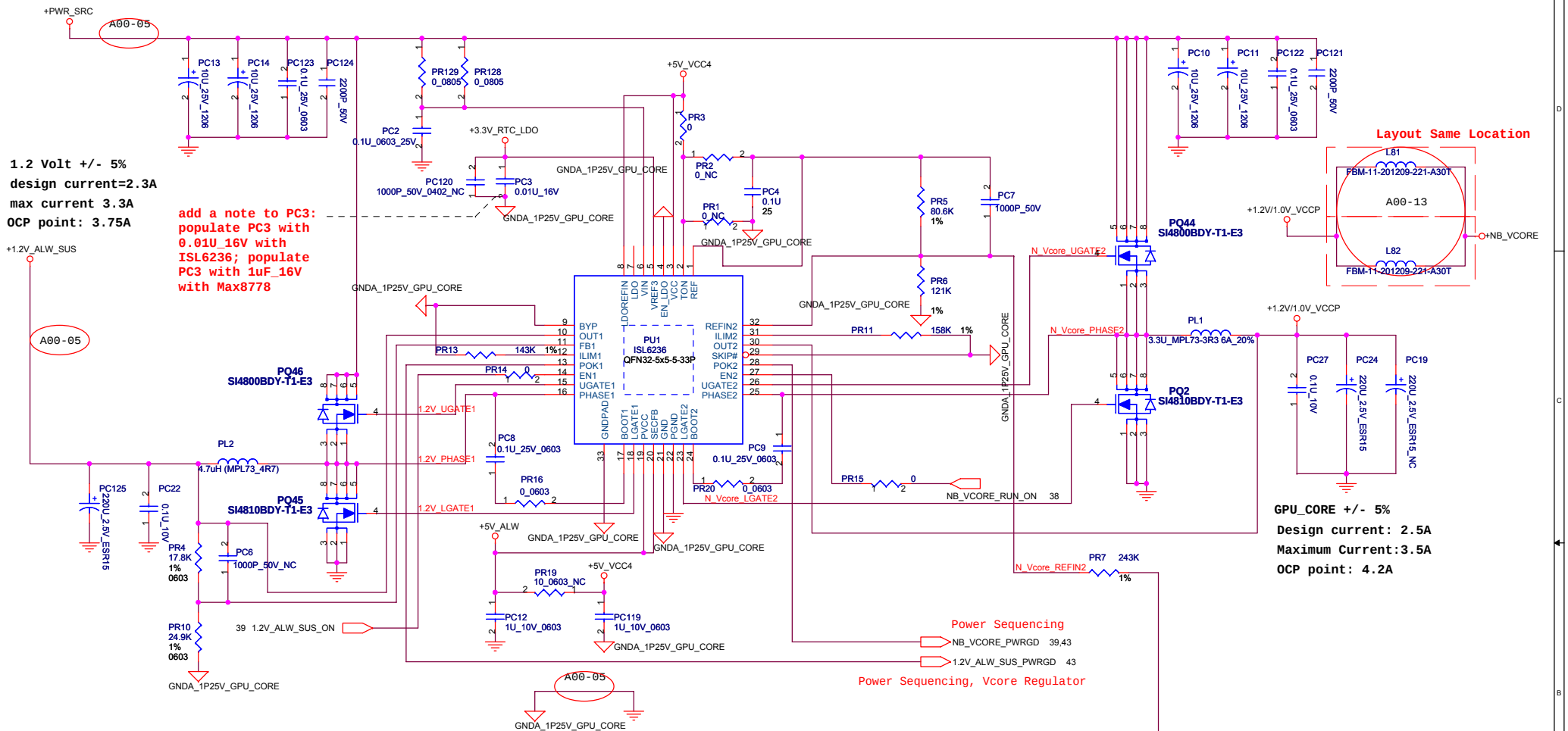


DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

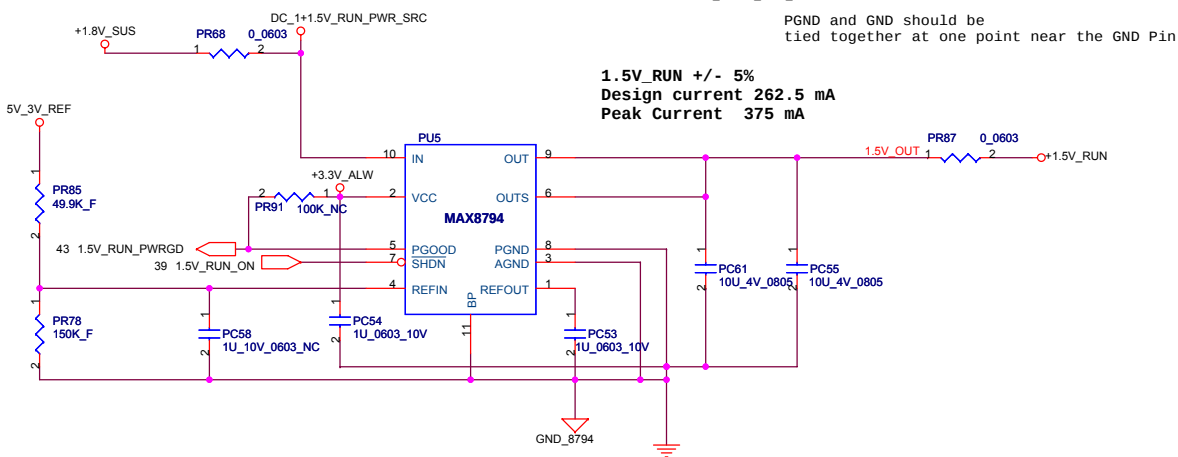


1.2 Volt +/- 5%
design current=2.3A
max current 3.3A
OCP point: 3.75A

add a note to PC3:
populate PC3 with
0.01u_16V with
ISL6236; populate
PC3 with 1uF_16V
with Max8778



GPU_CORE +/- 5%
Design current: 2.5A
Maximum Current:3.5A
OCP point: 4.2A



1.5V_RUN +/- 5%
Design current 262.5 mA
Peak Current 375 mA

PGND and GND should be
tied together at one point near the GND Pin

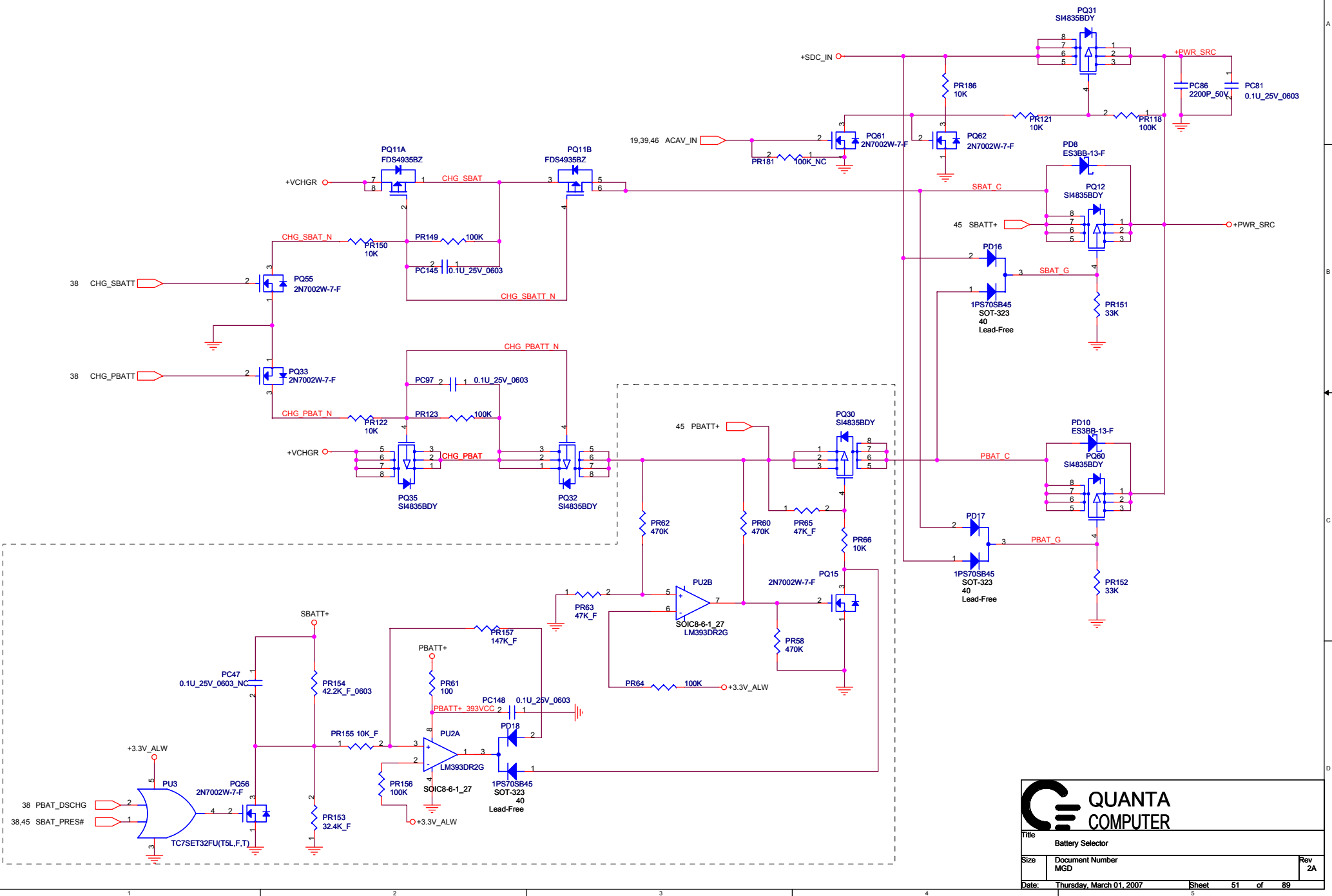
Power Sequencing
NB_VCORE_PWRGD 39,43
1.2V_ALW_SUS_PWRGD 43
Power Sequencing, Vcore Regulator

Symbol:
2N7002W-7-F

D(3)

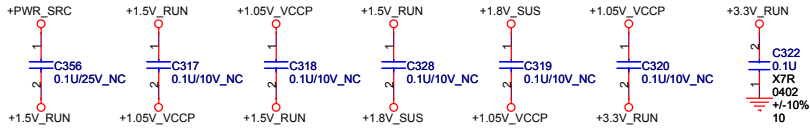
G(2)

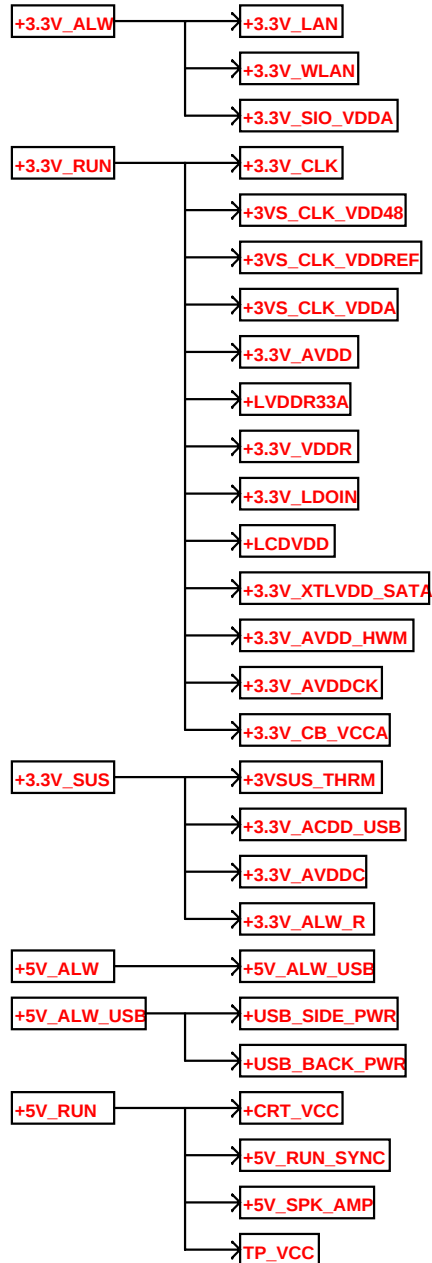
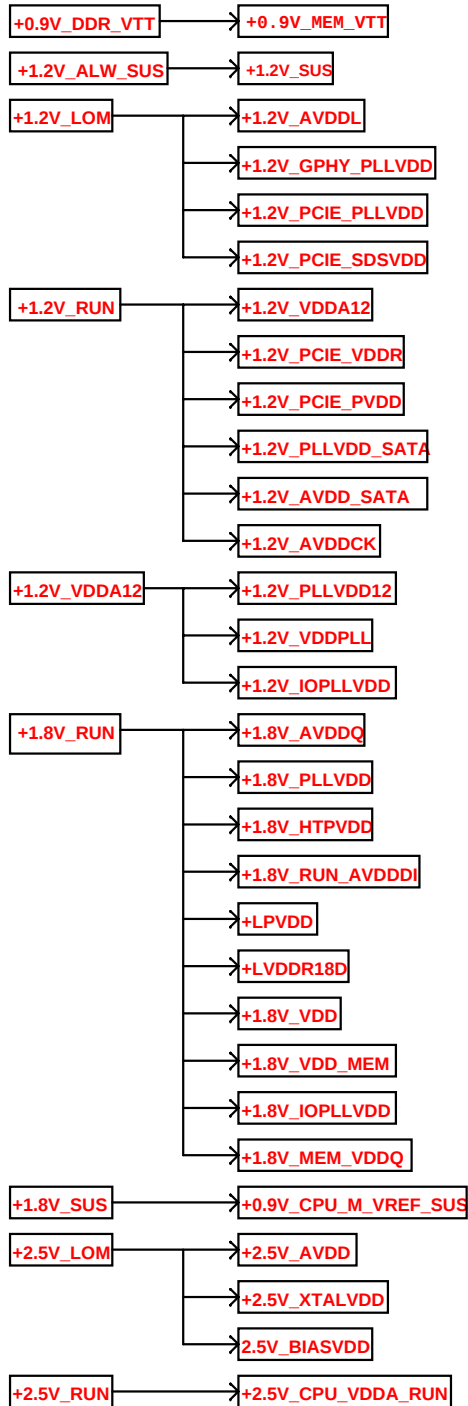
S(1)



Reserved for EMI.

Stitching caps





072806 PG.7

Add C722 0.47uF cap close to U1 on +3.3V_CLK_VDDA to GND after the ferrite for decoupling

072806 PG.7

Add C723 0.47uF cap close to U1 on +3VS_CLK_VDD48 to GND after the ferrite for decoupling

072806 PG.7

Add C724 0.47uF cap close to U1 on +3VS_CLK_VDDREF to GND after the ferrite for decoupling

072006 PG.7

Changed MINI2CLK_REQ# to route to CLKREQB# pin 32 of the clock chip, and MINI1CLK_REQ# routed to CLKREQC#.

072006 PG.7

All components of CLK_PCIE_MINI1 can be removed, including the series resistors R14, R15, R21, and R20.
No connect pins 47 and 46 of the clock chip, U1.

072206 PG.7

Remove the series resistor R27 on the CLK_SMCARD_48M, because this signal is not used.
No connect pin 7 of the clock chip, U1.

072206 PG.7

Add a 10pF NC cap to ground on the following clocks for WWAN antennae tuning:

CLK_SB_48M

CLK_SIO_14M

CLK_NB_14M

CLK_SB_14M

CLK_HTREF_66M

072206 PG.9

Because need to avoid DDR2 signals crossing, DIMM should be placed, routed and added notes as below:

DIMMA = Far = Bottom

DIMMB = Near = Top

072206 PG.9

Add note.

072206 PG.10

Change C32 from 470pF to 220pF

(This is the cap that is between H_THERMDC and H_THERMDA)

072206 PG.10

Removed C284/100uF form page 19 to close L5 on page 10.

071206 PG.10

Change C28 from 3900pF to 3300pF

(This cap is on +2.5V_CPU_VDDA_RUN)

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072206 PG.10
Populate Q3 and R90
(These parts populate the CPU_EC_PROCHOT# circuit)

072206 PG.10
Change R91 from the +3.3V_RUN rail to the +3.3V_SUS rail
(R91 is a pull-up on CPU_EC_PROCHOT#)

072206 PG.13
Delete R107 and R109.(Include NOTE)
(These pins are NC for RS690T, and are only used on the RS485 that will not be used.)

072806 PG.14
Added R641/33 and C726/22pF for AC term.And add note :RC closely clock
pin for length: 50 mils

072206 PG.14
Delete L11.
(L11 is a pop option to connect +LVDDR18A on the RS485 to +1.8V_RUN, but the RS690T uses +3.3V_RUN)
Change symbol pin name from LVDDR18A_ to LVDDR33A_
Change signal pin name from +LVDDR18A to +LVDDR33A

072206 PG.14,25,30,35
Populate R118
No pop R299-R301
Pop R387 (LOM control)
Pop R466 (WLAN)
(The plan is to use PLTRST_SYS# to reset PCIE devices at first, and not use the GPIOs)

072206 PG.14
Delete R120, and R122.
(These resistors are pull-ups on LCD_DDCCLK and LCD_DDCDAT, which are duplicates of R137, and R142)

072206 PG.14
Change C113 from 470pF to 220pF
(This cap is between NB_THERMDA, and NB_THERMDC)

072206 PG.14
No Connect R140, R139, and C115
(These parts are on the NC RS690T flash)

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072206 PG.14

No Connect R127, and C114.

(These parts are on the BMREQ# circuit.)

072406 PG.16

Added Resister/68ohm/0402/5% between MEM_CLKP and MEM_CLKN, and note place res to colse to U5.

072806 PG.17

Added Note for decoupling (total of 8 caps) for JDIM1, the note is "Place C185~C189 and C195~C198 close to JDIM1". Changed to "no pop" on C244-C251 with same as Beck for reserve stitching function between +1.8V_SUS and 0.9V_DDR_VTT.And change C185~189 to 0.1uF for memory power decoupling.

072806 PG.17

Added Note for decoupling (total of 8 caps) for JDIM2, the note is "Place C190~C194 and C199~C202 close to JDIM2". Changed to "no pop" on C252-C259 with same as Beck for reserve stitching function between +1.8V_SUS and 0.9V_DDR_VTT.And change C190~194 to 0.1uF for memory power decoupling.

072406 PG.18

No pop C244...C259.

(The 16 caps from +1.8V_SUS to +0.9V_DDR_VTT are only populated if needed.)

072406 PG.18

Delete C241, C242, C243.

(These are 3 additional +1.8V to +0.9V caps. The 16 caps C244...C259 are enough, and these 3 can be deleted.)

072806 PG.19

Change R166 and R168 to be pulled up by +3.3V_SUS, not +5V_SUS

(R166 and R168 are on the VCP2 circuit)

072806 PG.19

Change the Q13 pin 2 connection from 5V_CAL_SI02# to 5V_CAL_SI01# that connects to pin 14 on the ECE4001.

(Q13 is on the VCP2 circuit)

072806 PG.19

Populate the VCP 2 circuit for thermals.

The circuit includes: R166, C266, Q13, and R168.

072806 PG.19
Change R171 from 10k NC to 47k NC
(R171 is the pull-up on THERM_STP# to +RTC_CELL)

072806 PG.19
Add R634 7.5k resistor to pulled up to +3.3V_SUS on 2.5V_RUN_ON , and not routed to the EC.

072806 PG.19
Change C280 to 10uF caps and add C727 10uF cap.
(These are decoupling caps on +3.3V_RUN, and +2.5V_RUN for the +2.5V_RUN LDO circuit)

072806 PG.19
Add a RB751 diode in series between R170 pin 1, and J1 pin 2 of the fan connector.

072806 PG.19
No Pop C270
(C270 is a 100pF cap on FAN1_TACH)

072806 PG.20
Change R195 from 100k to 200k to match Becks.

072806 PG.20
Add 0.1uF cap to pin 1 of Q17, LCDVDD switch, to match Becks.

072806 PG.20
Add diode or circuit to pin 2 of Q20. For EC control of power to panel, add wire 0Red configuration with GPU and EC 0R control of LCDVCC power switch. Add a NoPop 0 ohm bypass resistor for diode in GPU control path so that this change can be backed out. Connect the EC control for LCDVCC to MEC5025 - GPIO12/AB2A_CLK. Signal name is LCDVCC_TST_EN

072706 PG.20
Change Q20 form DDTC124EUA-7-F to DTC124EUA_7-F. Because DDTC124EUA-7-F(Q20) is not available in Quanta warehouse, but we had DTC124EUAT-106(Q20) which feature is same as DDTC124EUA-7-F, and the vendor is ROHM who is in Dell PSL.

073006 PG.23
Add R637 0ohm series resistor at pin C1, X2 input of SB, of U10.
Series resistor needed for tuning crystal circuit

073006 PG.23
Remove R246. This signal is NoPop so resistor is not needed.

073006 PG.23
Connect PCI_REQ4# and PCI_GNT4# to test point and remove off page arrow symbol.

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073006 PG.24

No AC Term at load on CLK_SB_14M. Add AC term(R633,C710) close to load (~50 mils from clock pin).

073006 PG.24

No AC Term at load on CLK_SB_48M. Add AC term(R632,C709) close to load (~50 mils from clock pin).

073006 PG.24

Add one C439 0.1uF cap from +3.3V_AVDD_USB to GND for USB PWR decoupling. NoPop this capacitor.

073006 PG.24

Add FET isoation circuits on page 35 for SMBUS, signal MEM_SDATA and MEM_SCLK, to WLAN with pull ups connected to WLAN power plane. Pull up resitor should be connected to +3.3V_WLAN

073006 PG.24

Change pull up resistor to NoPop for R263, R267, R268, R269, R264, R259 and R260 same as Becks

073006 PG.24

Change SHUTDOWN#/GPIO5 pull up power plane, R259, from 3.3V_SUS to 3.3V_RUN, same as Becks

073006 PG.23

Add pad for cap C728 from PCI_CLK1 to GND for AC term. Place AC term close to load (~50 mils from clock pin).

073006 PG.23

Add pad for cap C725 on PCI_CLK0 to GND for AC term. Place AC term close to load (~50 mils from clock pin).

073006 PG.23

Add pad for cap C714 on CLK_PCI_PCCARD to GND for AC term. Place AC term close to load (~50 mils from clock pin).

073006 PG.23

Add pad for cap C713 on CLK_PCI_DOCK to GND for AC term. Place AC term close to load (~50 mils from clock pin).

073006 PG.25

Add three 0.1uF caps(C441,C442,C443) from +1.2V_AVDD_SATA to GND for Serial ATA Power decoupling. NoPop these capacitors.

073006 PG.25

Add one 0.1uF cap(C586) from +1.2V_PLLVDD_SATA to GND for Serial ATA Power decoupling NoPop capacitor

073006 PG.26

No EMI decoupling for +1.2V_RUN. Add two 0.1uF(C731,C732) caps from Power nets to GND. NoPop these capacitors

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073006 PG.26

No EMI decoupling for +3.3V_RUN. Add two 0.1uF(C733,C734) caps from Power nets to GND.
NoPop these capacitors.

073006 PG.26

Add two 0.1uF cap(C735,C736) on +3.3V_AWL_R to GND for decoupling

073006 PG.30

Add one more 0.1uF cap(C737) on +1.2V_AVDDL to GND for decoupling if space allows
NoPop capacitor

073006 PG.30

Add one more 0.1uF(C738) cap on +2.5V_AVDD to GND for decoupling if space allows.
NoPop capacitor.

073006 PG.30

Connect LOM_GPI00 to USI02 pin 1 (SGPIO35) -- This LOM_GPI00 is SMBALERT for SMBUS. Check SGPIOx of EC (USI02) connections to be consistent with Dell M08 design.

073006 PG.31

Add another 0.1uF(C721) capacitor in paralled with C510 to match Becks

073006 PG.31

Remove comment regarding "centerTap" voltage. Remove entire comment since only Broadcom LOMs are supported.

073006 PG.33

Delete C566 and C560.

(These caps are the 150uF no connect caps for USB side and back power. Only one 150uF cap is needed for each rail, and there is not any need to have an option for two per rail.)

073006 PG.33

No pop serial port capacitors same as Becks. C546, C552, C548, C550, C554-C557.

073006 PG.35

Add one 0.1uF cap(C560) on +1.5V_RUN to GND close to J9 for decoupling
NoPop capacitor

073006 PG.35

Populate R466 so that the WLAN is reset w/ PLTRST_SYS#

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073006 PG.37

Pin 31 GPIO_4 on the 1077 should connect to KYBRD_CONN_DETECT# w/ a 100k pull-up to +3.3V_ALW, and route to pin 1 of the keyboard connector. This signal is currently connected to the south bridge. That connection at the SB and the pull up resistor should be removed. Delete signal connection to Southbridge
Delete R309.

073006 PG.37

Change R489 from 0 Ohms to 1k
(R489 is a pull-down on the test pin on the ECE1077)

073006 PG.14

add a 0 ohm series resistor on LCD_DDCDAT between R142 pin 2 and Q8 pin 1. Pop this resistor
Connect DDC_DATA (U3 pinB3) to Q8 pin 1 through a 0 ohm resistor. Nopop this resistor.

073006 PG.13

Delete R103, R104, R105, R106 and C79, C80, C81, C82.
Add 0.1uF series capacitor to all the DVI_TX+ and DVI_TX- signals.
Name the signal on the output side of the capacitor to DVI_C_TX+ and DVI_C_TX-.
Add 499 ohm resistor from the DVI_C_TX+ and DVI_C_TX- signals to ground at the Dock side of the series capacitor. These need to be placed at the capacitors to prevent an additional via transition.

073006 PG.15

Change C134, C135, C136, C145, C146, C147 C148 to 0.01uF

073006 PG.14

Delete R120 and R122. These are extra. See R137 and R142

073006 PG.37

Add a 4.7k pullup to +3.3V_ALW on BC_A_DAT

073006 PG.40

Change Q50 power plane from +3.3V_RUN to +3.3V_WLAN, same as Becks

073006 PG.38

CPU_VR_PROCHOT signal moved from the 5018 GPIOF0 (pin 118) to the 5018 GPIOH6
5018 GPIOF0 left as NC

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073006 PG.39

5025 GPIO KSI4/GPIO9 connected to AC_OFF.

DDR_ON connected to 5025 GPIO KS05/GPIO1 per the M'08 GPIO map.

073006 PG.39

1. Change signal name CPU_EC_PROCHOT# to EC_CPU_PROCHOT# to match GPIO map definition.
2. Move EC_CPU_PROCHOT# from 5025 GPIO12 to 5025 OUT8 per the GPIO map
3. Connect signal LCDVCCTST_EN to 5025 GPIO12
4. Delete net 2.5V_RUN_ON signal at 5025 KS010/GPIOC6 and no connect pin

073006 PG.26

USB_PHY_1.2V inputs of SB connected to 1.2V_SUS.

Add a FET switch circuit for +1.2V_ALW_SUS -> +1.2V_SUS - same as Becks.

073006 PG.23

Add 10pF, NoPop capacitor from signal to GND for each of the following signals (same as Becks):

CLK_PCI_PCCARD

CLK_PCI_DOCK

CLK_PCI_5018

CLK_PCI_5025

073006 PG.24

Add 27pF, NoPop capacitor to following signals (same as Becks):

SB_AZ_MDC_SDOUT

SB_AZ_MDC_SYNC

SB_AZ_CODEEC_SDOUT

SB_AZ_CODEEC_SYNC

SB_AZ_CODEEC_RST#

Set C346 and C347 as NoPop

073006 PG.20

Q25 is installed backwards. Currently, 5V can be driven to NB via body diode. Reverse connection for pin 3 and pin 1.

073006 PG.20

NoPop R192 and R193. These are for D'05 inverter support and are not required.

073006 PG.15

Change C122 from 1uF to 0.1uF and add another 0.1uF capacitor in parallel.

NoPop C122.

073006 PG.15
Add another 0.1uF(C740) in parallel to C143
NoPop this capacitor

073006 PG.15
Add another 0.1uF(C739) in parallel to C155
NoPop this capacitor

073006 PG.25
Add another 0.1uF(C730) parallel to C352.
NoPop capacitor.

073006 PG.29
No diode protection on INT_MIC_L+/- & INT_MIC_C_L+/- lines. Add pads for SM05_SOT23 diode package.

073006 PG.21
Change R206 and R207 PU power plane from +CRT_VCC to +5V_RUN_SYNC

073006 PG.22
Change Svideo termination resistors, R214, R215, R217, from 75 ohms to 150ohms.

073006 PG.30
Connect the CLK_PCI_TPM to +3.3V_LAN using 10K Ohm resistor if TPM is not used.

073006 PG.25
add 1K ohm pullup resistor from SPI_CS# at 3V_ALW. Per ATI schematic review.

073006 PG.25
ADD LDO to power SB AVDD_SATA and PLVDD_SATA. Add pop option to remove the LDO for A13 SB silicon.
Per review by ATI.

073106 PG.25
Add 0 ohm series resistor(R313) to signal SATA_X2 to allow tuning of the crystal circuit.

073106 PG.27
Add a 0 ohm(R351), no pop, series resistor at pin 62 of JMOD1 to allow the signal PLTRST# as an option for driving the IDE_RST_MOD input of the JMOD1 connector.

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073106 PG.28

No stuff C448, C457 . May need to add for audio performance later.

073106 PG.28

R355 This resistor must connect to +3.3V_RUN .

Otherwise, there is a chance of backdriving the 3.3V rail through the codec.

073106 PG.28

R352 This resistor must be populated to pull up DOCK_HP_MUTE# to VDDA. Otherwise, the signal will not work.

073106 PG.28

R353 This resistor must be populated to pull up AUD_SPDIF_SHDN to VDDA. Otherwise, the signal will not work.

073106 PG.28

R345~R348 These should change to 100K per audio reference design to save power.

073106 PG.28

C439, C441, C442, C443, R349, R351 Remove these. These are not necessary for the design

073106 PG.35

Removed C586 and keep C585 same as C751 of Becks(6/22).

073106 PG.36

Change R479 from 100k to 200k same as Becks.

073106 PG.36

Change Q45 from FDS6679 to FDS4435, same as Becks.

073106 PG.38

Change R490 and R491 from 10k to 100k same as Becks.

073106 PG.38

Change R510 from 12k to 10k, same as Becks.

073106 PG.38

USI01 pin 81 should be connected to AUD_HP_NB_SENSE. Off page marker signal is there but net is not connected.

073106 PG.38

Change R518 from 22ohm to 10ohm and change C607 from 22pF to 4.7pF same as Becks.

073106 PG.39

Change R556 from 0ohm to 1k, same as Becks.

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073106 PG.39

Add 100k(R583) pull down resistor to DDR_ON signal, same as Becks.

073106 PG.39

Set AC_OFF PU, R521 as NoPop, same as Becks.

073106 PG.39

Change LID_CL_SIO# pull up resistor(R571) from 100k to 1M, same as Becks.

073106 PG.25

Delete R298 and the signal connection to pin V5 of the SB since WWAN is not supported

073106 PG.27

Add a 0ohm(R349) series resistor at JMOD1 pin 13
NoPop resistor

073106 PG.37,49

NoPop PC187, PopPC115

Delete D15, C599, U26 and C600. Circuit is not needed because RTC_LD0 is generated by PU5.

073106 PG.29

Add a 0.1uF capacitor(C703) at pin 8 of U15A - same as Becks

073106 PG.26

Add debug resistor strap options, pullup and pulldown, for the signals PCI_AD23-PCI_AD28 - same as Becks

080106 PG.43

Contact U36-pin5 and C707-pin1form +3.3V_SUS to +3.3V_ALW.And change D22-D27 form RB751V to RB751S40T

080106 PG.37

Add back in D15 and C599 with the connection to +3.3V_RTC_LD0.

080106 PG.38,39,40

Add sniffer circuit in schematic.

Follow below step

step1. Add SW1 in schematic and contact pin1 to SNIFFER2 and contact pin4 to SNIFFER1 and contact pin3 to GND.

Step2.Add R659 between "SNIFFER1" and "WIRELESS_ON/OFF#",and add R658 to pull high to +3.3V_RUN, and add C744 between "WIRELESS_ON/OFF#" and GND

Step2.Add R661 between "SNIFFER2" and "SNIFFER_PWR_SW#",and add R660 to pull high to +RTC_CELL, and add C745 between "SNIFFER_PWR_SW#" and GND

Step3. Add Q73,Q74,R662,R663 and D32 for sniffer display circuit

Step4.Remove R627 and add module port(SNIFFER_PWR_SW#) for USI02-pin119

Step5.Change module port and net form "SNIFFER_YELLOW#" to "SNIFFER_YELLOW" for USI02-pin 110

Step6.Remove T178 and add module port"WIRELESS_ON/OFF#" for USI01-pin 24

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080206 PG.35
modify as below

- 1.Swap pin1 and pin3 for Q49 and Q71
- 2.Contact Q71-pin2 to +3.3V_WLAN
- 3.change module port(MEM_SDATA) and net(MEM_SDATA) to
module port(SB_SMBDATA) and net(SB_SMBDATA) in Q49-pin3 in page 35
- 4.change module port(MEM_SCLK) and net(MEM_SCLK) to
module port(SB_SMBCLK) and net(SB_SMBCLK) in Q71-pin3 in page 35

080206 PG.17,18

Follow layout request to swap for DIMM as below

Pin RP12.6 moved to net DDR_A_MA8. Pin RP26.3 moved to net DDR_B_BS1. Pin JDIM1.135 moved to net DDR_A_D35.
Pin RP11.4 moved to net DDR_A_CAS#. Pin RP21.8 moved to net DDR_CKE3_DIMMB. Pin JDIM2.159 moved to net DDR_B_D48.
Pin RP16.3 moved to net DDR_A_MA2. Pin JDIM1.22 moved to net DDR_A_D8. Pin JDIM1.158 moved to net DDR_A_D48.
Pin RP18.2 moved to net DDR_B_MA1. Pin RP26.1 moved to net DDR_B_MA0. Pin JDIM2.19 moved to net DDR_B_D7.
Pin RP18.8 moved to net DDR_B_WE#. Pin JDIM1.6 moved to net DDR_A_D4. Pin JDIM1.25 moved to net DDR_A_D13.
Pin RP16.1 moved to net DDR_A_MA4. Pin JDIM1.154 moved to net DDR_A_D42. Pin JDIM2.157 moved to net DDR_B_D53.
Pin RP12.8 moved to net DDR_A_MA5. Pin RP12.2 moved to net DDR_A_MA12. Pin JDIM1.123 moved to net DDR_A_D36.
Pin RP13.2 moved to net DDR_CKE0_DIMMA. Pin JDIM2.140 moved to net DDR_B_D45. Pin JDIM2.22 moved to net DDR_B_D9.
Pin RP17.3 moved to net DDR_A_BS1. Pin RP11.2 moved to net DDR_A_WE#. Pin JDIM1.124 moved to net DDR_A_D37.
Pin RP20.6 moved to net DDR_B_MA5. Pin JDIM1.14 moved to net DDR_A_D3. Pin JDIM1.74 moved to net DDR_A_D26.
Pin RP18.6 moved to net DDR_B_BS0. Pin RP21.6 moved to net M_ODT2. Pin JDIM1.73 moved to net DDR_A_D30.
Pin RP13.6 moved to net DDR_A_BS2. Pin JDIM1.151 moved to net DDR_A_D43. Pin JDIM1.23 moved to net DDR_A_D9.
Pin JDIM1.45 moved to net DDR_A_D21. Pin RP20.2 moved to net DDR_B_MA9. Pin JDIM1.142 moved to net DDR_A_D40.
Pin RP9.8 moved to net DDR_A_BS0. Pin RP12.4 moved to net DDR_A_MA9. Pin JDIM2.25 moved to net DDR_B_D8.
Pin JDIM2.45 moved to net DDR_B_D21. Pin RP22.8 moved to net DDR_B_MA12. Pin JDIM1.36 moved to net DDR_A_D10.
Pin RP11.8 moved to net M_ODT1. Pin JDIM1.17 moved to net DDR_A_D6. Pin JDIM1.19 moved to net DDR_A_D2.
Pin RP11.6 moved to net DDR_CS1_DIMMA#. Pin RP21.2 moved to net DDR_B_CAS#. Pin JDIM2.160 moved to net DDR_B_D49.
Pin RP20.8 moved to net DDR_B_MA3. Pin JDIM1.143 moved to net DDR_A_D44. Pin JDIM1.55 moved to net DDR_A_D23.
Pin JDIM1.58 moved to net DDR_A_D19. Pin JDIM2.142 moved to net DDR_B_D44. Pin JDIM2.154 moved to net DDR_B_D43.
Pin JDIM1.181 moved to net DDR_A_D61. Pin JDIM1.141 moved to net DDR_A_D45. Pin JDIM2.46 moved to net DDR_B_D17.
Pin RP17.1 moved to net DDR_A_MA0. Pin JDIM2.137 moved to net DDR_B_D39. Pin JDIM2.125 moved to net DDR_B_D36.
Pin JDIM2.153 moved to net DDR_B_D47. Pin JDIM1.125 moved to net DDR_A_D32. Pin JDIM2.17 moved to net DDR_B_D3.
Pin JDIM1.57 moved to net DDR_A_D18. Pin JDIM1.153 moved to net DDR_A_D47. Pin JDIM1.61 moved to net DDR_A_D29.
Pin RP9.4 moved to net DDR_A_MA1. Pin JDIM1.182 moved to net DDR_A_D57. Pin JDIM2.136 moved to net DDR_B_D35.
Pin JDIM2.36 moved to net DDR_B_D10. Pin JDIM1.35 moved to net DDR_A_D14. Pin JDIM2.124 moved to net DDR_B_D33.
Pin RP9.2 moved to net DDR_A_MA3. Pin JDIM2.14 moved to net DDR_B_D2. Pin JDIM1.157 moved to net DDR_A_D49.
Pin RP22.6 moved to net DDR_B_BS2. Pin JDIM1.159 moved to net DDR_A_D52. Pin JDIM2.134 moved to net DDR_B_D34.
Pin JDIM2.35 moved to net DDR_B_D14. Pin JDIM2.143 moved to net DDR_B_D40. Pin JDIM1.174 moved to net DDR_A_D55.
Pin RP9.6 moved to net DDR_A_MA10. Pin JDIM1.126 moved to net DDR_A_D33. Pin JDIM2.141 moved to net DDR_B_D41.
Pin JDIM1.4 moved to net DDR_A_D5. Pin JDIM2.16 moved to net DDR_B_D6. Pin JDIM2.135 moved to net DDR_B_D38.
Pin JDIM1.140 moved to net DDR_A_D41. Pin JDIM1.137 moved to net DDR_A_D34. Pin JDIM2.61 moved to net DDR_B_D25.
Pin RP22.2 moved to net DDR_CKE2_DIMMB. Pin JDIM1.176 moved to net DDR_A_D54. Pin JDIM1.46 moved to net DDR_A_D17.
Pin JDIM2.23 moved to net DDR_B_D13. Pin JDIM1.64 moved to net DDR_A_D24. Pin JDIM2.63 moved to net DDR_B_D24.

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080206 PG.32

Follow layout request to swap for 1394 as below

Pin 'L65.1' moved to net 'IEEE1394_OZTPA-'.
Pin 'L66.1' moved to net 'IEEE1394_OZTPB+'.
Pin 'L66.4' moved to net 'IEEE1394_OZTPB-'.
Pin 'L65.4' moved to net 'IEEE1394_OZTPA+'.
Pin 'L65.2' moved to net 'OLTPA-'.
Pin 'L66.2' moved to net 'OLTPB+'.
Pin 'L66.3' moved to net 'OLTPB-'.
Pin 'L65.3' moved to net 'OLTPA+'.

080206 PG.33

Follow layout request to swap for USB2 as below

Pin 'L70.4' moved to net 'USBP2-'.
Pin 'L70.1' moved to net 'USBP2+'.
Pin 'L70.3' moved to net 'USBP2_D-'.
Pin 'L70.2' moved to net 'USBP2_D+'.

080206 PG.33

Follow layout request to swap for on board momory as below

Pin 'U5.G2' moved to net 'MEM_DQ3'. Pin 'RP7.3' moved to net 'MEM_A1'.
Pin 'U5.B9' moved to net 'MEM_DQ14'. Pin 'U5.C8' moved to net 'MEM_DQ15'.
Pin 'RP8.3' moved to net 'MEM_BA0'. Pin 'U5.F1' moved to net 'MEM_DQ1'.
Pin 'U5.D3' moved to net 'MEM_DQ12'. Pin 'RP1.3' moved to net 'MEM_A0'.
Pin 'U5.H3' moved to net 'MEM_DQ6'. Pin 'RP2.1' moved to net 'MEM_A6'.
Pin 'RP1.1' moved to net 'MEM_A2'. Pin 'RP5.1' moved to net 'MEM_A3'.
Pin 'U5.H1' moved to net 'MEM_DQ2'. Pin 'U5.D7' moved to net 'MEM_DQ11'.
Pin 'U5.H9' moved to net 'MEM_DQ4'. Pin 'RP6.1' moved to net 'MEM_BA2'.
Pin 'U5.H7' moved to net 'MEM_DQ0'. Pin 'RP3.1' moved to net 'MEM_A8'.
Pin 'RP2.3' moved to net 'MEM_A11'. Pin 'RP6.3' moved to net 'MEM_A10'.
Pin 'U5.B1' moved to net 'MEM_DQ10'. Pin 'U5.D1' moved to net 'MEM_DQ8'.
Pin 'RP4.1' moved to net 'MEM_A5'. Pin 'RP3.3' moved to net 'MEM_A4'.
Pin 'U5.G8' moved to net 'MEM_DQ5'.

080206 PG.19,39

Add module port(2.5V_RUN_ON) for U6-pin27 in page 19
Add module port(2.5V_RUN_ON) for USI02-pin 15 in page 39

080206 PG.19

change R182 voltage rail to from 3.3V_RUN to 3.3V_SUS

080206 PG.21

nopop R206

080206 PG.24

change pullup of R254, R255, R257, R261, R262 from 3.3V_SUS to 3.3V_ALW_R

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080206 PG.24
change pullup of R271 from 3.3V_RUN to 3.3V_ALW_R

080206 PG.25
add 22uF cap(C746) to 1.2V_PLLVDD_SATA. In parallel to C352

080206 PG.28
change U12 pin 22 from AUD_HP_NB_SENSE to AUD_HP_EN.
Add AND GATE(U38) on +5V_SPK_AMP. Inputs = (pin 1) AUD_HP_NB_SENSE,
(pin 2) AUD_NB_MUTE. Output (pin 4)= AUD_HP_EN

080206 PG.28
delete L44
Change AUD_VDD to +5V_SPK_AMP.
Change U12 pin 30 to +5V_SPK_AMP.

080206 PG.28
Nopop C420 C421, C422, C424

080206 PG.31
Delete PJP3
Add net name AUX_ON# to PQ2A pin 5
Add net name ENAB_3VLAN to signal at PQ2A pin3

080206 PG.31
Move BEEP form USI01 pin 78 to USI02 pin 69
Move 1.2V_RUN_ON from USI02 pin 98 to USI01 pin78

080206 PG.14
Add a 100K(R674) pulldown to DVI_DETECT at Q7 pin2

080206 PG.14
pop R229, Nopop R246

080206 PG.38
populate R490 and R491

080206 PG.39,47
Rename NC_ALW_PWRGD_3V_5V at PR91 to ALW_PWRGD_3V_5V
Connect ALW_PWRGD_3V_5V to USI02 pin 29

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080206
PG.39: Delete R519 and R520
PG.43: Delete D26,Q63,Q66,U35,C689,R616,R613,C693,R618,C691
PG.43: Change 1.8V_SUS_PWRGD at R607 to 1.2V_ALW_SUS_PWRGD, Delete U36 and C707, Connect U33B pin 4 to U31C pin 9, Delete 0.9V_DDR_VTT_PWRGD from circuit at U33A pin 1. Delete R609

080206 PG.45
change PC18 to 0.1uF. Populate

080206 PG.21
Add Fuse F2(0.12A_48V_NANOSMDC012F) between 5V_RUN and D3 pin 2

080206 PG.15
Delete L19

080206 PG.35
nopop C585

080206
Page 28: Move C444 to left side of R354 (Ver 0801).
Page 38 & 38: Move R359 to page 38.
Page 39 & 43: Delete 3.3V_LAN_PWRGD signal from USI02 pin 14, and delete the entire 3.3V_LAN_PWRGD circuit from page 43. (i.e. D26, Q63, Q66, U35)

0803 PG.24
Set SMB_ALERT# pull up, R271, as NoPop same as Becks

0803 PG.24
NoPop R263 and Pop R254,R255,R257 same as Beck(7/28)

0803 PG.28
R355 This resistor must connect to +3.3V_RUN
NoPop for Sigmatel codecs. Otherwise, there is a chance of backdriving the 3.3V rail through the codec.
So NoPop R355

0803 PG13
Add note "499 ohm resistors are placed at the same via as the series capacitors"

0803 PG25
Change R248 pullup from +3.3V_ALW to +3.3V_ALW_R.

0803 PG25
Follow below step to modify LDO circuit.
Step.1.Change C275 form 10U_6.3V_0805_X5R_NC to 2.2U_10V_0603_X5R_NC
Step.2.Change U37 form LM1117MPX-ADJ to TPS79601DCQRG4_NC
Step.3.Change R309 form 121_1%_NC to 1.37K_1%_NC
Step.4.Change R311 form)_NC to 66.5K_1%_NC
Step.5.Contact C275-pin1 and U37-pin2,3 to +3.3V_RUN
Step.6.Contact U37-pin3,6 to gnd
Step.7.Contact U37-pin4,R309-pin1,C747-pin1,C748-pin1 to +1.25V_SATA_VCC
Step.8.Contact U37-pin5 to R309-pin2 and R311-pin1 and C747-pin2
Step.9.Add C748 between +1.25V_SATA_VCC and gnd.

0803 PG21
Change pullup rail of R212 and R213 from +CRT_VCC to +5V_RUN_SYNC

0803 PG29
change R375 form 10K to 0 ohm per M08 Reference schematics

0803 PG32
change PCB footprint form "pci-1ca4c5ad1-jm-4f-68p"
to "PCI-1CA4C5AD1-JM-4F-68P-DX6" for CON5

0803 PG18
Follow below item to modify
Pin 'RP25.3' moved to net 'DDR_B_MA2'.
Pin 'RP25.1' moved to net 'DDR_B_MA4'.

0803 PG16
Pin 'RP3.1' moved to net 'MEM_A11'.
Pin 'RP3.3' moved to net 'MEM_A8'.
Pin 'RP2.3' moved to net 'MEM_A4'.

0803 PG17
Pin 'JDIM1.124' moved to net 'DDR_A_D32'.
Pin 'JDIM1.125' moved to net 'DDR_A_D33'.
Pin 'JDIM1.126' moved to net 'DDR_A_D37'.

0803 PG43
move R608 between R607pin 2 and R606 pin 2

0803 PG21
Add F1 PCB footprint in F2 for temp solution to layout.

0803 PG51
PQ59 is connected backwards. Pin 1 should connect to ground and pin 3 should connect to CHG_PBAT_N.
So swap PQ59-pin1 and PQ59-pin3

0803 PG40
Nopop C661 and C706
modify note :all C252 change to C661

0803 PG30,39
modify net(LOM_SMB_ALERT) and module port(LOM_SMB_ALERT) to net (LOM_SMB_ALERT#) and module port(LOM_SMB_ALERT#) in pg30 and pg39
Change R402 form pull up to +3.3V_LAN to pull up to +3.3V_ALW

0803 PG26
ADD BLM31PG121SN1L(L83) in schematic to SB VDD_[1:12] pins M13 to V17

0803 PG44
Delete H15,H18,H19,H20

0803 PG21
Change PCB footprint to "RC1206" for F2

0803 PG23
step.1 contact Q28-pin3 to R238 and Q75-pin2
step.2 add R675 between Q28-pin2 and net(CPU_PWRGD)
step.3 change R239 to 10K
step.4 contact Q75-pin3 to R239 and module port(CPU_PWRGD_Q)

0803 PG40
change Q73 and Q74 form MMST3904 to DDTA114EUA

0804 PG14
Modify PCB Footprint to CC0402 for C103

0804 PG15
Modify PCB Footprint to CC0805 for C131

0804 PG31
Change L56 form BLM11A601S_NC to BLM18AG601SN1D_NC
Because BLM11A601S is old P/N of Murata, So Murata request us to use new P/N

0804 PG29
Add R677 between L46-pin1 and C459-pin2
and add R678 between L47-pin1 and C460-pin2 in schematic

0804 PG29
Add a 0 ohm (R676) popped resistor at pin 3 of Q27 with a signal connection to DVI_SCLK and add note RS690 Revision A11 bring-up and qualification has identified an issue with the DAC_SCL pin
For A11:Pop R676 and Nonpop Q27,R204,R206
For A12:Pop Q27,R204,R206 and Nonpop R676

0804 PG.19
Nonpop R166,C266,Q12,R168 and modify note to "This unused thermistor circuit is located under the top memory module"

0804 PG.30
change R404 form 0ohm to 1K ohm

0804 PG.30
change R402 form contact to +3.3V_ALW to contact to +3.3V_LAN

0804 PG.10
No stuff JHDT1

0804 PG.14
Modify L6,L8,L9 PCB footprint form RC0603 to RC0402.(use cis item)

0807 PG.28
Change P/N form "AL009205B01" to "AL9205X5005" for STAC9205

0807 PG.19,39
Change R182 Input from 3.3V_SUS to 3.3V_RUN
Remove module port form USIO2-pin15 and U6-pin27

0807 PG.23
Add a 10K(R679) pulldown to SB_SPDIF_OUT_R signal. Nopop the resistor.

0807 PG.24
Move R272 pulldown from the SB_AZ_MDC_RST# signal to the SB_AZ_RST# signal. (pin K3)

0807 PG.25
add 20K(R680) Pulldown to WWAN_PCIE_RST# signal at U10B pin V5.
Per Beck's ATI feedback

0807 PG.14,25
Delete R301 and delete signal connection SB_NB_PCIE_RST# at U10B and U3C pin C10.
Rename signal NB_PCIE_RST# to NC_GPI056. (U10B pin V6)
Add 20K(R681) pulldown to NC_GPI056

0807 PG.39
Add 100K Pullupto 3.3V_ALW on USIO2 BC_DAT signal Pin 86. Pop resistor.
Add Note Under resistor "To support SIO BC Bus Speed Lower Speed.
Less than 12MHz"

0807 PG.30
Chage R402 from 100K to 4.7K

0807 PG.42
change PR17 from 100K ohms to 390K ohms

0807 PG.43
pop R608

0807 PG.43
Pop R590 and R591

0807 PG.38,39
Move 1.2V_RUN_ON pull down R538 to 5018 schematic page, since the net was moved to 5018.

0807 PG.38
Remove module port "wireless_on/off#" and net "wireless_on/off#" in USIO1-pin24

0807 PG.38
Remove module port "QBUFEN#" in USIO1-pin67

0807 PG.28,38
Change module port "AUD_NB_MUTE" to "NB_MUTE#" for Q36-pin2 and USIO1-pin77.
change Net "AUD_NB_MUTE" to "NB_MUTE#" in U38-pin2 and Add module prot "AUD_NB_MUTE" in U38-pin2

0807 PG.23
add option to disable CLKRUN#. Please add a populated 8.2k(R683) pull up to +3.3V_RUN and a no pop 10 ohm(R684) pull down to CLKRUN#. Place the components on the SB600 page. Add the comment: Option to "Disable" clkrun. Pulling it down will keep the clocks running.

0807 PG.17
Change P/N form "DGMK0003501" to "DGMK0005791" for JDIM1

080806
Page 28: Change footprint to QFN48-7X7-5-FM5 form LQFP48-9X9-5 for U13(STAC9205).

0808 PG.15
Change part form 0.01U to 0.1U CAP for C134,C135,C136,C145,146,C147,C148

0808 PG.25
Delete Net NB_PCIE_RST# and R321

0808 PG.25
Change U37 form TPS79601 to TPS72501

0808 PG.41
Remove Q53 and module port(LED_MASK#)

0808 PG.19
Add P/N:CS+2707J202 in R182

0808 PG.20
Add P/N:BC010U45Z06 in D3,D7

0808 PG.22
Add P/N:CH1300GKI08 in C315

0808 PG.36
Change Q45 form FDS4435_NL to FDS4435BZ.
Because FDS4435_NL will EOL in 2007 Q1.
And PN:change to "BAM44350097"

0808 PG.20
Change Q22 form FDS4435 to FDS4435BZ.
Because FDS4435 will EOL in 2007 Q1.
And PN:change to "BAM44350097"

0808 PG.30,35,41
Change P/N for C490,C499,C576,C577,C581,C583,C672 to CH3473K1B00.
Because vendor will not provide this materiel.

080806GC
Page 10, Single Net Issue, base on becks(7/28) to delete this
net(N52538896).
Page 32, Single Net Issue, net of CBS_CSTSCHG should be CBS_CSTSCHNG net
name and changed it.
Page 24 & 39, Single Net Issue, move R524 and net of HDT_RESET# to page 24
and also place them to close D11 (HDT_RESET# net) to fix issue.

0809 PG.14
add a note for resistors R476, R477 and R478 that
resistors should be placed close to NB.

0809 PG.23
Delete module port(PCI_PLOCK#) and net(PCI_PLOCK#).let U10A-pin AF6 NC.

0809 PG.21
Remove note "Setting R,G,B trace
impedance to 60 ohm." Because Impedance is not 60ohms.

0809 PG.30
Change R412 from 39 ohm to 39Kohm.

0809 PG.26
Refer to vendor suggest for 1.5uH 3A ferrite.
Change L83 form BLM31PG121SN1L to FBMJ4516HS111-T.
FBMJ4516HS111-T was 110 ohm@100MHz 4A DC 0.014ohm

081006GC
Page 40, Changed KB connector to ZIF and remove nets of SP_GND, SP_X, SP_Y
and SP_V+ on page 40.
Page 41, For SP's capacitors, C662, C663 & C664 on page 41, because we don't
use SP function, removed them together.

081106GC
Page 14:Added AC term at "CLK_HTREF_66M"and put them to close U3C's pin B23.
And also we will use value is 22_NC/22p_NC for AC term.

081206GC
Page 14: Add note: AC Term closely clock pin for length: 50 mils.

081406GC
Page 20: R193 is populated.

081406GC
Page 16 & 42: Changed the gate of Q9 to 1.8V_RUN_ENABLE instead of RUN_ENABLE
on page 16 and add one module port on net of 1.8V_RUN_ENABLE on page 42.

081406 PG 22
Change P/N of L30,L31,L32 form "CV+4701KZ07" to "CV+4701MZ00"

0814 PG 11
Change C50,C51,C52,C53 form "4.7u_10V_0805" to "10u 10V 0805 X7R"
But, it still have not P/N.

0814 PG 11
Change C33,C34,C35,C36,C37,C38,C39,C40,C41,C46,C47 form 22uF X5R to 22uF X6S
But, it still have not P/N.

0814 PG 11
Change C63,C64,C65,C66 FORM 4.7uF X5R TO 4.7uF X7R
But, it still have not P/N.

0814 PG 17
Change C181,C183,C207,C209 FORM 2.2uF X5R TO 2.2uF X7R

0814 PG 08
Change C19,C20 FORM 0.22uF X5R TO 0.22uF X7R

0814 PG 08
Change C16,C17,C18 FORM 4.7uF X5R TO 4.7uF X7R
But, it still have not P/N.

0814 PG 10
Change C26 FORM 4.7uF 6.3V 0603 X5R TO 4.7uF 10V 0805 X7R
But, it still have not P/N.
C27 form 0.22uF X5R to 0.22uF X7R

0814 PG 11
Add P/N "CH6221MEA01" in C33,C34,C35,C36,C37,C38,C39,C40,C41,C46,C47

081606GC
Page 19: Changed net name from THERM_VEST to THERM_VSET.
Page 31, 35 & 42: Changed net linking from 5V_ALW to 5V_ALW2 for PR1, R469,
PR4, PR16, and PR6.

081706GC
Page 17: Changed footprint to CC0603 from CC0805 for C181, C183, C207 & C209.

081806GC
Page 43 & 49: The signal of 1.2V_ALW_SUS_PWRGD is pulled up by R606 with
+3.3V_ALW on page 43, and PR132 is duplication, so we deleted PR132 on page
49.
Page 32: Changed footprint to lqfp128-16x16-4-129p-jm7 from
LQFP128-16x16-4-JM6 for U20(OZ711) on page 32. Changed requested by Dell: we
should try to implement the OZ711 revC stepping Ground pad for the OZ711. It
looks like we will have to switch to it for M08 platforms anyway.

082306GC
Page 11: For CPU power decoupling issue (RR-5-20), added
C292/22uF/0805/X6S/6.3V on +VCC_CORE and added C566/22uF/0805/X6S/6.3V on
+1.8V_SUS, two parts are nopop.

			
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082406GC
Page 37: Delete U27. There is not need for this option since 16Mb and 8Mb parts are available in the 200 mil S08 package.
Page 19: Changed R635 to no pop. "LDO_SET connected to GND for 2.5V out, or connect external divider for variable output voltage".
Page 31: Changed the comment above Q72 to read Design Current: 640.15 mA, Max Current: 914.5 mA from Design current: 1466mA, Max current: 3664mA.
Page 24: Changed R254, R255, R257 to no pop.

082506GC
Page 49 & 39: Because this pullup resistor (PR133) is used for net of NB_VCORE_PWRGD, it should be closed to I/P pin of MEC5025 (pin37), so I want to delete PR133 and reserve pullup resistor (R688 link to +3.3V_RUN) on page 39 to closed to I/P pin of MEC5025 (pin37).
Page 39 & 48: Remove 0.9V_DDR_VTT_PWRGD net of MEC5025 pin 73 (GPIOA3) and nopop PR101.

082606GC
Page 17: C185-C194 need to be changed back to 2.2 uF 0603. This bulk capacitance is needed per the reference design.
Page 18: Populate stitching caps C244, C245, C248, C251, C252, C254, C258, C259.
Page 30: Delete R391 and C485. No need for AC term on an unused clock.
Page 23: Change R684 to 8.2k_NC.
Page 28: Need to add a .1uF cap (C600) from U38 pin 5 to ground. Follow Becks and M08 Audio reference.
Page 39: Populate R551. Follow Becks.
Page 41: Delete R587, it is a duplicate.
Page 43: Populate Q54. Follow Becks.

082906GC
Page 25: Delete R658 and C725 (GGIL376), Delete R659 and C728 (GGIL377).
Page 21: Changed C303 and C304 to nopop. (GGIL 384).
Page 47: Changed PR81 to nopop. (GGIL 385)

083006GC
Page 44: Changed footprint to h-c197d63p2 from H-C197D114P2-4 for H1.

083106GC
Page 24: Populate R281, R284. No pop Q29, Q30, R277, R278.
Page 43: No pop R590.
Page 38 & 39: Move DOCK_SMB_PME# from MEC5025 SGPI037 to ECE5018/5011 GPIOC0. Move DOCK_SMB_ALERT# from the ECE5018/5011 GPIOC0 to MEC5025 SGPI037.
Page 17 & 22: Connect R218 Pin 2 to U3 NB DFT_GPIO5 (pin A8) through a FET Controlled by PLTRST_SYS#. See file SVID_vs_component.jpg, on the FTP site, and sent in email.

090106GC
Page 42: Changed to SI4336DY from FDS8880_NL for PQ19.
Page 7: Changed C722 from 0.47uF (0603) to 0.047uF (0603), Changed C723 from 0.47uF (0603) to 0.047uF (0603), Changed C724 from 0.47uF (0603) to 0.047uF (0603) for EMI requested.
Page 52: Added 0.1uF for stitching cap for +3.3V_RUN to GND for transition on page 52.
Page 32: Connect CON5.85-88 to GND and CON5.69-84 to GND too.

090706GC
Page 39: Changed to 2.7K from 100K for R189, R187, R181.

091106GC
Page 47: Changed to 0 from 0_NC for PR164.

092706GC
Page 43: Changed P/N to 0 from 100K for R276 to fix LDT_RST# Issue.
Page 43: Changed P/N to BCRB751SZ11(SOD-523) from BC000751Z05 (SOD-323) for D10, D12, D13, D14 & D15.
Page 24: Changed D29 to NC to fix can't boot issue.
Page 43: Changed to CS41002JB20(100K) from CS31002JB28 (10K) for PR118.

092706 W
page 34 : Change location form J6 to J12 for MDC_NUT to fix double J6 issue

092806 W
page 34 : Change location form J12 to MDC_NUT1 for MDC_NUT to follow Gordon command

092806 W
page 49 : modify module port "1.5V_RUN_PWRGD" form input module port to output module

092806 W
page 43 : Add function code and Subsystem ID in R276

102706 W
page 15 : Change C504 from CH4103K9B09 to CH4103K1B08 (form X5R to X7R) to meet derating criterion.

102706 W
page 50 : Change PC31 from CH5472K9A02 to CH5472KEA07 (form X5R to X6S) to meet derating criterion.
page 26 : Change C353 from CH6222M4A00 to CH6221MEA01 (form Y5U to X6S and form 10V change to 6.3V) to meet derating criterion.
page 26 : Change C695 from CH6221M9A07 to CH6221MEA01 (form X5R to X6S) to meet derating criterion.
page 26 : Change C688,C689,C701,C702 from CH5101K9B01 to CH5102KE901 (form X5R to X6S and from 0402 to 0603 and from 6.3V to 10V) to meet derating criterion.
page 24 : Change C358 from CH6222M4A00 to CH6221MEA01 (from Y5U to X6S and from 10V change to 6.3V) to meet derating criterion.
page 25 : Change C707 from CH5101K9B01 to CH5102KE901 (from X5R to X6S and from 0402 to 0603 and from 6.3V to 10V) to meet derating criterion.

102706 W
page 14 : Change C478 from CH5101M9B02 to CH5102KE901 (from X5R to X6S and from 0402 to 0603 and from 6.3V to 10V) to meet derating criterion.

102706 W
page 15 : Change C479,C482,C490,C496,C498 form CH5101M9B02 to CH5102KE901
(from X5R to X6S and from 0402 to 0603 and from 6.3V to 10V)
to meet derating criterion.

102706 W
page 23 : Change C378 from CH5101M9B02 to CH5102KE901
(from X5R to X6S and from 0402 to 0603 and from 6.3V to 10V)
to meet derating criterion.

102706 W
page 24 : Change C361 from CH5222K9907 to CH5222K1906
(from X5R to X7R) to meet derating criterion.

102706 W
page 16 : Change C508 from CH5222K9907 to CH5222K1906
(from X5R to X7R) to meet derating criterion.

102706 W
page 51 : Change PD8,PD10 from BC000032Z09 to BC0ES3BBZ00
(from UBM32PT to ES3BB-13-F) to meet DELL PSL.

103106GC
page 45 : Change PD2 from BC000204Z21 to BC000099034
(from CH204UPT to DA204U) to meet DELL PSL.

102706 W
page 48 : Change PD9 from BC000501Z09 to BCBAT165Z08
(from CH501H-40PT to RB500V-40) to meet DELL PSL.

102706 W
page 46 : Change PD19 from BC000501Z09 to BCBAT165Z08
(from CH501H-40PT to RB500V-40) to meet DELL PSL.

102706 W
page 47 : Change PD21 from BC000501Z09 to BCBAT165Z08
(from CH501H-40PT to RB500V-40) to meet DELL PSL.

102706 W
page 39 : Change W1 from BG332768909 to BG332768381
to meet DELL PSL.

102706 W
page 23 : Change Y2 from BG332768909 to BG332768381
to meet DELL PSL.

102706 W
page 32 : Change Y1 from BG624576431 to BG624576155
to meet DELL PSL.

102706 W
page 33 : Populate C12-C19 to solve EMI - 601.4MHZ off 14.318MHZ clk at RS690T

102706 W
page 41 : Add 0.1u cap C743-C748 to solve EMI - 601.4MHZ off 14.318MHZ for BT.
C743 need to close as possible to J2.3
C744 need to close as possible to J2.2
C745 need to close as possible to J2.4
C746 need to close as possible to J2.5
C747 need to close as possible to J2.6
C748 need to close as possible to J2.7

102706 W
page 35 : Add 0.1u cap C749-C752 to solve EMI for WLAN.
C749,C750 need to close as possible to J9.3
C751,C752 need to close as possible to J9.5

102706 W
page 28 : Modify C288-C291 from 100pf to 10pf and pop them
to solve WAND test - Speaker appear noise.

102706 W
page 50 : Modify PR29,PR36 from 0 ohm_0603 to 2.4 ohm_0805
to solve 48.9MHZ & 105.81MHZ B.B. noise.

103106GC
page 47 : Change PD11,PD12 from BCBAT54SZ39 to BCBAT54CZ88
to meet DELL PSL.

110106GC
page 51 : Change PD16,PD17,PD18 from BC000715Z09 to BC70SB45Z04
to meet DELL PSL.

110106GC
Page 43 : Change D10,D12,D13,D14,D15 from BCRB751SZ11 to BC000340033
to meet DELL PSL.

110106GC
Page 37 : Change D27 & D28 from BC000751Z05 to BC000340033 to meet DELL PSL.

110106GC
Page 32 :
1. Ref resistor, R220 change from 6.2k to 5.9k.
2. Cap C217 for TPB0- to GND, Change from 820pF to 270pF
3. The following schematic note should be added next to pin 129: "Ground
pin129 exposed die pad, dimension 5.72mm x 5.72mm, should connect to PCB
solder pad of same dimension."

110106GC
Page 27 & 38 :
HDDC_EN, and MODC_EN routing.
Page 23 & 30 :
Connect signal CLK_PCI_TPM from the SB resistor R356 to U29.J8.
Page 30:
TPM resistor change (Nopop) delete R53.
Add 33ohm(R649) in series with a 22pF(C753) termination to the CLK_PCI_TPM signal
at the LOM chip. Nopop the components.
Connect signal CLK_PCI_TPM from the SB resistor R356 to U29.J8
Page 35:
WLAN SMBUS. Depop Fets
depop Q34 and Q35
Page 29:
Swap HP and Mic jacks
Swap locations for these components on PWB. CON3 and CON4.

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110106GC
Page 48:
+1.8V source voltage change from +5V_SUS -> +5V_ALW
Change PU6 power source rail at PR105.2 / PD9.2 from +5V_SUS to +5V_ALW. Need to confirm with Power team if this was mocked up and tested.
Page 23:
connect FERR to +1.8V_RUN.
Change R358 connection from +1.8V_SUS to +1.8V_RUN.
Page 49:
Inductor change on 1.2V 3.3uH to 4.7uH (CV-47A0MZ19) lower Freq on 1.2VALWSUS. Change freq.
Change PL2 to 4.7uH/ CHOKE-MPL73-1R5 and PR3 is pop, PR2 is depop for lower frequency.

110106GC
page 15 : Change C495,C497 from CH6101M9905 to CH6100KMEE3 (from X5R to X6S) to meet derating criterion.

110106GC
page 15 : Change PC71 from CH6102M9A01 to CH6102K1A00 (from X5R to X6S) to meet derating criterion.

110306 W
page 30 : Add Function Code and Subsystem ID for C753 and R649

110306 W
Page 20 : Change D24,D25 from BCRB751SZ11 to BC000340033
Page 26 : Change D30 from BCRB751SZ11 to BC000340033
Page 19 : Change D26 from BCRB751SZ11 to BC000340033 to meet DELL PSL.

110306 W
Page 14 : Change D23 from BCRB751VZ16 to BC000340033
Page 24 : Change D29 from BCRB751VZ16 to BC000340033 to meet DELL PSL.

110306 W
Page 35 : Change D16 from BCRB751SZ02 to BC000340033 to meet DELL PSL.

110306 W
Page 19 : Change D11 from "" to BC000340033 to meet DELL PSL.

110706GC
Page 16 : The side port memory (U6) we use is 256Mbit 350MHz. It can't meet PFG. So, we need to change to 256Mbit 400MHz, and P/N need to change from AKD5JG-TW39 to AKD5JG-TW12 (HY5PS561621AFP-25).

110606 W
Re-change D10,D11,D12,D13,D14,D15,D16,D23,D24,D25,D26,D27,D28,D29,D30 to meet DELL's PSL
Page 14 : Change D23 from BC000340033 to BC0RB751Z01
Page 19 : Change D11,D26 from BC000340033 to BC0RB751Z01
Page 20 : Change D24,D25 from BC000340033 to BC0RB751Z01
Page 24 : Change D29 from BC000340033 to BC0RB751Z01
Page 26 : Change D30 from BC000340033 to BC0RB751Z01
Page 35 : Change D16 from BC000340033 to BC0RB751Z01
Page 37 : Change D27,D28 from BC000340033 to BC0RB751Z01
Page 43 : Change D10,D12,D13,D14,D15 from BC000340033 to BC0RB751Z01

110606 W
Page 35 : Change P/N from DA0JX6MB8A5 to DA0JX6MB8B0 to Rev. B for PCB board.

110606 W
Page 35 : In order to align with Becks, the following changes have to be made to fix EMI - 250MHz Issue related to LAN @ 1Gbps (Tyco RJ Mag) System fails at 250MHz.
1) Populate C430 and C431 in page 31
2) Depop R403 and populate L51 in page 31
3) Change L7, L9, L10, L11, L14, L15, L17 and L23 from 24nH to 36nH (P/N from "CVA2407JN01" to "CVA3607JN01")

110706GC
Page 30: Due to the PCB footprint size on location U30 is wrong in CIS, so change U30 to S08 from SOIC8.
U31's footprint is right, don't change it.

110706GC
Page 32: Mechanism enlarge 3 ground pad on Pcmcia screw tab.Location are c1,d2,and d3. Cardbus cage will modify in the same time.
So change footprint to PCI-1CA4C511-JM-4F-68P-JX6 from PCI-1CA4C5AD1-JM-4F-68P-DX6 on CON5.

110706GC
Page 41: Mechanism change T/P connector P/N from DFHD10MSB82 to DFHD10MS000(with align pin).
So change part to DFHD10MS000 from DFHD10MSB82 on JP1.

110806GC
Page 35:
For WLAN SMBUS.
NoPop pull up resistors, R297 and R298, also.

110806GC
Re-change D10,D11,D12,D13,D14,D15,D16,D23,D24,D25,D26,D27,D28,D29,D30 to BC000340033 to meet DELL's PSL
Page 14 : Change D23
Page 19 : Change D11,D26
Page 20 : Change D24,D25
Page 24 : Change D29
Page 26 : Change D30
Page 35 : Change D16
Page 37 : Change D27,D28
Page 43 : Change D10,D12,D13,D14,D15

110906GC, Because didn't get approval from Dell, so restore.
Page 48:
1. +1.8V source voltage change from +5V_ALW -> +5V_SUS
Change PU6 power source rail at PR105.2 / PD9.2 from +5V_ALW to +5V_SUS.
2. Delete C754.
3. PR96 change from 63.4K_0402 to 100K_0402.
4. 1.8V_SUS_PWRGD and 0.9V_DDR_VTT_PWRGD should also be pulled up to +3V_SUS.
Page 46: PR114 and PR125 change from 0.01_2512 to 0.01_3720.
Page 49: PR3 depop, PR2 pop.

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111006GC:
Page 29
C749, C750, C751, C752 are too far away from J9
in the layout with long stubs. Delete J10 from the schematic

111006W
Page 47
For system power regulator schematic change
1. change PR179 from 154k to 143k, PR172 from 178k to 100k
to adjust current limit setting.
2. change PL8 from SIQH125A-2R2 to HMP1340-4R7
3. depop PR164 to set 3V regulator switching frequency to 300kHz.
4. add a 0_0402(PR192) resistor from PU9.29 (skip#) to GNDA_3V5V
for optional ultrasonic mode per ref. schematic rev. A04
5. schematic clean-up: 5V rail max current=8.55A, TDC=6A;
3.3V rail max current=5.95A, TDC=4.2A

111006 GC
SCH X01 - DDR power regulator schematic change
Description: Description
A 4000 character field providing additional information that further
describes the issue; typically more detailed information than Title.
X00-090706 page 48:
1. change PR96 from 100k to 63.4k to adjust current limit setting
2. add a 0.01uF(C759) cap from PU6.16 (OUT pin) to GND_DDR per ref.
3. schematic clean-up: 1.8V rail, max current=13.2A, design current=9.24A

111006 GC p.28
add a 0 ohm series resistor (R651,R652)(Pop resistor) and
100pF capacitor (C754,C755)(NoPop cap) to ground for each
signal AUD_EAPD (pin 47 of U16) and AUD_SPDIF_OUT (pin 48 of U16)

111006 GC
Remove TPM PU
p.30
Delete R53, PU for CLK_PCI_TPM. This resistor is not required since
we have added TPM as a feature to our system

111006 W
p.33
Add a fuse(F2) and bypass jumper(PJP20) for the power input of U1,
the USB power switch. Circuit should be copied the same as PJP11 and F1

111006 W
p.25
Change pull up power plane for R605, R602 and R594 from 3.3V_ALW to 3.3V_RUN.

Add a table with the following information on the schematic page:

Memory Vendor	LBF_ID1	LBF_ID0	LBF_ID2
	0	0	0 - 32MB
Qimonda	0	1	1 - 64MB
Samsung	1	0	

111006 GC
Add errata items for STA9205 Codec
p.28
at pin 40 of U16, Codec, add a 100k ohm(R654) series resistor.
at the pin 40 side of the resistor, add a 1000pF(C756) capacitor to GND.
Pop both components.

111006 W p.42
Change PQ25 control signal from RUN_ON_5V# to SUS_ON_5V#.

111006 W p.46
Add a 470pF(C757) capacitor to GND at node +VCHGR_B. Nopop the capacitor.

111006 W p.40
1.Change Q8 from DDTA114YUA to 3906 part
2.Change input power to transistor from 3.3V_ALW to 3.3V_RUN
3.Add a 47k(R655) PU resistor at the base of Q8 with a power plane connection
of 3.3V_WLAN
4.Add a 10k(R656) series resistor from the base of Q8 to the signal LED_WLAN_OUT#
Same as Becks

111006 W
1. Delete Node name "+3.3V_ALW2" from node PU1 pin 7. Page 49
2. Delete PR168, page 47
3. Add a 0.1uF capacitor 0402(C758) from PU9 pin 5 to "GNDA_3V5V". Page 47
4. rename PU9 pin 5 as "+3.3V_ALW2"
refer to WI102939 for more information.

111006 GC
Delete WLAN SMBUS Switch Bypass Resistors
page .35
Delete R285 and R286
Remove signal traces. (MEM_SCLK, and MEM_SDATA stubs going to R285 and R286))

111006 GC
Page 21
Move CRT Fuse and NoPop
move FS1 to be parallel with R391. No pop FS1. Change to make circuit same as Becks.

111006 GC
Page 28
To fix the audio buzz issue the following modifications have to be done:
1) Populate C288, C289, C290 and C291 with 100pF caps.

111006 W
Page 46
Populate PR98 to enable the UL circuit

111006 W
p.46
Populate PD13 and PR126 per power team.

111006 W
Page.30
Change filters for 2.5V_LOM, L8, L21, L13,
from BLM18AG601SN1D to BK1608LM182,
same as Becks

111306 GC
Page 37
Change U10 form "M25P80-VMW6TG" to "M25P16-VMW6TG" to support TPM

111006 GC
Page 28
Change R301 from Pop to NoPop same as Becks.

111006 GC
Page 45
No pop PR51 and PR182, series resistors for NC_SBAT_ALARM#
and NC_PBAT_ALARM# signals. These signals are no connect signals
so series resistor does not have to be populated.

111006 GC
Page 49
add a note to PC3: populate PC3 with 0.01U_16V with ISL6236;
populate PC3 with 1uF_16V with Max8778

111006 W
Page 49:
1. schematic clean-up: 1.2V_ALW_SUS rail, max current 3.3A,
design current=2.3A
2. depop PR2 and pop PR3 to set the switching frequency to 200k/300kHz
3. change PR11 from 169k to 158k, change PR13 from 150k to 143k
to adjust current limit setting.
4. change PL2 from MPL_3R3_6A to MPL73_4R7_5.5A

111006 W
Page 20
Page It is due to noise coupling onto the BACKLITEON_R net
on the LCD connector and upsetting the RS690T.
Depop 1) R468 2) Q60 3) R462

111006 GC
Page 45
Populate DA204U TVS Diodes on PD20, PD22, PD23 and PD24

111206 GC
Page 45
Non-Populate DA204U TVS Diodes on PD20 for DELL request

111006 W
Page 23.
Populate CPU_PWRGD level shifter. R369, R370, Q43, Q44, R367

111006 W
Page 23.
Populate R623 (IGNNE# PD), NoPop R358 (FERR# PU)

111006 W
Page 19
Changed R165 from 12.1k to 40.2k, same as Becks

111006 W
Page 24
Change SIO_EXT_SMI# PU (R340) and SIO_EXT_SCI# PU (R336) from pop to NoPop.
Same as Becks
Change IDE_RST_MOD PD (R599) from pop to NoPop. Same as Becks.

111006 W
Page 34
Change SB_AZ_MDC_RST1# PD, R405 from 100k to 10k, same as Becks

111006 W
Page 37
Change R191 from 4.7k to 100k, same as Becks.

111006 W
Page 19
Populate all VCP2 circuit components.
R256, R260, C265, Q25, R243.

111006 W
Page 50
PC129, PC26, PC139 and PC140 on page 50 is out of spec on thermal test
PC129, PC26, PC139 and PC140 on page 50 change from X5R to X6S.

111006 W
Page 31
System fails at 250MHz. The emission is related to the Tyco RJ Mag.
Two systems were tested, both with Tyco RJ Mags. One system had a -10dB margin,
the other system had a failure at +0.3dB over the legal limit.
When disconnecting the LAN cable the emission goes away completely.
1) Populate C430 and C431
2) Depop R403 and populate L51
3) Change L7, L9, L10, L11, L14, L15, L17 and L23 from 24nH to 36nH

111406 W
Page 38
Change value form ECE5018 to ECE5028 for USI01

111506 W
Page 21
Change P/N from "BC000204Z21" to "BCDA204UZ09
" for D18, D19,D20 to meet DELL AVL
Page 22
Change P/N from "BC000204Z21" to "BCDA204UZ09
" for D1,D2,D3 to meet DELL AVL
Page 45
Change P/N from "BC000204Z21" to "BCDA204UZ09
" for PD1,PD4,PD5,PD6,PD7,PD20,PD22,PD23,PD24 to meet DELL AVL

111506 W
Change P/N from AJ007110F18 to AJ007110F26(Rev.C)for U12 (0Z711EZ1)
Change P/N from AL002532C03 to AL002532C11(Rev.C) for U18 (0Z2532)
Change P/N from AL9205X5005 (rev.B1)to AL9205X5013(rev.B2) for U16 (STAC9205)
Change P/N from AJA11FG0T34 to AJA12FG0TQ2 for U5(RS690T)
Change P/N from AJA13FG0TD0 to AJA21FG0T02 for U23(SB600)
to clear Rev. issue

111606 W
Modify Below items from lead part to Lead free part.
Page 46
Change P/N from CS21003F904 to CS21003F947 for PR126.
Page 40
Change P/N from CS51002JB05 to CS51002JB21 for R210.
Page 18
Change P/N from CS15102JB02 to CS15102FB19 for R484,R497.

11??06 GC
Page 37
R191 have to be nonpop
Page 35
C750 and C752 have to delete.

111606 W
Page 37
Change U10 from "M25P80-VMW6TG" to "SST25VF016B-50-4C-S2AF"
P/N from "AKE38ZP0600" to "AKE28FP0K07"

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111706 W
Page 47
Change PL8 from HMP1340-4R7 (CV-4790MZ00) to HMU1356-4R7 (CV-47A0MZ02).
Because vendor can't provide immediately in B2A build.

112006 W
Add function Code and Subsystem ID in below items
C757, C758, C759, R655, R656, L81, L82

121406 W PG.43
Pop R282 and Nonpop R281
Dell change from "+3.3V_RUN" plan to "+3.3V_SUS" plan to generate RUNPWR0K.

121406 W
PG.48
Change PD9 form BCBAT165Z08 to BC010K45004 (from RB500V-40 to SDM10K45-7-F)
PG.46
Change PD19 form BCBAT165Z08 to BC010K45004 (from RB500V-40 to SDM10K45-7-F)
PG.47
Change PD21 form BCBAT165Z08 to BC010K45004 (from RB500V-40 to SDM10K45-7-F)
Because we can't receive RB500V-40 on time for JX6 PT-build.

121406 W
PG.23
Non-pop Q43.Because CIS provide wrong footprint to us.
So, we inverted Q43-pin2 and Q43-pin3.This issue is hard to fix
in SMT product line.So we nonpop Q43 and get dell approve.

121406 W
PG.21
Pop Q2,R11,R8 and Nonpop R13
RS690 Revision A11 bring-up and qualification has
identified an issue with the DAC_SCL pin
For A11:Pop R13 and Nonpop Q2,R11,R8.
For A12:Pop Q2,R11,R8 and Nonpop R13.
In this time we use A12.

121406 W
PG.24
Nonpop R600 for SB600 A21.

121406 W
PG.25
Nonpop R347 for SB600 A21.

121406 W
PG.46
Change PR76 form "CS41052FB04" to "CS11022FB13", from 105 ohm to 102 ohm
for temp solution.Because, we have not P/N of 105 ohm 0402 in Quanta.

121406 W
PG.36
Remove module port "DOCK_DET#" in J11-pin S137.
Because this net have not contact to other page.

121506 W 3A
PG.23
Re-load Q43 from CIS to clear wrong footprint issue and pop it.

121506 W
PG.32
Change U12 from "AJ007110F26" TO "AJ007110F01" and from Rev. C to Rev. D

121506 W
PG.38
Pop R213,R204 and non-pop R205,R212
Change board ID from "001" to "010" for ENG3(X02)

121906 W
PG 28
Remove module prot "NB_MUTE#" on Q36-pin2 and add NET "NB_MUTE#" on Q36-pin 2

122006 W
PG 17
Modify note
From
"Place C181 2.2uF and C182 0.1uF <500mils from DDR connector"
To
"Place C635 2.2uF and C628 0.1uF <500mils from DDR connector"
From
"Place C183 2.2uF and C184 0.1uF <500mils from DDR connector"
To
"Place C275 2.2uF and C284 0.1uF <500mils from DDR connector"
From
"Note:
Place C185-C189 and C195-C198 close to JDIM1
Place C190-C194 and C199-C202 close to JDIM2"
To
"Note:
Place C280,C277,C624,C626,C623 and C632,C631,C337,C634 close to JDIM1
Place C281,C625,C627,C279,C278 and C338,C339,C633,C340 close to JDIM2"

122106 W
PG 22
Change S-Video connector(JTV1) from SMT type to DIP type,
footprint from"030006FB007S100XU-7P-H" to "SV-MH1177L-BG5N-7F-7P-V"
122506 W
P/N: from "DFMD07FR346" change to "DFMD07FR007"

122106 W
PG 13
Change cap footprint from Circle type to Square type,
footprint from"CC0402-C" to "CC0402" for C83-C92,C94,C96

122106 W
PG 46
Change PR76 from 102 ohm to 105 ohm .
This modify clear "we have P/N for 105 ohm 0402 size in Quanta" issue.
P/N from "CS11022FB13" change to "CS11052FB00"

122506 W
PG 30
Change P/N from normal P/N to win B/S P/N.
Change from "AJ057550T05" to "AJ057550T00"

122506 W
PG 37
Remove note "111306GC: U10 need to change to M25P16 (16Mb)"

122606 W
PG 46
To clear Bit issue :DF112036
Audible noise during battery charging.
Popular PC112 and change PC110, PC111 and PC112
from "CH6104KE201" to "CH6104K9207", from X6S change to X5R.

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122706 W
PG 25
Remove "RTC_CLK" option in "REQUIRED STRAPS" table

122706 W
PG 16
For Roger request, Change footprint for U6
from "PBGA84-SAMSUNG-K4N51163QC-ZC" to "PBGA84-SAMSUNG-K4N51163QC-JX6"

122706 W
PG 34
Change MDC connector from Tyco to Foxconn,
P/N from "DFHS12FS386" to "DFHS12FS548"

122706 W
PG 32 WI112230
According to TXC test report, they suggest us modify below items.
Change C219,C220 from 12pF to 15pF
P/N from "CH01206JB05" to "CH0156K0B06"
PG 7
Change C584,C588 from 22pF to 33pF
P/N from "CH02206JB08" to "CH03306JB04"

010307 W
PG 50 WI112475
PC128 and PC142 are measured 80 degrees
that exceed standard temperature de-rating for 80%.
So we need to modify PC142 and PC128 from Y5V to X7R
P/N from "CH4104Z3B07" to "CH41006K911"

010307 W
PG 10 WI113406
Change R85,R499,R88 from 10K to 680 ohm.
From "CS31002JB28" change to "CS16802JB27"
And add D31,R668,R667,R666,U35,C760,R669 to follow Beck for delay current

010507 W
PG 50 WI112641
PC137 are measured 78.8 degrees to exceed temperature de-rating for 80%.
So we need to modify PC137 from X5R to X7R
P/N from "CH5222K9907" to "CH5222K1906"

010507 W
PG 19 WI113399
Change R256 from "+3.3V_SUS" to "+5V_SUS"
To follow Beck to fixing BIOS report wrong temperature on Bottom
SODIMM

010507 W
PG 39 WI113420
Add pull down resistor R672 1K ohm at USIO2-pin 15 to follow Beck
to determine the chipset ID. And no-stuff it.

010507 W
PG 13 WI113432
Change R73-R76,R454,R452,R465,R460 from 499 ohm to 750 ohm.
P/N from "CS14992FB24" change to "CS17502FB19"
This modify is follow Beck to change DVI termination resistor value

010507 W
PG 13
Change note from
"Layout Note :499 ohm resistors are placed
at the same via as the series capacitors"
to
"Layout Note :750 ohm resistors are placed
at the same via as the series capacitors"

010507 W
PG 37 WI113425
Change R562 from 1K ohm to 390 ohm.
P/N from "CS21002JB34" change to "CS13902JB14"

010507 W
PG 28 WI113449
Add 1M ohm resistor(R670) on U20-pin 10 to gnd.
To follow Beck to improved HP pop performance.

010507 W
PG 28 WI113452
Add 10K ohm resistor(R671) on net "AUD_EAPD" to gnd.
To follow Beck to keeps speaker disabled during S3/S4 transitions.
Performance with MSFT UAA Class driver still needs to be confirmed.

010507 W
PG 38 WI113457
Modify Net "BID2" to "CHIPSET_ID1" on USIO1-pin 112 and between R198 and R199.
To follow BECK.

010507 W
PG 35 WI113465
No-stuff C644 and Pop C274.
when we open the system,the surge current will be find in +3.3V_WLAN
and hung up system.
To clear surge current issue.

010507 W
Page 47 WI113465
Change PL8 from HMP1340-4R7 (CV-4790MZ00) to HMU1356-4R7 (CV-47A0MZ02).
For DELL request.

010807 W
PG 47
Re-load PL8 from CIS.

010807 W
PG 39
Modify net name from "CHIPSET_ID" to "CHIPSET_ID0" on USIO2-pin14
and R169-pin 1.
Add table in PG 38.

010907 W
PG 49
Pop L81,L82 and Non-pop PJP1,PJP2
For DELL request to clear EMI issue.

010907 W
PG 26
Correct C655 from 22uF 10V Y5U 0805" to 22uF 6.3V X5R 0805"
P/N from "CH6222M4A00" correct to "CH6221M9A07"
PG 23
Correct C684 from 22uF 10V Y5U 0805" to 22uF 6.3V X5R 0805"
P/N from "CH6222M4A00" correct to "CH6221M9A07"

010907 W
PG 10
Modify Note from "NOTE: R67 and C29 close to JCPU pin F10"
to "NOTE: R499 and C564 close to JCPU pin F10"
And from "NOTE: Place R72 on the top of the board that is iaccessible,
and that shorting across this resistor will toggle
the hyper Transport reset signal."
to "NOTE: Place R88 on the top of the board that is iaccessible,
and that shorting across this resistor will toggle
the hyper Transport reset signal."

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010907 W
PG 12
Correct Note from "Place R101 < 100 mils from U3A.C25 and U3A.D24"
to "Place R450 < 100 mils from U5A.C25 and U5A.D24"

010907 W
PG 39
Add R673(no-stuff) between net "CHIPSET_ID0" and ground
to rsvd for "CHIPSET_ID0" select used.

010907 W
PG 17 WI113303
Change C280, C277, C624, C626, C623, C281, C625, C627, C279, C278
from "2.2uF 6.3V 0603 X5R" to "2.2uF 10V 0603 X7R"
P/N from "CH52201K991" change to "CH5222K1906"

011007 W
PG 40
NC JKB1-pin33
For DELL request.

011007 W
PG 19
Change P/N from "AL004001003" to "AL004001011" for EMC4001 to Rev.B

011007 W
PG 22
Add two pin for JTV1 part(schematic library).
Modify JTV1 part to meet pcb footprint.

011007 W
PG 28
Change P/N from "CH3330CK218" to "CH333CK1202" for C654,C653
to clear ROHS issue

011007 W
PG 21 WI114268
No-stuff R11,Q2,R8 and Pop R13
For DELL request to modify back to X00

011007 W
PG 22
Re-load JTV1 from CIS.

011107 W
PG 46
For DELL request to no-stuff PR98

011107 W
PG 10
Reload U35 from CIS to clear temp issue.

011107 W
PG 35
Del R297,R298,Q34,Q35,
PG 24
Pop Q41,Q42,R317,R325. Del R318,R324.
Add Net "SB_SMBCLK0" on U10D-pin C27.
Add Net "SB_SMBDATA0" on U10D-pin B28.
For DELL request to add SMBUS option, and modify SMBUS current

011107 W
PG 45
For DELL request to add FL5 for dual layout
to option two inductance or one chock.

011107 W
PG 50 WI113908
For DELL request to change PQ48, PQ51, PQ53 and PQ54 from IRF7821 to SI4386DY.
P/N from "BAM78210034" to "BAM43860000"

011107 W
PG 31 WI114390
Change R376 from 150ohm change to 110ohm
and R378 from 150ohm change to 200 ohm.
For DELL request to get the optimum mix of orange & green on Lan connector

011107 W
PG 31 WI114680
For DELL request to improve IEEE characteristic and EMI improvement.
Replace and pop R412,R413,R409,R410,R419,R426,R417,R418 to 2K ohm
Pop C447,C446,C448,C455

011207 GC from AMD PA_SB600AQ2's recommendation and get Dell's agreement.
Page 24
Pull-up R653/2.2K_NC to +3.3V_ALW_R on SB_SMBCLK0 and R650/2.2K_NC to
+3.3V_ALW_R on SB_SMBDATA0.

Page 35
Delete dangling net on WLAN_SMBCLK and WLAN_SMBDATA in schematic, and also
delete all of the traces on layout.

011207 W
PG 24
Rename R653 to R678 ,R650 to R679.

011207 W
PG 10
Reload U35 from CIS to clear temp issue,again.

011207 W
PG 50
Reload PQ48, PQ51, PQ53 and PQ54 from IRF7821 to follow CIS rules.

011207 W
PG 46
Add PC176(no-stuff) same as PC110.
Change footprint for PC110,PC111,PC112,PC176 from "CC1026" to "CC1210"
This modify is for clear acoustic issue to add cap option. 011307

011307 W
PG 46
Add PC177(no-stuff) same as PC110
PC177 and PC176 are for clear charger noise.

011307 W
PG 47
Add PR193 0 ohm no-stuff between "SKIP#" and "+VCC_+3P3V_+5V"(PU9-pin 3)
This modify is for DELL request.

011307 W
PG 45
For DELL request to Remove FL5 .

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011307W
PG 49
modify note from
"Temp part, Wait library engineer to create G-MAG
MHC2012S601NSn-80 600 ohm 0805 ferrite."
to
"Temp part, Wait library engineer to create
FBM-11-201209-221A30T 220 ohm 0805 ferrite."

011307W
PG 49
For clear EMI - 601.4MHZ off 14.318MHZ
modify Valur for L81,L82 from
"FBMH2012HM331-T."
to
"FBM-11-201209-221A30T"

011407GC
Page 47
Added 100uF/25V/Aluminum (Same as PC42) on PC178 and PC179 between
+3P3V_+5V_PWR_SRC and GND (Parallel connection with PC101) to fix +5VALW
noise.

011407GC
Page 46
Changed PC177 to PR168_2.37K/1%/1206 to fix charger noise.

011407GC
Page 24
Populate SMBus0 option. Pop R675, R677, Nopop R674, R676.

011407GC
Page 50
Populate PC42 and PC29

011407GC
Page 46
Populate PC176

011507 W
PG 10
For DELL request to pop "delay current for "LDT_STOP#".
No-stuff R498 , Pop U35,R667,D31,R668,C760
And change R668 to 10K ohm 1% , C760 to 39pF.

011507 W
PG 50
Change PC31 from 4.7uF 10V X6S 0805 to 4.7uF 25V X6S 0805
Because original has been EOL.

011507 W
PG 49
Add P/N "CX209221000" for L81,L82
PG 46
Add P/N "CS22376F200" for PR168

011607 W
PG 13
Re-load C83-C92,C94,C96 to clear issue
PG 24
Re-load R674-R679 to clear issue

011607 W
PG 33
For DELL request,
Pop F1,F2 and non-pop PJP 11,PJP 20

011607 W
PG 44
For ME request, Change P/N from "FDJM6003011" to "FDDM5001012" for PV15

011707 W
PG 47
For DELL request to change PL8 to HMP1340-4R7 (CV-4790MZ00)
from HMU1356-4R7 (CV-47A0MZ02)

011907 W
PG 10
For DELL request to change P/N from CH03906JB06 to CH04706JB01 for C760

011907 W
PG 49
Re-load L81,L82,PR168 from CIS.

012407W
PG 33
For DELL request to nonpop F1 and F2

012607 W
PG 47
Change PL8 Back to HMP1340-4R7,change P/N from "CV-47A0MZ02" to "CV-4790MZ00"

012607 W
PG 24
Add R678,R679 to pull high SMBus0

012907 W
PG 37
For Glan request to Change P/N for BT1 from DFHS02FS609 to DFHS02FS641.

012907 W
PG 22
Change P/N for JTV1 from DFMD07FR007 to DFMD07FR006.

012907 W
PG 10
Change R668 from 10K ohm to 20K ohm to meet ATI errata.

021307 W A00-01
Page 26
Remove "+3.3V_ALW" and "PJP4"
Remove "PJP5" and short trace.

021307 W A00-02
Page 46
Remove "PJP18","PJP19" and short trace.

021307 W A00-03
Page 47
Remove "PJP7","PJP8","PJP9","SJ2","SJ3" and short trace.

021307 W A00-04
Page 48
Remove "PJP6","PJP15","PJP16","PJP17","SJ5" and short trace.

		
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021307 W
Page 49
Remove "PJP3","PJP10","PJP12","SJ4" and short trace.

021307 W
Page 50
Remove "PJP13","PJP14","SJ1" and short trace.

021507 W
Page 33
Change F1 and F2 from 10A to 5A.Change P/N from "DKA00XFU301" to "DK500XFU112".
Original is over DELL spec.

021507 W
Page 29
For DELL request to change R575 from 10K ohm to 100K ohm 1%

021507 W
Page 19
For DELL request to change R172 from 147K ohm to 71.5K ohm 1%

021507 W
Page 21
For DELL request to change Q2,R11,R8 to pop and change R13 to no-stuff

021507 W
Page 46
For DELL request to change PR168 from 2.37K ohm to 1.8K ohm
022707 W
Page 46
For DELL request to change back. PR168 from 1.8K ohm to 2.37K ohm

021507 GC
Page 38
For DELL request to pop R205 and non-pop R204 to change Board ID to A00

021607 W
Page 49
For DELL request to Remove PJP1 and PJP2

021607 W
Page 33
For DELL request to do as below
Remove PJP11 and F1 and net "+5V_ALW_USB" and short to "+5V_ALW"
Remove PJP20 and F2 and net "+5V_ALW_USB_2" and short to "+5V_ALW"

022707 W
PG 37
Change SPI flash from 16Mbit to 8Mbit
030107 W
PG 37
Re-load U10 from CIS

022707 W
PG 50
For DELL request to change PR142 from 31.6K ohm to 26.1k ohm
Re-load from CIS

022707 W
PG 48
Change net on PU6-pin 17 from "+DDR_PWR_SRC" to "+PWR_SRC"

3

D

C

C

B

B

A

A



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5	4	3	2	1
D				D
C				C
B				B
A				A
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5	4	3	2	1

5	4	3	2	1
D				D
C				C
B				B
A				A
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5	4	3	2	1

072406
PQ4 change from SI4810BDY to SI4800BDY for 5VRUN load switch

072406
PQ6, PQ5, PQ9, PQ12, PQ20 change from 2N7002W-7-F-SOT323 to 2N7002DW

072406
Add RV1, RV2(VZ0603M260AGT_NC)

072406
Use PR31, PR36(4P2R-S-100) follow Dewson project for battery connector selection

072406
Use PQ21 (MMST3904) follow Dewson project for battery connector selection

072406
Use PQ25 (2N7002-7-F_NC) follow Dewson project for battery connector selection

072406
Use PE51 (0.01_3720) current sense resistor follow Quanta other M08 platform component selection

072506
To do PD16 and PR59 depopped

072506
Change to PC66 (0.1U_50V_0805)

072506
Change to PC69 (0.1U_10V_0402)

072406
SJ2 follow Sapporo for debug

072406
Change to PD20 (CH501H-40PT_NC) follow Quanta other M08 platform component selection

072406
Change to PC82 (4.7U_10V_0805) follow Quanta other M08 platform component selection

072406
Change to PR98 (10_F_0603) follow Quanta other M08 platform component selection

072406
Use PR99 (0_NC) OVP/UEP setting R, reserve for debug

073106
Change to PL5 (1.5uH_SIQH126_1R5_17A)

072706
To do pop PR98 for Max8632, Depop PR99, PR100 and PR101

072706
To do pop PR98 for Max8632, Depop PR99, PR100 and PR101

072406
Change to PQ37 (SI4800BDY) follow Sapporo component selection

072406
Change to PQ39 (SI4810BDY) follow Sapporo component selection

072406
Change to PQ36 (SI4800BDY) and PQ38 (SI4810BDY) follow Sapporo component selection

072406
PQ4 change from SI4810BDY to SI4800BDY for 5VRUN load switch

072406
Change to PQ40A and PA40B (2N7002DW)

072406
Change PC130, PC131 to 10U_4V_0805 follow Sapporo component selection

072406
Add PR124 (0_0402) enable pin reserve for debug

072406
To change PR197, PR198 (0_0603) instand fo PJP78 and PJP 80 for Beck

072406
PQ4 change from SI4810BDY to SI4800BDY for 5VRUN load switch

072406
Remove VID resistor due to space limit on PR206, PR207, PR208, PR209, PR210, PR211, PR212 (0_0402)

072406
PQ4 change from SI4810BDY to SI4800BDY for 5VRUN load switch

072406
Change PD21 (CH501H-40PT) follow Sapporo component selection

072406
Change PC136 (4.7U_10V_0805) follow Sapporo component selection

072406
Change PC145, PC169 (1500P_50V_0805_NC)

072406
PL8 and PL9 change to 0.45U(25A,+ -20%, MPC1040LR45)

072706
Delete PR202, PR203 and PR204 (0_0402) to directly connected

072406
Change to PR189 (42.2K_F_0603) follow Dewson component selection

072406
Change PD27, PD24, PD26(CH715FPT) follow Dewson component selection

072506
Change PC67 to a 0_0402 resistor. For Intersil IC, this resistor should depopped and for Maxim IC, this resistor should be popped. This will reduce quiescent current when the RTC LDO is not used.

072406
Change PC115 to 1U_10V_0603

072506
Remove pins 34-42 from PU5 and PU3

072406
Change PD18 (CH50501H-40PT) follow sapporo component selection

072506
Change PC113 to 1U_10V_0603

072406
Change to PR146 and PR149 (10KB_0603_ERTJ1VR103J)

073106
Change to PR146 and PR149 (10KB_0603_ERTJ1VR103J)

072406
Change to PC118, PC119 and PC124 (220U_2.5V_ESR15)

072506
Change PR89, PR88, PR102, PR126 and PR127 to 0_0603

073106
Change PQ34 to FDS6298 and PQ35 to FDS7066ASN3

073106
Change PC18 to 0.1U_25V_NC

073106
Add PR207, PR208 (22_1206_NC) and PC189, PC190 (1500P_50V_0805_NC)

073106
Change PQ25, PQ24 to IMD2A

080206
Add 1000P_50V on PC191, PC192, PC193, PC194

080306
Change from FDS4935_NL to SI4835 on PQ57 and PQ65

080306
PC10 change from 4700P_25V to 6800P_25V

080306
PR61 change from 0_0603 to 1_0603

080306
PQ34 change from FDS6298 to FDS8880_NL

080306
PQ35 change from FDS7066AN3_NL to FDS6676AS_NL

080306
PR128 change from 36K_F_0603 to 17.8K_F_0603
PR134 change from 51K_F_0603 to 24.9K_F_0603
PR118 change from 80.6K_F to 18.2K_F
PR120 change from 121K_F to 27.4K_F

080306
PC191, PC192, PC193 and PC194 change from 1000P to 1000P_NC

080306
PR157 change from 10 to 10_NC
PD21 PD 71 change from CH501H-40PT to CH501H-40PT_NC
PR155 change from 10_NC to 10

080306
PR151 change from 1.5K_F_0603 to 1.5K_F_0603_NC
PC152 change from 1000P_50V to 1000P_50V_NC

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080306
PC172 change from 470P_50V to 0.1U_16V

080306
PC154 change from 4700P_50V to 1000P_50V

080306
PR123 change from 140K_F to 90.9K_F
PR121 change from 178K_F to 150K_F

080306
PR82 change from 150K_F to 174K_F

080406
PQ53 change from FDS6679 to SI4835

080406
PC18 change from 0.1U_25V to 0.1U_25V_NC

080406
PR34 and PR39 change from 10K to 10K_NC

080406
PQ29 change from 2N7002W-7-F_NC to 2N7002W-7-F

080406
PQ23 change from FDS6679 to FDS6679AZ

080706
PR72 part number change from CS31302FB01 to CS31302FB19

080706
Page 42: PR17 change from 100K to 390K

080806
Page 49: Change PU5's pin 19, 20 and PC127's pin1 to link to +5V_ALW from +5V_ALWP.
Page 49: Change PR132's pin 2, pin 9 to link to +3.3V_ALW from +3.3V_ALWP.

080806
Page 49: PC167 part number change from CH1476K1927 to CH14706K919

080806
Page 42: PQ3 and PQ8 change from FDC653N_NL to FDC655BN

080806
Page 45: PQ23 change from FDS6679 to FDS6679AZ

080806
Page 51: PQ56 change from FDS4935_NL to FDS4935BZ

080806
Page 47: PC65 change from 4.7U_10V_1206 to 4.7U_10V_0805

080806
Page 48: Add PR209 (0_0402)
PR104 change from 0 to 0_NC

080806
Page 49: PC112 change from 0.1U_25V_0603 to 0.1U_25V_0402

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080806
Page 50: Add PR210 (0_0603_NC), PR211 (0_0603) and PR212 (100K_NC)

080806
Page 47: PR84 change from 300K_F to 255K_F
Page 48: PR111 change from 48.7K_F to 255K_F

080806
Page 49: PR122 change from 100K_0603 to 100K_0603_NC

080906
Page 49: PR122 link to +3.3V_ALW from +3.3V_ALWP
Page 49: PU6 pin 2 link to +3.3V_ALW from +3.3V_ALWP

080906
Page 49: PR122 link to +3.3V_ALW from +3.3V_ALWP
Page 49: PU6 pin 2 link to +3.3V_ALW from +3.3V_ALWP

080906
Page 45: Add PL4 and PL5 (FMBA-L11-453215-900LMAT_1812)

080906
Page 49: PR136 link to REF_P1 from +5V_ALWP

080906
Page 49: PR136 change from 19.1K_F to 49.9K_F
Page 49: PR138 change from 8.2K_F to 150K_F

080906
Page 48: Add PR196 (1000P_0402_NC)

080906
Page 48: Populate PR99 and no pop PR205

080906
Page 48: Delete PR113 and PR112

080906
Page 49: PR115 change from 1U_10V_0603 to 0.01U_16V

080906
Page 50: PR207 and PR208 change to 2.4_1206

080906
Page 45: PQ25 change from IMD2A to IMD2A_NC

080906
Page 49: Delete PR122 and PR130

080906
Page 49: PR91 should pull up to +3.3V_ALW

080906
Page 46: PD16 chnage to 1SS355

081106GC
Page 45: Rename JABT1 to JBAT1 and JABT2 to JBAT2.

080906
Page 48: PR107 change from 0_NC to 0

080906
Page 49: PR132 change to 200K_F, PR133 change to 100K_F

081106
Page 47: Change PQ31 and PQ30 to FDS8880_NL
Change PQ33, and PQ32 to FDS6676AS
Add a capacitor PR198 (1U_6.3V)
Change PL4 and PL3 to 2.2uH_SIQH125A-2R2 13A
Add PC197 (1U_6.3V) from PU3 pin 9 to digital/power ground

081106
Page 47: Break connection between REF_P1 PU5 pin 1.
Reconnect REF_P1 to PU3 pin 1. Rename REF_P1 to
"5V_3V_REF". --- Name to connect to 1.5V LDO resistor voltage divider.

081106
Page 49: No pop PC113
Remove +3.3V_ALW connection from PU5 pin 9
and connect PU5 pin 9 direct to Analog Ground. ---
no need to bypass, since platform does not use 3.3V
LDO
PU5 pin 4, remove connection from +5V_VCC4 and connect to
analog ground
Change PR120 to 121K 1%
Change PR118 to 80.6K 1%
Change PR129 to 243K 1%

080906
Page 48: No install PR107
Change PR111 to 75K
Change PQ34 to FDS629
Change PQ35 to FDS6299S

081106
Page 49: Delete PR200 and PR201

081706
Page 46: Changed PR62 schematic symbol to R-4P-1 Type.

082106GC:
Page 46: Changed PR51 schematic symbol to R-4P-1 Type.

081406
Page 47: PR197 and PR198 change to 0.1uF_10V

081406
Page 48: PR111 change to 100K_F

081406
Page 50: PR145 & PR168 from 3.01Kohm to 4.02Kohm
PR144 & PR167 from 1.62Kohm to 2Kohm.
PC167 change to 470P_50V_0603_NC

081406
Page 49: PR123 change to 150K_F
PR121 change to 169K_F

081406
Page 47: PR84 change to 154K_F
PR82 change to 178K_F

081506
Page 42: PQ5, PQ6, PQ9, PQ12, PQ20 change footprint to SOT-363

081506
Page 49: PQ40 change footprint to SOT-363

081506
Page 42: PQ19 change to S11NF30L(1224)

082206
Page 46: N17754031(layout net) change to CHAGER_SRC
N17754069(layout net) change to MAX8731_DHO

082206
Page 47: N52515842(layout net) change to +3PV_+5V_PWR_SRC
+3.3V_ALW_DL(layout net) change to +3.3V_ALW_LGATE

082206
Page 49: N17279942(layout net) change to N_Vcore_UGATE2
N17280085(layout net) change to N_Vcore_LGATE2
+DC_PWR_SRC (layout net) change to N_Vcore_PWRSRC

082206
Page 50: N17212693(layout net) change to 8774DL2

082506
PU3 and PU5 footprint change from QFN32-5x5-5-42P to QFN32-5x5-5-33P
PU7 footprint change from QFN44-6x6-5-50P to QFN44-6x6-5-41P
PU4 footprint change from QFN28-5x5-5-33P to QFN28-5x5-5-29P

082906
Page 47: Add PR213 and PR214 as a resistor divider.