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# CANNES-L / BONN-L NVIDIA(N-10M-GE)

CPU : Intel Pentium  
Chip Set : Intel Cantiga & ICH9M  
Remarks : Montevina Platform

Model Name : R719 / R519  
PBA Name : MAIN  
PCB Code : GCE BA41-01146A  
          NANYA BA41-01147A  
          HST BA41-01148A  
Dev. Step : PR  
Revision : 1.0  
T.R. Date : 2009.08.07

Design	CHECK	APPROVAL

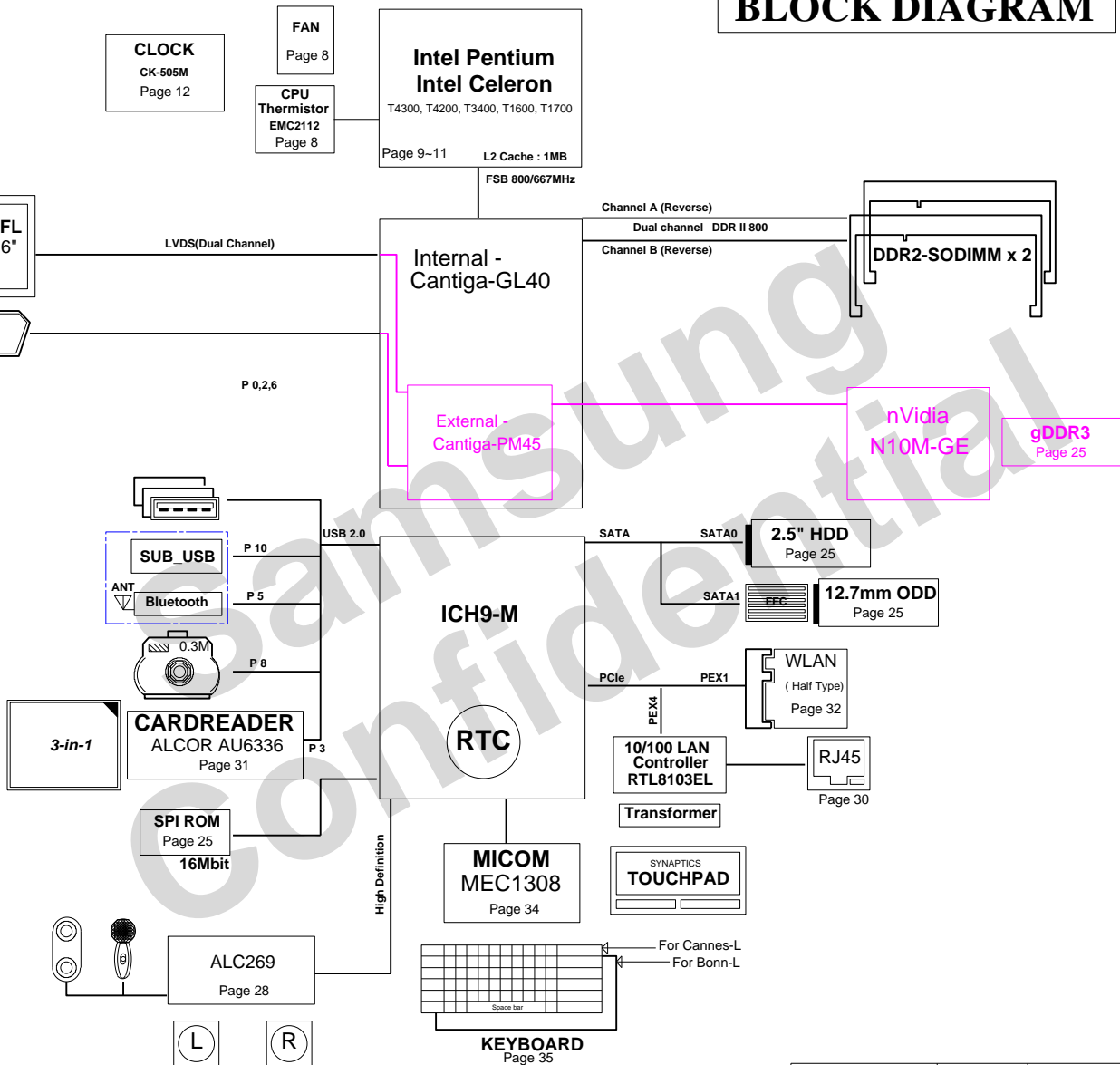
■ Owner : SEC Mobile R & D      Signature :      X

DRAW	Jun PARK	DATE	10/10/2008	TITLE	CANNES-L_EXT	<b>SAMSUNG</b> ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MAIN	COVER	
APPROVAL	HJ KIM	REV	1.0			PART NO. BA41-
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 1 OF 55	

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**BLOCK DIAGRAM**



DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT MAIN BLOCK DIAGRAM	<b>SAMSUNG</b> ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	PART NO.		
APPROVAL	HJ KIM	REV	1.0	BA41-		
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	2	OF 55

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**BOARD INFORMATION**

**SCHEMATIC ANNOTATIONS AND BOARD INFORMATION**

**I<sup>2</sup>C / SMB Address**

Devices	Address	Hex	Bus
<b>ICH9M</b>	<b>Master</b>		<b>SMBUS Master</b>
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 001X	A4h	-
<b>MICOM</b>	<b>Master</b>		
BATTERY	0001 011X	16h	
EMC2102	0111 101X	7Ah	

**USB PORT Assigination**

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0	0 USB PORT (LEFT, BOTTOM)	UHCL_3	6 USB PORT (LEFT, TOP)
UHCL_1	2 USB PORT (LEFT,CENTER)	UHCL_4	8 CAMERA
UHCL_2	4 CARD READER(AU6336)	UHCL_5	10 SUB_USB(TBD)
	5 BLUETOOTH		11

**SATA Assigination**

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
SATA0	HDD	SATA1	ODD
SATA2	-	SATA3	-

**PCI EXPRESS Assigination**

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
PCle1	WLAN	PCle2	Wired LAN
PCle3	-	PCle4	-

**Crystal / Oscillator**

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	
Crystal	10MHz	MICOM	
Crystal	14.318MHz	CLOCK-Generator	
Crystal	25MHz	LAN	

**Voltage Rails**

Power Rail	Descriptions	Power Rail	Descriptions
<b>VDC_ADP</b>	Primary DC system power supply (9 to 19V)	<b>P1.05V_PEG</b>	P1.05V (Direct Media Interface Compensation)
<b>VDC</b>	Charger Reference Voltage Source	<b>P5.0V</b>	5.0V Power Rail (off in S3-S5)
<b>VDC_CHG</b>	3.3V supply for the RTC well.	<b>P3.3V</b>	3.3V Power Rail (off in S3-S5)
<b>PRTC_BAT</b>	5.0V always power well	<b>P1.05</b>	1.05V Power Rail (off in S3-S5)
<b>P5.0V_ALW</b>	12.0V always power well	<b>P0.9V</b>	DDR2 Termination
<b>P1.7V_VREF</b>	Power Chip Reference	<b>P5.0V_AUX</b>	5.0V Power Rail (off in S4-S5)
<b>P2.0V_VREF</b>	Power Chip Reference	<b>P3.3V_AUX</b>	3.3V Power Rail (off in S4-S5)
<b>P5.0V_VREF_FILT</b>	Power Chip Reference	<b>P1.8_AUX</b>	1.8V Power Rail (off in S4-S5)
		<b>CPU_CORE</b>	Core Voltage for CPU
<b>P3.3V_MICOM</b>	Output voltage of TPS51125 (if VDC is removed, it will be off)	<b>AUD_P5V</b>	5.0V supply for Audio
<b>LCD_VDD3V</b>	3.3V (LED LCD)	<b>P4.75V_AUD</b>	Audio Analog Voltage
<b>KBC3_CHG4.2V</b>	To charge battery	<b>P5.0V_STB</b>	To charge USB device at sleep status
<b>P1.2V_LAN</b>	Internal Regulator's Power of LAN Controller	<b>P5.0V_ODD</b>	5.0V supply at SUB_ODD Board
<b>P3.3V_MCD</b>	3.3V (3-in-1 Socket)	<b>EGFX_CORE</b>	nVidia Graphic Chip power
		<b>P1.5V</b>	1.5V Power Rail (off in S3-S5)
		<b>P1.5_AUX</b>	1.5V Power Rail (off in S4-S5)
		<b>P1.8V</b>	1.8V Power Rail (off in S3-S5)

Power source of External

**REVISION HISTORY**

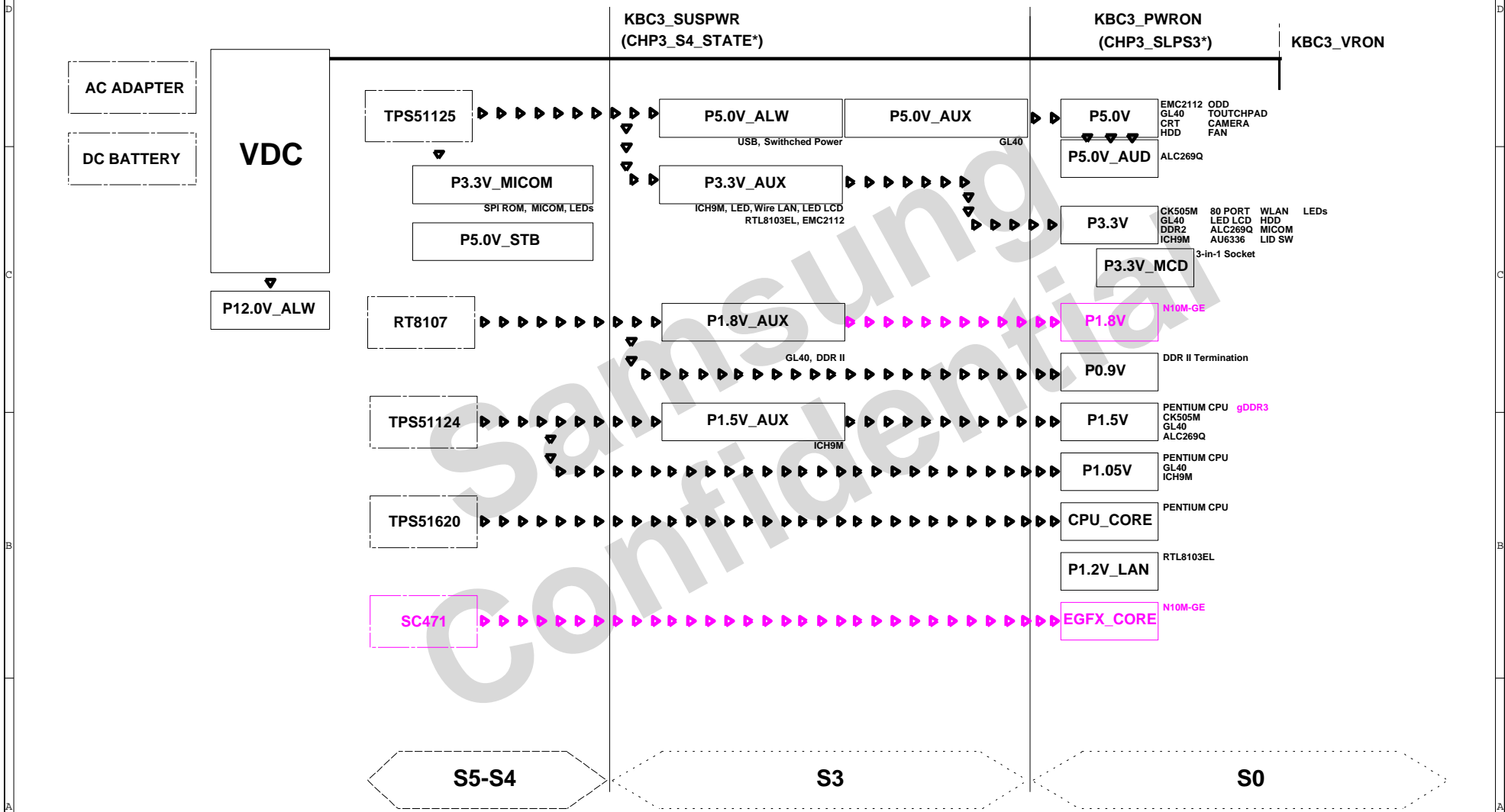
See rev notes for more information.

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	MAIN		
APPROVAL	HJ KIM	REV	1.0	BOARD INFO	PART NO.	BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	3	OF 55

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# POWER DIAGRAM



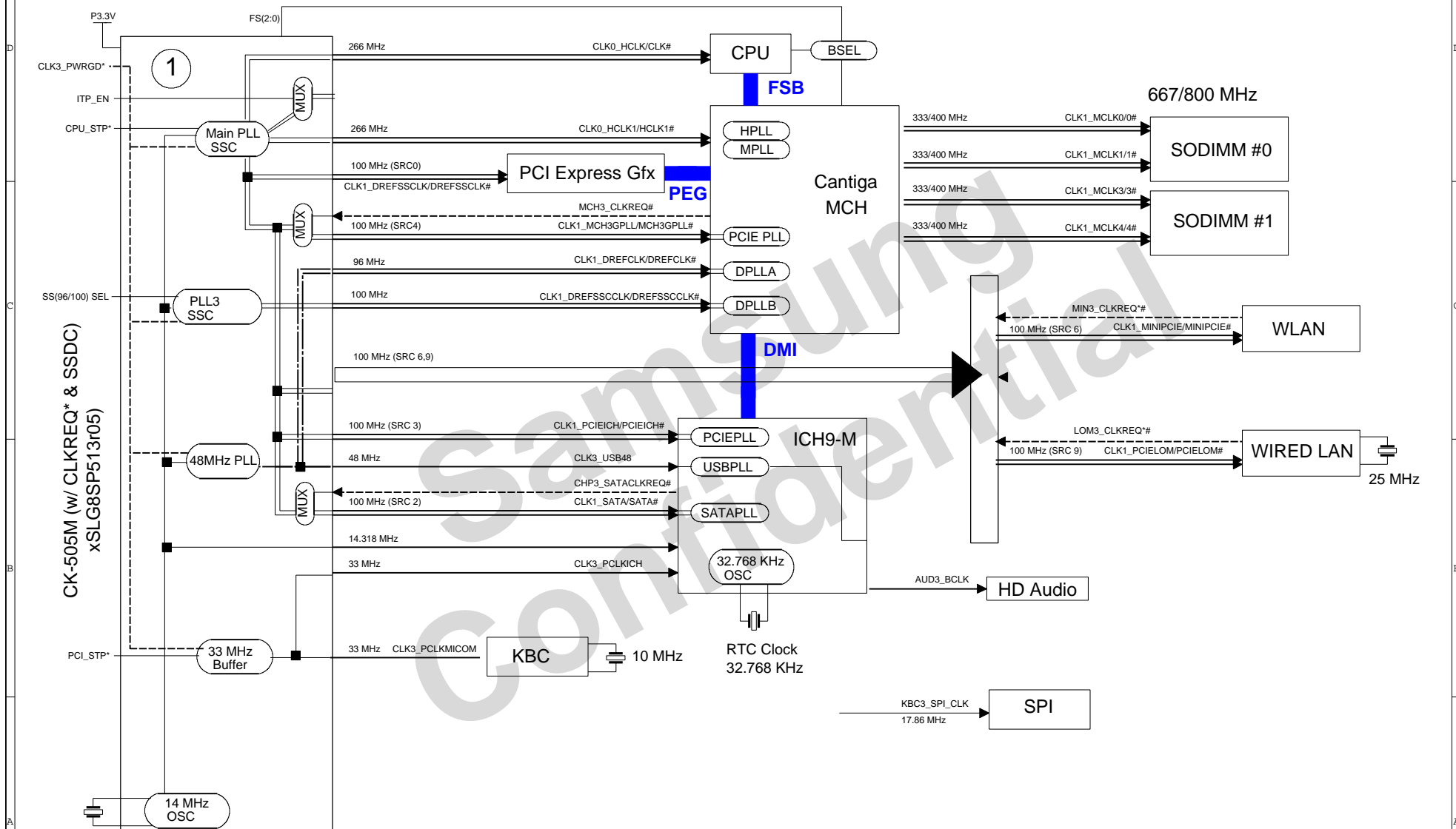
DRAW	Jun PARK	DATE	9/23/2008	TITLE	<b>CANNES-L_EXT</b> <b>MAIN</b> <b>POWER DIAGRAM</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO. <b>BA41-</b>
CHECK	YM AN	DEV. STEP	PR			
APPROVAL	HJ KIM	REV	1.0			
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM			
				PAGE	4	OF 55



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# CLOCK DISTRIBUTION



CK-505M (w/ CLKREQ\* & SSDC)  
xSLG8SP513105

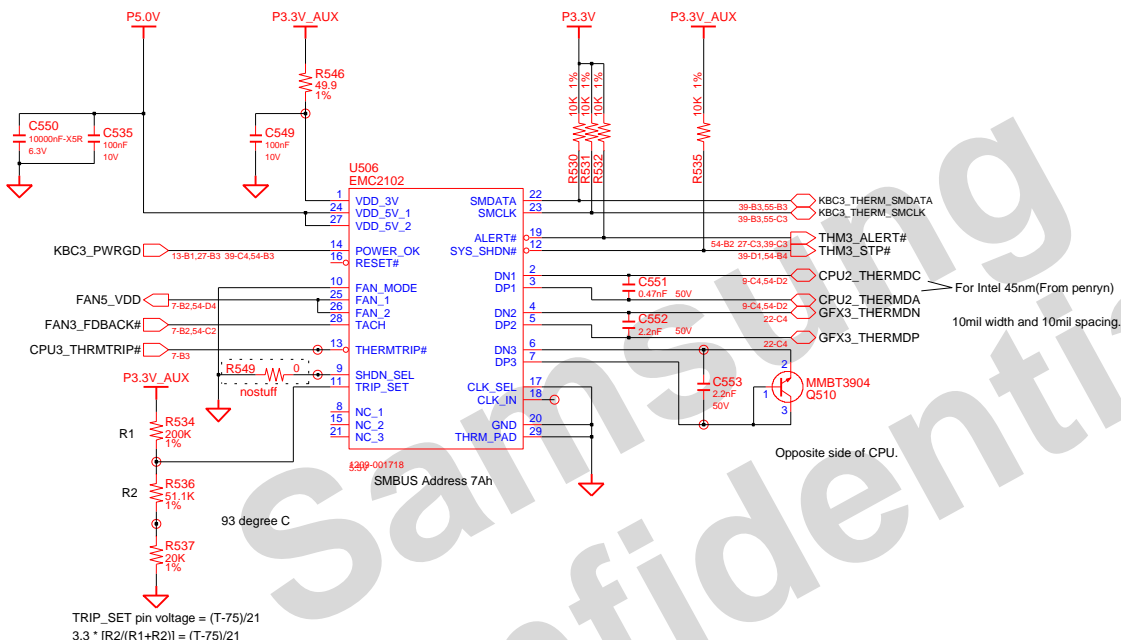
Page 8

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MAIN		
APPROVAL	HJ KIM	REV	1.0	CLOCK DIAGRAM	PART NO.	BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	6	OF 55

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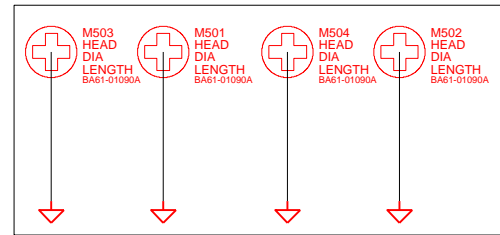
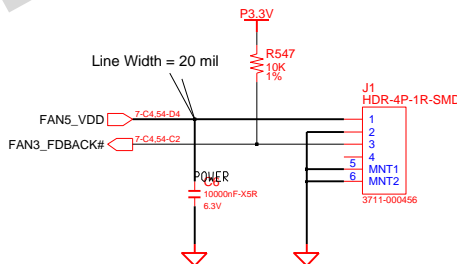
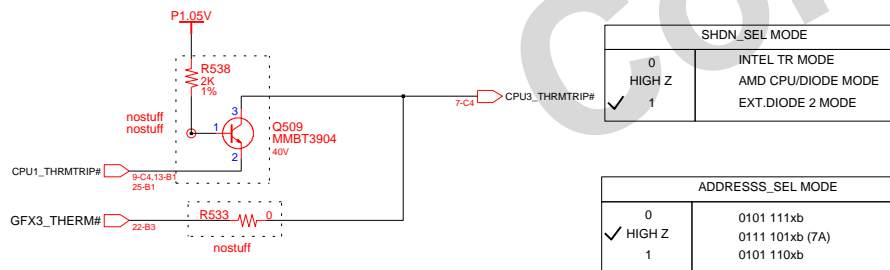
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# THERMAL SENSOR & FAN CONTROL



TRIP\_SET pin voltage =  $(T-75)/21$   
 $3.3 * [R2/(R1+R2)] = (T-75)/21$

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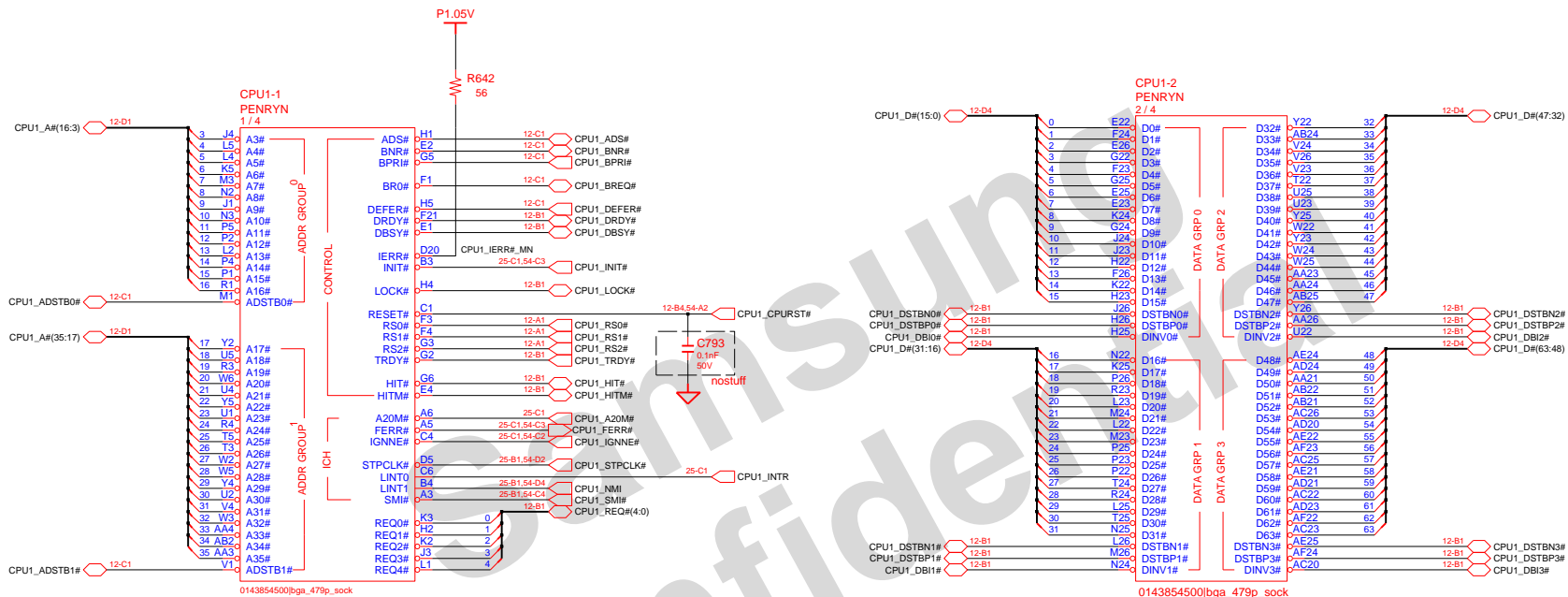


To support heatsink

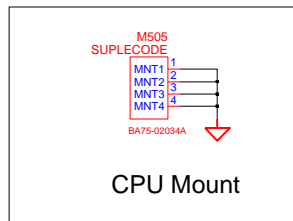
DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT THERMAL SENSOR	SAMSUNG ELECTRONICS	
CHECK	YM AN	DEV.STEP	PR	REV			1.0
APPROVAL	HJ KIM	REV	1.0	MODULE CODE	August 07, 2009 15:14:35 PM	PAGE 7 OF 55	
						PART NO.	BA41-

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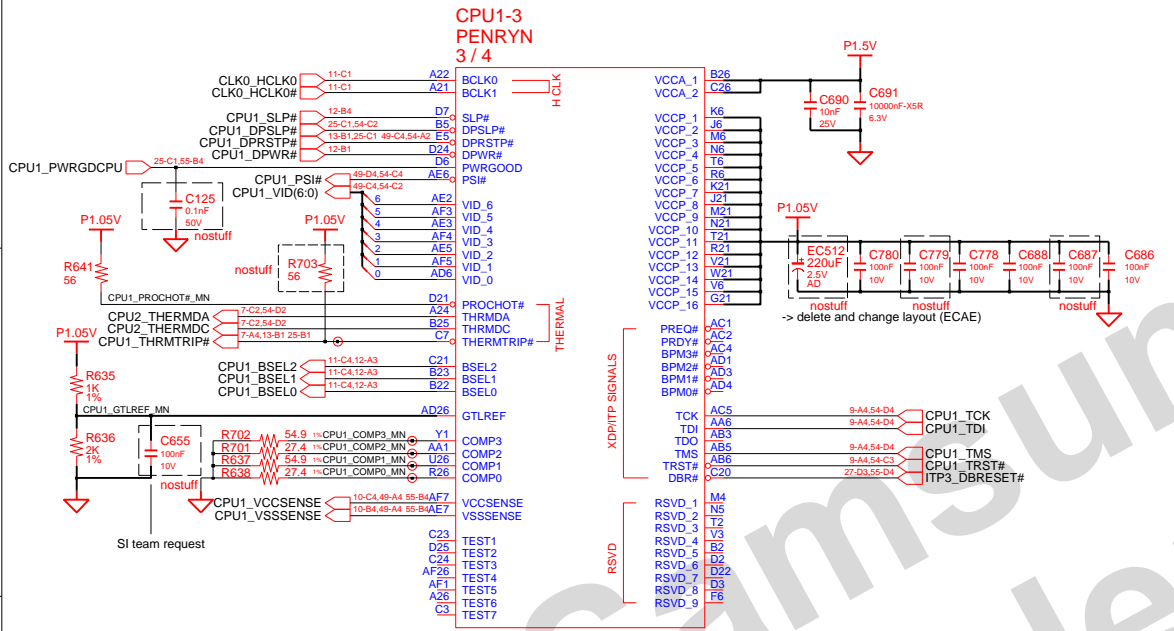
CPU Socket : 3704-001153



DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT CPU	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		PART NO.	
APPROVAL	HJ KIM	REV	1.0		PENRYN (1/3)	BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	8	OF 55



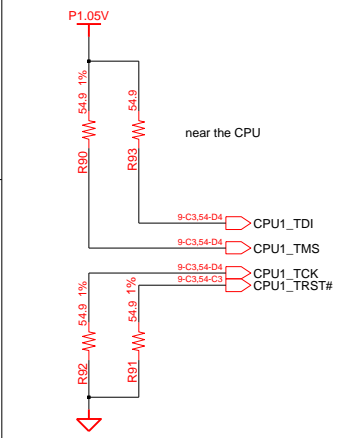
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0143854500bga\_47ap\_sock

CPU Socket : 3704-001153

FSC	FSB	FSA	FRQ
0	0	0	266M
0	1	0	200M
0	1	1	166M



**BSEL**

FSB	Pull-down
FSB 1067 MHz	BSEL0, BSEL1, BSEL2
FSB 800 MHz	BSEL0, BSEL2

**CPU Core Voltage Table** IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 1 0 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 1	0.9625 V	1 0 1 1 0 1 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 1 0 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 1 0 1 1	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 1	0.9250 V	1 0 1 1 1 1 1	0.4125 V
0 0 0 1 0 0 0	1.4125 V	0 1 1 0 0 0 0	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 1	1.4000 V	0 1 1 0 0 0 1	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 1 0	1.3875 V	0 1 1 0 0 1 0	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 1	1.3750 V	0 1 1 0 1 0 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 1 0 0	1.3625 V	0 1 1 0 1 0 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 1	1.3500 V	0 1 1 0 1 1 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 1 0	1.3375 V	0 1 1 1 0 0 0	0.8375 V	1 0 1 1 1 0 1	0.3250 V
0 0 0 1 1 1 1	1.3250 V	0 1 1 1 0 0 1	0.8250 V	1 0 1 1 1 1 0	0.3125 V
0 0 1 0 0 0 0	1.3125 V	0 1 1 1 0 1 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 1	1.3000 V	0 1 1 1 1 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 1 0	1.2875 V	0 1 1 1 1 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 1	1.2750 V	0 1 1 1 1 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 1 0 0	1.2625 V	0 1 1 1 1 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 1	1.2500 V	0 1 1 1 1 1 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 1 0	1.2375 V	0 1 1 1 1 1 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 1	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 1 0	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 1	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 1 0 0 0 0 0	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 1	1.1000 V	1 0 0 0 1 1 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 1 0	1.0875 V	1 0 0 0 1 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 1	1.0750 V	1 0 0 0 1 0 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 1 0 0	1.0625 V	1 0 0 1 0 0 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 1	1.0500 V	1 0 0 1 0 1 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 1 0	1.0375 V	1 0 0 1 1 0 0	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 1	1.0250 V	1 0 0 1 1 0 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 1 0 0 0	1.0125 V	1 0 0 1 1 1 0	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 1 0 0 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 1	0.0000 V
		1 0 0 1 0 0 0	0.5000 V	1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

GTLREF : Keep the Voltage divider within 0.5° of the first GTLREF pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

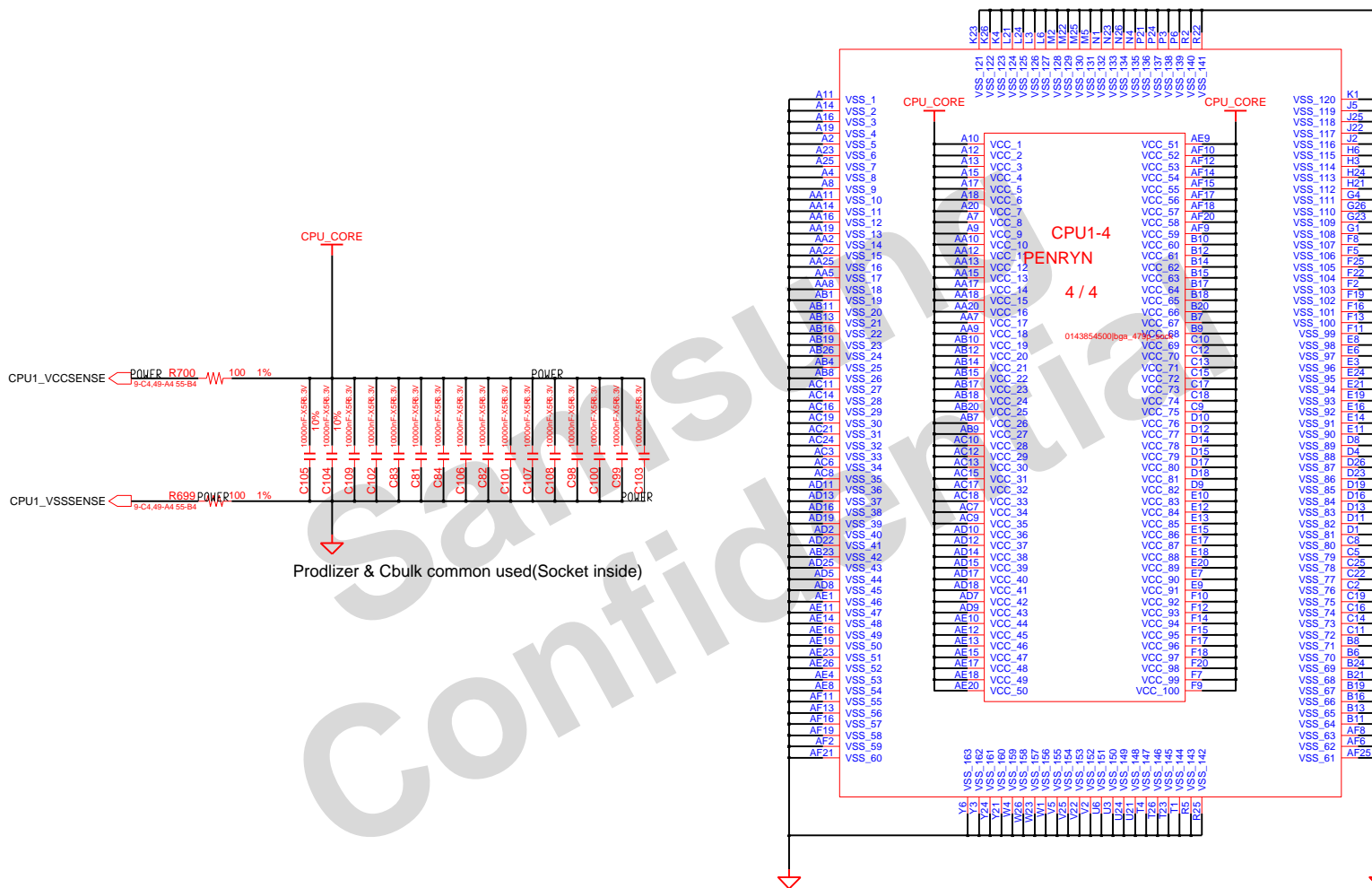
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

\*Yonah Processor (2.33 GHz / 800 MHz : T8D)

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		CPU	
APPROVAL	HJ KIM	REV	1.0		PENRYN (2/3)	PART NO.
MODULE CODE	undefined	LAST EDIT				BA41-
				August 07, 2009 15:14:35 PM	PAGE	9 OF 55

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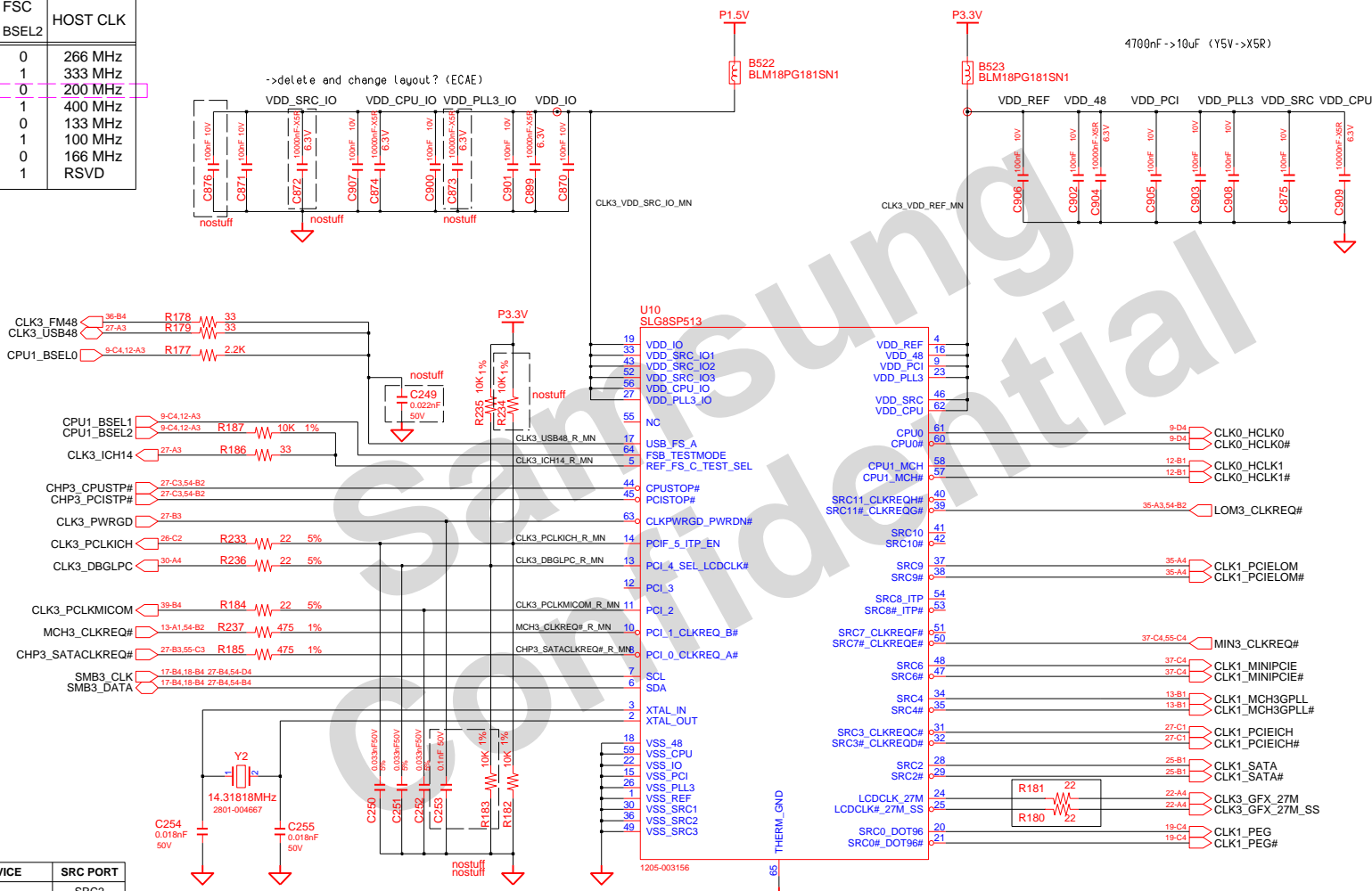
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		CPU	
APPROVAL	HJ KIM	REV	1.0		PENRYN (3/3)	PART NO.
MODULE CODE	undefined	LAST EDIT		August 07, 2009 15:14:35 PM	PAGE	10 OF 55
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# CK505M

FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCDCCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0SRC_0#	27M & 27M_SS

Place 14.31818MHz within 500mils of CK-505

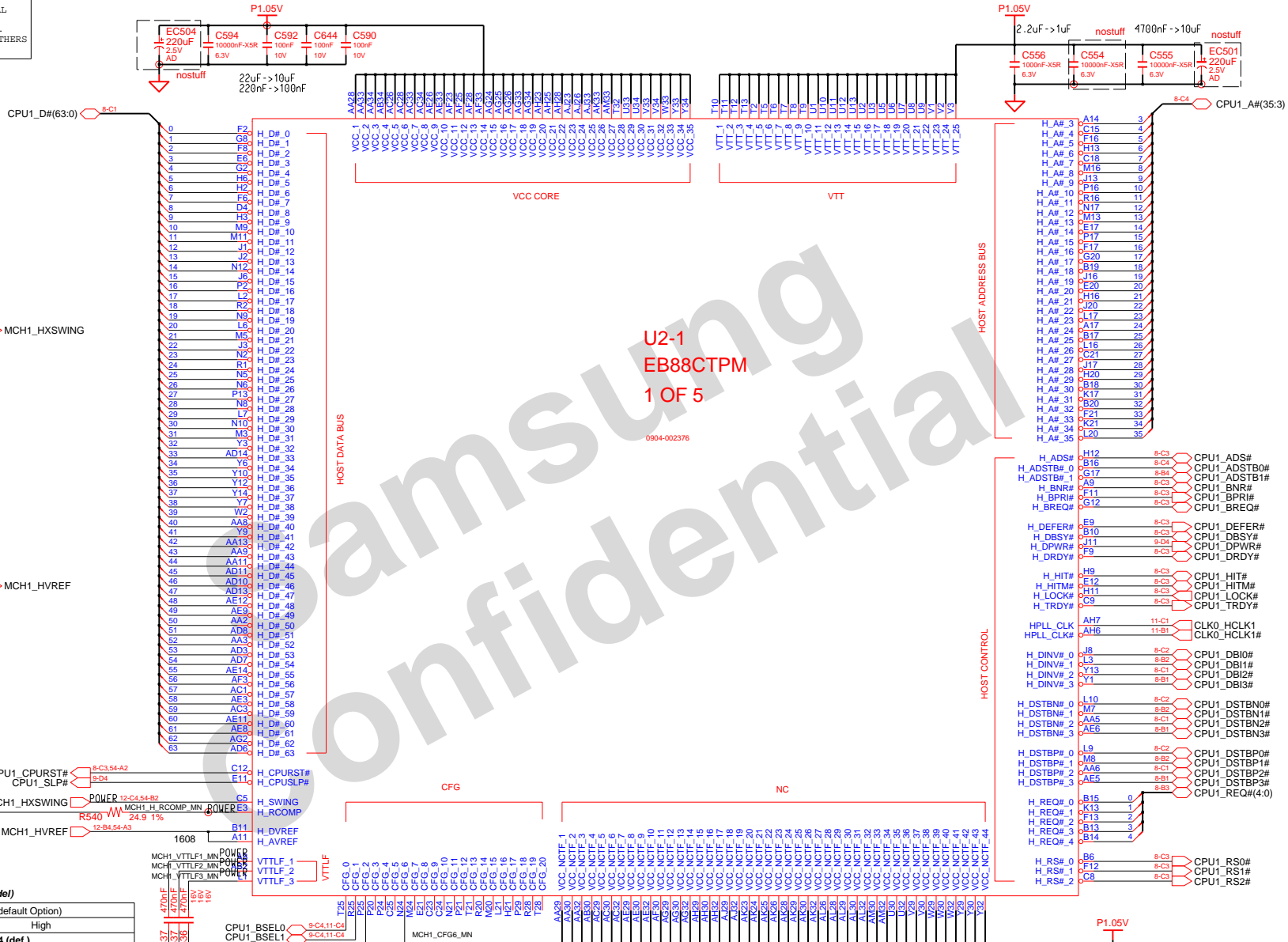
This part is 64pin QFN package.

IDT : 1205-003159  
SL : 1205-003533

DRAW	Jun PARK	DATE	TITLE	SAMSUNG ELECTRONICS	
CHECK	YM AN	DEV.STEP	PR	PART NO. BA41-	
APPROVAL	HJ KIM	REV	1.0	CANNES-L_EXT MAIN_CLOCK_CIRCUIT CK_CLOCK_505M	
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	11 OF 55

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U2-1  
EB88CTPM  
1 OF 5  
0904-002376

**\*POCAFEB-12 Only (Remove in MP Model)**

CFG#	Current Setting (def.: default Option)	
	Low	High
CFG(5)	DMiX2	DMiX4 (def.)
CFG(6)	iTPM Host Interface Enable	iTPM Host Interface Disable (def.)
CFG(7)	ME Crypto non confidentiality	ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)	Normal
CFG(10)	PCIe Loop Back Enable	PCIe Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)	DMI Lane Reversal
CFG(20)	SDVO or PCIe X1 Only(def.)	SDVO and PCIe X1 Simultaneously

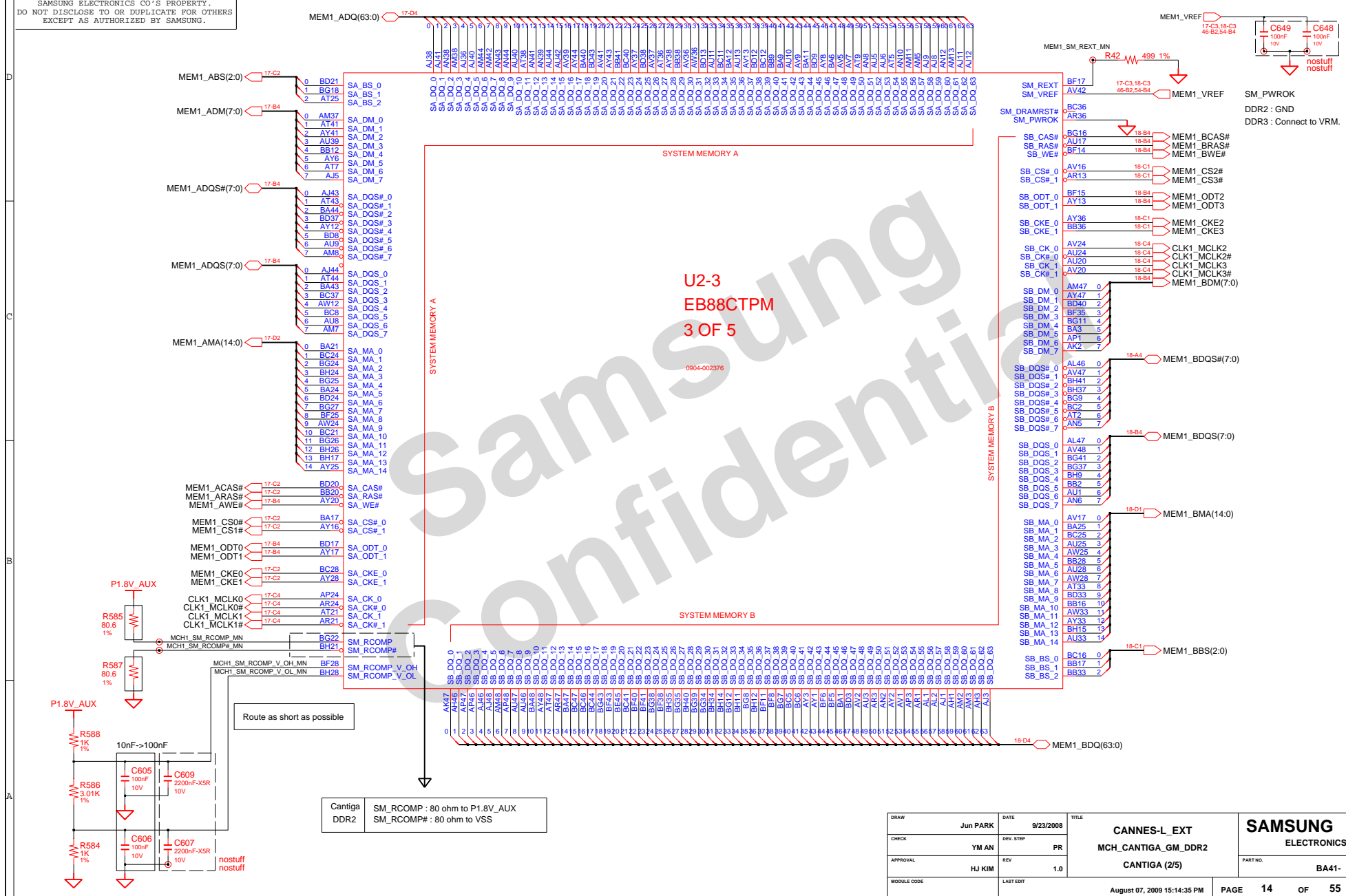
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MCH_CANTIGA_GM_DDR2	PART NO.	
APPROVAL	HJ KIM	REV	1.0	CANTIGA (1/5)	August 07, 2009 15:14:35 PM	PAGE 12 OF 55
MODULE CODE	undefined	LAST EDIT				



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PLACE EACH CAP NEAR AV42 PIN



DRAW		Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT
CHECK		YM AN	DEV.STEP	PR		MCH_CANTIGA_GM_DDR2
APPROVAL		HJ KIM	REV	1.0		CANTIGA (2/5)
MODULE CODE			LAST EDIT			
					August 07, 2009 15:14:35 PM	PAGE 14 OF 55

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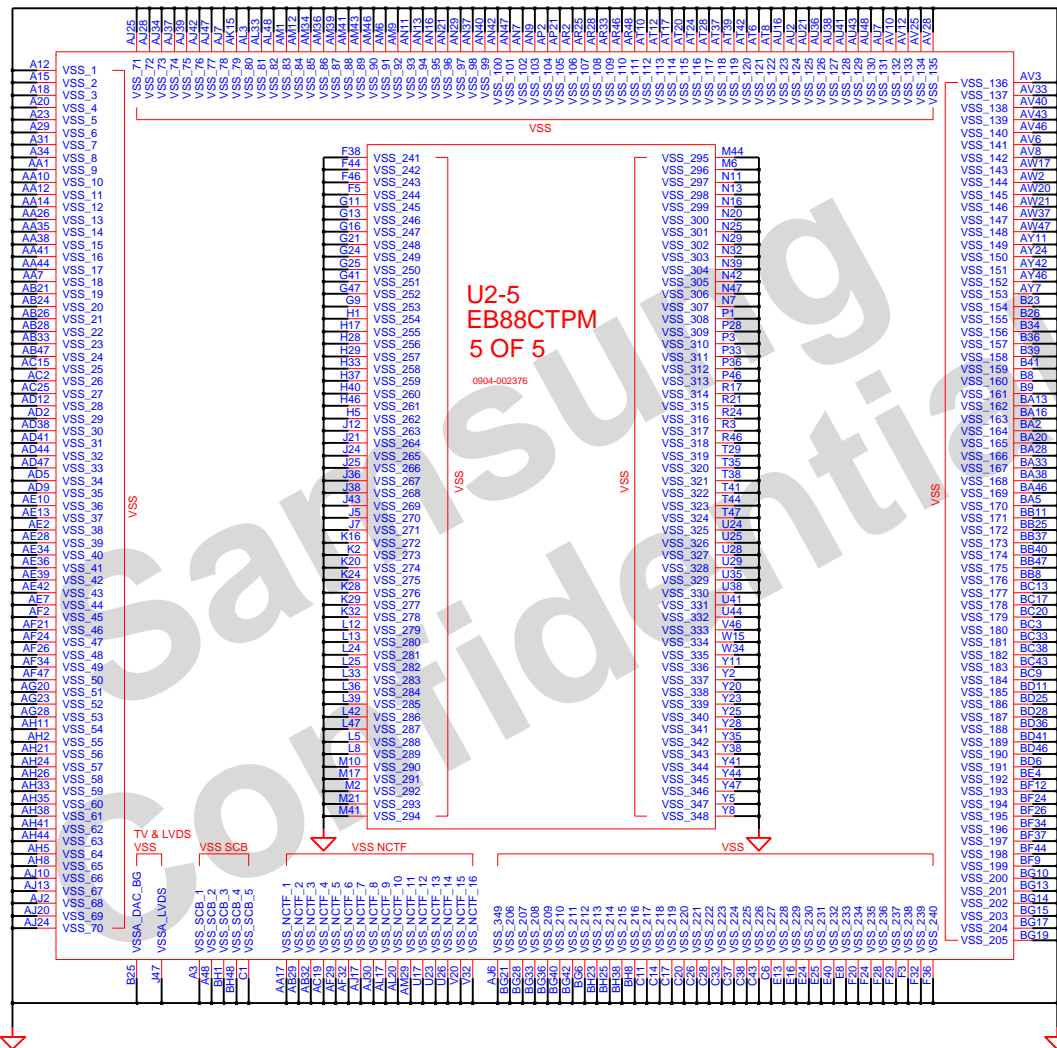
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U2-5  
EB88CTPM  
5 OF 5

0904-002376

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MCH_CANTIGA_GM_DDR2	PART NO.	
APPROVAL	HJ KIM	REV	1.0	CANTIGA (4/5)	BA41-	
MODULE CODE		LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	16	OF 55

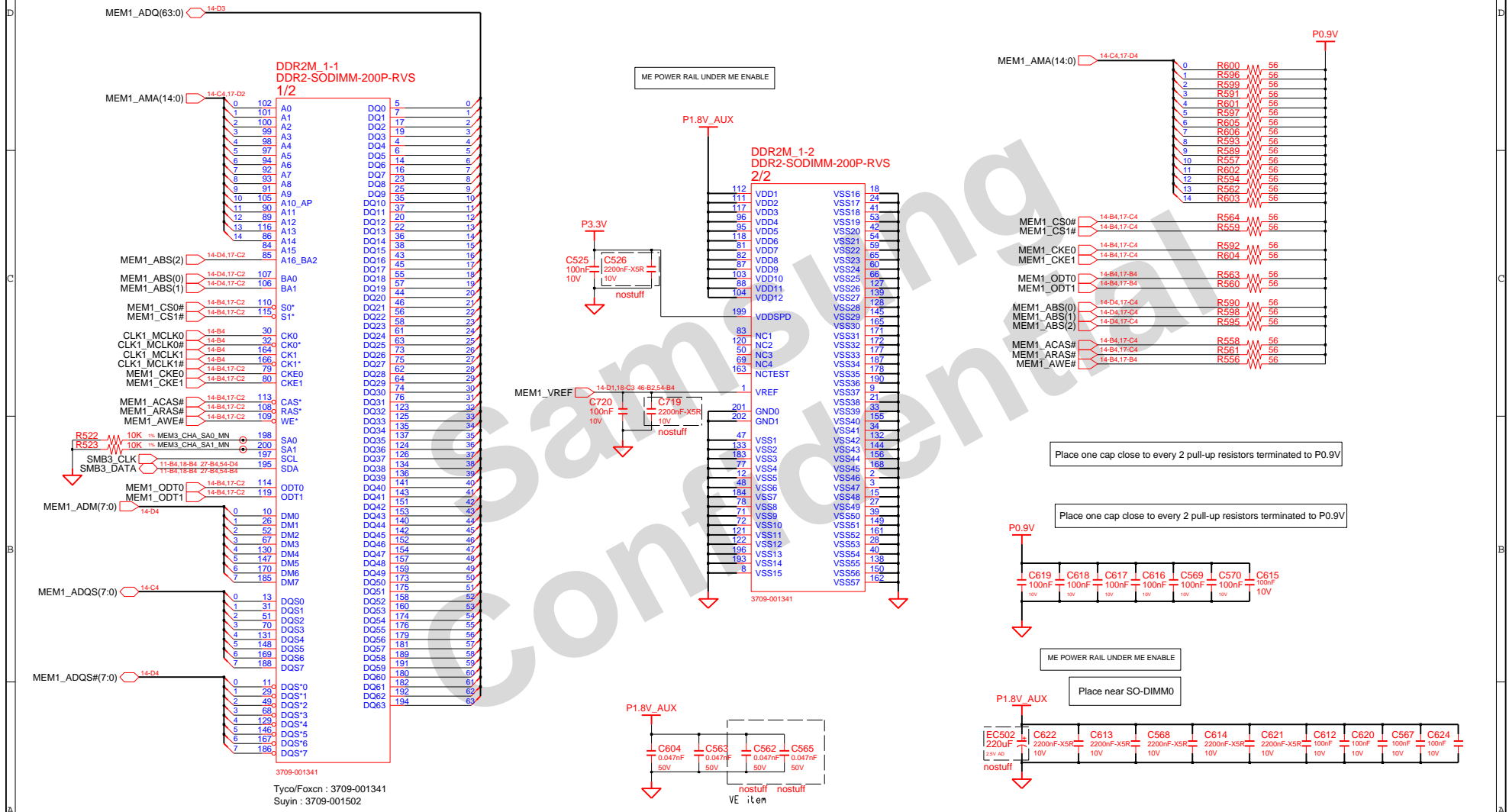


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**DDR SO-DIMM #0**

Height : 5.2mm (Reverse)



Tyco/Foxcn : 3709-001341  
Suyin : 3709-001502

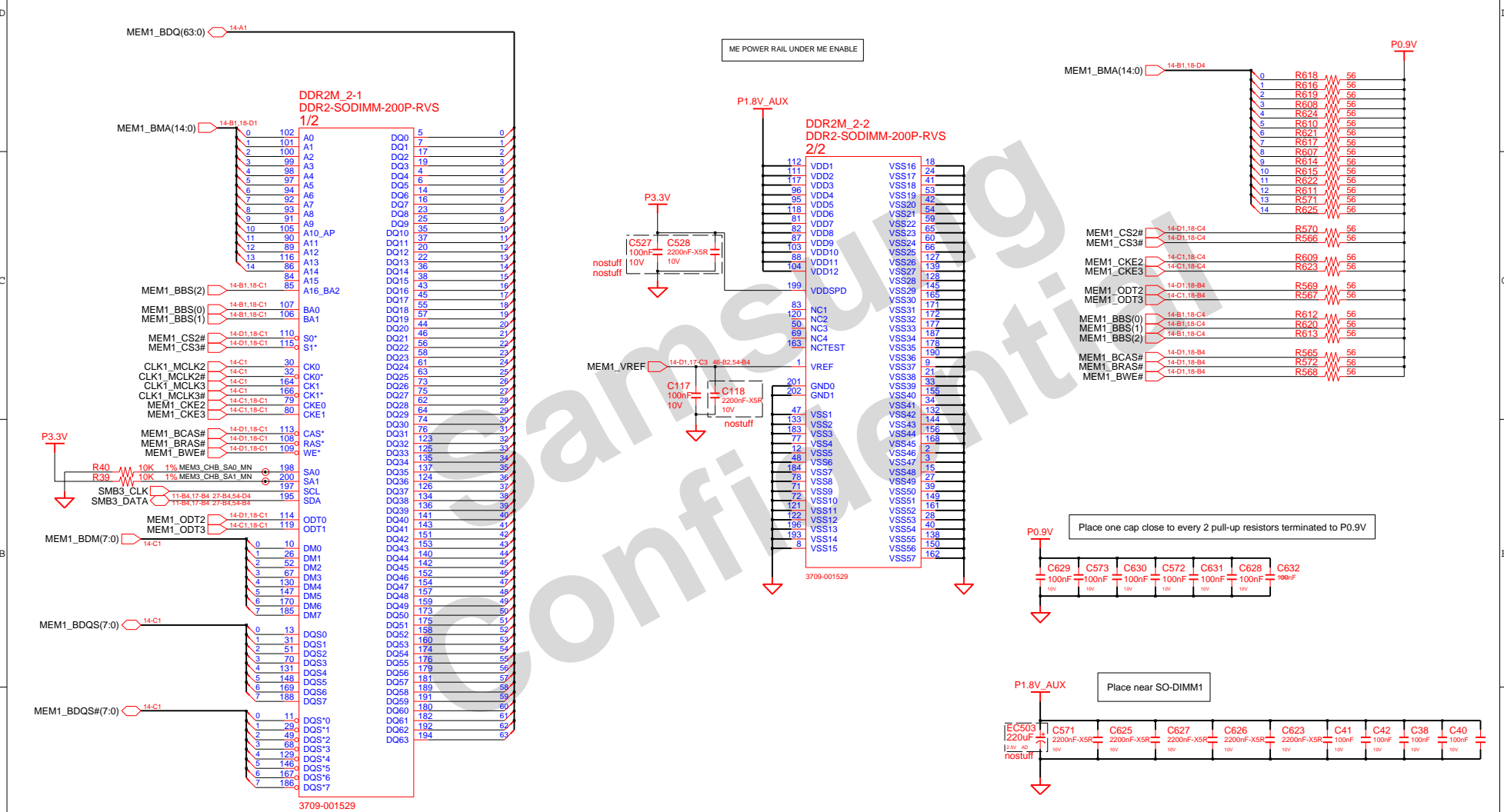
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	MCH_CANTIGA_GM_DDR2	PART NO.	
APPROVAL	HJ KIM	REV	1.0	CANTIGA (5/5)	BA41-	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE	17 OF 55

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**DDR SO-DIMM #1**

Height : 9.2mm (Reverse)

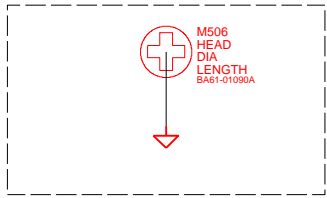
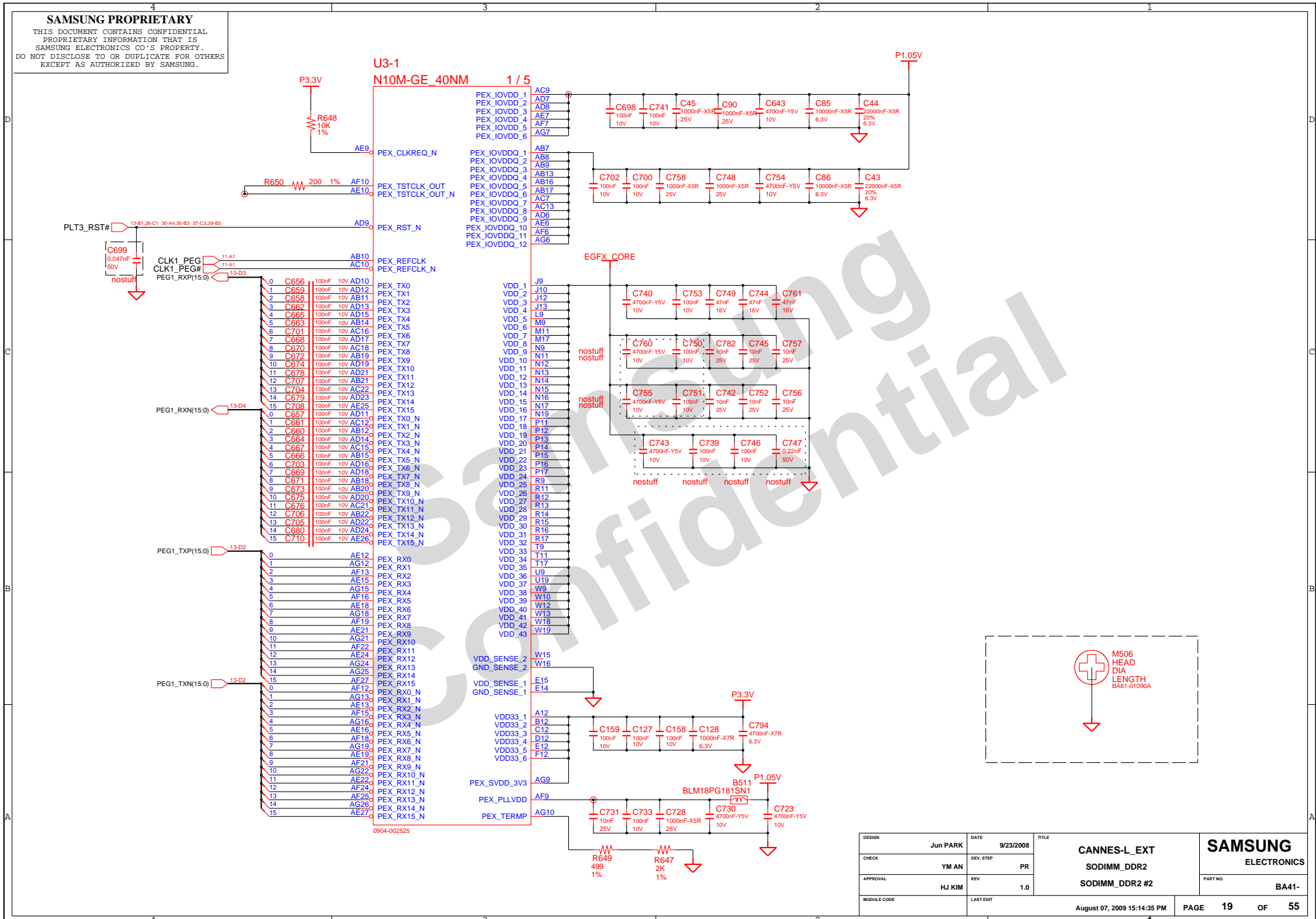


3709-001529  
Foxcon : 3709-001529  
Suyin : 3709-001503

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV. STEP	PR	SODIMM_DDR2		
APPROVAL	HJ KIM	REV	1.0	SODIMM_DDR2 #1		
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE 18	OF 55

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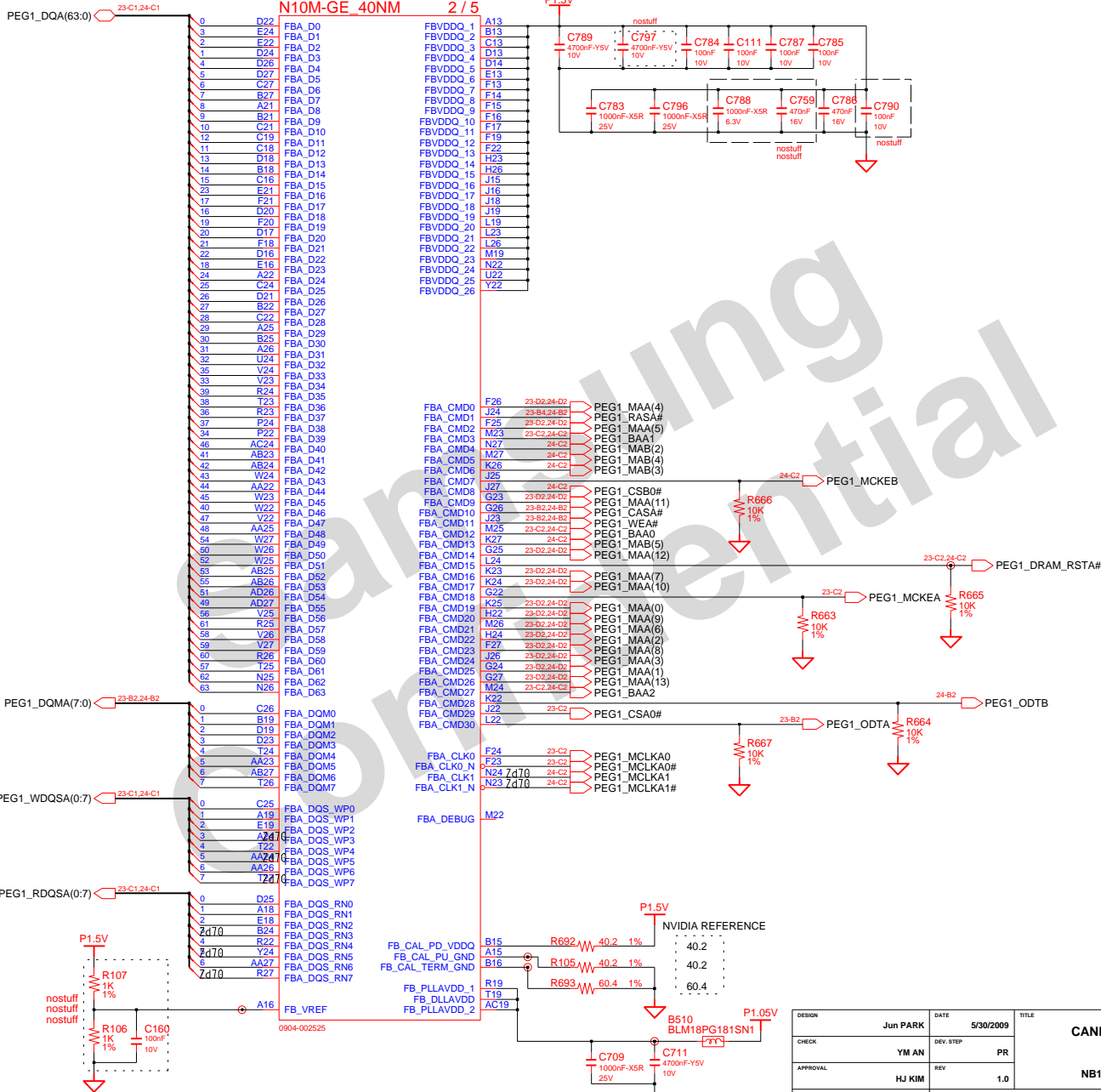


DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV. STEP	PR		SODIMM_DDR2	
APPROVAL	HJ KIM	REV	1.0		SODIMM_DDR2 #2	
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 19 OF 55

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**U3-2  
N10M-GE\_40NM 2 / 5**



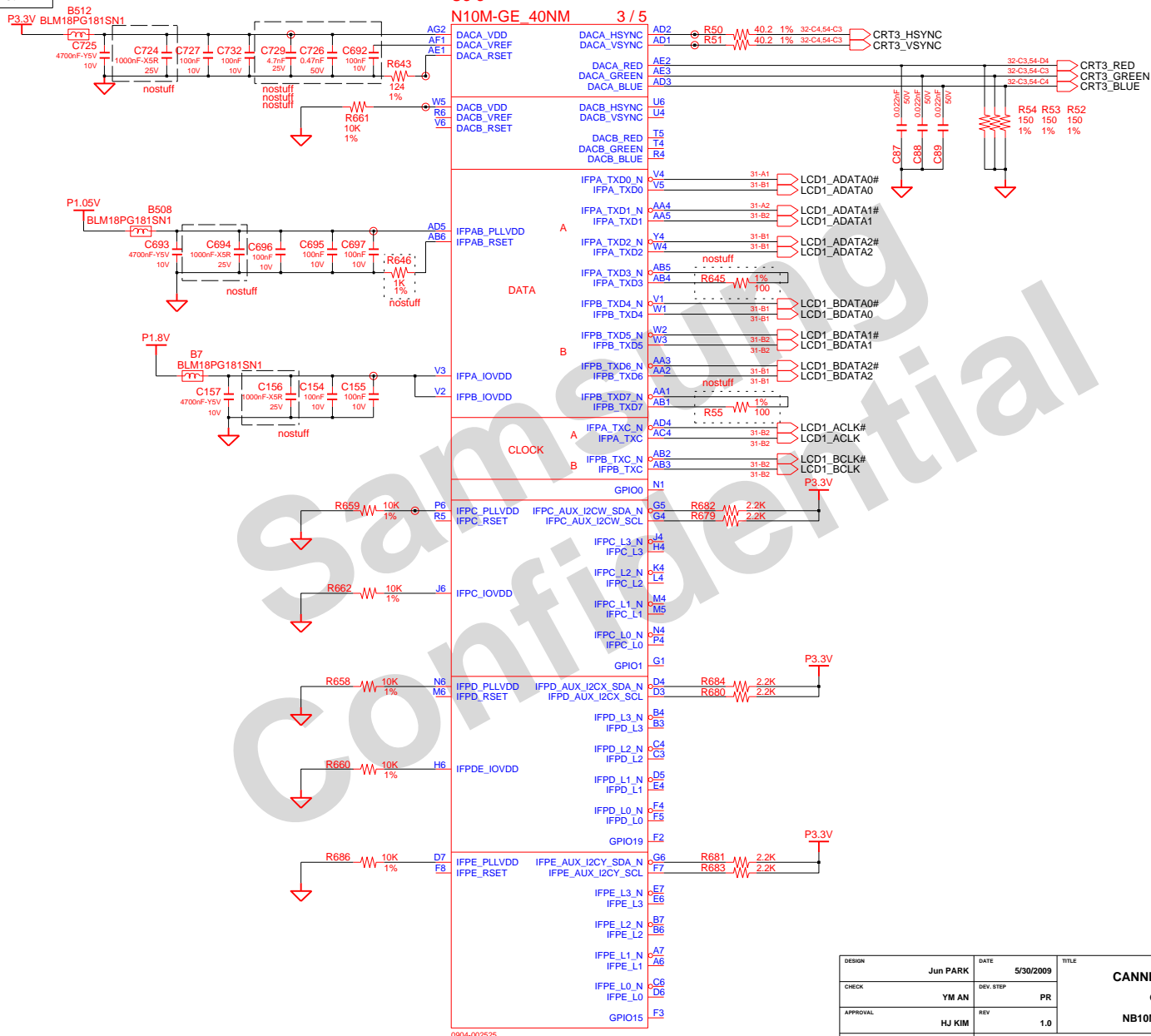
DESIGN	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT
CHECK	YM AN	DEV. STEP	PR	GFX	
APPROVAL	HJ KIM	REV	1.0	NB10M-LP (1/4)	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	

<b>SAMSUNG</b>	
ELECTRONICS	
PART NO.	BA41-
PAGE	20 OF 55

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**U3-3  
N10M-GE 40NM 3 / 5**



DESIGN	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT GFX	<b>SAMSUNG</b> ELECTRONICS
CHECK	YM AN	DEV. STEP	PR			
APPROVAL	HJ KIM	REV	1.0		NB10M-LP (2/4)	PART NO. BA41-
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 21 OF 55

0904-002525

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Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LCD0_BL_PWM	High
GPIO(3)	LCD0_VDD	High
GPIO(4)	LCD0_BL_EN	High
GPIO(5)	GPU VID0	00 0.8V
GPIO(6)	GPU VID1	10 0.85V
GPIO(7)	GPU VID2	NC
GPIO(8)	OVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO(11)	SLI_SYNC	NC
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

Resistor value	PU to VDD	PD to GND	XCLK417 = 0 27MHz
5K ohm	1000	0000	RAM CFG (SEC)
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit
15K ohm	1010	0010	USER[3:0]=1111 for EDID
20K ohm	1011	0011	PADCFG[3:0]=0110 for NB
25K ohm	1100	0100	N10M-GS:0x0A74
30K ohm	1101	0101	N10M-GE:0x0A68
35K ohm	1110	0110	N10M-LP:0x0A69
45K ohm	1111	0111	N10M-NS:0x0A6C
			N10M-NE:0x0A6A
			N10M-GLM:0x0A7C

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	GFX TPYE
SI	0	1	1	1	1Gb

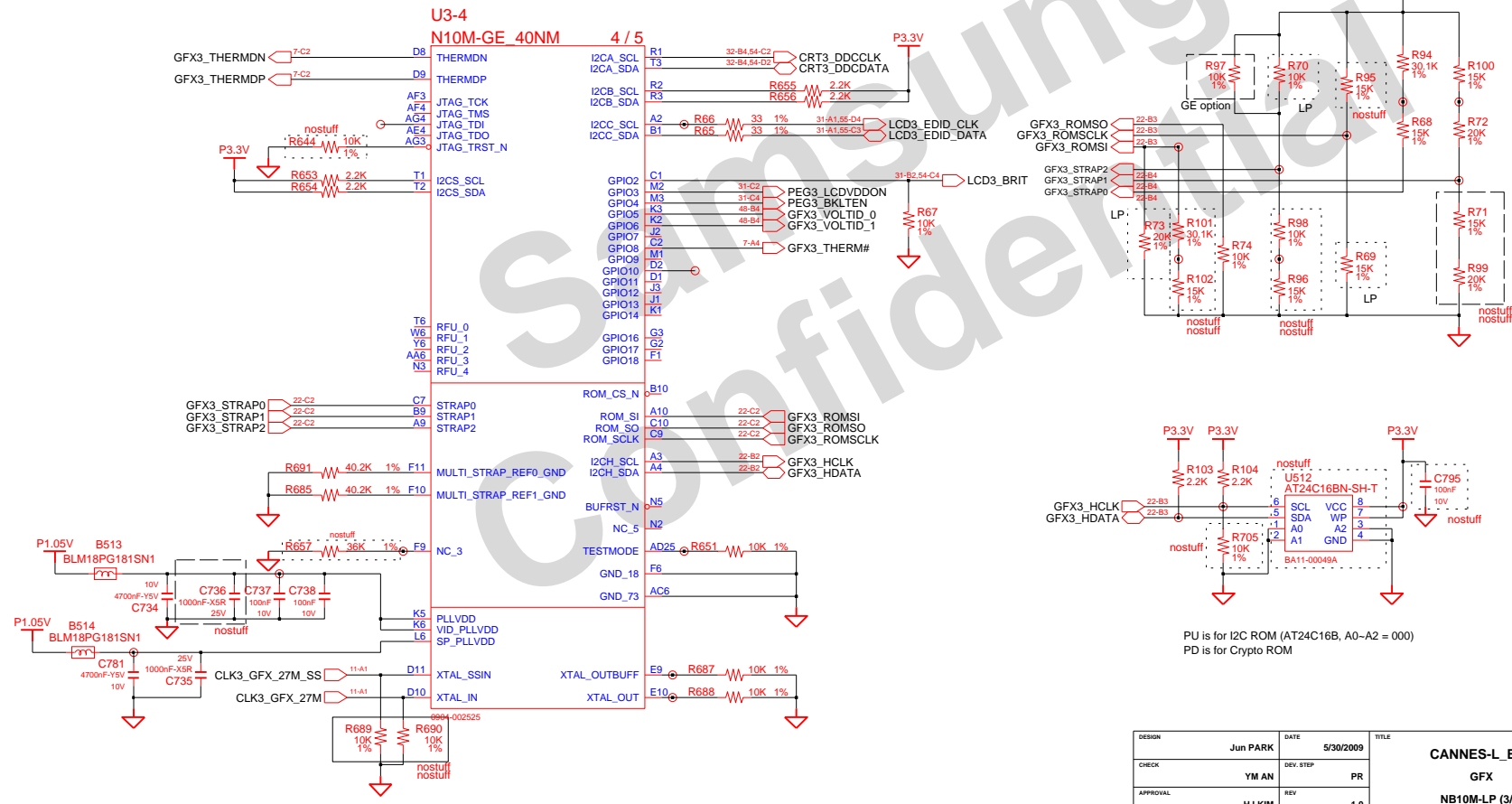
  

Strap2	1	0	0	1	N10M-LP	DEVICE ID
Strap1	1	0	0	0	N10M-GE	
Strap0	1	1	1	0	For NB	
	1	1	1	1	EDID_EN	

**U3-5  
N10M-GE 40NM**

5 / 5

- B2 GND\_1
- B5 GND\_2
- B8 GND\_3
- B11 GND\_4
- B14 GND\_5
- B17 GND\_6
- B20 GND\_7
- B23 GND\_8
- B26 GND\_9
- E2 GND\_10
- E5 GND\_11
- E8 GND\_12
- E11 GND\_13
- E17 GND\_14
- E20 GND\_15
- E23 GND\_16
- E26 GND\_17
- H2 GND\_19
- H5 GND\_20
- J11 GND\_21
- J14 GND\_22
- J17 GND\_23
- K9 GND\_24
- K19 GND\_25
- L2 GND\_26
- L5 GND\_27
- L11 GND\_28
- L12 GND\_29
- L13 GND\_30
- L14 GND\_31
- L15 GND\_32
- L16 GND\_33
- L17 GND\_34
- M12 GND\_35
- M13 GND\_36
- M14 GND\_37
- M15 GND\_38
- M16 GND\_39
- P2 GND\_40
- P5 GND\_41
- P9 GND\_42
- P18 GND\_43
- P23 GND\_44
- P26 GND\_45
- T12 GND\_46
- T13 GND\_47
- T14 GND\_48
- T15 GND\_49
- T16 GND\_50
- U2 GND\_51
- U11 GND\_52
- U12 GND\_53
- U13 GND\_54
- U15 GND\_55
- U14 GND\_56
- U15 GND\_57
- U17 GND\_58
- U23 GND\_59
- U26 GND\_60
- U26 GND\_61
- V9 GND\_62
- V19 GND\_63
- W11 GND\_64
- W14 GND\_65
- W17 GND\_66
- Y2 GND\_67
- Y5 GND\_68
- Y26 GND\_69
- Y26 GND\_70
- AC2 GND\_71
- AC8 GND\_72
- AC8 GND\_74
- AC11 GND\_75
- AC14 GND\_76
- AC17 GND\_77
- AC20 GND\_78
- AC23 GND\_79
- AC26 GND\_80
- AF2 GND\_81
- AF5 GND\_82
- AF8 GND\_83
- AF11 GND\_84
- AF14 GND\_85
- AF17 GND\_86
- AF20 GND\_87
- AF23 GND\_88
- AF26 GND\_89



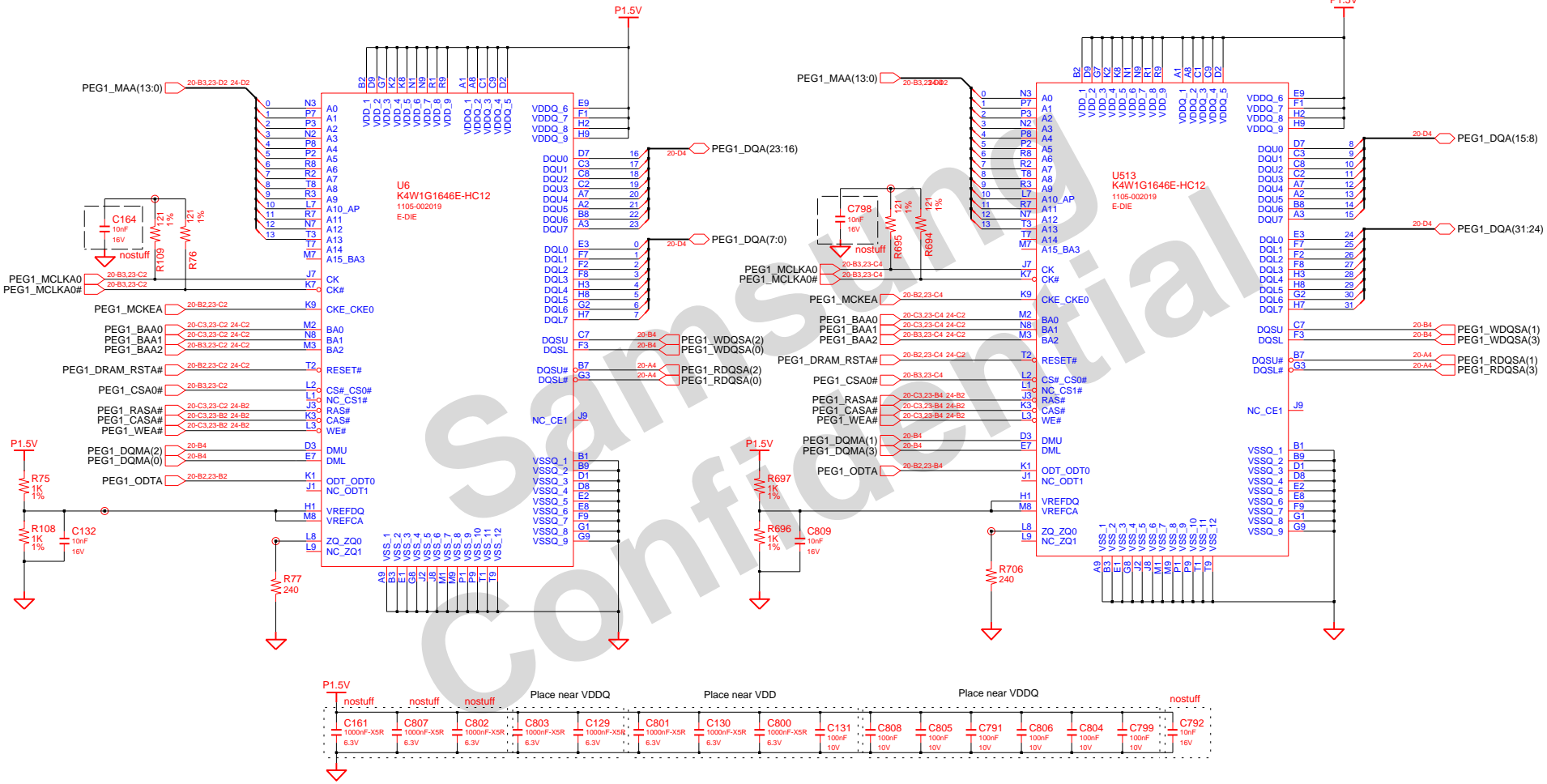
DESIGN	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT GFX NB10M-LP (3/4)
CHECK	YM AN	DEV. STEP	PR		
APPROVAL	HJ KIM	REV	1.0		
MODULE CODE		LAST EDIT			

August 07, 2009 15:14:35 PM	PAGE 22 OF 55
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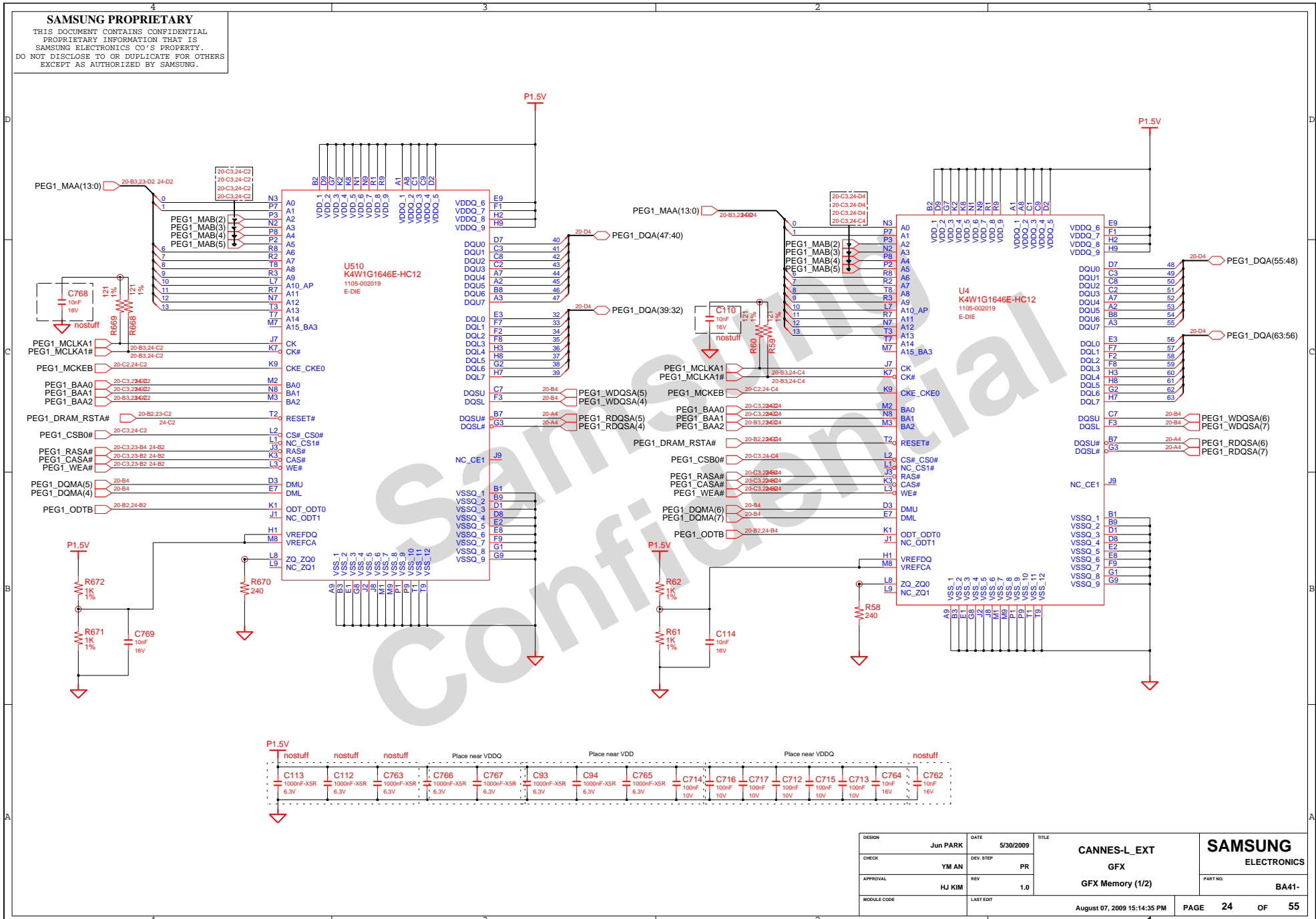


DESIGN	Jun PARK	DATE	5/30/2009	TITLE	<b>CANNES-L_EXT</b> GFX NB10M-LP (4/4)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV. STEP	PR			
APPROVAL	HJ KIM	REV	1.0			
MODULE CODE		LAST EDIT				
					August 07, 2009 15:14:35 PM	PAGE 23 OF 55



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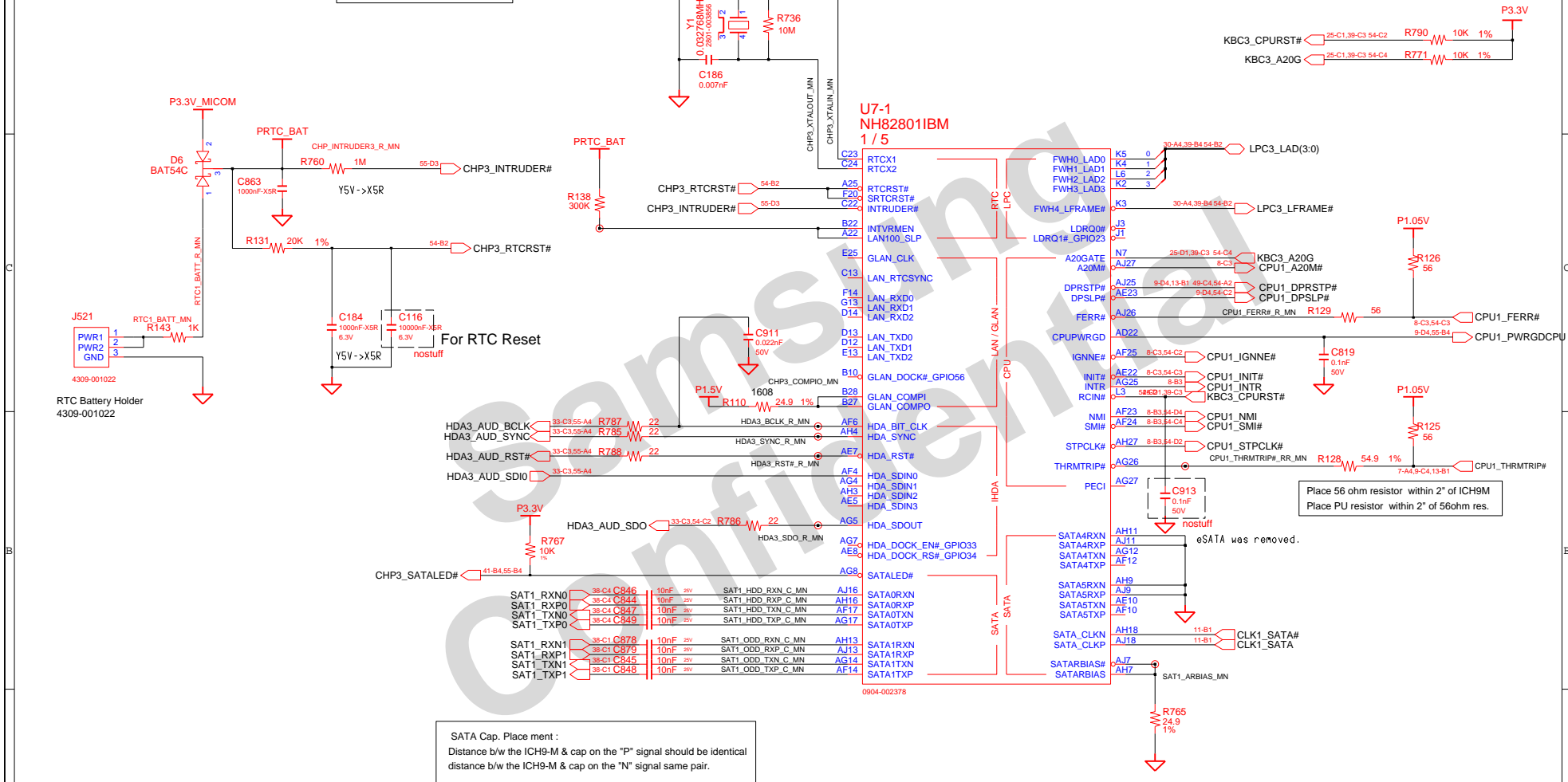
DESIGN	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV. STEP	PR		GFX	
APPROVAL	HJ KIM	REV	1.0		GFX Memory (1/2)	
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 24 OF 55



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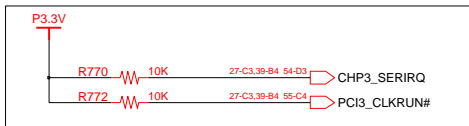
Internal VR Strap	
INTVRMEN	Pull up
VccSus1_05, VccSus1_5, VccCL1_5	
VccLAN1_05, VccCL1_05	



DRAW	DATE	TITLE	SAMSUNG ELECTRONICS	
Jun PARK	5/30/2009	CANNES-L_EXT GFX	PART NO. BA41-	
Y.M AN	DEV. STEP PR	GFX Memory (2/2)	August 07, 2009 15:14:35 PM	
HJ KIM	REV 1.0		PAGE 25	OF 55
MODULE CODE	LAST EDIT			

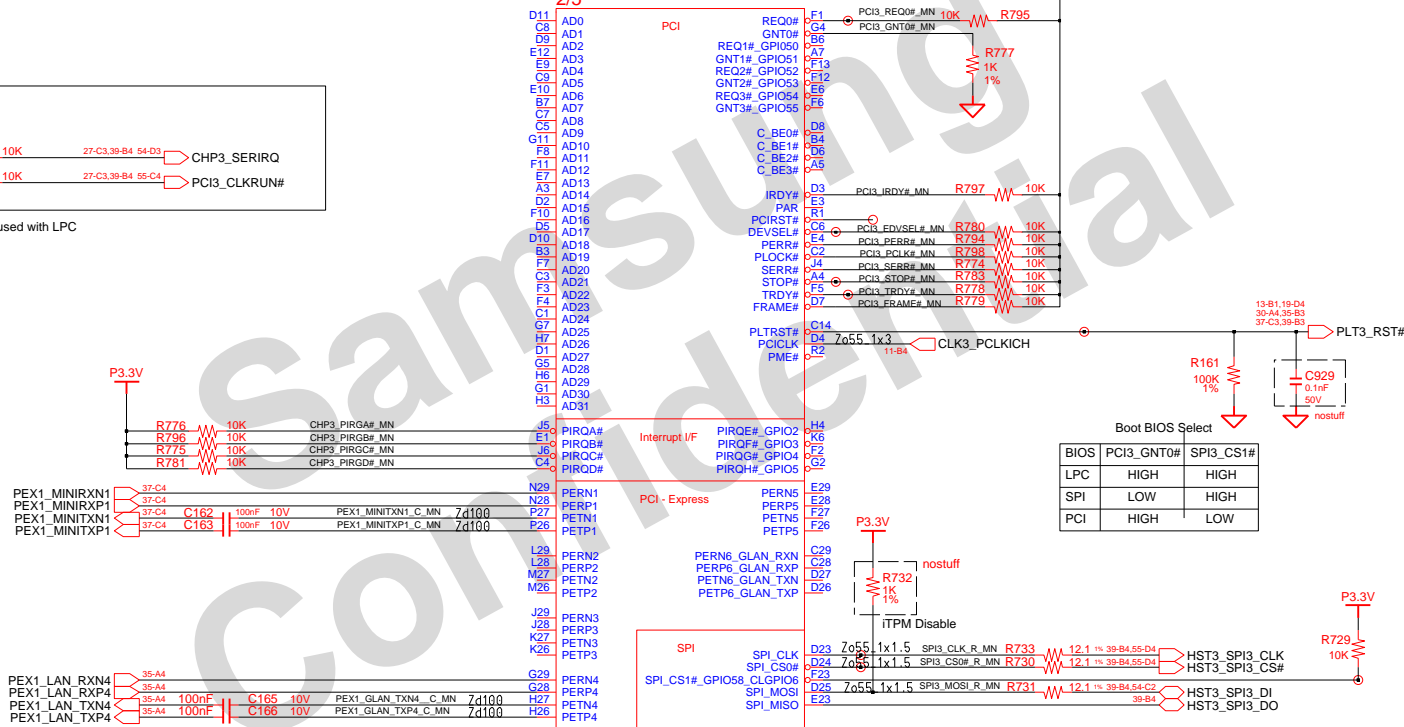
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LPC option ; These are used with LPC

**U7-2  
NH82801IBM  
2/5**



Boot BIOS Select

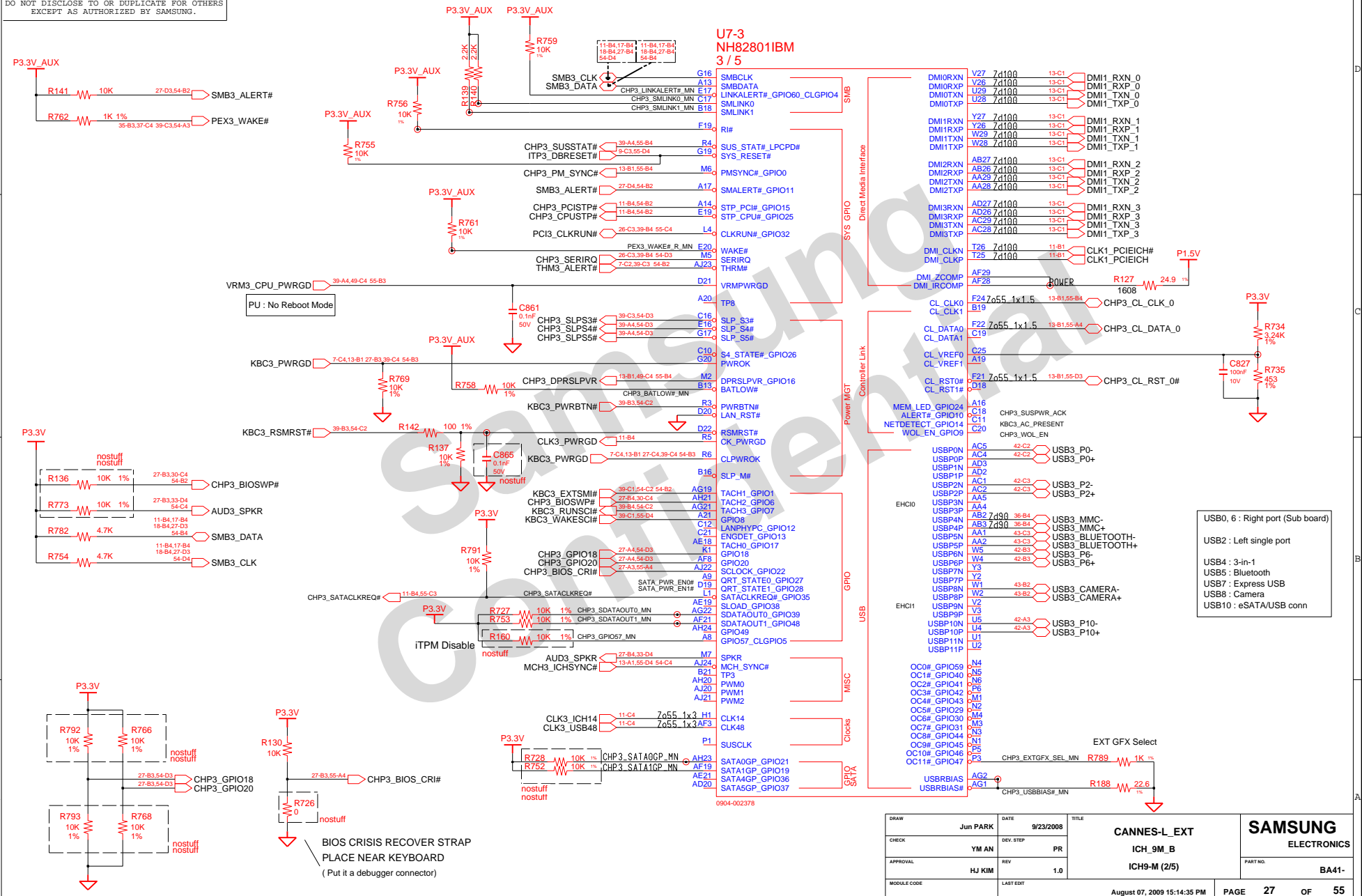
	BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH	HIGH
SPI	LOW	HIGH	HIGH
PCI	HIGH	LOW	LOW

AC caps : PCIE need to be within 250mils of the driver  
Resistor for Test : Place Stuffing Option to minimize stubs

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	ICH_9M_B	PART NO.	
APPROVAL	HJ KIM	REV	1.0	ICH9-M (1/5)	BA41-	
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	26	OF 55

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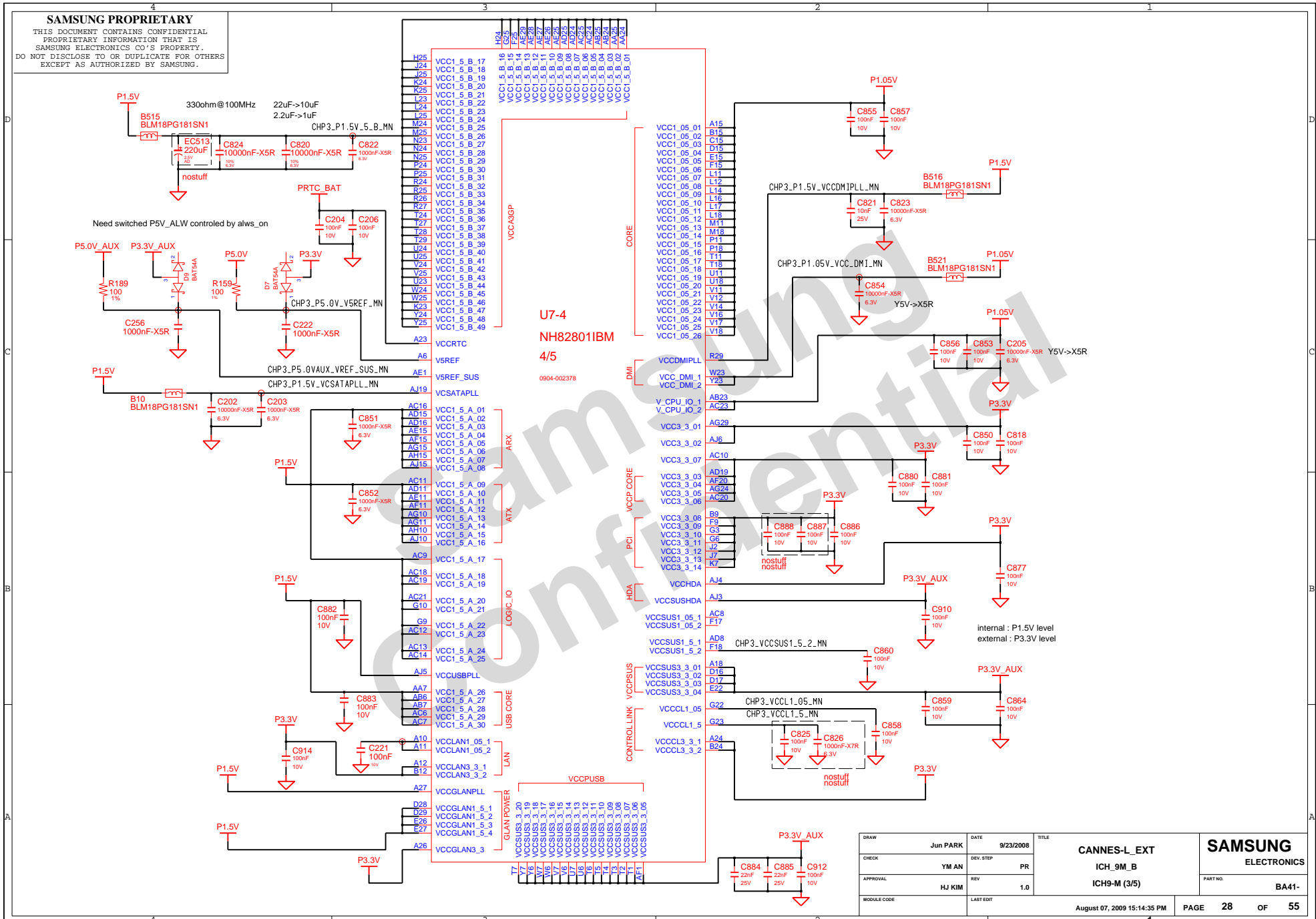
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DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	<b>SAMSUNG</b> ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		ICH9_M_B	
APPROVAL	HJ KIM	REV	1.0		ICH9-M (2/5)	PART NO. BA41-
MODULE CODE		LAST EDIT			August 07, 2009 15:14:35 PM	PAGE 27 OF 55

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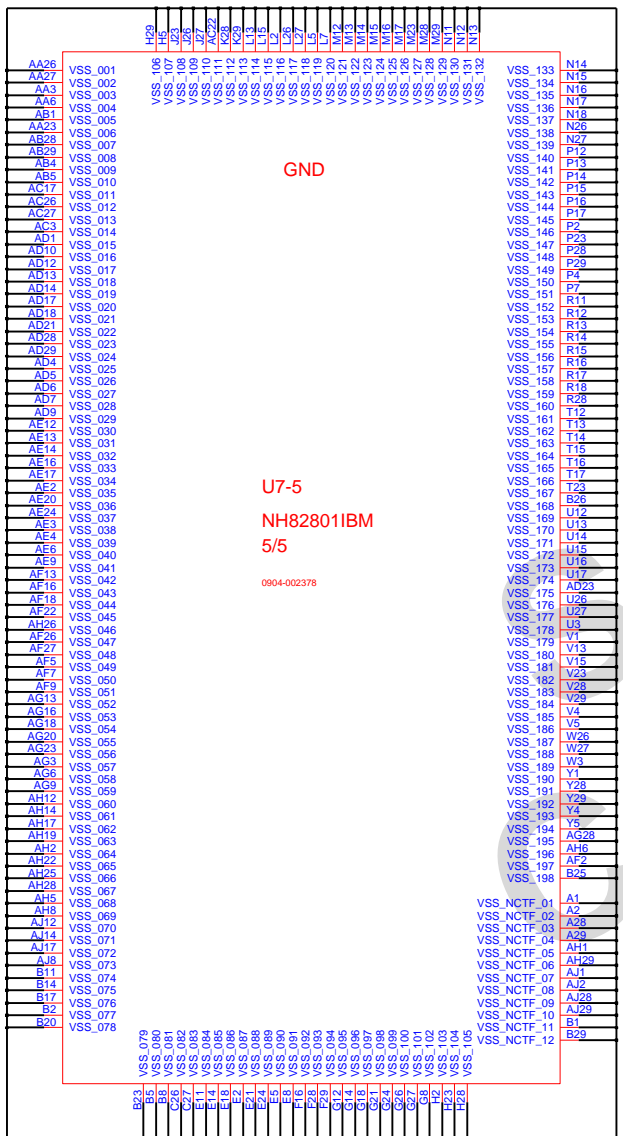
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DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		ICH_9M_B	
APPROVAL	HJ KIM	REV	1.0		ICH9-M (3/5)	PART NO. BA41-
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE 28	OF 55

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GND

U7-5  
NH828011BM  
5/5

0904-002378

Samsung  
Confidential

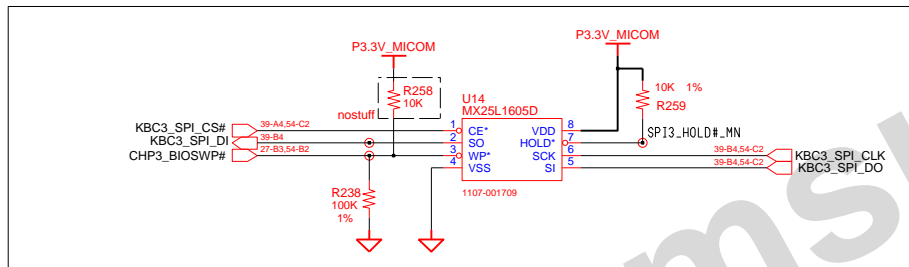
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CHECK	YM AN	DEV. STEP	PR		ICH9_M_B	
APPROVAL	HJ KIM	REV	1.0		ICH9-M (4/5)	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 29 OF 55	PART NO. BA41-

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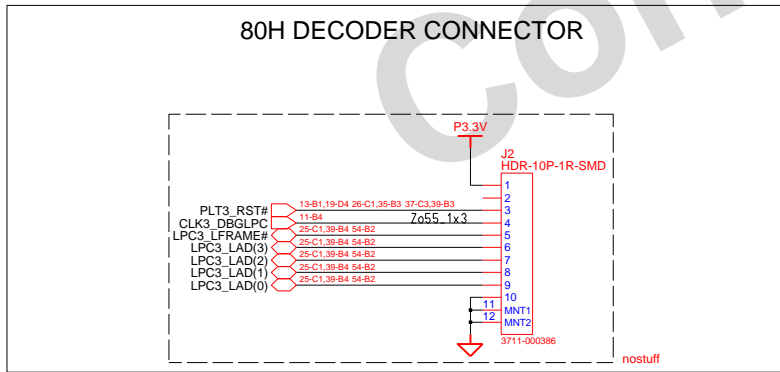
# SPI\_BIOS\_ROM

16MBit



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT ON-BOARD I/O PORT
		88	INIT BIOS DATA ROM
	WITH INITIAL POST VALUE	8A	INIT EXTENDED BIOS DATA AREA
14	INIT KEYBOARD CONTROLLER	8C	INIT FDD CONTROLLER
16	CHECK CHECKSUM	8E	SHADOW OPTION ROMS
18	8254 TIMER INIT	9A	SETUP POWER MANAGEMENT
1A	8237 DMA CONTROLLER INIT.	9E	ENABLE H/W INTERRUPT
1C	RESET INTERRUPT CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT TYPEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ENTER SETUP
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
32	COMPUTE THE CPU SPEED	B0	CHECK FOR ERRORS
34	TEST CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
38	SHADOW SYSTEM BIOS ROM	B4	ONE BEEP
3A	AUTO SIZING CACHE	B6	CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	B7	ACPI INIT
3D	LOAD ALTERNATE REG. WITH CMOS VALUE	BA	DMI INIT
42	INIT INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT BIOS INTERRUPT	C0	TRY BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT A20 SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
49	INIT PCI BUS AND DEVICE	D6	SHUTDOWN 5
4A	INIT ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	SHUTDOWN 10
52	TEST KEYBOARD	D9	ENABLE NMI
54	SET KEY CLICK IF ENABLED	90	INIT HDD CONTROLLER
56	ENABLE KEYBOARD	91	INIT LOCAL BUS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 2
5A	DISPLAY PRESS SETUP	94	DISABLE A20 ADDRESS LINE
5C	TEST RAM BETWEEN 812K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
60	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PATCH 1		

## 80H DECODER CONNECTOR



80port will be removed in MP stage.

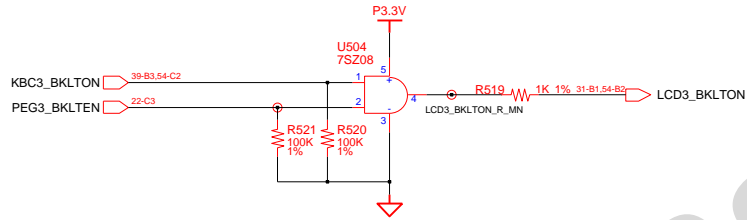
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	ICH_9M_B	PART NO.	
APPROVAL	HJ KIM	REV	1.0	ICH9-M (5/5)	BA41-	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE	30 OF 55

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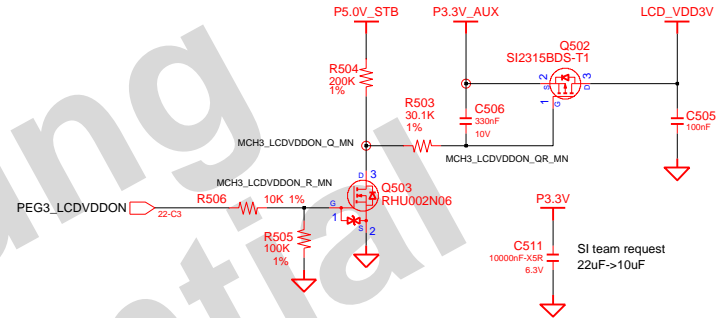
# LVDS

## Backlight On

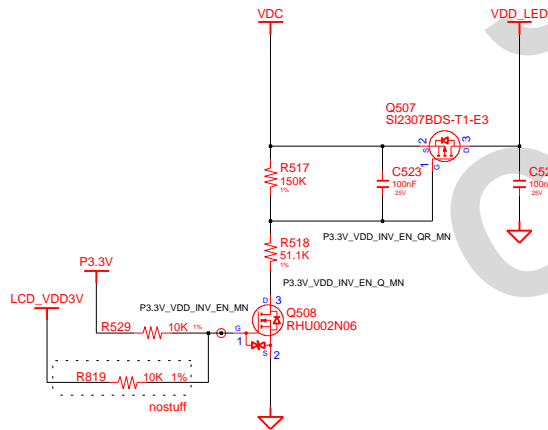


## LCD Power

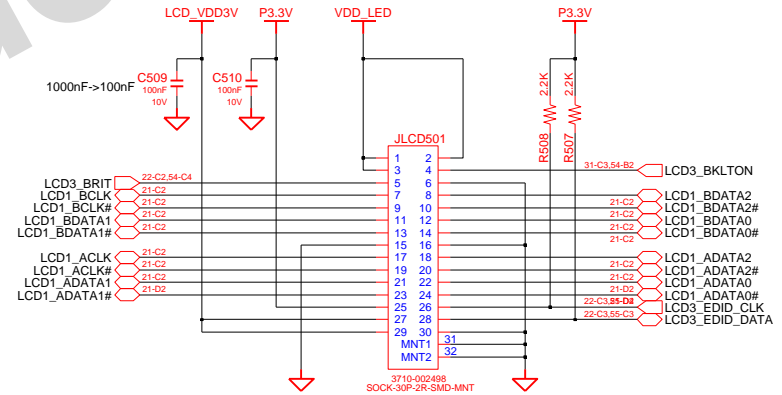
EBL Purpose



## LED Power



## 2Ch. LCD Connector



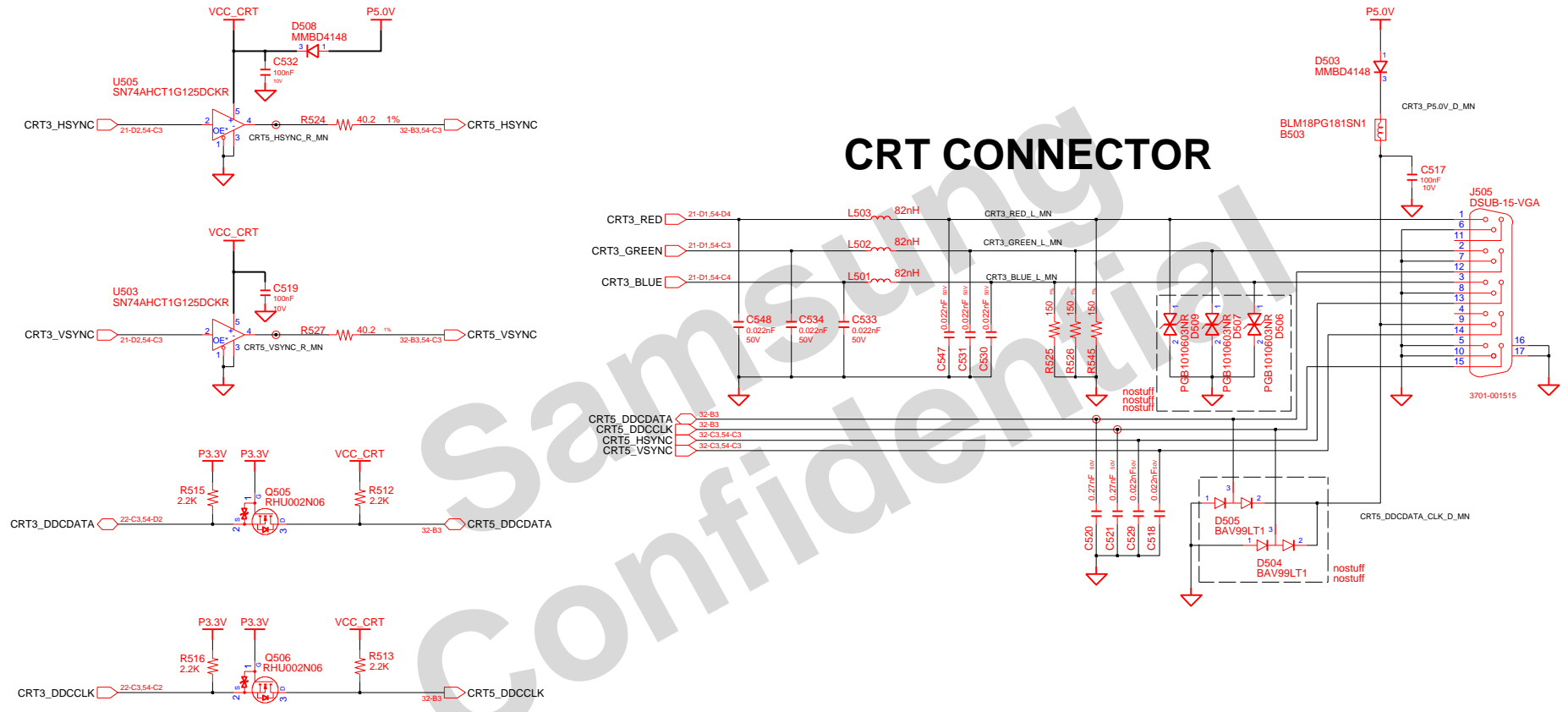
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CHECK	YM AN	DEV. STEP	PR		SPI_BIOS_ROM	ELECTRONICS
APPROVAL	HJ KIM	REV	1.0		SPI_BIOS_ROM	PART NO.
MODULE CODE		LAST EDIT				BA41-
				August 07, 2009 15:14:35 PM	PAGE 31	OF 55

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# CRT

## CRT CONNECTOR



Check "CRT3\_DDCCLK/DATA" Voltage Level  
2N06 Can be replaced with SM6K2

DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	GRAPHICS_IF	PART NO.	
APPROVAL	HJ KIM	REV	1.0	LVDS	BA41-	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 32 OF 55	

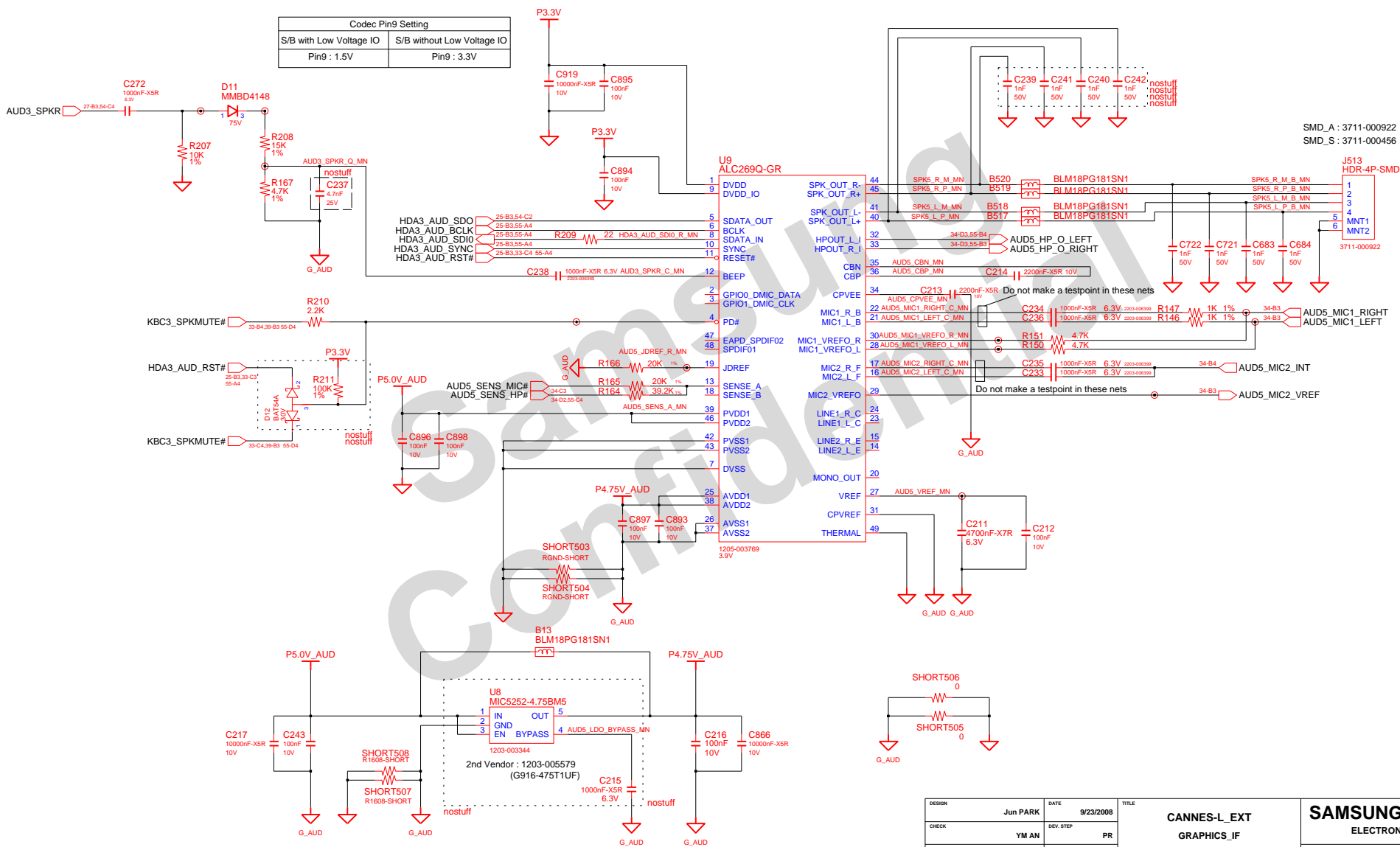


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# AUdio Codec (ALC269)

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



SMD\_A : 3711-000922  
SMD\_S : 3711-000456

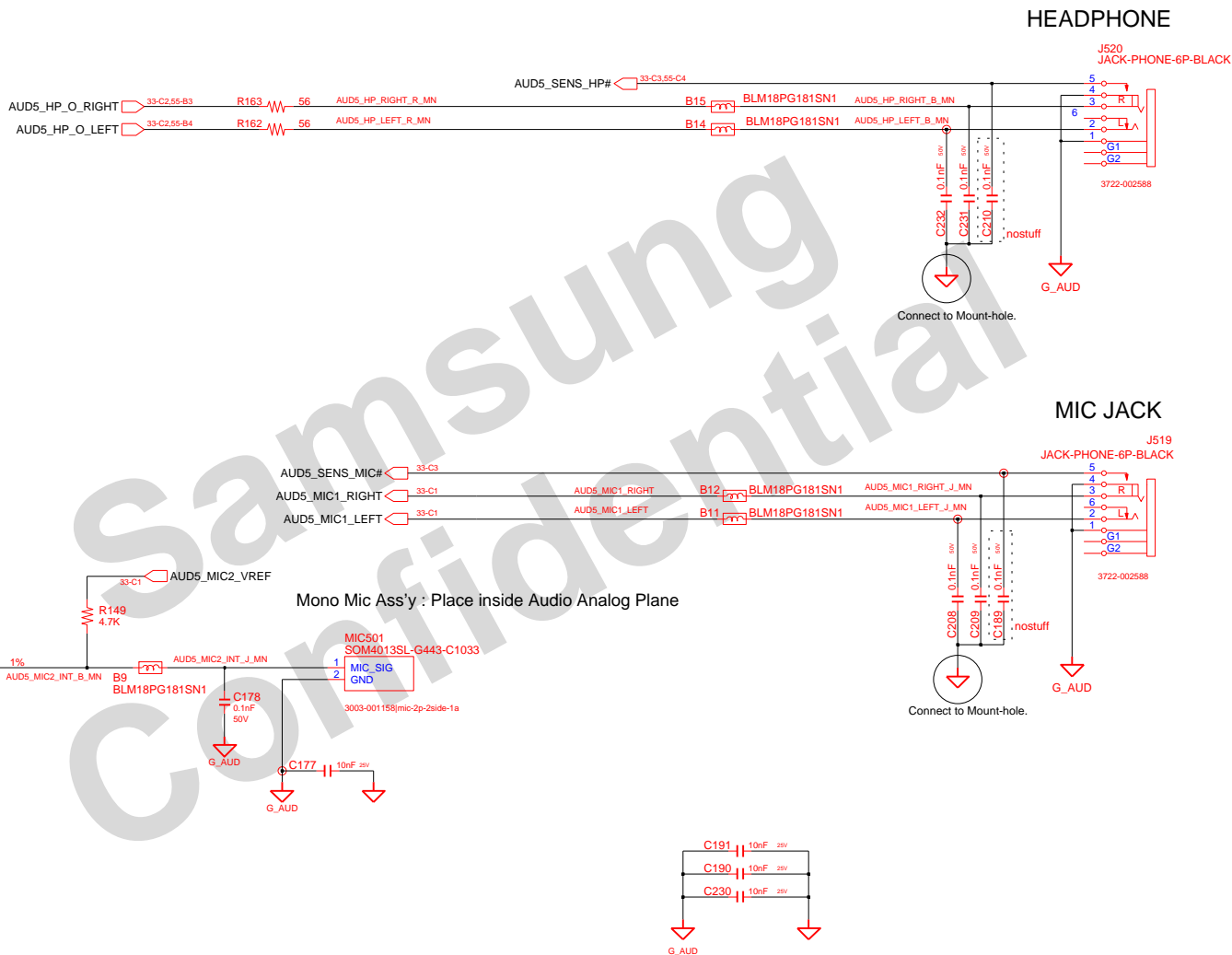
3711-000922

DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT
CHECK	YM AN	DEV. STEP	PR	GRAPHICS_IF	
APPROVAL	HJ KIM	REV	1.0	CRT	
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 33 OF 55

<b>SAMSUNG</b>
ELECTRONICS
PART NO. BA41-

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DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		HDA_CODEC	
APPROVAL	HJ KIM	REV	1.0		AUDIO CODEC ALC269_GR	PART NO. BA41-
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 34 OF 55	



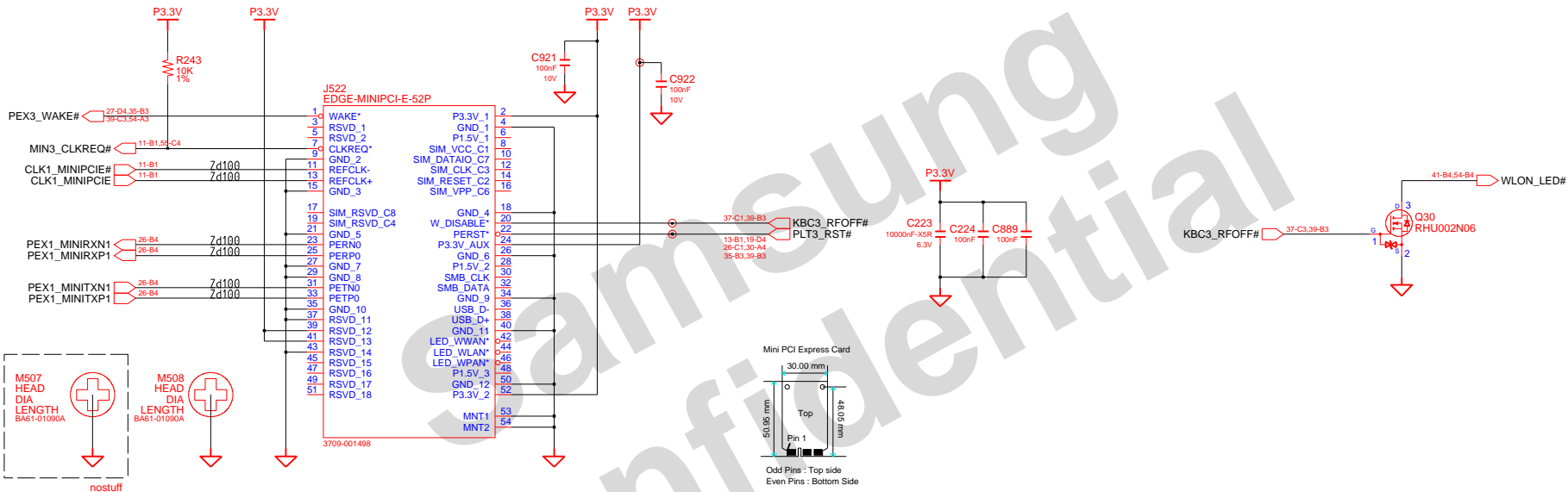


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# Wireless LAN

## WLAN, 4mm



PEM : WLAN minicard + Half minicard

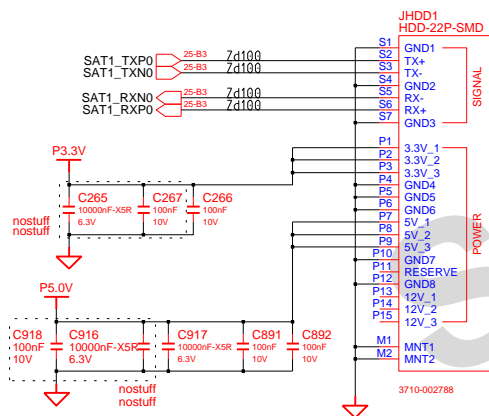
DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT MULTICARD 2 IN 1 CARD	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	PART NO.		
APPROVAL	HJ KIM	REV	1.0	BA41-		
MODULE CODE		LAST EDIT		August 07, 2009 15:14:35 PM	PAGE 37 OF 55	

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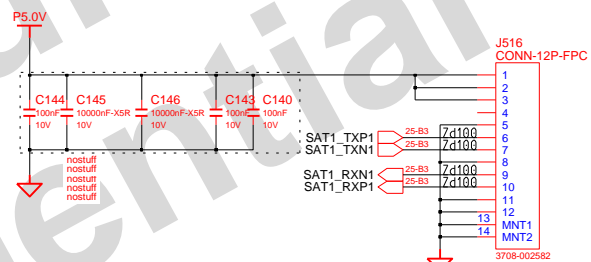
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# SATA I/F CONN

SATA HDD CONN



MAIN TO SUB SATA ODD CONN

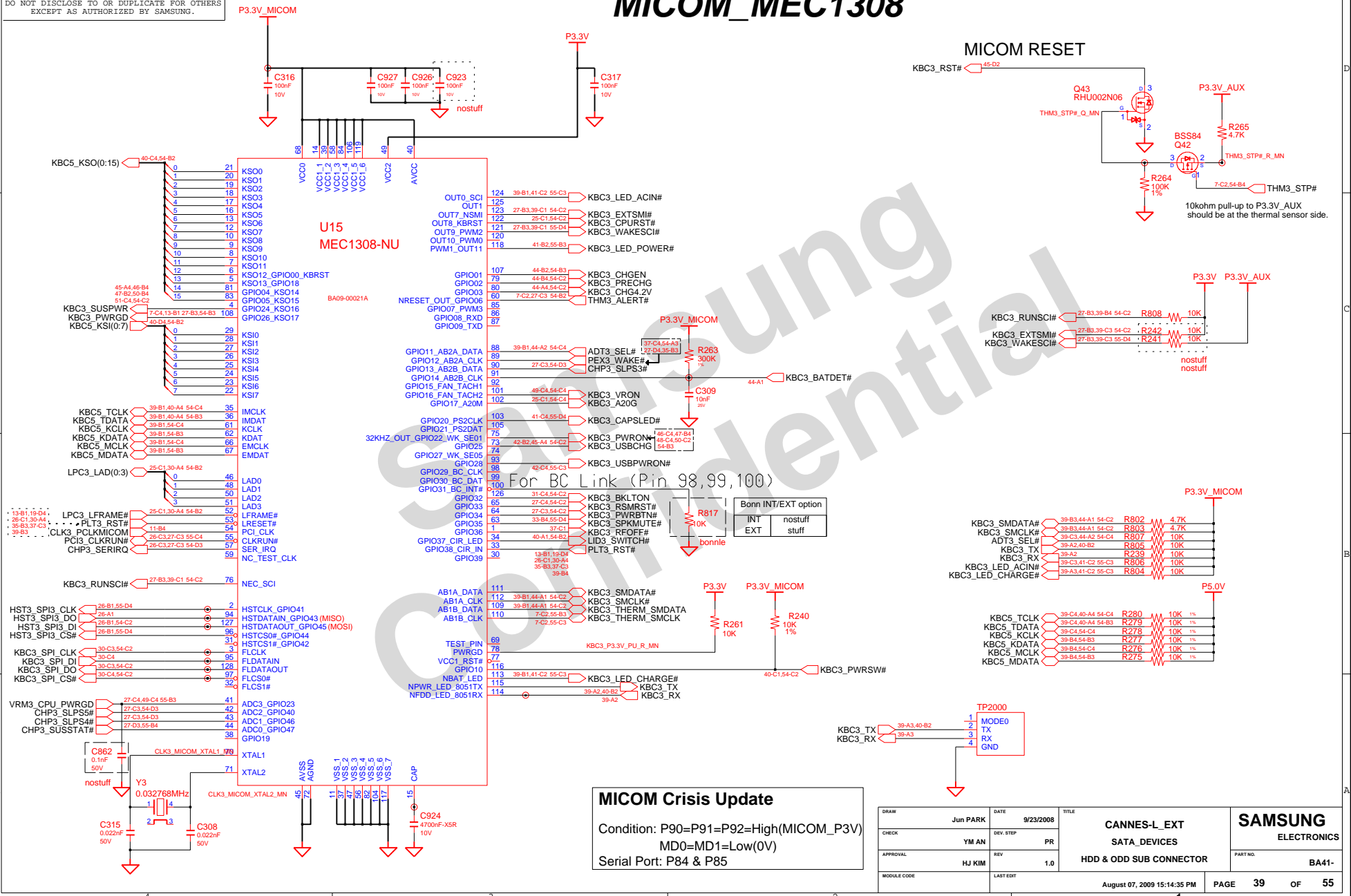


DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	MINI_PCIE_CONN	PART NO.	
APPROVAL	HJ KIM	REV	1.0	WLAN & HSDPA & SIM CARD	BA41-	
MODULE CODE		LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	38	OF 55

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# MICOM\_MEC1308



**MICOM Crisis Update**  
 Condition: P90=P91=P92=High(MICOM\_P3V)  
 MD0=MD1=Low(0V)  
 Serial Port: P84 & P85

DRAW		DATE	TITLE	SAMSUNG ELECTRONICS	
Jun PARK		9/23/2008	CANNES-L_EXT	PART NO. BA41-	
CHECK		DEV. STEP	SATA_DEVICES	PAGE 39 OF 55	
APPROVAL		REV	HDD & ODD SUB CONNECTOR	August 07, 2009 15:14:35 PM	
HJ KIM		1.0			
MODULE CODE		LAST EDIT			

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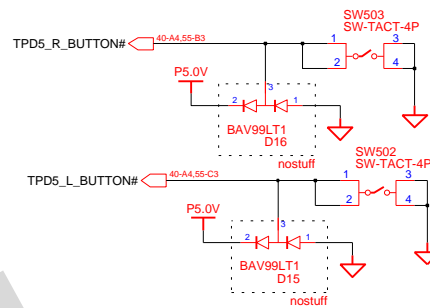
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# Micom Glue Logic

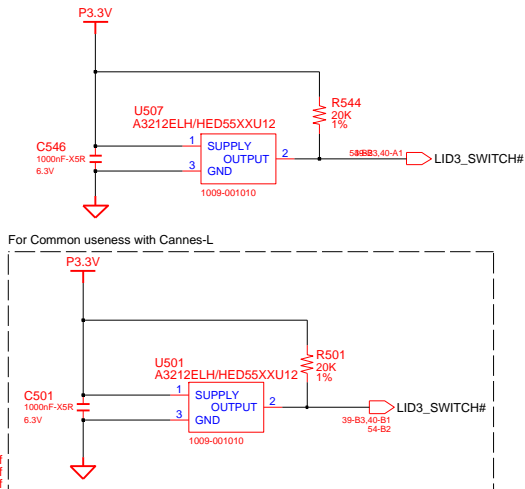
## KEYBOARD



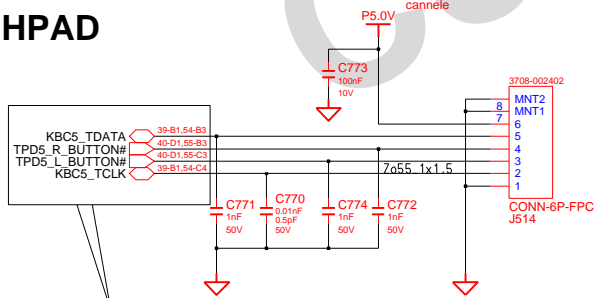
## Power Switch Button



## LID SWITCH



## TOUCHPAD



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR		MICOM	
APPROVAL	HJ KIM	REV	1.0		MICOM_SMSC MEC1308	PART NO.
MODULE CODE		LAST EDIT				BA41-
				August 07, 2009 15:14:35 PM	PAGE	40 OF 55



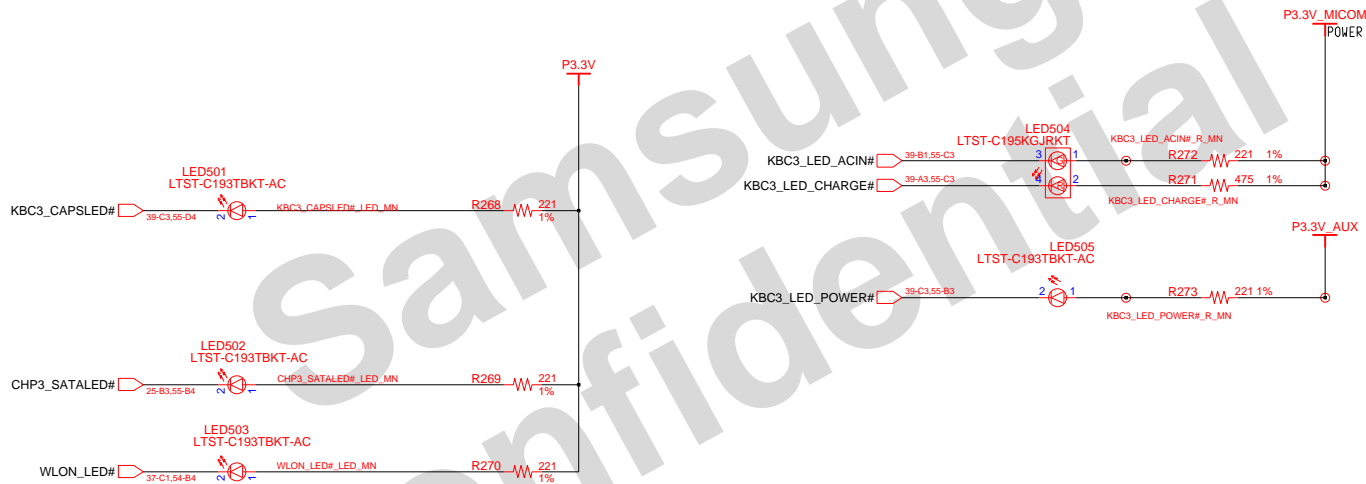
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# LEDs

## FUNCTION KEY LED

## ADAPTERIN/CHARGING LED



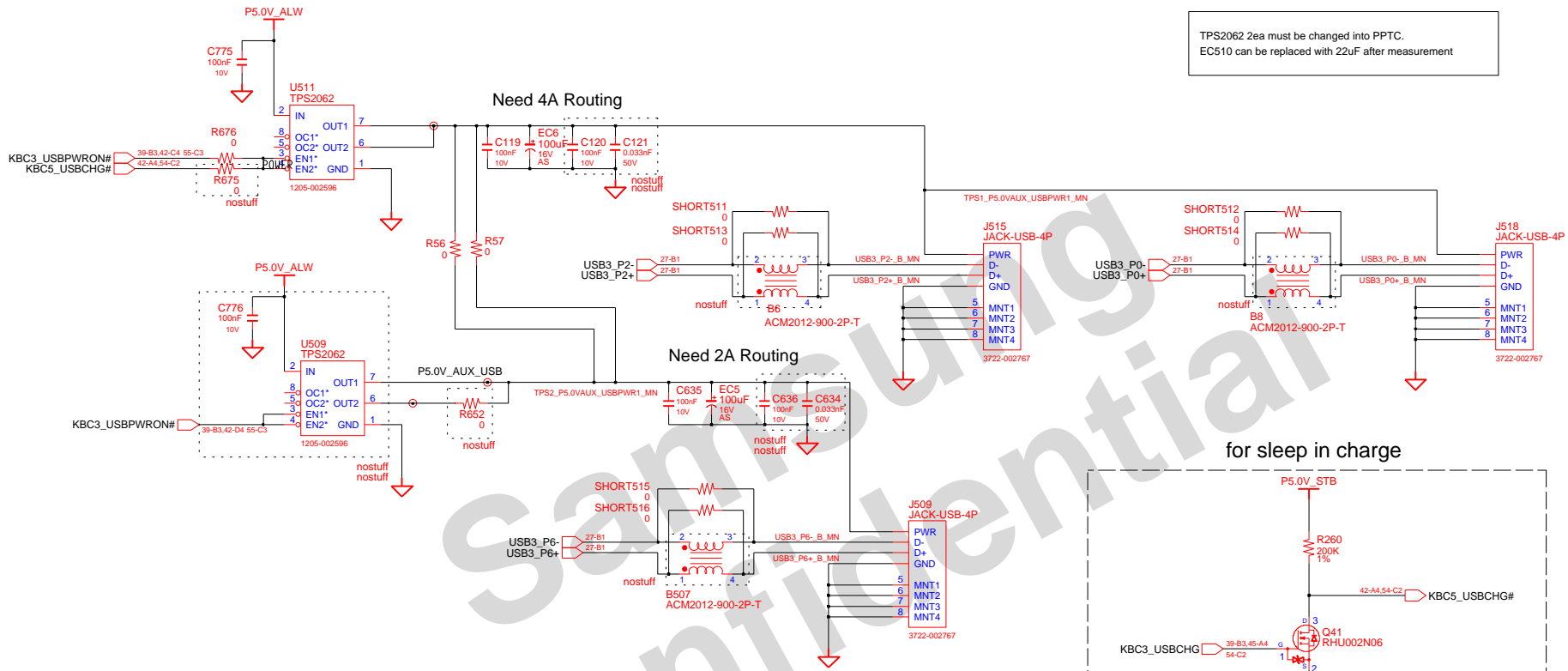
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT MICOM GLUE LOGIC KEYBOARD & TOUCHPAD	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	PART NO.		
APPROVAL	HJ KIM	REV	1.0	August 07, 2009 15:14:35 PM		PAGE 41 OF 55
MODULE CODE	LAST EDIT					

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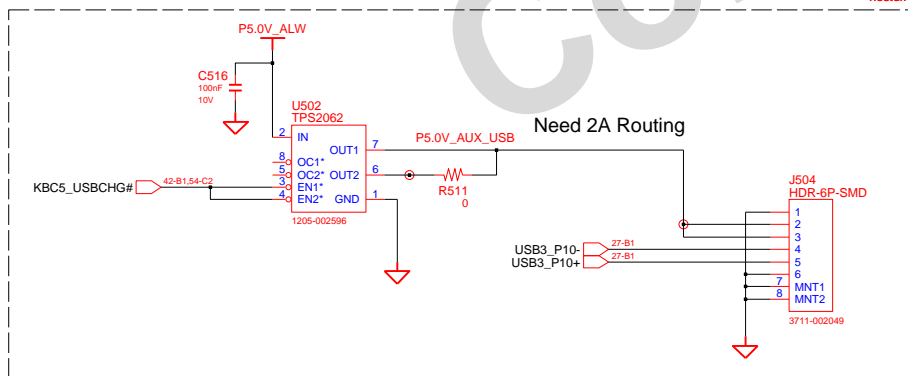
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# USB Single connector X 3 (Left)

TPS2062 2ea must be changed into PPTC.  
EC510 can be replaced with 22uF after measurement



## USB SUB B'D CONNECTOR



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV. STEP	PR		LED_SWITCH	
APPROVAL	HJ KIM	REV	1.0		LED_SWITCH	
MODULE CODE		LAST EDIT				
				August 07, 2009 15:14:35 PM	PAGE 42	OF 55

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# USB I/F Devices

## Bluetooth Interface

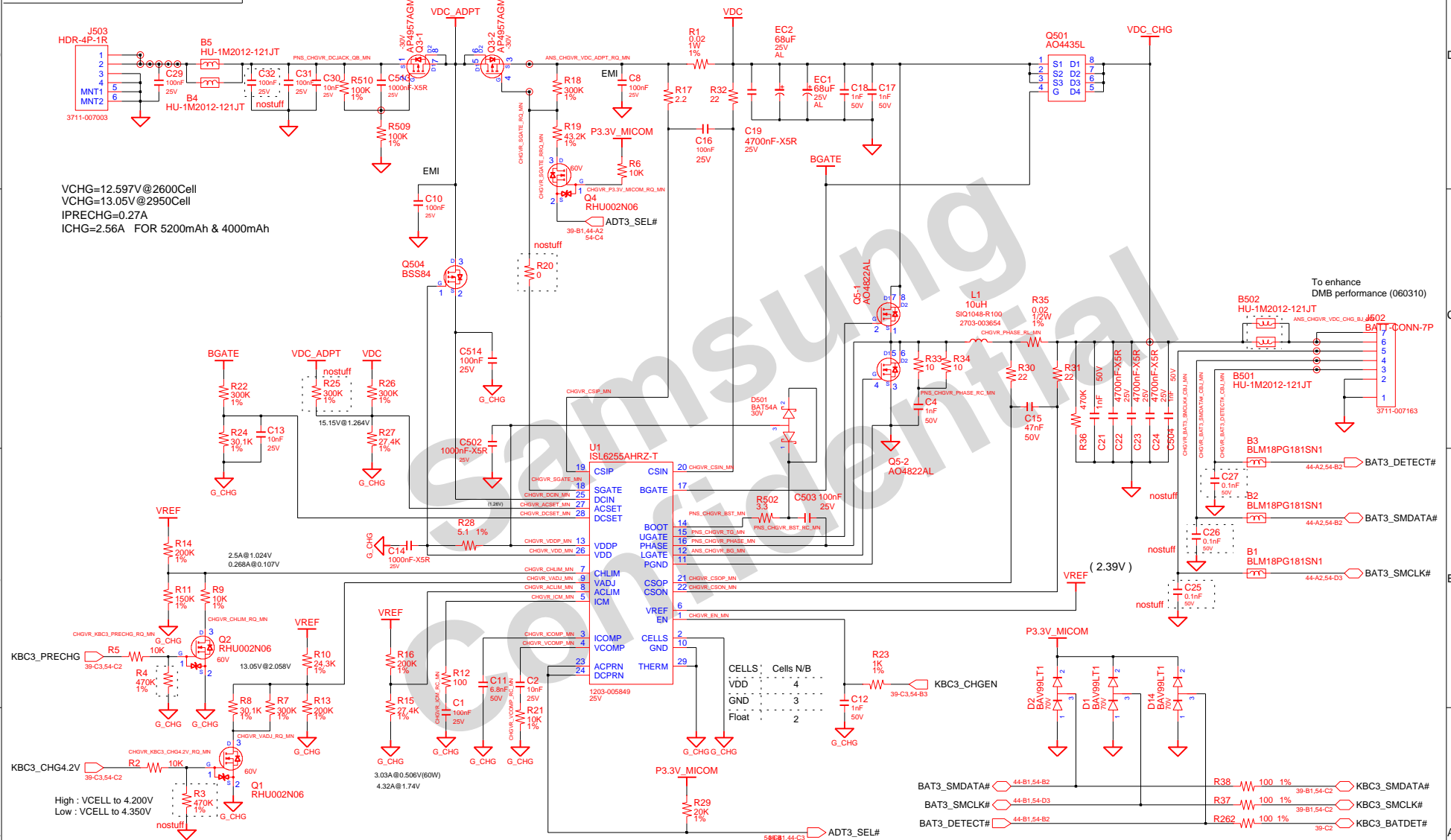
## CAMERA



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	USB_CONN		
APPROVAL	HJ KIM	REV	1.0	USB & eSATA	PART NO.	BA41-
MODULE CODE		LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	43	OF 55

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# CHARGE & POWER MANAGEMENT



VCHG=12.597V @2600Cell  
 VCHG=13.05V @2950Cell  
 IPRECHG=0.27A  
 ICHG=2.56A FOR 5200mAh & 4000mAh

To enhance DMB performance (060310)

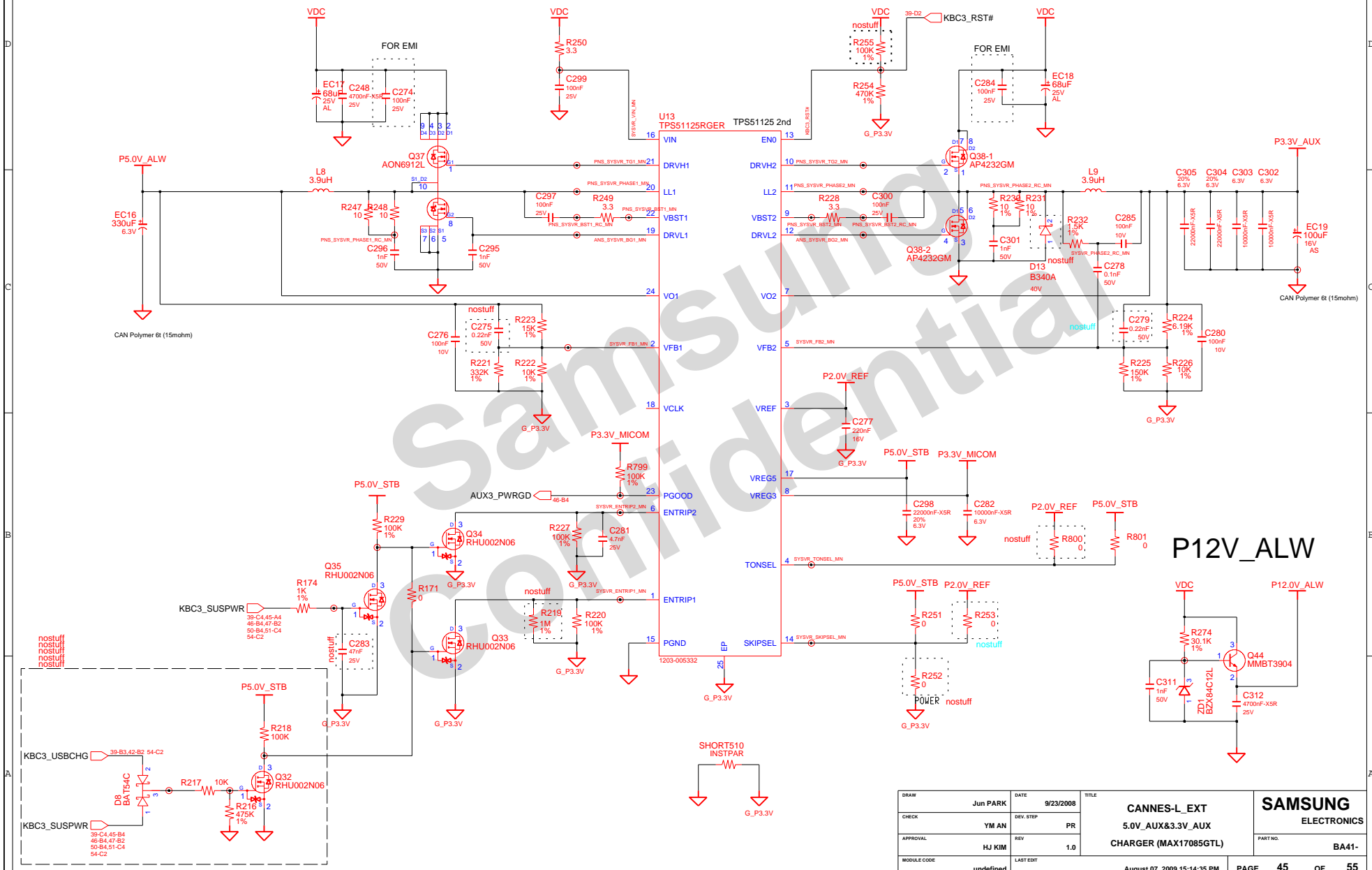
Adapter configuration				
60W / 3.03A / 96%		90W / 4.32A / 91.2%		
Value	SEC Code	Value	SEC Code	
Rtop	200K	2007-007334	10K	2007-007142
Rbot	27.4K	2007-007274	30.1K	2007-002910

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	<b>SAMSUNG</b> ELECTRONICS	
CHECK	YM AN	DEV. STEP	PR		USB_DEVICES		
APPROVAL	HJ KIM	REV	1.0		BLUETOOTH & CAMERA	PART NO.	
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	44	OF	55

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# P3.3V\_AUX & P5.0V\_ALW

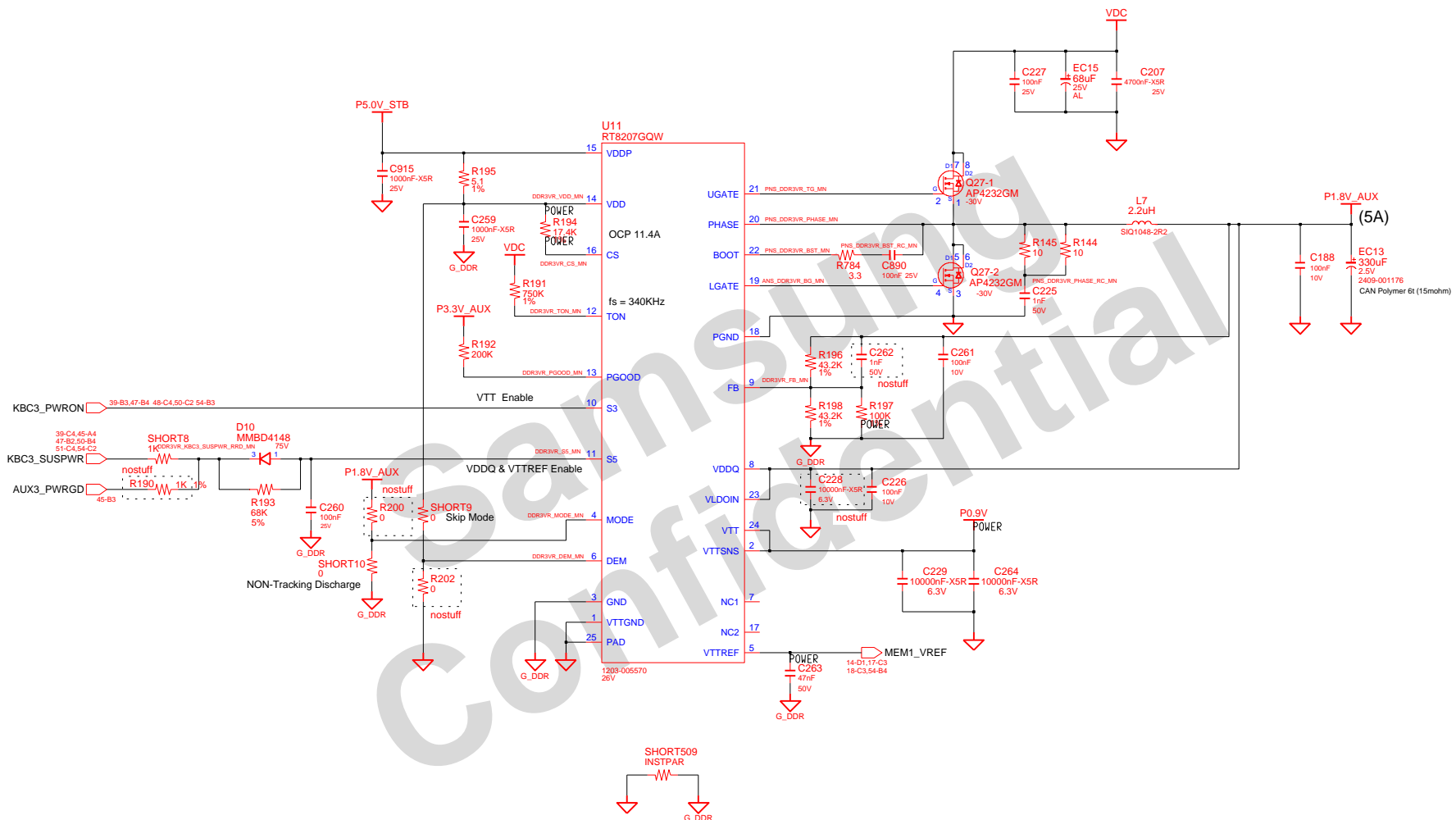


DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT 5.0V_AUX&3.3V_AUX CHARGER (MAX17085GTL)	<b>SAMSUNG</b> ELECTRONICS
CHECK	YM AN	DEV. STEP	PR			
APPROVAL	HJ KIM	REV	1.0		PART NO.	BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	45	OF 55

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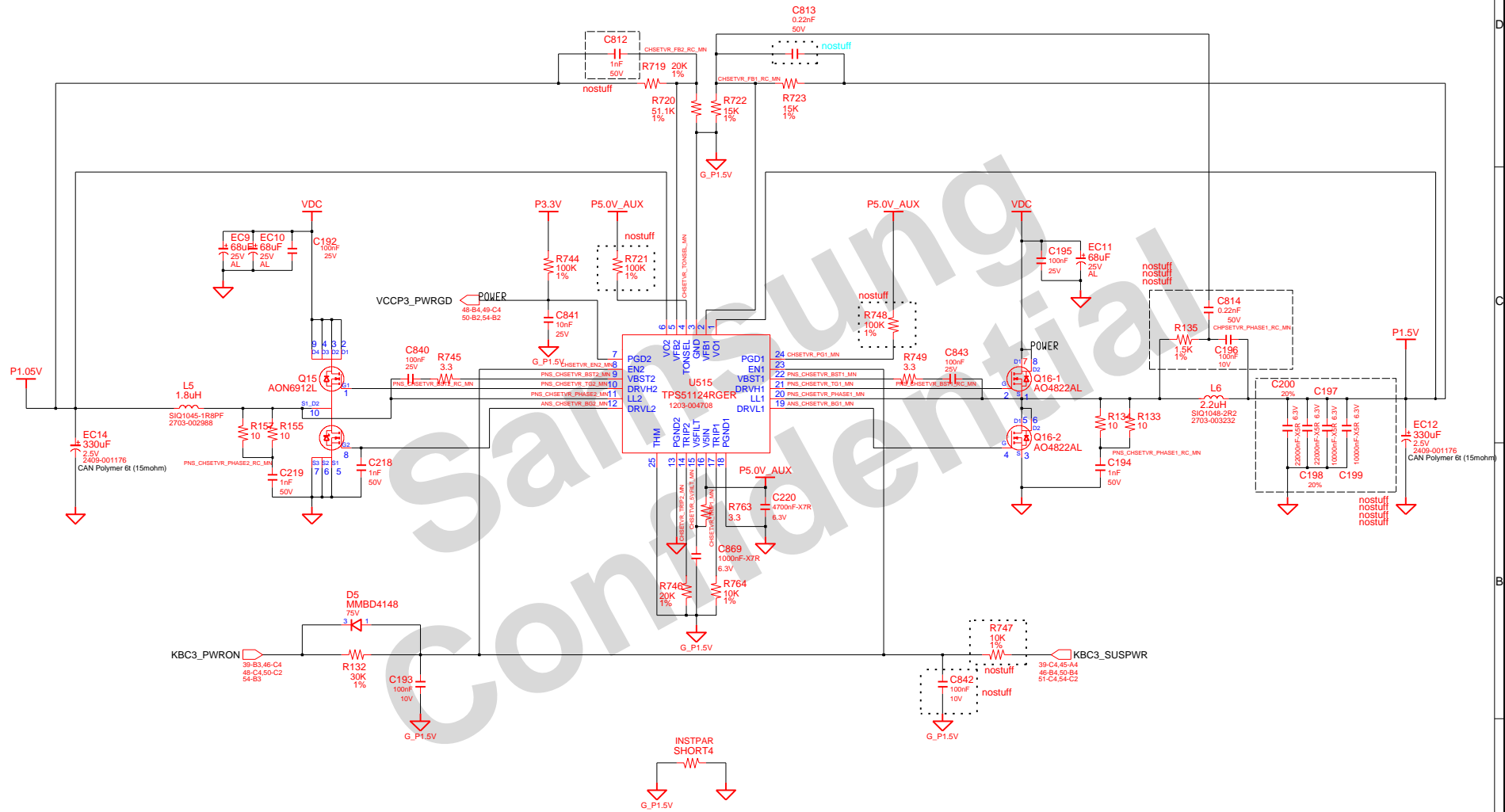
# DDR2 Power



DRAW	Jun PARK	DATE	01/09/2008	TITLE	<b>CANNES-L_EXT</b> <b>PWR_MV_3V_5V</b> <b>P3.3V_AUX / P5.0V_AUX</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b>
CHECK	YM AN	DEV. STEP	PR	PART NO.		
APPROVAL	HJ KIM	REV	1.0	BA41-		
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE 46 OF 55		

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# CHIPSET POWER(P1.5V\_AUX & P1.05V)



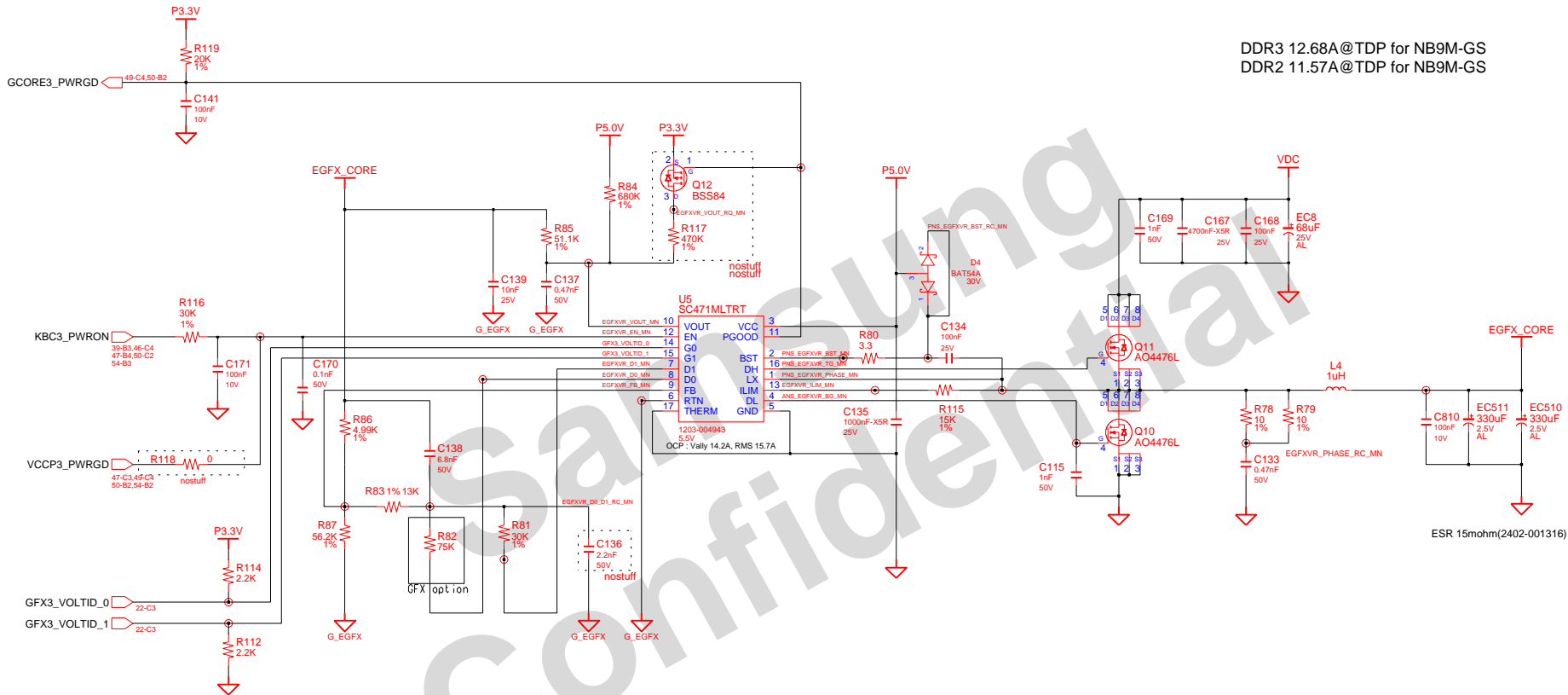
DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	PWR_MEMORY	PART NO.	
APPROVAL	HJ KIM	REV	1.0	DDR2 POWER	BA41-	
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	47	OF 55

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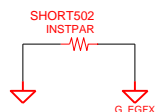
# Graphic Core Power

DDR3 12.68A@TDP for NB9M-GS  
DDR2 11.57A@TDP for NB9M-GS



GFX3_VOLTD		
G0	G1	
0	0	0.8V(0.8166V)
1	0	0.85V(0.8591V)
0	1	0.90V(0.9036V)
1	1	RESERVED

R845 GFX option		
LP	GE	
75K		(2007-001161)
30.1K		(2007-002910)



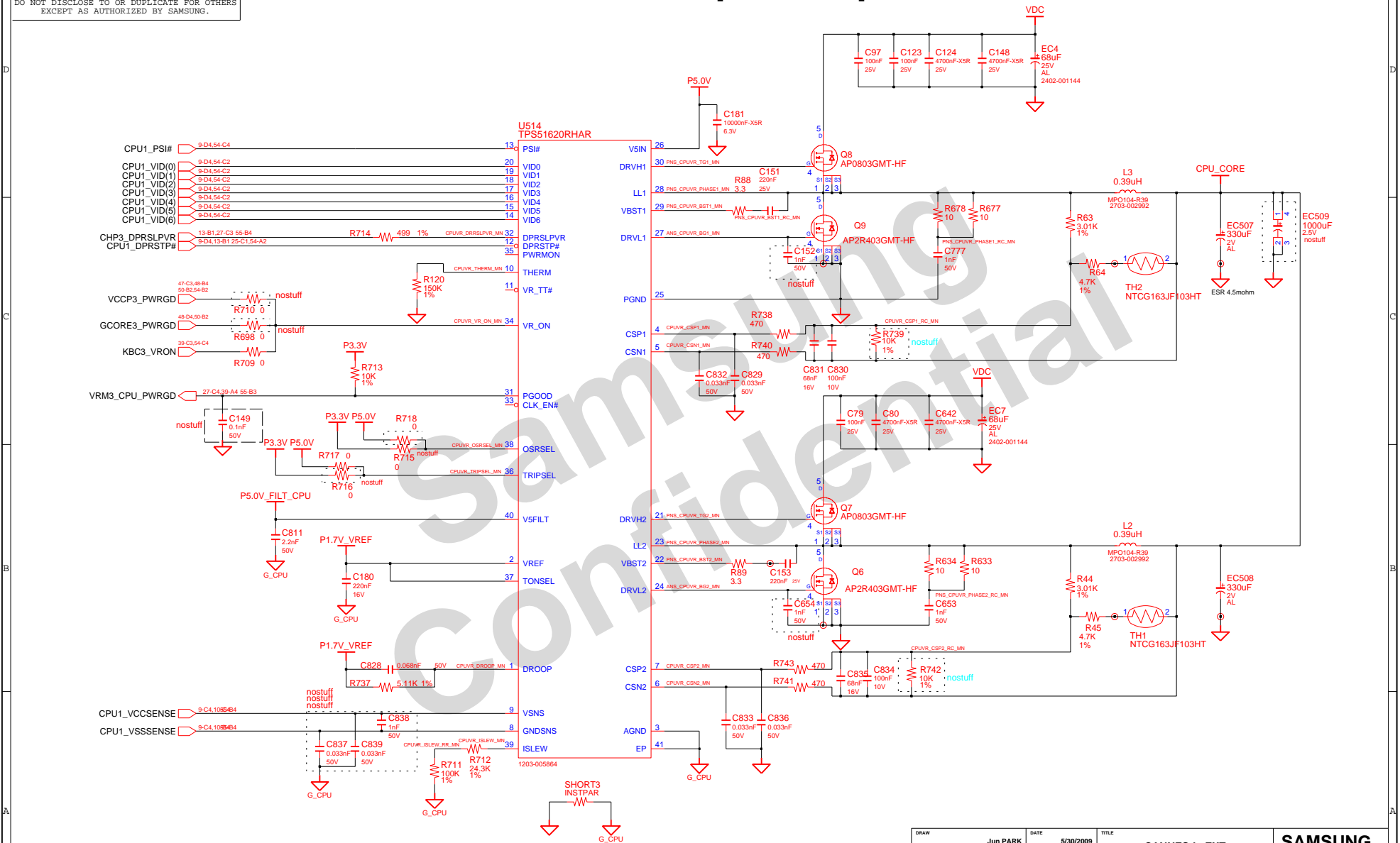
DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT PWR_MV_Cantiga P1.5V_AUX, P1.05V	SAMSUNG ELECTRONICS	
CHECK	YM AN	DEV. STEP	PR			PART NO. BA41-	
APPROVAL	HJ KIM	REV	1.0			August 07, 2009 15:14:35 PM	
MODULE CODE	LAST EDIT		PAGE 48		OF 55		



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# CPU VRM [TI IMVP6+]



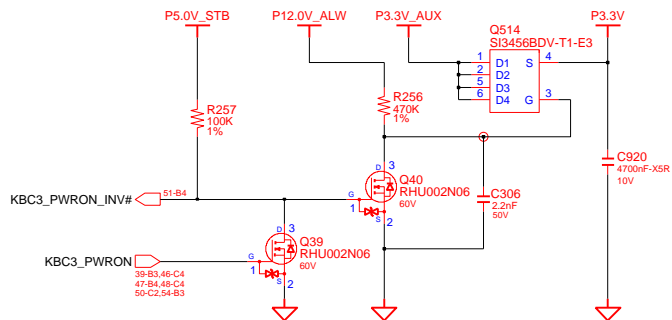
DRAW	Jun PARK	DATE	5/30/2009	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV. STEP	PR	PWR GFX		
APPROVAL	HJ KIM	REV	1.0	GFX Power		PART NO.
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	49	OF 55

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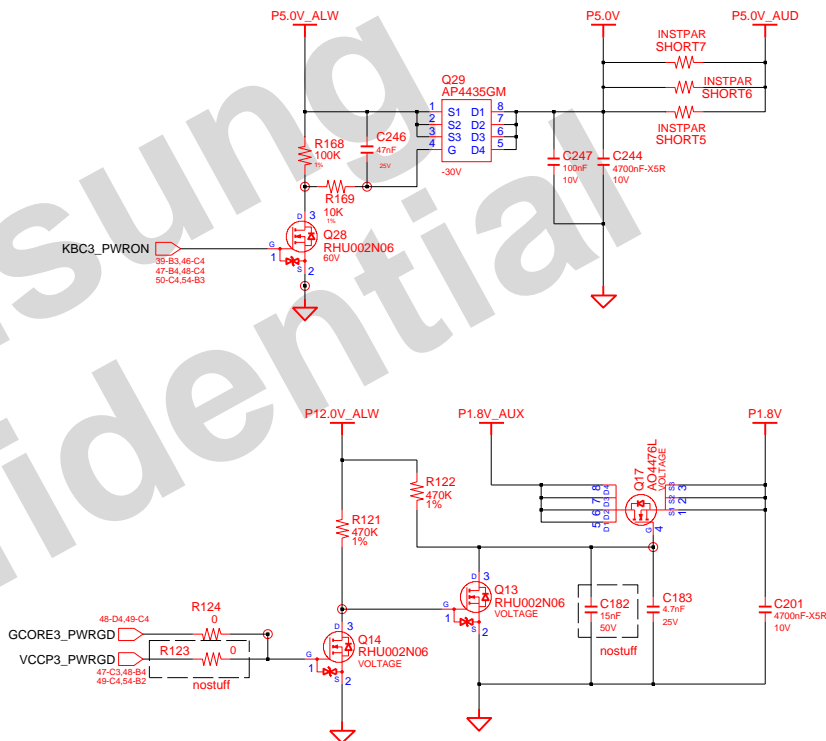
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# Switched Power

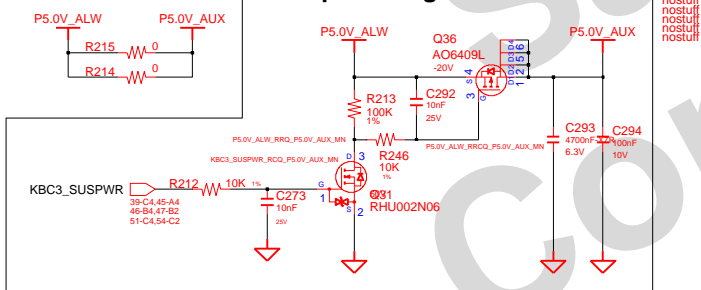
## Switched Power On (P3.3V)



## Switched Power On (P5.0V)



## Sleep'n Charger



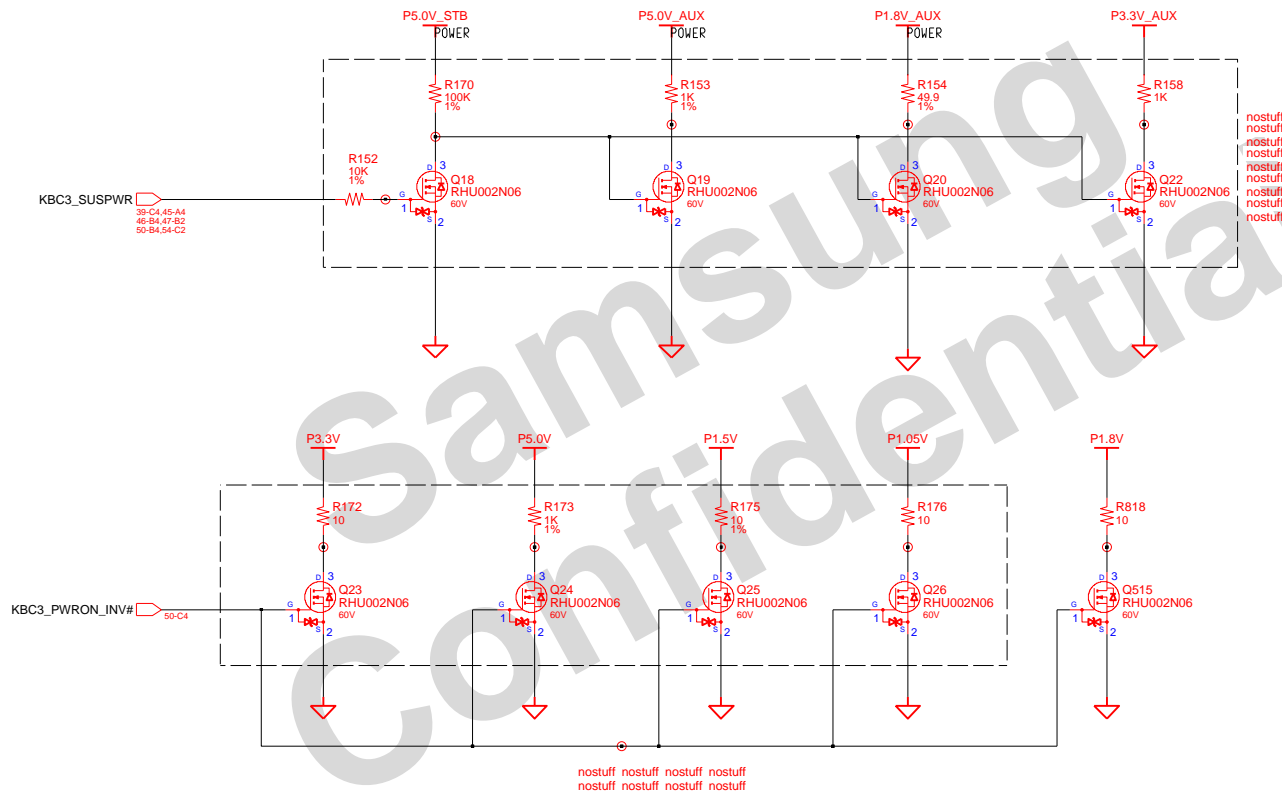
DRAW	Jun PARK	DATE	9/23/2008	TITLE	<b>CANNES-L_EXT</b> <b>PWR_CPU_MV_TPS51620</b> <b>CPUI VRM (IMVP6+)</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO. <b>BA41-</b>
CHECK	YM AN	DEV. STEP	PR			
APPROVAL	HJ KIM	REV	1.0			
MODULE CODE		LAST EDIT	August 07, 2009 15:14:35 PM	PAGE <b>50</b> OF <b>55</b>		

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# POWER DISCHARGER

This page will be deleted in PV stage.

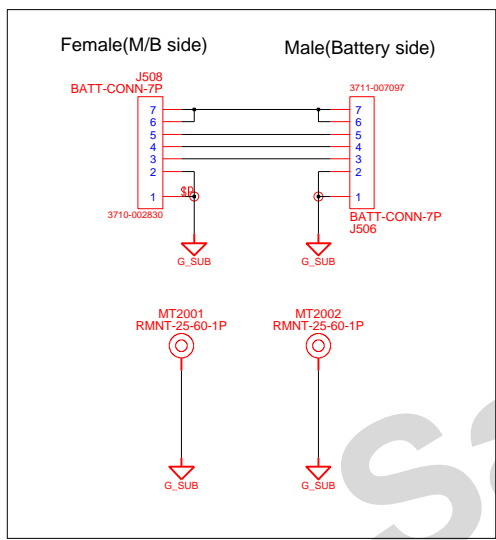


DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	PWR_MV_SWITCHED		
APPROVAL	HJ KIM	REV	1.0	SWITCHED POWER	PART NO.	BA41-
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE	51	OF 55

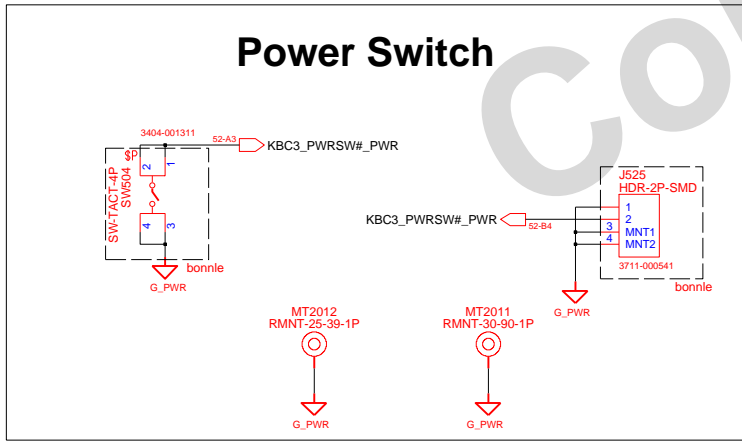
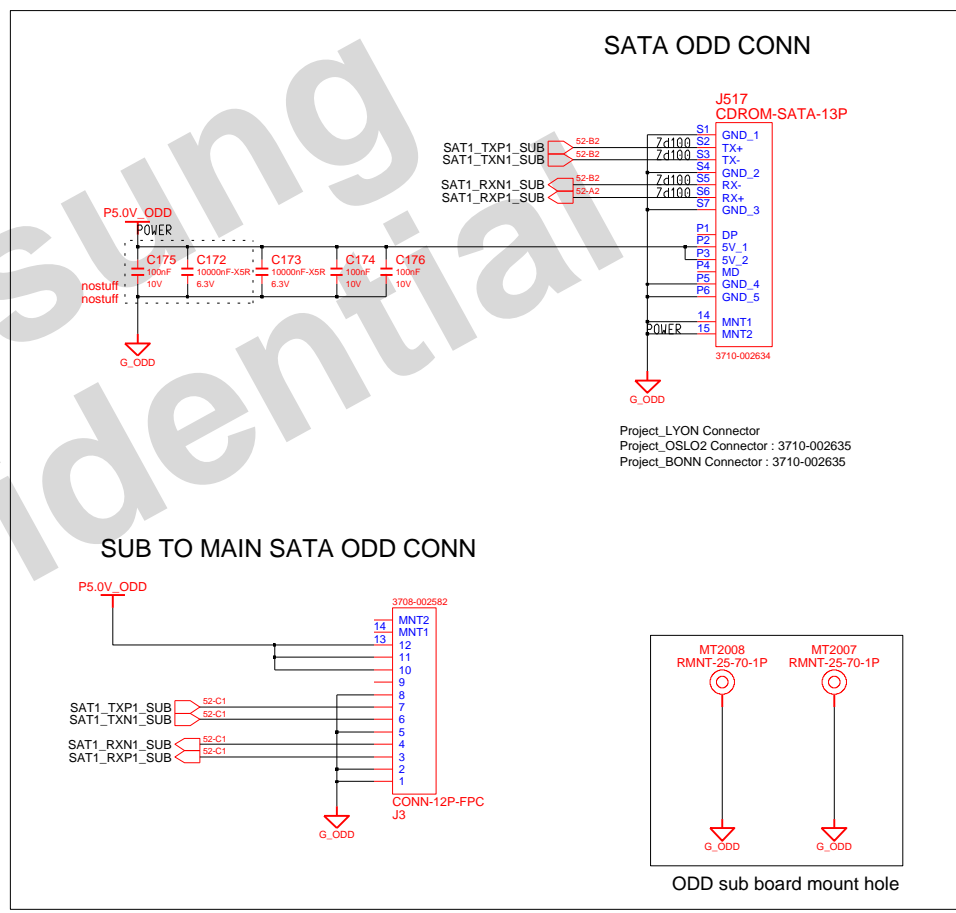
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# Battery & SATA ODD SUBBOARD



## SATA ODD SUB BOARD

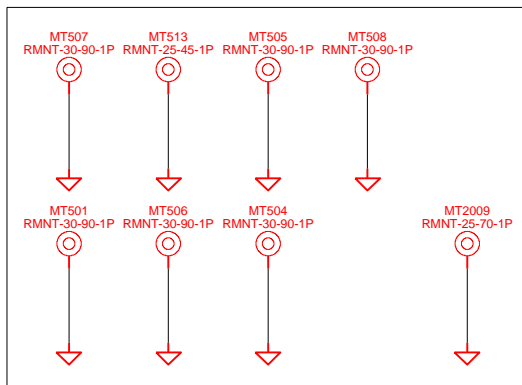


DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-
CHECK	YM AN	DEV.STEP	PR	PWR_MV_DISCHARGER		
APPROVAL	HJ KIM	REV	1.0	DISCHARGING LOGIC		
MODULE CODE	undefined	LAST EDIT	August 07, 2009 15:14:35 PM	PAGE 52 OF 55		

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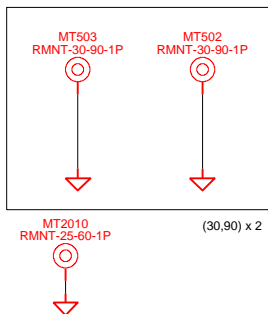
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**Mainboard Mount**



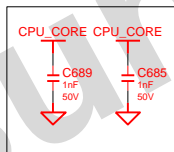
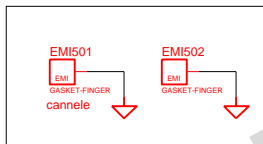
(30.90) x 7, (25.70) x 1

**Keyboard Mount**

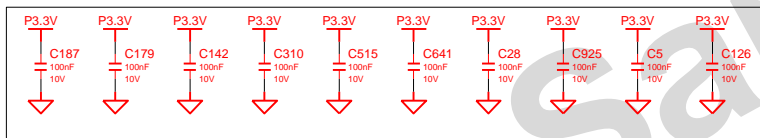


(30.90) x 2

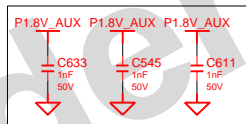
**EMI FINGER**



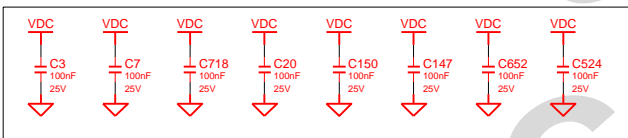
Add for EMC (Top), 2008.11.19



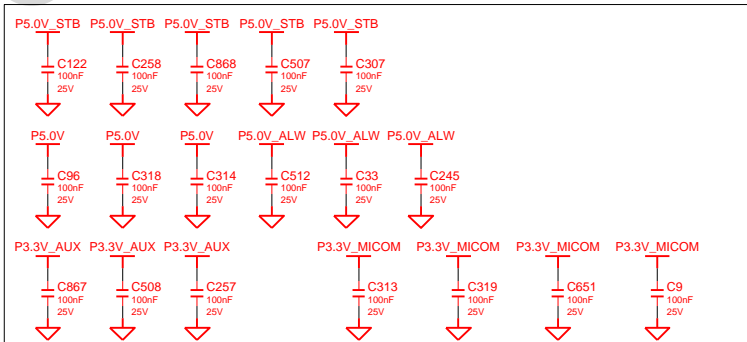
Add for EMC (5th Layer), 2008.11.19



Add for EMC (Bottom), 2008.11.19



Add for EMC (Bottom), 2008.11.19



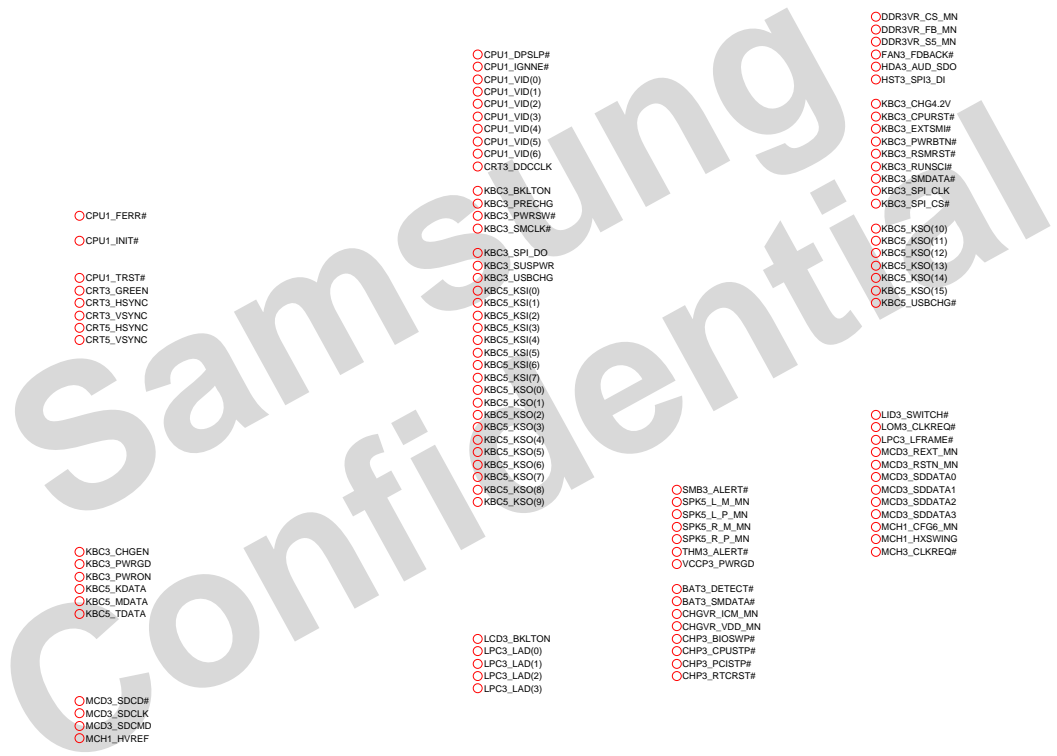
Add for EMC (Bottom), 2009.01.28

DRAW	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT SUB BOARD2	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	REV		
APPROVAL	HJ KIM	REV	1.0	MODULE CODE	SATA ODD SUB BOARD	PART NO. BA41-
				LAST EDIT	August 07, 2009 15:14:35 PM	PAGE 53 OF 55

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- CPU1\_NMI
- CPU1\_TCK
- CPU1\_TDI
- CPU1\_TMS
- CRT3\_RED
- FAN5\_VDD
- SMB3\_CLK
- ADT3\_SEL#
- AUD3\_SPKR
- CPU1\_PSI#
- CPU1\_SMI#
- CRT3\_BLUE
- KBC3\_A20G
- KBC3\_VRON
- KBC5\_KCLK
- KBC5\_MCLK
- KBC5\_TCLK
- LCD3\_BRIT
- MCD3\_SDWP
- MEM1\_VREF
- SMB3\_DATA
- THM3\_STP#
- WLON\_LED#
- PEX3\_WAKE#
- CPU1\_FERR#
- CPU1\_INIT#
- CPU1\_TRST#
- CRT3\_GREEN
- CRT3\_HSYNC
- CRT3\_VSYNC
- CRT5\_HSYNC
- CRT5\_VSYNC
- KBC3\_CHGEN
- KBC3\_PWRGD
- KBC3\_PWRON
- KBC5\_KDATA
- KBC5\_MDATA
- KBC5\_TDATA
- MCD3\_SDCD#
- MCD3\_SDCLK
- MCD3\_SDCMD
- MCH1\_HVREF
- AUD5\_CBP\_MN
- BAT3\_SMCLK#
- CHGVR\_EN\_MN
- CHP3\_GPIO18
- CHP3\_GPIO20
- CHP3\_SERIRQ
- CHP3\_SLPS3#
- CHP3\_SLPS4#
- CHP3\_SLPS5#
- CPU1\_DPSLP#
- CPU1\_IENNE#
- CPU1\_VID(0)
- CPU1\_VID(1)
- CPU1\_VID(2)
- CPU1\_VID(3)
- CPU1\_VID(4)
- CPU1\_VID(5)
- CPU1\_VID(6)
- CRT3\_DCCCLK
- KBC3\_BKLTON
- KBC3\_PRECHG
- KBC3\_PWRSW#
- KBC3\_SMCLK#
- KBC3\_SPI\_DO
- KBC3\_SUSPWR
- KBC3\_USBCHG
- KBC5\_KSI(0)
- KBC5\_KSI(1)
- KBC5\_KSI(2)
- KBC5\_KSI(3)
- KBC5\_KSI(4)
- KBC5\_KSI(5)
- KBC5\_KSI(6)
- KBC5\_KSI(7)
- KBC5\_KSO(0)
- KBC5\_KSO(1)
- KBC5\_KSO(2)
- KBC5\_KSO(3)
- KBC5\_KSO(4)
- KBC5\_KSO(5)
- KBC5\_KSO(6)
- KBC5\_KSO(7)
- KBC5\_KSO(8)
- KBC5\_KSO(9)
- LCD3\_BKLTON
- LPC3\_LAD(0)
- LPC3\_LAD(1)
- LPC3\_LAD(2)
- LPC3\_LAD(3)
- CPU1\_CPURST#
- CPU1\_DPRSTP#
- CPU1\_STPCLK#
- CPU2\_THERMDA
- CPU2\_THERMDC
- CRT3\_DCCDATA
- DDR3V3\_CS\_MN
- DDR3V3\_FB\_MN
- DDR3V3\_S5\_MN
- FAN3\_FDBACK#
- HDA3\_AUD\_SDO
- HST3\_SPI3\_DI
- KBC3\_CHG4.2V
- KBC3\_CPURST#
- KBC3\_EXTSMI#
- KBC3\_PWRBTN#
- KBC3\_RSMRST#
- KBC3\_RUNSCI#
- KBC3\_SMDATA#
- KBC3\_SPL\_CLK
- KBC3\_SPL\_CS#
- KBC5\_KSO(10)
- KBC5\_KSO(11)
- KBC5\_KSO(12)
- KBC5\_KSO(13)
- KBC5\_KSO(14)
- KBC5\_KSO(15)
- KBC5\_USBCHG#
- LID3\_SWITCH#
- LOM3\_CLKREG#
- LPC3\_LFRAME#
- MCD3\_REXT\_MN
- MCD3\_RSTN\_MN
- MCD3\_SDDATA0
- MCD3\_SDDATA1
- MCD3\_SDDATA2
- MCD3\_SDDATA3
- MCH1\_CFG6\_MN
- MCH1\_HXSWING
- MCH3\_CLKREG#
- BAT3\_DETECT#
- BAT3\_SMDATA#
- CHGVR\_ICM\_MN
- CHGVR\_VDD\_MN
- CHP3\_BIOSWTP#
- CHP3\_CPUSTP#
- CHP3\_POISTP#
- CHP3\_RTCSRST#



DESIGN	Jun PARK	DATE	9/23/2008	TITLE	CANNES-L_EXT	SAMSUNG ELECTRONICS
CHECK	YM AN	DEV.STEP	PR	ICT PORT		
APPROVAL	HJ KIM	REV	1.0	ICT PORT		PART NO. BA41-
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