ZZZ1	ZZZ2	ZZZ3	ZZZ4	ZZZ5	ZZZ6
PCB	PCB	Power Switch	Left LED	Right LED	Touch Sensor
	DAZ@	DAZ@	DAZ@	DAZ@	DAZ@

JIWA1/A2

Schematics Document

Compal confidential

Mobile Penryn uFCPGA

Intel Cantiga_GM/PM+ICH9-M

Saturday, June 06, 2009

REV:2.0

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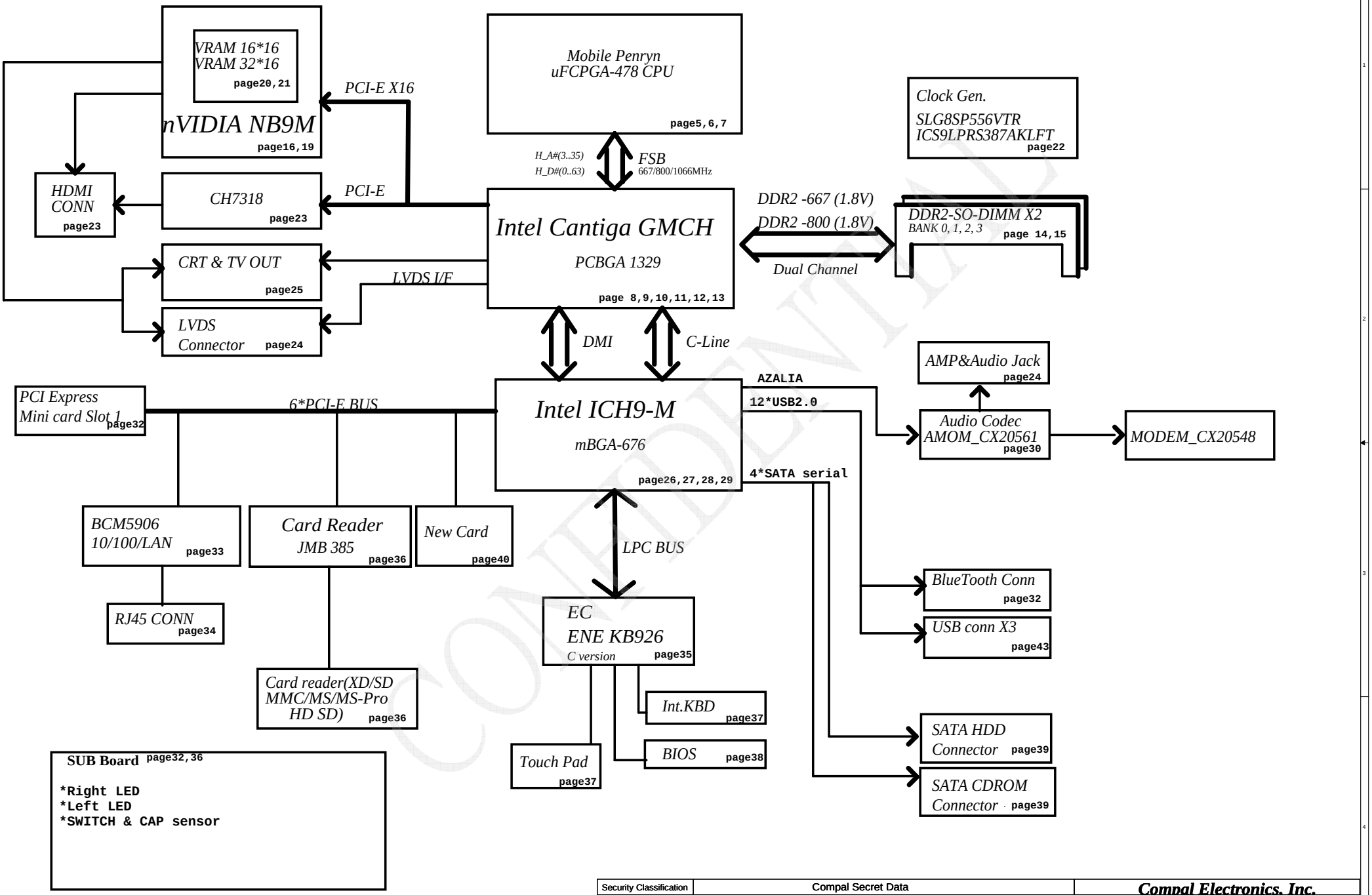
Right LED Board | **Swithch & CAP SENSE LEDs Board** | **Left LED Board**



SUB Board page32,36

*Right LED
*Left LED
*SWITCH & CAP sensor

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM@
GM@
X76@

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

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Voltage Rails

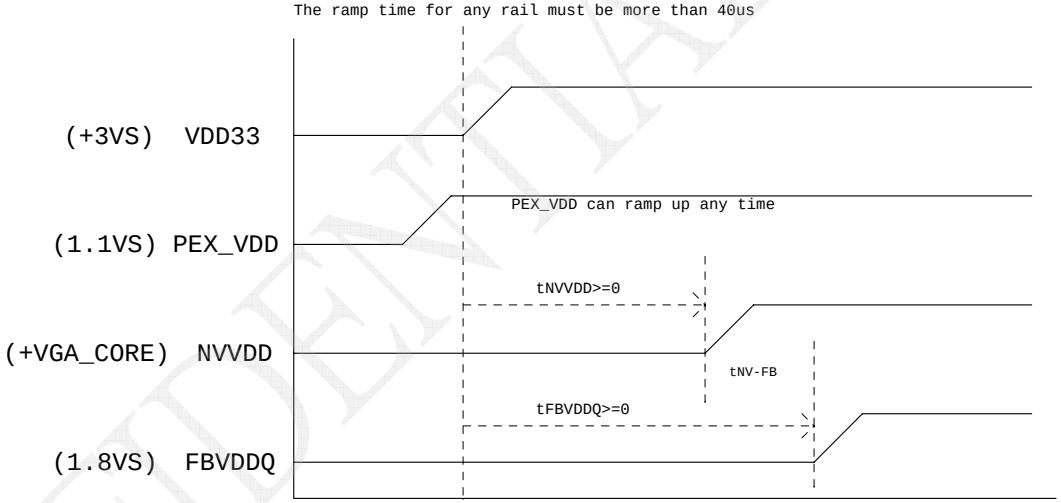
Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EDP at Tj = 97C*

Power Supply Rail	(V)	NB9M-GS		NB9M-GE	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	12.68A	11.57A	10.52A	9.59A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1400mA			
PEX_PLLVDD	1.1	110mA			
PLLVDD	1.1	65mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.225A			
FBVDD/Q	1.8	3080mA	1720mA	3010mA	1680mA
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	3.6A	2.24A	3.53A	2.2A
DACA_VDD	3.3	130mA			
DACB_VDD	3.3	255mA			
DACC_VDD	3.3	130mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	110mA			
TOTAL	3.3	0.645A			

POWER SQUENCE



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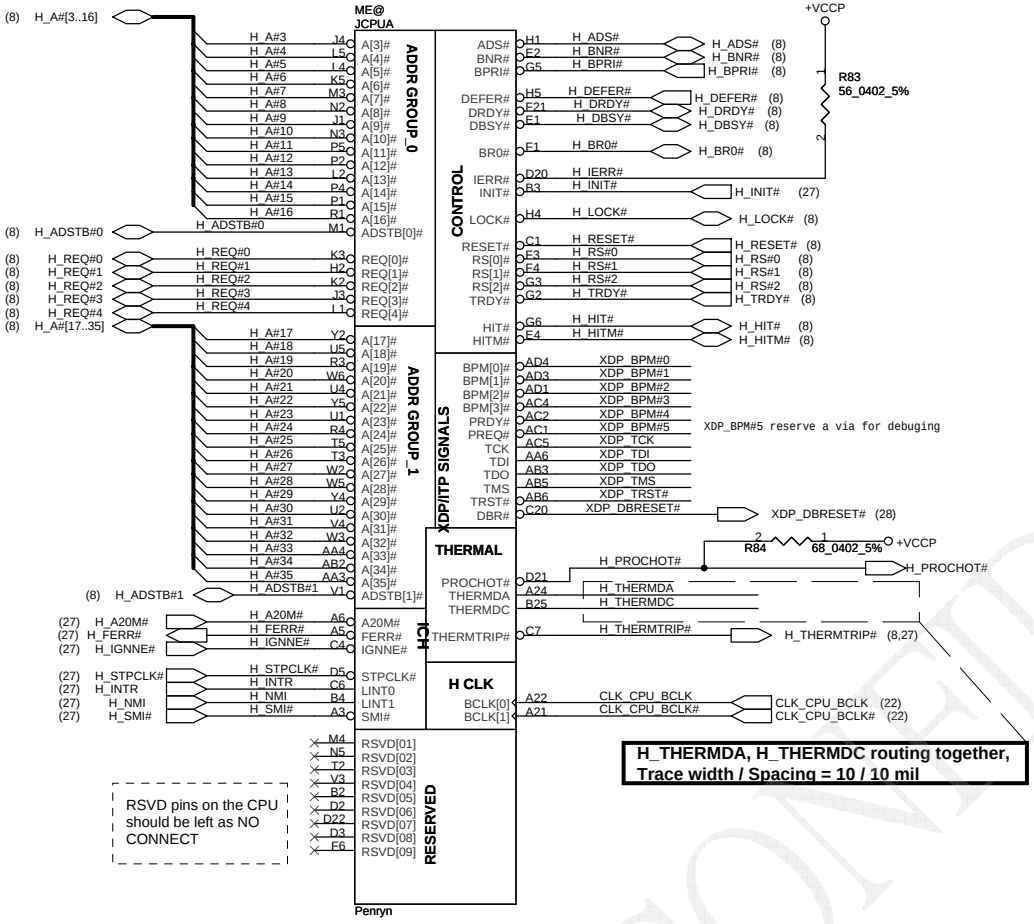
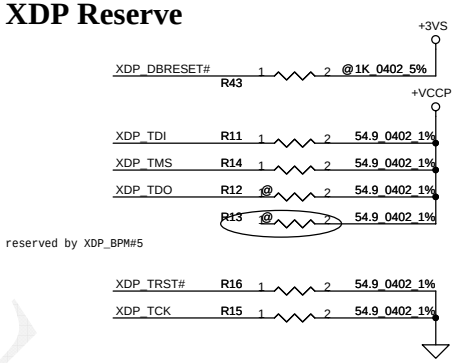
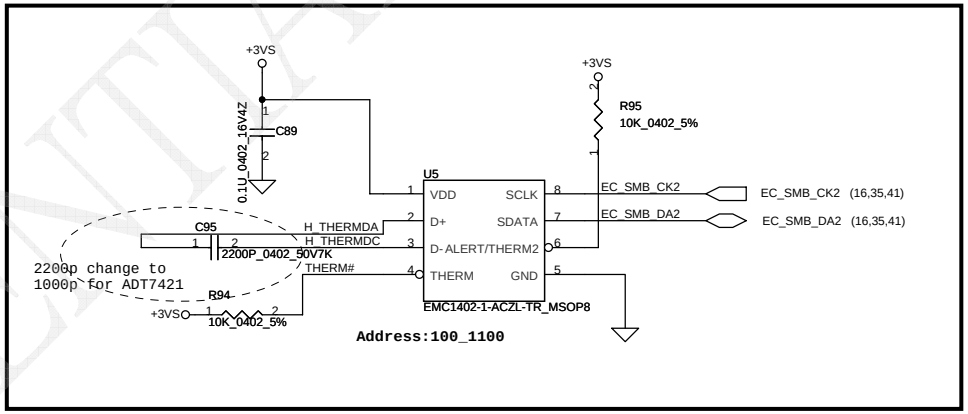
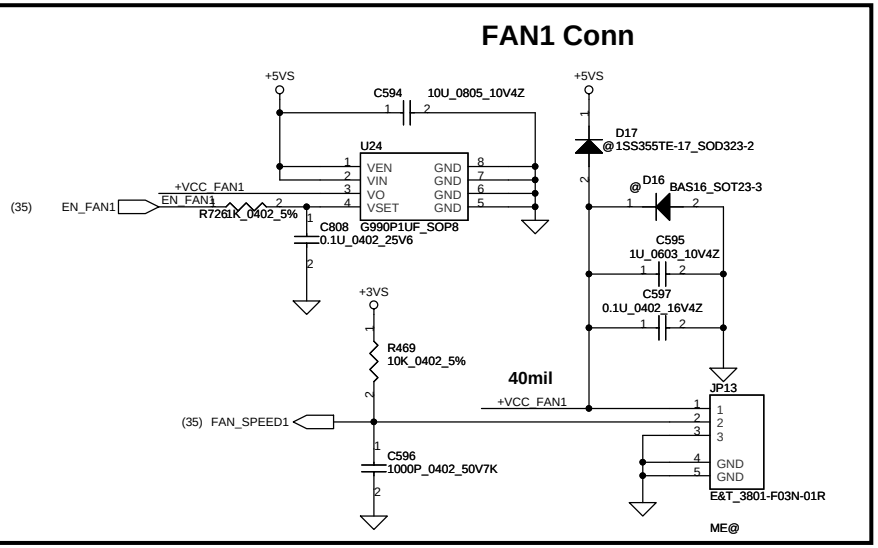


XDP Reserve





FAN1 Conn



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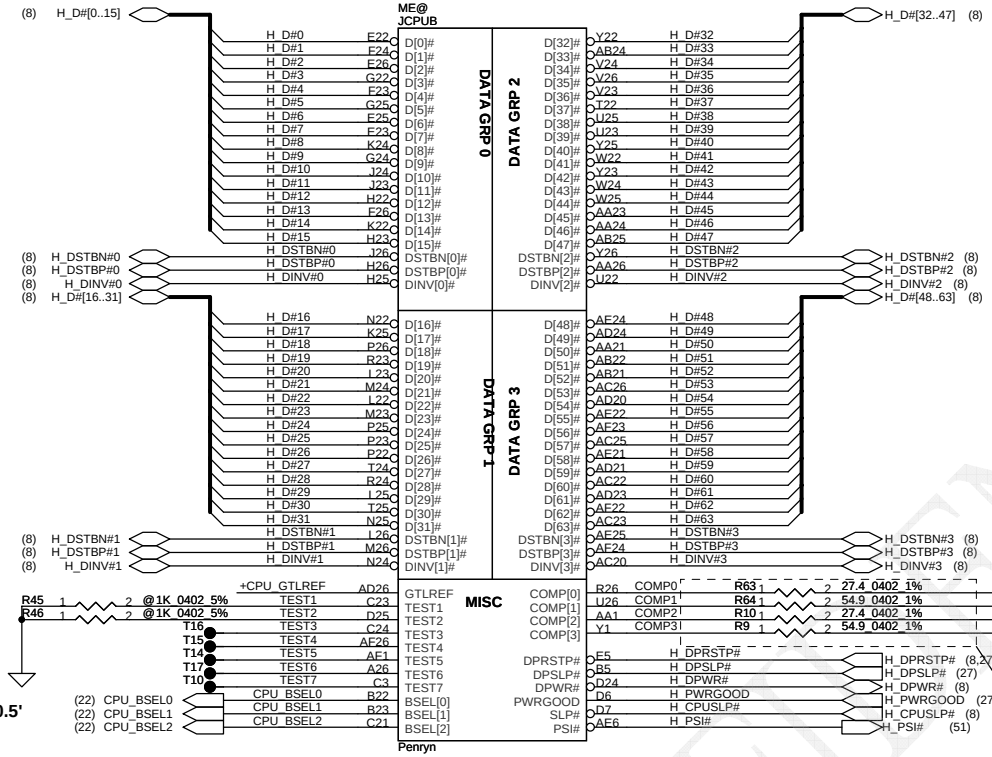
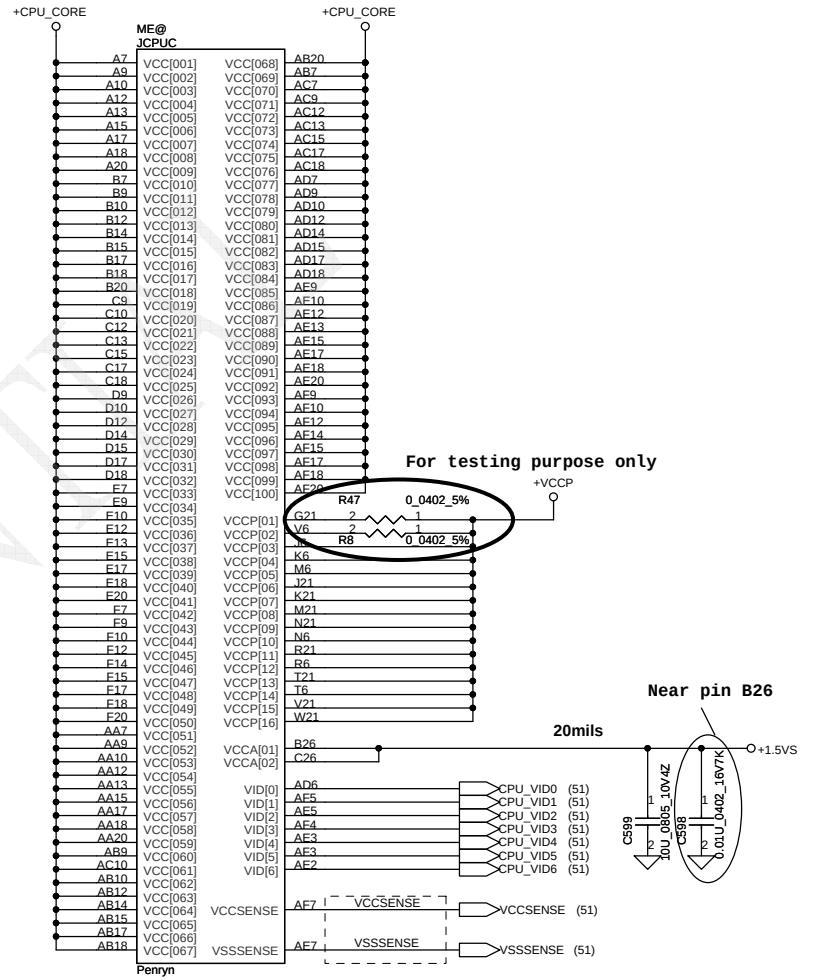
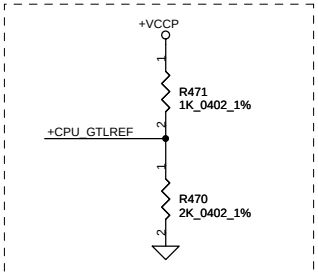




layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

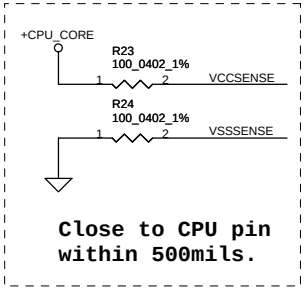


Layout note: Z0=55 ohm
0.5" max for GTLREF.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Length match within 25 mils. The trace width/space/other is 16/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



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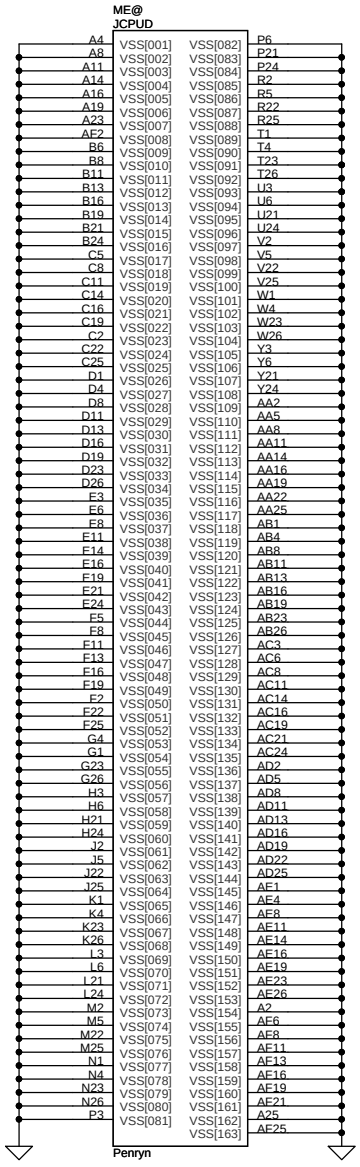
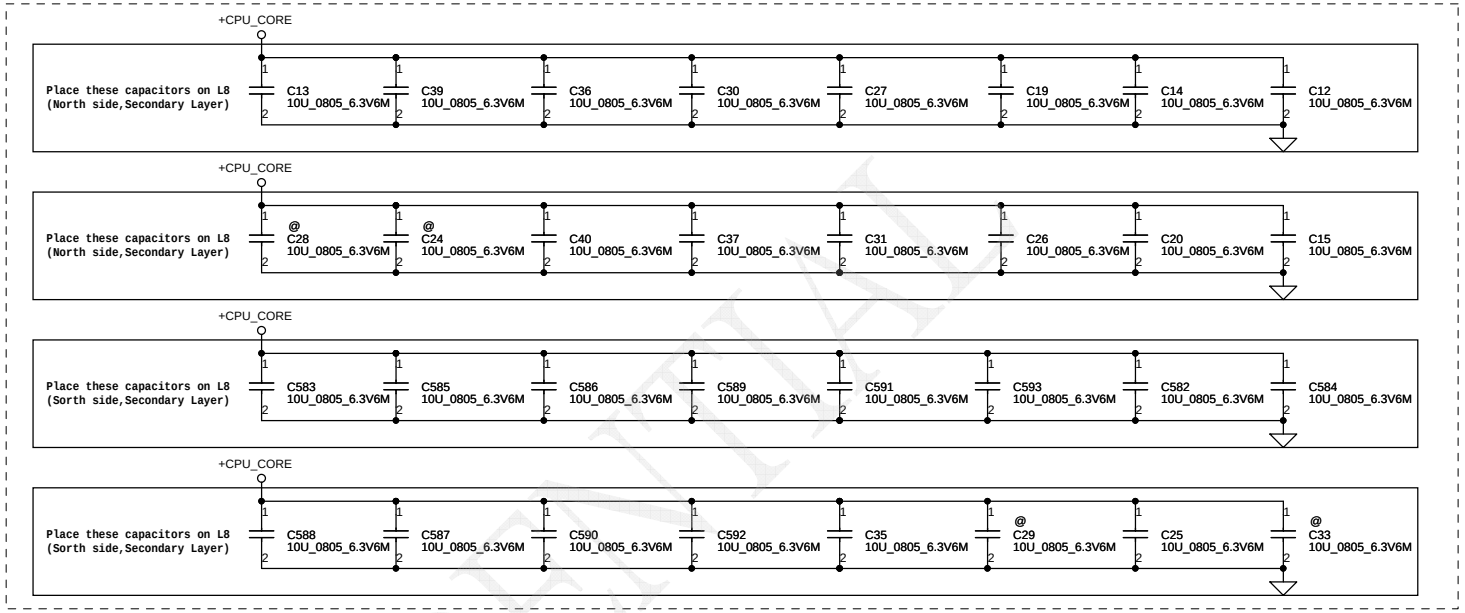
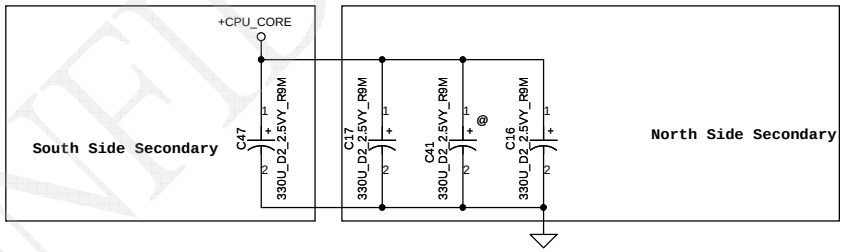
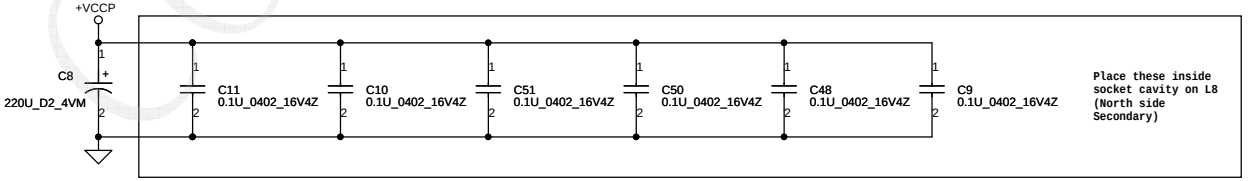




Mid Frequence Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF



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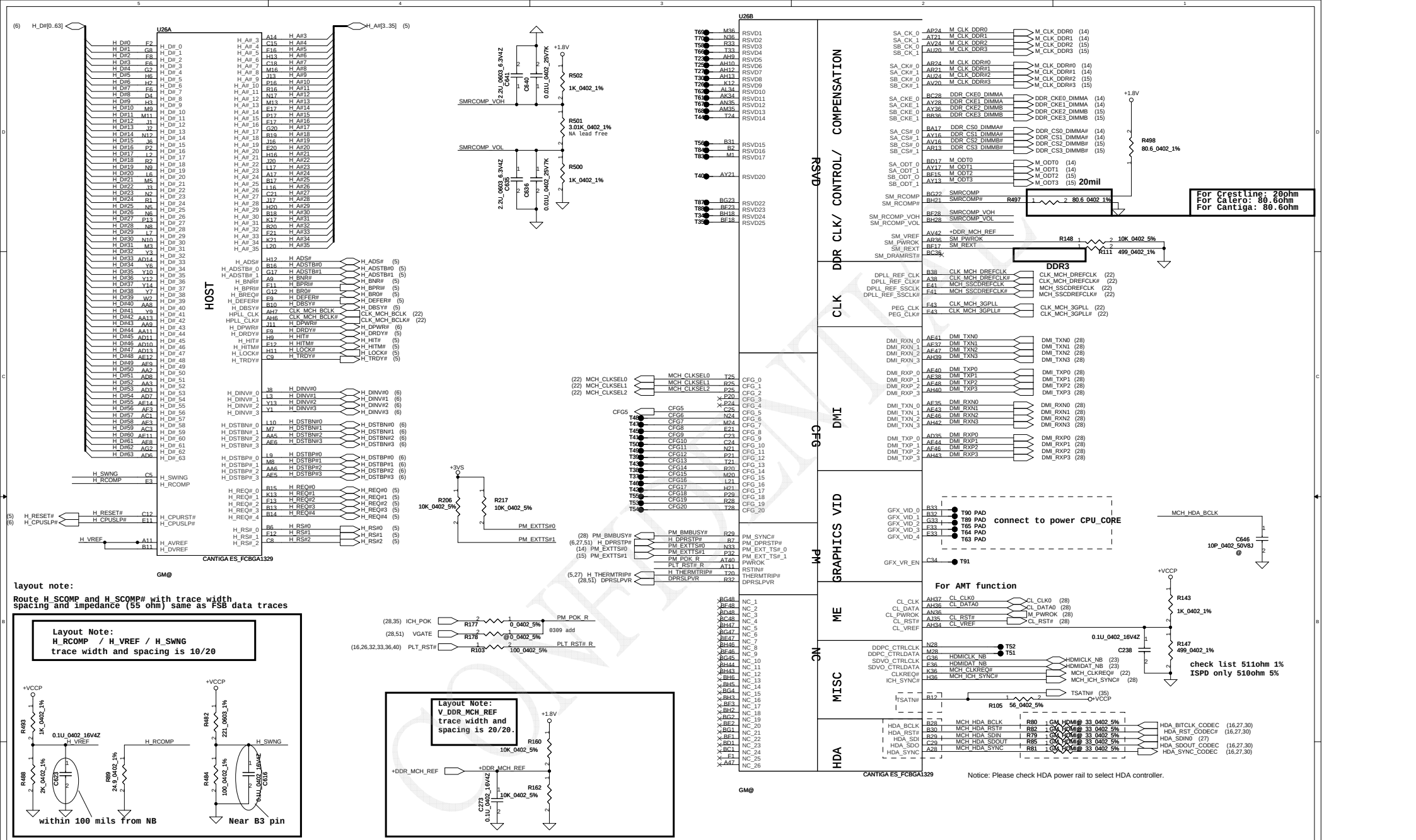

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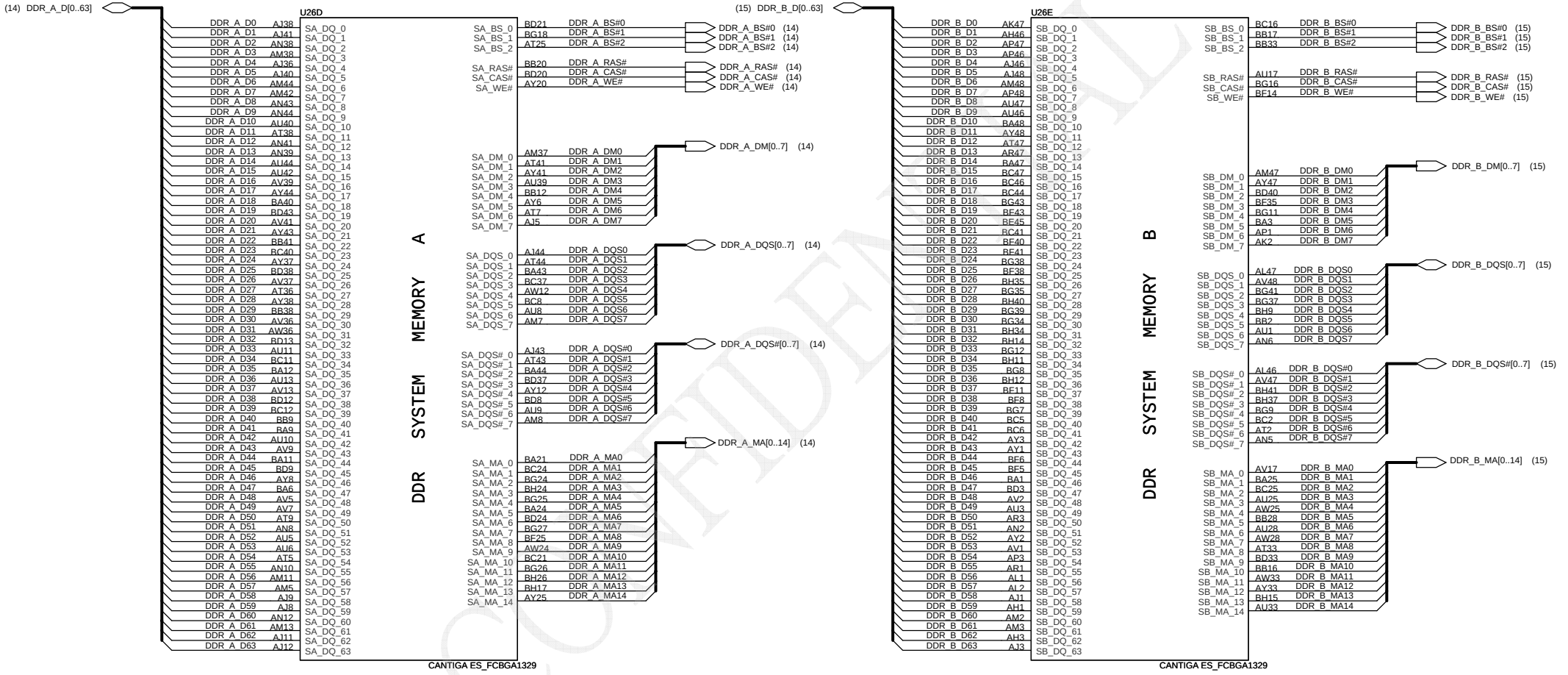

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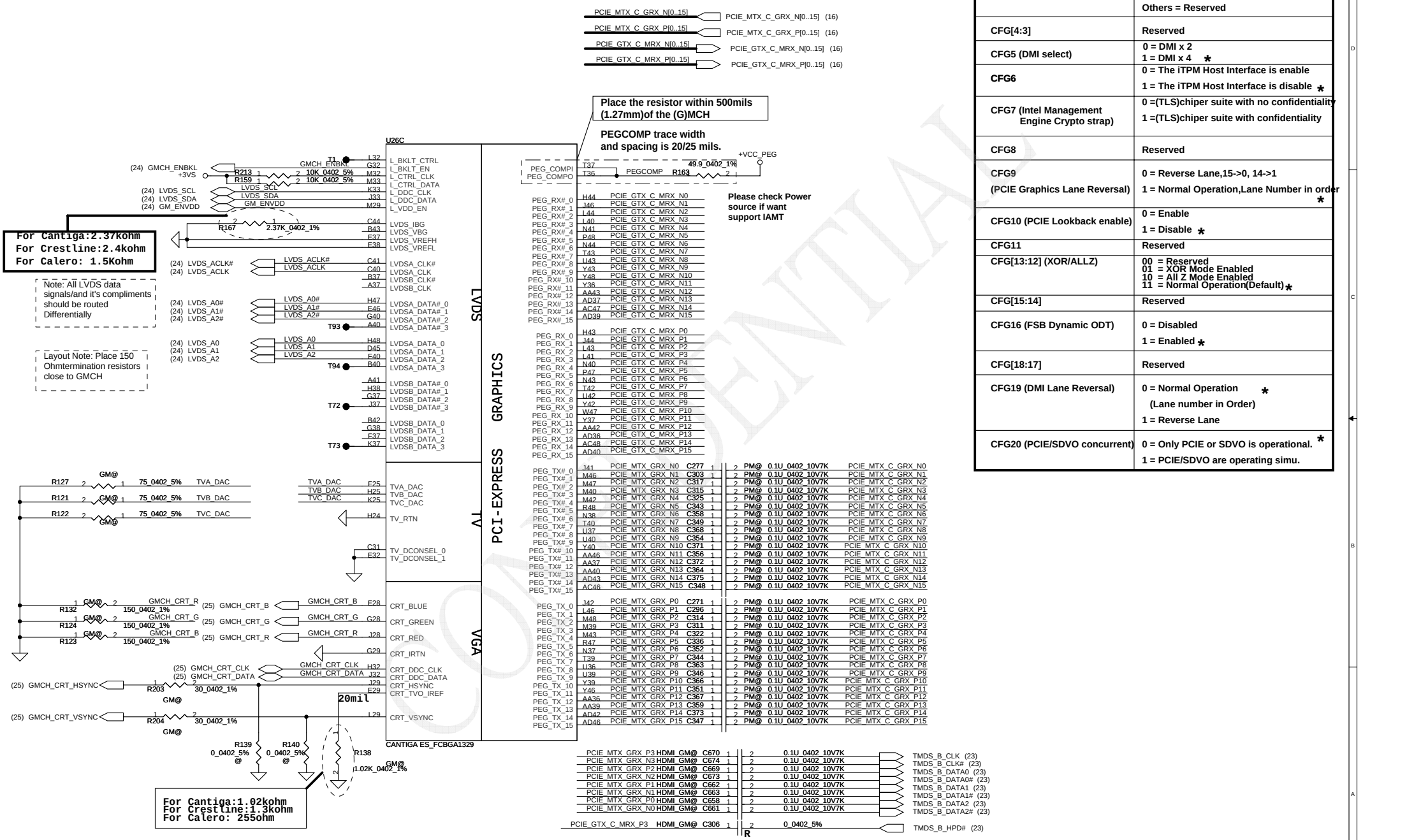
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



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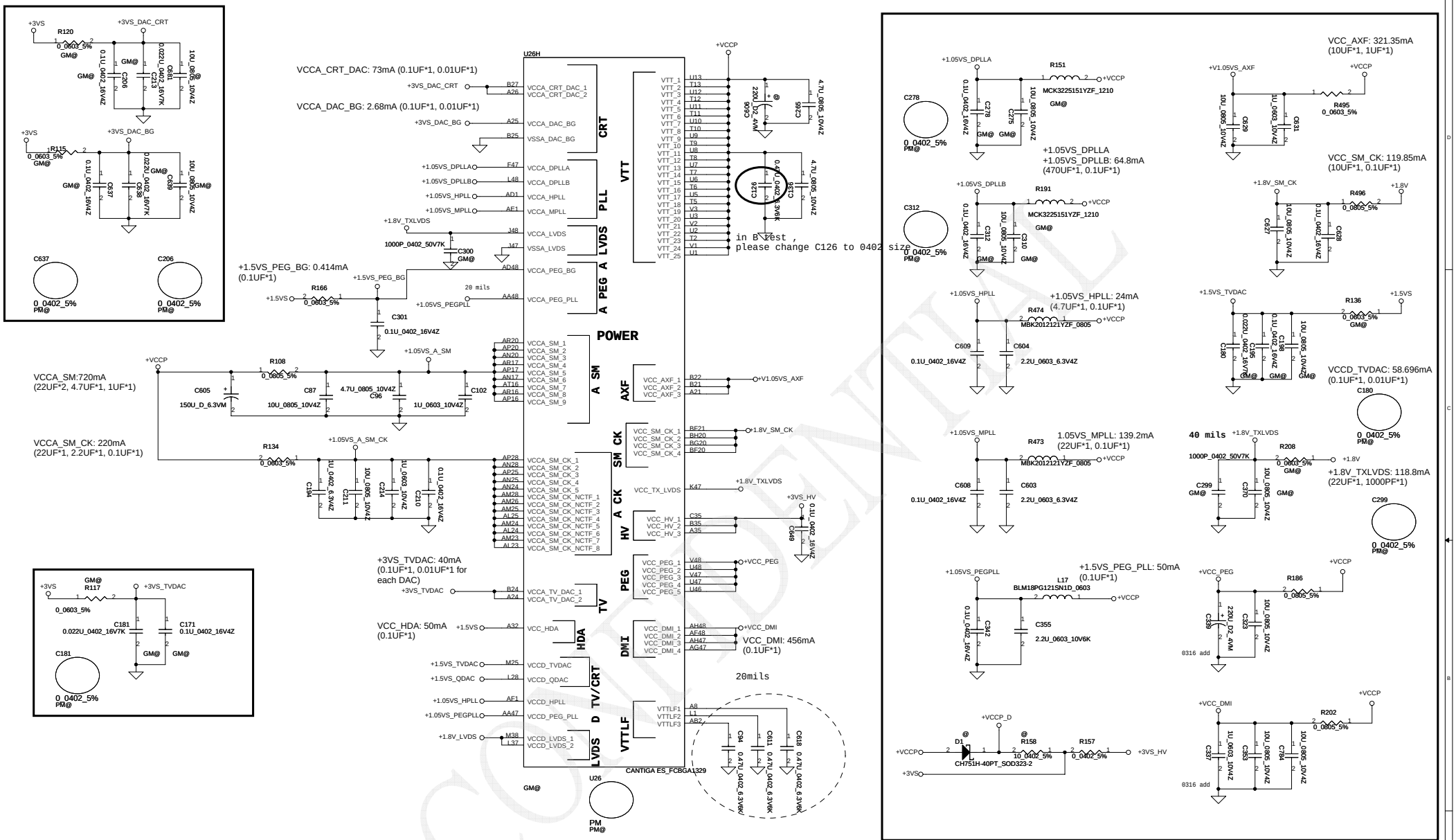

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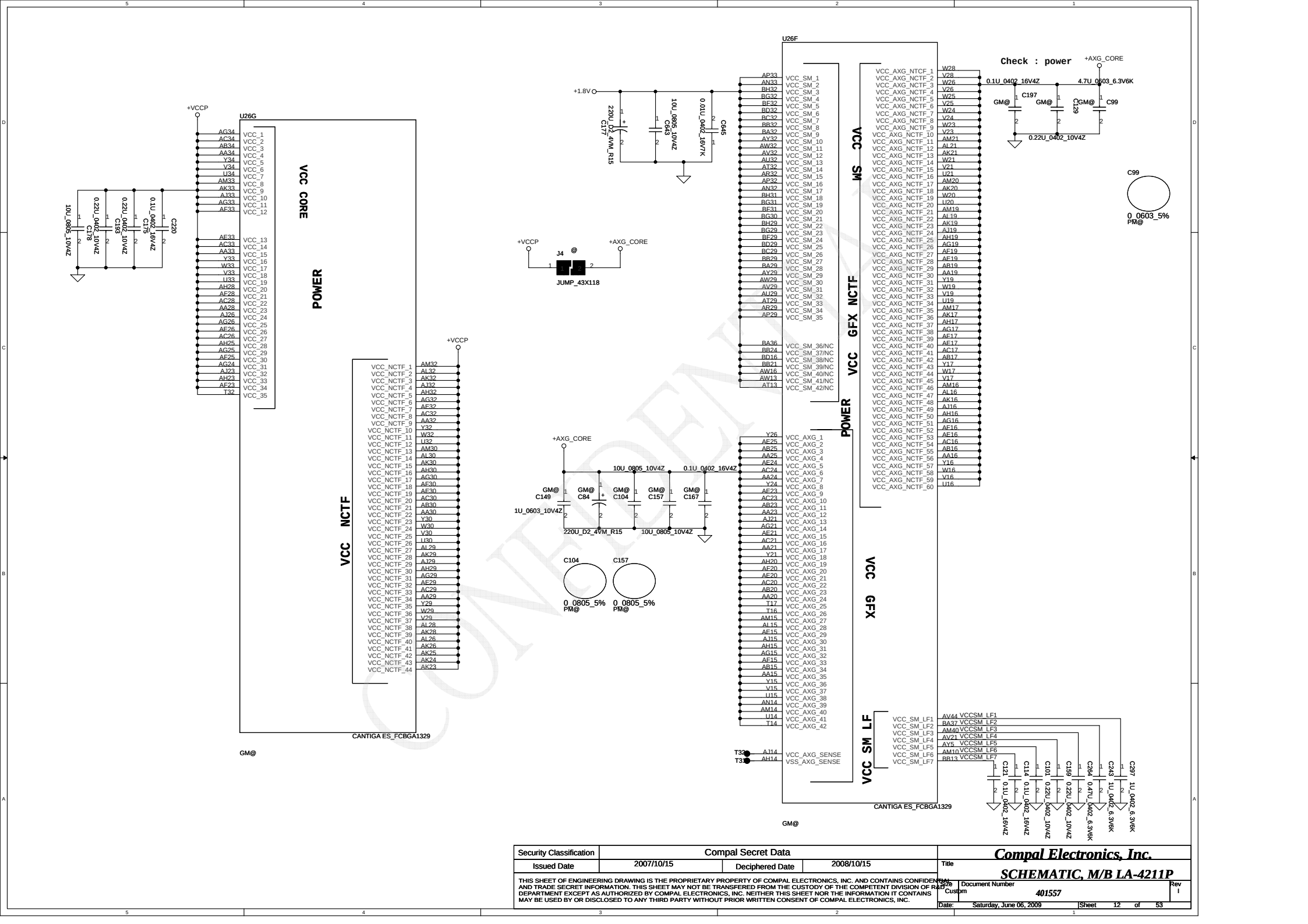

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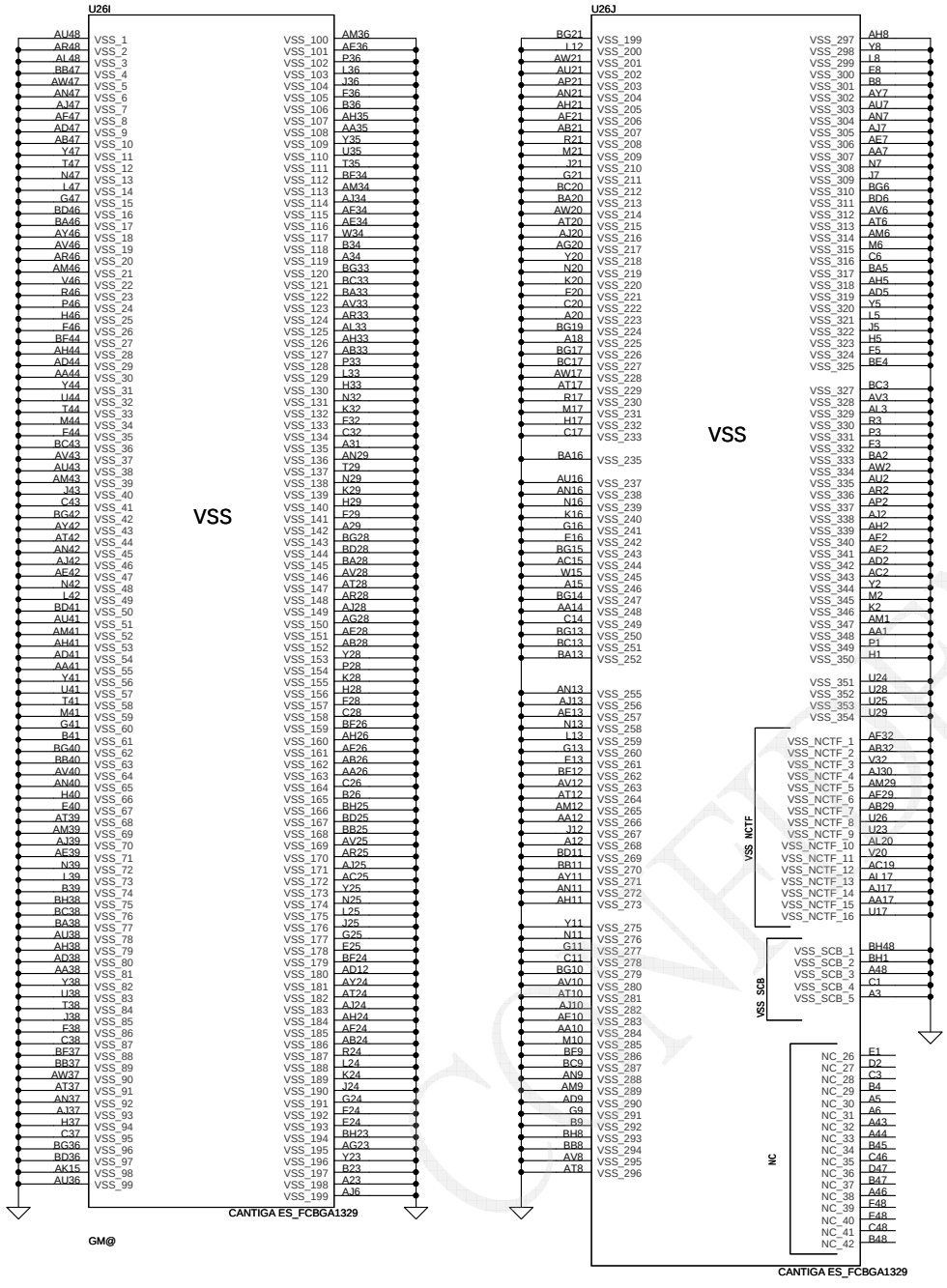

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Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20.

Layout Note:
Place near JP41

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

Layout Note:
Place these resistor closely JP41,all trace length Max=1.5"

(9) DDR_A_DQS#[0..7]
(9) DDR_A_D[0..63]
(9) DDR_A_DM[0..7]
(9) DDR_A_DQS[0..7]
(9) DDR_A_MA[0..13]

+1.8V
R225 100_0402_1%
(15) +DDR_MCH_REF1
+DDR_MCH_REF1
R232 100_0402_1%
C404 0.1U_0402_16V4Z

+1.8V
C235 2.2U_0805_16V4Z
C152 2.2U_0805_16V4Z
C644 2.2U_0805_16V4Z
C268 2.2U_0805_16V4Z
C151 2.2U_0805_16V4Z
C218 0.1U_0402_16V4Z
C219 0.1U_0402_16V4Z
C653 0.1U_0402_16V4Z
C650 0.1U_0402_16V4Z
C215 470U_D2_2.5VM_R15 @

+0.9VS
C170 0.1U_0402_16V4Z
C179 0.1U_0402_16V4Z
C209 0.1U_0402_16V4Z
C228 0.1U_0402_16V4Z
C236 0.1U_0402_16V4Z
C161 0.1U_0402_16V4Z
C230 0.1U_0402_16V4Z
C162 0.1U_0402_16V4Z
C223 0.1U_0402_16V4Z
C217 0.1U_0402_16V4Z
C163 0.1U_0402_16V4Z
C242 0.1U_0402_16V4Z
C164 0.1U_0402_16V4Z

+0.9VS
RP1: DDR_A_WE#, DDR_A_CAS#, M_ODT1, DDR_CS1_DIMMA# — M_ODT0, DDR_A_MA13, DDR_CS0_DIMMA# — 56_0804_8P4R_5%
RP2: DDR_A_RAS# — 56_0804_8P4R_5%
R128 DDR_A_BS#0 56_0402_5%
R133 DDR_A_MA10 56_0402_5%
R146 DDR_A_MA14 56_0402_5%
RP5: DDR_A_BS#1, DDR_A_MA0, DDR_A_MA2, DDR_A_MA4 — 56_0804_8P4R_5%
RP6: DDR_A_MA1, DDR_A_MA3, DDR_A_MA5, DDR_A_MA8 — 56_0804_8P4R_5%
RP9: DDR_A_MA6, DDR_A_MA7, DDR_A_MA11, DDR_CKE1_DIMMA — 56_0804_8P4R_5%
RP10: DDR_A_MA9, DDR_A_MA12, DDR_A_BS#2, DDR_CKE0_DIMMA — 56_0804_8P4R_5%

JP17 — FOX_ASOA426-M2RN-7F ME@

DDR_A_D4	DDR_A_D1	DDR_A_D6	DDR_A_D0
DDR_A_DQS#0	DDR_A_DQS0	DDR_A_DM0	
DDR_A_D2	DDR_A_D3	DDR_A_D5	DDR_A_D7
DDR_A_D8	DDR_A_D14	DDR_A_D13	DDR_A_D12
DDR_A_DQS#1	DDR_A_DQS1	DDR_A_DM1	
DDR_A_D9	DDR_A_D15	M_CLK_DDR0 (8)	M_CLK_DDR#0 (8)
DDR_A_D16	DDR_A_D17	DDR_A_D11	DDR_A_D10
DDR_A_DQS#2	DDR_A_DQS2	DDR_A_D20	DDR_A_D21
DDR_A_D18	DDR_A_D19	PM_EXTTS#0 (8)	
DDR_A_D29	DDR_A_D24	DDR_A_DM2	
DDR_A_DM3		DDR_A_D23	DDR_A_D22
DDR_A_D26	DDR_A_D27	DDR_A_D28	DDR_A_D25
DDR_CKE0_DIMMA		DDR_A_DQS#3	DDR_A_DQS3
DDR_A_BS#2		DDR_A_D31	DDR_A_D30
DDR_A_MA12	DDR_A_MA9	DDR_CKE1_DIMMA	
DDR_A_MA5	DDR_A_MA3	DDR_A_MA14	
DDR_A_MA10	DDR_A_BS#0	DDR_A_MA11	DDR_A_MA7
DDR_A_CAS#	DDR_CS1_DIMMA#	DDR_A_MA4	DDR_A_MA2
M_ODT1		DDR_A_BS#1	DDR_A_RAS#
DDR_A_D37	DDR_A_D36	M_ODT0	
DDR_A_DQS#4	DDR_A_DQS4	DDR_A_D33	DDR_A_D39
DDR_A_D38	DDR_A_D32	DDR_A_DM4	
DDR_A_D40	DDR_A_D44	DDR_A_D35	DDR_A_D34
DDR_A_DM5		DDR_A_D45	DDR_A_D43
DDR_A_D41	DDR_A_D46	DDR_A_DQS#5	DDR_A_DQS5
DDR_A_D49	DDR_A_D48	DDR_A_D47	DDR_A_D42
EC_RX_P80_CLK_R		DDR_A_D52	DDR_A_D53
DDR_A_DQS#6	DDR_A_DQS6	M_CLK_DDR1 (8)	M_CLK_DDR#1 (8)
DDR_A_D54	DDR_A_D50	DDR_A_DM6	
DDR_A_D61	DDR_A_D60	DDR_A_D51	DDR_A_D55
DDR_A_DM7		DDR_A_D57	DDR_A_D56
DDR_A_D59	DDR_A_D58	DDR_A_DQS#7	DDR_A_DQS7
CLK_SMBDATA	CLK_SMBCLK	DDR_A_D62	DDR_A_D63

(15,35,37) EC_TX_P80_DATA
(8) DDR_CKE0_DIMMA
(15,35,37) EC_RX_P80_CLK
(9) DDR_A_BS#2
(9) DDR_A_BS#0
(9) DDR_A_WE#
(9) DDR_A_CAS#
(8) DDR_CS1_DIMMA#
(8) M_ODT1
(15) EC_RX_P80_CLK_R
(15,22) CLK_SMBDATA
(15,22) CLK_SMBCLK
+3VS
C83 0.1U_0402_16V4Z

+1.8V
+DDR_MCH_REF1
C388 2.2U_0805_16V4Z
C402 0.1U_0402_16V4Z
R73 10K_0402_5%
R77 10K_0402_5%

SO-DIMM A
Top side

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(9) DDR_B_DQS#[0..7]
(9) DDR_B_D[0..63]
(9) DDR_B_DM[0..7]
(9) DDR_B_DQS[0..7]
(9) DDR_B_MA[0..13]

Layout Note:
Place near JP42

+1.8V

2.2U_0805_16V4Z C232
2.2U_0805_16V4Z C150
2.2U_0805_16V4Z C387
2.2U_0805_16V4Z C156
2.2U_0805_16V4Z C241
0.1U_0402_16V4Z C192
0.1U_0402_16V4Z C188
0.1U_0402_16V4Z C199
0.1U_0402_16V4Z C191
C155 470U_D2_2.5VM_R15 @

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS

0.1U_0402_16V4Z C244
0.1U_0402_16V4Z C240
0.1U_0402_16V4Z C227
0.1U_0402_16V4Z C216
0.1U_0402_16V4Z C196
0.1U_0402_16V4Z C187
0.1U_0402_16V4Z C247
0.1U_0402_16V4Z C246
0.1U_0402_16V4Z C229
0.1U_0402_16V4Z C222
0.1U_0402_16V4Z C204
0.1U_0402_16V4Z C195
0.1U_0402_16V4Z C176

Layout Note:
Place these resistor closely JP42,all trace length Max=1.5"

+0.9VS

RP3: DDR_B_CAS# — DDR_B_WE# — DDR_CS3_DIMMB# — M_ODT3 — DDR_B_MA13 — M_ODT2 — DDR_CS2_DIMMB# — DDR_B_RAS# — 56_0804_8P4R_5%
RP4: 56_0804_8P4R_5%
R135 DDR_B_BS#0 — 56_0402_5%
R131 DDR_B_MA10 — 56_0402_5%
R152 DDR_B_MA14 — 56_0402_5%
RP7: DDR_B_BS#1 — DDR_B_MA0 — DDR_B_MA2 — DDR_B_MA4 — 56_0804_8P4R_5%
RP8: DDR_B_MA1 — DDR_B_MA3 — DDR_B_MA5 — DDR_B_MA9 — 56_0804_8P4R_5%
RP11: DDR_B_MA7 — DDR_B_MA6 — DDR_B_MA11 — DDR_CKE3_DIMMB — 56_0804_8P4R_5%
RP12: DDR_CKE2_DIMMB — DDR_B_BS#2 — DDR_B_MA12 — DDR_B_MA8 — 56_0804_8P4R_5%

+1.8V +1.8V +DDR_MCH_REF1 → +DDR_MCH_REF1 (14)

C403 2.2U_0805_16V4Z
C407 0.1U_0402_16V4Z

JP16

1	VREF	2	VSS		
3	VSS	4	DQ4	DDR_B_D0	DDR_B_D4
5	DQ0	6	DQ5	DDR_B_D1	DDR_B_D5
7	DQ1	8	VSS		
9	VSS	10	DM0		DDR_B_DM0
11	DQS0#	12	VSS	DDR_B_DQS#0	
13	DQS0	14	DQ6	DDR_B_DQS0	DDR_B_D6
15	VSS	16	DQ7		DDR_B_D7
17	DQ2	18	VSS	DDR_B_D2	
19	DQ3	20	DQ12	DDR_B_D3	DDR_B_D12
21	VSS	22	DQ13		DDR_B_D13
23	DQ8	24	VSS	DDR_B_D8	
25	DQ9	26	DM1	DDR_B_D9	DDR_B_DM1
27	VSS	28	VSS		
29	DQS1#	30	CK0	DDR_B_DQS#1	M_CLK_DDR2 (8)
31	DQS1	32	CK0#	DDR_B_DQS1	M_CLK_DDR#2 (8)
33	VSS	34	VSS		
35	DQ10	36	DQ14	DDR_B_D10	DDR_B_D14
37	DQ11	38	DQ15	DDR_B_D11	DDR_B_D15
39	VSS	40	VSS		
41	VSS	42	VSS		
43	DQ16	44	DQ20	DDR_B_D17	DDR_B_D21
45	DQ17	46	DQ21	DDR_B_D20	DDR_B_D16
47	VSS	48	VSS		
49	DQS2#	50	NC	DDR_B_DQS#2	PM_EXTTS#1 (8)
51	DQS2	52	DM2	DDR_B_DQS2	DDR_B_DM2
53	VSS	54	VSS		
55	DQ18	56	DQ22	DDR_B_D18	DDR_B_D22
57	DQ19	58	DQ23	DDR_B_D19	DDR_B_D23
59	VSS	60	VSS		
61	DQ24	62	DQ28	DDR_B_D25	DDR_B_D26
63	DQ25	64	DQ29	DDR_B_D28	DDR_B_D24
65	VSS	66	VSS		
67	DM3	68	DQS3#	DDR_B_DM3	DDR_B_DQS#3
69	NC	70	DQS3		DDR_B_DQS3
71	VSS	72	VSS		
73	DQ26	74	DQ30	DDR_B_D30	DDR_B_D29
75	DQ27	76	DQ31	DDR_B_D31	DDR_B_D27
77	VSS	78	VSS		
79	CKE0	80	NC/CKE1	DDR_CKE2_DIMMB	DDR_CKE3_DIMMB → DDR_CKE3_DIMMB (8)
81	VDD	82	VDD		
83	NC	84	NC/A15		
85	BA2	86	NC/A14	DDR_B_BS#2	DDR_B_MA14 → DDR_B_MA14 (9)
87	VDD	88	VDD		
89	A12	90	A11	DDR_B_MA12	DDR_B_MA11
91	A9	92	A7	DDR_B_MA9	DDR_B_MA7
93	A8	94	A6	DDR_B_MA8	DDR_B_MA6
95	VDD	96	VDD		
97	A5	98	A4	DDR_B_MA5	DDR_B_MA4
99	A3	100	A2	DDR_B_MA3	DDR_B_MA2
101	A1	102	A0	DDR_B_MA1	DDR_B_MA0
103	VDD	104	VDD		
105	A10/AP	106	BA1	DDR_B_MA10	DDR_B_BS#1 → DDR_B_BS#1 (9)
107	BA0	108	RAS#	(9) DDR_B_BS#0	DDR_B_RAS# → DDR_B_RAS# (9)
109	WE#	110	S0#	(9) DDR_B_WE#	DDR_CS2_DIMMB# → DDR_CS2_DIMMB# (8)
111	VDD	112	VDD		
113	CAS#	114	ODT0	(9) DDR_B_CAS#	M_ODT2 → M_ODT2 (8)
115	NC/S1#	116	NC/A13	(8) DDR_CS3_DIMMB#	DDR_B_MA13
117	VDD	118	VDD		
119	NC/ODT1	120	NC	(8) M_ODT3	
121	VSS	122	VSS		
123	DQ32	124	DQ36	DDR_B_D32	DDR_B_D36
125	DQ33	126	DQ37	DDR_B_D33	DDR_B_D37
127	VSS	128	VSS		
129	DQS4#	130	DM4	DDR_B_DQS#4	DDR_B_DM4
131	DQS4	132	VSS	DDR_B_DQS4	
133	VSS	134	DQ38		DDR_B_D39
135	DQ34	136	DQ39	DDR_B_D34	DDR_B_D38
137	DQ35	138	VSS	DDR_B_D35	
139	VSS	140	DQ44		DDR_B_D44
141	DQ40	142	DQ45	DDR_B_D40	DDR_B_D45
143	DQ41	144	VSS	DDR_B_D41	
145	VSS	146	DQS5#		DDR_B_DQS#5
147	DM5	148	DQS5	DDR_B_DM5	DDR_B_DQS5
149	VSS	150	VSS		
151	DQ42	152	DQ46	DDR_B_D42	DDR_B_D46
153	DQ43	154	DQ47	DDR_B_D43	DDR_B_D47
155	VSS	156	VSS		
157	DQ48	158	DQ52	DDR_B_D48	DDR_B_D52
159	DQ49	160	DQ53	DDR_B_D49	DDR_B_D53
161	VSS	162	VSS		
163	NC,TEST	164	CK1	EC_RX_P80_CLK_R	M_CLK_DDR3 (8)
165	VSS	166	CK1#		M_CLK_DDR#3 (8)
167	DQS6#	168	VSS	DDR_B_DQS#6	
169	DQS6	170	DM6	DDR_B_DQS6	DDR_B_DM6
171	VSS	172	VSS		
173	DQ50	174	DQ54	DDR_B_D51	DDR_B_D54
175	DQ51	176	DQ55	DDR_B_D50	DDR_B_D55
177	VSS	178	VSS		
179	DQ56	180	DQ60	DDR_B_D56	DDR_B_D60
181	DQ57	182	DQ61	DDR_B_D61	DDR_B_D57
183	VSS	184	VSS		
185	DM7	186	DQS7#	DDR_B_DM7	DDR_B_DQS#7
187	VSS	188	DQS7		DDR_B_DQS7
189	DQ58	190	VSS	DDR_B_D58	
191	DQ59	192	DQ62	DDR_B_D59	DDR_B_D62
193	VSS	194	DQ63		DDR_B_D63
195	SDA	196	VSS	(14,22) CLK_SMBDATA	
197	SCL	198	SAO	(14,22) CLK_SMBCLK	
199	VDDSPD	200	SA1	+3VS	R74 10K_0402_5% → +3VS

T80 — (14,35,37) EC_TX_P80_DATA
(8) DDR_CKE2_DIMMB
(14,35,37) EC_RX_P80_CLK
(9) DDR_B_BS#2
T22 — (14) EC_RX_P80_CLK_R
R78 10K_0402_5%
C82 0.1U_0402_16V4Z
FOX_AS0A426-NARN-7F--NME@

SO-DIMM B

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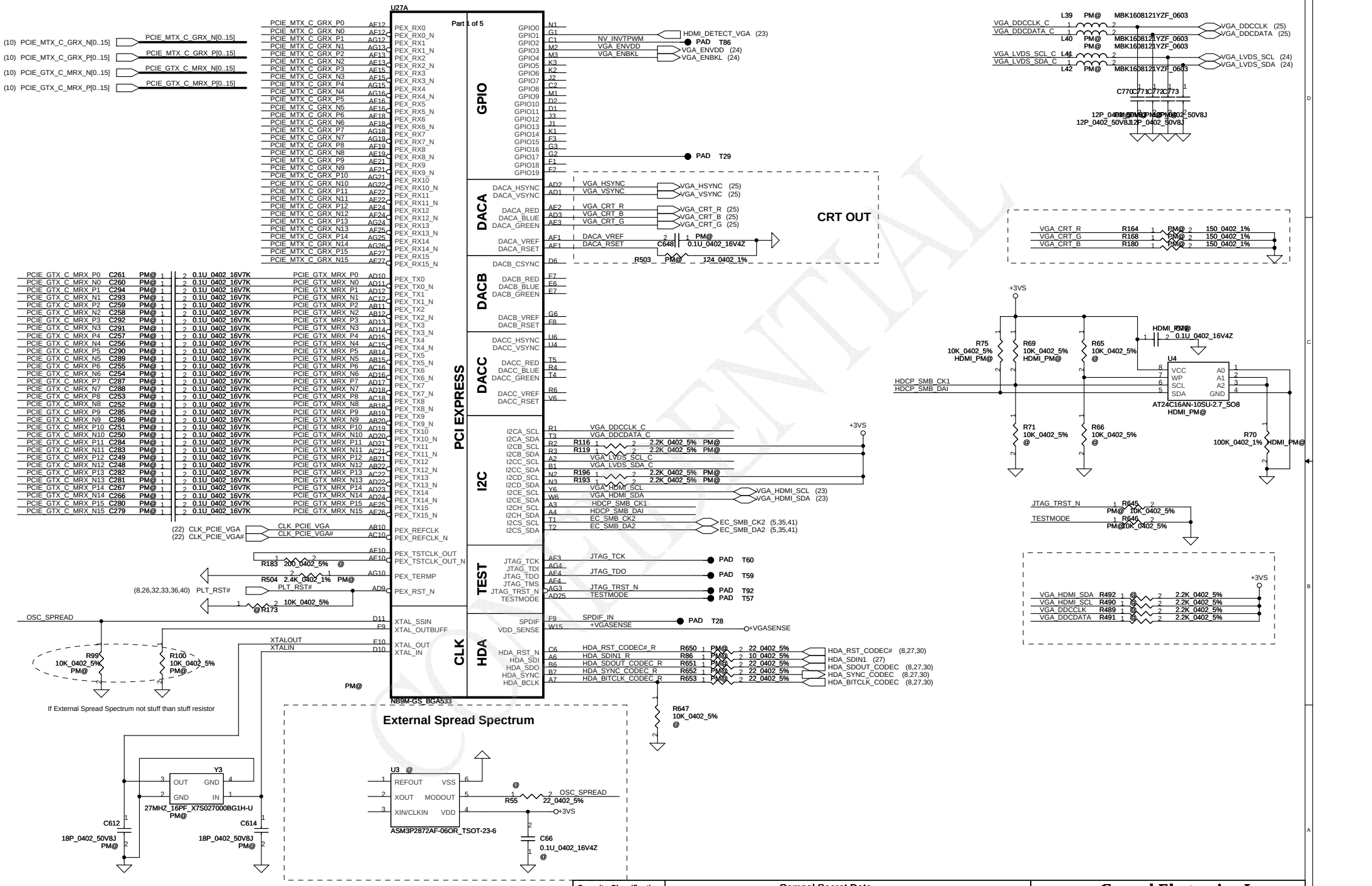

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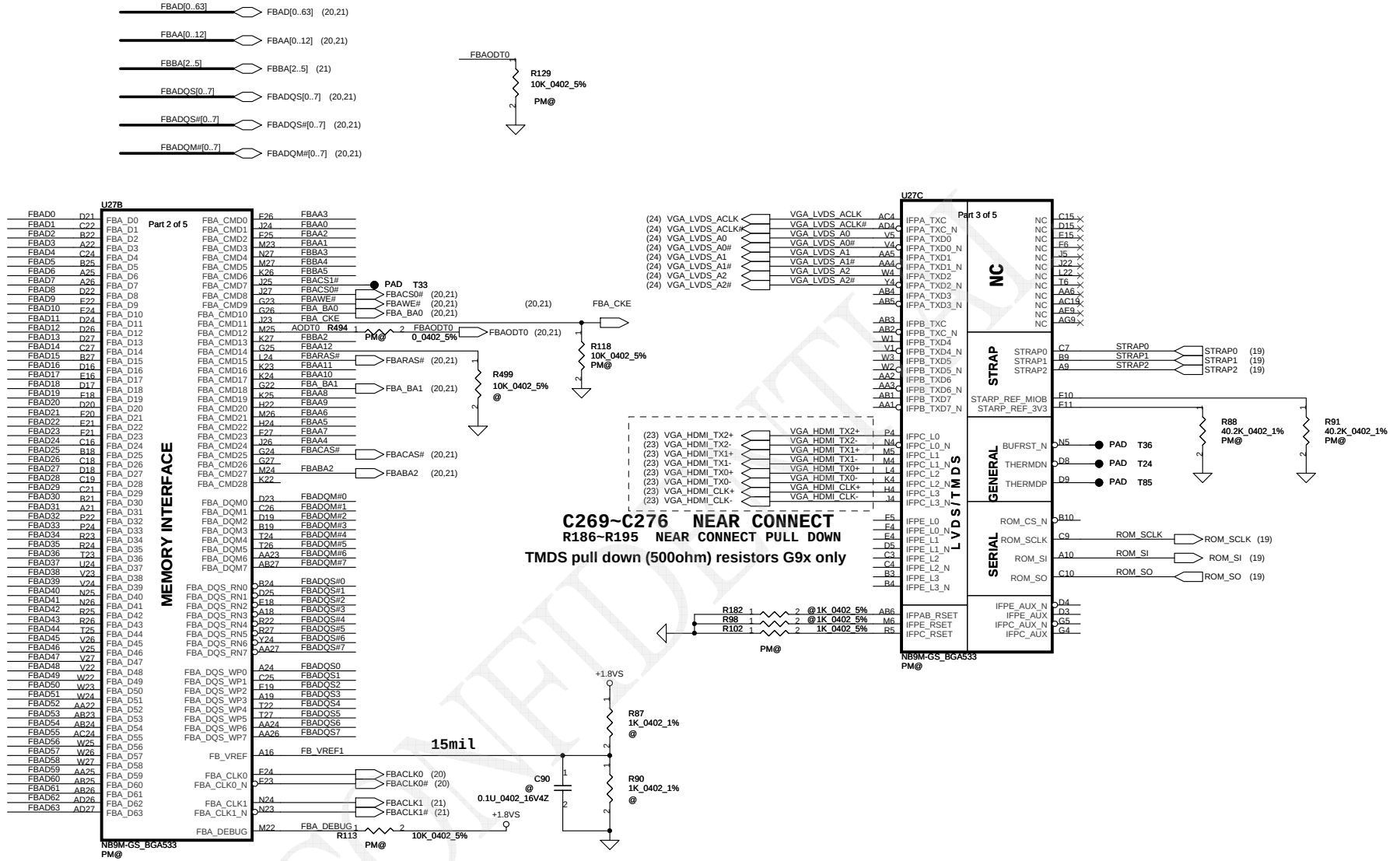

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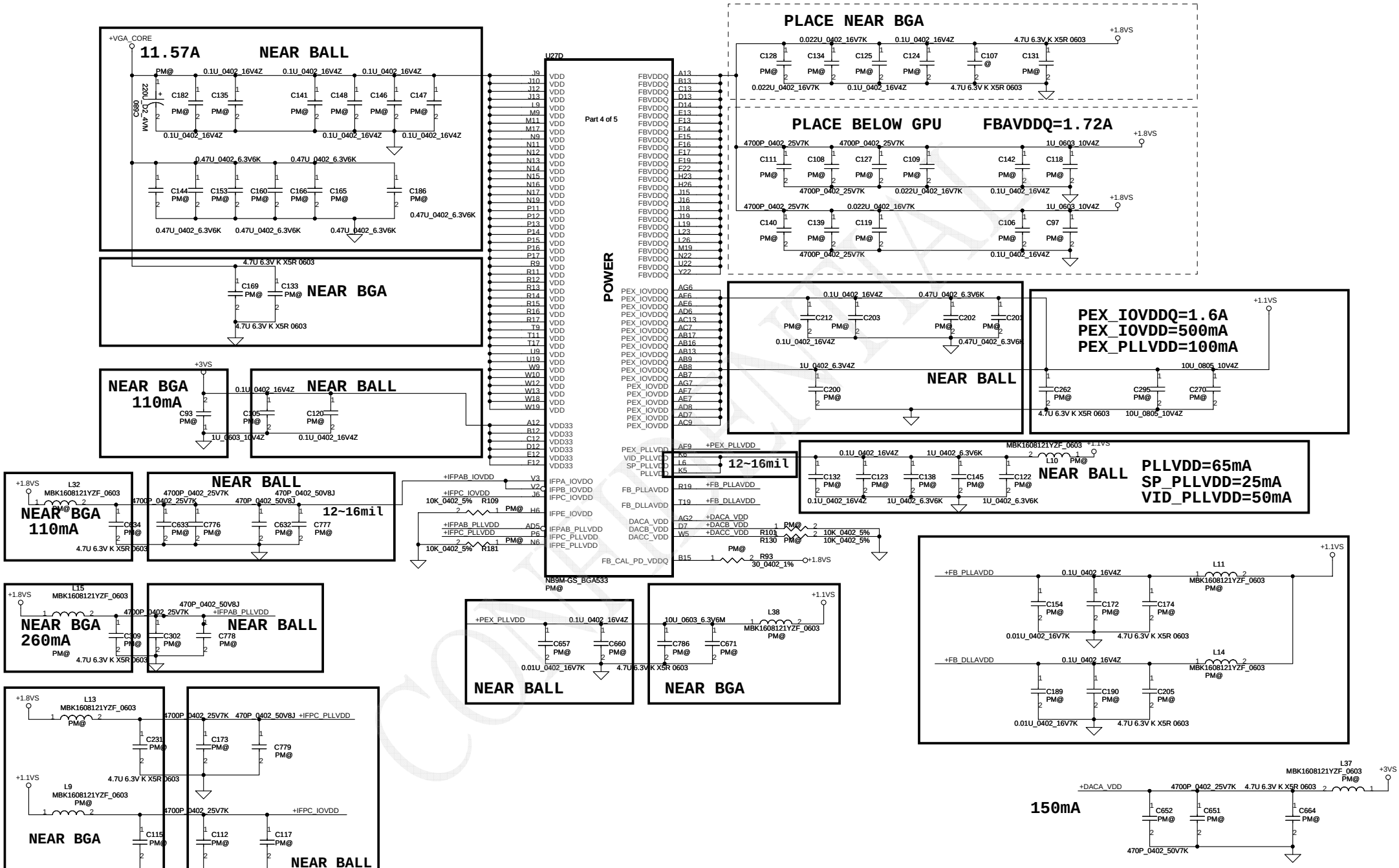

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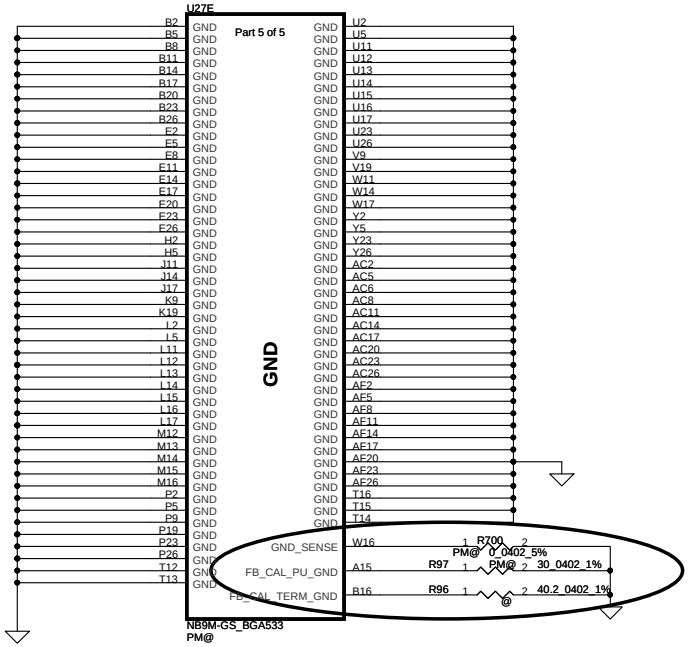
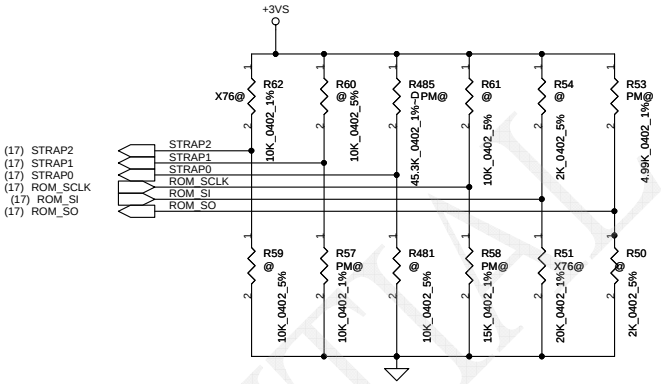
A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available





GB1 Family GPU Strap Qptions

GPU	FB Memory		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K	PU 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K	PU 45K
NB9M-GE (0x06E8)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PU 5K	PD 10K	PU 45K
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 5K	PD 10K	PU 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PU 5K	PD 10K	PU 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 5K	PD 10K	PU 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PU 5K	PD 10K	PU 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 5K	PD 10K	PU 45K

Component	Manufacturer	Compal PN	Compal X76 PN
DDR2 VRAM (16M*16)	Hynix	SA000012G30	X7611338L01
	Qimonda	SA00001YF10	X7611338L02
	Samsung	SA00001KH10	X7611338L03
DDR2 VRAM (32M*16)	Hynix	SA00000FF30	X7611338L04
	Qimonda	SA00000S820	X7611338L05
	Samsung	SA00001VX10	X7611338L06

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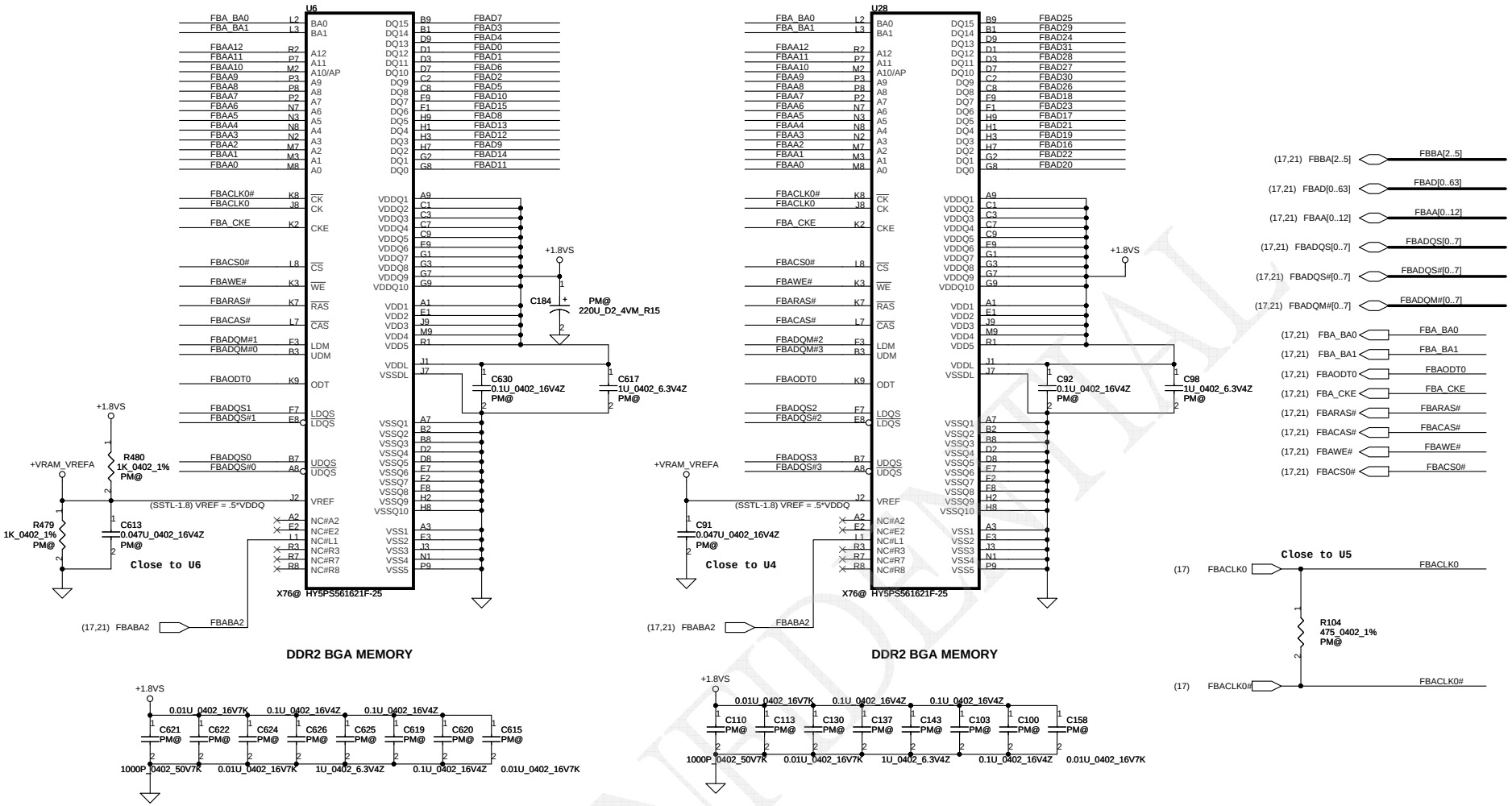

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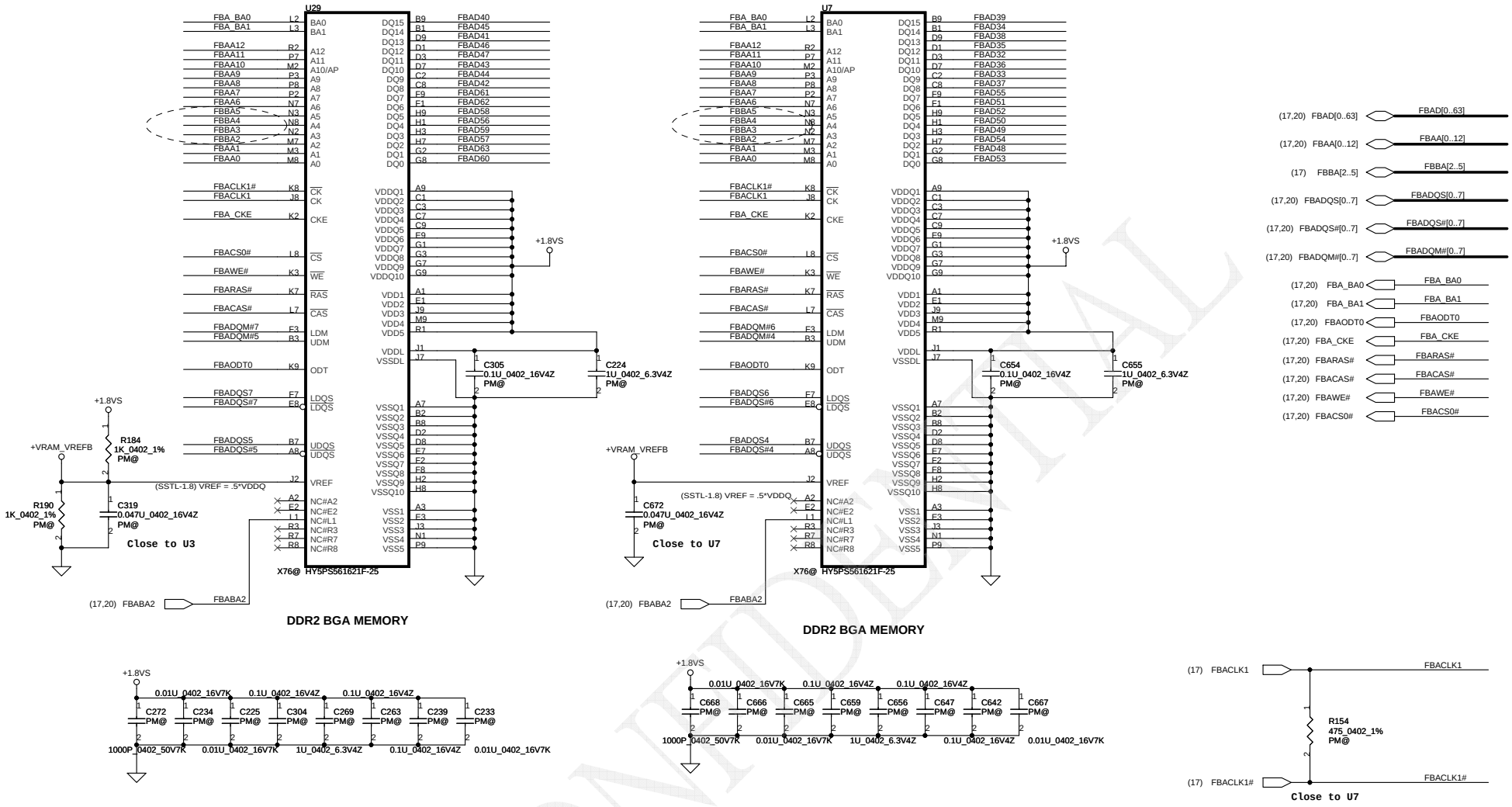

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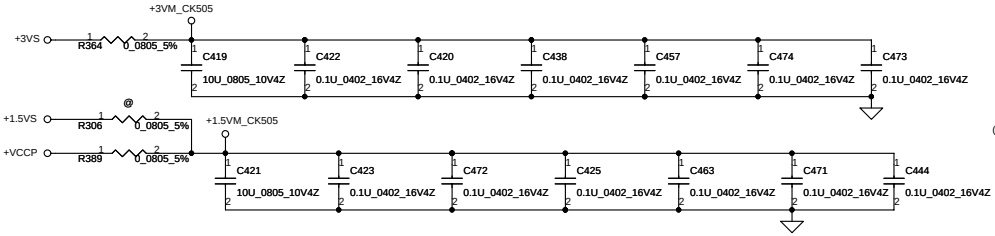
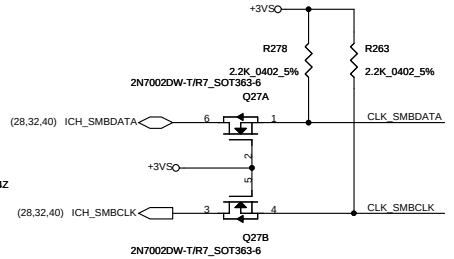
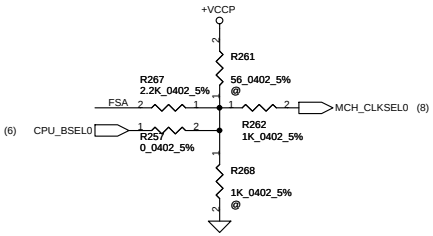
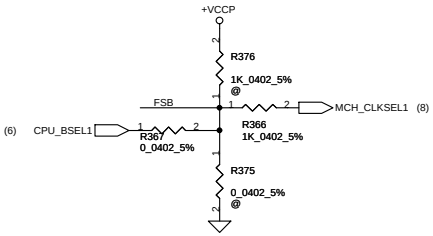
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

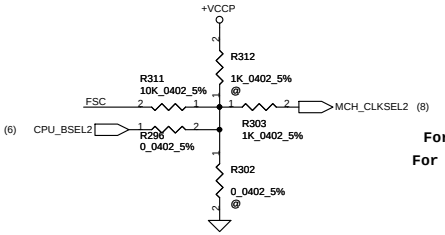


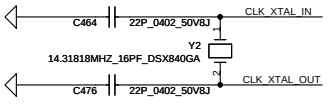


SA000020K00 (Silego : SLG8SP556VTR)
SA000020H00 (ICS : ICS9LPRS387AKLFT)

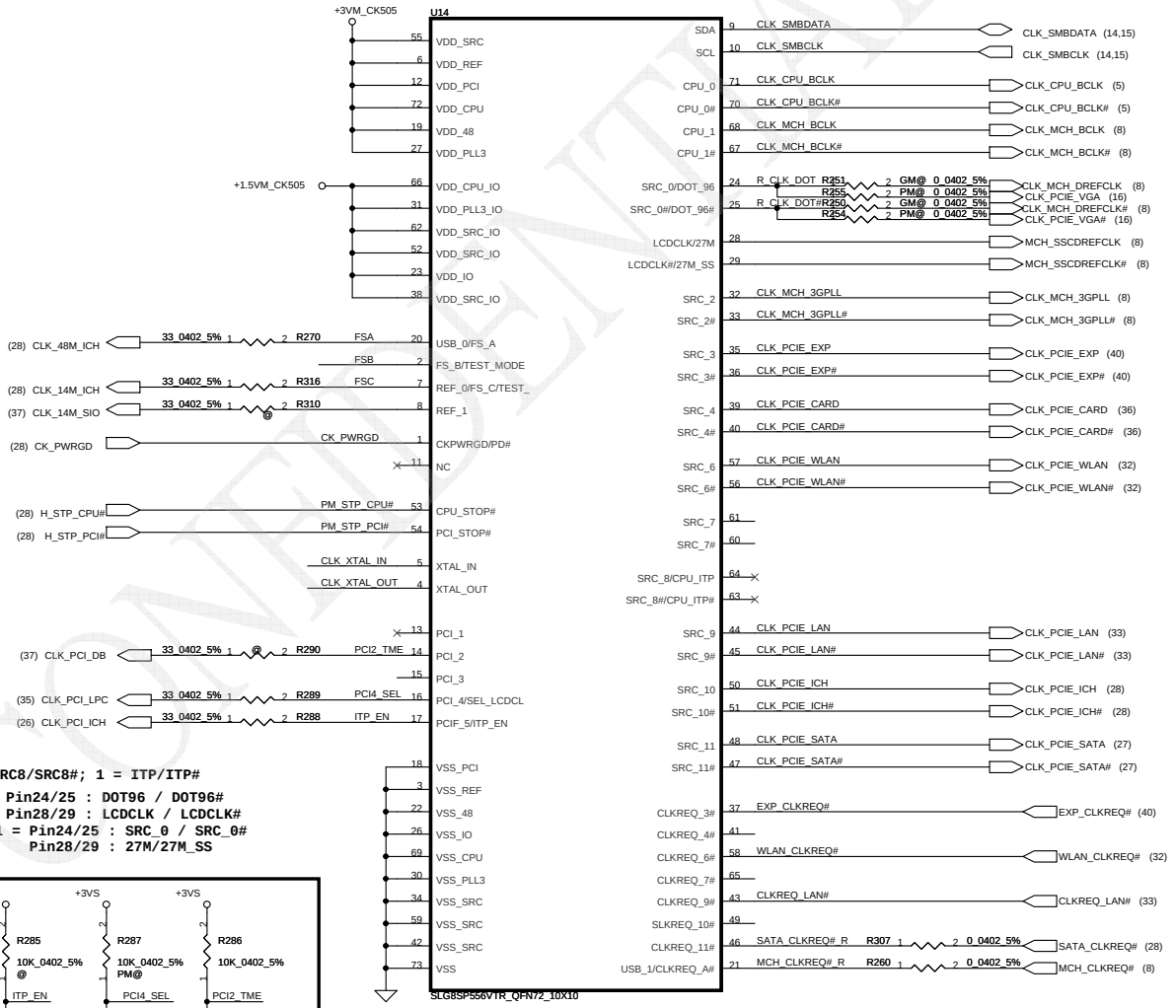




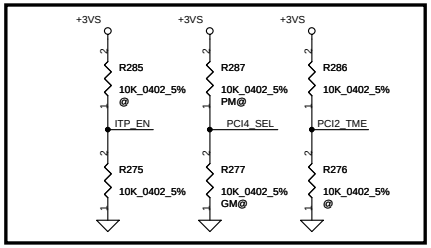




Routing the trace at least 10mil

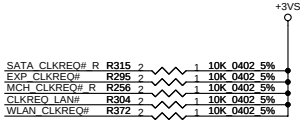


For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

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09/13 change pull low enable

09/13 change pull high enable

pull down for PS8101T

P/N:SA00001U900

9/14 Change from 4.7K to 2.2K base on Design Guide P.274

TMDS pull down (500ohm) resistors G9x only

NEAR CONNECT

9/14 Modify for UMA used

9/14 Reserve for VGA used;check pin name

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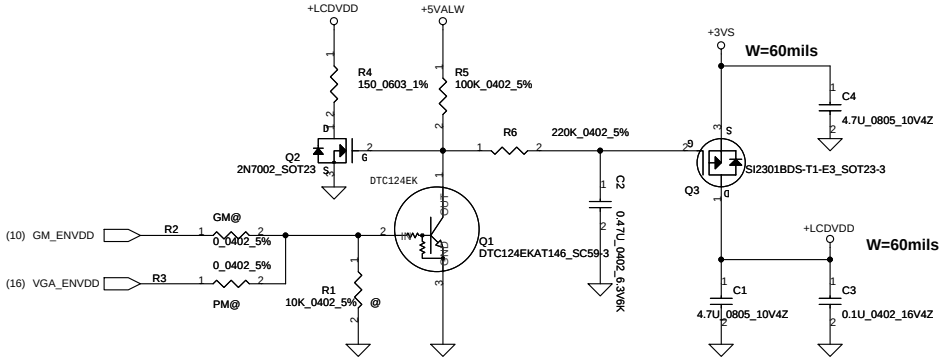
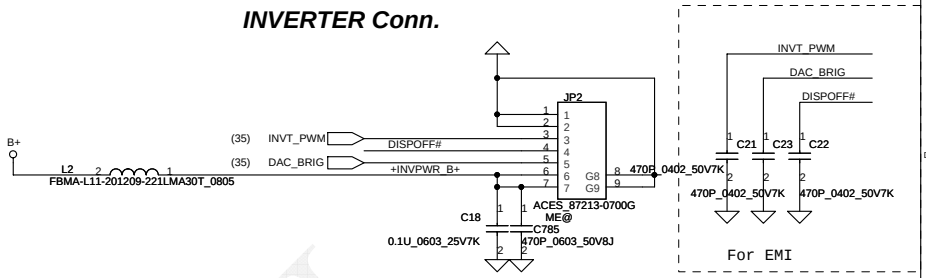
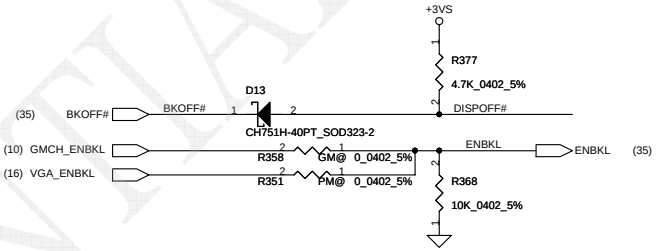
LCD POWER CIRCUIT

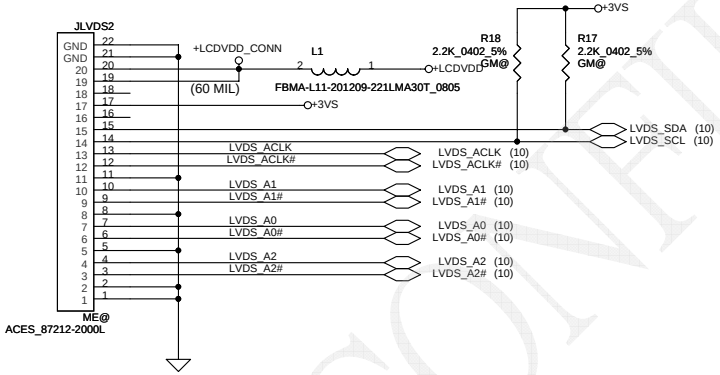


INVERTER Conn.

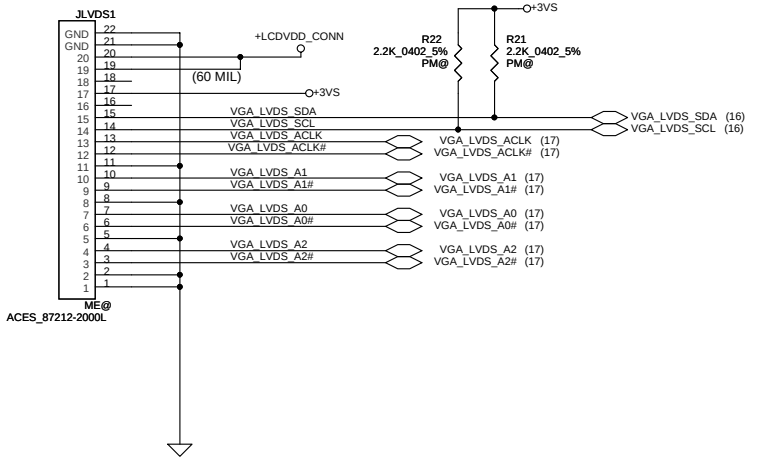




LCD/PANEL BD. Conn.



LCD/PANEL BD. Conn.



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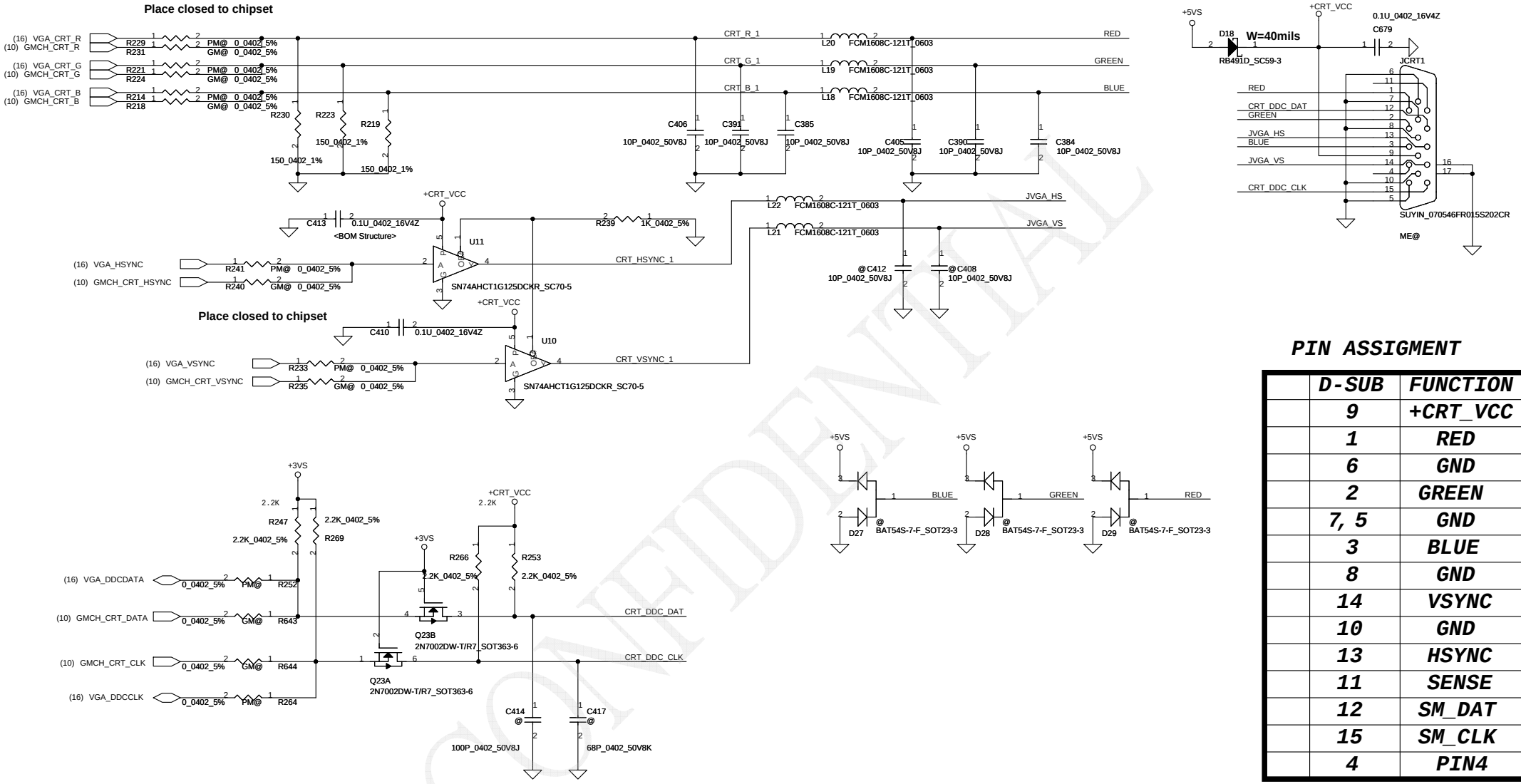
CRT Connector



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

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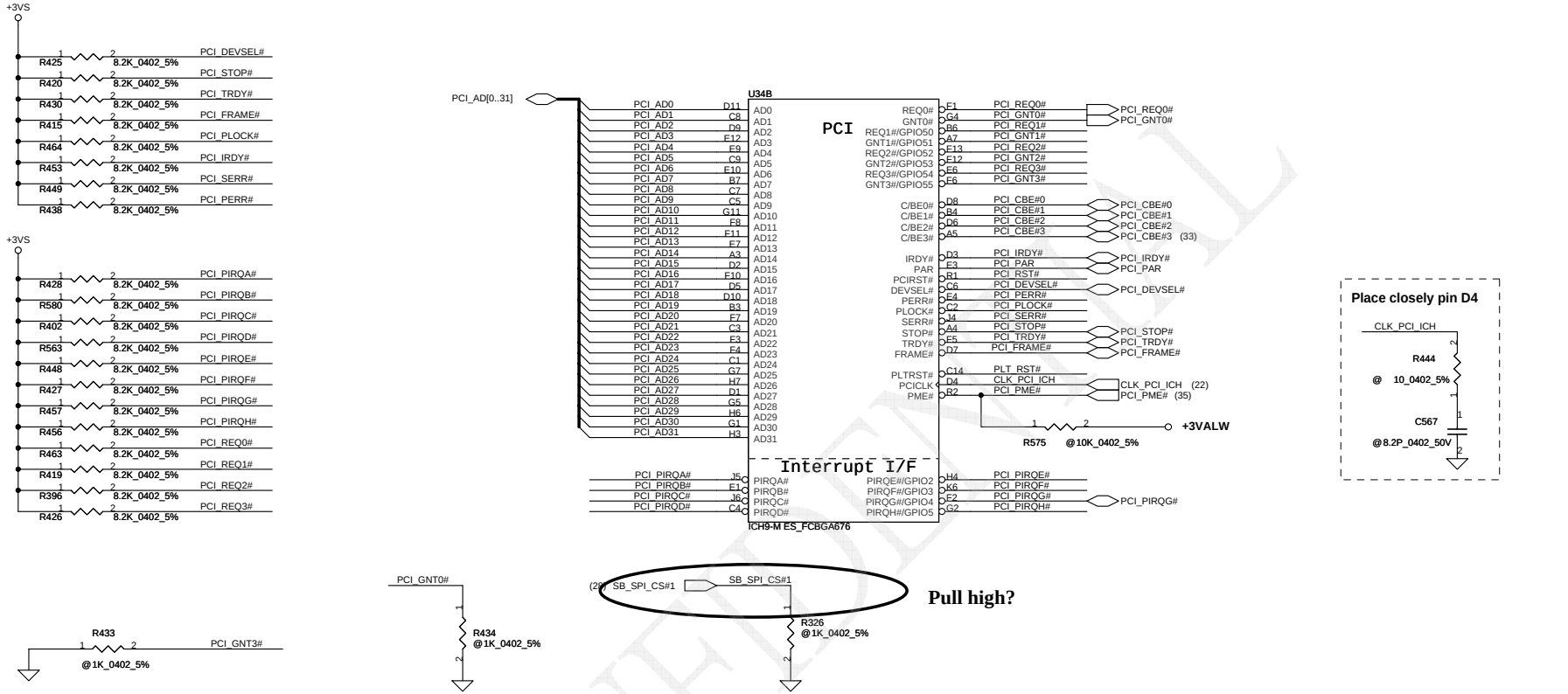

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

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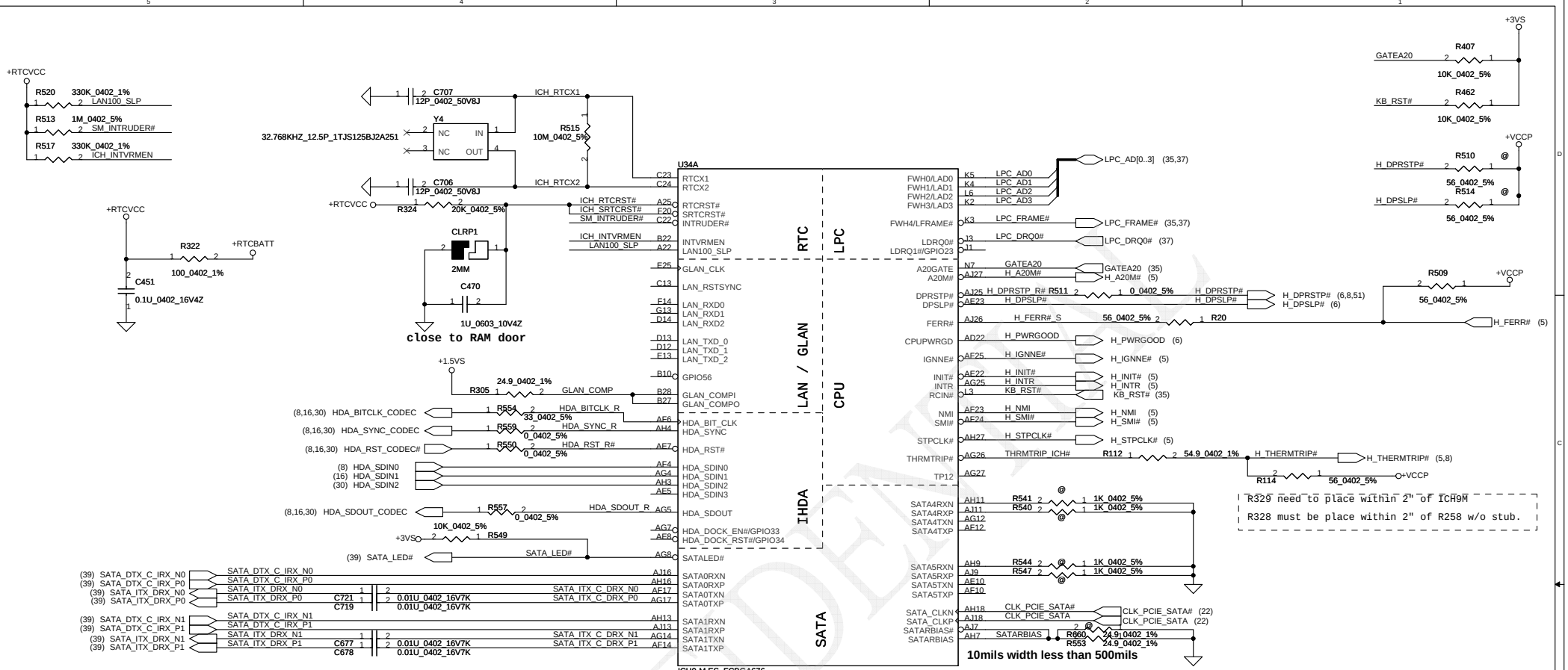

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

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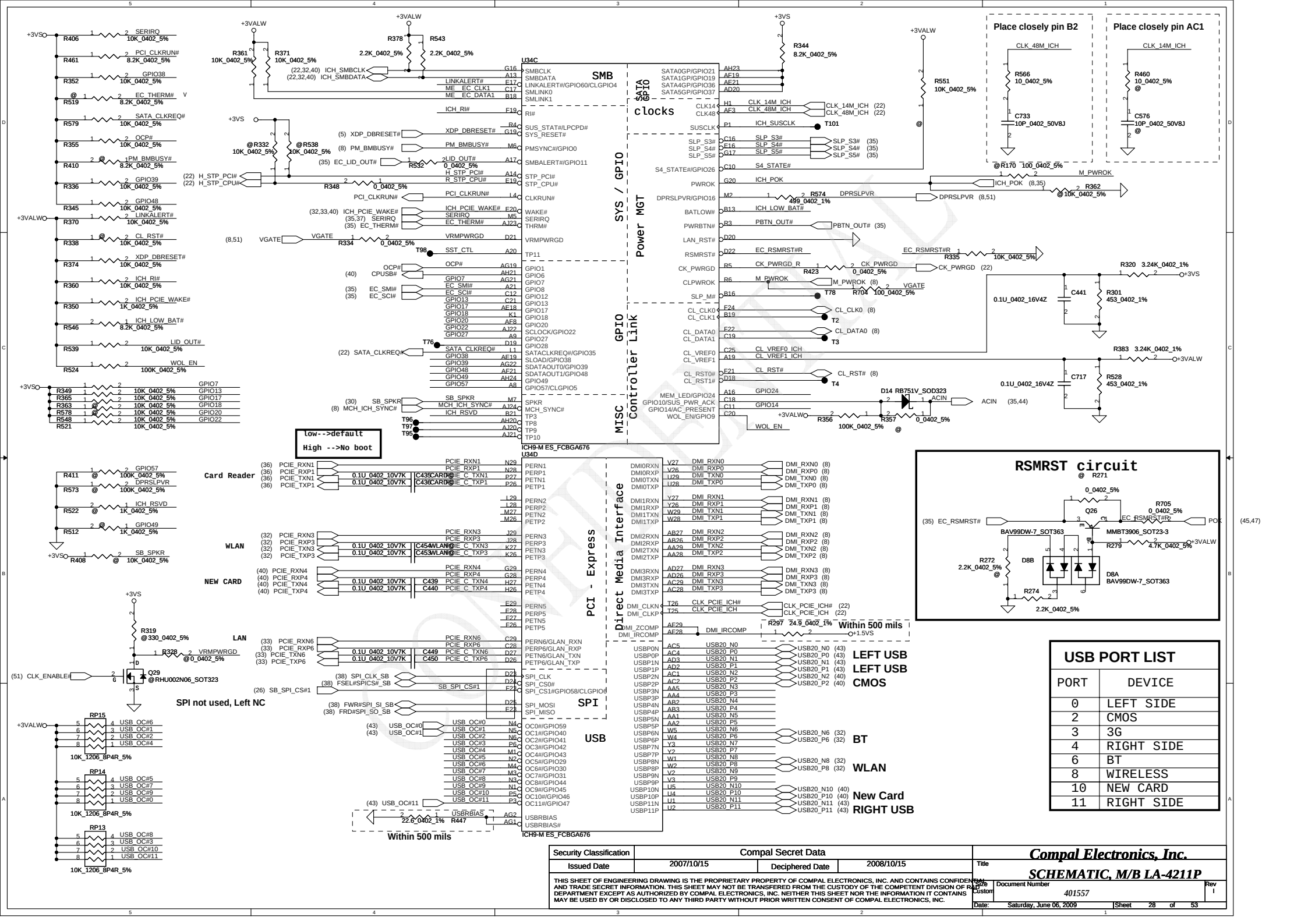

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
2	CMOS
3	3G
4	RIGHT SIDE
6	BT
8	WIRELESS
10	NEW CARD
11	RIGHT SIDE

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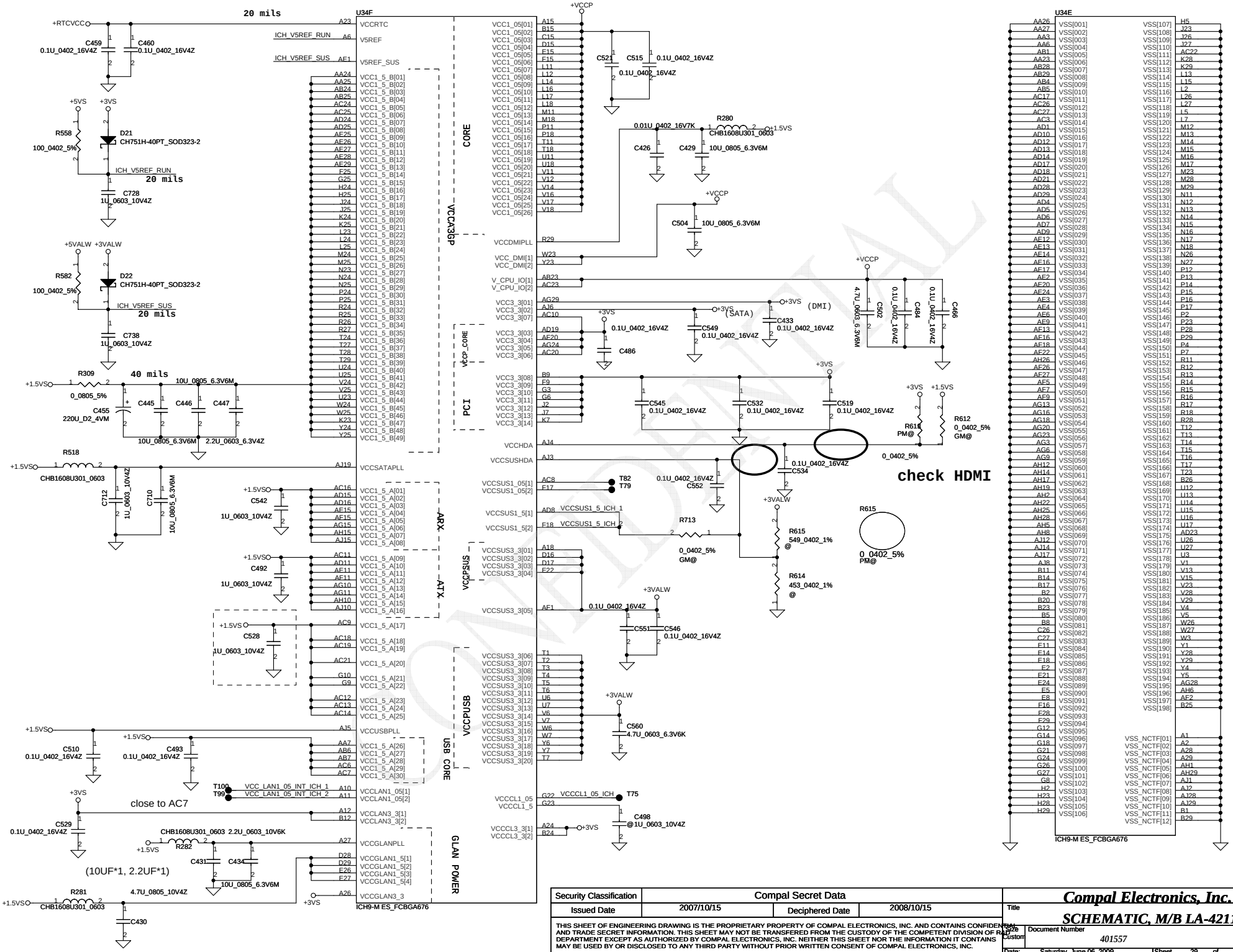

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AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CX20548 AMOM DAA

U15 — CX20561-12Z_LQFP48_7X7

PC_BEEP dB control

0216_Change value.

CODEC POWER

(3.33V)
250mW

W=40Mil

2.2kohm for MICL + MICR
4.7kohm for MICL or MICR

APE8805A-33Y5P_SOT23-5

external MIC

Internal MIC / Array MIC
Internal WOOFER
Internal SPKR.

port A : 5.11K ohm
port B : 10.0K ohm
port C : 20.0K ohm
port D : 39.2K ohm

DIGITAL ANALOG

GND GNDA

Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

CX20548 AMOM DAA

FOX_JM74613-P2002-7F
ME@

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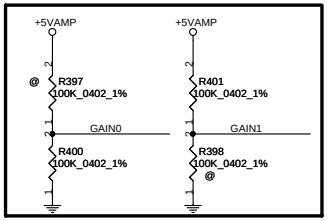
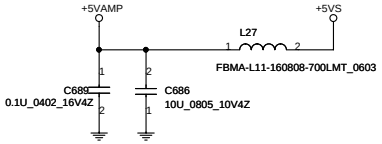
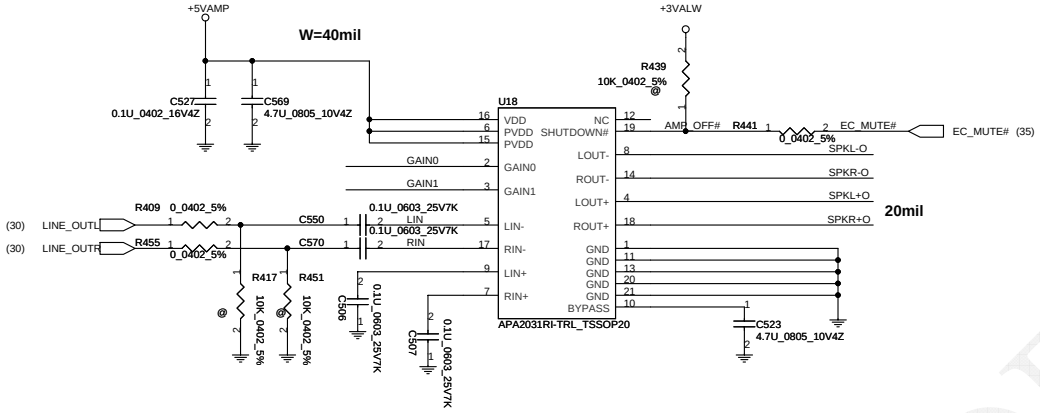
Speaker Amplifier

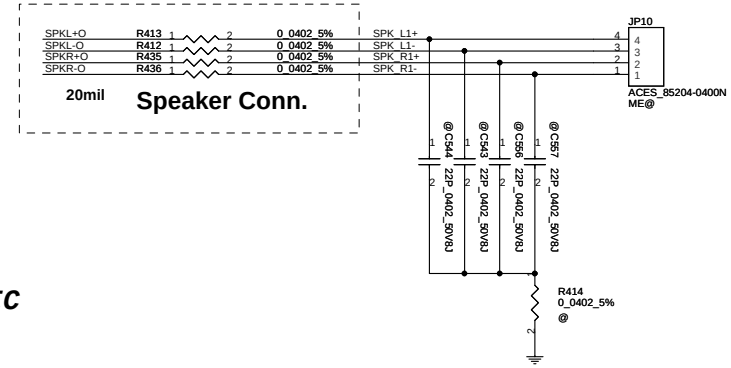
1nd = TPA6017 (SA601720010)
2nd = APA2031 (SA00001RZ00)



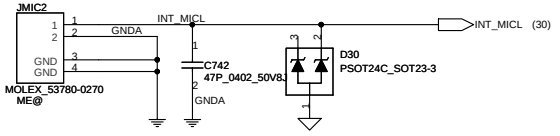
GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB







INT MIC



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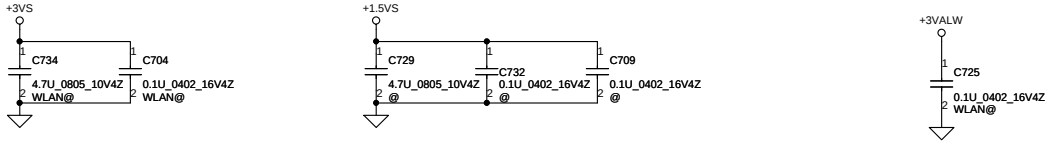
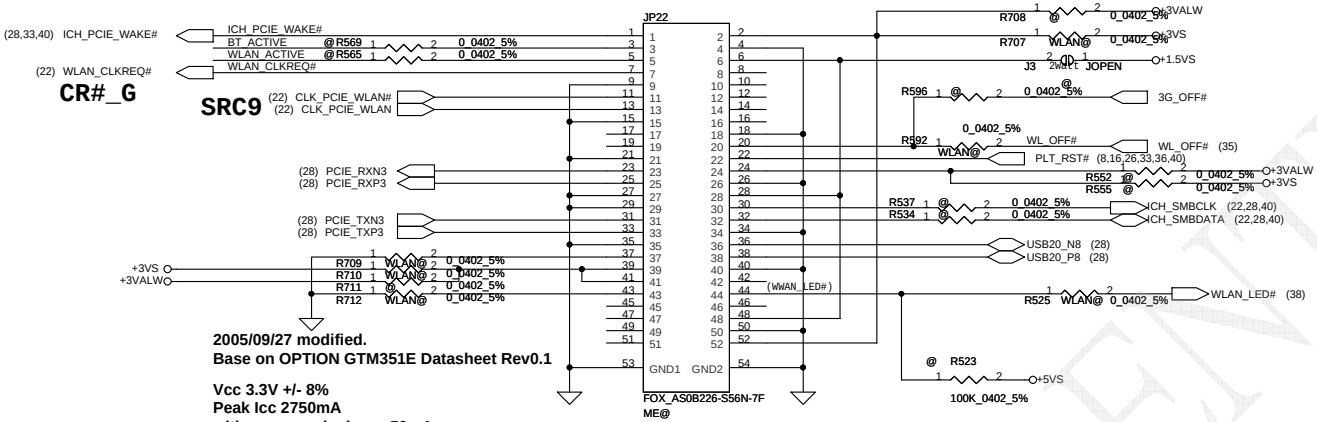
Mini-Express Card for 3G Or TV Tuner
Mini-Express Card for WLAN



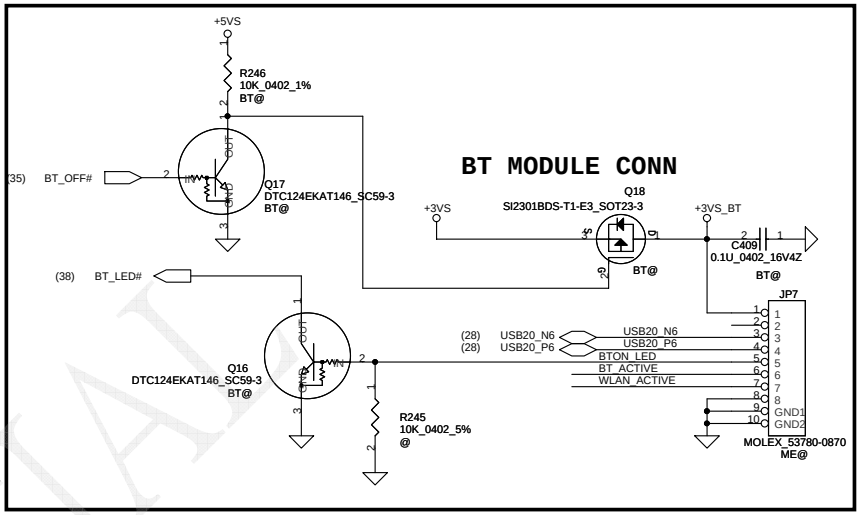
Mini-Express Card(Slot 1-WLAN)



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

BT MODULE CONN



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Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

Notice : 4.7u 6.3V capactor Thickness 1.25mm

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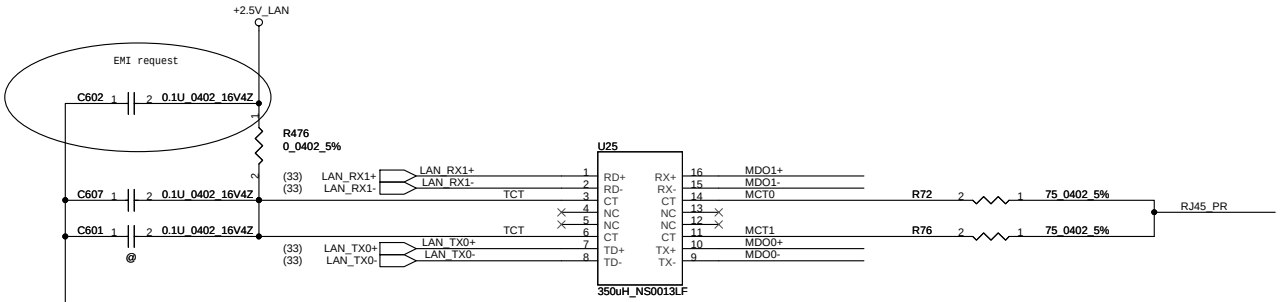
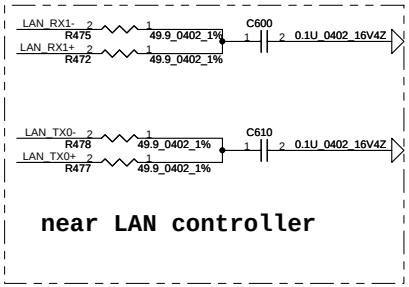
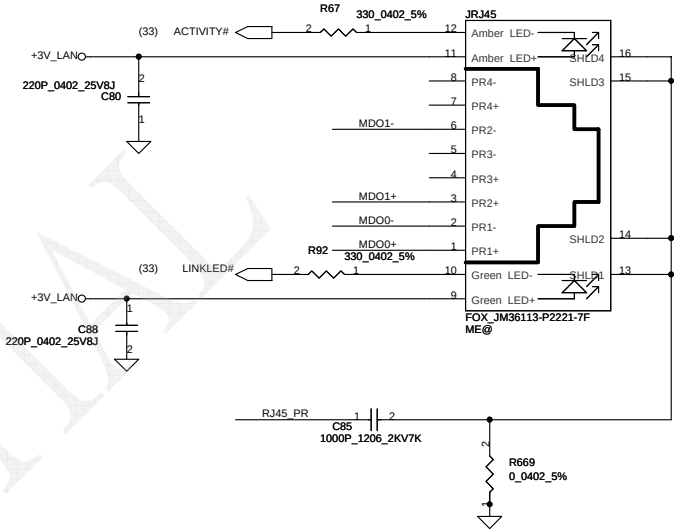
RJ45 CONN



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF





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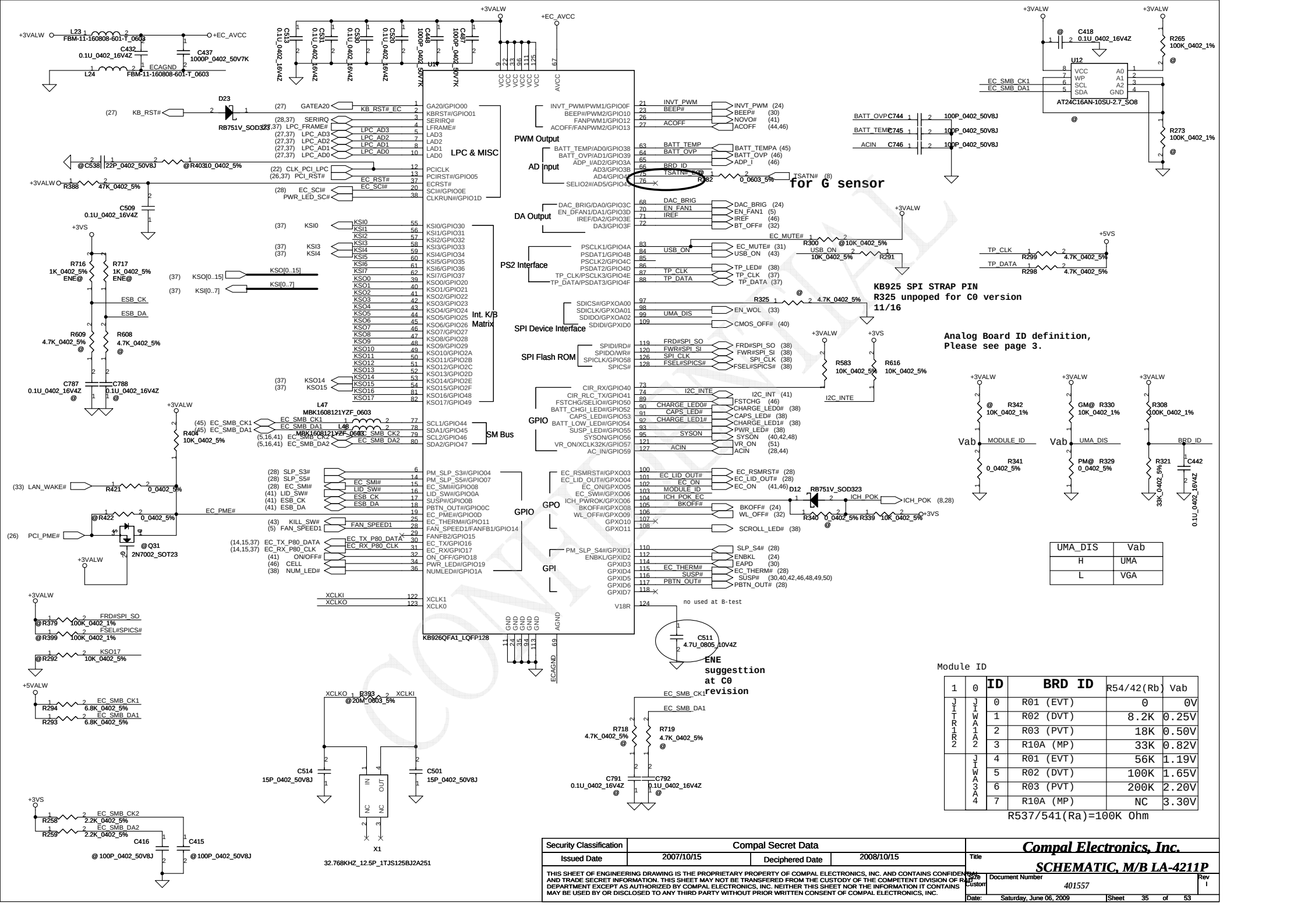

UMA_DIS	Vab
H	UMA
L	VGA

Module ID

1	0	ID	BRD ID	R54/42(Rb)	Vab
JITR12	JIWA12	0	R01 (EVT)	0	0V
		1	R02 (DVT)	8.2K	0.25V
		2	R03 (PVT)	18K	0.50V
		3	R10A (MP)	33K	0.82V
	JIWA34	4	R01 (EVT)	56K	1.19V
		5	R02 (DVT)	100K	1.65V
		6	R03 (PVT)	200K	2.20V
		7	R10A (MP)	NC	3.30V

R537/541(Ra)=100K Ohm

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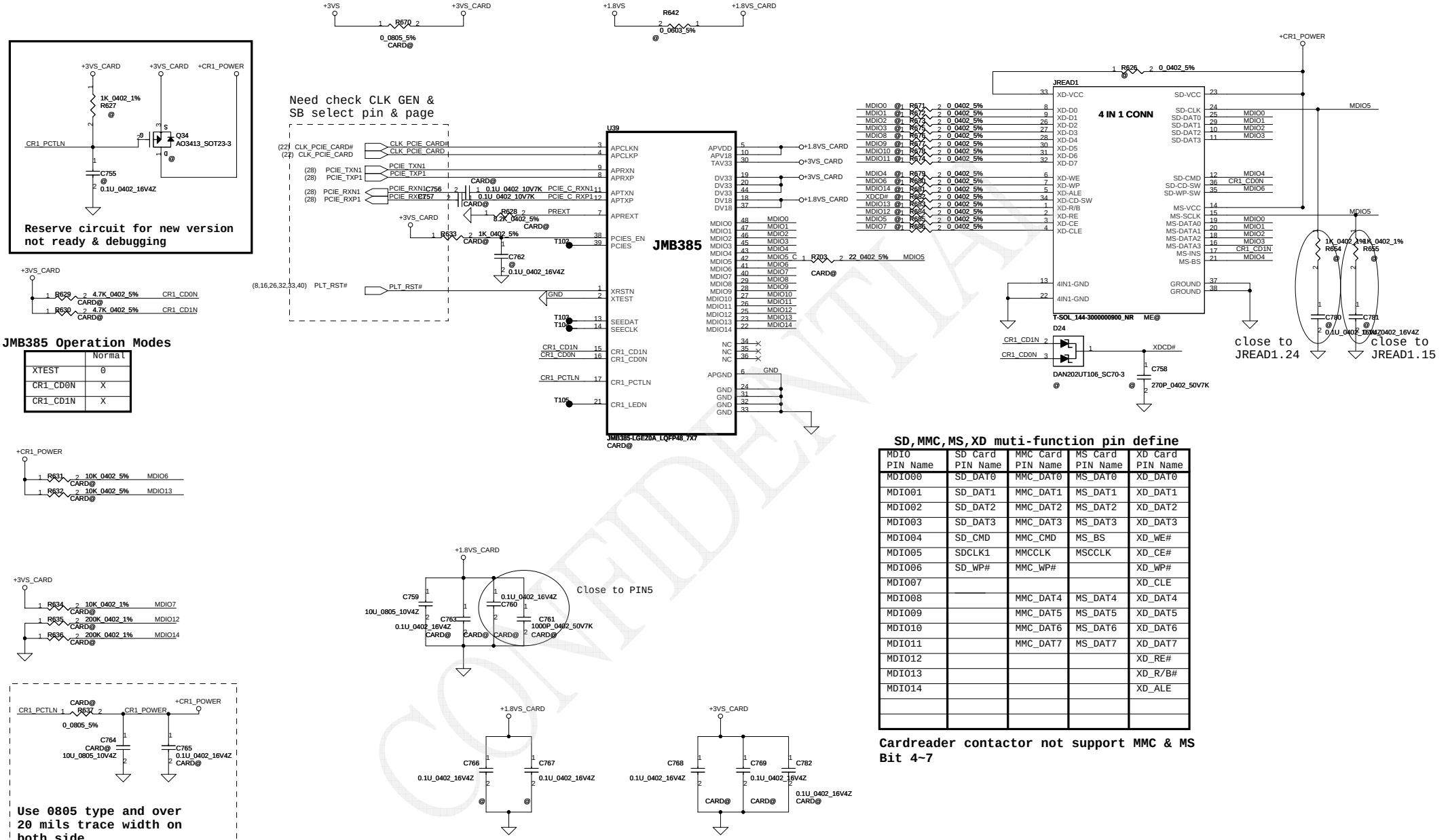

JMB385 Operation Modes

	Normal
XTEST	0
CR1_CD0N	X
CR1_CD1N	X

SD,MMC,MS,XD muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SD_DAT0	MMC_DAT0	MS_DAT0	XD_DAT0
MDIO01	SD_DAT1	MMC_DAT1	MS_DAT1	XD_DAT1
MDIO02	SD_DAT2	MMC_DAT2	MS_DAT2	XD_DAT2
MDIO03	SD_DAT3	MMC_DAT3	MS_DAT3	XD_DAT3
MDIO04	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO05	SDCLK1	MMCCLK	MSCCLK	XD_CE#
MDIO06	SD_WP#	MMC_WP#		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_DAT4	MS_DAT4	XD_DAT4
MDIO09		MMC_DAT5	MS_DAT5	XD_DAT5
MDIO10		MMC_DAT6	MS_DAT6	XD_DAT6
MDIO11		MMC_DAT7	MS_DAT7	XD_DAT7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE

Cardreader contactor not support MMC & MS Bit 4~7

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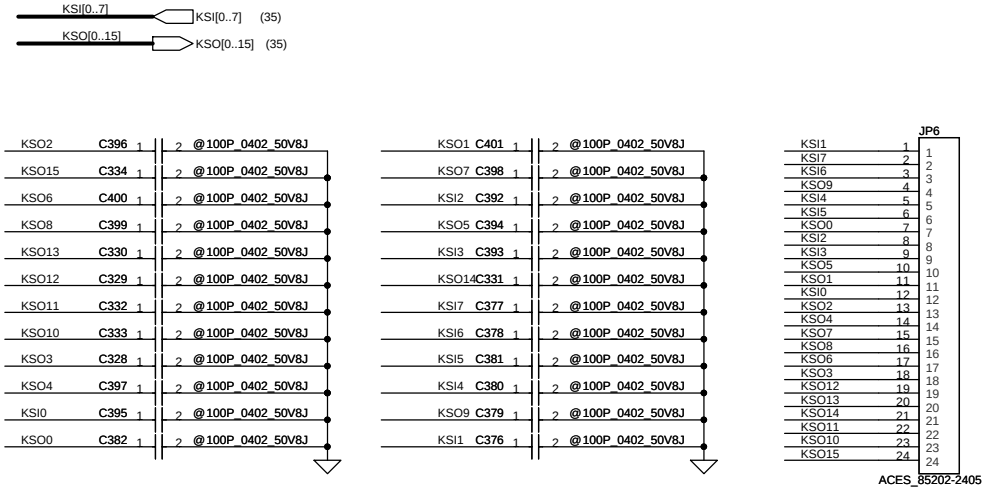
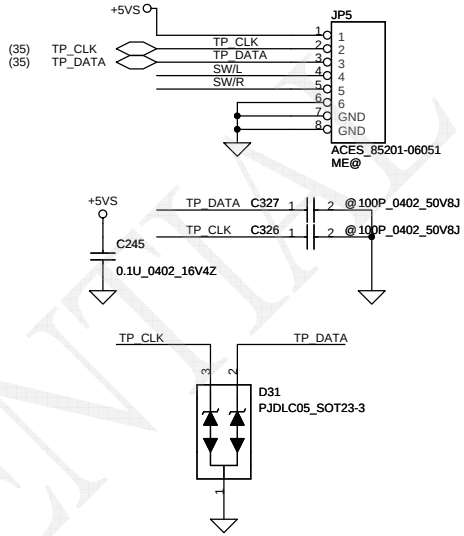
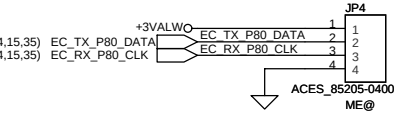
INT_KBD Conn.

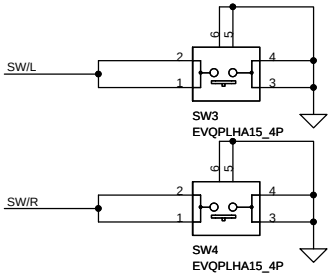


To TP/B Conn.

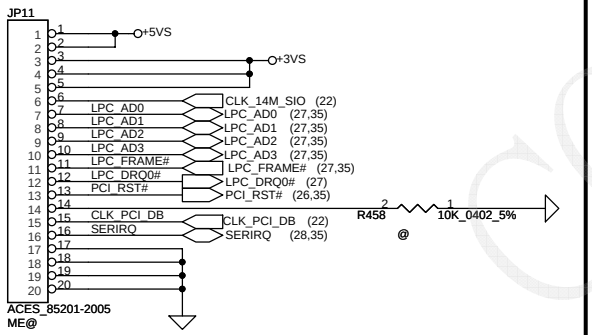


EC DEBUG PORT





FOR LPC SIO DEBUG PORT



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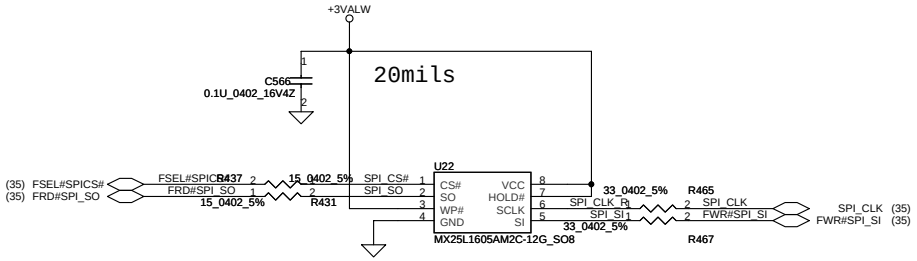
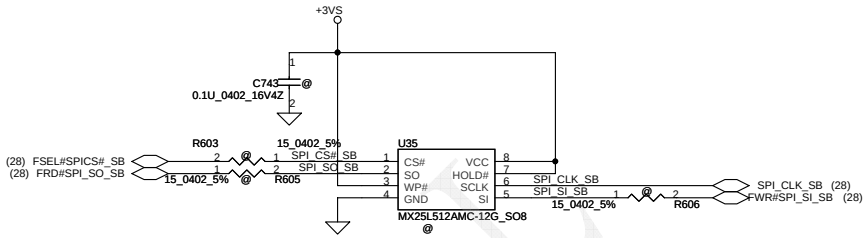
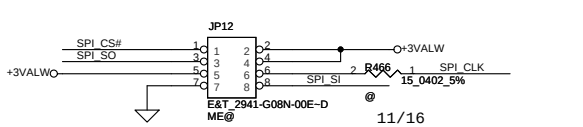
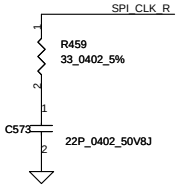
FOR EC 8M SPI ROM



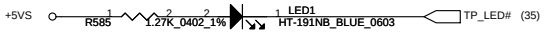


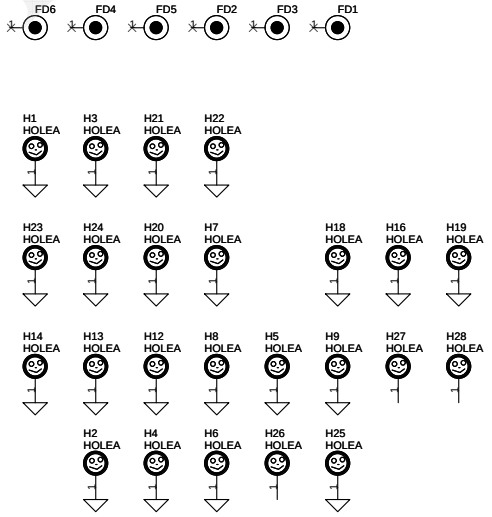


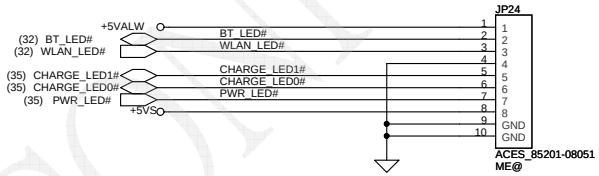
11/16
R466 poped for A test

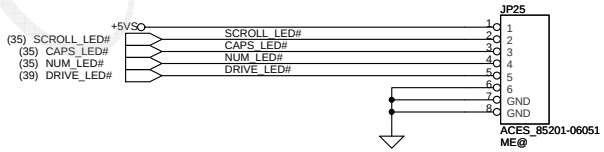


LED









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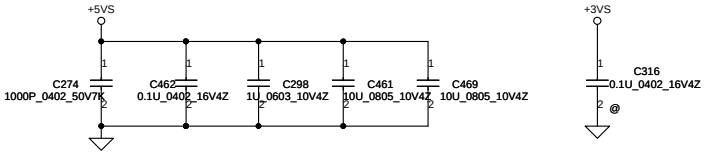
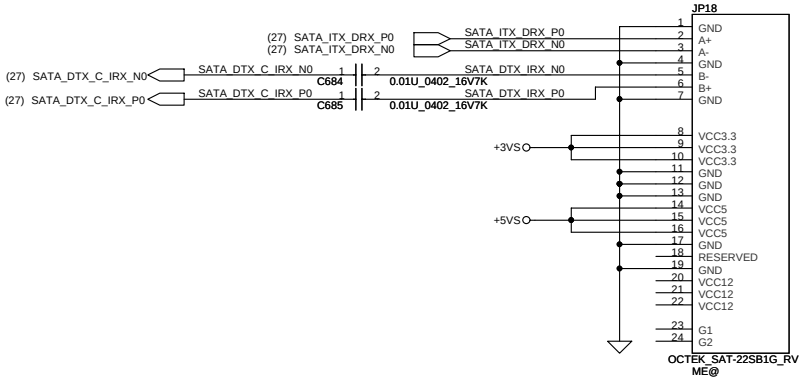
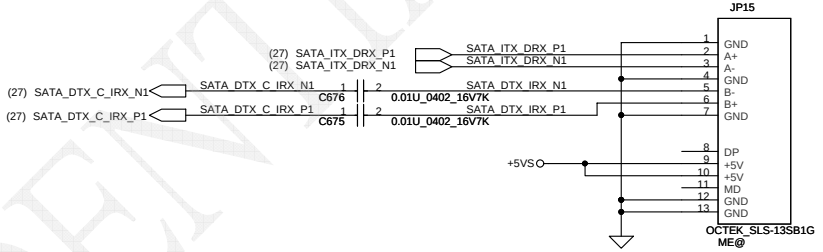
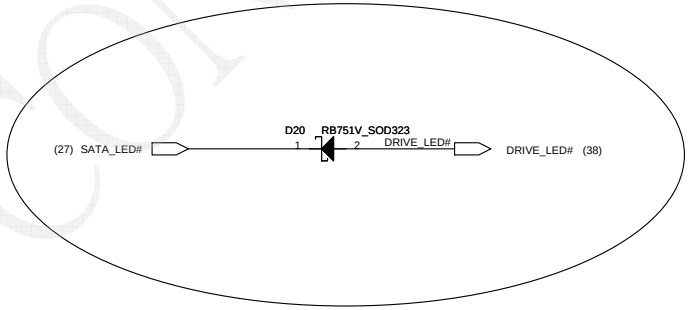


SATA HDD Conn.



SATA ODD Conn.





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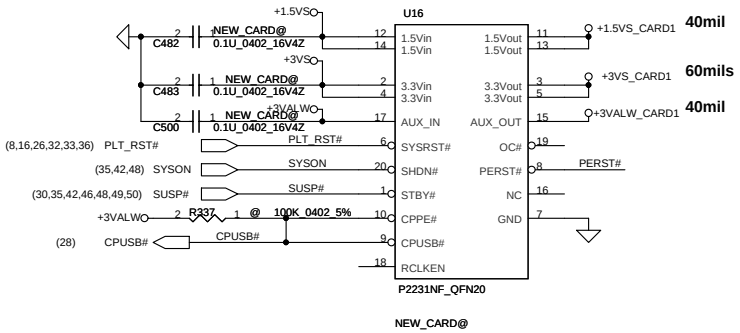
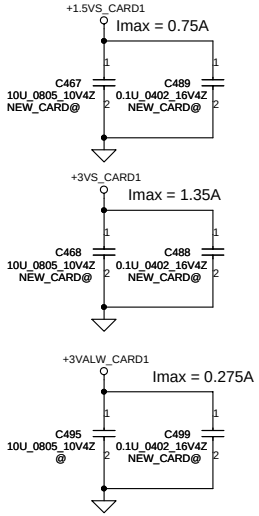
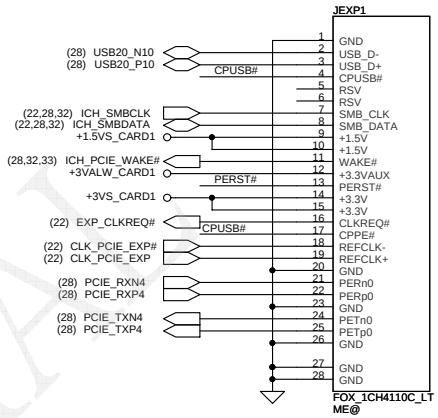
Express Card Power Switch



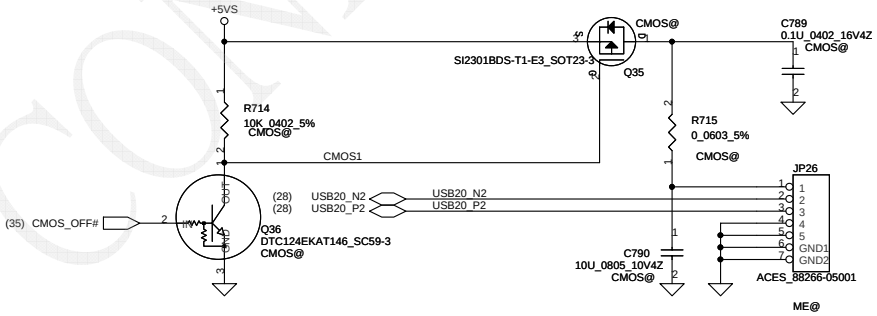


New Card Socket (Left/TOP)



(NEW)

CMOS Camera Conn



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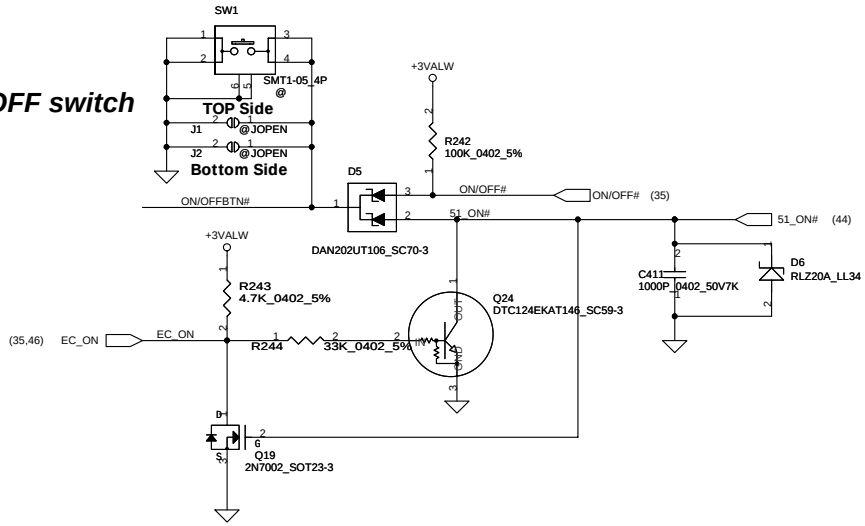
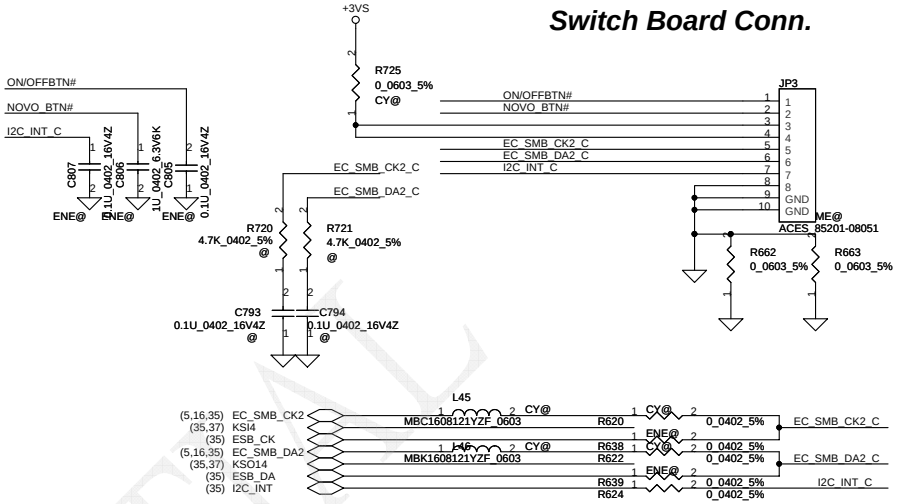
Power Button

ON/OFF switch

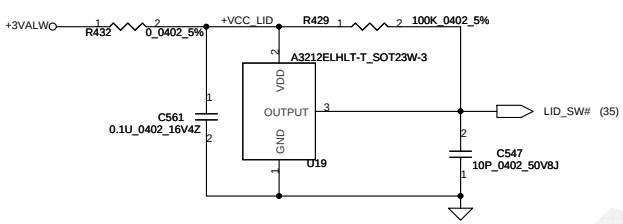


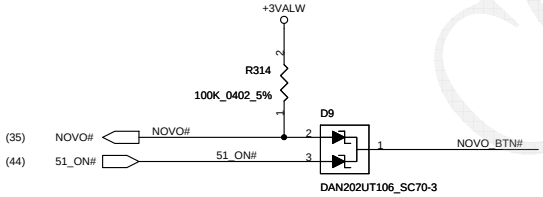
Switch Board Conn.



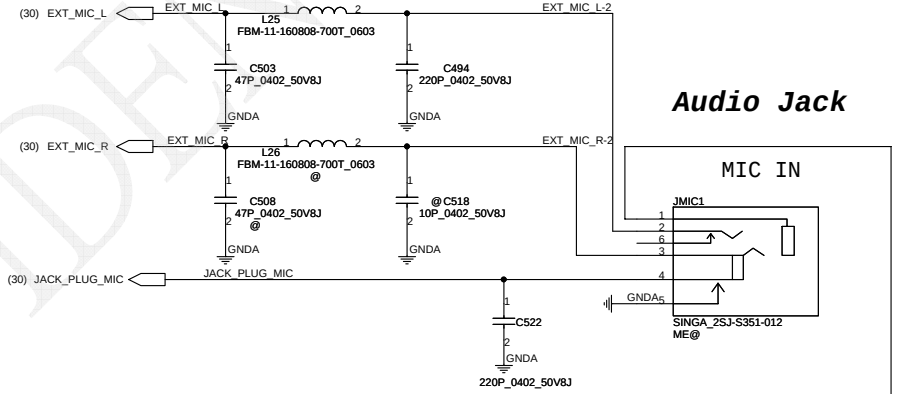
8 mil

Lid Switch

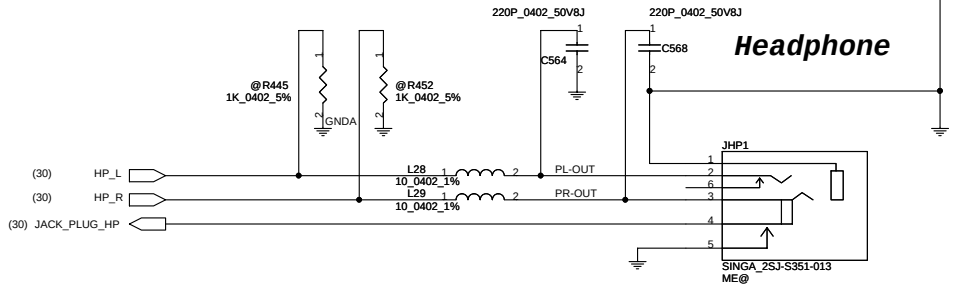




Audio Jack



Headphone



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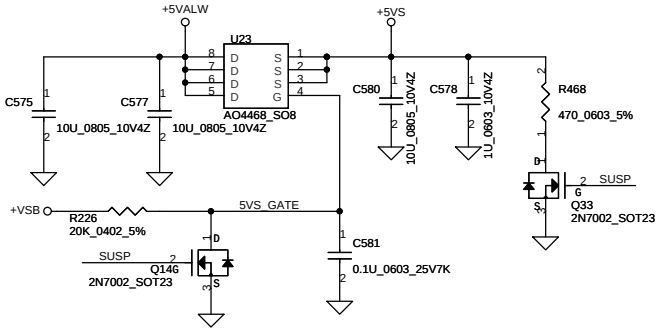
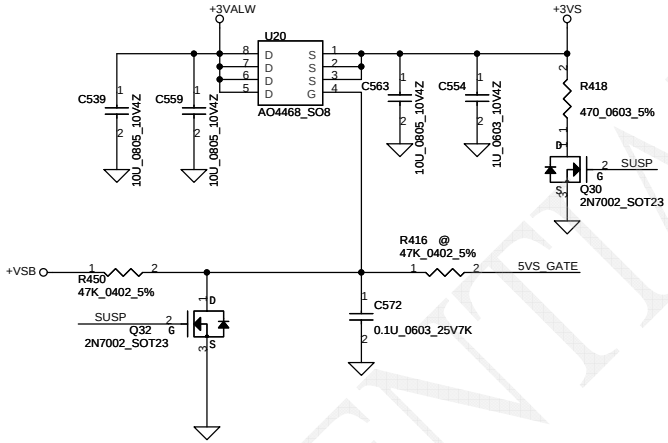
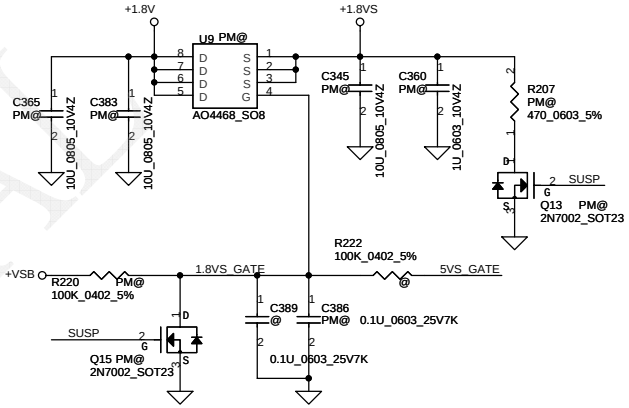
+5VALW TO +5VS

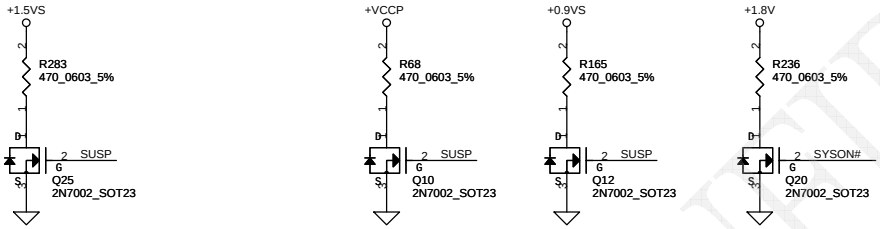


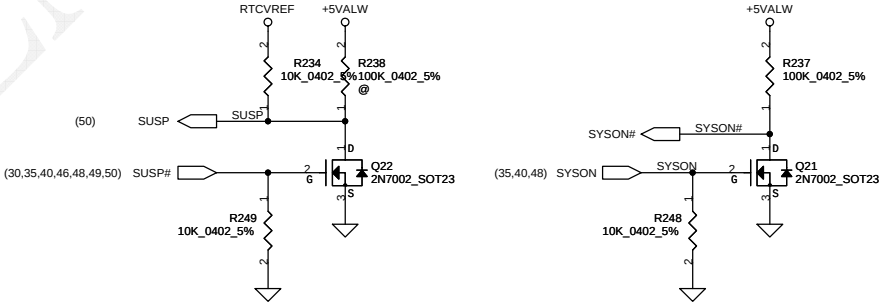
+3VALW TO +3VS



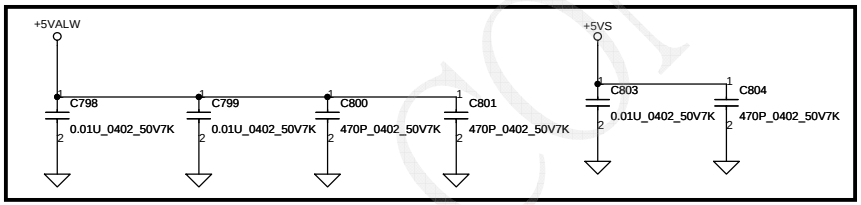
+1.8V to +1.8VS







for EMI



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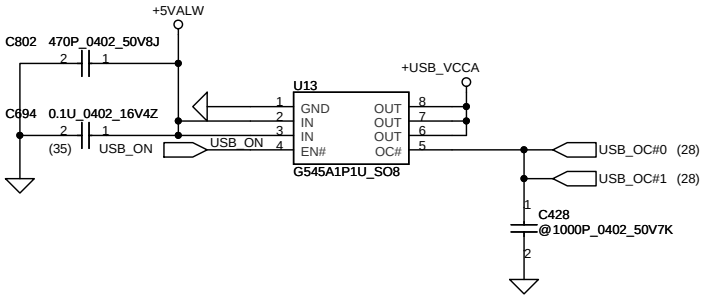
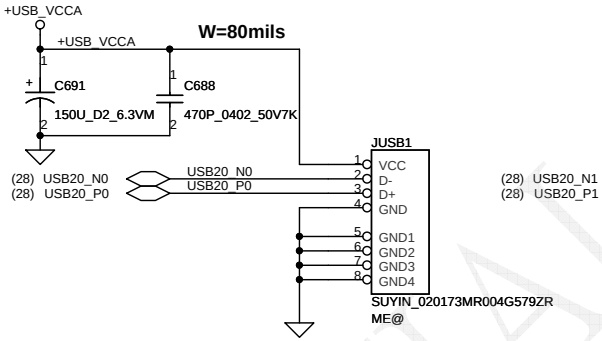
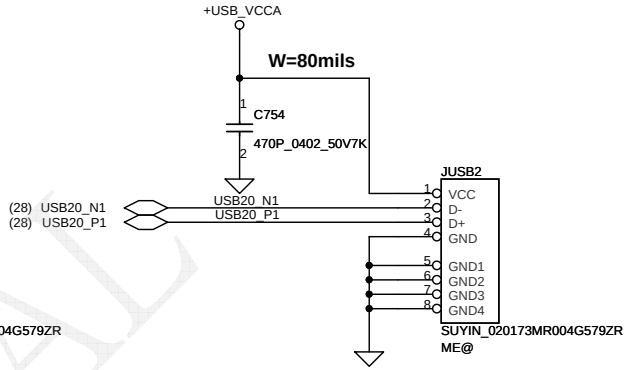


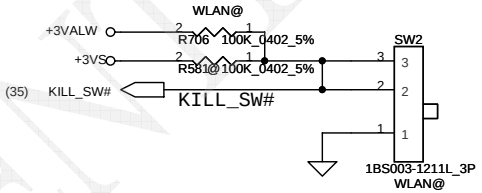
LIFT USB CONN. 1

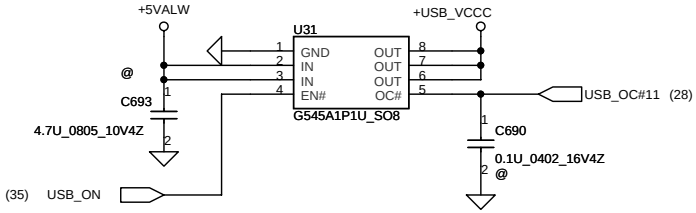


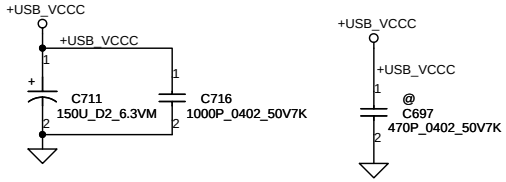
LIFT USB CONN. 2



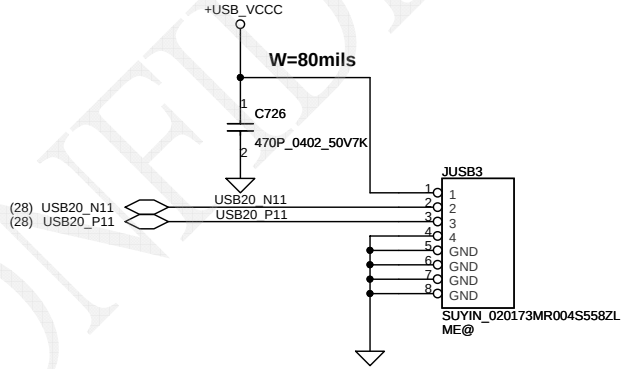
Kill Switch







RIGHT USB CONN. 3



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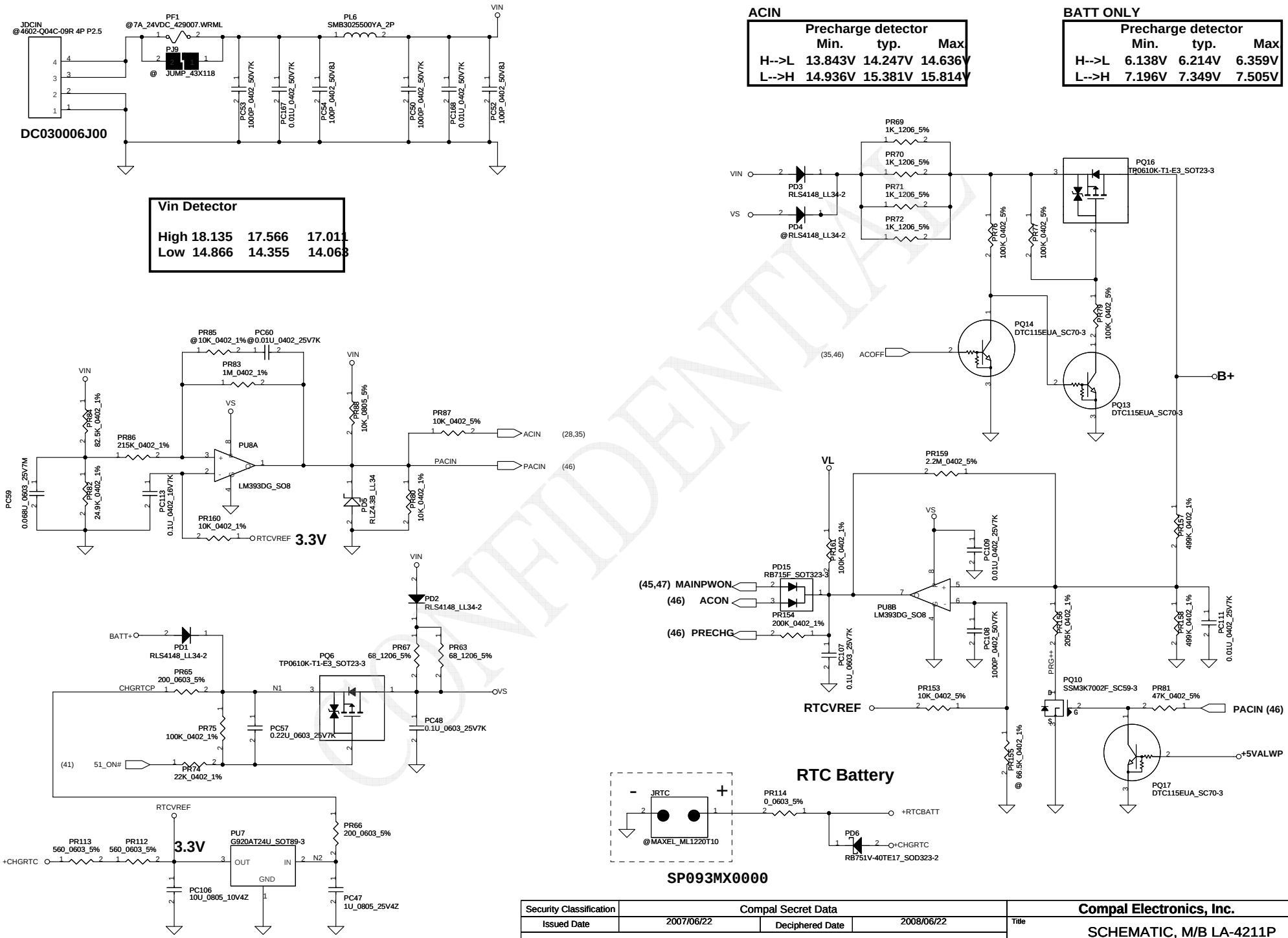

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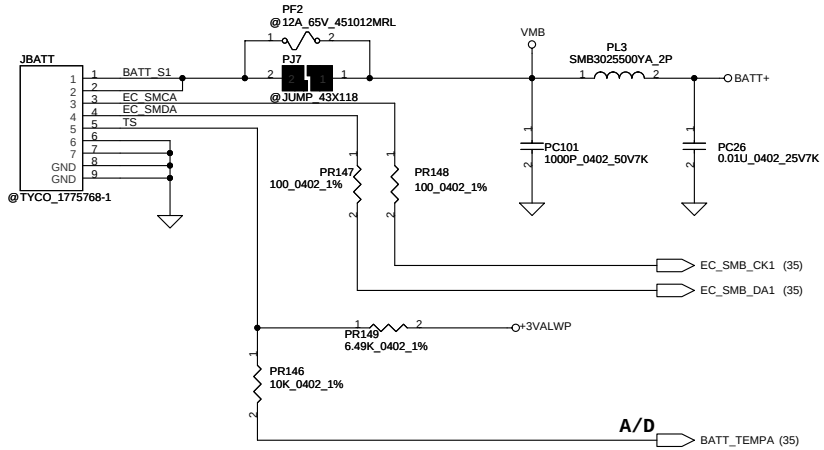
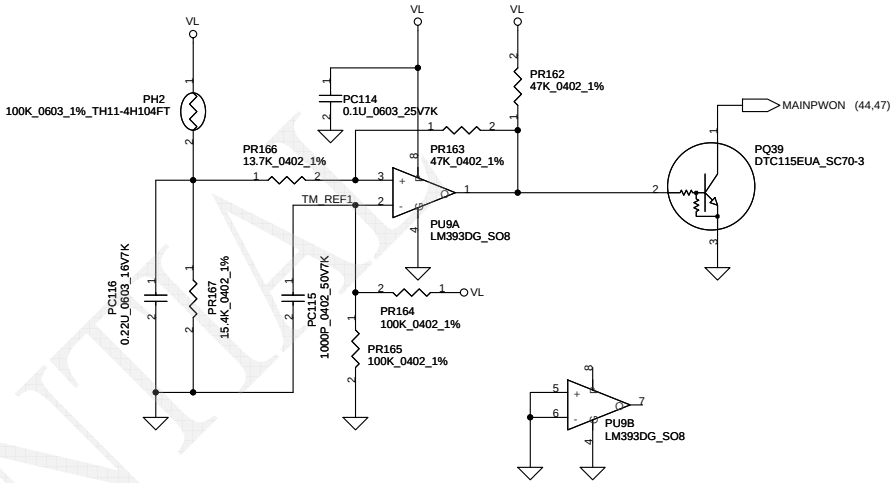
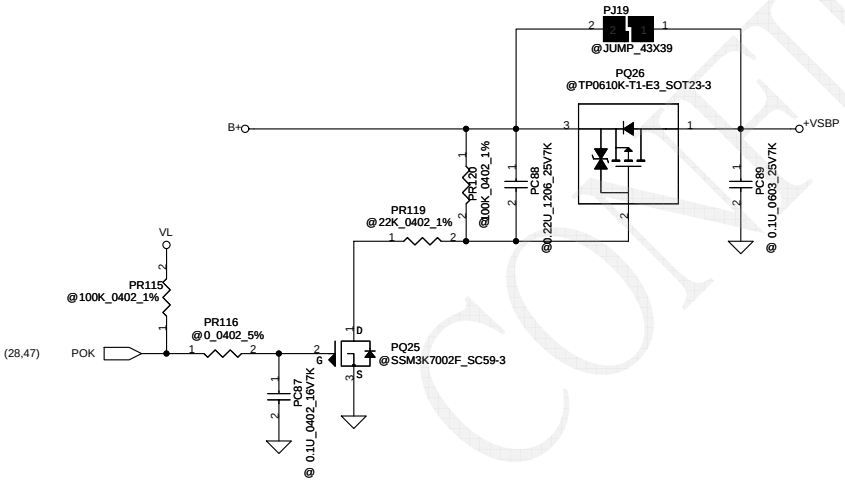
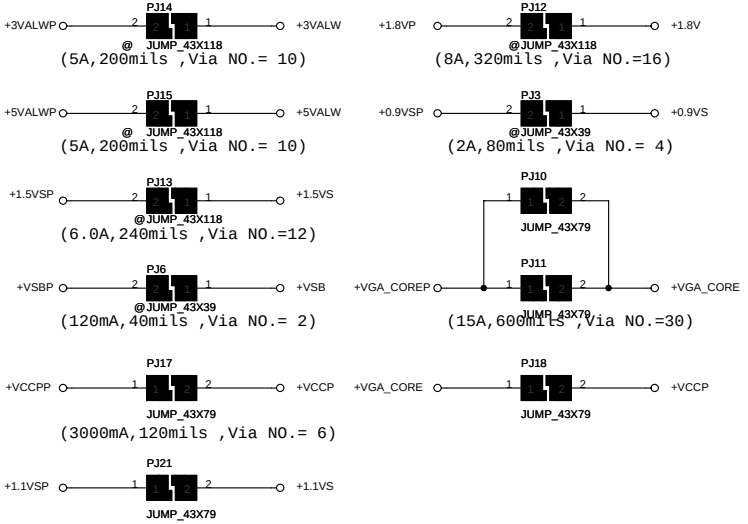
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C









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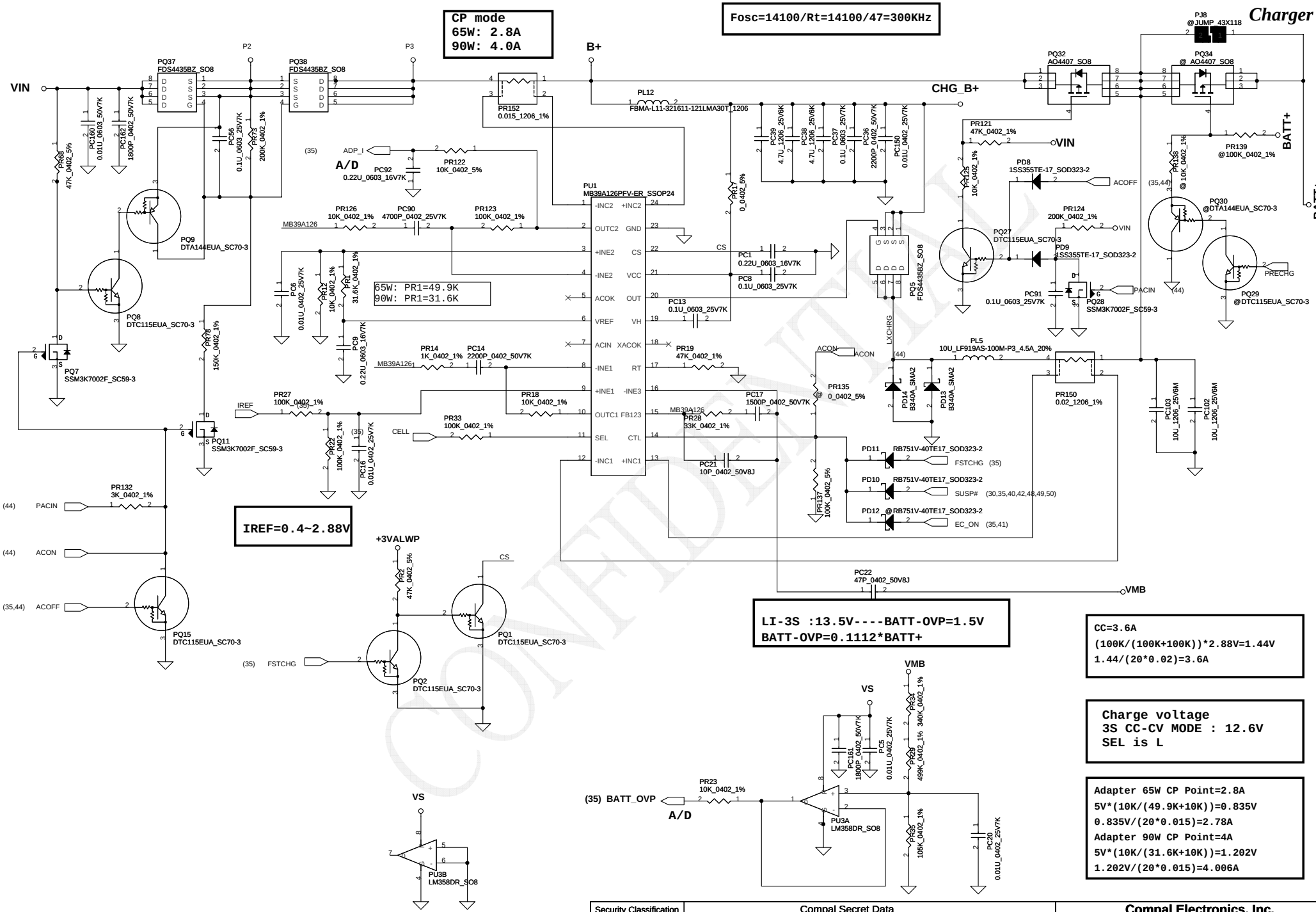
Charger

CP mode
65W: 2.8A
90W: 4.0A

Fosc=14100/Rt=14100/47=300KHz



Security Classification	Compal Secret Data		
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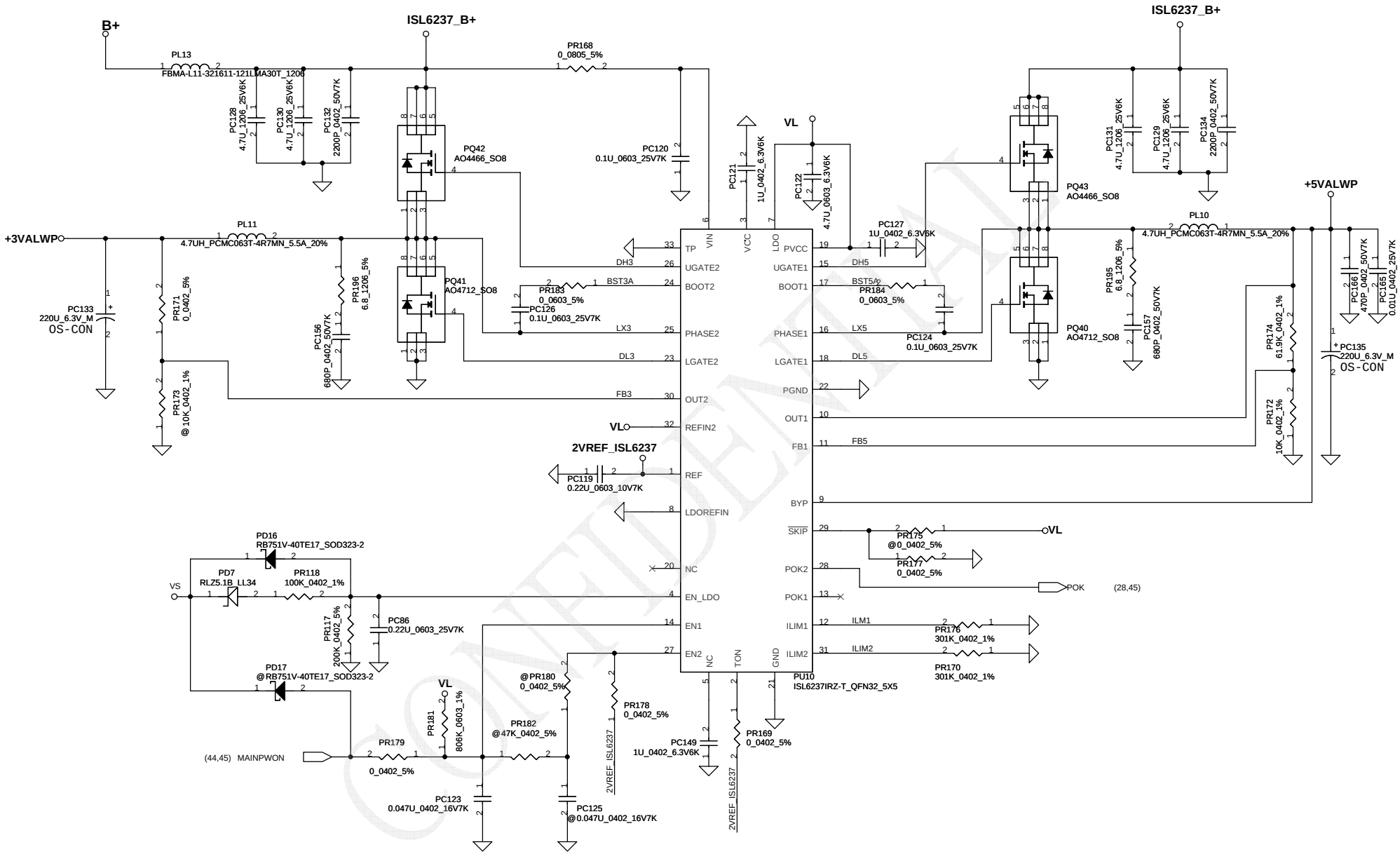

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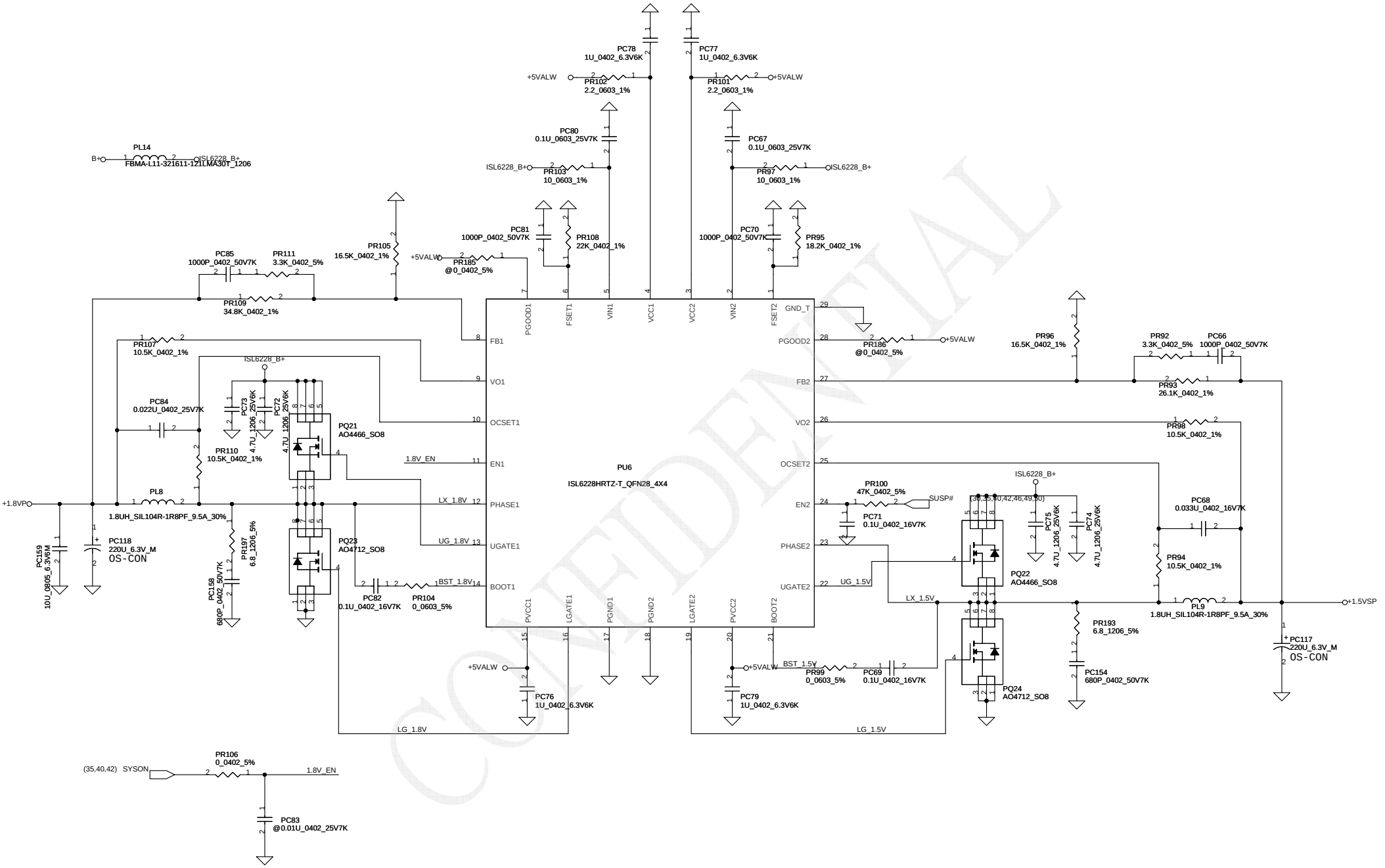

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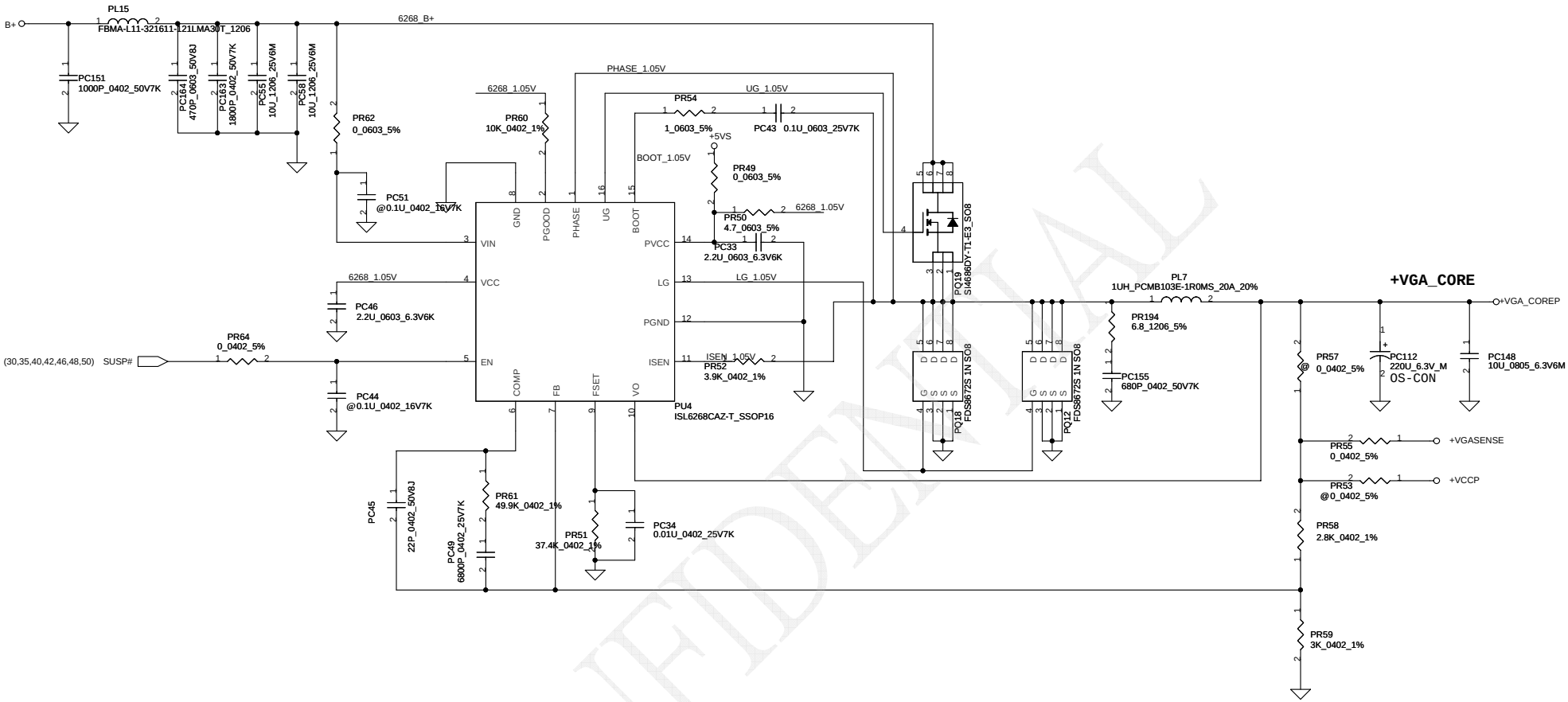

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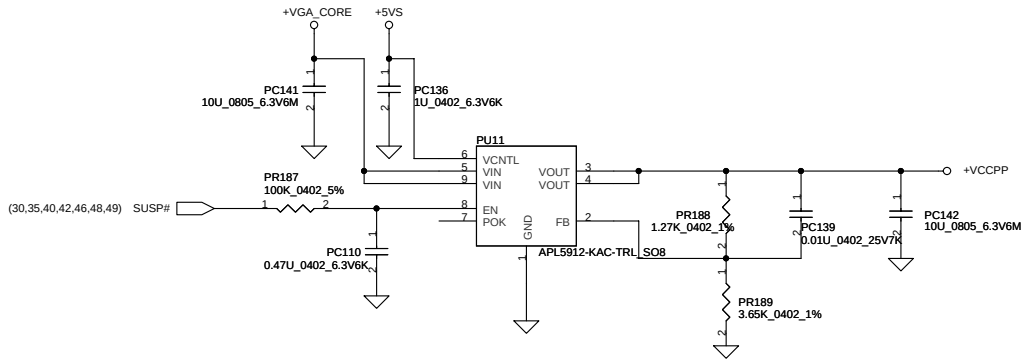

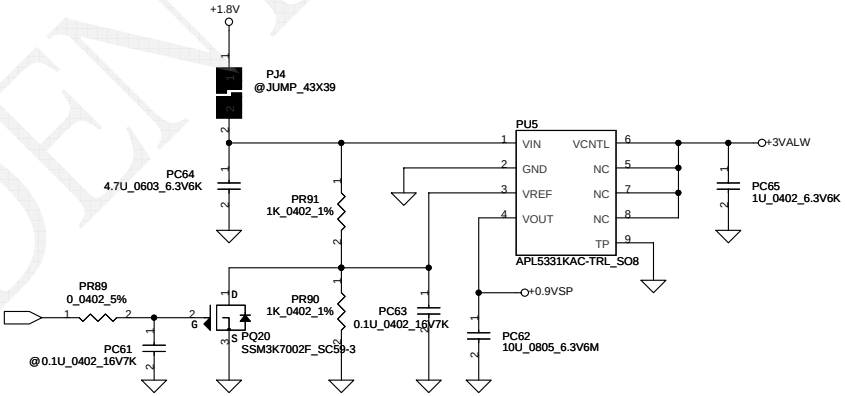

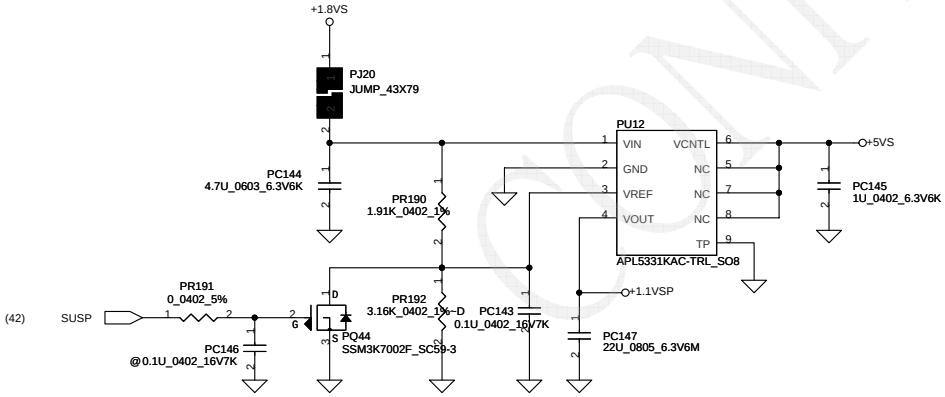

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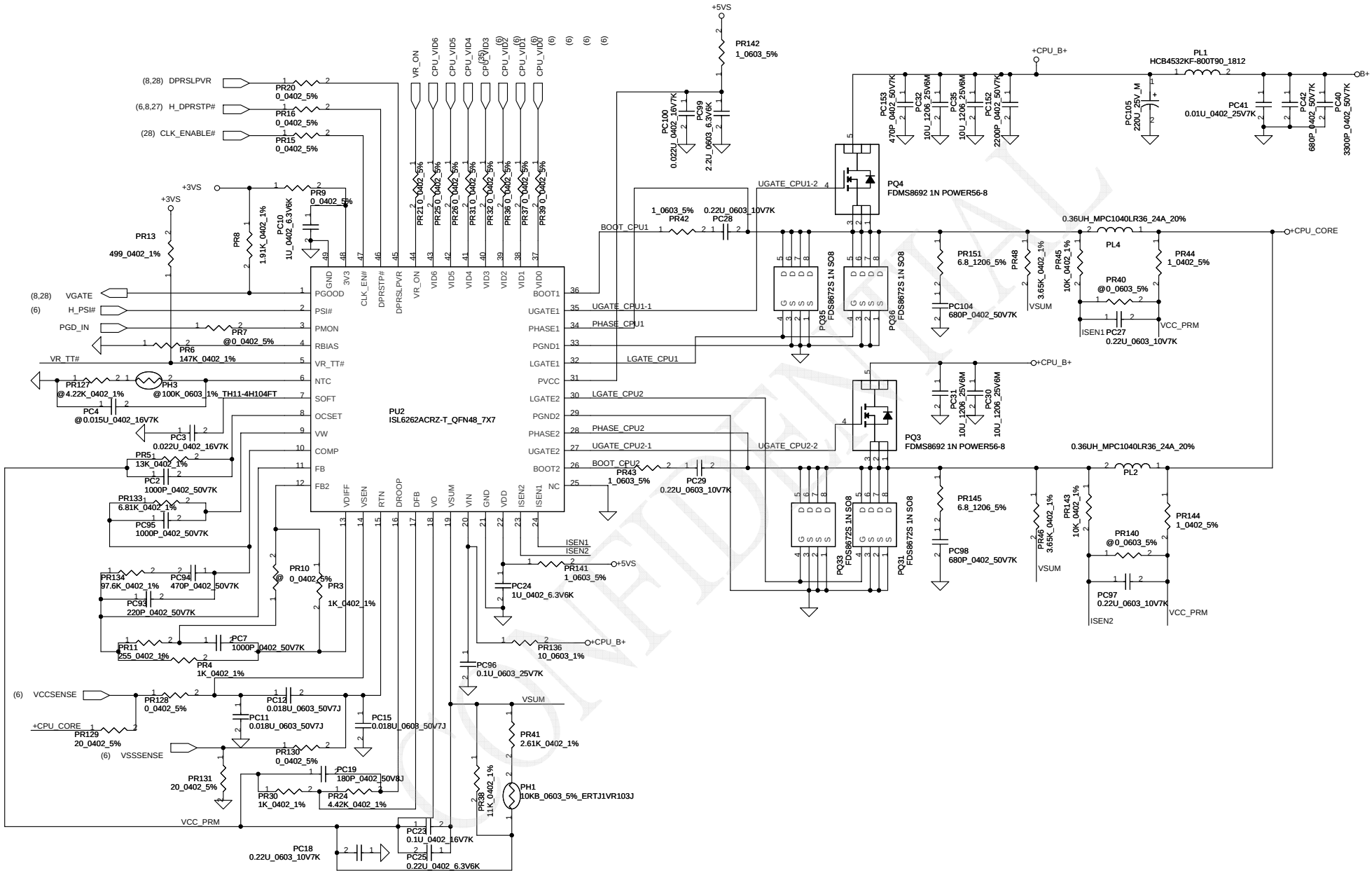

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	10/12	P48	Add PR185, PR186	Reserve for debug use.
	10/12	P49	Delete PC110	Because HW reserve enough CAP.
	10/17	P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
	10/17	P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/10	P29	C615 change to R615 and BOM Structure change to PM@	Fix DIS Audio issue
2	12/10	P20、P21	R104 & R154 BOM Structure change to PM@	Reduce cost
3	12/10	P16	R86、R645、R646、R650、R651、R652 & R653 BOM Structure change to PM@	Reduce cost
4	12/10	P29	R614 change from 10K to 45.3ohm R615 change from 12K to 54.9ohm	Fix UMA Audio issue
5	12/10	P08	R79 change from 33 to 10ohm R80、R81、R82 & R85 change from 0 to 22 ohm	Fix UMA Audio issue
6	12/10	P30	The C783 links to GND	Fix Internal MIC issue
7	12/10	P41	Add L45 & L46 MBC1608121YZF Bead	Fix F/B issue
8	01/02	P11	Change C126 package	
9	01/02	P28	Add R704 to connect VGATE to M_PWROK	Modify power sequence
10	01/02	P16	Add R699 to connect +VGASENSE	
11	01/02	P16	Remove U3.P1	
12	01/02	P16	Add R700 to connect GND	
13	02/15	P08	Change R147 from 511 ohm 1% to 499 ohm 1%	
14	02/15	P23	Change D4 location	
15	02/15	P23	Add D25 & D26 for ESD	
16	02/15	P25	Add D27、D28 & D29 for ESD	
17	02/15	P29	Add R713 connect to 1.5V	
18	05/08	P05	Add R726 1k ohm & C808 0.1uF to fix issue.	
19	05/08	P16	Remove R48 for EMI request.	
20	05/08	P23	Remove HDMI function.	
21	05/08	P27	Change R554 from 0 ohm to 33 ohm for EMI request.	
22	05/08	P28	Add R566 10 ohm & C733 10pF for EMI request.	
23	05/08	P30	Add R327 47 ohm & C458 33pF for EMI request.	
24	05/08	P35	Change C501 & C514 from 15pF to 12pF	
25	05/08	P37	Add D31 (PJDLC05_SOT23-3) for ESD request.	
26	05/08	P41	Add C494、C522、C564 & C568 220pF for EMI request	

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