LC22 Schematic

Pentium-M

RS400MD+SB400

DATE: May. 5th Revision: 0.1

Compal Electronics, Inc.		
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36	PWR-CHARGER
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38	PWR-3.3V/5V
39	+1.2VSP & +1.8VALWP
40	PWR 0.9VSP/VCCP
41	PWR CPU_CORE
42	Optional VGA MVCORE Power

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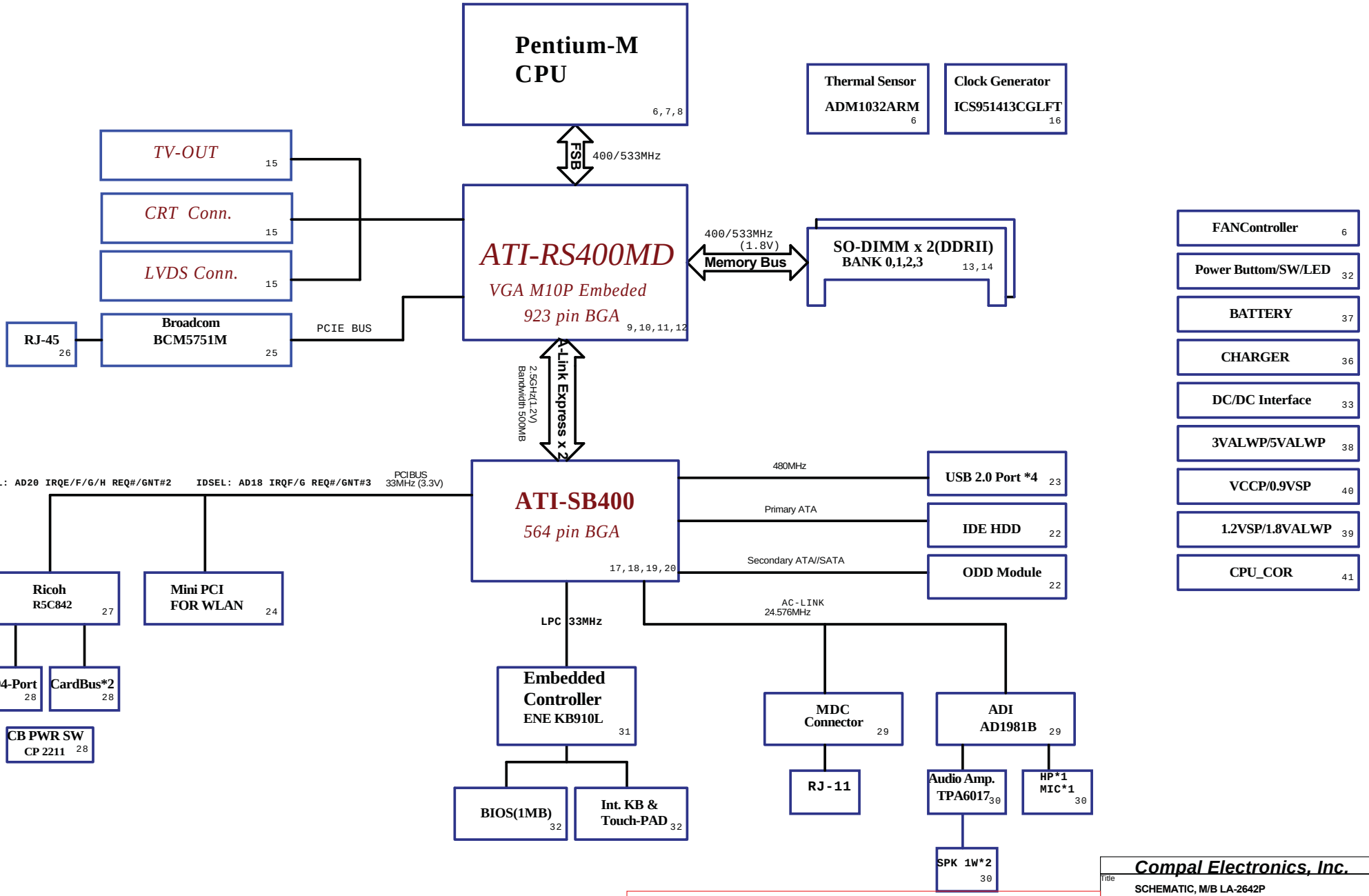
BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+0.9VS	0.9V power rail	ON	OFF	OFF
+3.3V	3.3V switched power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(R5C842)	AD20	2	PIRQE/PIRQF/PIRQG/PIRQH
Mini-PCI(WLAN)	AD18	3	PIRQF/PIRQG

EC SM Bus1 address

Device	Address
Main Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
Second Battery	

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b

SB400 SM Bus address

Device	Address
Clock Generator (ICS951413CYGLFT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

Dip SW function

KBSEL0/1#	11:JP K/B 01:US K/B 10:UK K/B 00: Reserve
PASSWORD#	0:Override 1:Avaliable
FINGERPRINT#	0:Existence 1:Non-Existence

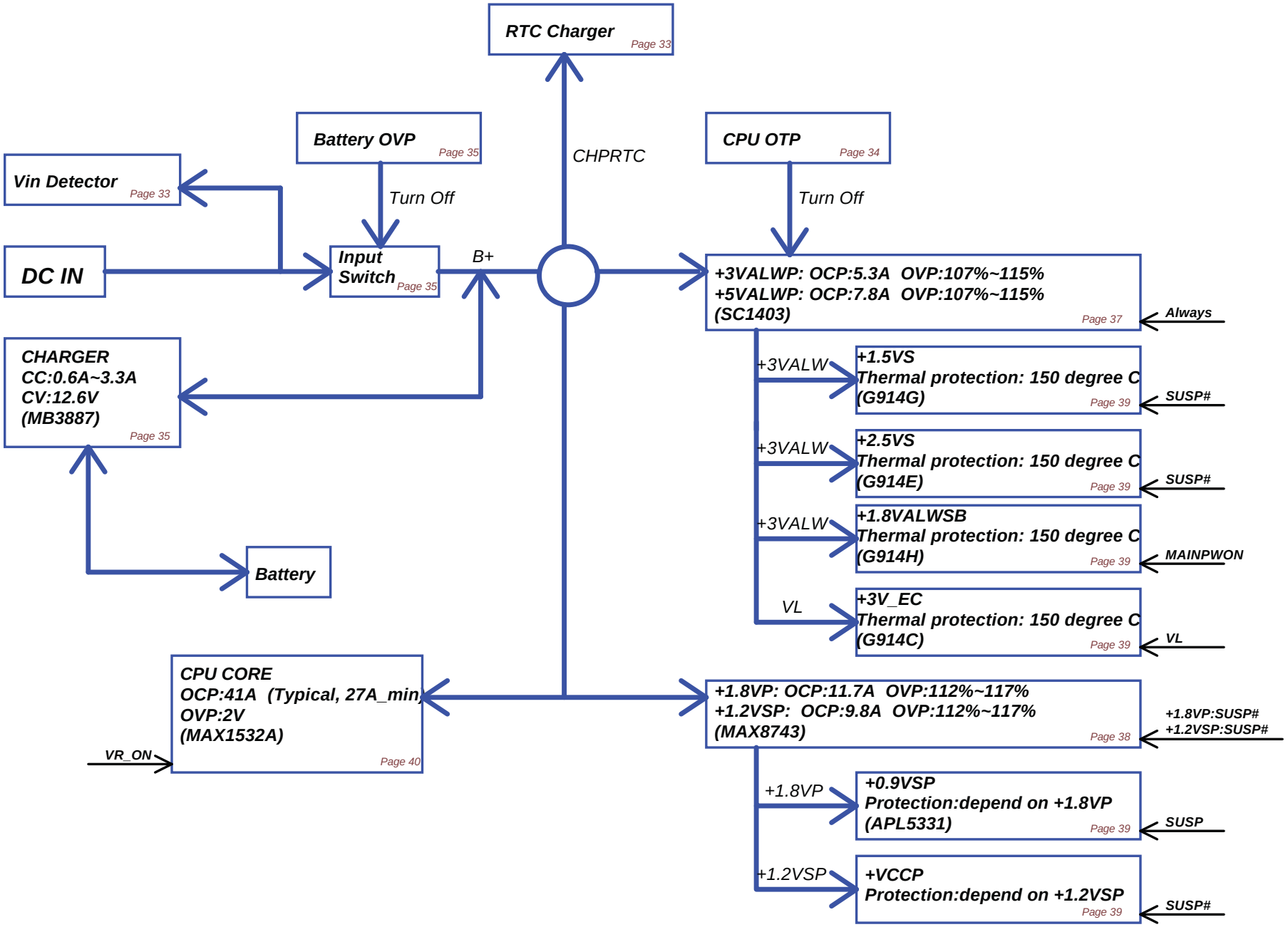
Function Table

Function	Japan			HK/CHINA	Comment
	Commercial	Consumer			
		LaVie	NEC Direct(Internet Retailing)		
TV-OUT	Yes	<—	<—	<—	
Bluetooth	No	Yes	<—	<—	Need BTO
PWR LED (Odekake)	No	<—	<—	<—	Not need Odekake
S/W	I/II Key	<—	<—	<—	all same
4 in 1 Card Adapter	No	Yes	<—	<—	
Finger Print	Yes (BTO)	No	Yes (BTO)	No	Need BTO
TPM	Yes	No	<—	<—	Need BTO
W-LAN	JP	JP	JP	Oversea	

Chip Reversion

Chip \ Phase	ES Phase	PP Phase	MP1 Phae	DR2
RS400MD	A12	A21-LF	A21-LF	
SB400	A31	A31-LF	A32-LF	
Clk Gen	B	C	C	
KB910L	A0	A1	A1	
AD1981B	A	A	A	

LC2 Power block



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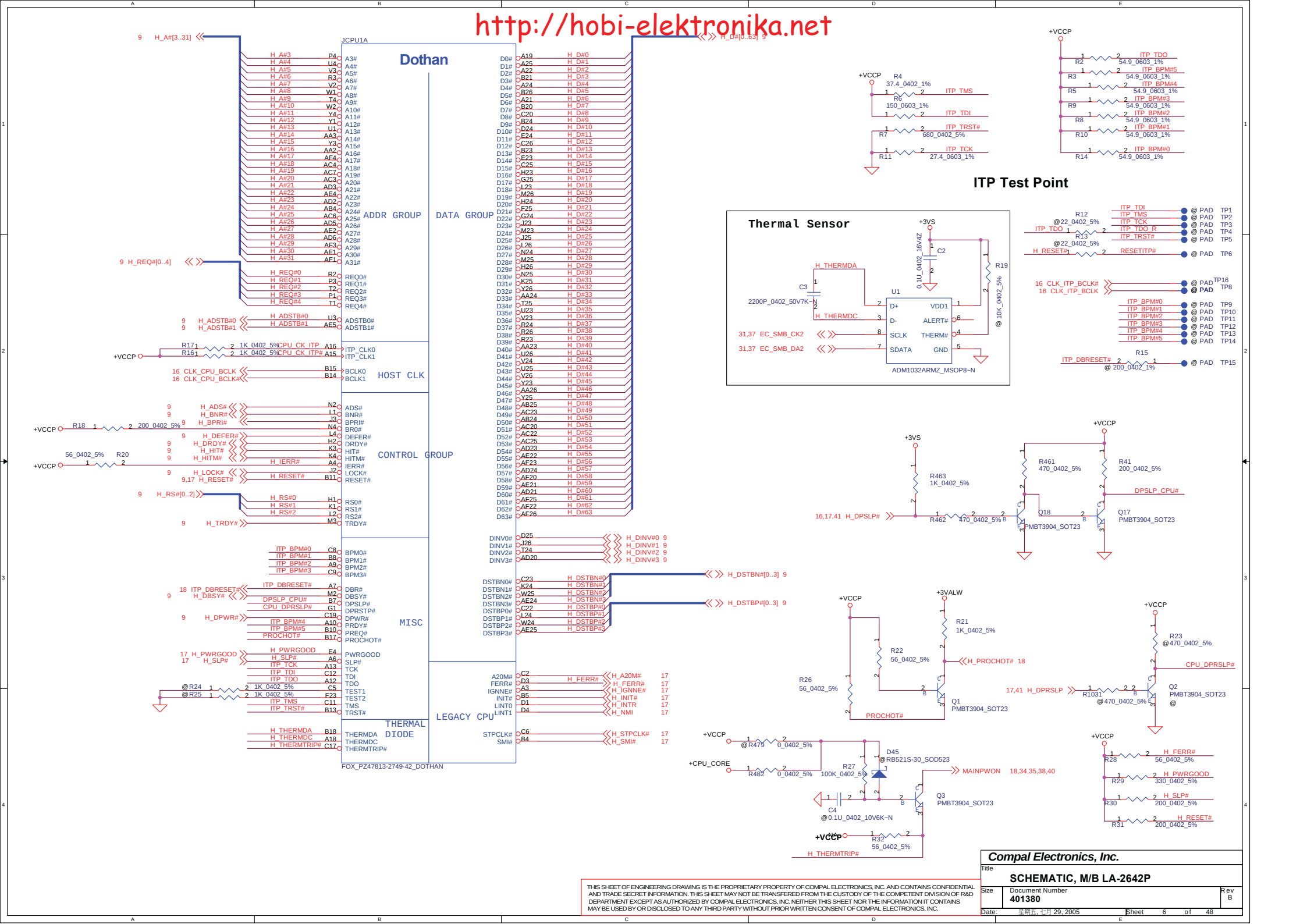

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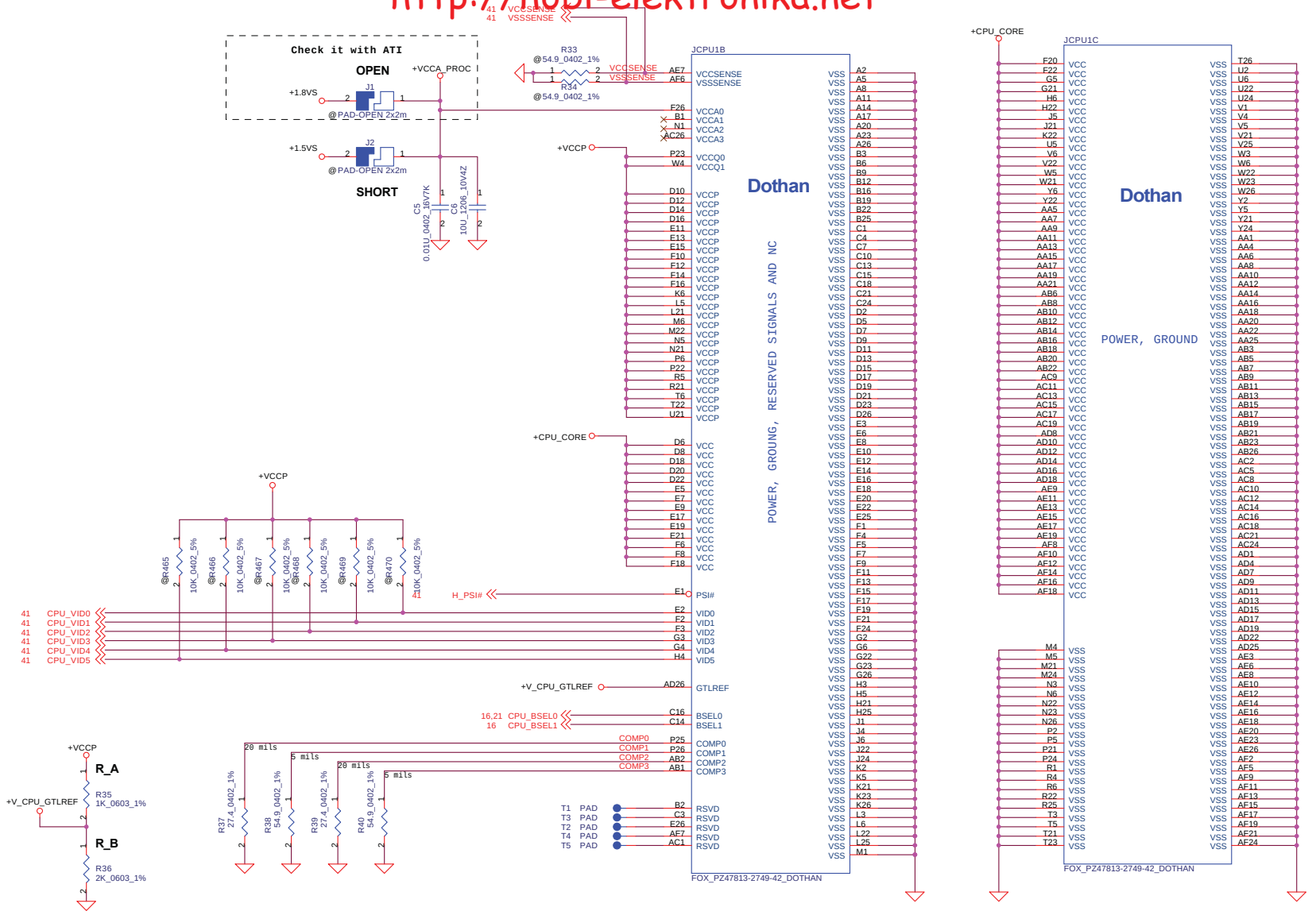

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+CPU_CORE

C7 10U_0805_6.3V6M
C8 10U_0805_6.3V6M
C9 10U_0805_6.3V6M
C10 10U_0805_6.3V6M
C11 10U_0805_6.3V6M

+CPU_CORE

C12 10U_0805_6.3V6M
C13 10U_0805_6.3V6M
C14 10U_0805_6.3V6M
C15 10U_0805_6.3V6M
C16 10U_0805_6.3V6M

+CPU_CORE

C17 10U_0805_6.3V6M
C18 10U_0805_6.3V6M
C19 10U_0805_6.3V6M
C20 10U_0805_6.3V6M
C21 10U_0805_6.3V6M

+CPU_CORE

C22 10U_0805_6.3V6M
C23 10U_0805_6.3V6M
C24 10U_0805_6.3V6M
C25 10U_0805_6.3V6M
C26 10U_0805_6.3V6M

+CPU_CORE

C32 10U_0805_6.3V6M
C33 10U_0805_6.3V6M
C30 10U_0805_6.3V6M
C34 10U_0805_6.3V6M
C35 10U_0805_6.3V6M

+CPU_CORE

C36 10U_0805_6.3V6M
C27 10U_0805_6.3V6M
C28 10U_0805_6.3V6M
C37 10U_0805_6.3V6M
C38 10U_0805_6.3V6M

+CPU_CORE

C41 10U_0805_6.3V6M
C42 10U_0805_6.3V6M
C43 10U_0805_6.3V6M
C44 10U_0805_6.3V6M
C45 10U_0805_6.3V6M

10uF 0805 X5R

High Frequence Decoupling

ESR <= 3m ohm
Capacitor > 880 uF

Near VCORE regulator.

+CPU_CORE

C39 330U_D2E_2.5VM_R9
C40 330U_D2E_2.5VM_R9
C29 @ 330U_D2E_2.5VM_R9
C31 @ 330U_D2E_2.5VM_R9

+VCCP

C46 150U_D2_6.3VM
C47 0.1U_0402_10V6K~N
C48 0.1U_0402_10V6K~N
C49 0.1U_0402_10V6K~N
C50 0.1U_0402_10V6K~N
C51 0.1U_0402_10V6K~N
C52 0.1U_0402_10V6K~N
C53 0.1U_0402_10V6K~N
C54 0.1U_0402_10V6K~N
C55 0.1U_0402_10V6K~N
C56 0.1U_0402_10V6K~N

FAN CONN. 1

+5VS
+5VS_FAN
F2 1.1A_6VDC_FUSE
R68 1K_0402_5%
SI3443DV_TSOP6
Q56 2N7002_SOT23
Q52
C57 0.1U_0402_16V4Z
U2A LM358AMX-NOPB_SO8~N
31 EN_FAN1
R43 100K_0402_5%
ENFAN1
C59 0.1U_0402_16V4Z
C909 2200P_0402_50V7K~N
R44 100K_0402_5%
FAN1
U2B LM358AMX-NOPB_SO8~N
R42 150K_0402_5%
D2 RB751V_SOD323
@C911
C60 1000P_0402_50V7K~N
22U_1206_10V4Z
JP2 MOLEX_53398-0371~N
+3VS
R45 10K_0402_5%
31 FAN1_SPEED
C910 0.01U_0402_16V7K

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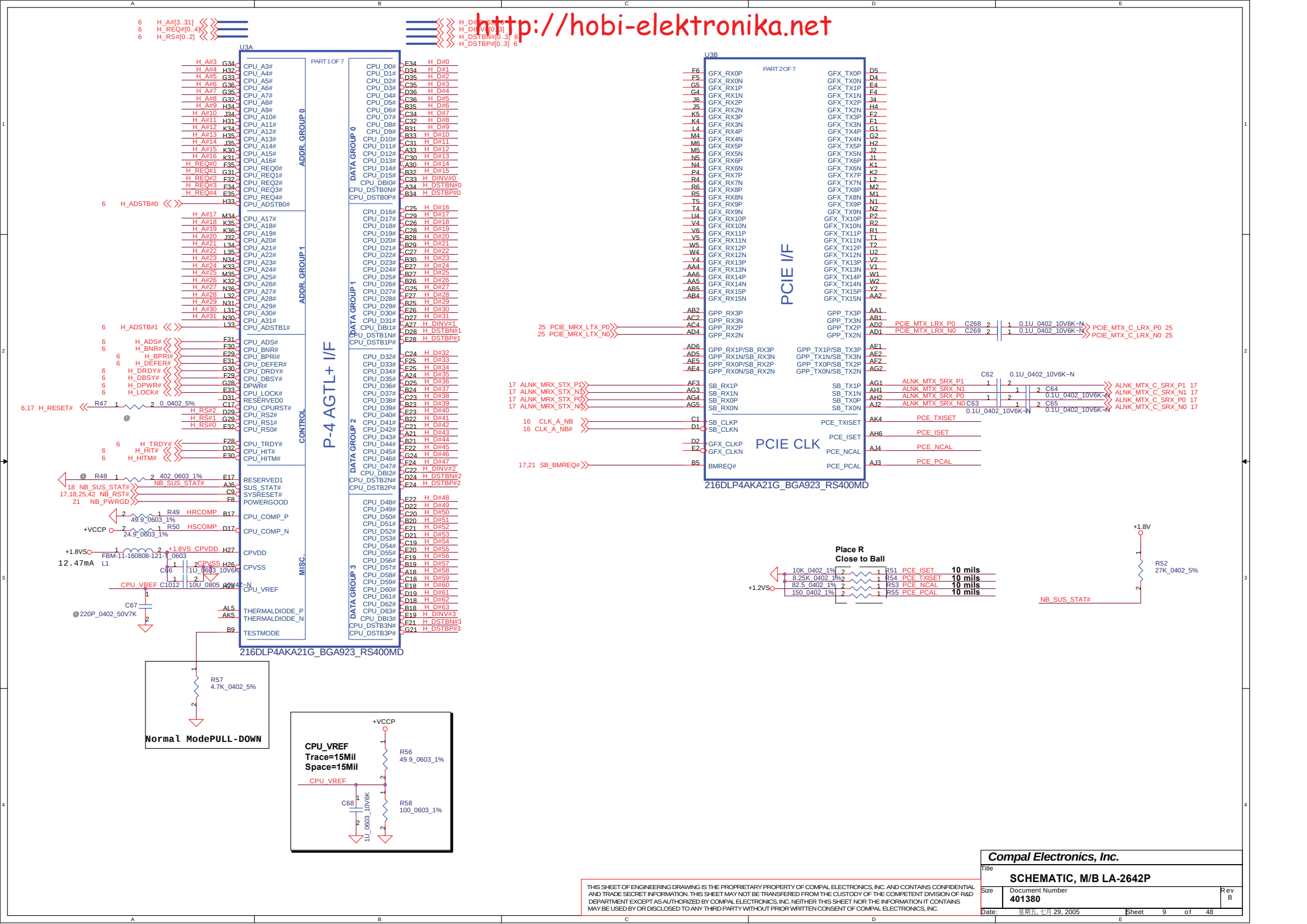

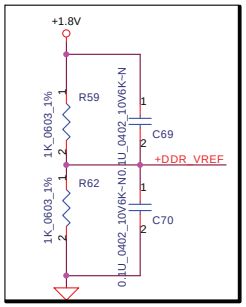

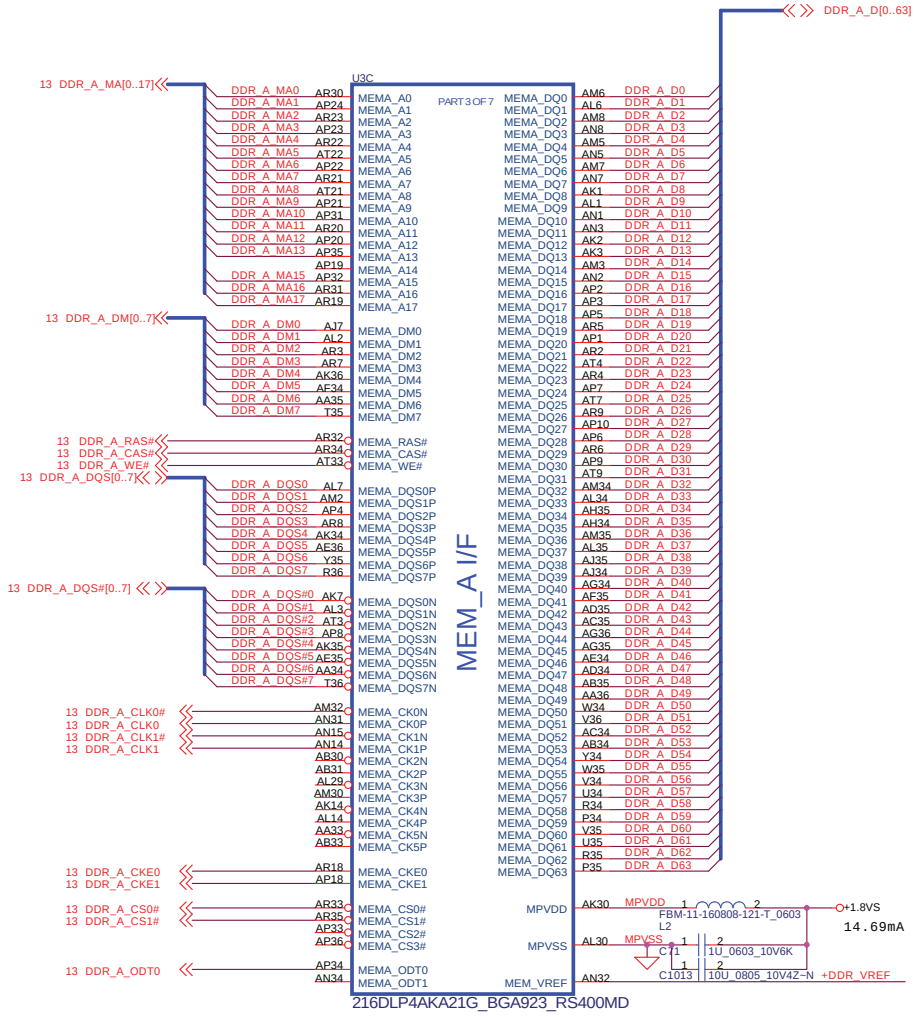

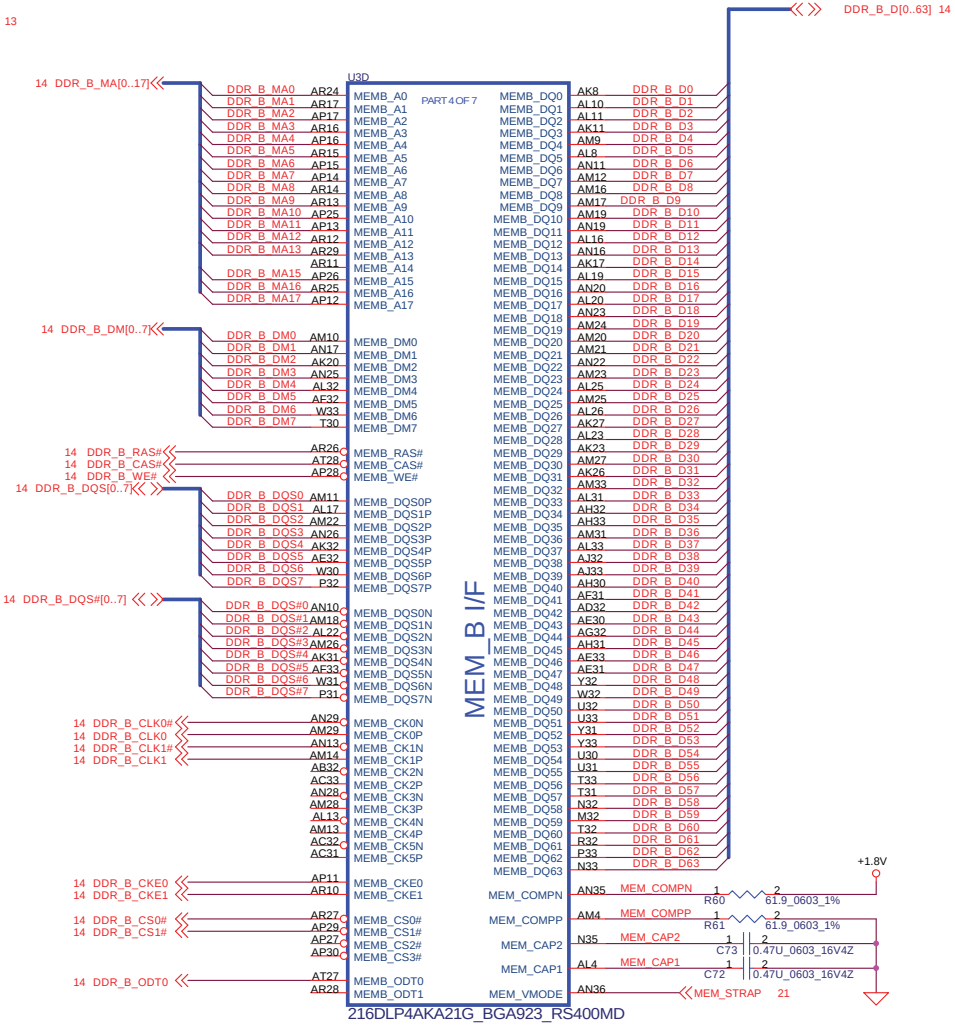

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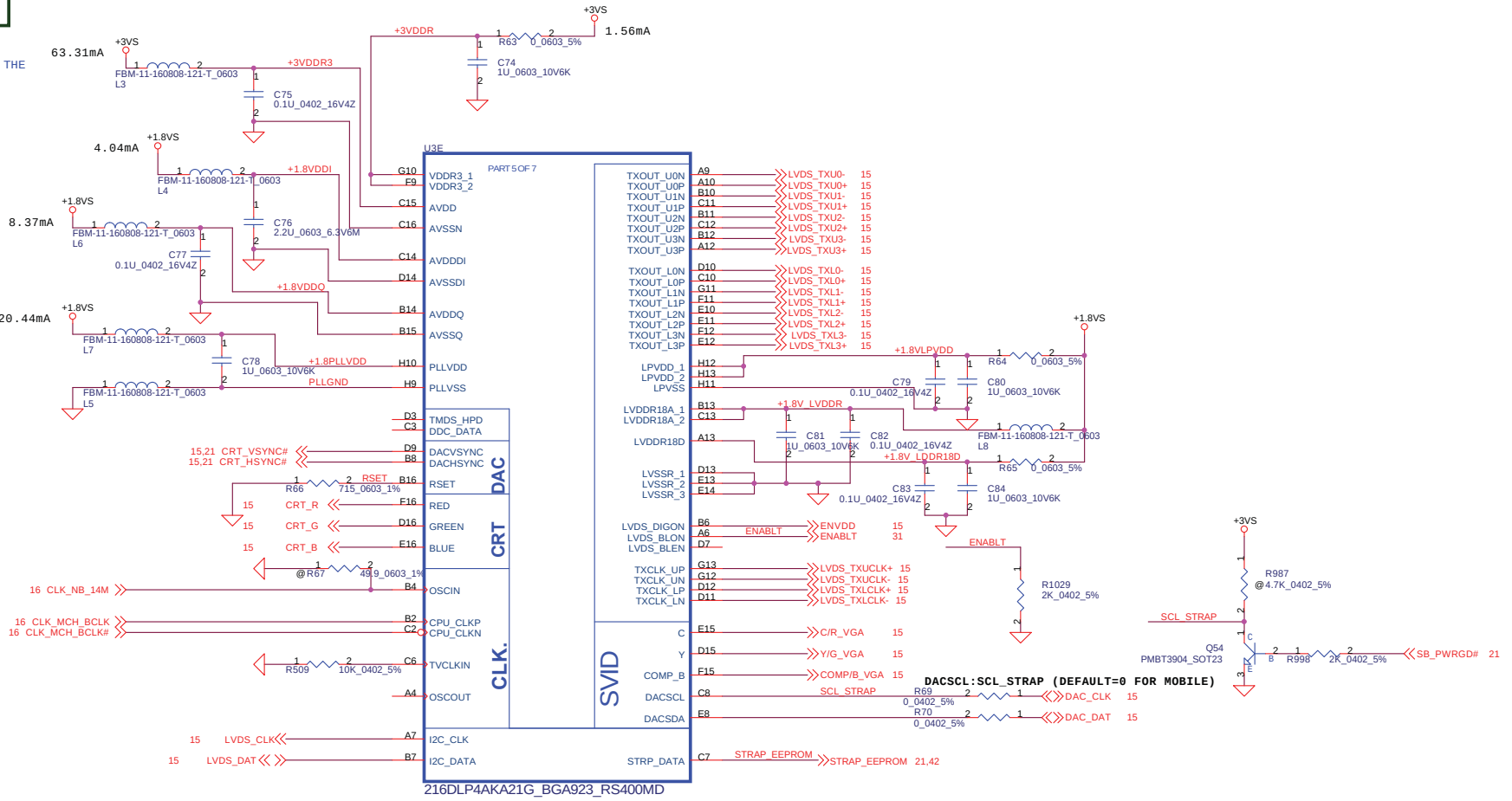
AVDD	DAC VDD (2.5V/3.3V)
AVDDDI	DIGITAL VDD (1.8V)
AVDDQ	DAC2 BANDGAP REF (1.8V)
PLLVDD	PLL VDD (1.8V)

PUT AVDD, AVDDDI, AVDDQ, PLVDD DECOUPLING CAPS ON THE BOTTOM, CLOSE TO BALLS



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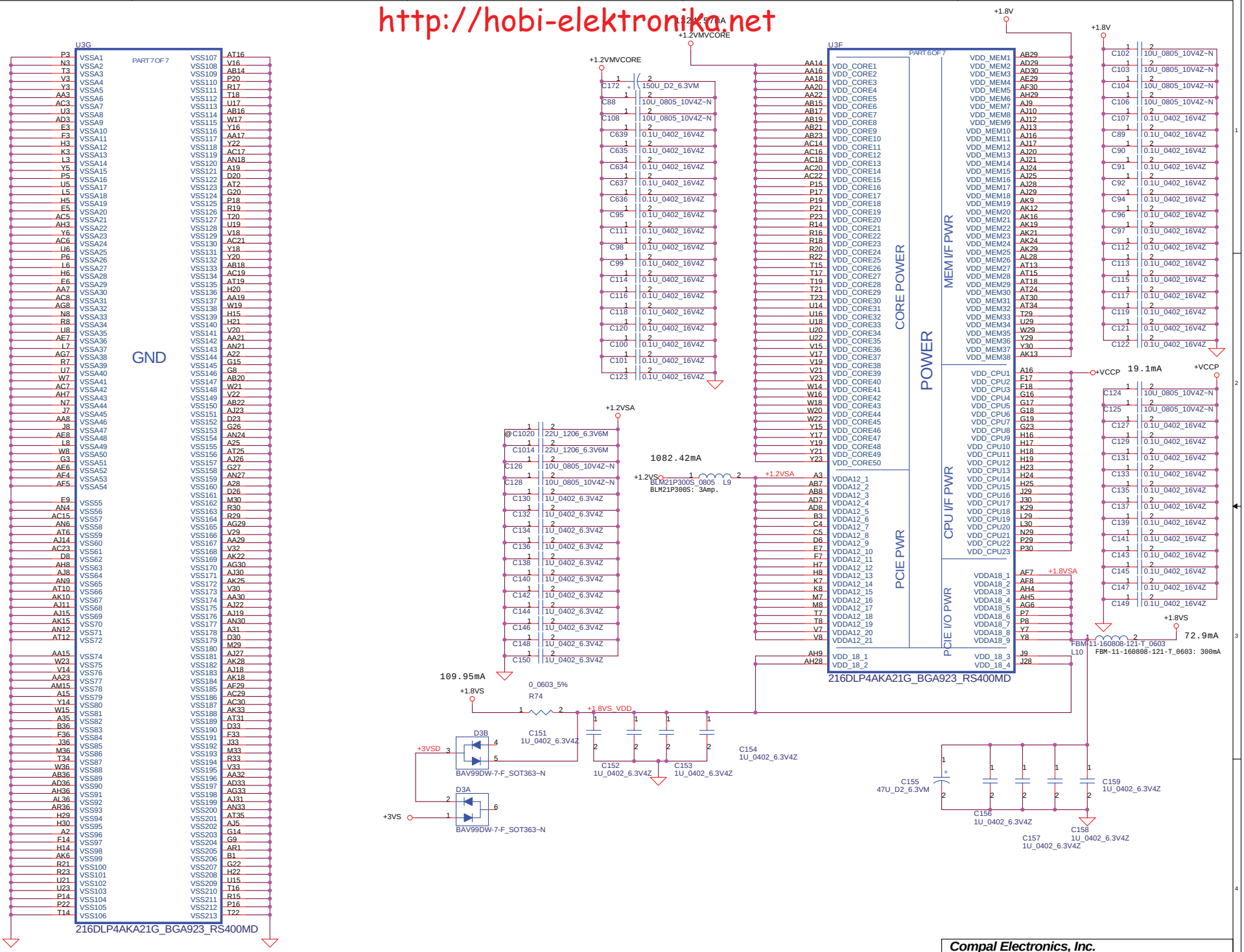

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10 DDR_A_DQS#[0..7]
10 DDR_A_D[0..63]
10 DDR_A_DM[0..7]
10 DDR_A_MA[0..13]
10 DDR_A_DQS[0..7]

Layout Note:
Place near JDIM1

+1.8V

C170 470U_D2_2.5VM

0.1U_0402_16V4Z: C162, C163, C164, C168, C169, C173, C174, C167, C629

DDR_A_CLK0 — C165 (10P_0402_50V8J) — DDR_A_CLK0#
DDR_A_CLK1 — C166 (10P_0402_50V8J) — DDR_A_CLK1#

Layout Note:
Place one cap close to every 2 pullup resistors terminated to V_DDR_MCH_REF

+0.9VS

0.1U_0402_16V4Z: C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C188

+0.9VS

RP1: DDR_A_MA5, DDR_A_MA8 — DDR_A_MA17, DDR_A_CKE0
RP2: DDR_A_MA1, DDR_A_MA3 — DDR_A_MA7, DDR_A_MA6
RP3: DDR_A_RAS#, DDR_A_CS0# — DDR_A_MA9, DDR_A_MA12
RP4: DDR_A_MA15, DDR_A_MA10 — DDR_A_MA4, DDR_A_MA2
RP5: DDR_A_CAS#, DDR_A_WE# — DDR_A_MA0, DDR_A_MA16
RP6: DDR_A_ODT0, DDR_A_MA13
RP7: DDR_A_CS1# — DDR_A_CKE1, DDR_A_MA11

56_0404_4P2R_5%

Layout Note:
Place these resistor closely JDIM2,all trace length<750 mil

Layout Note:
Place these resistor closely JDIM2,all trace length Max=1.3"

Trace=20mil

+1.8V, +1.8V
V_DDR_MCH_REF — V_DDR_MCH_REF 14

JDIM2 — FOX_ASOA426-M2R-TR

	VREF	1	2	VSS	
DDR_A_D8	VSS	3	4	DQ4	DDR_A_D12
DDR_A_D13	DQ0	5	6	DQ5	DDR_A_D9
	DQ1	7	8	VSS	
	VSS	9	10	DM0	DDR_A_DM1
DDR_A_DQS#1	DQS0#	11	12	VSS	
DDR_A_DQS1	DQS0	13	14	DQ6	DDR_A_D15
	VSS	15	16	DQ7	DDR_A_D11
DDR_A_D10	DQ2	17	18	VSS	
DDR_A_D14	DQ3	19	20	DQ12	DDR_A_D17
	VSS	21	22	DQ13	DDR_A_D21
DDR_A_D20	DQ8	23	24	VSS	
DDR_A_D16	DQ9	25	26	DM1	DDR_A_DM2
	VSS	27	28	VSS	
DDR_A_DQS#2	DQS1#	29	30	CK0	DDR_A_CLK1
DDR_A_DQS2	DQS1	31	32	CK0#	DDR_A_CLK1# — DDR_A_CLK1 10, DDR_A_CLK1# 10
	VSS	33	34	VSS	
DDR_A_D23	DQ10	35	36	DQ14	DDR_A_D18
DDR_A_D22	DQ11	37	38	DQ15	DDR_A_D19
	VSS	39	40	VSS	
		41	42		
DDR_A_D1	VSS	43	44	VSS	
DDR_A_D4	DQ16	45	46	DQ20	DDR_A_D5
	DQ17	47	48	DQ21	DDR_A_D0
DDR_A_DQS#0	VSS	49	50	VSS	
DDR_A_DQS0	DQS2#	51	52	NC	
	DQS2	53	54	DM2	DDR_A_DM0
DDR_A_D6	VSS	55	56	VSS	
DDR_A_D2	DQ18	57	58	DQ22	DDR_A_D7
	DQ19	59	60	DQ23	DDR_A_D3
DDR_A_D29	VSS	61	62	VSS	
DDR_A_D28	DQ24	63	64	DQ28	DDR_A_D24
	DQ25	65	66	DQ29	DDR_A_D25
DDR_A_DM3	VSS	67	68	VSS	
	DM3	69	70	DQS3#	DDR_A_DQS#3
	NC	71	72	DQS3	DDR_A_DQS3
	VSS	73	74	VSS	
DDR_A_D30	DQ26	75	76	DQ30	DDR_A_D31
DDR_A_D26	DQ27	77	78	DQ31	DDR_A_D27
	VSS	79	80	VSS	
DDR_A_CKE0	CKE0	81	82	NC/CKE1	DDR_A_CKE1 — DDR_A_CKE1 10
10 DDR_A_CKE0	VDD	83	84	VDD	
	NC	85	86	NC/A15	
10 DDR_A_MA14	BA2	87	88	NC/A14	
	VDD	89	90	VDD	
DDR_A_MA12	A12	91	92	A11	DDR_A_MA11
DDR_A_MA9	A9	93	94	A7	DDR_A_MA7
DDR_A_MA8	A8	95	96	A6	DDR_A_MA6
	VDD	97	98	VDD	
DDR_A_MA5	A5	99	100	A4	DDR_A_MA4
DDR_A_MA3	A3	101	102	A2	DDR_A_MA2
DDR_A_MA1	A1	103	104	A0	DDR_A_MA0
	VDD	105	106	VDD	
DDR_A_MA10	A10/AP	107	108	BA1	DDR_A_MA16 — DDR_A_MA16 10
10 DDR_A_MA15	BA0	109	110	RAS#	DDR_A_RAS# — DDR_A_RAS# 10
10 DDR_A_WE#	WE#	111	112	S0#	DDR_A_CS0# — DDR_A_CS0# 10
	VDD	113	114	VDD	
10 DDR_A_CAS#	CAS#	115	116	ODT0	DDR_A_ODT0 — DDR_A_ODT0 10
10 DDR_A_CS1#	NC/S1#	117	118	NC/A13	DDR_A_MA13
	VDD	119	120	VDD	
DDR_A_ODT1	NC/ODT1	121	122	NC	
	VSS	123	124	VSS	
DDR_A_D32	DQ32	125	126	DQ36	DDR_A_D36
DDR_A_D33	DQ33	127	128	DQ37	DDR_A_D37
	VSS	129	130	VSS	
DDR_A_DQS#4	DQS4#	131	132	DM4	DDR_A_DM4
DDR_A_DQS4	DQS4	133	134	VSS	
	VSS	135	136	DQ38	DDR_A_D35
DDR_A_D39	DQ34	137	138	DQ39	DDR_A_D34
DDR_A_D38	DQ35	139	140	VSS	
	VSS	141	142	DQ44	DDR_A_D45
DDR_A_D40	DQ40	143	144	DQ45	DDR_A_D41
DDR_A_D44	DQ41	145	146	VSS	
	VSS	147	148	DQS5#	DDR_A_DQS#5
DDR_A_DM5	DM5	149	150	DQS5	DDR_A_DQS5
	VSS	151	152	VSS	
DDR_A_D46	DQ42	153	154	DQ46	DDR_A_D47
DDR_A_D42	DQ43	155	156	DQ47	DDR_A_D43
	VSS	157	158	VSS	
DDR_A_D52	DQ48	159	160	DQ52	DDR_A_D53
DDR_A_D48	DQ49	161	162	DQ53	DDR_A_D49
	VSS	163	164	VSS	
	NC,TEST	165	166	CK1	DDR_A_CLK0 — DDR_A_CLK0 10
	VSS	167	168	CK1#	DDR_A_CLK0# — DDR_A_CLK0# 10
DDR_A_DQS#6	DQS6#	169	170	VSS	
DDR_A_DQS6	DQS6	171	172	DM6	DDR_A_DM6
	VSS	173	174	VSS	
DDR_A_D54	DQ50	175	176	DQ54	DDR_A_D50
DDR_A_D55	DQ51	177	178	DQ55	DDR_A_D51
	VSS	179	180	VSS	
DDR_A_D60	DQ56	181	182	DQ60	DDR_A_D61
DDR_A_D56	DQ57	183	184	DQ61	DDR_A_D57
	VSS	185	186	VSS	
DDR_A_DM7	DM7	187	188	DQS7#	DDR_A_DQS#7
	VSS	189	190	DQS7	DDR_A_DQS7
DDR_A_D62	DQ58	191	192	VSS	
DDR_A_D58	DQ59	193	194	DQ62	DDR_A_D63
	VSS	195	196	DQ63	DDR_A_D59
14,16,18,26 SB_SMDATA	SDA	197	198	VSS	
14,16,18,26 SB_SMCLK	SCL	199	200	SA0	
+3VS	VDDSPD			SA1	

R1045 0_0402_5%

+3VS
0.1U_0402_16V4Z: C190
2.2U_0805_10V6K: C189
10K_0402_5%: R75, R76

DIMMA Reverse

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Trace=20mil

10 DDR_B_DQS#[0..7]
10 DDR_B_D[0..63]
10 DDR_B_DM[0..7]
10 DDR_B_DQS[0..7]
10 DDR_B_MA[0..13]

Layout Note:
Place near JDIM2

+1.8V

C171 470U_D2_2.5VM

0.1U_0402_16V4Z: C192, C200, C193, C194, C201, C196, C197, C198, C630

DDR_B_CLK0 — @ 10P_0402_50V8J C202 — DDR_B_CLK0#

DDR_B_CLK1 — @ 10P_0402_50V8J C195 — DDR_B_CLK1#

Layout Note:
Place one cap close to every 2 pullup resistors terminated to V_DDR_MCH_REF

+0.9VS

0.1U_0402_16V4Z: C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219

+0.9VS

RP14: DDR_B_MA1, DDR_B_MA3 — DDR_B_MA9, DDR_B_MA12
RP15: DDR_B_MA9, DDR_B_MA12
RP17: DDR_B_MA15, DDR_B_MA10 — DDR_B_CKE1, DDR_B_MA11
RP16: DDR_B_CKE1, DDR_B_MA11
RP18: DDR_B_MA0, DDR_B_MA16 — DDR_B_MA5, DDR_B_MA8
RP19: DDR_B_MA5, DDR_B_MA8
RP20: DDR_B_RAS#, DDR_B_CS0# — DDR_B_MA7, DDR_B_MA6
RP21: DDR_B_MA7, DDR_B_MA6
RP22: DDR_B_MA4, DDR_B_MA2 — DDR_B_ODT0, DDR_B_MA13
RP23: DDR_B_ODT0, DDR_B_MA13
RP24: DDR_B_CAS#, DDR_B_WE#
RP25: DDR_B_CS1# — DDR_B_MA17, DDR_B_CKE0
RP26: DDR_B_MA17, DDR_B_CKE0

All: 56_0404_4P2R_5%

Layout Note:
Place these resistor closely JDIM1,all trace length<750 mil

Layout Note:
Place these resistor closely JDIM1,all trace length Max=1.3"

JDIM1 — TYCO_1720800-2

+1.8V

V_DDR_MCH_REF 13

R473 1K_0402_5% — C902 0.1U_0402_16V4Z
R474 1K_0402_5% — C903 0.1U_0402_16V4Z

DDR_B_D0, DDR_B_D5, DDR_B_DQS#0, DDR_B_DQS0, DDR_B_D2, DDR_B_D6, DDR_B_D12, DDR_B_D8, DDR_B_DQS#1, DDR_B_DQS1, DDR_B_D14, DDR_B_D15, DDR_B_D17, DDR_B_D20, DDR_B_DQS#2, DDR_B_DQS2, DDR_B_D22, DDR_B_D23, DDR_B_D28, DDR_B_D29, DDR_B_DM3, DDR_B_D26, DDR_B_D30, DDR_B_CKE0, DDR_B_MA17, DDR_B_MA12, DDR_B_MA9, DDR_B_MA8, DDR_B_MA5, DDR_B_MA3, DDR_B_MA1, DDR_B_MA10, DDR_B_MA15, DDR_B_WE#, DDR_B_CAS#, DDR_B_CS1#, DDR_B_ODT1, DDR_B_D36, DDR_B_D38, DDR_B_DQS#4, DDR_B_DQS4, DDR_B_D32, DDR_B_D35, DDR_B_D41, DDR_B_D45, DDR_B_DM5, DDR_B_D47, DDR_B_D46, DDR_B_D54, DDR_B_D52, DDR_B_DQS#6, DDR_B_DQS6, DDR_B_D55, DDR_B_D49, DDR_B_D57, DDR_B_D60, DDR_B_DM7, DDR_B_D62, DDR_B_D58

10 DDR_B_CKE0
10 DDR_B_MA17
10 DDR_B_MA15
10 DDR_B_WE#
10 DDR_B_CAS#
10 DDR_B_CS1#

R1046 0_0402_5%

13,16,18,26 SB_SMDATA
13,16,18,26 SB_SMCLK
+3VS

C220 0.1U_0402_16V4Z
C221 2.2U_0805_10V6K

DDR_B_D1, DDR_B_D4, DDR_B_DM0, DDR_B_D7, DDR_B_D3, DDR_B_D9, DDR_B_D13, DDR_B_DM1, DDR_B_CLK1, DDR_B_CLK1#, DDR_B_D10, DDR_B_D11, DDR_B_D21, DDR_B_D16, DDR_B_DM2, DDR_B_D18, DDR_B_D19, DDR_B_D25, DDR_B_D24, DDR_B_DQS#3, DDR_B_DQS3, DDR_B_D31, DDR_B_D27, DDR_B_CKE1, DDR_B_MA11, DDR_B_MA7, DDR_B_MA6, DDR_B_MA4, DDR_B_MA2, DDR_B_MA0, DDR_B_MA16, DDR_B_RAS#, DDR_B_CS0#, DDR_B_ODT0, DDR_B_MA13, DDR_B_D33, DDR_B_D34, DDR_B_DM4, DDR_B_D37, DDR_B_D39, DDR_B_D40, DDR_B_D44, DDR_B_DQS#5, DDR_B_DQS5, DDR_B_D42, DDR_B_D43, DDR_B_D48, DDR_B_D53, DDR_B_CLK0, DDR_B_CLK0#, DDR_B_DM6, DDR_B_D50, DDR_B_D51, DDR_B_D61, DDR_B_D56, DDR_B_DQS#7, DDR_B_DQS7, DDR_B_D63, DDR_B_D59

DDR_B_CLK1 10
DDR_B_CLK1# 10
DDR_B_CKE1 10
DDR_B_MA16 10
DDR_B_RAS# 10
DDR_B_CS0# 10
DDR_B_ODT0 10
DDR_B_CLK0 10
DDR_B_CLK0# 10

R78 10K_0402_5%
R77 10K_0402_5%

DIMMB Standar

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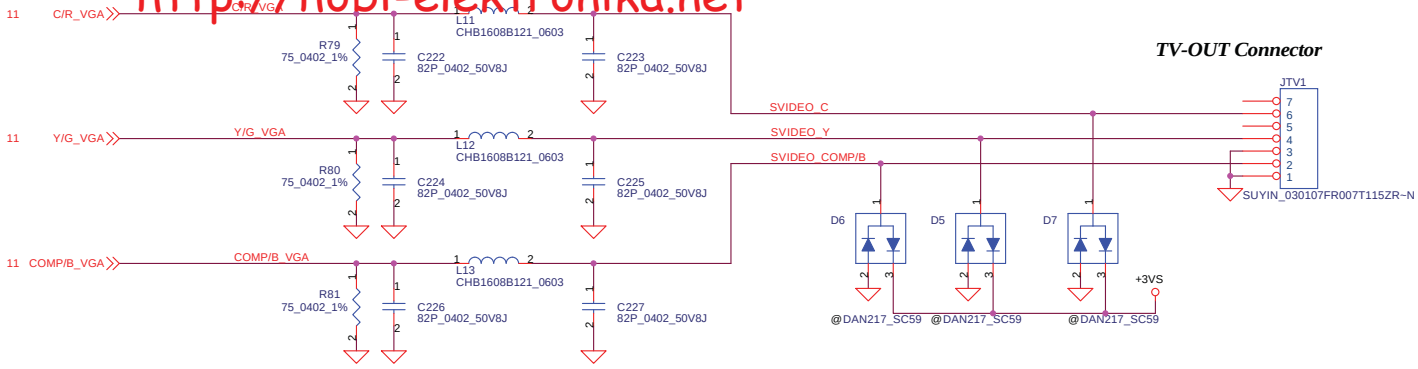
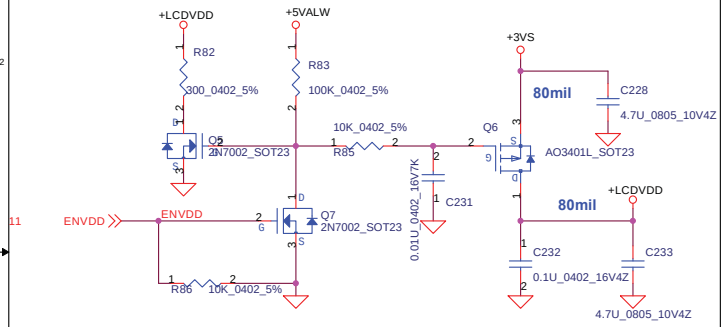
TV-OUT Connector



PANEL +LCDVDD CTRL CKT



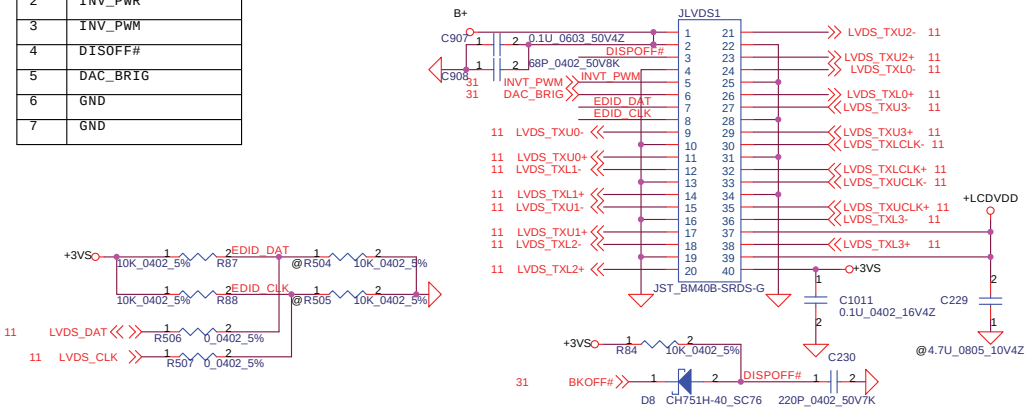
W to B Pin Define

B+	1	2	B+
DISPOFF#	3	4	GND
INVT_PWM	5	6	DAC_BRIG
EDID_DAT	7	8	EDID_CLK
UTX0-	9	10	GND
UTX0+	11	12	LTX1-
GND	13	14	LTX1+
UTX1-	15	16	GND
UTX1+	17	18	LTX2-
GND	19	20	LTX2+
UTX2-	21	22	GND
UTX2+	23	24	LTX0-
GND	25	26	LTX0+
UTX3-	27	28	GND
UTX3+	29	30	LCLK-
GND	31	32	LCLK+
UCLK-	33	34	GND
UCLK+	35	36	LTX3-
LCDVDD	37	38	LTX3+
LCDVDD	39	40	+3VS

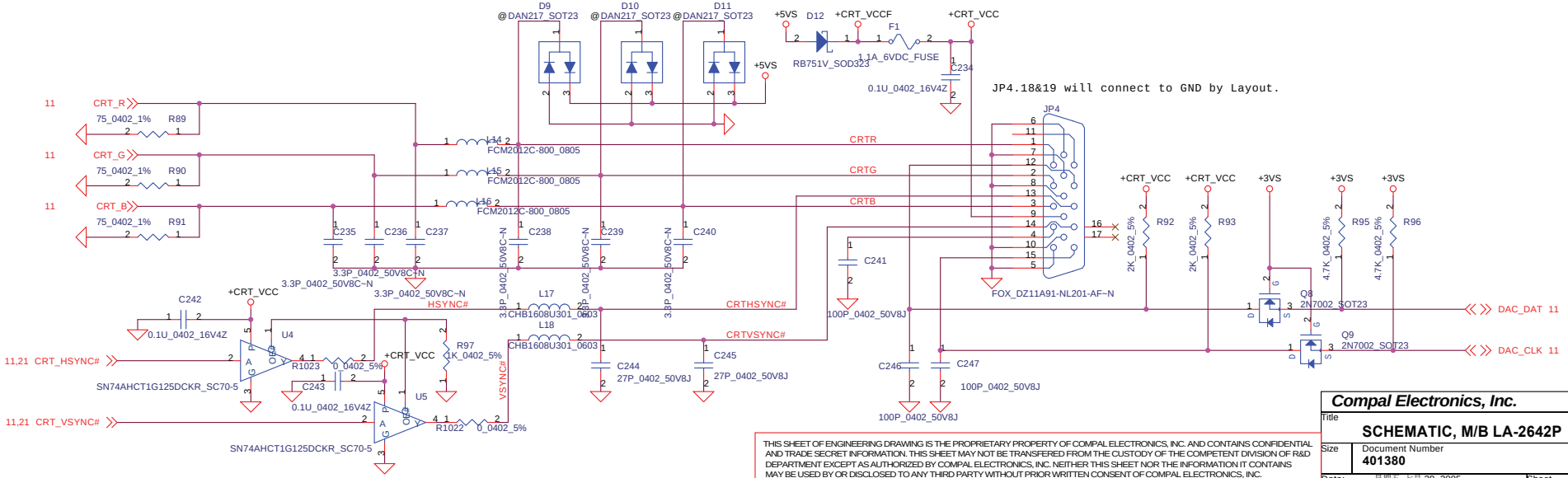
Inverter Pin Define

1	INV_PWR
2	INV_PWR
3	INV_PWM
4	DISOFF#
5	DAC_BRIG
6	GND
7	GND

LVDS from NB



CRT CONNECTOR



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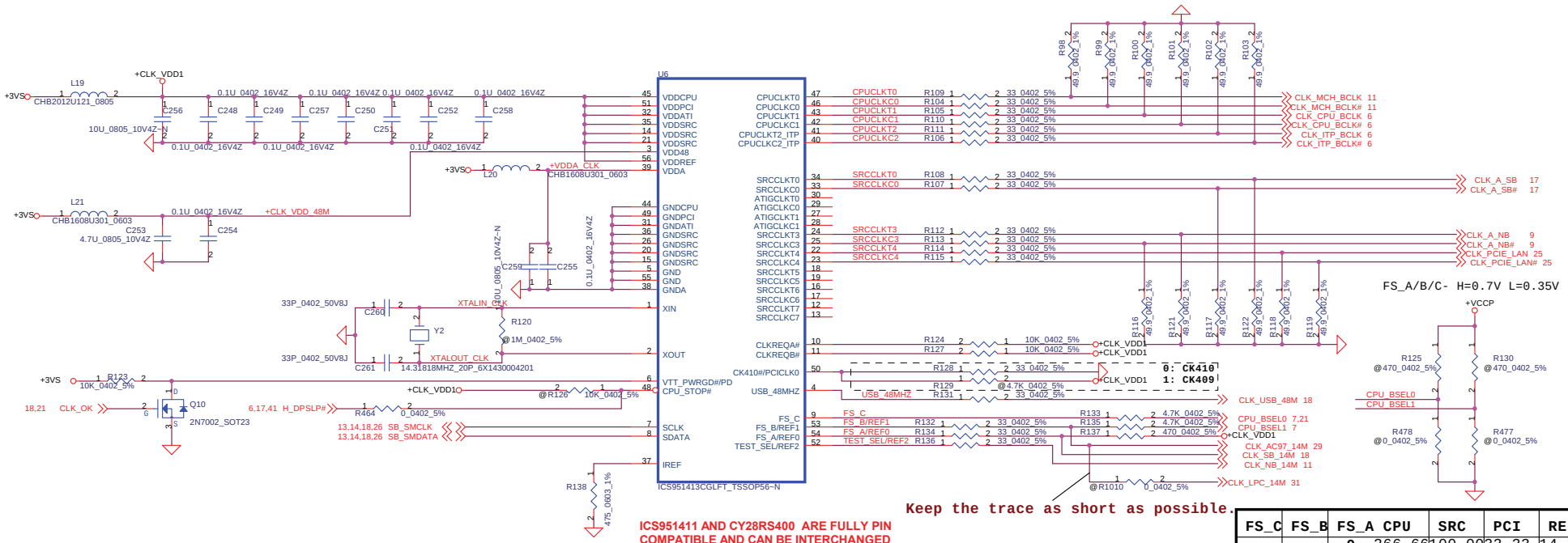
Clock Generator



ICS951411 AND CY28RS400 ARE FULLY PIN COMPATIBLE AND CAN BE INTERCHANGED WITHOUT ANY HARDWARE MODIFICATION.

Internal Pull-low 120k: pin48
Internal Pull-up 120k: pin 52, 53 and 54.

FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
0	0	0	266.66	100.00	33.33	14.318	48.000
		1	133.33	100.00	33.33	14.318	48.000
	1	0	200.00	100.00	33.33	14.318	48.000
		1	166.66	100.00	33.33	14.318	48.000
1	0	1	100.00	100.00	33.33	14.318	48.000
	1	0	400.00	100.00	33.33	14.318	48.000
		1	RESERVED			14.318	48.000

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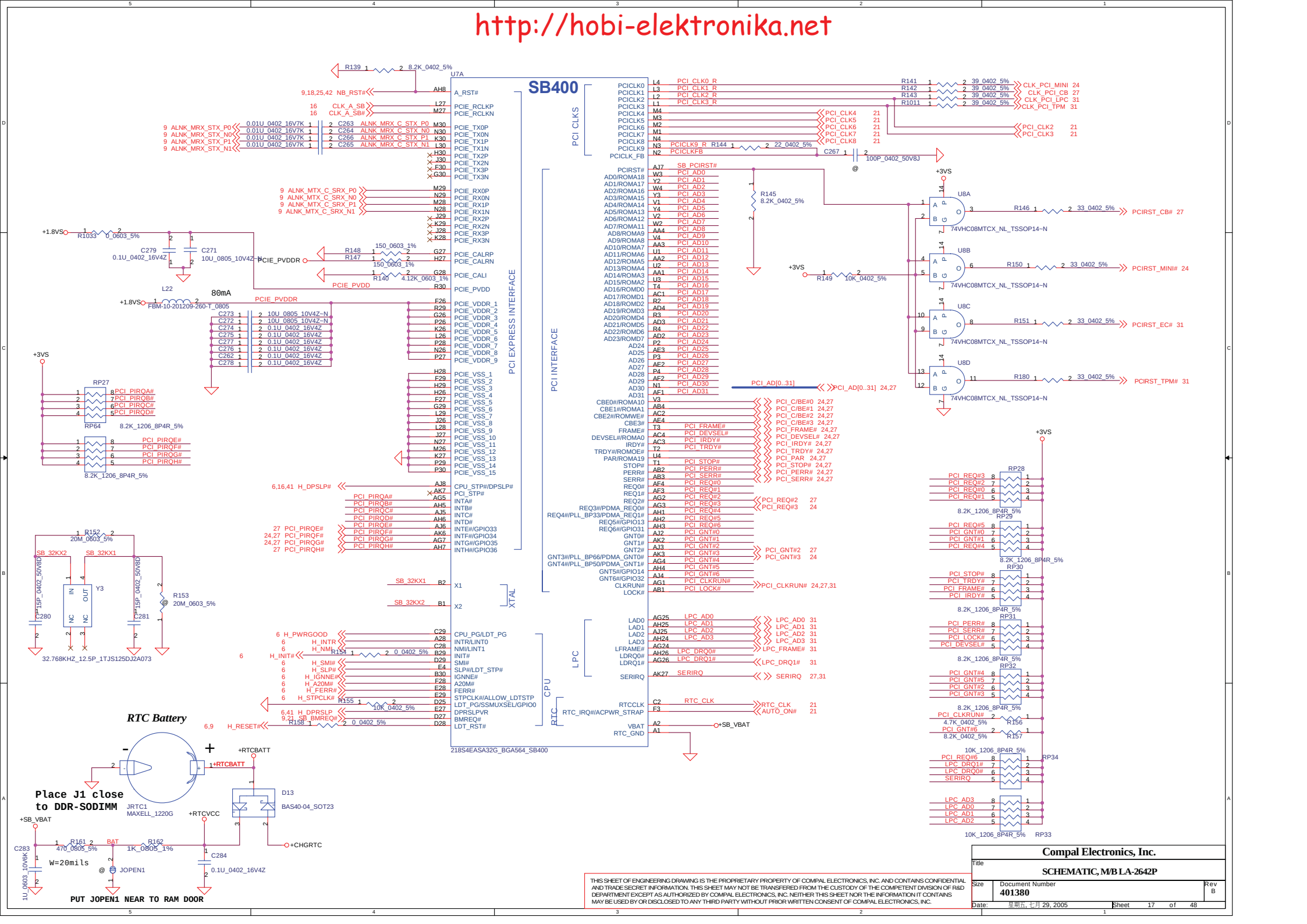

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Title	SCHEMATIC, M/B LA-2642P
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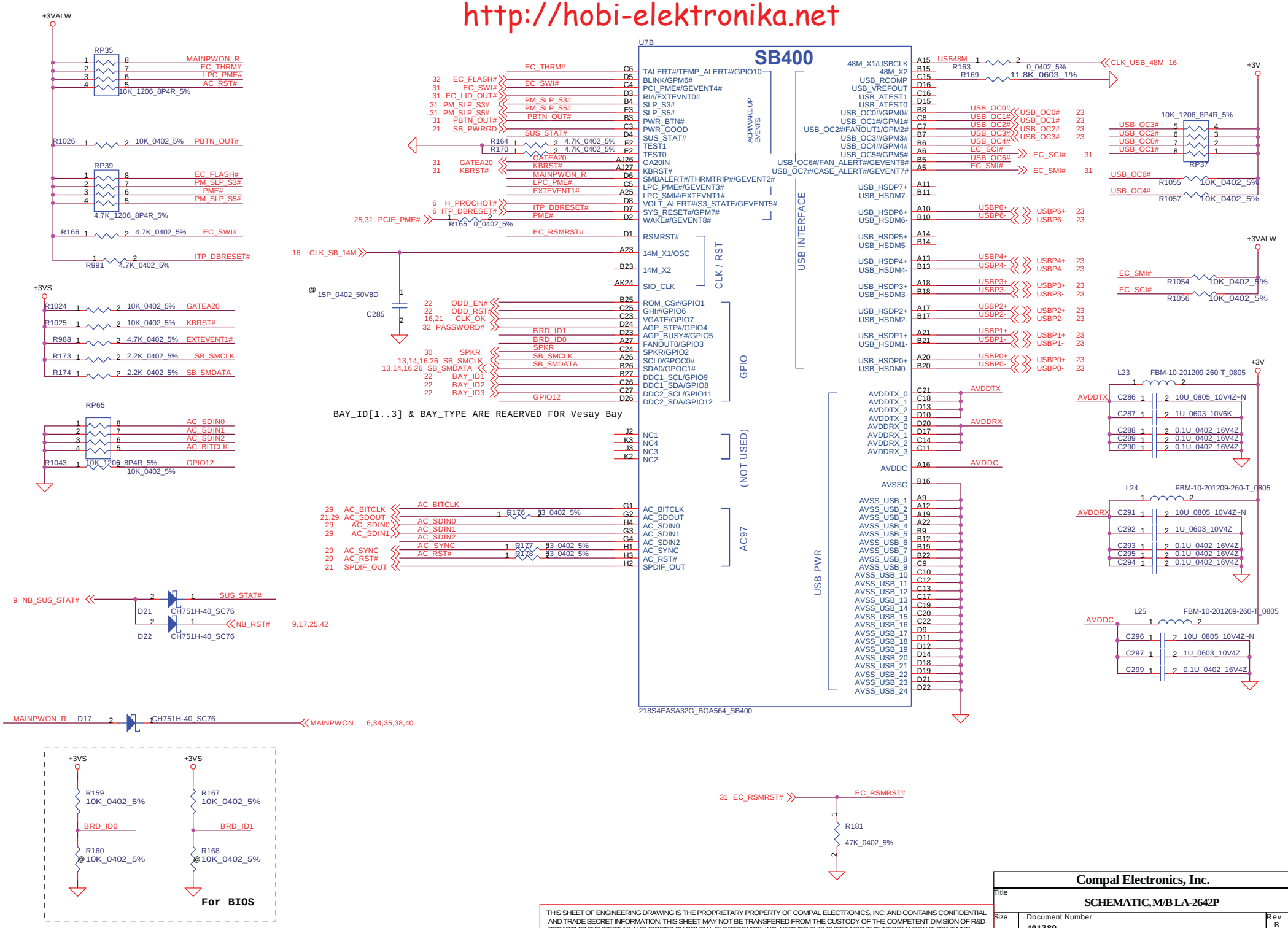

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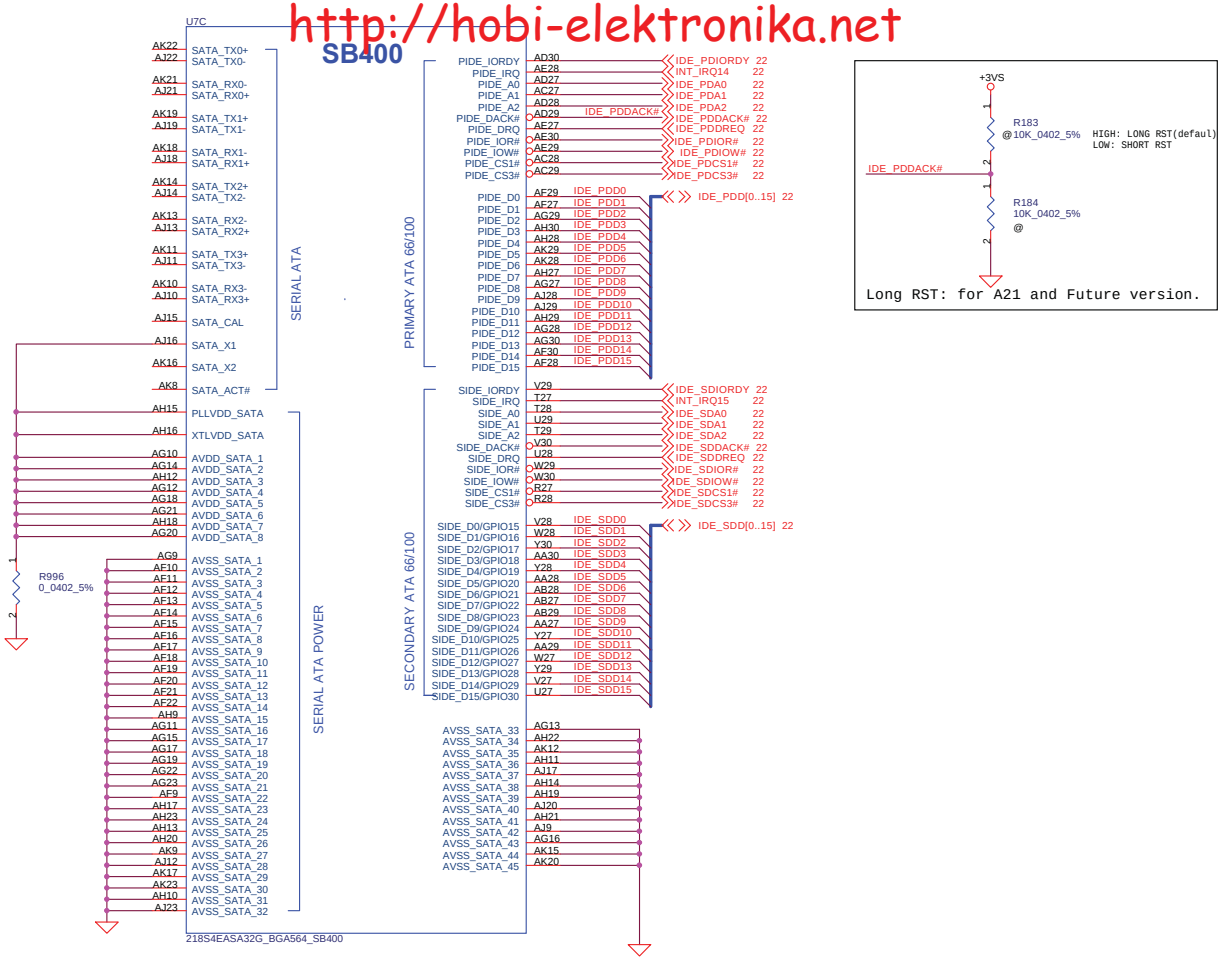

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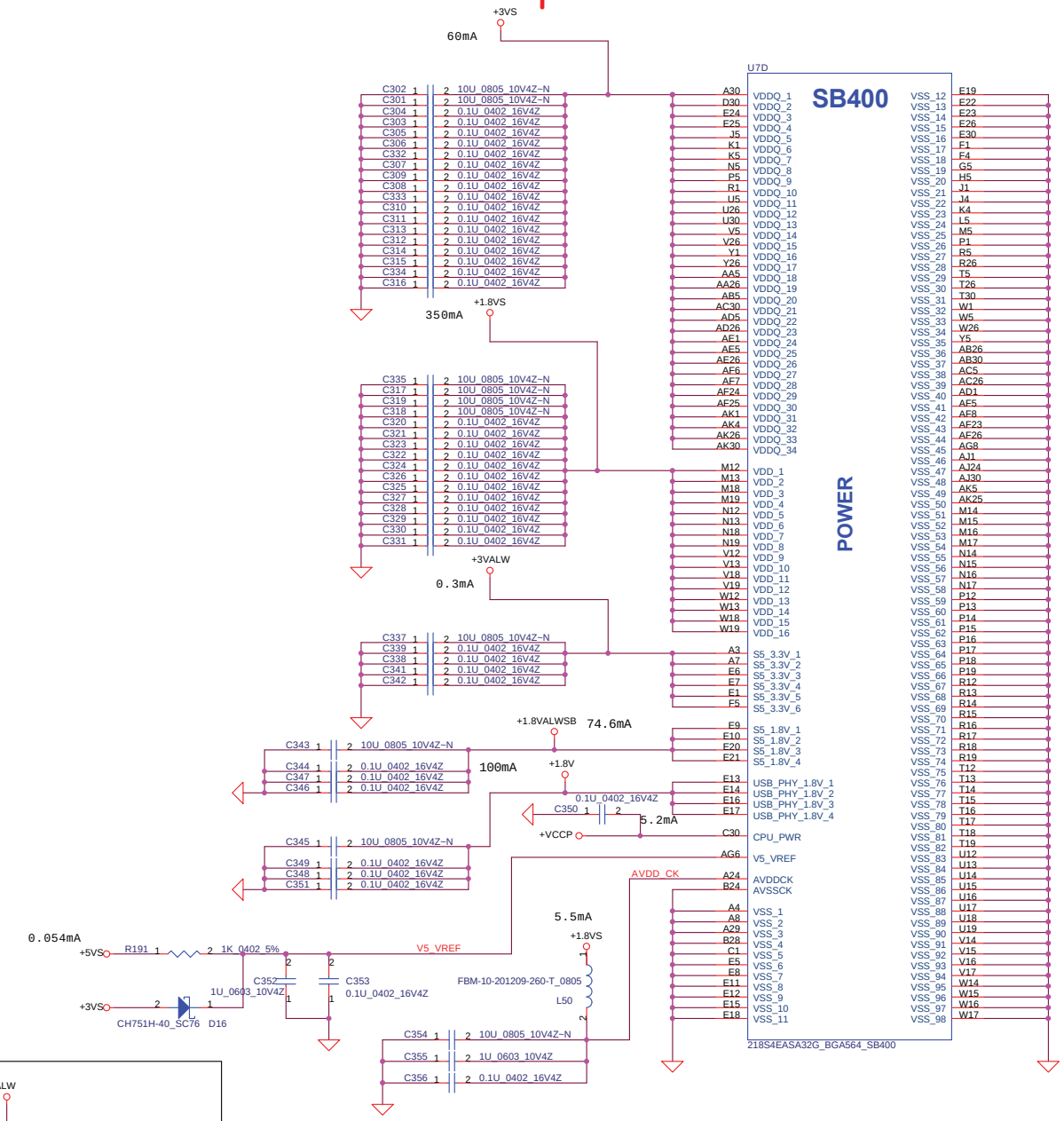

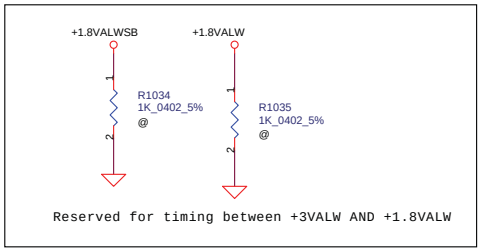

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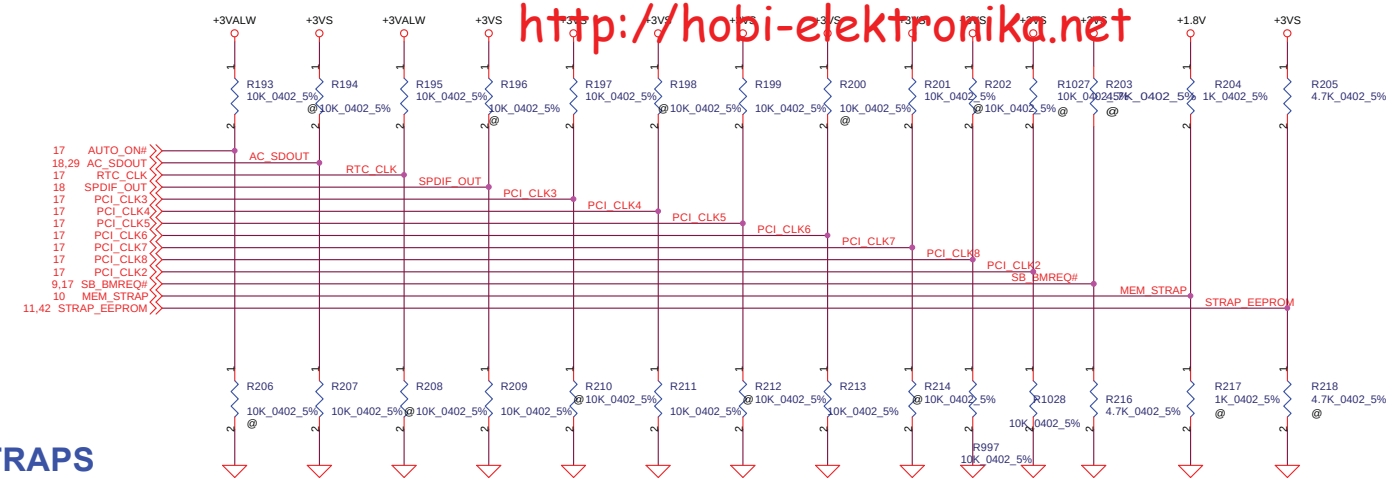
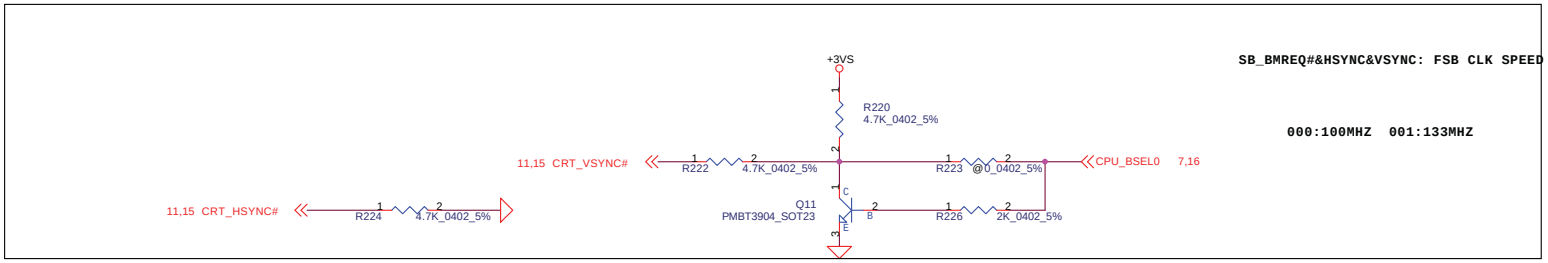
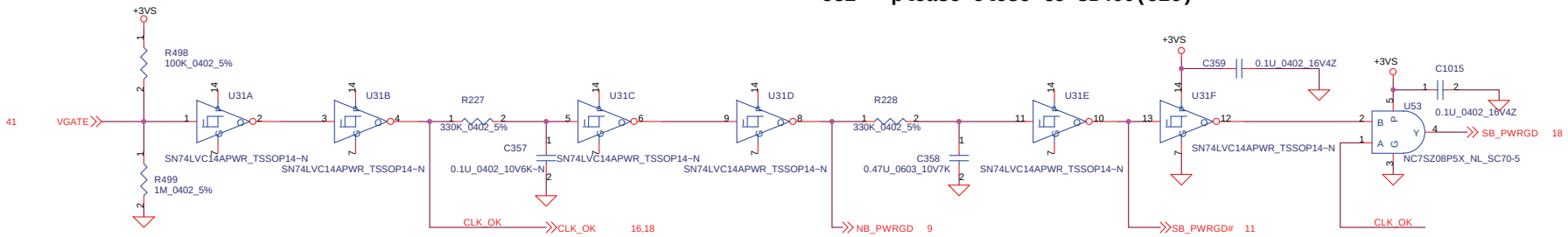


REQUIRED STRAPS

	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7 PCI_CLK8	SB_BMREQ#	MEM_STRAP	STRAP_EEPROM
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	USB PHY PWRDOWN DISABLE	Use internal PLL for 48MHZ	PCIE_CM SET LOW	CPU I/F = AMD	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM DEFAULT		1.8V DDR	EEPROM STRAP
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	48MHz XTAL MODE DEFAULT	PCIE_CM SET HIGH DEFAULT	CPU I/F = INTEL DEFAULT	L,H = NORMAL LPC ROM L,L = FWH ROM	0= NORMAL (Default)	2.5V DDR	MEM CHANNEL



U32-->please close to SB400(U16)



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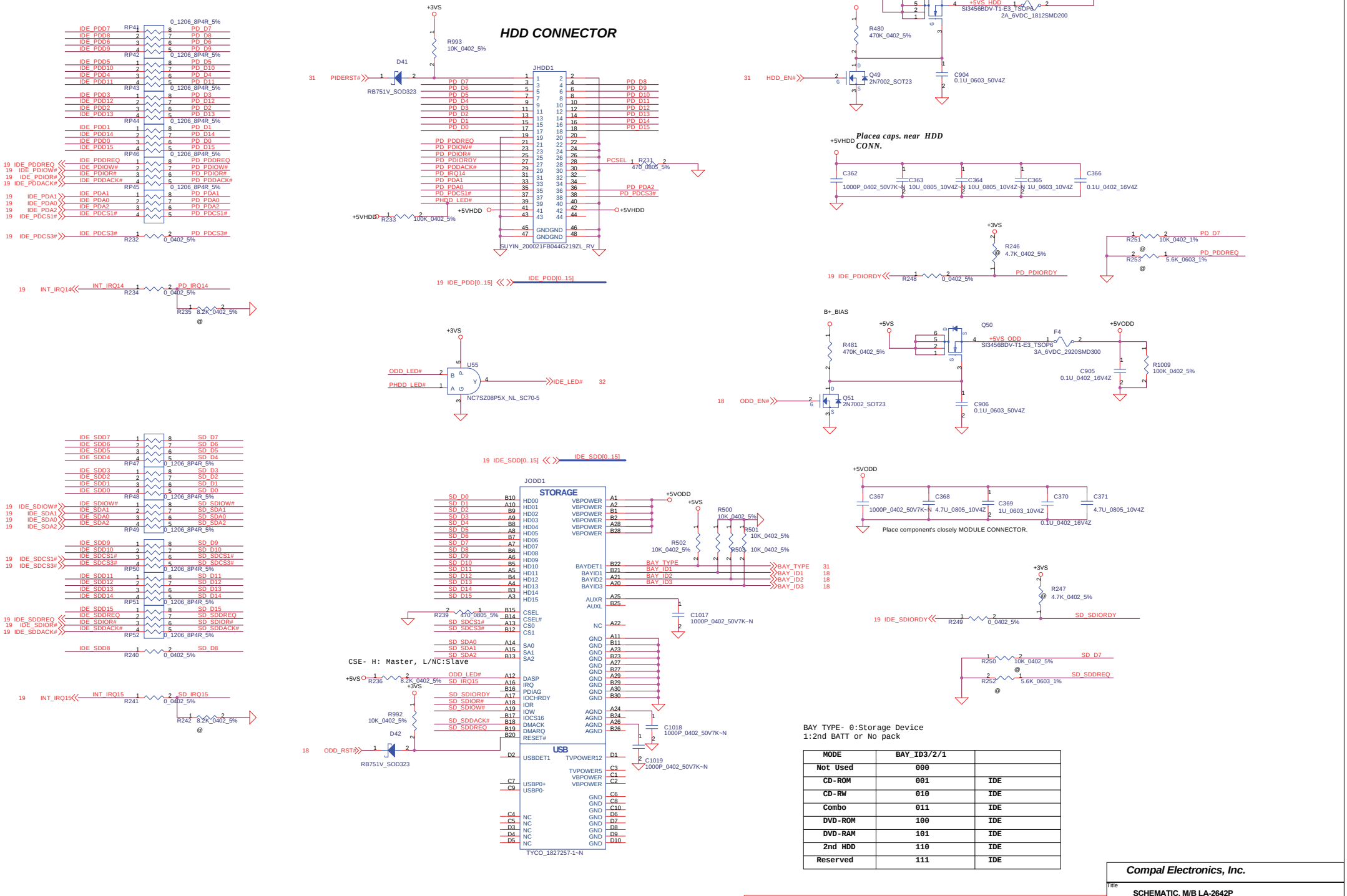

MODE	BAY_ID3/2/1	
Not Used	000	
CD-ROM	001	IDE
CD-RW	010	IDE
Combo	011	IDE
DVD-ROM	100	IDE
DVD-RAM	101	IDE
2nd HDD	110	IDE
Reserved	111	IDE

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+USB_BS=60 mils

80 mils

U15
TPS2061DGNG4_MSOP8-N
C380 0.1U_0402_16V4Z
C377 150U_D2_6.3VM
C381 @150U_D2_6.3VM
C379
R1000 0_0402_5%
R999 0_0402_5%
R46 30K_0402_5%
Q4 2N7002_SOT23
L36 WCM2012F2S-900T04_0805
JUSBP1 SUYIN_020122MR008G570ZL-N
L37 WCM2012F2S-900T04_0805
C384 @2.2P_0402_50V8C
C385 @2.2P_0402_50V8C
C382 @2.2P_0402_50V8C
C383 @2.2P_0402_50V8C
L45 WCM2012F2S-900T04_0805
JUSBP3 SUYIN_020133MR004S529ZL-N
@C393 2.2P_0402_50V8C
@C394 2.2P_0402_50V8C

80 mils

U16
TPS2061DGNG4_MSOP8-N
C390 0.1U_0402_16V4Z
C387 150U_D2_6.3VM
@C386 150U_D2_6.3VM
C388 0.1U_0402_16V4Z
R1001 0_0402_5%
R1002 0_0402_5%
R1 30K_0402_5%
Q12 2N7002_SOT23
L44 WCM2012F2S-900T04_0805
JUSBP2 SUYIN_020133MR004S529ZL-N
@C391 2.2P_0402_50V8C
@C392 2.2P_0402_50V8C

FINGERPRINT

F5 1.1A_6VDC_FUSE
JP19 JST_BM04B-SRSS-N

BLUETOOTH

200mA

JP10 ACES_87151-2007L-N
L26 BLM11A601S_0603
F6 1.1A_6VDC_FUSE
C395 0.1U_0402_16V4Z

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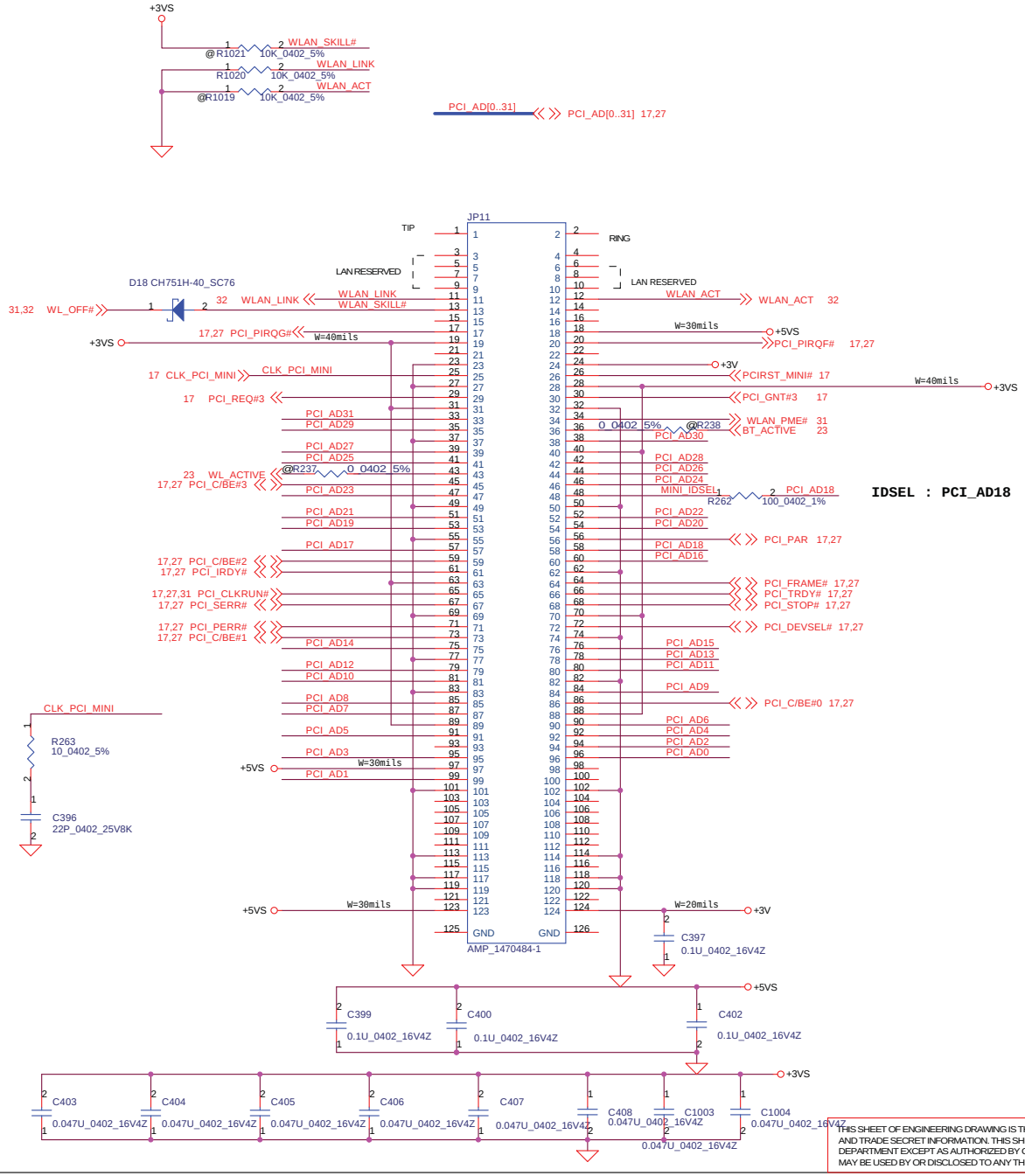

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MMJT9435

C		
	2	
B	C	E
1	4	3

Layout Notice : Place as close chip as possible.

Layout Notice : 3.3V filter. Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

Notice : 4.7u 6.3V capactor Thickness 1.25mm

Pin L9, if TPM supported, Pull down via 4.7K resister. L09 floating to disable TPM function.

Pin L06:Low Power Mode
Driven High-IDDQ Mode(less than 20mA)
Driven Low-Normal Mode

Layout Notice : Place as close chip as possible.

Layout Notice : Filter place as close chip as possible.

Layout Notice : Filter place as close chip as possible.

Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC

No_CIS_Symbol

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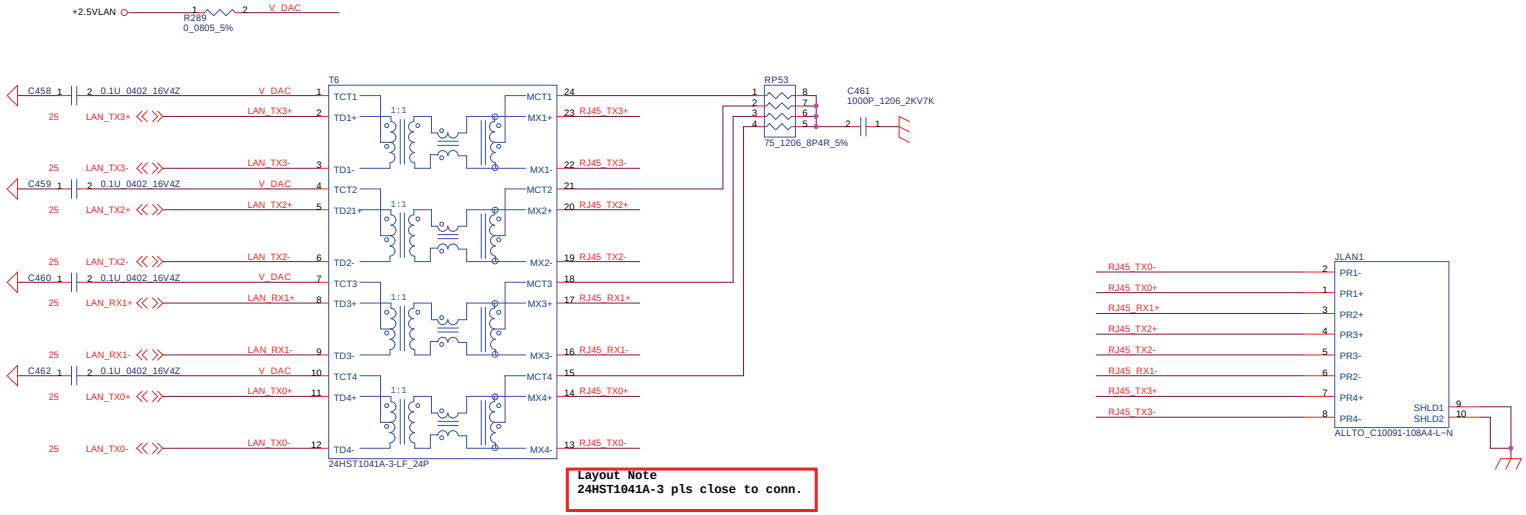
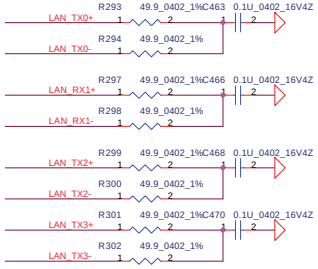
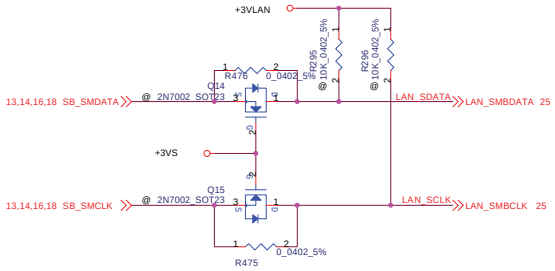
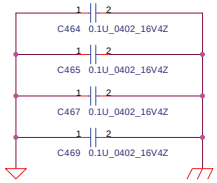


Layout Note
24HST1041A-3 pls close to conn.



All 49.9 ohm + 0.1 uF termination components close to BCM5751M





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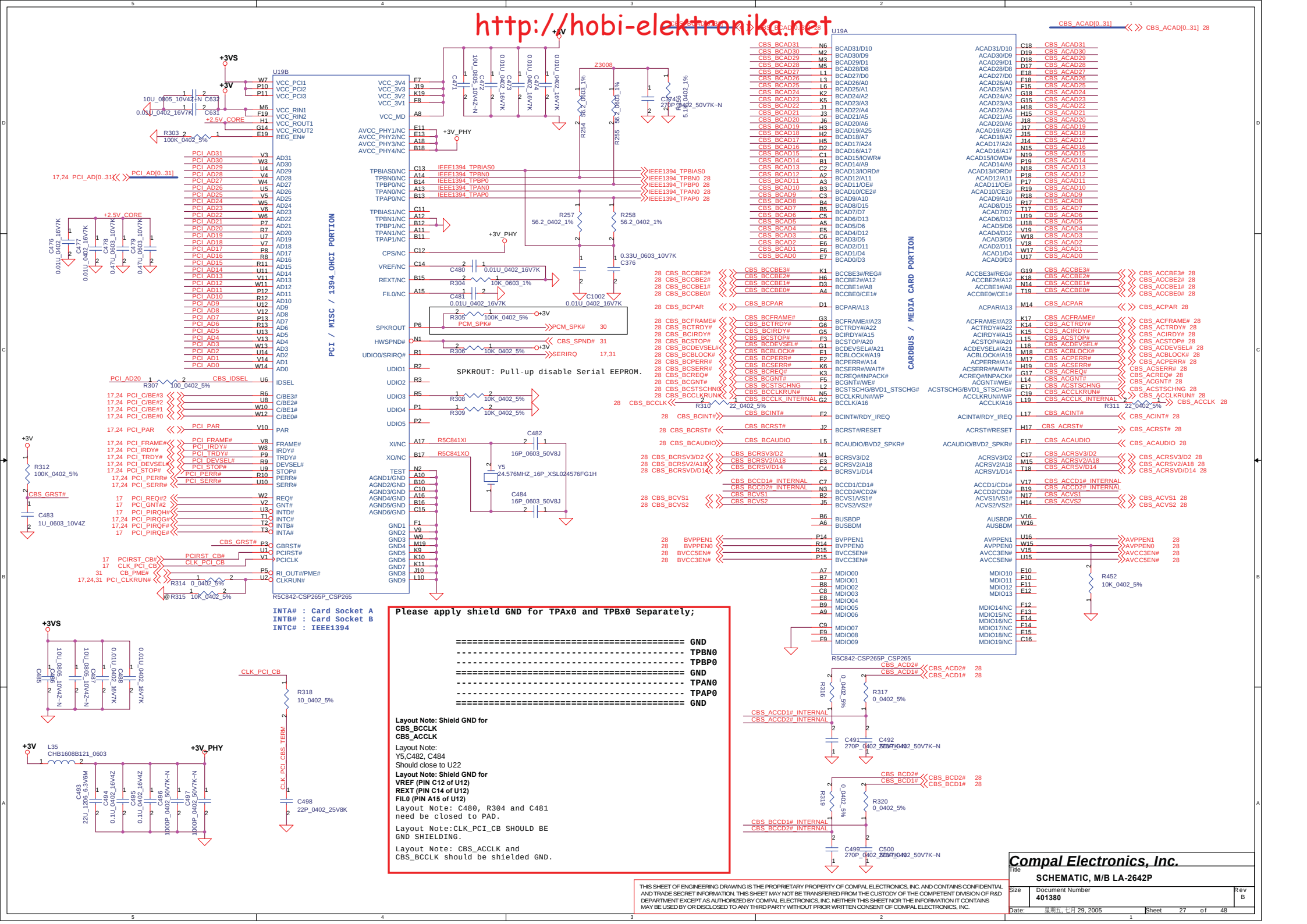

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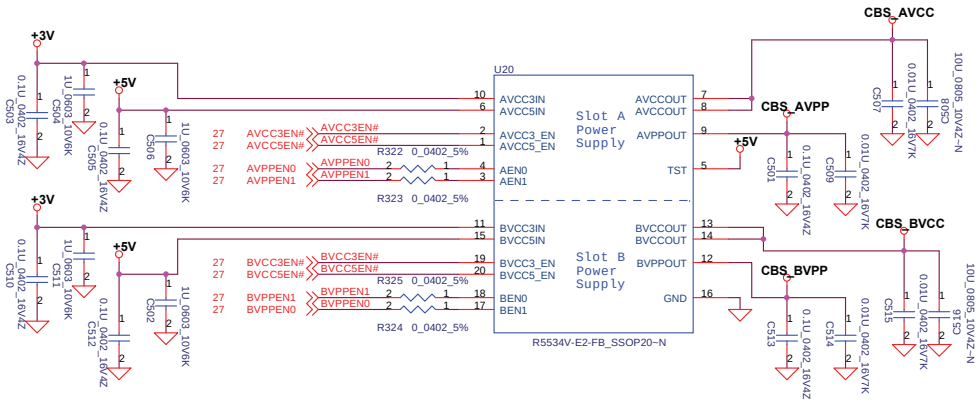
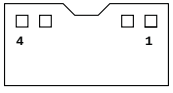
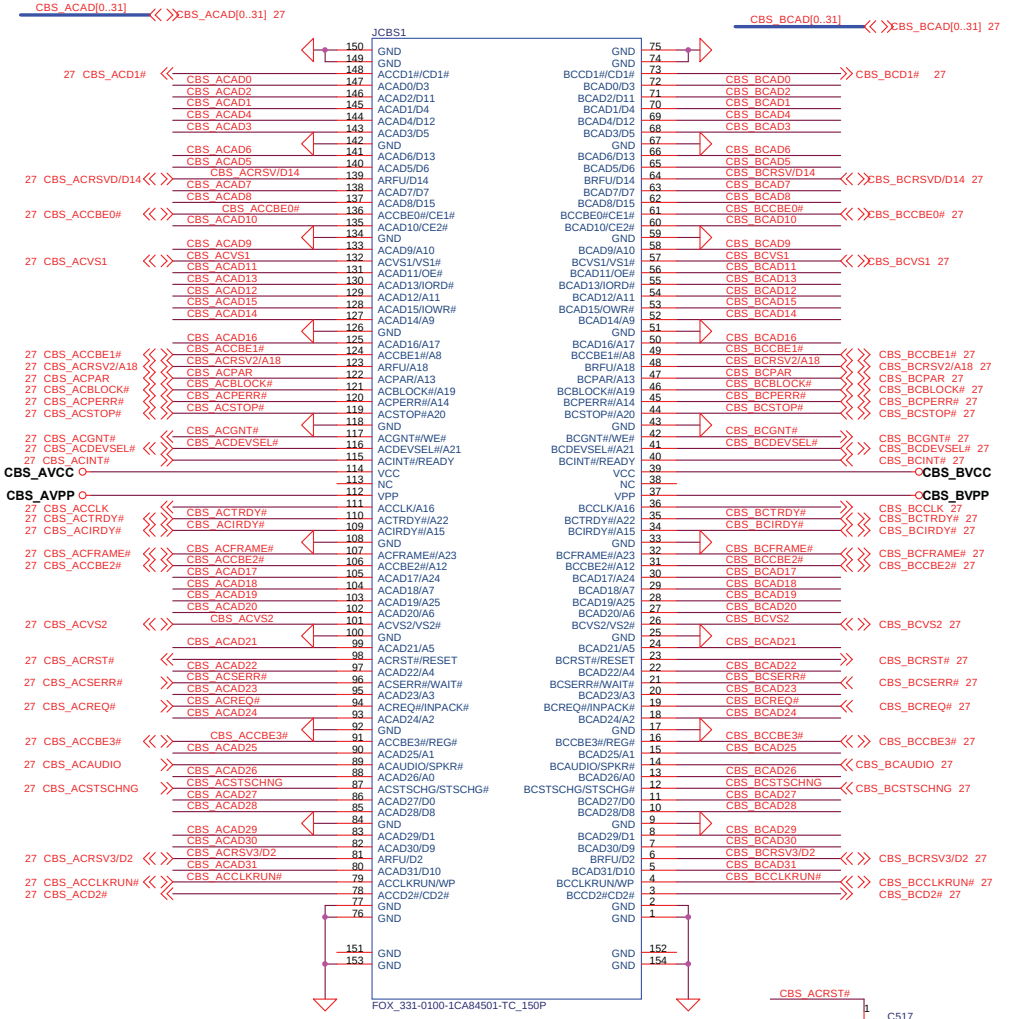
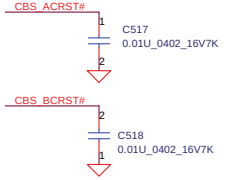




1: TPB#
2: TPB
3: TPA#
4: TPA





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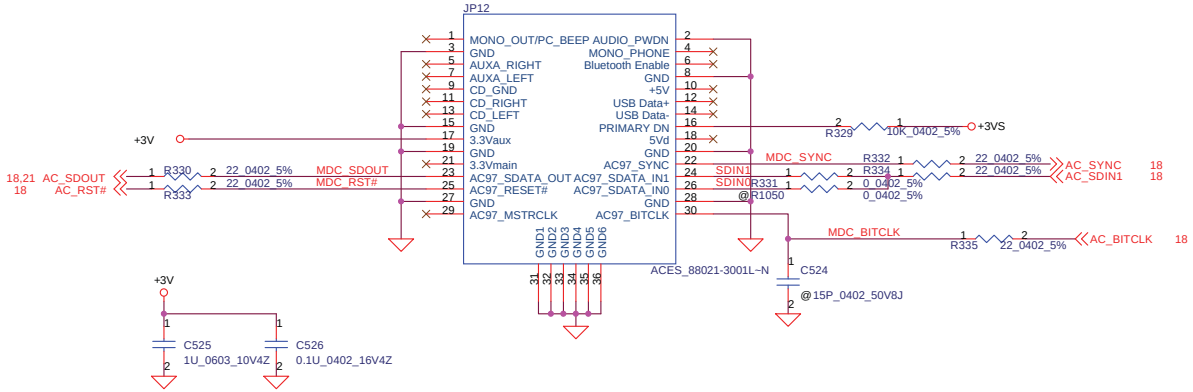
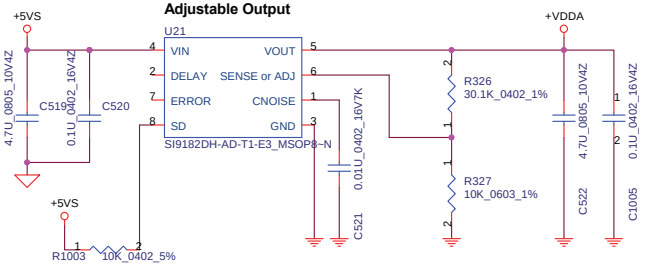
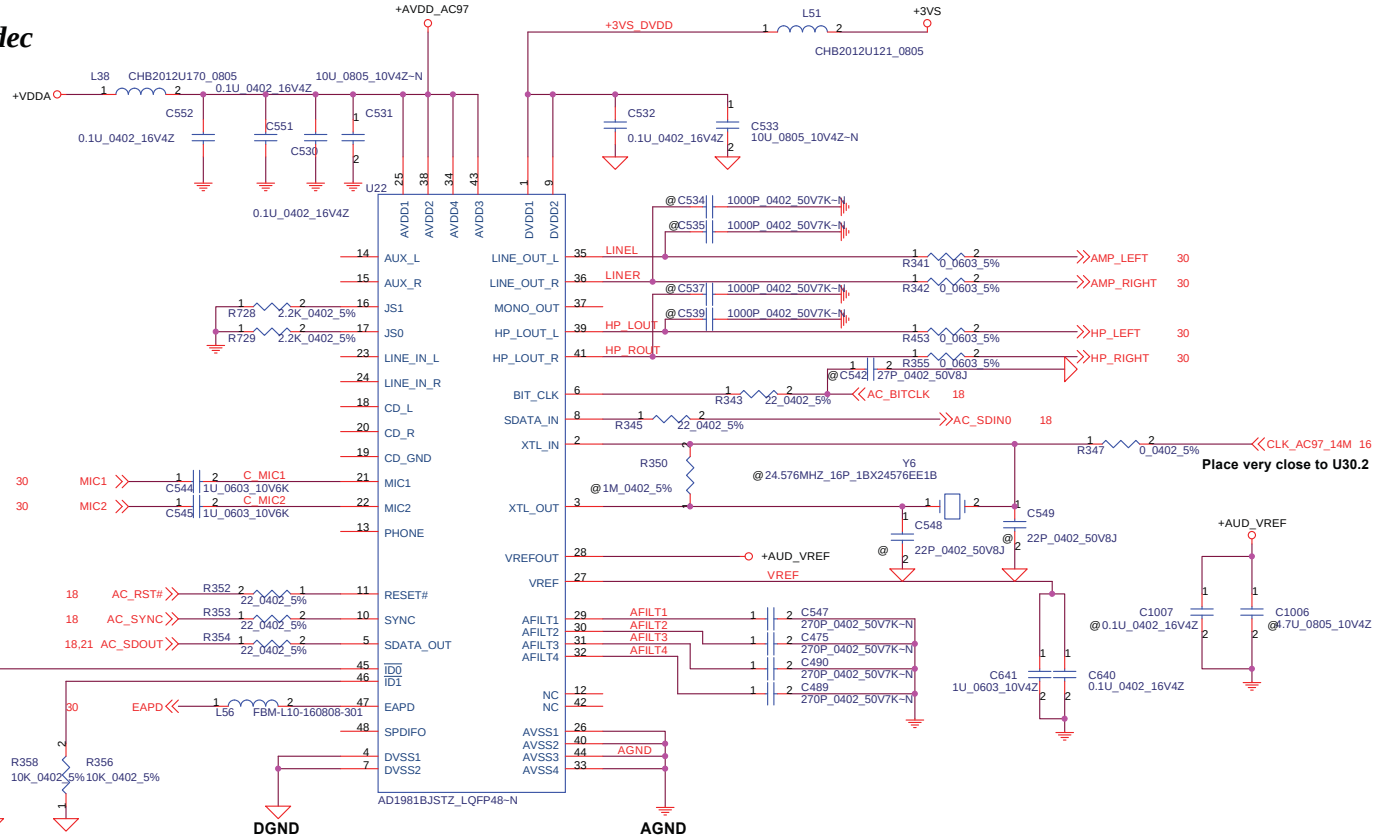
MDC CONN.



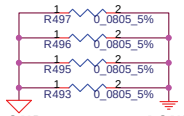
Adjustable Output



AC97 Codec



Reserved for TEST



Add ID table

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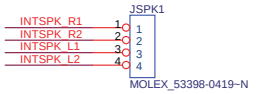
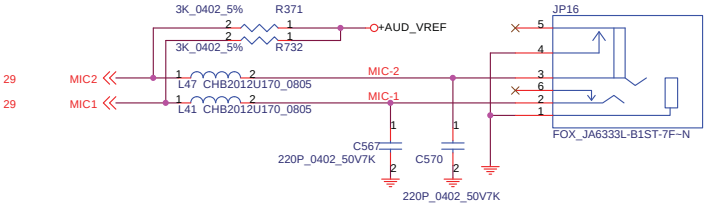
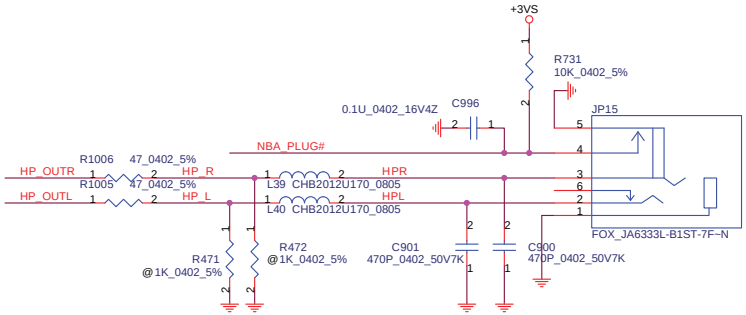
Speaker Connector

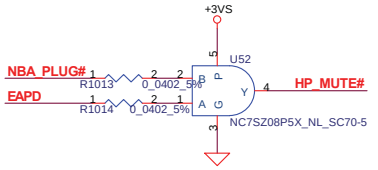


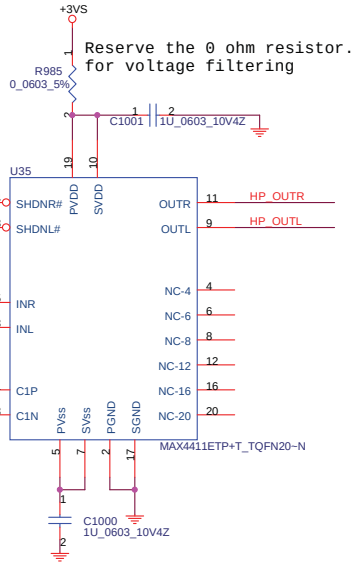
MICROPHONE IN JACK

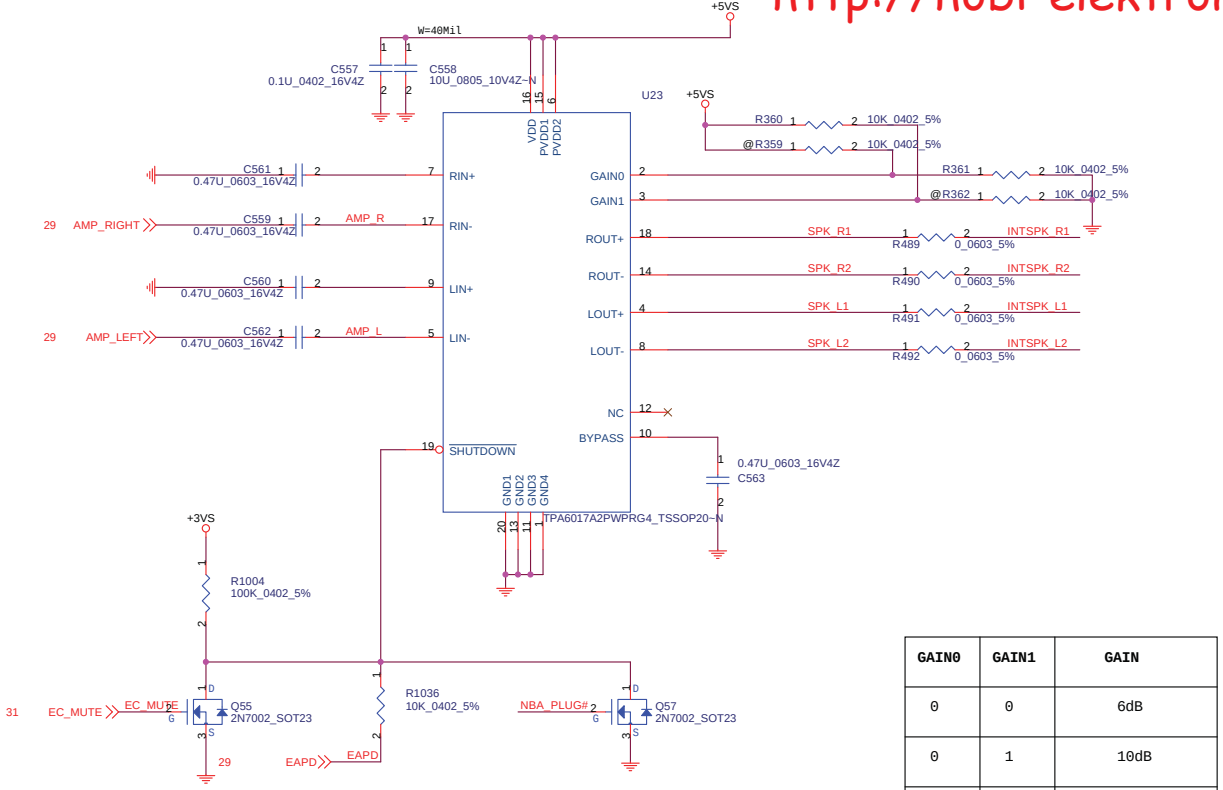


HEADPHONE OUT JACK



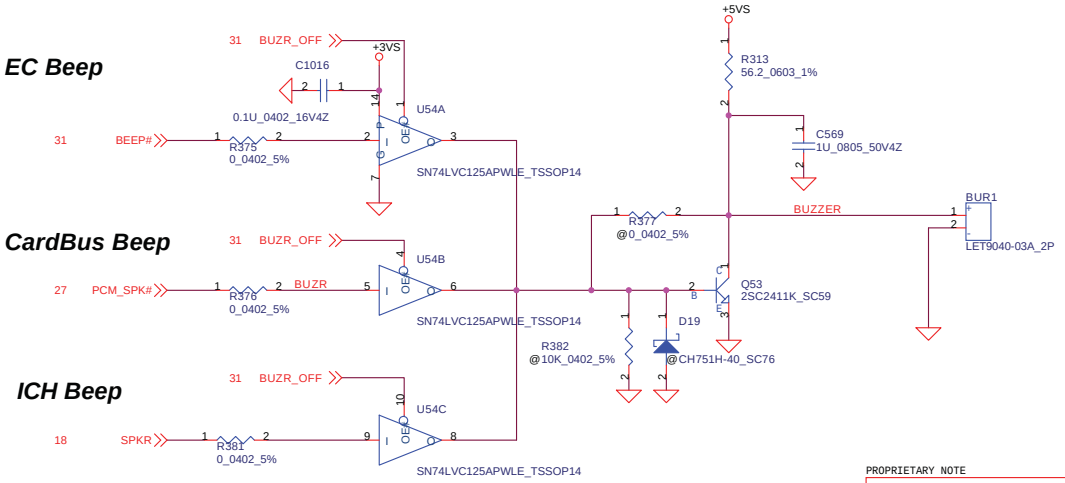






GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off



PROPRIETARY NOTE

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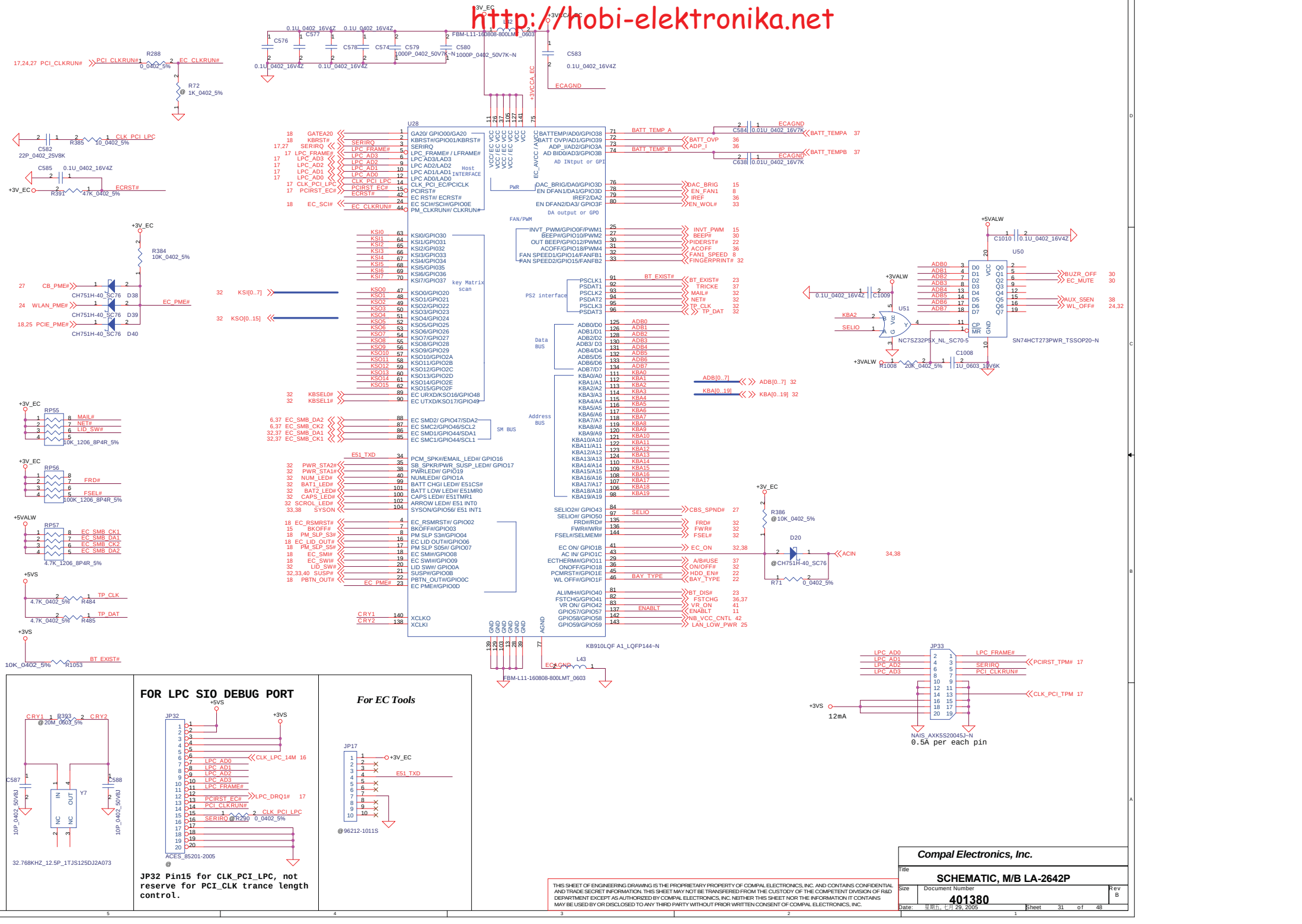
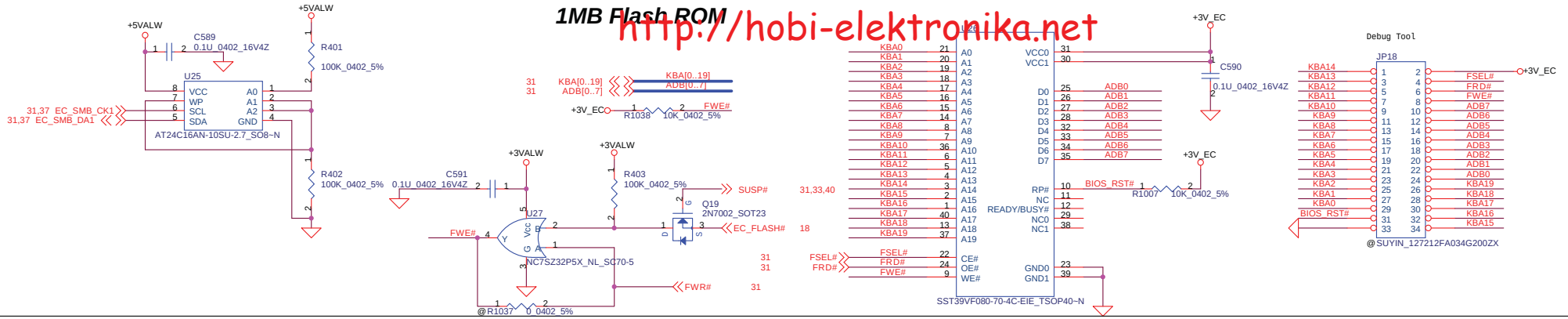
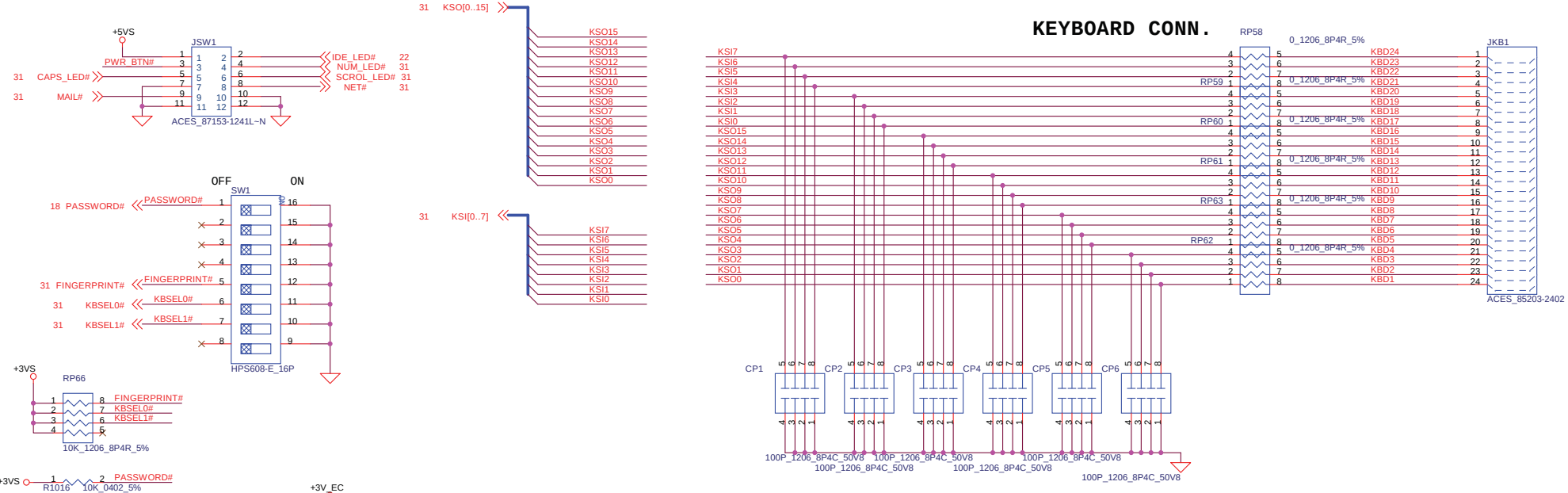
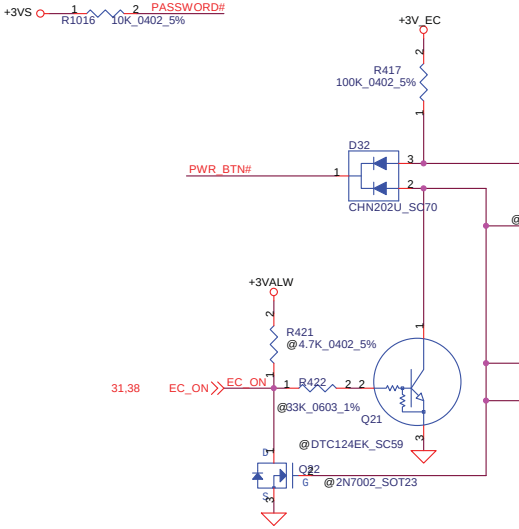


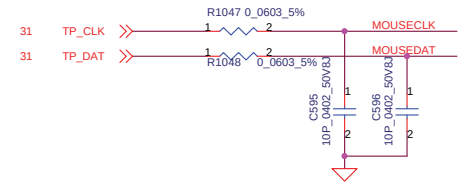
1MB Flash ROM



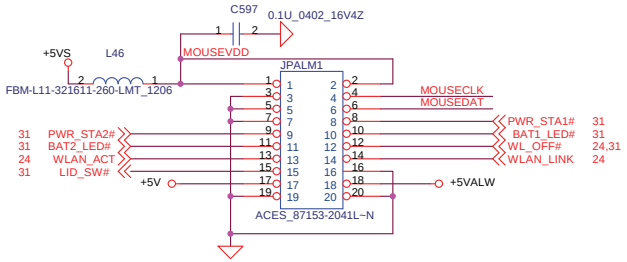
KEYBOARD CONN.







Touch-Pad CONN.



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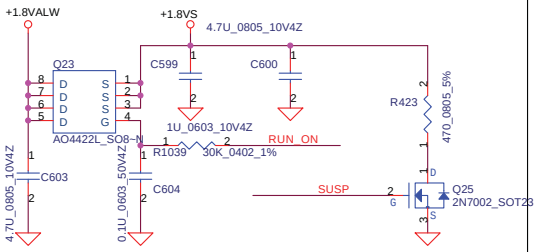
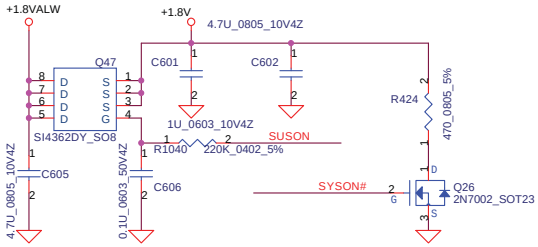
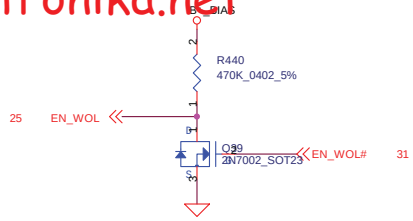
+1.8VALW TO +1.8VS

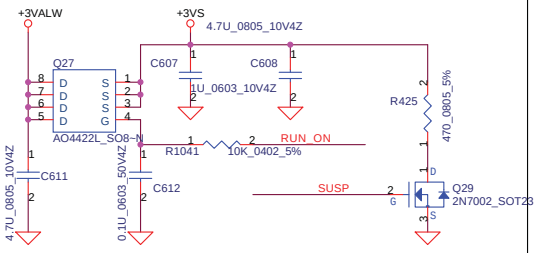


+1.8VALW TO +1.8V

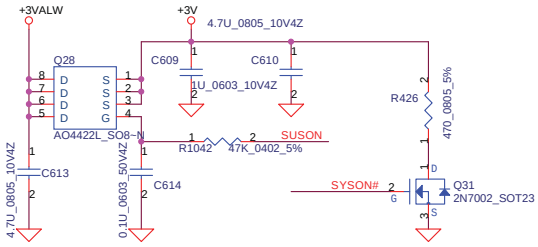




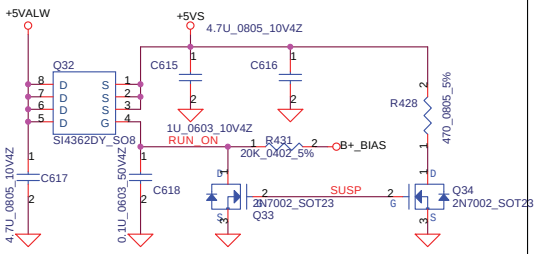
+3VALW TO +3VS



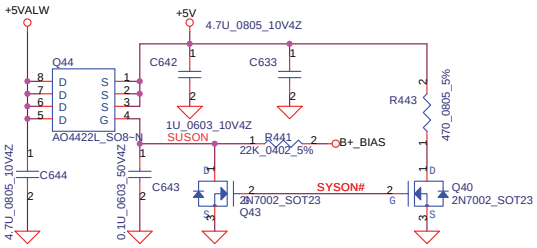
+3VALW TO +3V

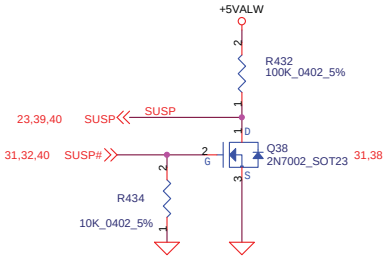


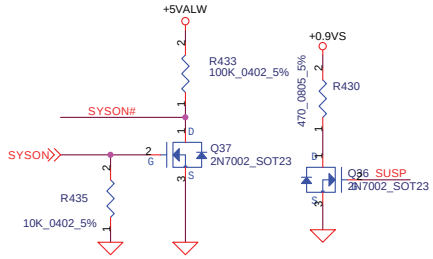
+5VALW TO +5VS

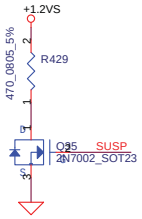


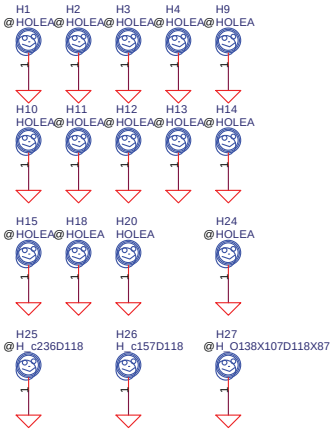
+5VALW TO +5V

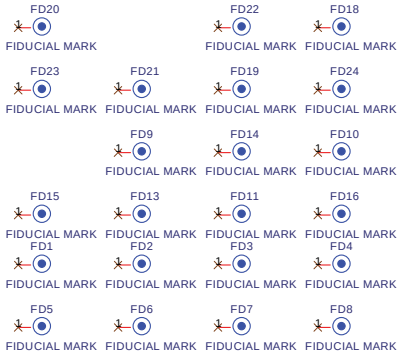


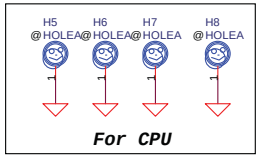












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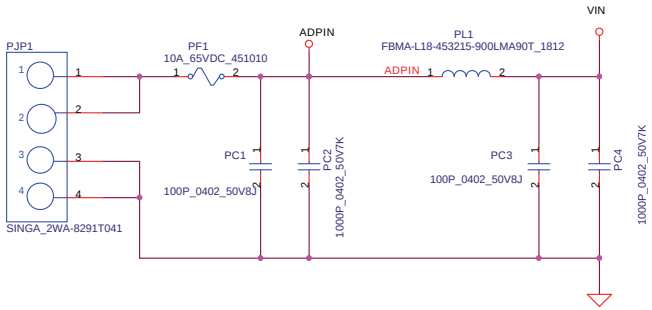
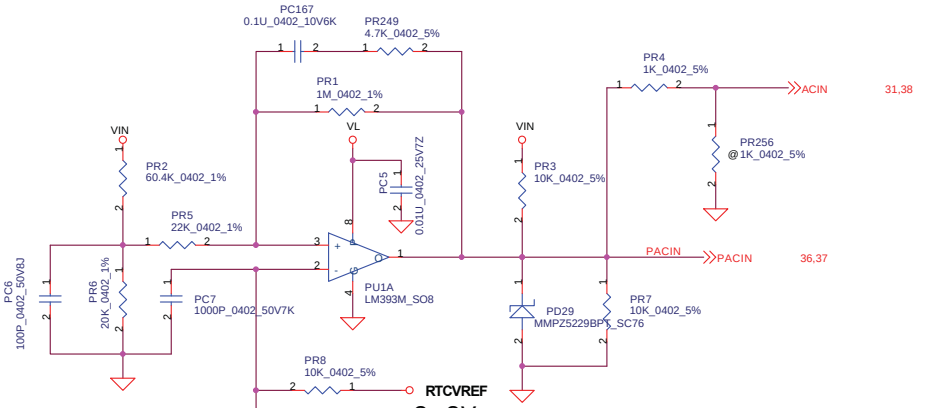
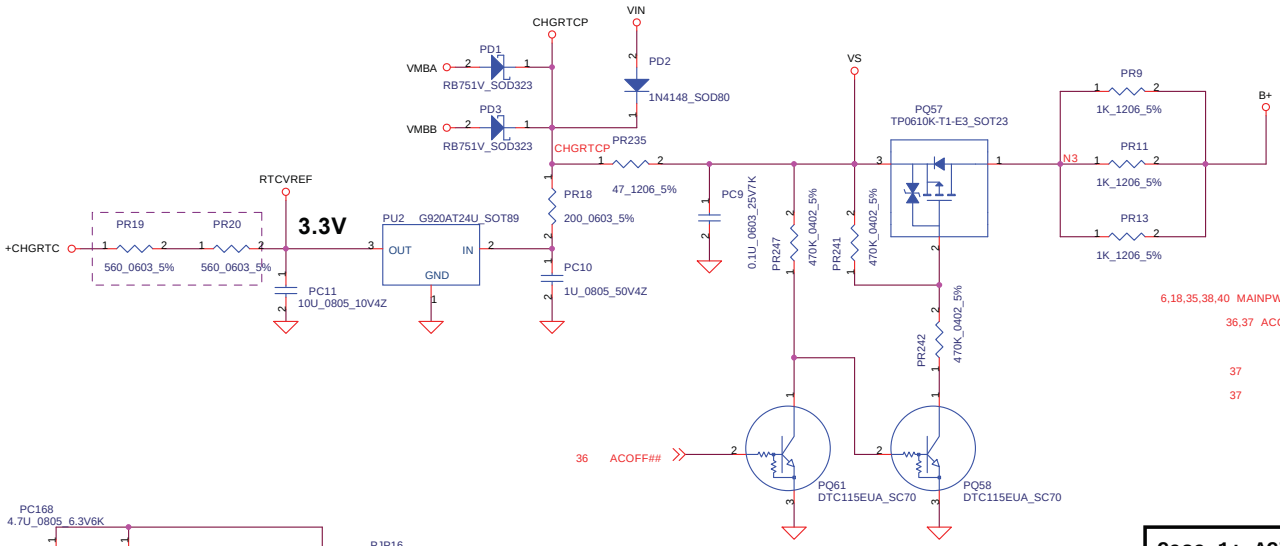
Detector

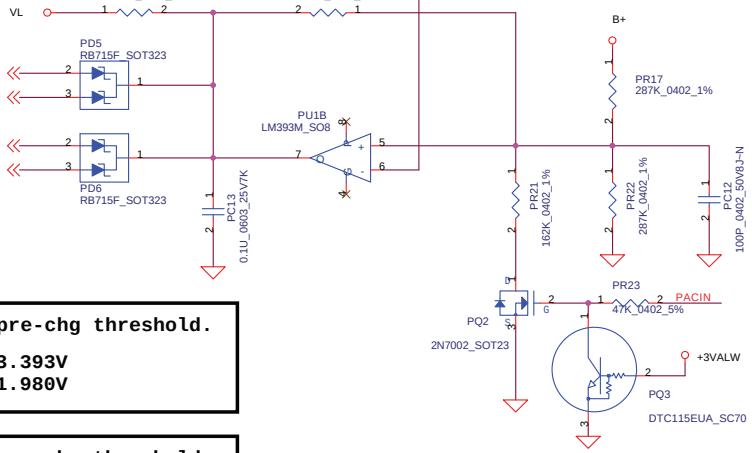
Vin Detector Threshold:

Low > High: 13.757V
High > Low: 13.160V







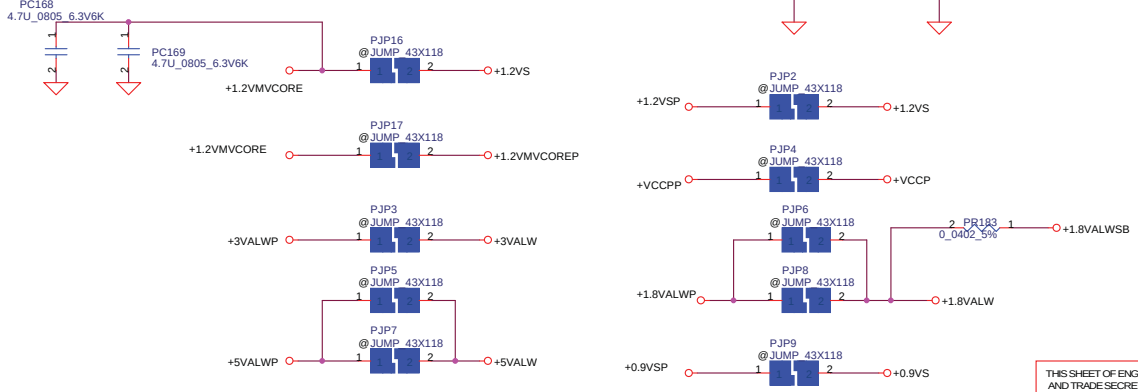


Case 1: ACIN pre-chg threshold.

Low > High: 13.393V
High > Low: 11.980V

Case 2: BATT pre-chg threshold.

Low > High: 7.547V
High > Low: 6.134V



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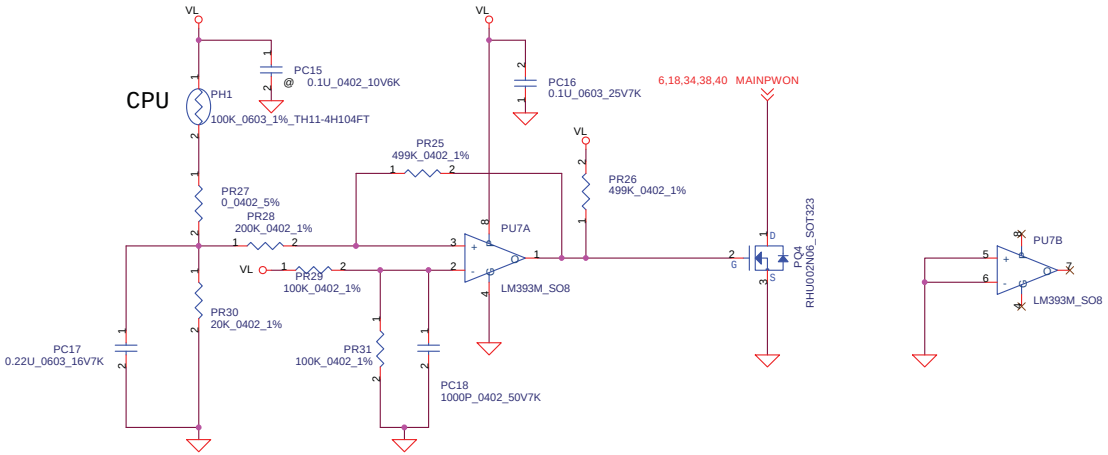
PH1 under CPU botten side :
CPU thermal protection at 86 +-3 degree C
Recovery at 51 +-3 degree C



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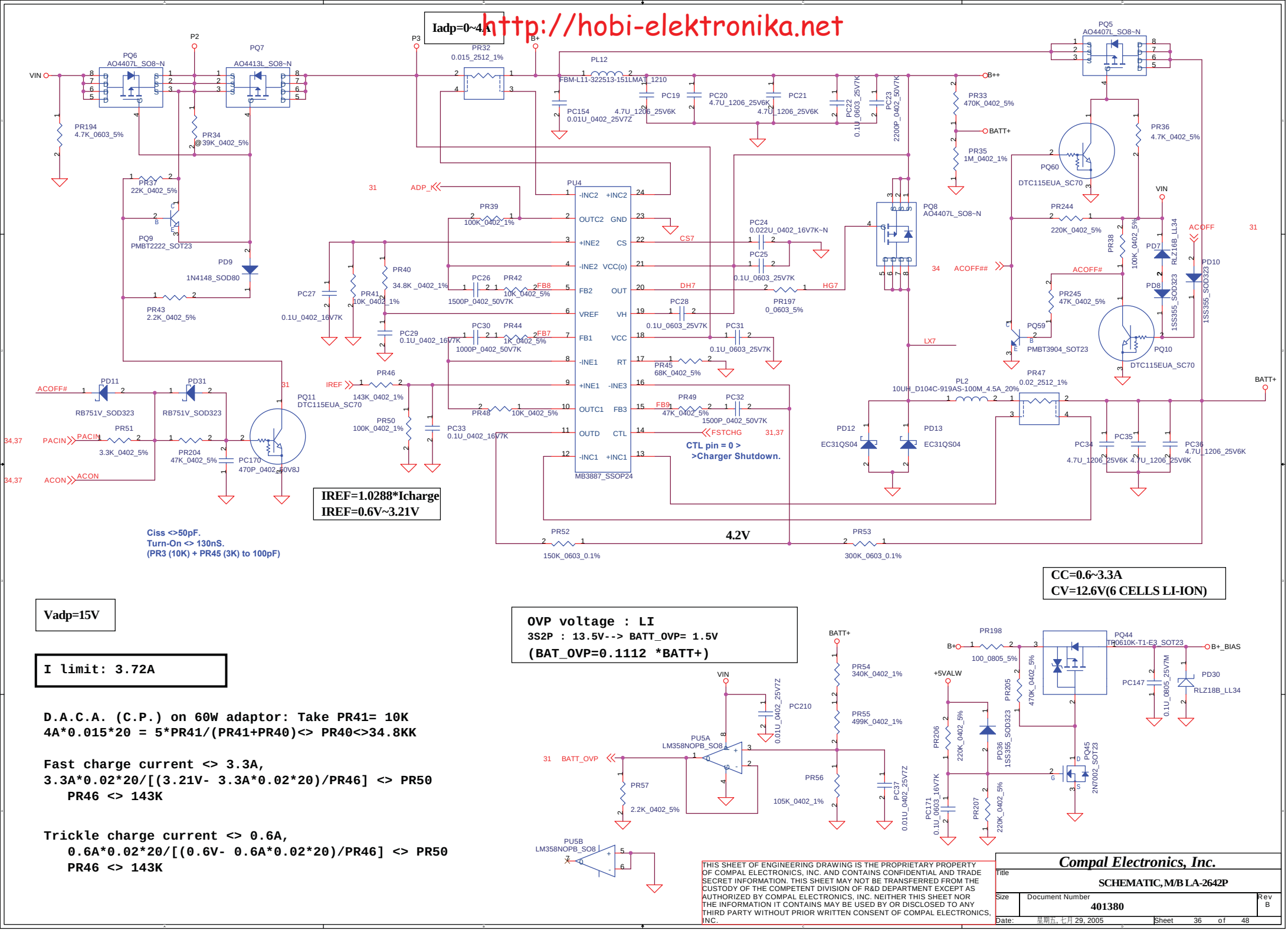

D.A.C.A. (C.P.) on 60W adaptor: Take PR41= 10K
4A*0.015*20 = 5*PR41/(PR41+PR40)<> PR40<>34.8KK

Fast charge current <> 3.3A,
3.3A*0.02*20/[(3.21V- 3.3A*0.02*20)/PR46] <> PR50
PR46 <> 143K

Trickle charge current <> 0.6A,
0.6A*0.02*20/[(0.6V- 0.6A*0.02*20)/PR46] <> PR50
PR46 <> 143K

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Battery Selector

Ciss<3000pF.
Qg<40nC.

Ciss<3000pF.
Qg<40nC.

PBJ1 — SUYIN_250233MR007GX26ZU
1.BAT+
2.ID
3.B/I
4.TS
5.SMD
6.SMC
7.GND

PF6 12A_65VDC_451012 — PL3 FBMA-L18-453215-900LMA90T_1812 — AB/I — TSA
PC38 1000P_0402_50V7K
VMBA
PR58 1K_0603_5%
PC40 0.01U_0402_25V7Z
PR64 6.49K_0402_1%
+3VALWP
PR68 100_0402_5%
PR69 100_0402_5%
PR66 1K_0402_5%
BATT_TEMPA 31
EC_SMB_DA1 31,32
EC_SMB_CK1 31,32

PQ12 AO4407L_SO8-N
PQ13 AO4413L_SO8-N
PQ14 AO4413L_SO8-N
PQ15 AO4407L_SO8-N
P5
P4
BATT+
PR61 39K_0402_5% @
PR59 39K_0402_5% @
PR62 22K_0402_5%
PR63 22K_0402_5%
PQ16 PMBT2222_SOT23
PQ17 PMBT2222_SOT23
PD14 1N4148_SOD80
PD15 1N4148_SOD80
PR70 2.2K_0402_5%
PR71 2.2K_0402_5%

34 GA
GA
PD33 RB751V_SOD323
PR74 10K_0402_5%
PC173 2200P_0402_50V7K
PQ18 DTC115EUA_SC70

34 GB
GB
PD32 RB751V_SOD323
PR75 10K_0402_5%
PC172 2200P_0402_50V7K
PQ19 DTC115EUA_SC70

VMBB
PC39 1000P_0402_50V7K
PF7 12A_65VDC_451012 — PL4 FBMA-L18-453215-900LMA90T_1812 — BB/I — TSB
PBJ2 — SUYIN_250233MR007GX26ZU
PC41 0.01U_0402_25V7Z
PR60 1K_0603_5%
+3VALWP
PR65 6.49K_0402_1%
PR67 1K_0402_5%
31 BATT_TEMPB
PR72 100_0402_5%
PR73 100_0402_5%
6,31 EC_SMB_DA2 — EC_SMD2
6,31 EC_SMB_CK2 — EC_SMC2

1.BAT+
2.ID
3.B/I
4.TS
5.SMD
6.SMC
7.GND

Turn-On Delay
<> (10K + 3K + 100K) * (100pF+50pF)
<> 4uS.
Turn-Off < 2uS.

PU6 74HC253
VL
PC43 0.1U_0402_16V7K
34,36 ACON
PR78 27K_0402_1%
PR208 100K_0402_5%
PC45 100P_0402_50V8J
PQ20 DTC115EUA_SC70
PQ46 DTC115EUA_SC70
31,36 FSTCHG
PR83 100K_0402_1%
RR84 100K_0402_1%
A/B#USE 31
PQ21 DTC115EUA_SC70

PR76 100K_0402_5%
PU3B LM393M_SO8
PC42 0.01U_0402_25V7Z
PR80 27K_0402_5%
PR82 5.6M_0603_5%
PR79 100K_0402_5%
PR77 649K_0402_1%
PR81 499K_0402_1%
PC44 47P_0402_50V8J

{Vbatt_max *[499K/(499K+649K)]+V_dischg}
* {1- exp^[-Δt/(R*C)]}
> {Vbatt_max *[499K/(499K+649K)] +V_dischg}
-RTCVREF +V_hysteresis

Sense Delay Time by hysteresis and R/C
is about 24.8uS.

2nd B Battery Detector
High:8.117V
Low :7.36V

RTCVREF
PR86 100K_0402_5%
PU3A LM393M_SO8
PR89 27K_0402_5%
PR91 5.6M_0603_5%
PR85 10K_0402_5%
PR88 100K_0402_5%
PR87 649K_0402_1%
PR90 499K_0402_1%
PC46 47P_0402_50V8J
PC47 100P_0402_50V8J

Main A Battery Detector
High:8.117V
Low :7.36V

A/B#USE
High: Main Battery (A)
Low : Second Battery (B)

TRICKLE EC Override time:
<> 3* (R-C) charging time
<> 3* (1K * 1000pF)
<> 3uS.

PQ22 RHU002N06_SOT323
PR92 47K_0402_5%
PACIN
34,36 When in Trickle charge, battery is selected by EC "A/B#USE" pin
PD17 1N4148_SOD80
TRICKE 31

S0	S1	nC0	nC1	nC2	nC3	nOE	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

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+3.3V/+5V

B+
PF3
10A_65VDC_451010
PL13
FBM-L11-322513-151LMAT_1210
PC155
0.01U_0402_25V7Z
PC166
4.7U_1206_25V6K
@
B+++
PC48
0.1U_0402_16V7K
PR95
0_0603_5%
PQ23
SI4914DY-T1-E3_SO8
HG2
PR93
0_0603_5%
PC50
4.7U_1206_25V6K
PC51
0.1U_0603_25V7K
PC52
@2200P_0603_50V7K
PC53
4.7U_1206_25V6K
LX2
DL2
DH2
DAP202U_SOT323
PD18
VS
PR94
10_1206_5%
VL
PD19
1SS355_SOD323
PC62
1U_1206_25V4Z
PC54
4.7U_0805_6.3V6K
PC59
100P_0402_50V8J
PC60
100P_0402_50V8J
I-thermal=0.05A,
I-OCP=0.1A.
PR96
0_0603_5%
PC49
0.1U_0402_16V7K
PL5
4.7U_#892NAS-4R7M=P3_5.6A_20%
PQ24
SI4810BDY-T1-E3_SO8
HG1
PC56
4.7U_1206_25V6K
PC55
@2200P_0603_50V7K
PC57
0.1U_0603_25V7K
PC58
4.7U_1206_25V6K
PQ25
AO4704L_SO8_N
PC61
47P_0402_50V8J
@
PR98
0_0603_5%
PR100
@2M_0402_1%
PL6
4.7U_#892NAS-4R7M=P3_5.6A_20%
PR97
1.1K_0402_1%
PC64
47P_0402_50V8J
@
PR99
1K_0402_1%
PC65
0.47U_0603_16V7K
PU8
SC1403ITSTR_TSSOP28
BST2
BST3
DH3
PHASE3
DL3
V+
VL
COMP3
COMP5
BST5
DH5
PHASE5
DL5
PGND
CSH5
CSL5
FB5
SEQ
REF
SYNC
RESET#
CSH3
CSL3
FB3
PSAVE#
SHDN#
ON5
ON3
GND
BST1
DH1
LX1
DL1
CS1+
CS1-
CS2+
CS2-
FB2
FB1
2.5VREF
PC70
4.7U_0805_6.3V6K
f=300KHz
PR101
1.62K_0402_1%
PC66
0.47U_0603_16V7K
PR104
715_0402_1%
Use DCR * 1.3
to calculate O.C.P.
+3VALWP
PR102
1M_0402_1%
@
PR103
0_0402_5%
ACIN
31,34
PC68
150U_D_6.3VM_R18M
PD20
SKUL30-02AT_SMA
PR107
3.57K_0402_1%
PC67
100P_0402_50V8J
PR106
10K_0402_5%
PR108
@300K_0402_5%
PC69
0.022U_0402_16V7K-N
PR255
15K_0402_5%
PC213
0.1U_0402_16V7K
PR237
0_0402_5%
PR232
0_0402_5%
MAINPWON
6,16,34,35,40
PR111
220K_0402_5%
PR233
0_0402_5%
@
PU16
TC7SH32FU_SSOP5
MAINPWON
6,18,34,35,40
AUX_S5EN
31
PR200
@220K_0402_5%
PC75
@0.47U_0603_10V7K
PC153
@0.01U_0402_25V7Z
PC148
@
0.1U_0603_25V7K
CHGRTCP
PR112
47K_0402_5%
PR110
10K_0402_1%
PC76
0.047U_0603_25V7K
@
31,32
PR105
200K_0402_5%
@
PR234
@ 200K_0402_5%
SYSON
EC_ON
31,33,39
PC74
0.1U_0402_16V7K
(3V*5%)/5.3A=28.3mOhm ESR
PC71
0.1U_0402_16V7K
PR109
10.2K_0402_1%
PC73
100P_0402_50V8J
PD21
SKUL30-02AT_SMA
PC72
150U_D_6.3VM_R18M
+5VALWP
(5V*5%)/7.8A=32mOhm ESR
PR113
10K_0402_1%
Use DCR * 1.3
to calculate O.C.P.
CSH3-CSL3=48mV, OCP=5.3A, DCR=18mOhm
Rsens=48mv/5.3A=9mOhm
C*R1=L/Rsens<> 0.47UF*PR96=4.7UH/9mOhm<> PR97=1.1K Ohm
R2=R1*Rsens/(Iload*DCR)-Rsens
PR99=PR96*Rsens/(Iload*DCR*1.3)-Rsens
PR99=1.13K*48mV/{(5.3A*15mOhm*1.3)-48mV}=976Ohm
delta I= (Vin-Vo)*D/L*f=[(15-3)*(3/15)]/4.7u*300K=1.7
delta Vripple=deltal*ESR=1.7*25m=42.5mV
delta I= (Vin-Vo)*D/L*f=[(15-5)*(5/15)]/4.7u*300K=2.364
delta Vripple=deltal*ESR=2.364*25m=59.1mV
CSH5-CSL5=48mV, OCP=7.8A, DCR=18mOhm
Rsens=48mv/7.8A=6.15mOhm
C*R1=L/Rsens<> 0.47UF*PR100=4.7UH/6.15mOhm
<> PR101=1.62K Ohm
R2=R1*Rsens/(Iload*DCR)-Rsens
PR104=PR100*Rsens/(Iload*DCR*1.3)-Rsens
PR104=1.62K*48mV/{(7.8A*18mOhm*1.3)-48mV}=576 Ohm

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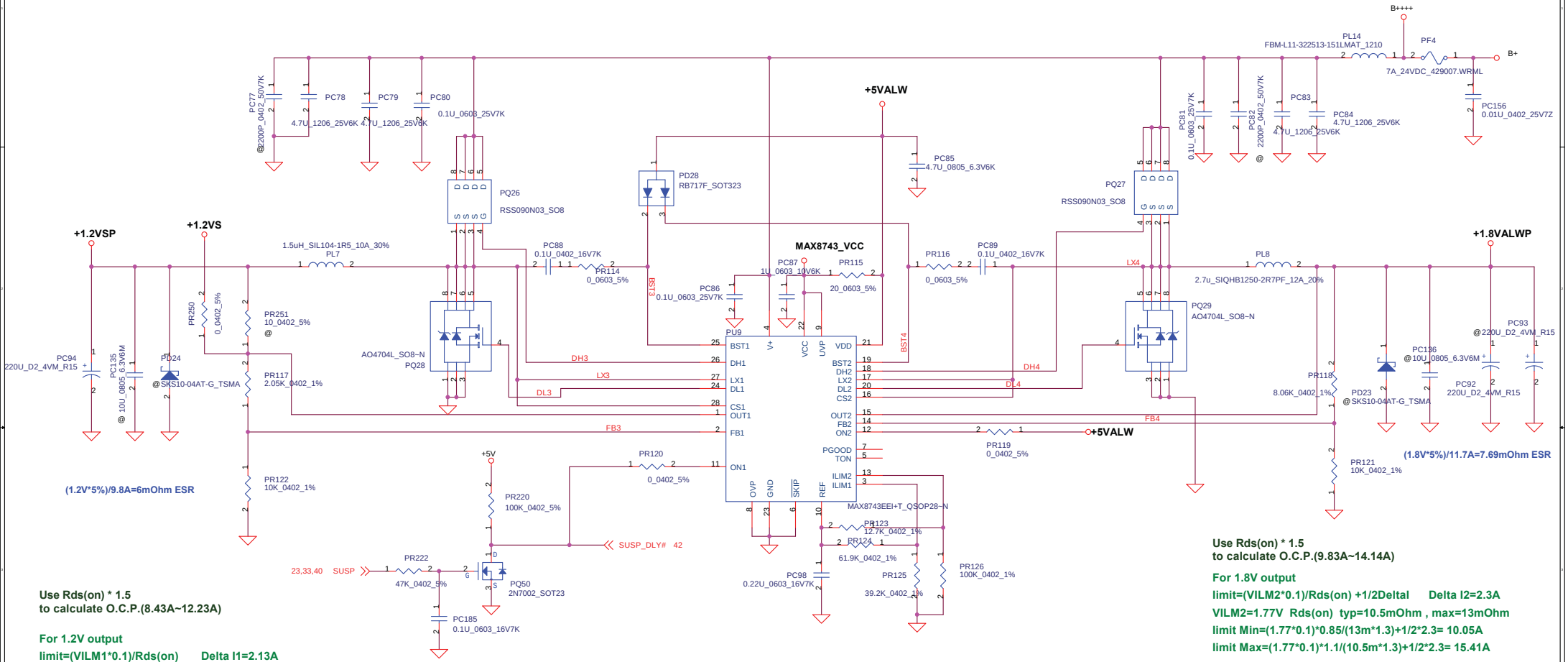

Use Rds(on) * 1.5
to calculate O.C.P.(8.43A~12.23A)

For 1.2V output
limit=(VILM1*0.1)/Rds(on) Delta I1=2.13A
VILM1=0.775V Rds(on) typ=10.3mOhm , max=13mOhm
limit Min=(0.775*0.1)*0.85/(13m*1.3)+1/2*2.13= 4.963A
limit Max=(0.775*0.1)*1.1/(13m*1.3)+1/2*2.13= 5.947A

delta Vripple=deltal*ESR=2.2*7.5m=16.5mV

Rds_Is=13mOhm , R125=39.2KOhm , VREF=2V,Iload=5.5A
delta I1=(Vin-Vo)*D/L*f=[(15-1.2)*(1.2/15)]/1.5u*345K=2.13A
[Iload-(0.5*delta I1)]*Rdson*1.5=VREF*[PR125/(PR124+PR125)]*0.1
[5.5-(0.5*2.13)]*13m*1.3=2*[39.2K/(PR124+39.2K)]*0.1
PR125=61.9K

Rds_Is=13mOhm , R126=100KOhm , VREF=2V,Iload=11.5A
delta I2=(Vin-Vo)*D/L*f=[(15-1.8)*(1.8/15)]/2.7u*255K=2.3A
[Iload-(0.5*delta I2)]*Rdson*1.5=VREF*[PR126/(PR123+PR126)]*0.1
[11.5-(0.5*2.3)]*13m*1.3=2*[100K/(PR123+100K)]*0.1
PR123<>12.7K

Use Rds(on) * 1.5
to calculate O.C.P.(9.83A~14.14A)

For 1.8V output
limit=(VILM2*0.1)/Rds(on) +1/2Deltal Delta I2=2.3A
VILM2=1.77V Rds(on) typ=10.5mOhm , max=13mOhm
limit Min=(1.77*0.1)*0.85/(13m*1.3)+1/2*2.3= 10.05A
limit Max=(1.77*0.1)*1.1/(10.5m*1.3)+1/2*2.3= 15.41A

delta Vripple=deltal*ESR=3*7.5m=22.5mV

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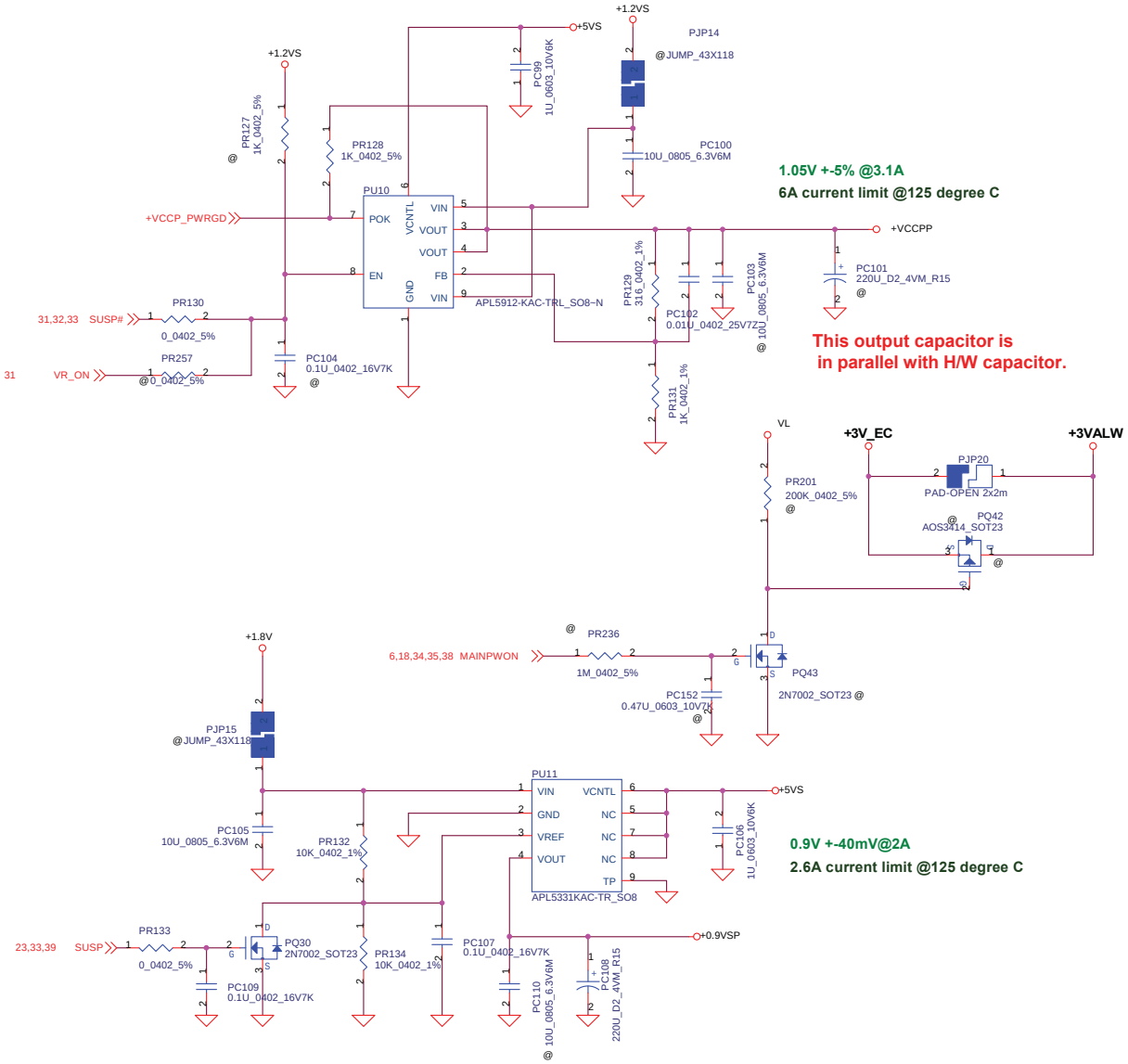
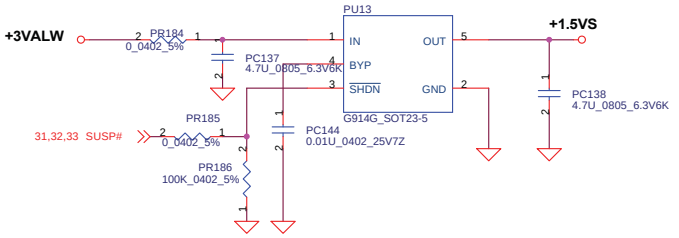
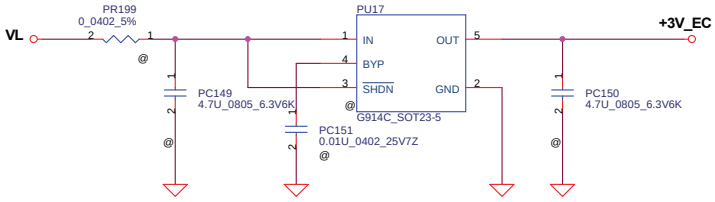
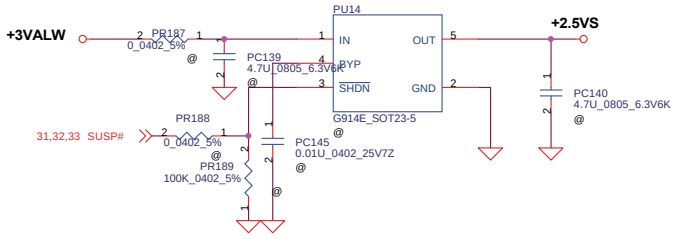
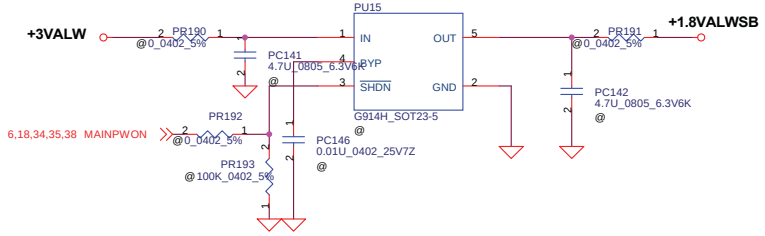
0.9VSP/VCCP











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CPU CORE

delta I= (Vin-Vo)*D/L*f=[(15-1.308)*(1.308/15)]/(.56u*300K)=7.1A

OCP=41A(TYP), DCR=1.4mOhm

Ilimit(min) per phase=41/2-7.1/2=16.95A

16.95A*1.4mOHM(DCR)*1.3(temperature factor)*20=VLLIM(TYP)=0.61698V

Take PR156=200K, PR158=90.9K

VILIM=VREF*PR158/(PR158+PR156)=0.625(TYP)

VILIM/20=Ilimit*DCR*1.3

OCP(TYP)=(0.625/20/1.3/1.4mOHM+delta I/2)*2=41A

OCP(min)=((0.625/20-2mV)/1.3/1.4mOHM+delta I/2)*2=38.83A

OCP(max)=((0.625/20+2mV)/1.3/1.4mOHM+delta I/2)*2=43.23A

C*R>=L/DCR<> 0.47UF*PR147=0.56UH/1.4mOhm
<> PR147=851Ohm<>866 Ohm

CPU Remote - - Sensing Pairs

MAX1532AETL_TQFN40

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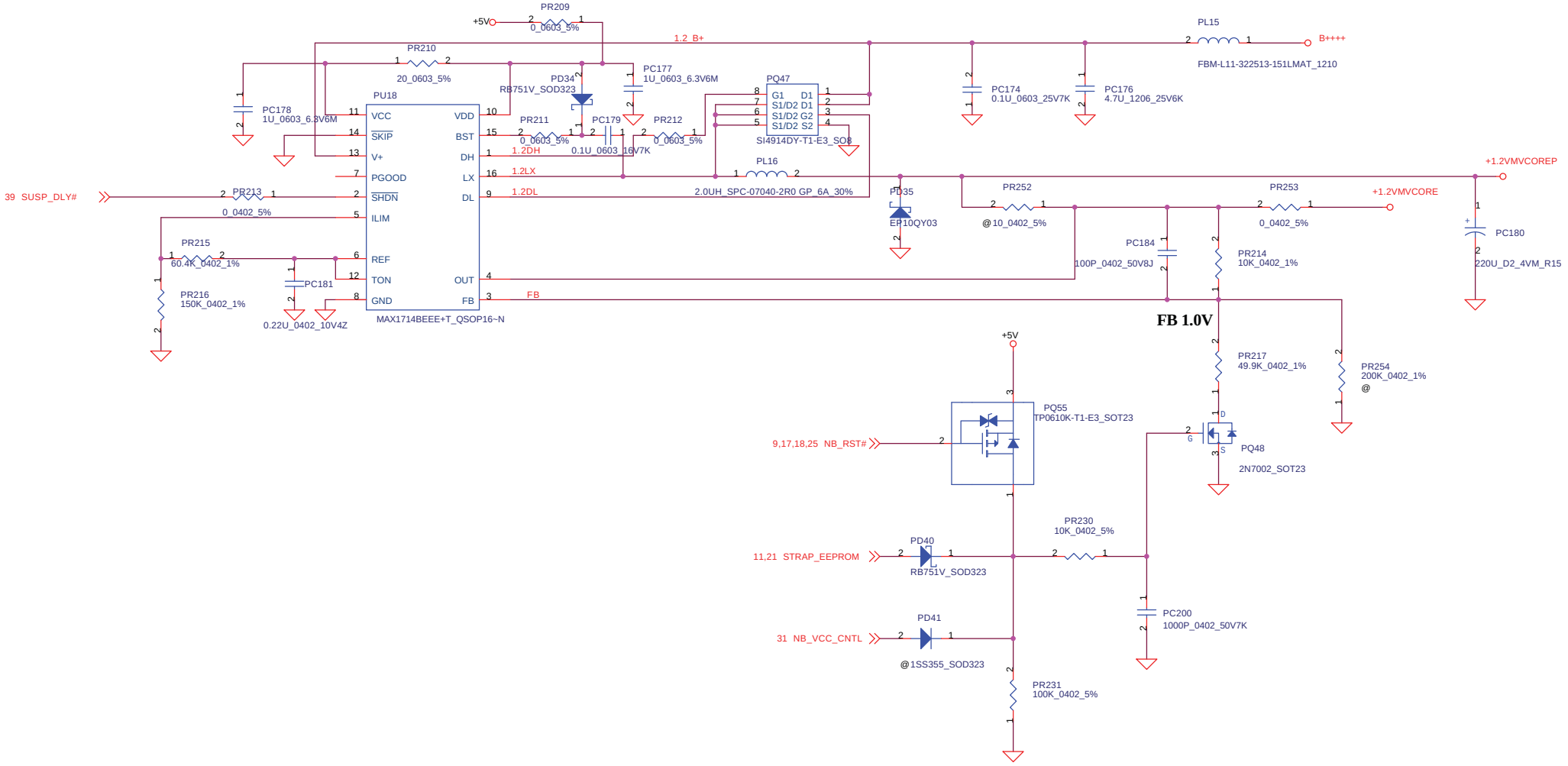

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	Pentium-M(1/3)	Nov. 19th	Compal	Correct circuit.	Add R1031	0.2
2	9, 17, 25	RS400MD-FSB/A-PCIE(1/4) SB400-PCIE/PCI/LPC/RTC(1/4) BCM5751M-GLAN	Nov. 19th	Compal	Correct net name	Easy to identify net connection between RS400MD and SB400/BCM5751M	0.2
3	8	CPU Decoupling/FAN(3/3)	Nov. 19th	Compal	U2.1 and U2.3 is short togather.	Correct net name of U2.3	0.2
4	21	Hardware Trap	Nov. 19th	Compal	Fix it to follow SB400 A31 request	Change the status of PCI_CLK2 to low	0.2
5	24	MINI_PCI SLOT-WLAN	Nov. 19th	Compal	Follow Compal standard design	Change the IRQ routing to IRQF# and IRQG#	0.2
6	18	P18-SB400-USB/AC97/MISC.(2/4)	Nov. 19th	Compal	Different power plane maybe cause some leakage.	Correct Power plane from +3valw to +3v to match USB_PHY_1.8v plane	0.2
7	25	BCM5751M-GLAN	Nov. 19th	Compal	For Debug	Reserve Pull-up R1030.	0.2
8	31	ENE-KB910L/TPM	Nov. 19th	Compal	Fix S5 boot function and sequence	Correct AUXS5_EN# and VGATE and VGATE_EC control type	0.2
9	32	BIOS/EE-Prom/TP/KB/SW	Nov. 19th	Compal	Re-assignt K/B ESD cap	Deleted C592.	0.2
10	33	DC TO DC	Nov. 22th	Compal	Follow M/E requirement	Deleted H16, H17, H23	0.2
11	11	RS400MD-DISPLAY(3/4)	Nov. 22th	Compal	LCD Backlight can't function.	Change the control signal from BLEN" U3.D7" to BLON" U3.A6.	0.2
12	22	IDE/CD_ROM Conn.	Nov. 22th	Compal	correct the Poly-fuse spec for HDD requirement.	Change the Poly-fuse from 1.1A to 1.8A	0.2
13	25 31	BCM5751M-GLAN ENE-KB910L/TPM	Nov. 22th	Compal	Reserved GPIO of KB910L for other function	Change the GLAN restet timing by A_RST# signal.	0.2
14	29	AC97 Codec AD1981B/MDC	Nov. 24th	Compal	MDC be changed.	Correct pin definition	0.2
15	16	ClockGen ICS951413	Nov. 24th	Compal	ICS951411 will function fail with CPU Speedstep	Change Clock Gen from ICS951411 to ICS951413	0.2
16		RS400MD & SB400	Nov. 24th	Compal	For Lead-free process	Change RS400MD & SB400 to Lead-Free part.	0.2
17	30	AMP./Audio Jack	Nov. 24th	Compal	To smooth the Cable routing	Swap Left and Right sound signals.--JSPK1	0.2
18	31	ENE-KB910L/TPM	Nov. 24th	Compal	Separate TPM to Module type	Removed TPM Chip and add JP23	0.2
19	23	USB/BlueTooth/FP	Nov. 25th	Compal	Bluetooth be changed	Correct connector" JP10" pin define and type.	0.2
20	32	BIOS/EE-Prom/TP/KB/SW	Nov. 25th	Compal	For M/E Requirement	Change the connecotr type" JPALM1" from Cable to FFC.	0.2
21	11	RS400MD-DISPLAY(3/4)	Nov. 25th	Compal	Reserved EEPROM" U49" debugging	Delete reserved circuit for PP phase	0.2
22	11	RS400MD-DISPLAY(3/4)	Nov. 25th	Compal	Reserved R508 for debugging	Delete R508 for PP phase	0.2
23	15	TV-OUT/LVDS/CRT	Nov. 25th	Compal	Reservd Resistors for LCD EDID	Update the R87, R88, R506, R507, R504 and R505 status for PP phase. Delete R1032 and R1049 at page 11	0.2
24			Nov. 25th	Compal	Reserved for PWR consumption measurement.	Delete R63, R189, JOPEN2, JOPEN3 and JOPEN4.	0.2
25	30	AMP./Audio Jack	Nov. 25th	Compal	Beep function fail	Correct Beep circuit	0.2
26	15	TV-OUT/LVDS/CRT	Nov. 25th	Compal	Lack of this part in vendor side	Change C907 from 0.1U_0402_25V4K to 0.1U_0805_50V.	0.2

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27	22	IDE/CD_ROM Conn.	Nov. 30th	NEC	For safety	Add F4" Fuse" for ODD	0.2
28	15	TV-OUT/LVDS/CRT	Dec. 1st	Compal	CRT Function abnormal	Change the D12 to correct library	0.2
29	23	USB/BlueTooth/FP	Dec. 6th	NEC	For Safety.	Add Poly-Fuse for B/T and F/P.	0.2
30	30	AMP./Audio Jack	Dec. 6th	Compal	Correct Buzzer drive circuit	Remove serial Resistors, Capacitor and Transtor. Change to Buffer to separate the signals and improve the driveing capacity.	0.2
31	6	Pentium-M(1/3)	Dec. 7th	Compal	Correct Thermal trip timing	Change R27 from 47k to 100k and fine-tune pwr sequnse between +1.5vs and VCCP.	0.2
32			Dec. 8th	EMI	PCI Clock will cause EMI issue.	Add AC-termination 10-ohm and 22pf for PCI Clocks.	0.2
33	30	AMP./Audio Jack	Dec. 8th	Compal	1. Follow Buzzer voltage rangeˊ 2V ~ 4Vˊ requirement 2. Follow NEC Audio team test result for HP signals.	1. Change the pull-up power to +3VS. 2. Change R1005 & R1006 from 0-ohm to 47-ohm	0.2
34	31	ENE-KB910L/TPM	Dec. 8th	Compal	Correct Extension IO control signal.	Change the control signal of U51A from KBA1 to KBA2	0.2
35	29	AC97 Codec AD1981B/MDC	Dec. 8th	EMI	EAPD will cause EMI issue with 197MHz	Change Resistor' R494' to Bead' L56'	0.2
36	23	USB/BlueTooth/FP	Dec. 9th	EMI	USB EMI problem	Add Common Choke for USB port	0.2
37	22	IDE/CD_ROM Conn.	Dec. 9th	EMI	Pin A24 ~ A26 will over 10dB for EMI	Add bypass capacitors' 1000p.	0.2
38	15	TV-OUT/LVDS/CRT	Dec. 10th	EMI	Reserved R to measure pwr consumption	Delete R488.	0.2
39	22	IDE/CD_ROM Conn.	Dec. 13th	NEC	For ODD Module Safety	Correct the Fuse with 3A for ODD	0.2
40	31	ENE-KB910L/TPM	Dec. 13th	Compal	For Power Play function	Reserved NB_VCC_CNTL for Power Play circuit.	0.2
41	22 33	IDE/CD_ROM Conn. DC TO DC	Dec. 13th	Compal	Correct cap power rating for B+_BIAS	Change cap from 0.1u_0402_16V to 0.1u_0805_50V.	0.2
42	18	P18-SB400-USB/AC97/MISC.(2/4)	Dec. 13th	Compal	Prevent leakage currect for EC_SI# and EC_SCI# signals.	Change these signals pull-up from +3V to +3VLAW.	0.2
43	32	BIOS/EE-Prom/TP/KB/SW	Dec. 30th	Compal	Update the Battery mode power-on circuit.	Un-pop. R422, R421, Q22, Q21, D33, D43, D44 and C598.	0.3
45	6	Pentium-M(1/3)	Jan. 11th	Compal	Improve thermal trip timing.	Change R32 from 75 to 10-ohm.	0.3
46	31	ENE-KB910L/TPM	Jan. 11th	Compal	Correct Extension buffer function	Swap AUX_S5EN and TRICKE signal. Move HDD_EN# from extension buffer, U50, to KB910L. Move A/B#USE signal to KB910L and delted EC_THERM.	0.3
47	31	ENE-KB910L/TPM	Jan. 12th	Compal	To save space and cost.	Change U51 from SN74LVC32APWR TSSOP14 to NC7SZ32P5X_NL SC70-5.	0.3
48	30	AMP./Audio Jack	Jan. 13th	Compal	To solve Int. Speaker GAIN issue.	Change the POWER source of R360 & R359 from +5VAMP to +5VS. +5VAMP is single Power plane.	0.3
49	24	MINI_PCI SLOT-WLAN	Jan. 13th	Compal	Correct net name for WL_OFF# signal.	Change the pull-up R, R1021, from D18.1 to D18.2. Correct the net name for WL_OFF# to prevent confuse.	0.3
50	32	BIOS/EE-Prom/TP/KB/SW	Jan. 14th	Compal	Follow NEC DPD R02 for DIP SW function	Remove USBSEL and CONFIG signals.	0.3
51	30	AMP./Audio Jack	Jan. 14th	NEC	To improve Audio Dolby quality.	Change the C997 & C998 to 2.2U.	0.3
52	08 22 33	CPU Decoupling/FAN(3/3) IDE/CD_ROM Conn. DC TO DC	Jan. 18th	POWER	To save cost for CPU Decoupling Caps. To Save Power consumption for Battery life. To Save Power consumption for Battery life.	Depopulated C29. Change R480 & R481 from 100k to 470k. Change R440 from 100K to 470K	0.3
53	27	R5C842-PCI/CARD BUS/OHCI	Jan. 19th	Compal	For Sn-Zn-Bi process.	Change Y5 from SJ124P5M500 to SJ124P5MF00 for Sn-Zn-Bi process.	0.3
54	23	USB/BlueTooth/FP	Jan. 20th	Compal	Solve USB leackage voltage problem.	Add Dis-charge circuit R46, R1, Q4 and Q12.	0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
27	23	USB/BlueTooth/FP	Jan. 21th	Compal	For EMI	Add Common Chock to solve the issue.	0.3
28	30	AMP./Audio Jack	Jan. 24th	Vendor	To prevent leakage from +AUD_VREF	Float JP16 pin6.	0.3
30	12	RS400MD-PWR/GND(4/4)	Jan. 26th	Compal	improve the +1.2VSA and +1.2VMCOORE be stability.	Add C1020 & C172 to solve +1.2VSA and +1.2VMCORE voltage drop issue.	0.3
31	08	CPU Decoupling/FAN(3/3)	Jan. 26th	Compal	To improve Battery Life when S4/S5 status.	Add Q56' SB570020000' and R68' SD028100100,Change Q52 to SB934430000.	0.3
32	18	SB400-USB/AC97/MISC.(2/4)	Jan. 26th	ATI	Work around for CKE# Glitch.	Add D21 & D22 with SC1H751H000.	0.3
33	8	RS400MD-FSB/A-PCIE(1/4)	Jan. 27th	NEC	Work around for CKE# Glitch.	Change R52 Value to 27K.	0.3
34	17	SB400-PCIE/PCI/LPC/RTC(1/4)	Feb. 16th	ATI	To solve SB400-A32 boot fail with PCIE I/F.	Change C263, C264, C265 and C266 from 0.1uf to 0.01uf.	1.0
35	31	ENE-KB910L/TPM	Feb. 23th	Compal	To by pass the ACIN to the EC	Add R71 and change D20 & R386 to @.	0.4
36	17	SB400-PCIE/PCI/LPC/RTC(1/4)	Feb. 23th	Compal	To improve Battery Life when S4/S5 status.	Change power source of U8.pin14 and R149.1 from +3VALW to +3VS	0.4
37	21	Hardware Trap	Feb. 23th	Compal	To improve Battery Life when S4/S5 status.	Change power source of U31F.pin14 and U53.pin5 from +3VALW to +3VS	0.4
38	31	ENE-KB910L/TPM	Feb. 23th	Compal	To improve Battery Life when S4/S5 status.	Change power source of R1053 from +3V_EC to +3VS	0.4
39	32	BIOS/EE-Prom/TP/KB/SW	Feb. 23th	Compal	To improve Battery Life when S4/S5 status.	Change power source of RP6 from +3V_EC to +3VS	0.4
40	9	RS400MD-FSB/A-PCIE(1/4)	Feb. 24th	ATI	To improve LAN performance.	Change LAN port from GPP0 to GPP2	0.4
41	18	SB400-USB/AC97/MISC.(2/4)	Feb. 24th	ATI	To improve LAN performance(For BIOS).	Add pull H & L to U7.A27(GPIO).	0.4
42	21	Hardware Trap	Feb. 25th	ATI	Strap on PCICLK5 has beed redefined	Pop R212 to pull low and unpop R199	0.4
43	18	SB400-USB/AC97/MISC.(2/4)	Feb. 25th	NEC	To improve LAN performance(For BIOS).	Add pull H & L to U7.D23(GPIO).	0.4
44	18	SB400-USB/AC97/MISC.(2/4)	Mar. 8th	NEC	To improve LAN performance(For BIOS-IRT).	Pop R160 & R167, unpop R159 & R168	0.5
45	8	RS400MD-FSB/A-PCIE(1/4)	Mar. 8th	Compal	Solve Fan noise	Deleted C911	0.5
46	21	Hardware Trap	Mar. 8th	ATI	Strap on PCICLK5 has beed redefined	Pop R199 to pull low and unpop R212	0.5
47	12	RS400MD-PWR/GND(4/4)	Mar. 8th	Compal	For voltage stable	Add C172	0.5
48	06	Pentium-M(1/3)	Apr. 7th	Compal	To solve S3 shut-down issue.	Add Diod D40, RB521S-30, to discharge Base voltage when shut-down.	2.0
49	22	IDE/CD_ROM Conn.	Apr. 28th	NEC	To solve ODDLED abnormal light.	Change the R236 power source from +5VODD to +5VS.	2.0
1	18	SB400-USB/AC97/MISC.(2/4)	May. 5th	NEC	To improve LAN performance(For BIOS).	Change pull H R159	0.1
2	17	SB400-PCIE/PCI/LPC/RTC(1/4)	May. 5th	Compal	Change PCI_CLK trace for EMI	Change R141, 142, 143, 1011 size from 0603 to 0402	0.1
3	31	ENE-KB910L/TPM	May. 5th	Compal	Add CLKRUN	Reserve 1K resistance pull down	0.1
4	22	IDE/CD_ROM Conn.	May. 5th	Compal	To solve ODDLED abnormal light.	Change R236 from 100K to 8.2K	0.1
5	6	Pentium-M(1/3)	Jun. 16th	Compal	To solve can't boot after high loading test..	Change R227 power source from VCCP to CPUCORE	0.2
6	18	SB400-USB/AC97/MISC.(2/4)	Jun. 16th	NEC	To meet ATi spec(USB_RCOMP)	Change R169 from 10K to 11.8K	0.2
7	27	R5C842-PCI/CARD BUS/OHCI	Jul. 21th	Compal	RICOH recommand	Change R452 from 0 to 10K	1.0
8	9	RS400MD-FSB/A-PCIE(1/4)	Jul. 21th	ATI	ATI recommand	1.Change R51 from 10K_0402_5% to 10K_0402_1% 2.Change R53 from 100_0402_1% to 82.5_0402_1% 3.Change R54 from 8.2K_0402_1% to 8.25K_0402_1% 5.Change C130,C132,C134,C136,C138,C140,C142,C144,C146,C148,C150,C151,C152,C153,C154,C156,C157,C158,C159 from 0.1U_0402_16V4Z to 1U_0402_6.3V4Z	1.0

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42	Optional VGA MVCORE Power	Dec. 07th	Compal	In order to use ATI's new power saving feature of Power Play, the VGA chip core Voltage has to to adjusted down to 1.0V. A new power regulator circuit is added using MAX1714 to have high efficiency at light load to make this feature able to prolong battery life.	Add optional PC174, PC176, PC177, PC178, PC179, PC180, PC181, PC184, PD34, PD35, PL15, PL16, PQ47, PQ48, PQ49, PR209, PR210, PR211, PR212, PR213, PR214, PR215, PR216, PR217, PR218, PR219, PU18. Add PC168 , PC169 to replace PC143 (deleted). Add PJP16, PJP17.	0.2
2	34	PWR DCIN / Precharge	Dec. 07th	Compal	To prevent adaptor plug in or plug out glitches.	Added PC167 (1000P_0402_50V7K).	0.2
3	34	PWR DCIN / Precharge	Dec. 07th	Compal	To adjust adaptor input precharge Voltage and Battery input precharge Voltage thresholds.	Change PR17 to 127K 1%, PR21 to 340K 1%, PC14 to 0.1uF.	0.2
4	36	Charger	Dec. 07th	Compal	Change adaptor isolation MOSFET turn-on turn-off delay time for proper multiple power source hot swap.	Change PQ11 to DTC115EUA. Add PD31, PR214, PC170.	0.2
5	36	Charger	Dec. 07th	Compal	To prevent power on single time short duration LED flashing by introducing delay in V_BIAS.	Add in PR205, PR206, PR207, PC171, PD36, PQ45, PQ44.	0.2
6	37	Battery Select	Dec. 07th	Compal	To provide proper multiple power source hot swap (main and second battery), component values are changed and extra components are added for extra delay to do "Break" before "Make" function.	Added PD33, PD32, PC173, PC172, PQ46, PC208. Change PC44, PC46 to 47pF. Change PR79, PR88 to 100K 5%.	0.2
7	39	+1.2VSP & +1.8VALWP	Dec. 07th	Compal	Correct wrong pin connection.	Change PQ28 pin 4 and pin 1,2,3 connection.	0.2
8	40	0.9VSP/VCCPP	Dec. 07th	Compal	Correct wrong pin connection.	Swap PQ42 pin 1 and pin 3 connection.	0.2
9	41	CPU_CORE	Dec. 07th	Compal	Correct CPU Vcore load line.	Change PR159 and PR153 from 3K to 2K 1%.	0.2
10	34	PWR DCIN / Precharge	Dec. 10th	Compal	Change to horizontal intertion type on-board adaptor connector jack.	Change PJP1 to use "SINGA_2WA-8291T041".	0.2
11	38	3.3V/5V	Dec. 10th	Compal	Change to use lower height Inductor to fit into low height area (5.5A rating is still > 4A requirement).	Change PL8 to use TOKO part: "4.7UH_D104C-919AS-47M_5A_20%".	0.2
12	35, 36, 37	CPU OTP Page, Charger Page, and Battery Select Page.	Dec. 13th	Compal	To save power in S4, change PU3, PU5, and PU7 power to be powered from +5VL (not Vs).	Change PU3, PU5, and PU7 pin 8 to VL net. Add PC210 to VL net close to PU5 pin 8.	0.2
13	42	Optional VGA MVCORE Power	Dec. 13th	Compal	To change Voltage control pin active polarity on ATI Power Play.	Add PR230, PR231, PQ50, PC200, PD40, and PD41. uninstall PD41. Delete PQ49, PR218, PR219.	0.2
14	38	3.3V/5V	Dec. 14th	Compal	Add option ckt to let +3VALW always on when batteries are in bay. Add option ckt to let +5VALW to be independantly controlled by ECON signal.	Add PR232, PR233, PR234. Uninstall PC148, PR105, pr233, and PU16.	0.2
15	34	PWR DCIN / Precharge	Dec. 14th	Compal	Add option ckt to let +3VALW always on when batteries are in bay.	Add PR235. Delete PC8, PR12, PR14, and PQ1.	0.2
16	34	PWR DCIN / Precharge	Dec. 14th	Compal	Change pre-charge time to be shorter by use smaller value.	Change PR9, PR11, PR13 to 1K.	0.2
17	40	0.9VSP/VCCPP	Dec. 14th	Compal	With option ckt to let +3VALW always on when batteries are in bay, old circuit components should be uninstalled.	Uninstall PC152, PR201, PQ43, PQ42, PR199, PC149, PC15, PU17, PC150. Add PJP20. Add PR236, but uninstall it.	0.2
18	39	+1.2VSP & +1.8VALWP	Dec. 22th	Compal	Add delay circuit requested by HW to form SUSP_DLY# signal for 1.2V and 1.0/1.2V regualtors enable control.	Add PR220, PR222, PC185, PQ50.	0.2
19	36	Charger	Dec. 22th	Compal	Add control signal to prevent Voltage droop when adaptor is inserted. Change resistor value to slow down in-rush current.	Add PD43. Change PR43=33K 5%, and unpopulate PR34.	0.3
20	34	PWR DCIN / Precharge	Dec. 22th	Compal	Add control signal to prevent Voltage droop problem when adaptor is inserted.	Added PR249=4.7k. Changed PC13=1000pF, PC167 = 0.1uF.	0.3

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21	34	PWR DCIN / Precharge	Dec. 30th	Compal	To provide full protection in wrong adaptor over-Voltage or Battery charger over-Voltage conditions, A switch is inserted into Pre-charge path to stop pre-charge during over-Voltage.	Deleted PR10 , and added in PR241, PR242, PR247, PQ57, PQ58, and PQ61.	0.3
22	36	Charger	Dec. 30th	Compal	To provide better protection for wrong adaptor over-Voltage, a threshold protection circuit is added on ACOFF# control signal and PQ5 control signal.	Added PQ59, PQ60, PR244, PR245, and PR246. Changed PR36, and PR38. Changed PU5A pin8 to "VIN" net.	0.3
23	35	CPU OTP	Dec. 30th	Compal	To improve shutdown mode quiescent current, change CPU OVP circuit resistors to have higher value.	Changed PH1 to 100K (TH11-4H104FT), PR30, 0R28, PR29, PR31, PR25, and PR26 value to larger values to reduce shutdown mode current. Changed PQ4 to RHU002N06 and PC18 to 1000pF.	0.3
24	39	+1.2VSP & +1.8VALWP	Dec. 30th	Compal	To correct the polarity of control signal for 1.0V/1.2V regualtor for VGA.	Deleted PR221, PQ51. Changed "SUSP_DLY" connection to PQ50 pin1.	0.3
25	36	Charger	Jan. 04th	Compal	To save more power in S3, S4, S5 modes and increase switching speed during power source hot swaping.	Depopulated PR34, PR59, and PR61. Changed PR43, PR70, and PR71 to 2.2K.	0.3
26	41	CPU_CORE	Jan. 13th	Compal	Changed back CPU load line resistor value.	Change PR159 and PR153 from 2K to 3K 1%.	0.3
27	40	0.9VSP/VCCPP	Jan. 14th	Compal	De-populate paralleled polymer capacitor on 1.05V rail (H/W has one already).	De-populate PC101.	0.3
28	42	Optional VGA MVCORE Power	Jan. 20th	Compal	North Bridge Chip Core Voltage on the lower band change to higher band.	Changed PR217 to 44.2K 1%.	0.3
29	34	PWR DCIN / Precharge	Jan. 20th	Compal	To save S4 mode current, Change PU1 pin8 power to VL.	Changed PR22=330K 1%, PR21=169K 1%, PR17=287K 1%, PR16=820K 1%, PR15 to 47K 5%. PU1 pin6 to pin2. PU1 pin8 to VL, Deleted PR24, and PC14.	0.3
30	39	+1.2VSP & +1.8VALWP	Jan. 24th	Compal	Add remote sense resistors.	Added PR250, PR251.	0.3
31	42	Optional VGA MVCORE Power	Jan. 24th	Compal	Add remote sense resistors.	Added PR252, PR253.	0.3
32	41	CPU_CORE	Jan. 24th	Compal	To prevent in-phase operation due to un-predicted noise problems.	Added/reserved PC211, PC212, but not install them.	0.3
33	38	3.3V/5V	Jan. 24th	Compal	To reduce temperature rise on NB skin.	Changed PL5, PL6 to use TOKO inductors.	0.3
34	34 38 39 41 36	PWR DCIN / Precharge 3.3V/5V +1.2VSP & +1.8VALWP CPU_CORE Charger	Jan. 24th	NEC	Add fuse at input trace for each DC/DC circuit and charger ouput trace.	Changed PF1 to 12A and add PF2 for charger output trace, PF3 for 3V/5V, PF4 for 1.2VSP/1.8VALWP/1.2VMVCOREP, PF5forCPU_CORE.	0.3
35	36	Charger	Jan. 28th	NEC	Add fuse at batery input trace.	Del PF2 and add PF6 and PF7 at PBJ1 pin 1 and PBJ2 pin 1.	0.3
36	39 42	+1.2VSP & +1.8VALWP Optional VGA MVCORE Power	Jan. 28th	Compal	System hang up at running 3DMark, chang +1.2VSP and +1.2VMVCOREP to remote sense.	De-populate PR251 and in series with PR250 to +1.2VS . De-populate PR252 and in series with PR253 to +1.2VMVCORE .	0.3
37	34	PWR DCIN / Precharge	Fab. 24th	Compal	To reduce power consumption at S4 mode.	Reserve PR256 to as a volatagr divider with PR4.	0.4
38	38	3.3V/5V	Fab. 24th	Compal	To change +3VALWP and +5VALWP sequence, let +3VALWP turns on after +5VALWP.	Add PR255 and PC213 to delay the turn on sequence of +3VALWP.	0.4

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39	34	PWR DCIN / Precharge	Mar. 8th	Compal	To change RTC battery charger current to meet RTC battery spec.	Change PR19 and PR20 to 560 Ohm.	0.4
40	34 42	PWR DCIN / Precharge Optional VGA MVCORE Power	Mar. 8th	Compal	To change 1.2VMVCORE nomial voltage level and add output capacitor to meet spec.	Populate PC169 with 4.7U and change PR217 to 49.9K Ohm.	0.4
41	35	PWR CPU OTP	Mar. 8th	Compal	To change OTP triggle point at 86 degree C for thermal team request.	Change PR28 to 200K Ohm.	0.4
42	36	PWR-CHARGER	Mar. 8th	Compal	To faster the CP protection.	Change PC26 to 1500PF.	0.4
43	38	PWR-+1.2VSP & +1.8VALWP	Mar. 8th	Compal	To decreace +1.2VSP OCP point.	Change PR124 to 61.9K Ohm and PR125 to 39.2K Ohm.	0.4
44	42	Optional VGA MVCORE Power	Mar. 8th	Compal	To increace +1.2VMVCORE OCP point.	Change PR126 to 150K Ohm.	0.4
45	42	Optional VGA MVCORE Power	Mar. 11th	Compal	To increace +1.2VMVCORE 1.2V and 1.0V switch design margine.	Change PD40 to RB751V and PR231 to 100K Ohm.	0.4
46	38	3.3V/5V	Mar. 16th	Compal	To change +3VALWP and +5VALWP sequence, let +3VALWP turns on after +5VALWP.	Change PR255 to 15K Ohm and PC213 to 0.1u F.	0.5
47	34 38	PWR DCIN / Precharge 3.3V/5V	Mar. 29th	Compal	To solve can't power on when remove the AC outlet without battery	Change PR16 to 1M Ohm , PR21 to 162K Ohm ,PR22 to 287K Ohm , PC13 to 0.1UF , PC12 to 100PF and PD21 to SKUL30-02AT.	0.5
48	37	Battery Select	Mar. 29th	Compal	To solve can't power on when discharge battery to shut down mode	Change PR81 to 499K Ohm , PR90 to 499K Ohm and PQ22 to RHU002N06.	0.5
49	37	Battery Select	Mar. 29th	Compal	To solve can't charge when discharge battery to shut down mode	Change PR80 to 27K Ohm and PR89 to 27K Ohm.	0.5
50	41 40	CPU_CORE 0.9VSP/VCCPP	Apr. 28th	Compal	To reserve VR_ON control signal for +VCCPP and change CPU_CORE enable signal pull down resistor to capacitor.	Add PR257 and change PR155 to PC214	2.0
51	38	3.3V/5V	May. 10th	Compal	To solve no Power issue on Lavie and VersaPro MP status.	Change PC68 and PC72 to 150U 6.3V 18mOhm UD type and change PQ24 to SI481-DY-T1-E3	2.0