Compal Confidential

KBYF0 Schematics Document

AMD Griffin Processor with RS780M+SB700

(With ATI MXM/B)

2009-01-22

REV:0.3

ZZZ1

PCB

DA60000B600-*

Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

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Title: Cover Page

Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 1 of 46

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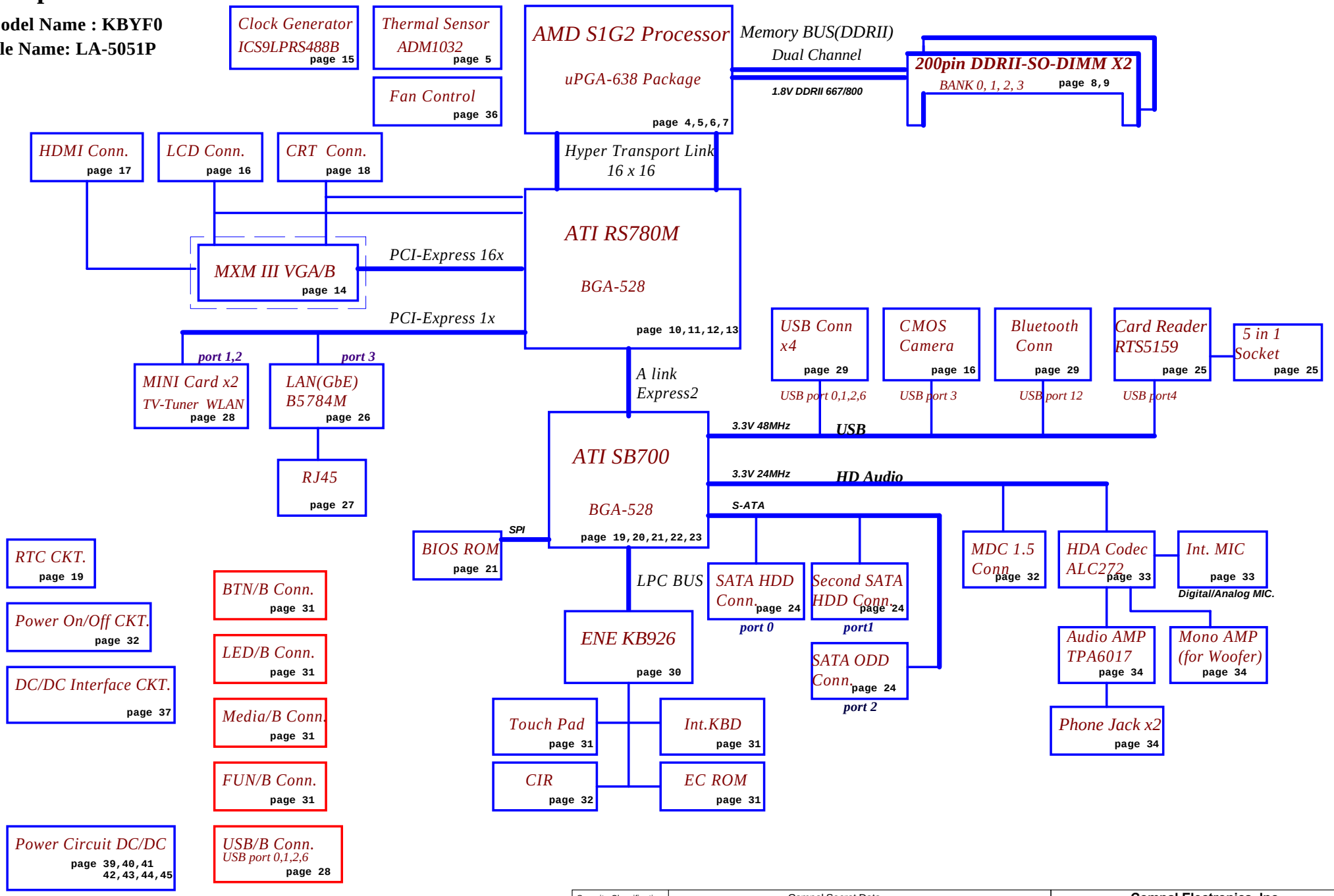
Model Name : KBYF0
File Name: LA-5051P



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Title: Block Diagrams

Size	Document Number	Rev
B	KBKC0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 2 of 46

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.05V switched power rail	ON	OFF	OFF
+1.2V_HT	1.25V switched power rail	ON	OFF	OFF
+NB_CORE	1.0V~1.1V switched power rail for NB VDDC	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA and MXM/B	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
No PCI device			

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
MXM GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
CPU SB	1001 101X b

SB700 SM Bus 0 address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Minicard	
Minicard	

SB700 SM Bus 1 address

Device	Address
Lan	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
* 2	0.3 0.4 1.0
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@

PROJECT ID Table

Board ID	PROJECT
0	KBKC0 (SJM70)
1	KBYF0 (SJV70)
2	
3	
4	
5	
6	
7	

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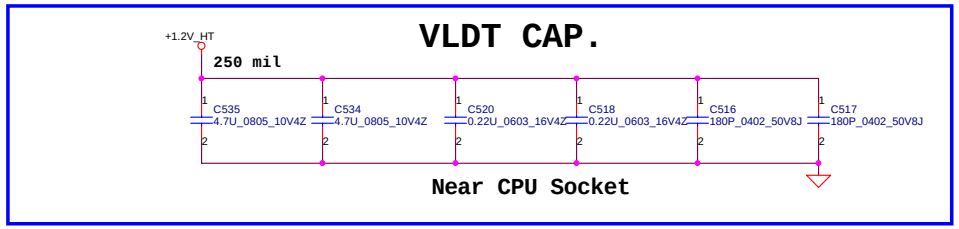
Title: Notes List

Size: B | Document Number: KBYF0 LA-5051P | Rev: 0.3

Date: Tuesday, February 03, 2009 | Sheet 3 of 46



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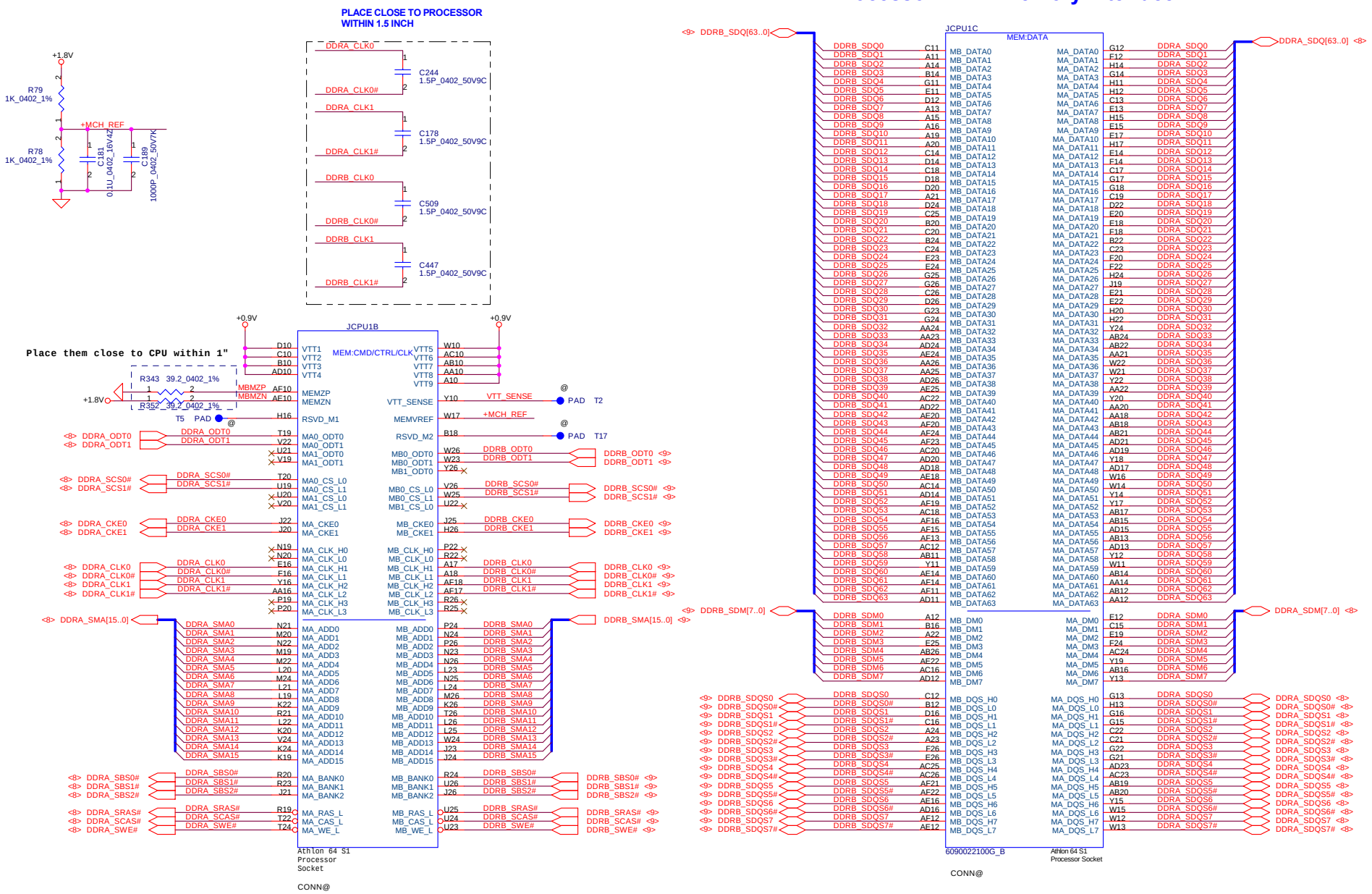
Compal Electronics, Inc.			
Title: AMD CPU S1G2 HT I/F			
Size: Custom	Document Number: KBYF0 LA-5051P		Rev: 0.3
Date: Tuesday, February 03, 2009	Sheet 4 of 46		

Processor DDR2 Memory Interface



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Compal Electronics, Inc.

Title: **AMD CPU S1G2 DDRII I/F**

Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 5 of 46

A:Need to re-Link "SGN00000200"

+2.5VS

+2.5VDDA VDDA=300mA

L33 FBM_L11_201209_300L_0805

C282 150U_D2_6.3VM

4.7U_0805_10V4Z C264 C255 3300P_0402_50V7K C261 0.22U_0603_16V4Z

<BOM Structure>

JCPU1D

6090022100G_B

<15> CLK_CPU_BCLK C531 3900P_0402_50V7K CPU_CLKIN_SC_P CPU_CLKIN_SC_N

R409 169_0402_1%

<15> CLK_CPU_BCLK# C532 3900P_0402_50V7K

<11> CPU_LDT_REQ#

Address:100_1100

Place close to CPU wihtin 1.5"

LDT_RST# H_PWRGD LDT_STOP# CPU_LDT_REQ# CPU_SIC CPU_SID

R356 1K_0402_5%

R82 44.2_0402_1% CPU_HTREF0

R86 44.2_0402_1% CPU_HTREF1

+1.2V_HT

<44> CPU_VDD0_FB_H CPU_VDD0_FB_L

<44> CPU_VDD1_FB_H CPU_VDD1_FB_L

CPU_DBRDY CPU_TMS CPU_TCK CPU_TRST# CPU_TDI

T10 PAD CPU_TEST23_TSTUPD

T27 PAD CPU_TEST18_PLLTEST1

T28 PAD CPU_TEST19_PLLTEST0

TEST25_H TEST25_L

T21 PAD CPU_TEST21_SCANEN

T22 PAD CPU_TEST20_SCANCLK2

T23 PAD CPU_TEST24_SCANCLK1

T24 PAD CPU_TEST22_SCANSHIFTEN

T25 PAD CPU_TEST12_SCANSHIFTENB

T26 PAD CPU_TEST27_SINGLECHAIN

R418 0_0402_5%

CPU_CLKIN_SC_P CPU_CLKIN_SC_N

CPU_SVC CPU_SVD

CPU_THERMTRIP# CPU_PROCHOT# CPU_MEMHOT#

THERMDC_CPU THERMDA_CPU

CPU_VDDNB_FB_H CPU_VDDNB_FB_L

CPU_DBREQ# CPU_TDO

CPU_TEST28_H_PLLCHRZ_P CPU_TEST28_L_PLLCHRZ_N

route as differential as short as possible testpoint under package

CPU_TEST17_BP3 CPU_TEST16_BP2 CPU_TEST15_BP1 CPU_TEST14_BP0

CPU_TEST10

CPU_TEST29_H_FBCLKOUT_P CPU_TEST29_L_FBCLKOUT_N

CPU_TEST18_PLLTEST1 CPU_TEST19_PLLTEST0 CPU_TEST22_SCANSHIFTEN

R531 R532 R533 300_0402_5%

+1.8V sense no support

+1.8V

R364 10K_0402_5%

R358 300_0402_5%

Q32 MMBT3904_NL_SOT23-3

R335 @0_0402_5% MAINPWON

R334 0_0402_5% H_THERMTRIP#

MAINPWON <38,39>

H_THERMTRIP# <20>

R357 300_0402_5%

H_PROCHOT# R370 0_0402_5% H_PROCHOT# <19>

R353 300_0402_5%

+CPU_CORE_NB

R101 10_0402_5%

R106 10_0402_5%

Close to CPU

+1.2V_HT R337 0_0402_5%

CPU_TEST10

0718 AMD --> 1K ohm

R415 1K_0402_5%

R416 1K_0402_5%

CPU_TEST20_SCANCLK2 R537 300_0402_5%

CPU_TEST21_SCANEN R538 300_0402_5%

CPU_TEST24_SCANCLK1 R539 300_0402_5%

CPU_TEST23_TSTUPD R535 300_0402_5%

+CPU_CORE_0

R92 10_0402_5%

R95 10_0402_5%

Close to CPU

+CPU_CORE_1

R80 10_0402_5%

R81 10_0402_5%

+1.8VS

R420 300_0402_5%

<19> LDT_RST# C554 0.01U_0402_16V7K

R419 300_0402_5%

<19> H_PWRGD C553 0.01U_0402_16V7K

R113 300_0402_5%

<11,19> LDT_STOP# C245 0.01U_0402_16V7K

R108 300_0402_5% R107 300_0402_5%

TEST25_H TEST25_L

R98 300_0402_5% R105 300_0402_5%

CPU internal thermal sensor

C436 0.1U_0402_16V4Z

+3VS

R351 20K_0402_5%

R360 34.8K_0402_1%~N

2.09V for Gate

R361 390_0402_5%

<20> CPU_SID_SB R564 0_0402_5% CPU_SID

Q31 FDV301N_NL_SOT23-3

R567 0_0402_5% EC_SMB_DA1 <14,30,38>

R365 390_0402_5%

<20> CPU_SIC_SB R565 0_0402_5% CPU_SIC

Q30 FDV301N_NL_SOT23-3

R569 0_0402_5% EC_SMB_CK1 <14,30,38>

EC is PU to 5VALW

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

+3VS C446 0.1U_0402_16V4Z

C449 3300p for tigris

C449 2200P_0402_50V7K

2200p change to 1000p for ADT7421

U27 ADM1032ARMZ_MSOP8

THERMDA_CPU THERMDC_CPU

EC_SMB_CK2 EC_SMB_CK2 <30>

EC_SMB_DA2 EC_SMB_DA2 <30>

Address:100_1101

JP29 ACES_85201-1005N

CPU_DBREQ# CPU_DBRDY CPU_TCK CPU_TMS CPU_TDI CPU_TRST# CPU_TDO HDT_RST#

HDT Connector

JP1 SAMTEC_ASP-68200-07

R112 R115 R118 R119 220_0402_5%

300_0402_5%

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

R93 0_0402_5%

U8 @NC7SZ08P5X_NL_SC70-5

LDT_RST# SB_PWRGD <20,32>

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Title: AMD CPU S1G2 CTRL

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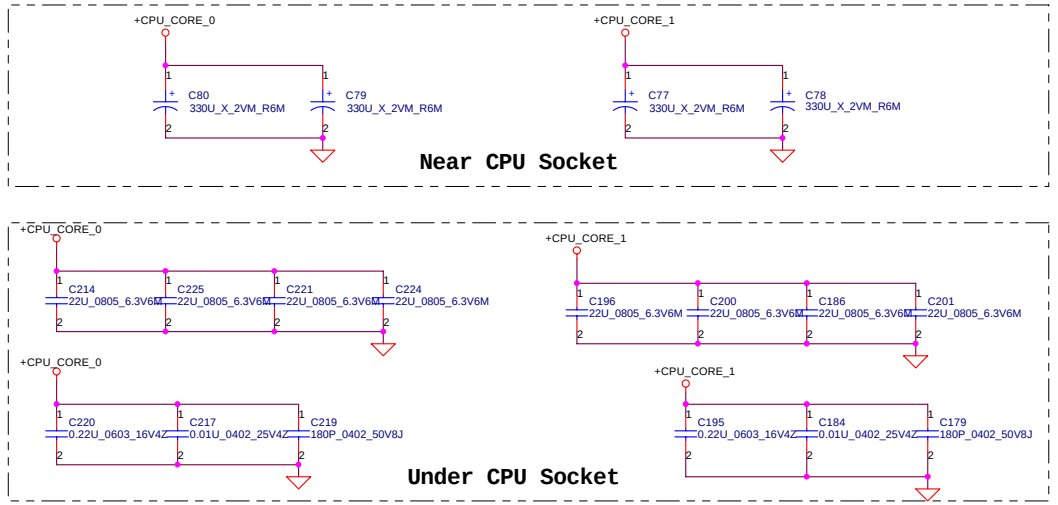
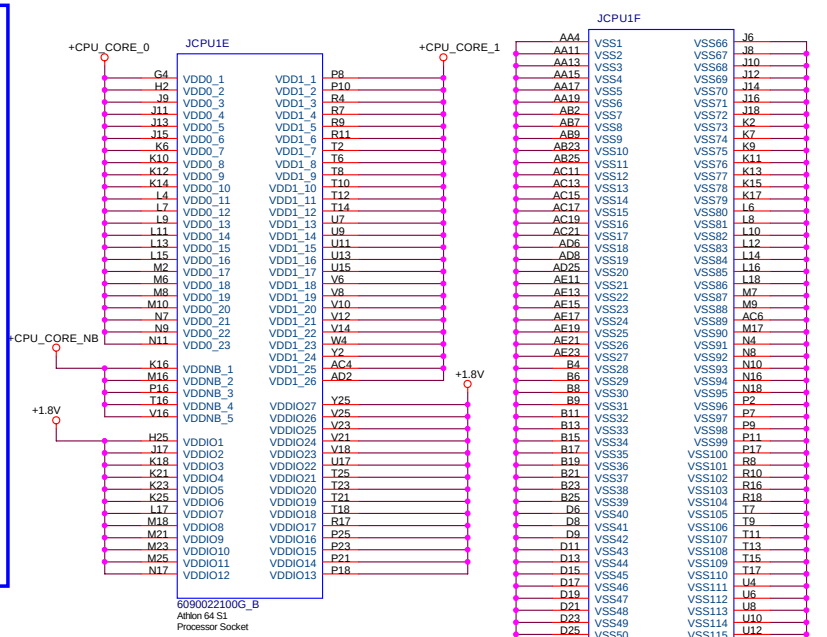
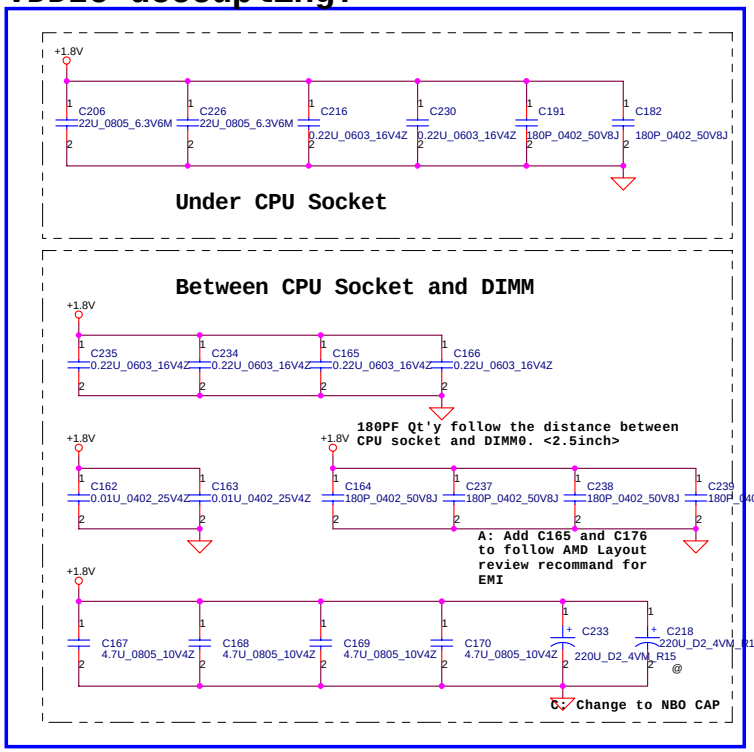
Date: Tuesday, February 03, 2009 | Sheet 6 of 46

VDD(+CPU_CORE) decoupling.

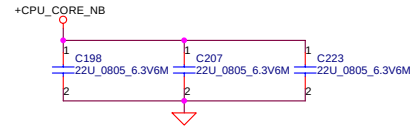




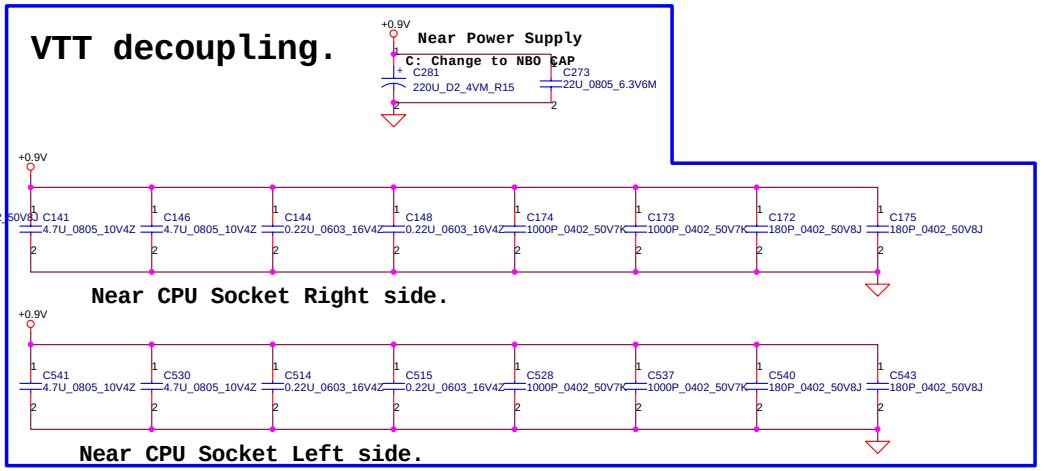
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.



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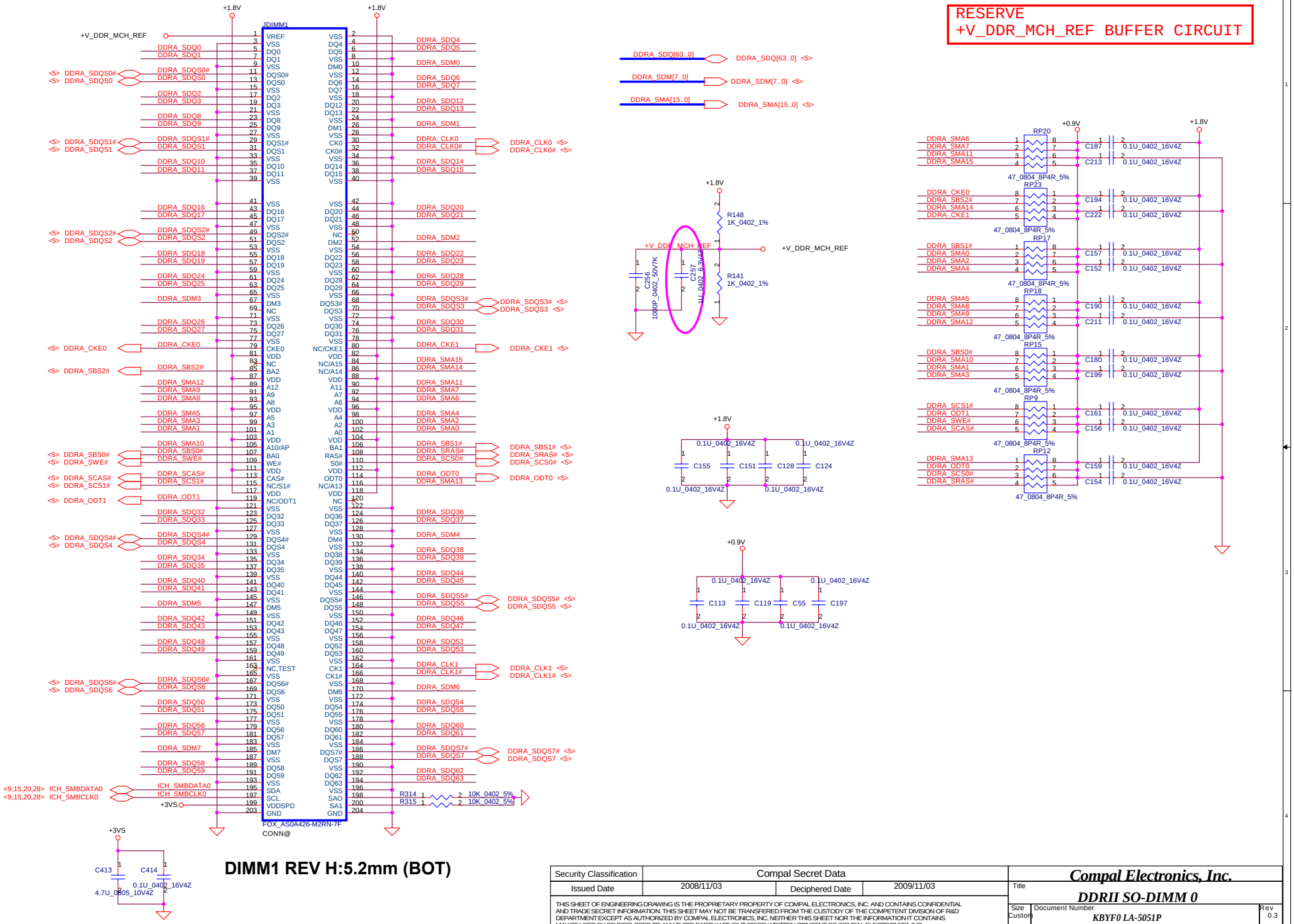
Compal Electronics, Inc.

Title: AMD CPU S1G2 PWR & GND

Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 7 of 46



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Compal Electronics, Inc.			
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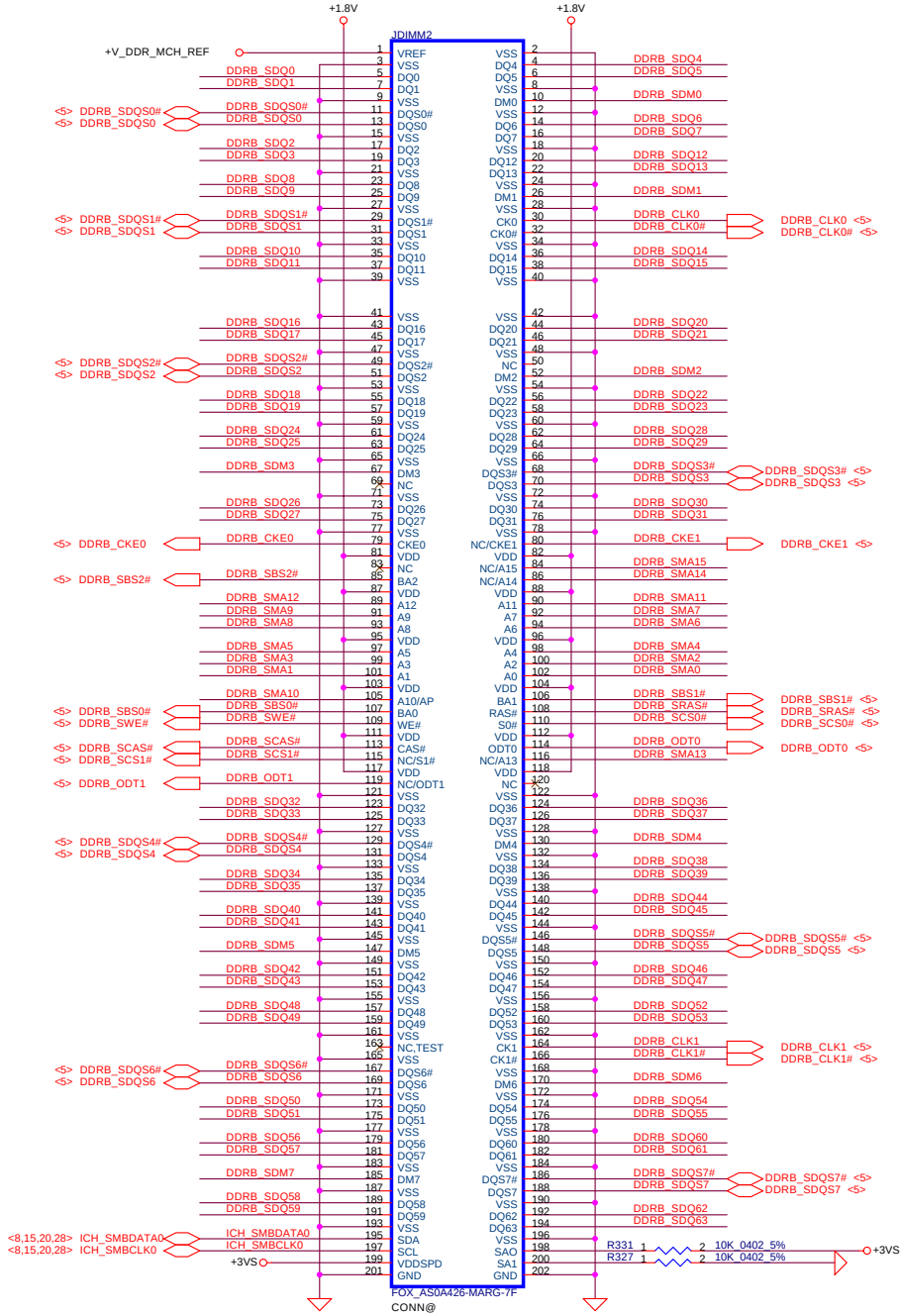
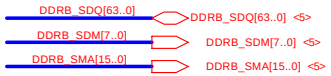
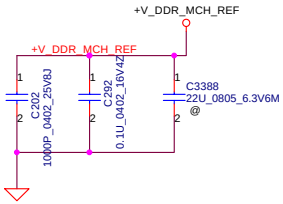
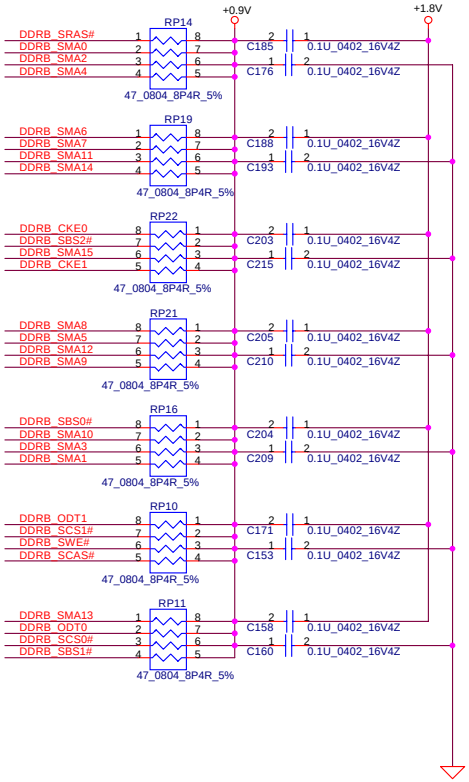
Size: Custom	Document Number: KBYF0 LA-5051P		Rev: 0.3
Date: Tuesday, February 03, 2009	Sheet 8 of 46		



DIMM1 REV H:9.2mm (BOT)







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Title: DDRII SO-DIMM 1

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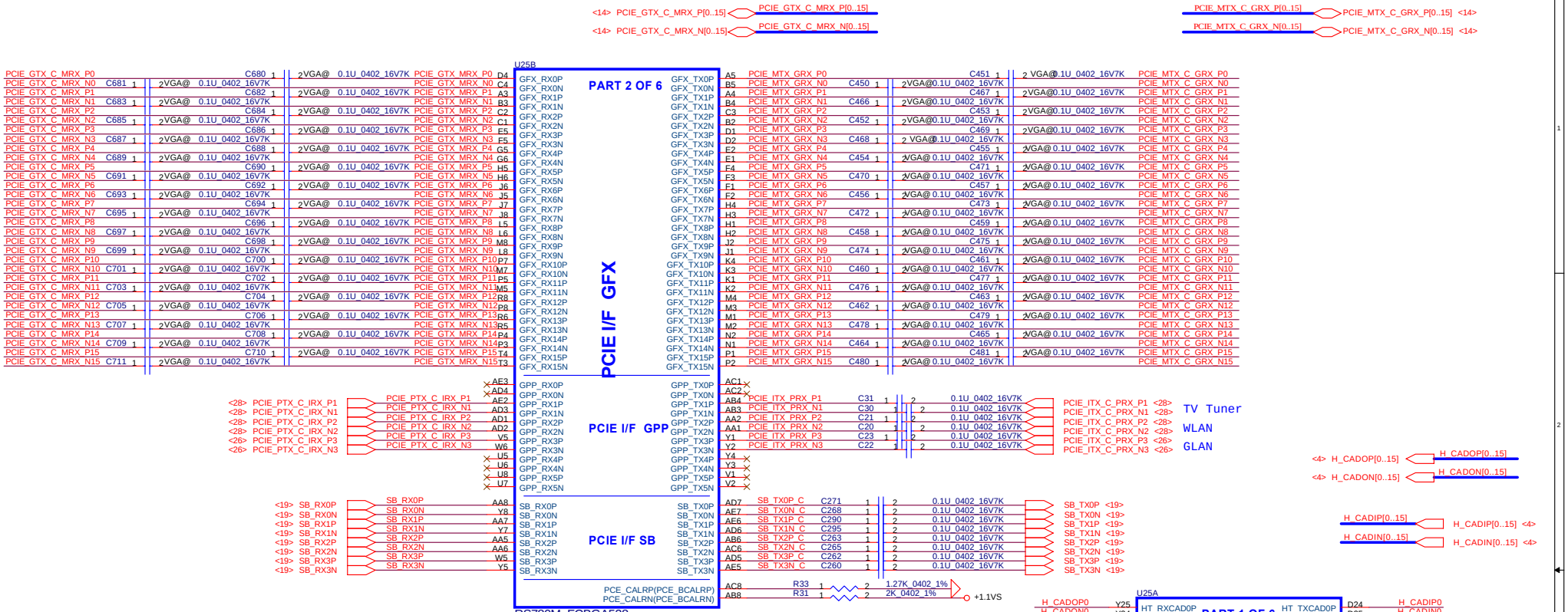
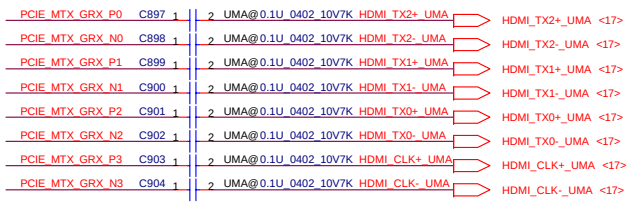
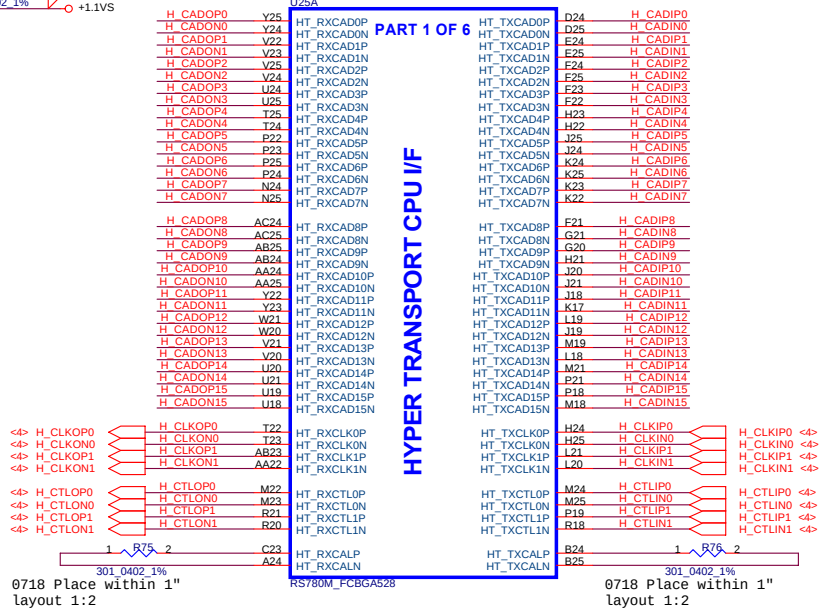
Date: Tuesday, February 03, 2009 | Sheet 9 of 46



RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1





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Title: **RS780-HT/PCIE**

Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 10 of 46

140

For RS780M A13

AVDD=100mA

R540 1k for RS880M

Strap pin

Strap pin

Strap pin

NB temp to SB

U25C

PART 3 OF 6

RS780M_FCBGA528

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Title: **RS780 VEDIO/CLK GEN**

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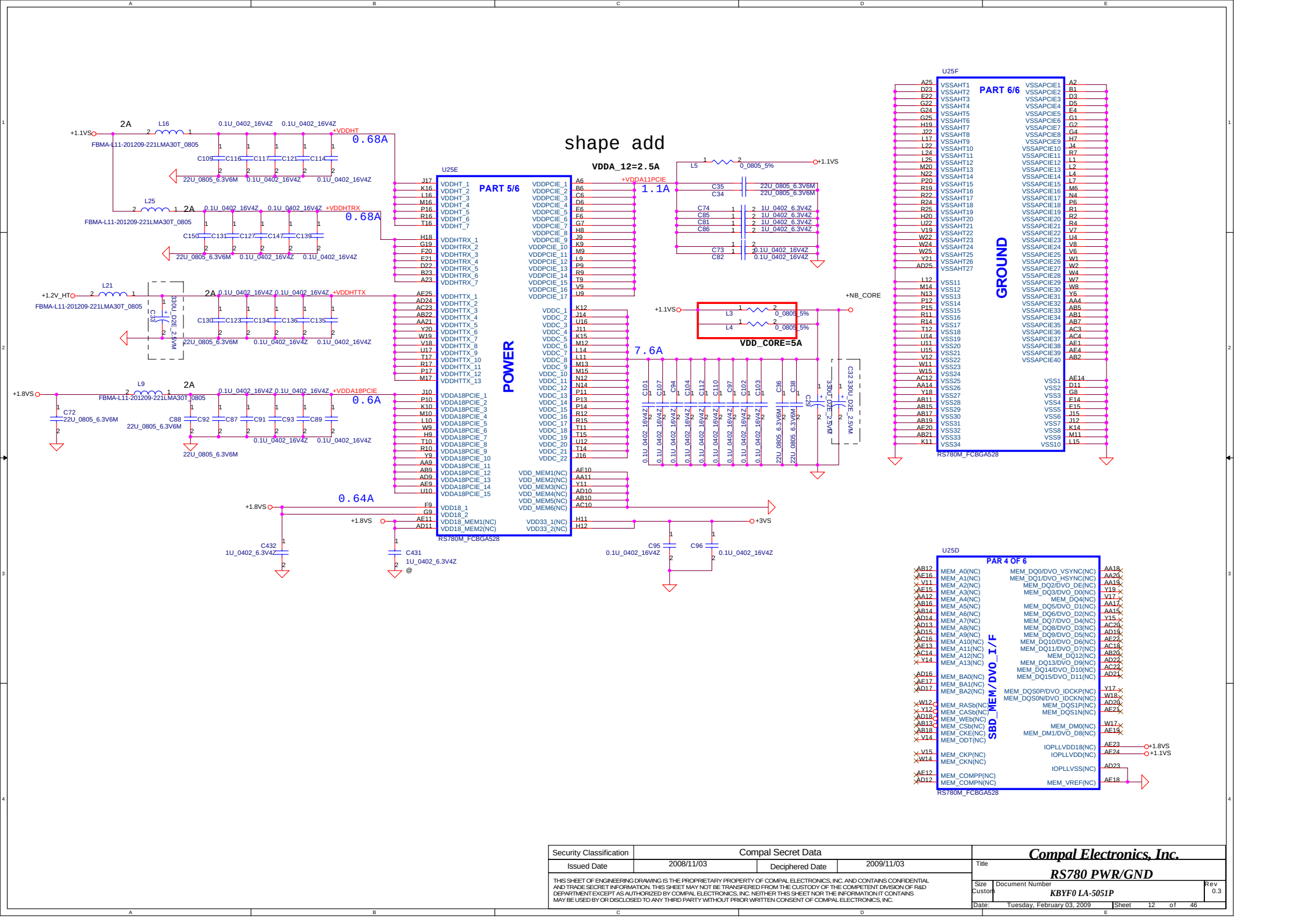
Date: Tuesday, February 03, 2009 | Sheet 11 of 46



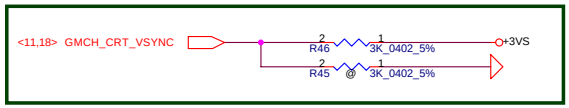
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: **RS780 PWR/GND**

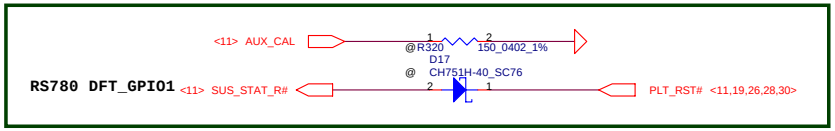
Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 12 of 46



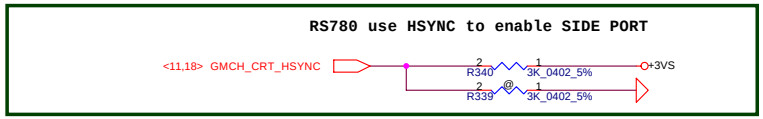
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)
```



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```



RS780 use HSYNC to enable SIDE PORT

```
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
0.   Enable (RS780)
1 :  Disable(RS780)
```

Security Classification	Compal Secret Data		
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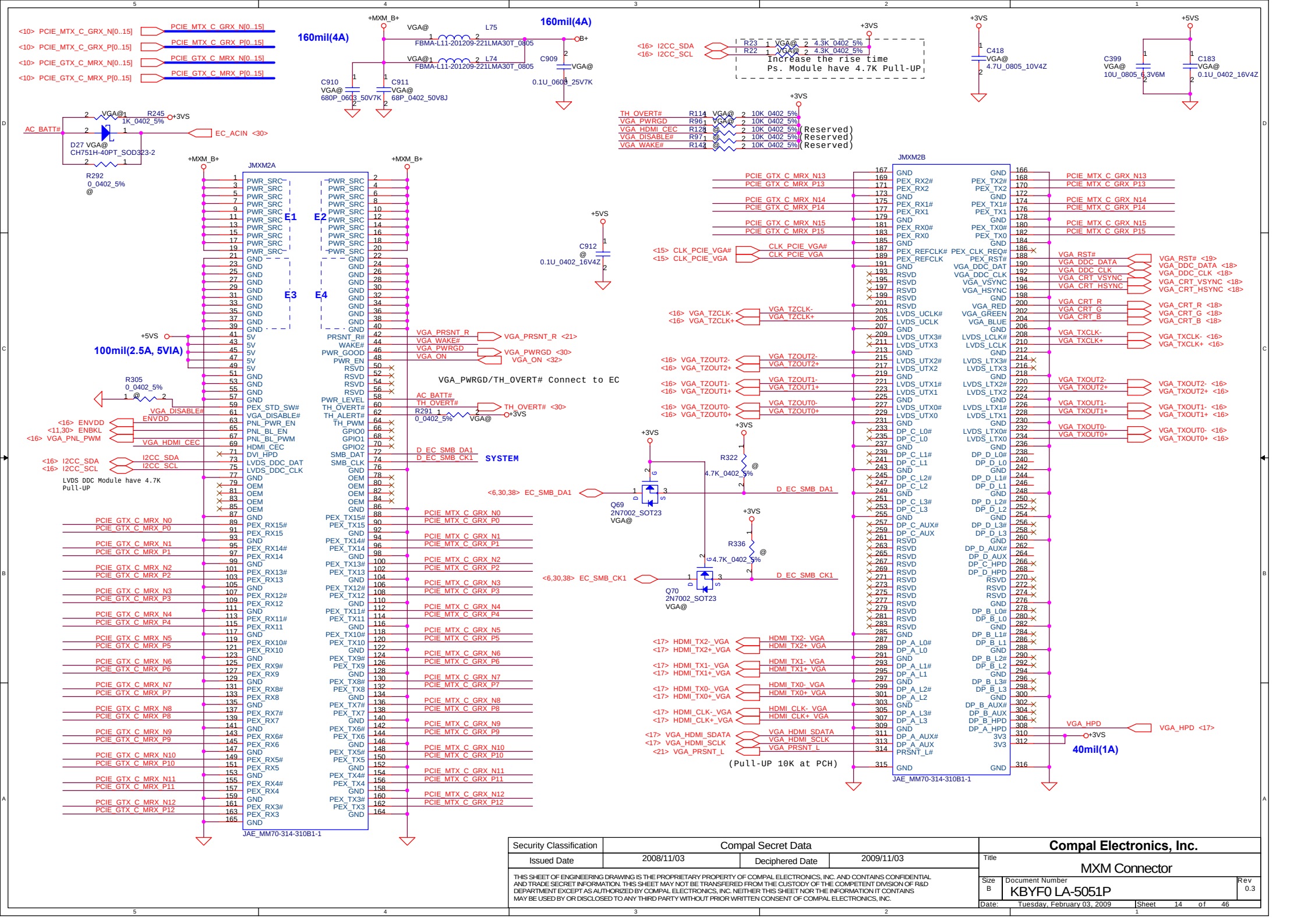
Compal Electronics, Inc.		
Title: RS780 STRAPS		
Size: Custom	Document Number: KBYF0 LA-5051P	Rev: 0.3
Date: Tuesday, February 03, 2009	Sheet 13 of 46	



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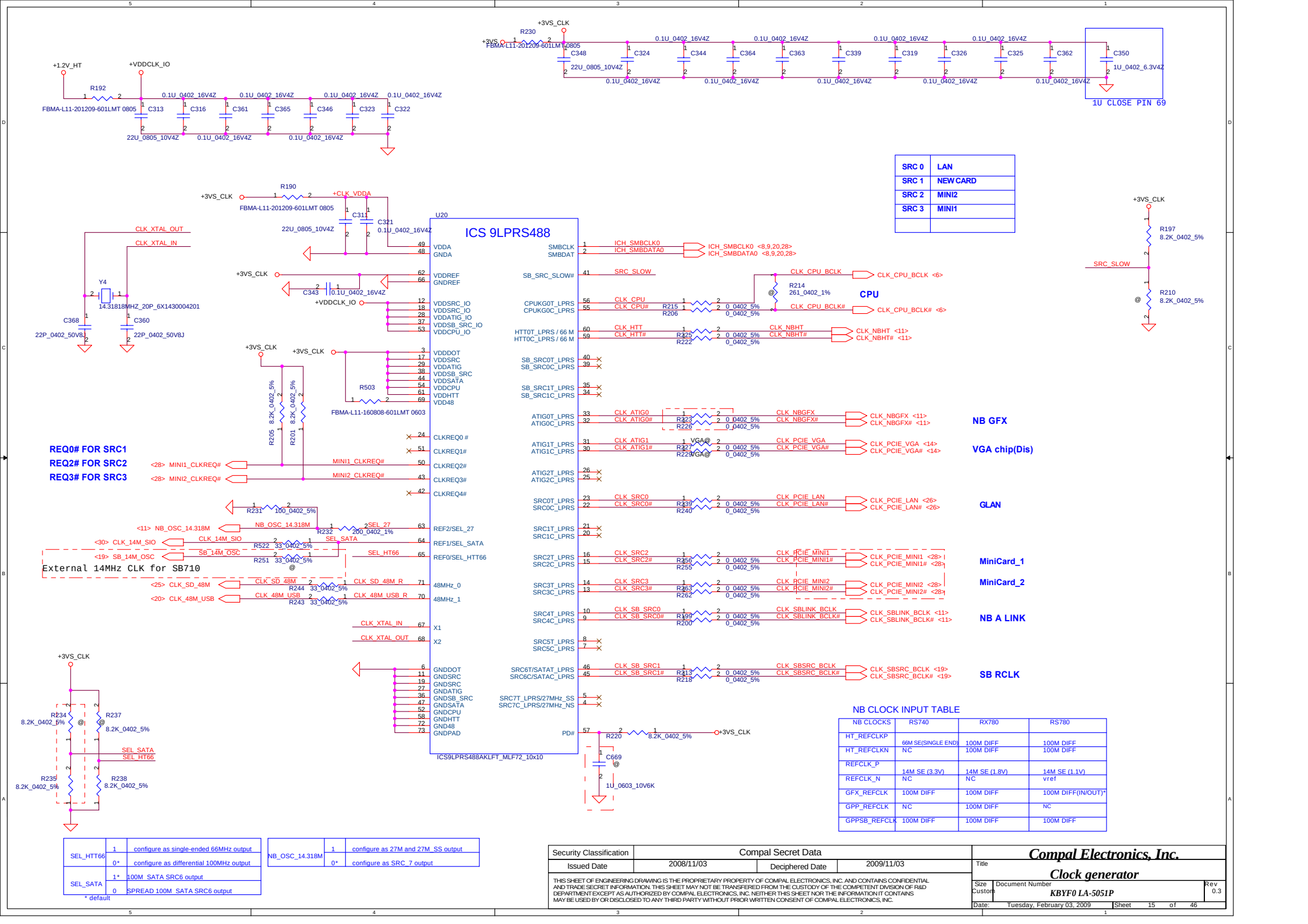
Compal Electronics, Inc.

Title: MXM Connector

Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 14 of 46


+3VS_CLK
R230
FBMA-L11-201209-601LMT 0805
C348
22U_0805_10V4Z
C324
C344
C364
C363
C339
C319
C326
C325
C362
C350
0.1U_0402_16V4Z
1U_0402_6.3V4Z
1U CLOSE PIN 69
+1.2V_HT
+VDDCLK_IO
R192
C313
C316
C361
C365
C346
C323
C322
SRC 0 LAN
SRC 1 NEW CARD
SRC 2 MINI2
SRC 3 MINI1
R190
+CLK_VDDA
C311
C321
U20
ICS 9LPRS488
CLK_XTAL_OUT
CLK_XTAL_IN
Y4
14.31818MHZ_20P_6X1430004201
C368
22P_0402_50V8J
C360
C343
VDDREF
GNDREF
VDDSRC_IO
VDDATIG_IO
VDDSB_SRC_IO
VDDCPU_IO
VDDDOT
VDDSRC
VDDATIG
VDDSB_SRC
VDDSATA
VDDCPU
VDDHTT
VDD48
R503
FBMA-L11-160808-601LMT 0603
R205
R201
8.2K_0402_5%
REQ0# FOR SRC1
REQ2# FOR SRC2
REQ3# FOR SRC3
<28> MINI1_CLKREQ#
<28> MINI2_CLKREQ#
MINI1_CLKREQ#
MINI2_CLKREQ#
CLKREQ0 #
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
R231
100_0402_5%
<11> NB_OSC_14.318M
NB_OSC_14.318M
R232
200_0402_1%
SEL_27
<30> CLK_14M_SIO
CLK_14M_SIO
R522
33_0402_5%
SEL_SATA
<19> SB_14M_OSC
SB_14M_OSC
R251
SEL_HT66
External 14MHz CLK for SB710
<25> CLK_SD_48M
CLK_SD_48M
R244
CLK_SD_48M_R
<20> CLK_48M_USB
CLK_48M_USB
R243
CLK_48M_USB_R
CLK_XTAL_IN
CLK_XTAL_OUT
REF2/SEL_27
REF1/SEL_SATA
REF0/SEL_HTT66
48MHz_0
48MHz_1
X1
X2
GNDDOT
GNDSRC
GNDSRC
GNDATIG
GNDSB_SRC
GNDSATA
GNDCPU
GNDHTT
GND48
GNDPAD
ICS9LPRS488AKLFT_MLF72_10x10
SMBCLK
SMBDAT
ICH_SMBCLK0
ICH_SMBDATA0
ICH_SMBCLK0 <8,9,20,28>
ICH_SMBDATA0 <8,9,20,28>
SB_SRC_SLOW#
SRC_SLOW
CPUKG0T_LPRS
CPUKG0C_LPRS
CLK_CPU
CLK_CPU#
R215
R206
CLK_CPU_BCLK
CLK_CPU_BCLK#
R214
261_0402_1%
CPU
CLK_CPU_BCLK <6>
CLK_CPU_BCLK# <6>
HTT0T_LPRS / 66 M
HTT0C_LPRS / 66 M
CLK_HTT
CLK_HTT#
R225
R222
CLK_NBHT
CLK_NBHT#
CLK_NBHT <11>
CLK_NBHT# <11>
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
ATIG0T_LPRS
ATIG0C_LPRS
CLK_ATIG0
CLK_ATIG0#
R223
R226
CLK_NBGFX
CLK_NBGFX#
CLK_NBGFX <11>
CLK_NBGFX# <11>
NB GFX
ATIG1T_LPRS
ATIG1C_LPRS
CLK_ATIG1
CLK_ATIG1#
R227
R224
VGA@
CLK_PCIE_VGA
CLK_PCIE_VGA#
CLK_PCIE_VGA <14>
CLK_PCIE_VGA# <14>
VGA chip(Dis)
ATIG2T_LPRS
ATIG2C_LPRS
SRC0T_LPRS
SRC0C_LPRS
CLK_SRC0
CLK_SRC0#
R239
R240
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_PCIE_LAN <26>
CLK_PCIE_LAN# <26>
GLAN
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
CLK_SRC2
CLK_SRC2#
R256
R255
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
CLK_PCIE_MINI1 <28>
CLK_PCIE_MINI1# <28>
MiniCard_1
SRC3T_LPRS
SRC3C_LPRS
CLK_SRC3
CLK_SRC3#
R263
R262
CLK_PCIE_MINI2
CLK_PCIE_MINI2#
CLK_PCIE_MINI2 <28>
CLK_PCIE_MINI2# <28>
MiniCard_2
SRC4T_LPRS
SRC4C_LPRS
CLK_SB_SRC0
CLK_SB_SRC0#
R199
R200
CLK_SBLINK_BCLK
CLK_SBLINK_BCLK#
CLK_SBLINK_BCLK <11>
CLK_SBLINK_BCLK# <11>
NB A LINK
SRC5T_LPRS
SRC5C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
CLK_SB_SRC1
CLK_SB_SRC1#
R213
R218
CLK_SBSRC_BCLK
CLK_SBSRC_BCLK#
CLK_SBSRC_BCLK <19>
CLK_SBSRC_BCLK# <19>
SB RCLK
SRC7T_LPRS/27MHz_SS
SRC7C_LPRS/27MHz_NS
PD#
R220
8.2K_0402_5%
+3VS_CLK
C669
1U_0603_10V6K
R197
8.2K_0402_5%
SRC_SLOW
R210
8.2K_0402_5%
R234
R237
R235
R238
SEL_SATA
SEL_HT66
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
SEL_HTT66 | 1 configure as single-ended 66MHz output | 0* configure as differential 100MHz output
SEL_SATA | 1* 100M_SATA SRC6 output | 0 SPREAD 100M_SATA SRC6 output
* default
NB_OSC_14.318M | 1 configure as 27M and 27M_SS output | 0* configure as SRC_7 output
Security Classification | Compal Secret Data
Issued Date | 2008/11/03 | Deciphered Date | 2009/11/03
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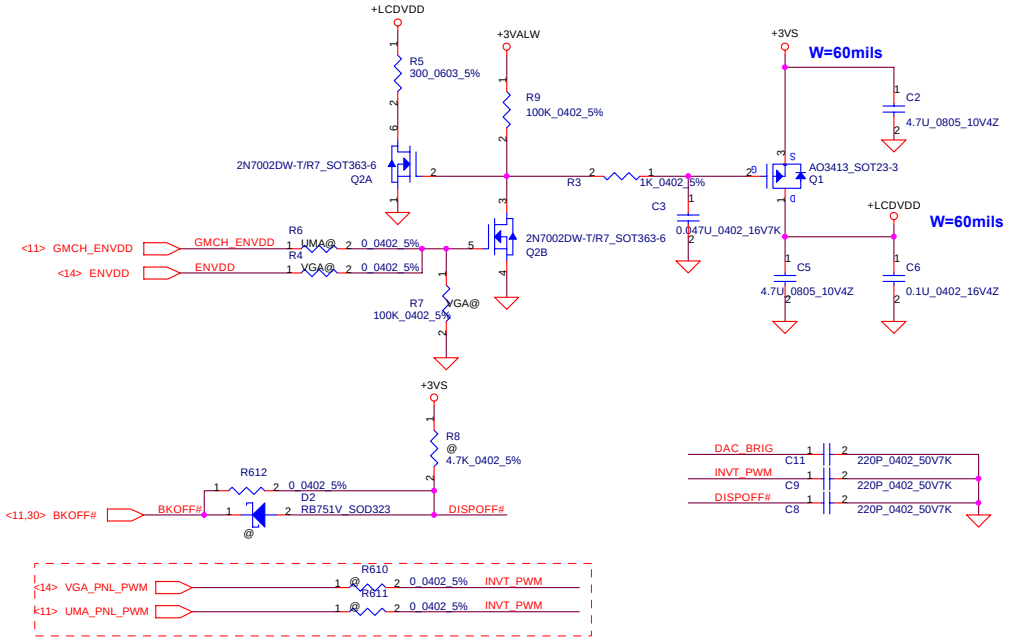
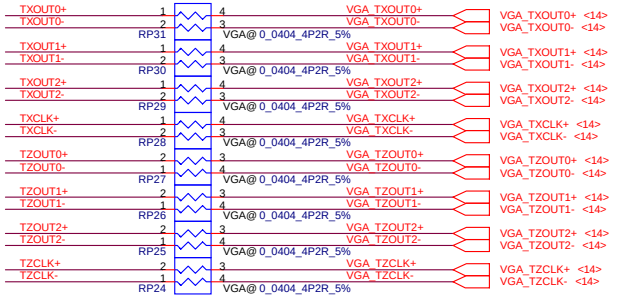
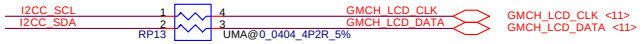
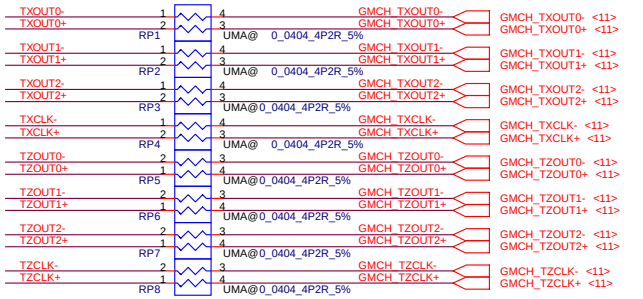
Compal Electronics, Inc.
Title
Clock generator
Size Custom
Document Number
KBYF0 LA-5051P
Rev 0.3
Date: Tuesday, February 03, 2009
Sheet 15 of 46

LCD POWER CIRCUIT

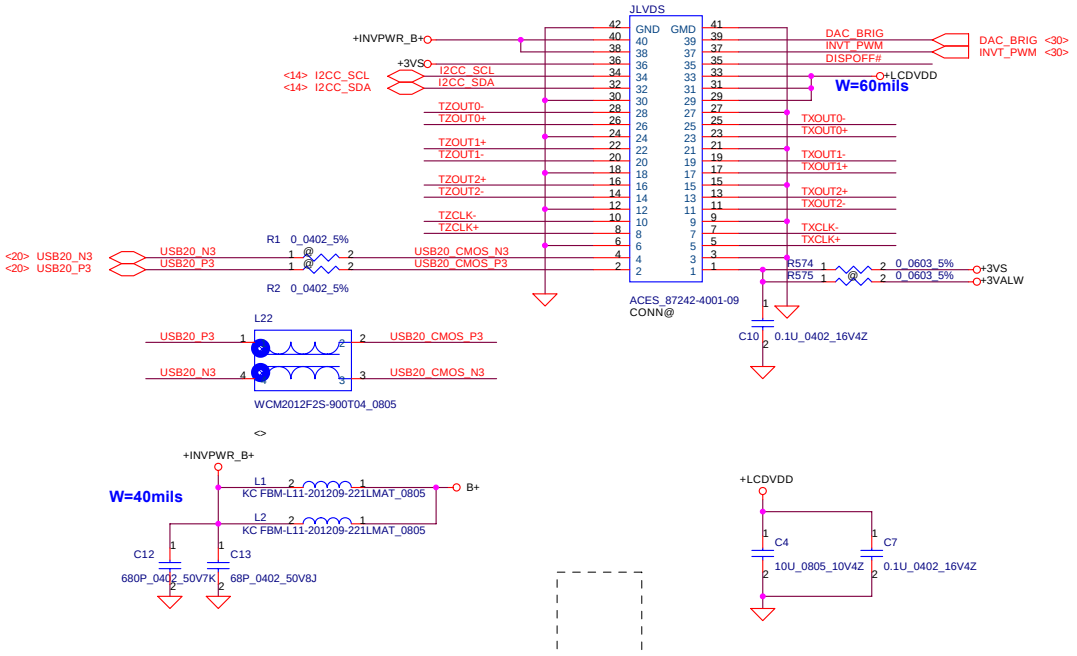








LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: LVDS & DVI Connector

Size: B | Document Number: KBYF0 LA-5051P | Rev: 0.3

Date: Tuesday, February 03, 2009 | Sheet 16 of 46

reserve HDMI I2C ESD diode

DDC to HDMI CONN

Place closed to JHDMI1

W=40mils

715-Ω for RS880M

Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

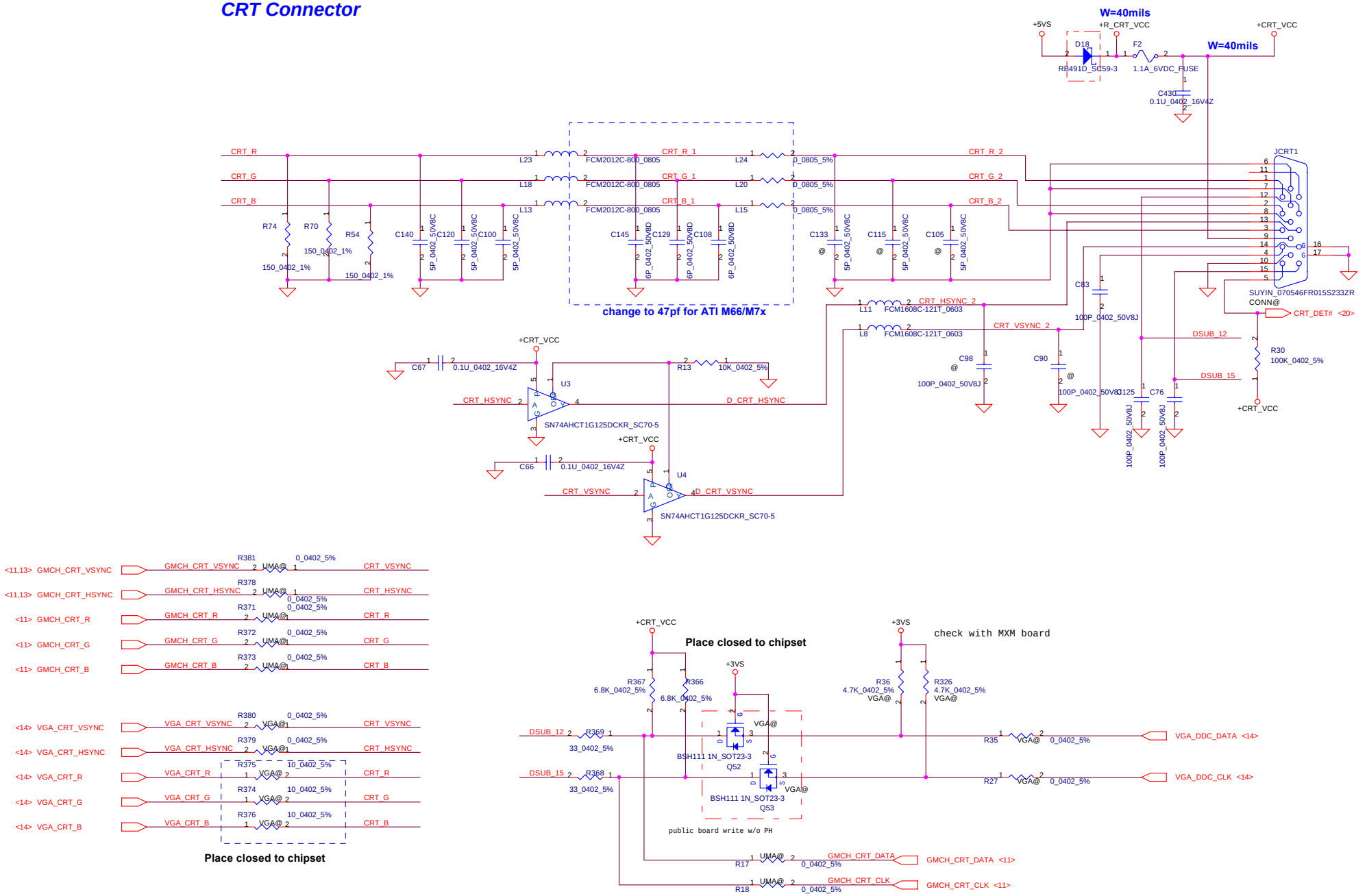
Compal Electronics, Inc.

Title: DVI/HDMI Connector

Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 17 of 46

CRT Connector



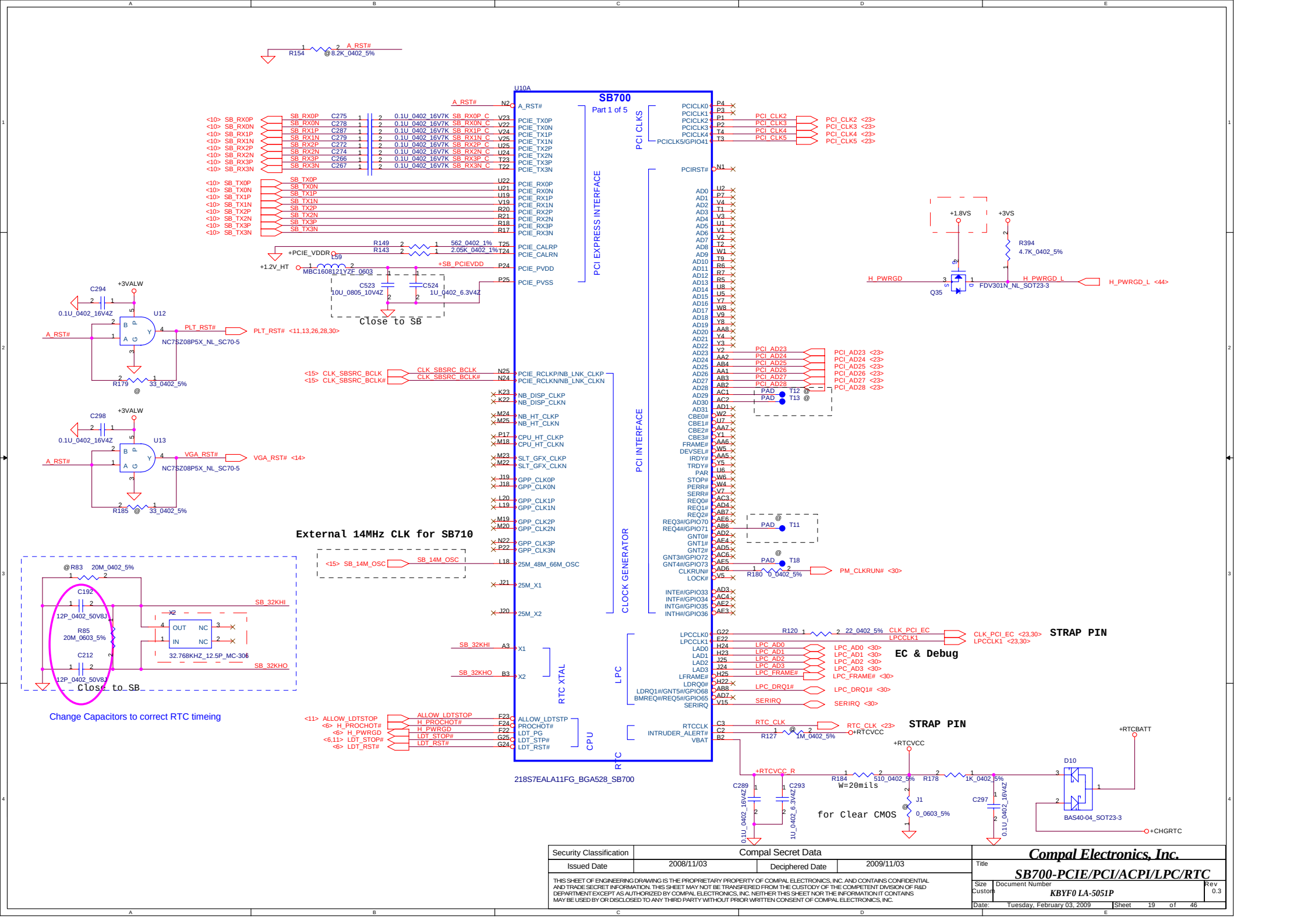
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 18 of 46



Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: SB700-PCIE/PCI/ACPI/LPC/RTC

Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 19 of 46

SKU-ID	R509	R510
UMA		POP
DIS	POP	

USB-12 Bluetooth

USB-8 MiniCard(WLAN)

USB-6 HS-USB

USB-5 MiniCard(TV)

USB-4 Card Reader

USB-3 USB Camera

USB-2 USB (eSATA) for SJM70
Ext.USB/B for SJV70

USB-1 Ext.USB/B

USB-0 Ext.USB/B

demo circuit LID use RI#

SB700 has internal PD

SB Power Domain :S5

High: CRT Plugged

STRAP PIN

STRAP PIN

U10D — SB700 Part 4 of 5 — 218S7EALA11FG_BGA528_SB700

Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

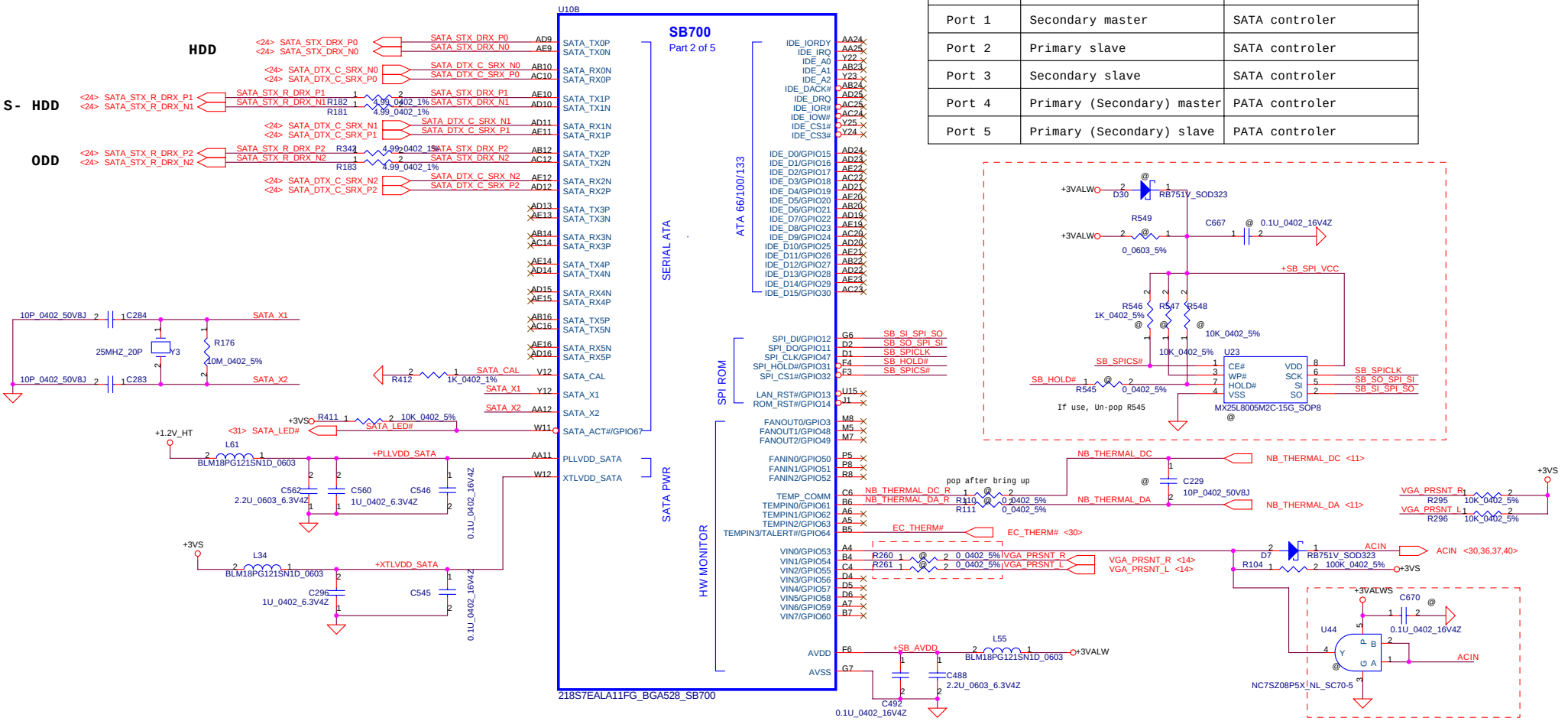
Compal Electronics, Inc.

Title: **SB700 USB/HD audio**

Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 20 of 46

Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controler
Port 1	Secondary master	SATA controler
Port 2	Primary slave	SATA controler
Port 3	Secondary slave	SATA controler
Port 4	Primary (Secondary) master	PATA controler
Port 5	Primary (Secondary) slave	PATA controler



Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

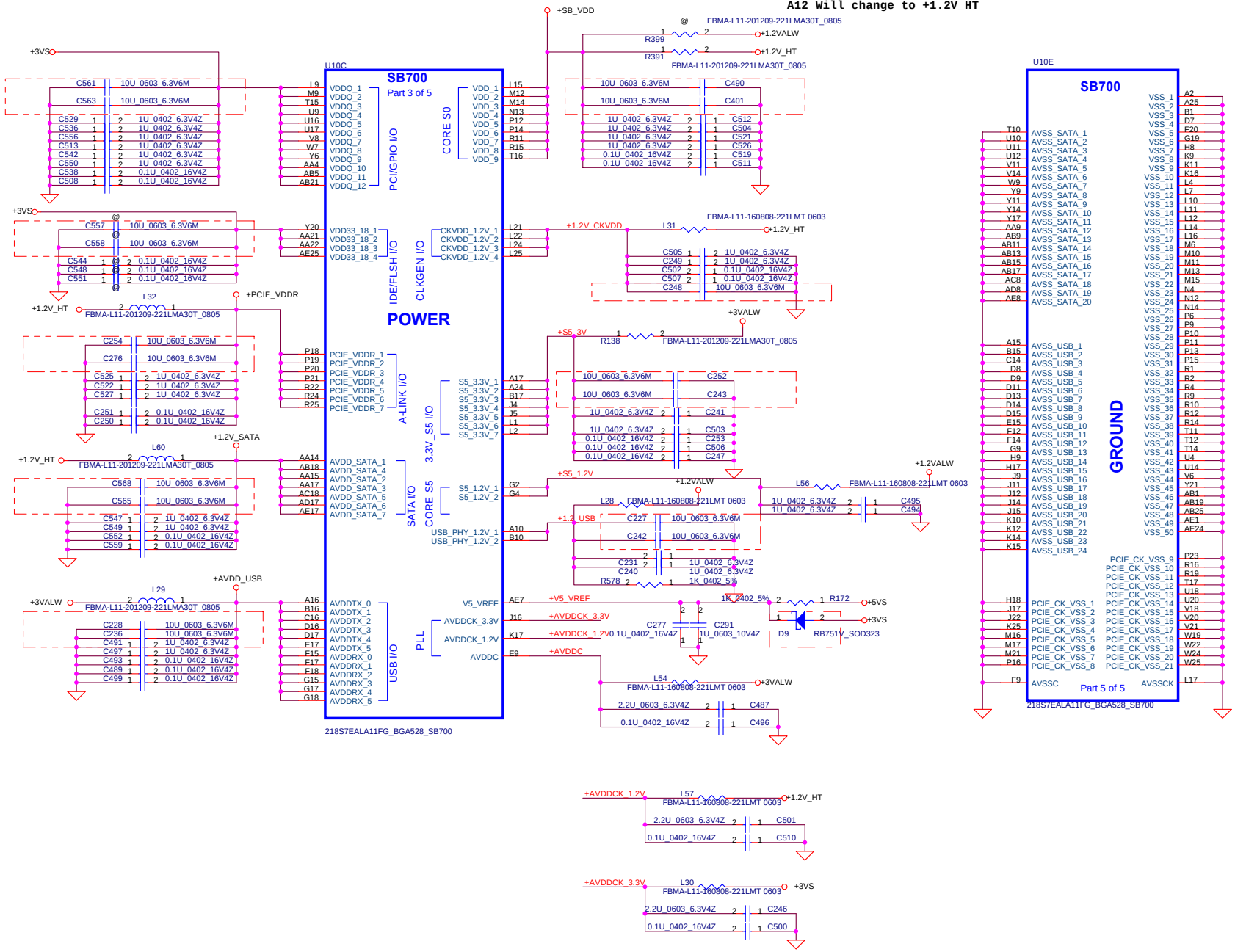
Compal Electronics, Inc.

Title: SB700 SATA/IDE/SPI

Size: Custom | Document Number: KBYF0 LA-5051P | Rev: 0.3

Date: Tuesday, February 03, 2009 | Sheet 21 of 46

FOR SB700 ALL issue
A12 Will change to +1.2V_HT



Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: **SB700 power/GND**

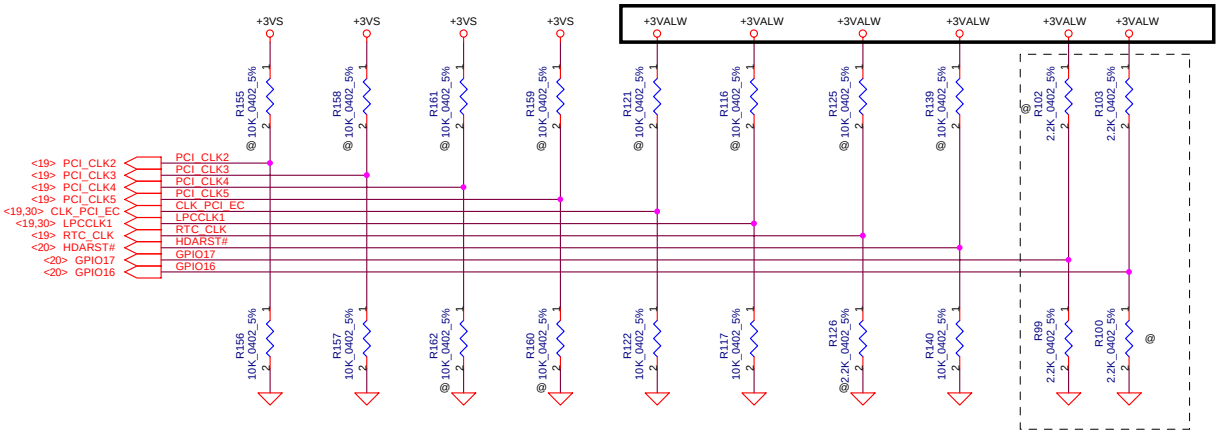
Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 22 of 46

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

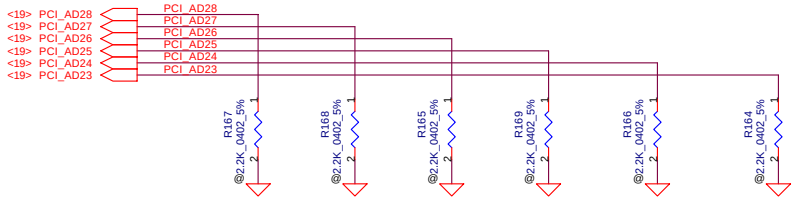
	PCI_CLK2 CLK_PCI_PCM	PCI_CLK3 CLK_PCI_DBG	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	**INTERNAL RTC** DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM **L,H = LPC ROM (Default L,NC)** L,L = FWH ROM
PULL LOW	**BOOTFAIL TIMER DISABLED** DEFAULT	**IGNORE DEBUG STRAPS** DEFAULT			**DISABLE PCI MEM BOOT** DEFAULT	**CLKGEN DISABLED** DEFAULT	**EXT. RTC** (PD on X1, apply 32KHz to RTC_CLK)	**EC DISABLED** DEFAULT	



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	**USE LONG RESET** DEFAULT	**USE PCI PLL** DEFAULT	**USE ACPI BCLK** DEFAULT	**USE IDE PLL** DEFAULT	**USE DEFAULT PCIE STRAPS** DEFAULT	**RESERVED**
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.			
Title: SB700 STRAPS			
Size: Custom	Document Number: KBYF0 LA-5051P		Rev: 0.3
Date: Tuesday, February 03, 2009	Sheet 23 of 46		

HDD

Pleace near HD CONN (JSATA1)

Pleace near HD CONN

JSATA1 — SUYIN_127043FR022G226ZL_NR <BOM Structure>

SATA_STX_RC_DRX_P0 C336 0.01U_0402_16V7K SATA_STX_DRX_P0 → SATA_STX_DRX_P0 <21>
SATA_STX_RC_DRX_N0 C332 0.01U_0402_16V7K SATA_STX_DRX_N0 → SATA_STX_DRX_N0 <21>
SATA_DTX_SRX_N0 C345 0.01U_0402_16V7K SATA_DTX_C_SRX_N0 → SATA_DTX_C_SRX_N0 <21>
SATA_DTX_SRX_P0 C347 0.01U_0402_16V7K SATA_DTX_C_SRX_P0 → SATA_DTX_C_SRX_P0 <21>

U2 — PI2EQX3231BLZHE_TQFN20_3P5X4P5

SATA_PTX_RPI_DRX_P0 C622 0.01U_0402_16V7K SATA_PTX_RPO_DRX_P0
SATA_PTX_RPI_DRX_N0 C620 0.01U_0402_16V7K SATA_PTX_RPO_DRX_N0
SATA_DTX_RPO_PRX_N0 C618 0.01U_0402_16V7K SATA_DTX_RPI_PRX_N0
SATA_DTX_RPO_PRX_P0 C617 0.01U_0402_16V7K SATA_DTX_RPI_PRX_P0

Adjust HDD1 CHA I/O EQ
Adjust HDD1 CHB I/O EQ
R680 R679 R677 R676 470K_0402_5%

R404 R403 R402 R401 0_0402_5%
SATA_PTX_RPO_DRX_P0 R425 470_0402_5%
SATA_PTX_RPO_DRX_N0
SATA_DTX_RPI_PRX_N0
SATA_DTX_RPI_PRX_P0

Adjust HDD1 PCH TX Swing

Second-HDD

Pleace near HD CONN (JSATA3)

Pleace near HD CONN

JSATA3 — OCTEK_SAT-22SB1G_RV CONN@

SATA_STX_RC_DRX_P1 C379 0.01U_0402_16V7K SATA_STX_R_DRX_P1 → SATA_STX_R_DRX_P1 <21>
SATA_STX_RC_DRX_N1 C384 0.01U_0402_16V7K SATA_STX_R_DRX_N1 → SATA_STX_R_DRX_N1 <21>
SATA_DTX_SRX_N1 C378 0.01U_0402_16V7K SATA_DTX_C_SRX_N1 → SATA_DTX_C_SRX_N1 <21>
SATA_DTX_SRX_P1 C369 0.01U_0402_16V7K SATA_DTX_C_SRX_P1 → SATA_DTX_C_SRX_P1 <21>

HDD1 Redriver Chip Enable
R426 10K_0402_5%
SATA1_CE

ODD

JSATA2 — CONN@ OCTEK_0709015-SD001_RV

SATA_STX_RC_DRX_P2 C302 0.01U_0402_16V7K SATA_STX_R_DRX_P2 → SATA_STX_R_DRX_P2 <21>
SATA_STX_RC_DRX_N2 C301 0.01U_0402_16V7K SATA_STX_R_DRX_N2 → SATA_STX_R_DRX_N2 <21>
SATA_DTX_SRX_N2 C300 0.01U_0402_16V7K SATA_DTX_C_SRX_N2 → SATA_DTX_C_SRX_N2 <21>
SATA_DTX_SRX_P2 C299 0.01U_0402_16V7K SATA_DTX_C_SRX_P2 → SATA_DTX_C_SRX_P2 <21>

Placea caps. near ODD CONN.

U30 — TPS2061DRG4_SO8 — 80mil

+5VALW, +3VALW, +USB_VCCA
C340 4.7U_0805_10V4Z
R242 100K_0402_5%
R228 10K_0402_5%
C333 0.1U_0402_16V4Z
USB_OC#2 <20,29>
<29,36,43> SYSON#

+USB_VCCA — W=60mils
C806 150U_Y_6.3VM
C808 C807 0.1U_0402_16V4Z 1000P_0402_50V7K

JUSB4 — SUYIN_020173MR004S512ZL

USB20_N2_R
USB20_P2_R

<20> USB20_P2_1 → R389 0_0402_5% → USB20_P2_R
<20> USB20_N2_1 → L37 WCM2012F2S-900T04_0805 → USB20_N2_R
R377 0_0402_5%

D39 PJDLC05_SOT23-6

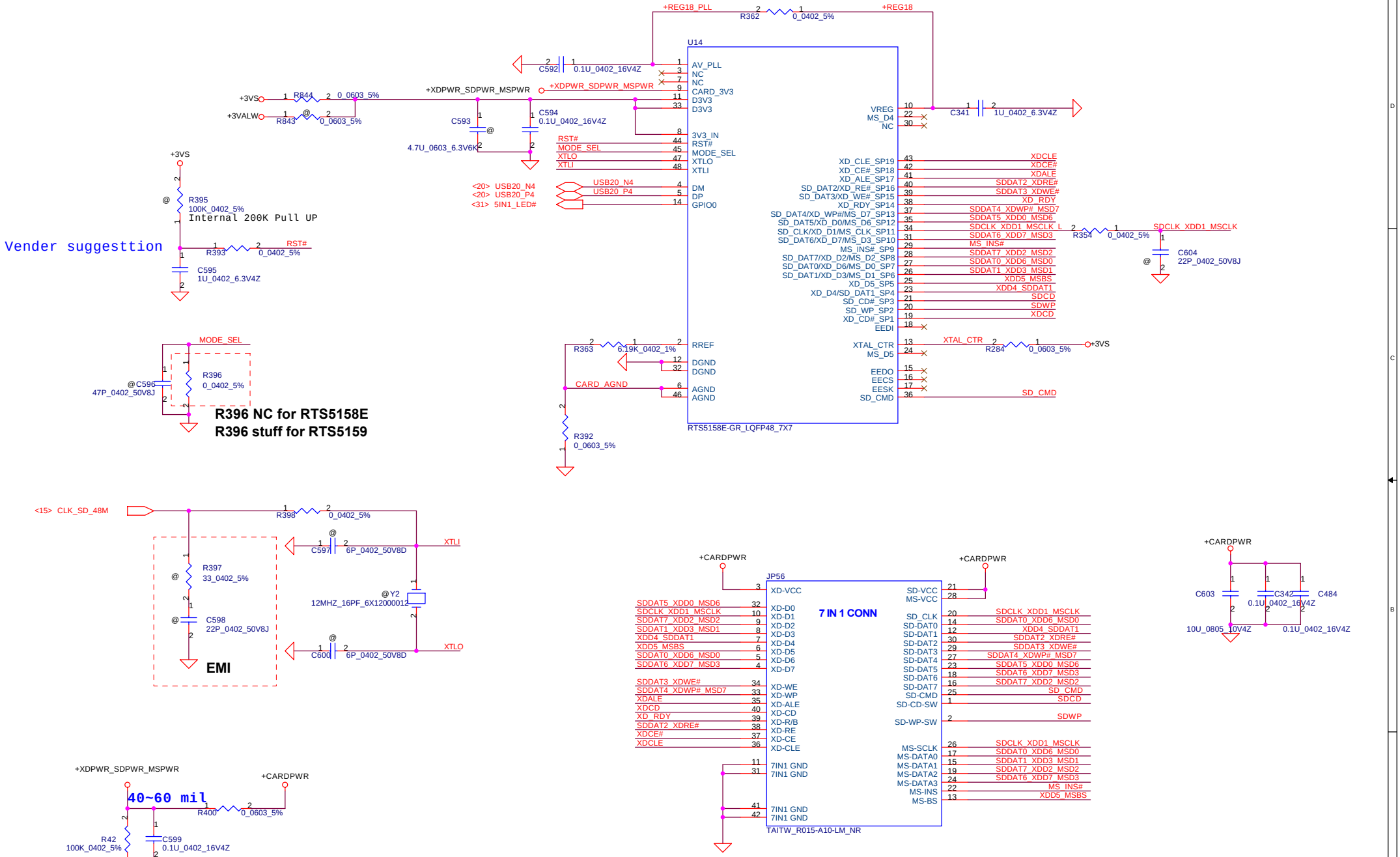
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 24 of 46



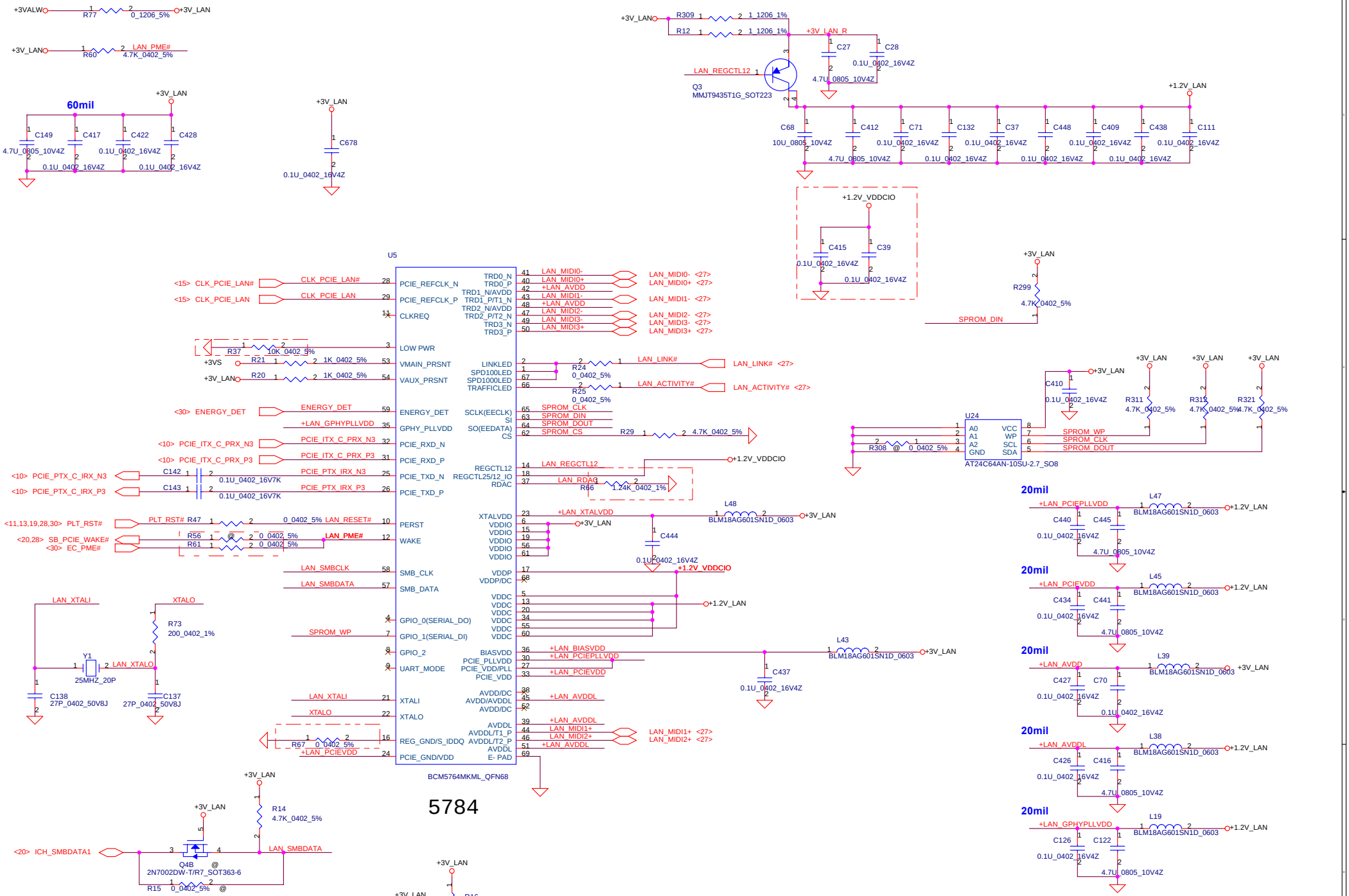
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: Card Reader JMB385

Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 25 of 46



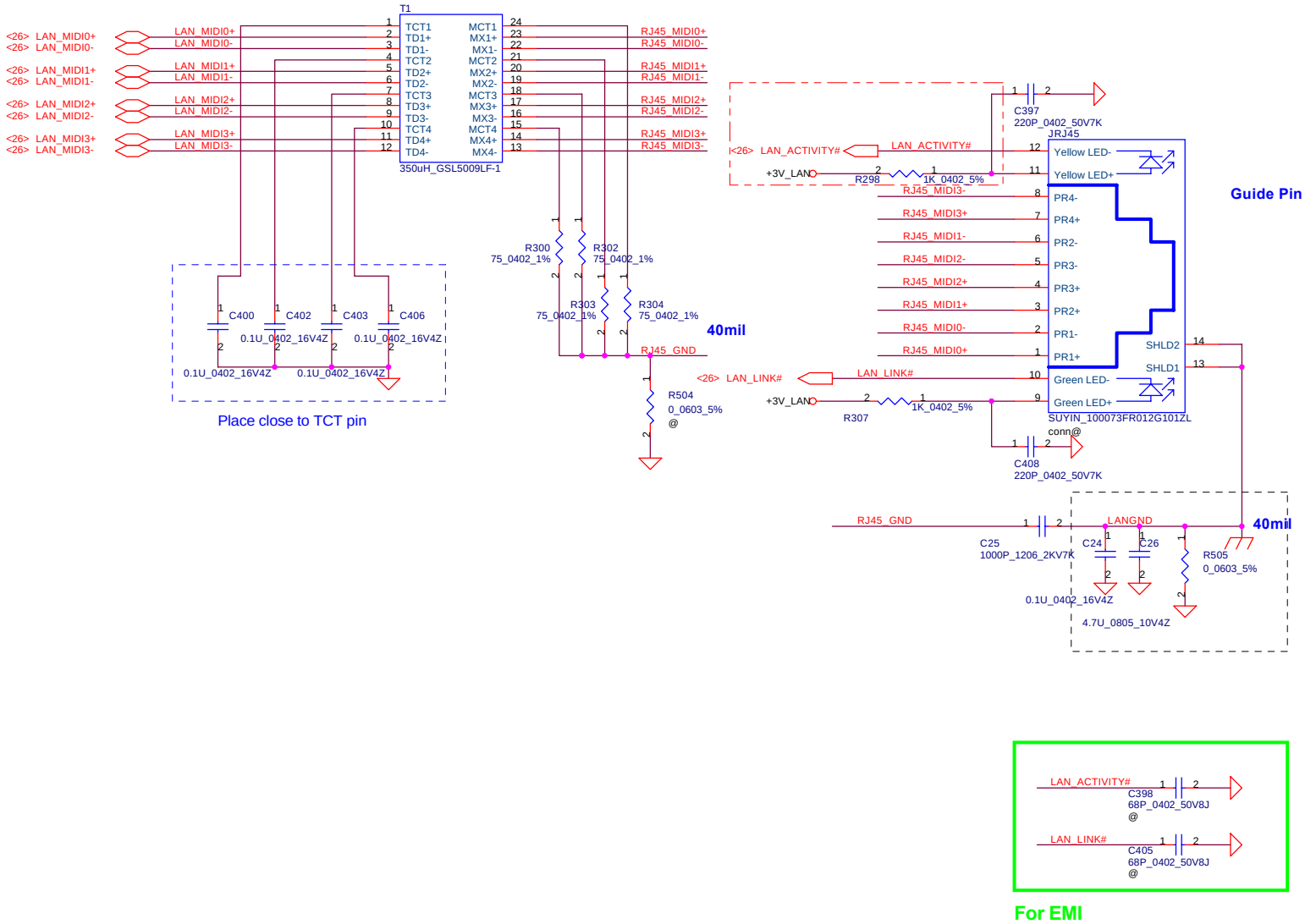
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: BCM5764M_5787M

Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 26 of 46



Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

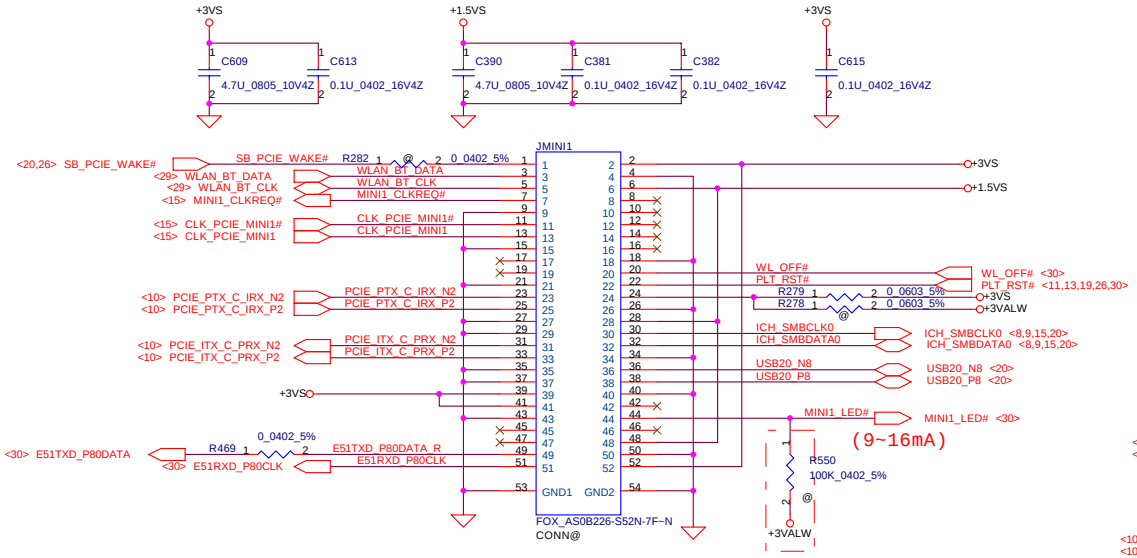
Compal Electronics, Inc.

Title: LAN Magnetic & RJ45/RJ11

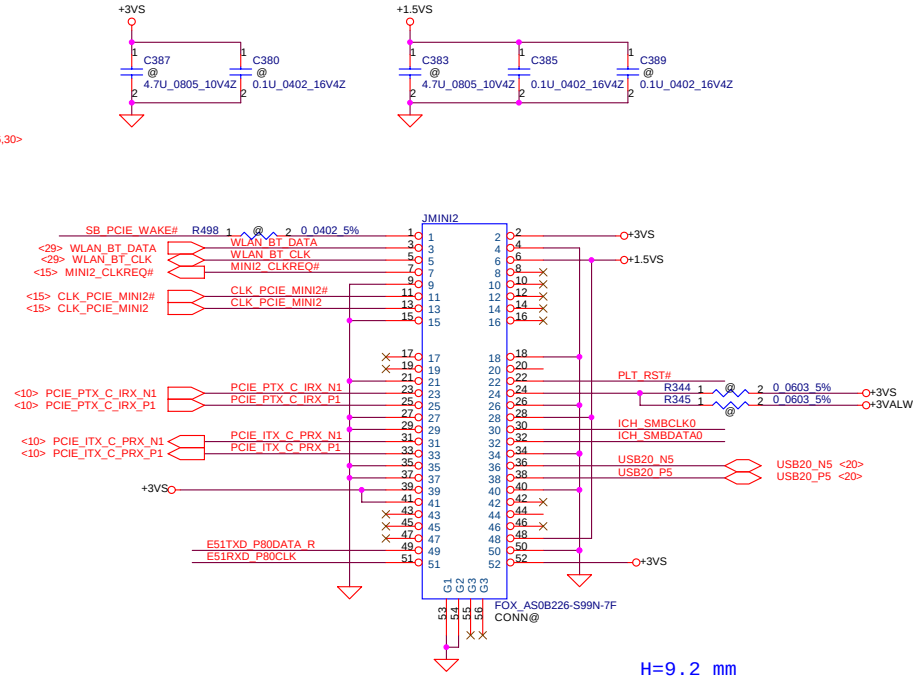
Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 27 of 46

For Wireless LAN



For TV-Tuner/HW MPEG



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

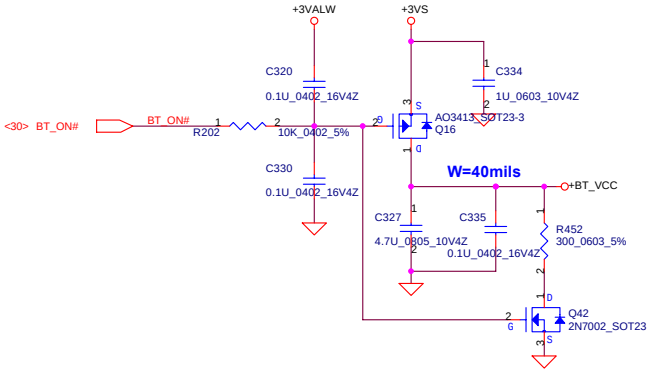
Compal Electronics, Inc.

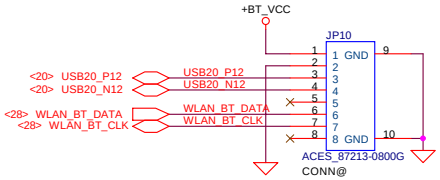
Title: MINI CARD (WLAN & TV-Tuner)

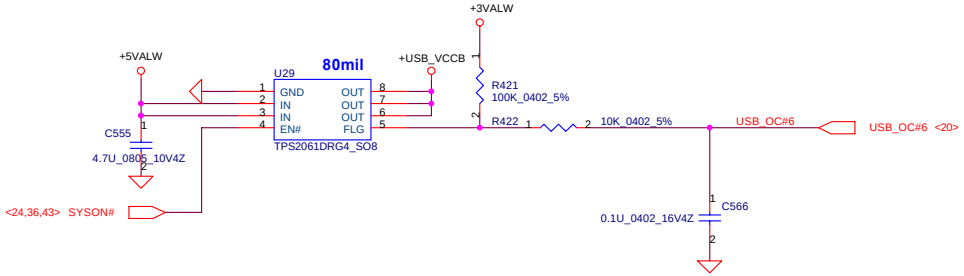
Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 28 of 46

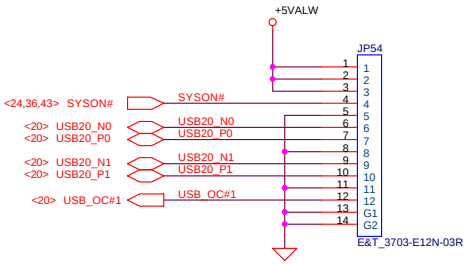
Bluetooth Conn.



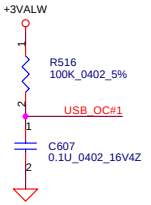


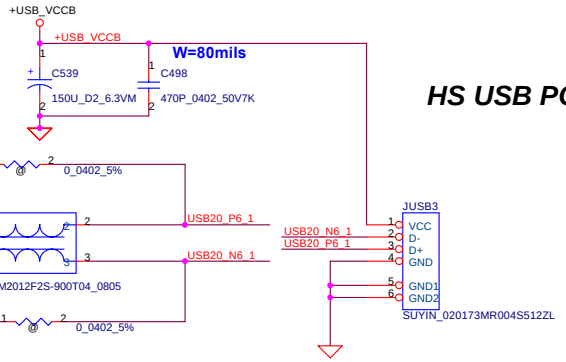


2 PORT

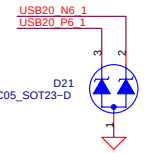


right

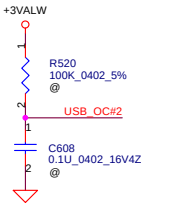


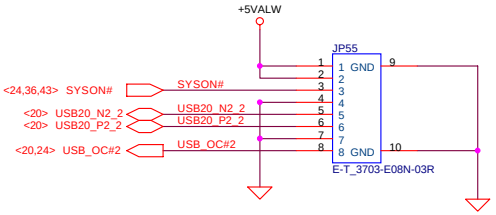


HS USB PORT



1 PORT FOR JV70





Right Up

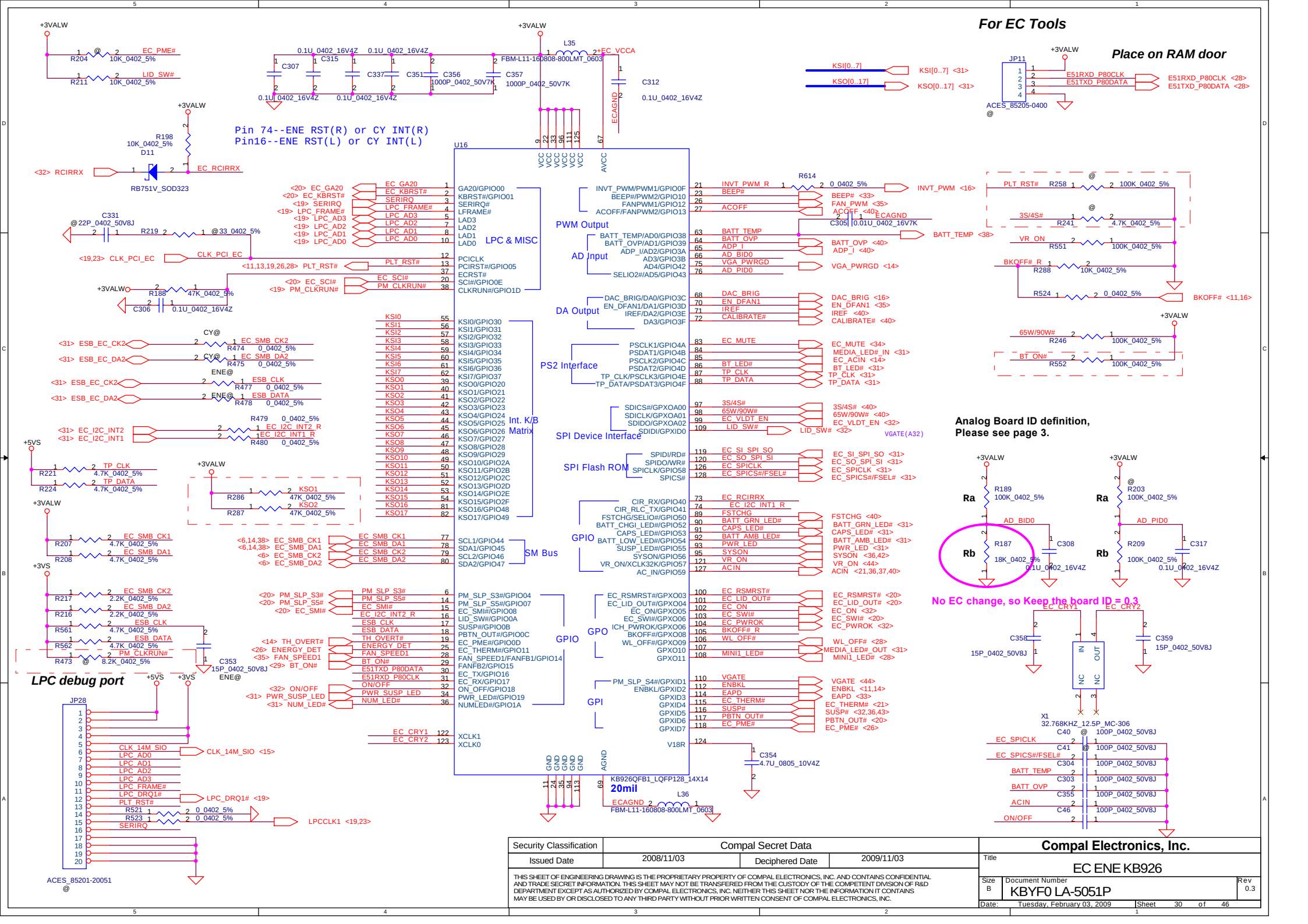
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

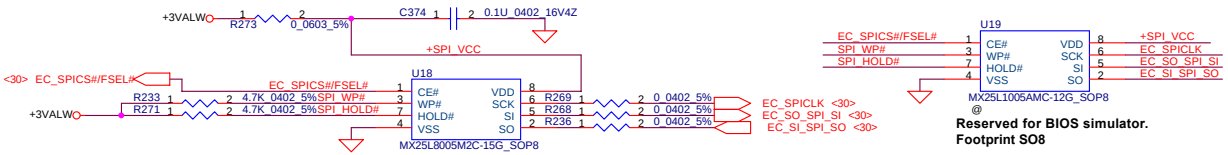
Compal Electronics, Inc.

Title: NEW CARD & USB Connector

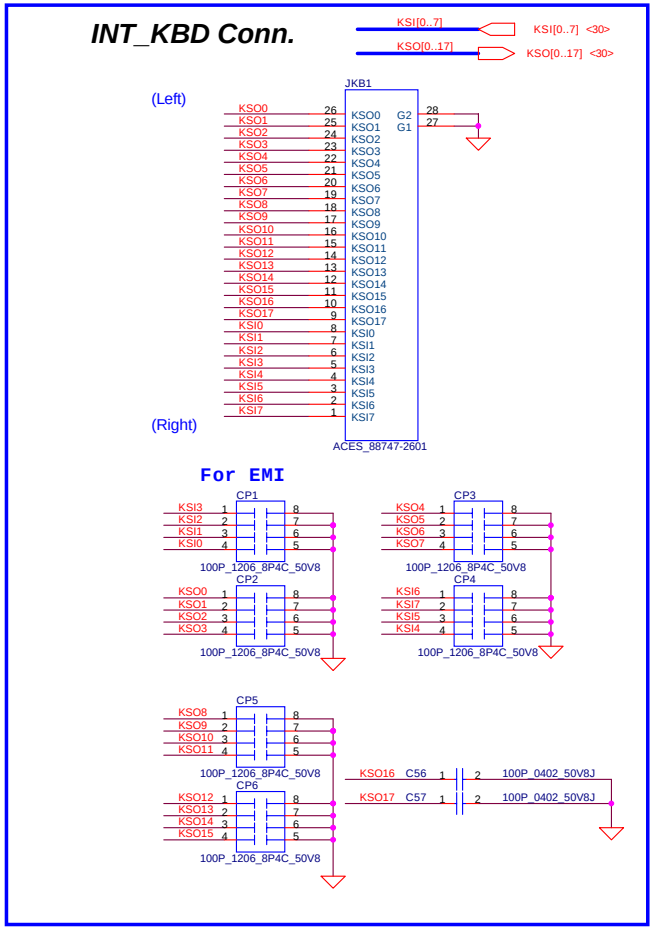
Size: B | Document Number: KBYF0 LA-5051P | Rev: 0.3

Date: Tuesday, February 03, 2009 | Sheet 29 of 46


For EC Tools
Place on RAM door
Pin 74--ENE RST(R) or CY INT(R)
Pin16--ENE RST(L) or CY INT(L)
U16
KB926QFB1_LQFP128_14X14
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Analog Board ID definition, Please see page 3.
No EC change, so Keep the board ID = 0.3
LPC debug port
Security Classification
Compal Secret Data
Issued Date
2008/11/03
Deciphered Date
2009/11/03
Compal Electronics, Inc.
EC ENE KB926
KBYF0 LA-5051P
Rev 0.3
Tuesday, February 03, 2009
Sheet 30 of 46

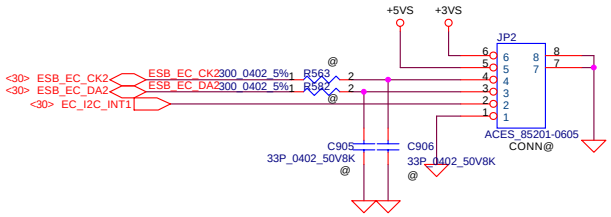


INT_KBD Conn.

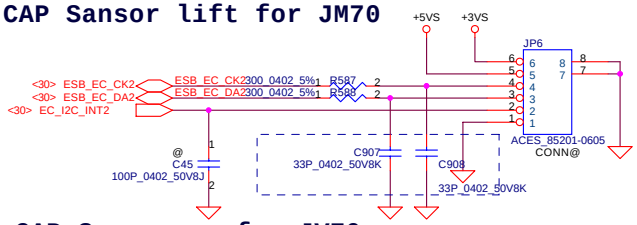


To Media/B Conn.

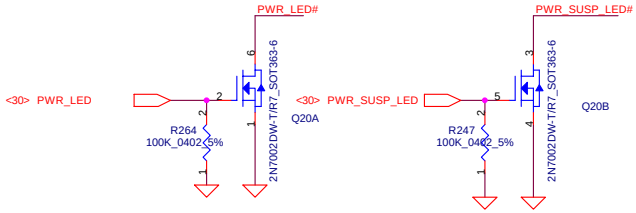
CAP Sansor right JM70



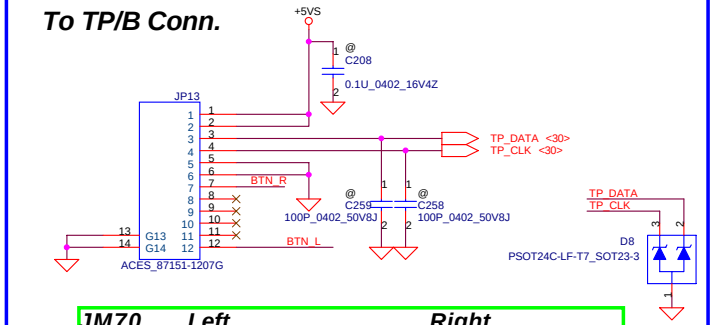
CAP Sansor lift for JM70



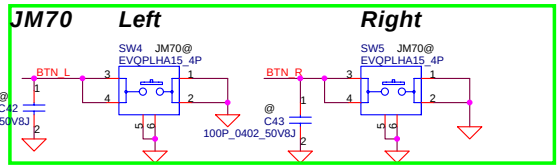
CAP Sansor up for JV70



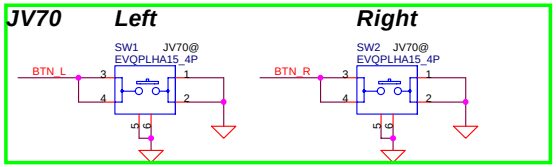
To TP/B Conn.



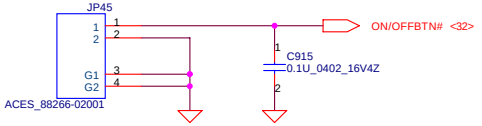
JM70



JV70

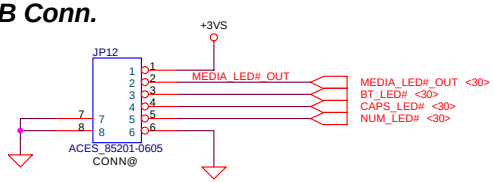


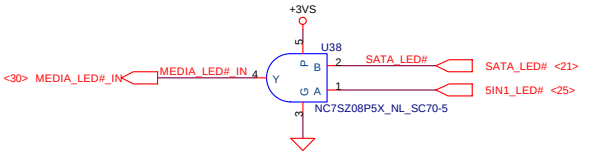
TO POWER BTN/B for JV70



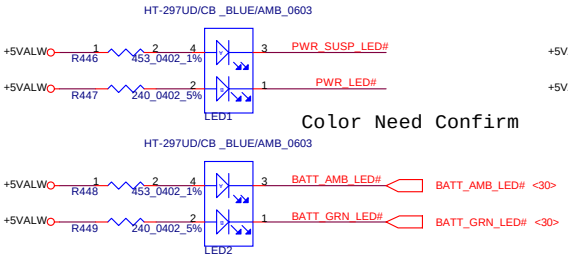
Need Check

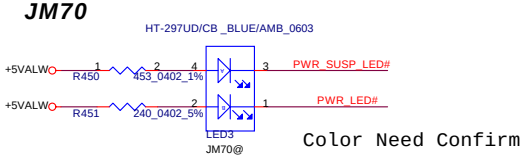
To LED/B Conn.





JM70





JM70	JV70
1.HDD	1.HDD
2.BT_LED	2.BT_LED
3.CAP LED	4.NUM_LED
4.NUM_LED	3.CAP LED

Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

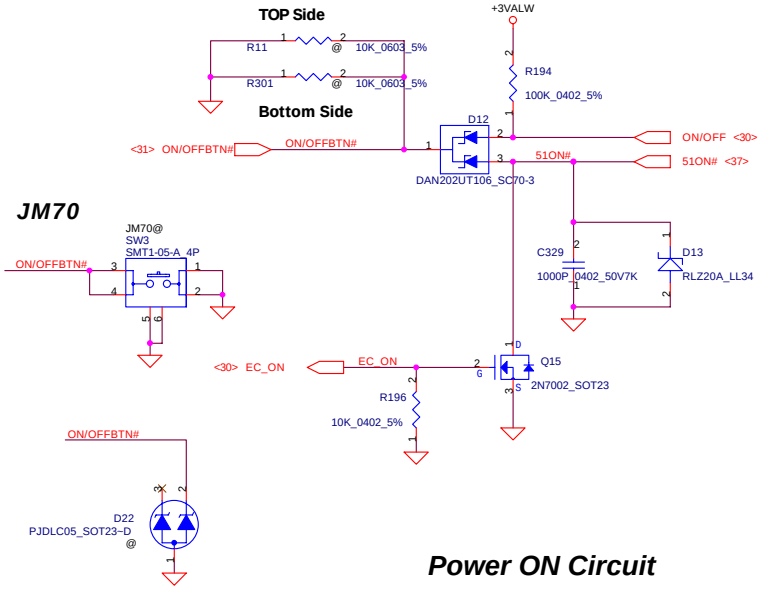
Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3

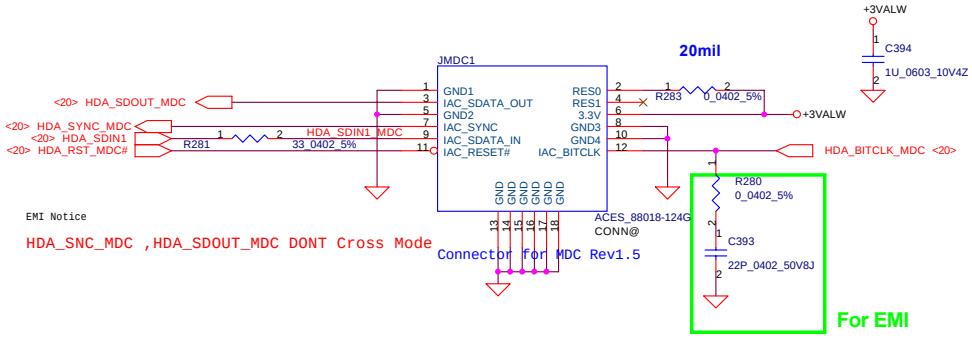
Date: Tuesday, February 03, 2009 Sheet 31 of 46

Power Button

ON/OFF switch

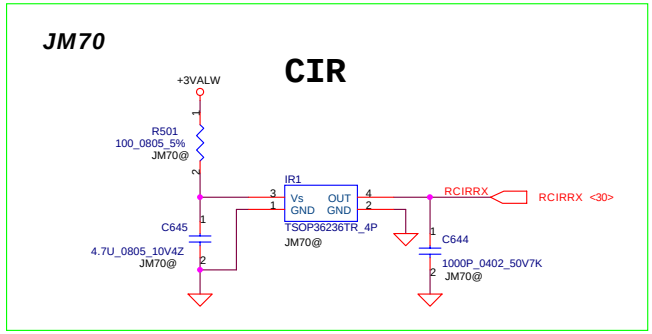


HDA MDC Conn.

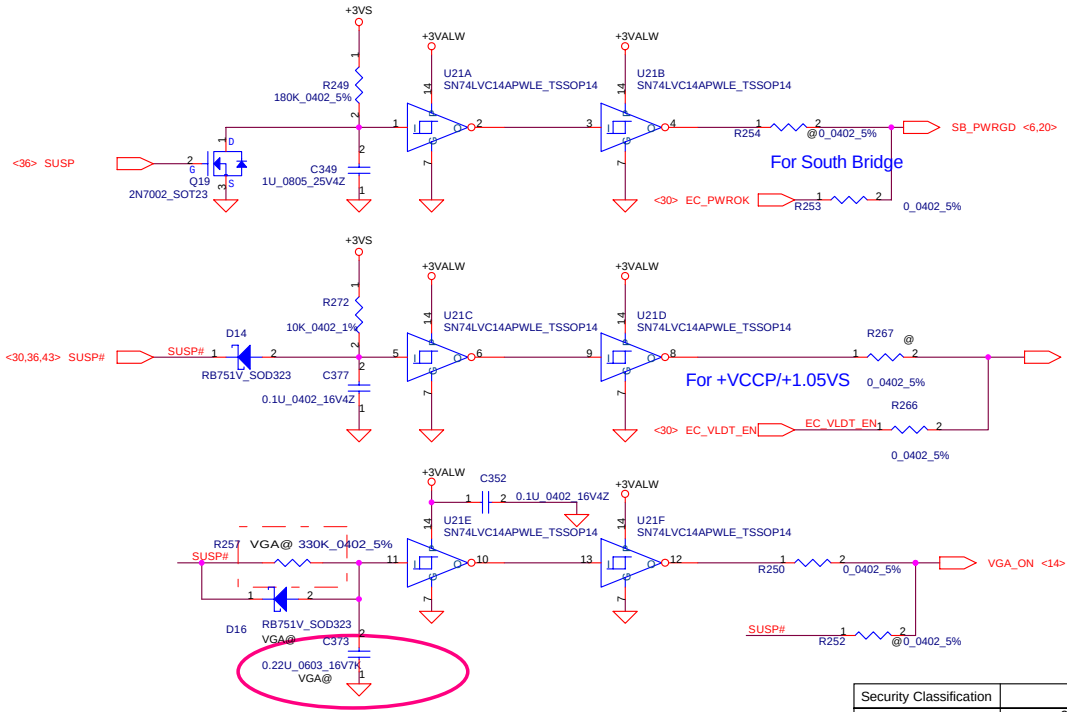


JM70

CIR

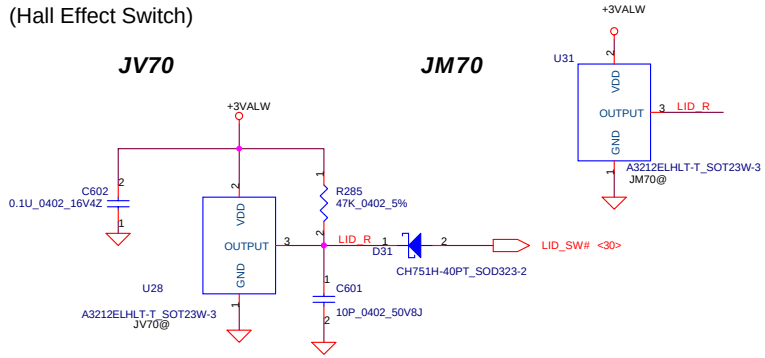


Power ON Circuit



Lid Switch

(Hall Effect Switch)



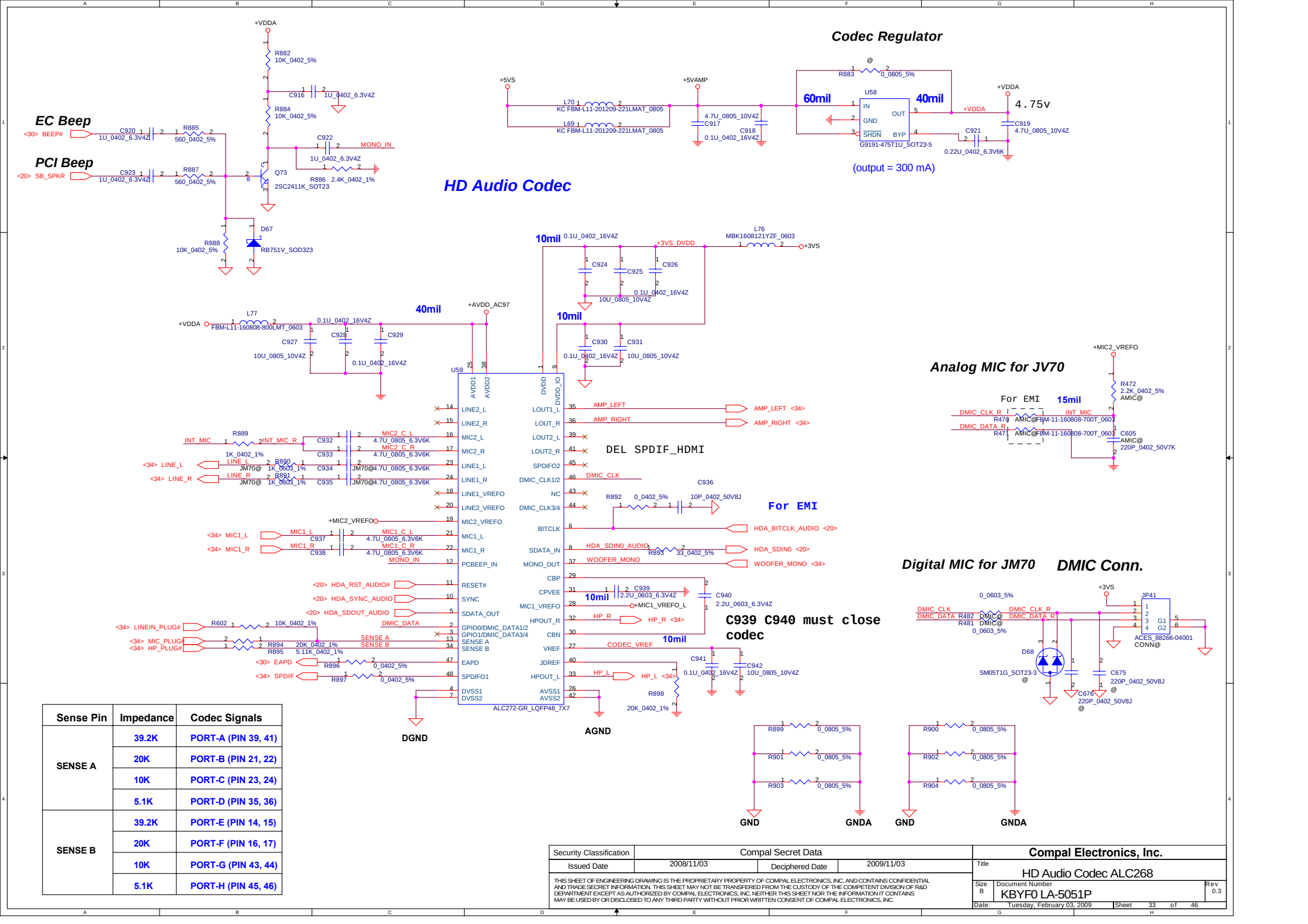
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 32 of 46



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

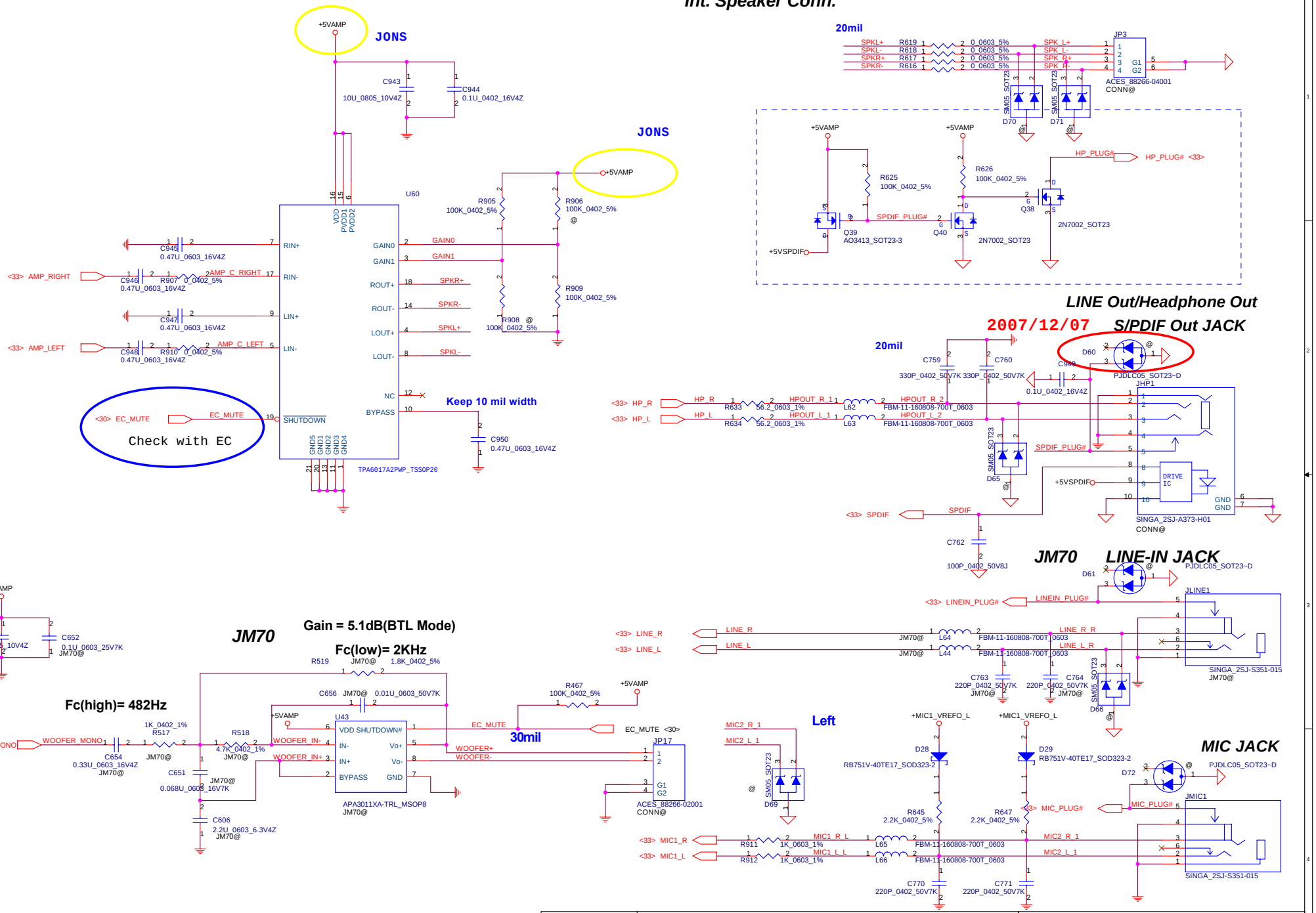
Compal Electronics, Inc.

Title: HD Audio Codec ALC268

Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 33 of 46

Int. Speaker Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

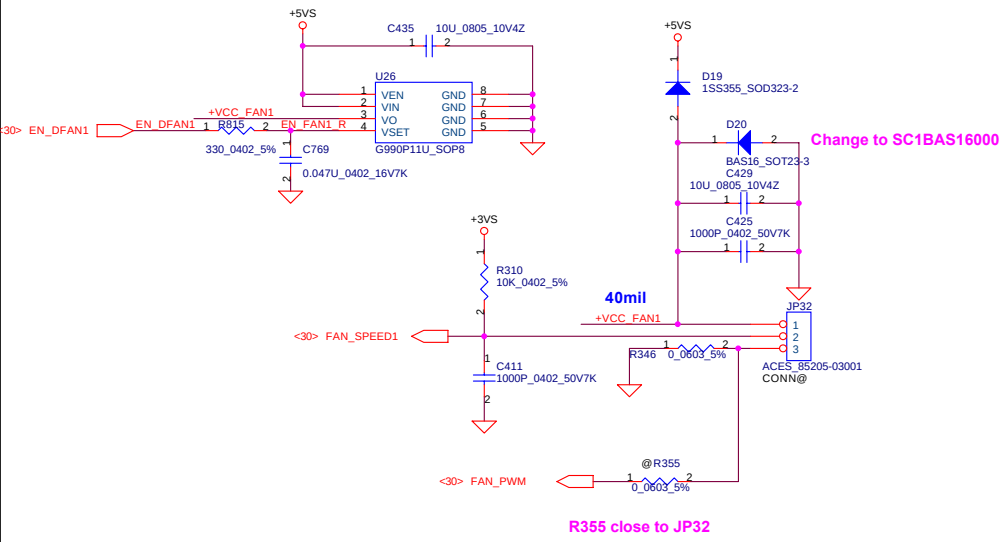
Compal Electronics, Inc.

Title: Amplifier & Audio Jack

Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 34 of 46

FAN1 Conn



R355 close to JP32

H1 H_3P0 @
H2 H_3P0 @
H3 H_3P0 @
H4 H_3P0 @
H5 H_3P0 @
H6 H_3P0 @
H7 H_3P0 @
H8 H_3P0 @
H9 H_3P0 @
H10 H_3P0 @
H11 H_3P0 @
H12 H_3P0 @
H29 H_3P0 @
H42 H_3P0 @
H17 H_3P2 @
H18 H_3P2 @
H23 H_3P2 @
H26 H_3P2 @
H32 H_3P2 @
H25 H_3P2 @
H27 H_3P2 @
H40 H_3P2 @
H41 H_3P2 @
H35 H_3P2 @
H38 H_3P2 @
H39 H_3P2 @
H19 H_4P2 @
H20 H_4P2 @
H21 H_4P2 @
H22 H_4P2 @
H31 H_4P1N @
H28 H_4P1X4P6N @
H43 H_10P0N @
FD1 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80
FD5 FIDUCIAL_C40M80
FD6 FIDUCIAL_C40M80

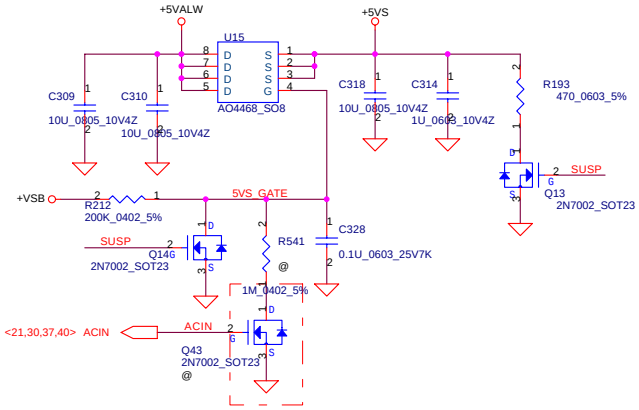
Compal Electronics, Inc.

Title: FAN & Screw Hole

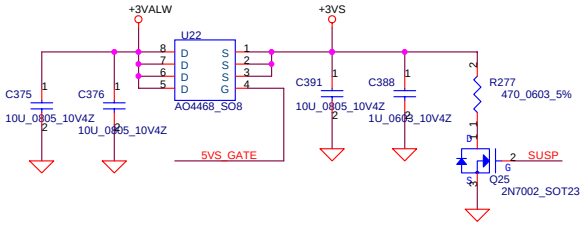
Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 35 of 46

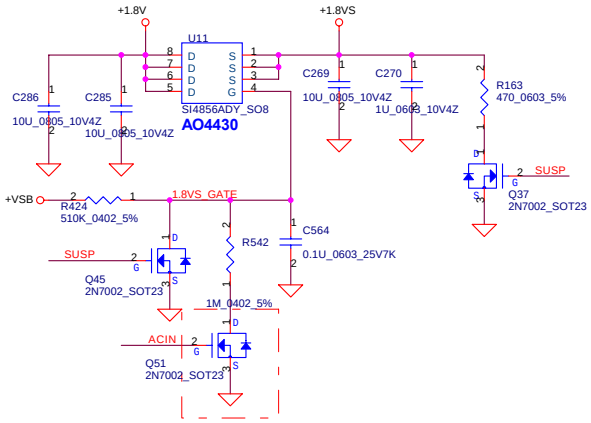
+5VALW TO +5VS

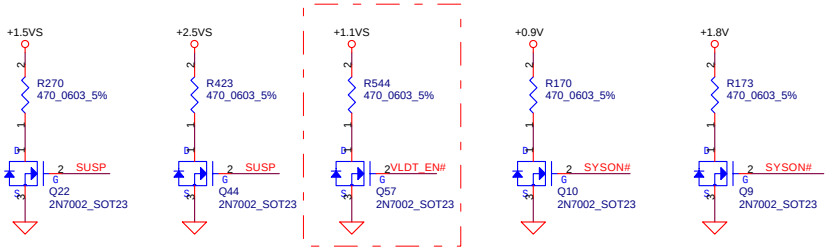


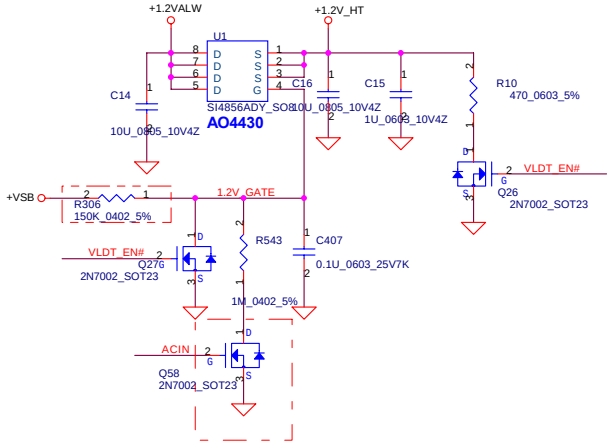
+3VALW TO +3VS

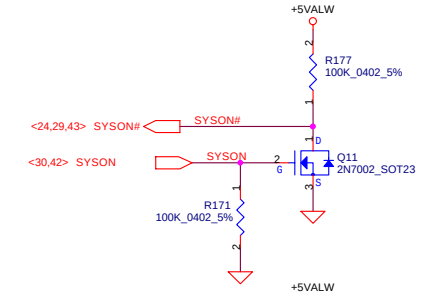


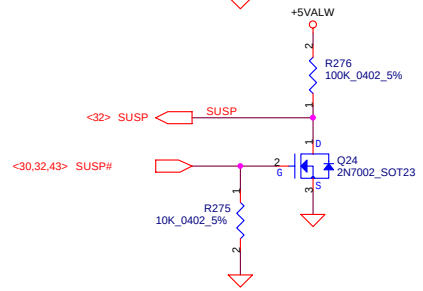
+1.8V to +1.8VS

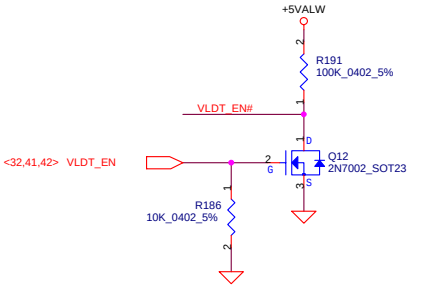












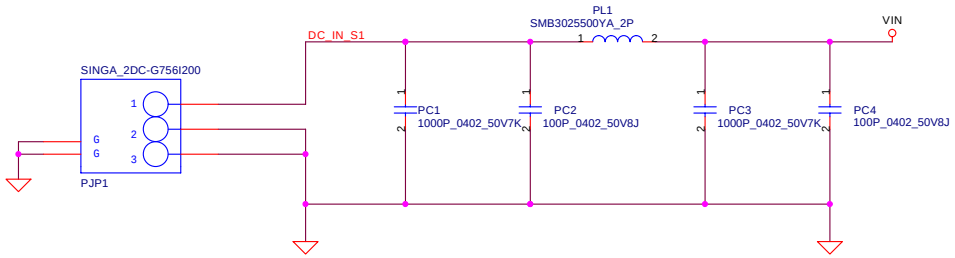
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

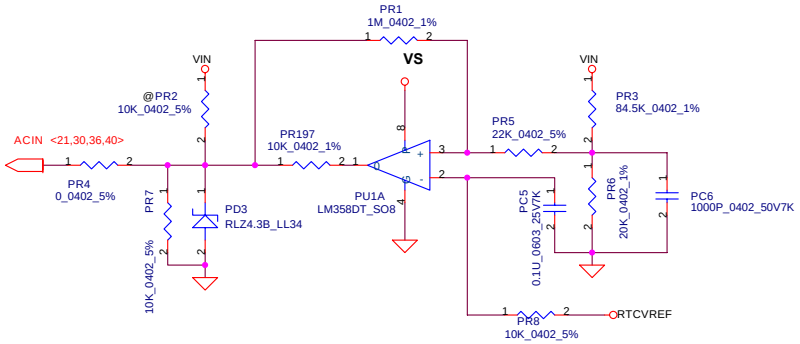
Compal Electronics, Inc.

Title: DC Interface

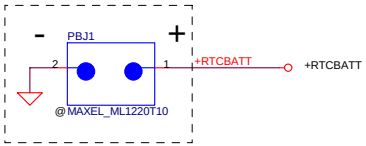
Size	Document Number	Rev
B	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 | Sheet 36 of 46





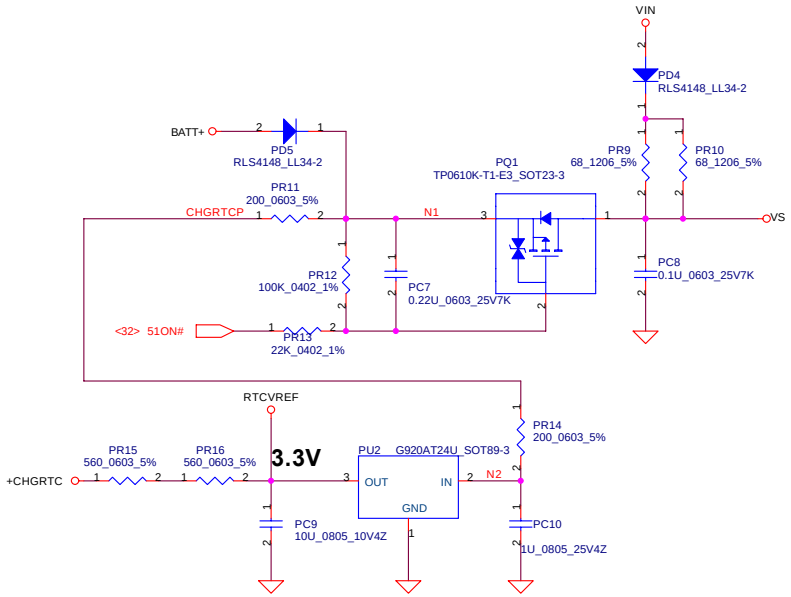
RTC Battery

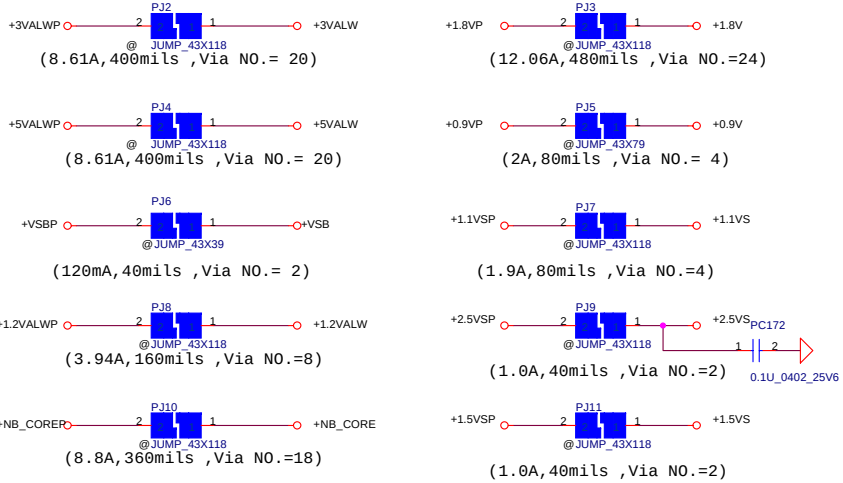


SP093MX0000

Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





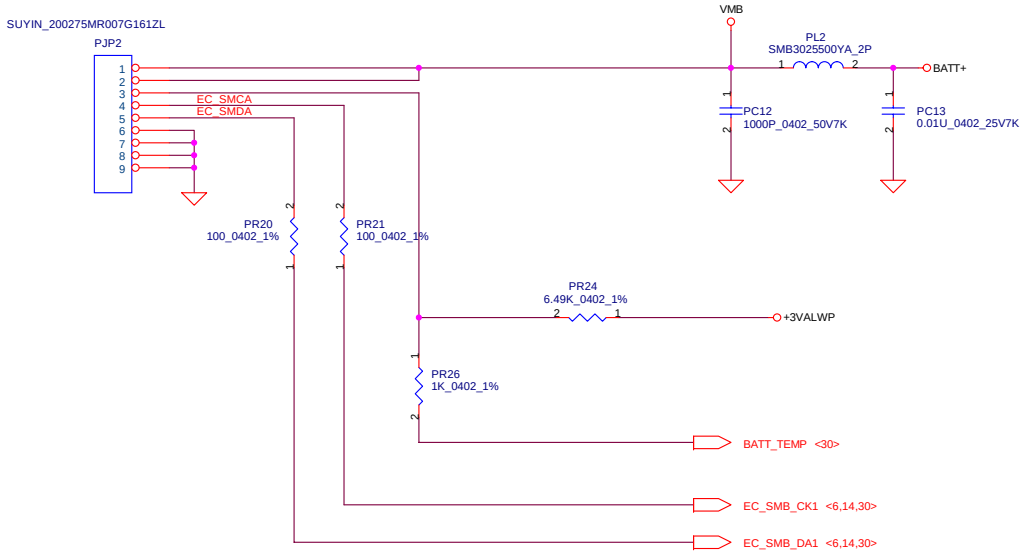
Compal Electronics, Inc.

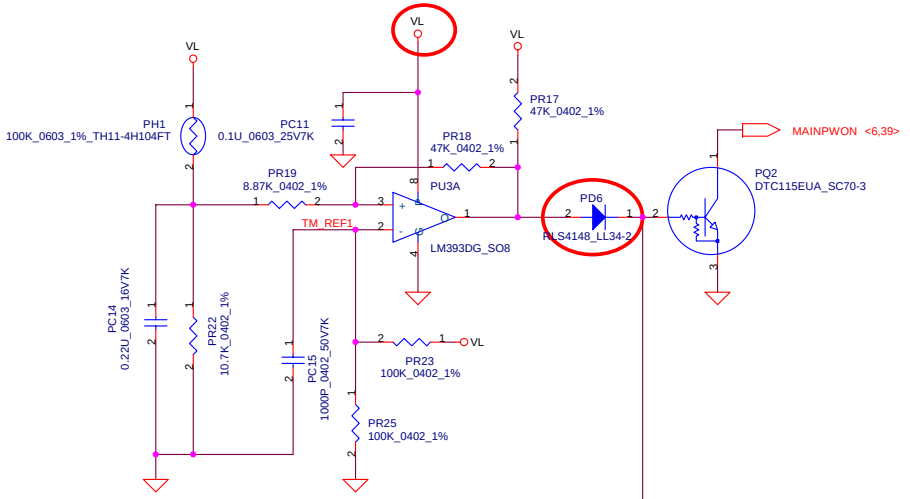
Title: DCIN & DETECTOR

Size | Document Number: KBKC0_KBYF0 | Rev: 0.3

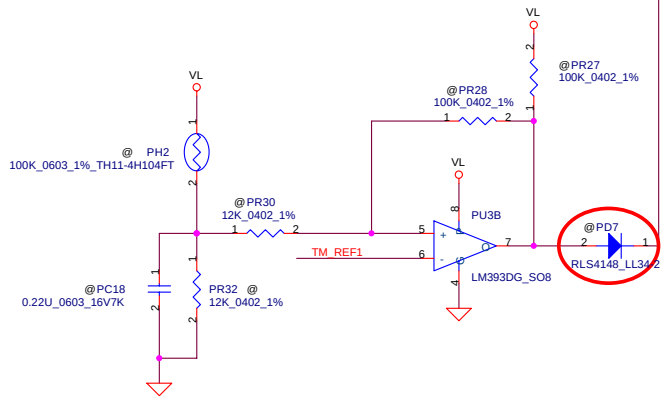
Date: Tuesday, February 03, 2009 | Sheet 37 of 46

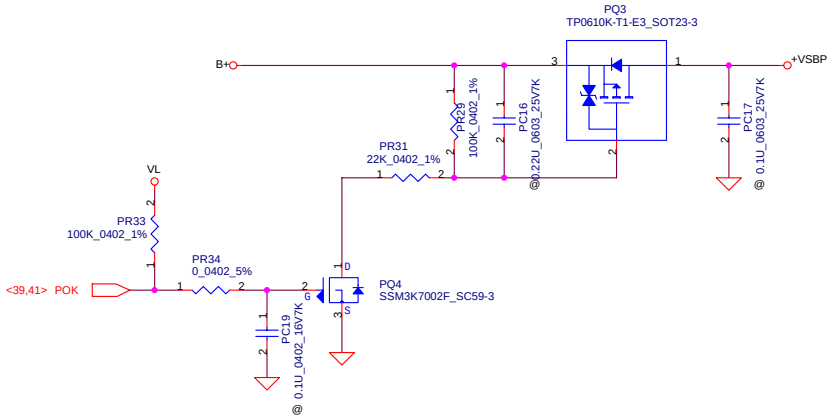
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C





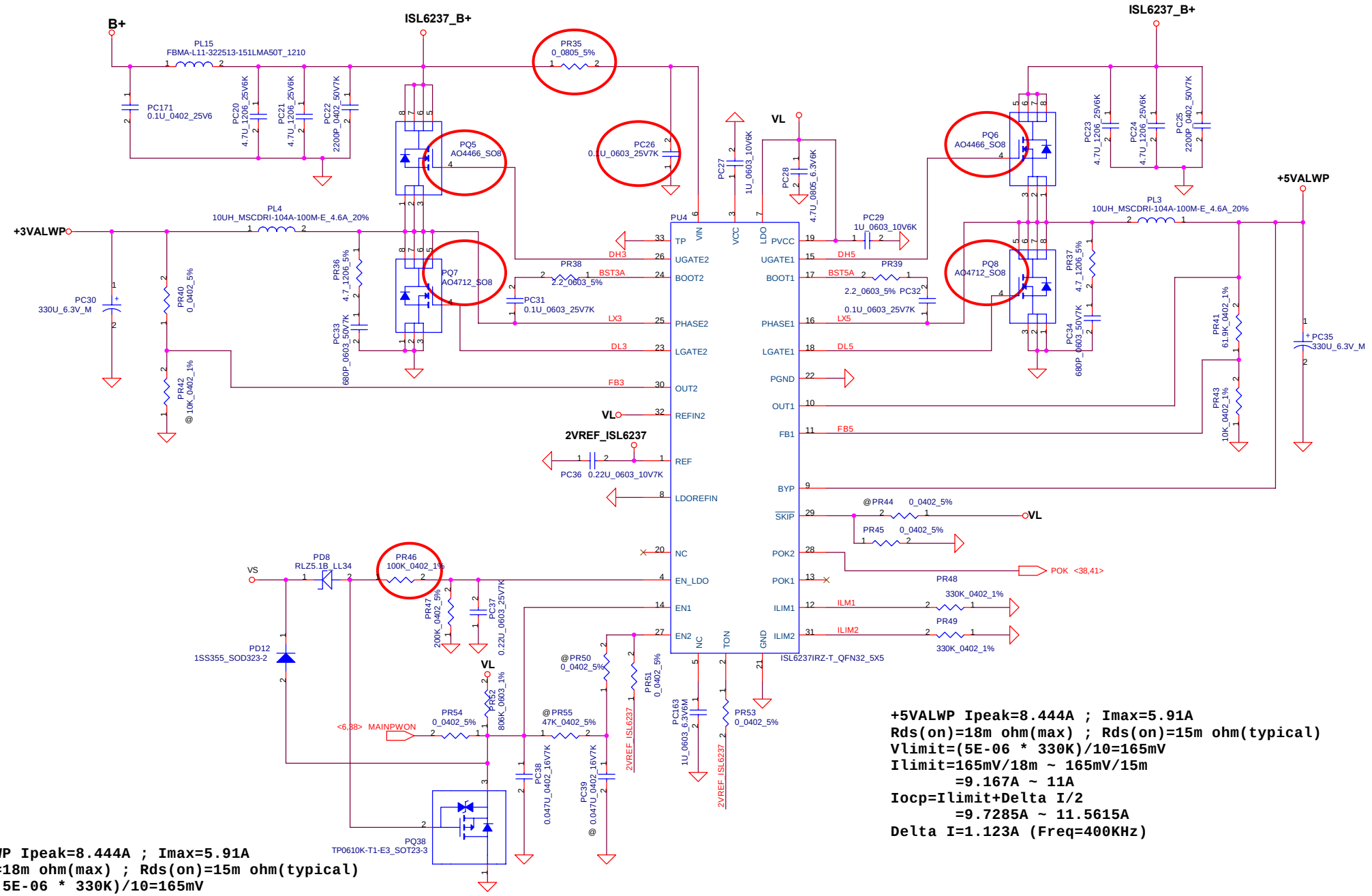
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
	KBKC0_KBYF0	0.3

Date: Tuesday, February 03, 2009 | Sheet 38 of 46



+5VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.7285A ~ 11.5615A
Delta I=1.123A (Freq=400KHz)

+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.721A ~ 11.554A
Delta I=1.108A (Freq=300KHz)

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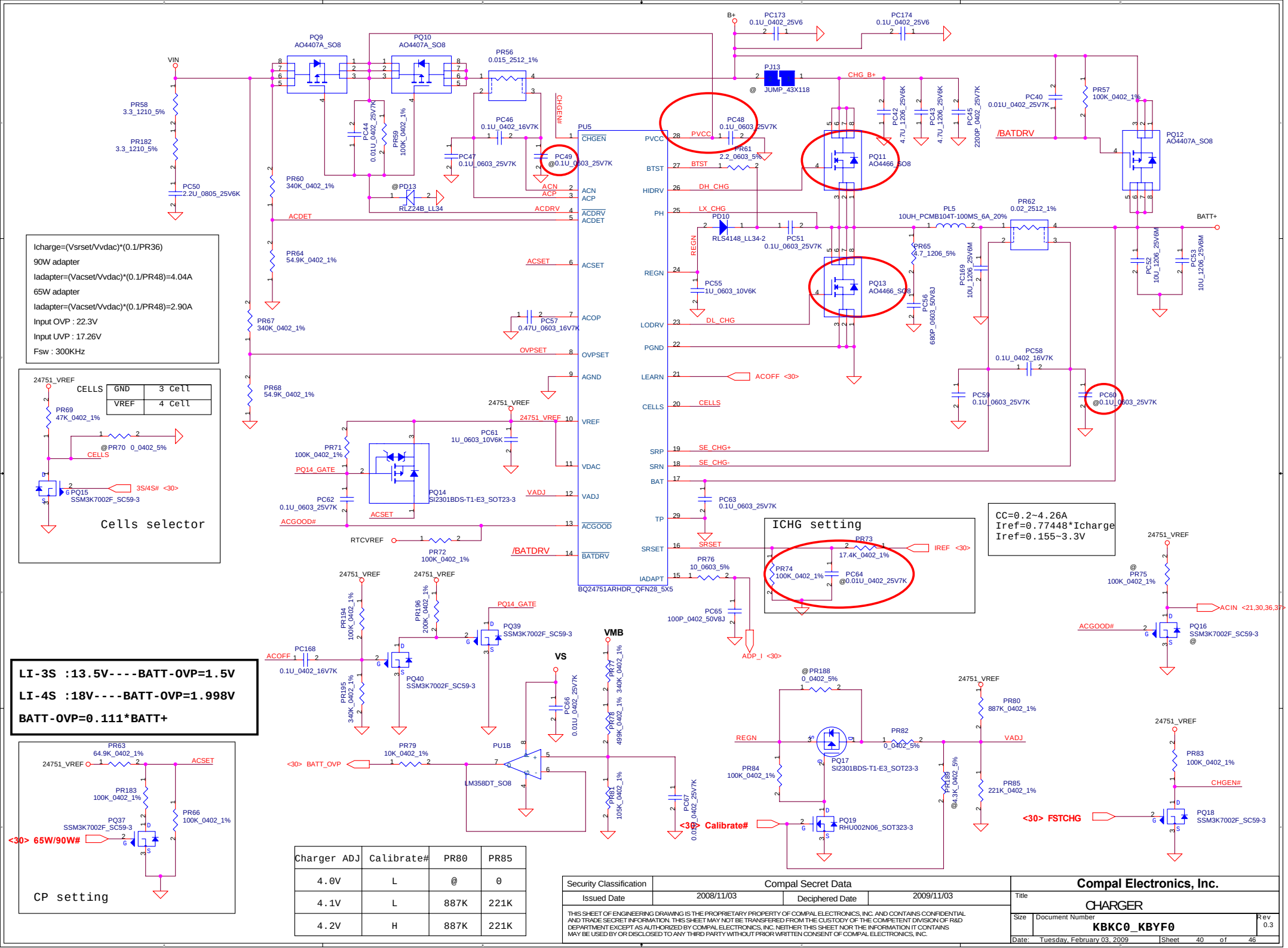
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: +5V/+3V

Size: Custom | Document Number: KBKC0_KBYF0 | Rev: 0.3

Date: Tuesday, February 03, 2009 | Sheet 39 of 46


Icharge=(Vsrset/Vvdac)*(0.1/PR36)
90W adapter
Iadapter=(Vacset/Vvdac)*(0.1/PR48)=4.04A
65W adapter
Iadapter=(Vacset/Vvdac)*(0.1/PR48)=2.90A
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz
Cells selector
CELLS | GND | 3 Cell
VREF | 4 Cell
ICHG setting
CC=0.2~4.26A
Iref=0.77448*Icharge
Iref=0.155~3.3V
LI-3S :13.5V----BATT-OVP=1.5V
LI-4S :18V----BATT-OVP=0.111*BATT+
CP setting
Charger ADJ | Calibrate# | PR80 | PR85
4.0V | L | @ | 0
4.1V | L | 887K | 221K
4.2V | H | 887K | 221K
Security Classification | Compal Secret Data
Issued Date | 2008/11/03 | Deciphered Date | 2009/11/03
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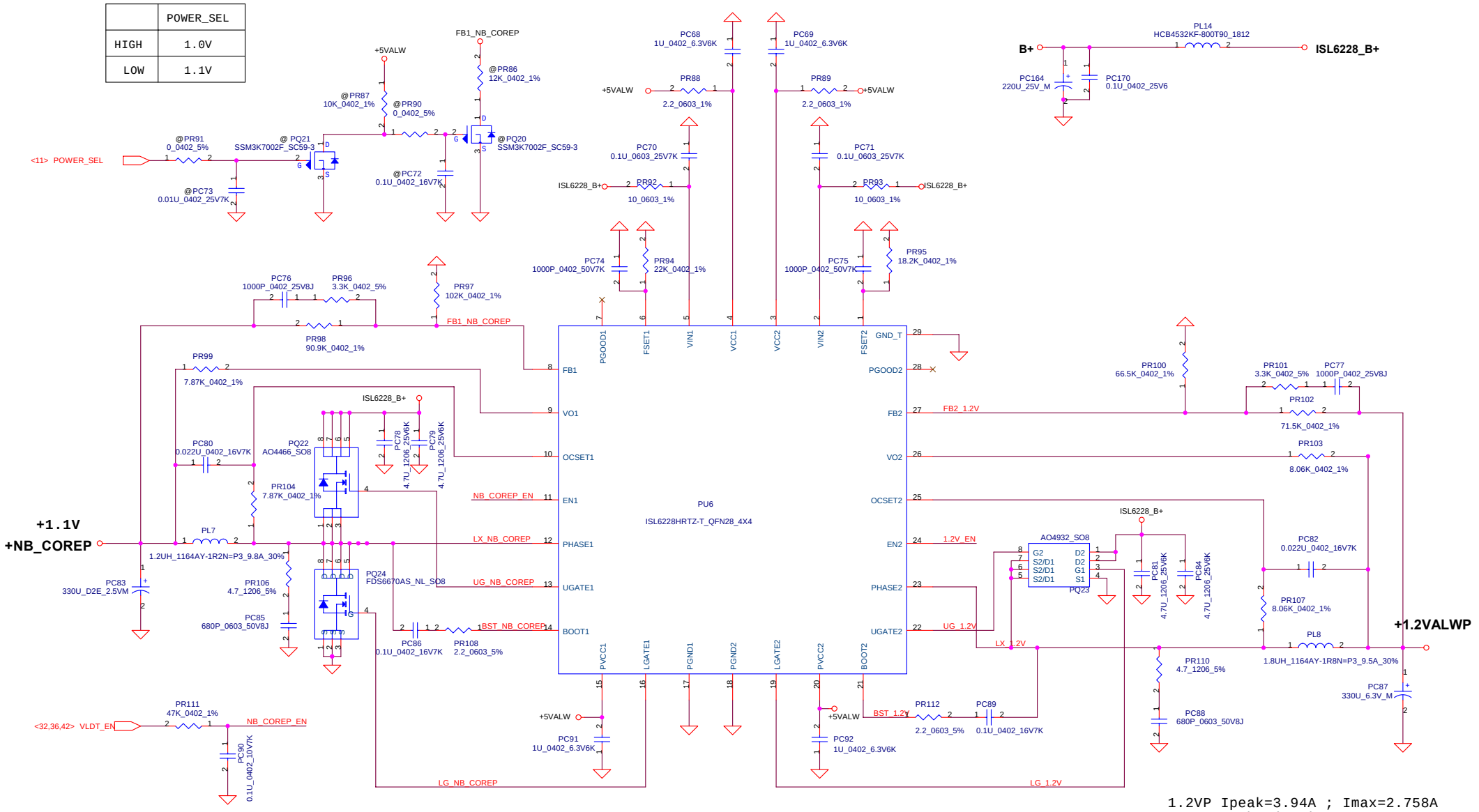
Title
CHARGER
Size
Document Number
KBKC0_KBYF0
Rev
0.3
Date: Tuesday, February 03, 2009
Sheet 40 of 46

	POWER_SEL
HIGH	1.0V
LOW	1.1V



1.1VP Ipeak=8.9A ; Imax=6.23A
DCR=6m ohm (max)
Rocset=(Iocp*DCR)/10E-06=7.68K ohm
Iocp=9.846A(1.3*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=303KHz
Rfset=1/(1.5E-10 * Freq)=22K

1.2VP Ipeak=3.94A ; Imax=2.758A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=6.65K ohm
Iocp=5.542A(1.2*DCR)
Csen=L/(Rocset*DCR)=0.027uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

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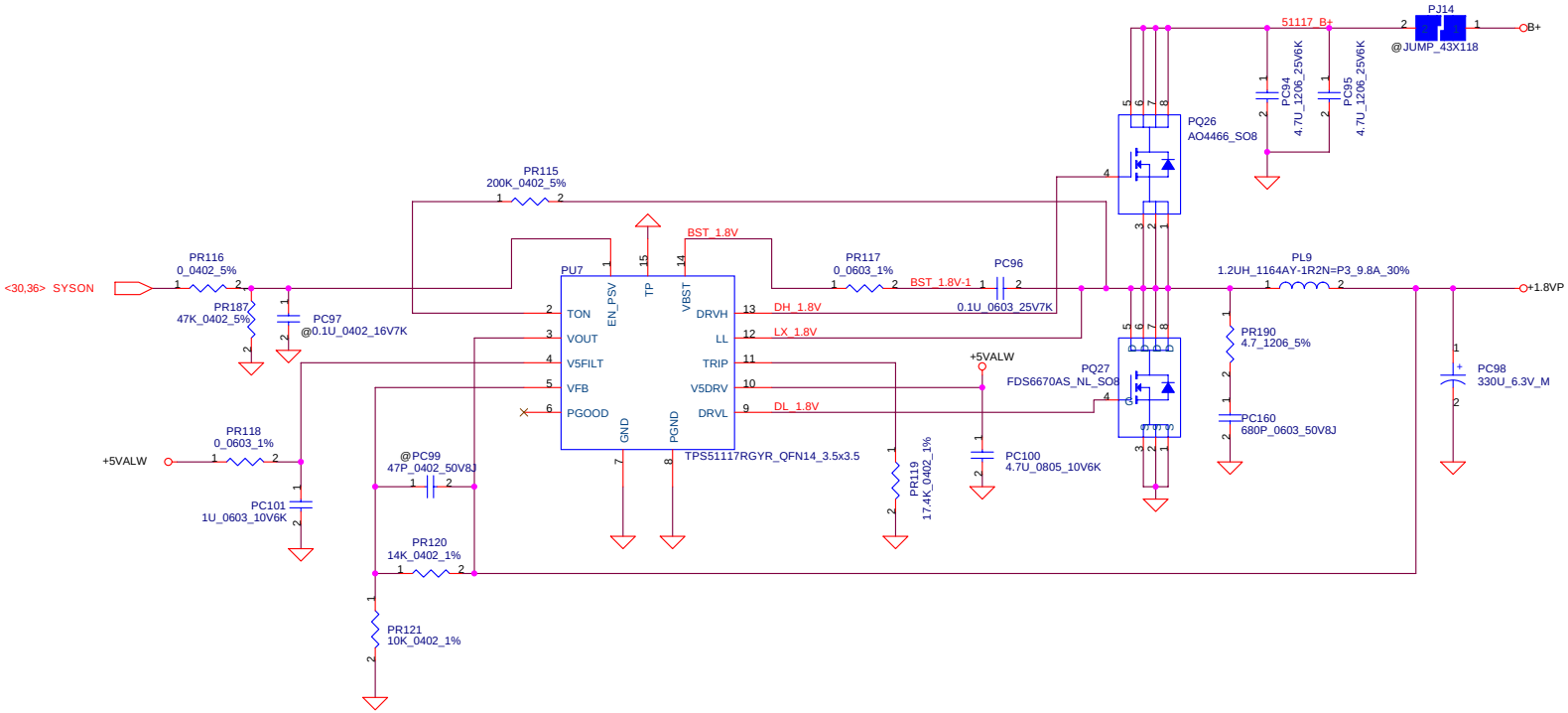
Title: NB_COREP / 1.2VSB

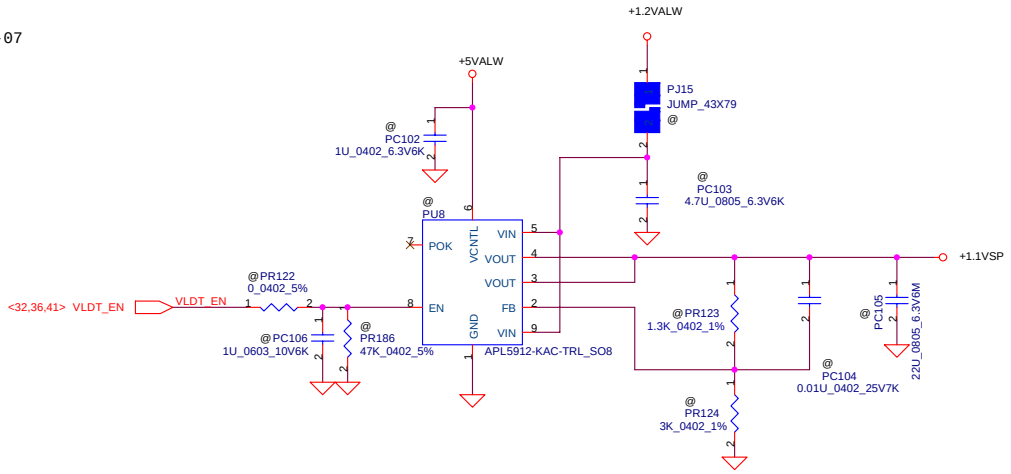
Size	Document Number	Rev
	KBKC0_KBYF0	0.3

Date: Tuesday, February 03, 2009 | Sheet 41 of 46



VFB=0.75V
Vo=VFB*(1+PR120/PR121)=1.8V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=3.1E-07
Freq=305KHz

Cesr=15m ohm
Ipeak=12.6A Imax=8.82A
Delta I=((19-1.8)*(1.8/19))/(L*Freq)=5.332A
Vtrip=Rtrip*10uA=0.24V
Iocp-min=Vtrip/Rdsonmax*1.4+2.666=17.573A
Iocp-max=Vtrip/Rdsontyp*1.2+2.666=26.908A
Iocp=17.573~26.908A



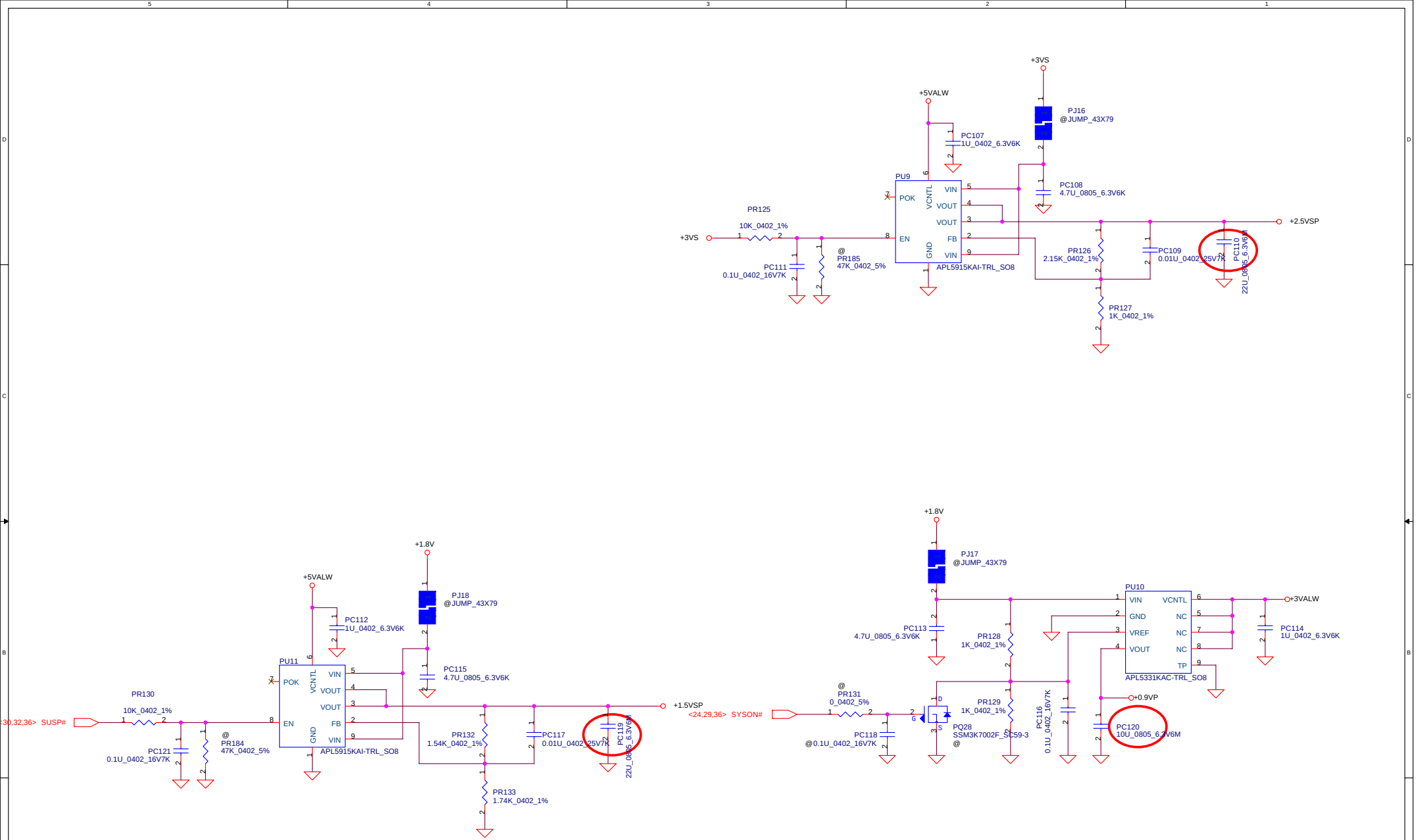
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: 1.8VSP/+1.1VSP

Size	Document Number	Rev
	KBKC0_KBYF0	0.3

Date: Tuesday, February 03, 2009 | Sheet 42 of 46



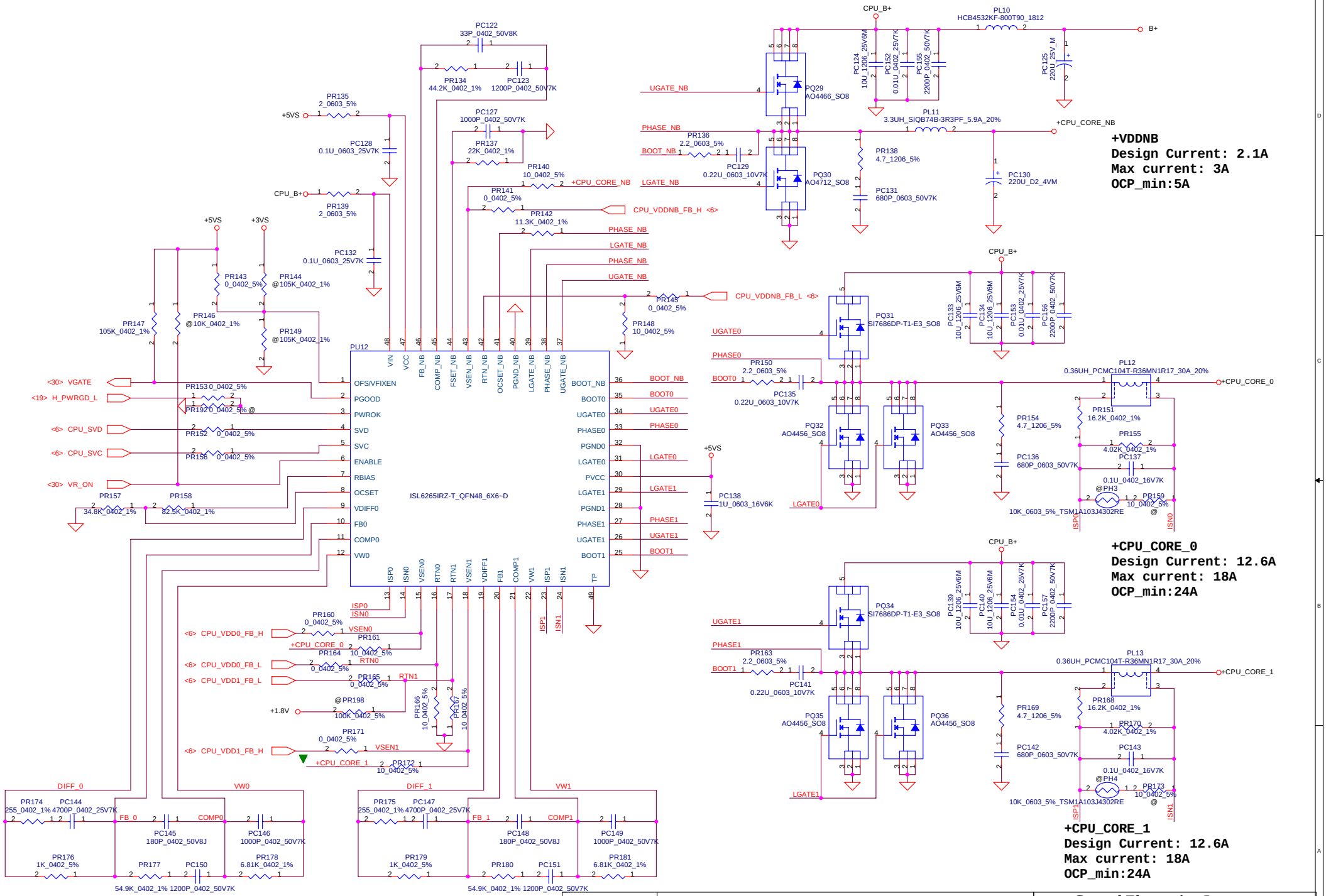
Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: 0.9VP//1.5VSP/2.5VSP

Size	Document Number	Rev
	KBKC0_KBYF0	0.3

Date: Tuesday, February 03, 2009 | Sheet 43 of 46



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Issued Date	2008/11/03	Deciphered Date	2009/11/03

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Title	+CPU_CORE
Size	Custom
Document Number	KBKC0_KBYF0
Rev	0.3
Date:	Tuesday, February 03, 2009
Sheet	44 of 46

Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	EMI request.	EMI request.	0.1	40	Change PR38,PR39,PR108,PR112,PR136,PR150,PR163 from SD013000080 to SD013220B80.	08, 12/24	to DVT
2	EMI request.	EMI request.	0.1	40	Add PC170,PC171,PC172,PC173,PC174 SE00000G880 S CER CAP 0.1U 25V K X5R 0402	08, 12/24	to DVT
3	EMI request.	EMI request.	0.1	39	Add PL15 SM010016410 S SUPPRE_ KC FBMA-L11-322513-151LMA50T	08, 12/24	to DVT
4	EMI request.	EMI request.	0.1	41	Add PL14 SM010018210 S SUPPRE_ TAI-TECH HCB4532KF -800T90 1812	08, 12/24	to DVT
5	Link CIS error.	Link CIS error.	0.1	40	Change PQ9, PQ10, PQ12 from SB944070000 S TR AO4407 1P SO8 W/D to SB00000DL00 S TR AO4407A 1P SO8	08, 12/24	to DVT
6	cost down	cost down	0.1	40	Change PC30 from SGA19331360 S POLY C 330U 6.3V M D3L ESR25M TPE H2.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
7	cost down	cost down	0.1	40	Change PC35 from SGA20151320 S POLY C 150U 6.3V M D2E TPE ESR18 H1.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
8	cost down	cost down	0.1	41, 42	Change PC87, PC98 from SGA19331D00 S POLY C 330U 2.5V M D2 TPE LESR15M H1.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
9	schematic update.	schematic update.	0.1	44	Delete PR198 SD028100380 S RES 1/16W 100K +-5% 0402	08, 12/24	to DVT
10	layout space too small.	layout space too small.	0.1	41	Change PQ23 from SB00000CG00 S TR AO4466 1N SO8 to SB00000BG00 S TR AO4932 2N SO8 Delete PQ25 SB00000AJ00 S TR AO4712 1N SO8	08, 12/24	to DVT
11							
12							
13							
14							
15							
16							
17							
18							

Security Classification	Compal Secret Data		
Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: PIR List

Size: Custom | Document Number: KBKC0_KBYF0 | Rev: 0.3

Date: Tuesday, February 03, 2009 | Sheet 45 of 46

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	12/17	p.12	L3,L4 change from bead to 0 Ohm	
	12/17	P.17	Add R858~R865 for VGA HDMI	
	12/17	P.18	R374,R375,R376 change from 0 ohm to 10 ohm	
	12/17	P.20	R50 ,R53 change from JV70@ to @	
	12/17	P.20	R51 ,R52 change from JM70@ to JV70@	
	12/17	P.24	JP18 change from ESATA to USB port	
	12/17	P.25	R396 change from 10K to 0 Ohm	
	12/17	P.31	C905~C907 change from 0.1u to 33P	
	12/17	P.31	U19 change from mount to @ ; U18 change from @ to mount	
	12/17	P.32	D22 change from mount to @	
	12/18	P.24	SATA re-driver IC reserved	
	12/22	P.8	Add c124,c128,c151,c155,c55,c119,c113,c197 0.1uF	EMI request
	12/22	P.30	Add c40 c41 100P	EMI request
	12/22	P.30	Add c42,c43,c45	EMI request
	12/22	P.37~p.45	upgrade PWR schematic	
	12/22	P.30	Add C65 22uF for CRT flicker	
	12/23	P.21	Delete R174,R175	
	01/16	P.16	Add r611,r612 connect to INVT_PWM	Vari-Bright reserved
	01/16	P.11	Add r347 connect to BKOFF#	Vari-Bright reserved
	01/16	P.30	add r288 BKOFF# 4.7k pull low	

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Issued Date	2008/11/03	Deciphered Date	2009/11/03

Compal Electronics, Inc.

Title: **HW PIR**

Size	Document Number	Rev
	KBYF0 LA-5051P	0.3

Date: Tuesday, February 03, 2009 Sheet 46 of 46