Compal Confidential

PAWF5/F6 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2010-02-03

REV:0.1

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Title	Cover Page	
Size: Custom	Document Number: NAWF3 M/B LA-4854P Schematic	Rev: 1.0
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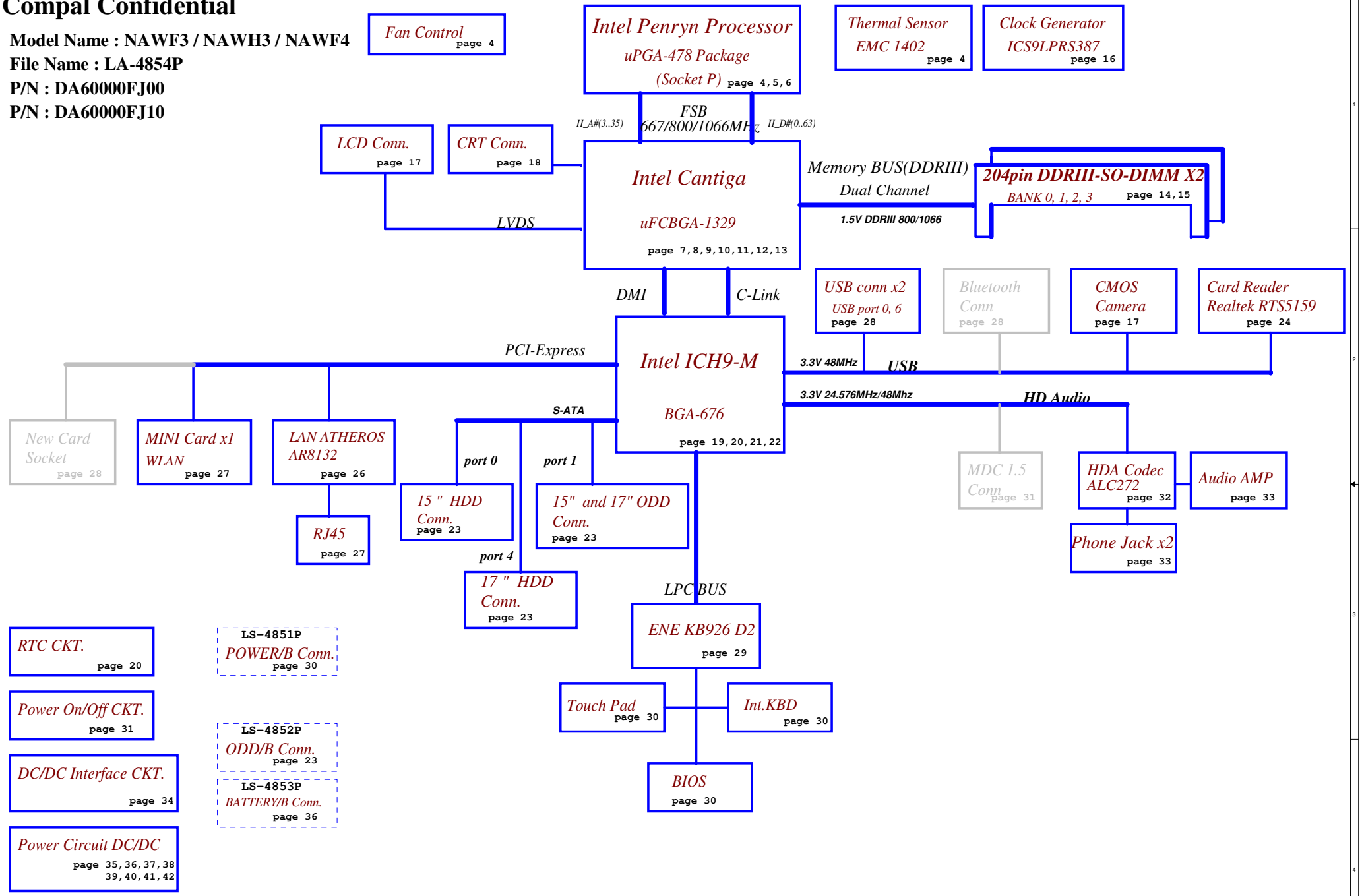
Model Name : NAWF3 / NAWH3 / NAWF4
File Name : LA-4854P
P/N : DA60000FJ00
P/N : DA60000FJ10



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Issued Date	2009/08/25	Deciphered Date	2010/08/25
Title	Block Diagrams		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for LVDS	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADT7421	1001 100X b

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	0.1 (PVT)
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45	GM@
GL40	GL@
PAWF5	F5@
PAWF7	F7@
8114	8114@
8132	8132@

USB table

EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	
	UHCI2	Port2	
		Port3	CMOS Camera
	UHCI3	Port4	Card Reader
		Port5	New Card(Reserved)
EHCI2	UHCI4	Port6	MB USB Conn.
		Port7	
	UHCI5	Port8	Blue Tooth
		Port9	
	UHCI6	Port10	Wireless Card
		Port11	

PCIE table

PCIE port1	Express Card(Reserved)
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	for 17" 2nd HDD
SATA port5	

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Title	Notes List		
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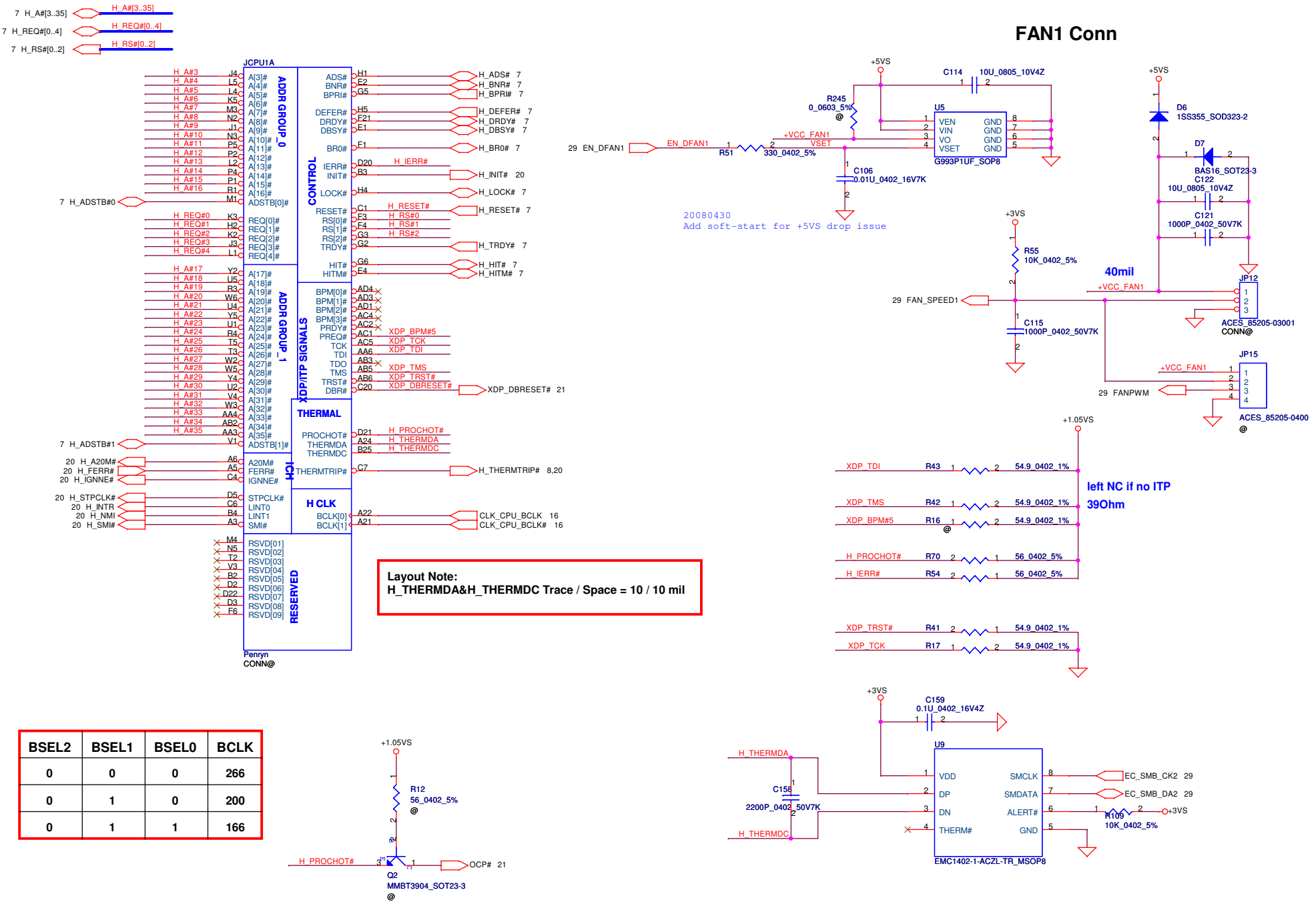

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

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Title	Penryn (1/3) & FAN		
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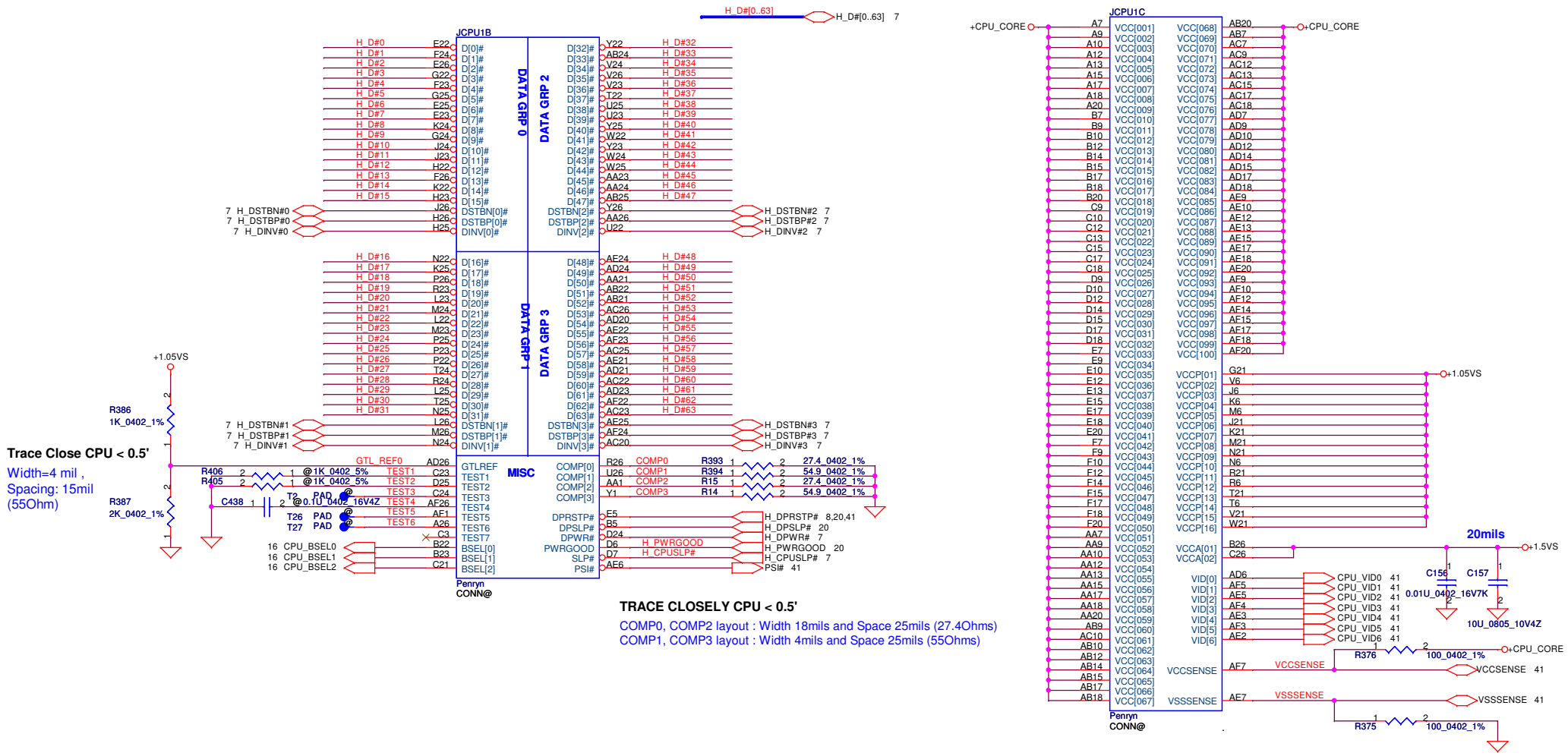

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Compal Electronics, Inc.

Title: Penryn (2/3)

Size: B | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

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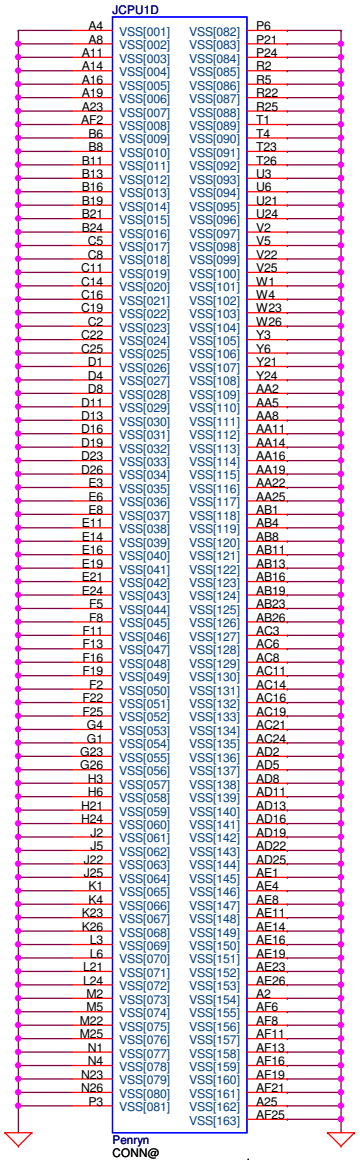
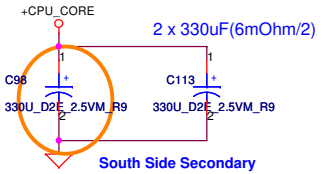
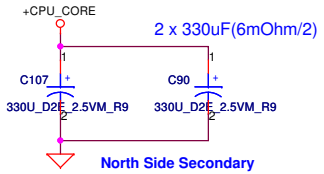
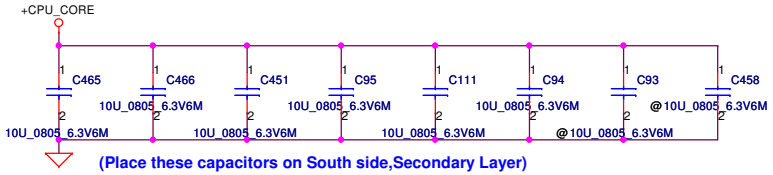
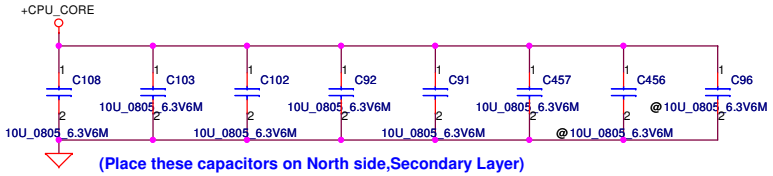
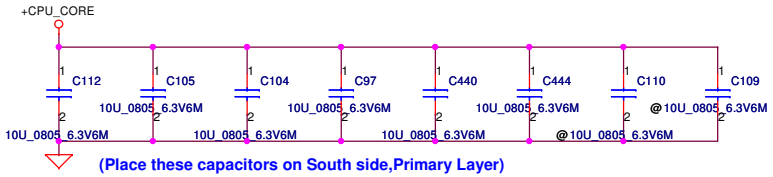


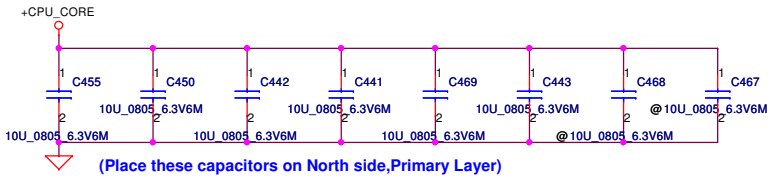




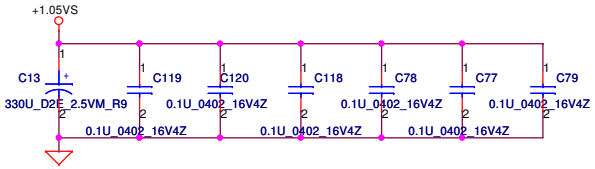








+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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Compal Electronics, Inc.

Title: Penryn (3/3)

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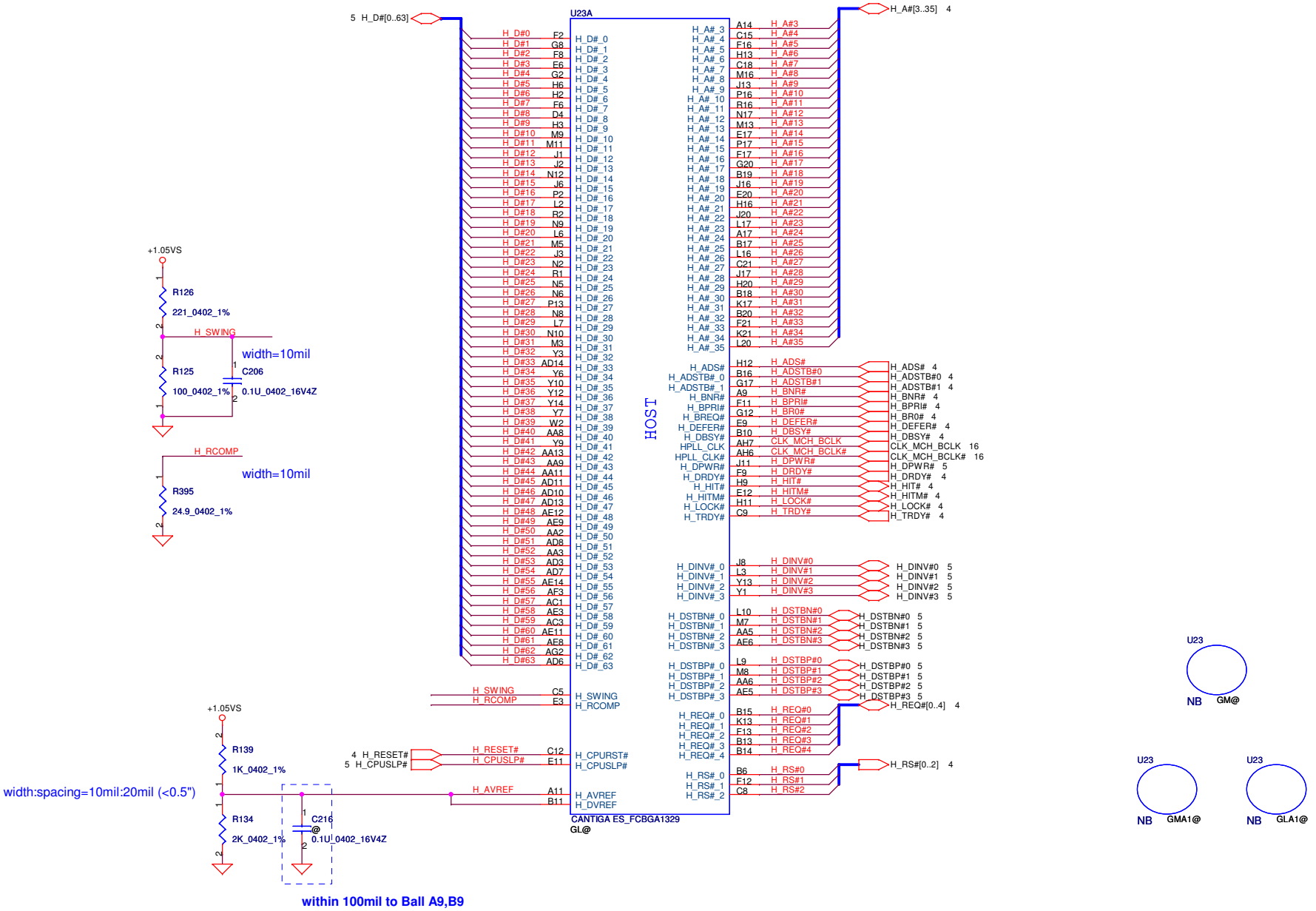

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Compal Electronics, Inc.

Title: Cantiga GMCH(1/7)-GTL

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All RSVD balls on GMCH should be left No Connect.

U23B

RSVD: M36 RSVD1, N36 RSVD2, R33 RSVD3, T33 RSVD4, AH9 RSVD5, AH10 RSVD6, AH12 RSVD7, AH13 RSVD8, K12 RSVD9, AL34 RSVD10, AK34 RSVD11, AN35 RSVD12, AM35 RSVD13, T24 RSVD14; R31 RSVD15, B2 RSVD16, M1 RSVD17; AY21 RSVD20; BG23 RSVD22, BF23 RSVD23, BH18 RSVD24, BF18 RSVD25

CLK DDR CLK/ CONTROL/ COMPENSATION: SA_CK_0 AP24, SA_CK_1 AT21, SB_CK_0 AV24, SB_CK_1 AU20 → DDRA_CLK0 14, DDRA_CLK1 14, DDRB_CLK0 15, DDRB_CLK1 15; SA_CK#_0 AR24, SA_CK#_1 AR21, SB_CK#_0 AU24, SB_CK#_1 AV20 → DDRA_CLK0# 14, DDRA_CLK1# 14, DDRB_CLK0# 15, DDRB_CLK1# 15; SA_CKE_0 BC28, SA_CKE_1 AY28, SB_CKE_0 AY36, SB_CKE_1 BB36 → DDRA_CKE0 14, DDRA_CKE1 14, DDRB_CKE0 15, DDRB_CKE1 15; SA_CS#_0 BA17, SA_CS#_1 AY16, SB_CS#_0 AV16, SB_CS#_1 AR13 → DDRA_SCS0# 14, DDRA_SCS1# 14, DDRB_SCS0# 15, DDRB_SCS1# 15; SA_ODT_0 BD17, SA_ODT_1 AY17, SB_ODT_O BF15, SB_ODT_1 AY13 → DDRA_ODT0 14, DDRA_ODT1 14, DDRB_ODT0 15, DDRB_ODT1 15

DDR3

SM_DRAMRST# would be needed for DDR3 only

For Cantiga 80 Ohm

SM_RCOMP BG22 SMRCOMP → R368 80.6_0402_1%; SM_RCOMP# BH21 SMRCOMP# → R367 80.6_0402_1%

SM_RCOMP_VOH BF28 → R363 1K_0402_1% → +1.5V; SM_RCOMP_VOH → R369 3.01K_0402_1% → C419 2.2U_0603_6.3V6K → C423 0.01U_0402_16V7K

SM_RCOMP_VOL BH28 → R362 1K_0402_1% → C418 2.2U_0603_6.3V6K → C422 0.01U_0402_16V7K

SM_VREF AV42 → R220 1K_0402_1% <BOM Structure> → R221 0_0402_5% → +DIMM_VREF; R222 1K_0402_1% <BOM Structure>; C278 0.1U_0402_16V4Z

20mil

SM_PWROK AR36, SM_REXT BF17 → R366 499_0402_1% → SM_PWROK_31

SM_DRAMRST# BC36 → SM_DRAMRST# 14,15

CLK_DREF_96M B38, CLK_DREF_96M# A38, CLK_DREF_SSC E41, CLK_DREF_SSC# F41 → CLK_DREF_96M 16, CLK_DREF_96M# 16, CLK_DREF_SSC 16, CLK_DREF_SSC# 16

DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#

CLK_MCH_3GPLL F43, CLK_MCH_3GPLL# E43 → CLK_MCH_3GPLL 16, CLK_MCH_3GPLL# 16

PEG_CLK, PEG_CLK#

CFG: 16 MCH_CLKSEL0 → MCH_CLKSEL0 T25, 16 MCH_CLKSEL1 → MCH_CLKSEL1 R25, 16 MCH_CLKSEL2 → MCH_CLKSEL2 P25; CFG_0 … CFG_20

+3VS → R177 10K_0402_5% PM_EXTTS#0; R202 10K_0402_5% PM_EXTTS#1; R189 10K_0402_5% MCH_CLKREQ#

MCH_CFG_5 C25, MCH_CFG_6 N24, MCH_CFG_7 M24, MCH_CFG_9 C23, MCH_CFG_10 C24, MCH_CFG_12 P21, MCH_CFG_13 T21, MCH_CFG_16 L21, MCH_CFG_19 R28, MCH_CFG_20 T28

16,21,41 VGATE → R224 @0_0402_5% → GMCH_PWROK

21 ICH_PWROK → R223 0_0402_5%

DMI: DMI_RXN_0 AE41, DMI_RXN_1 AE37, DMI_RXN_2 AE47, DMI_RXN_3 AH39 → DMI_ITX_MRX_N0 … N3; DMI_RXP_0 AE40, DMI_RXP_1 AE38, DMI_RXP_2 AE48, DMI_RXP_3 AH40 → DMI_ITX_MRX_P0 … P3; DMI_TXN_0 AE35, DMI_TXN_1 AE43, DMI_TXN_2 AE46, DMI_TXN_3 AH42 → DMI_MTX_IRX_N0 … N3; DMI_TXP_0 AD35, DMI_TXP_1 AE44, DMI_TXP_2 AF46, DMI_TXP_3 AH43 → DMI_MTX_IRX_P0 … P3

GRAPHICS VID: GFX_VID_0 B33, GFX_VID_1 B32, GFX_VID_2 G33, GFX_VID_3 F33, GFX_VID_4 E33; GFX_VR_EN C34

PM: 21 PM_SYNC# → R141 0_0402_5% → PM_SYNC# R29; 5,20,41 H_DPRSTP# → R135 0_0402_5% → PM_DPRSTP# R B7; 14 PM_EXTTS#0 → PM_EXTTS#0 N33; 15 PM_EXTTS#1 → PM_EXTTS#1 P32; GMCH_PWROK AT40; 19,25,29 PLT_RST# → R133 100_0402_5% → MCH_RSTIN# AT11; 4,20 H_THERMTRIP# → R143 0_0402_5% → THERMTRIP# R T20; 21,41 PM_DPRSLPVR → R140 0_0402_5% → DPRSLPVR_R R32

PM_SYNC#, PM_DPRSTP# B7, PM_EXT_TS#_0 N33, PM_EXT_TS#_1 P32, PWROK AT40, RSTIN# AT11, THERMTRIP# T20, DPRSLPVR R32

ME: CL_CLK AH37, CL_DATA AH36, CL_PWROK AN36, CL_RST# AJ35, CL_VREF AH34 → CL_CLK0 21, CL_DATA0 21, CL_RST#0 21

+1.05VS → R183 1K_0402_1%; R182 511_0402_1%; C264 0.1U_0402_16V4Z

MISC: DDPC_CTRLCLK N28, DDPC_CTRLDATA M28, SDVO_CTRLCLK G36, SDVO_CTRLDATA E36, CLKREQ# K36 → MCH_CLKREQ# 16, ICH_SYNC# H36 → MCH_ICH_SYNC# 21; TSATN# B12 → MCH_TSATN#

HDA: HDA_BCLK B28, HDA_RST# B30, HDA_SDI B29, HDA_SDO C29, HDA_SYNC A28

NC: BG48 NC_1, BF48 NC_2, BD48 NC_3, BC48 NC_4, BH47 NC_5, BG47 NC_6, BE47 NC_7, BH46 NC_8, BF46 NC_9, BG45 NC_10, BH44 NC_11, BH43 NC_12, BH6 NC_13, BH5 NC_14, BG4 NC_15, BH3 NC_16, BF3 NC_17, BH2 NC_18, BG2 NC_19, BE2 NC_20, BG1 NC_21, BF1 NC_22, BD1 NC_23, BC1 NC_24, F1 NC_25, A47 NC_26

CANTIGA ES_FCBGA1329

GL@

+1.05VS → R398 54.9_0402_1% → R397 330_0402_5% → MCH_TSATN#

+3VS → R403 1K_0402_5% → Q34 MMBT3904_SOT23-3; R404 1K_0402_5% → Q33 MMBT3904_SOT23-3 → MCH_TSATN_EC# 29

Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable * (Default) 1 = LFP Card Present; PCIE disable
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present

MCH_CFG_5 R175 @2.21K_0402_1%; MCH_CFG_6 R142 @4.02K_0402_1%; MCH_CFG_7 R162 @2.21K_0402_1%; MCH_CFG_9 R158 @2.21K_0402_1%; MCH_CFG_10 R161 @2.21K_0402_1%; MCH_CFG_12 R154 @2.21K_0402_1%; MCH_CFG_13 R153 @2.21K_0402_1%; MCH_CFG_16 R155 @2.21K_0402_1%

MCH_CFG_19 R159 @4.02K_0402_1%; MCH_CFG_20 R163 @4.02K_0402_1% → +3VS

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Title: Cantiga GMCH(2/7)-DMI/DDR

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14 DDR_A_D[0..63] → DDR_A_D[0..63]
14 DDR_A_DM[0..7] → DDR_A_DM[0..7]
14 DDR_A_MA[0..14] → DDR_A_MA[0..14]
14 DDR_A_DQS#[0..7] → DDR_A_DQS#[0..7]

15 DDR_B_D[0..63] → DDR_B_DQ[0..63]
15 DDR_B_DM[0..7] → DDR_B_DM[0..7]
15 DDR_B_MA[0..14] → DDR_B_MA[0..14]
15 DDR_B_DQS#[0..7] → DDR_B_DQS#[0..7]

U23D

DDR_A_D0	AJ38	SA_DQ_0			
DDR_A_D1	AJ41	SA_DQ_1			
DDR_A_D2	AN38	SA_DQ_2			
DDR_A_D3	AM38	SA_DQ_3			
DDR_A_D4	AJ36	SA_DQ_4			
DDR_A_D5	AJ40	SA_DQ_5			
DDR_A_D6	AM44	SA_DQ_6			
DDR_A_D7	AM42	SA_DQ_7			
DDR_A_D8	AN43	SA_DQ_8			
DDR_A_D9	AN44	SA_DQ_9			
DDR_A_D10	AU40	SA_DQ_10			
DDR_A_D11	AT38	SA_DQ_11			
DDR_A_D12	AN41	SA_DQ_12			
DDR_A_D13	AN39	SA_DQ_13			
DDR_A_D14	AU44	SA_DQ_14			
DDR_A_D15	AU42	SA_DQ_15			
DDR_A_D16	AV39	SA_DQ_16			
DDR_A_D17	AY44	SA_DQ_17			
DDR_A_D18	BA40	SA_DQ_18			
DDR_A_D19	BD43	SA_DQ_19			
DDR_A_D20	AV41	SA_DQ_20			
DDR_A_D21	AY43	SA_DQ_21			
DDR_A_D22	BB41	SA_DQ_22			
DDR_A_D23	BC40	SA_DQ_23			
DDR_A_D24	AY37	SA_DQ_24			
DDR_A_D25	BD38	SA_DQ_25			
DDR_A_D26	AV37	SA_DQ_26			
DDR_A_D27	AT36	SA_DQ_27			
DDR_A_D28	AY38	SA_DQ_28			
DDR_A_D29	BB38	SA_DQ_29			
DDR_A_D30	AV36	SA_DQ_30			
DDR_A_D31	AW36	SA_DQ_31			
DDR_A_D32	BD13	SA_DQ_32			
DDR_A_D33	AU11	SA_DQ_33			
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DDR_A_D36	AU13	SA_DQ_36			
DDR_A_D37	AV13	SA_DQ_37			
DDR_A_D38	BD12	SA_DQ_38			
DDR_A_D39	BC12	SA_DQ_39			
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DDR_A_D48	AV5	SA_DQ_48			
DDR_A_D49	AV7	SA_DQ_49			
DDR_A_D50	AT9	SA_DQ_50			
DDR_A_D51	AN8	SA_DQ_51			
DDR_A_D52	AU5	SA_DQ_52			
DDR_A_D53	AU6	SA_DQ_53			
DDR_A_D54	AT5	SA_DQ_54			
DDR_A_D55	AN10	SA_DQ_55			
DDR_A_D56	AM11	SA_DQ_56			
DDR_A_D57	AM5	SA_DQ_57			
DDR_A_D58	AJ9	SA_DQ_58			
DDR_A_D59	AJ8	SA_DQ_59			
DDR_A_D60	AN12	SA_DQ_60			
DDR_A_D61	AM13	SA_DQ_61			
DDR_A_D62	AJ11	SA_DQ_62			
DDR_A_D63	AJ12	SA_DQ_63			

		SA_BS_0	BD21	DDR_A_BS0	14
		SA_BS_1	BG18	DDR_A_BS1	14
		SA_BS_2	AT25	DDR_A_BS2	14
		SA_RAS#	BB20	DDR_A_RAS#	14
		SA_CAS#	BD20	DDR_A_CAS#	14
		SA_WE#	AY20	DDR_A_WE#	14
		SA_DM_0	AM37	DDR_A_DM0	
		SA_DM_1	AT41	DDR_A_DM1	
		SA_DM_2	AY41	DDR_A_DM2	
		SA_DM_3	AU39	DDR_A_DM3	
		SA_DM_4	BB12	DDR_A_DM4	
		SA_DM_5	AY6	DDR_A_DM5	
		SA_DM_6	AT7	DDR_A_DM6	
		SA_DM_7	AJ5	DDR_A_DM7	
		SA_DQS_0	AJ44	DDR_A_DQS0	
		SA_DQS_1	AT44	DDR_A_DQS1	
		SA_DQS_2	BA43	DDR_A_DQS2	
		SA_DQS_3	BC37	DDR_A_DQS3	
		SA_DQS_4	AW12	DDR_A_DQS4	
		SA_DQS_5	BC8	DDR_A_DQS5	
		SA_DQS_6	AU8	DDR_A_DQS6	
		SA_DQS_7	AM7	DDR_A_DQS7	
		SA_DQS#_0	AJ43	DDR_A_DQS#0	
		SA_DQS#_1	AT43	DDR_A_DQS#1	
		SA_DQS#_2	BA44	DDR_A_DQS#2	
		SA_DQS#_3	BD37	DDR_A_DQS#3	
		SA_DQS#_4	AY12	DDR_A_DQS#4	
		SA_DQS#_5	BD8	DDR_A_DQS#5	
		SA_DQS#_6	AU9	DDR_A_DQS#6	
		SA_DQS#_7	AM8	DDR_A_DQS#7	
		SA_MA_0	BA21	DDR_A_MA0	
		SA_MA_1	BC24	DDR_A_MA1	
		SA_MA_2	BG24	DDR_A_MA2	
		SA_MA_3	BH24	DDR_A_MA3	
		SA_MA_4	BG25	DDR_A_MA4	
		SA_MA_5	BA24	DDR_A_MA5	
		SA_MA_6	BD24	DDR_A_MA6	
		SA_MA_7	BG27	DDR_A_MA7	
		SA_MA_8	BF25	DDR_A_MA8	
		SA_MA_9	AW24	DDR_A_MA9	
		SA_MA_10	BC21	DDR_A_MA10	
		SA_MA_11	BG26	DDR_A_MA11	
		SA_MA_12	BH26	DDR_A_MA12	
		SA_MA_13	BH17	DDR_A_MA13	
		SA_MA_14	AY25	DDR_A_MA14	

DDR SYSTEM MEMORY A

GM@ CANTIGA ES_FCBGA1329

U23E

DDR_B_D0	AK47	SB_DQ_0			
DDR_B_D1	AH46	SB_DQ_1			
DDR_B_D2	AP47	SB_DQ_2			
DDR_B_D3	AP46	SB_DQ_3			
DDR_B_D4	AJ46	SB_DQ_4			
DDR_B_D5	AJ48	SB_DQ_5			
DDR_B_D6	AM48	SB_DQ_6			
DDR_B_D7	AP48	SB_DQ_7			
DDR_B_D8	AU47	SB_DQ_8			
DDR_B_D9	AU46	SB_DQ_9			
DDR_B_D10	BA48	SB_DQ_10			
DDR_B_D11	AY48	SB_DQ_11			
DDR_B_D12	AT47	SB_DQ_12			
DDR_B_D13	AR47	SB_DQ_13			
DDR_B_D14	BA47	SB_DQ_14			
DDR_B_D15	BC47	SB_DQ_15			
DDR_B_D16	BC46	SB_DQ_16			
DDR_B_D17	BC44	SB_DQ_17			
DDR_B_D18	BG43	SB_DQ_18			
DDR_B_D19	BF43	SB_DQ_19			
DDR_B_D20	BE45	SB_DQ_20			
DDR_B_D21	BC41	SB_DQ_21			
DDR_B_D22	BF40	SB_DQ_22			
DDR_B_D23	BF41	SB_DQ_23			
DDR_B_D24	BG38	SB_DQ_24			
DDR_B_D25	BF38	SB_DQ_25			
DDR_B_D26	BH35	SB_DQ_26			
DDR_B_D27	BG35	SB_DQ_27			
DDR_B_D28	BH40	SB_DQ_28			
DDR_B_D29	BG39	SB_DQ_29			
DDR_B_D30	BG34	SB_DQ_30			
DDR_B_D31	BH34	SB_DQ_31			
DDR_B_D32	BH14	SB_DQ_32			
DDR_B_D33	BG12	SB_DQ_33			
DDR_B_D34	BH11	SB_DQ_34			
DDR_B_D35	BG8	SB_DQ_35			
DDR_B_D36	BH12	SB_DQ_36			
DDR_B_D37	BF11	SB_DQ_37			
DDR_B_D38	BF8	SB_DQ_38			
DDR_B_D39	BG7	SB_DQ_39			
DDR_B_D40	BC5	SB_DQ_40			
DDR_B_D41	BC6	SB_DQ_41			
DDR_B_D42	AY3	SB_DQ_42			
DDR_B_D43	AY1	SB_DQ_43			
DDR_B_D44	BF6	SB_DQ_44			
DDR_B_D45	BF5	SB_DQ_45			
DDR_B_D46	BA1	SB_DQ_46			
DDR_B_D47	BD3	SB_DQ_47			
DDR_B_D48	AV2	SB_DQ_48			
DDR_B_D49	AU3	SB_DQ_49			
DDR_B_D50	AR3	SB_DQ_50			
DDR_B_D51	AN2	SB_DQ_51			
DDR_B_D52	AY2	SB_DQ_52			
DDR_B_D53	AV1	SB_DQ_53			
DDR_B_D54	AP3	SB_DQ_54			
DDR_B_D55	AR1	SB_DQ_55			
DDR_B_D56	AL1	SB_DQ_56			
DDR_B_D57	AL2	SB_DQ_57			
DDR_B_D58	AJ1	SB_DQ_58			
DDR_B_D59	AH1	SB_DQ_59			
DDR_B_D60	AM2	SB_DQ_60			
DDR_B_D61	AM3	SB_DQ_61			
DDR_B_D62	AH3	SB_DQ_62			
DDR_B_D63	AJ3	SB_DQ_63			

		SB_BS_0	BC16	DDR_B_BS0	15
		SB_BS_1	BB17	DDR_B_BS1	15
		SB_BS_2	BB33	DDR_B_BS2	15
		SB_RAS#	AU17	DDR_B_RAS#	15
		SB_CAS#	BG16	DDR_B_CAS#	15
		SB_WE#	BF14	DDR_B_WE#	15
		SB_DM_0	AM47	DDR_B_DM0	
		SB_DM_1	AY47	DDR_B_DM1	
		SB_DM_2	BD40	DDR_B_DM2	
		SB_DM_3	BF35	DDR_B_DM3	
		SB_DM_4	BG11	DDR_B_DM4	
		SB_DM_5	BA3	DDR_B_DM5	
		SB_DM_6	AP1	DDR_B_DM6	
		SB_DM_7	AK2	DDR_B_DM7	
		SB_DQS_0	AL47	DDR_B_DQS0	
		SB_DQS_1	AV48	DDR_B_DQS1	
		SB_DQS_2	BG41	DDR_B_DQS2	
		SB_DQS_3	BG37	DDR_B_DQS3	
		SB_DQS_4	BH9	DDR_B_DQS4	
		SB_DQS_5	BB2	DDR_B_DQS5	
		SB_DQS_6	AU1	DDR_B_DQS6	
		SB_DQS_7	AN6	DDR_B_DQS7	
		SB_DQS#_0	AL46	DDR_B_DQS#0	
		SB_DQS#_1	AV47	DDR_B_DQS#1	
		SB_DQS#_2	BH41	DDR_B_DQS#2	
		SB_DQS#_3	BH37	DDR_B_DQS#3	
		SB_DQS#_4	BG9	DDR_B_DQS#4	
		SB_DQS#_5	BC2	DDR_B_DQS#5	
		SB_DQS#_6	AT2	DDR_B_DQS#6	
		SB_DQS#_7	AN5	DDR_B_DQS#7	
		SB_MA_0	AV17	DDR_B_MA0	
		SB_MA_1	BA25	DDR_B_MA1	
		SB_MA_2	BC25	DDR_B_MA2	
		SB_MA_3	AU25	DDR_B_MA3	
		SB_MA_4	AW25	DDR_B_MA4	
		SB_MA_5	BB28	DDR_B_MA5	
		SB_MA_6	AU28	DDR_B_MA6	
		SB_MA_7	AW28	DDR_B_MA7	
		SB_MA_8	AT33	DDR_B_MA8	
		SB_MA_9	BD33	DDR_B_MA9	
		SB_MA_10	BB16	DDR_B_MA10	
		SB_MA_11	AW33	DDR_B_MA11	
		SB_MA_12	AY33	DDR_B_MA12	
		SB_MA_13	BH15	DDR_B_MA13	
		SB_MA_14	AU33	DDR_B_MA14	

DDR SYSTEM MEMORY B

GM@ CANTIGA ES_FCBGA1329

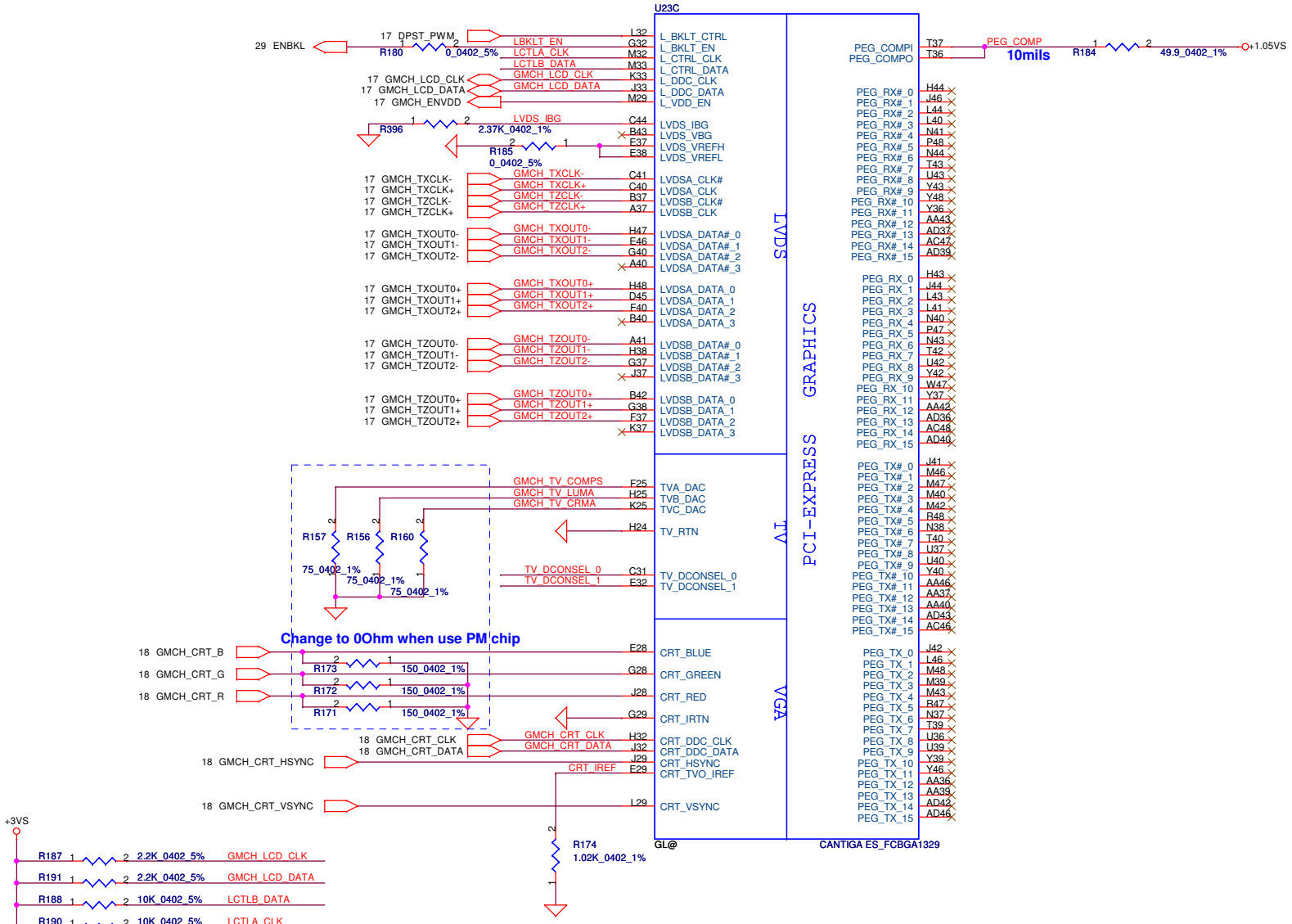
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Cantiga GMCH(3/7)-DDR

Size	Document Number	Rev
B	NAWF3 M/B LA-4854P Schematic	1.0

Date: Wednesday, March 03, 2010 Sheet 9 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Cantiga GMCH(4/7)-VGA/LVDS/TV

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 10 of 45

U23F

2600mA

VCC_SM_1 … VCC_SM_42/NC

VCC_AXG_NTCF_1 … VCC_AXG_NTCF_60

VCC_AXG_1 … VCC_AXG_42

VCC_SM_LF1 … VCC_SM_LF7

VCC_AXG_SENSE / VSS_AXG_SENSE

CANTIGA ES_FCBGA1329

GL@

Reference PILLAR_ROCK CRB Rev1.0

Pins BA36, BB24, BD16, BB21, AW16, AW13, AT13 could be left NC for DDR2 board.

VCC_SM_BA36 VCC_SM_BB24 VCC_SM_BD16 VCC_SM_AW16 VCC_SM_AT13

T17 PAD @ VCC_AXG_SENSE

T18 PAD @ VSS_AXG_SENSE

Place close to the GMCH

VCC: 1930.4mA (GMCH), 1210.34mA (MCH)
(270UF*1, 22UF*1, 0.22UF*2, 0.1UF*1)

C485 220U_D2_4VM_R15
C255 10U_0805_10V4Z
C265 0.22U_0402_6.3V6K
C266 0.22U_0402_6.3V6K
C256 0.1U_0402_16V4Z

Cavity Capacitors

VCC_AXG: 6326.84mA
(330UF*2, 22UF*1, 10UF*1, 1U*1, 0.47U*1, 0.1UF*2)

C243 0.47U_0603_16V4Z
C244 1U_0402_6.3V4Z
C234 10U_0805_10V4Z
C235 10U_0805_10V4Z
C236 0.1U_0402_16V4Z
C242 0.1U_0402_16V4Z

Cavity Capacitors

C482 330U_D2E_2.5VM_R9

Place close to the GMCH

VCC_SM: 2600mA
(330UF*1, 22UF*2, 0.1UF*1)

C269 330U_D2E_2.5VM_R9
C252 10U_0805_10V4Z
C251 10U_0805_10V4Z
C263 0.1U_0402_16V4Z

Place on the edge

Reference PILLAR_ROCK CRB Rev1.0

C214 @ 0.1U_0402_16V7K
C229 @ 0.1U_0402_16V7K
C228 @ 0.1U_0402_16V7K
C240 @ 0.1U_0402_16V7K
C271 @ 0.1U_0402_16V7K

C213 0.1U_0402_16V7K
C215 0.1U_0402_16V7K
C205 0.22U_0402_6.3V6K
C230 0.22U_0402_6.3V6K
C272 0.47U_0603_16V4Z
C270 1U_0402_6.3V4Z
C279 1U_0402_6.3V4Z

U23G

VCC_1 … VCC_12 VCC_13 … VCC_35

VCC CORE POWER

CANTIGA ES_FCBGA1329

GL@

VCC_NCTF_1 … VCC_NCTF_44

VCC NCTF

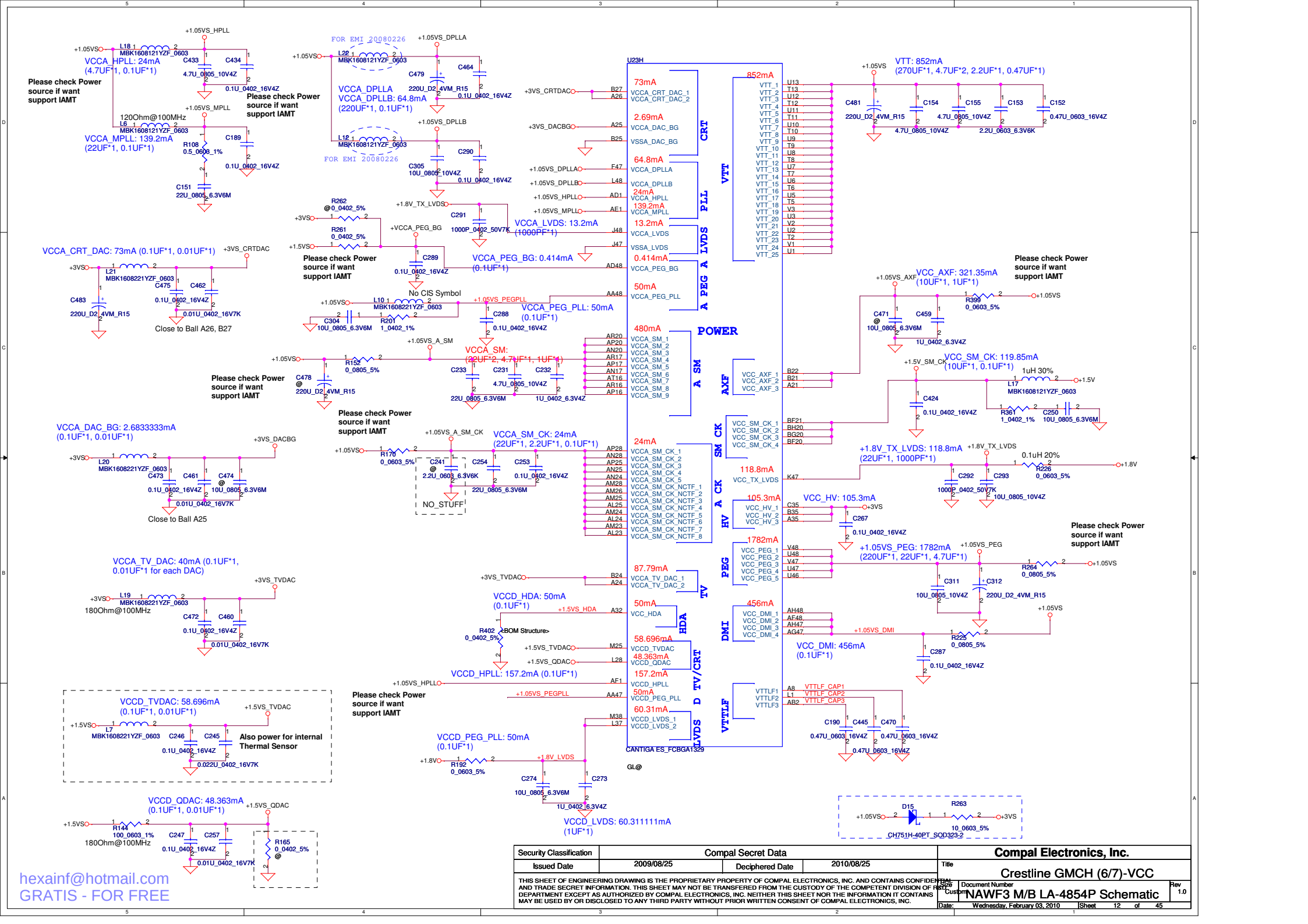
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Cantiga GMCH(5/7)-VCC

Size: B (5/25 Custom) | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, February 03, 2010 | Sheet 11 of 45



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date 2010/08/25	Title: Crestline GMCH (6/7)-VCC
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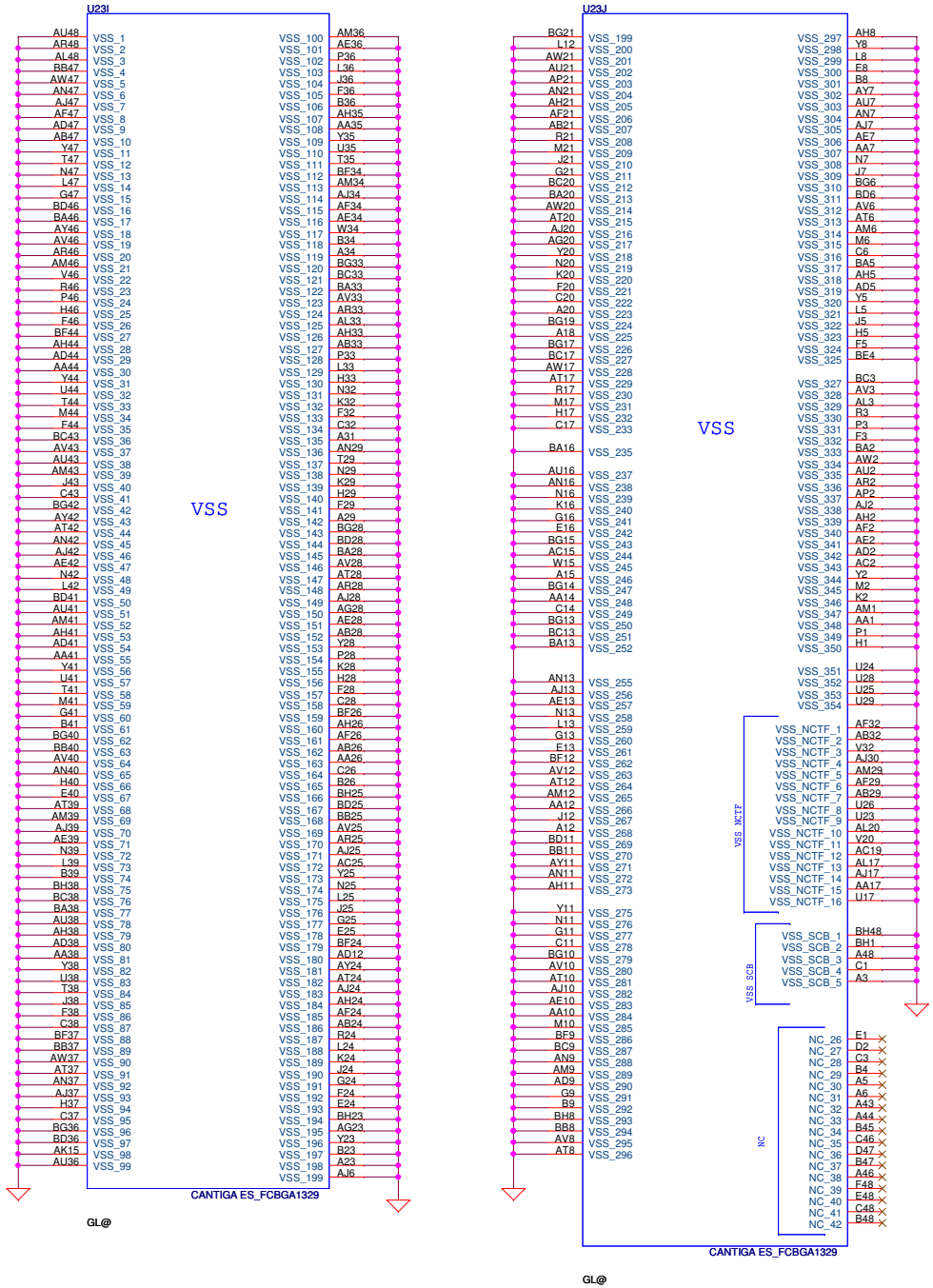
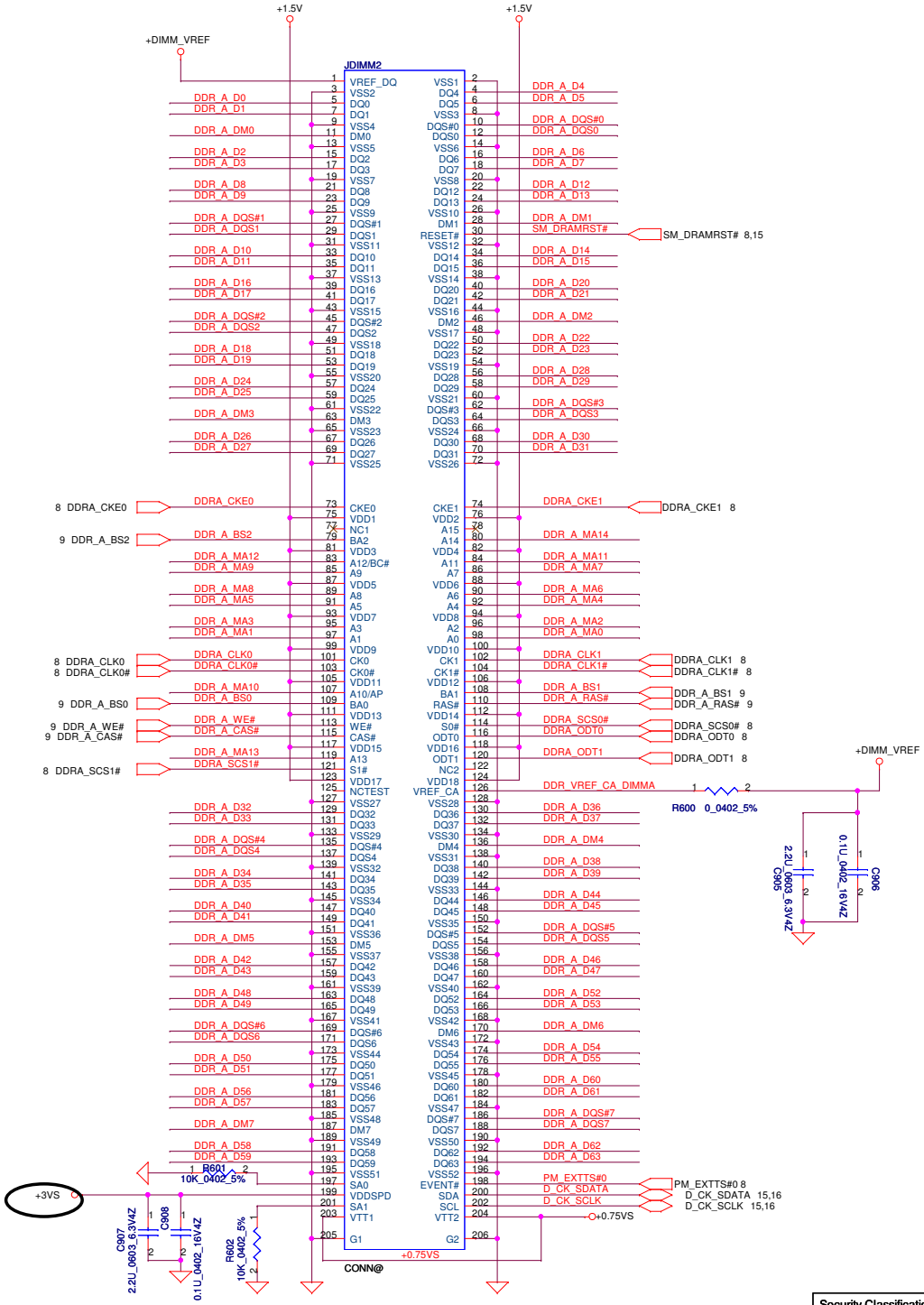
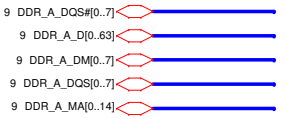
			Date: Wednesday, February 03, 2010; Sheet 12 of 45

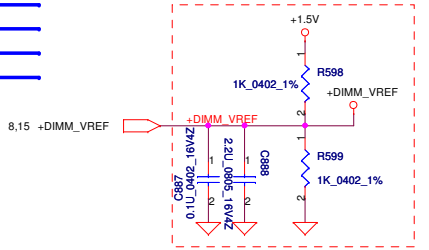


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Title	Cantiga GMCH(1/7)-GTL	
Size: B/26 Custom	Document Number: NAWF3 M/B LA-4854P Schematic	Rev: 1.0
Date: Wednesday, February 03, 2010	Sheet 13 of 45	

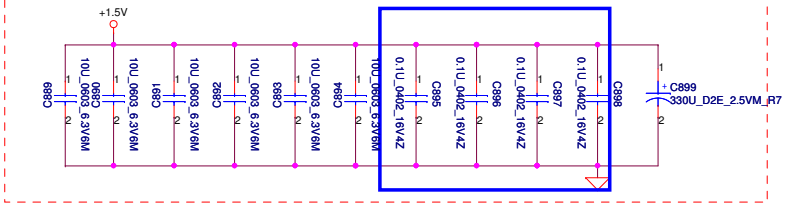




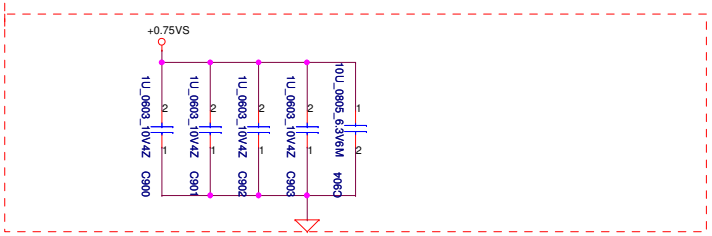


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



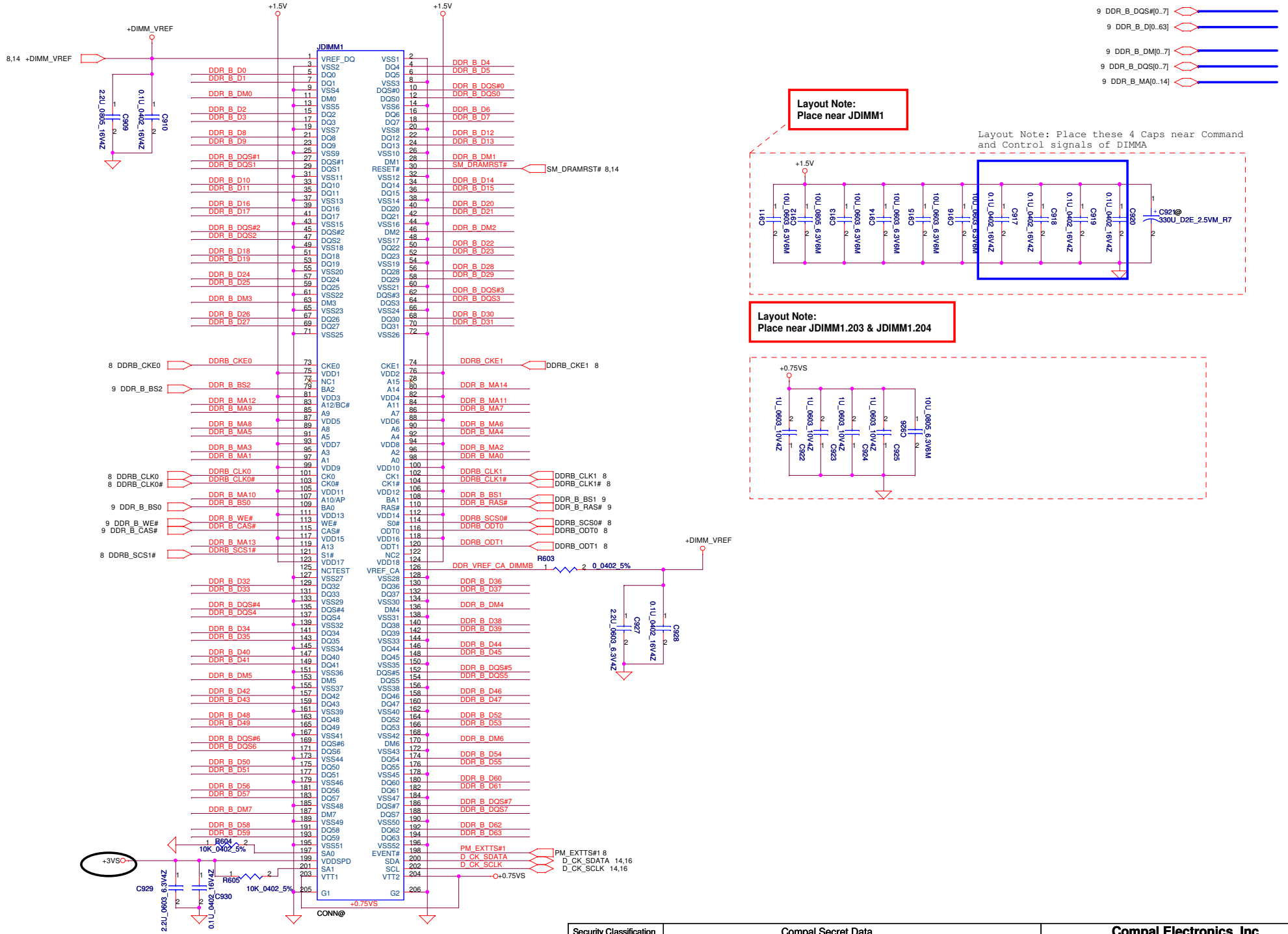
Layout Note:
Place near JDIMM2.203 & JDIMM2.204



DIMM0 REV H:5.2mm (BOT)

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	DDRIII-SODIMM0		
Size B	Document Number NAWF3 M/B LA-4854P Schematic		Rev 1.0
Date: Wednesday, March 03, 2010	Sheet 14 of 45		



DIMM1 REV H:9.2mm (BOT)

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.		
Title	DDRIII-SODIMM1	
Size B	Document Number NAWF3 M/B LA-4854P Schematic	Rev 1.0
Date: Wednesday, March 03, 2010	Sheet 15 of 45	

Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

+3VS R306 10K_0402_5% CLK_PCI2
CLK_PCI2=1, Trusted Mode Enable(No overclocking allowed)
R312 @10K_0402_5% — mount to Enable ITP_CLK
R310 10K_0402_5% CLK_PCI5
CLK_PCI5=0, Pin63,64 is SRC_CLK
CLK_PCI5=1, Pin63,64 is ITP_CLK
R308 10K_0402_5% CLK_PCI4
CLK_PCI4=0, Pin28, 29 is SRC_CLK
Pin24, 25 is DOT96_CLK
R292 @10K_0402_5% CK_PWRGD
C345 @ 10P_0402_50V8J CLK_PCI_LPC
C346 @ 10P_0402_50V8J CLK_PCI_ICH
For EMI 10/9

+1.05VS R327 @56_0402_5%
R326 2.2K_0402_5% CLKSEL0
R313 1K_0402_5%
MCH_CLKSEL0 8
R328 @1K_0402_5%
R314 0_0402_5%
CPU_BSEL0 5

+1.05VS R384 @1K_0402_5%
R383 1K_0402_5% CLKSEL1
MCH_CLKSEL1 8
R379 @0_0402_5%
R380 0_0402_5%
CPU_BSEL1 5

+1.05VS R389 @1K_0402_5%
R388 10K_0402_5% CLKSEL2
R392 1K_0402_5%
MCH_CLKSEL2 8
R390 @0_0402_5%
R391 0_0402_5%
CPU_BSEL2 5

+1.05VS — L15 FBMA-L11-201209-221LMA30T_0805 — +CLK_VDDSRC
C347 10U_0805_10V4Z
C358 10U_0805_10V4Z
C371 C387 C370 C380 C381 C386 0.1U_0402_16V4Z

+3VS — L16 FBMA-L11-201209-221LMA30T_0805 — +CLK_VDD
C390 10U_0805_10V4Z
C384 10U_0805_10V4Z
C356 C357 C355 C352 C372 C385 0.1U_0402_16V4Z

U16
ICS9LPRS387, PN:SA000020H10
SLG8SP556V, PN:SA000020K00

+CLK_VDD	6	VDDREF	
	19	VDD48	
	72	VDDCPU	
	12	VDDPCI	
	27	VDDPLL3	
	55	VDDSRC	
+CLK_VDDSRC	52	VDDSRC_IO	
	38	VDDSRC_IO	
	62	VDDSRC_IO	
	31	VDDPLL3_IO	
	66	VDDCPU_IO	
	23	VDD96_IO	
21 H_STP_CPU#	53	CPU_STOP#	H_STP_CPU#
21 H_STP_PCI#	54	PCI_STOP#	H_STP_PCI#
	13	PCI1	
CLK_PCI2	14	PCI2/TME	
29 CLK_PCI_LPC CLK_PCI_LPC R307 33_0402_5%	15	PCI3	CLK_PCI3
CLK_PCI4	16	PCI4/27_SELECT	
19 CLK_PCI_ICH CLK_PCI_ICH R309 33_0402_5%	17	PCI_F5/ITP_EN	CLK_PCI5
21 CK_PWRGD 8,21,41 VGATE 0_0402_5% R303 0_0402_5% R302	1	CK_PWRGD/PD#	CK505_PWRGD
C354 27P_0402_50V8J CLK_XTALIN	5	X1	
C353 27P_0402_50V8J CLK_XTALOUT	4	X2	
Y2 14.31818MHz_20P_FSX8L14.318181M20FDB	11	NC	
21 CLK_ICH_48M CLK_ICH_48M R325 22_0402_5%	20	USB_48MHz/FSLA	CLKSEL0
24 CLK_SD_48M CLK_SD_48M R311 22_0402_5%	2	FSLB/TEST_MODE	CLKSEL1
21 CLK_ICH_14M CLK_ICH_14M R304 33_0402_5%	7	FSLC/TEST_SEL/REF0	CLKSEL2
	8	REF1	
	69	GNDCPU	
	3	GNDREF	
	18	GNDPCI	
	22	GND48	
	30	GND	
	26	GND	
	34	GNDSRC	
	59	GNDSRC	
	42	GNDSRC	
	73	GND_THERMAL_PAD	

ICS9LPRS387BKLFT_MLF72_10x10

SDATA	9	D_CK_SDATA	D_CK_SDATA 14,15
SCLK	10	D_CK_SCLK	D_CK_SCLK 14,15
CPUT0_LPR_F	71	CLK_CPU_BCLK	CLK_CPU_BCLK 4
CPUC0_LPR_F	70	CLK_CPU_BCLK#	CLK_CPU_BCLK# 4
CPUT1_LPR_F	68	CLK_MCH_BCLK	CLK_MCH_BCLK 7
CPUC1_LPR_F	67	CLK_MCH_BCLK#	CLK_MCH_BCLK# 7
SRCT0_LPR/DOTT_96_LPR	24	CLK_DREF_96M	CLK_DREF_96M 8
SRCC0_LPR/DOTC_96_LPR	25	CLK_DREF_96M#	CLK_DREF_96M# 8
27MHz_NonSS/SRCT1_LPR/SE1	28	CLK_DREF_SSC	CLK_DREF_SSC 8
27MHz_SS/SRCC1_LPR/SE2	29	CLK_DREF_SSC#	CLK_DREF_SSC# 8
SRCT2_LPR/SATAT_LPR	32	CLK_PCIE_SATA	CLK_PCIE_SATA 20
SRCC2_LPR/SATAC_LPR	33	CLK_PCIE_SATA#	CLK_PCIE_SATA# 20
SRCT3_LPR	35	CLK_PCIE_ICH	CLK_PCIE_ICH 21
SRCC3_LPR	36	CLK_PCIE_ICH#	CLK_PCIE_ICH# 21
SRCT4_LPR	39	CLK_PCIE_CARD	CLK_PCIE_CARD 28
SRCC4_LPR	40	CLK_PCIE_CARD#	CLK_PCIE_CARD# 28
SRCT6_LPR	57	CLK_MCH_3GPLL	CLK_MCH_3GPLL 8
SRCC6_LPR	56	CLK_MCH_3GPLL#	CLK_MCH_3GPLL# 8
SRCT7_LPR	61		
SRCC7_LPR	60		
CPUT2_ITP_LPR/SRCT8_LPR	64		
CPUC2_ITP_LPR/SRCC8_LPR	63		
SRCT9_LPR	44	CLK_PCIE_MINI2	CLK_PCIE_MINI2 27
SRCC9_LPR	45	CLK_PCIE_MINI2#	CLK_PCIE_MINI2# 27
SRCT10_LPR	50		
SRCC10_LPR	51		
SRCT11_LPR	48	CLK_PCIE_LAN	CLK_PCIE_LAN 25
SRCC11_LPR	47	CLK_PCIE_LAN#	CLK_PCIE_LAN# 25
CR#3	37		
CR#4	41	R337 10K_0402_5% +3VS	EXP_CLKREQ# 28
CR#6	58	(Pull High to +3VS at GMCH side)	MCH_CLKREQ# 8
CR#7	65		
CR#9	43	R336 10K_0402_5% +3VS	MINI2_CLKREQ# 27
CR10#	49		
CR#11	46	R364 10K_0402_5% +3VS	LAN_CLKREQ# 25
CR#A	21	(Pull High to +3VS at ICH side)	SATA_CLKREQ# 21

VGA: disable this pair by BIOS
VGA: disable this pair by BIOS
UMA: disable this pair by BIOS

+3VS R301 10K_0402_5% @ CK505_PWRGD
Q28 2N7002_SOT23 @ CLK_ENABLE# 41

+3VS R305 4.7K_0402_5% +3VS
21,27,28 ICH_SMBDATA Q22 2N7002_SOT23 D_CK_SDATA

+3VS R293 4.7K_0402_5% +3VS
21,27,28 ICH_SMBCLK Q23 2N7002_SOT23 D_CK_SCLK

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

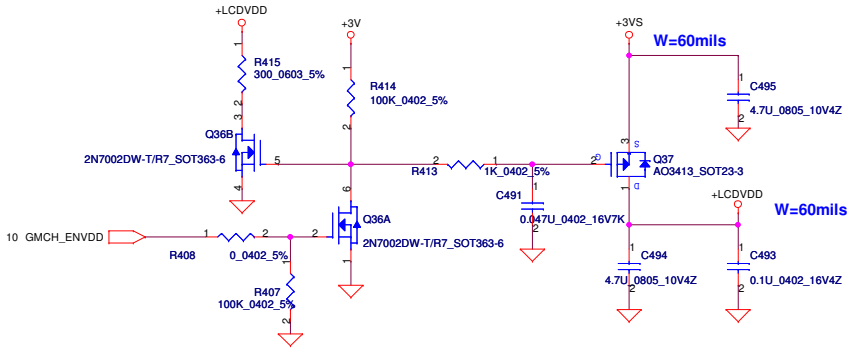
Compal Electronics, Inc.

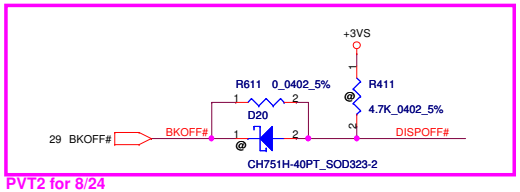
Title: Clock Generator (CK505)

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

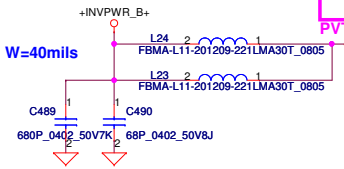
Date: Wednesday, March 03, 2010 | Sheet 16 of 45

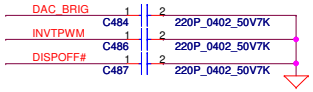
LCD POWER CIRCUIT

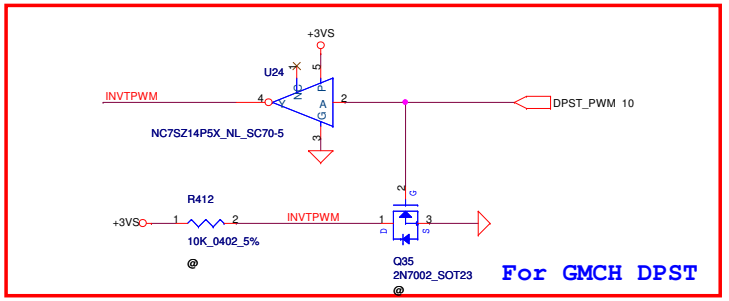




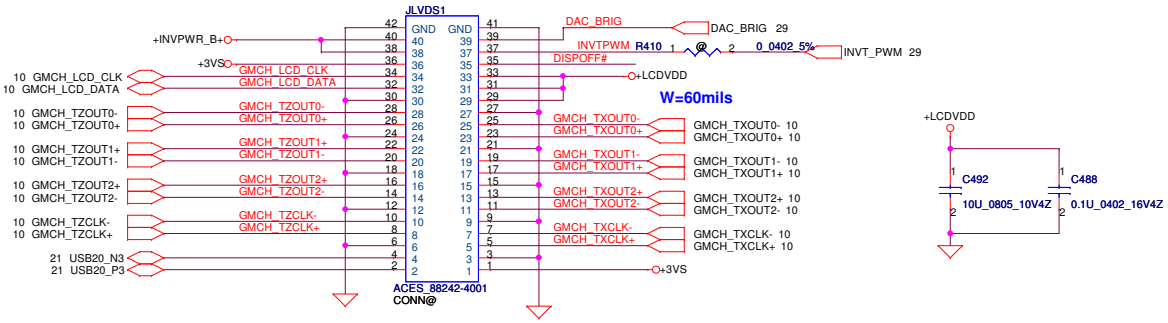
PVT2 for 8/24





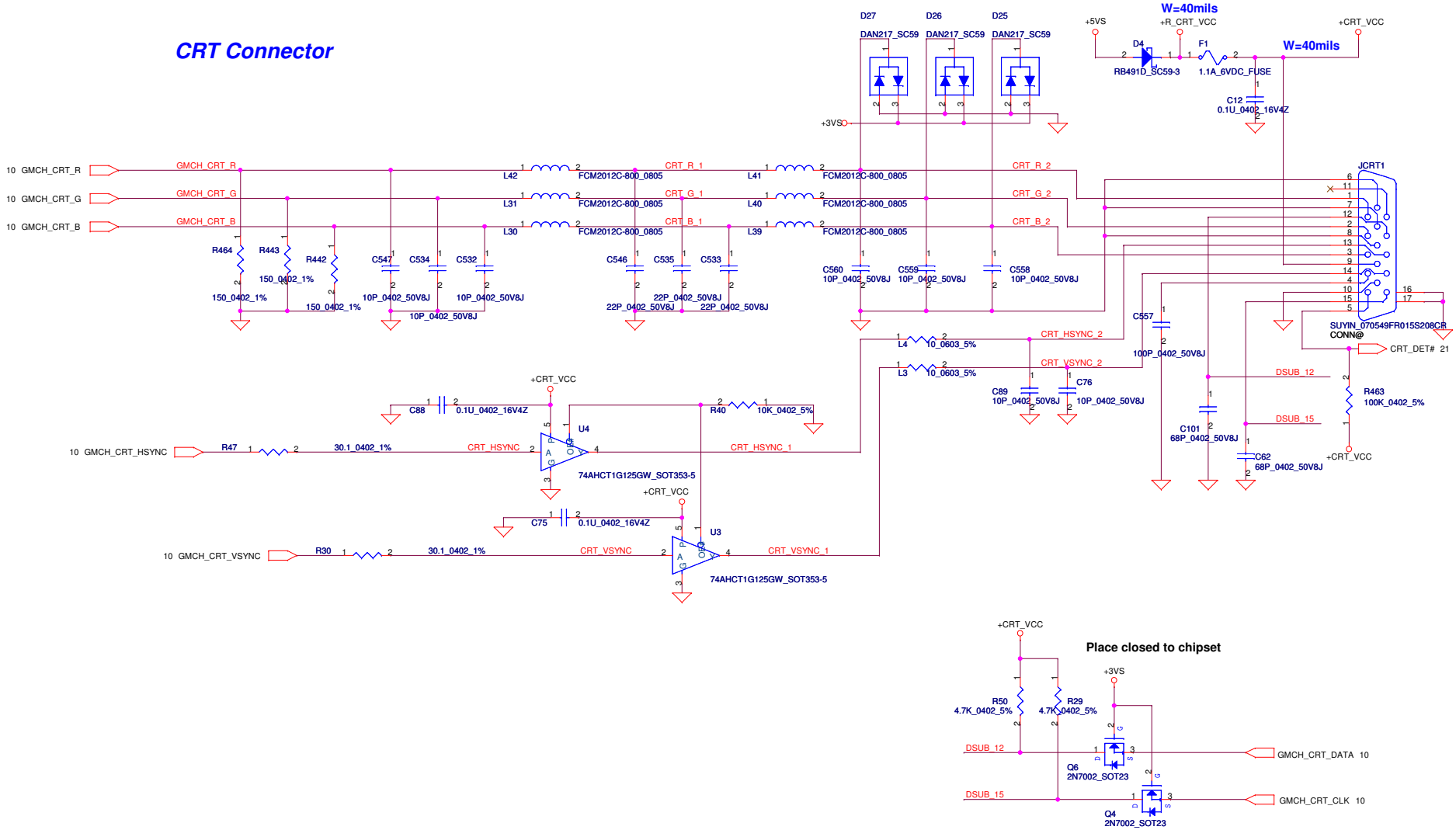


LCD/PANEL BD. Conn.



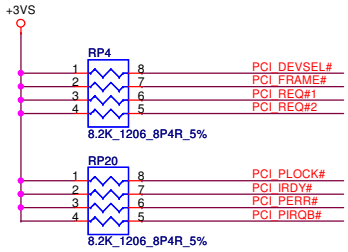
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date	2010/08/25
Title	LVDS Connector		
Size	Custom	Document Number	NAWF3 M/B LA-4854P Schematic
Rev	1.0		
Date:	Wednesday, March 03, 2010	Sheet	17 of 45

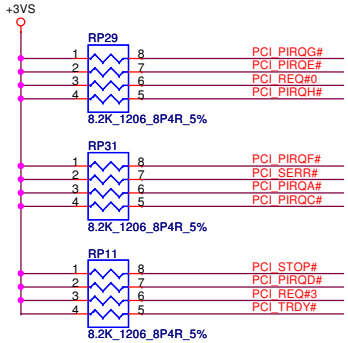
CRT Connector



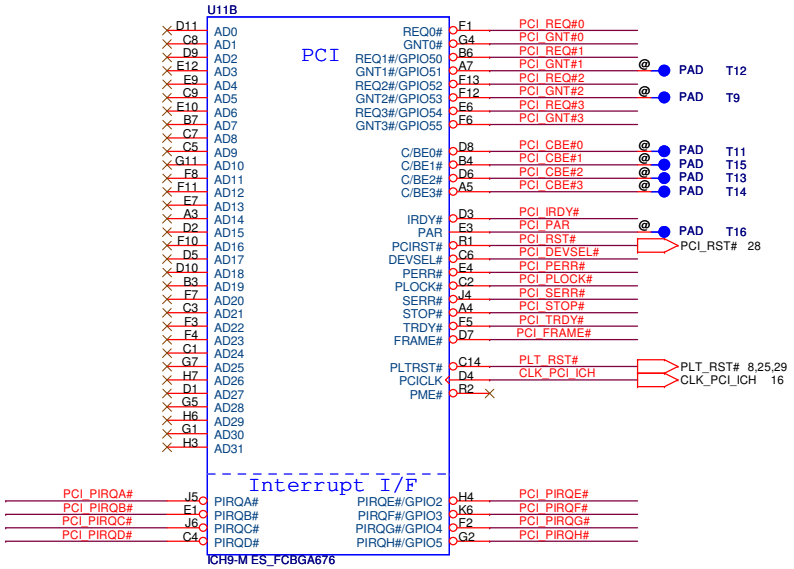
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date 2010/08/25	Title: CRT Connector

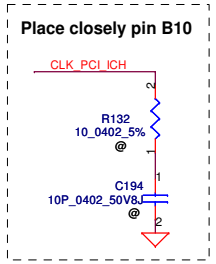
Size B	Document Number NAWF3 M/B LA-4854P Schematic		Rev 1.0
Date: Wednesday, March 03, 2010	Sheet 18 of 45		



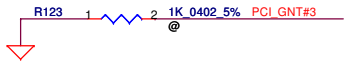


DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)

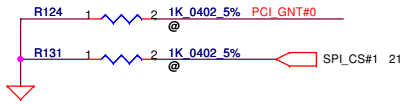


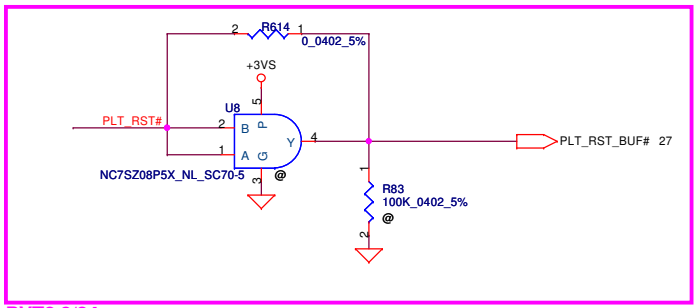


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*





PVT2 8/24

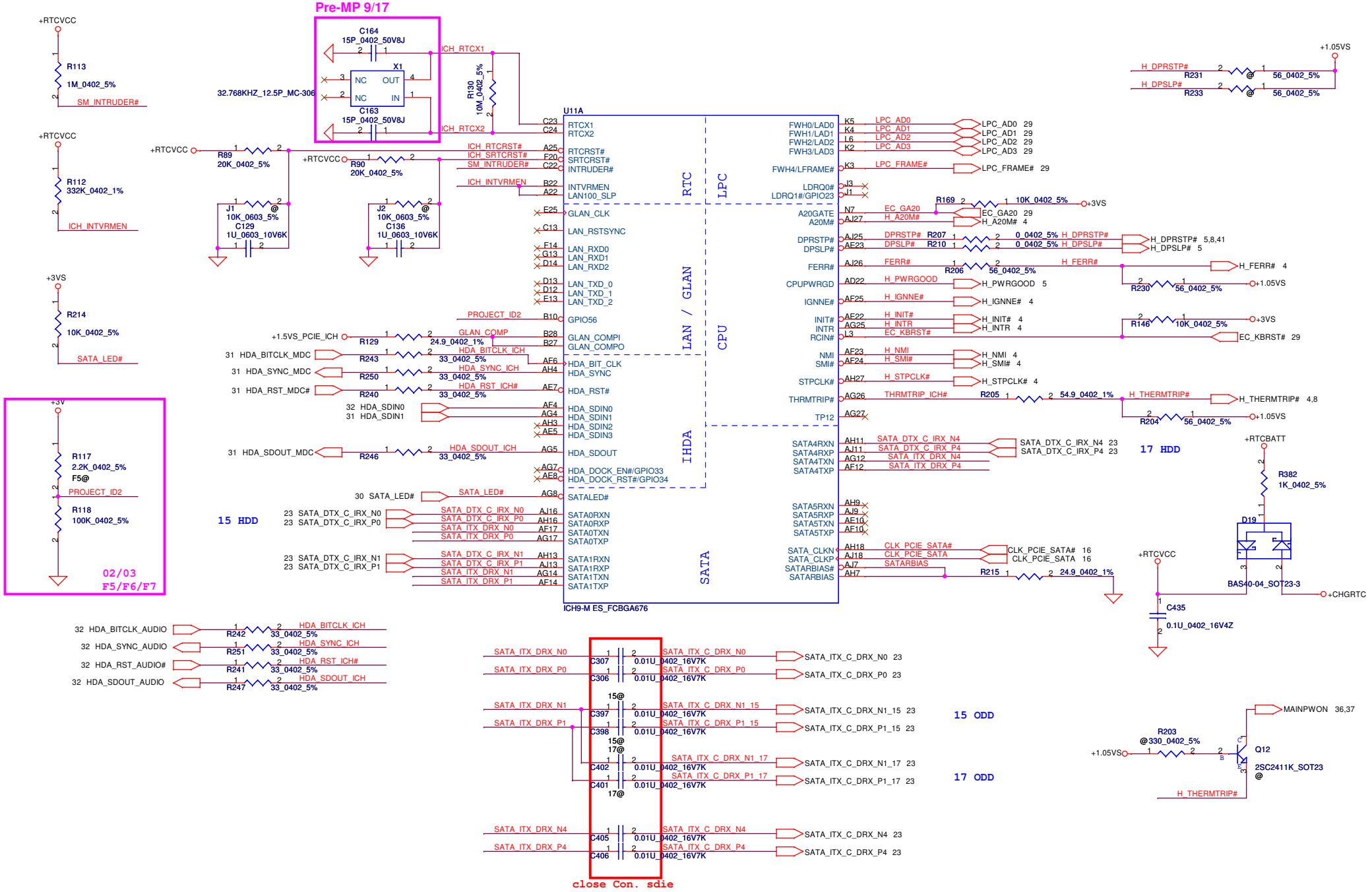
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: ICH9M(1/4)-PCI

Size | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 19 of 45



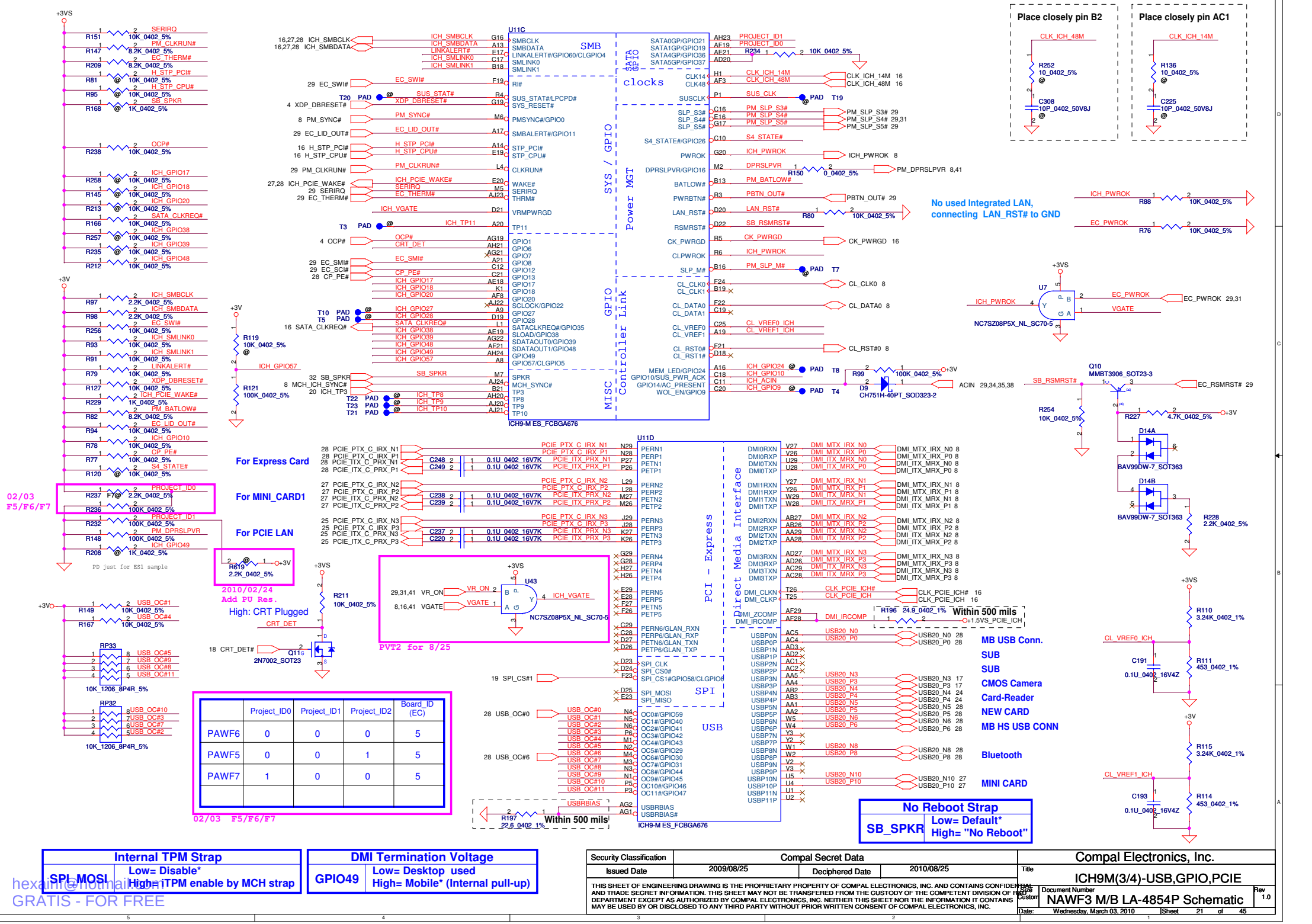
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 20 of 45



	Project_ID0	Project_ID1	Project_ID2	Board_ID (EC)
PAWF6	0	0	0	5
PAWF5	0	0	1	5
PAWF7	1	0	0	5

02/03 F5/F6/F7

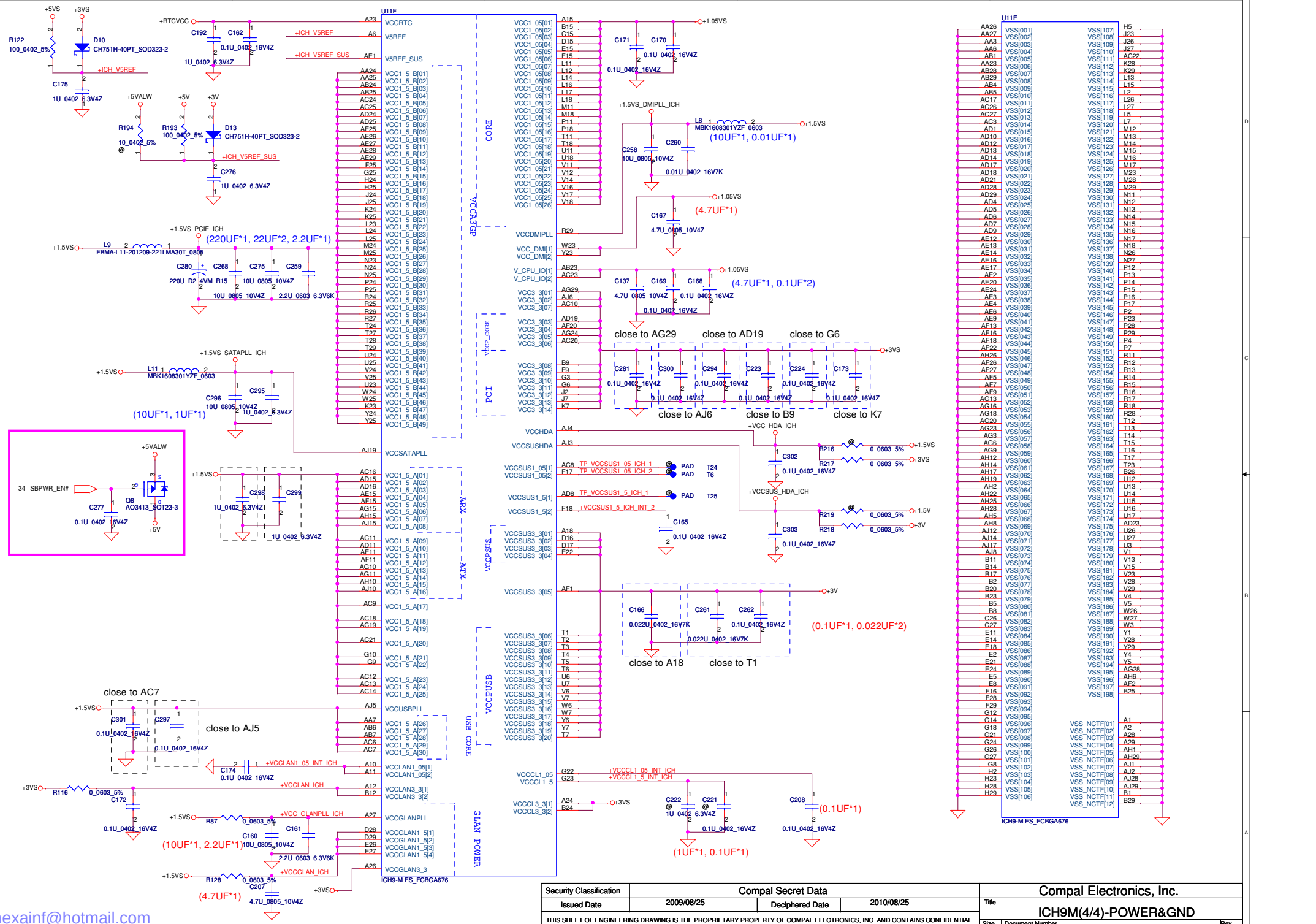
Internal TPM Strap	
SPI_MOSI	Low= Disable* High= TPM enable by MCH strap

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

No Reboot Strap	
SB_SPKR	Low= Default* High= "No Reboot"

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.	
Title	ICH9M(3/4)-USB,GPIO,PCIE
Size: Custom	Document Number: NAWF3 M/B LA-4854P Schematic
Rev	1.0
Date: Wednesday, March 03, 2010	Sheet 21 of 45



hexainf@hotmail.com
GRATIS - FOR FREE

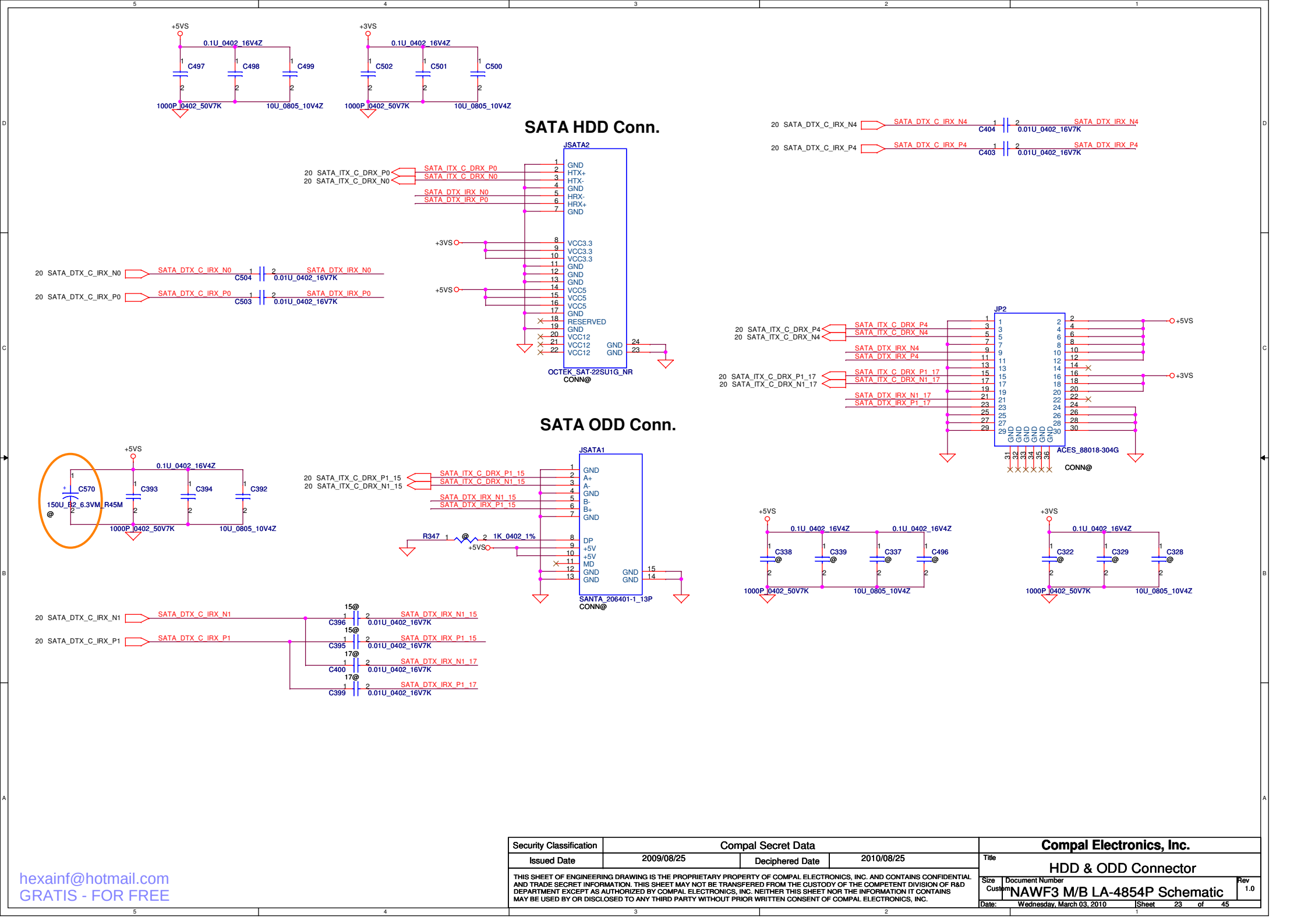
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: ICH9M(4/4)-POWER&GND

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 22 of 45



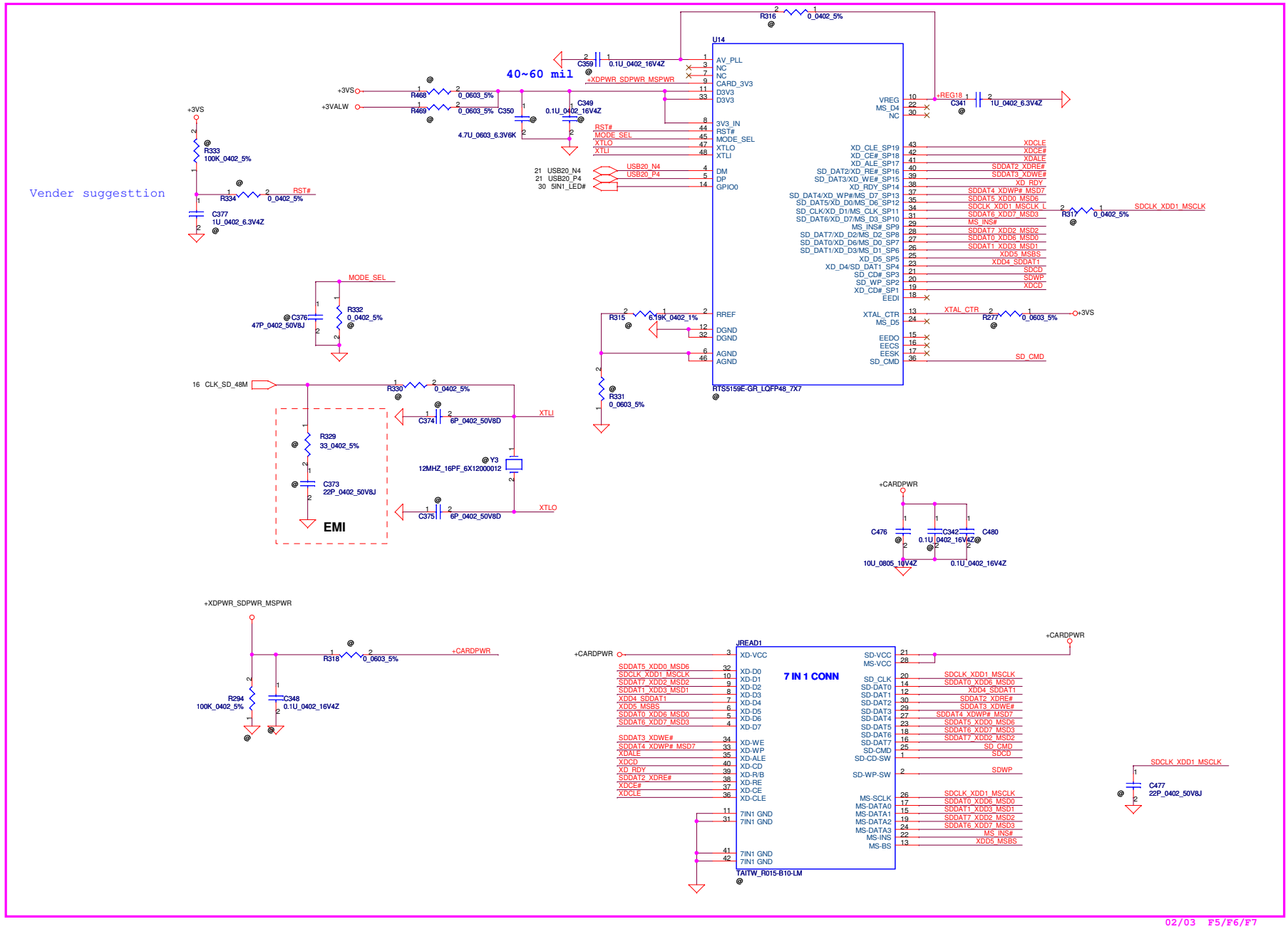
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 23 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: 5 in 1 Card reader

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 24 of 45

Layout Notice : Place as close chip as possible.

60mil

Atheros
AR8132L 10/100 LAN

AR8132L-AL1E_QFN48_6X6

Place Close to Chip

Place Close to Chip

Pre-MP 9/17

If overclocking, R39, L1 stuffed and R28 removed.
If not overclocking, R28, L1 stuffed and R39 removed.

AR8132:
L1=0ohm(SD002000080),C67=0.1uF(SE070104Z80). remove C80

Place Close to Pin 28、32、45、46

Place Close to Pin15、19、25

Place Close to Pin8、16、22、36、39

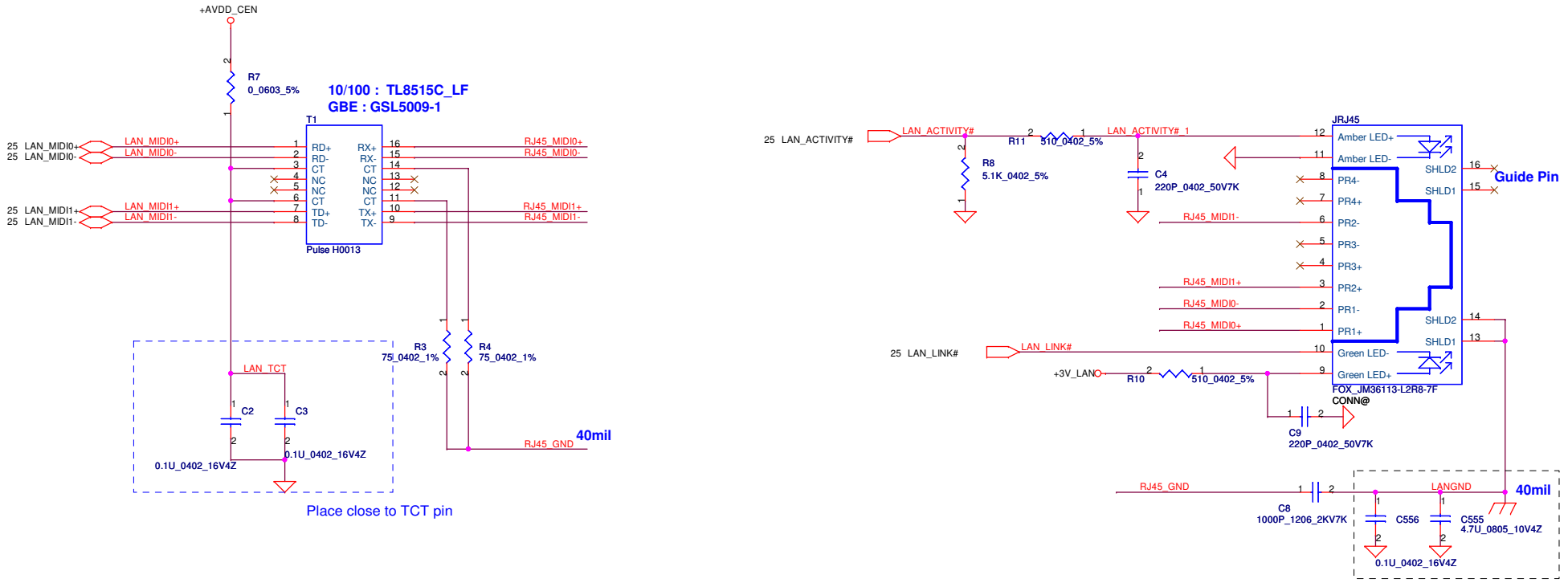
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: AR8114

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 25 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

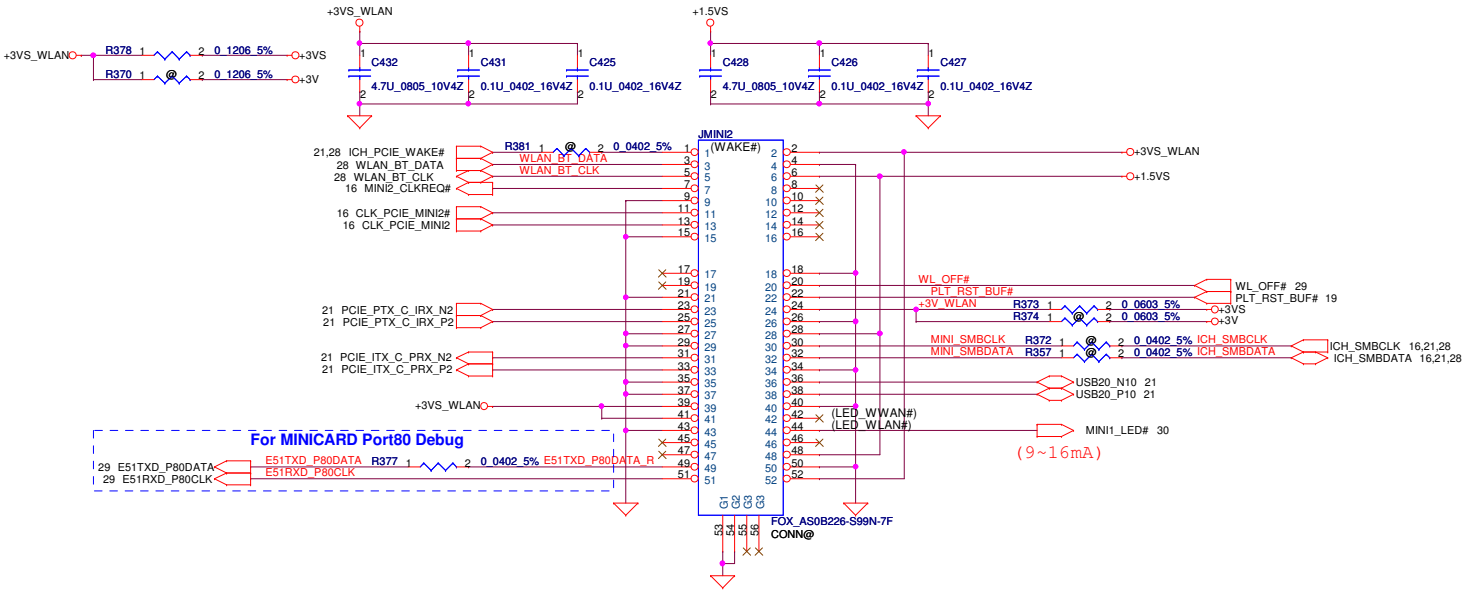
Title: LAN Magnetic & RJ45

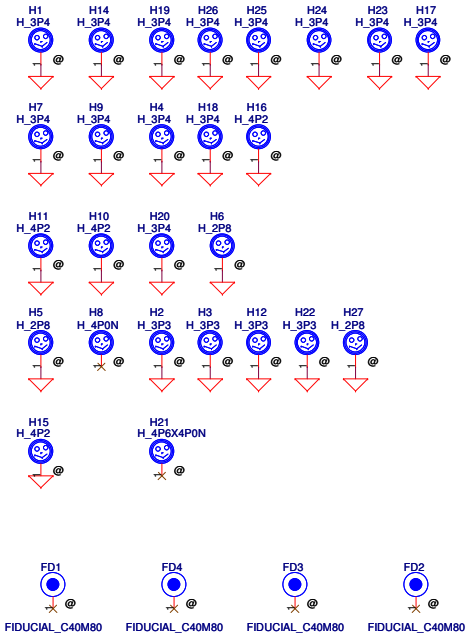
Size	Document Number	Rev
B	NAWF3 M/B LA-4854P Schematic	1.0

Date: Wednesday, March 03, 2010 Sheet 26 of 45

For Wireless LAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)





Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

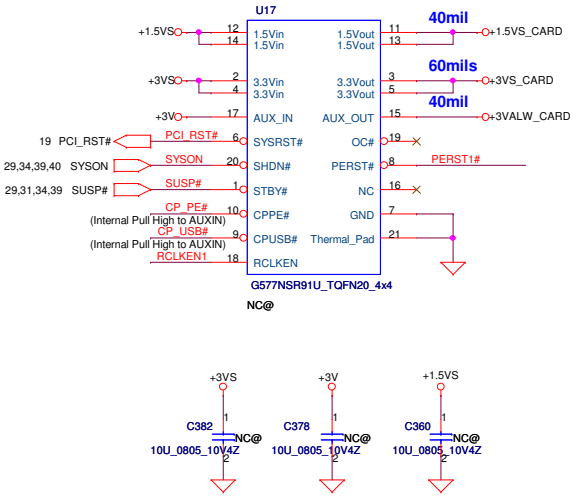
Compal Electronics, Inc.

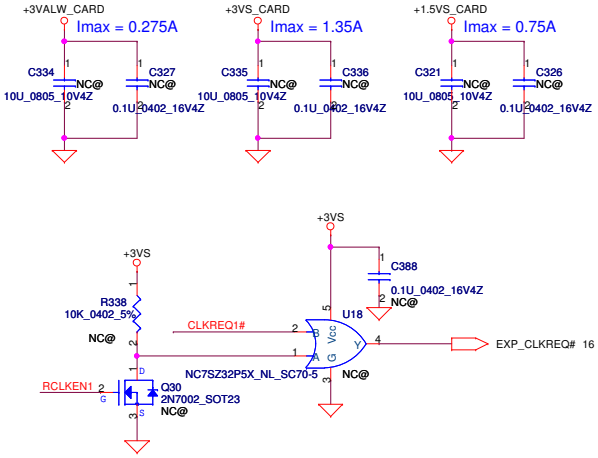
Title: MINI CARD (WLAN & TV-Tuner)

Size: B | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

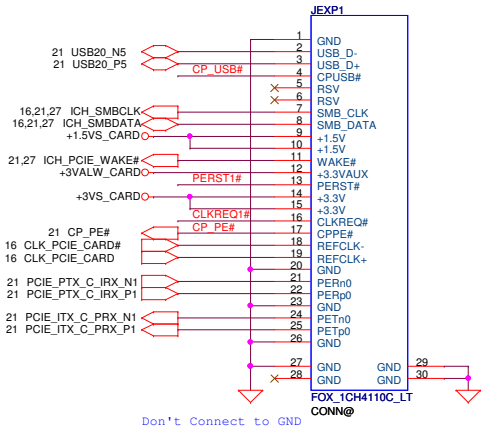
Date: Wednesday, March 03, 2010 | Sheet 27 of 45

New Card Power Switch



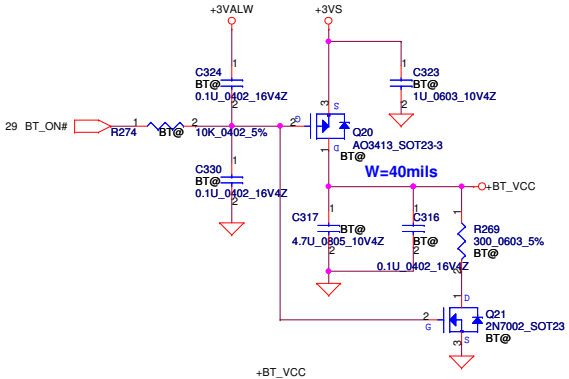


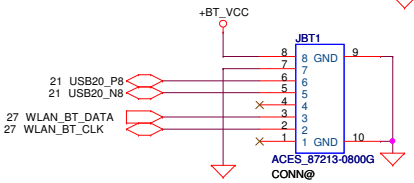
New Card Socket (Left/TOP)



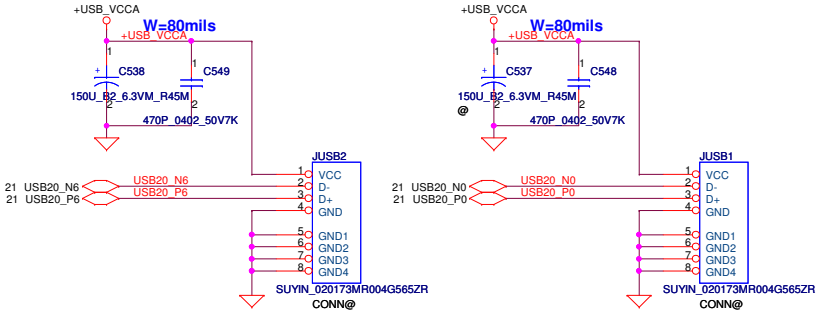
Don't Connect to GND
2008/02/22

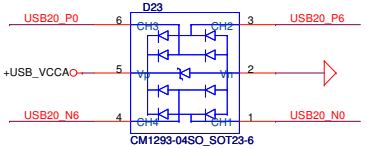
Bluetooth Conn.

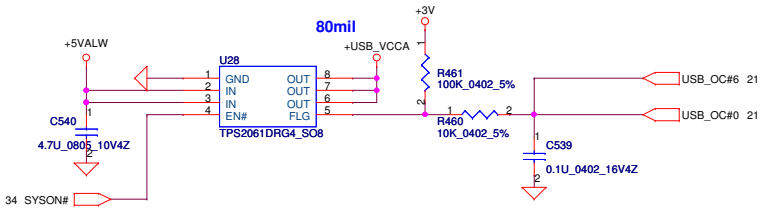




USB CONN.

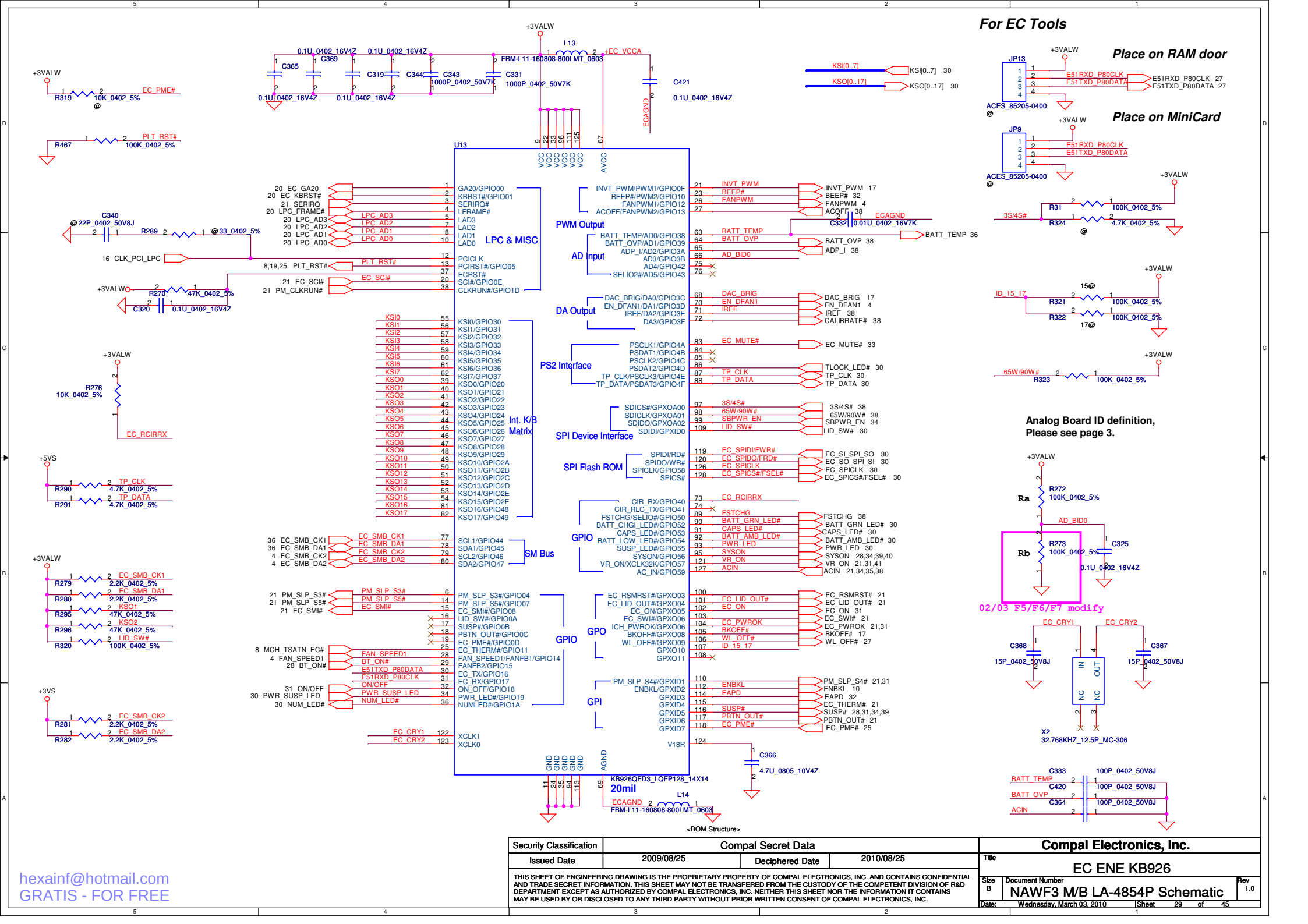






Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	NEW CARD & USB Connector		
Size B	Document Number NAWF3 M/B LA-4854P Schematic		Rev 1.0
Date: Wednesday, March 03, 2010	Sheet 28 of 45		



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

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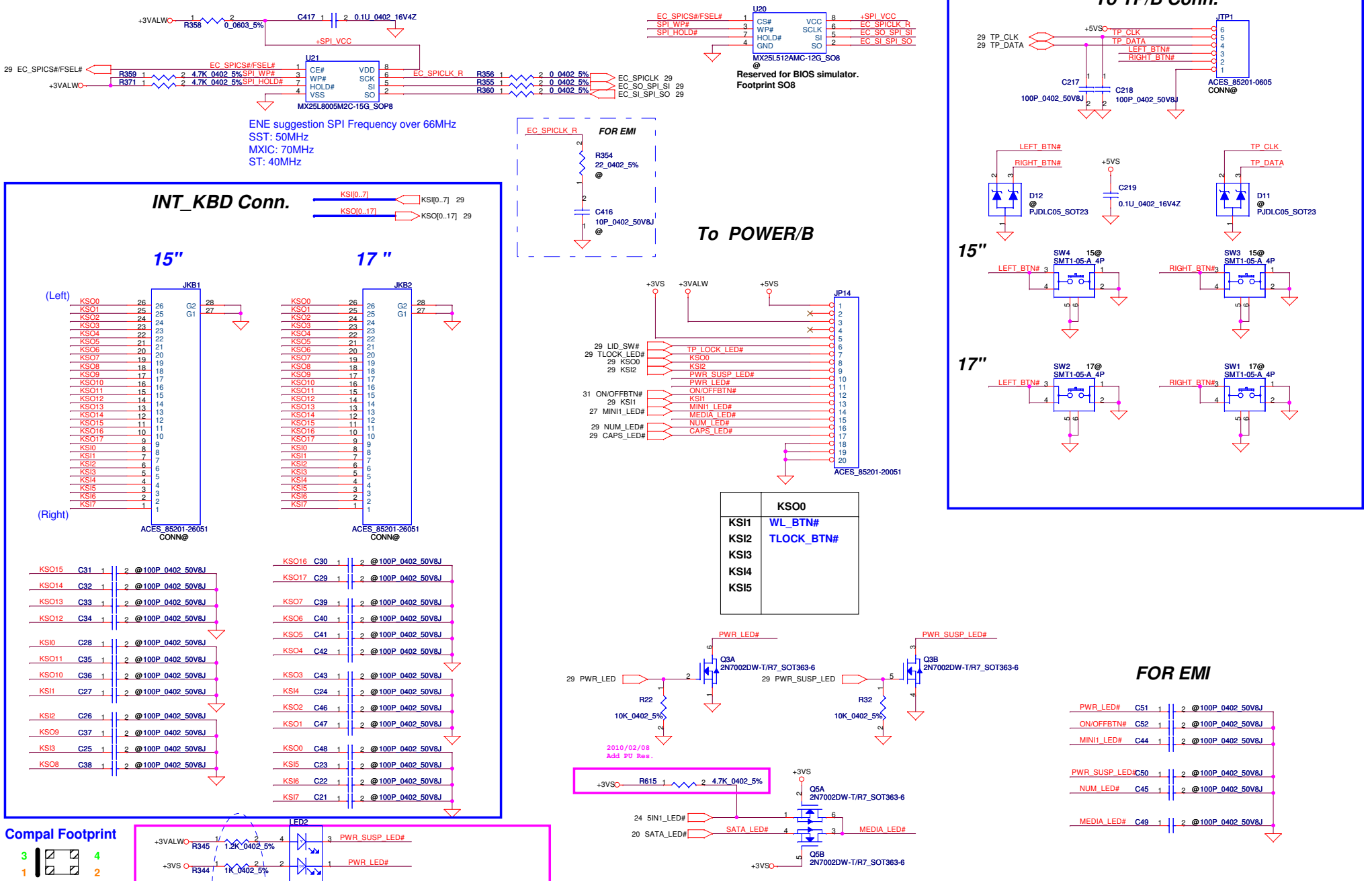
Compal Electronics, Inc.

Title	EC ENE KB926	
Size B	Document Number NAWF3 M/B LA-4854P Schematic	Rev 1.0
Date: Wednesday, March 03, 2010	Sheet 29 of 45	



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

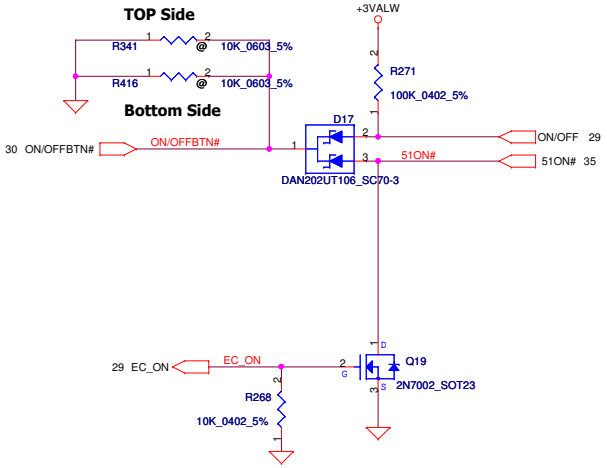
Title: BIOS, I/O Port & K/B Connector

Size: B | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

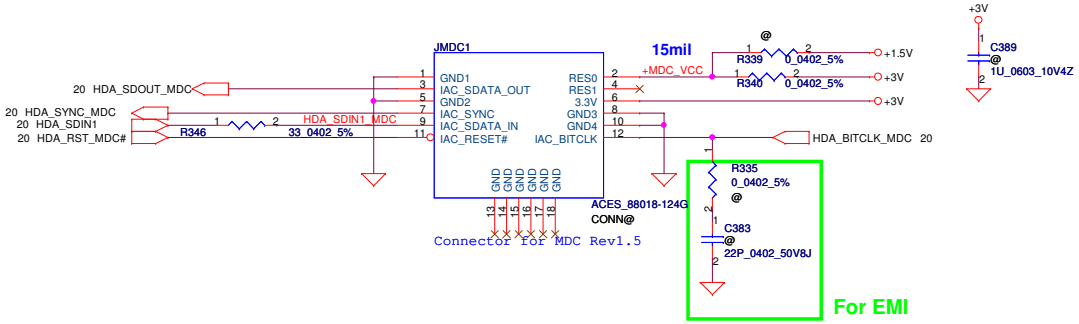
Date: Wednesday, March 03, 2010 | Sheet 30 of 45

Power Button

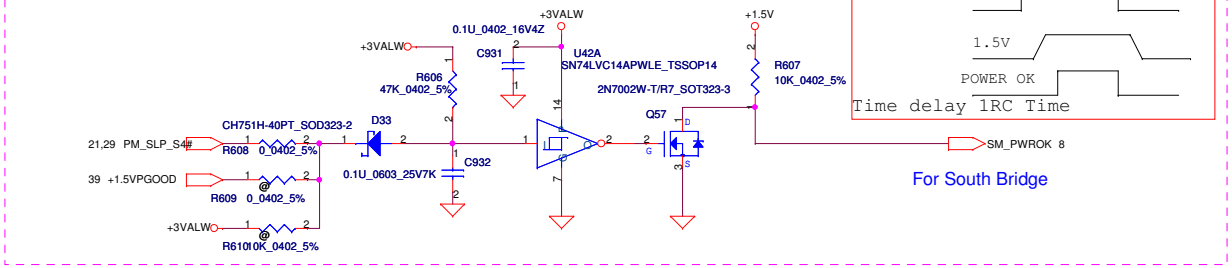
ON/OFF switch



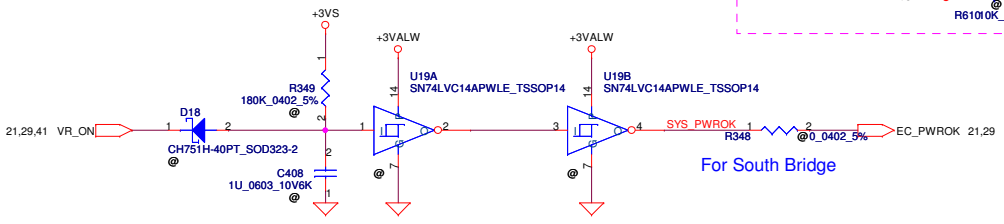
HDA MDC Conn.

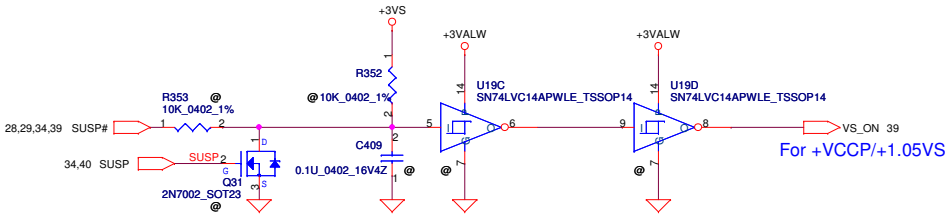


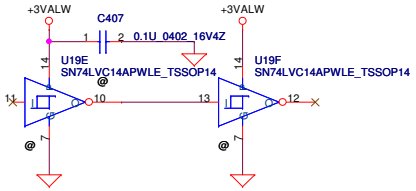
DDR3



Power ON Circuit



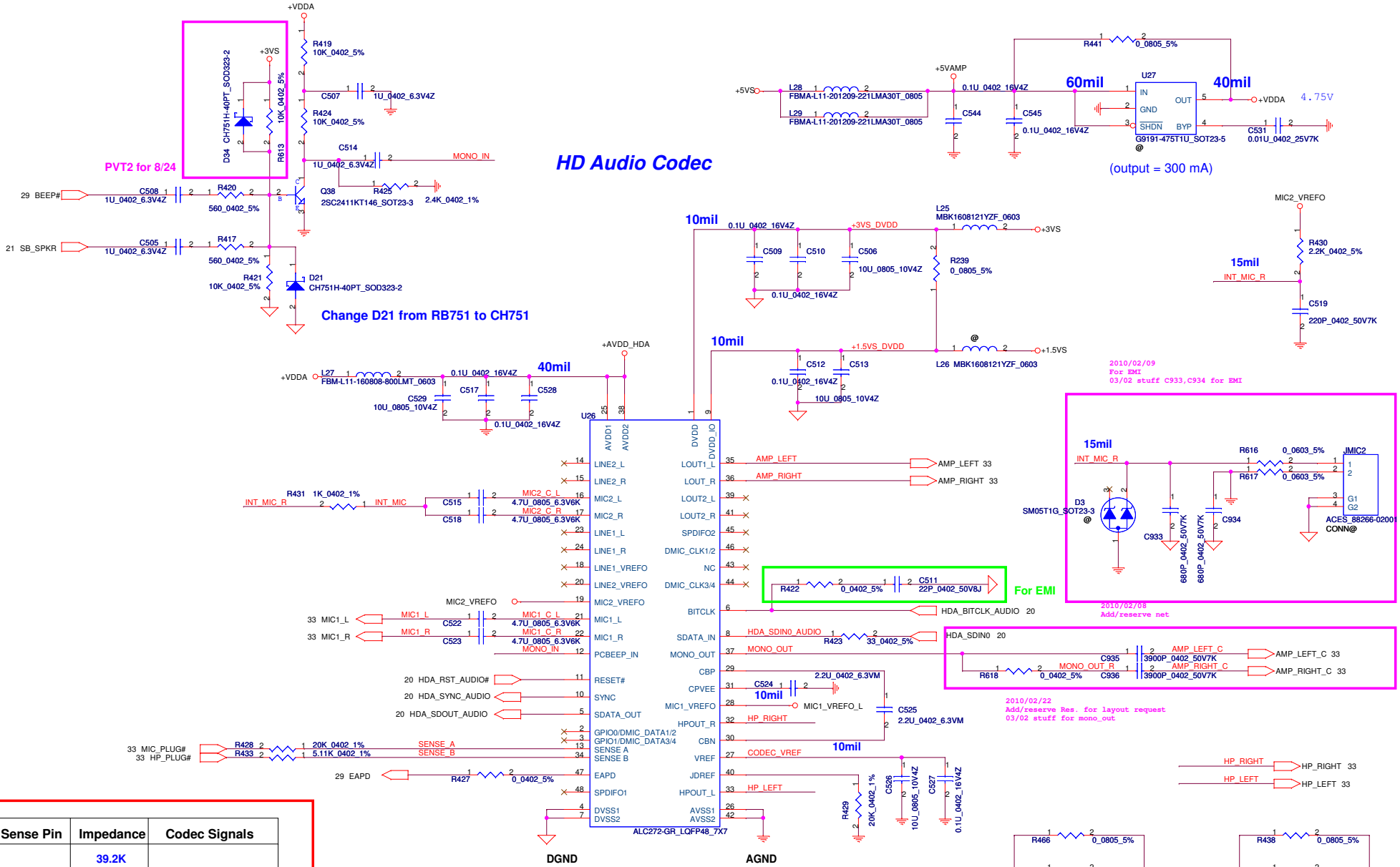




Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.	
Title	Power OK, Reset , MDC
Size B	Document Number NAWF3 M/B LA-4854P Schematic
Rev	1.0
Date: Wednesday, March 03, 2010	Sheet 31 of 45

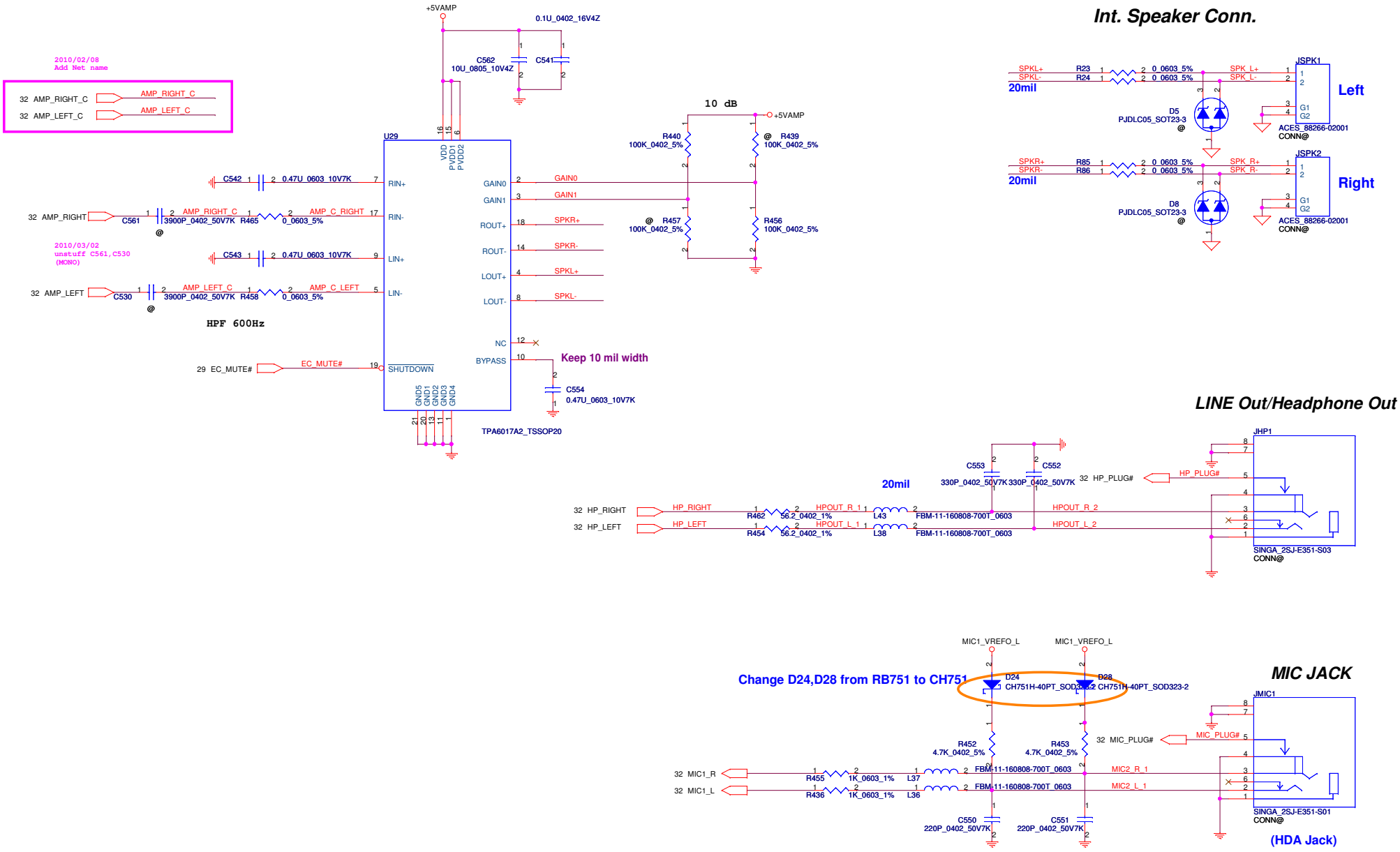
HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	
	20K	PORT-B (PIN 21, 22)
	10K	
	5.1K	
SENSE B	39.2K	
	20K	
	10K	
	5.1K	PORT-H (PIN 32,33)

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

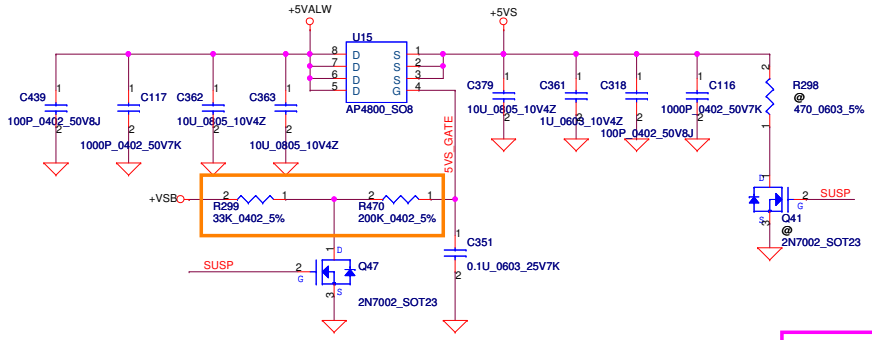
Compal Electronics, Inc.	
Title	HD Audio Codec ALC272
Size: B	Document Number: NAWF3 M/B LA-4854P Schematic
Rev	1.0
Date: Wednesday, March 03, 2010	Sheet 32 of 45



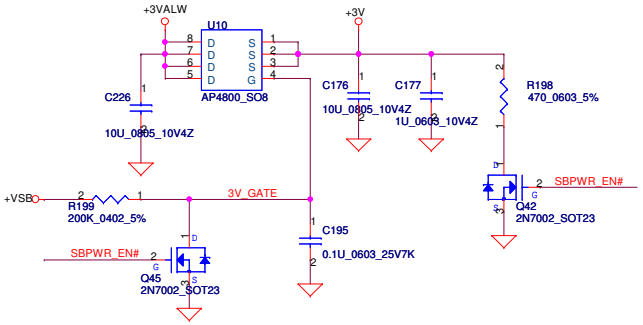
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date 2010/08/25	Title: Amplifier & Audio Jack

Size B	Document Number NAWF3 M/B LA-4854P Schematic		Rev 1.0
Date: Wednesday, March 03, 2010	Sheet 33 of 45		

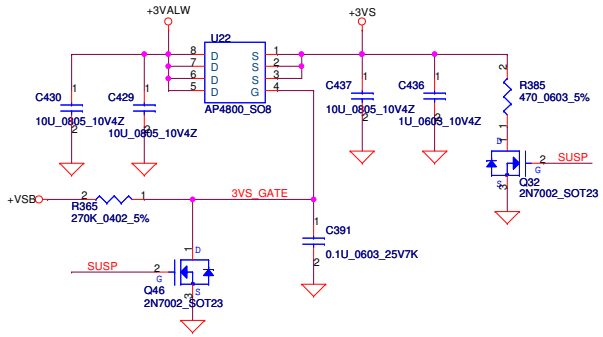
+5VALW TO +5VS



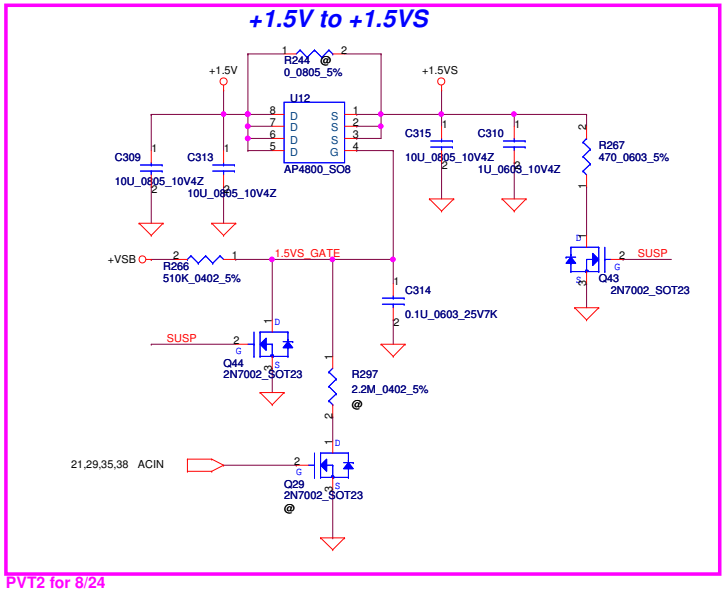
+3VALW TO +3V_SB(ICH8M AUX Power)



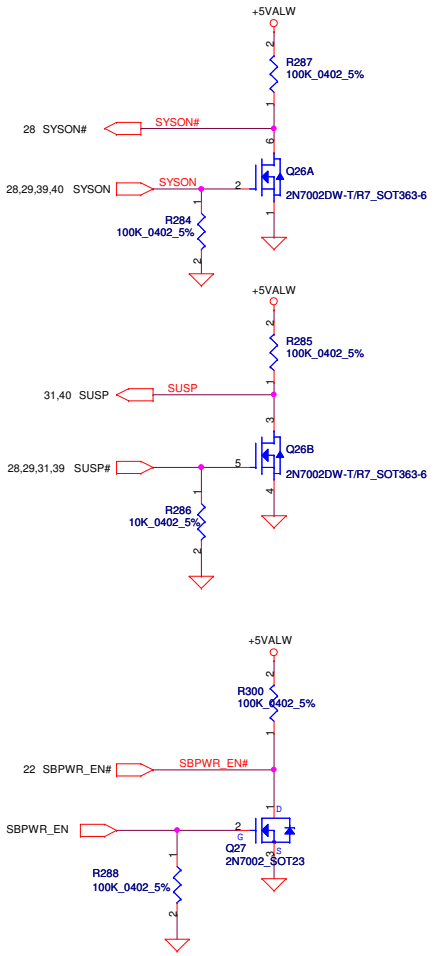
+3VALW TO +3VS

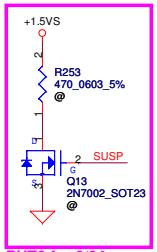


+1.5V to +1.5VS

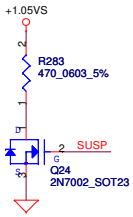


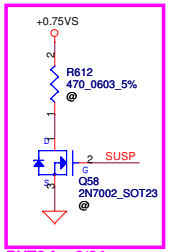
PVT2 for 8/24



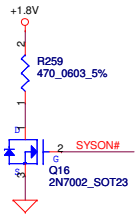


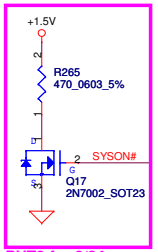
PVT2 for 8/24





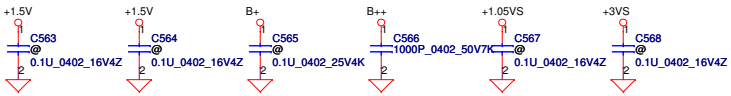
PVT2 for 8/24





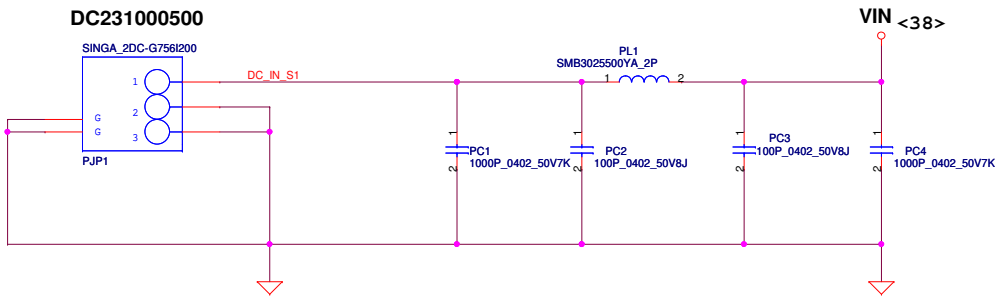
PVT2 for 8/24

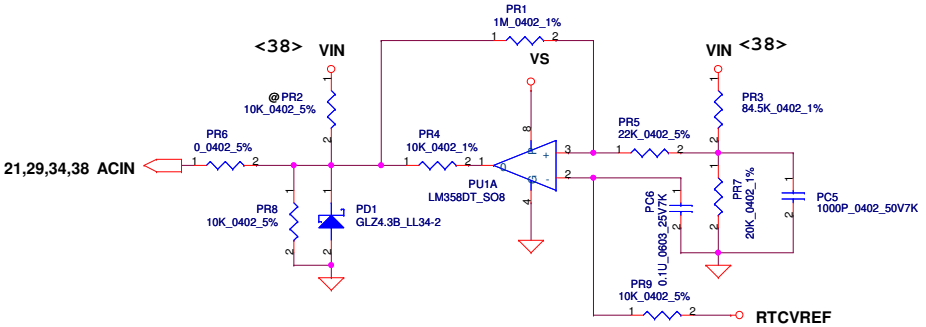
Reserve for EMI request

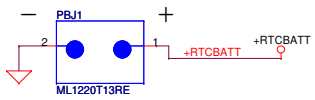


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date 2010/08/25	Title: DC Interface

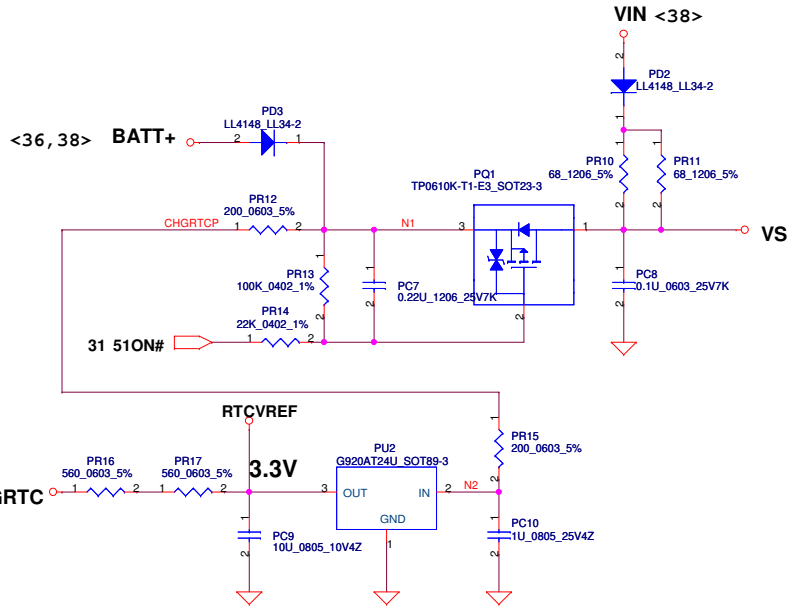
Size: B	Document Number: NAWF3 M/B LA-4854P Schematic		Rev: 1.0
Date: Wednesday, March 03, 2010	Sheet 34 of 45		

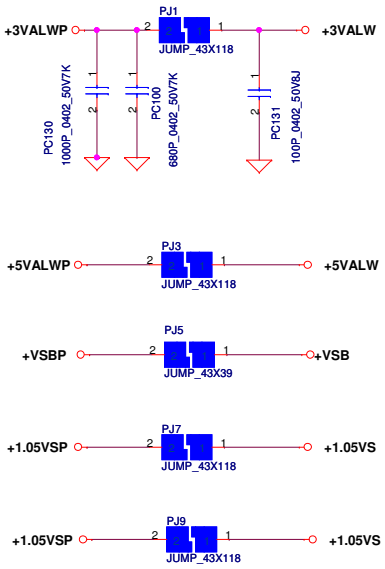




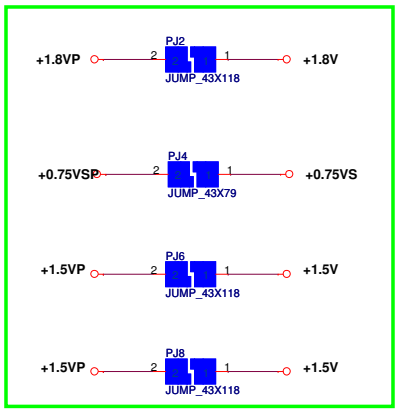


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





Delete (PJ16/PJ17/PJ18)
1.1VLDO + VGA_CORE JUMPER



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	DCIN & DETECTOR		
Size: Custom	Document Number: NAWF3 M/B LA-4854P Schematic		Rev: 1.0
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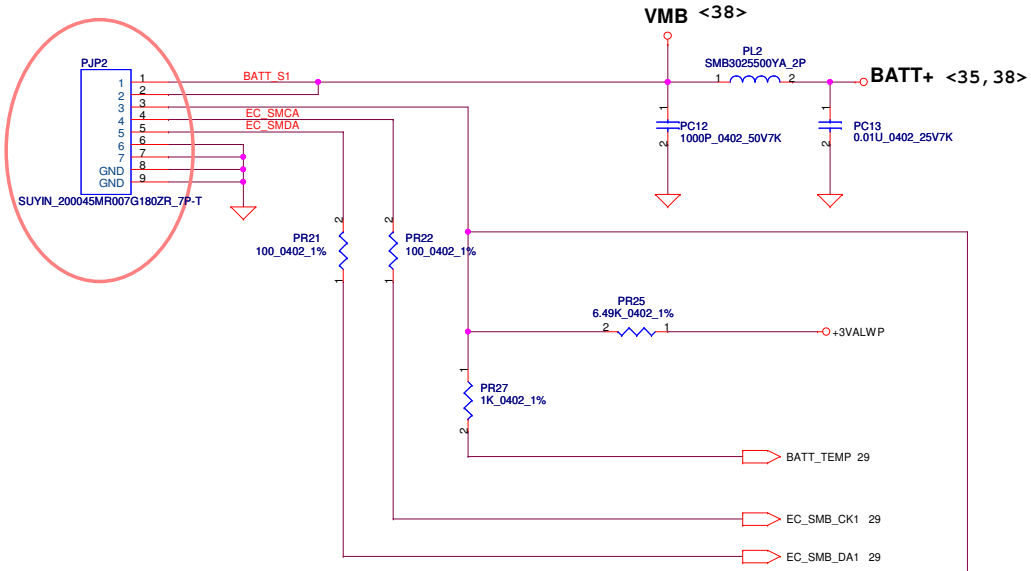
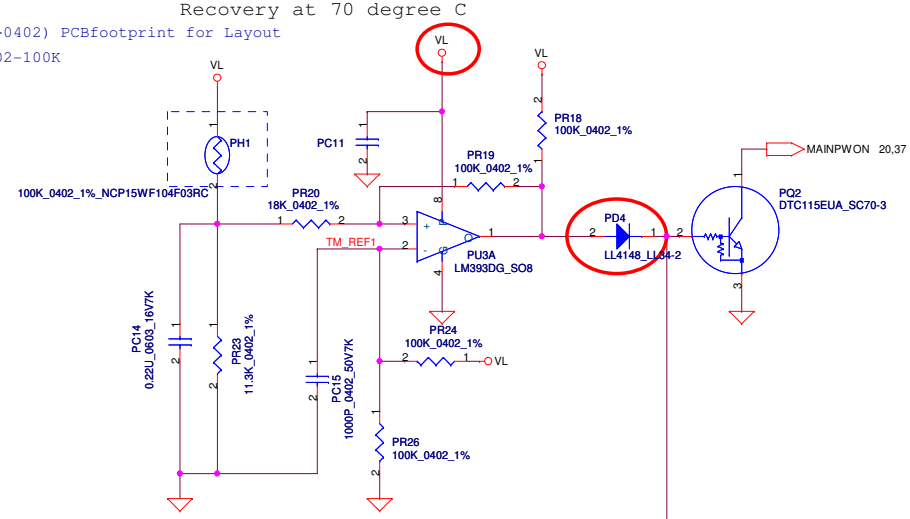
PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C

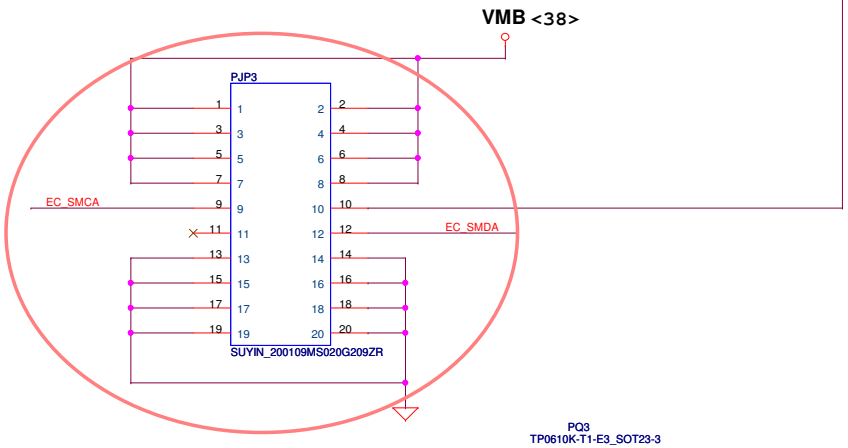
2009_08_06 (0603->0402) PCBfootprint for Layout
Change P/N for 0402-100K

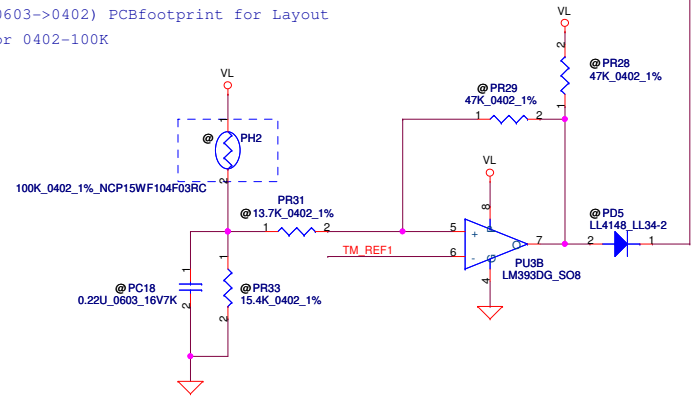


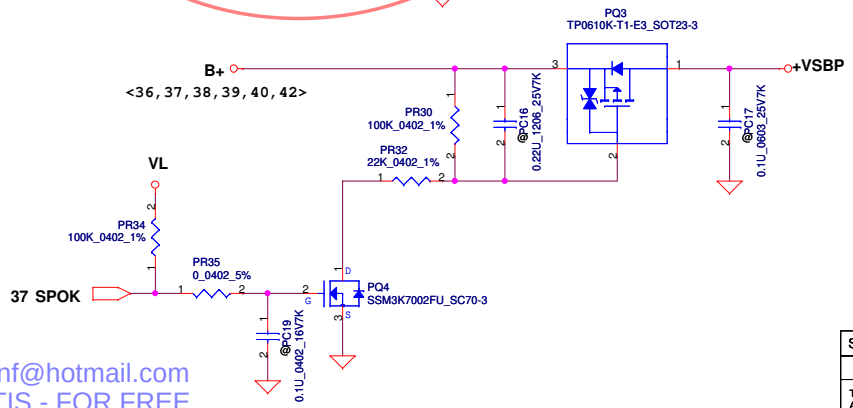


PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 70 degree C

2009_08_06 (0603->0402) PCBfootprint for Layout
Change P/N for 0402-100K







Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

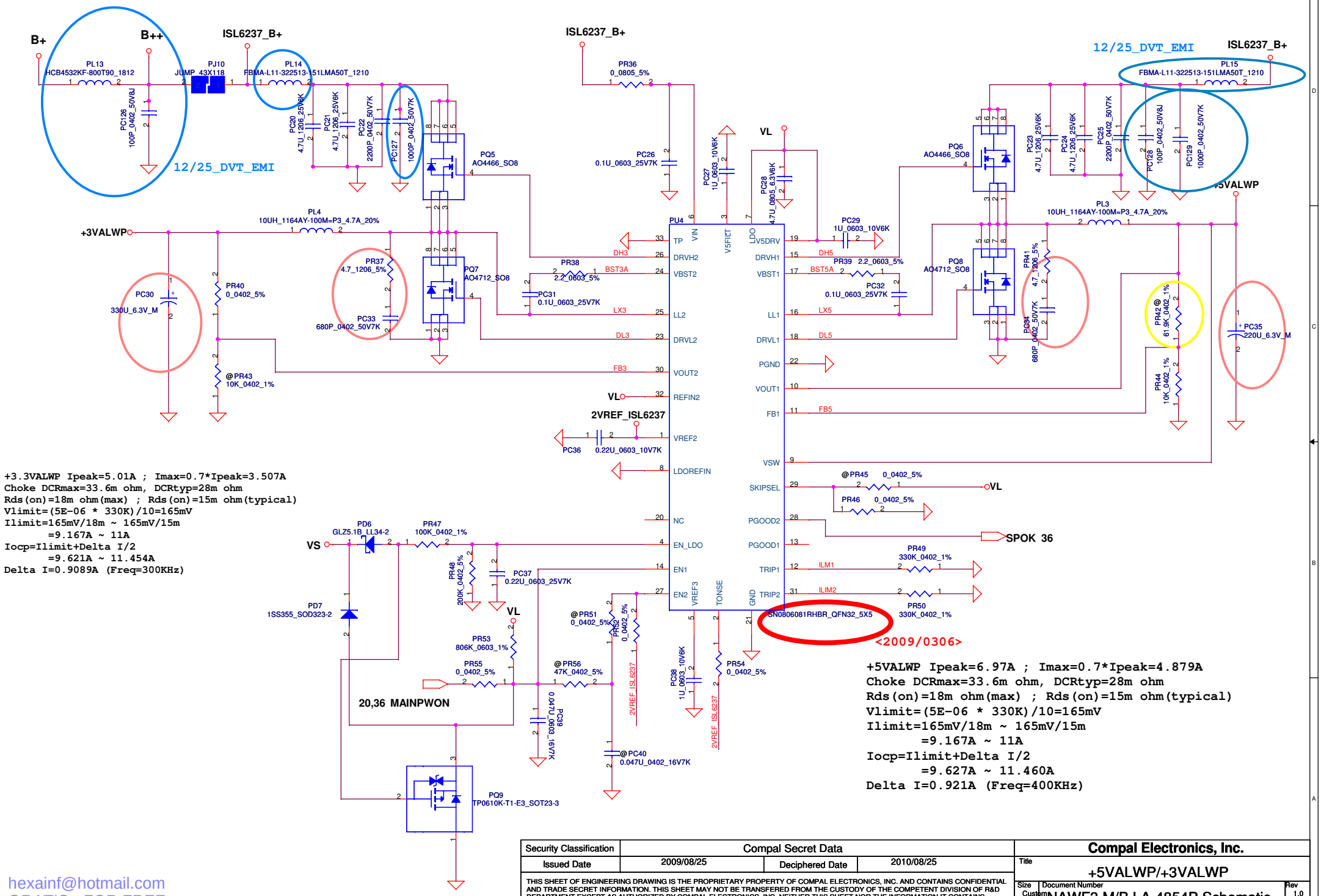
Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 36 of 45

<36,37,38,39,40,42>



+3.3VALWP Ipeak=5.01A ; Imax=0.7*Ipeak=3.507A
Choke DCRmax=33.6m ohm, DCRtyp=28m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.621A ~ 11.454A
Delta I=0.9089A (Freq=300KHz)

<2009/0306>

+5VALWP Ipeak=6.97A ; Imax=0.7*Ipeak=4.879A
Choke DCRmax=33.6m ohm, DCRtyp=28m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.627A ~ 11.460A
Delta I=0.921A (Freq=400KHz)

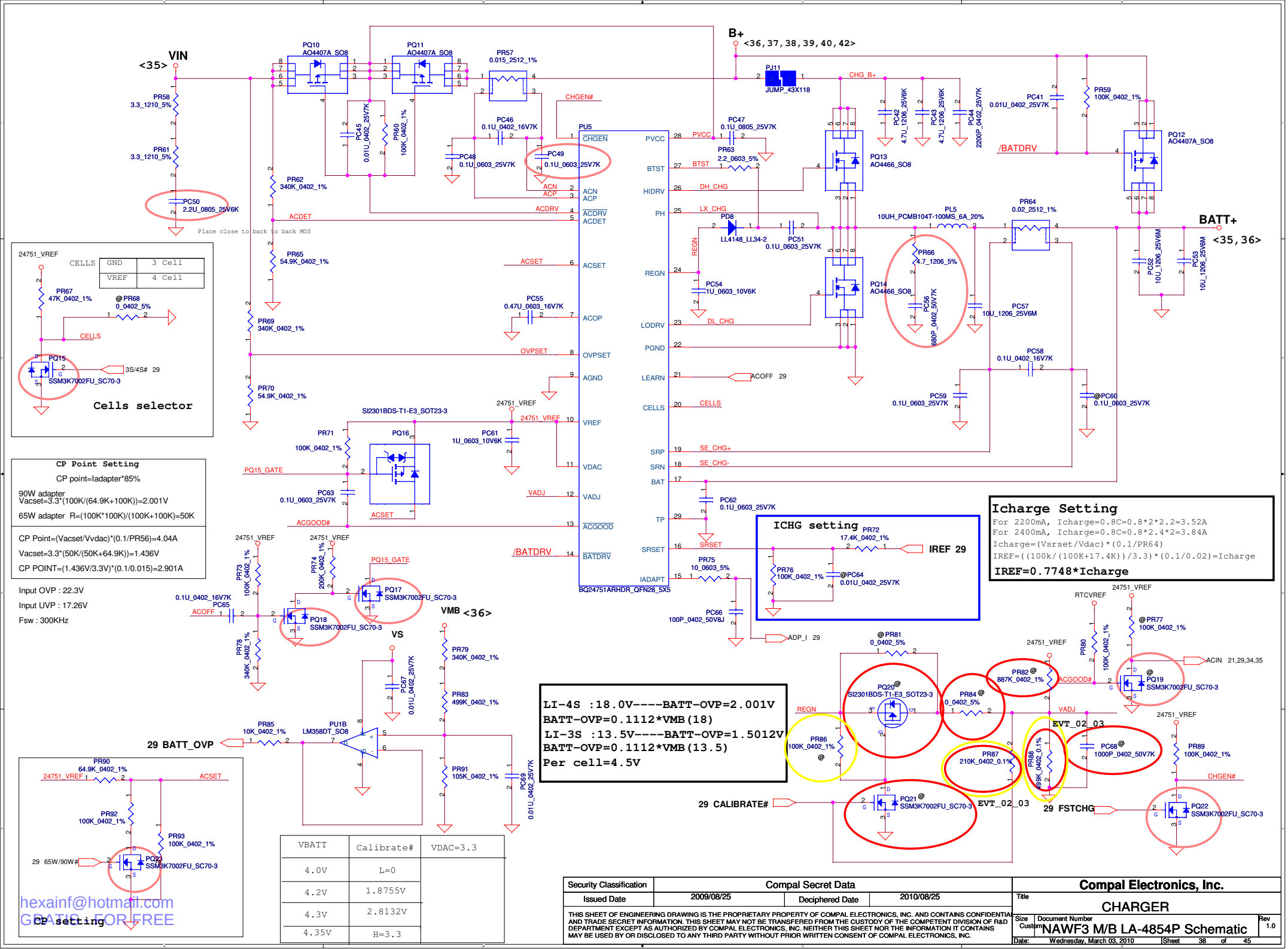
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 37 of 45


VIN
<35>
B+
<36,37,38,39,40,42>
BATT+
<35,36>
PQ10 AO4407A_SO8
PQ11 AO4407A_SO8
PR57 0.015_2512_1%
PJ11 JUMP_43X118
CHG_B+
PR58 3.3_1210_5%
PR61 3.3_1210_5%
PC50 2.2U_0805_25V6K
Place close to back to back MOS
PC45 0.01U_0402_25V7K
PR60 100K_0402_1%
PC46 0.1U_0402_16V7K
PC48 0.1U_0603_25V7K
PC49 0.1U_0603_25V7K
CHGEN#
PU5
BQ24751ARHDR_QFN28_5X5
PC47 0.1U_0805_25V7K
PR63 2.2_0603_5%
PC41 0.01U_0402_25V7K
PR59 100K_0402_1%
PC42 4.7U_1206_25V6K
PC43 4.7U_1206_25V6K
PC44 2200P_0402_25V7K
/BATDRV
PQ12 AO4407A_SO8
PQ13 AO4466_SO8
PR62 340K_0402_1%
ACDET
ACN
ACP
ACDRV
DH_CHG
LX_CHG
PD8 LL4148_LL34-2
PC51 0.1U_0603_25V7K
PL5 10UH_PCMB104T-100MS_6A_20%
PR64 0.02_2512_1%
PR65 54.9K_0402_1%
ACSET
PC55 0.47U_0603_16V7K
ACOP
PR66 4.7_1206_5%
PC56 680P_0402_50V7K
PQ14 AO4466_SO8
PC57 10U_1206_25V6M
PC52 10U_1206_25V6M
PC53 10U_1206_25V6M
PR69 340K_0402_1%
OVPSET
PC54 1U_0603_10V6K
REGN
DL_CHG
LODRV
PGND
LEARN
ACOFF 29
PC58 0.1U_0402_16V7K
PC59 0.1U_0603_25V7K
@PC60 0.1U_0603_25V7K
PR70 54.9K_0402_1%
AGND
CELLS
SRP
SRN
BAT
SE_CHG+
SE_CHG-
24751_VREF
VREF
SI2301BDS-T1-E3_SOT23-3
PR71 100K_0402_1%
PQ16
PC61 1U_0603_10V6K
PQ15_GATE
PC63 0.1U_0603_25V7K
VDAC
VADJ
ACGOOD#
ACGOOD
PC62 0.1U_0603_25V7K
TP
SRSET
IADAPT
PR75 10_0603_5%
PC66 100P_0402_50V8J
ADP_I 29
ICHG setting
PR72 17.4K_0402_1%
IREF 29
PR76 100K_0402_1%
@PC64 0.01U_0402_25V7K
Icharge Setting
For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
For 2400mA, Icharge=0.8C=0.8*2.4*2=3.84A
Icharge=(Vsrset/Vdac)*(0.1/PR64)
IREF=((100k/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge
IREF=0.7748*Icharge
24751_VREF
CELLS
GND 3 Cell
VREF 4 Cell
PR67 47K_0402_1%
@PR68 0_0402_5%
PQ15 SSM3K7002FU_SC70-3
3S/4S# 29
Cells selector
CP Point Setting
CP point=ladapter*85%
90W adapter
Vacset=3.3*(100K/(64.9K+100K))=2.001V
65W adapter R=(100K*100K)/(100K+100K)=50K
CP Point=(Vacset/Vvdac)*(0.1/PR56)=4.04A
Vacset=3.3*(50K/(50K+64.9K))=1.436V
CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz
PR73 100K_0402_1%
PR74 200K_0402_1%
PQ17 SSM3K7002FU_SC70-3
0.1U_0402_16V7K
PC65
ACOFF
PQ18 SSM3K7002FU_SC70-3
PR78 340K_0402_1%
VMB <36>
VS
PC67 0.01U_0402_25V7K
PR79 340K_0402_1%
PR83 499K_0402_1%
PR85 10K_0402_1%
PU1B LM358DT_SO8
29 BATT_OVP
PR91 105K_0402_1%
PC69 0.01U_0402_25V7K
LI-4S :18.0V----BATT-OVP=2.001V
BATT-OVP=0.1112*VMB(18)
LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB(13.5)
Per cell=4.5V
@PR81 0_0402_5%
PQ20@ SI2301BDS-T1-E3_SOT23-3
PR84@ 0_0402_5%
PR82@ 887K_0402_1%
REGN
VADJ
PR86 100K_0402_1%
PR87 210K_0402_0.1%
PR88 499K_0402_0.1%
EVT_02_03
PC68@ 1000P_0402_50V7K
PQ21@ SSM3K7002FU_SC70-3
29 CALIBRATE#
29 FSTCHG
RTCVREF
@PR77 100K_0402_1%
PR80 100K_0402_1%
ACIN 21,29,34,35
@PQ19 SSM3K7002FU_SC70-3
PR89 100K_0402_1%
CHGEN#
PQ22 SSM3K7002FU_SC70-3
PR90 64.9K_0402_1%
ACSET
PR92 100K_0402_1%
PR93 100K_0402_1%
29 65W/90W#
PQ23 SSM3K7002FU_SC70-3
CP setting
VBATT
Calibrate#
VDAC=3.3
4.0V
L=0
4.2V
1.8755V
4.3V
2.8132V
4.35V
H=3.3
hexainf@hotmail.com
GRATIS FOR FREE
Security Classification
Compal Secret Data
Issued Date
2009/08/25
Deciphered Date
2010/08/25
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Compal Electronics, Inc.
Title
CHARGER
Size Custom
Document Number
NAWF3 M/B LA-4854P Schematic
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Date: Wednesday, March 03, 2010
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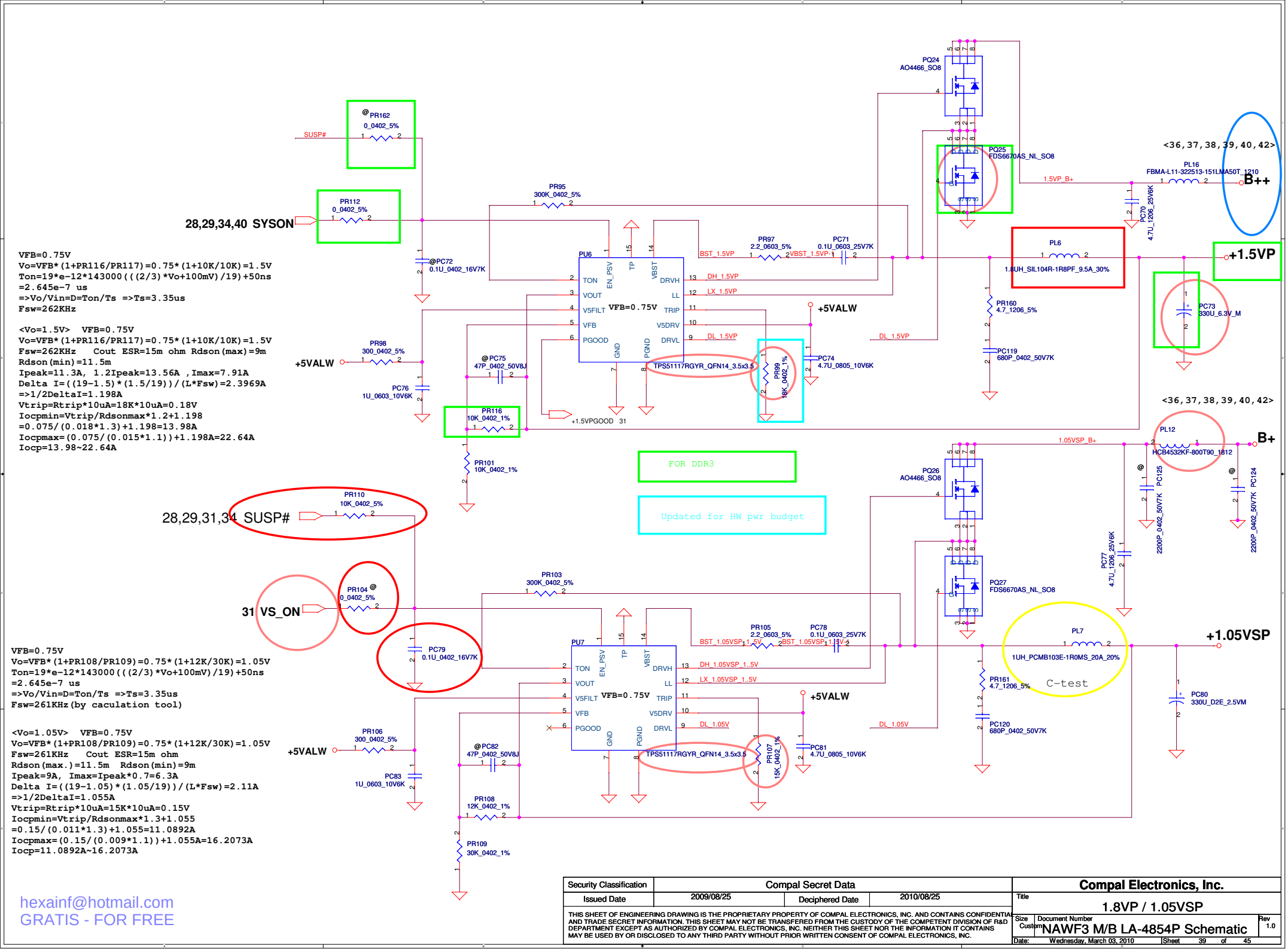


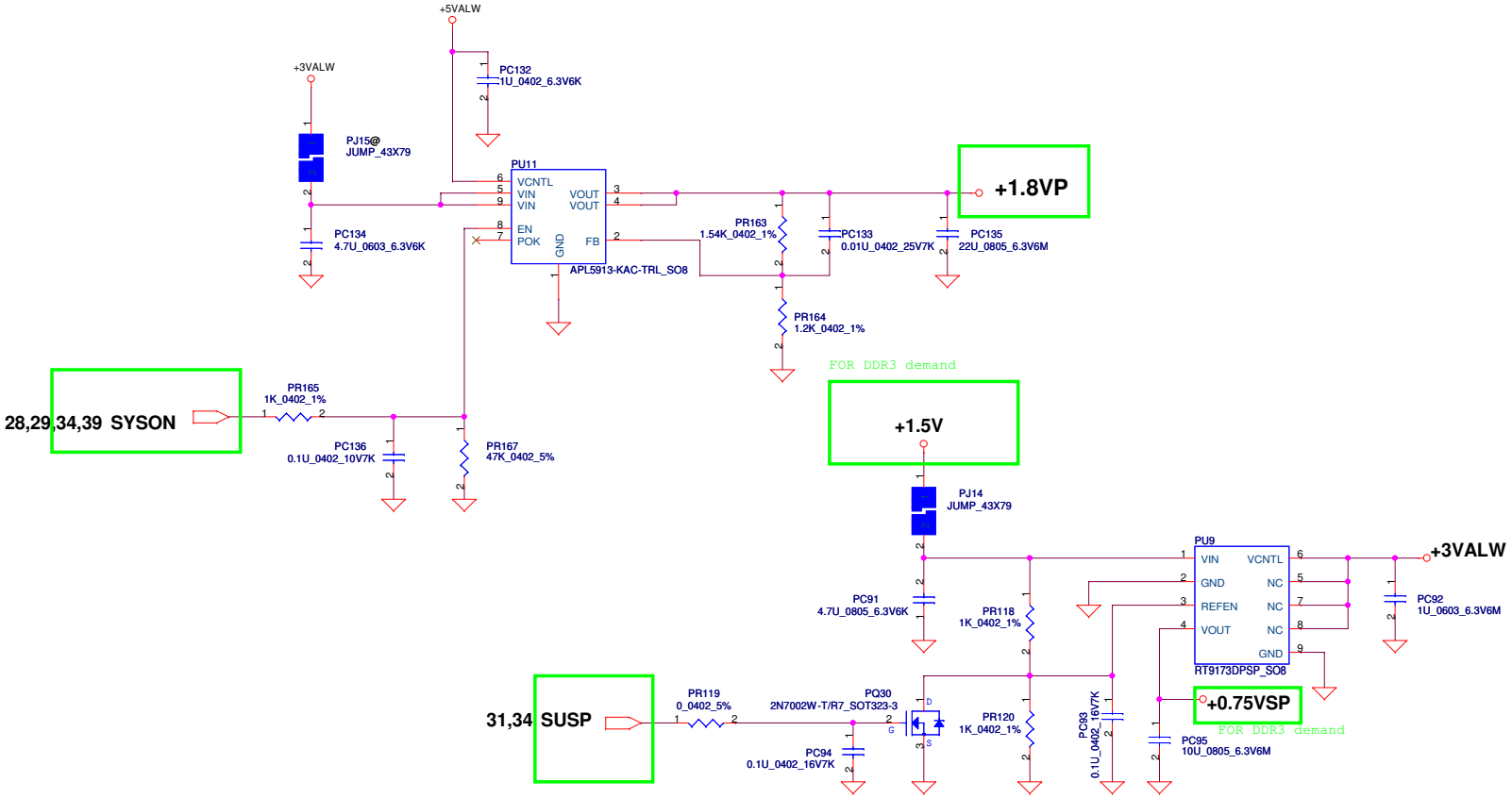
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: 1.8VP / 1.05VSP

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 39 of 45



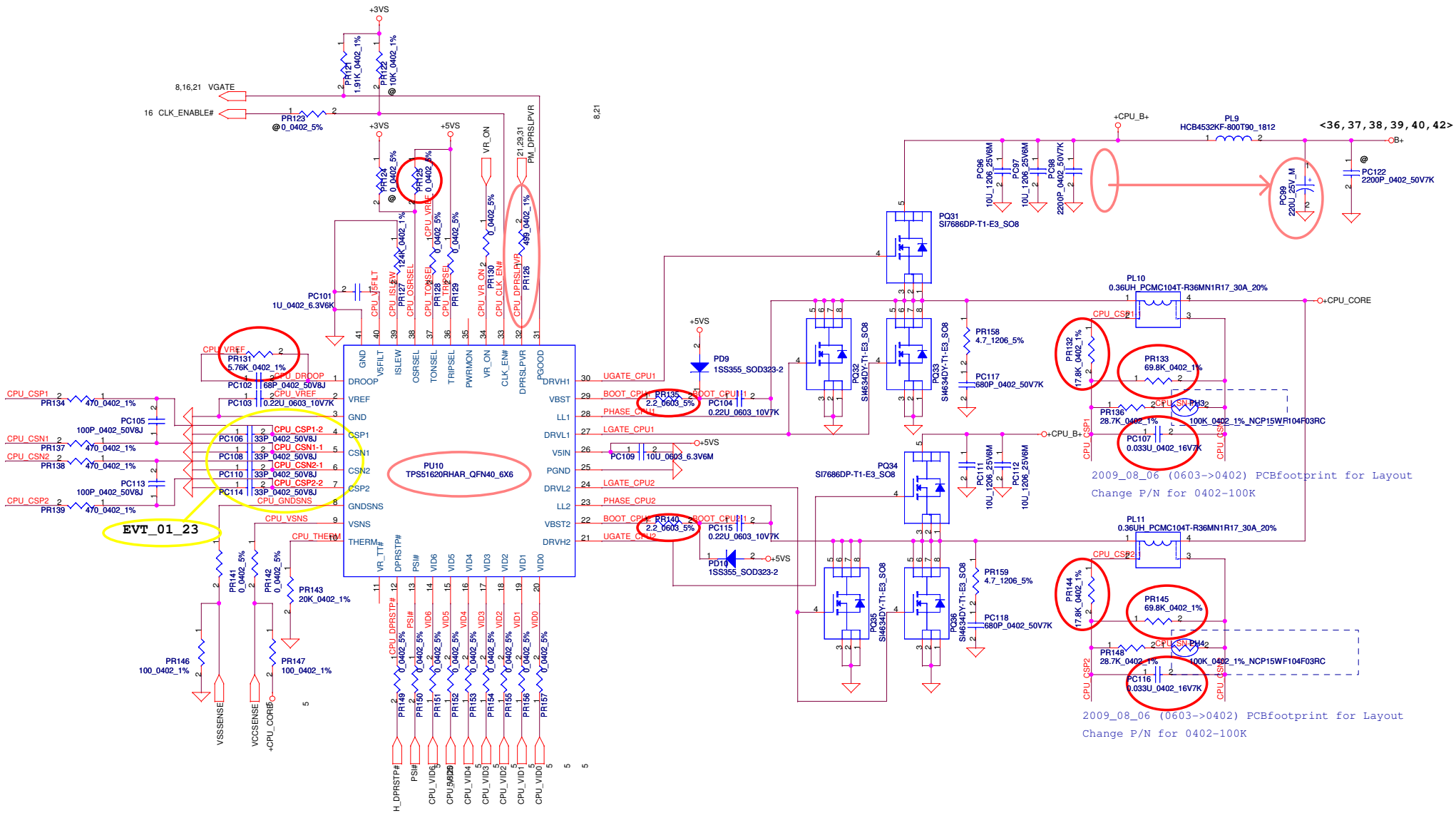
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: +1.5VP

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

Date: Wednesday, March 03, 2010 | Sheet 40 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	+CPU_CORE		
Size: Custom	Document Number: NAWF3 M/B LA-4854P Schematic		Rev: 1.0
Date: Wednesday, March 03, 2010	Sheet 41 of 45		

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add PC57 :10U_1206_25V_6M	0.1	38	Add PC57 :10U_1206_25V_6M	20080902	EVT
2		Add snubber for EMI	0.1	42	Add snubber for EMI	20080915	EVT
3		Shift PC99 from +cpu_B+ to B+	0.1	42	Shift PC99 from +cpu_B+ to B+	20080915	EVT
4		Add PJ15 to B+	0.1	39	Add PJ15 to B+	20080915	EVT
5		PR135 and PR140 change to 0_0603_5%	0.1	42	PR135 and PR140 change to 0_0603_5%	20080915	EVT
6	Charger feedback trace too long	ADD PC49	0.2	38	ADD PC49	20081124	DVT
7	Power sequence error	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	0.2	40	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	20081124	DVT
8	Load line over spec	PR131: change to 5.76K_0402_1%	0.2	42	PR131: change to 5.76K_0402_1%	20081124	DVT
9	3D hang	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	0.2	38	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	20081124	DVT
10	3D hang	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	0.2	39	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	20081124	DVT
11	3D hang	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	0.2	39	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	20081124	DVT
12	EMI solution	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	0.2	37	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	20081124	DVT
13	EMI solution	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	0.2	42	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	20081124	DVT
16	EMI solution	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	0.2	42	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	20081124	DVT
17	EMI solution	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	0.2	39	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	20081124	DVT

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
18	Battery & HW solution	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1% +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K +1.5VP PR112: Reserve(@) 0_0402_5%	0.2	38 39 40	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1% +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K +1.5VP PR112: Reserve(@) 0_0402_5%	20081124	DVT
19	EMI soultion	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	0.3	35 40	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	20081224	PVT
20	POWER Solution	+3VALWP/+5VALWP RT8206- Fix output 5V for HW no HDMI	0.3	37	+3VALWP/+5VALWP PR42: Reserve 61.9K_0402_1%	20090111	PVT

COMPAL ELECTRONICS		
Title: PIR POWER2		
Size	Document Number: KAWF0 M/B LA-4431P Schematic	Rev: 0.2
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Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
21	EMI solution	Reduce the Noise	0.3	37	Add PL 13 (HCB4532KF-800T90_1812) Add PL 14 (FBMA-L11-322513-151LMA50T_1210) Add PL 15 (FBMA-L11-322513-151LMA50T_1210) Add PC126 (100P_0402_50V8J) Add PC128 (100P_0402_50V8J) Add PC129 (1000P_0402_50V7K)	20090112	PVT
22	Battery solution	Adjust battery voltage	0.3	38	Reserve PR86 (100K_0402_1%)	20090112	PVT
23	Saturation current	1.8u choke saturation current too small	0.3	39	change PL7 to 1UH_PCMB103E-1R0MS_20A_20%	20090113	PVT
24	GP BOM	Tolerance: K:+-10% ; J:+-5%	0.4	42	Change PC106 to 33P_0402_50V8J Change PC108 to 33P_0402_50V8J Change PC110 to 33P_0402_50V8J Change PC114 to 33P_0402_50V8J	20090123	PVT

COMPAL ELECTRONICS

Title <Title> PIR POWER3

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09/01 Change DDR2 as DDR3 PIR

1. P.8 Remove R181 ; Stuff R220, R222 ; Unstuff R221
2. P.14 Remove RP28, RP27, RP19, RP18, RP10, RP9, RP3, RP25, RP26, RP17, RP16, RP8, RP7, R138, R200, R195, R350, R351
   Remove C148, C186, C185, C134, C202, C415, C412, C413, C414, C187, C149, C146,C183, C188, C147, C203, C150, C135
   Remove C201, C204, C184, C200, C285, C411, C410
   Change JDIMM2 P/N
   Add R598~R602 ; C887~C908
3. P.15 Remove RP30, RP24, RP23, RP15, RP14, RP6, RP2, RP22, RP21, RP13, RP12, RP5, RP1, R137, R52, R53
   Remove C283, C284, C197, C181, C143, C198, C144, C182, C210, C180, C142, C131, C212, C133, C179
   Remove C211, C196, C199, C132, C209, C141, C140, C178, C145
   Change JDIMM1 P/N
   Add R603~R605 ; C909~C930
4. P.31 Add R608, R607, R606, C931, C932, D33, U42, Q57
5. P.34 Unstuff R244, R253, Q13 ; Stuff C309, C313, C310, C314, R266, R267, Q43, Q44, U12, R265, Q17

09/01 Other PIR

1. P.17 Unstuff D20, R411 ; Add R611 for DISPOFF#
2. P.19 Unstuff U8, R83 ; Add R614 for PLT_RST#
3. P.21 Add U43 ; Remove R75 for ICH_VGATE
4. P.23 Unstuff C570
5. P.30 Change LED1, LED2 P/N
6. P.32 Add D34, R613 for Audio BEEP#

09/17

1. P.25 Change C81, C82 27pF as 33pF for Xtal 25MHz(TXC suggest value)
2. P.20 Change C163, C164 18pF as 15pF for Xtal 32.768kHz (TXC suggest value)
3. P.29 Change R273 8.2k ohm as 18k ohm for Board ID

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Compal Electronics, Inc.

Title: HW (PWR)

Size: Custom | Document Number: NAWF3 M/B LA-4854P Schematic | Rev: 1.0

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