UMA & Optimus Schematics Document

Sandy Bridge

Intel PCH

2010-08-16

REV : SB

DY :None Installed
UMA:UMA platform installed
OPS:Optimus

<Core Design>

緯創資通 Wistron Corporation
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Title: Cover Page		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 1 of 103	

Block Diagram (UMA/Optimus co-lay)

Project code : 91.4KZ01.001
PCB P/N : 48.4KZ01.0SB
Revision : 10250-SB

Audio BD
POWER BD
Finger Printer BD
IO BD (Cardreader+Audio+USB)
LED BD
USB

##OnMainBoard

VRAM 2GB/1GB/512MB 88,89,90,91
DDR3 800MHz
NVIDIA N12P-GE/GV N12M-GE 83.84,85,86,87
PCIe x 16 (Discrete only)

Intel CPU
Sandy Bridge
DDRIII: 1066/1333/1666 MHz 4,5,6,7,8,9,10
DDRIII 1066/1333/1666 Channel A
DDRIII 1066/1333/1666 Channel B
DDRIII Slot 0 1066/1333/1666 14
DDRIII Slot 1 1066/1333/1666 15

FDI x 4 x 2 (UMA only)
DMI x 4

HDMI 51
LCD 49
CRT 50
HDMI
LVDS
RGB CRT

Intel PCH Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25

PCIE x 1 → GLAN RTL8111E 31 → RJ45 CONN 55
PCIE x 1/USB2.0 x 1 → Mini-Card WLAN 65
SATA x 1/USB2.0 x 1 → Mini-Card WWAN 66 → SIM 66
USB 2.0 x 3 → MB USB x 3
USB 2.0 x 1/SATA x 1 → E-SATA/USB comb 57
SATA x 2 → HDD 56, ODD 56

Bluetooth 63
USB2.0 x 3
CAMERA 49
Finger Print BD
Finger Print 64
CardReader Realtek RTS5139 74
USB 2.0 x 1
I/O BD
SD/MMC+/MS/ MS Pro/xD

AZALIA
Azalia CODEC Codec_ALC272 29
Internal DMIC
HP1
MIC IN
I/O BD
2CH SPEAKER

SPI
Flash ROM 4MB 60
LPC Bus
LPC debug port 71

KBC NUVOTON NPCE795G 27
SMBus
G-Sensor 79
Touch PAD 69
Int. KB 69
Thermal EMC2103-2-AP 28
Fan 28

SYSTEM DC/DC RT8208A 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51218 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208A 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8015B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

<Core Design>

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Title: Block Diagram
Size: A3 | Document Number: LA470 | Rev: SB
Date: Tuesday, September 07, 2010 | Sheet 2 of 103

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Core Design>

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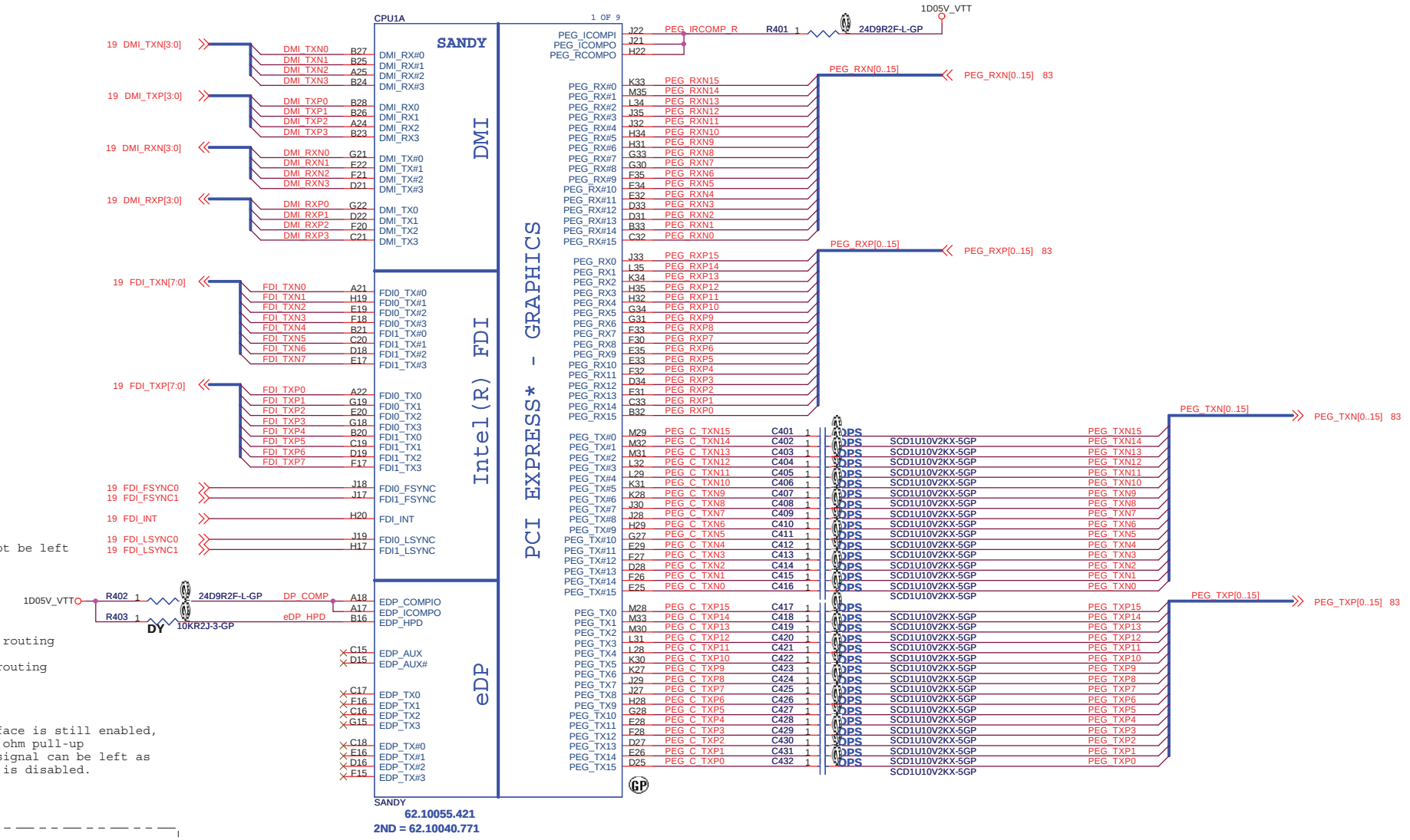
Title: Table of Content

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 3 of 103

SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-k ohm pull-up resistor on the motherboard. This signal can be left as no connect if entire eDP interface is disabled.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

<Core Design>

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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 4 of 103

SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

RN502 CLK_DP_P_R CLK_DP_N_R SRN1KJ-7-GP DY 1D05V_VTT SB_0830

CPU1D SANDY

MISC
18 H_SNB_IVB# C26 SNB_IVB#
TPAD14-GP TP501 SKTOCC# R AN34 SKTOCC#

CLOCKS
BCLK A28 BCLK# A27 CLK_EXP_P 20 CLK_EXP_N 20
DPLL_REF_SSCLK A16 DPLL_REF_SSCLK# A15 CLK_DP_P_R CLK_DP_N_R CLK_DP_P_R 20 CLK_DP_N_R 20

THERMAL
TPAD14-GP TP502 H_CATERR# AL33 CATERR#
22,27 H_PECI AN33 PECI
27,42 H_PROCHOT# R513 56R2J-4-GP H_PROCHOT# R AL32 PROCHOT#
22,36 H_THERMTRIP# AN32 THERMTRIP#

DDR3 MISC
SM_DRAMRST# R8 R502 4K99R2F-L-GP SM_DRAMRST# 37
SM_RCOMP0 AK1 SM_RCOMP_0 R506 140R2F-GP
SM_RCOMP1 A5 SM_RCOMP_1 R507 25D5R2F-GP
SM_RCOMP2 A4 SM_RCOMP_2 R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

1D05V_VTT R501 62R2J-GP H_PROCHOT# C502 SC47P50V2JN-3GP
R503 10KR2J-3-GP H_CPUPWRGD_R

PWR MANAGEMENT
19 H_PM_SYNC AM34 PM_SYNC
11,22,36,97 H_CPUPWRGD R504 0R2J-2-GP H_CPUPWRGD_R AP33 UNCOREPWRGOOD
19,37 PM_DRAM_PWRGD R505 0R2J-2-GP DY VDDPWRGOOD V8 SM_DRAMPWROK
37 VDDPWRGOOD
BUF_CPU_RST# AR33 RESET#

JTAG & BPM
PRDY# AP29 XDP_PRDY# TP511 TPAD14-GP
PREQ# AP27 XDP_PREQ# TP512 TPAD14-GP
TCK AR26 XDP_TCLK TP513 TPAD14-GP
TMS AR27 XDP_TMS TP514 TPAD14-GP
TRST# AP30 XDP_TRST# TP515 TPAD14-GP
TDI AR28 XDP_TDI TP516 TPAD14-GP
TDO AP26 XDP_TDO TP517 TPAD14-GP
DBR# AL35 XDP_DBRESET#
BPM#0 AT28 XDP_BPM0 TP503 TPAD14-GP
BPM#1 AR29 XDP_BPM1 TP504 TPAD14-GP
BPM#2 AR30 XDP_BPM2 TP505 TPAD14-GP
BPM#3 AT30 XDP_BPM3 TP506 TPAD14-GP
BPM#4 AP32 XDP_BPM4 TP507 TPAD14-GP
BPM#5 AR31 XDP_BPM5 TP508 TPAD14-GP
BPM#6 AT31 XDP_BPM6 TP509 TPAD14-GP
BPM#7 AR32 XDP_BPM7 TP510 TPAD14-GP

SB_0820

TPAD14-GP TP518 VDDPWRGOOD

SANDY
62.10055.421
2ND = 62.10040.771

1D05V_VTT RN501 XDP_TDO XDP_TMS XDP_TDI XDP_TCLK SRN51J-1-GP XDP_TRST# R511 51R2J-2-GP

3D3V_S0 22,36 XDP_DBRESET# XDP_DBRESET# R516 1KR2J-1-GP

11,18,27,31,36,65,66,71,83,97 PLT_RST# R510 1K5R2F-2-GP BUF_CPU_RST# R509 750R2F-GP

SB_0805

<Core Design>

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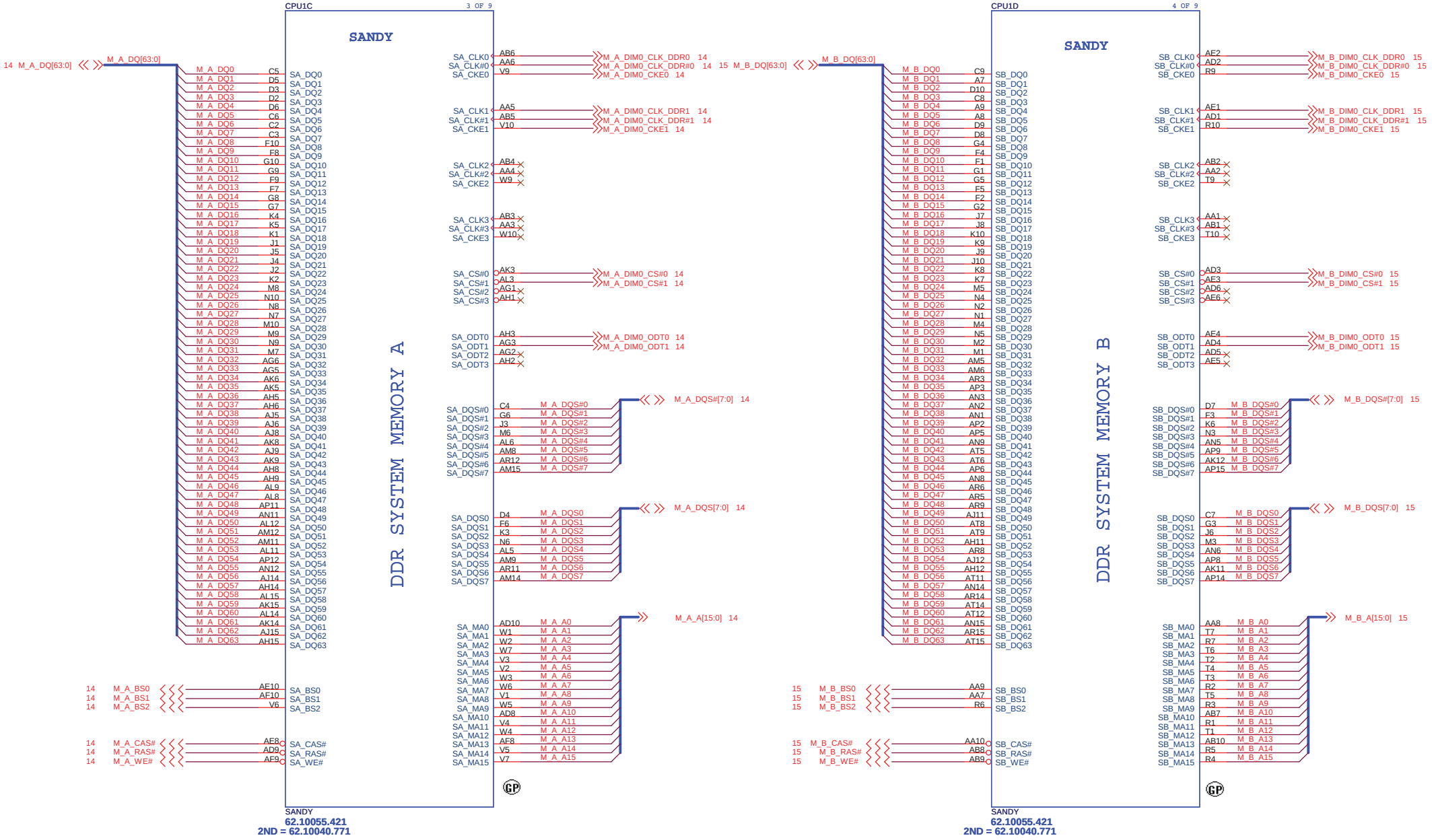
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 5 of 103

SSID = CPU



<Core Design>

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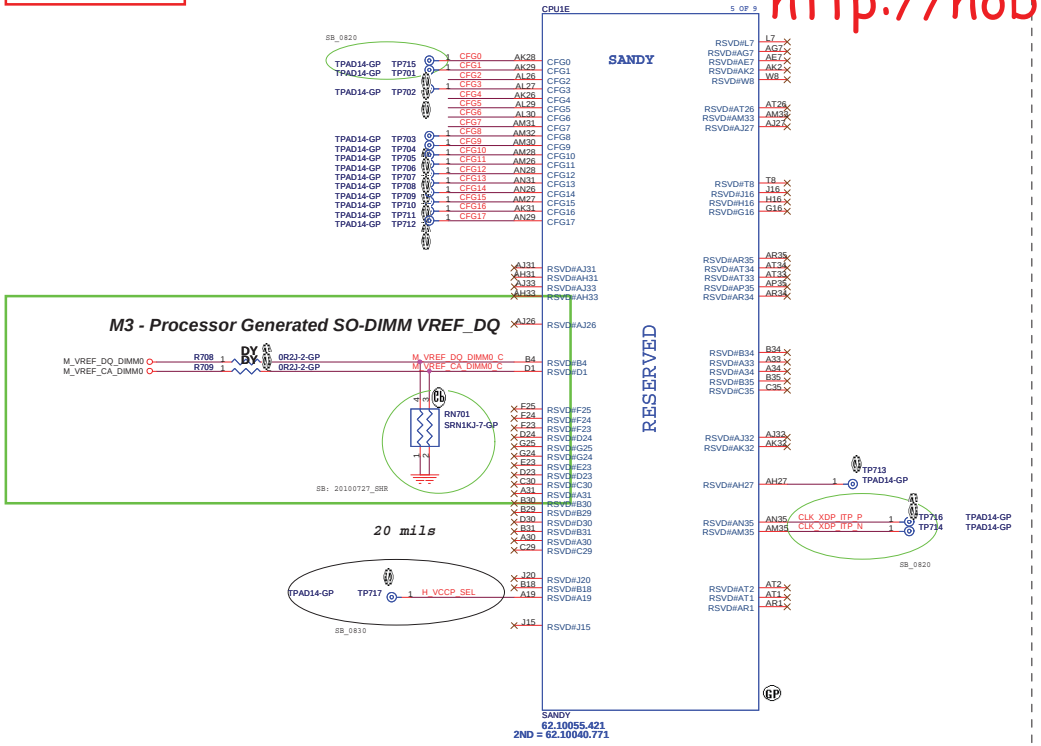
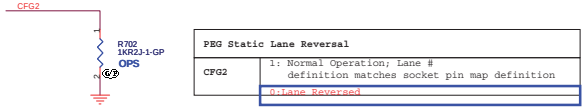
Title: CPU (DDR)

Size	Document Number	Rev
A3	LA470	SB

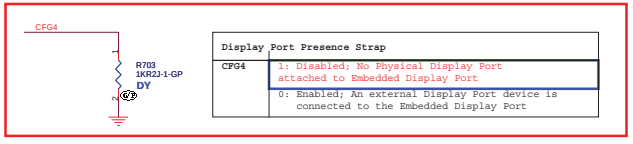
Date: Tuesday, September 07, 2010 Sheet 6 of 103

SSID = CPU

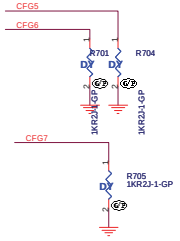




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

<Core Design>

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Title: CPU (RESERVED)

Size: A2 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 7 of 103

SSID = CPU

PROCESSOR CORE POWER

53A

VCC_CORE

C801 SC10U6D3V5KX-1GP
C802 SC10U6D3V5KX-1GP
C803 SC10U6D3V5KX-1GP
C804 SC10U6D3V5KX-1GP
C811 SC10U6D3V5KX-1GP

C815 SC10U6D3V5KX-1GP
C817 SC10U6D3V5KX-1GP
C818 SC10U6D3V5KX-1GP
C819 SC10U6D3V5KX-1GP
C820 SC10U6D3V5KX-1GP

C816 SC10U6D3V5KX-1GP
C821 SC10U6D3V5KX-1GP
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C824 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 SC10U6D3V5KX-1GP
C831 SC10U6D3V5KX-1GP
C828 SC10U6D3V5KX-1GP

CPU1F

SANDY

POWER

6 OF 9

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26
AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26
AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26
AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26
AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26
Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26
V35 V34 V33 V32 V31 V30 V29 V28 V27 V26
U35 U34 U33 U32 U31 U30 U29 U28 U27 U26
R35 R34 R33 R32 R31 R30 R29 R28 R27 R26
P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
VCC

PEG AND DDR

SVID

SENSE LINES

CORE SUPPLY

SANDY
62.10055.421
2ND = 62.10040.771

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 F14 E12

1D05V_VTT

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841 SC10U6D3V5KX-1GP

VCCIO: E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

1D05V_VTT

C812 C813 C814 C829 C830 C842 C843 C844 C845 SC10U6D3V5KX-1GP

VCCIO: J23

R804 need to close to CPU

1D05V_VTT

SB_0819

H_CPU_SVIDDAT_R R804 1 130R2F-1-GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 1 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK_R R805 1 0R2J-2-GP H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT_R R806 1 0R2J-2-GP H_CPU_SVIDDAT 42

SB_0819

R801, R802 need to close to CPU

VCC_CORE

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 VCCSENSE 42
VSS_SENSE AJ34 VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 VCCIO_SENSE 45
VSSIO_SENSE A10 VSSIO_SENSE 45

<Core Design>

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 8 of 103

SSID = CPU

POWER

CPU1G — 7 OF 9 — SANDY

PROCESSOR VAXG: 24A

VCC_GFXCORE

C901 C902 C903 C904 C905 C906 — SC10U6D3V5KX-1GP

RC901 SC33P50V2JN-3GP DY

C907 C908 C918 C919 C920 C921 — SC10U6D3V5KX-1GP

RC902 SC33P50V2JN-3GP DY

SB_0831

VAXG: AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

SENSE LINES

VAXG_SENSE — AK35
VSSAXG_SENSE — AK34

VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

VREF

SM_VREF — AL1

+V_SM_VREF_CNT → +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

GRAPHICS DDR3 -1.5V RAILS

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

VDDQ: AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 LJ7 U4 U1 P7 P4 P1

C909 C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

C916 C915 C917 — SC10U6D3V5KX-1GP

TC903 ST330U2VDM-4-GP DY

VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

0D85V_S0

R902 10R2J-2-GP — R902 need be close to pin H23.

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C925 C923 C922 C924 — SC10U6D3V5KX-1GP / SC1U10V2KX-1GP

VCCPLL: B6 A6 A2

MISC

VCCSA_SENSE — H23 → VCCSA_SENSE 48

FC_C22 — C22
VCCSA_VID1 — C24

H_FC_C22 → H_FC_C22 48
VCCSA_SEL → VCCSA_SEL 48

RN901 SRN1KJ-7-GP

SANDY
62.10055.421
2ND = 62.10040.771

Close to CPU

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

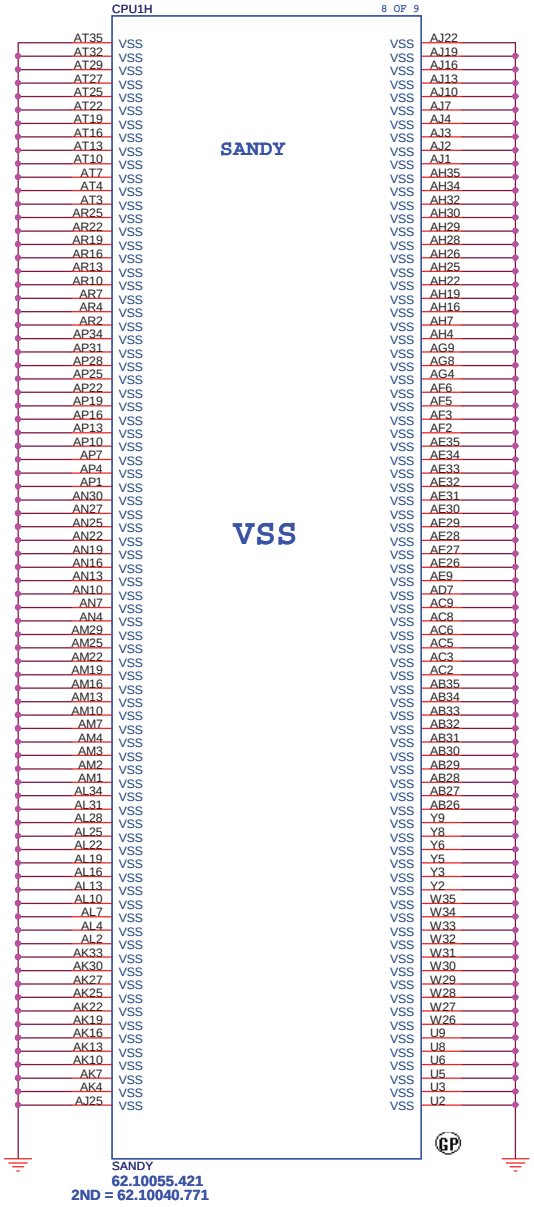
<Core Design>

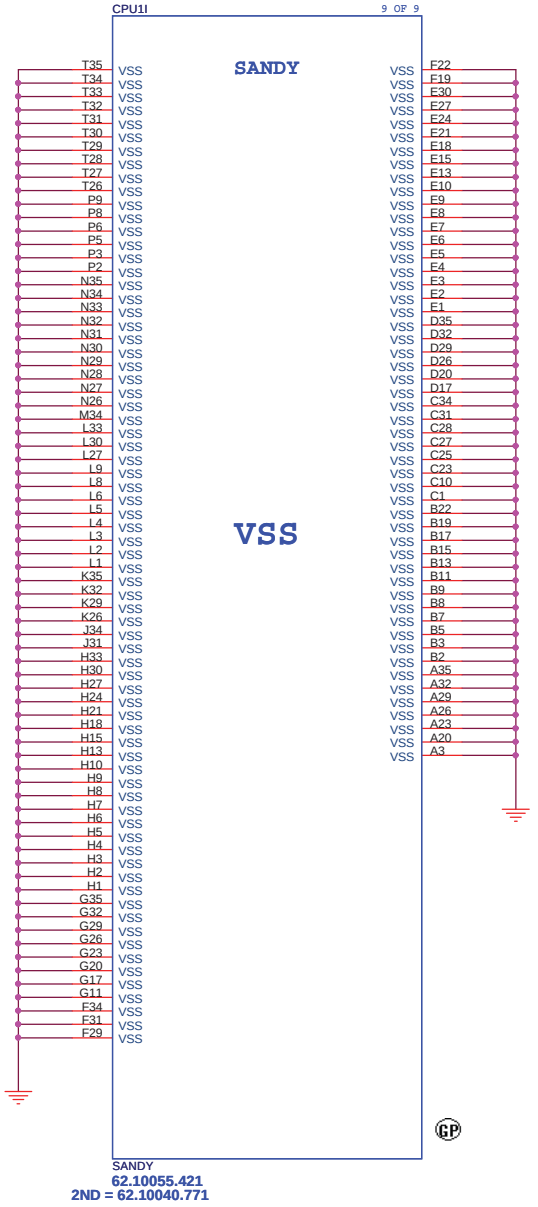
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (VCC_GFXCORE)		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 9 of 103	

SSID = CPU

http://hobi-elektronika.net





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 10 of 103

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 11 of 103

(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 12 of 103

(Blanking)

<Core Design>

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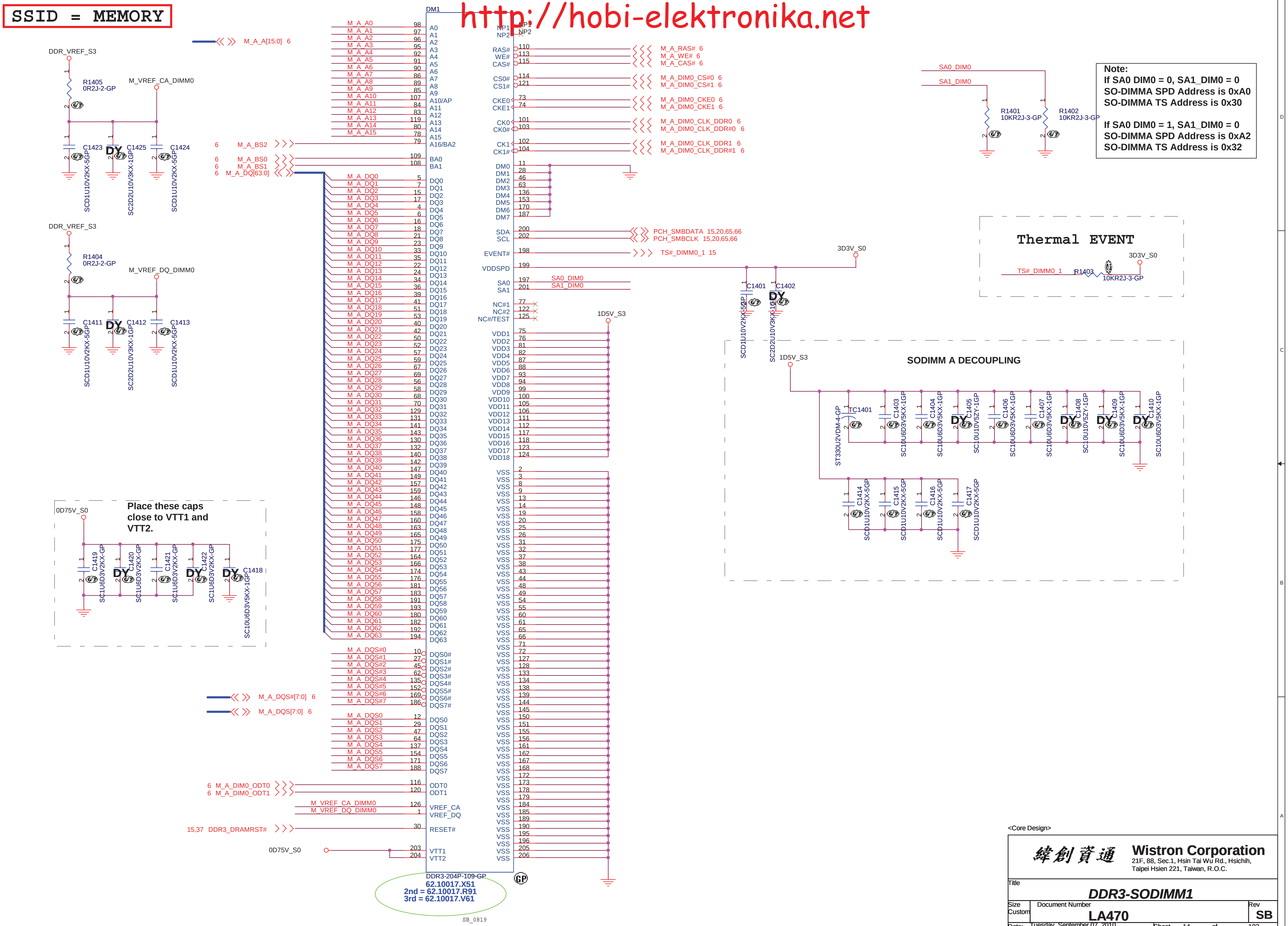
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 13 of 103

SSID = MEMORY


http://hobi-elektronika.net
DM1
DDR3-204P-109-GP
62.10017.X51
2nd = 62.10017.R91
3rd = 62.10017.V61
SB_0819
M_A_A[15:0] 6
M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15
6 M_A_BS2 79 A16/BA2
6 M_A_BS0 109 BA0
6 M_A_BS1 108 BA1
6 M_A_DQ[63:0]
M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 15 DQ2
M_A_DQ3 17 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 16 DQ6
M_A_DQ7 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ10 33 DQ10
M_A_DQ11 35 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 24 DQ13
M_A_DQ14 34 DQ14
M_A_DQ15 36 DQ15
M_A_DQ16 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ18 51 DQ18
M_A_DQ19 53 DQ19
M_A_DQ20 40 DQ20
M_A_DQ21 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ24 57 DQ24
M_A_DQ25 59 DQ25
M_A_DQ26 67 DQ26
M_A_DQ27 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ29 58 DQ29
M_A_DQ30 68 DQ30
M_A_DQ31 70 DQ31
M_A_DQ32 129 DQ32
M_A_DQ33 131 DQ33
M_A_DQ34 141 DQ34
M_A_DQ35 143 DQ35
M_A_DQ36 130 DQ36
M_A_DQ37 132 DQ37
M_A_DQ38 140 DQ38
M_A_DQ39 142 DQ39
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M_A_DQ43 159 DQ43
M_A_DQ44 146 DQ44
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M_A_DQ46 158 DQ46
M_A_DQ47 160 DQ47
M_A_DQ48 163 DQ48
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M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63
M_A_DQS#0 10 DQS0#
M_A_DQS#1 27 DQS1#
M_A_DQS#2 45 DQS2#
M_A_DQS#3 62 DQS3#
M_A_DQS#4 135 DQS4#
M_A_DQS#5 152 DQS5#
M_A_DQS#6 169 DQS6#
M_A_DQS#7 186 DQS7#
M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6
M_A_DQS0 12 DQS0
M_A_DQS1 29 DQS1
M_A_DQS2 47 DQS2
M_A_DQS3 64 DQS3
M_A_DQS4 137 DQS4
M_A_DQS5 154 DQS5
M_A_DQS6 171 DQS6
M_A_DQS7 188 DQS7
6 M_A_DIM0_ODT0 116 ODT0
6 M_A_DIM0_ODT1 120 ODT1
M_VREF_CA_DIMM0 126 VREF_CA
M_VREF_DQ_DIMM0 1 VREF_DQ
15,37 DDR3_DRAMRST# 30 RESET#
0D75V_S0 203 VTT1 204 VTT2
NP1 NP2
RAS# 110 M_A_RAS# 6
WE# 113 M_A_WE# 6
CAS# 115 M_A_CAS# 6
CS0# 114 M_A_DIM0_CS#0 6
CS1# 121 M_A_DIM0_CS#1 6
CKE0 73 M_A_DIM0_CKE0 6
CKE1 74 M_A_DIM0_CKE1 6
CK0 101 M_A_DIM0_CLK_DDR0 6
CK0# 103 M_A_DIM0_CLK_DDR#0 6
CK1 102 M_A_DIM0_CLK_DDR1 6
CK1# 104 M_A_DIM0_CLK_DDR#1 6
DM0 11 DM1 28 DM2 46 DM3 63 DM4 136 DM5 153 DM6 170 DM7 187
SDA 200 PCH_SMBDATA 15,20,65,66
SCL 202 PCH_SMBCLK 15,20,65,66
EVENT# 198 TS#_DIMM0_1 15
VDDSPD 199 3D3V_S0
SA0 197 SA0_DIM0
SA1 201 SA1_DIM0
NC#1 77 NC#2 122 NC#/TEST 125
1D5V_S3
VDD1 75 VDD2 76 VDD3 81 VDD4 82 VDD5 87 VDD6 88 VDD7 93 VDD8 94 VDD9 99 VDD10 100 VDD11 105 VDD12 106 VDD13 111 VDD14 112 VDD15 117 VDD16 118 VDD17 123 VDD18 124
VSS 2 3 8 9 13 14 19 20 25 26 31 32 37 38 43 44 48 49 54 55 60 61 65 66 71 72 127 128 133 134 138 139 144 145 150 151 155 156 161 162 167 168 172 173 178 179 184 185 189 190 195 196 205 206
DDR_VREF_S3
R1405 0R2J-2-GP
M_VREF_CA_DIMM0
C1423 SCD1U10V2KX-5GP
C1425 SC2D2U10V3KX-1GP DY
C1424 SCD1U10V2KX-5GP
DDR_VREF_S3
R1404 0R2J-2-GP
M_VREF_DQ_DIMM0
C1411 SCD1U10V2KX-5GP
C1412 SC2D2U10V3KX-1GP DY
C1413 SCD1U10V2KX-5GP
0D75V_S0
Place these caps close to VTT1 and VTT2.
C1419 SC1U6D3V2KX-GP
C1420 SC1U6D3V2KX-GP DY
C1421 SC1U6D3V2KX-GP
C1422 SC1U6D3V2KX-GP DY
C1418 SC10U6D3V5KX-1GP DY
C1401 SCD1U10V2KX-5GP
C1402 SC2D2U10V3KX-1GP DY
SA0_DIM0
SA1_DIM0
R1401 10KR2J-3-GP
R1402 10KR2J-3-GP
Thermal EVENT
3D3V_S0
TS#_DIMM0_1
R1403 10KR2J-3-GP
SODIMM A DECOUPLING
1D5V_S3
TC1401 ST330U2VDM-4-GP
C1403 SC10U6D3V5KX-1GP
C1404 SC10U6D3V5KX-1GP
C1405 SC10U10V5ZY-1GP DY
C1406 SC10U6D3V5KX-1GP
C1407 SC10U6D3V5KX-1GP
C1408 SC10U10V5ZY-1GP DY
C1409 SC10U6D3V5KX-1GP DY
C1410 SC10U6D3V5KX-1GP DY
C1414 SCD1U10V2KX-5GP
C1415 SCD1U10V2KX-5GP
C1416 SCD1U10V2KX-5GP
C1417 SCD1U10V2KX-5GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR3-SODIMM1	
Size: Custom	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 14 of 103	

SSID = MEMORY

DM2

M_B_A[15:0] 6

M_B_BS2 6

M_B_BS0 6
M_B_BS1 6
M_B_DQ[63:0] 6

M_VREF_CA_DIMM0

C1523 SCD1U10V2KX-5GP
C1524 SC2D2U10V3KX-1GP
C1522 SCD1U10V2KX-5GP

Place these caps close to VTT1 and VTT2.

0D75V_S0

C1518 SC1U6D3V2KX-GP
C1519 SC1U6D3V2KX-GP
C1520 SC1U6D3V2KX-GP
C1521 SC1U6D3V2KX-GP

M_B_DQS#[7:0] 6

M_B_DQS[7:0] 6

6 M_B_DIM0_ODT0
6 M_B_DIM0_ODT1

M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0

14,37 DDR3_DRAMRST#

0D75V_S0

RAS# M_B_RAS# 6
WE# M_B_WE# 6
CAS# M_B_CAS# 6

CS0# M_B_DIM0_CS#0 6
CS1# M_B_DIM0_CS#1 6

CKE0 M_B_DIM0_CKE0 6
CKE1 M_B_DIM0_CKE1 6

CK0 M_B_DIM0_CLK_DDR0 6
CK0# M_B_DIM0_CLK_DDR#0 6

CK1 M_B_DIM0_CLK_DDR1 6
CK1# M_B_DIM0_CLK_DDR#1 6

SDA PCH_SMBDATA 14,20,65,66
SCL PCH_SMBCLK 14,20,65,66

EVENT# TS#_DIMM0_1 14

SA0 SA0_DIM1
SA1 SA1_DIM1

1D5V_S3

3D3V_S0

C1501 SCD1U10V2KX-5GP
C1502 SC2D2U10V3KX-1GP

3D3V_S0

R1501 10KR2J-3-GP
R1502 10KR2J-3-GP

SA1_DIM1
SA0_DIM1

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

1D5V_S3

SODIMM B DECOUPLING

C1503 SC10U10V5ZY-1GP
C1504 SC10U10V5ZY-1GP
C1505 SC10U6D3V5KX-1GP
C1506 SC10U6D3V5KX-1GP
C1507 SC10U6D3V5KX-1GP
C1508 SC10U10V5ZY-1GP
C1509 SC10U6D3V5KX-1GP
C1510 SC10U6D3V5KX-1GP

C1511 SCD1U10V2KX-5GP
C1512 SCD1U10V2KX-5GP
C1513 SCD1U10V2KX-5GP
C1514 SCD1U10V2KX-5GP

H = 8mm

DDR3-204P-108-GP
62.10017.X41
2nd = 62.10017.M51
3rd = 62.10017.V51

SB_0819

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 15 of 103

(Blanking)

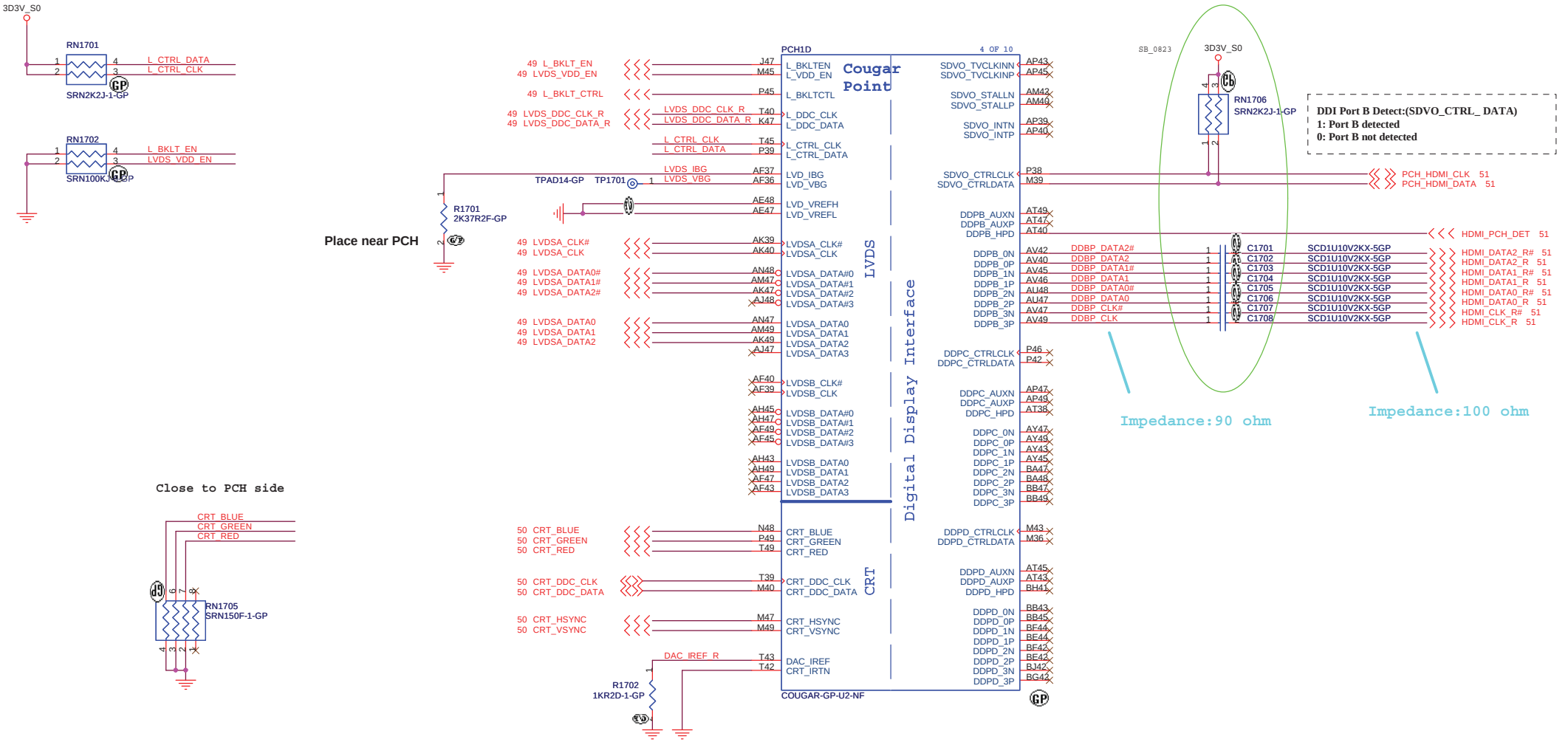
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
A4	LA470	SB

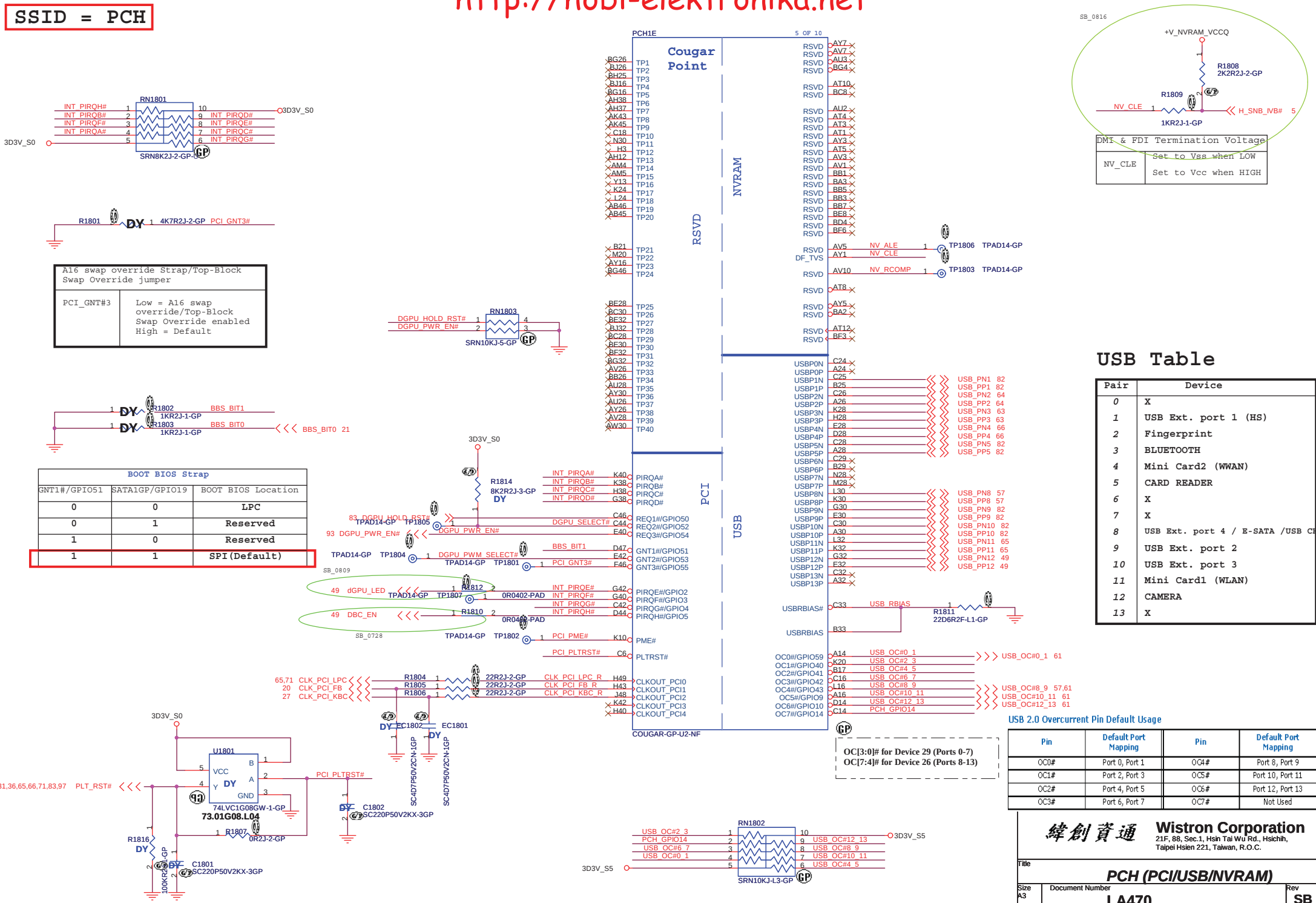
Date: Tuesday, September 07, 2010 Sheet 16 of 103



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (LVDS/CRT/DDI)		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 17 of 103	

SSID = PCH



USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGE
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	X

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI/USB/NVRAM)**

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 18 of 103

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

4 DMI_RXN[3:0]
4 DMI_RXP[3:0]
4 DMI_TXN[3:0]
4 DMI_TXP[3:0]

FDI_TXN[7:0] 4
FDI_TXP[7:0] 4

PCH1C — 3 OF 10

Cougar Point

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

DMI_ZCOMP — R1901 49D9R2F-GP — 1D05V_VTT
DMI_IRCOMP — R1902 750R2F-GP — RBIAS_CPY

System Power Management

SUSACK# — SUS_PWR_ACK — R1903 0R0402-PAD — SUSACK# C12
SYS_RESET# — 5,11 XDP_DBRESET# — R1922 0R2J-2-GP — SYS_RESET# K3
SYS_PWROK — 11,36,37 SYS_PWROK — R1905 10KR2J-3-GP — R1923 0R2J-2-GP — SYS_PWROK P12
PWROK — 27,36 S0_PWR_GOOD — R1924 0R2J-2-GP — R1906 0R2J-2-GP — PWROK L22
APWROK — 36,45,46,47 RUNPWROK — R1907 0R2J-2-GP — MEPWROK — APWROK L10
DRAMPWROK — 5,37 PM_DRAM_PWRGD — DRAMPWROK B13
RSMRST# — PM_RSMRST# — RSMRST# C21
SUSWARN#/SUSPWRDNACK/GPIO30 — 27 SUS_PWR_ACK — SUSWARN#/SUSPWRDNACK/GPIO30 K16
PWRBTN# — 11,27,97 PM_PWRBTN# — PWRBTN# E20
ACPRESENT/GPIO31 — 27 AC_PRESENT — ACPRESENT/GPIO31 H20
BATLOW#/GPIO72 — BATLOW# — BATLOW#/GPIO72 E10
RI# — PM_RI# — RI# A10

DY: R1926 10KR2J-3-GP SYS_PWROK; R1904 100KR2J-1-GP PWROK

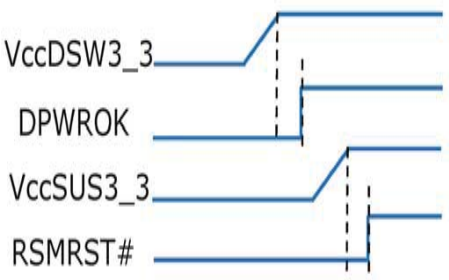
DSWVRMEN — A18 DSWODVREN
DPWROK — F22 PCH_DPWROK — R1910 0R2J-2-GP PM_RSMRST# — R1911 10KR2J-3-GP — RTC_AUX_S5
WAKE# — B9 — PCIE_WAKE# 31,65,66
CLKRUN#/GPIO32 — N3 — PM_CLKRUN# 27
SUS_STAT#/GPIO61 — G8 PM_SUS_STAT# — TP1901 TPAD14-GP
SUSCLK/GPIO62 — N14 SUS_CLK — R1913 0R2J-2-GP — PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63 — D10 PM_SLP_S5# — TP1902 TPAD14-GP
SLP_S4# — H4 SLP_S4#_R — R1914 0R2J-2-GP — PM_SLP_S4# 27,46
SLP_S3# — F4 SLP_S3#_R — R1915 0R2J-2-GP — PM_SLP_S3# 27,36,37,47,92
SLP_A# — G10 PM_SLP_A# — TP1903 TPAD14-GP
SLP_SUS# — G16 PM_SLP_SUS# — TP1904 TPAD14-GP
PMSYNCH — AP14 H_PM_SYNC — H_PM_SYNC 5
SLP_LAN#/GPIO29 — K14 PM_SLP_LAN# — TP1905 TPAD14-GP

SLP_S3#_R — TP1906 TPAD14-GP

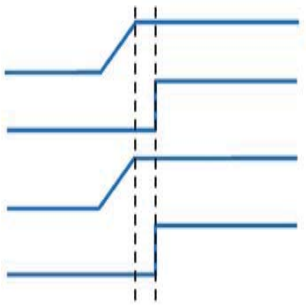
GP

COUGAR-GP-U2-NF

Deep S4/S5 Supported



Deep S4/S5 Not Supported



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5 — R1917 330KR2J-L1-GP — DSWODVREN — R1918 DY 330KR2J-L1-GP

3D3V_S0 — PM_CLKRUN# — R1919 8K2R2J-3-GP

3D3V_S5 — RN1901 SRN10KJ-6-GP: BATLOW#, PM_RI#, AC_PRESENT, SUS_PWR_ACK
R1921 10KR2J-3-GP PCIE_WAKE#
R1922 10KR2J-3-GP PM_PWRBTN#
DY R1920 10KR2J-3-GP PM_SLP_LAN#

This signal has an internal pull-up resistor

R1908 10KR2J-3-GP PM_RSMRST#

3D3V_AUX_S5 — R1909 100KR2J-1-GP — R1916 10KR2J-3-GP — Q1901 2N7002KDW-GP
PM_RSMRST# — R1912 1KR2J-1-GP — RSMRST#_KBC 27
3V_5V_POK # — 3V_5V_POK 41

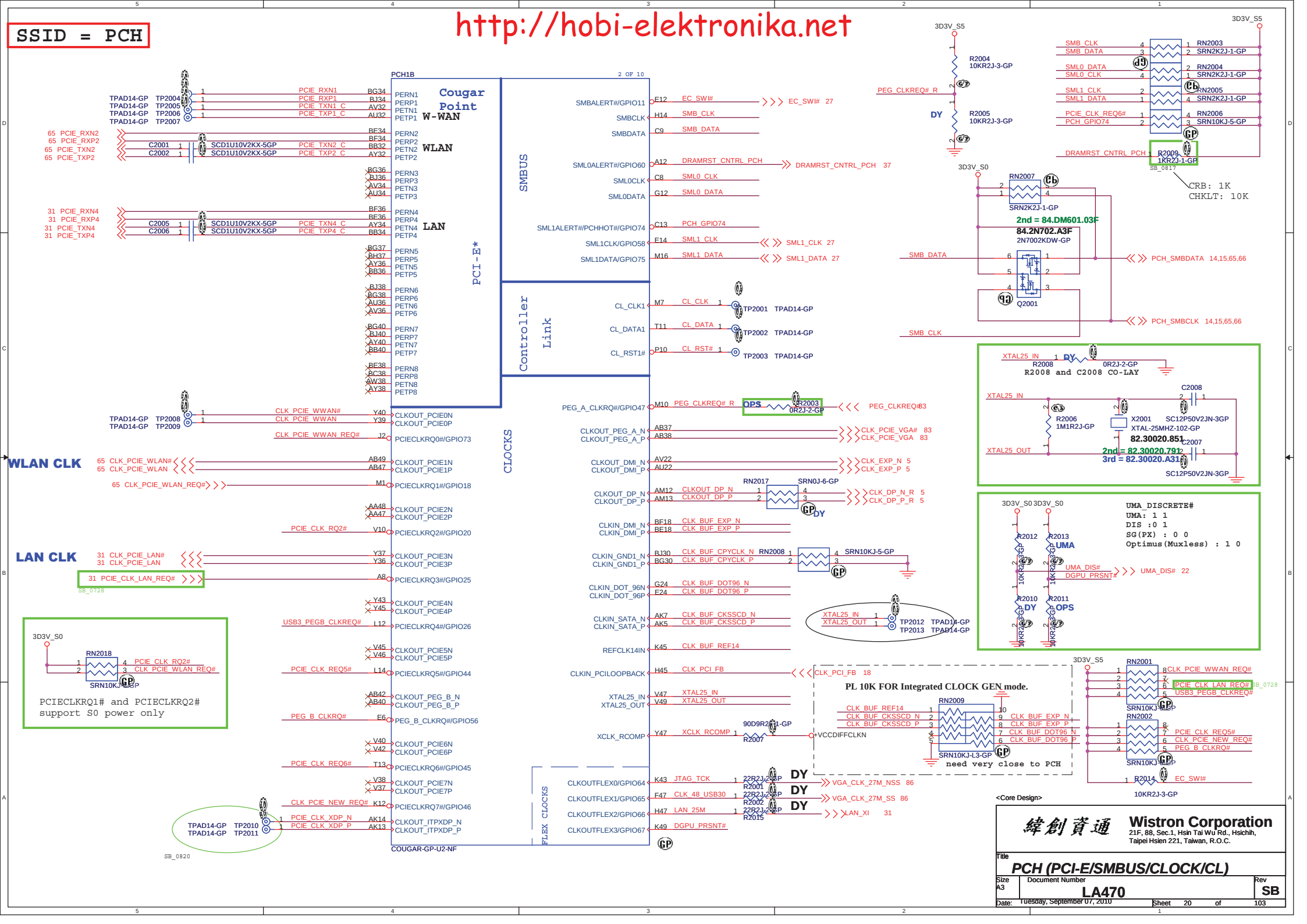
84.2N702.A3F
2nd = 84.DM601.03F

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**
Size: A3 | Document Number: **LA470** | Rev: **SB**
Date: Tuesday, September 07, 2010 | Sheet 19 of 103

SSID = PCH



SSID = PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

PCH1A — Cougar Point — 1 OF 10

RTC_X1 A20 · RTC_X2 C20 · RTC_RST# D20 · SRTC_RST# G22 · SM_INTRUDER# K22 · PCH_INTVRMEN C17 · HDA_BITCLK N34 · HDA_SYNC L34 · SPKR T10 · HDA_RST# K34 · HDA_SDIN0 E34 · HDA_SDIN1 G34 · HDA_SDIN2 C34 · HDA_SDIN3 A34 · HDA_SDO A36 · HDA_DOCK_EN#/GPIO33 C36 · HDA_DOCK_RST#/GPIO13 N32 · JTAG_TCK J3 · JTAG_TMS H7 · JTAG_TDI K5 · JTAG_TDO H1 · SPI_CLK T3 · SPI_CS0# Y14 · SPI_CS1# T1 · SPI_MOSI V4 · SPI_MISO U3

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0–3, HDA_SDO, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

COUGAR-GP-U2-NF

LPC: FWH0/LAD0 C38 LPC_AD0 · FWH1/LAD1 A38 LPC_AD1 · FWH2/LAD2 B37 LPC_AD2 · FWH3/LAD3 C37 LPC_AD3 · FWH4/LFRAME# D36 → LPC_FRAME# 27,65,71 · LDRQ0# E36 · LDRQ1#/GPIO23 K36 → APS_LED_R 68 · SERIRQ V5 → INT_SERIRQ 27

SATA 6G:
SATA0RXN AM3 · SATA0RXP AM1 · SATA0TXN AP7 SATA_TXN0_C C2105 → SCD01U16V2KX-3GP · SATA0TXP AP5 SATA_TXP0_C C2106 → SCD01U16V2KX-3GP → SATA_RXN0_C 56 · SATA_RXP0_C 56 · SATA_TXN0 56 · SATA_TXP0 56 — HDD1
SATA1RXN AM10 · SATA1RXP AM8 · SATA1TXN AP11 SATA_TXN1_C C2112 → SCD01U16V2KX-3GP · SATA1TXP AP10 SATA_TXP1_C C2111 → SCD01U16V2KX-3GP → SATA_RXN1_C 66 · SATA_RXP1_C 66 · SATA_TXN1 66 · SATA_TXP1 66 — SATA SSD
SATA2RXN AD7 · SATA2RXP AD5 · SATA2TXN AH5 · SATA2TXP AH4
SATA3RXN AB8 · SATA3RXP AB10 · SATA3TXN AF3 · SATA3TXP AF1
SATA4RXN Y7 · SATA4RXP Y5 · SATA4TXN AD3 SATA_TXN4_C C2109 → SCD01U16V2KX-3GP · SATA4TXP AD1 SATA_TXP4_C C2110 → SCD01U16V2KX-3GP → SATA_RXN4_C 56 · SATA_RXP4_C 56 · SATA_TXN4 56 · SATA_TXP4 56 — ODD
SATA5RXN Y3 · SATA5RXP Y1 · SATA5TXN AB3 SATA_TXN5_C C2107 → SCD01U16V2KX-3GP · SATA5TXP AB1 SATA_TXP5_C C2108 → SCD01U16V2KX-3GP → SATA_RXN5_C 57 · SATA_RXP5_C 57 · SATA_TXN5 57 · SATA_TXP5 57 — ESATA
SATAICOMPO Y11 · SATAICOMPI Y10 SATA_COMP R2112 37D4R2F-GP → 1D05V_VTT
SATA3RCOMPO AB12 · SATA3COMPI AB13 SATA3_COMP R2113 49D9R2F-GP → 1D05V_VTT
SATA3RBIAS AH1 RBIAS_SATA3 R2114 806R2F-GP
SATALED# P3 → SATA_LED# 68
SATA0GP/GPIO21 V14 SATA_DET#0
SATA1GP/GPIO19 P1 BBS_BIT0 → BBS_BIT0 18

Move Cap close to Device or Connector.

RTC_AUX_S5 · RN2104 SRN20KJ-GP-U · C2103 SC1U6D3V2KX-GP · C2104 SC1U6D3V2KX-GP · G2101 CAP-OPEN · R2104 1M1R2J-GP · R2105 330KR2F-L-GP

X2101 X-32D768KHZ-34GPU · C2101 SC12P50V2JN-3GP · C2102 SC12P50V2JN-3GP · R2101 10MR2J-L-GP

SHR_V1.4 SB_0809
29 HDA_CODEC_SYNC · 29 HDA_CODEC_SDOUT · R2122 33R2J-2-GP HDA_SYNC · R2123 33R2J-2-GP HDA_SDOUT
29 HDA_CODEC_RST# · 29 HDA_CODEC_BITCLK · RN2102 SRN33J-5-GP-U HDA_RST# · HDA_BITCLK

+3VS_+1.5VS_HDA_IO · DY · R2102 1KR2J-1-GP HDA_SDOUT

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

3D3V_S0 · DY · R2106 1KR2J-1-GP HDA_SPKR

NO REBOOT STRAP

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

27 ME_UNLOCK · R2107 1KR2J-1-GP HDA_SDOUT · TPAD14-GP TP2105 PCH_GPIO33

TPAD14-GP TP2101 PCH_JTAG_TCK_BUF · TP2102 PCH_JTAG_TMS · TP2103 PCH_JTAG_TDI · TP2104 PCH_JTAG_TDO

27,60 SPI_CLK_R · R2108 0R2J-2-GP PCH_SPI_CLK
27,60 SPI_CS0#_R · R2109 0R2J-2-GP PCH_SPI_CS0#
27,60 SPI_SI_R · R2110 0R2J-2-GP PCH_SPI_SI
27,60 SPI_SO_R

+3VS_+1.5VS_HDA_IO · R2103 1KR2J-1-GP HDA_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

3D3V_S0 · RN2103 SRN10KJ-GP · SATA_LED# · INT_SERIRQ · SATA_DET#0

SB_0817
PCH_JTAG_TCK_BUF · R2121 4K7R2J-2-GP
PCH_GPIO33 · R2125 1KR2J-1-GP DY

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: A3 · Document Number: LA470 · Rev: SB
Date: Tuesday, September 07, 2010 · Sheet 21 of 103

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

Note:
For PCH debug with XDP, need to NO STUFF R2218

3D3V_S0 — R2202 1 — 200KR2F-L-GP — SATA_ODD_PRSNT#

20100625 V1.2

3D3V_S0 — RN2203 — H_A20GATE, H_RCIN# — SRN10KJ-5-GP

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

3D3V_S0 — R2224 10KR2J-3-GP — PCH_TEMP_ALERT#
PCH_GPIO27 — DY R2223 10KR2J-3-GP
DY R2225 10KR2J-3-GP

3D3V_S0 — RN2201 — PSW_CLR#, DGPU_HPD_INTR#, EC_SMI# — SRN10KJ-8-GP

RN2202 — MFG_MODE, S_GPIO, EC_SCI#, PCH_GPIO22 — SRN10KJ-8-GP
PCH_GPIO48 — R2227 10KR2J-3-GP

3D3V_S5 — RN2205 — PCH_GPIO12, USB3_PWR_ON — SRN10KJ-8-GP

PCH_GPIO15 — R2201 1KR2J-1-GP
PCH_GPIO24 — R2221 10KR2J-3-GP
20100625 V1.2
PLL_ODVR_EN — R2226 10KR2J-3-GP

NC_FP_DET# — R2220 10KR2J-3-GP
20100705

PCH1F — 6 OF 10 — Cougar Point

S_GPIO — R2218 100R2J-2-GP — GPIO0 T7
EC_SMI# A42
DGPU_HPD_INTR# H36
27 EC_SCI# — EC_SCI# E38
ICC_EN# C10
PCH_GPIO12 C4
PCH_GPIO15 G2
56 SATA_ODD_PRSNT# — R2213 0R2J-2-GP — PCH_GPIO16 U2
92,93 DGPU_PWROK — DGPU_PWROK D40
49 Color_Engine# — R2228 0R2J-2-GP — PCH_GPIO22 T5
TPAD14-GP TP2202 — PCH_GPIO24 E8
PCH_GPIO27 E16
PLL_ODVR_EN P8
PSW_CLR# K1
TPAD14-GP TP2204 — NC_FP_DET# K4
DMI_OVRVLTG V8
FDI_OVRVLTG M5
MFG_MODE N2
GFX_CRB_DET M3
TP2209 — PCH_GPIO48 V13
PCH_TEMP_ALERT# V3
USB3_PWR_ON D6
TPAD14-GP TP2205 A4
TPAD14-GP TP2206 A46
A5
A6
B3
B47
BD1
BD49
TPAD14-GP TP2210 BE1
TPAD14-GP TP2211 BE49
TPAD14-GP TP2212 BF1
BF49

BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24/MEM_LED
GPIO27
GPIO28
STP_PCI#/GPIO34
GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57

GPIO | CPU/MISC

TACH4/GPIO68 — C40 — SATA_ODD_PWRGT 56
TACH5/GPIO69 — B41 — UMA_DIS# — UMA_DIS# 20
TACH6/GPIO70 — C41 — VRAM_SIZE1
TACH7/GPIO71 — A40 — VRAM_SIZE2

A20GATE — P4 — H_A20GATE 27
PECI — AU16 — H_PECI_R — DY R2203 0R2J-2-GP — H_PECI 5,27
RCIN# — P5 — H_RCIN# 27
PROCPWRGD — AY11 — H_CPUPWRGD 5,11,36,97
THRMTRIP# — AY10 — PCH_THERMTRIP_R — R2204 390R2J-1-GP — H_THERMTRIP# 5,36
INIT3_3V# — T14 — INIT3_3V# — TP2201 TPAD14-GP

TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10 — TS_VSS — R2219 0R0402-PAD
NC_1 P37

NCTF_VSS#BG2 BG2
NCTF_VSS#BG48 BG48
NCTF_VSS#BH3 BH3
NCTF_VSS#BH47 BH47
NCTF_VSS#BJ4 BJ4
NCTF_VSS#BJ44 BJ44
NCTF_VSS#BJ45 BJ45
NCTF_VSS#BJ46 BJ46
NCTF_VSS#BJ5 BJ5
NCTF_VSS#BJ6 BJ6
NCTF_VSS#C2 C2
NCTF_VSS#C48 C48
NCTF_VSS#D1 D1
NCTF_VSS#D49 D49
NCTF_VSS#E1 E1
NCTF_VSS#E49 E49
NCTF_VSS#F1 F1
NCTF_VSS#F49 F49

NCTF_VSS#A4
NCTF_VSS#A44
NCTF_VSS#A45
NCTF_VSS#A46
NCTF_VSS#A5
NCTF_VSS#A6
NCTF_VSS#B3
NCTF_VSS#B47
NCTF_VSS#BD1
NCTF_VSS#BD49
NCTF_VSS#BE1
NCTF_VSS#BE49
NCTF_VSS#BF1
NCTF_VSS#BF49

NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47,BD1,BD49,BE1,BE49,BF1,BF49 BG2,BG48,BH3,BH47,BJ4,BJ44,BJ45,BJ46,BJ5,BJ6,C2,C48 D1,D49,E1,E49,F1,F49

COUGAR-GP-U2-NF

SB_0811
SHR_V1.5

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

3D3V_S0 — R2205 10KR2J-3-GP — DY — GFX_CRB_DET — R2206 100KR2J-1-GP

PCH_THERMTRIP_R — R2222 — 1D05V_VTT — DY 56R2J-4-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

3D3V_S0 — R2207 10KR2J-3-GP — DY — FDI_OVRVLTG
TP2207 TPAD14-GP
TP2208 TPAD14-GP — R2208 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

3D3V_S0 — R2209 10KR2J-3-GP — DY — DMI_OVRVLTG
R2210 10KR2J-3-GP

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

ICC_EN# — R2211 1KR2J-1-GP

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

3D3V_S0 — R2214 10KR2J-3-GP 2G — R2216 10KR2J-3-GP 1G
[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G
VRAM_SIZE1
VRAM_SIZE2
R2215 10KR2J-3-GP 1G_512M — R2217 10KR2J-3-GP 2G_512M

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN DY 1 — R2212 1KR2J-1-GP

<Core Design>

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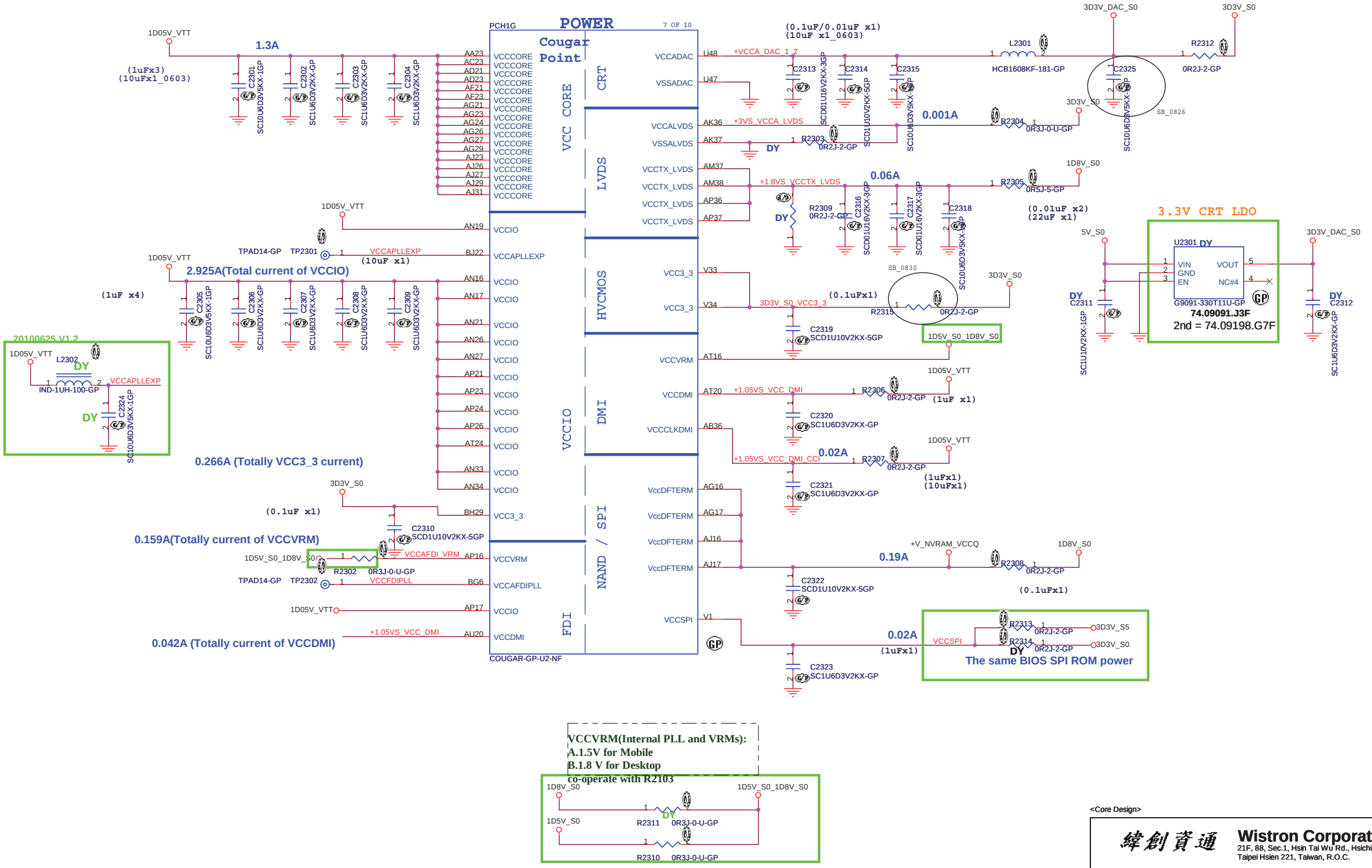
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)
Size: A3 | Document Number: LA470 | Rev: SB
Date: Tuesday, September 07, 2010 | Sheet 22 of 103

SSID = PCH 6A



<Core Design>
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 23 of 103

SSID = PCH

PCH1J

POWER

10 OF 10

Cougar Point

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.08A

0.16A (Totally current of VCCVRM)

0.055A

0.095A

6uA

0.01A

<Core Design>

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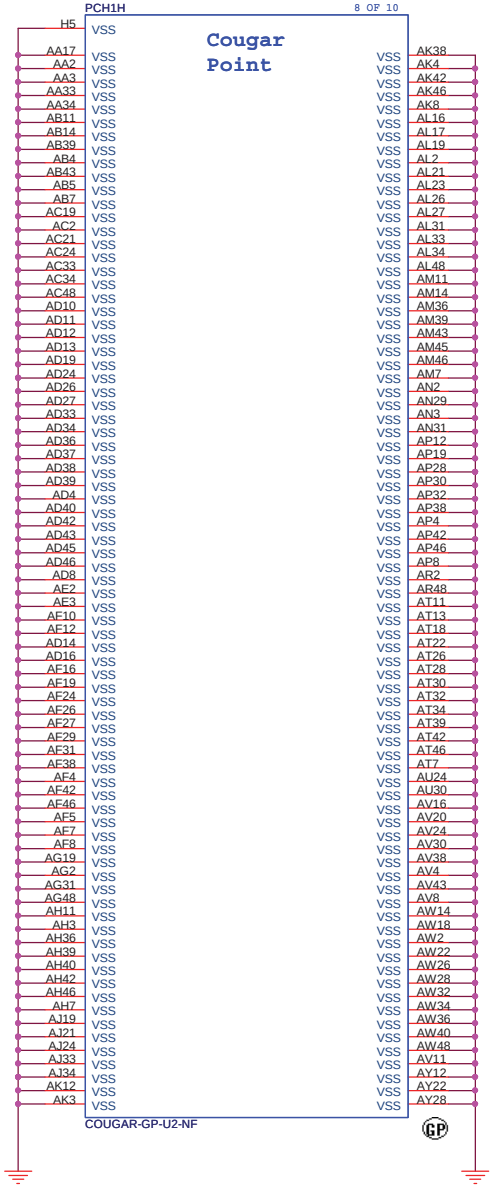
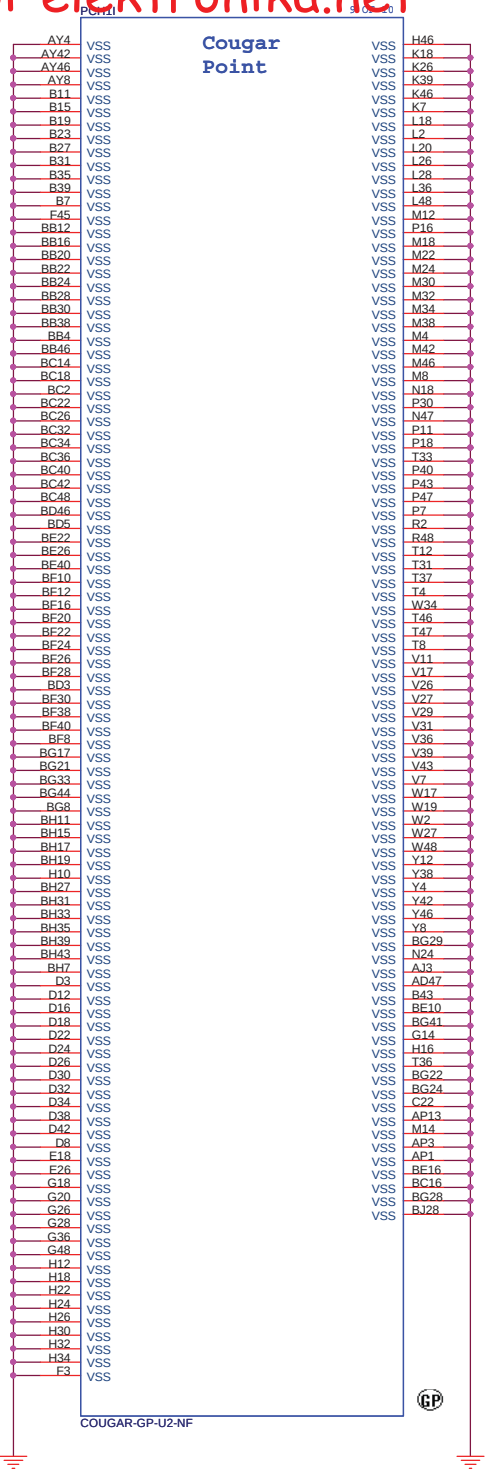
Title: PCH (POWER2)

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 24 of 103

SSID = PCH





<Core Design>

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Title: PCH (VSS)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 25 of 103

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 26 of 103

SSID = KBC

NOTE: Locate resistors R2719 and R2722 close to the NPCE791L.

NOTE: Connect GND and AGND planes via either 0R resistor or one point layout connection.

R2701 and C2716 Need very close to EC

65W_90W#
High: 65W / Low 90W

G Sensor ID:
High: ST
Low:ADI

EC GPIO standard PH/PL

Prevent BIOS data loss solution

EC_GPIO47 High Active

LILI Multi GPIO setting

Model_ID_AD (Rev1.0)	Pull-Low Register	Pull-High Register	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.48 V
.1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

MODEL_ID_AD (Rev1.0)	Pull-Low Register	Pull-High Register	Voltage
V/B 47 UMA	100.0 K	33.0 K (63.33334.1DL)	2.481 V
V/B 47 OPTIMUS	100.0 K	47.0 K (63.47334.1DL)	2.245 V

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Title: KBC Nuvoton NPCE795
Size: A1 | Document Number: LA470 | Rev: SB
Date: Monday, September 07, 2009 | Sheet 27 of 53

SSID = Thermal

Thermal sensor

Close to PCH on top side.

SA_0905 change to 390p

3
Q6
MMBT3904WT1G-GP
C183
SC390P50V2KX-GP

2
Q42
MMBT3904WT1G-GP
C434
SC390P50V2KX-GP
DY

2200p close to smsc2103 chip
REMOTE2-
REMOTE2+
C569
SC2200P50V2KX-2GP

between CPU, VGA and DIMM on bottom side

T8

1
Q9
MMBT3904WT1G-GP

2200p close to smsc2103 chip
H_THERMDA
H_THERMDC
C389
SC2200P50V2KX-2GP

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

4 WIRE PWM Fan Control circuit

Close to connector

SA_0905

5V_S0
D2801
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
DY
C39
C4D7U6D3V3KX-GP
R2801
0R3J-0-U-GP
R426
10KR2J-3-GP
SB_0819
FAN_TACH
FAN_PWM
5V_S0_FAN
FAN_PWM_C
R427
0R0402-PAD
EC2801
EC2802
SCI-KP50V2KX-1-GP
20100707_EMI
FAN1
ACES-CON4-4-GP
20.F0765.004
2nd = 20.F1808.004

3D3V_S0
R280
6K8R2J-GP
SHDN_SEL

SHDN --> 2N3904 ON External diode

3D3V_S0
R260
68R2-GP
C388
SCD1U10V2KX-4GP
2103_VDD
U31
VDD
DP1
DN1
DP2/DN3
ND2/DP3
SYS_SHDN#
ALERT#
SMCLK
SMDATA
GPIO1
GPIO2
TACH
PWM
TRIP_SET
SHDN_SEL
GND
GND
EMC2103-2-AP-GP
H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-
THERM_SYS_SHDN#
THERM_SCI#_R
SC 1203
THERM_SCI#
TP66
TPAD14-GP
R272
0R0402-PAD
27,86 SMBC_THERM
27,86 SMBD_THERM
2103_4
2103_5
TP65 TPAD14-GP
TP67 TPAD14-GP
TRIP_SET_R276
SHDN_SEL
2K05R2F-GP
T8 = 105
RN49
SRN10KJ-5-GP
3D3V_S0
D2802
CH551H-30PT-GP
FAN_TACH
FAN_PWM
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
83.R5003.C8F

pin6, ALERT# OD
pin7, SYS_SHDN# OD

AFTP2803
AFTP2802
AFTP2801
FAN_PWM_C
FAN_TACH
5V_S0_FAN
SB_0825

3D3V_AUX_S5
D2803
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.BAT54.S81
DY
27,36,86 PURE_HW_SHUTDOWN#
R2812
10KR2J-GP
C2811
SCD1U10V2KX-GP
Q2802
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
THERM_SYS_SHDN#
R2809
100KR2J-1-GP
R2810
0R2J-2-GP
R2811
0R2J-2-GP
3D3V_S0
IMVP_PWRGD 36,42
SB_0812

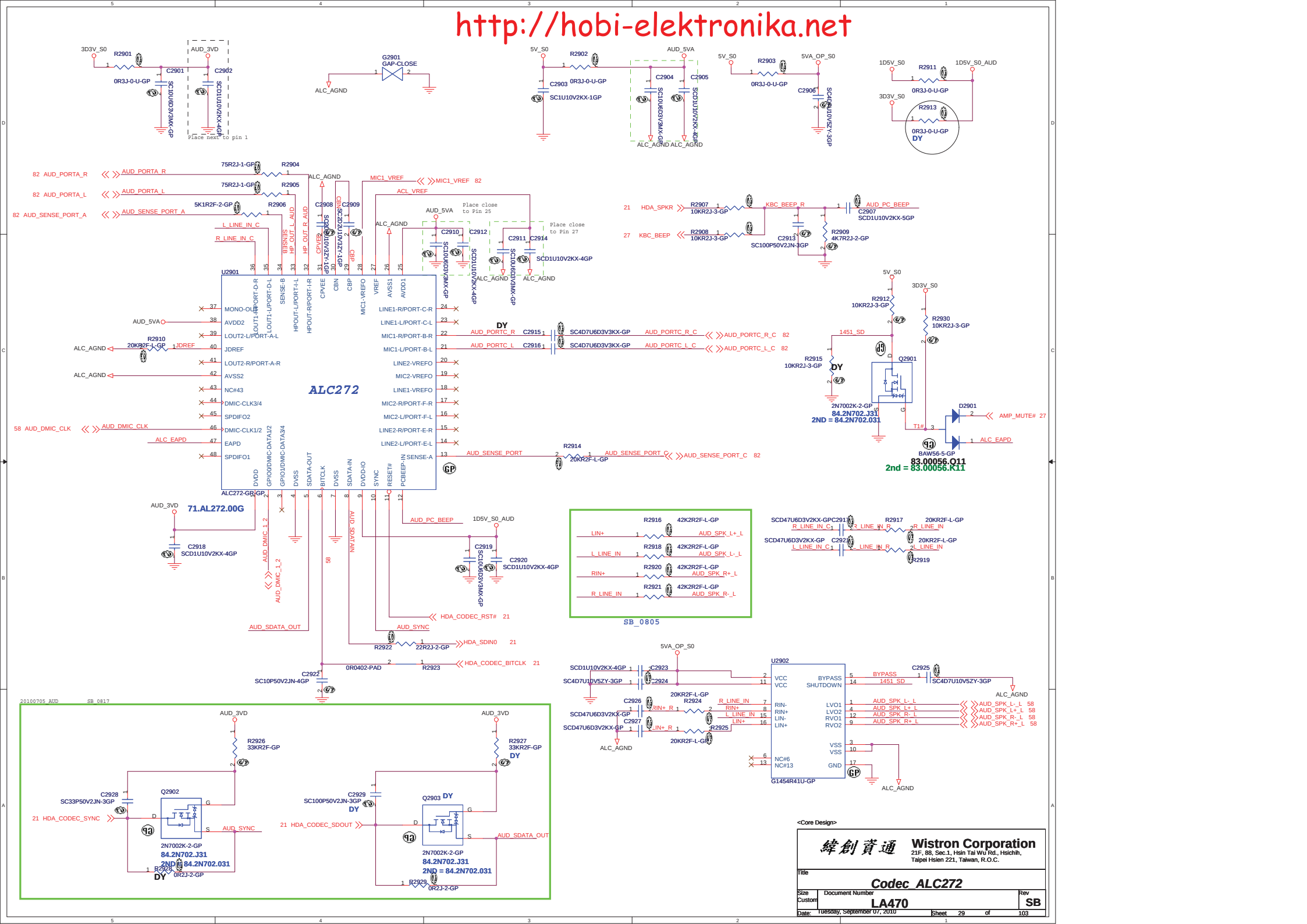
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL SENSOR SMSC EMC2103

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 28 of 103



<Core Design>

緯創資通 **Wistron Corporation**
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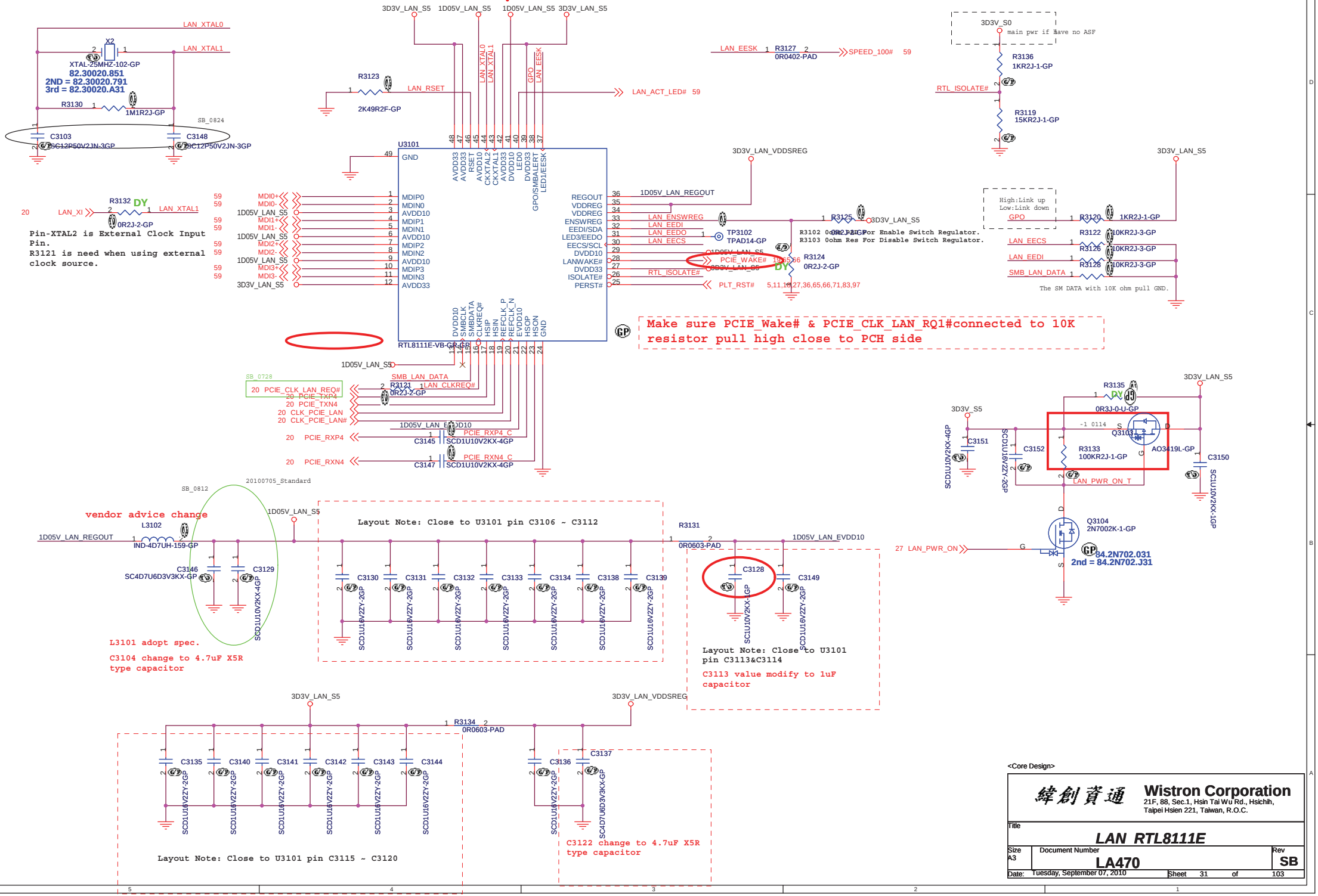
Title
Audio AMP

Size	Document Number	Rev
A4	**LA470**	**SB**

Date: Tuesday, September 07, 2010 Sheet 30 of 103

25MHz XTAL



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111E

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 31 of 103

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RTS5159 (CARD READER)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 32 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 33 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 34 of 103

<Core Design>

緯創資通 **Wistron Corporation**

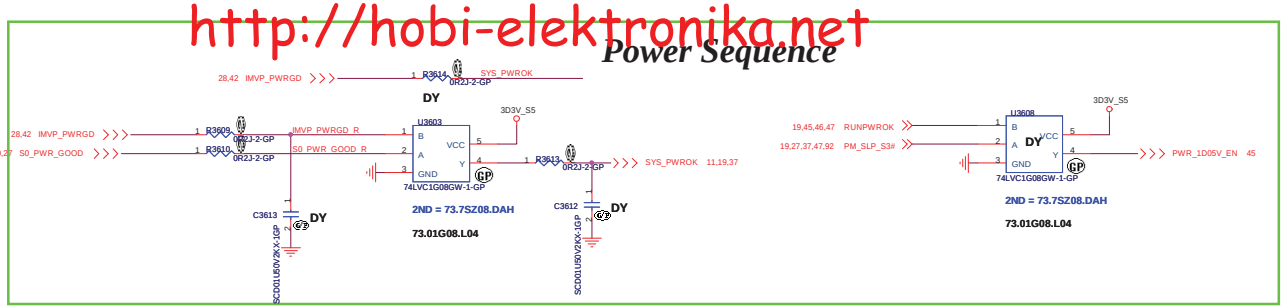
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

Size	Document Number	Rev
A3	LA470	SB

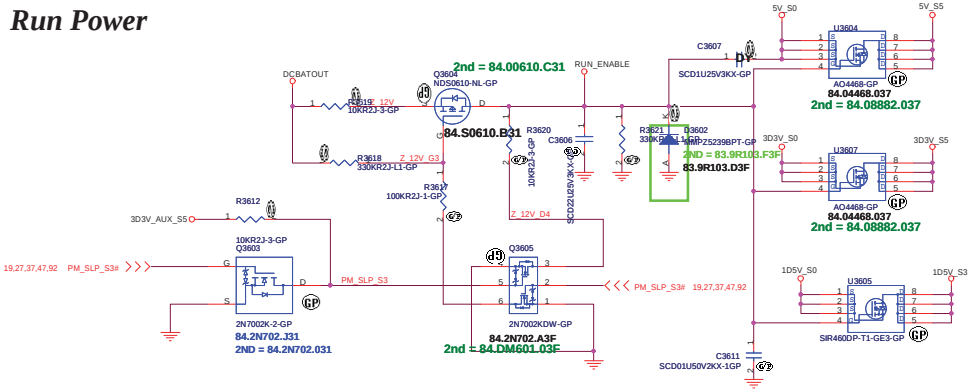
Date: Tuesday, September 07, 2010 Sheet 35 of 103

Power Sequence



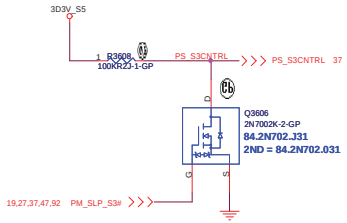
SSID = Reset.Suspend

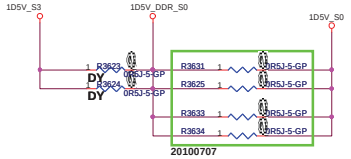
Run Power

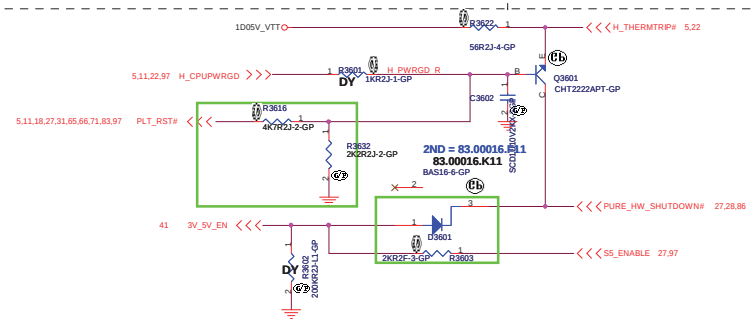


1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A







<Core Design>

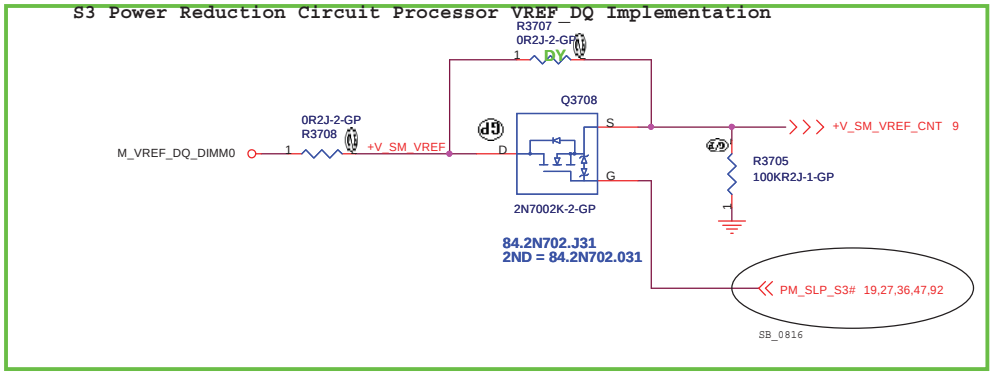
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

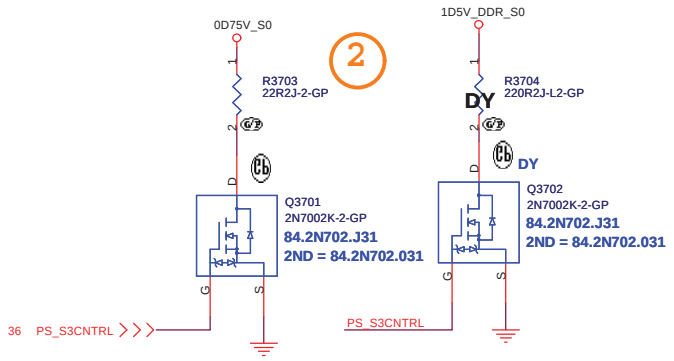
Size	Document Number	Rev
A2	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 36 of 103

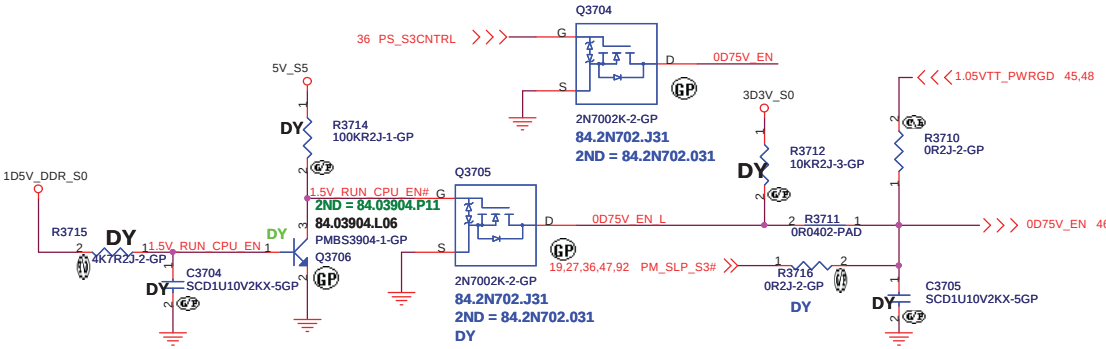
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



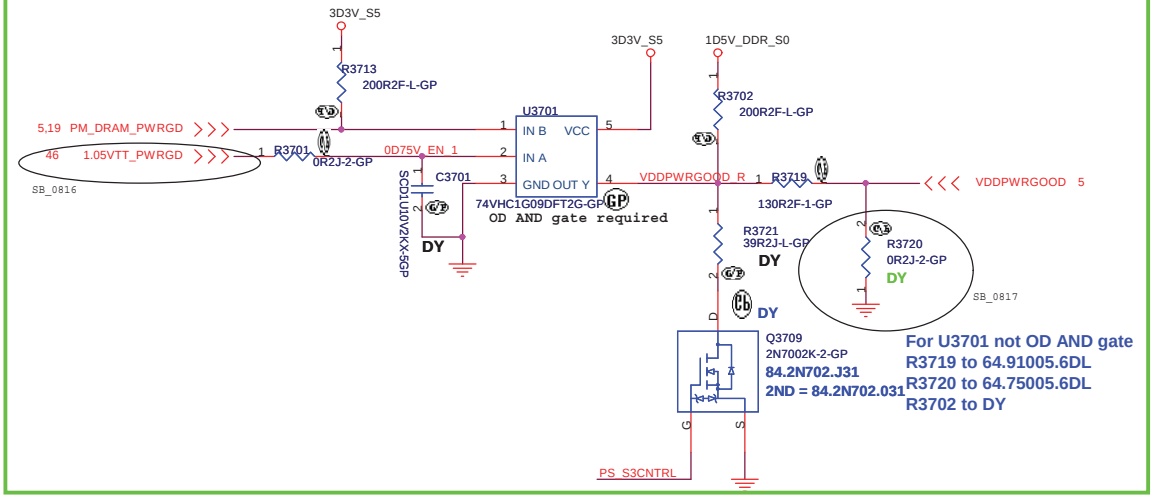
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



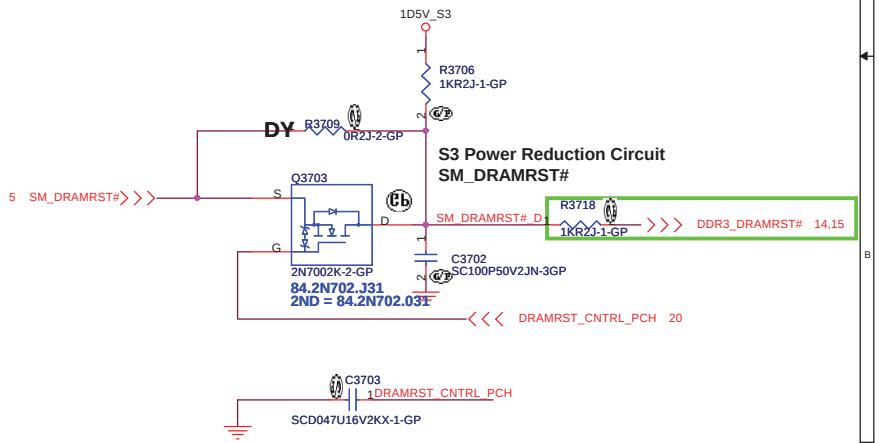
5 S3 Power Reduction X01 20091111



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

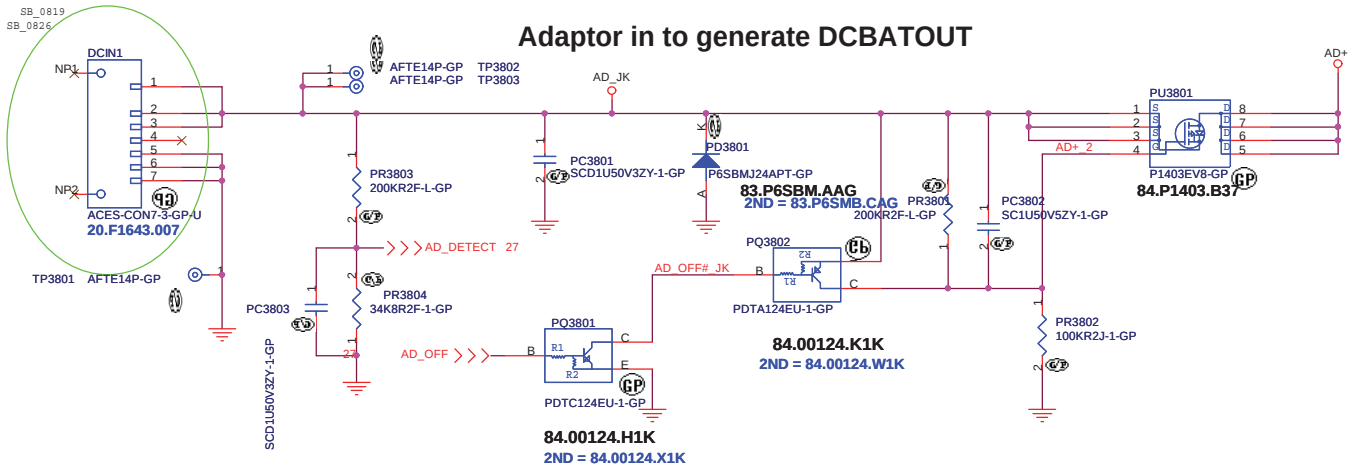


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ADAPTER		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 37 of 103	

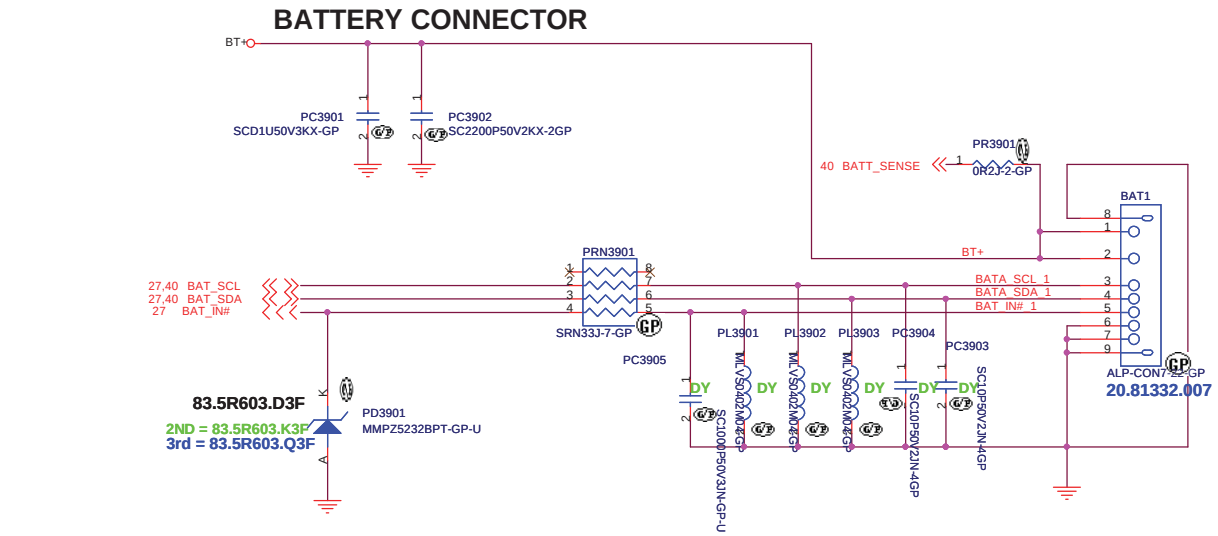


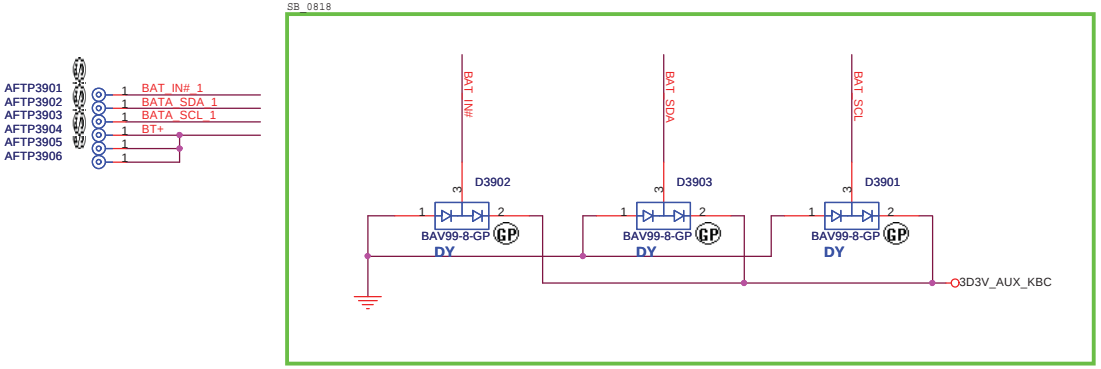
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*DCIN_JACK*	
Size	Document Number **LA470**	Rev **SB**
Date: Tuesday, September 07, 2010	Sheet 38 of 103	

BATTERY CONNECTOR





DY ???

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT_CONN

Size | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 39 of 103

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

NEAR

AD+ TO SYS

20100518 WAYNE

STOP_CHG# connects to KBC

74.24745.073

79.10712.L02

83.R0203.08F
2nd = 83.1R003.I8F

20100518 WAYNE

AC_IN to KBC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

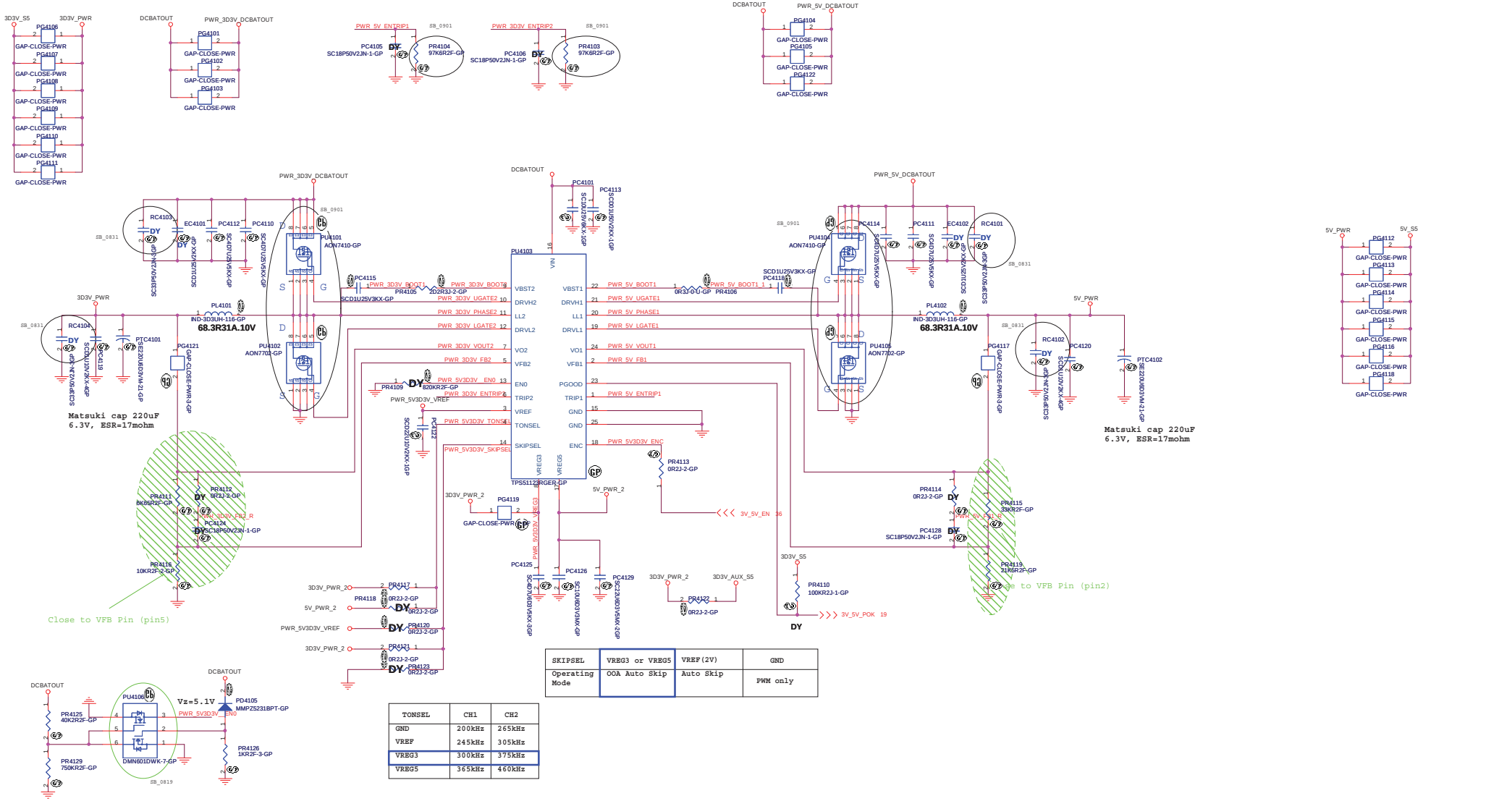
Title: Charger_BQ24745

Size: | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 40 of 103

SSID = PWR.Plane.Regulator_5v3p3v

http://hobi-elektronika.net



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

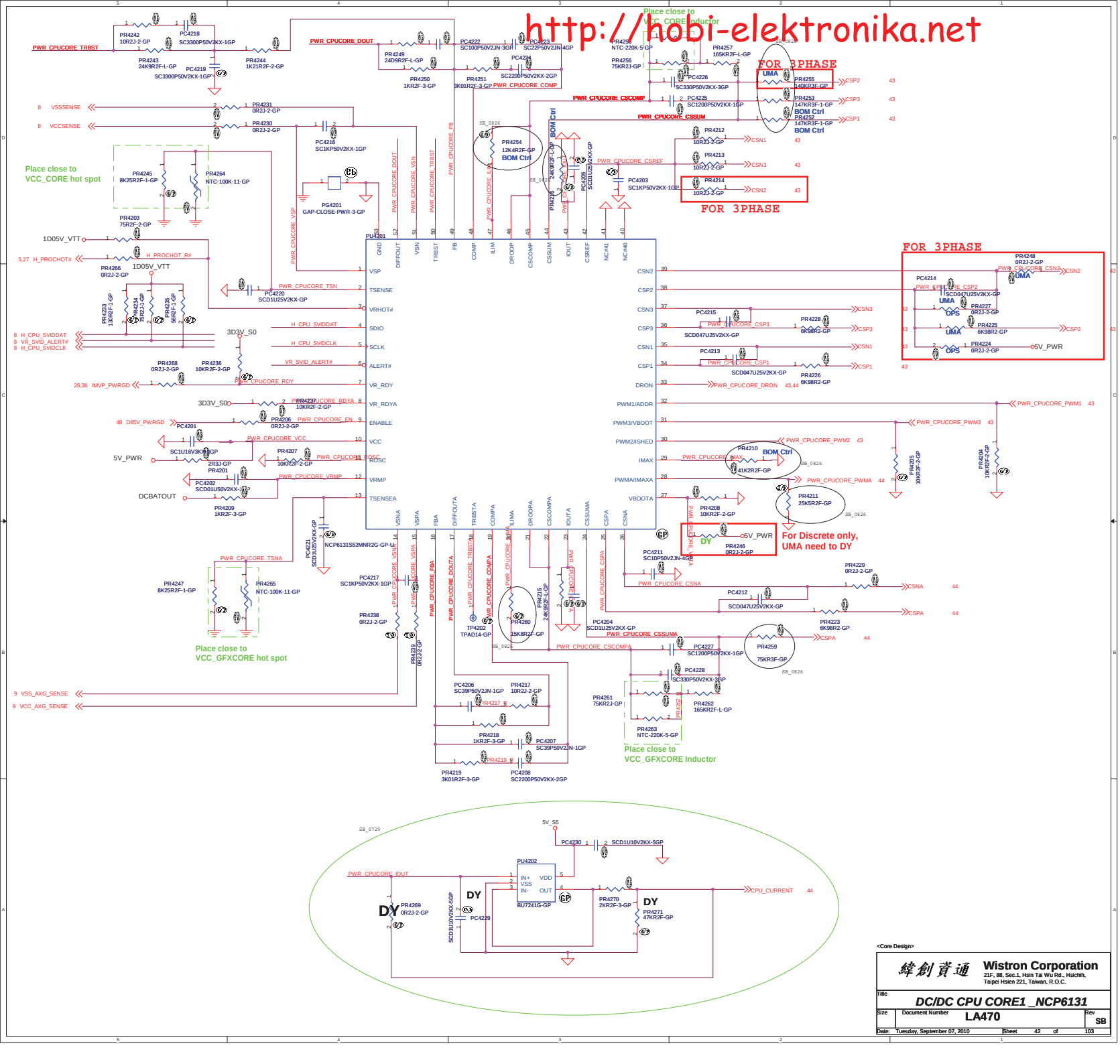
<Core Design>

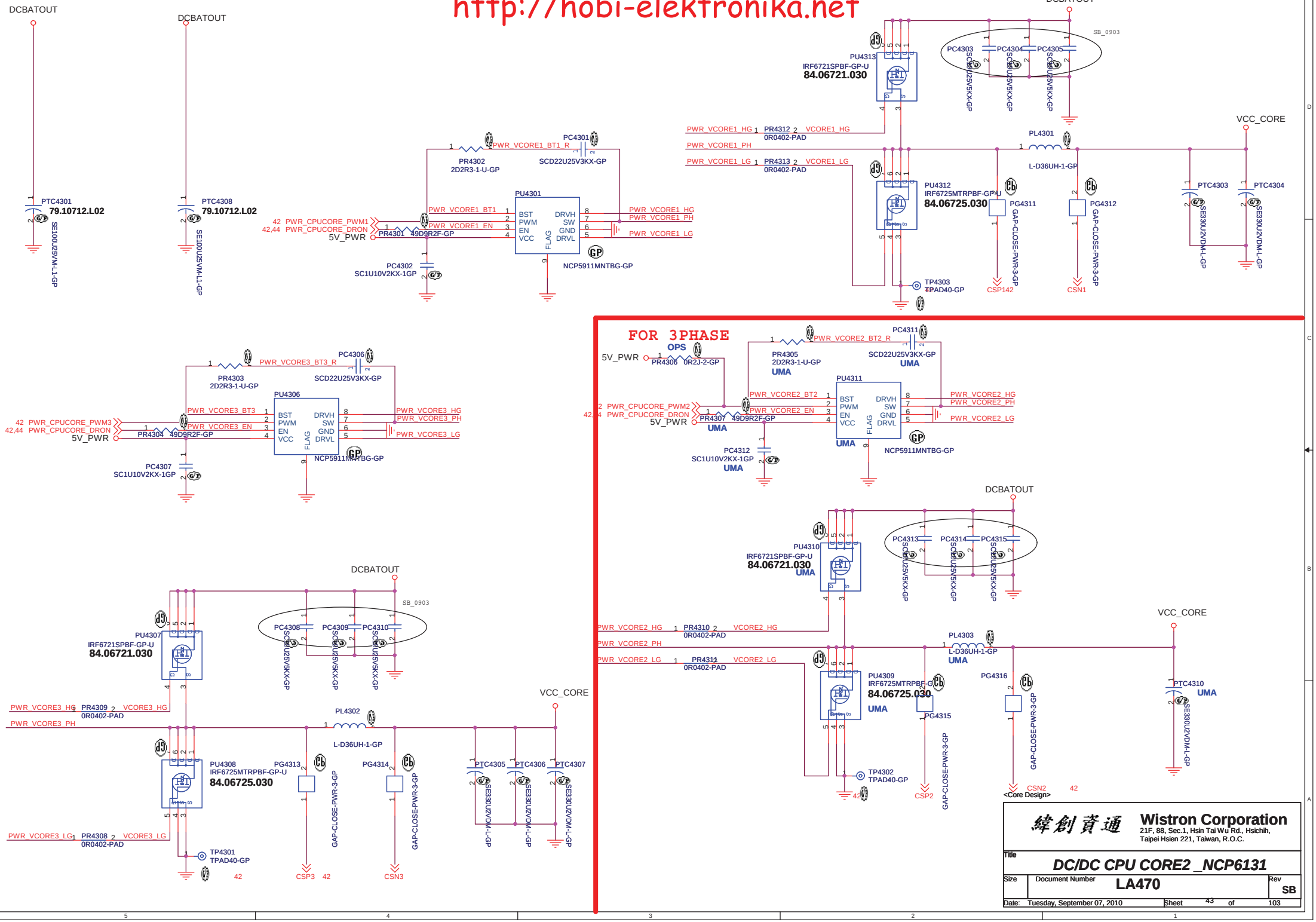
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 3D3V5V

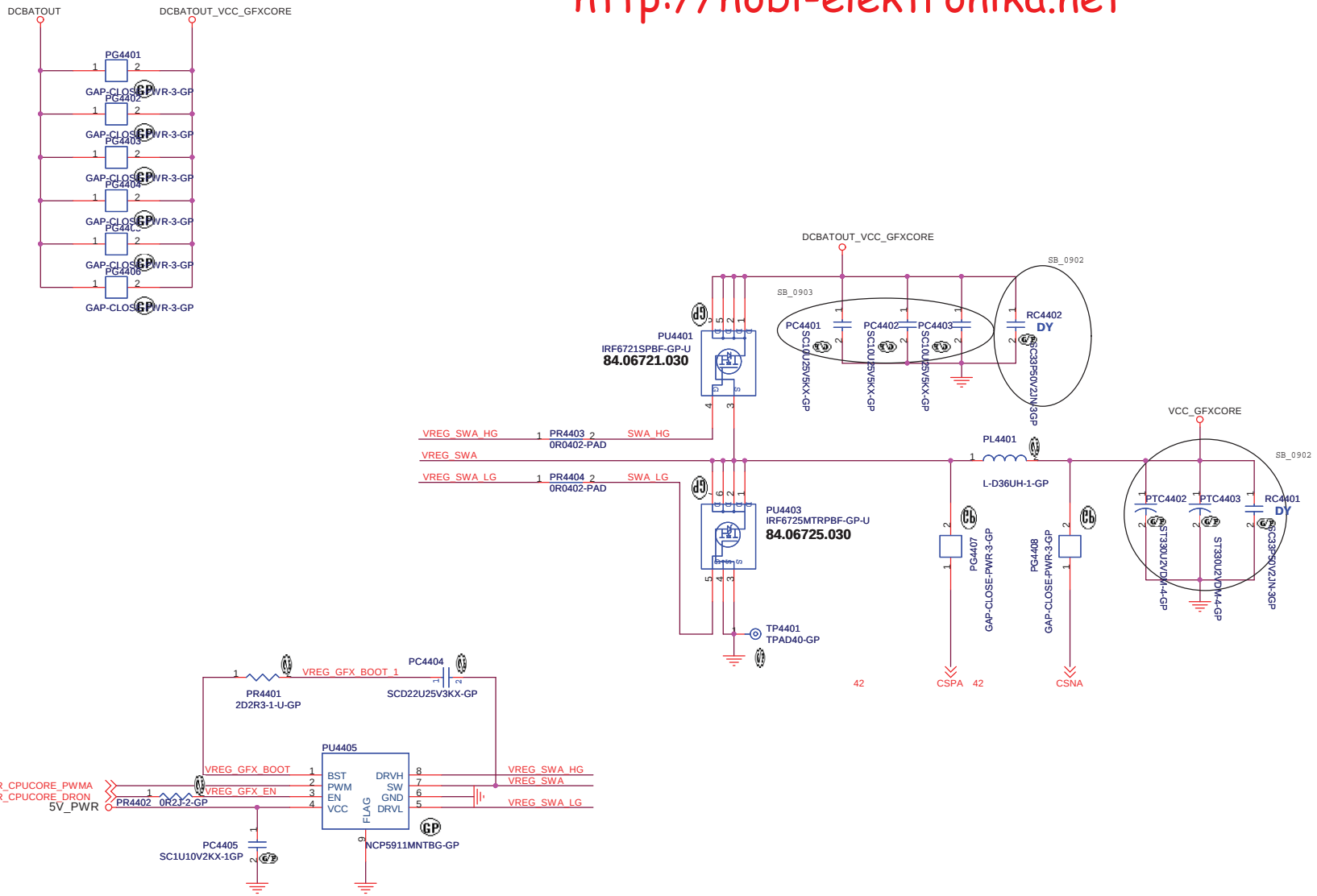
Size: | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 41 of 103



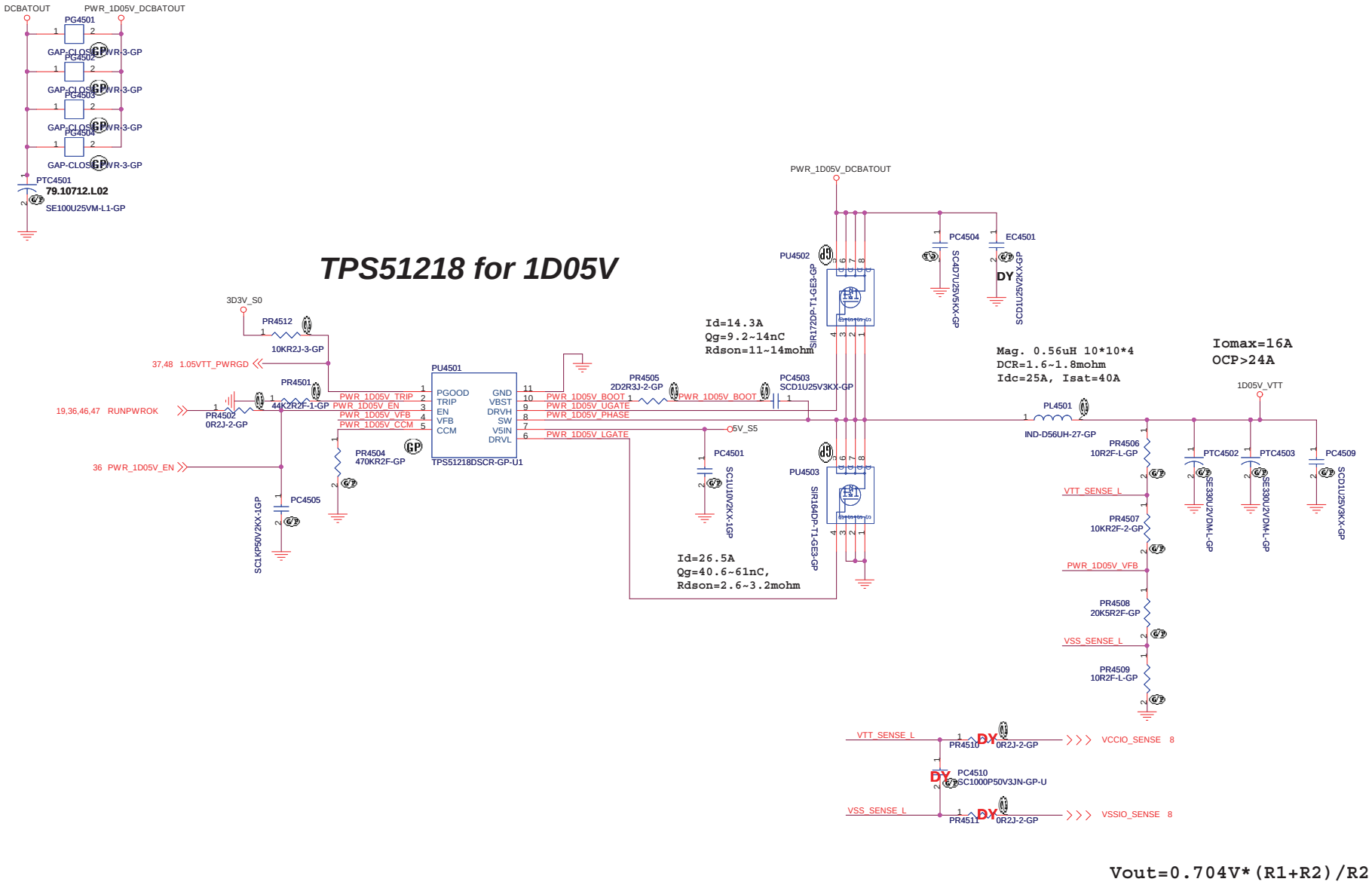


緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DC/DC CPU CORE2 _NCP6131		
Size	Document Number LA470	Rev SB	
Date: Tuesday, September 07, 2010	Sheet 43 of 103		



<Core Design>

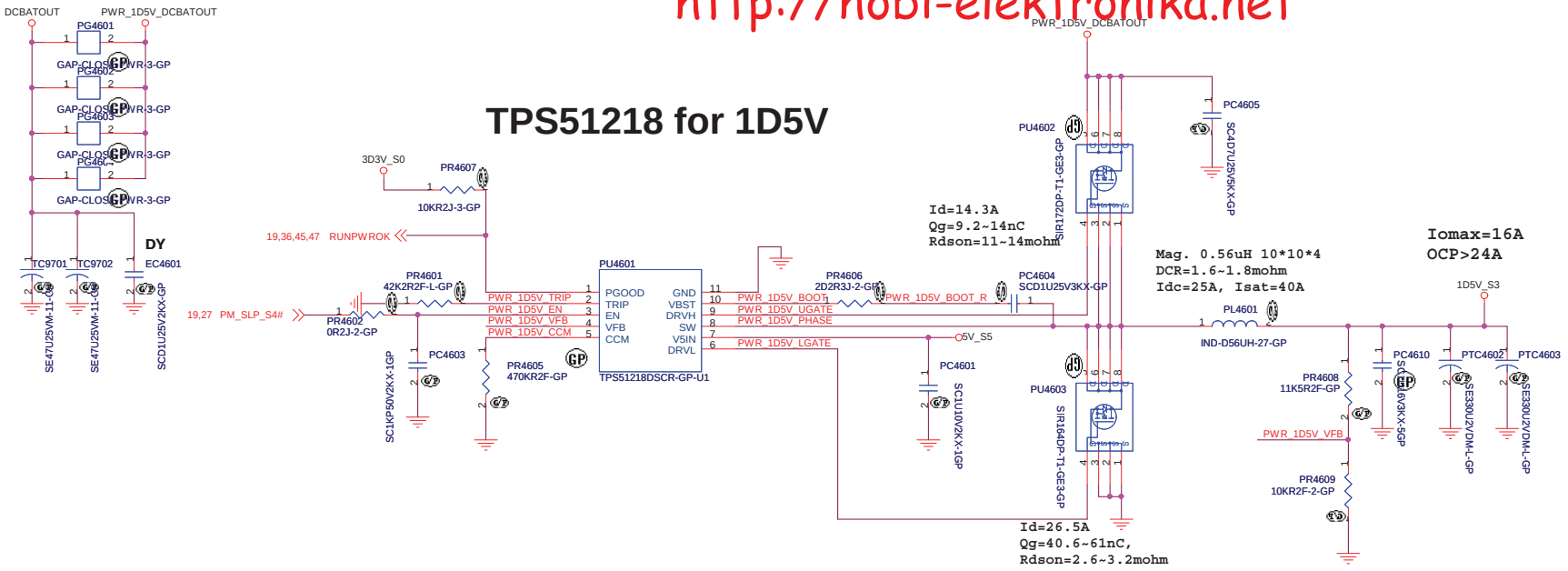
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DC/DC CPU CORE3 _NCP6131
Size / Document Number	LA470
Rev	SB
Date: Tuesday, September 07, 2010	Sheet 44 of 103



<Core Design>

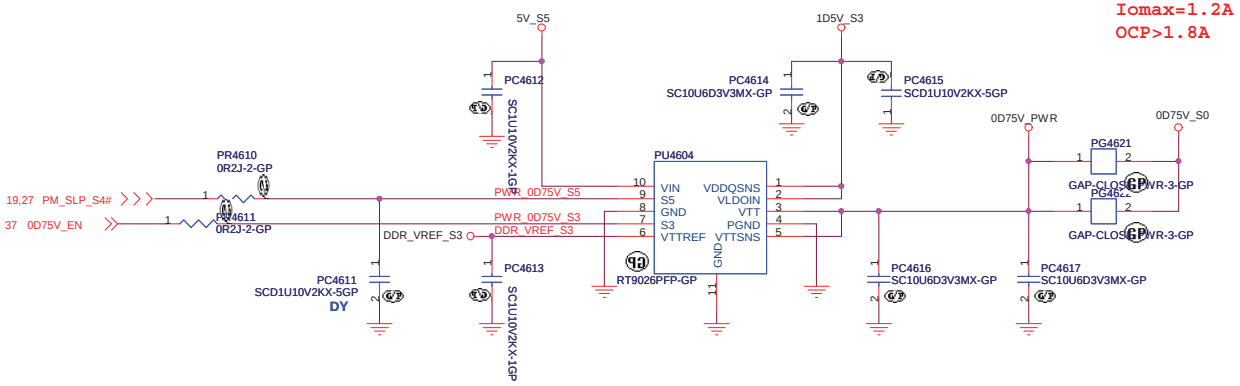
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51218_1D05V		
Size	Document Number	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 45 of 103	

TPS51218 for 1D5V



Vout=0.704V*(R1+R2)/R2

RT9026 for 0D75V_S3



<Core Design>

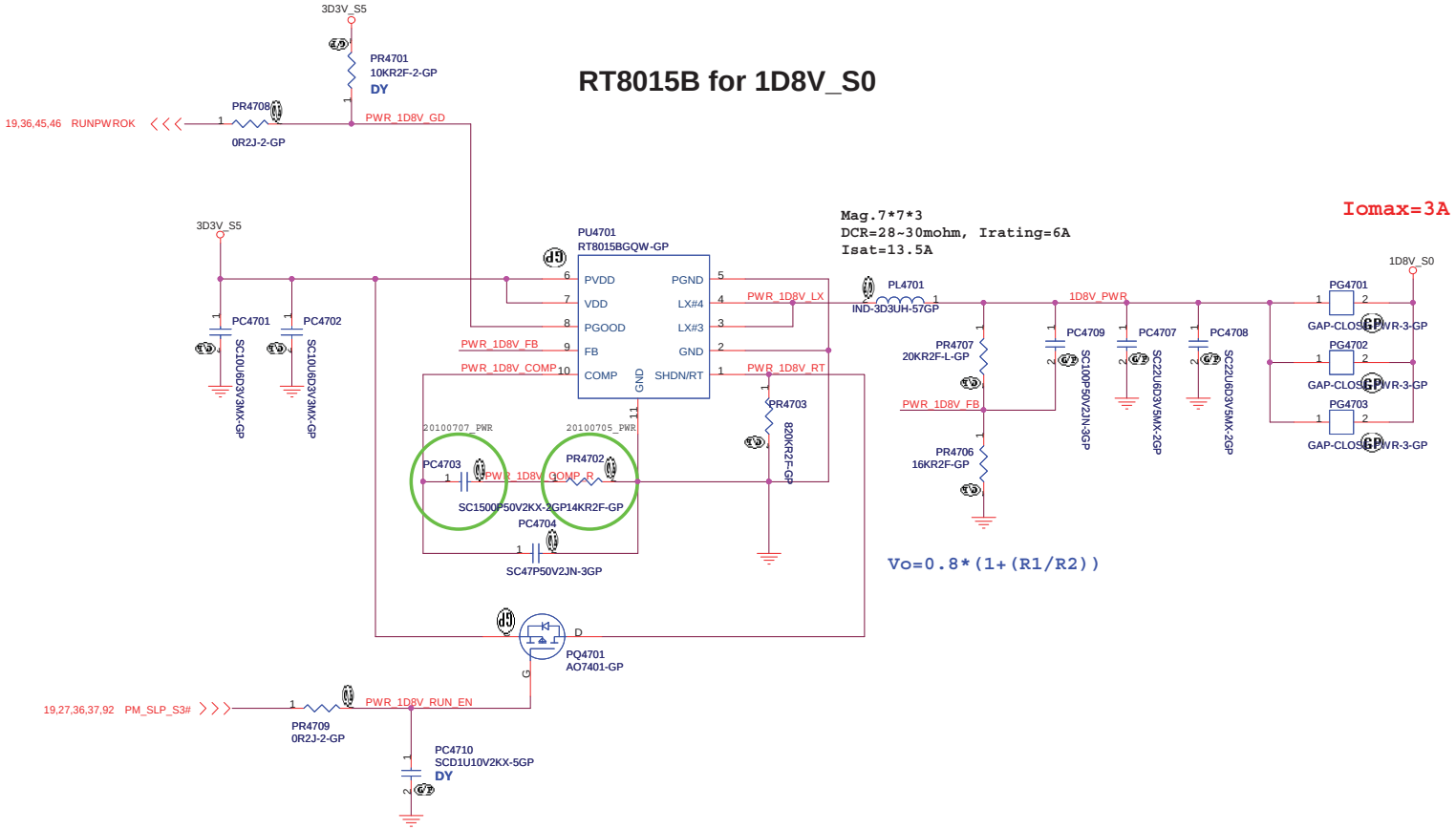
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		SB

Date: Tuesday, September 07, 2010 Sheet 46 of 103

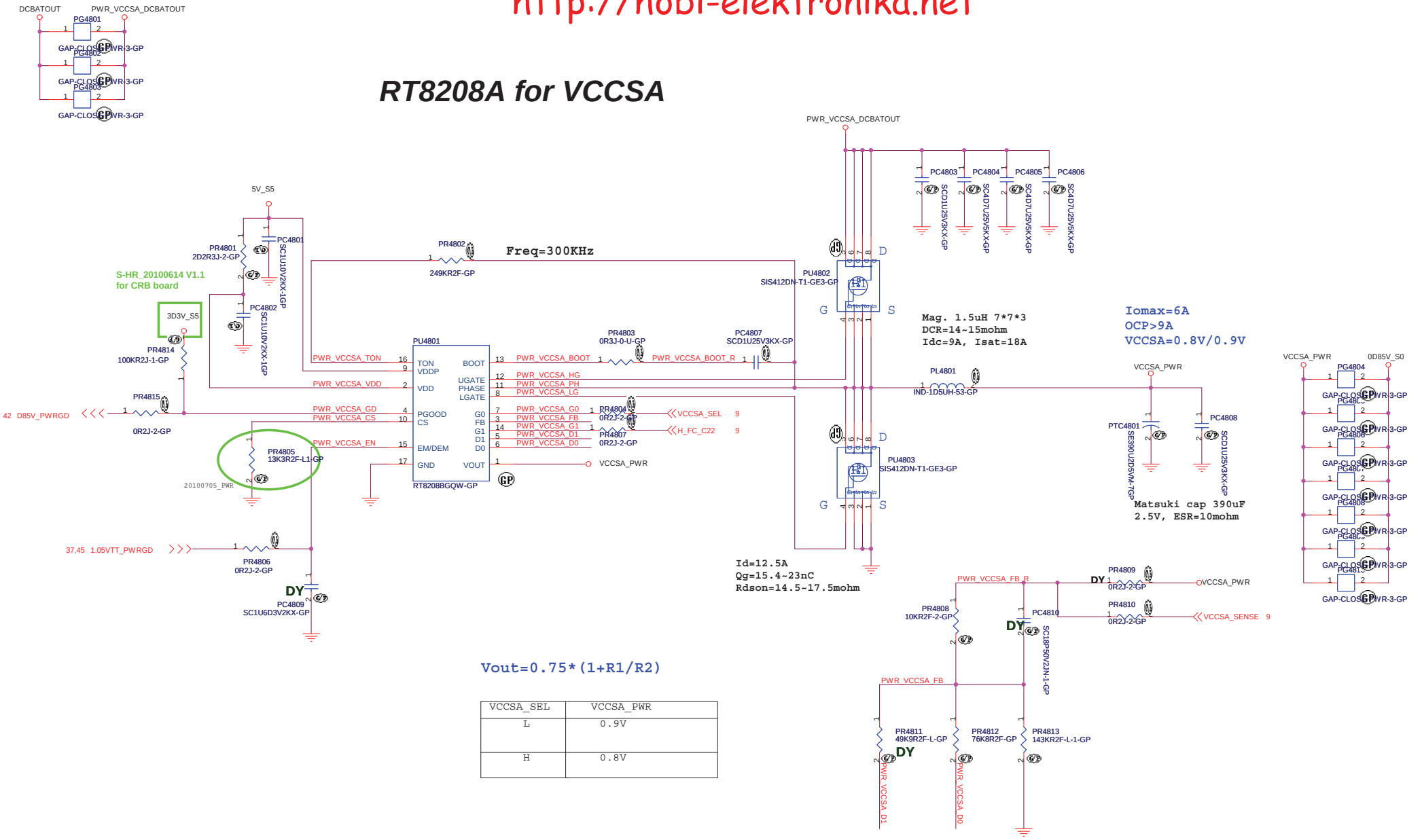
RT8015B for 1D8V_S0



<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PWM_1D8V_RT8015B
Size	Document Number: LA470 — Rev: SB
Date: Tuesday, September 07, 2010	Sheet 47 of 103

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

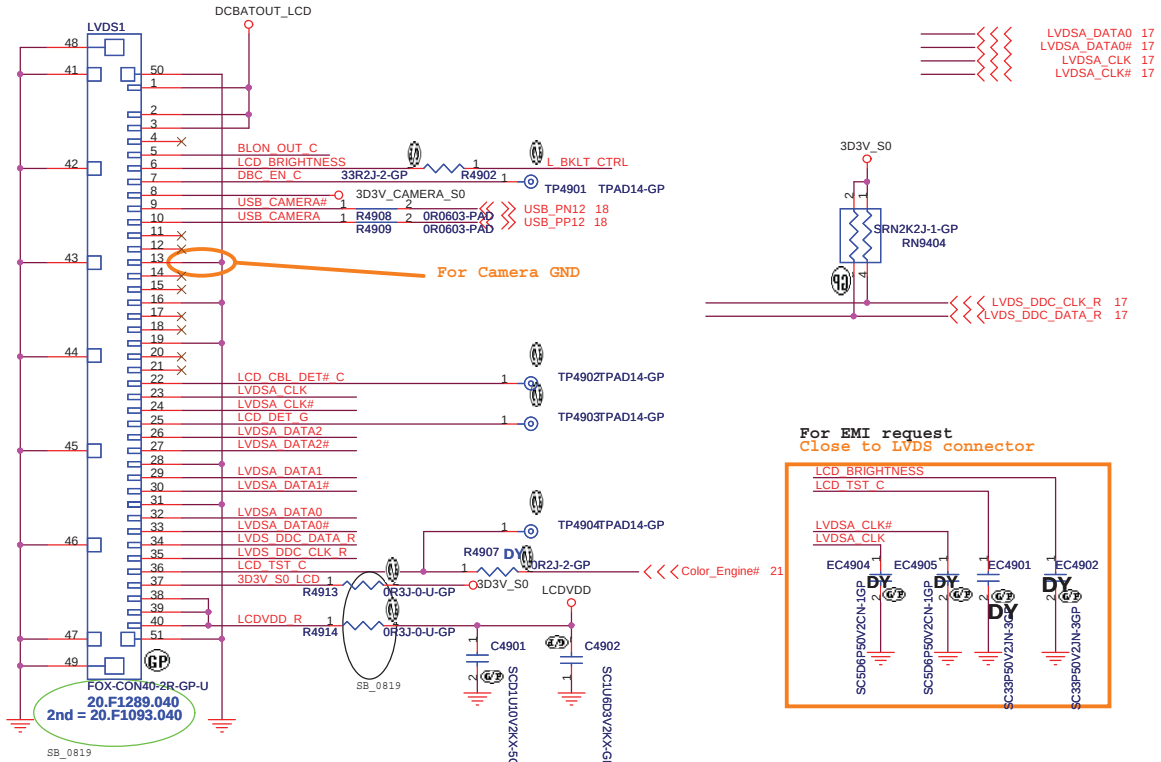
<Core Design>

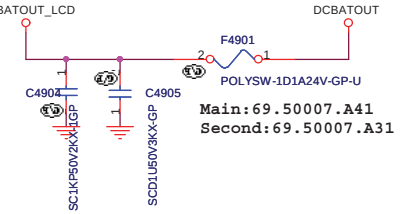
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

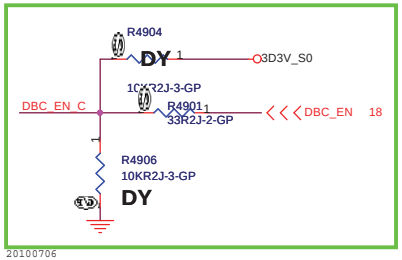
Title	RT8208B_VCCSA	
Size	Document Number LA470	Rev SB
Date: Tuesday, September 07, 2010	Sheet 48 of 103	

SSID = VIDEO

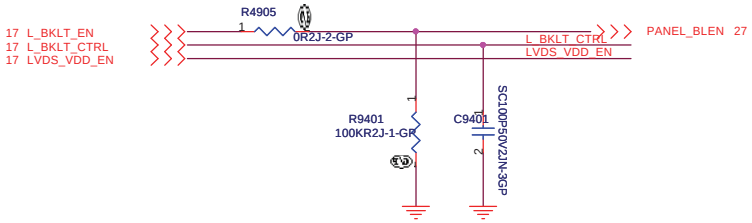
LVDS CONNECTOR



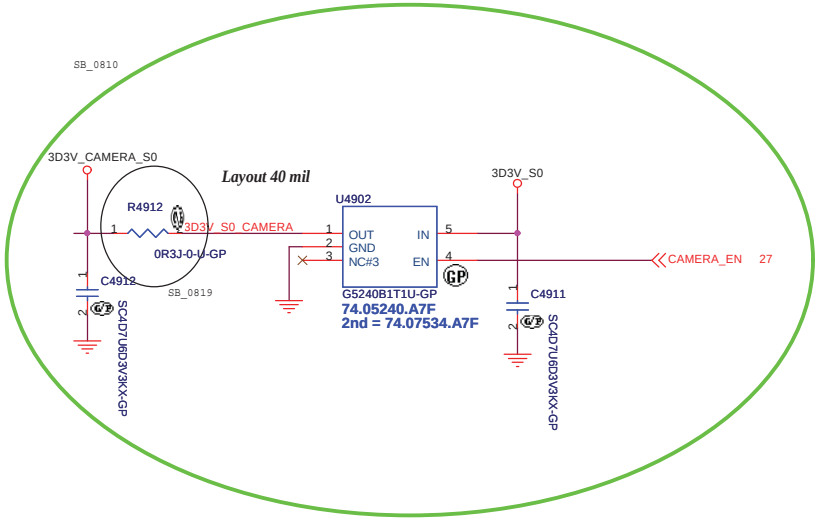




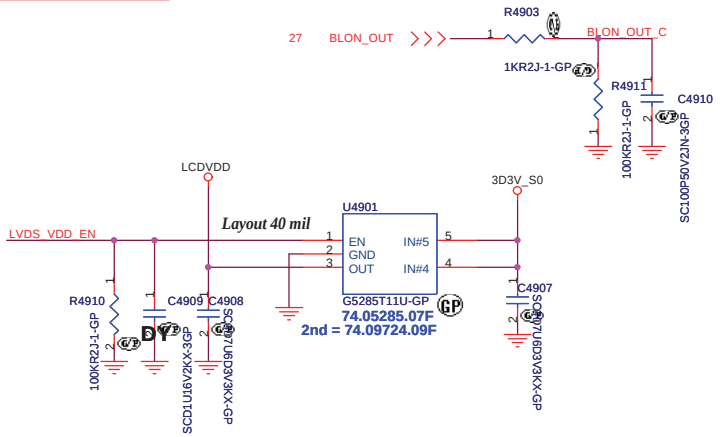
Panel BL brightness/Power En/BL En



CAMERA POWER



SSID = VIDEO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

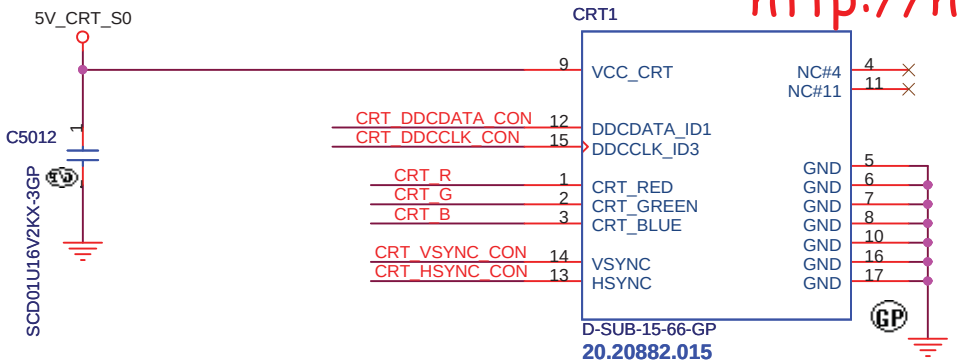
Title: LCD Connector

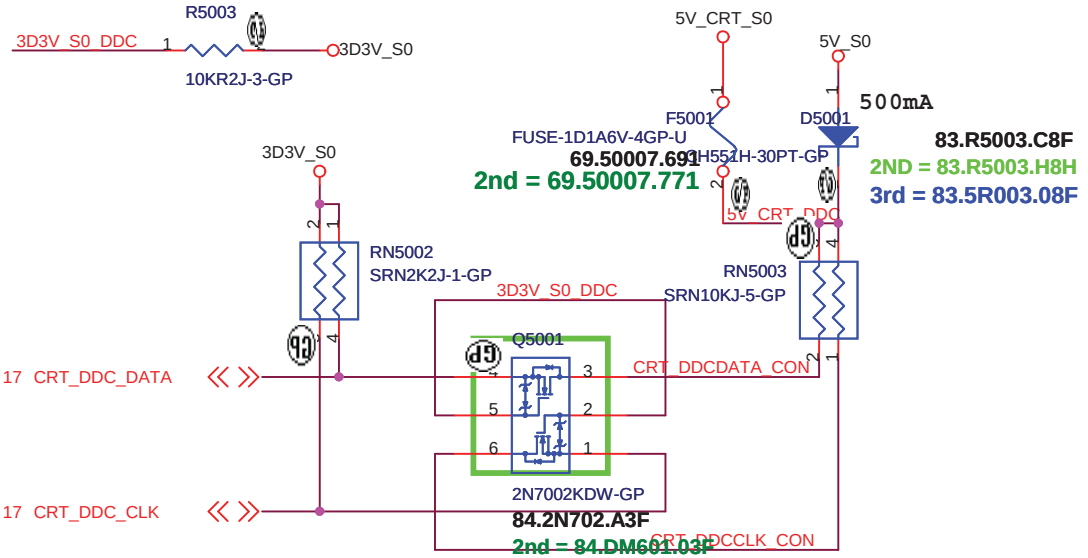
Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 49 of 103

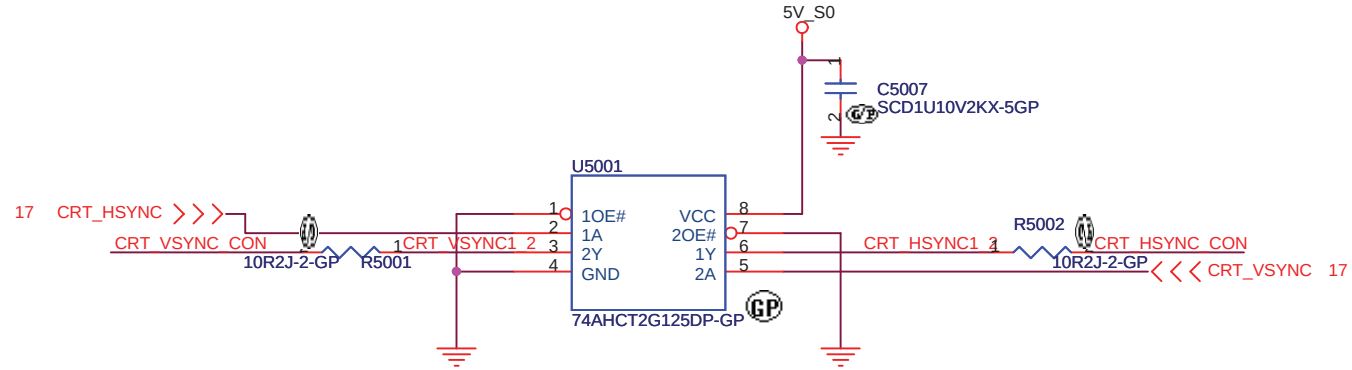
CRT DDCDATA & DDCCLK level shift

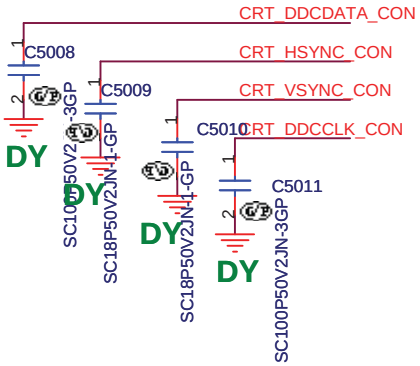
Pull High 5V Design on CRT Board



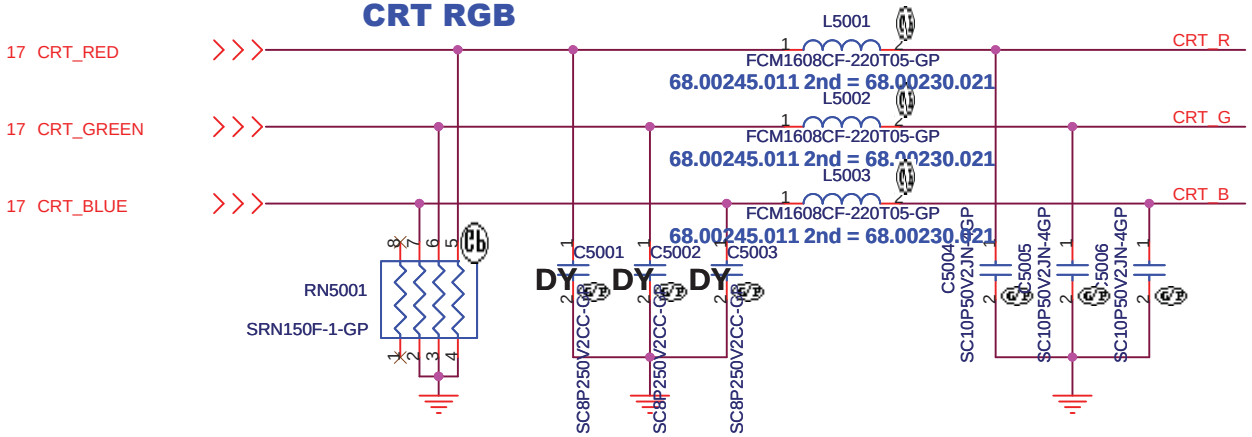


CRT Hsync & Vsync level shift





CRT RGB



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT Connector***	
Size A4	Document Number **LA470**	Rev **SB**
Date: Tuesday, September 07, 2010	Sheet 50 of 103	

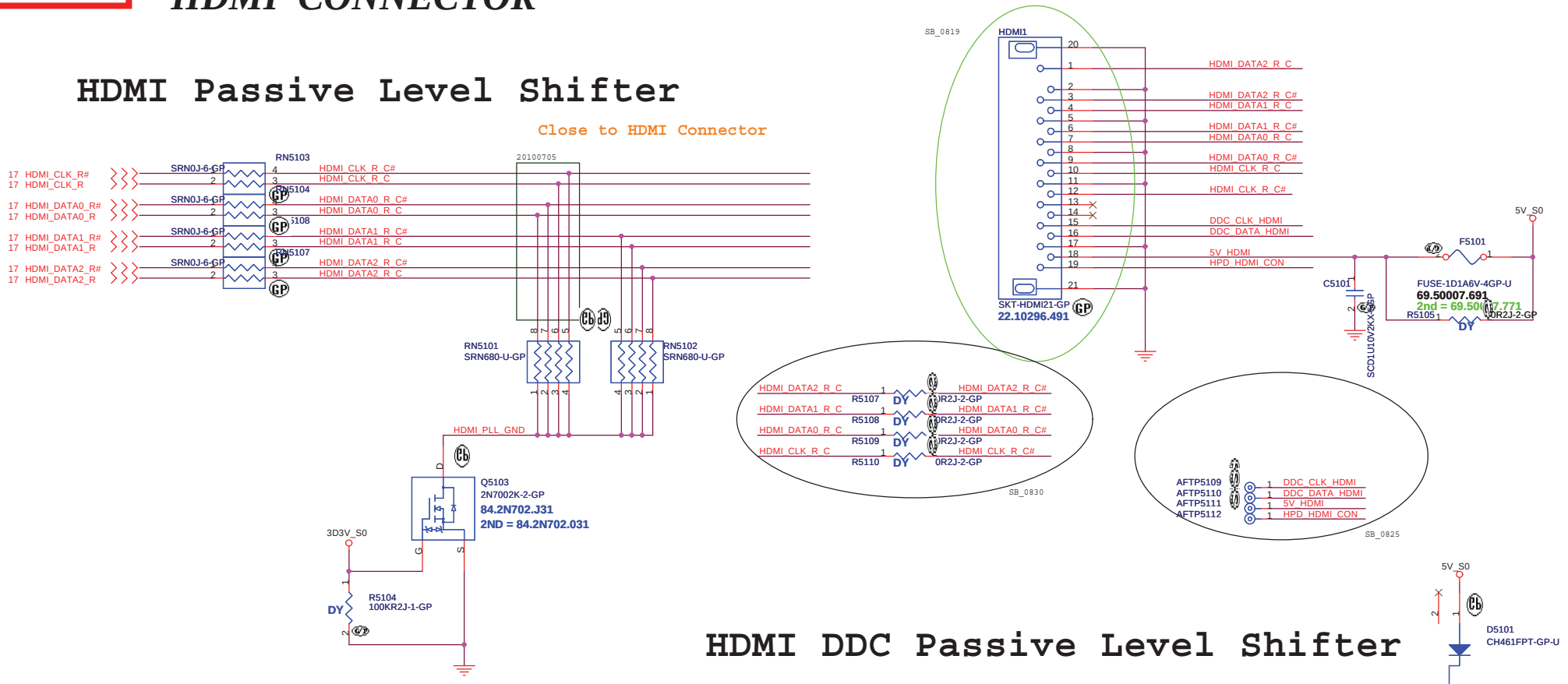
SSID = VIDEO

HDMI CONNECTOR

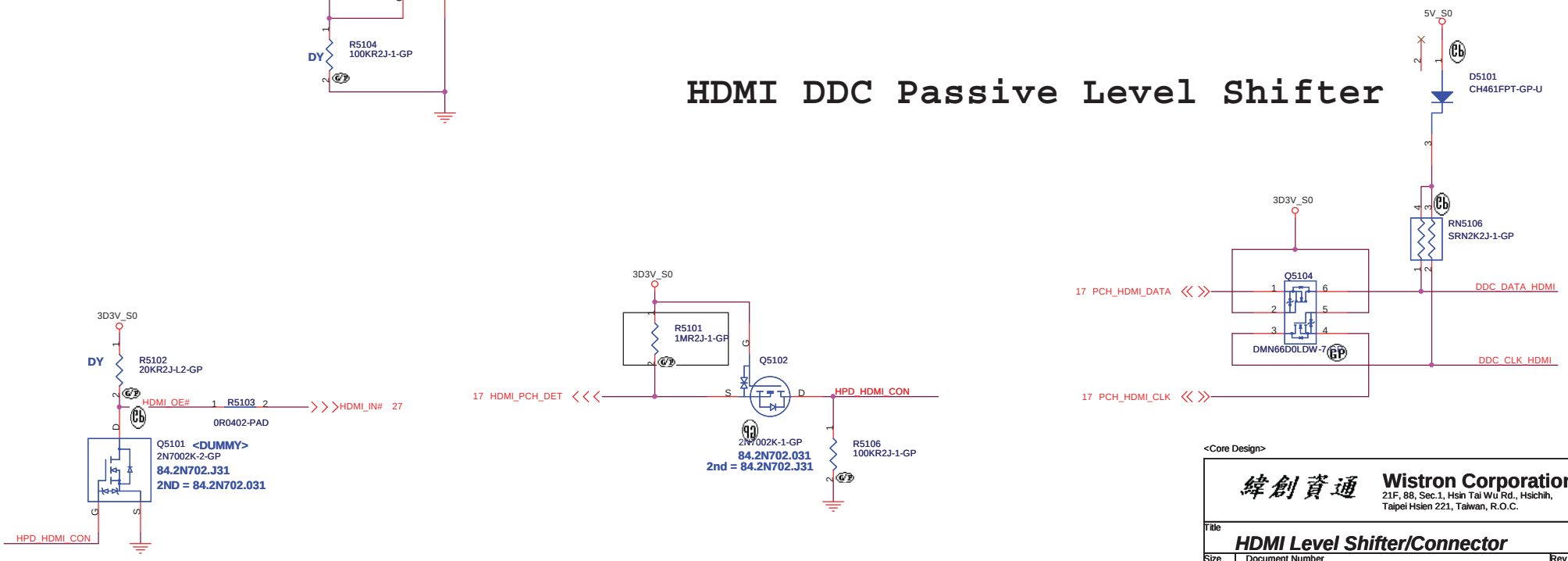
HDMI CONN

HDMI Passive Level Shifter

Close to HDMI Connector



HDMI DDC Passive Level Shifter



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDMI Level Shifter/Connector		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 51 of 103	

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: eDP

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 52 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: S-VIDEO

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 53 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

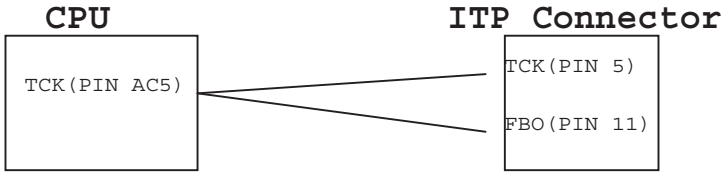
Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



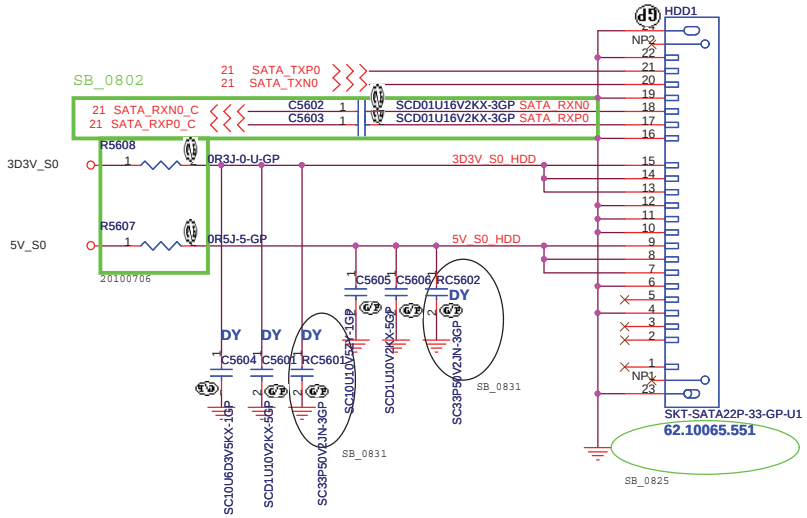
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

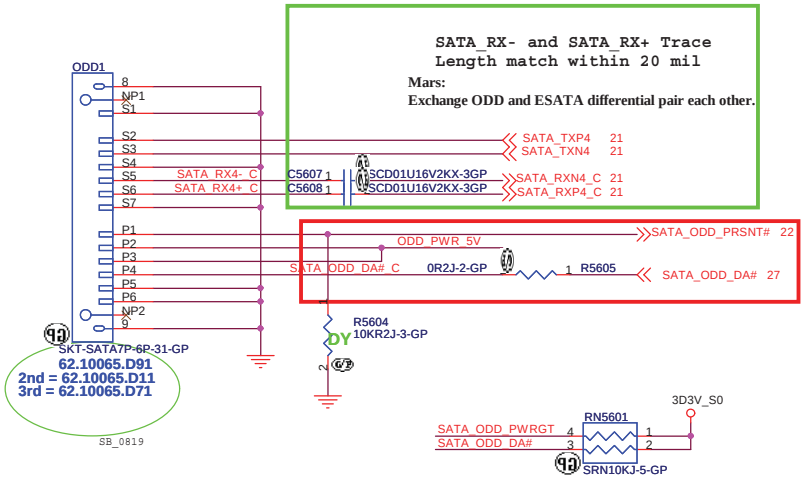
Title: ITP		
Size: A4	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 55 of 103	

SSID = SATA

SATA HDD Connector

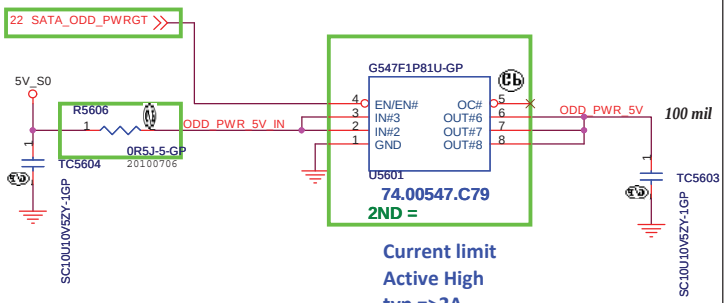


ODD Connector



SUPPORT ZERO SATA ODD

SATA Zero Power ODD



<Core Design>

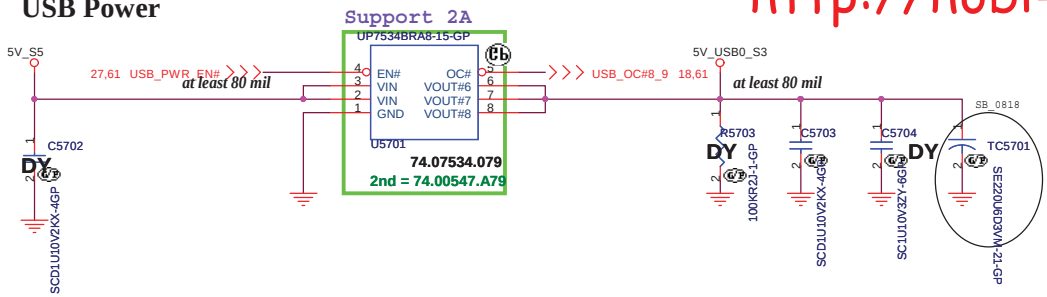
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

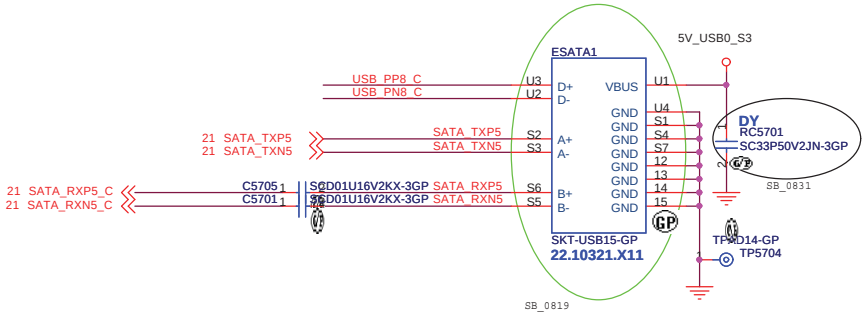
Title: HDD/ODD

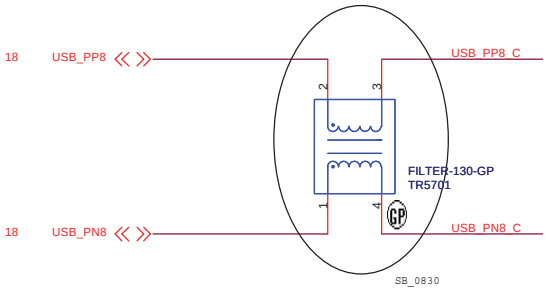
Size	Document Number	Rev
A3	LA470	SB

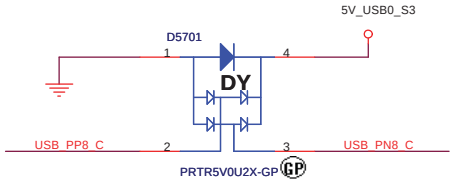
Date: Tuesday, September 07, 2010 Sheet 56 of 103

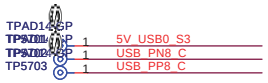
USB Power











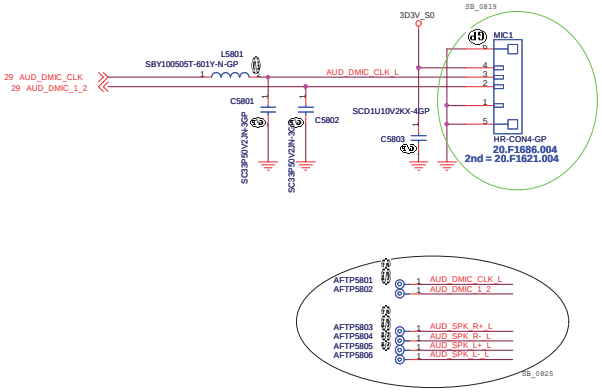
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: E-SATA

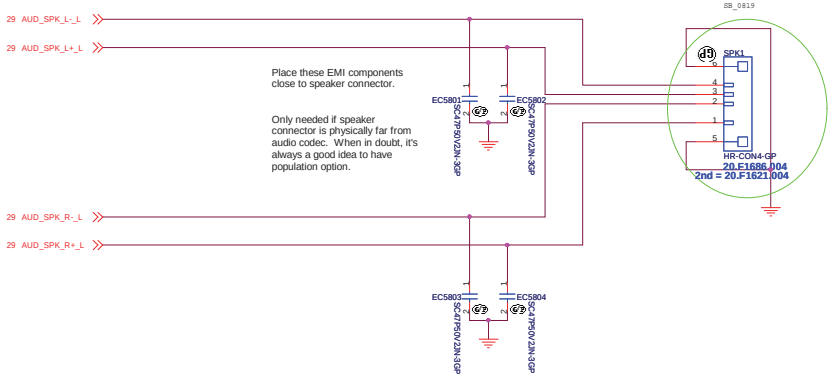
Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 57 of 103



INTERNAL STEREO SPEAKERS

Port G



<Core Design>

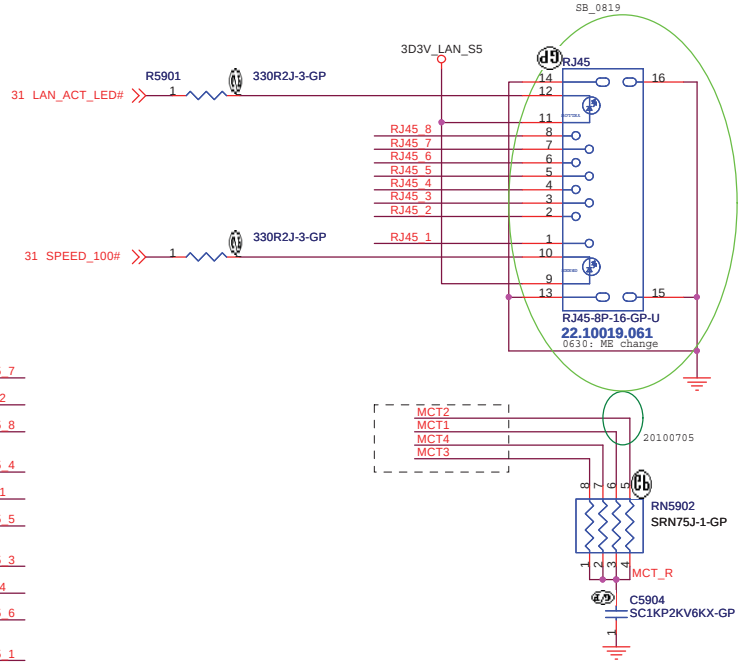
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MIC/SPEAKER/AUDIO JACK

Size	Document Number	Rev
A2	LA470	SB

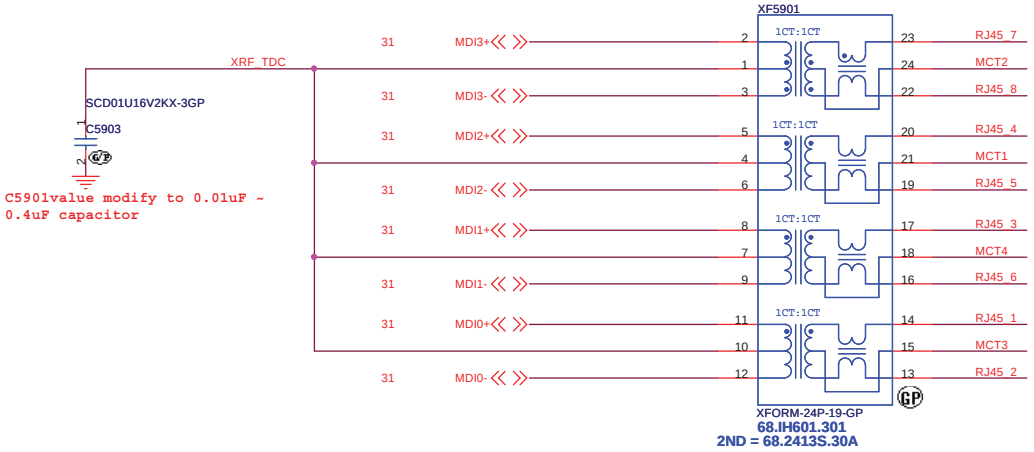
Date: Tuesday, September 07, 2010 Sheet 58 of 103

LAN Connector



FOR CO-LAY

GIGA Lan Transformer



1st
68.IH601.301(Taimag) for 1000
68.HH035.301(Taimag) for 10/100
2nd
68.2413S.30A(Lankom) for 1000
68.H6441.301(Lankom) for 10/100

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

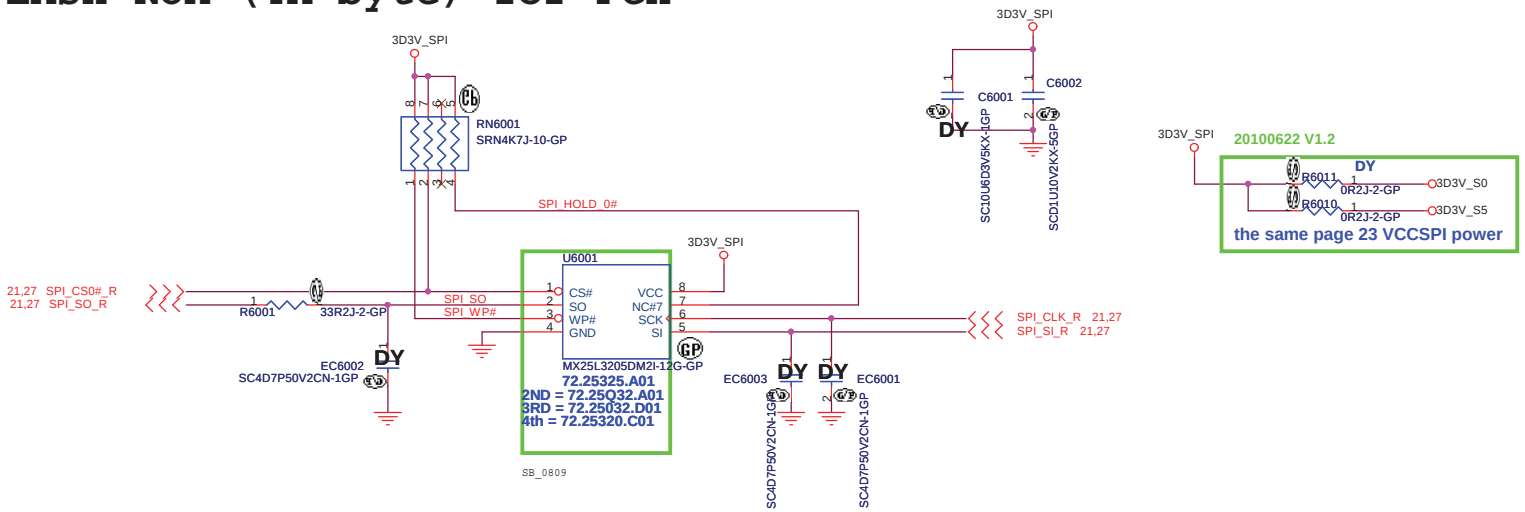
Title: ***RJ45 / Transformer***

Size	Document Number	Rev
A3	LA470	SB

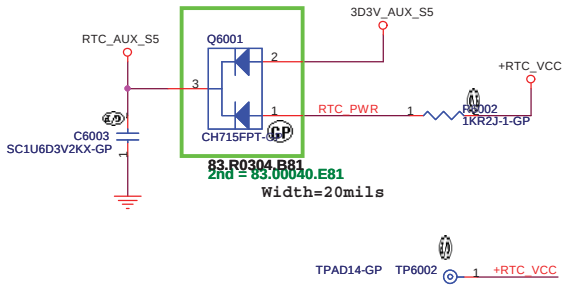
Date: Tuesday, September 07, 2010 Sheet 59 of 103

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

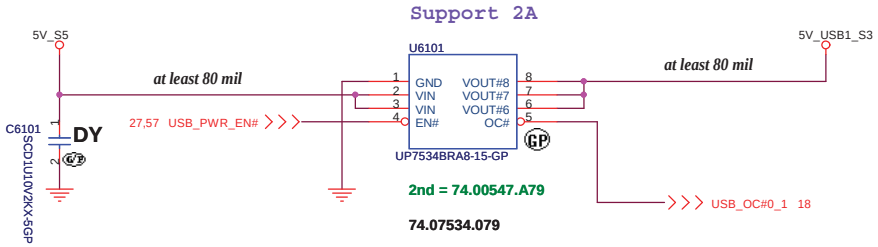
Title: Flash/RTC

Size	Document Number	Rev
A3	LA470	SB

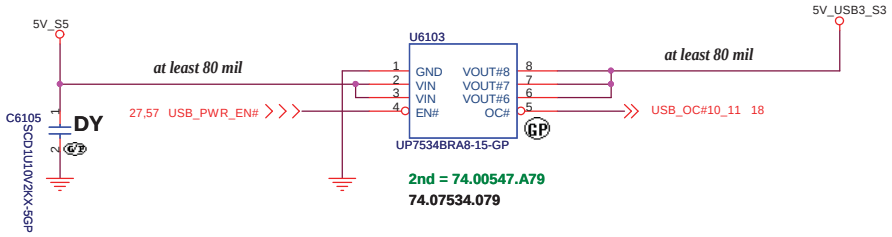
Date: Tuesday, September 07, 2010 Sheet 60 of 103

SSID = USB

IO Board USB Power



Sub-USB Board Power



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 61 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Port

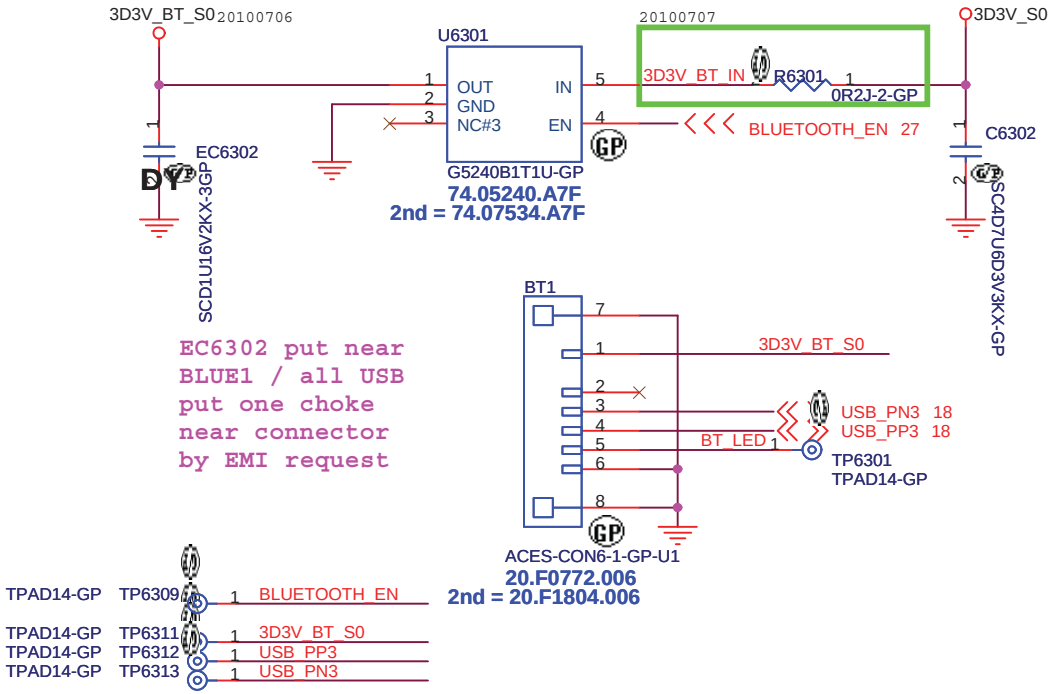
Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 62 of 103

SSID = User.Interface

Bluetooth Module conn.

Bluetooth Module

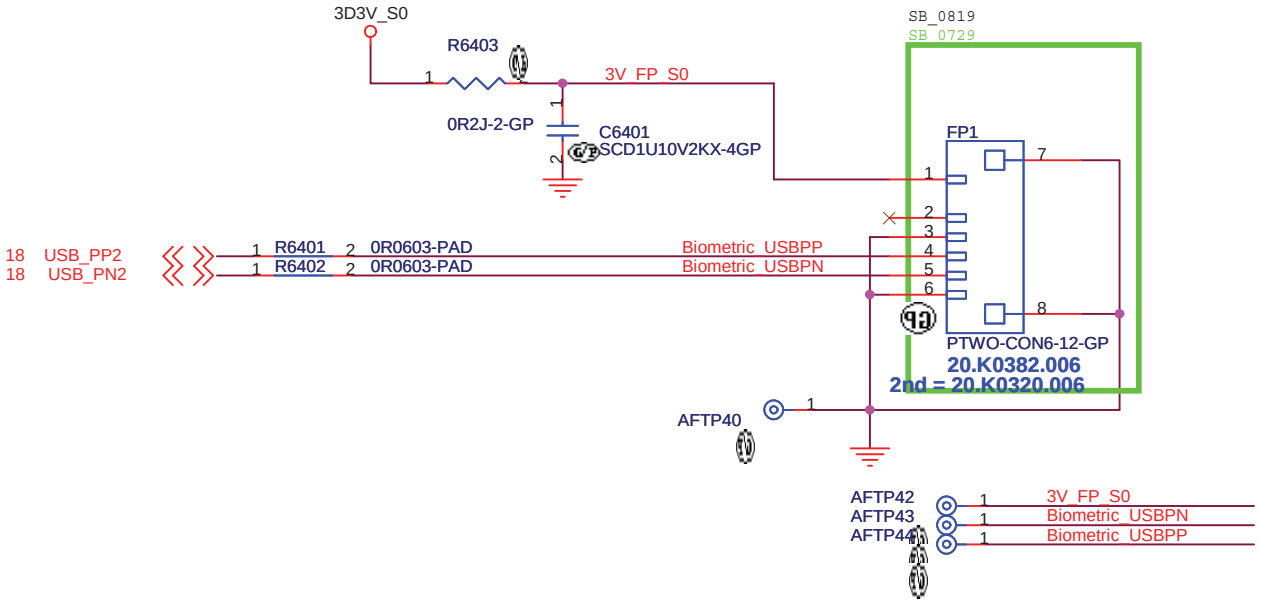


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Bluetooth**		
Size: A4	Document Number: **LA470**	Rev: **SB**
Date: Tuesday, September 07, 2010	Sheet 63 of 103	

Finger Printer Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

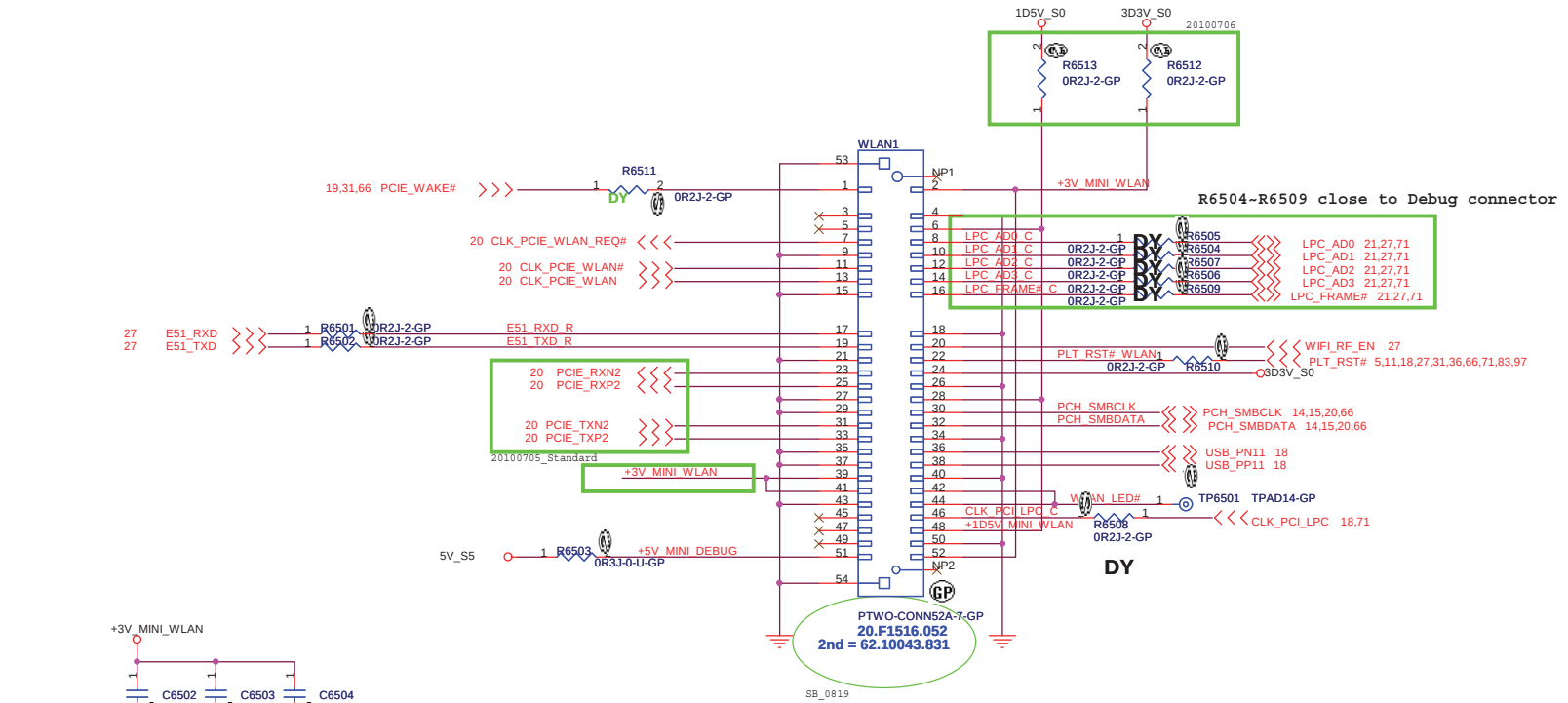
Title: **RESERVED**

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

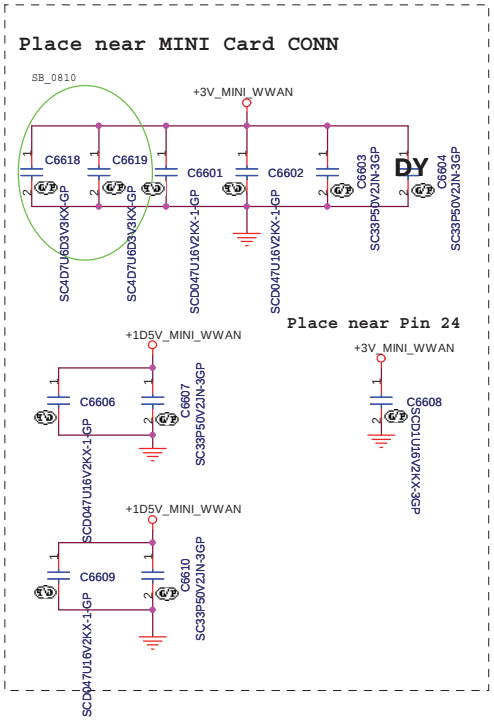
Title: MINICARD(WLAN)/ITP CONN

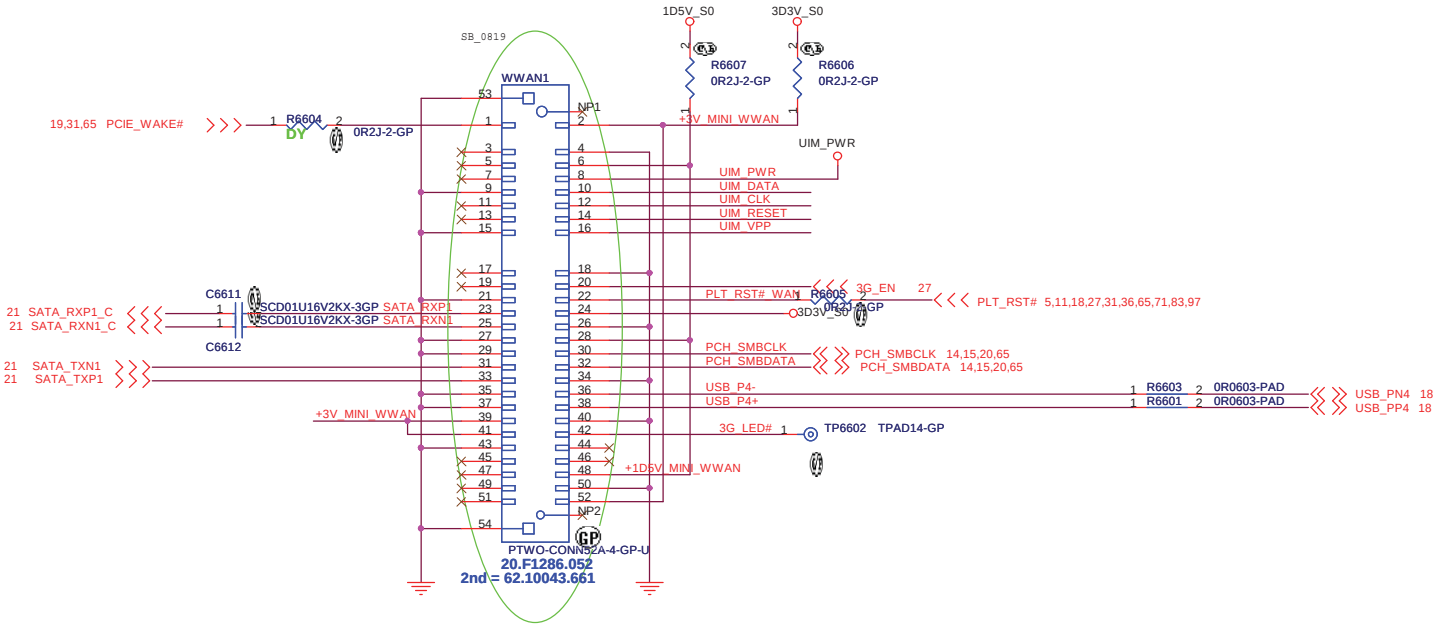
Size	Document Number	Rev
A3	LA470	SB

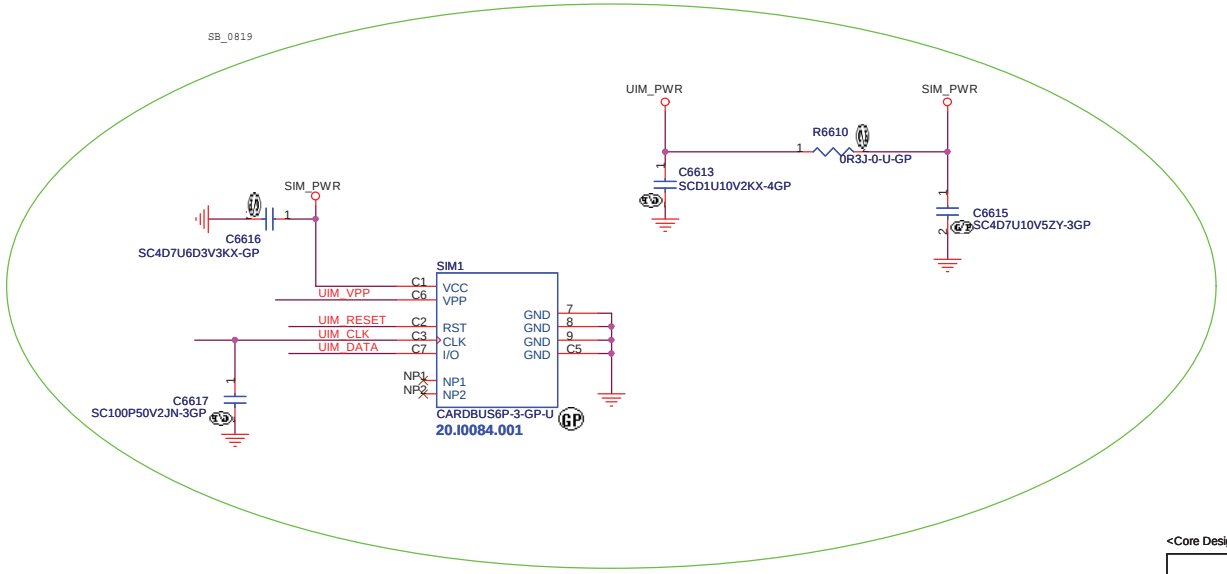
Date: Tuesday, September 07, 2010 Sheet 65 of 103

Mini Card Connector(WWAN)

SSID = Wireless







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **WWAN Connector**

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 66 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

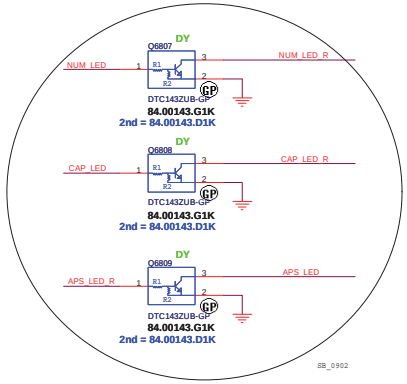
Size	Document Number	Rev
A4	LA470	SB

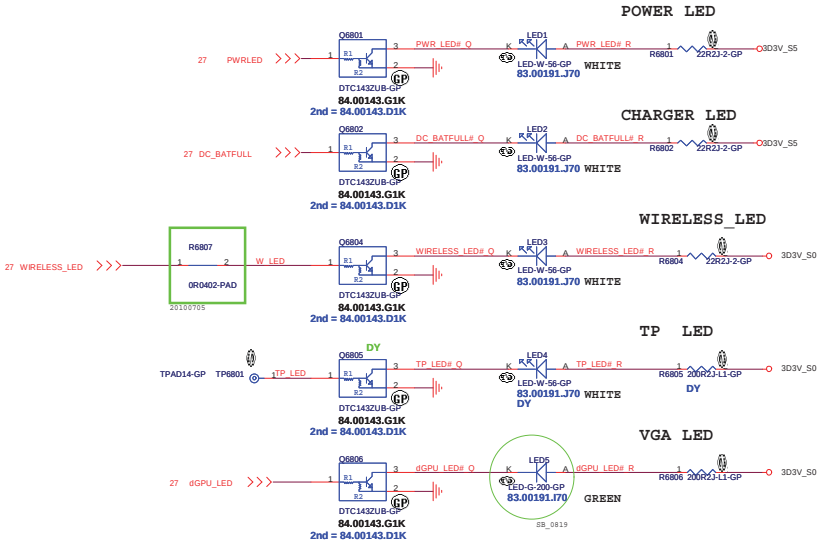
Date: Tuesday, September 07, 2010 Sheet 67 of 103

SSID = User.Interface

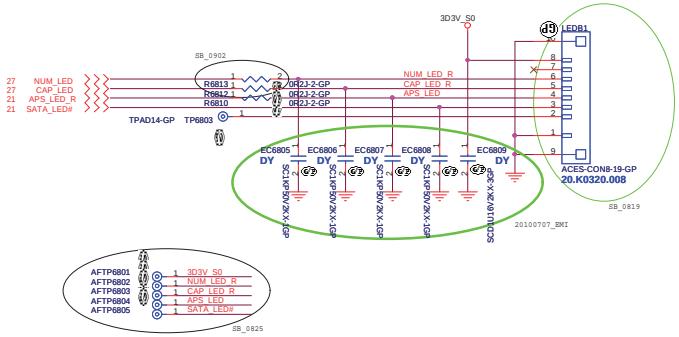
http://hobi-elektronika.net

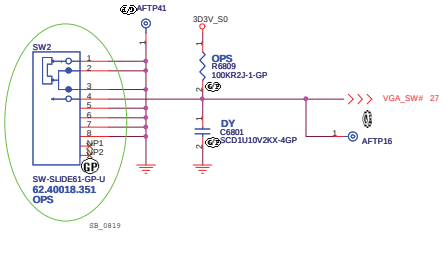
Power button LED

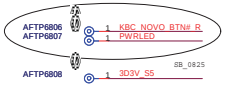




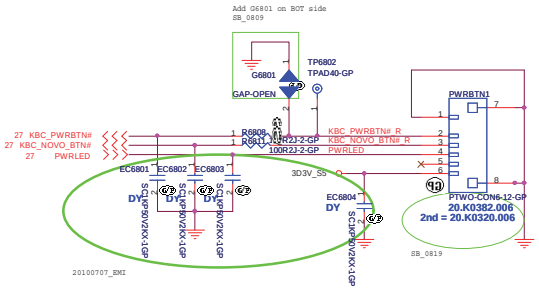
LED Bord CONN.







Power button LED(White)



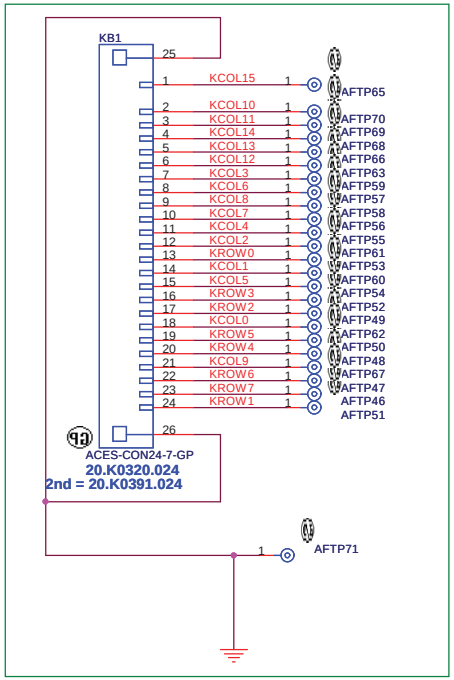
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button
Size: A2 | Document Number: LA470 | Rev: SB
Date: Tuesday, September 07, 2010 | Sheet 68 of 103

SSID = KBC

Internal KeyBoard Connector



KROW[0..7] 27

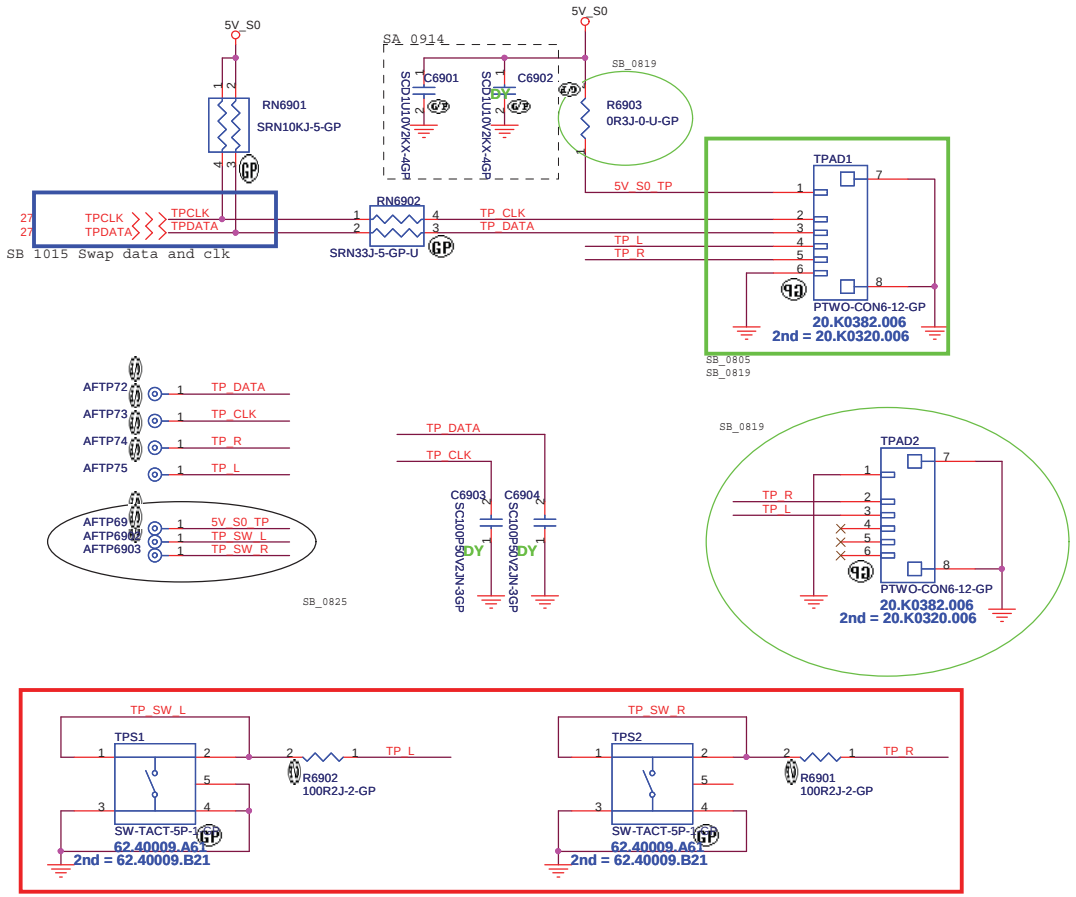
KCOL[0..15] 27

20100705

* Membrane Pin Out Top View :

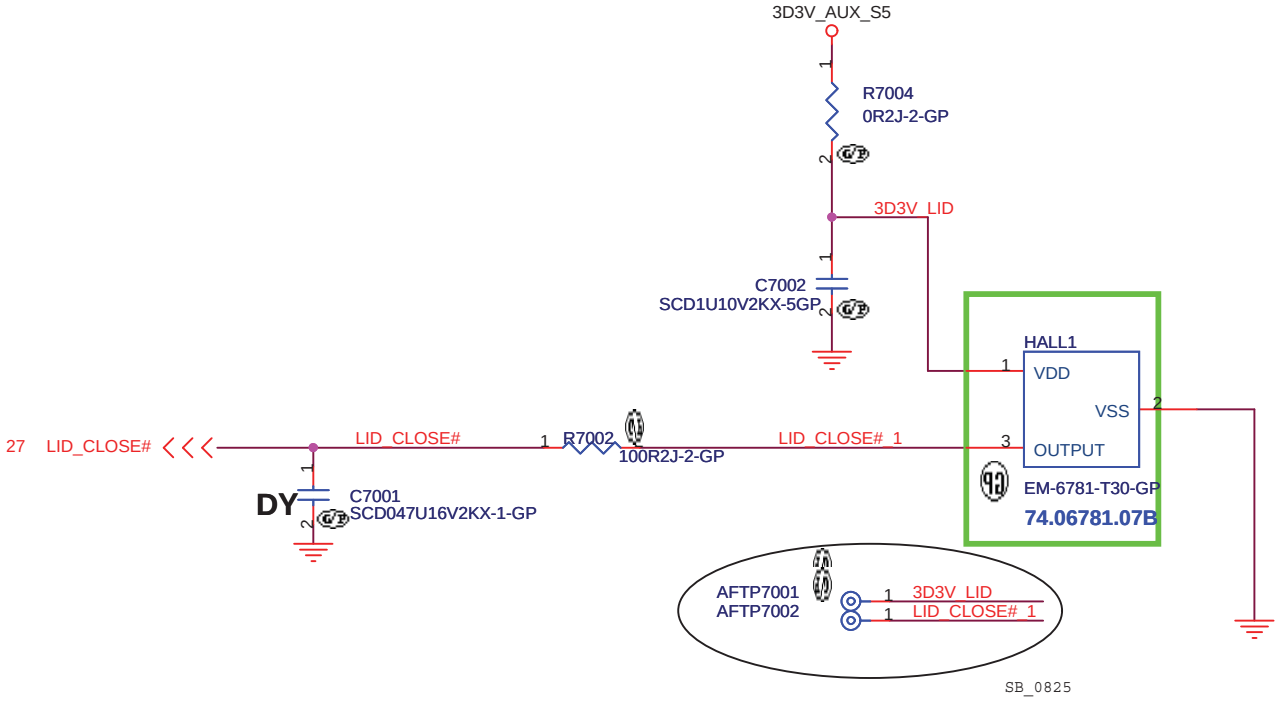
PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad



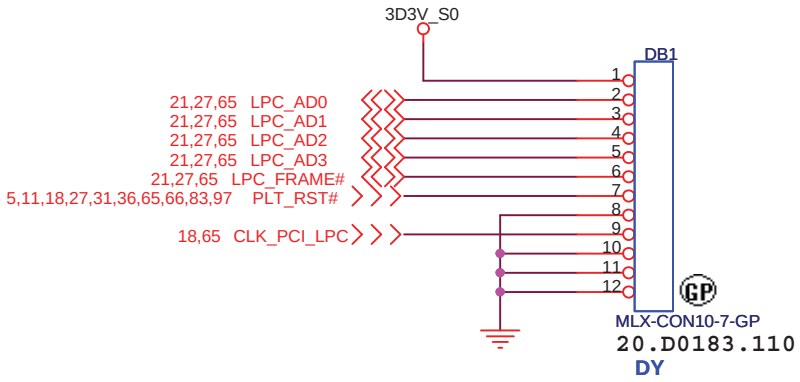
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Key Board/Touch Pad**
Size A3 / Document Number	LA470
Rev	SB
Date: Tuesday, September 07, 2010	Sheet 69 of 103



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Hall Sensor***
Size: A4	Document Number: **LA470**
Rev: **SB**	
Date: Tuesday, September 07, 2010	Sheet 70 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 71 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 72 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 73 of 103

<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 74 of 103

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 75 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 76 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 77 of 103

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<Core Design>

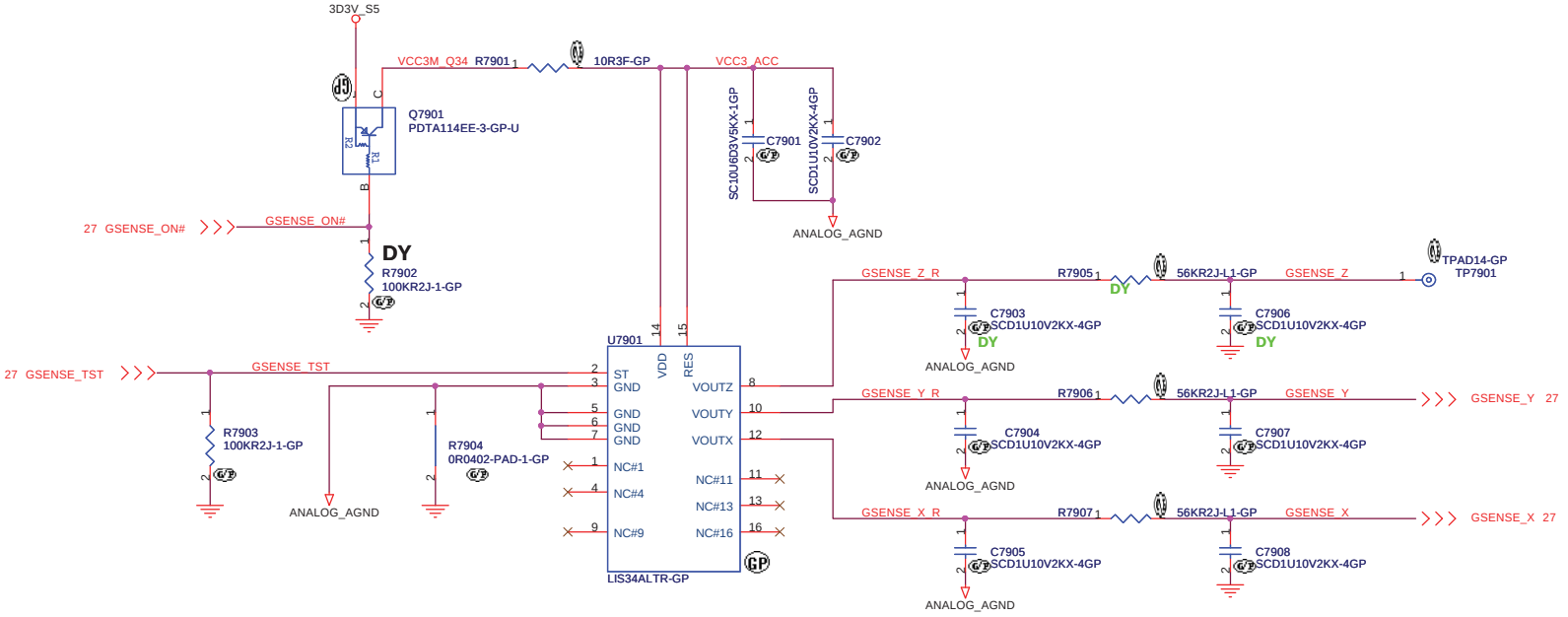
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 78 of 103

G-Sensor



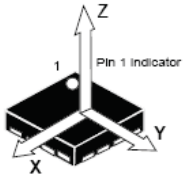
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G-Sensor**

Size: Custom | Document Number: **LA470** | Rev: **SB**

Date: Tuesday, September 07, 2010 | Sheet 79 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 80 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

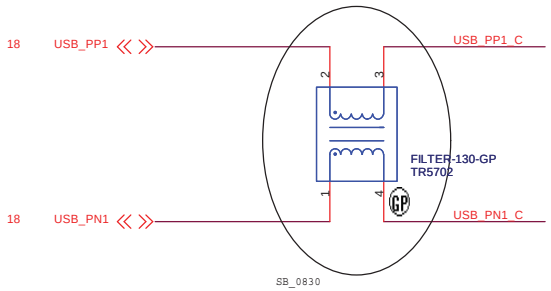
Title: ***Reserved***

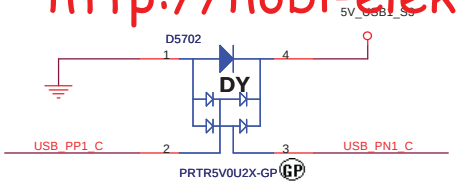
Size	Document Number	Rev
A4	LA470	SB

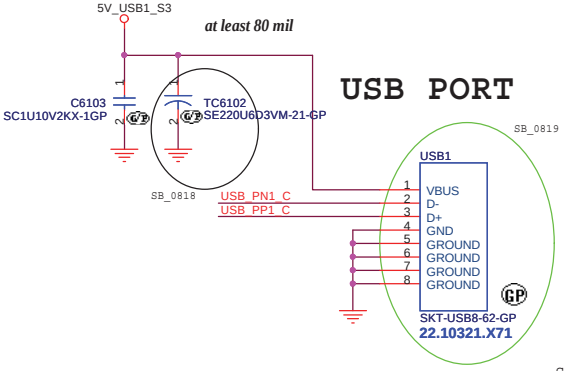
Date: Tuesday, September 07, 2010 Sheet 81 of 103

IO Board CONN 80 pin

USB1



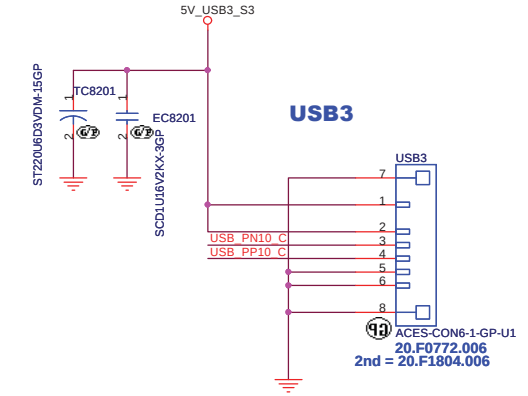




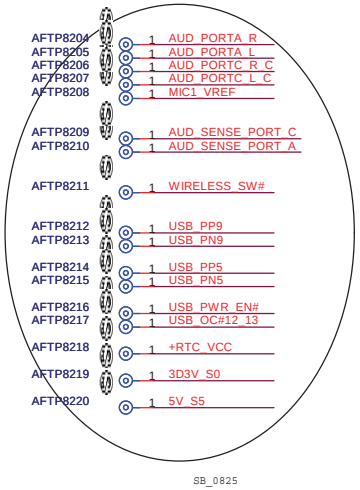
USB PORT

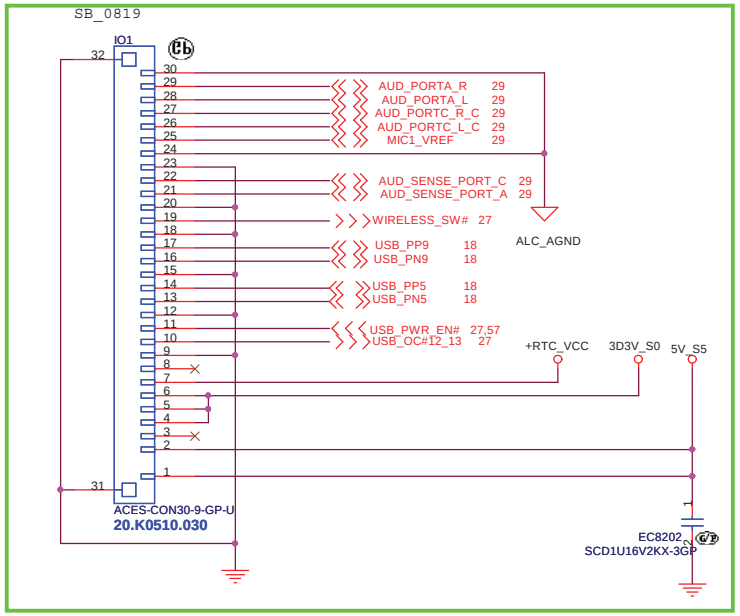
Mars:
Exchange ODD and ESATA differential pair each other.

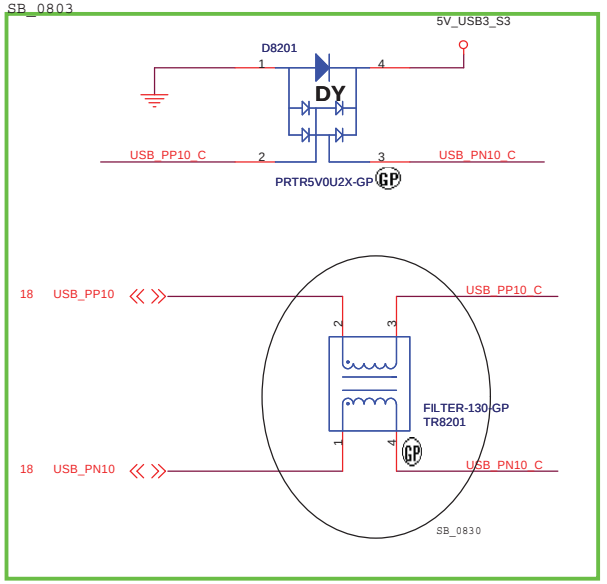
USB Board CONN.

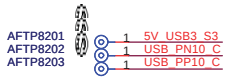


I/O Board CONN.









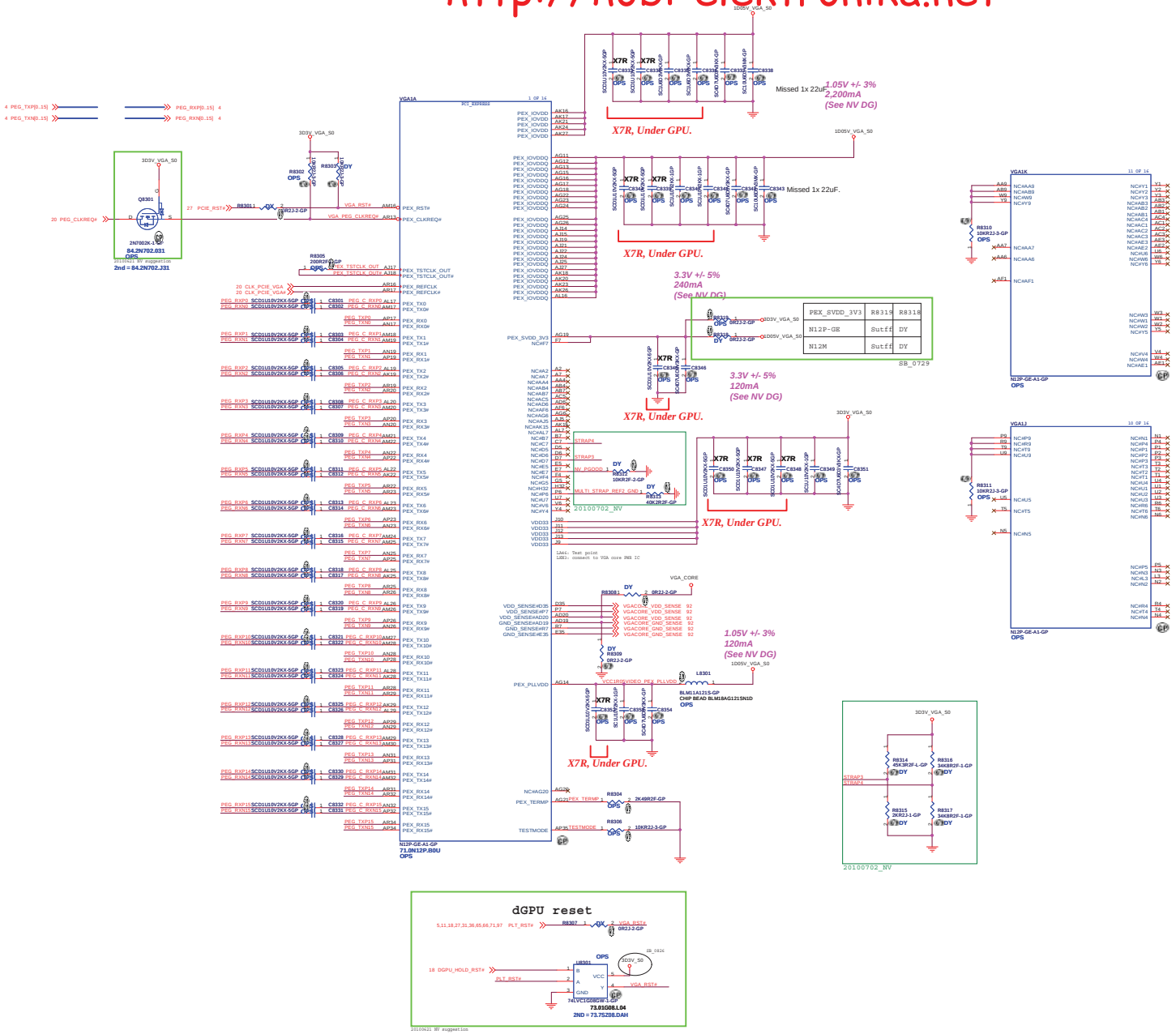
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 82 of 103



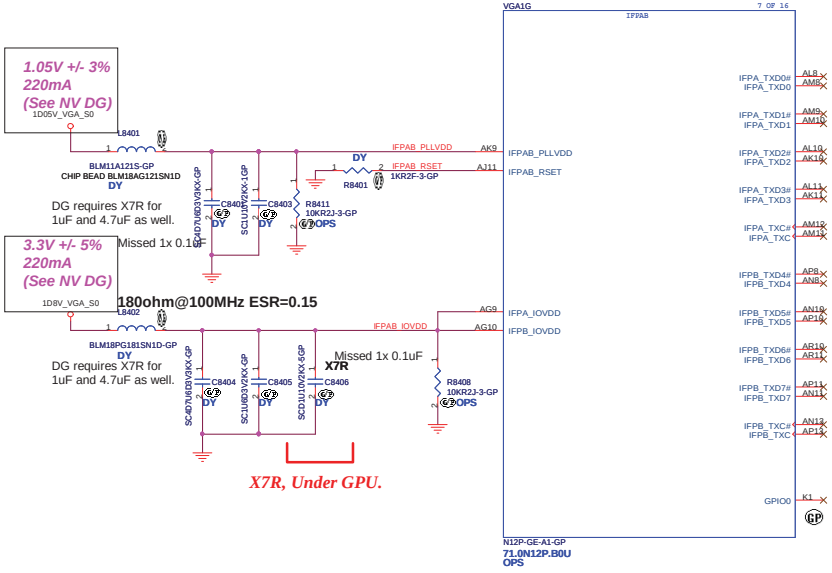
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

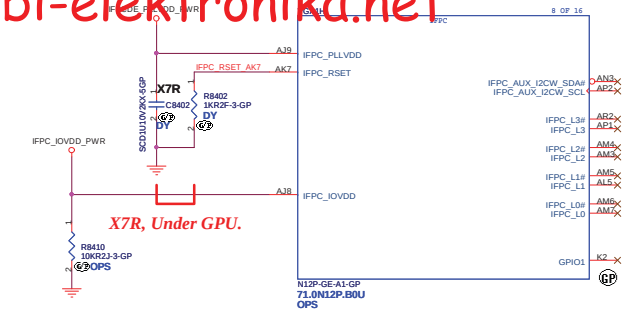
Title: N12P-GE(1/6): PEG I/F

Size	Document Number	Rev
D	LA470	SB

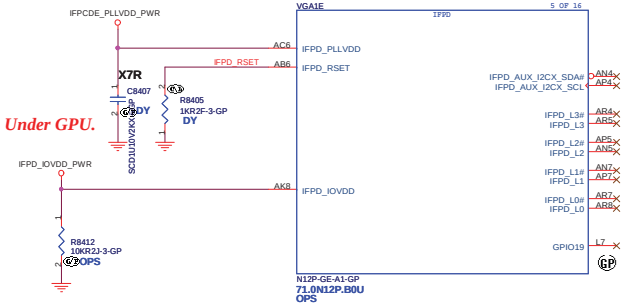
Date: Tuesday, September 07, 2010 Sheet 83 of 103

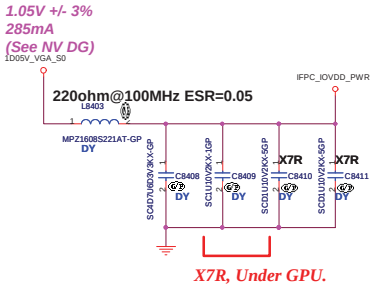
LVDS Interface

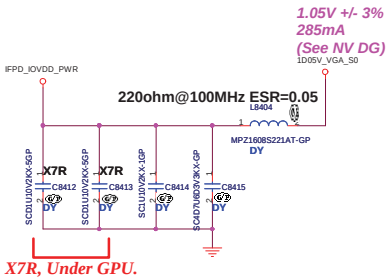


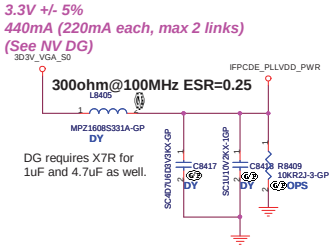


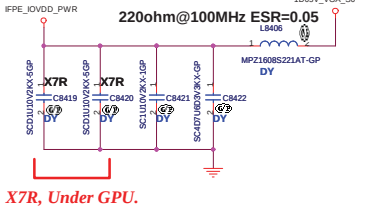
HDMI Interface

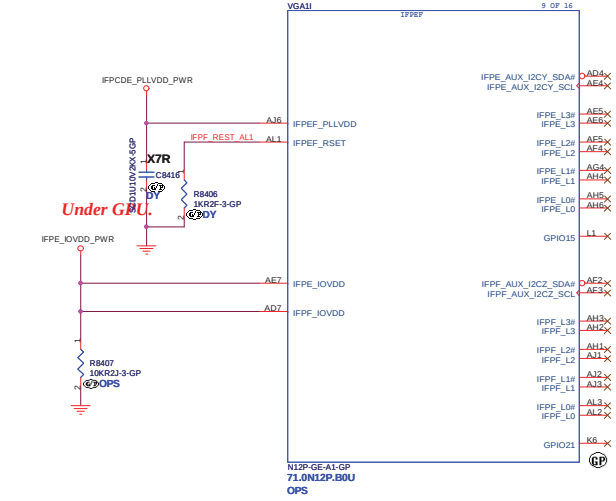












<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N12P-Q1/Q3 (2/6): DIGITAL OUT

Size	Document Number	Rev
A2	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 84 of 103

EDR 20A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz

1.05V +/- 3%
200mA
(See NV DG)

X7R, Under GPU.

X7R, Near GPU.

X7R, Under GPU.

20100702_Change to Mode E

FBCLK Termination place on VRAM side

FBCLK Termination	R8504-R8507
N12P	Stuff 162 ohm 64.16205.DIL
N12M	Stuff 243 ohm 64.24305.DIL

FBCLK Termination place on VRAM side

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N12P-Q1/Q3 (3/6): VRAM I/F

Size: A1 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 85 of 103

3.3V +/- 5%
120mA
(See NV DG)

300ohm@100MHz ESR=0.25ohm

Missed 3x 0.1uF

X7R, Under GPU.

1.05V +/- 5%
150mA
(See NV DG)

X7R, Under GPU.

Should be placed near GFX

Should be placed near GFX

HARMORY 27MHz
12P 30PPM
HSX530G

I2CA=>CRT, I2CC=>LVDS.

TABLE
VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
	72.52G63.00U ~~72.52G63.A0U~~	72.42164.C0U ~~72.42164.D0U~~	72.51G63.C0U	72.41164.H0U
ROM_SIPD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

LOGIC

TABLE
NVIDIA

	N12P-GE DEV ID: 0xDF5 0101	N12P-GV1 DEV ID: 0x0DF7	N12M-GE DEV ID: 0xA7A 1010
STRAP2	PD R8635 30Kohm 64.30025.6DL	PD R8635 45Kohm 64.45325.6DL	PU R8634 15Kohm 64.15025.6DL

P-State	PWRCNTL_0	PWRCNTL_1	VGA_CORE_PWR
P8 & P12	0	0	0.85V
ES	1	0	0.90V
P0(Hot)	0	1	0.95V
P0(Cold)	1	1	1.00V

P-State	N12P-GE	N12P-GV1	N12M-GE	N12P-GV
NVVDD Boot Voltage	0.95V	0.90V	0.85V	TBD

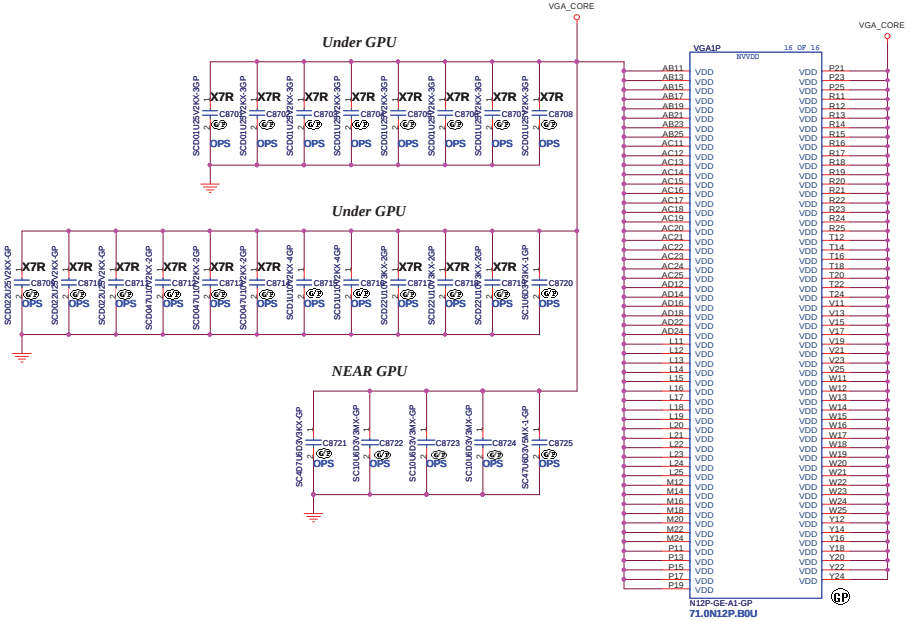
<Core Design>

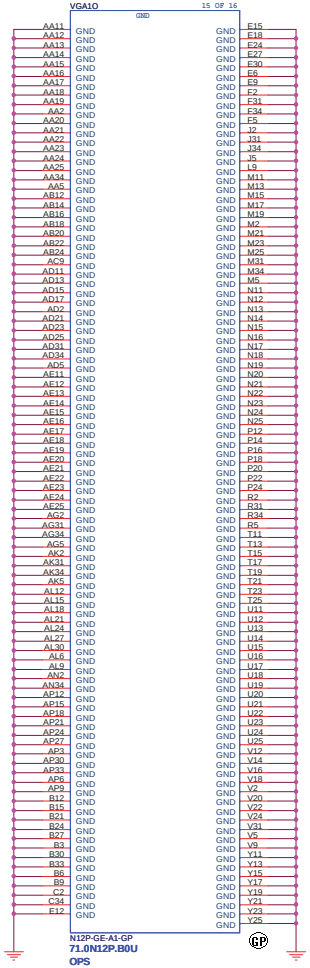
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N12P-Q1/Q3 (4/6): GPIO

Size	Document Number	Rev
A1	LA470	SB

Date: Tuesday, September 07, 2010 | Sheet 86 of 103





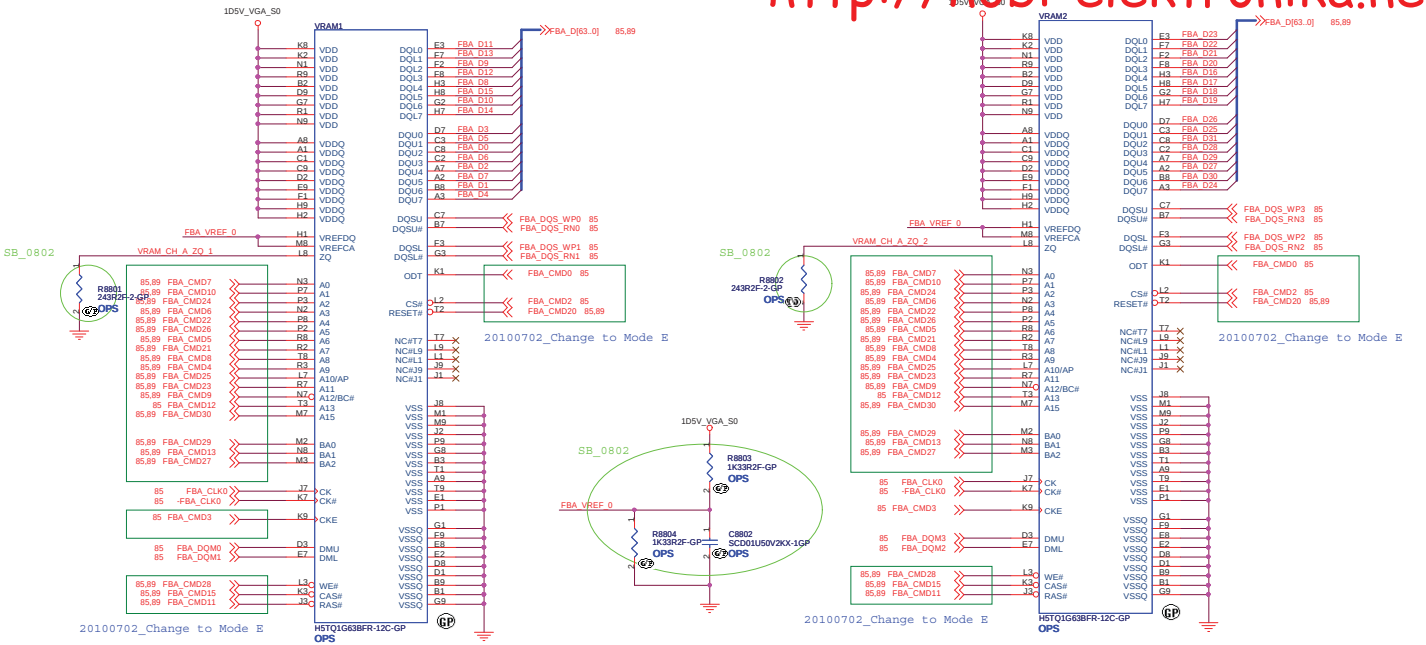
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

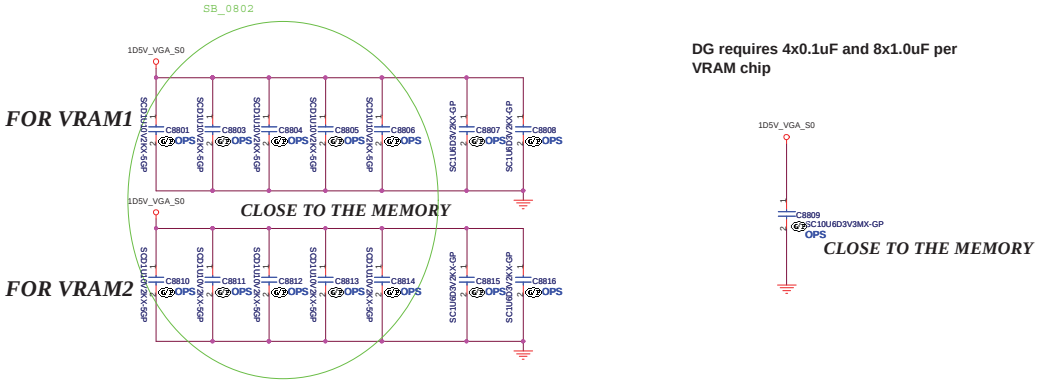
Title: N12P-Q1/Q3 (5/6): POWER

Size	Document Number	Rev
A2	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 87 of 103



FB CMD mapping Mode D-N12x



DG requires 4x0.1uF and 8x1.0uF per VRAM chip

CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

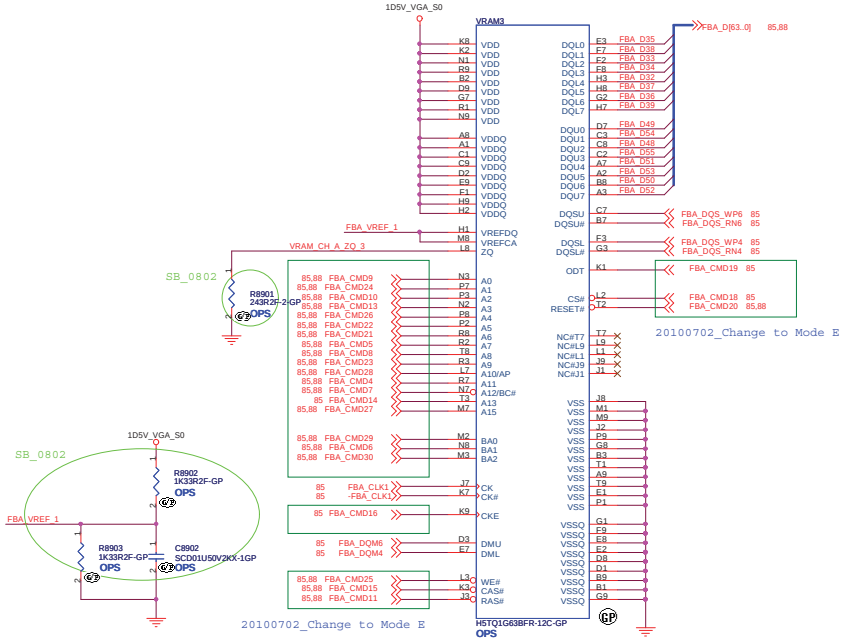
<Core Design>

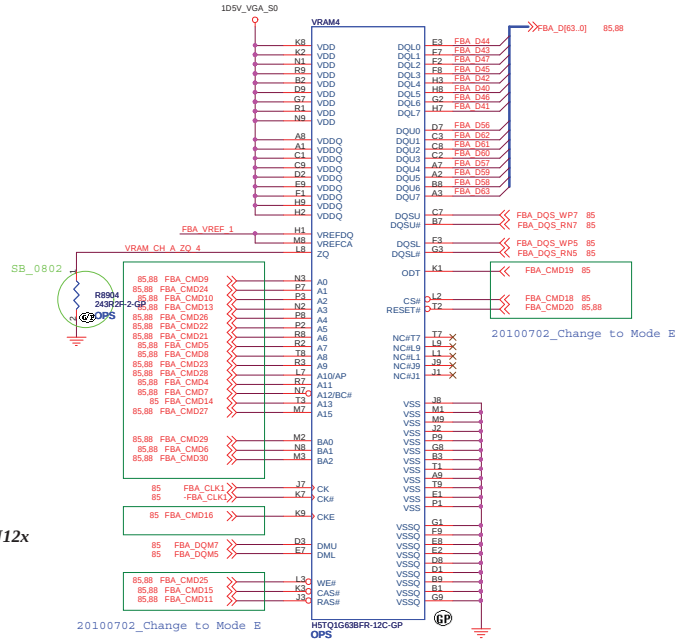
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM CHANNEL-A

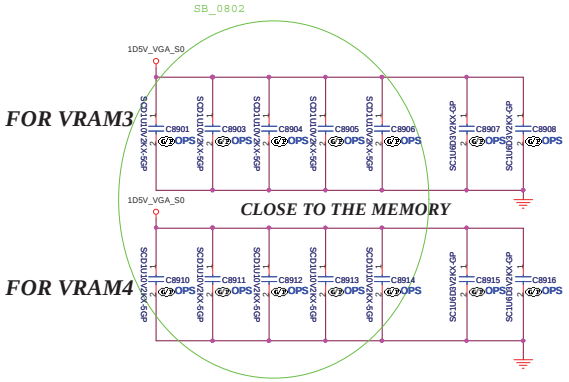
Size	Document Number	Rev
A2	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 88 of 103





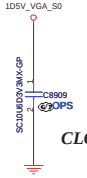
FB CMD mapping Mode D-N12x



FOR VRAM3

CLOSE TO THE MEMORY

FOR VRAM4



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

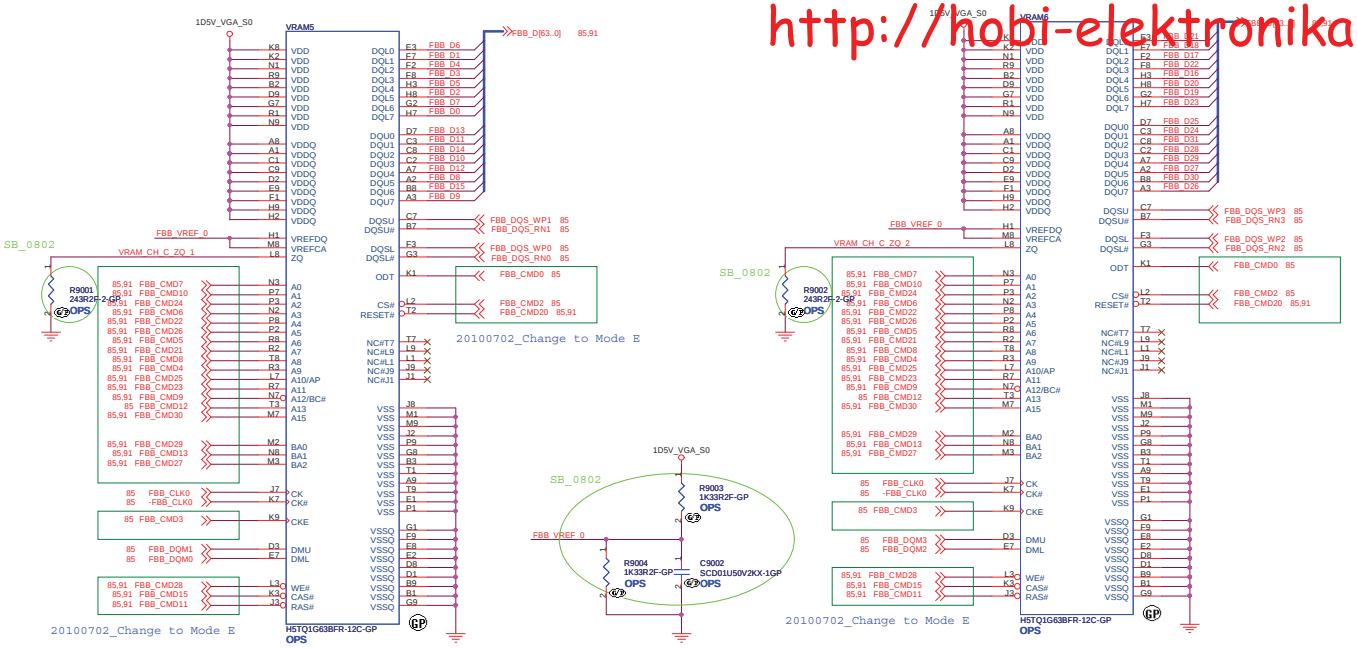
<Core Design>

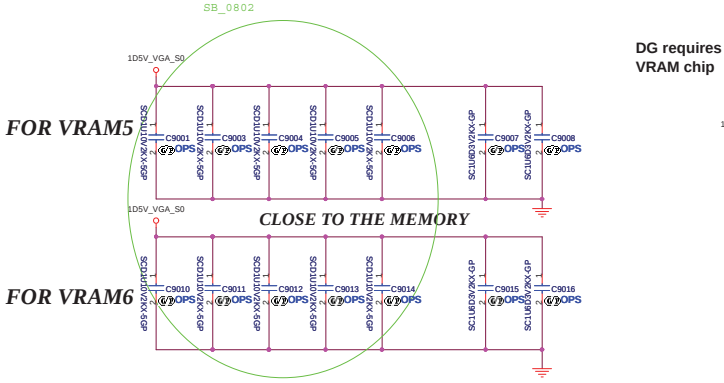
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM CHANNEL-A

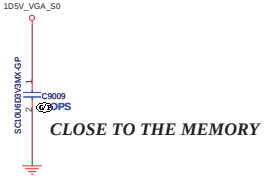
Size: A2 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 89 of 103





DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT C

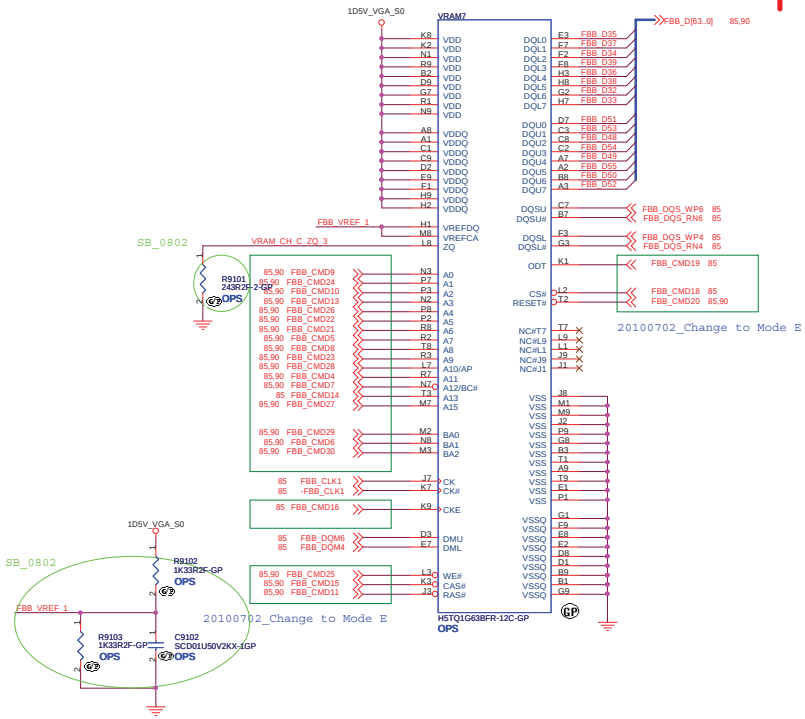
<Core Design>

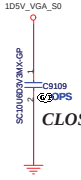
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM CHANNEL-C***

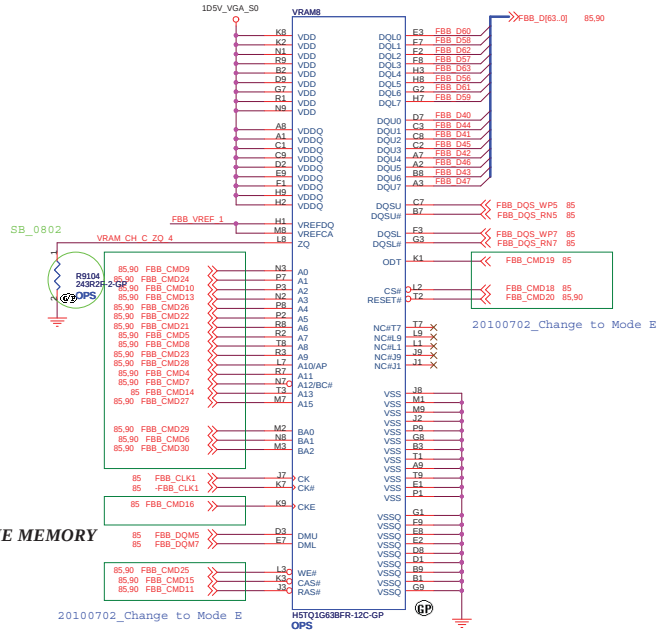
Size	Document Number	Rev
A2	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 90 of 103

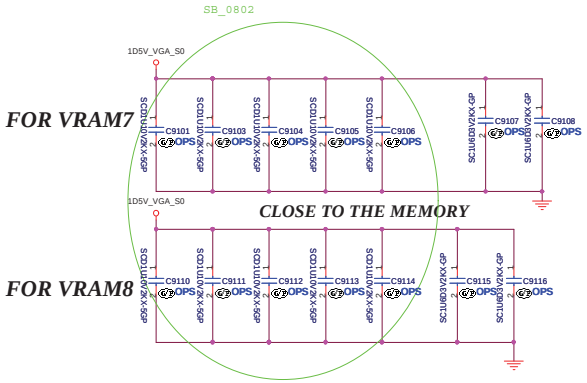




CLOSE TO THE MEMORY



CLOSE TO THE MEMORY



VIDEO FRAME BUFFER PORT C

<Core Design>

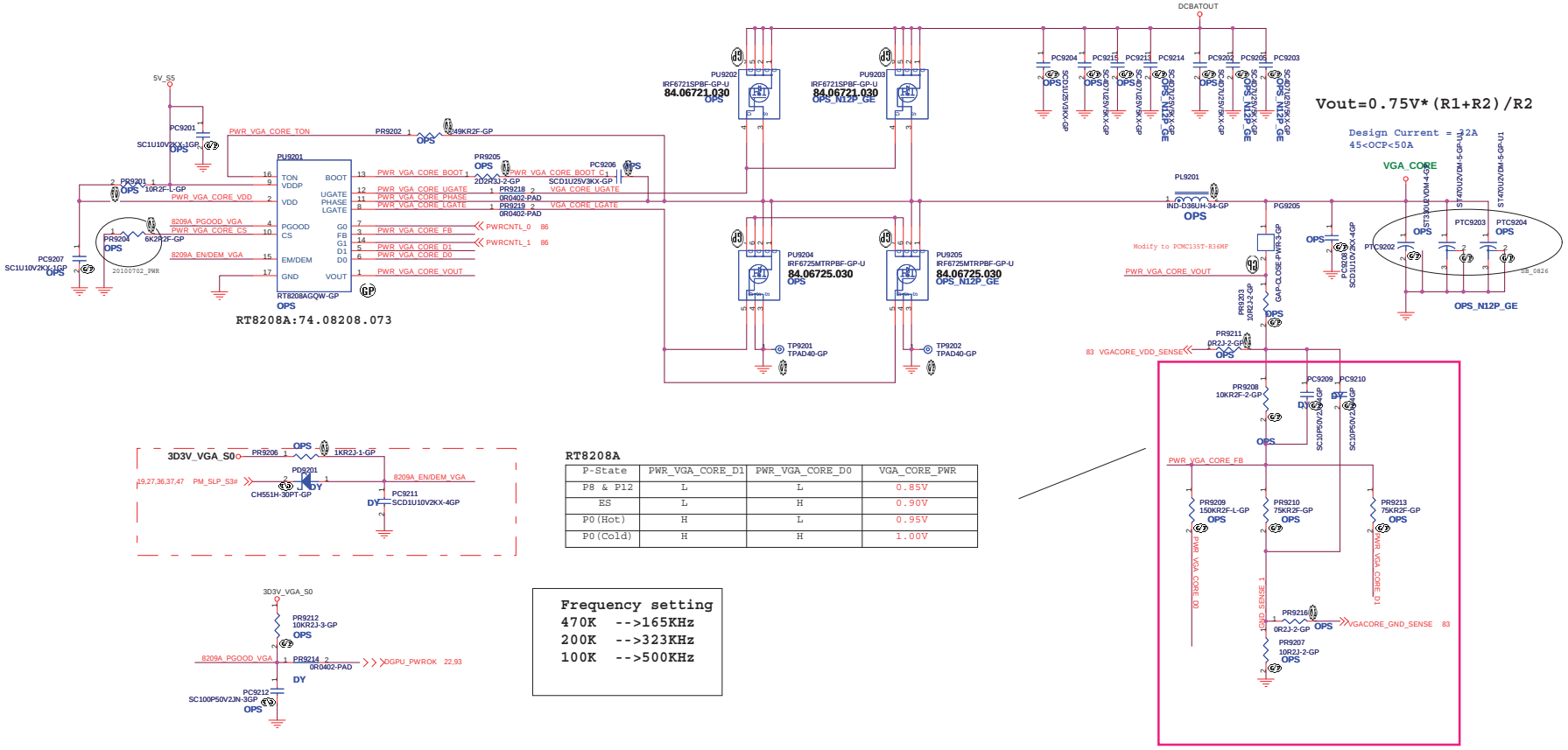
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM CHANNEL-C**

Size	Document Number	Rev
A2	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 91 of 103

SSID = PWR.Plane.Regulator_GFX



RT8208A

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 & P12	L	L	0.85V
ES	L	H	0.90V
P0(Hot)	H	L	0.95V
P0(Cold)	H	H	1.00V

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

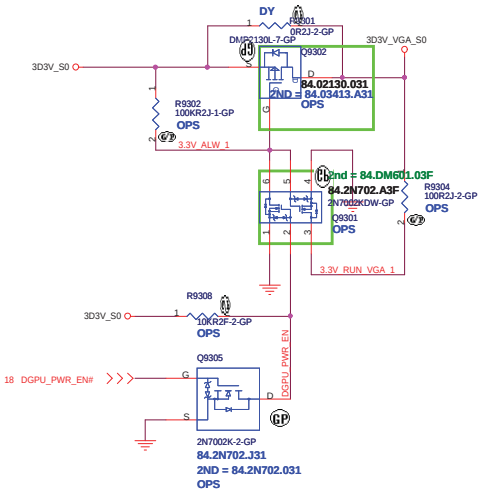
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC_VGA CORE_RT8208A

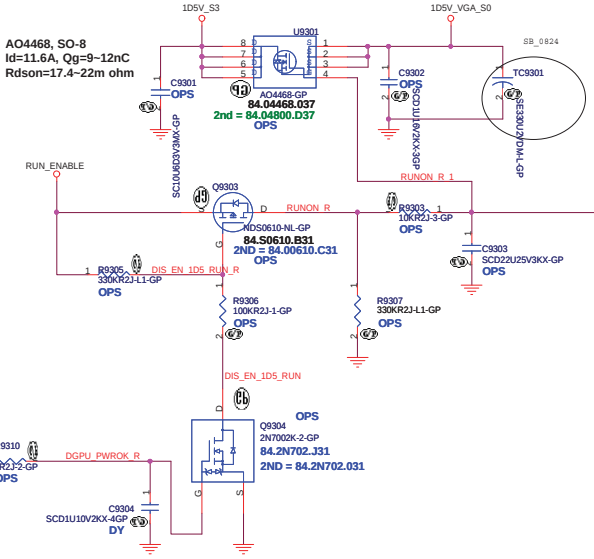
Size: | Document Number: LA47 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 92 of 103

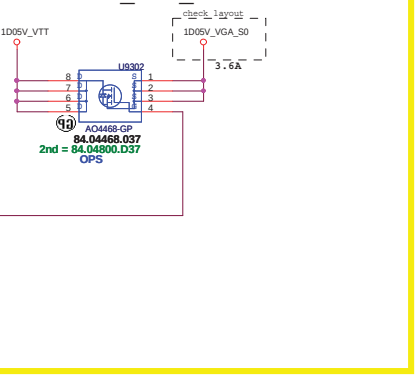
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

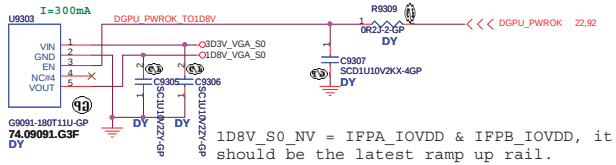


1.05V to 1.05V_VGA_S0 Transfer



20100707

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DISCRETE VGA POWER	
Size	Document Number LA470	Rev SB
Date: Tuesday, September 07, 2010	Sheet 93 of 103	

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS Switch

Size: A2 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 94 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT_Switch

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 95 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
TOUCH PANEL

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 96 of 103

CPU Plate

H1 HOLE276R178-GP — ZZ.00PAD.N11
H2 HOLE276R178-GP — ZZ.00PAD.N11
H3 HOLE276R178-GP — ZZ.00PAD.N11

VGA Std-Off

H4 STF237R128H42-1-GP — 34.4GD01.001
H5 STF237R128H42-1-GP — 34.4GD01.001

Structure boss

H7 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H8 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H9 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H10 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H11 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H12 HOLE256R115-GP — ZZ.00PAD.D11
H13 HOLE256R115-GP — ZZ.00PAD.D11
H15 HOLE256R115-GP — ZZ.00PAD.D11

MiniPCI Std-Off

H14 STF237R113H115-GP — 34.4V802.101

Check test point

3D3V_S0	1	AFTP1
3D3V_AUX_S5	1	AFTP7
3D3V_S5	1	AFTP8
5V_S5	1	AFTP9
11,19,27 PM_PWRBTN#	1	AFTP10
5,11,22,36 H_CPUPWRGD	1	AFTP11
27,36 S5_ENABLE	1	AFTP12
5,11,18,27,31,36,65,66,71,83 PLT_RST#	1	AFTP13

Test Point放在Dimm Door打開可量測處

AD+

EC9702 DY SCD1U25V2KX-GP
EC9703 DY SCD1U25V2KX-GP
EC9704 DY SCD1U25V2KX-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: LA470 | Rev: SB
Date: Tuesday, September 07, 2010 | Sheet 97 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

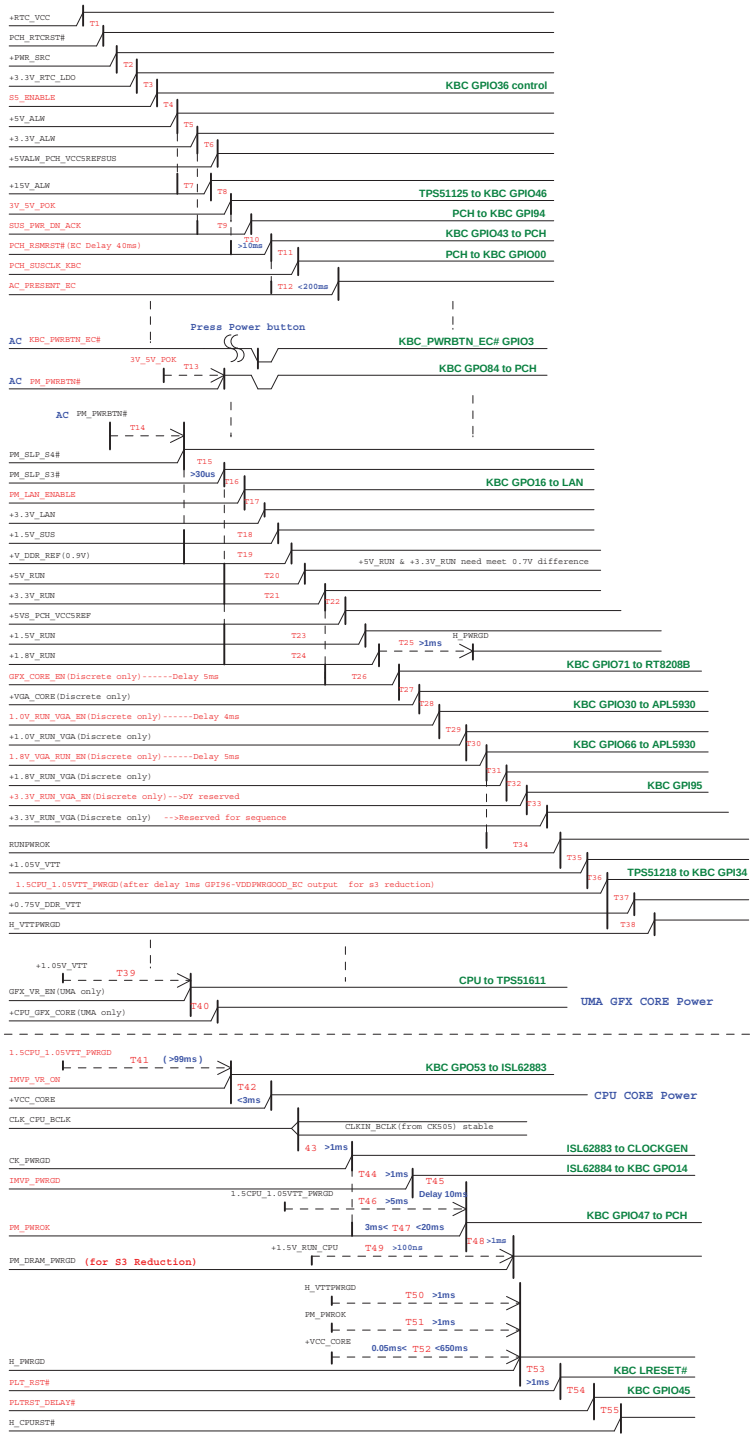
Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 98 of 103

Intel-Power Up Sequence

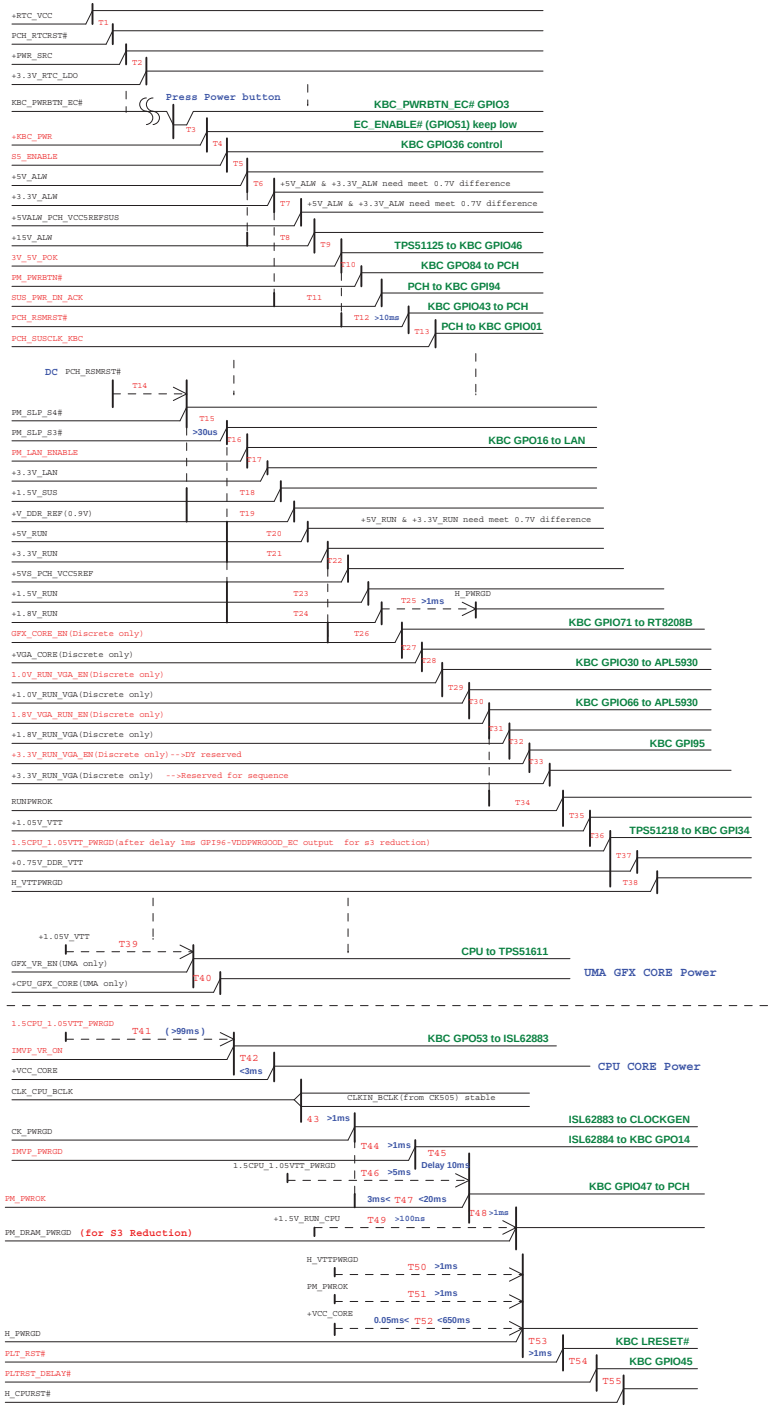
(AC mode)

red word: KBC GPIO

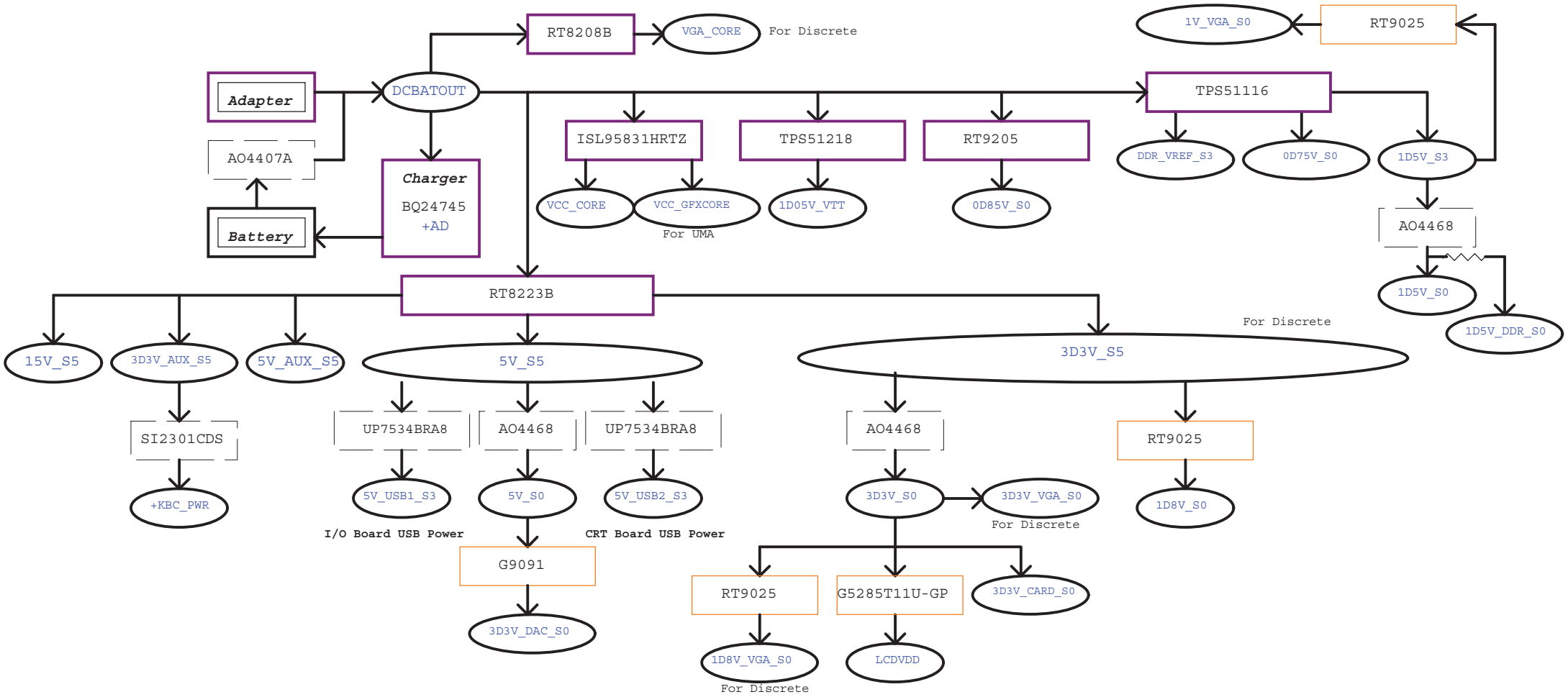


(DC mode)

red word: KBC GPIO



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: Power Sequence
Size: A3 | Document Number: LA470 | Rev: SB
Date: Tuesday, December 19, 2006 | Sheet 38 of 39



Power Shape

Regulator	LDO	Switch

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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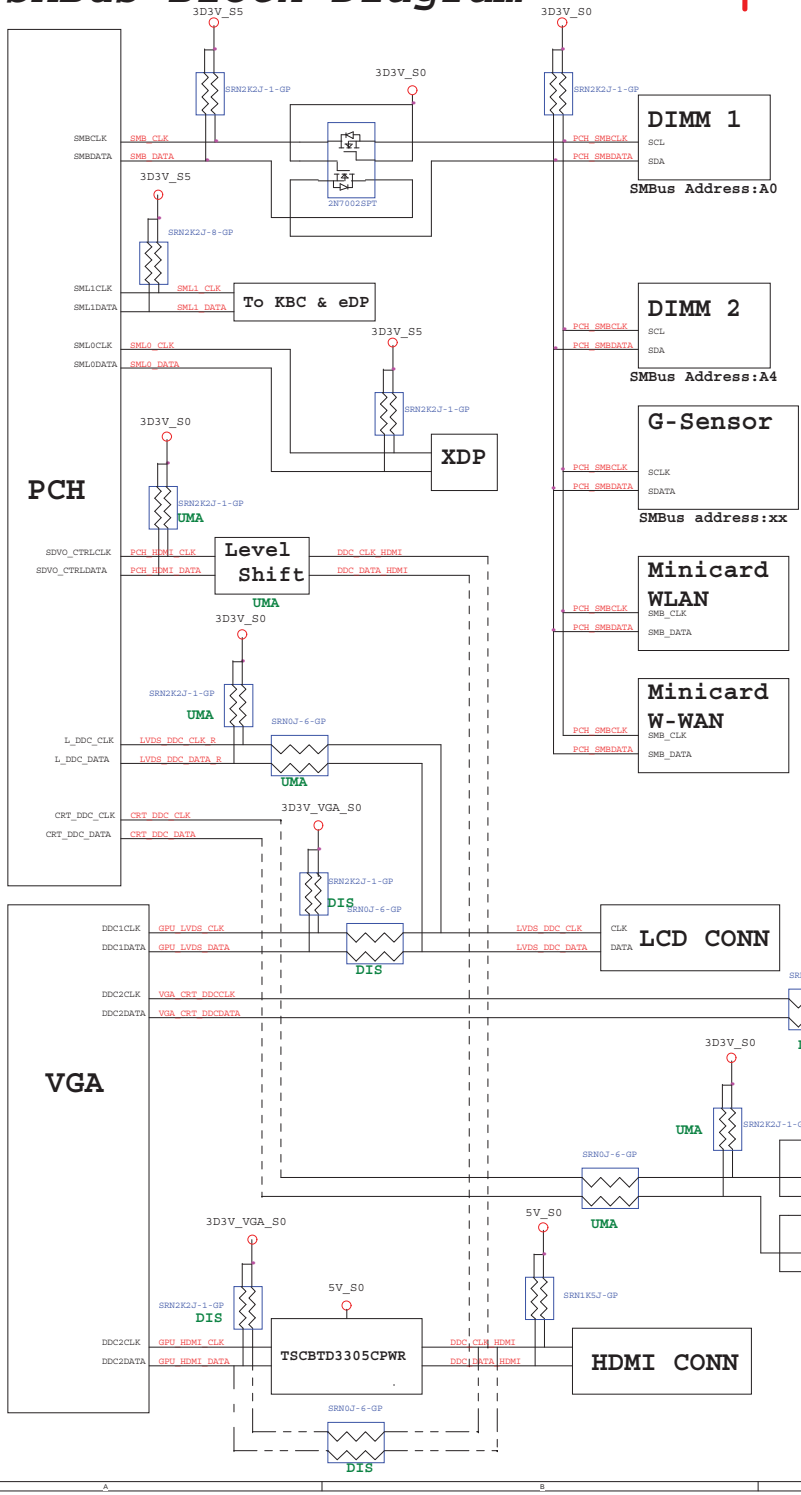
Title: ***Power Block Diagram***

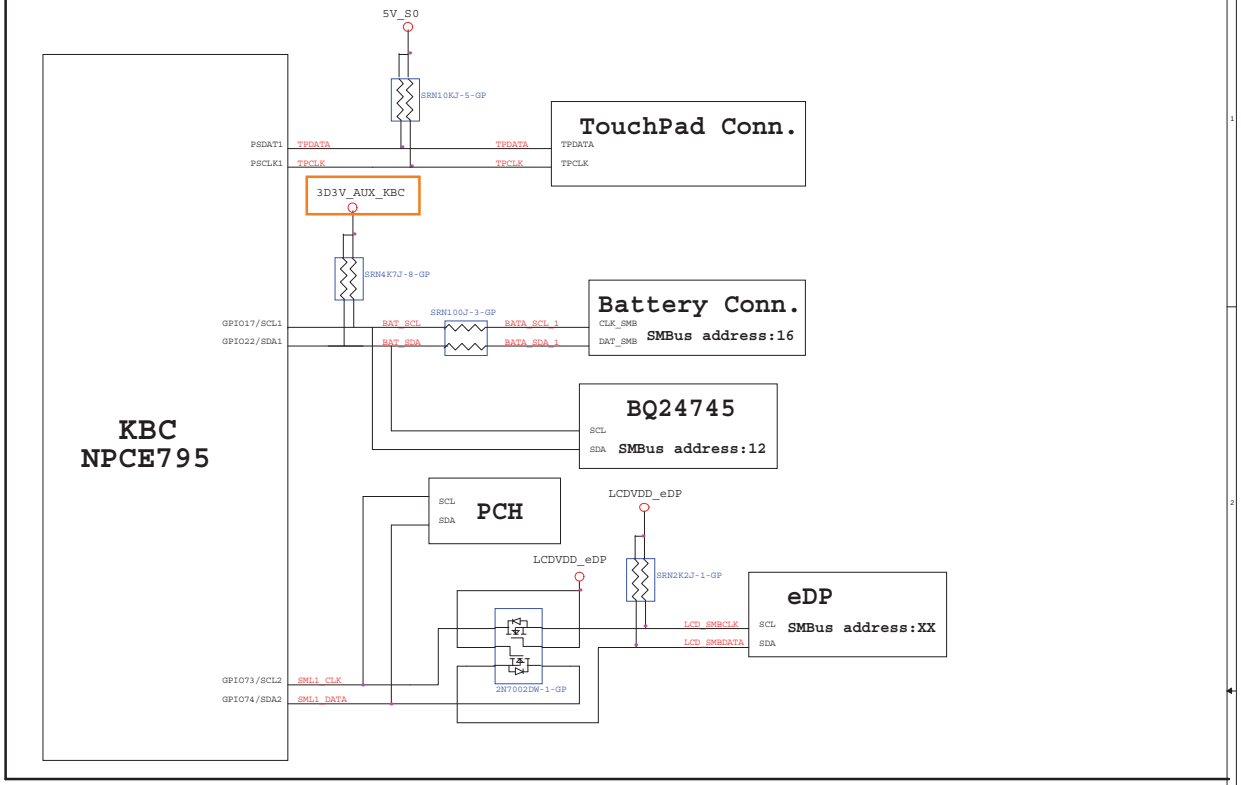
Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 100 of 103

PCH SMBus Block Diagram



KBC SMBus Block Diagram



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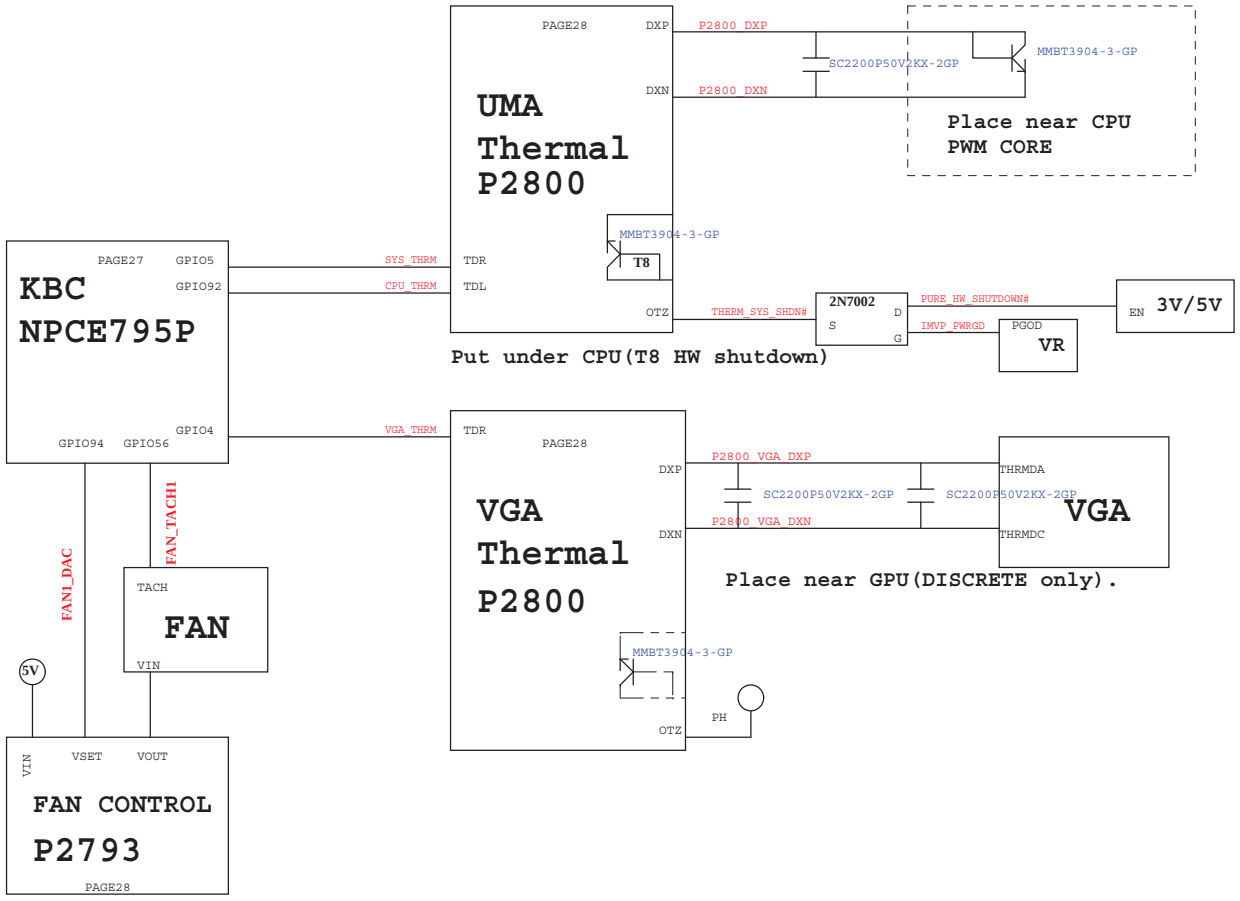
Title: SMBUS Block Diagram

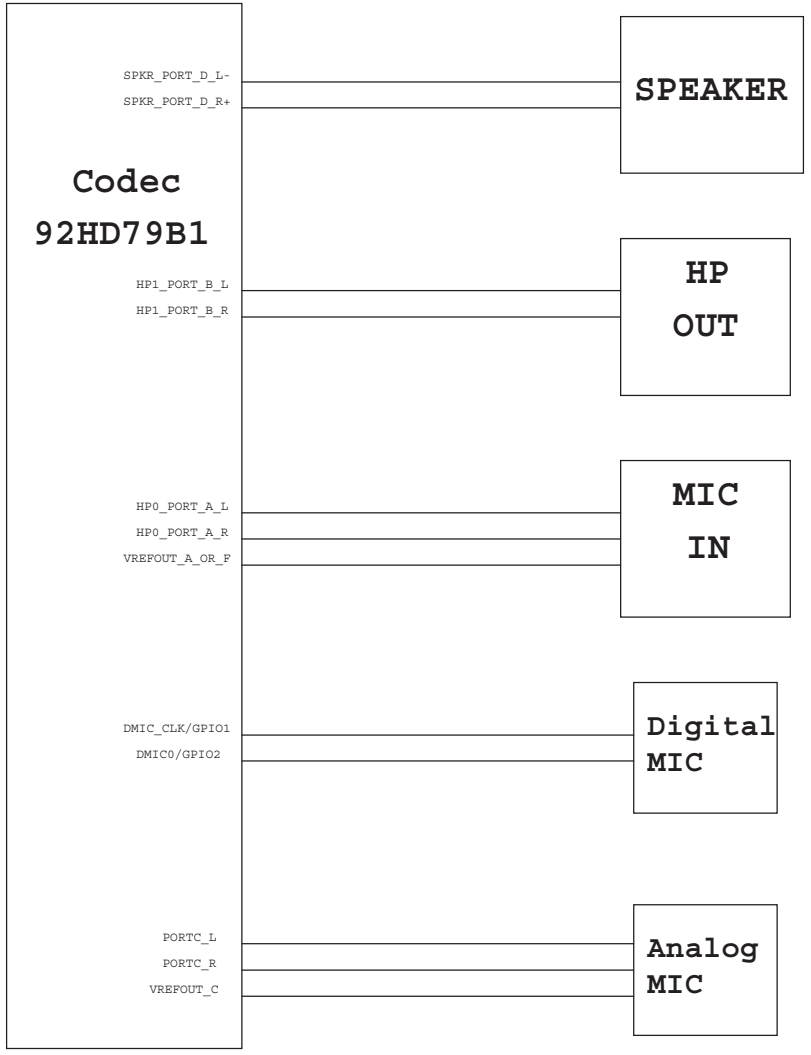
Size	Document Number	Rev
A2	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 101 of 103

Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 102 of 103

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Title: *Change History*

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 103 of 103