

Lindbergh Schematic Document

uFCPGA Northwood

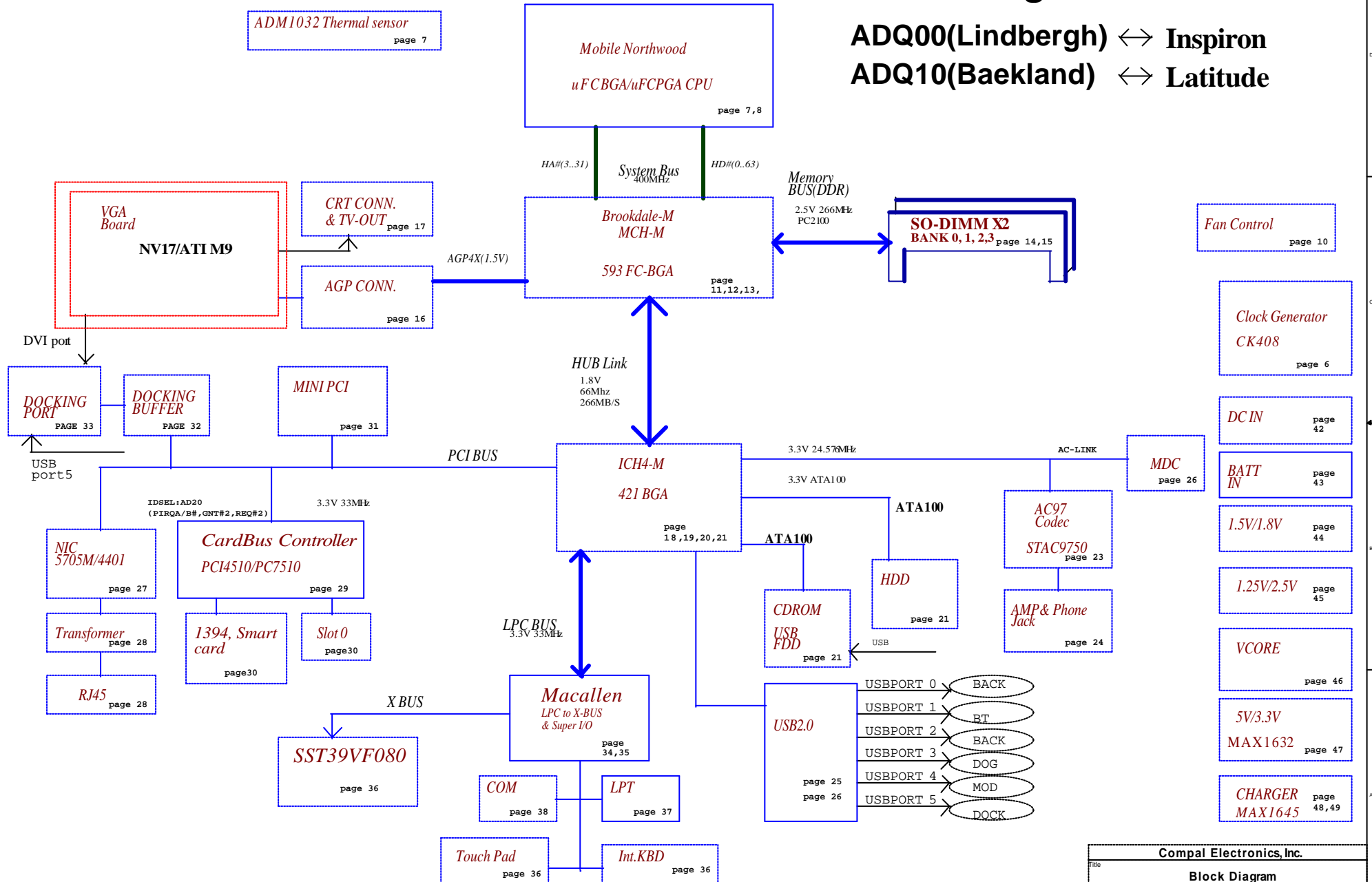
2002-10-23

Rev:X025

Compal Electronics, Inc.		
Title	Cover Sheet	
Size	Document Number	Rev
	ADQ00/LA-1351	X025
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Block Diagram

ADQ00(Lindbergh) ↔ Inspiron
 ADQ10(Baekland) ↔ Latitude



PM TABLE

power plane State	+3VALW +5VALW	+3VSRC +3VSUS +5VSUS +2.5VSUS +1.8VSUS +1.5VSUS +12V	+3VRUN +5VRUN +1.8VRUN +1.5VRUN +VCC_CORE
s0	ON	ON	ON
s1	ON	ON	ON
s3	ON	ON	OFF
s5 s4/AC	ON	OFF	OFF
s5 s4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCIDEVICE	IDSEL	REQ#/GNT#
CARDBUS	AD17	1
LAN	AD16	4
DOCK	AD24	0
MINIPCI	AD19	3

USB TABLE

USB PORT#	DESTINATION
0	BACK
1	BLUETOOTH
2	BACK
3	DOG
4	MOD
5	DOCK

BOM Structure:

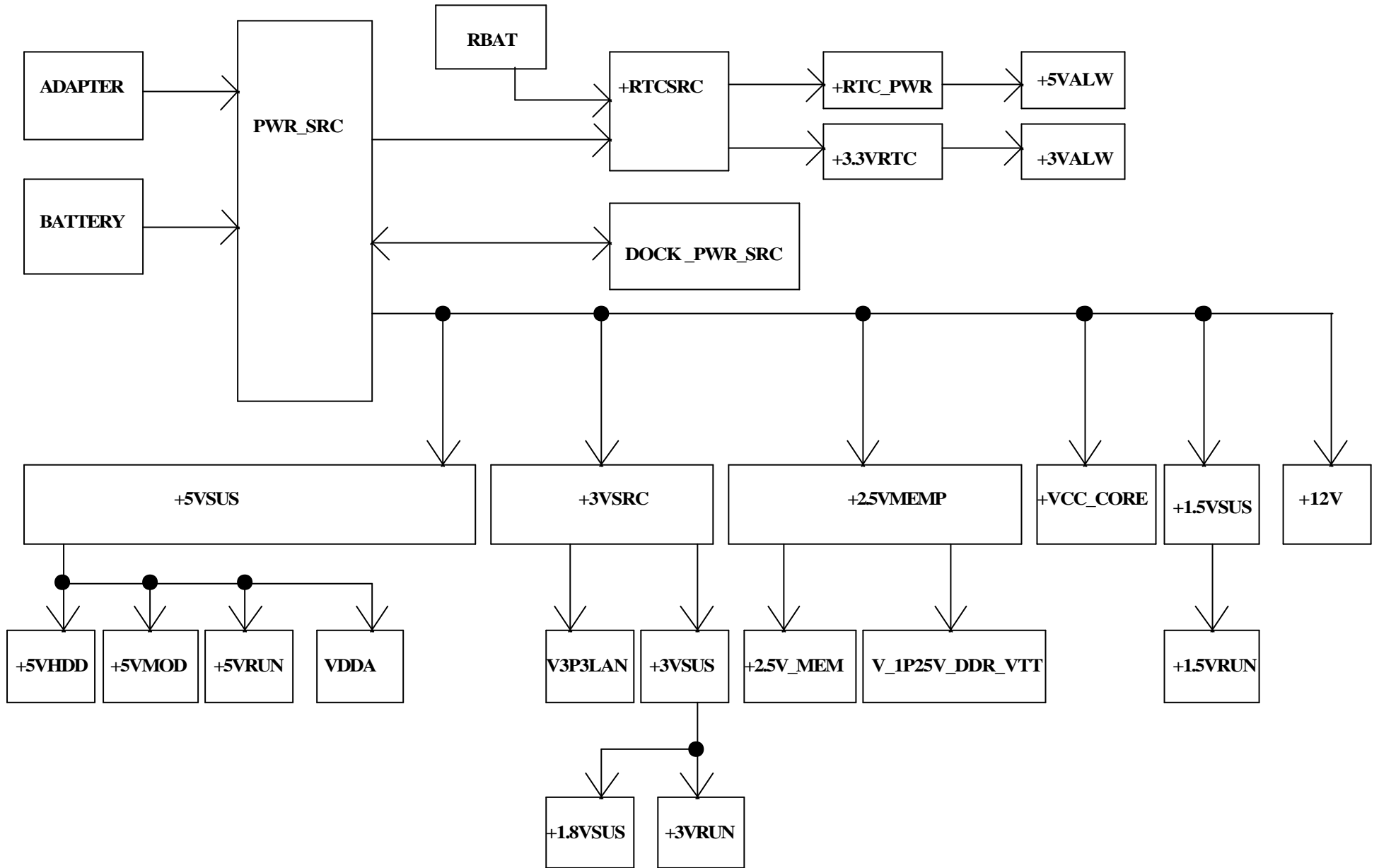
Backland- 43122231001, with 1@

Lindbergh- 43122231002, with 2@

Note: "@" means all model depop
 "?" means Kapalua pop only (ie Lindbergh depop)
 "#" means Lindbergh pop only (ie baekland depop)

Configuration List

BOM Structure		
Function	Lindbergh	Kapalua \ Baekland



Compal Electronics, Inc.			
Title			
Power Rail			
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ICH4-M

ICH_SMBCLK

ICH_SMBDATA

DIMM0

DIMM1

+3VRUN

CK_SCLK

CLK GEN.

CK_SDATA

V_3P3_LAN

LAN_SMBCLK

NIC

LAN_SMBDATA

MPCI

SIO
Macallen

CLK_SMB

DAT_SMB

24C05

ADM1032

DH PORT

DOCK_SMB_CLK

DOCK_SMB_DAT

DOCKING

SBAT_SMBCLK

SBAT_SMBDAT

2'nd BATTERY

VGA
Inverter & ADM1032

PBAT_SMBCLK

PBAT_SMBDAT

1'nd BATTERY

CHARGER

+3VALW

+5VALW

+5VALW

+5VALW

+3VSUS

7002

7002

7002

7002

7002

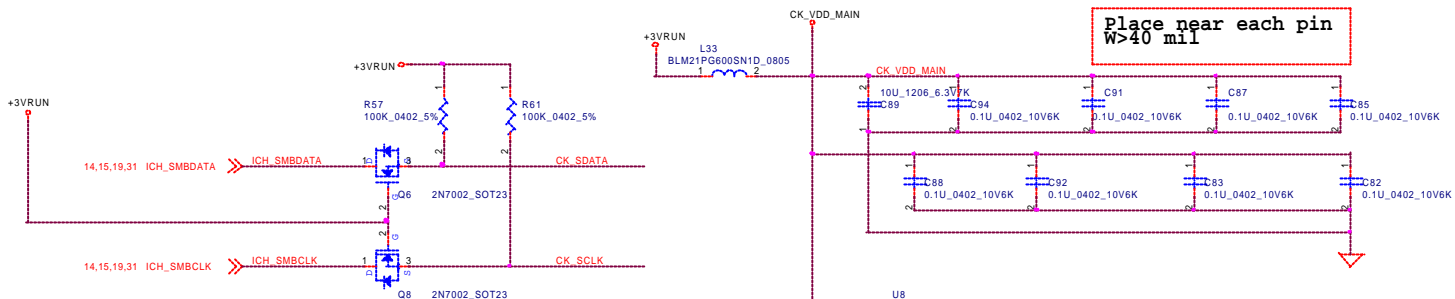
7002

7002

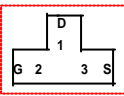
7002

Compal Electronics, Inc.

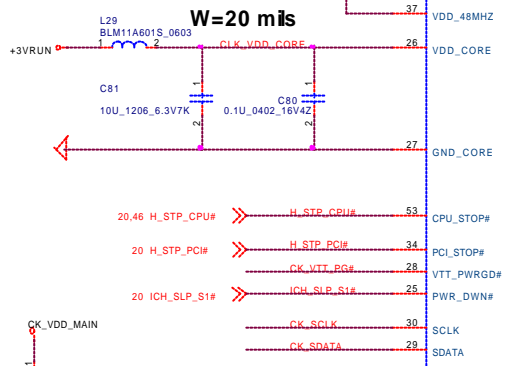
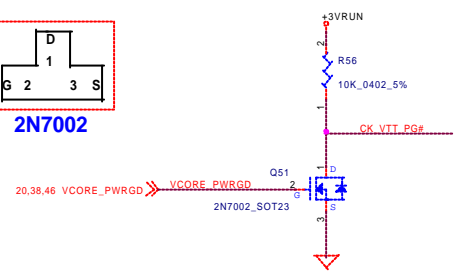
Title			SMBUS TOPOLOGY		
Size	Document Number	Rev			
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Place near each pin
W>40 mil

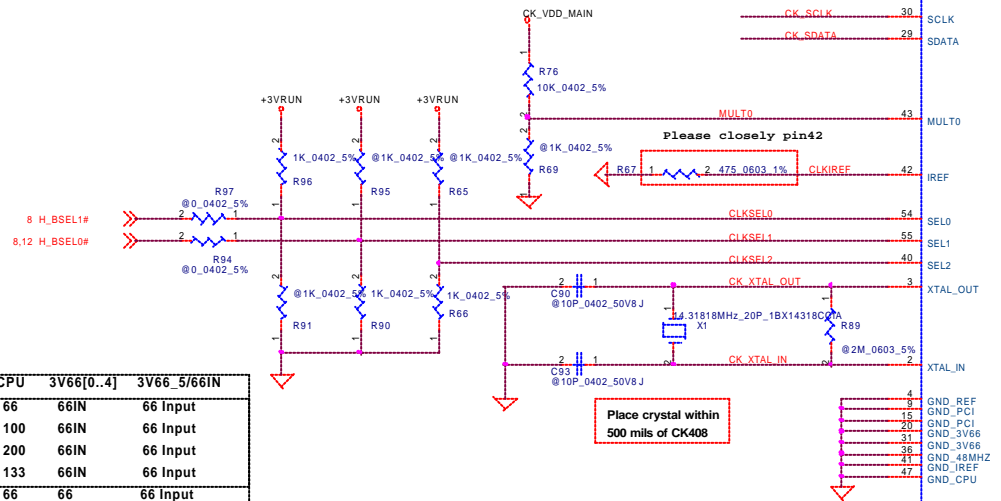


2N7002



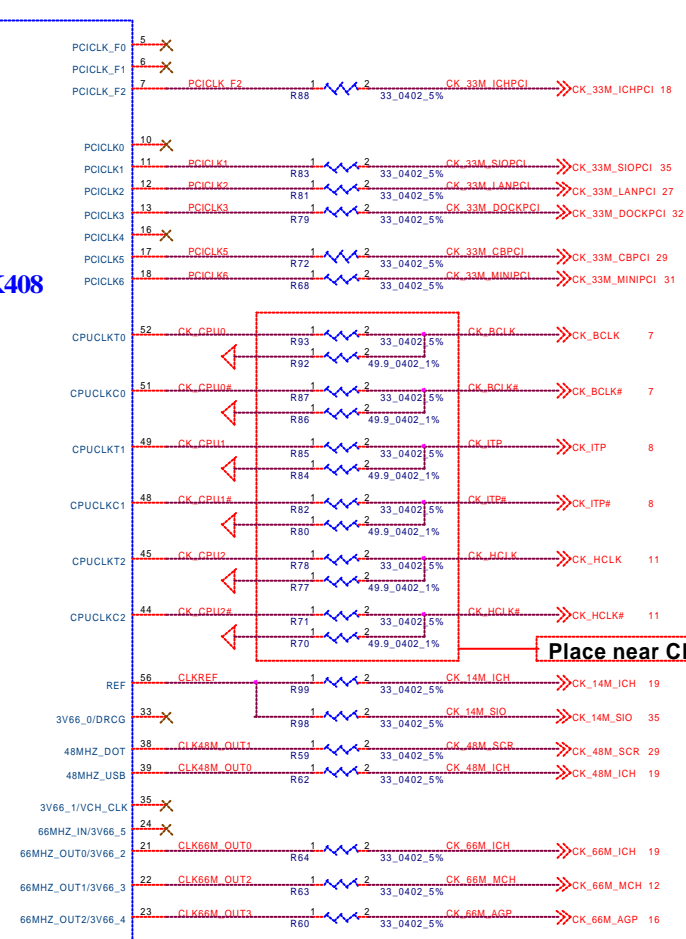
W=20 mils

CK408



Please closely pin42

Place crystal within
500 mils of CK408



Place near CK408

S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
0	0	1	100	66	66 Input
0	1	0	200	66	66 Input
0	1	1	133	66	66 Input
Mid	0	0	Hi-z	Hi-z	Hi-z
Mid	0	1	TCLK/2	TCLK/2	TCLK/2
Mid	1	0	Reserve	Reserve	Reserve
Mid	1	1	Reserve	Reserve	Reserve

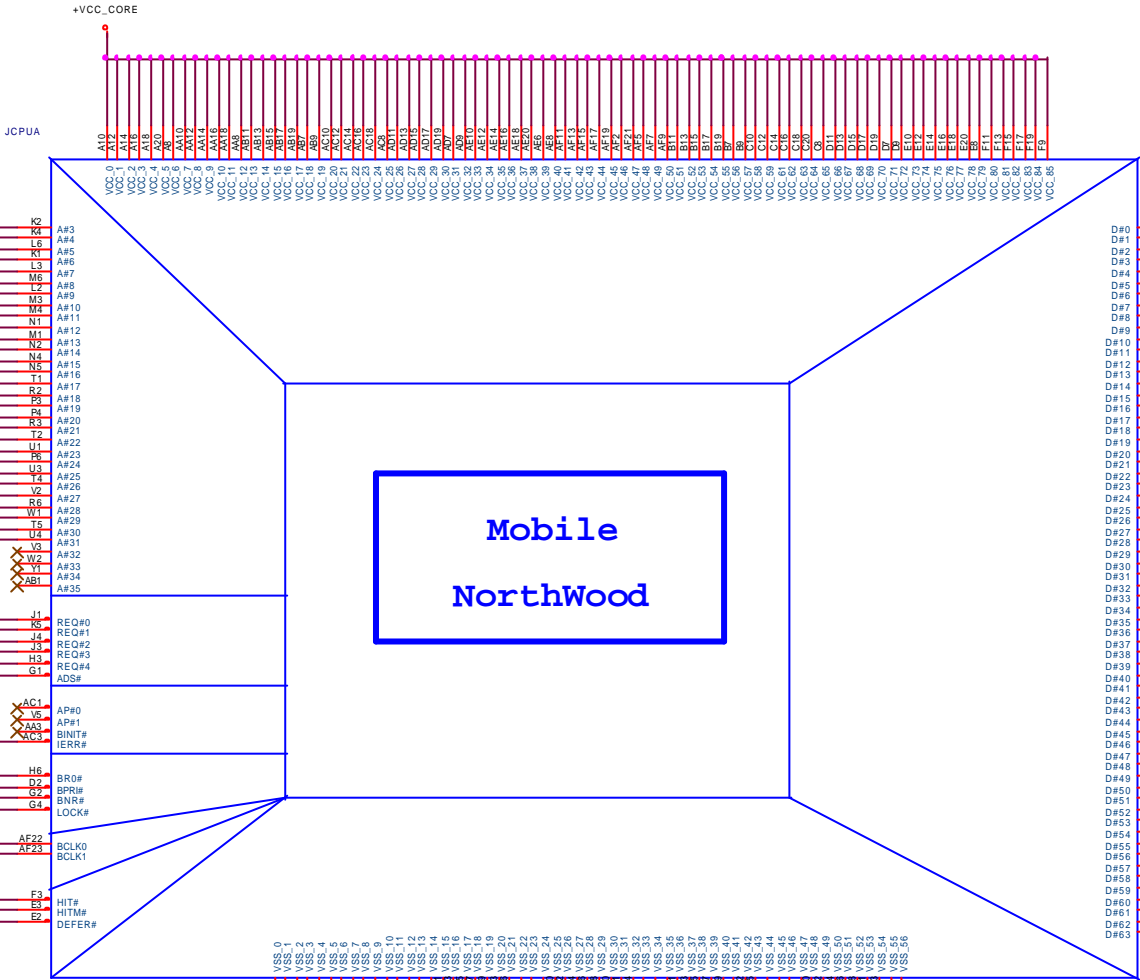
Compal Electronics, Inc.

Clock Generator

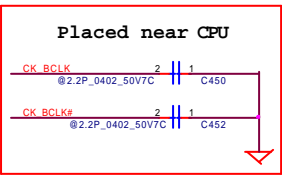
ADQ00/LA-1351

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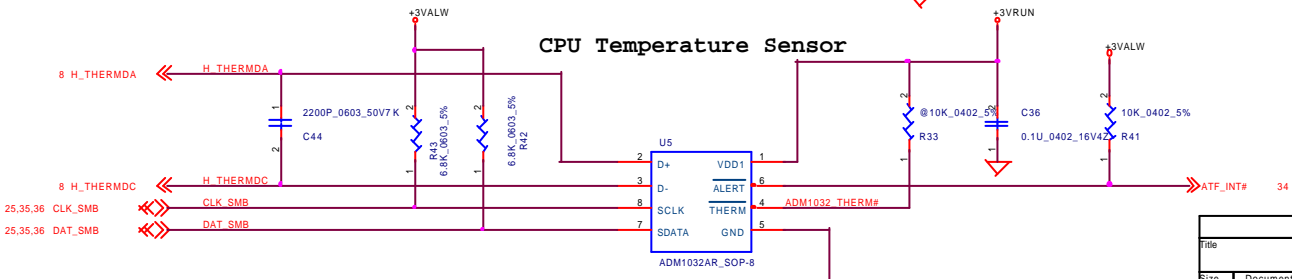
Mobile NorthWood



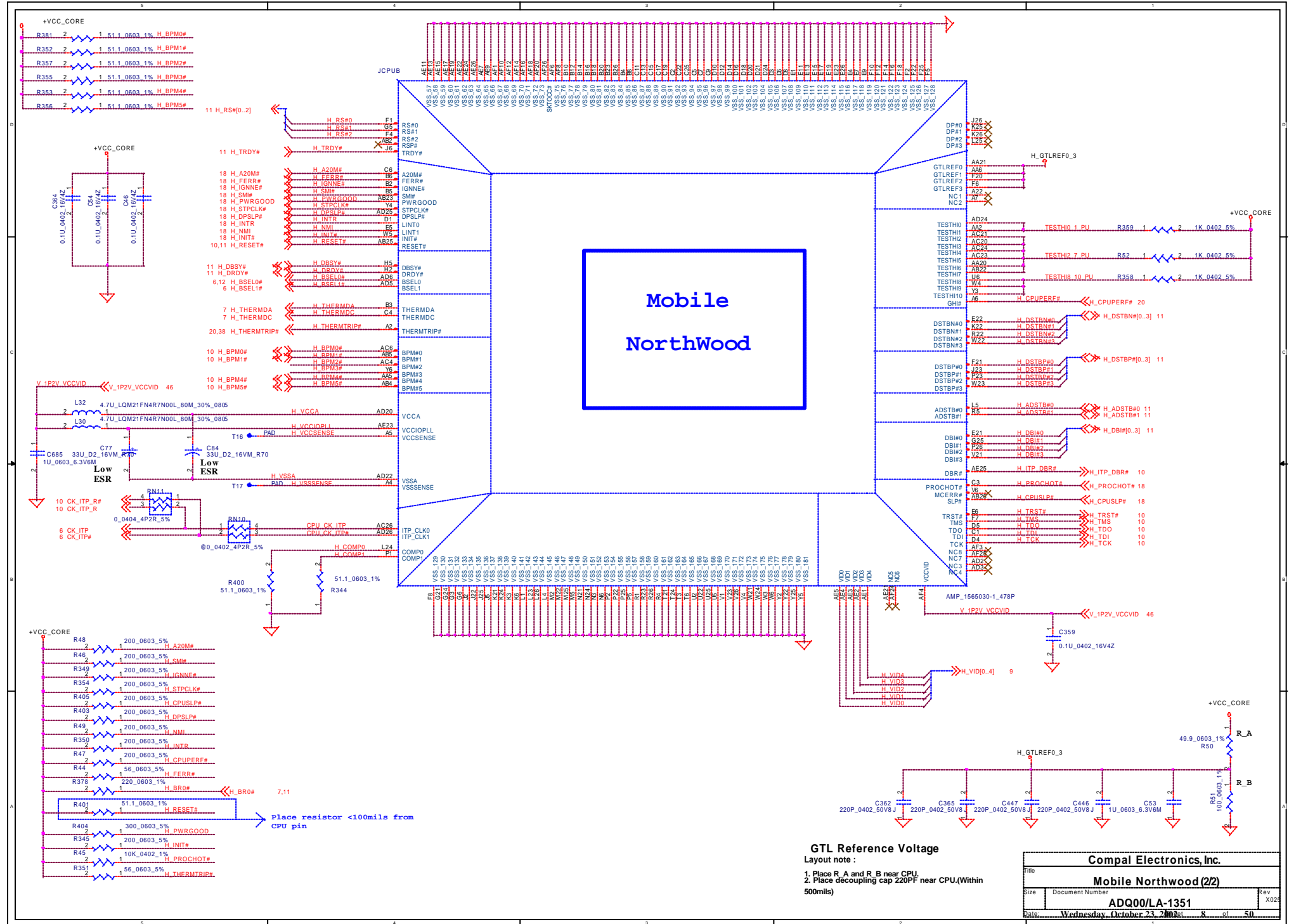
AMP_1565030-1_478P



JCPU DELL P/N changed to IM568(mobil socket)



Mobile NorthWood



11 H_RS#[0..2]

11 H_TRDY#

18 H_A20M#
18 H_FERR#
18 H_IGNNE#
18 H_SM#
18 H_PWRGOOD
18 H_STPCLK#
18 H_DPSP#
18 H_INTR#
18 H_NMI#
18 H_INIT#
10,11 H_RESET#

11 H_DBSY#
11 H_DRDY#
6,12 H_BSEL0#
6 H_BSEL1#

7 H_THERMDA
7 H_THERMDC
20,38 H_THERMTRIP#

10 H_BPM0#
10 H_BPM1#
10 H_BPM4#
10 H_BPM5#

10 CK_ITP_R#
10 CK_ITP_R

6 CK_ITP#
6 CK_ITP#

0_0404_4P2R_5%

51.1_0603_1%

51.1_0603_1%

200_0603_5%

200_0603_5%

200_0603_5%

200_0603_5%

200_0603_5%

200_0603_5%

200_0603_5%

200_0603_5%

10K_0402_1%

156_0603_5%

Place resistor <100mils from CPU pin

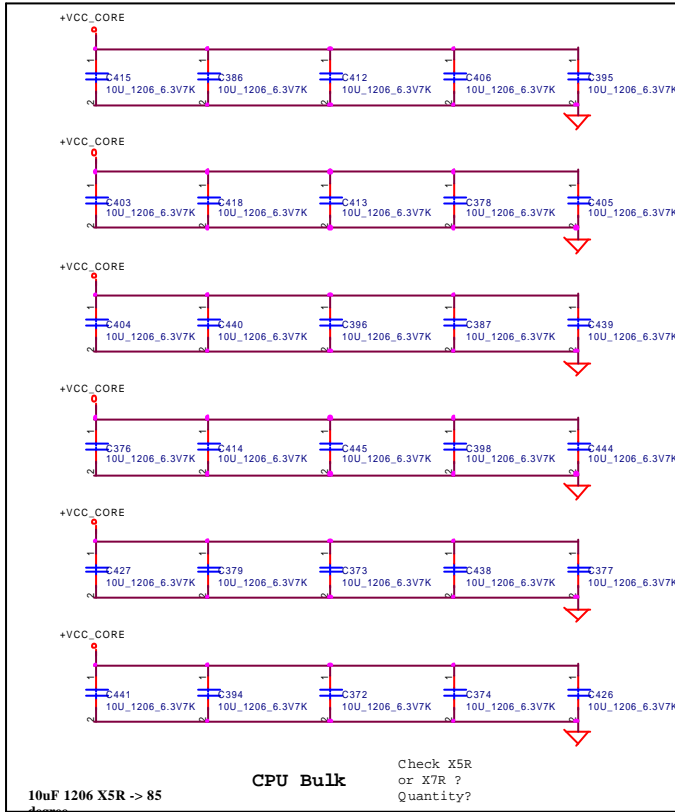
GTL Reference Voltage

- Layout note:
1. Place R_A and R_B near CPU.
 2. Place decoupling cap 220PF near CPU.(Within 500mils)

Compal Electronics, Inc.		
Mobile NorthWood(2/2)		
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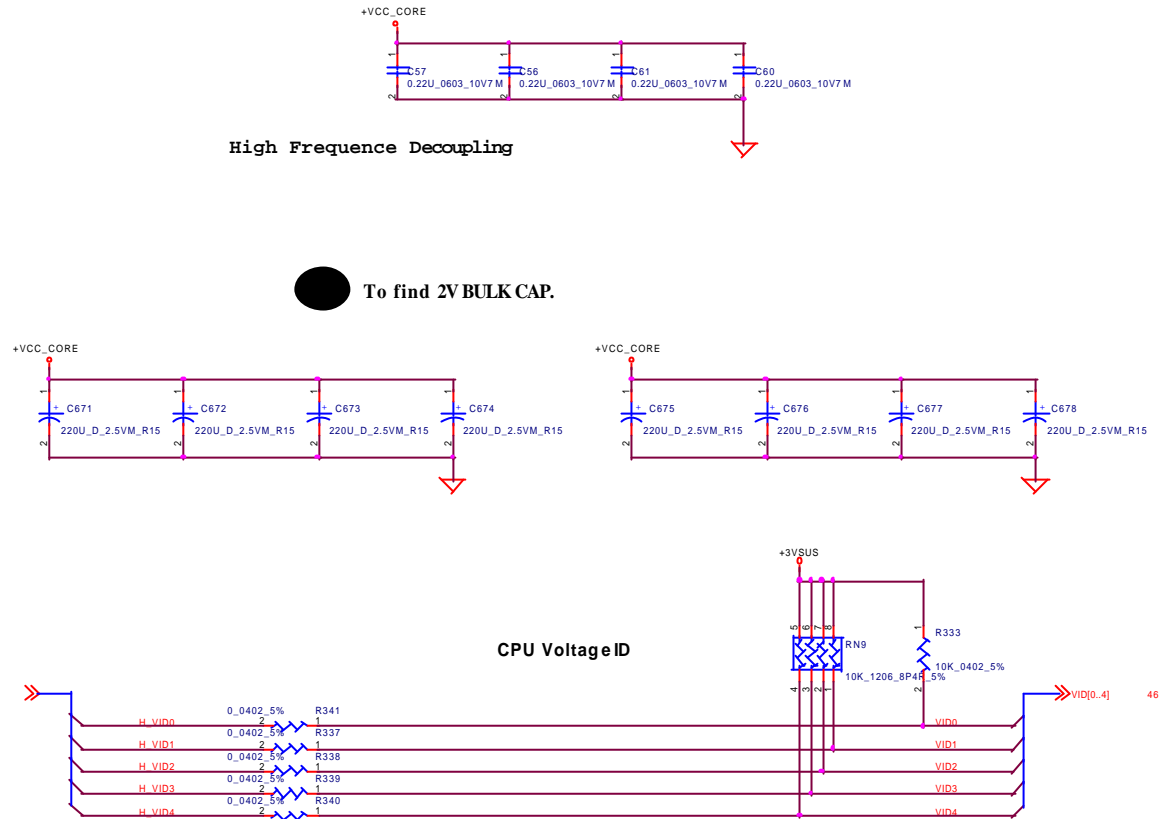
Layout note :
 Place close to CPU. Use 2-3 vias per PAD.
 Place 22uF caps underneath balls on solder side.
 Place 10uF caps on the peripheral near balls.
 Use 2-3 vias per PAD.

Layout note :
 Place close to CPU power and ground pin as possible (<1inch)



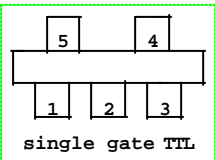
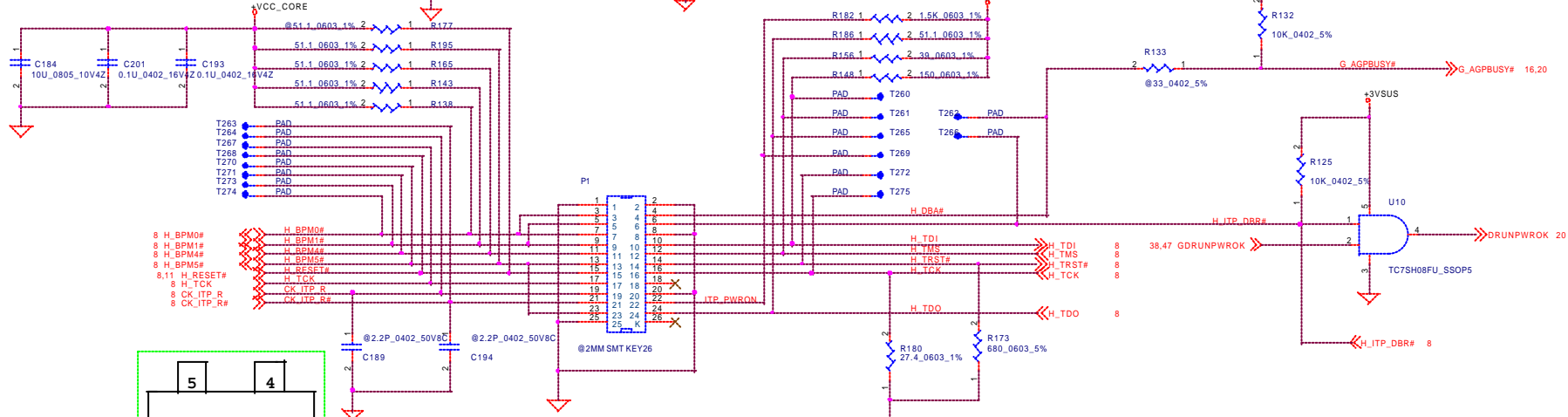
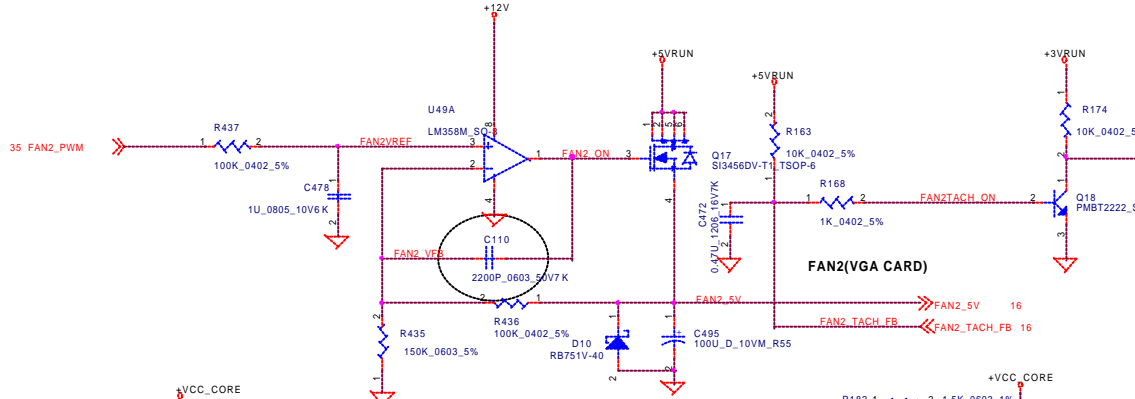
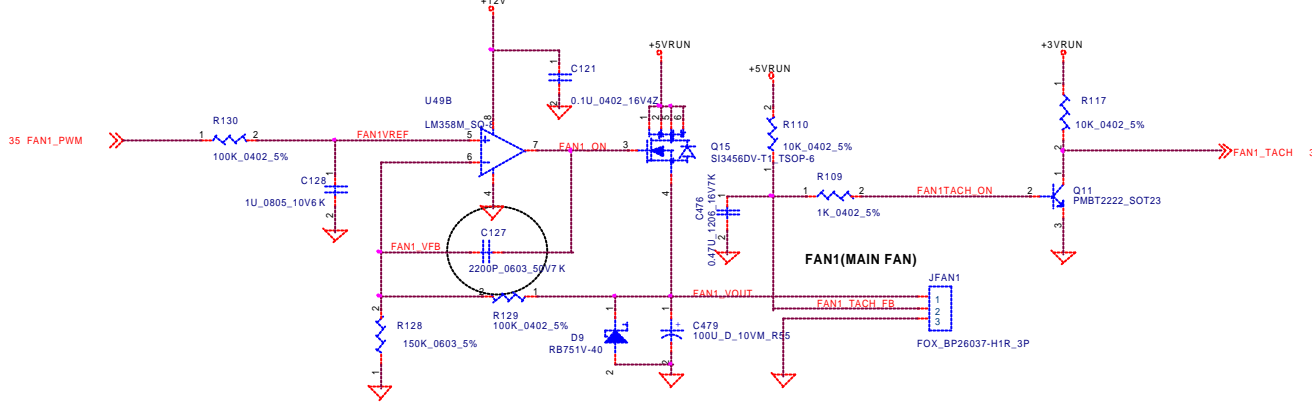
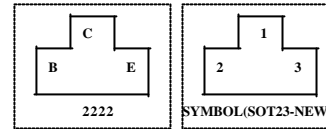
High Frequency Decoupling

To find 2V BULK CAP.



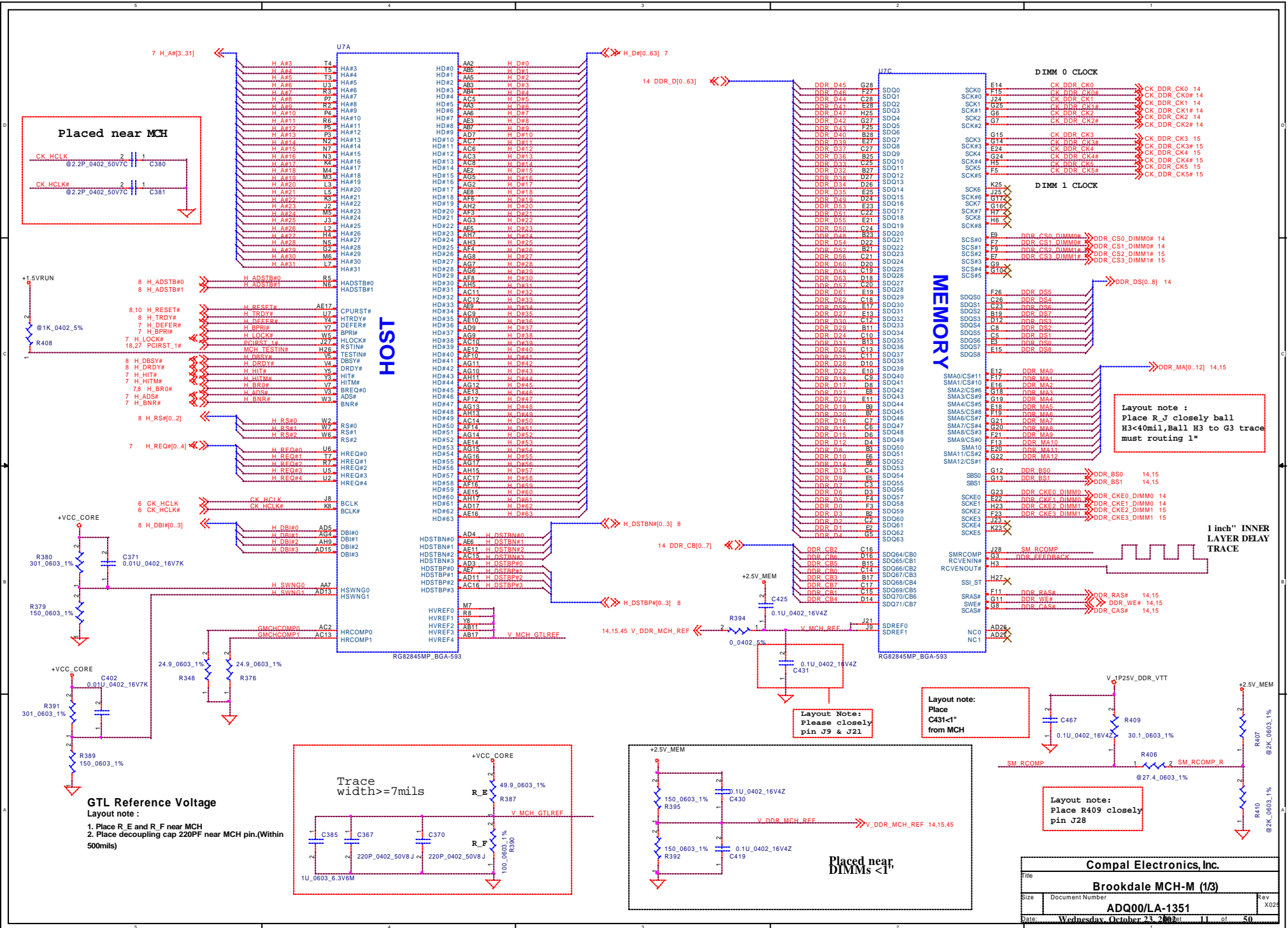
V I D					Vcore
VID4	VID3	VID2	VID1	VID0	V
0	1	0	0	0	1.350
0	1	0	0	1	1.300
0	1	0	1	0	1.250
0	1	0	1	1	1.200
0	1	1	0	0	1.150
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.000
1	0	0	0	0	0.975
1	0	0	0	1	0.950

FAN1 Control and Tachometer



ITP Debug Connector

Compal Electronics, Inc.		
Title: ITP Debug CONN. & FAN		
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Placed near MCH

CK_HCLK @2.2P_0402_50V7C C380

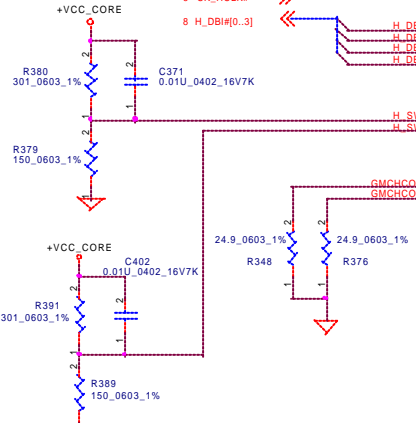
CK_HCLK# @2.2P_0402_50V7C C381

HOST

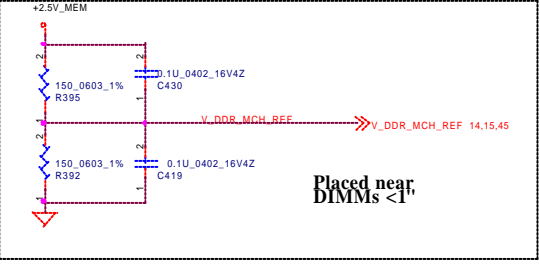
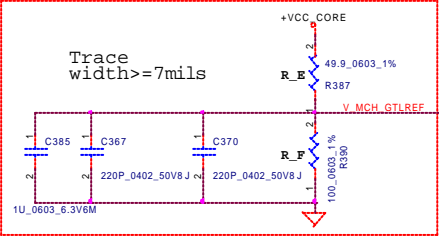
MEMORY

Layout note :
Place R_J closely ball
H3<40mil, Ball H3 to G3 trace
must routing 1"

**1 inch" INNER
LAYER DELAY
TRACE**



GTL Reference Voltage
Layout note :
1. Place R_E and R_F near MCH
2. Place decoupling cap 220PF near MCH pin.(Within 500mils)



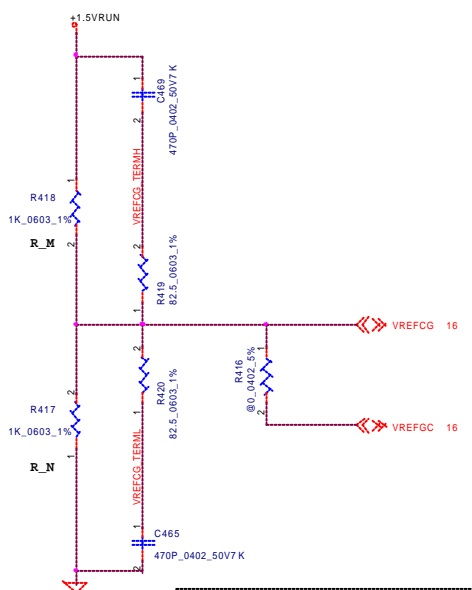
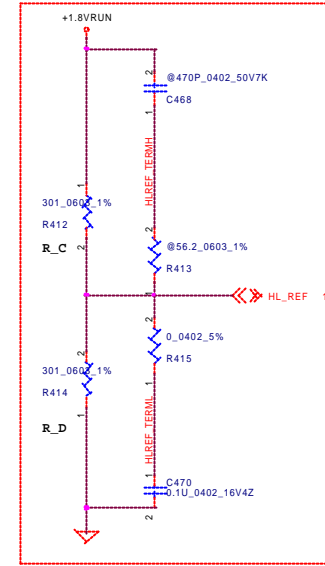
Layout note:
Place C431<1" from MCH

Layout note:
Place R409 closely pin J28

HUB Interface Reference

Layout note :

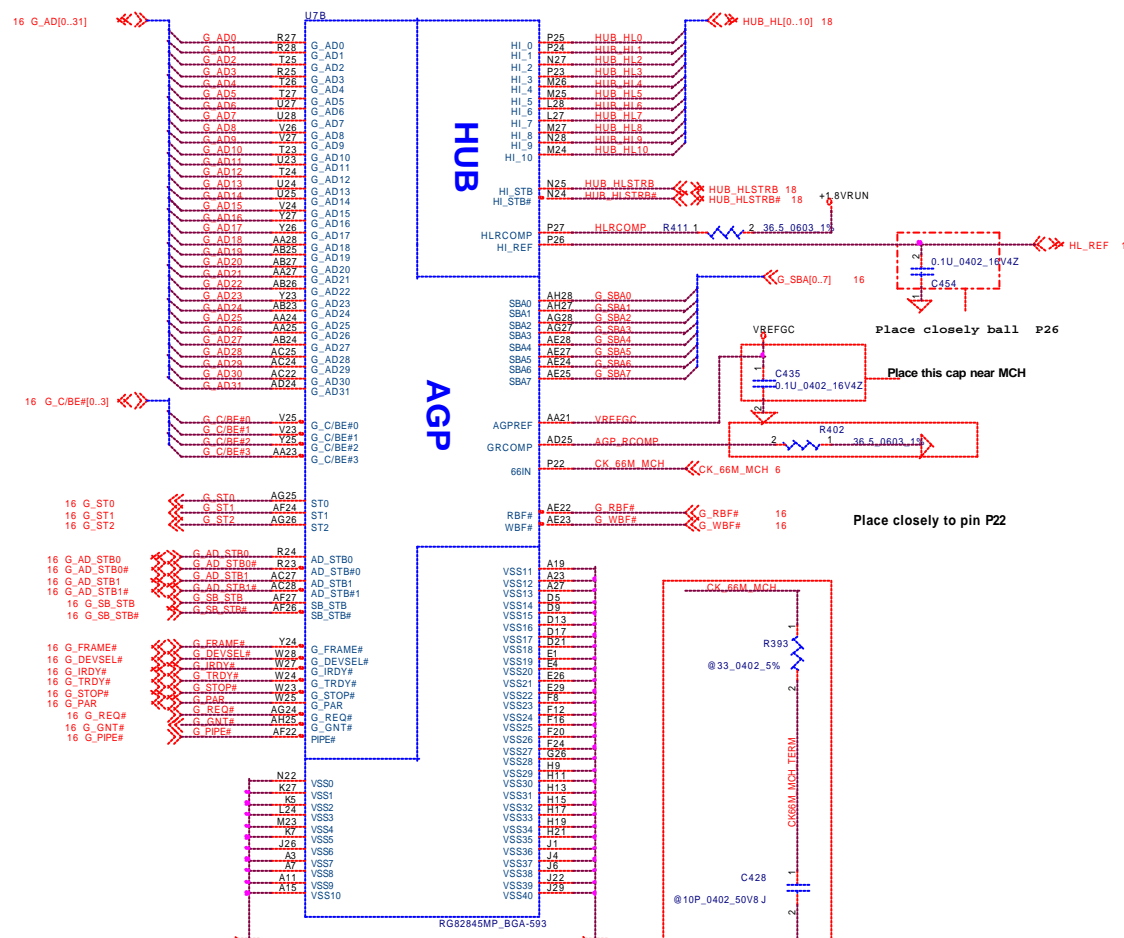
- 1. Place R_C and R_D in middle of Bus.
- 2. Place capacitors near MCH.



AGP Interface Reference

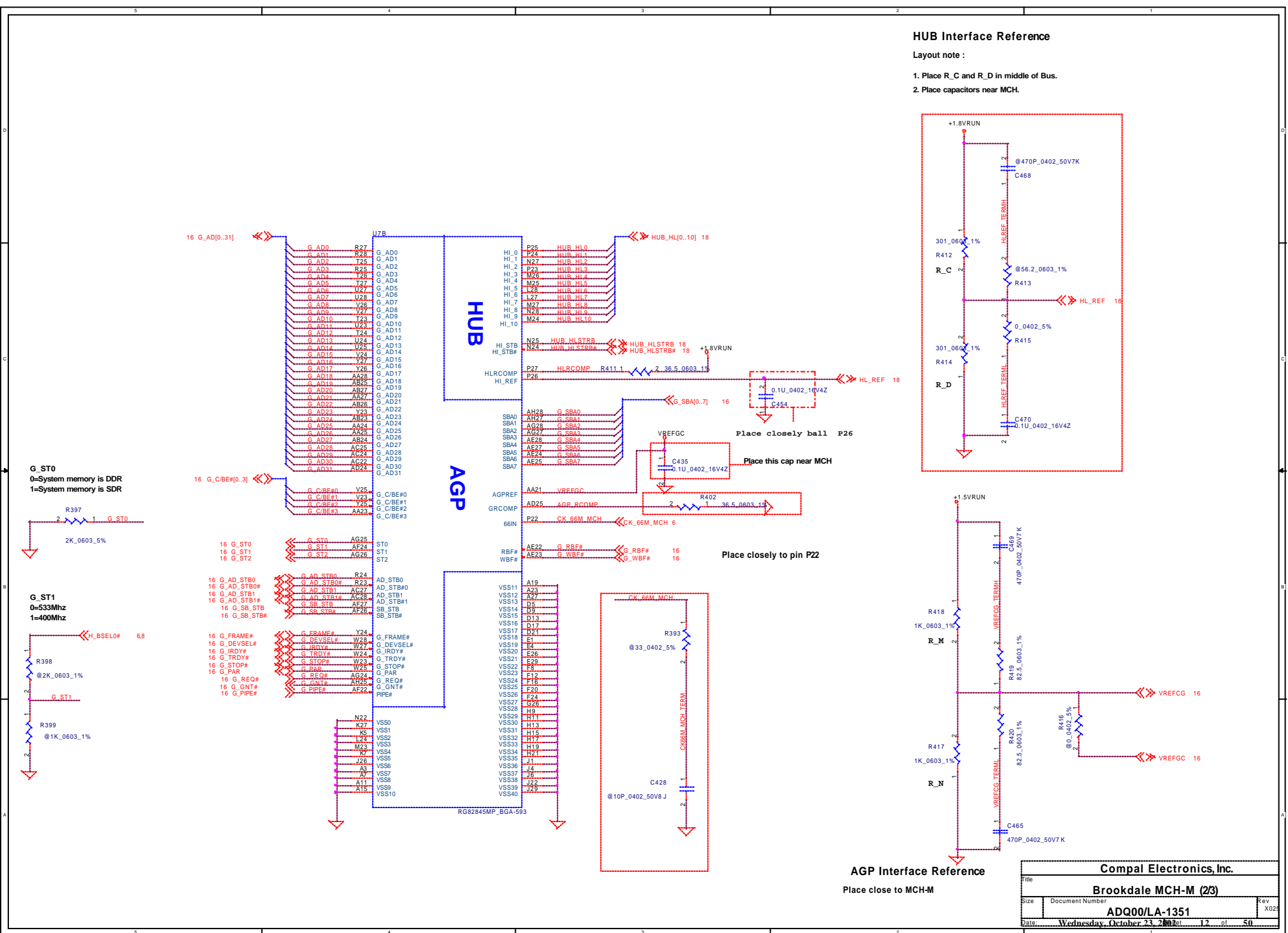
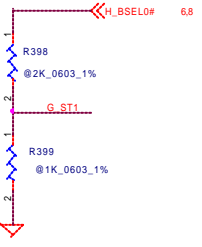
Place close to MCH-M

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Brookdale MCH-M (2/3)		
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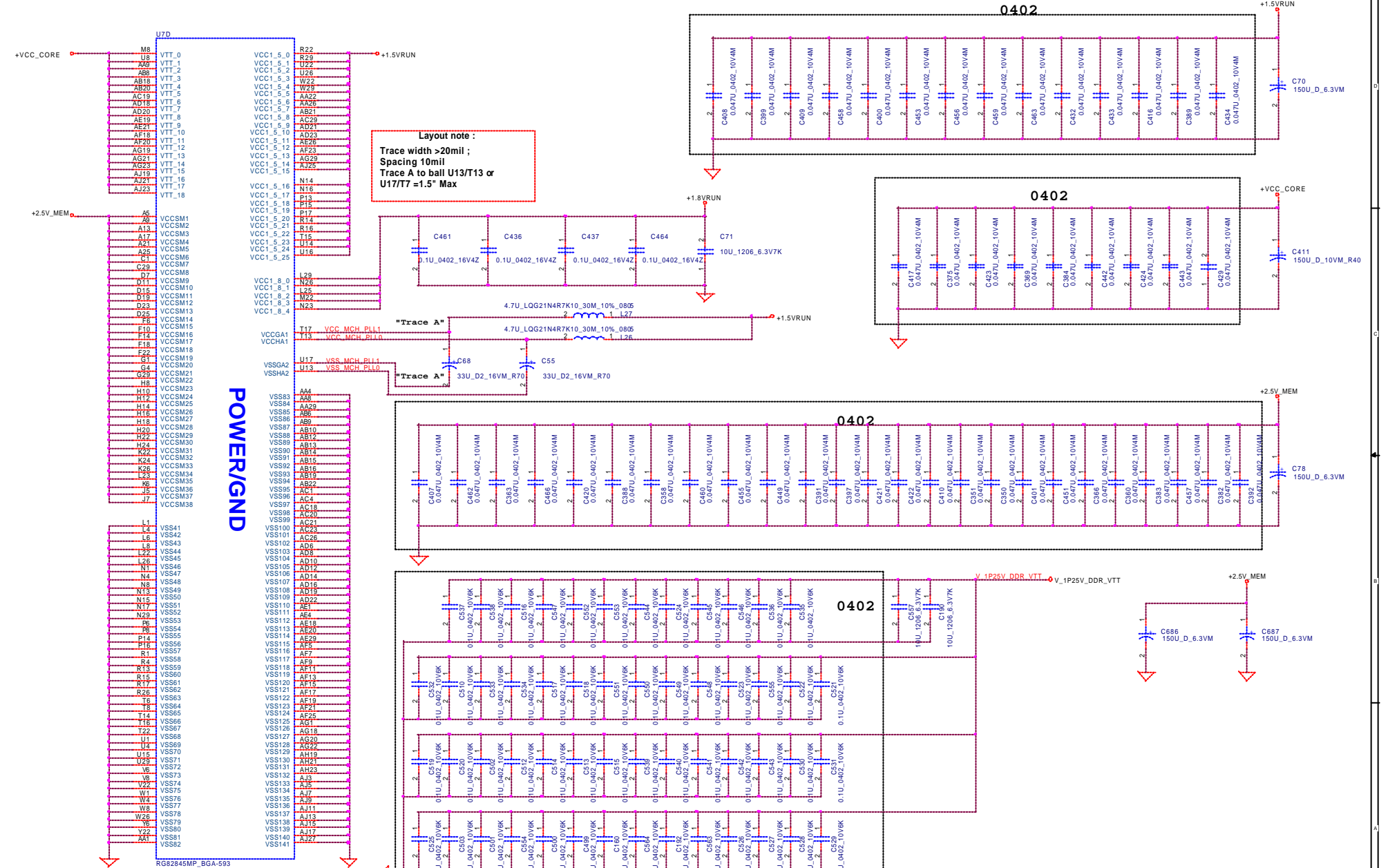


G_ST0
 0=System memory is DDR
 1=System memory is SDR

G_ST1
 0=533Mhz
 1=400Mhz



POWER/GND

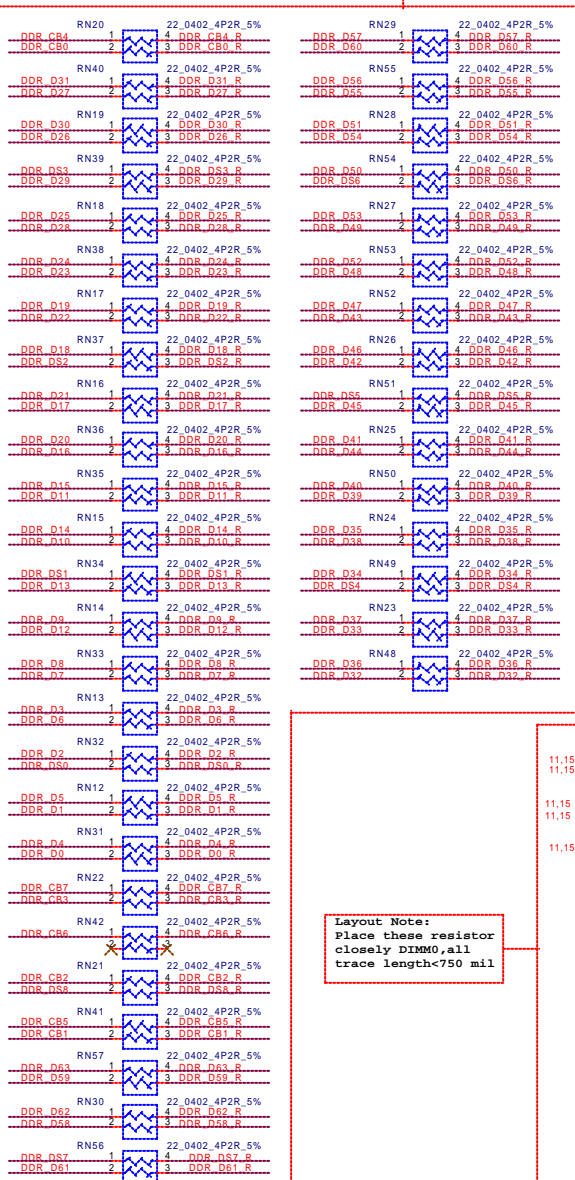


Layout note:
 Trace width >20mil ;
 Spacing 10mil
 Trace A to ball U13/T13 or
 U17/T7 =1.5" Max

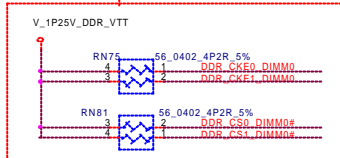
Title		Compal Electronics, Inc.	
Size		Brookdale MCH-M (3/3)	
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- 11 DDR_D[0..63]
- 11 DDR_CB[0..7]
- 11 DDR_DS[0..8]

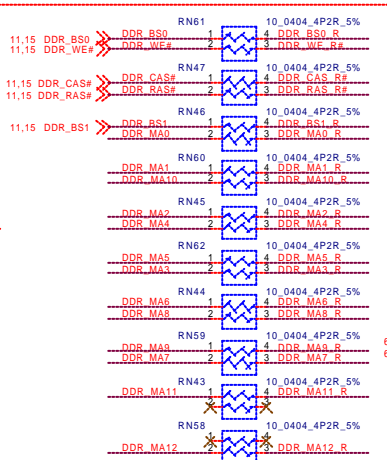
Layout Note:
Place these resistor
closely DIMM0,all
trace length<750 mil



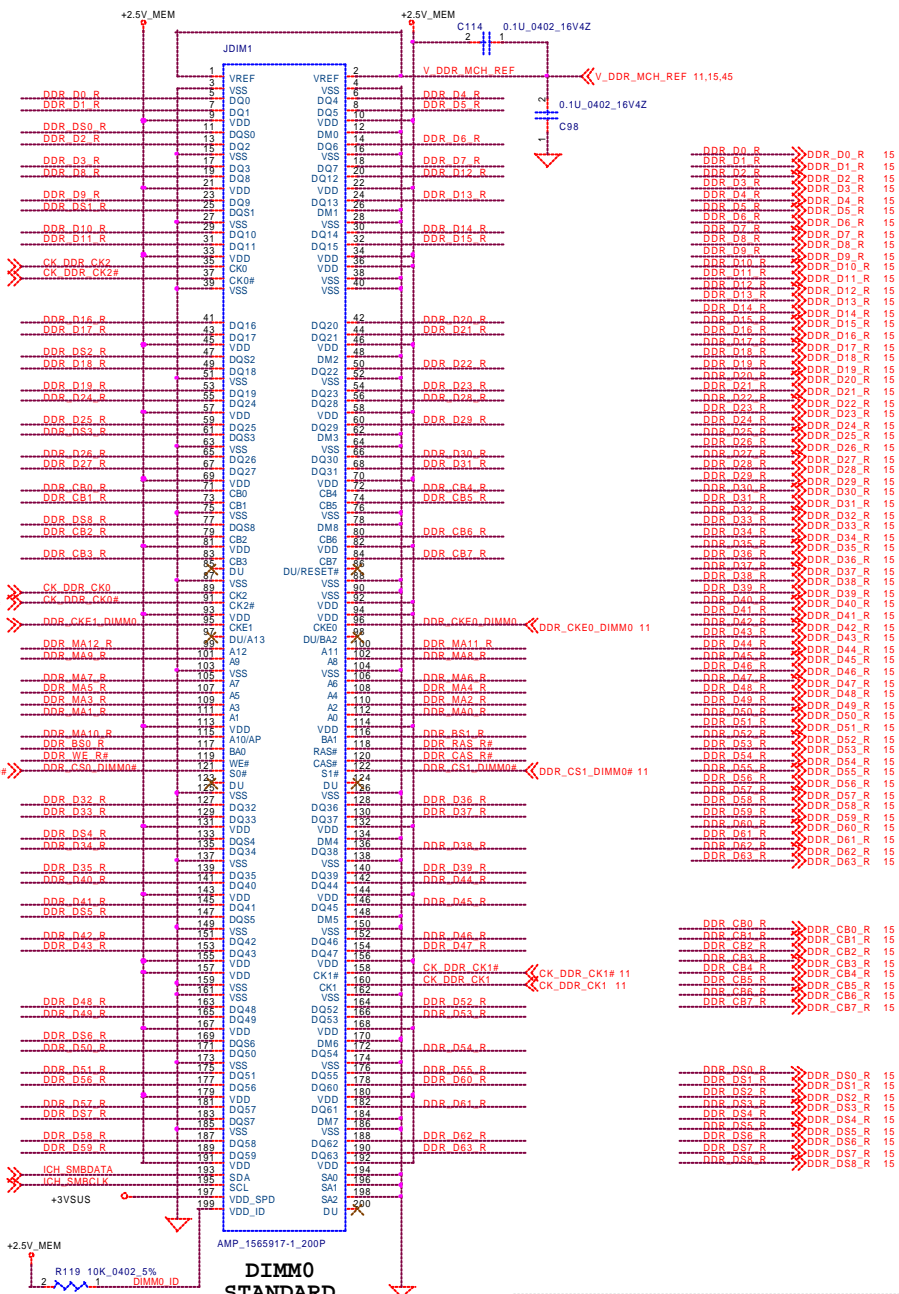
Layout Note:
Place these resistor
closely DIMM0,all
trace length
Max=1.3"



11.15 DDR_MA[0..12]



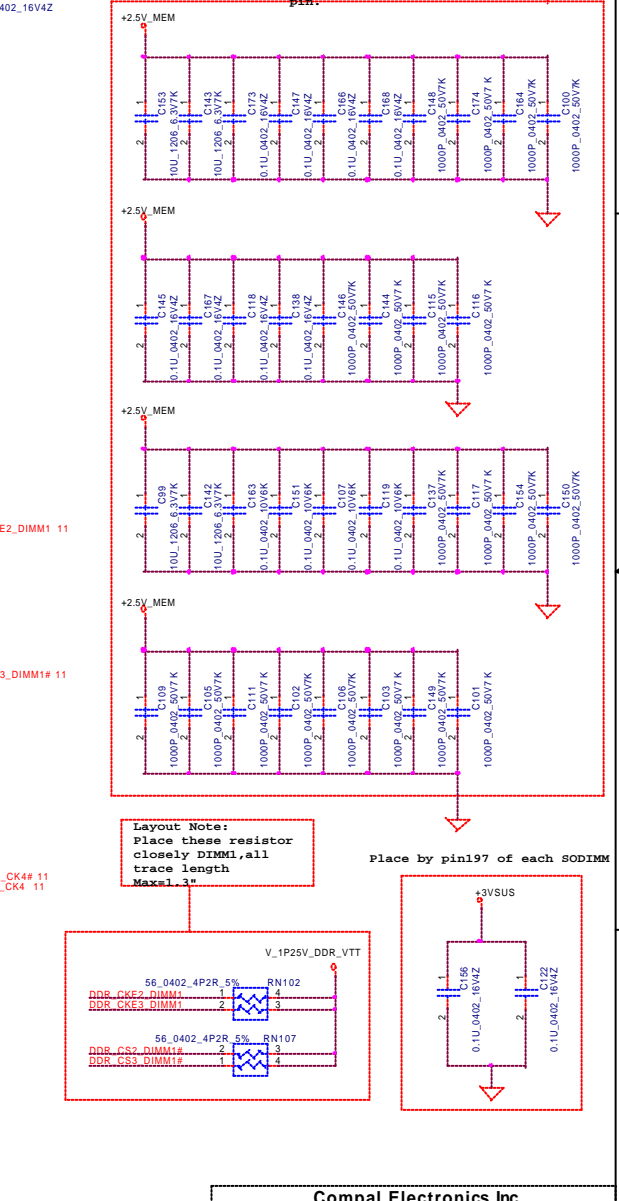
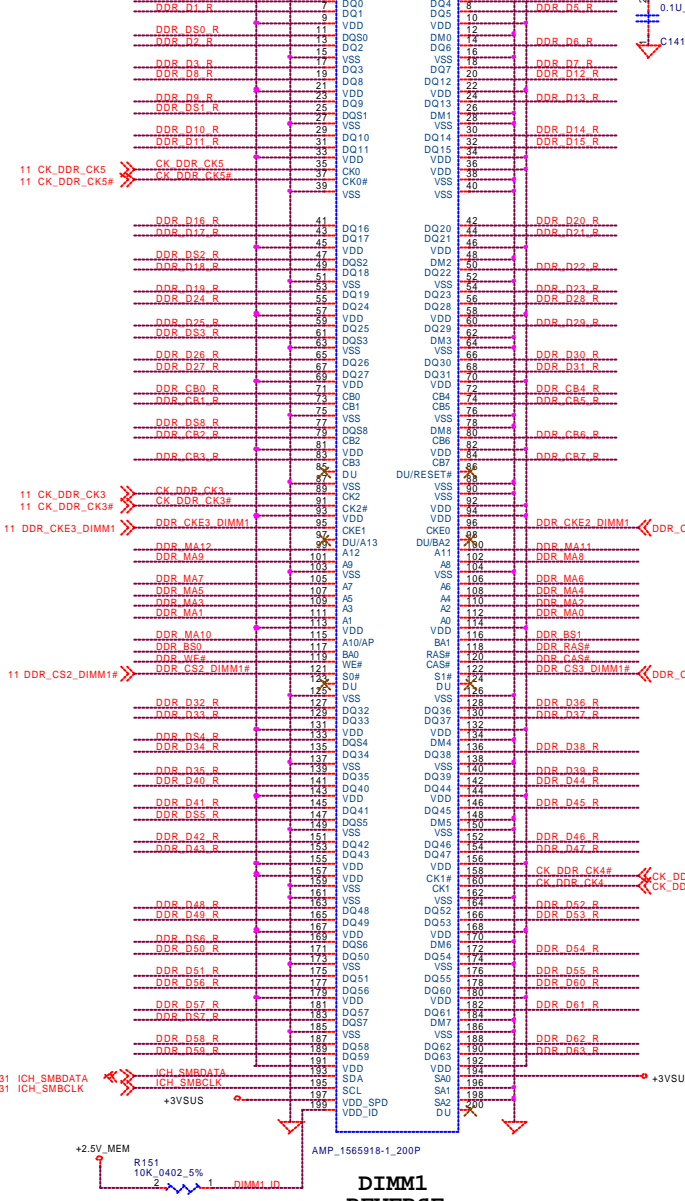
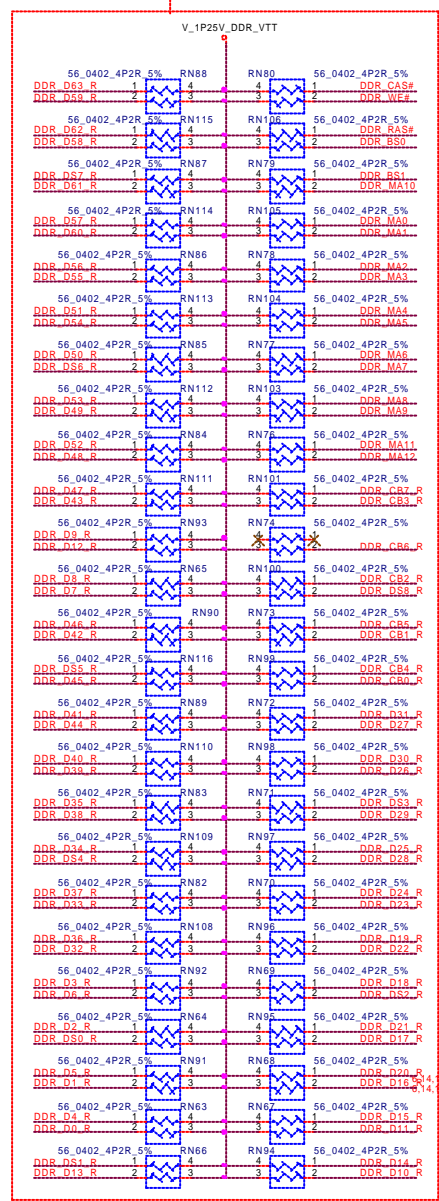
Layout Note:
Place these resistor
closely DIMM0,all
trace length<750 mil



Layout Note:
Place these resistors
closely DIMM1, all
trace length<=800 mll

Layout Note:
Place CAP
near SODIMM
One .1uF cap per power pin.
Place each cap close to
pin.

11,14 DDR_MA0[.12]



14 DDR_C80_R DDR_C80_R
14 DDR_C81_R DDR_C81_R
14 DDR_C82_R DDR_C82_R
14 DDR_C83_R DDR_C83_R
14 DDR_C84_R DDR_C84_R
14 DDR_C85_R DDR_C85_R
14 DDR_C86_R DDR_C86_R
14 DDR_C87_R DDR_C87_R

14 DDR_D50_R DDR_D50_R
14 DDR_D51_R DDR_D51_R
14 DDR_D52_R DDR_D52_R
14 DDR_D53_R DDR_D53_R
14 DDR_D54_R DDR_D54_R
14 DDR_D55_R DDR_D55_R
14 DDR_D56_R DDR_D56_R
14 DDR_D57_R DDR_D57_R
14 DDR_D58_R DDR_D58_R

11,14 DDR_B50 DDR_B50
11,14 DDR_B51 DDR_B51
11,14 DDR_WE# DDR_WE#
11,14 DDR_CAS# DDR_CAS#
11,14 DDR_RAS# DDR_RAS#

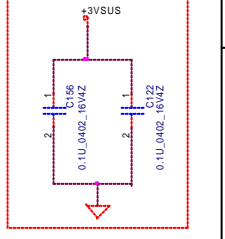
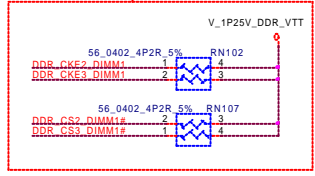
4,9,31 ICH_SMBDATA
4,9,31 ICH_SMBCLK

+2.5V_MEM R151
10K_0402.5% DIMM1_ID

**DIMM1
REVERSE**

Layout Note:
Place these resistor
closely DIMM1, all
trace length
Max<1.3"

Place by pin197 of each SODIMM

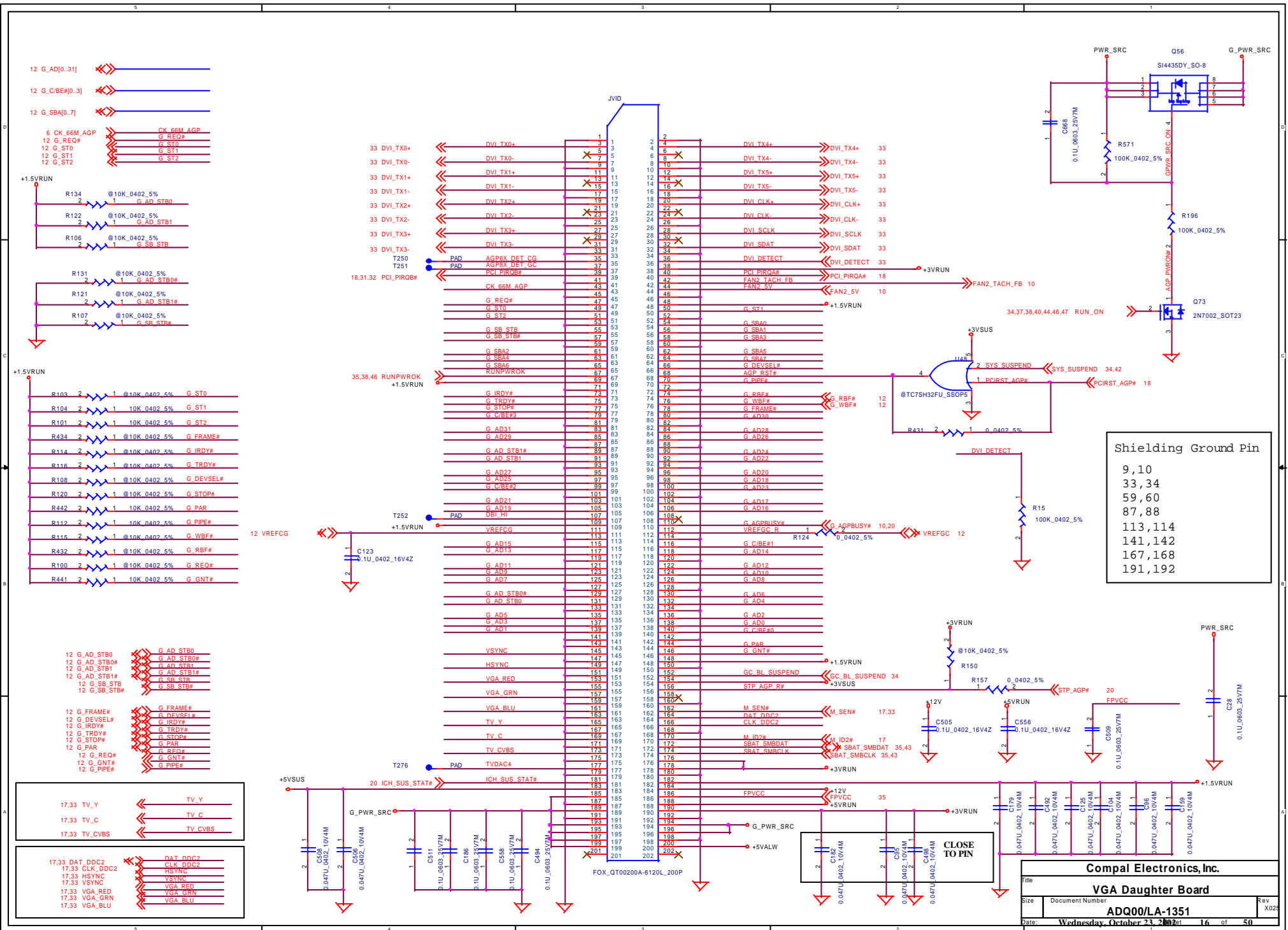


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DDR-SODIMM SLOT2

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Shielding Ground Pin

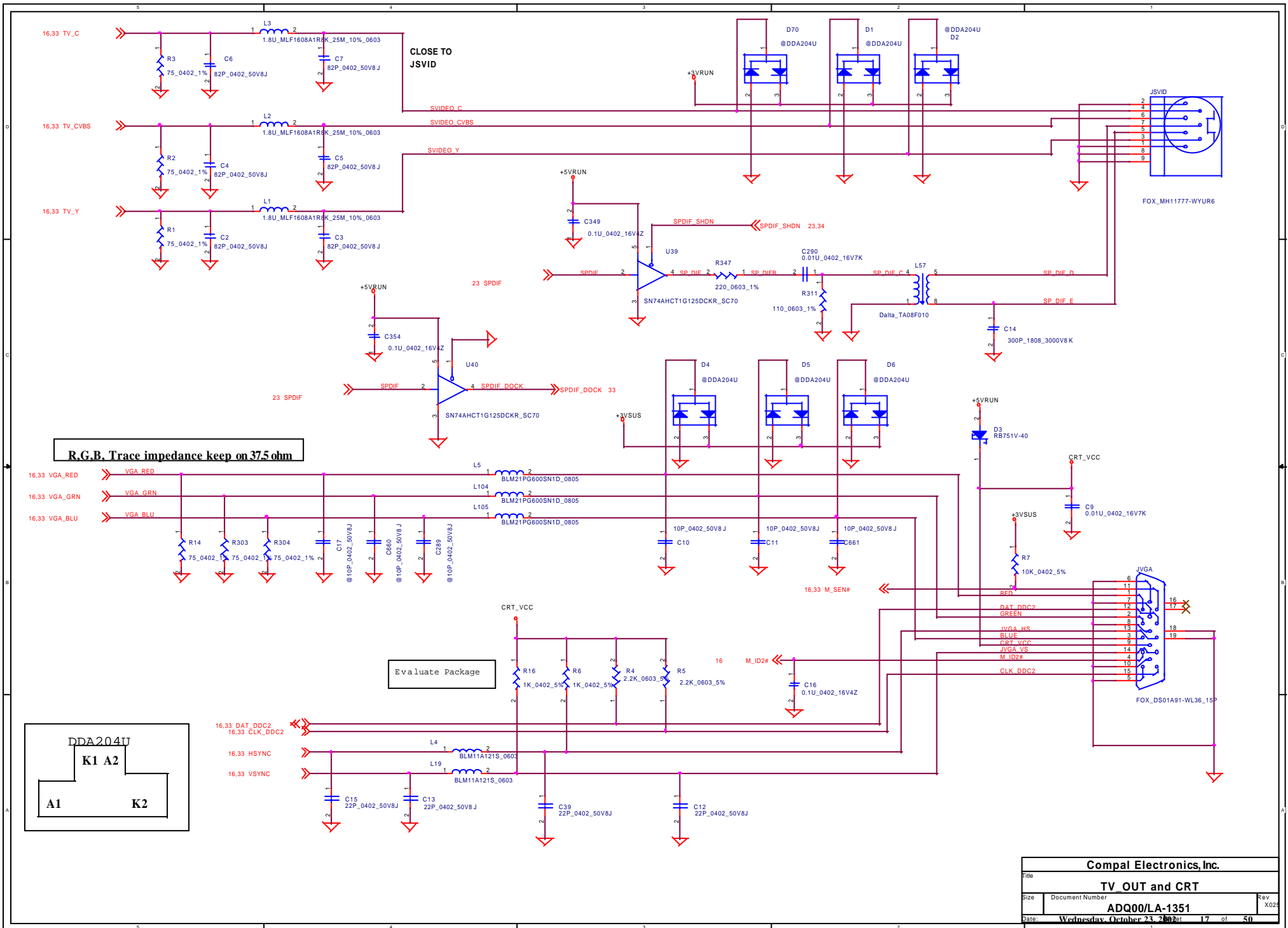
9,10
33,34
59,60
87,88
113,114
141,142
167,168
191,192

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VGA Daughter Board

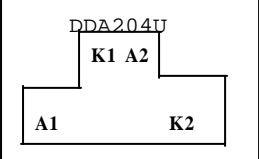
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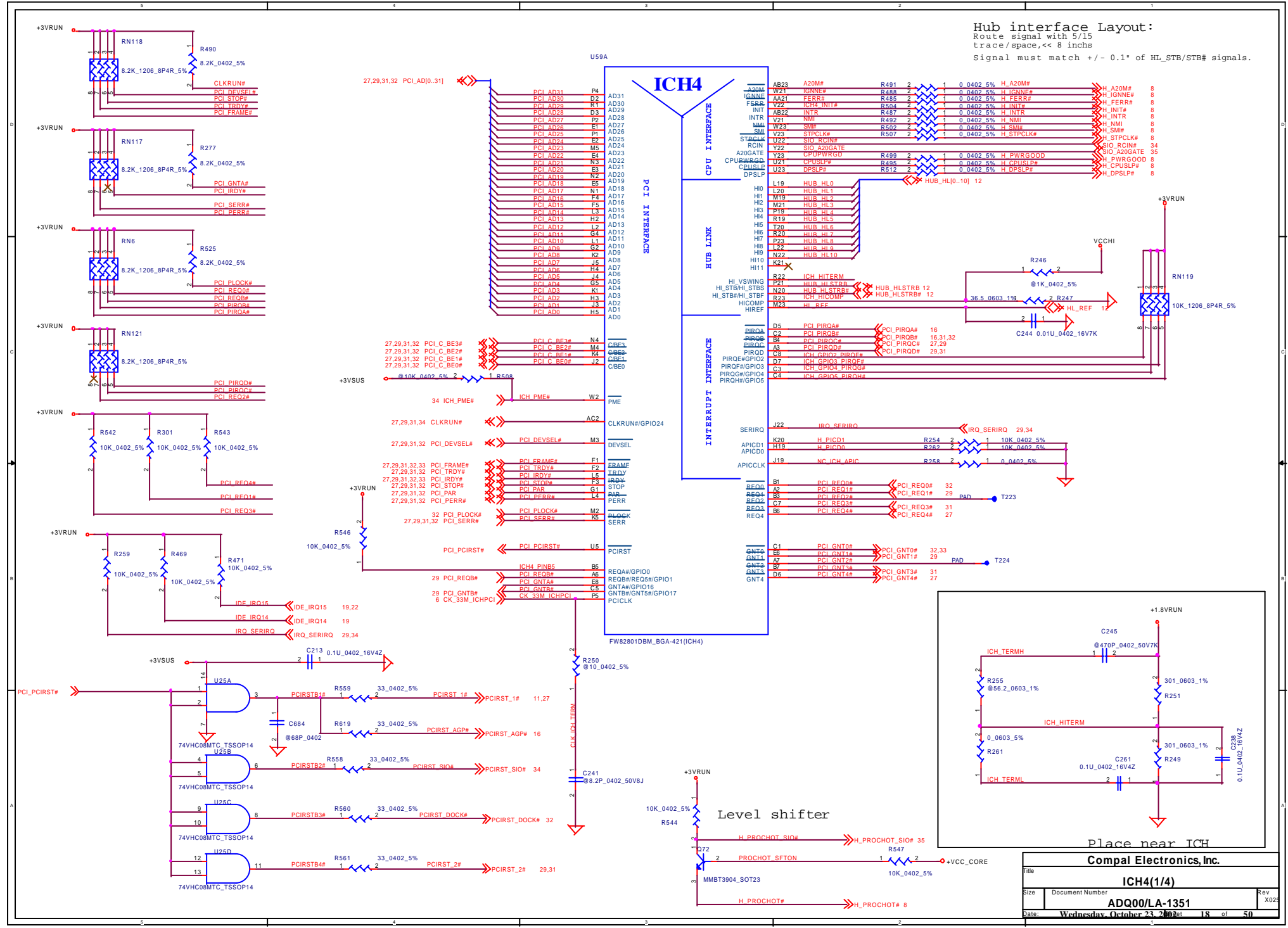
R.G.B. Trace impedance keep on 37.5 ohm

Evaluate Package

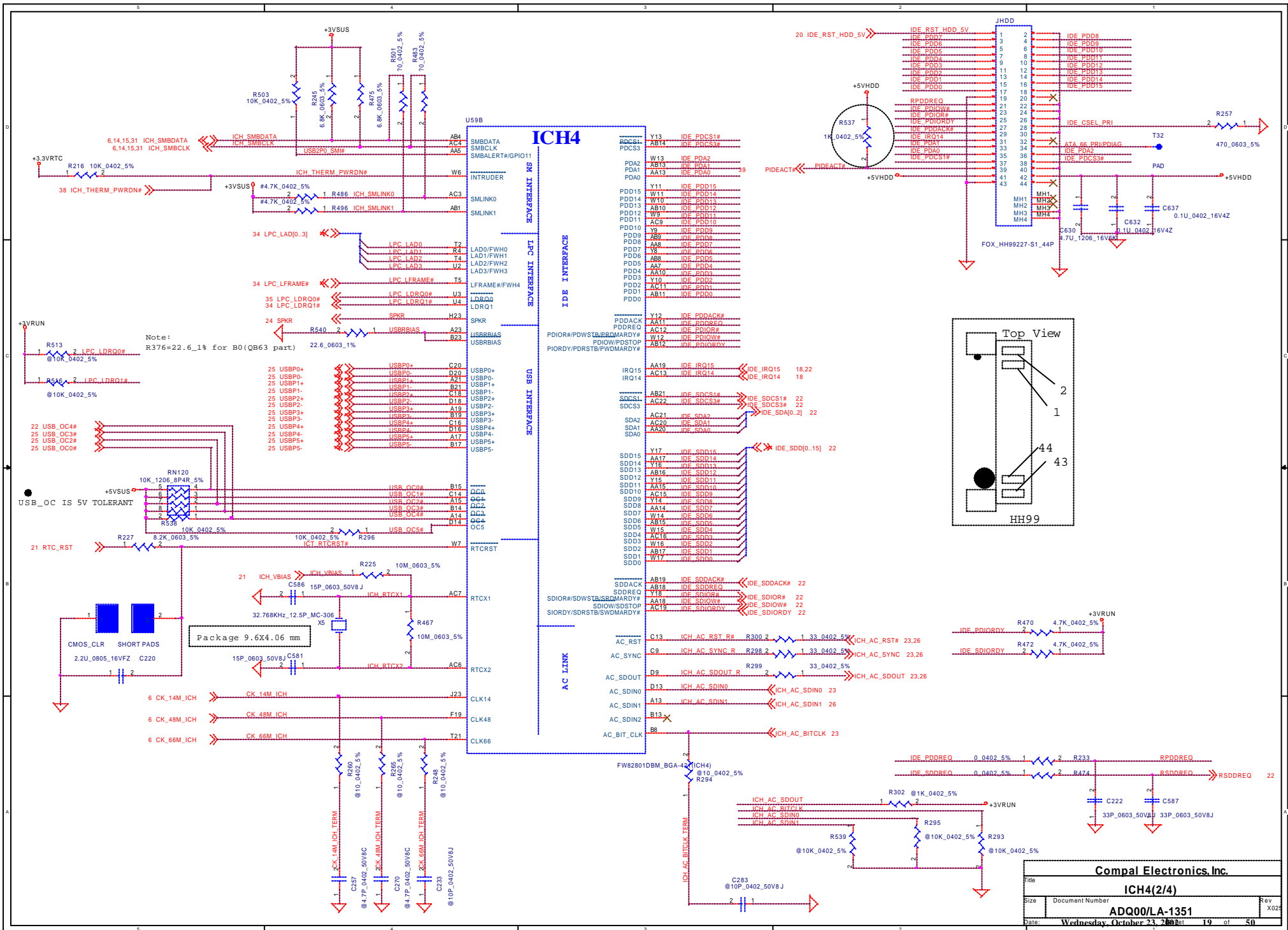


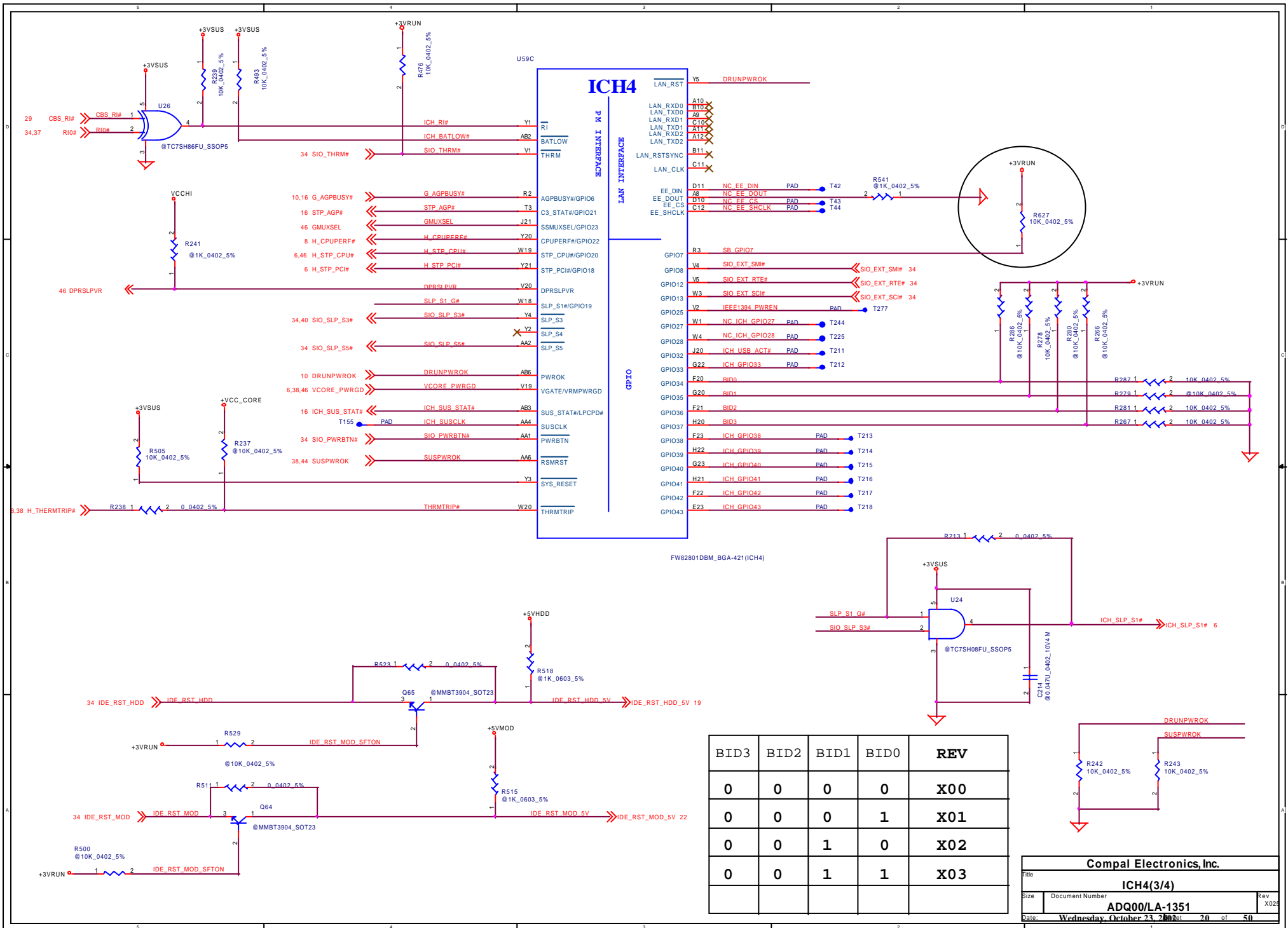
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TV_OUT and CRT		
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Hub interface Layout:
 Route signal with 5/15
 trace/space, < 8 inches
 Signal must match +/- 0.1" of HL_STB/STB# signals.

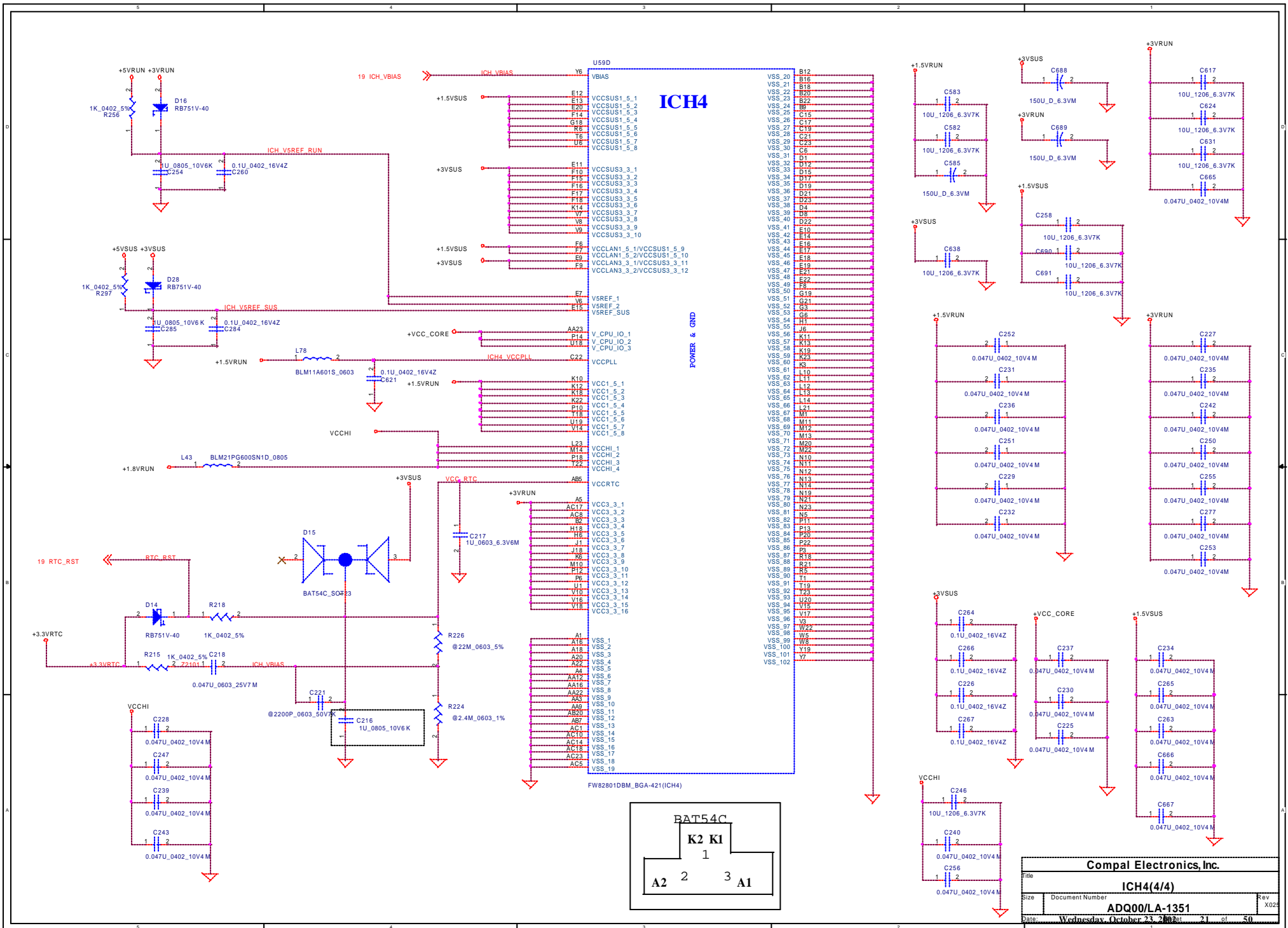


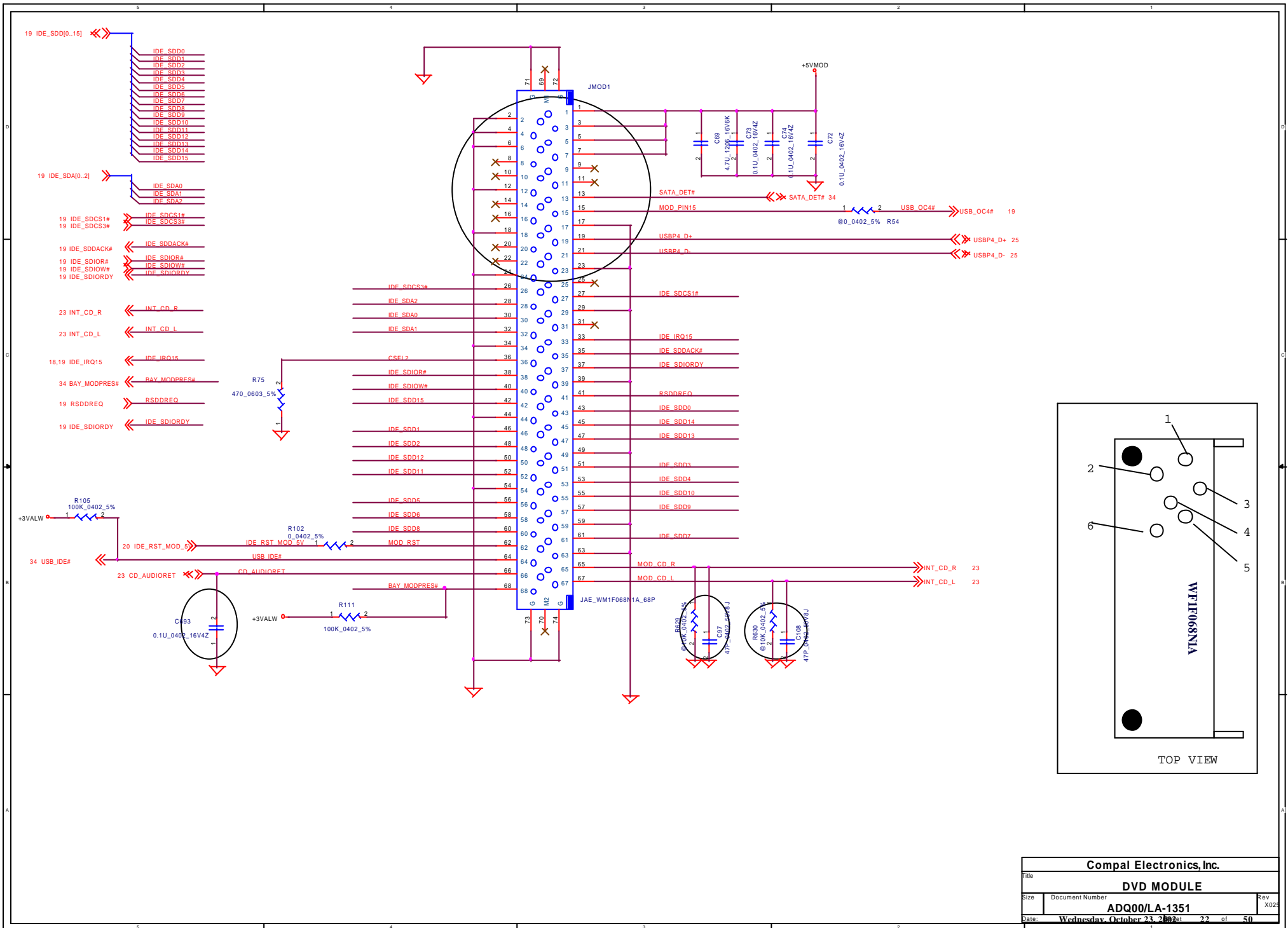
Title		ICH4(1/4)	
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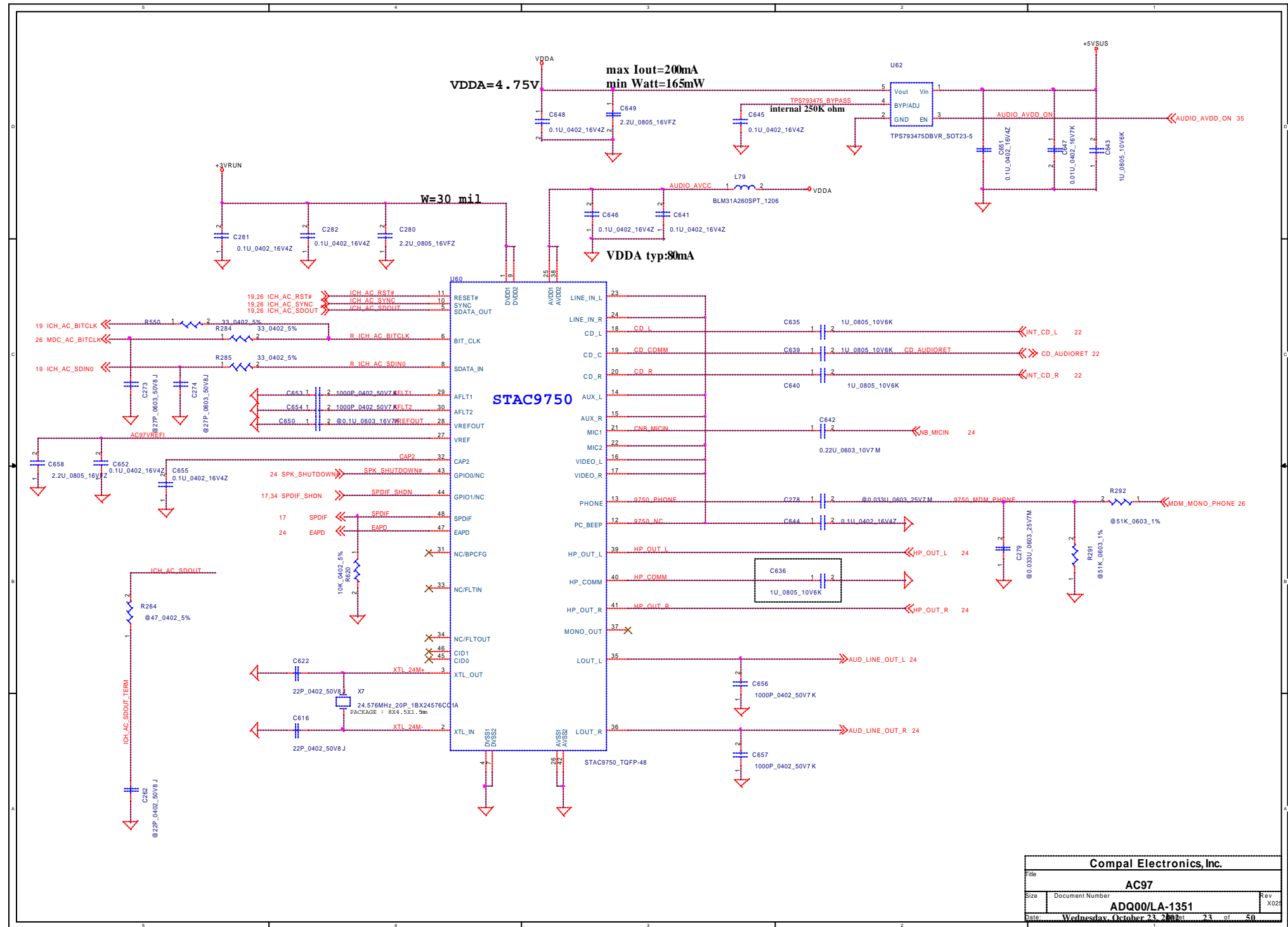




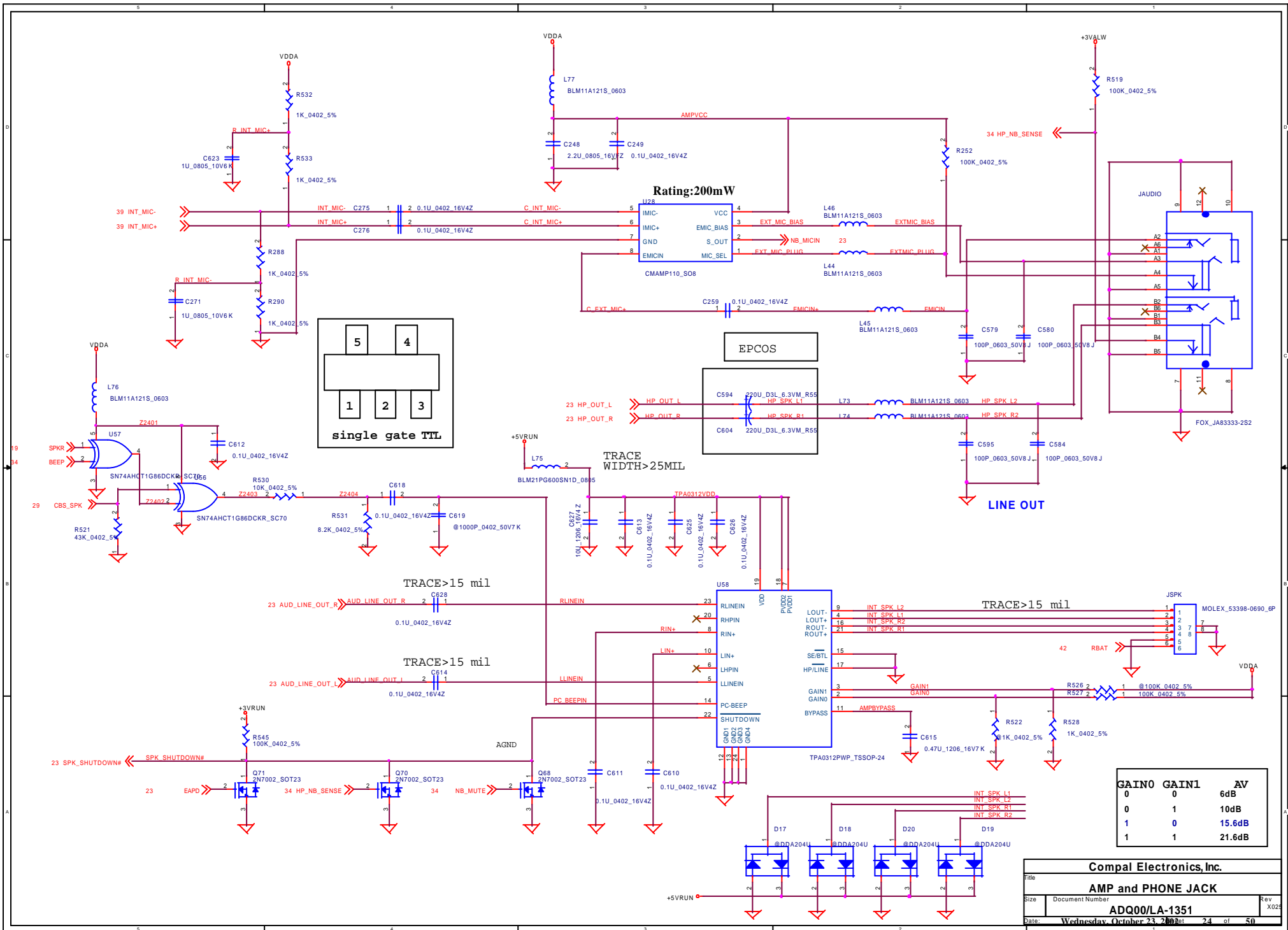
BID3	BID2	BID1	BID0	REV
0	0	0	0	X00
0	0	0	1	X01
0	0	1	0	X02
0	0	1	1	X03



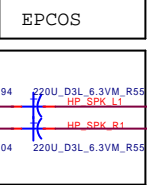
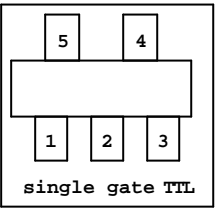




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AC97		
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Rating:200mW



TRACE WIDTH > 25MIL

TRACE > 15 mil

TRACE > 15 mil

TRACE > 15 mil

GAIN	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Compal Electronics, Inc.

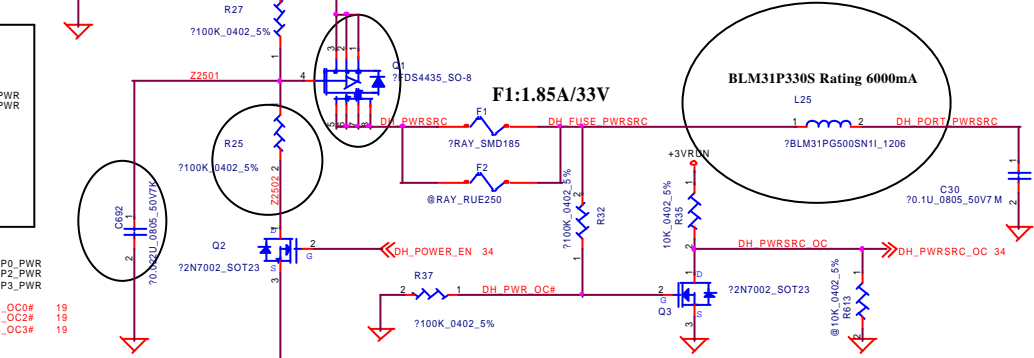
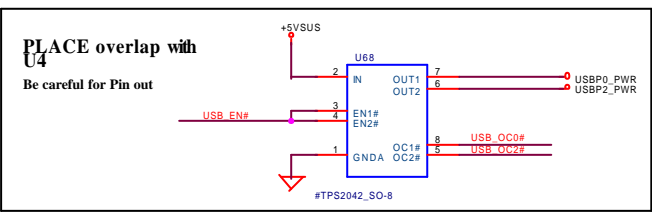
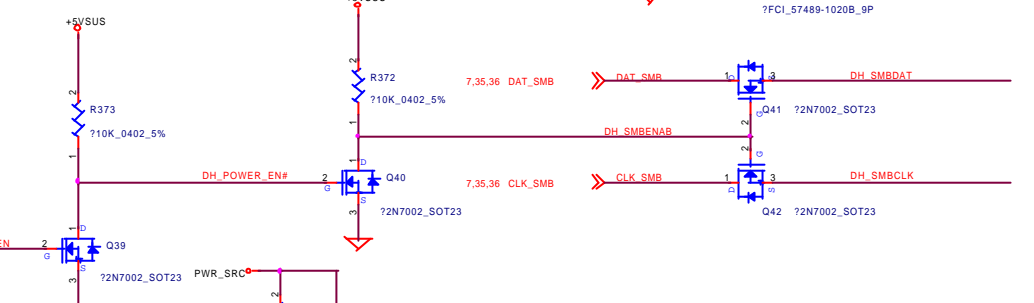
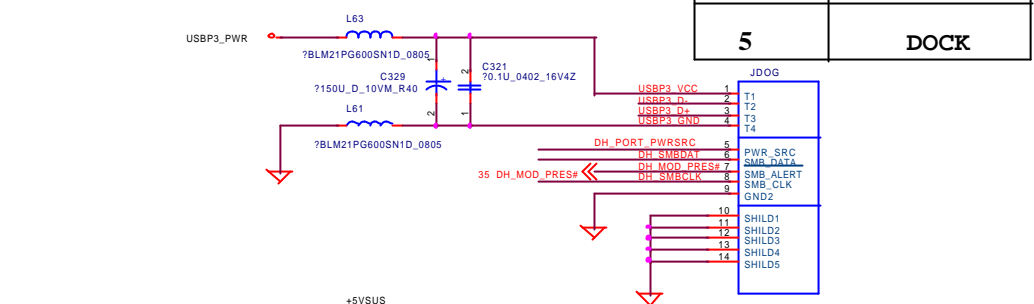
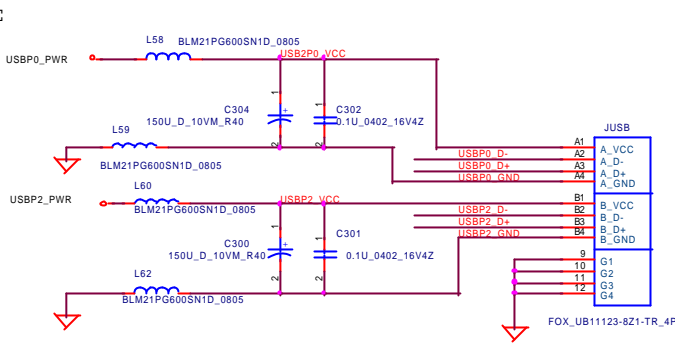
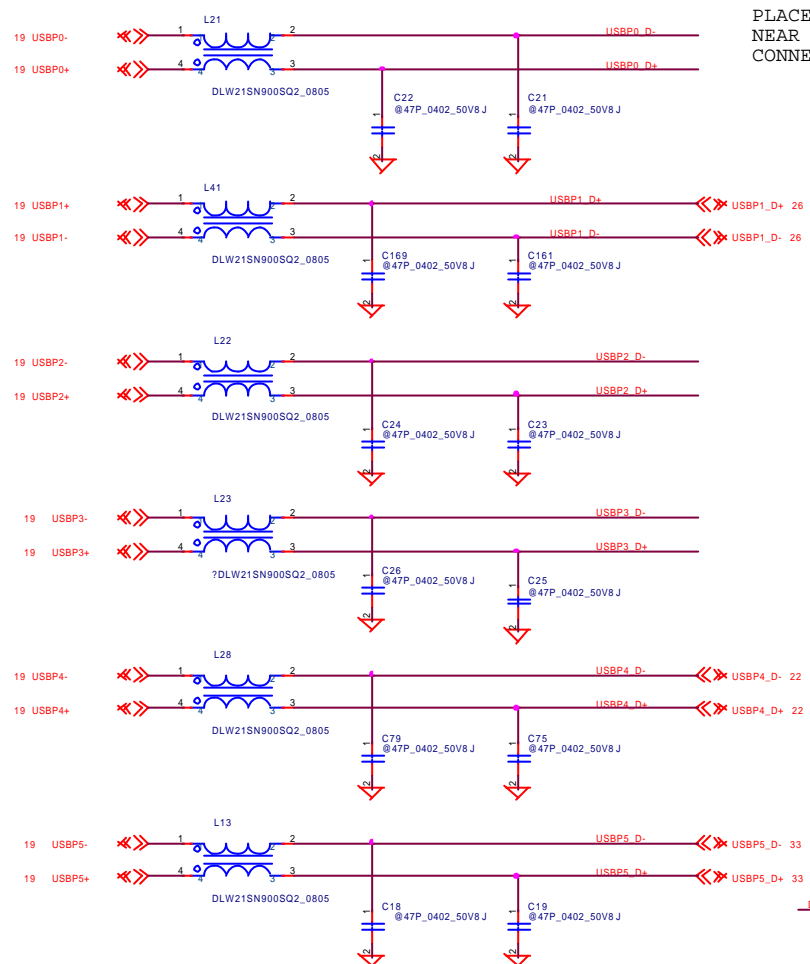
AMP and PHONE JACK

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USB PORT#	DESTINATION
0	BACK
1	BT
2	BACK
3	DOG
4	MOD
5	DOCK

PLACE CHOKE
NEAR
CONNECTOR



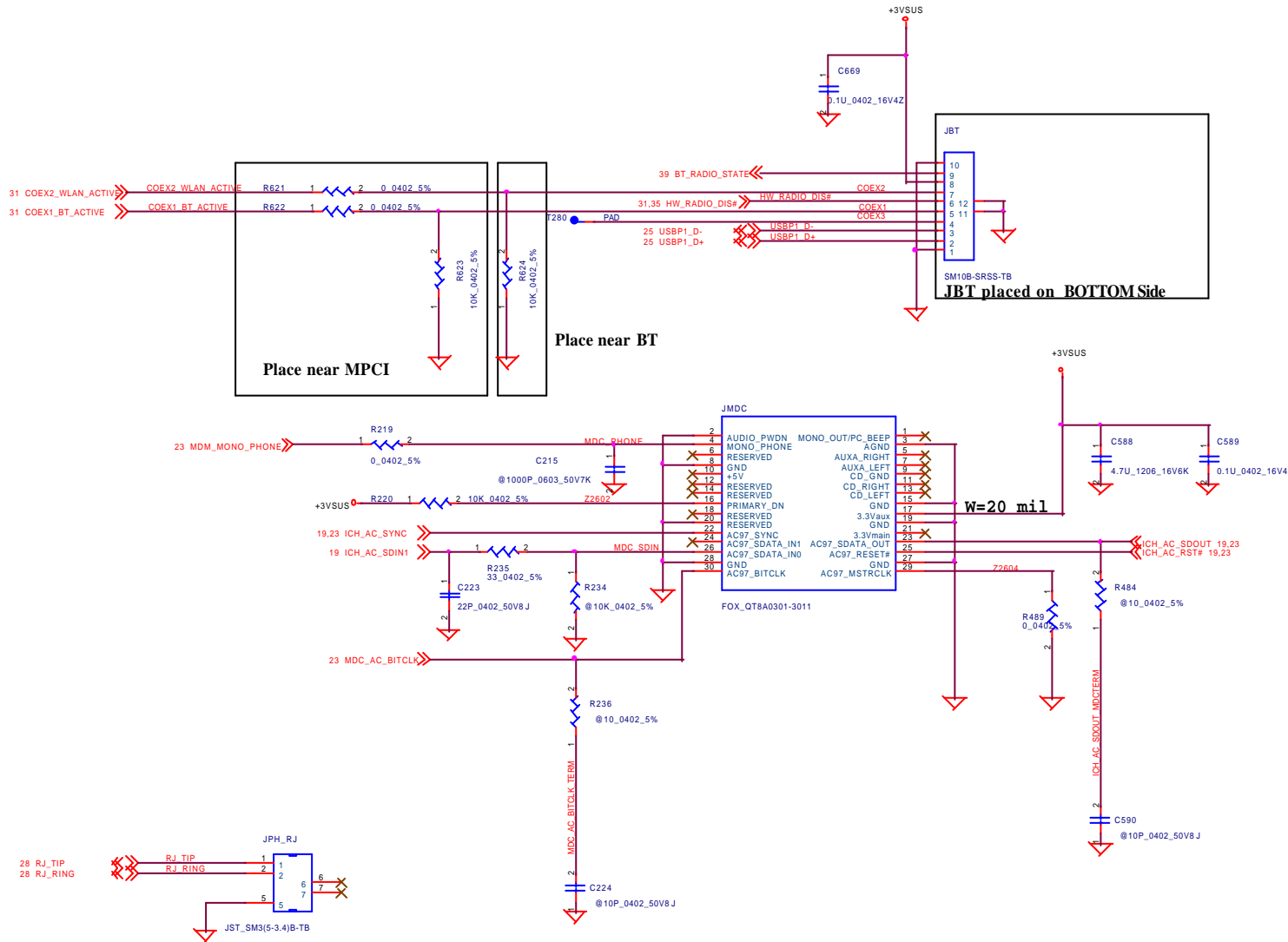
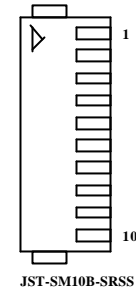
Compal Electronics, Inc.

USB/Doghouse

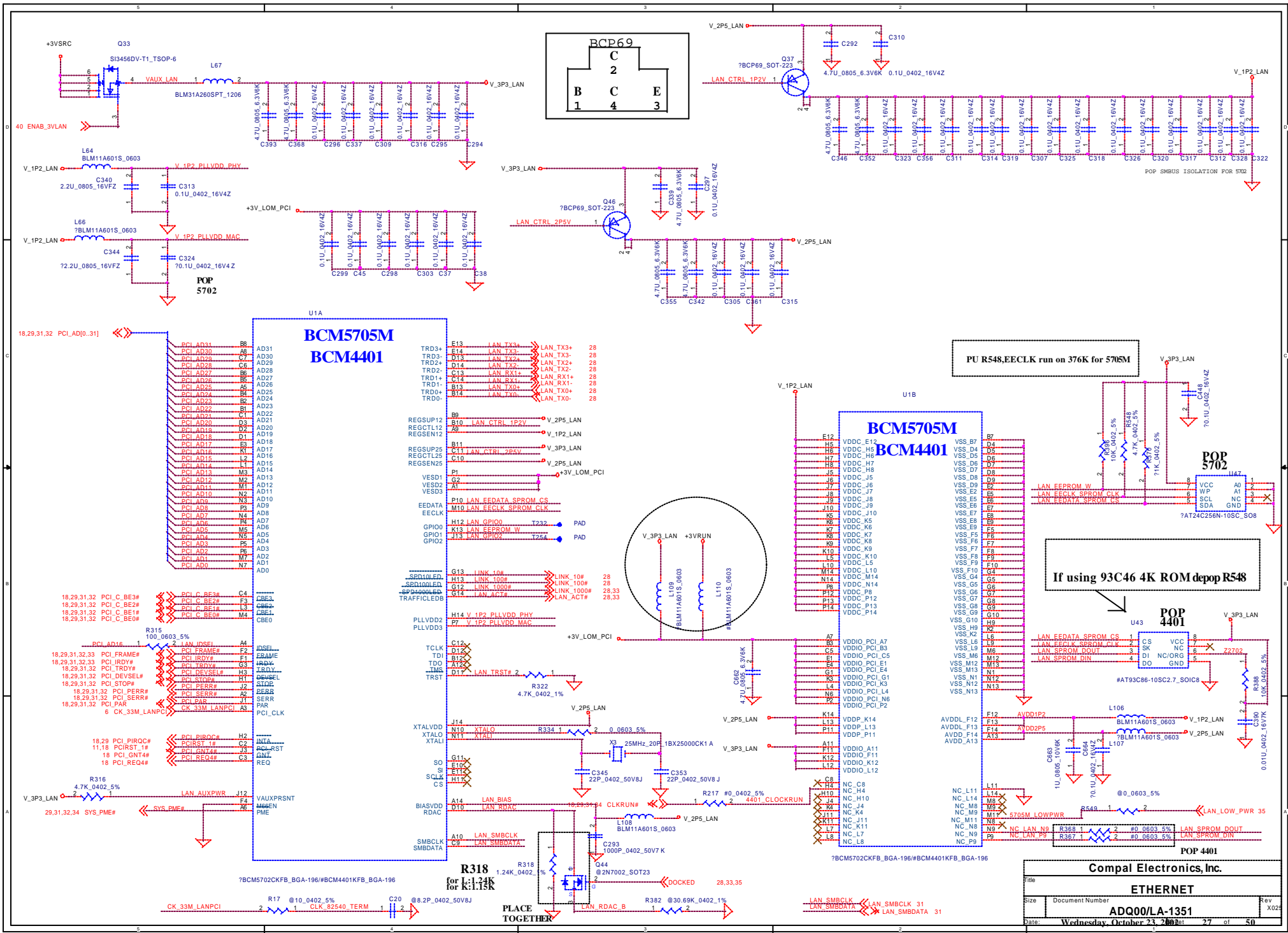
ADQ00/LA-1351

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TOP view



Compal Electronics, Inc.		
Title		
BT PORT and MDC		
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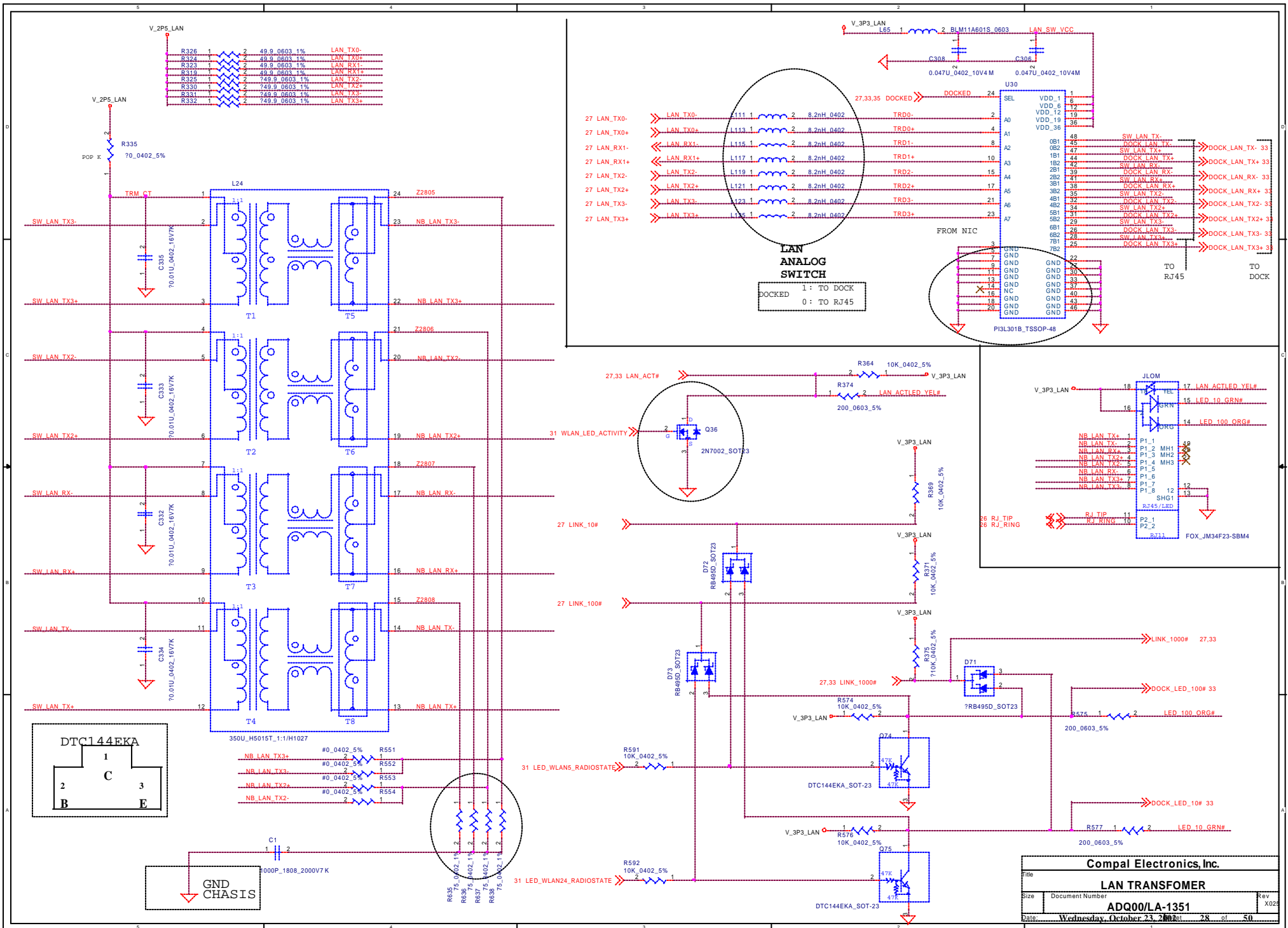


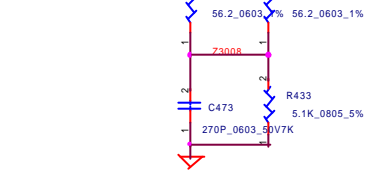
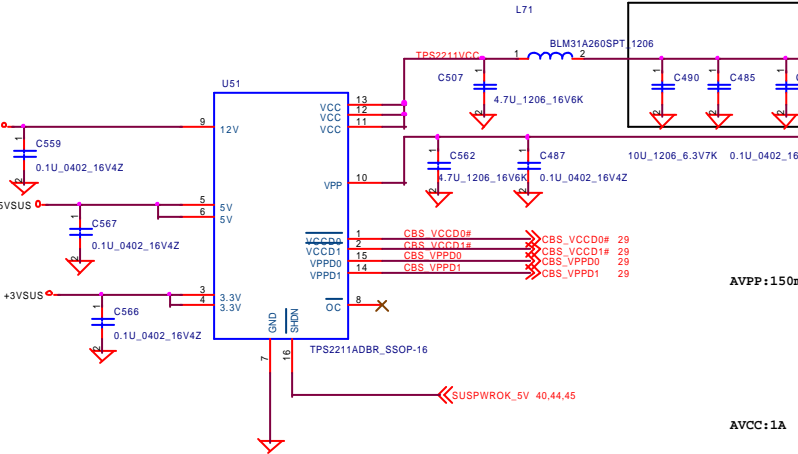
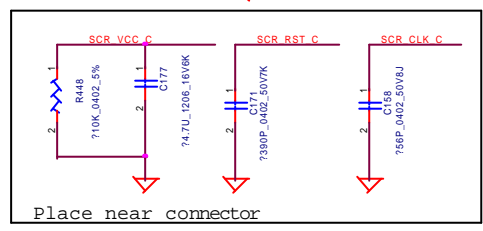
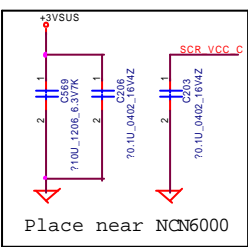
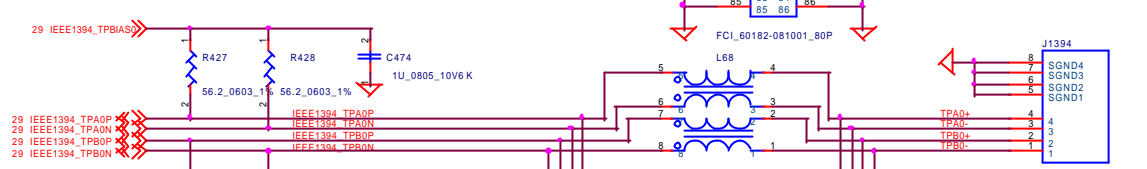
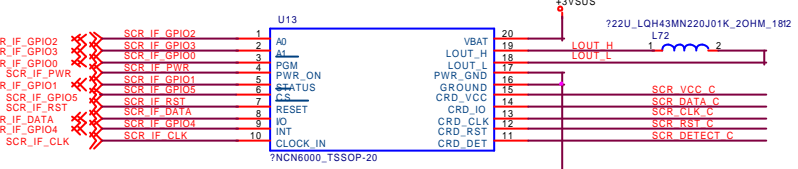
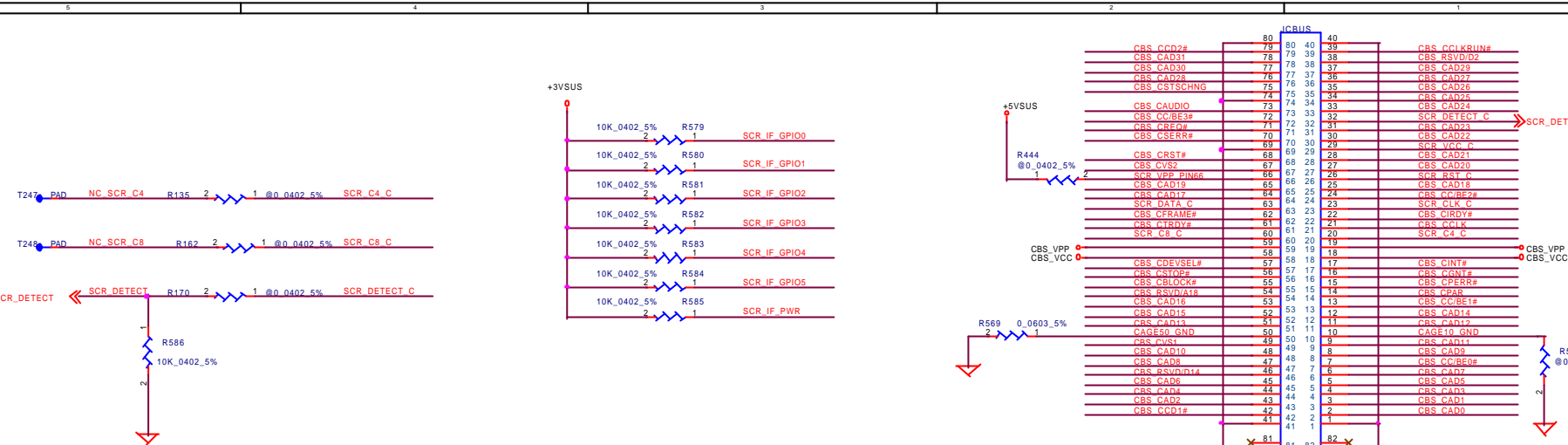
PU R548,EECLK run on 376K for 5705M

If using 93C46 4K ROM depop R548

POP 4401

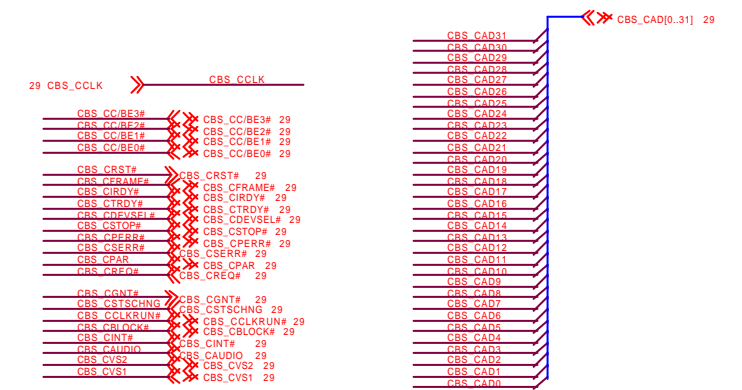
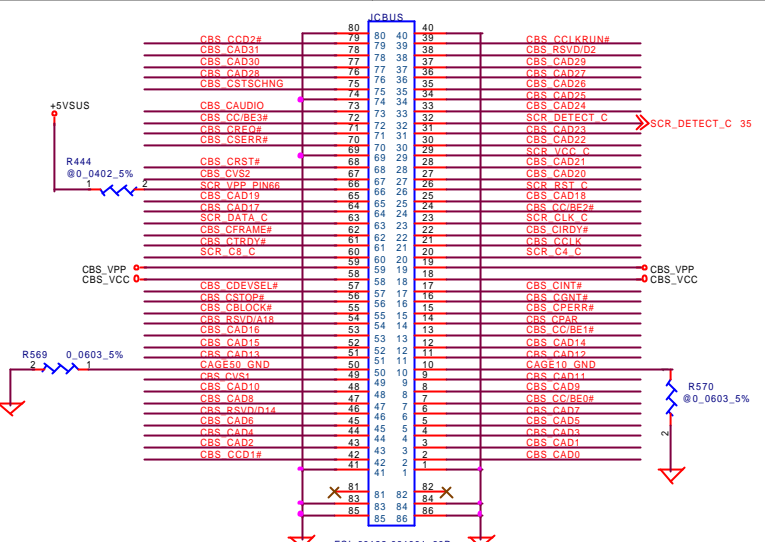
Compal Electronics, Inc.		
ETHERNET		
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SHDN#	VPPD1	VPPD0	CBS_VPP
1	0	0	0V
1	0	1	CBS_VCC
1	1	0	12V
1	1	1	Hi-Z
0	X	X	Hi-Z

SHDN#	VCCD1#	VCCD0#	CBS_VCC
1	0	0	0V
1	0	1	3.3V
1	1	0	5V
1	1	1	0V
0	X	X	Hi-Z

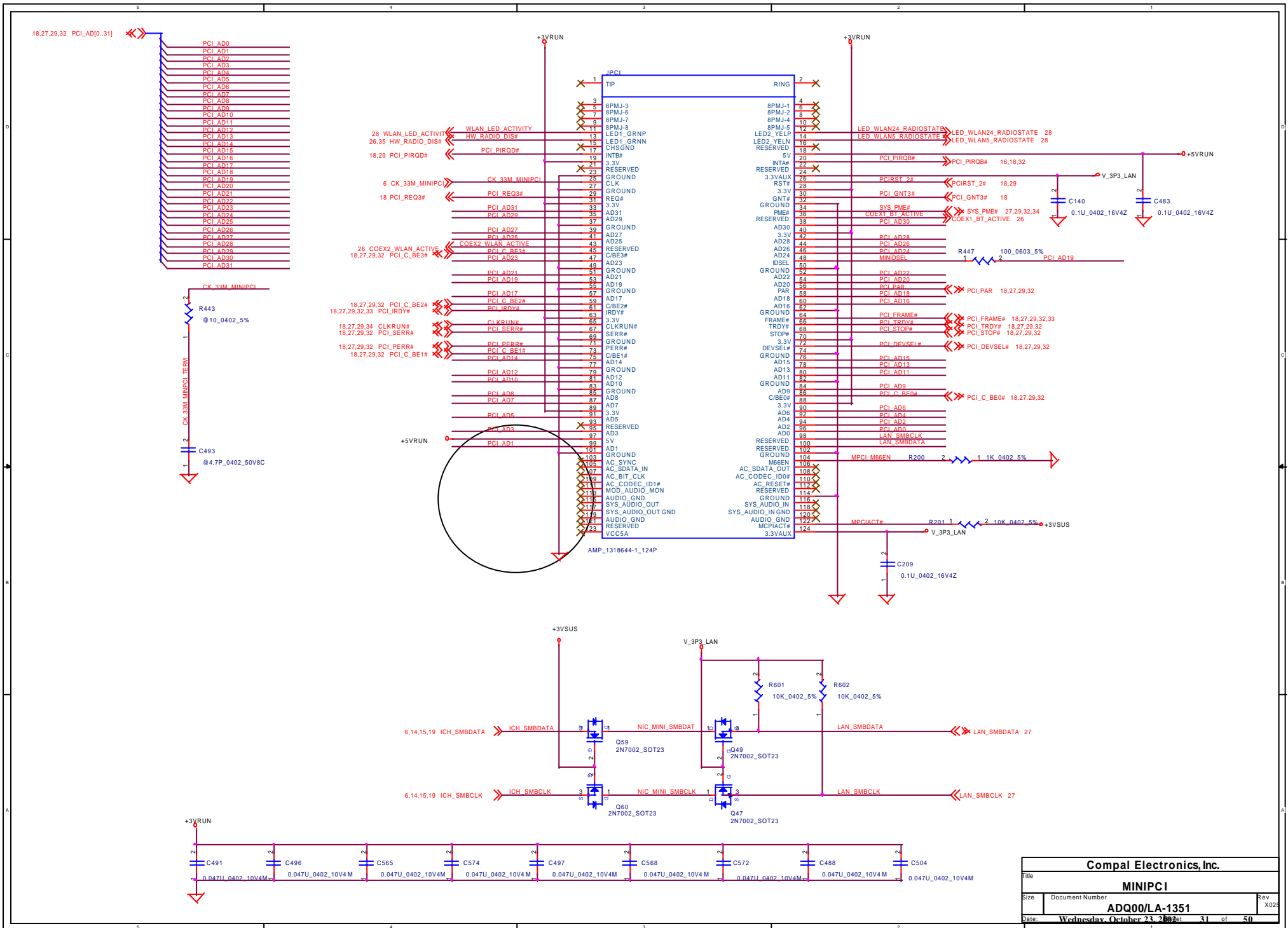


Compal Electronics, Inc.

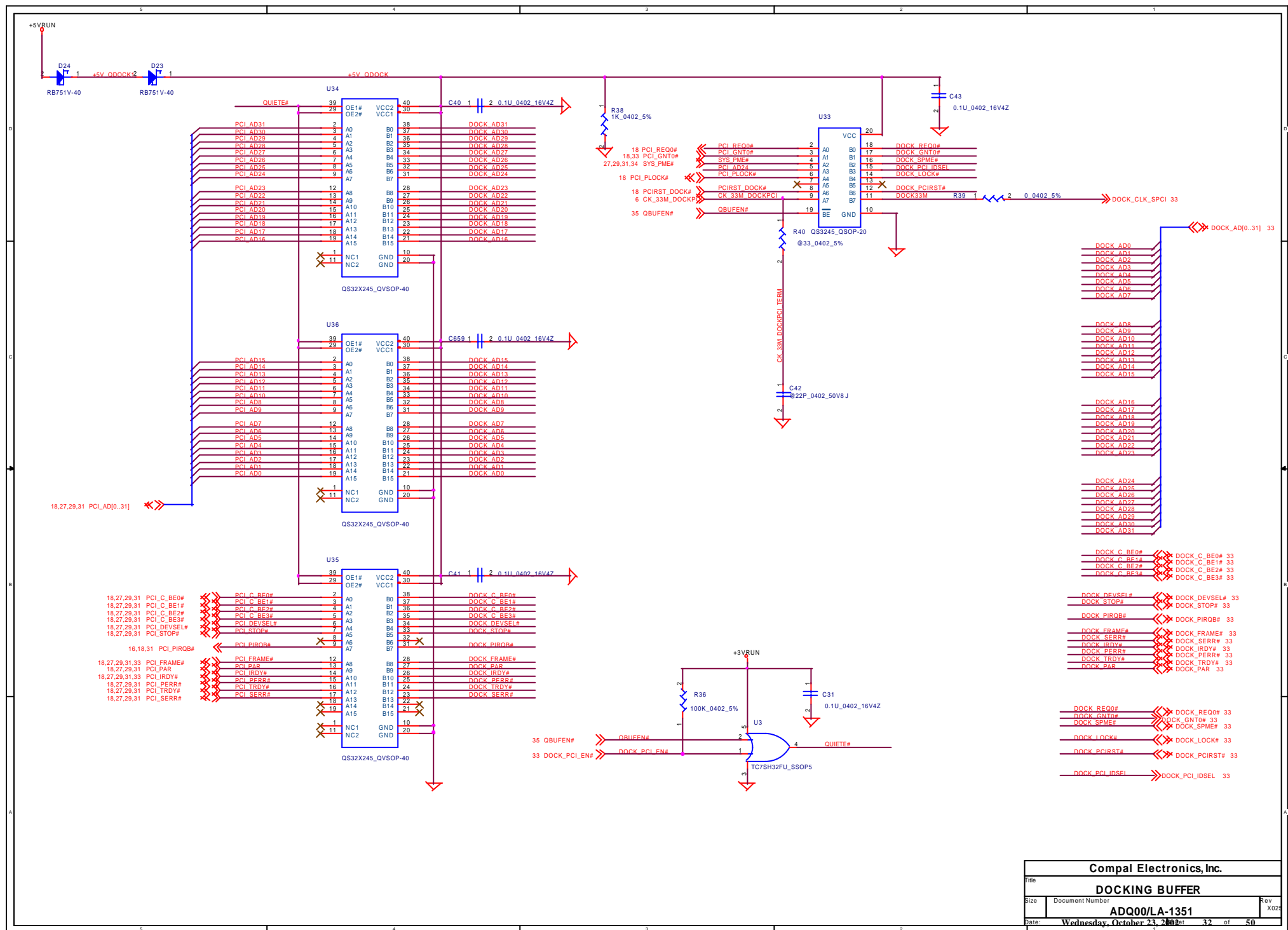
CardBus Socket

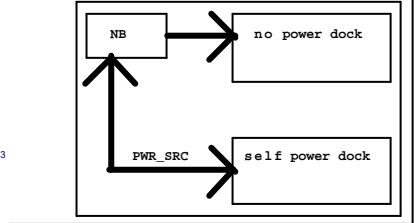
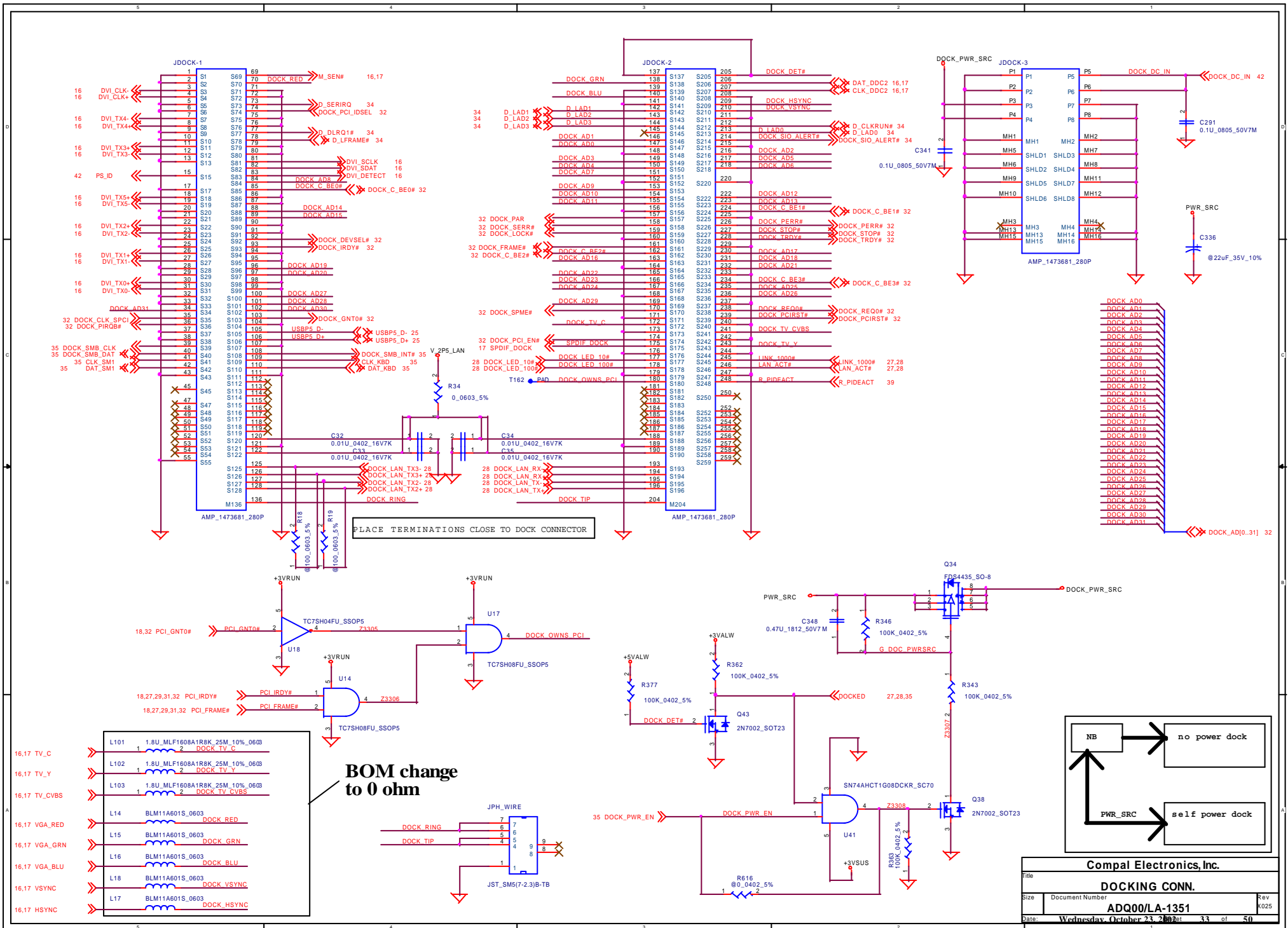
ADQ00/LA-1351

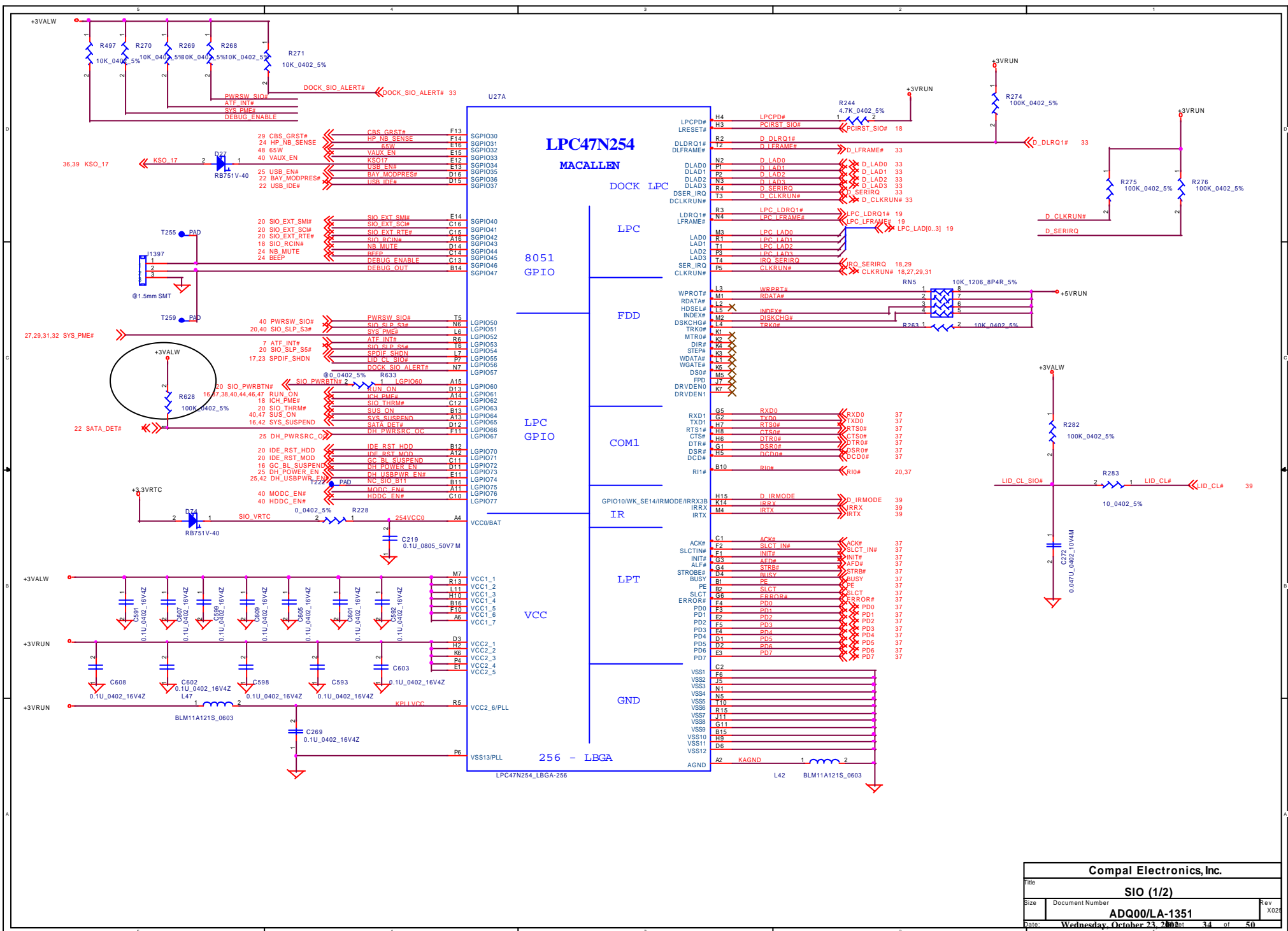
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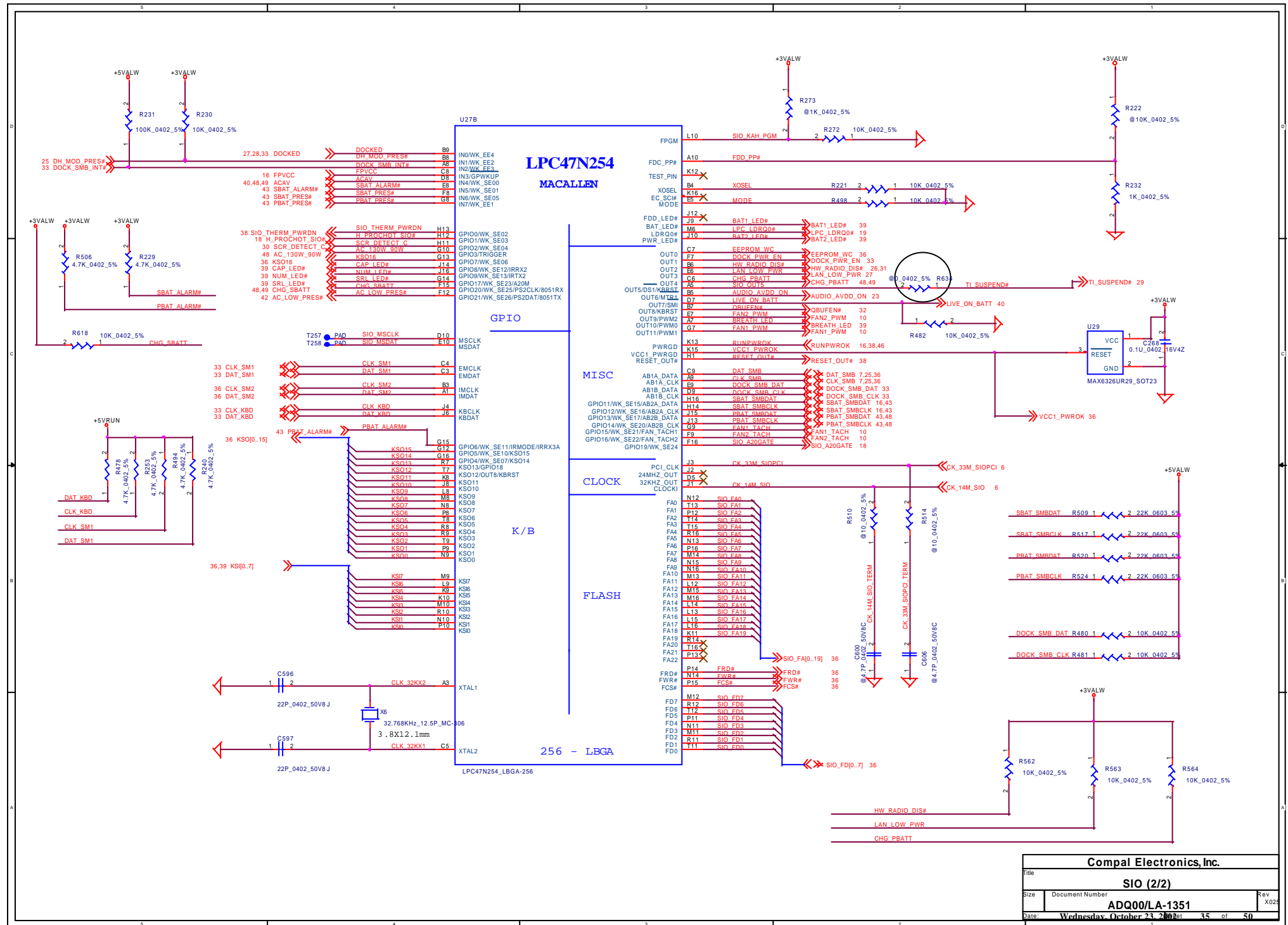


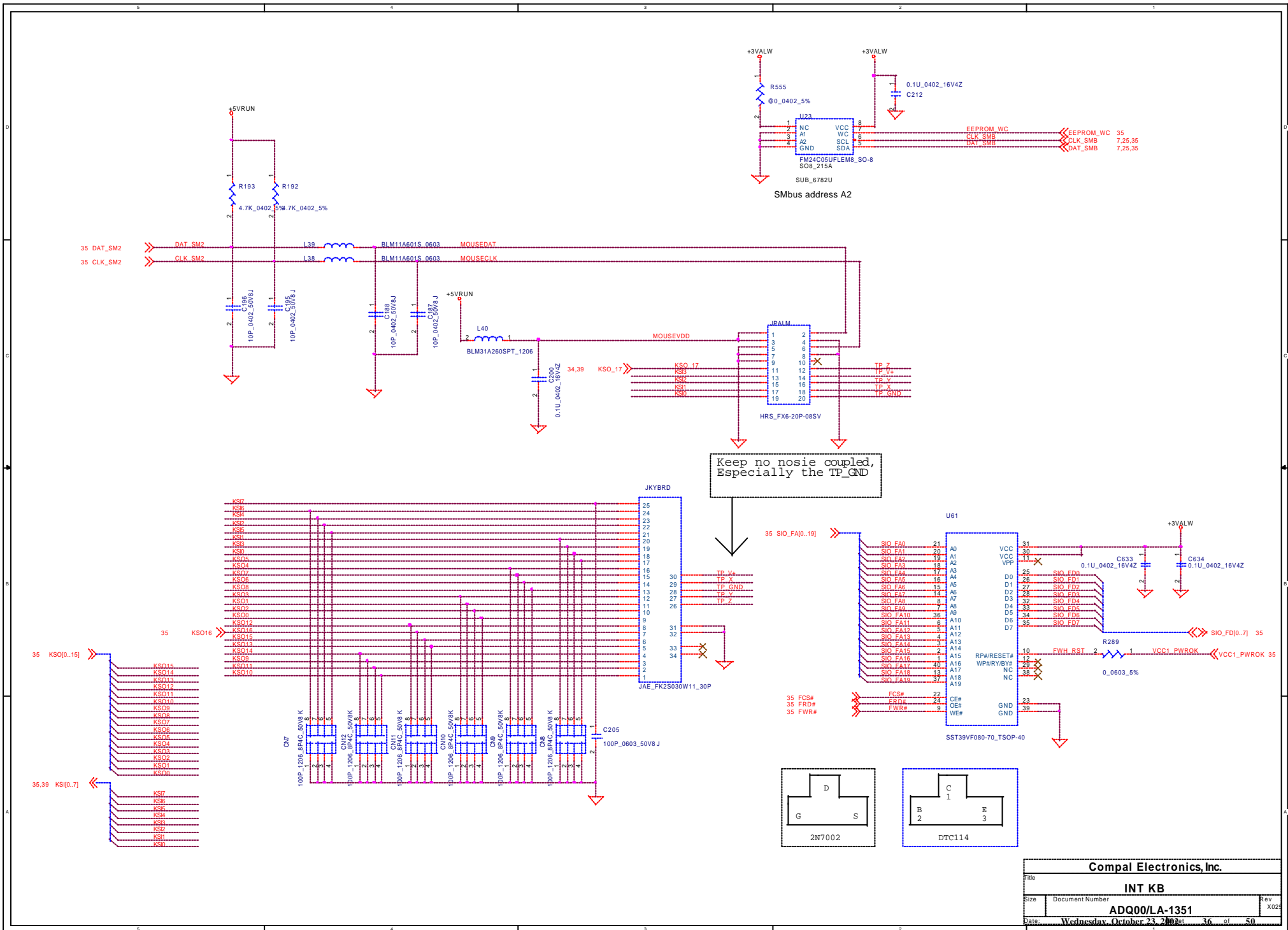
Compal Electronics, Inc.		
MINIPCI		
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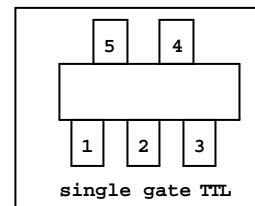
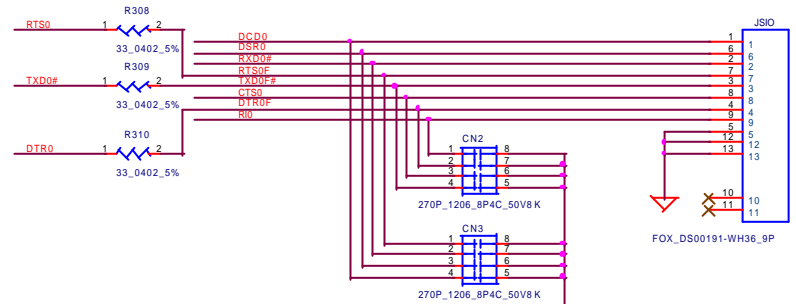
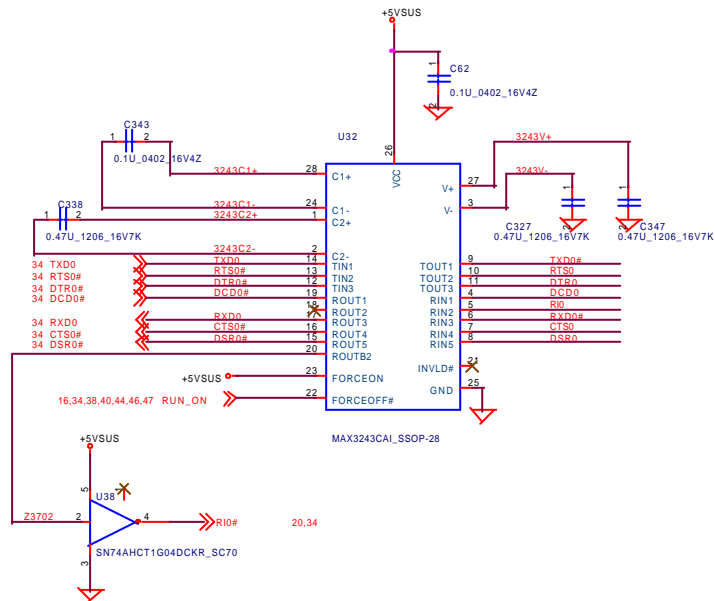
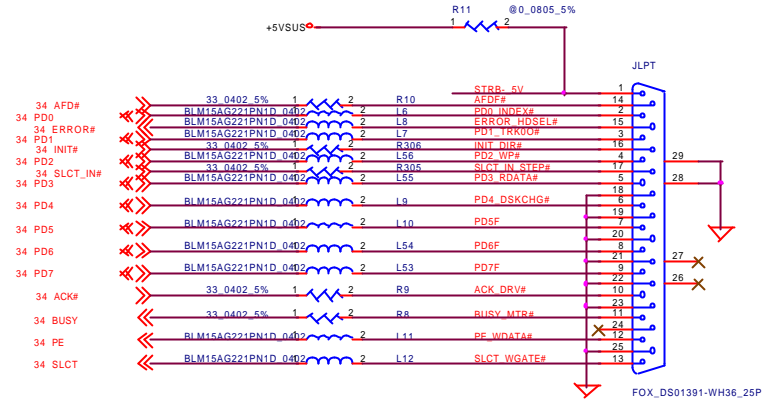
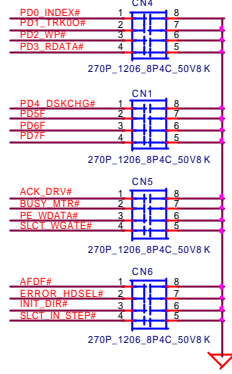
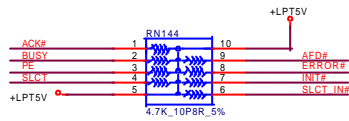
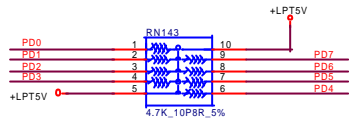
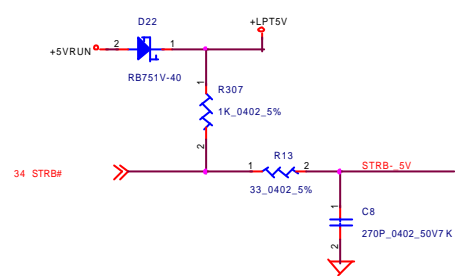


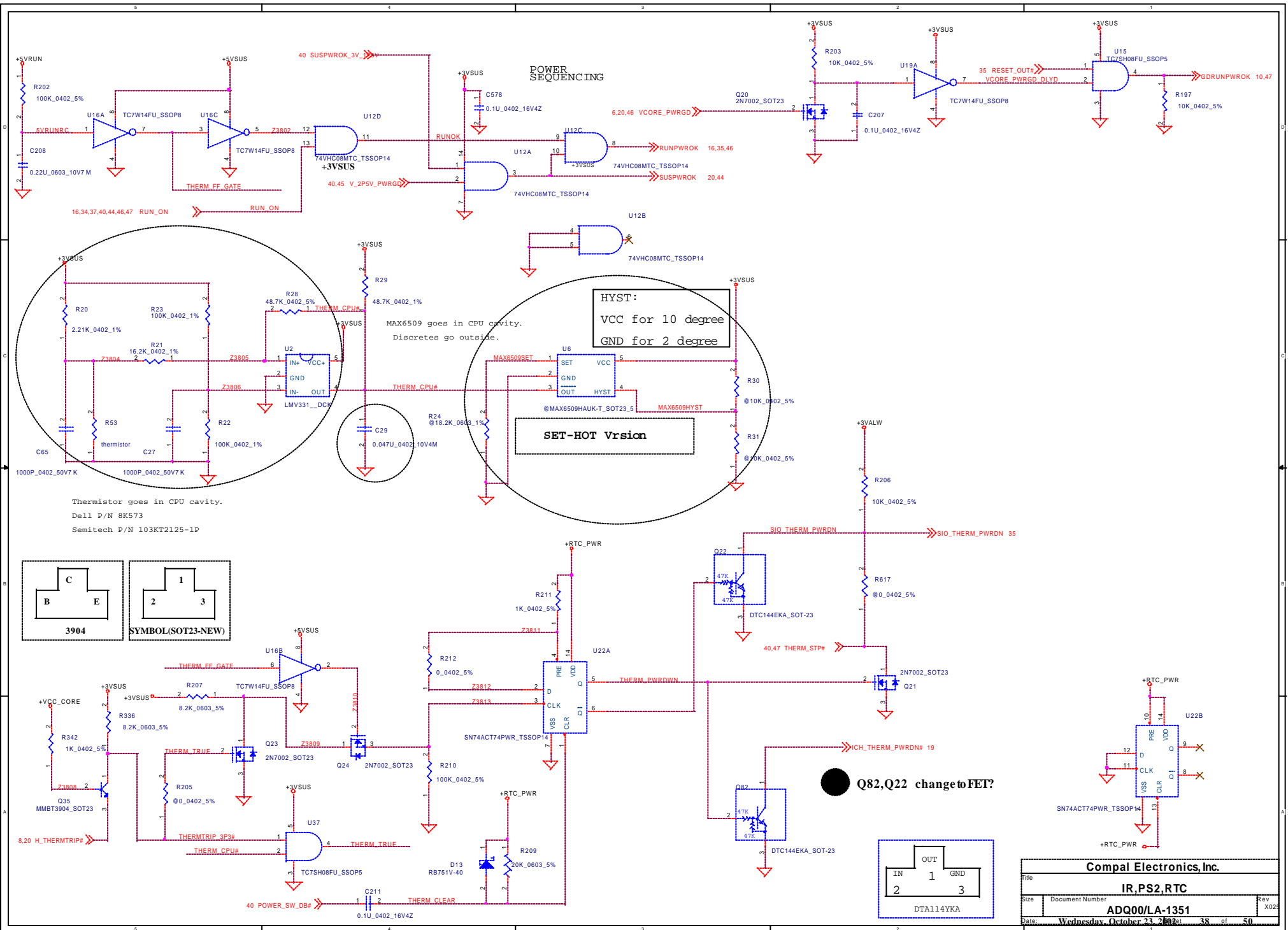




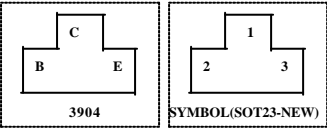


Parallel Port

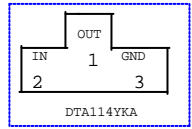




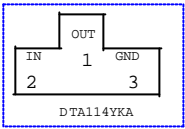
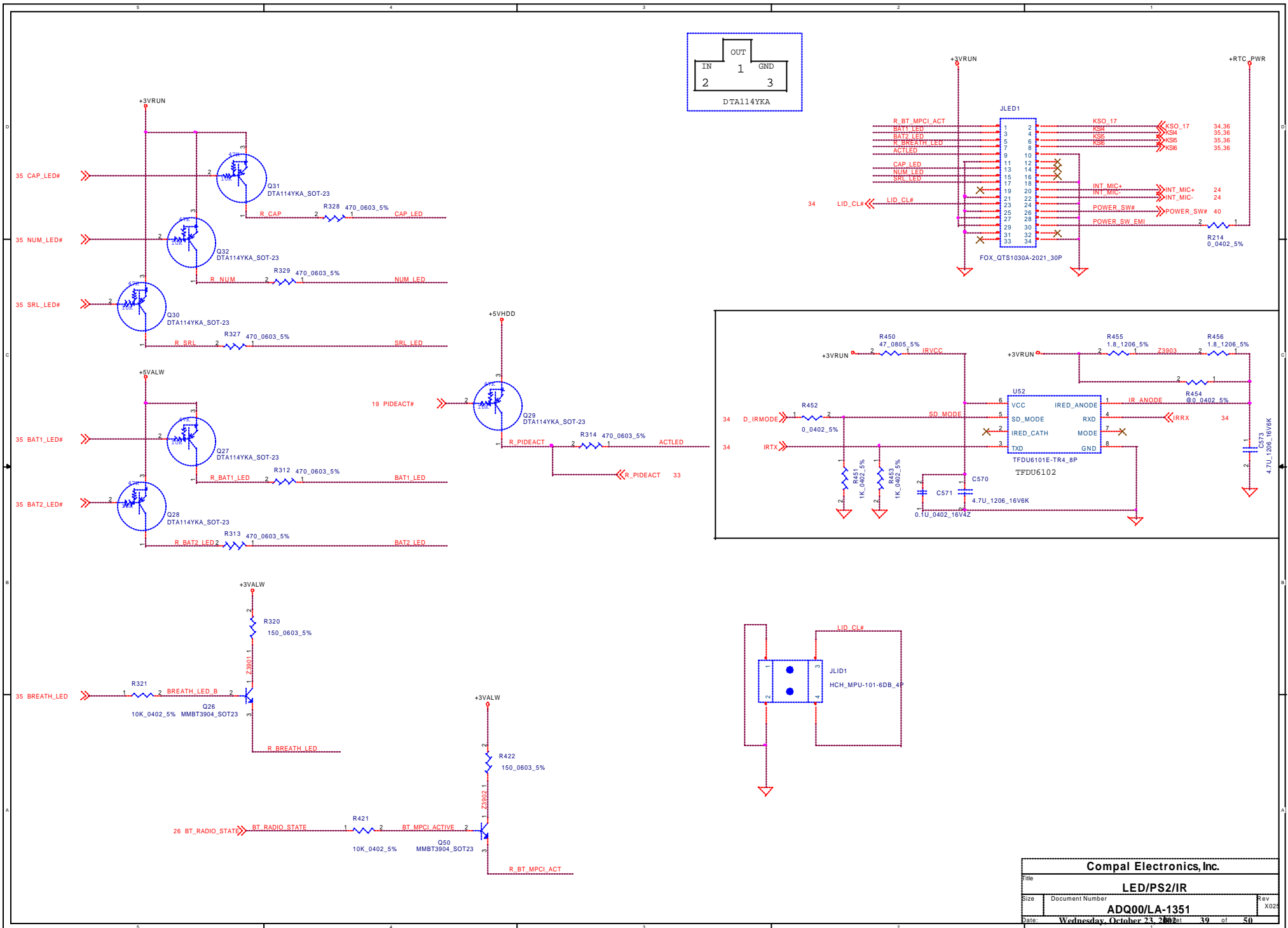
Thermistor goes in CPU cavity.
 Dell P/N 8K573
 Semitech P/N 103KT2125-1P



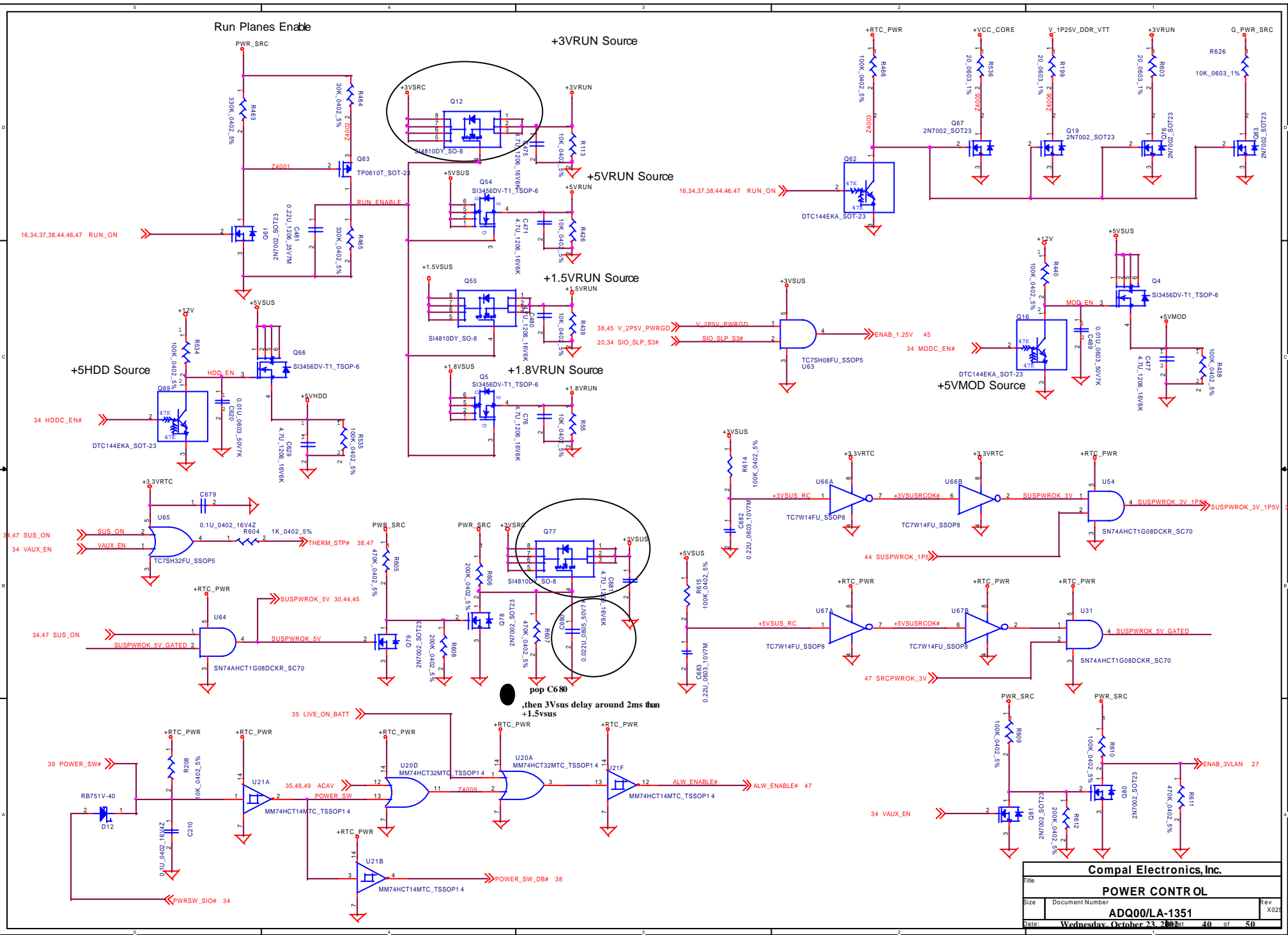
Q82, Q22 change to FET?

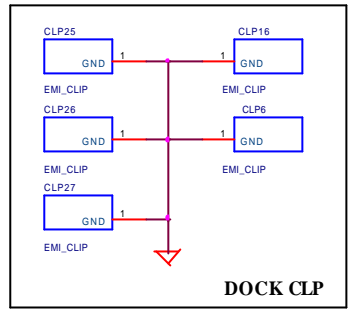
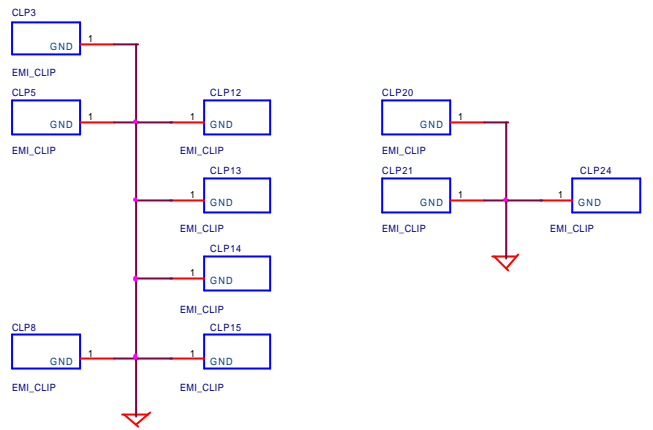


Compal Electronics, Inc.		
IR, PS2, RTC		
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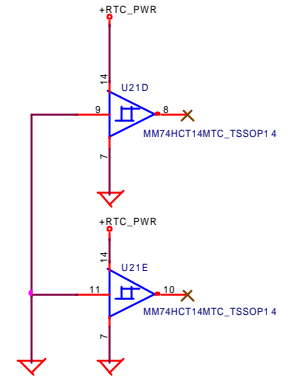
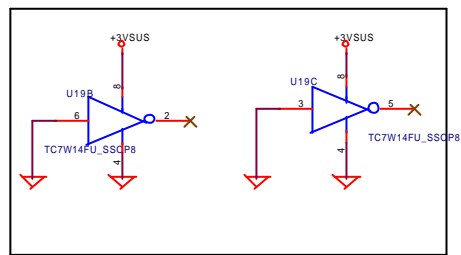
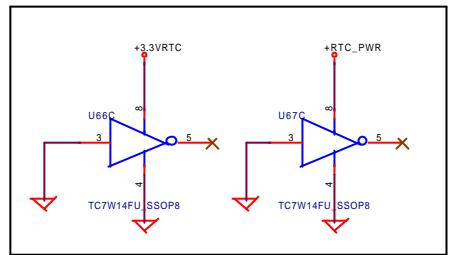
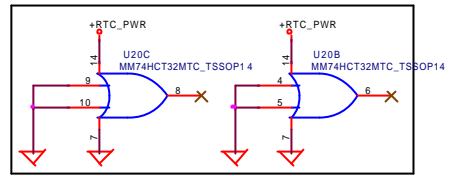
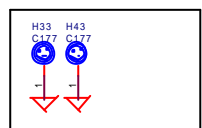
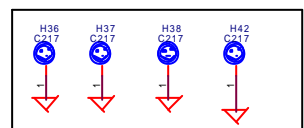
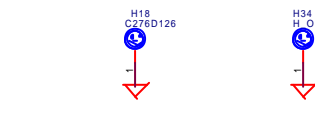
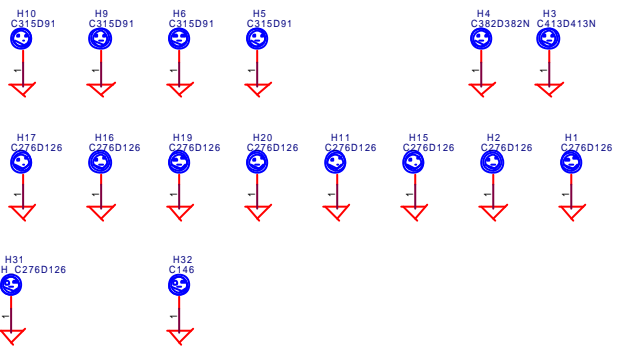
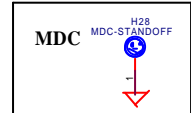
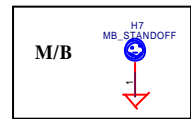
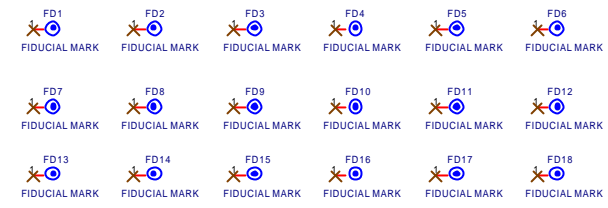
Compal Electronics, Inc.		
Title		
LED/PS2/IR		
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DOCK CLP

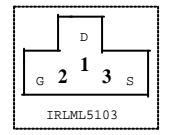
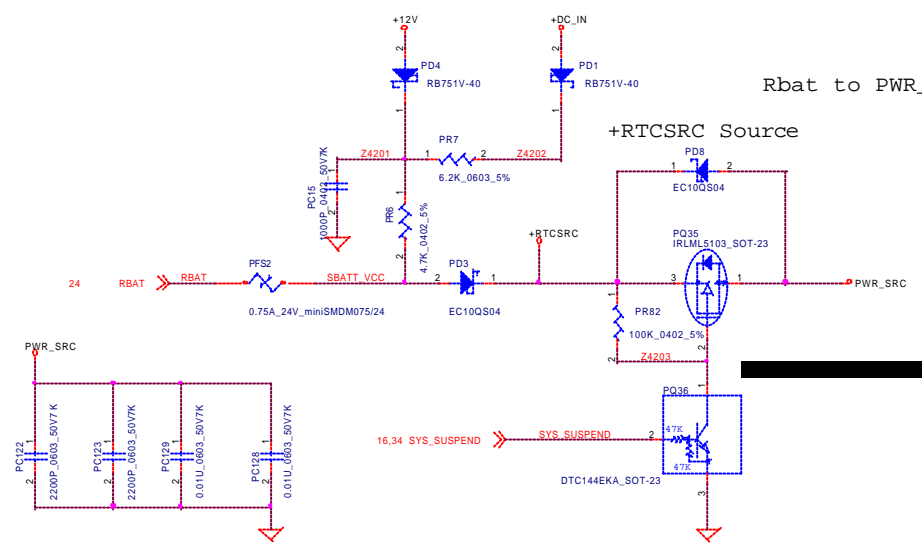
Fiducial Mark



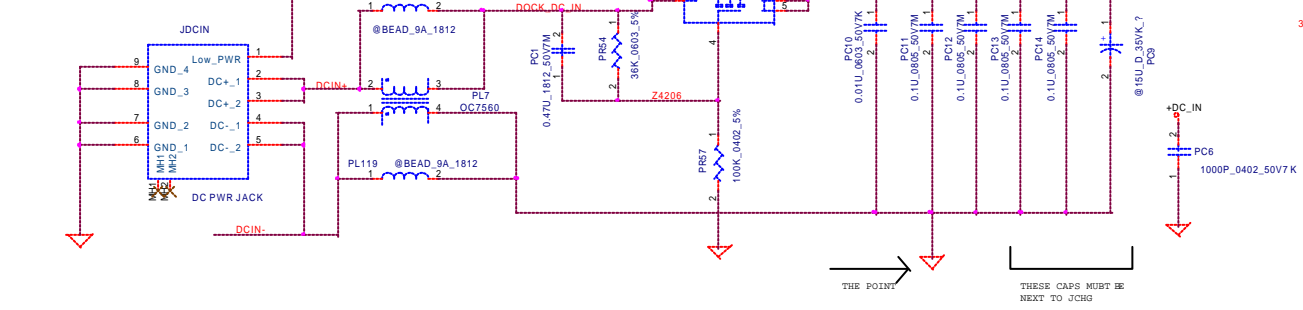
Compal Electronics, Inc.		
PAD and Standoff		
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Rbat to PWR_SRC Enable

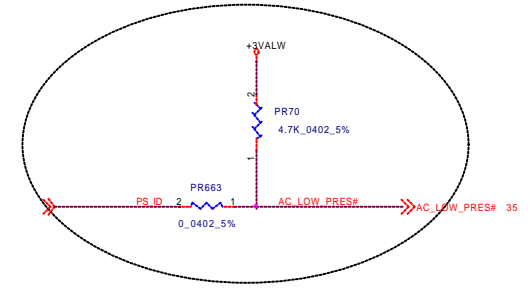
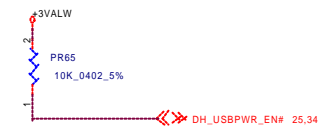
+RTCSRC Source



Z-series AC Adaptor Connector



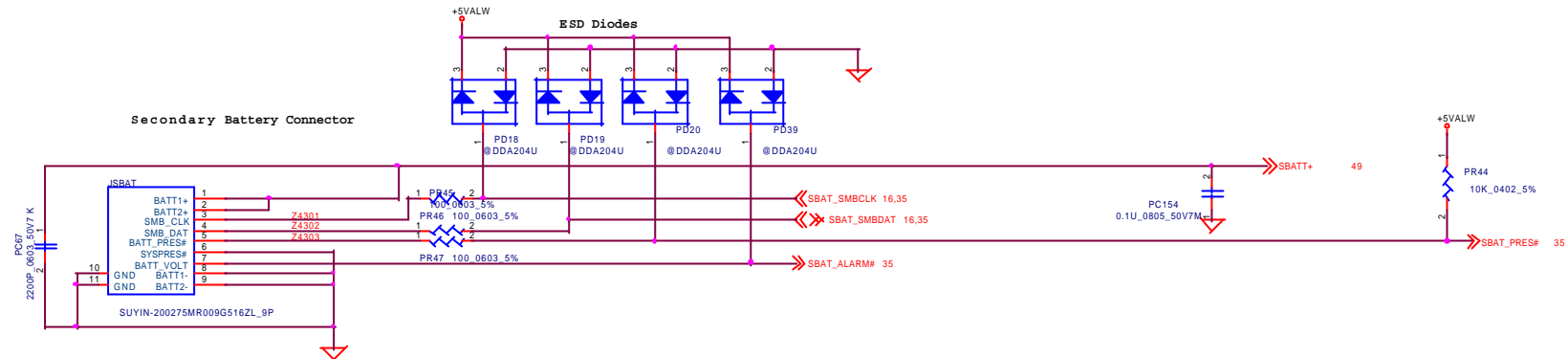
NOTE: *THE POINT LOCKED AT PS MODULE



Old Low-Power Adapter Detection

Compal Electronics, Inc.		
Title DC-IN		
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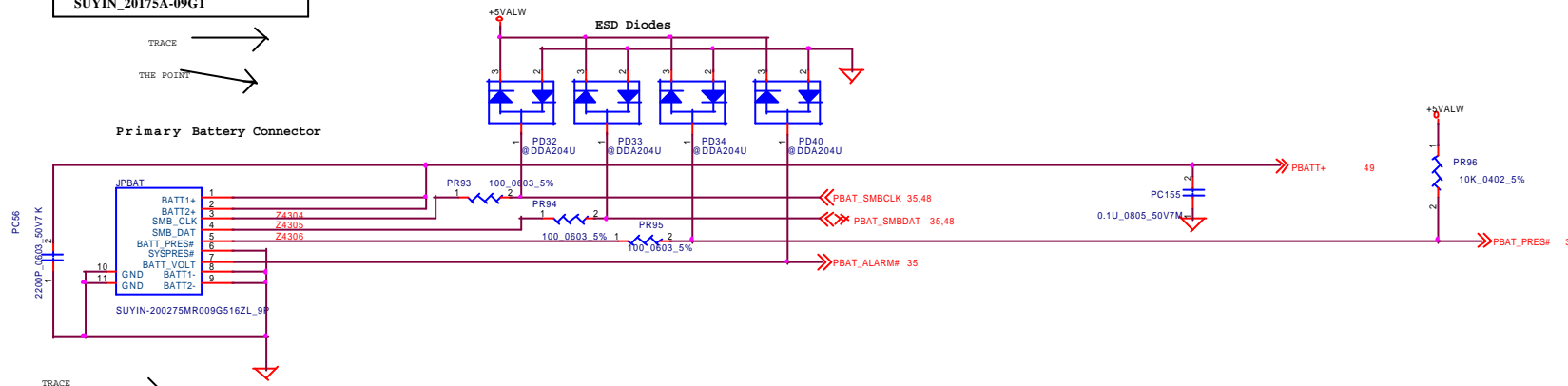
Secondary Battery Connector



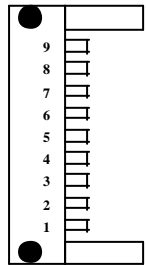
SUYIN_20175A-09G1

TRACE →
THE POINT →

Primary Battery Connector

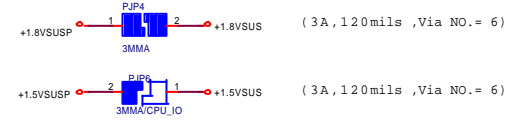
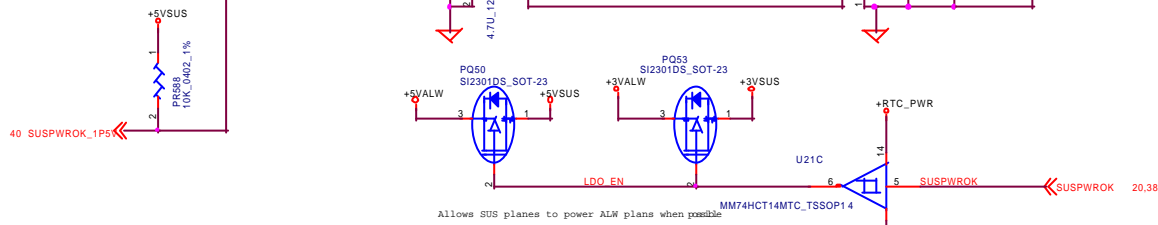
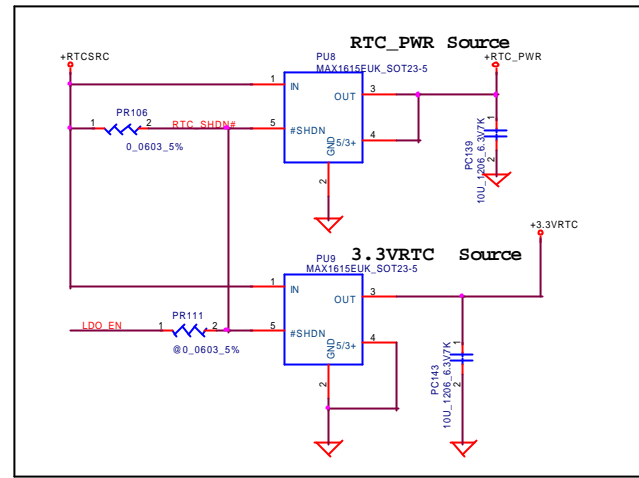
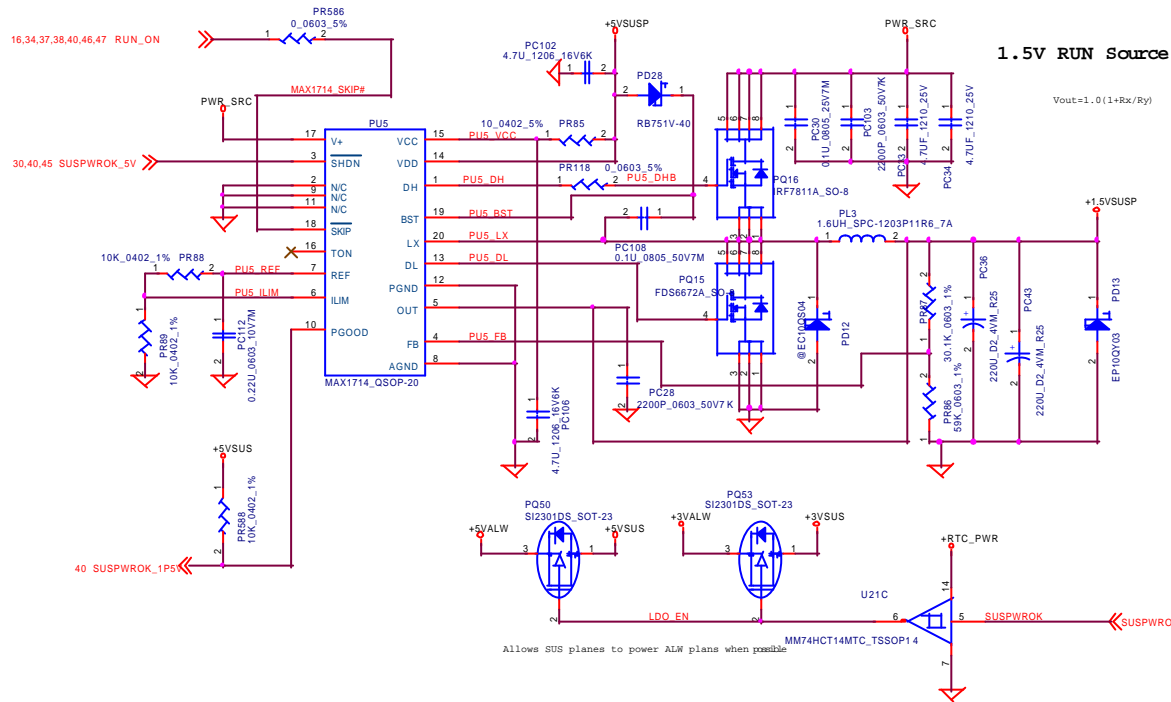


TRACE →
THE POINT →

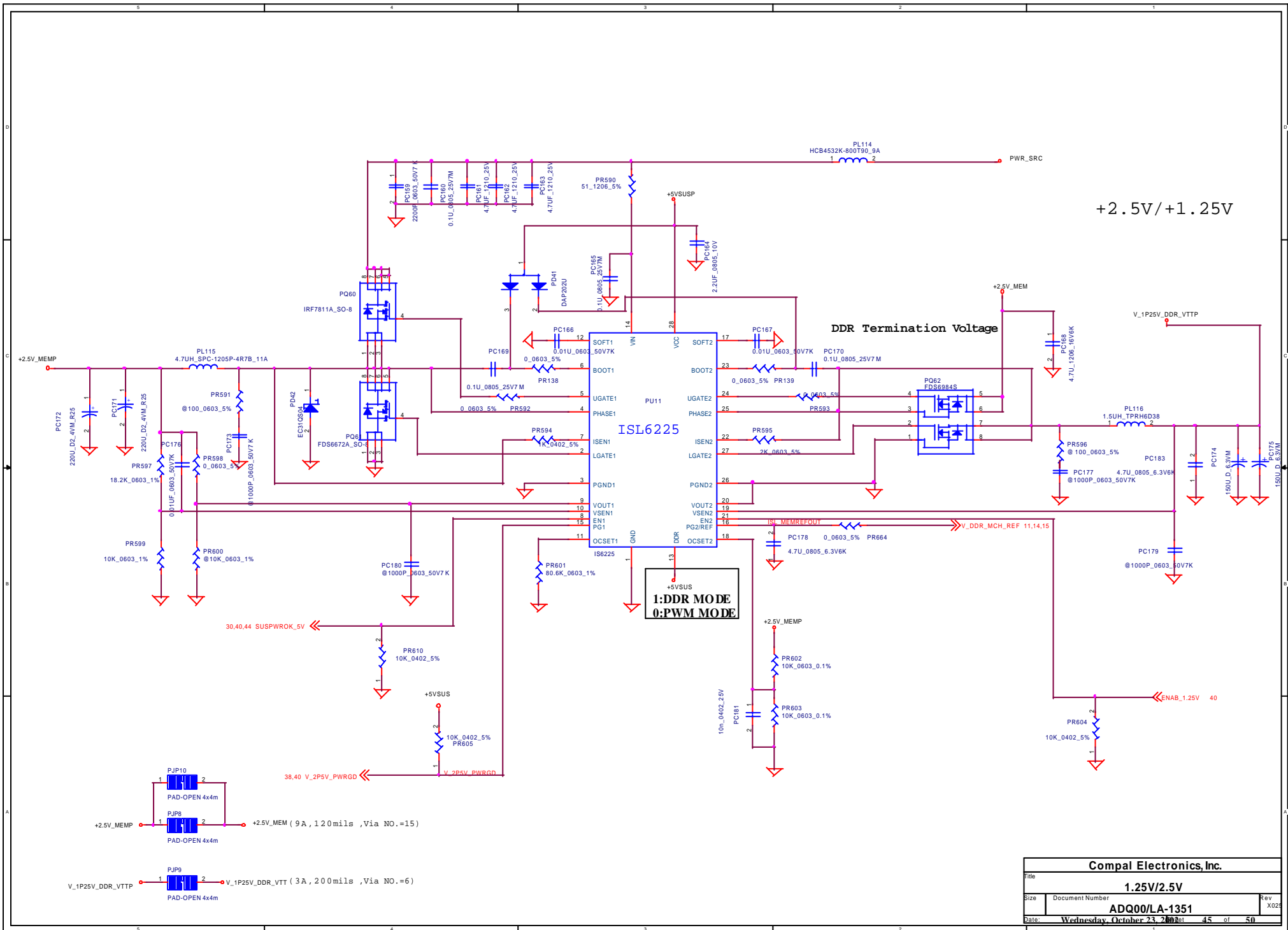


SUYIN_20175A-09G1
TOP view

Compal Electronics, Inc.		
Title Battery CONN.		
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Compal Electronics, Inc.		
Title 1.5V/1.8V		
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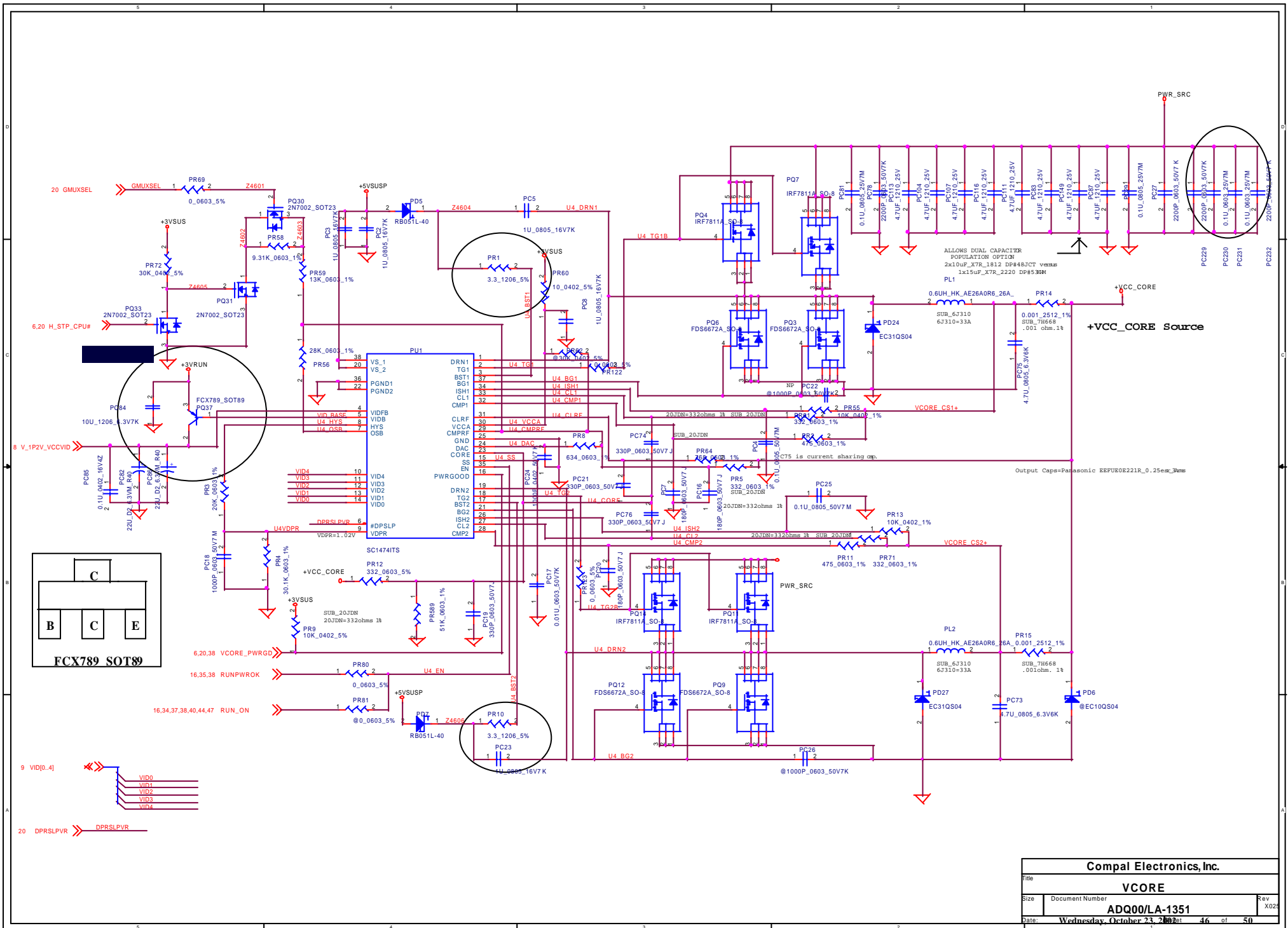


+2.5V/+1.25V

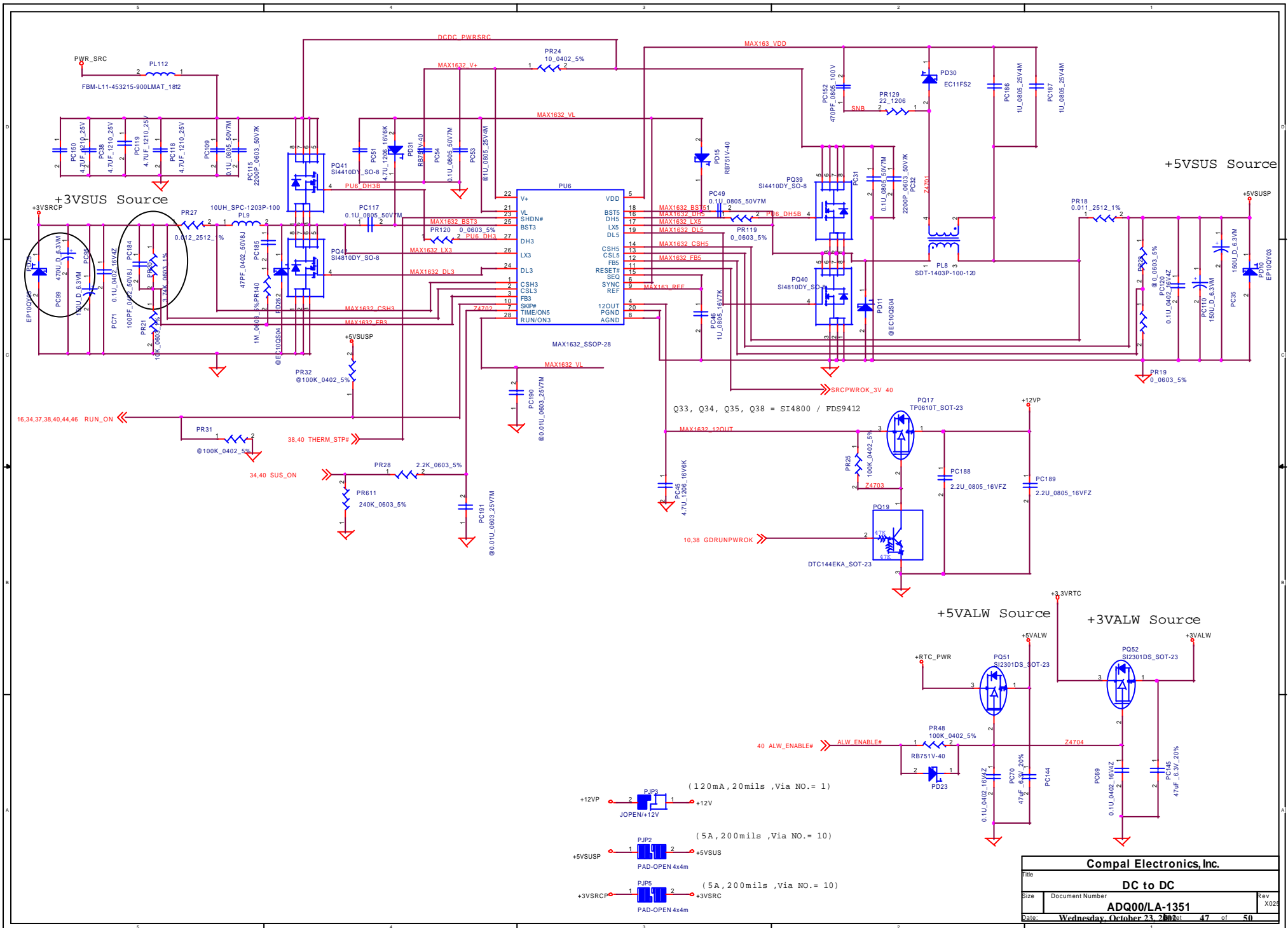
DDR Termination Voltage

1:DDR MODE
0:PWM MODE

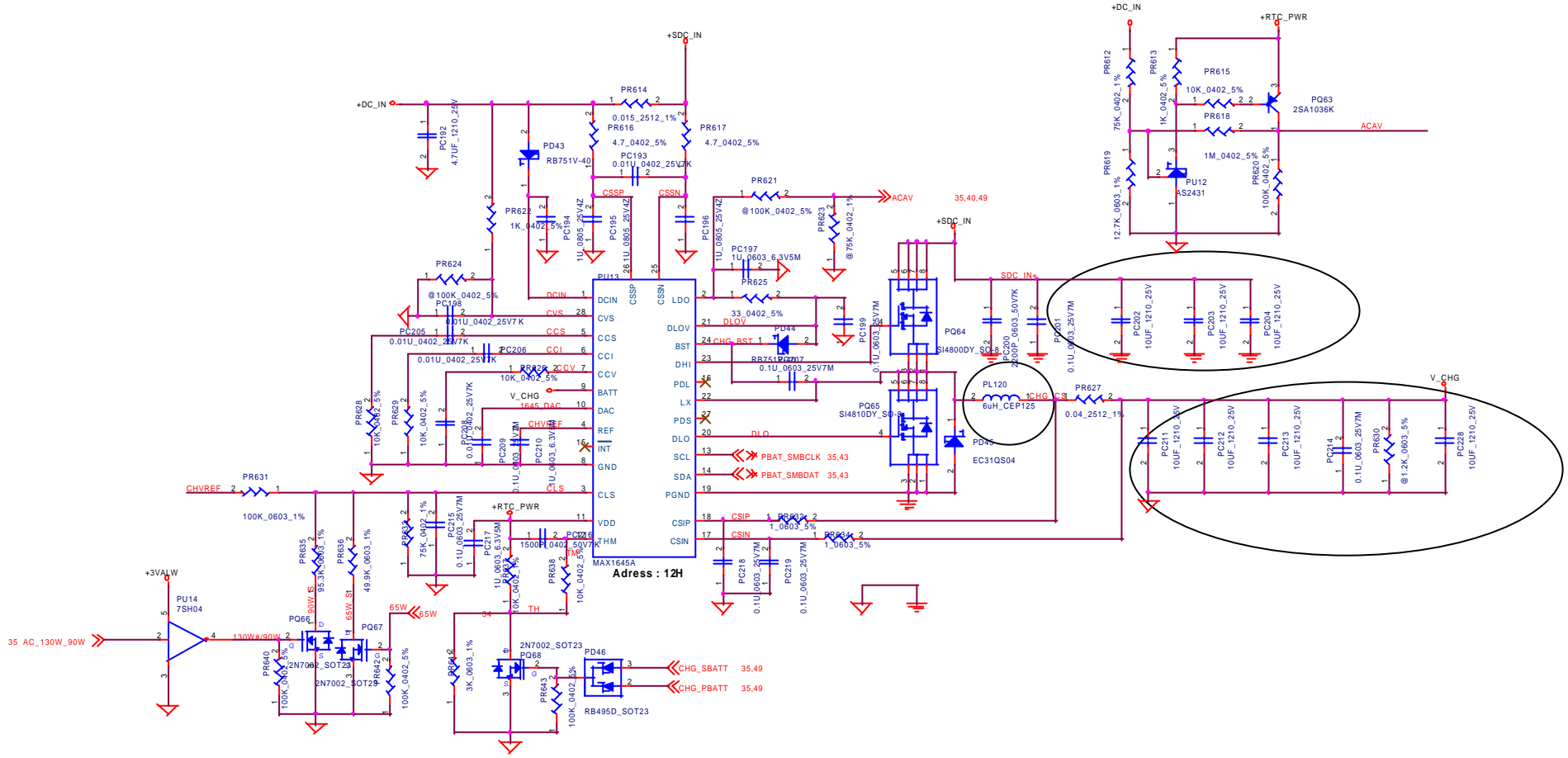
Compal Electronics, Inc.		
Title 1.25V/2.5V		
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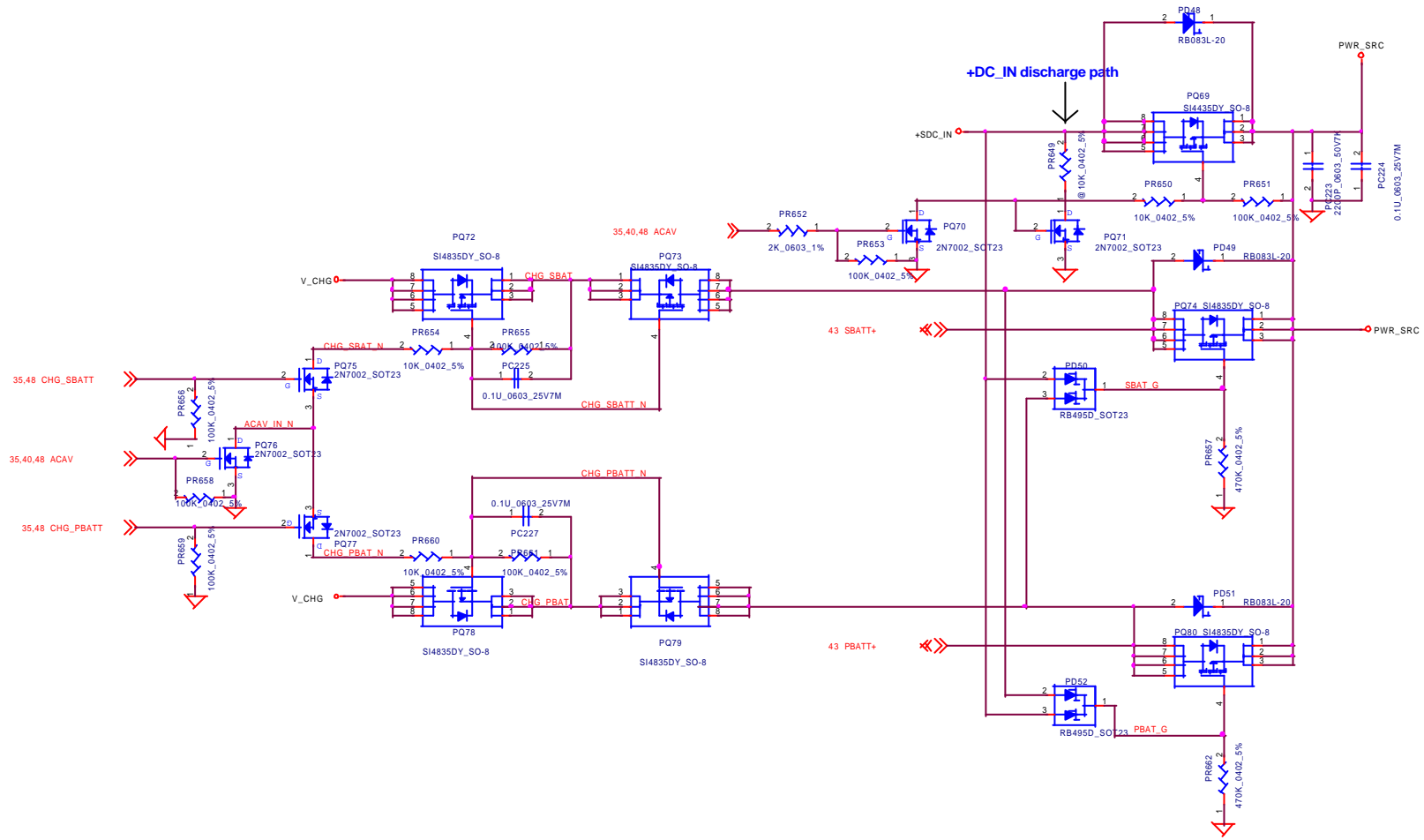
Compal Electronics, Inc.		
VCORE		
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Compal Electronics, Inc.		
DC to DC		
ADQ00/LA-1351		
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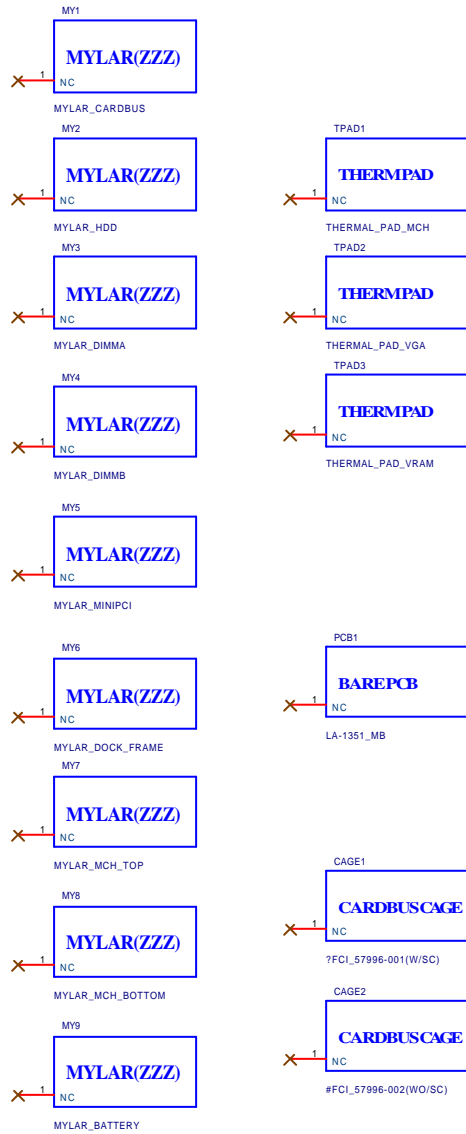
	65W (2.53A)	90W (4.03A)	130W (5.85A)
65W	H	L	L
130W#/90W	H	H	L



Compal Electronics, Inc.		
CHARGER		
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**THIS PAGE IS ONLY FOR
B.O.M. INFORMATION**

PIR



ITEM	PAGE	REV.	NOTE		
1	9	X025	remove CPU VCCID jumper		
2	19	X025	Change R537 to 1K for PIDEACT# PU		
3	20	X025	remove SIO_LID_EC# signal ,PU 1CH4GPIO to +3VRUN		
4	21	X025	change JMOD1 pin8,10,14,16,9,11, to NC,conect SATA_DET# to pin13	reserve C693,R629,R630 for CD AUDIO termination	
5	25	X025	change Q1,F1,F2,L25 part to meet Doghouse power current requirement	add R639 for USB port 3 power enable, reserve R640	
6	27	X025	add L109, L110 for BCM4401 PCI power for WOL issue		
7	28	X025	add eight 8.2uH inductor to TX/RX line	seperate RN1 to 4 small resistors	Change Q36 to 2N7002
8	29	X025	remove D11 for TI_SUSPEND#		
9	31	X025	Change JPC11 pin109 and pin 123 to NC and remove R457,C576		
10	34	X025	add R628 PU to U27 pin D12		
11	35	X025	reserve R634 for TI_SUSPEND#		
12	38	X025	change OTP to discrete solution		
13	40	X025	change Q12 and Q77 to SI4810		
14	42	X025	remove AC LOW PRES circuit		
15	46	X025	change PQ37 to FCX789	remove PC147 change PR1,PR10 to 3.3ohm	add PC229,PC230,PC231,PC232
16	47	X025	change PR20 to 3.74K		
17	48	X025	addPC228,change C202,PC203, PC204,PC211,PC212,PC213,PC214 to 10uF/25V	Change PL120 to 6uH	