

NWQAA

Marseille 10

LA-6061P REV 2.0 Schematic

Intel Processor (ARD) / PCH (HM55)
2010-03-24 Rev 2.0

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

BTO Option Table

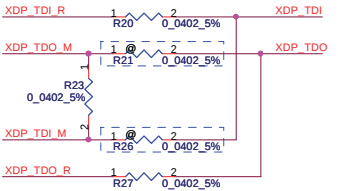
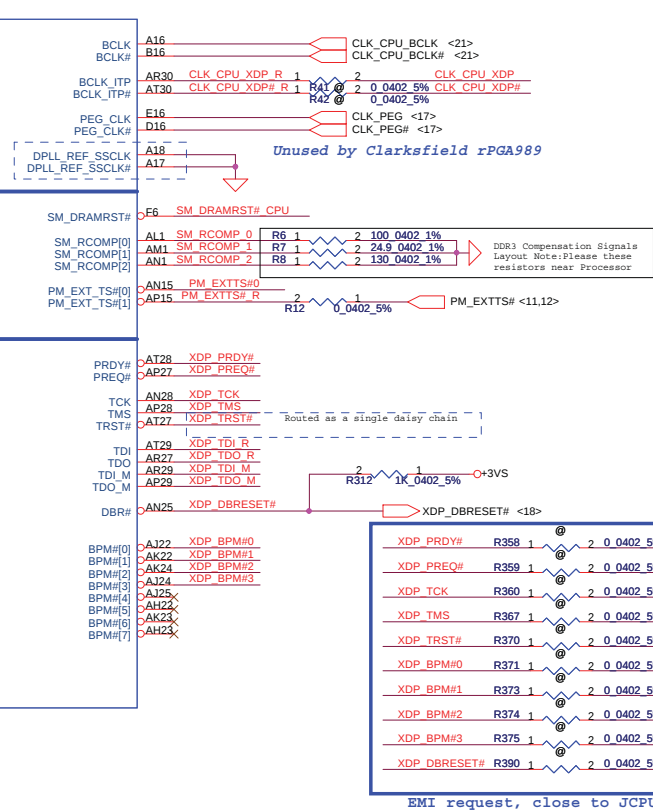
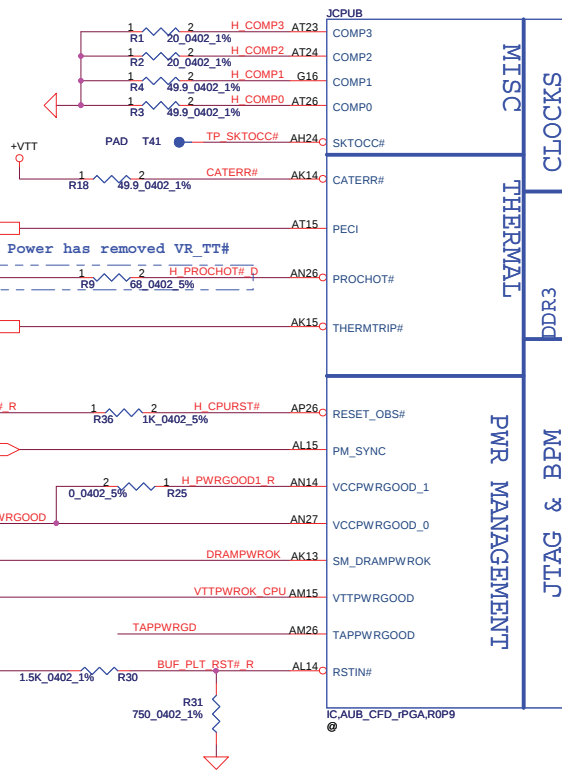
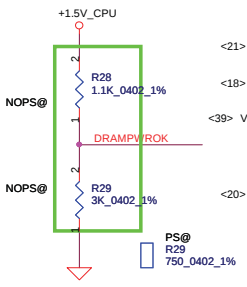
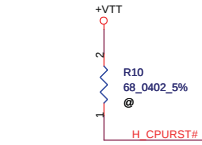
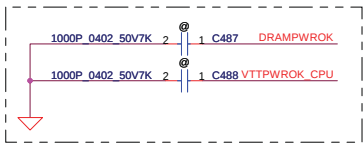
Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FPE@	MDC@	CIR@	KBL@

Function	Felica	BLUE TOOTH	G-SENSOR	Camera & Mic	HDMI		Card reader	
description	Felica	BLUE TOOTH	G-SENSOR	Camera & Mic	HDMI		JMB385C/389C	
explain	Felica	BLUE TOOTH	G-SENSOR	Camera & Mic	UMA	CEC	JMB385C	JMB389C
BTO	FELICA@	BT@	GSENSOR@	CAM@	IHDMI@	CEC@	JMB385@	JMB389@

Function	S3 Power Saving		New Card
description	S3 Power Saving		New Card
explain	No Power Saving	Power Saving	New Card
BTO	NOPS@	PS@	NEW@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

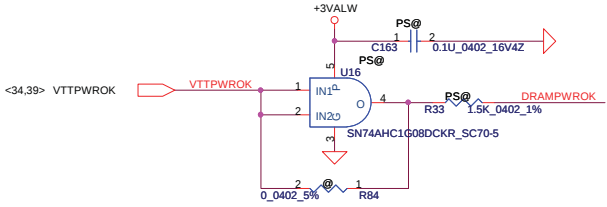
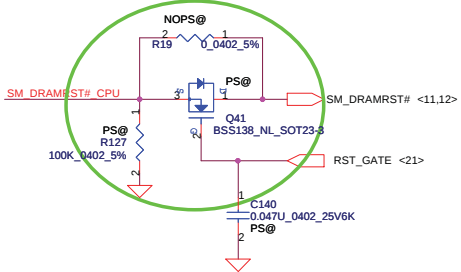
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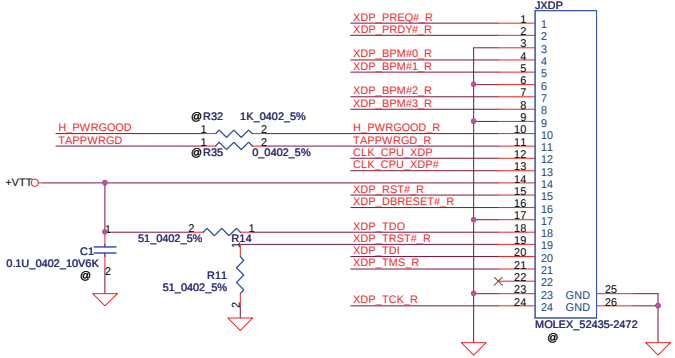
JTAG MAPPING

Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

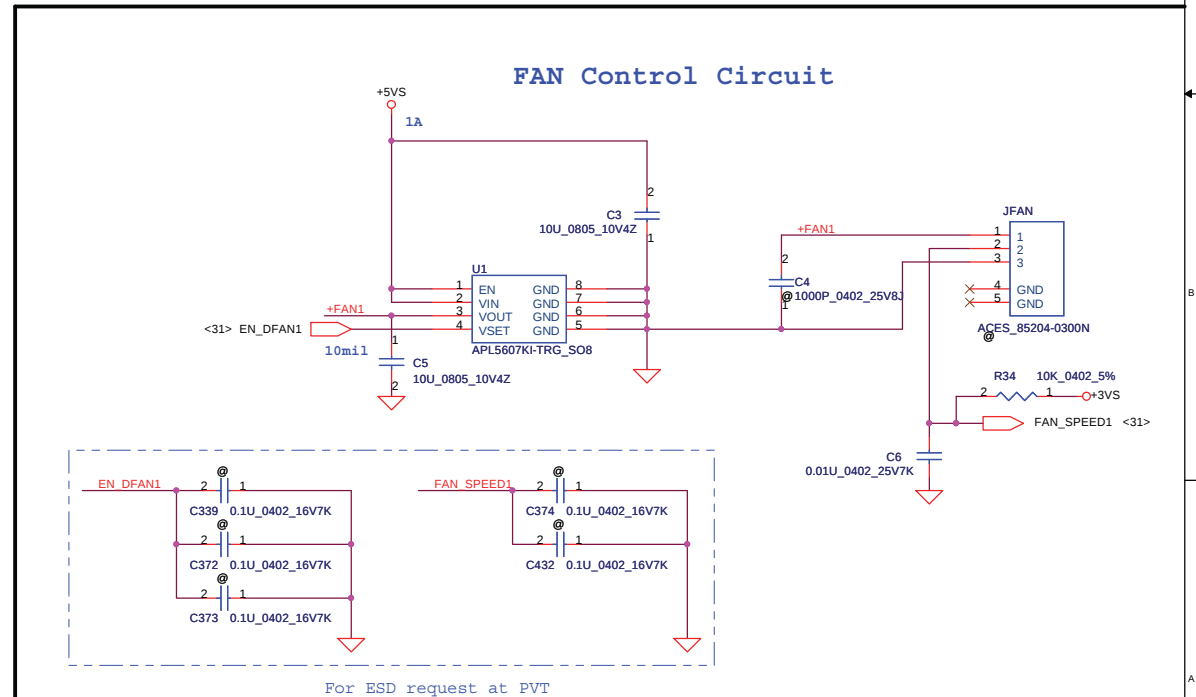
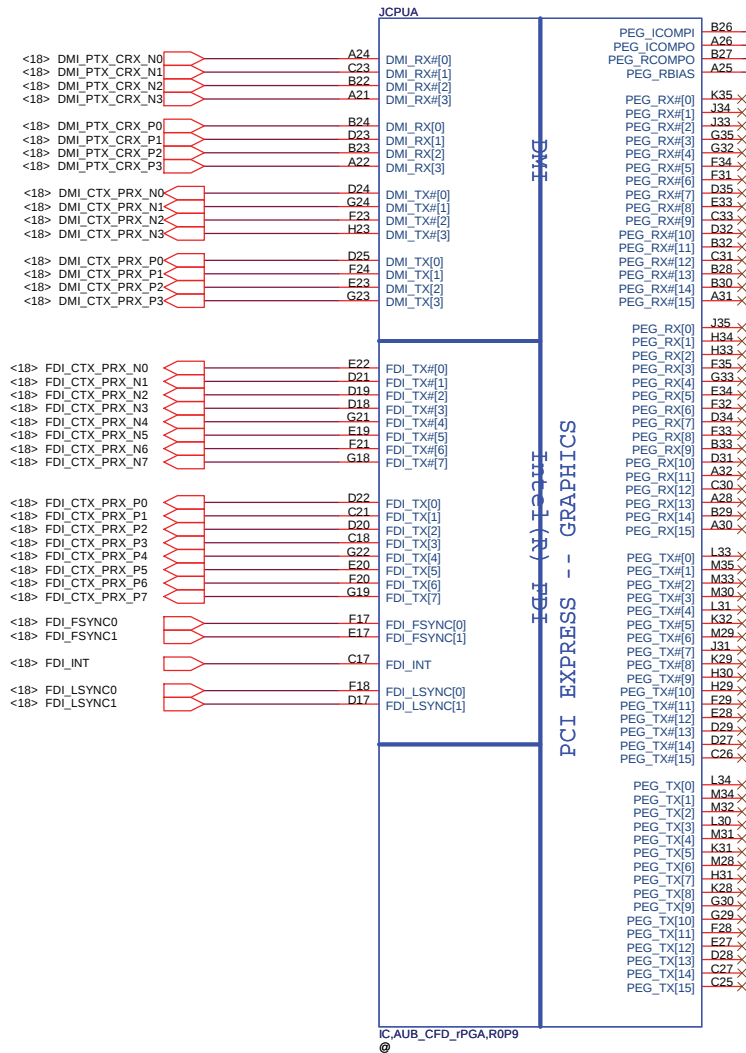
For S3 CPU Power Saving



XDP Connector



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[illegible]

PCB layout showing the addition of a decoupling capacitor C496. The top section shows a power plane with a +GFX_CORE net connected to a series of capacitors (C271, C95, C127, C117, C96, C120, C86) connected to ground. The bottom section shows a dashed box labeled "Add C496 Co-Layout with C271" containing a capacitor C496 (330U_D2_2VM_R6M) connected to +GFX_CORE and ground. A list of components is shown on the right side of the layout.

Components listed on the right:

- JCPU0
- AT21
- VAXG1
- VAXG2
- AT19
- VAXG3
- AT18
- VAXG4
- AT16
- VAXG5
- AR21
- AR19
- AR18
- VAXG6
- AR16
- VAXG7
- AP21
- VAXG8
- AP19
- VAXG9
- AP18
- VAXG10
- AP16
- VAXG11
- AN21
- VAXG12
- AN19
- VAXG13
- AN18
- VAXG14
- AN16
- VAXG15
- AM21
- VAXG16
- AM19
- VAXG17
- AM18
- VAXG18
- AM16
- VAXG19
- AL21
- VAXG20
- AL19
- VAXG21
- AL18
- VAXG22
- AK21
- VAXG23
- AK19
- VAXG24
- AK18
- VAXG25
- AK16
- VAXG26
- AJ21
- VAXG27
- AJ19
- VAXG28
- AJ18
- VAXG29
- AJ16
- VAXG30
- AH21
- VAXG31
- AH19
- VAXG32
- AH18
- VAXG33
- AH16
- VAXG34

POWER

PEG & DMI

DDR3 - 1.5V RAILS

1.1V

1.8V

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[illegible]

The schematic diagram illustrates the S3 CPU Power Saving circuit. Key components and connections include:

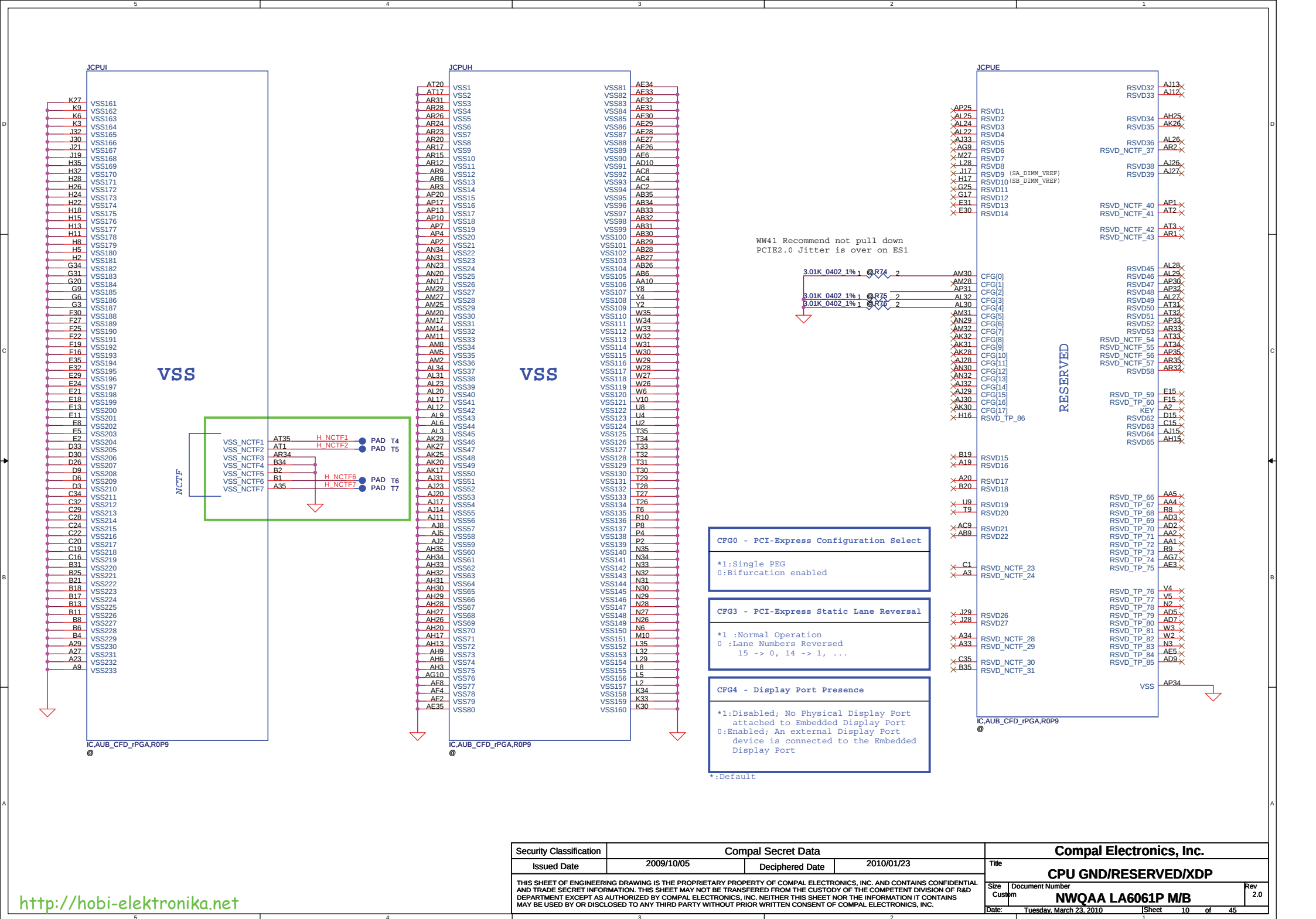
- Power Request Section:**
 - Resistors R69 and R82 are connected to the power request lines (1, 2, 4).
 - Capacitors C230, C314, C205, and C186 are connected to the power request lines (1, 2, 4).
- Near CPU Section:**
 - Resistor R50 is connected to the power request lines (1, 2, 4).
 - Resistor R687 is connected to the power request lines (1, 2, 4).
- Power Saving Section:**
 - Capacitor C216 is connected to the power request lines (1, 2, 4).
 - Jumpers JUMP_43X79 are connected to the power request lines (1, 2, 4).
- Power Lines:**
 - The circuit is connected to the +1.5V_CPU and +1.5V lines.
- Notes:**
 - Change R136 to 470 ohm for GFX issue.
 - J30, PJ31 need to open for S3 CPU Power Saving.

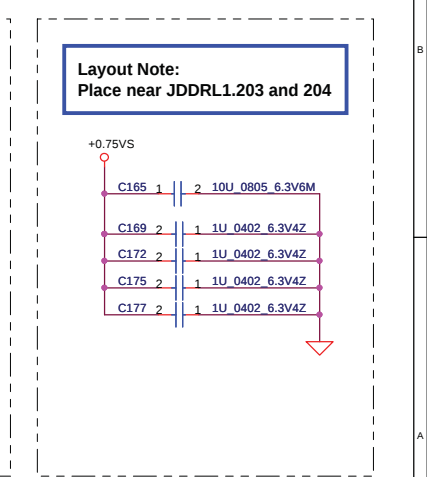
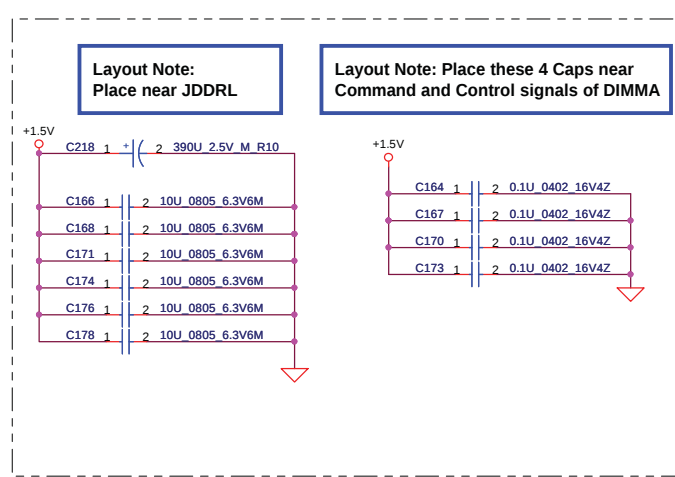
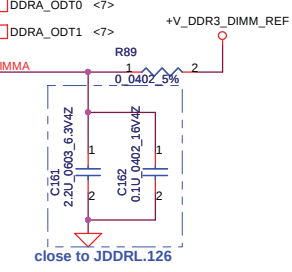
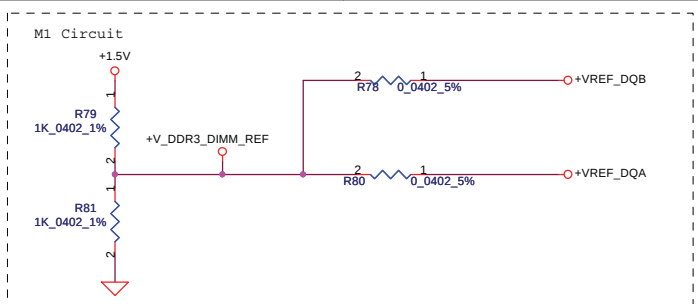
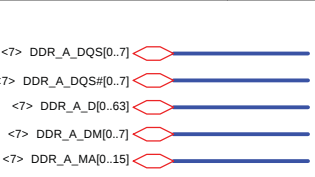
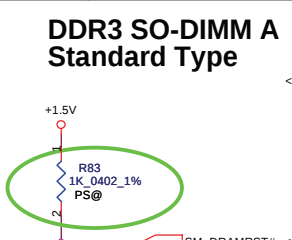
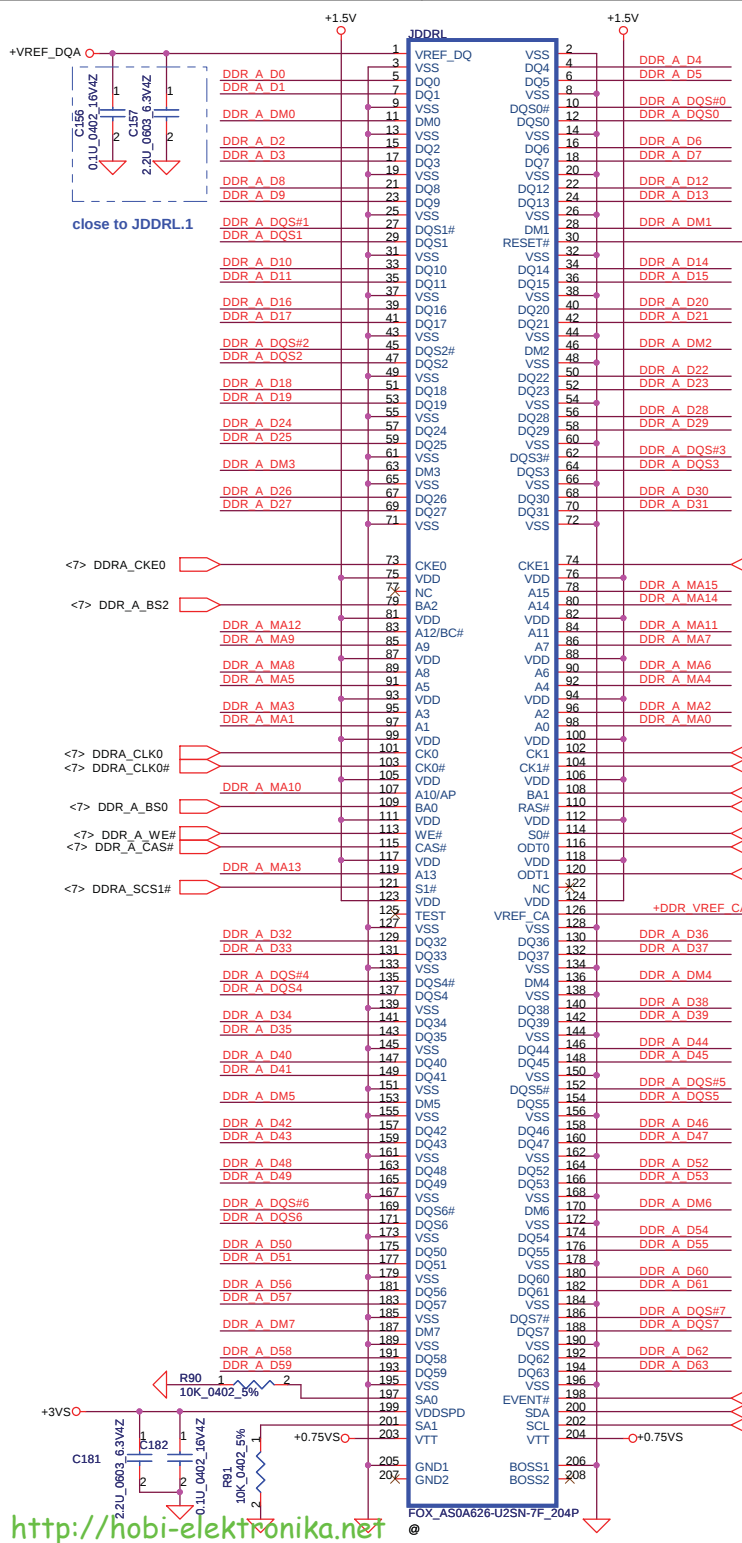
(Place these capacitors under CPU socket Edge, top layer)

(Place these capacitors under CPU socket Edge, top layer)

(Place these capacitors under CPU socket, top layer)

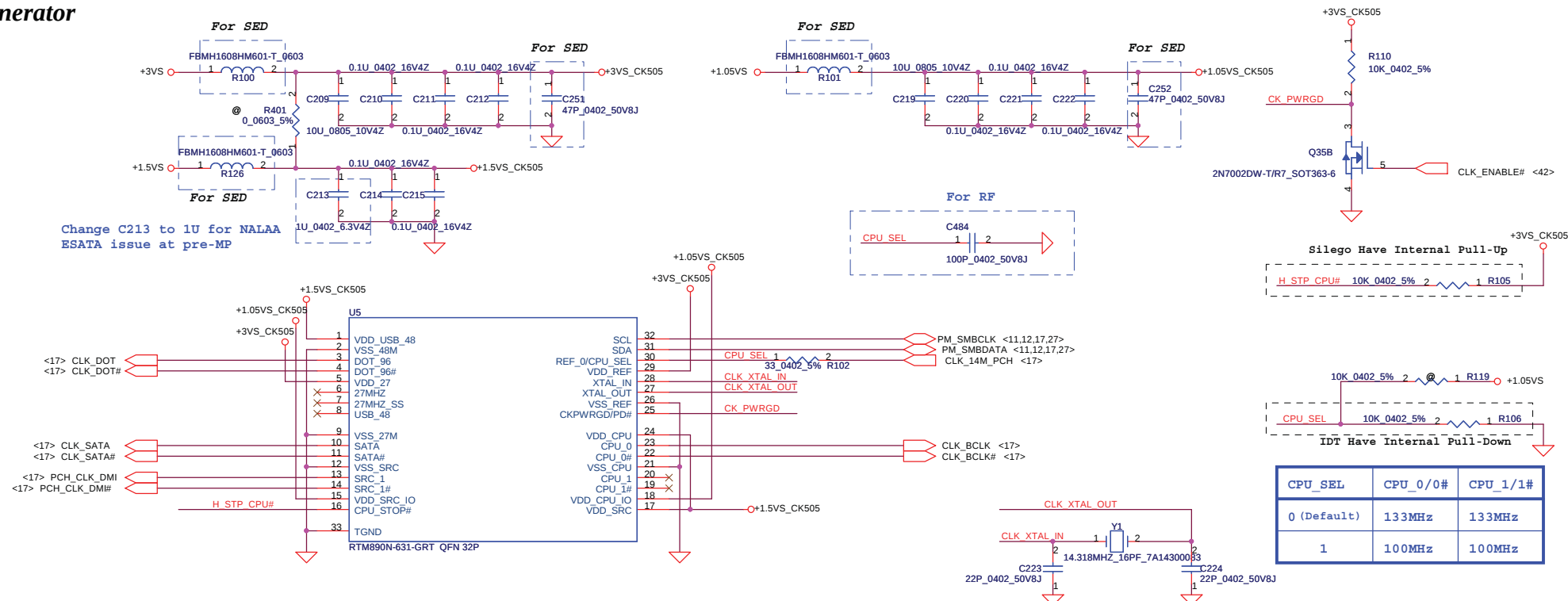
<http://hobi-elektronika.net>



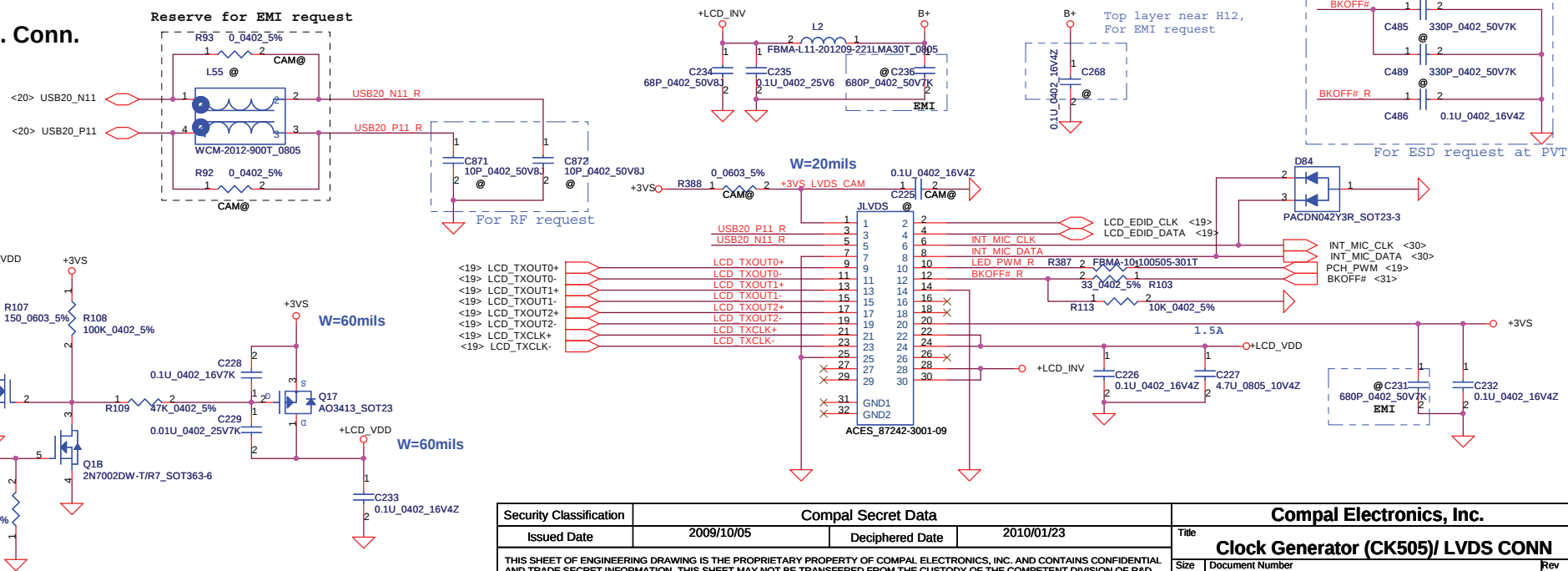


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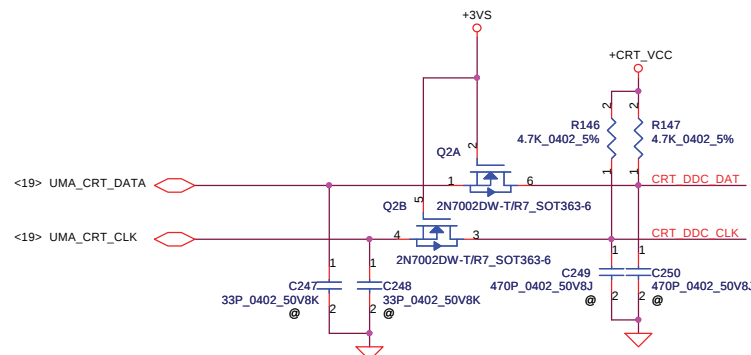
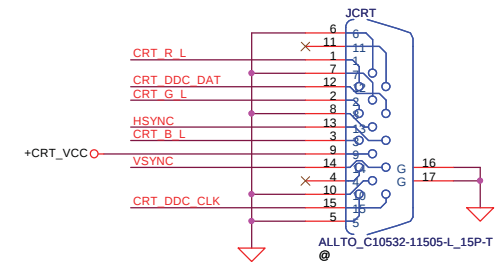
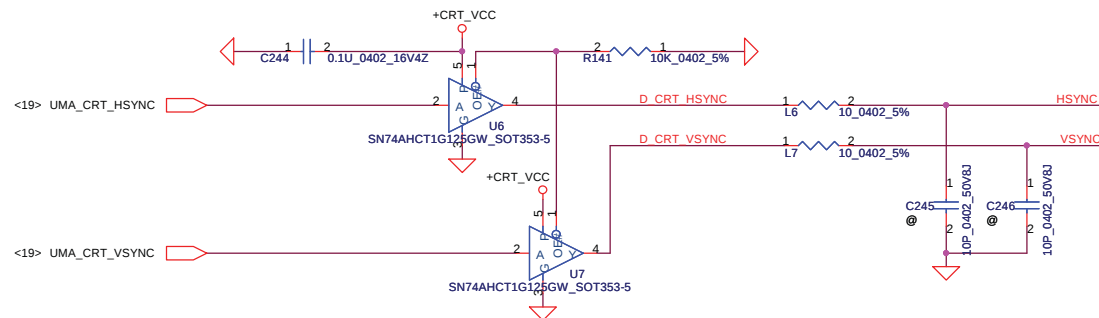
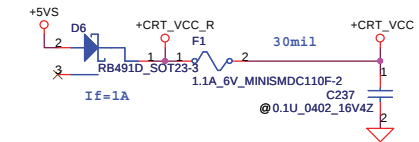
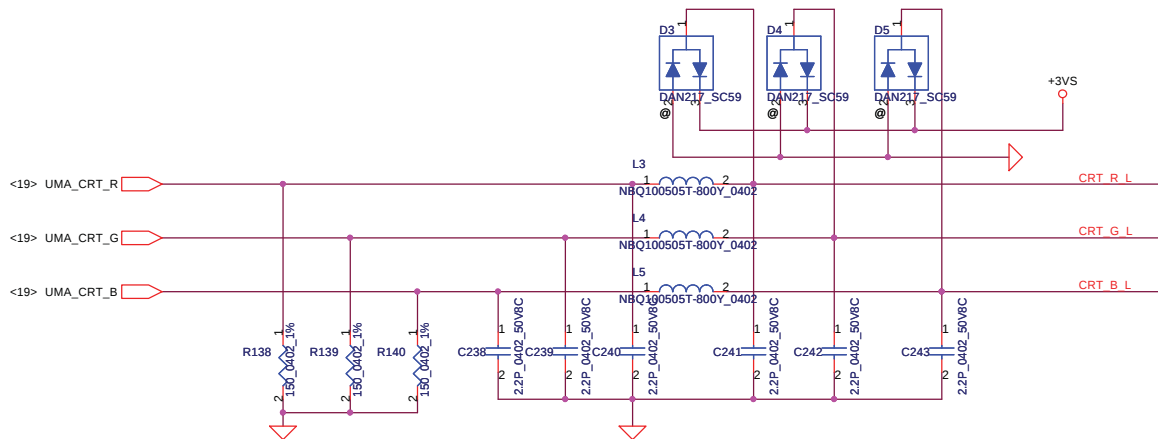
Clock Generator



LCD/PANEL BD. Conn.

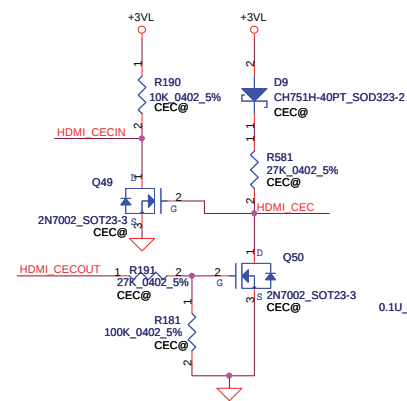


CRT CONNECTOR

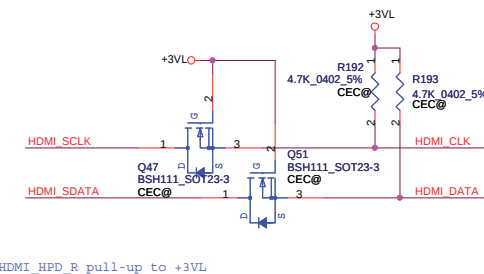
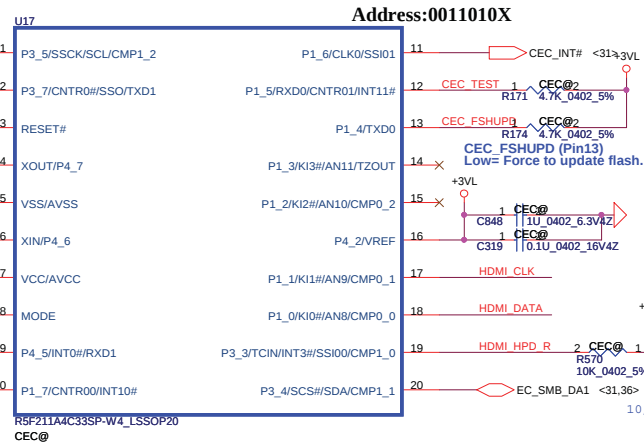
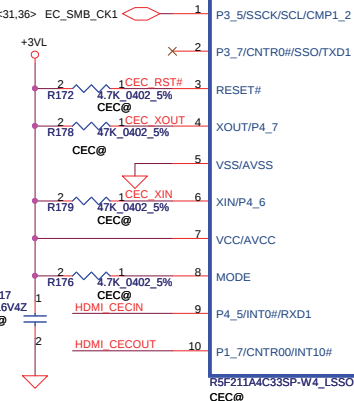
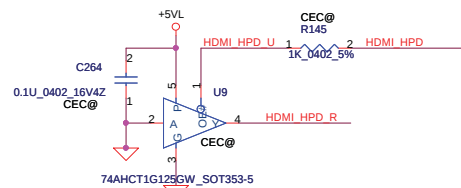


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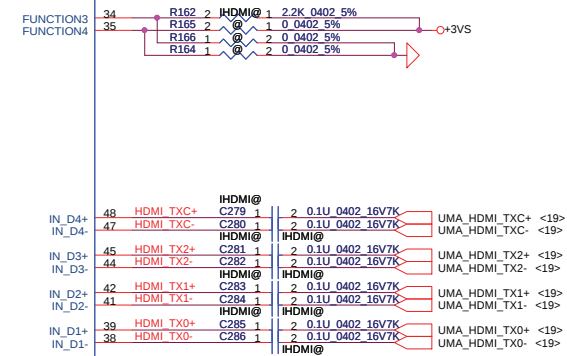
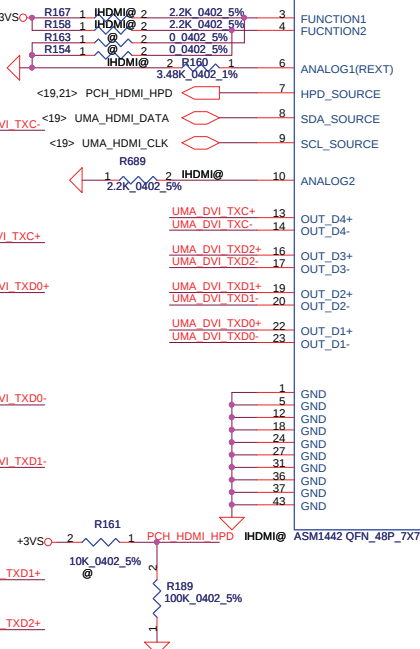
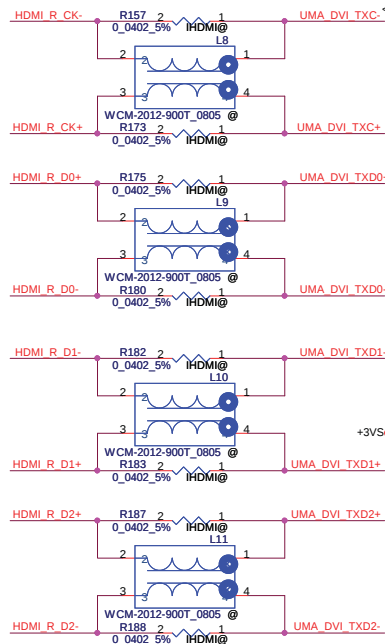
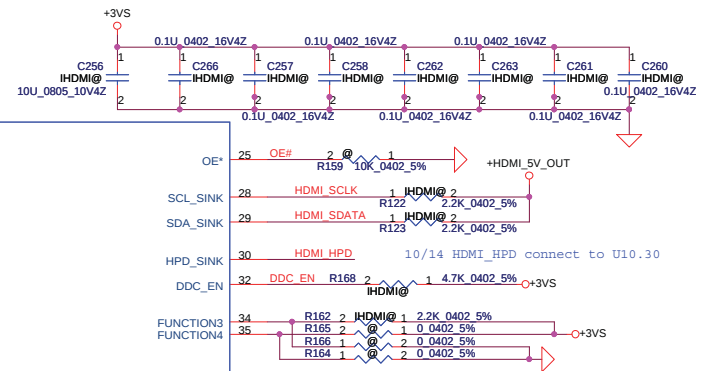
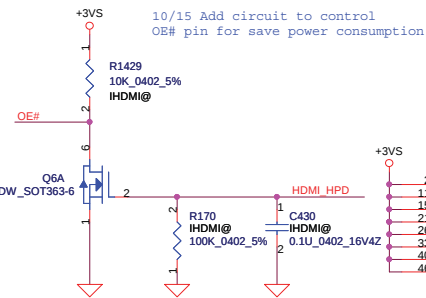
HDMI CEC Controller



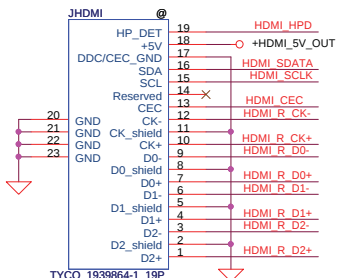
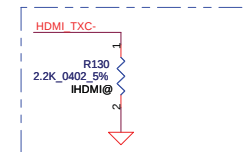
10/14 Remove R691 and change BOM Structure to CEC®



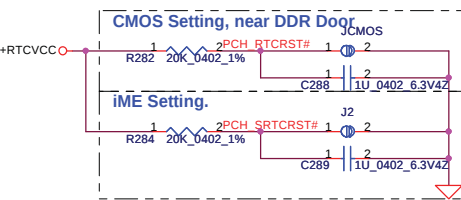
10/14 HDMI_HPD_R pull-up to +3V



Add R130 for AOC monitor
issue at PVT



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Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN

High - Enable Internal VRs
(must be always pulled high)

HDA_SYNC

This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V

HDA_SDO

This signal has a weak internal pull down.
This signal can't PU

Flash Descriptor Security Override

HDA_DOCK_EN#

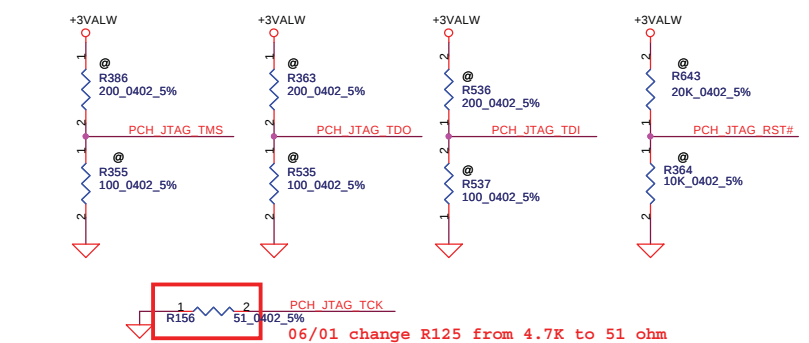
Low = Enabled
High = Disabled *



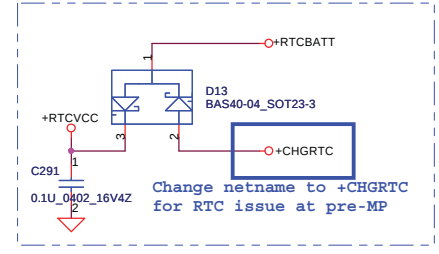
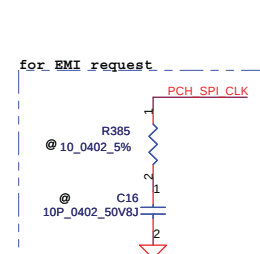
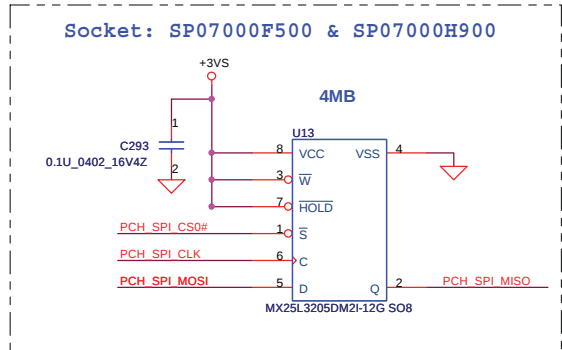
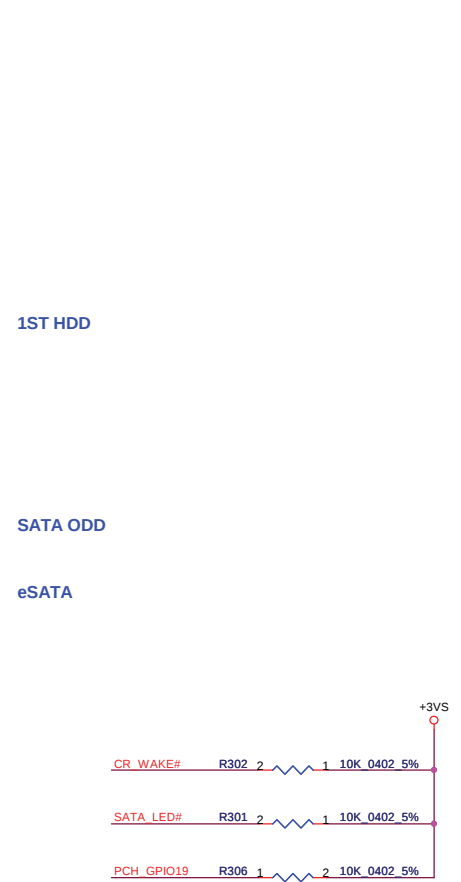
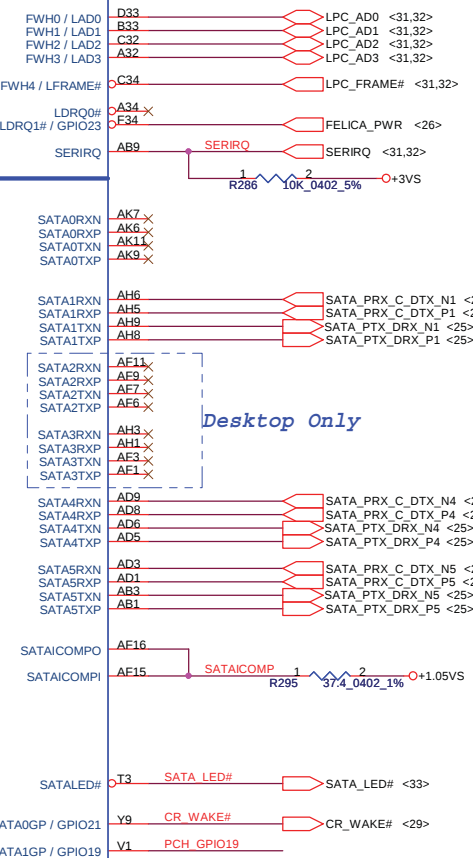
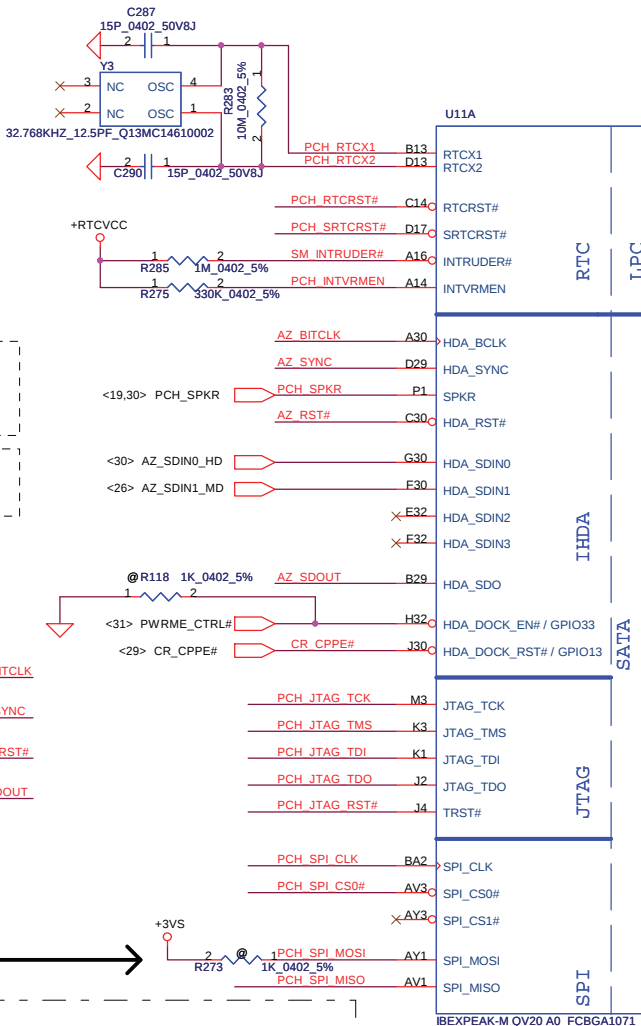
ITPM Enabled Internal: Pull down 20k

SPI_MOSI

High = Enabled
Low = Disabled (Default)



PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_RST#	R536	200ohm	200ohm	20Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_TDO	R355	No Install	100ohm	No Install	No Install



Security Classification

Issued Date

2009/10/05

Deciphered Date

2010/01/23

Compal Secret Data

Title

PCH-SPI/SATA/LPC/RTC/HDA

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Size

Document Number

NWQAA LA6061P M/B

Rev

2.0

Date

Wednesday, March 24, 2010

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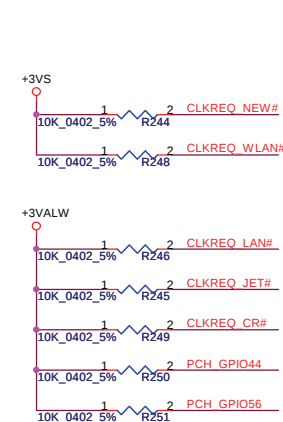
For LAN

For WLAN

For NewCard

For JET

For Card Reader

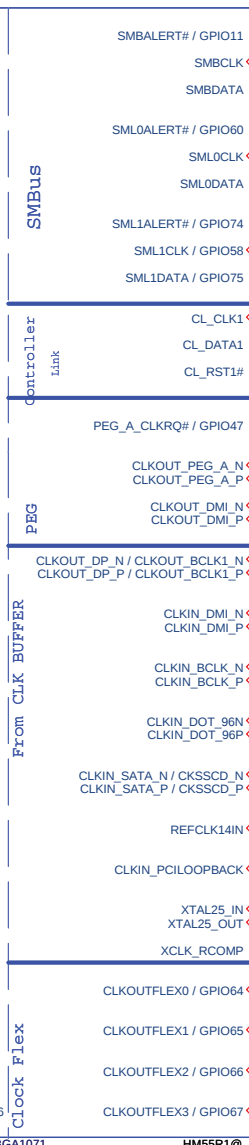


U118

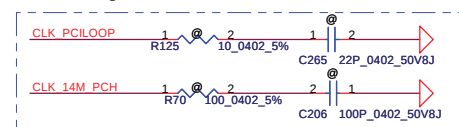
NC

PCI-E*

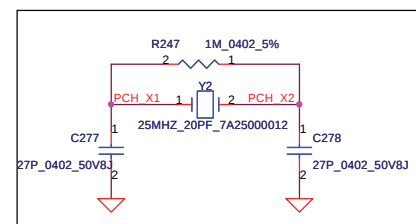
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for EMI request

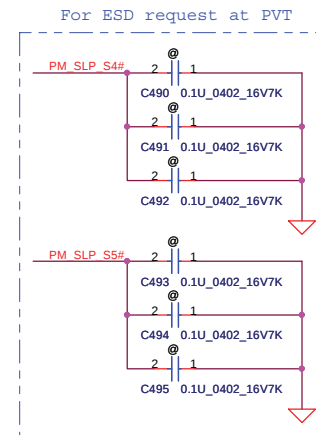
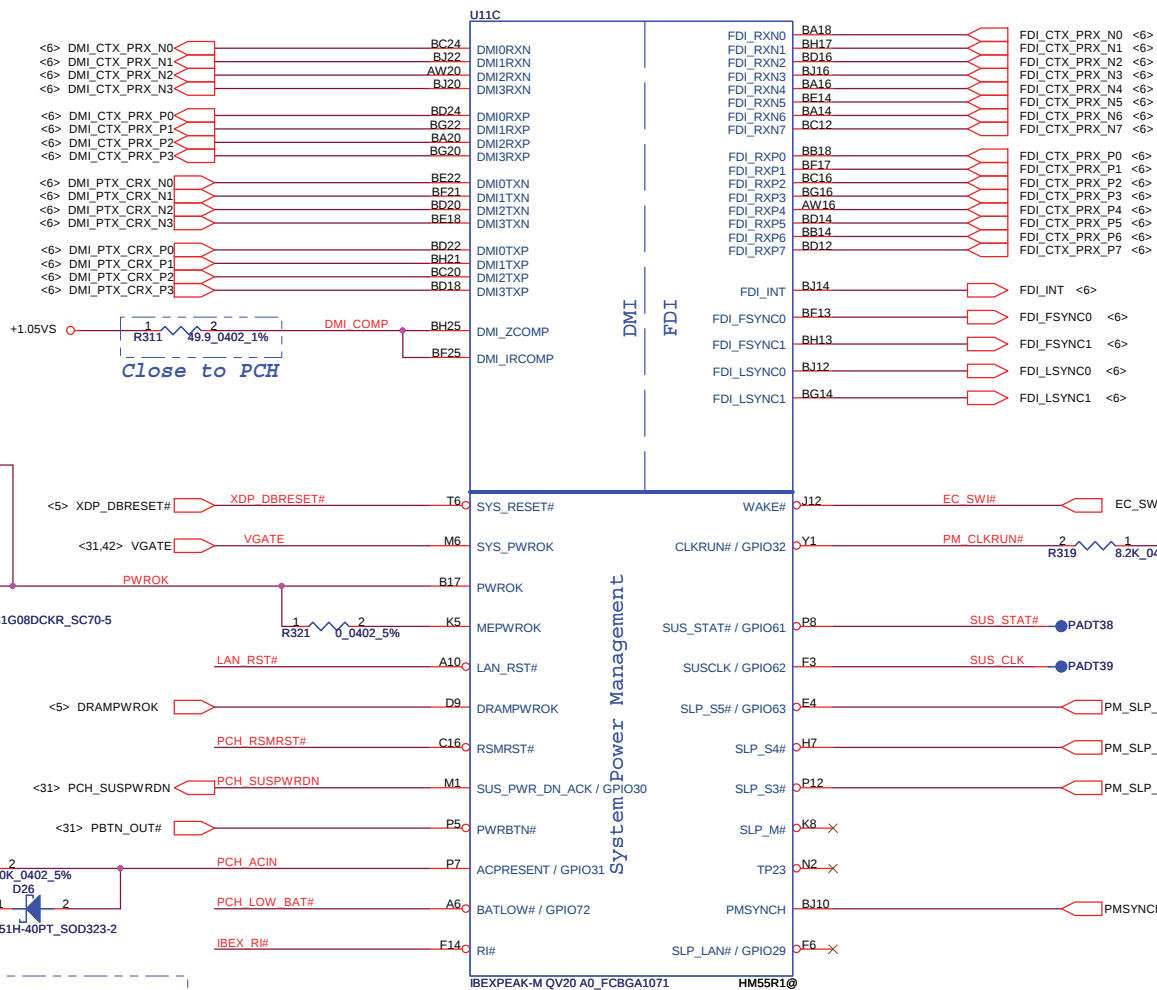
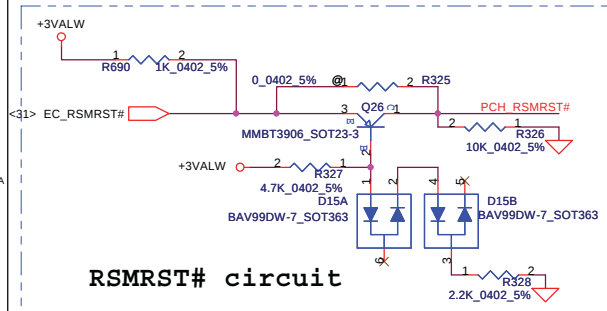
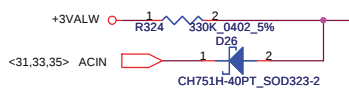
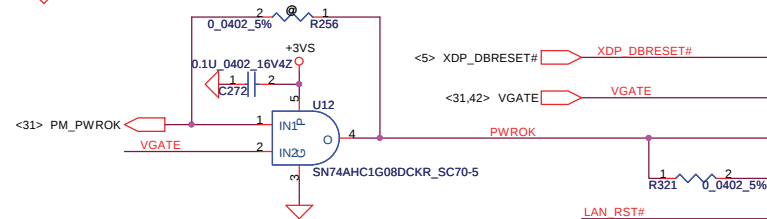
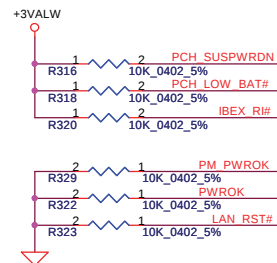
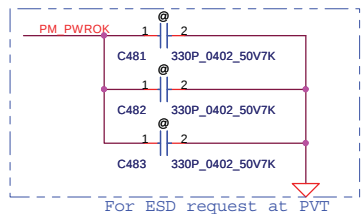


FROM CLK GEN FOR: 133/100/96/14.318 MHZ



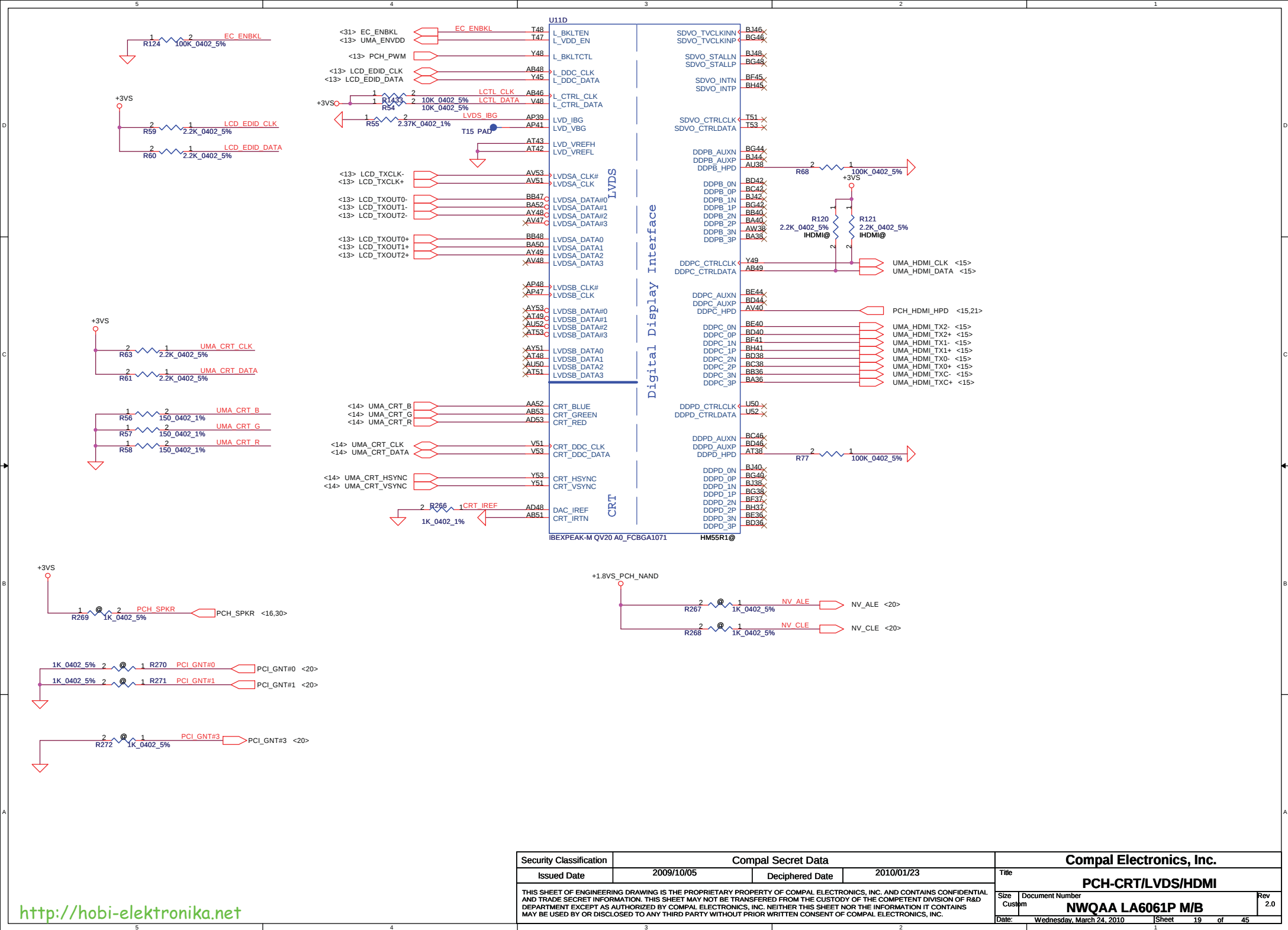
Note: Stuff 0 ohm if 25MHz crystal un-stuff

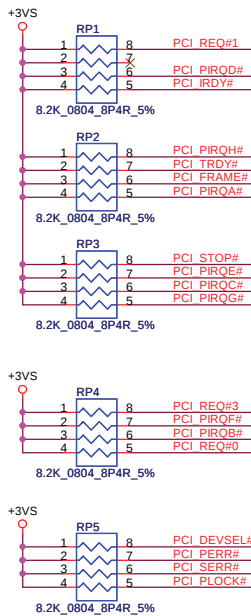
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										PCH-DMI/FDI/PWM	
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GNT2#: Not pull low, internal pull up 20K

<34> ODD_EN#

<19> PCI_GNT#0

<19> PCI_GNT#1

<19> PCI_GNT#3

<27,28,29,31,32> PLT_RST#

<32> CLK_PCI_DDR

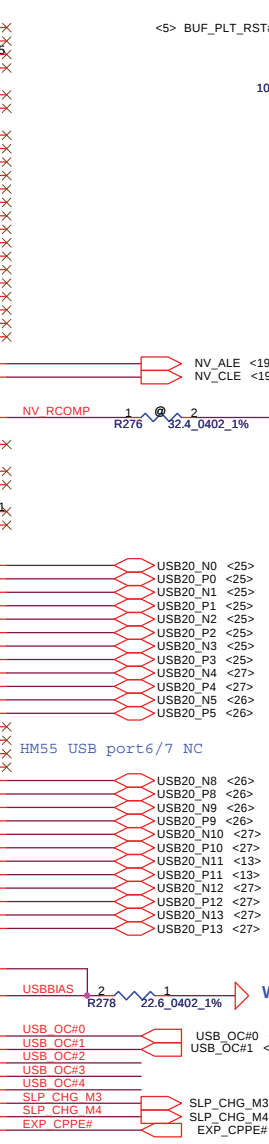
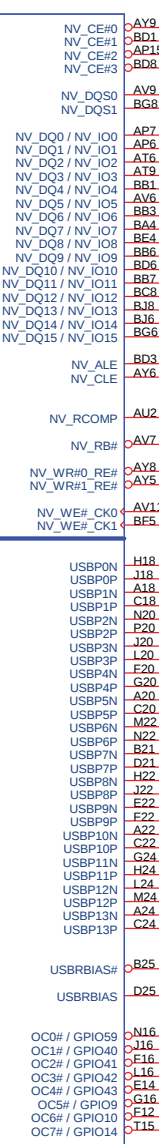
<31> CLK_PCI_EC

<17> CLK_PCILOOP



U11E
IBEXPEAK-M QV20 A0_FCBGA1071
H55R1@
HM55R1@

NV
PCI
USB

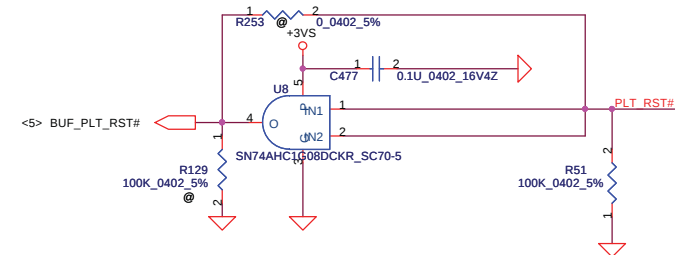


USB-RIGHT1
USB-RIGHT2
USB-Left1
eSATA-USB
NewCard
BT
FPM
Felica
TV#2
Int. Camera
3G/TV#1
WiMax(WLAN)

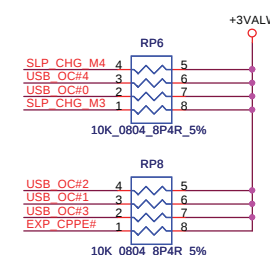
Within 500 mils

(USB-Right)
(USB-Left & eSATA)

SLP_CHG_M3 <25>
SLP_CHG_M4 <25>
EXP_CPPE# <27>



Swap USB port4 and port8 at PVT



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						Size B		Document Number			Rev 2.0	
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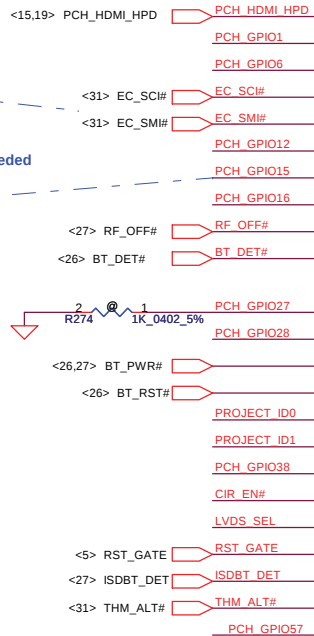
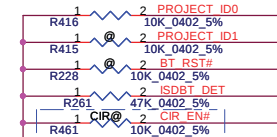
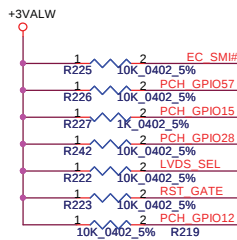
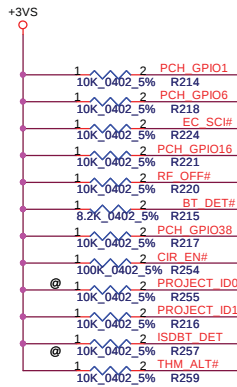
GPIO8 Not pull down

Internal: Pull up 20k
During Reset: High
Initial: High

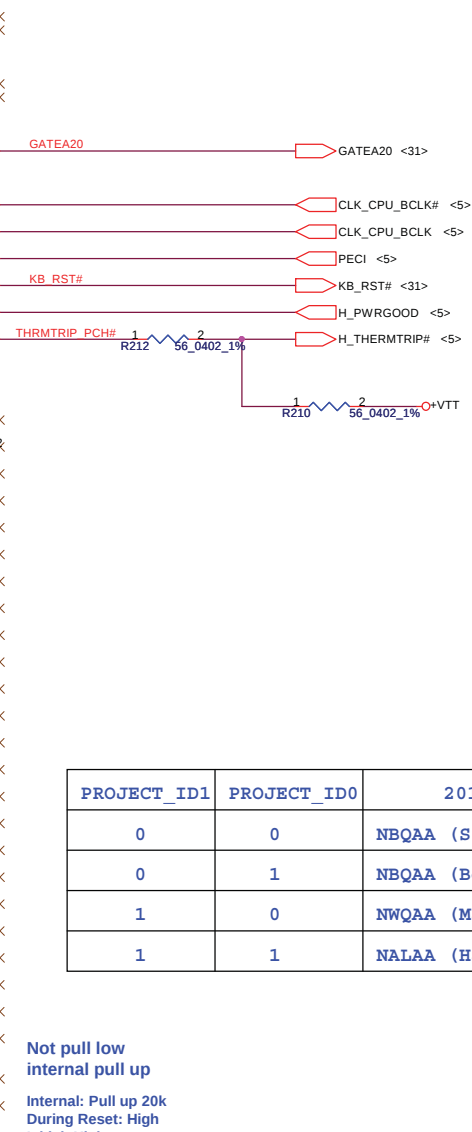
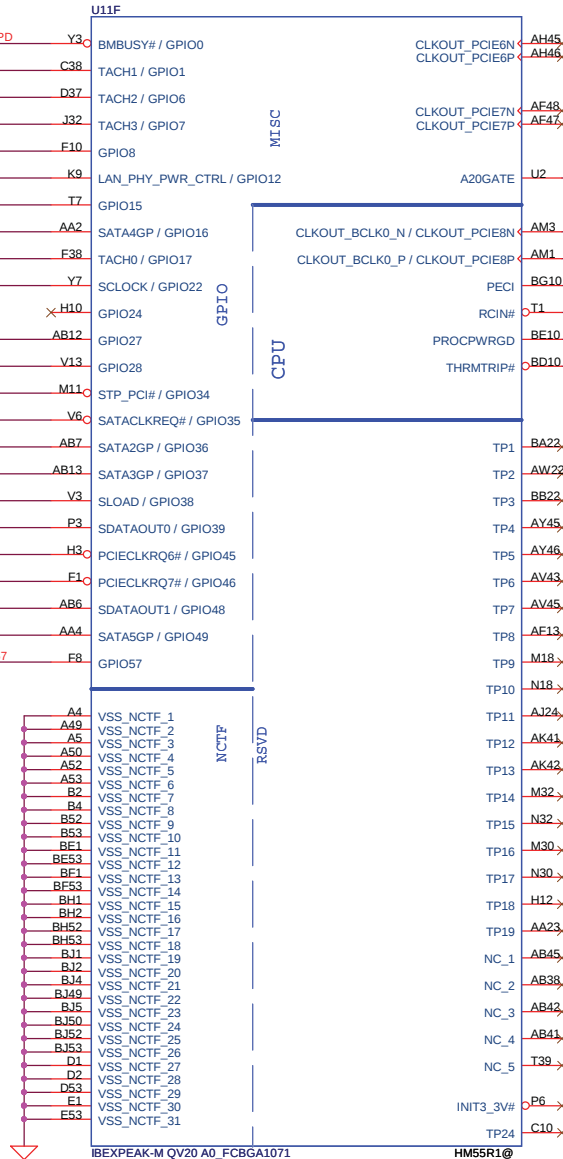
GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR

PCH_GPIO27 High = Enabled (Default)
Low = Disabled

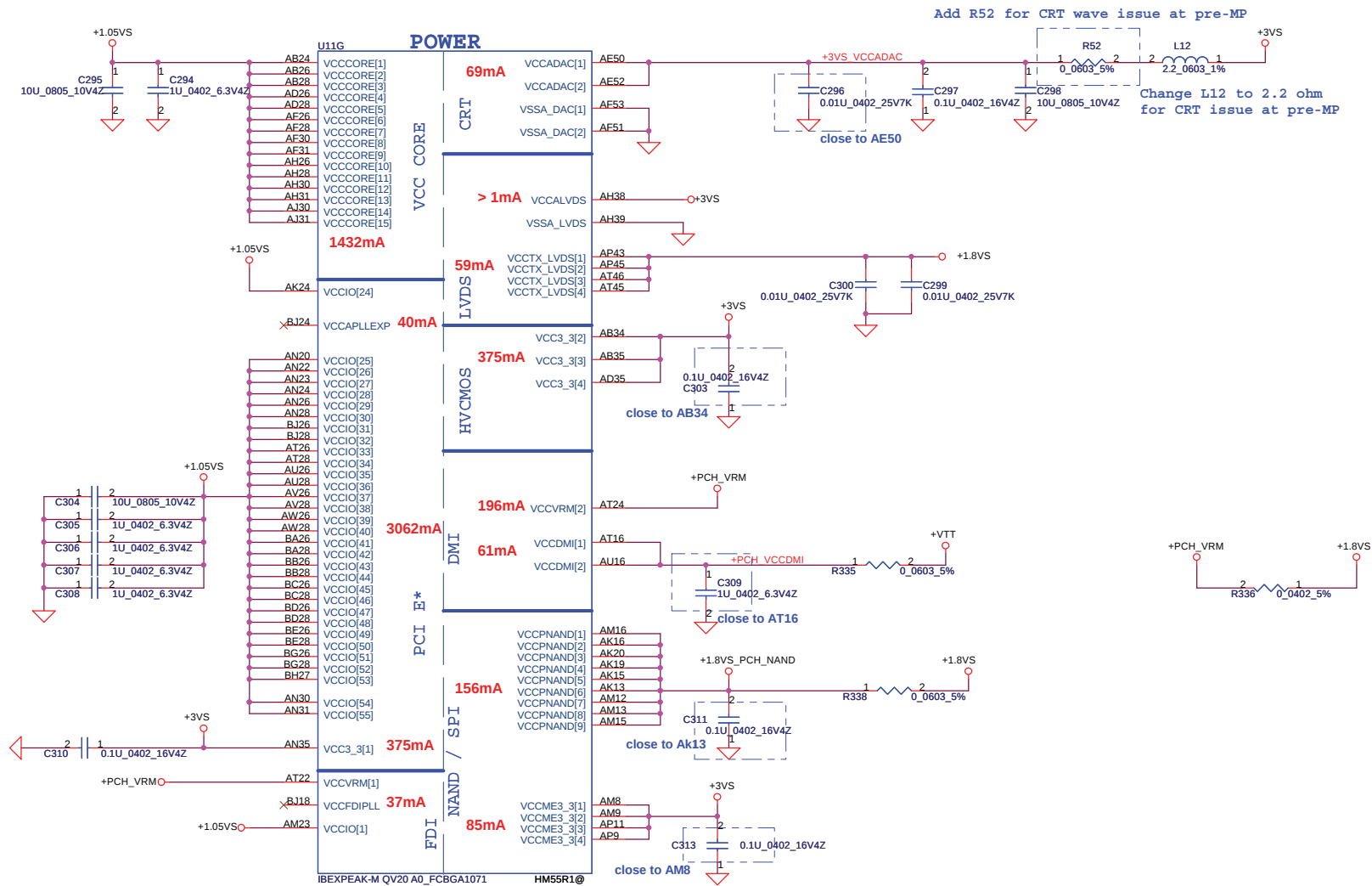


LVDS_SEL=H
for Single Channel LVDS



PROJECT_ID1	PROJECT_ID0	2010 Project ID setting
0	0	NBQAA (Streamline-M/-S 11.6/13.3")
0	1	NBQAA (Bordeaux 14")
1	0	NWQAA (Marseille 16")
1	1	NALAA (Hamburg 17.3")

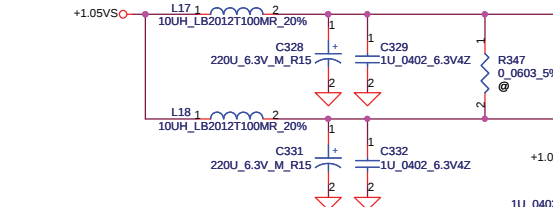
Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High



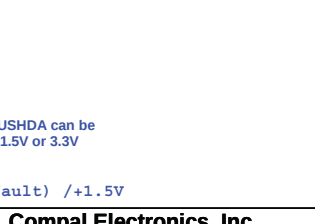
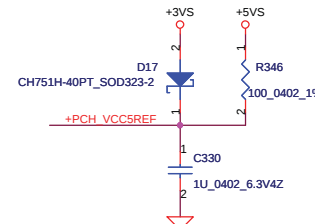
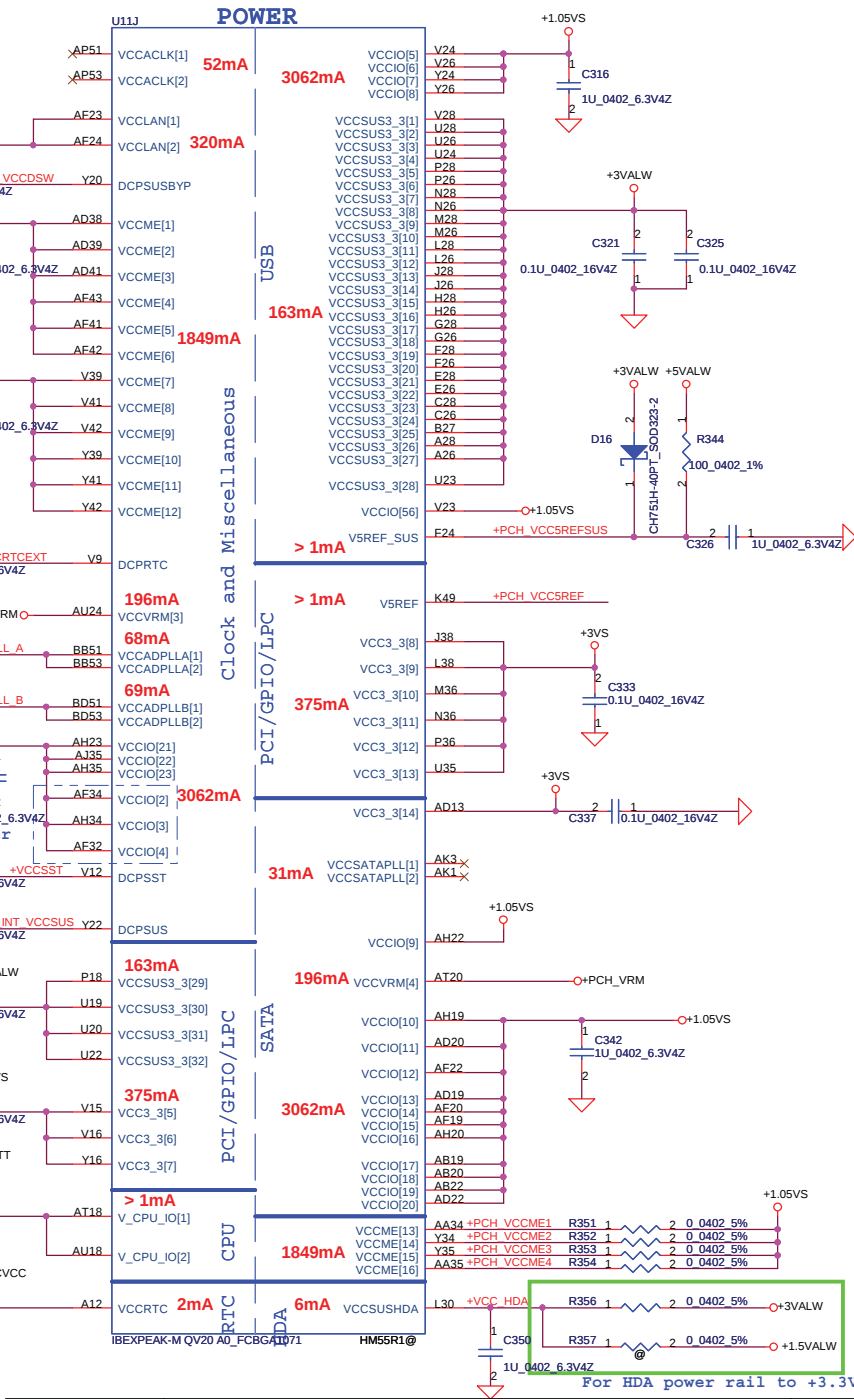
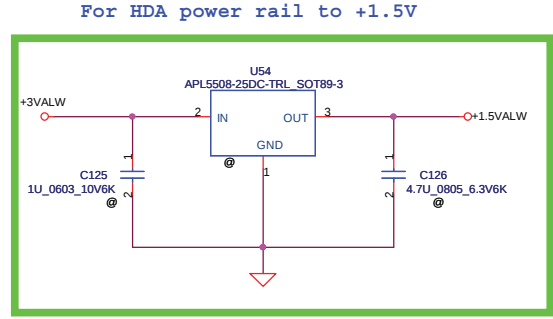
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VccLAN may be grounded if Intel LAN is disabled

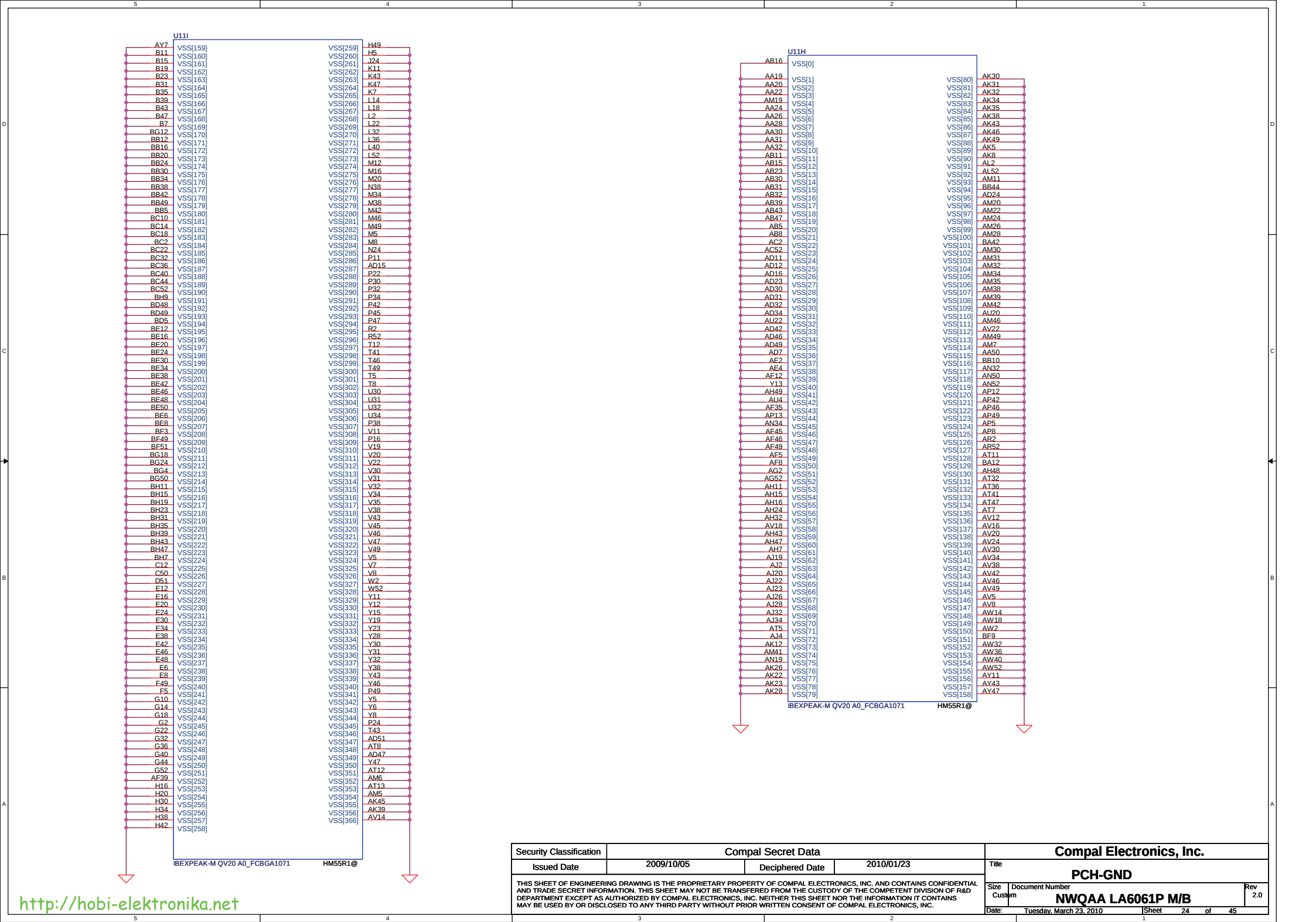
If two VccME rails can be combined, only total 2 x 22 μ F and 2 x 1 μ F caps are necessary



Short AF34, AH34 and AF32 power for HDMI Deep Color



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				Custom	NWQAA LA6061P M/B
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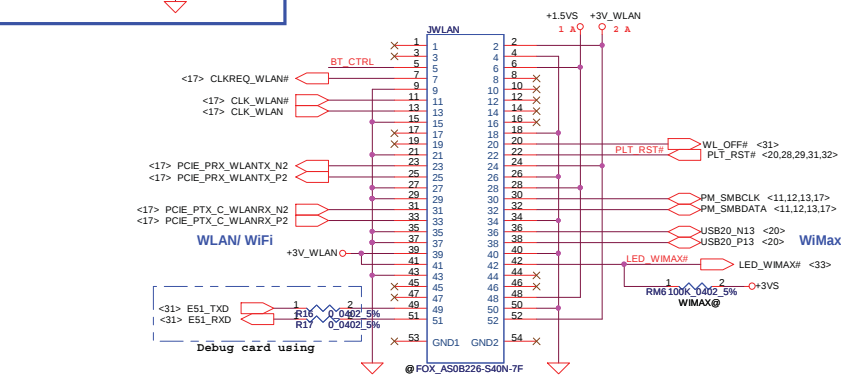


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Size	Document Number	Rev		2.0	
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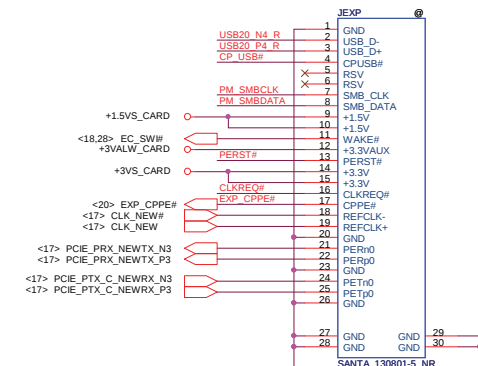
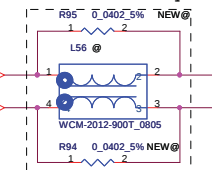
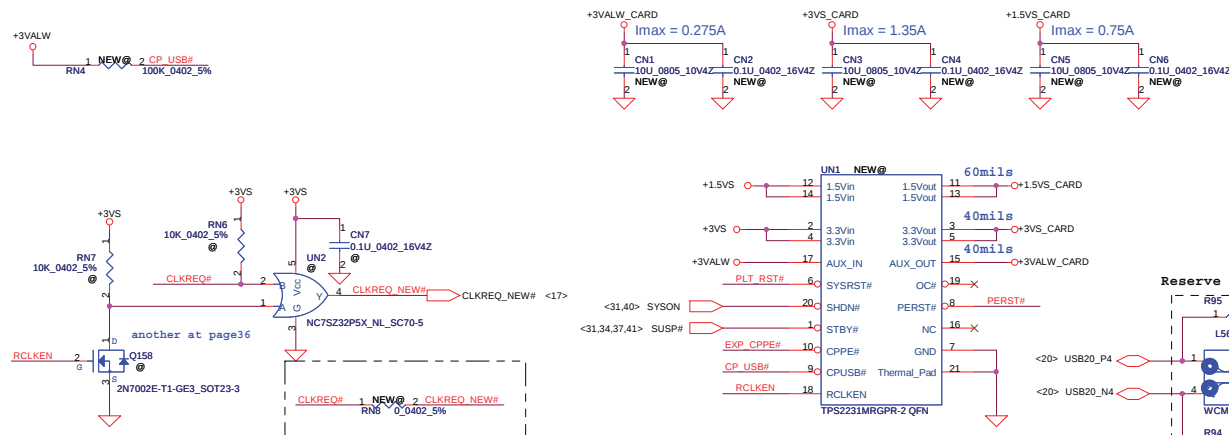
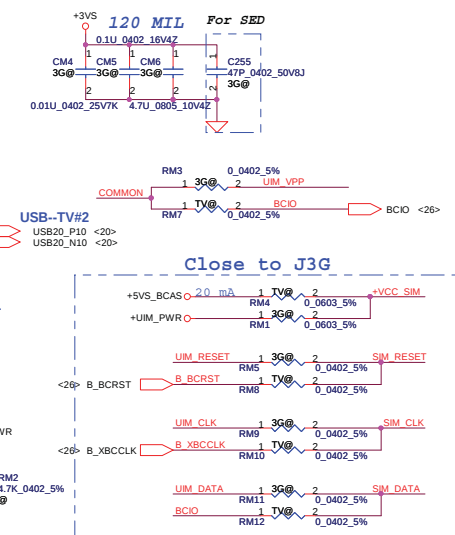
Short PJ26 for Wi-Fi (WLAN)/WiMax combo module
Short PJ26 for Wi-Fi (WLAN) module only.

****If +3V_WLAN is +3VS, please remove D21.**

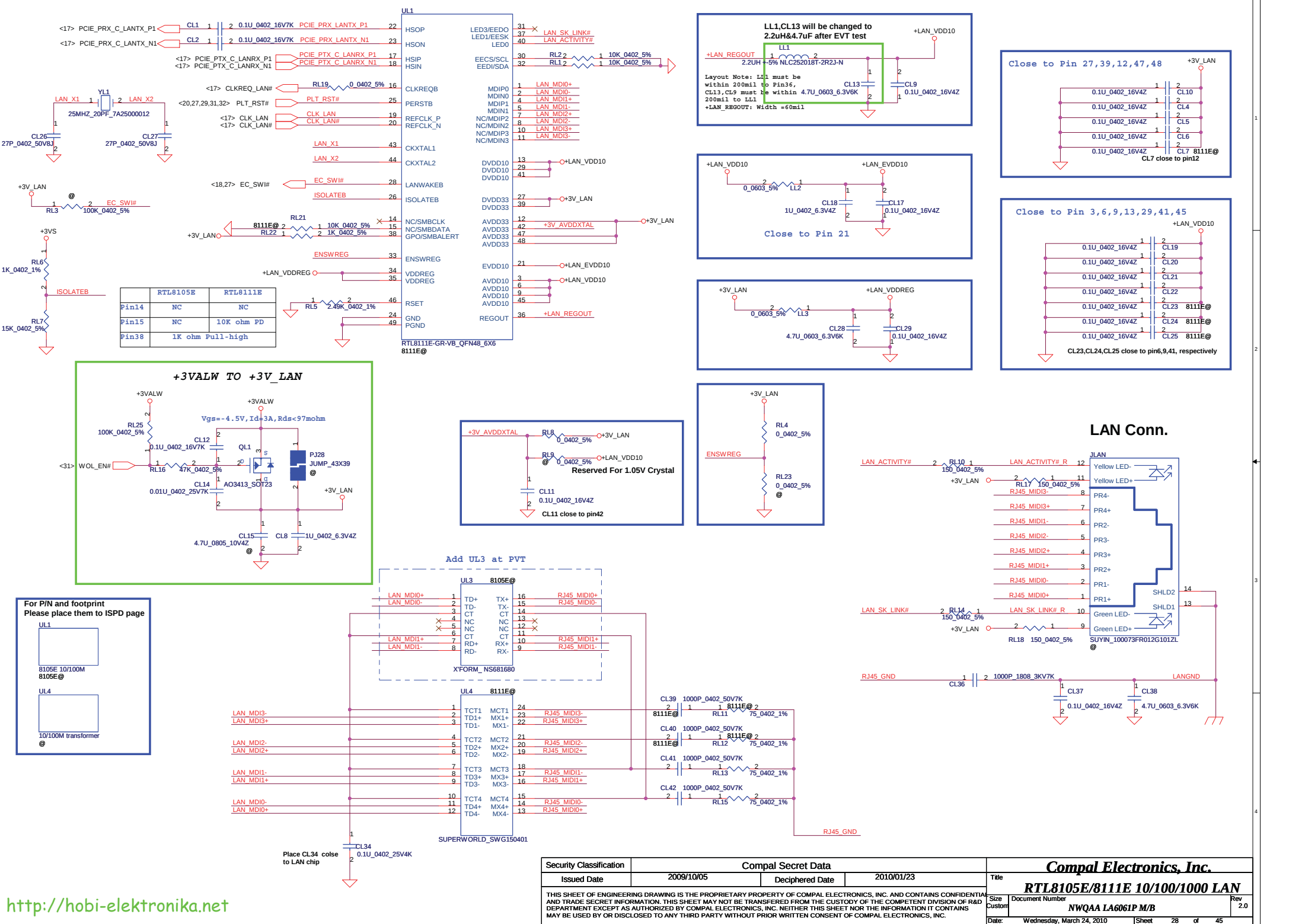
21,26> BT_PWR#  2
G Q36
S 2N7002_SOT23-



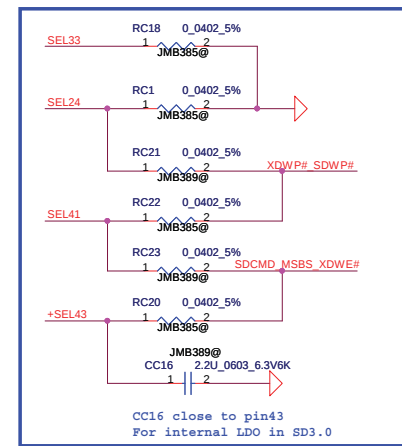
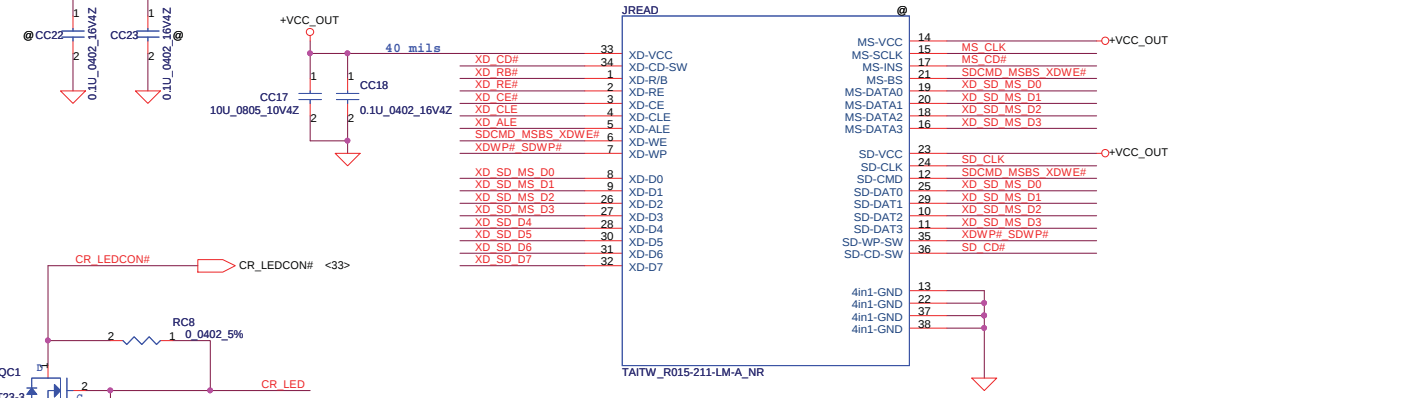
The diagram illustrates a USB-to-PCIe bridge circuit. The top section, labeled 'B-CAS', shows the USB interface with a USB20L16-0001-D connector. It includes pins for USB20_P10_TV, USB20_P11_TV, USB20_P12, USB20_N12, and USB20_P13. The bottom section, also labeled 'B-CAS', shows the PCIe interface with a PCI9420-0001-D connector. It includes pins for PCIE_P1X_JETTX_P4, PCIE_P1X_JETTX_N4, PCIE_P1X_C_JETRX_P4, PCIE_P1X_C_JETRX_N4, and TMPTU1_SXP. The circuit includes various components like resistors (R72, R85, R307), capacitors (CM15, CM16), and a MOSFET (DM1, RLZ20A_LL34). It also shows power supply connections for +1.5V, +3V, and +2.75V. The schematic is divided into two main sections: 'B-CAS' and 'B-CAS'.



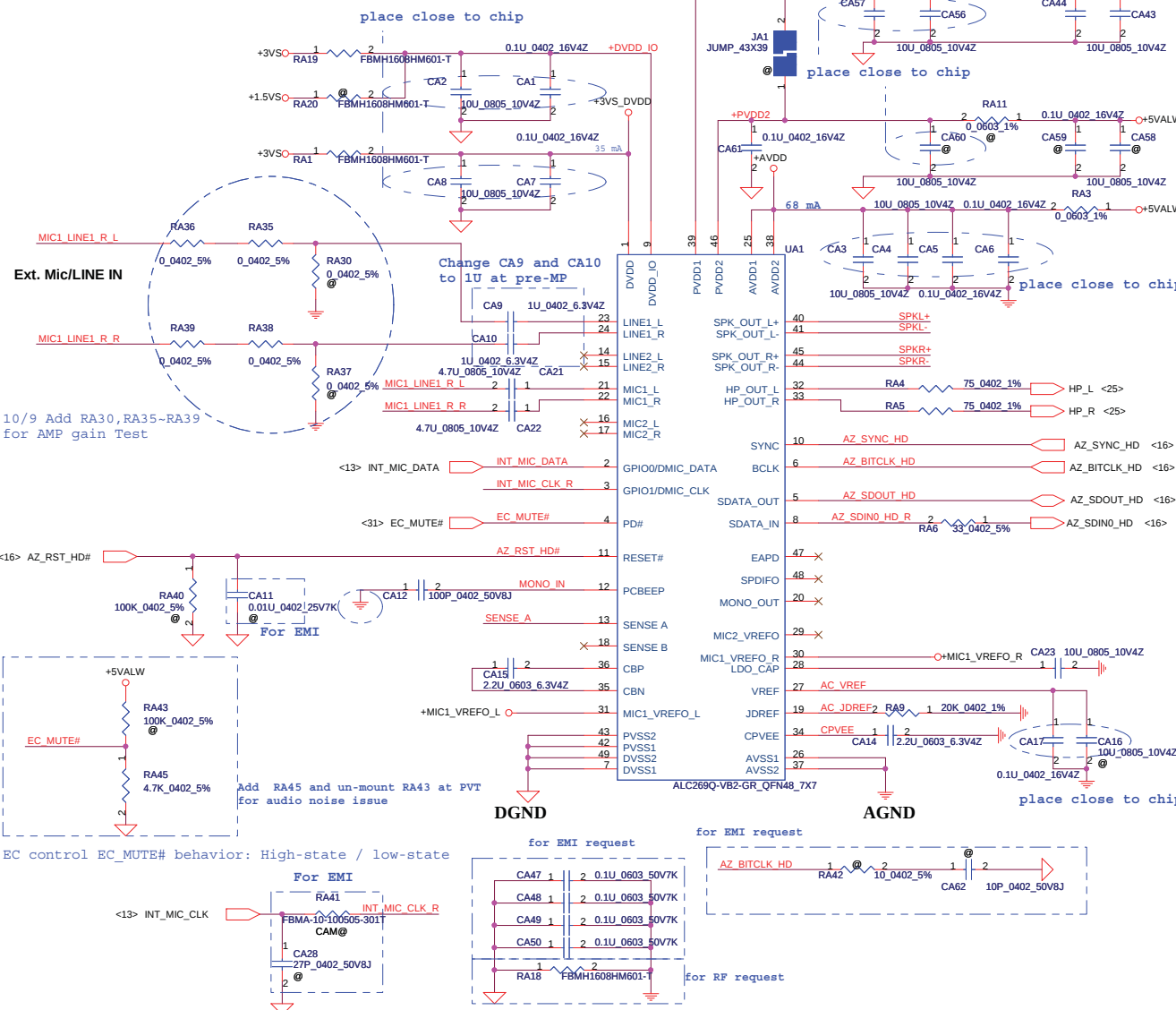
Security Classification	Compal Secret Data			Compal Electronics, Inc.					
Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title	PCIe-WLAN/JET/3G/TV#1/TV#2/NewCard				
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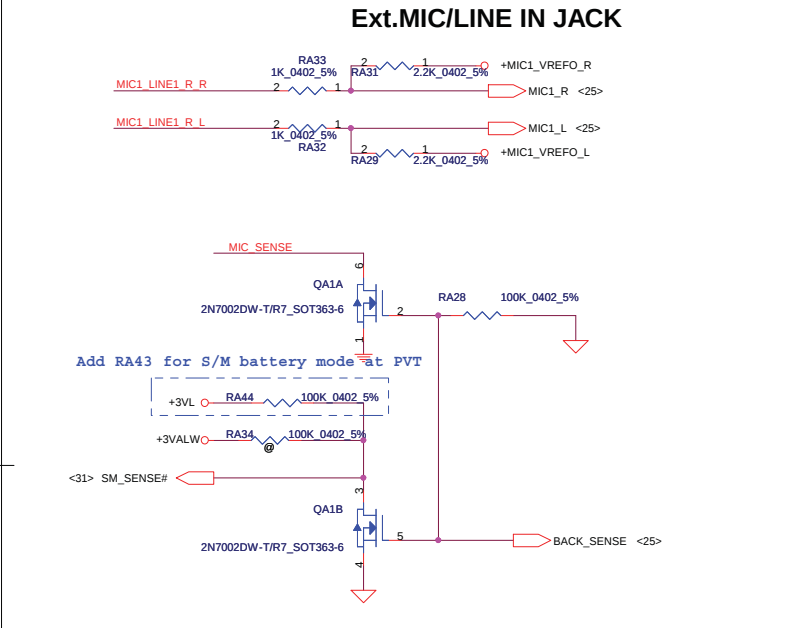
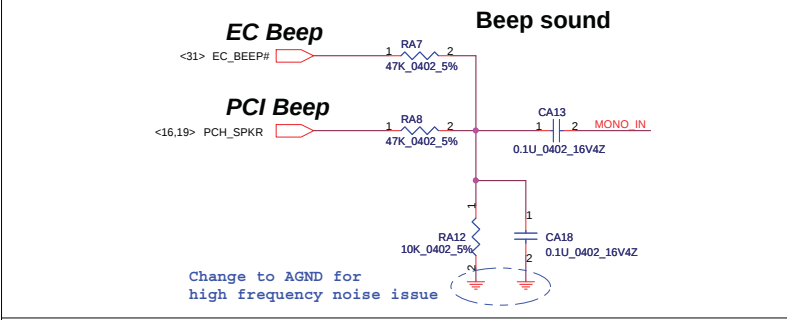
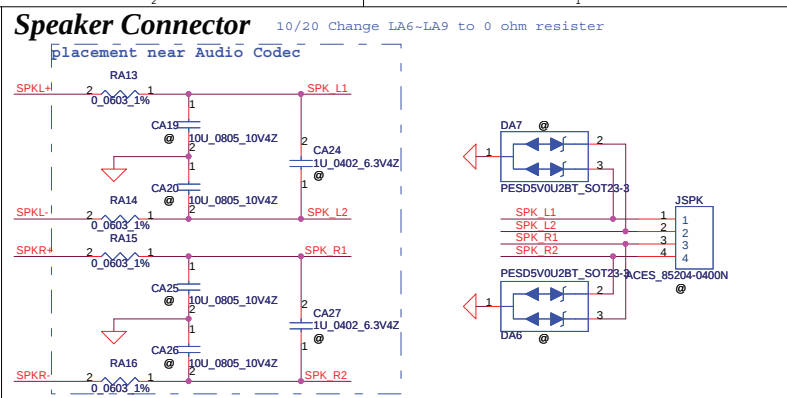
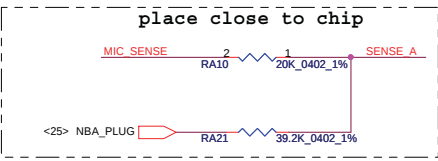
UC2 JMB389@

[illegible]

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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	





The diagram illustrates the timing for the SPI interface between the C451 and the U22. The C451 is configured with a 0.1μ 0402_16V4Z capacitor. The U22 is an MX25L2005CM1-12G SOP 8P. The timing diagram shows the relationship between the SPI_CLK signal and the SPI data lines. A callout box highlights the timing for the SPI_CLK signal, showing a delay of 10 ns from the C451 output to the U22 input, with a note "reserve for EMI, close to U22".

[illegible]

The diagram illustrates the H7 debug pad connections. The H7 chip has pins 6, 7, 8, 9, 10, and 0. Pin 6 is connected to +3VS. Pin 7 is connected to SERIRQ (16,31) through a resistor R392 (0_0402_5%). Pin 8 is connected to LPC_AD3 (16,31). Pin 9 is connected to LPC_AD1 (16,31). Pin 10 is connected to LPC_FRAME# (16,31). Pin 0 is connected to CLK_PCI_DDR (20) and is also labeled as a debug pad. A callout box shows a detailed view of the connection to CLK_PCI_DDR, showing a resistor R393 (22_0402_5%) and a capacitor C457 (22P_0402_50VB3) connected to ground.

[illegible][illegible]

The diagram shows the pin connections for the MMA7360L2R2_LGA14 sensor. It includes three main components: UG1, GSENSOR, and UG4.

UG1 Pin Connections:

- Pin 1: GND1
- Pin 2: Vdd1
- Pin 3: Voutx
- Pin 4: PD
- Pin 5: Vouty
- Pin 6: FS
- Pin 7: Voutz
- Pin 8: ST
- Pin 9: Rev
- Pin 10: NC1
- Pin 11: NC2
- Pin 12: NC3
- Pin 13: NC4
- Pin 14: NC5

GSENSOR Pin Connections:

- Pin 1: VOUTX CG1
- Pin 2: VOUTY CG2
- Pin 3: VOUTZ CG3

UG4 Pin Connections:

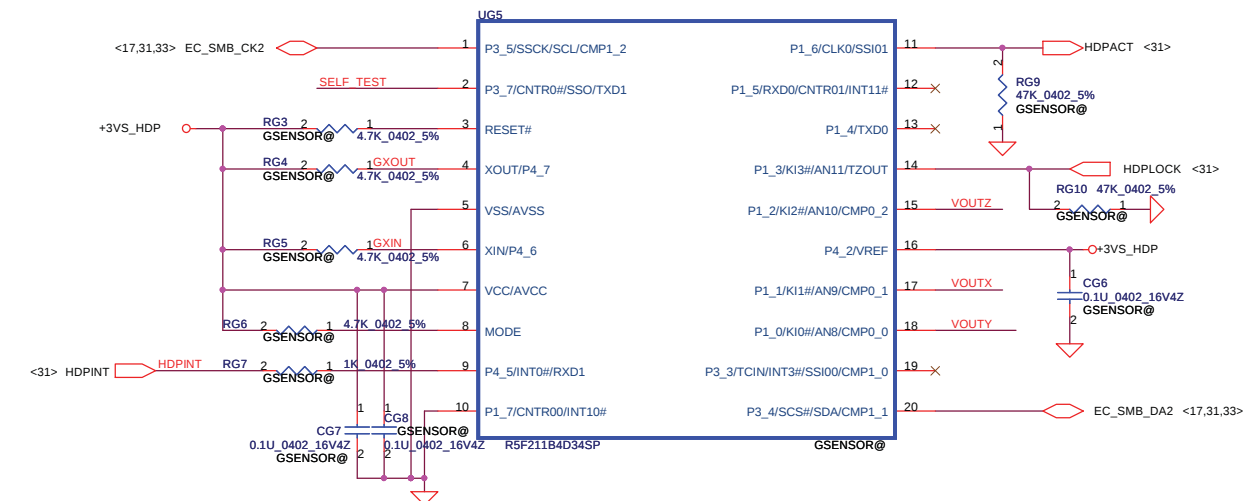
- Pin 1: XOUT
- Pin 2: YOUT
- Pin 3: ZOUT
- Pin 4: OG-DET
- Pin 5: SLEEP#
- Pin 6: G-SELECT
- Pin 7: ST
- Pin 8: VSS
- Pin 9: VDD
- Pin 10: NC
- Pin 11: NC
- Pin 12: NC
- Pin 13: NC
- Pin 14: NC

External Connections:

- +3VS_HDPO is connected to pins 2, 4, and 9.
- SELF TEST is connected to pins 8, 10, and 13.
- CG9 is connected to pins 1, 2, and 3.
- 0.033uF capacitors are connected to pins 1, 2, and 3.
- 0.033uF capacitors are connected to pins 1, 2, and 3.
- 0.033uF capacitors are connected to pins 1, 2, and 3.

Notes:

- UG1 & UG4 must place on TOP side
- Reserve for 2nd Source



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Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title SPI ROM/TP/KB/Debug			
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					NWQAA LA6061P M/B		2.0
				Date:	Wednesday, March 24, 2010	Sheet	32

[illegible]

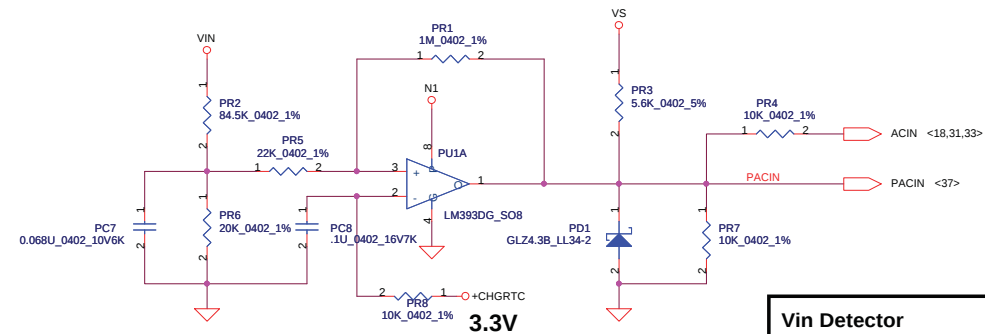
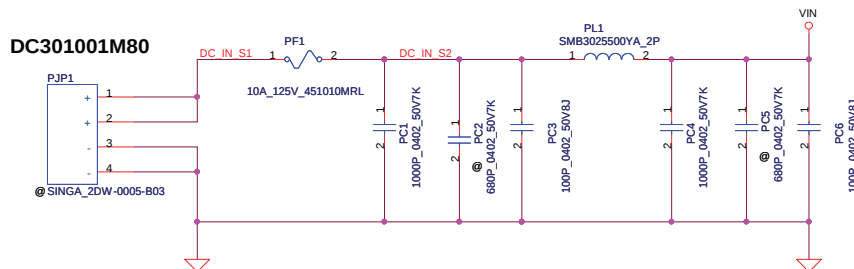
For EMI request

[illegible]

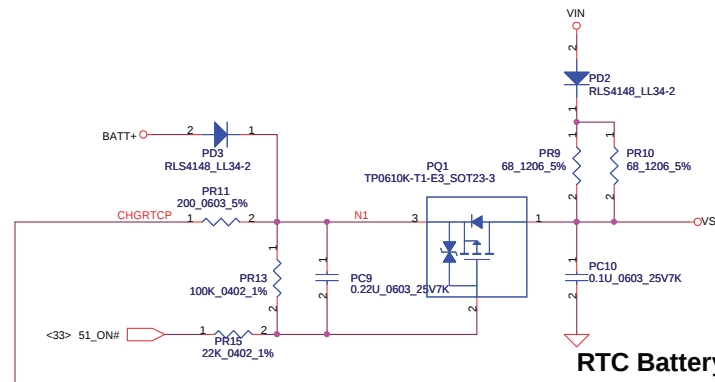
For EMI request

Two circuit diagrams for the SUSP pin are shown. The left diagram shows the pin connected to +5VALW through a 100K resistor (R422) and a MOSFET (Q5A, 2N7002DW-T/R7_SOT363-6) controlled by SUSP#. The right diagram shows the pin connected to +0.75VS through a 470 ohm resistor (R421) and a MOSFET (Q5B, 2N7002DW-T/R7_SOT363-6) controlled by SUSP. Both diagrams include a note 'another at page42'.

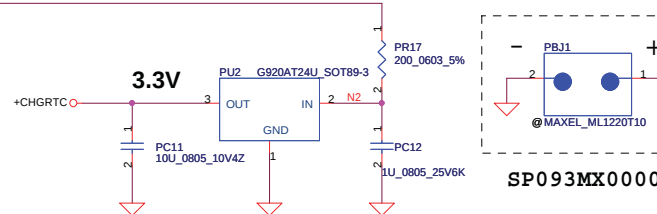
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title DC-DC INTERFACE		
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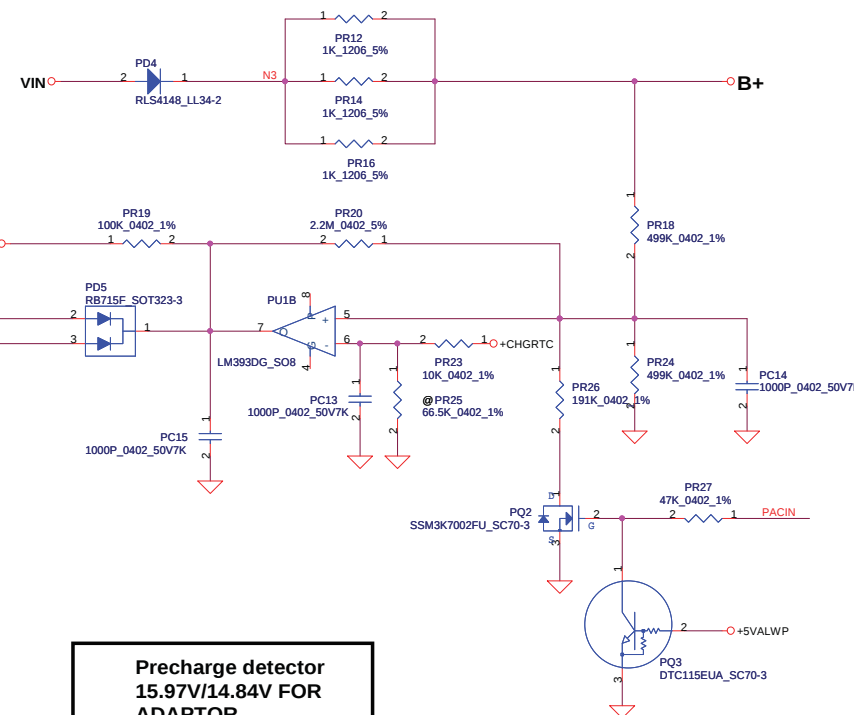
Vin Detector		
High	18.384	17.901 17.430
Low	17.728	17.257 16.976



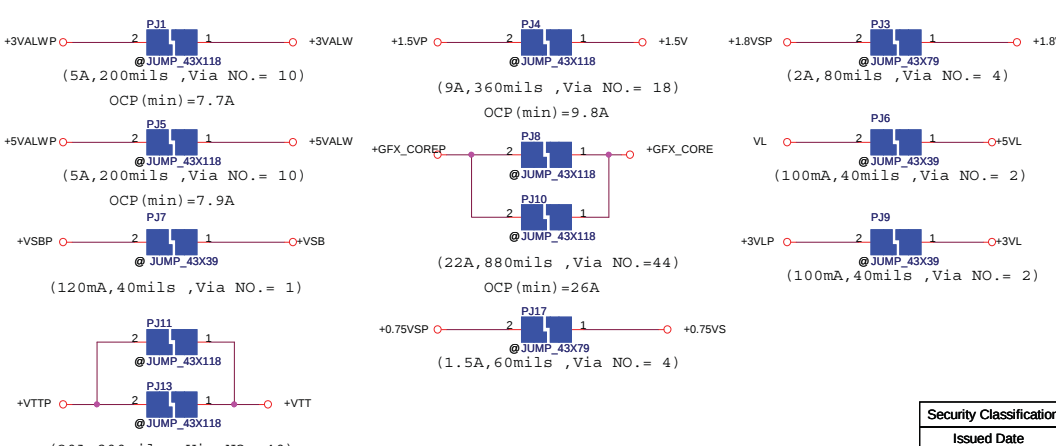
RTC Battery



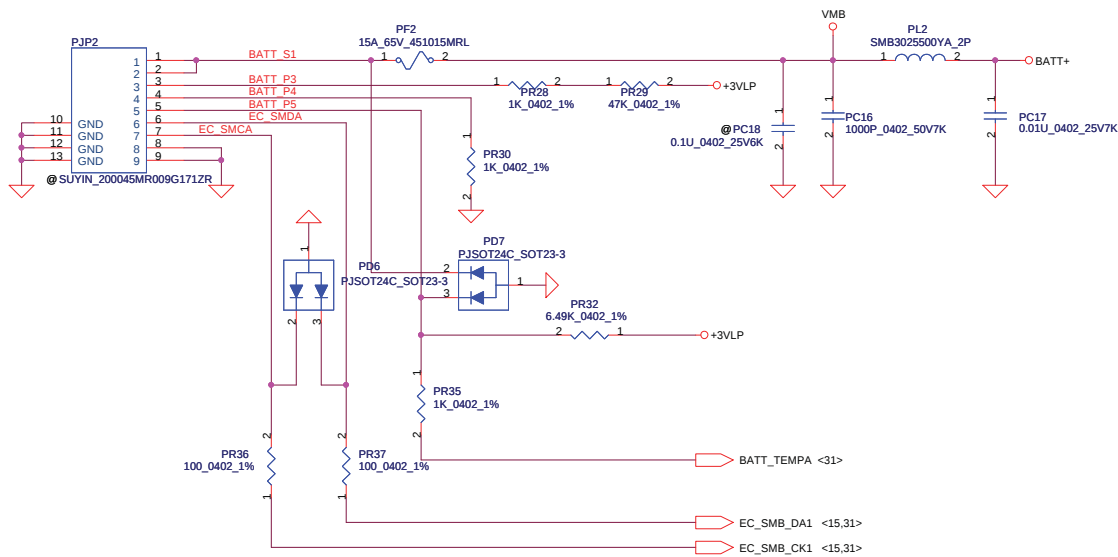
SP093MX0000



**Precharge detector
15.97V/14.84V FOR
ADAPTOR**



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/01/23				Title			
				Deciphered Date				DCIN / DETECTOR			
				2010/01/23				Size			
								Document Number			
								NWQAA LA6061P M/B			
								Rev			
								2.0			
								Date			
								Wednesday, March 24, 2010			
								Sheet			
								35 of 45			

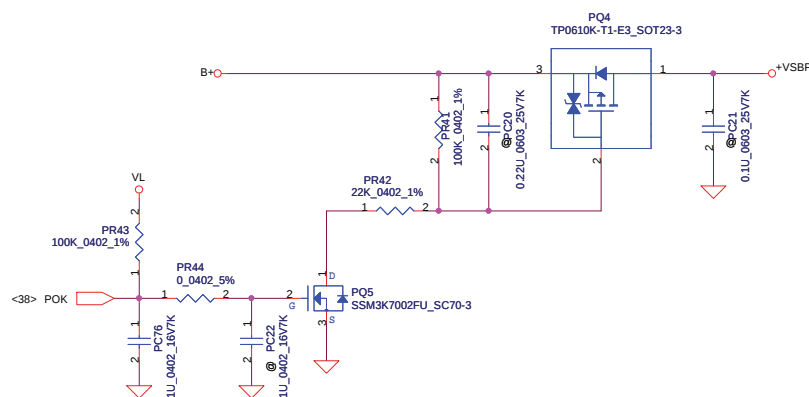
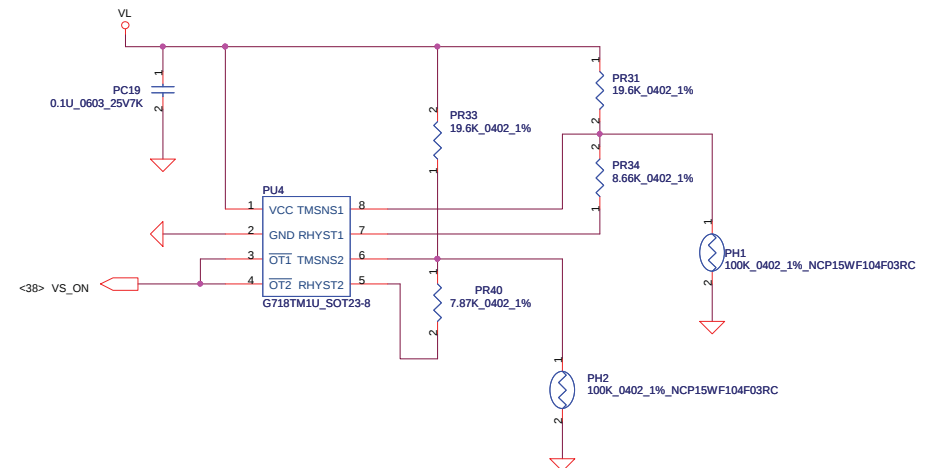


PH1 under CPU botten side :

CPU thermal protection at 95degree C
Recovery at 56 degree C

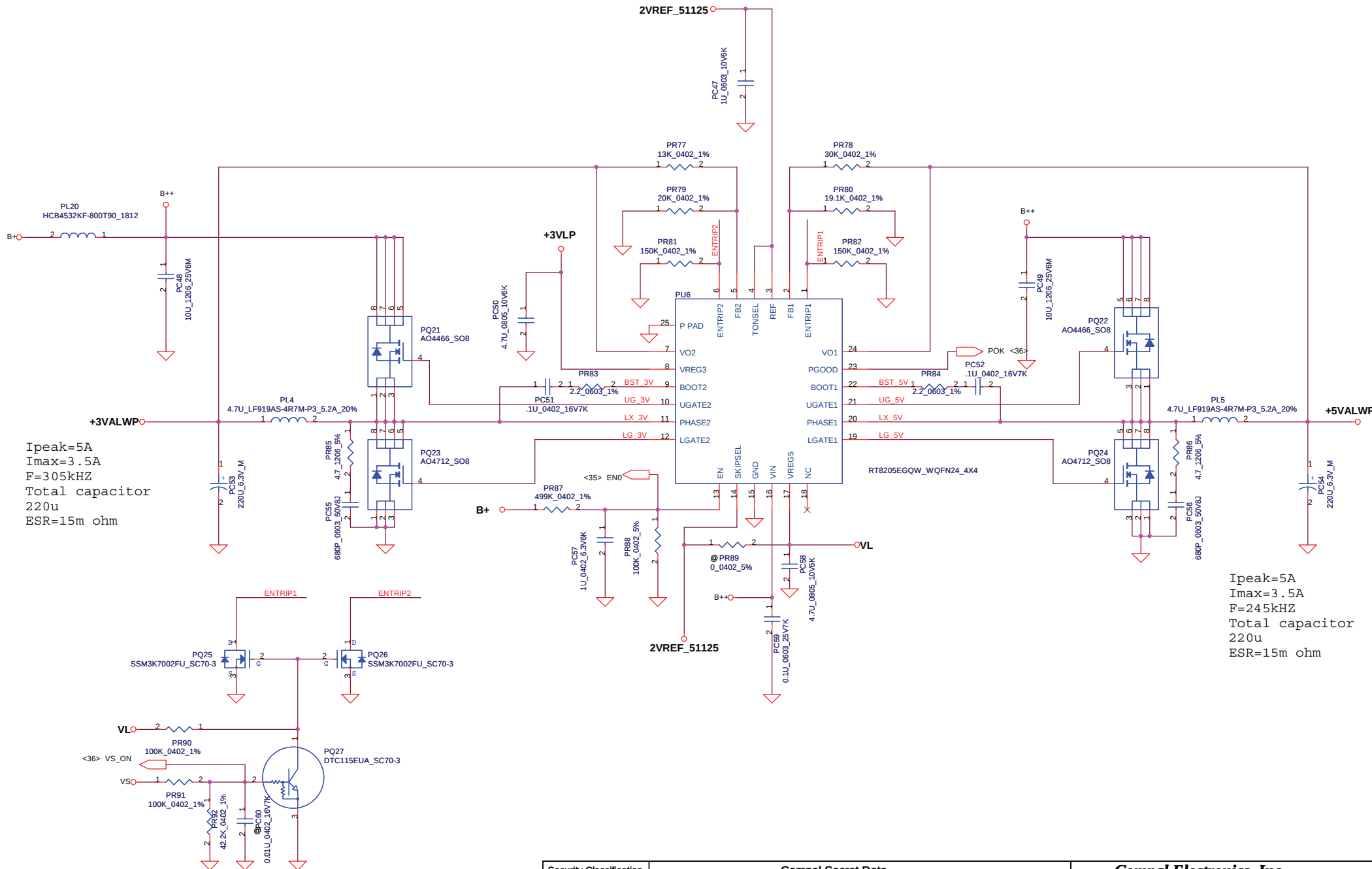
PH2 near main Battery CONN :

BAT. thermal protection at 95 degree C
Recovery at 48 degree C

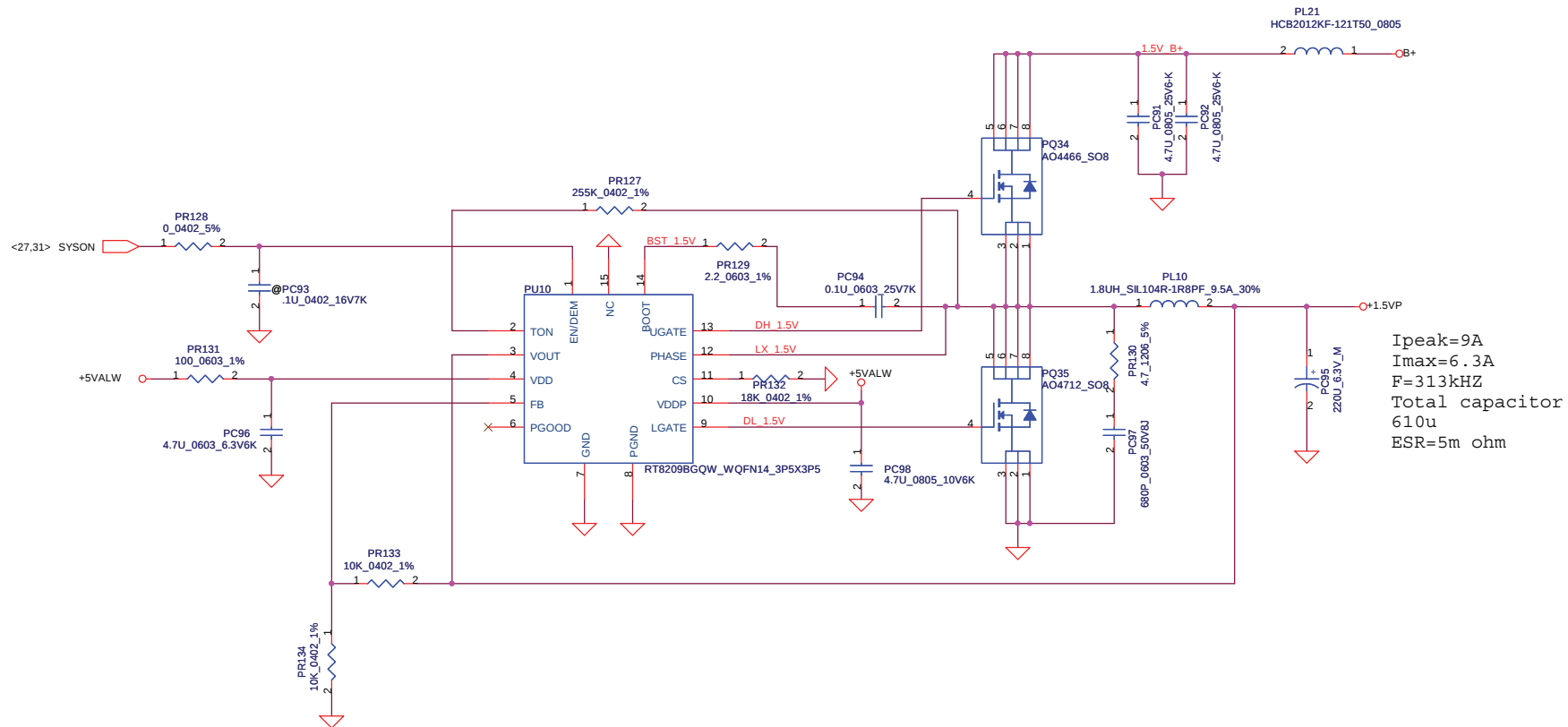


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					NWQAA LA6061P M/B
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				Sheet	36 of 45
				Rev	2.0





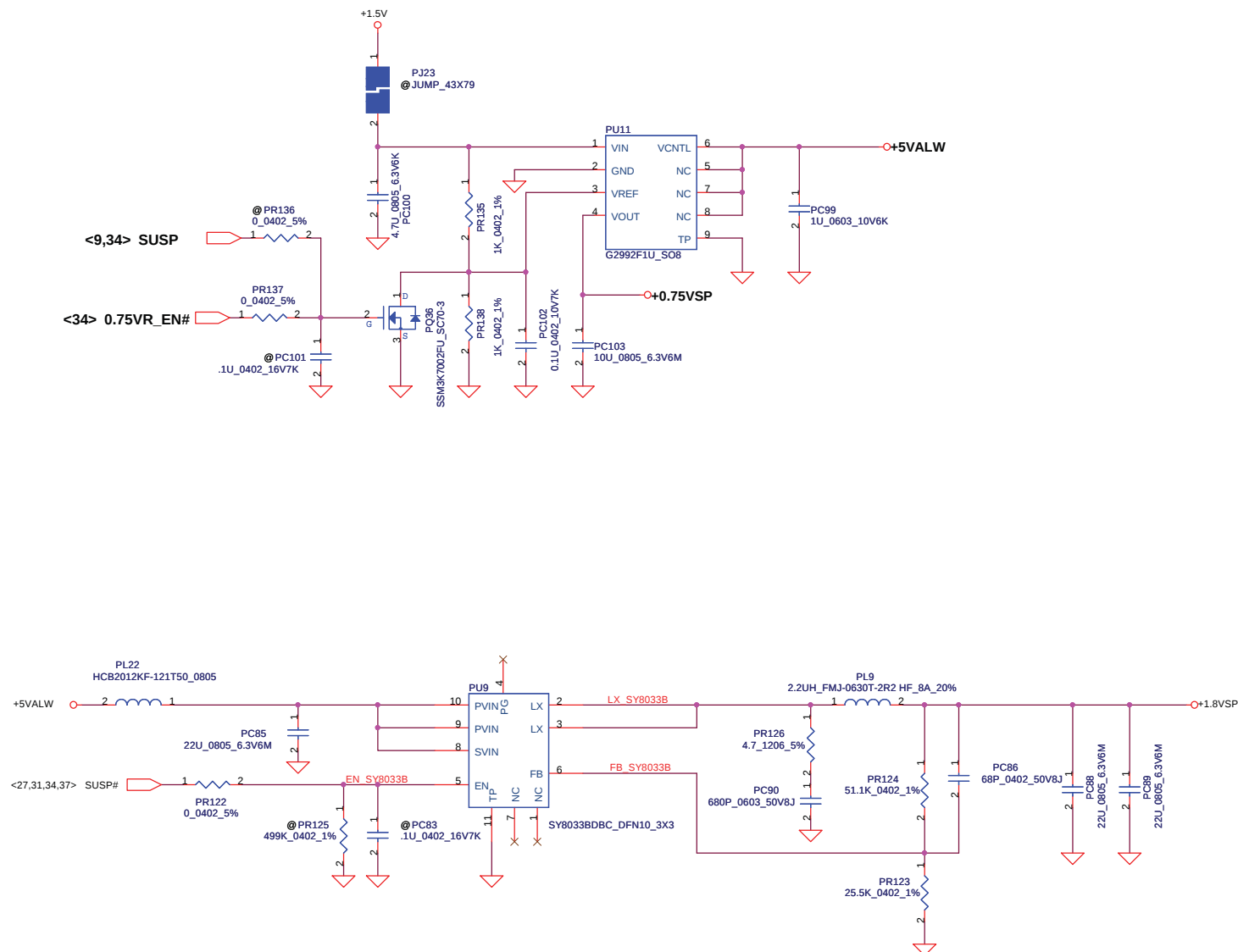
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Document Number	NWQAA LA6061P M/B		2.0	Rev
Date:	Wednesday, March 24, 2010	Sheet	38	of 45	



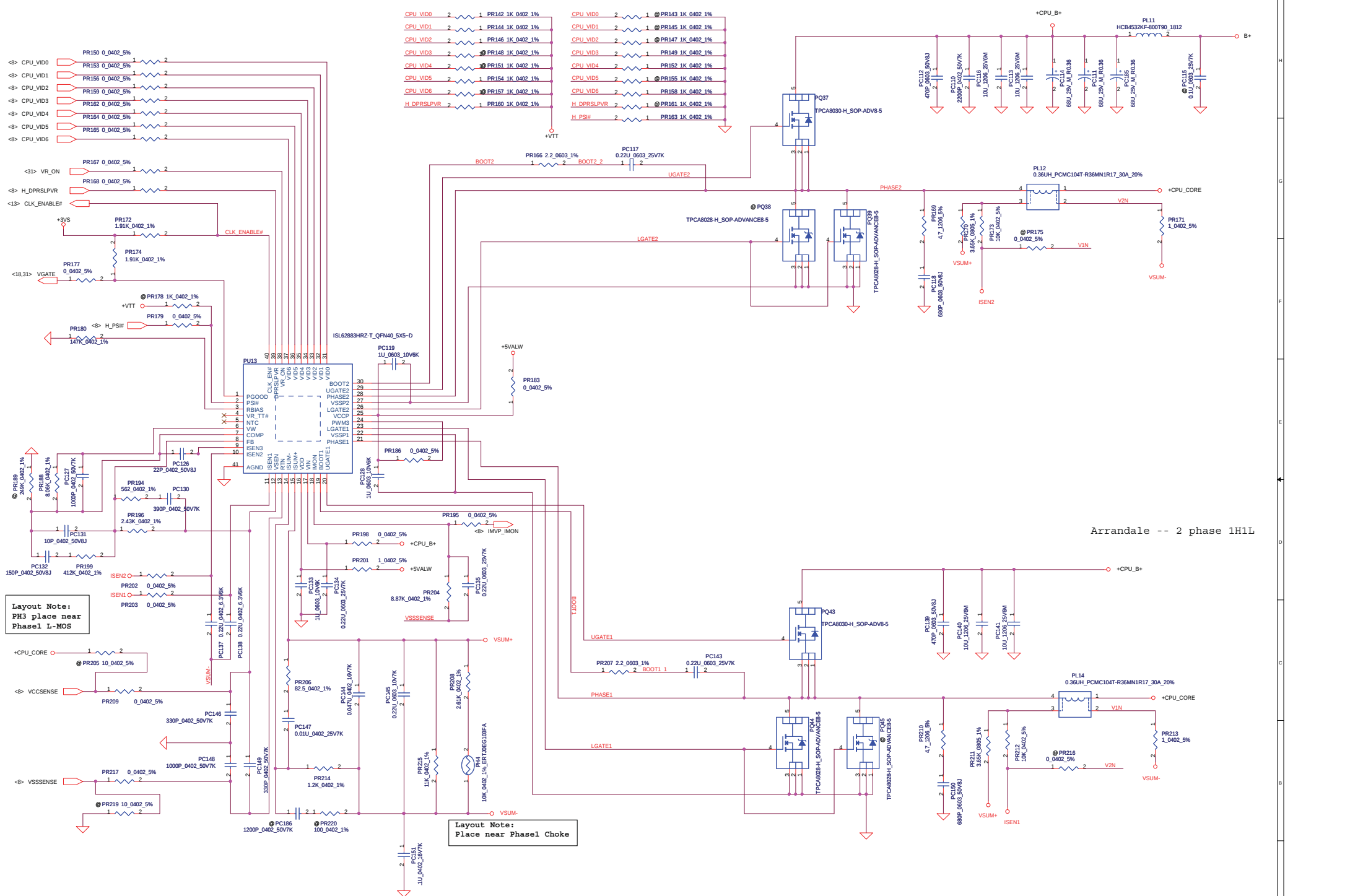
Ipeak=9A
Imax=6.3A
F=313kHz
Total capacitor
610u
ESR=5m ohm

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/01/23		Deciphered Date		2010/01/23		Title	
										+1.5VP	
										NWQAA LA6061P M/B	
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										Date: Wednesday, March 24, 2010	
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Issued Date		2009/01/23		Deciphered Date		2010/01/23		Title	
								0.75VSP/+1.8VSP	
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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT	P39-PWR_+VTTP	Change PR141 2.26k to 2.43k	Modify VTTPPWROK voltage (2009/11/25)
EVT	P39-PWR_+VTTP	Remove PC71 33P, PC72 2200P, PR101 33.2k	APW7138 not use this function (2009/11/25)
EVT	P38-PWR_3VALWP/5VALWP	Change PR92 49.9k to 42.2k	Modify VS divider voltage to drive MOS (2009/11/25)
EVT	P42-PWR_CPU_CORE	Change PL12,PL14 SH000005680 to SH00000IK00	Use 5% DCR choke (2009/11/25)
EVT	P43-PWR_GM VGA_CORE	Change PH5 SL20000058L to SL200000500	Use Compal PN (2009/11/25)
DVT	P48-PWR_BATTERY CONN / OTP	Add PD6, PD7 ESD diode	For ESD solution(2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change PL16 SH00000HK00 to SH00000IK00	Use same PN choke (2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PC114, PC111, PC185 from SF000000F80 to SF000000W00	Cost down (2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change PC161 to SGA00002680	For DVT budding(thermal issue), it will change to original type for PVT (2009/12/28)
DVT	P50-PWR_3VALWP/5VALWP	Change PR83,PR84 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR85,PR86 4.7 and PC55,PC56 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PR166,PR207 0 to 2.2	
		Add PR169,PR210 4.7 and PC118,PC150 680P	
DVT	P55-PWR_GM VGA_CORE	Change PR234 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR235 4.7 and PC163 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P48-PWR_BATTERY CONN / OTP	Change PR33 10k,PR31 21k to 19.6k, PR34 9.53k to 8.66k, PR40 47k to 7.87k	Adjust OTP setting point(2009/12/28)
DVT	P39-PWR_+VTTP	Change PR98 4.99k to 6.49k	Adjust VTT_DIS OCP to 27.49A (2009/12/31)
DVT	P49-PWR_CHARGER	Add PC73,PC74,PC75 10U	Reserve for EMI solution(2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PR204 8.25k to 8.87k	Adjust resistor for Imon (2009/12/31)
DVT	P55-PWR_GM VGA_CORE	Change PR247 34.8k to 40.2k	Adjust GFX load line (2009/12/31)
DVT	P41-PWR_0.75VSP/1.8VSP	Change PC90 SE025681K80 to SE024681J80	Use same PN (2009/12/31)
PVT	P41-PWR_0.75VSP/1.8VSP	Remove PR136, Add PR137 0 Ohm	For S3 power saving function (2010/02/03)
PVT	P43-PWR_GM VGA_CORE	Change PC161 to SF000002000	Change to original type for PVT (2010/02/03)
PVT	P49-PWR_CHARGER	Change PC24,PC25,PC26 4.7U to 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC107 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC73,PC74,PC75 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC76 0.1U	For ESD solution (2010/02/03)
PVT	P38-PWR_3VALWP/5VALWP	Change PQ27 from SSMK7002 to DTC115EUA	Use low Vth Transistor (2010/02/03)
PVT	P43-PWR_GM VGA_CORE	Change PQ46 TPCA8030 to NTMFS4921NHT1G	For EMI solution (2010/02/03)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change PR123 316k to 25.5k,PR124 402k to 51.1k	Adjust 1.8V voltage divided resistor (2010/03/07)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change PU9 from MP2121 to SY8033	MP2121 ESD fail (2010/03/07)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Delete PR125 0 Ohm	Change for SY8033 solution(2010/03/07)
		Change PC85 from 0.1U to 22U	
		Delete PC87 10UF, PC84 0.1U	
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change PC86 10U to 68P	Improve 1.8V transient under shoot(2010/03/07)
Pre MP	P49-PWR_CHARGER	Change PC24,PC25,PC26 10U to 4.7U	10U 0805 size price too high(2010/03/07)
Pre MP	P47-PWR_DCIN/DECTOR	Change PC12 from SE033105Z80 to SE000001380	Change PN(2010/03/07)

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				Power PIR		
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PIR (Product Improve Record)

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2009/12/30

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/7	25	Add +5VALW for JPIO pin5	For BACK_SENSE detect
2	12/7	13	Remove JLVDS pin10 and pin12 for +LCDVDD_R	3D Panel max. current is 1.5A
3	12/8	33	Combine JTOUCH and JLP to JTPL and remove C648	For ME cost down
4	12/17	33	Remove D19	Move D19 to LS-6061P
5	12/18	26	Reverse JBT pin definition	Due to pin reverse
6	12/18	30	Add RA43	For codec EC_MUTE# issue
7	12/21	29	Change JREAD to Push-push type (R015-211-LM-A)	For PRD update
8	12/21	13	Move LED_PWM and BKOFF#_R to JLVDS pin10 and pin12	For avoiding +LCD_INV short issue
9	12/22	32	Change H7 footprint to "DEBUG_PAD-MB-S"	For debug use
10	12/23	27	Add D24 and Q36 for BT_CTRL	For WLAN & BT combo module
11	12/23	21	Add R461	For CIR_EN#
12	12/24	25	Change JPIO footprint and reverse its pin definition	For ME request
13	12/24	15	Add R145	For U9 ESD damage issue
14	12/24	29	Add F3	For Card reader issue
15	12/29	25	Add R148 and R149	For Sleep & play music
16	12/29	13	Add C871 and C872	For RF request

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3
GERBER-OUT DATE: 2010/02/08

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	30	Add RA43	For sleep & music on battery mode
2	1/21	31	Add R462	Avoid VR_ON floating
3	1/25	32	Change UG3 to SA000022I00	For LDO issue
4	1/25	33	Change SW2 to @	For ME interfere issue
5	2/1	15	Add R130	For AOC monitor issue
6	2/1	31	Change U19 to SA00001J5A0	For KB926 E0 version
7	2/1	29	Remove F3	For UC1 ES2 sample
8	2/1	16	Add D19 and R150	For RTC charge issue
9	2/2	31	Add CAP_RST# to EC	For ESD issue
10	2/3	29	Change RC7 to 33 ohm	For EMI request

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0
GERBER-OUT DATE: 2010/03/15

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/6	29	Add QC2 and RC16	For O2 B0 workaround
2	3/7	16	Change D13.2 power to +CHGRTC	For RTC issue
3	3/12	33	Change H15-H19 to H_3P3	For ME request
4	3/15	33	Remove SW2	For ESD request
5	3/15	30	Change CA9 and CA10 to 1U	For cut-off frequency
6	3/16	30	Change MONO_IN to AGND	For high frequency noise issue

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0 TO 2.0
GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/17	29	Change cardreader to JMB385/389	For customer request
2	3/18	31	Remove D86	For ESD request
3	3/18	22	Add R52	For CRT wave issue
4	3/19	22	Change L12 to 2.2 ohm	For CRT wave issue
5	3/22	15	Add D54	For HDMI CEC issue
6	3/24	13	Change C213 to 1U	For NALAA ESATA performance low issue

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