

COMPAL CONFIDENTIAL

MODEL NAME : *KML50*

PCB NO : *LA-4596P (DA60000B710)*

BOM P/N : *11*

Half Penny Bridge 15.4

Compal Confidential

Schematic Document

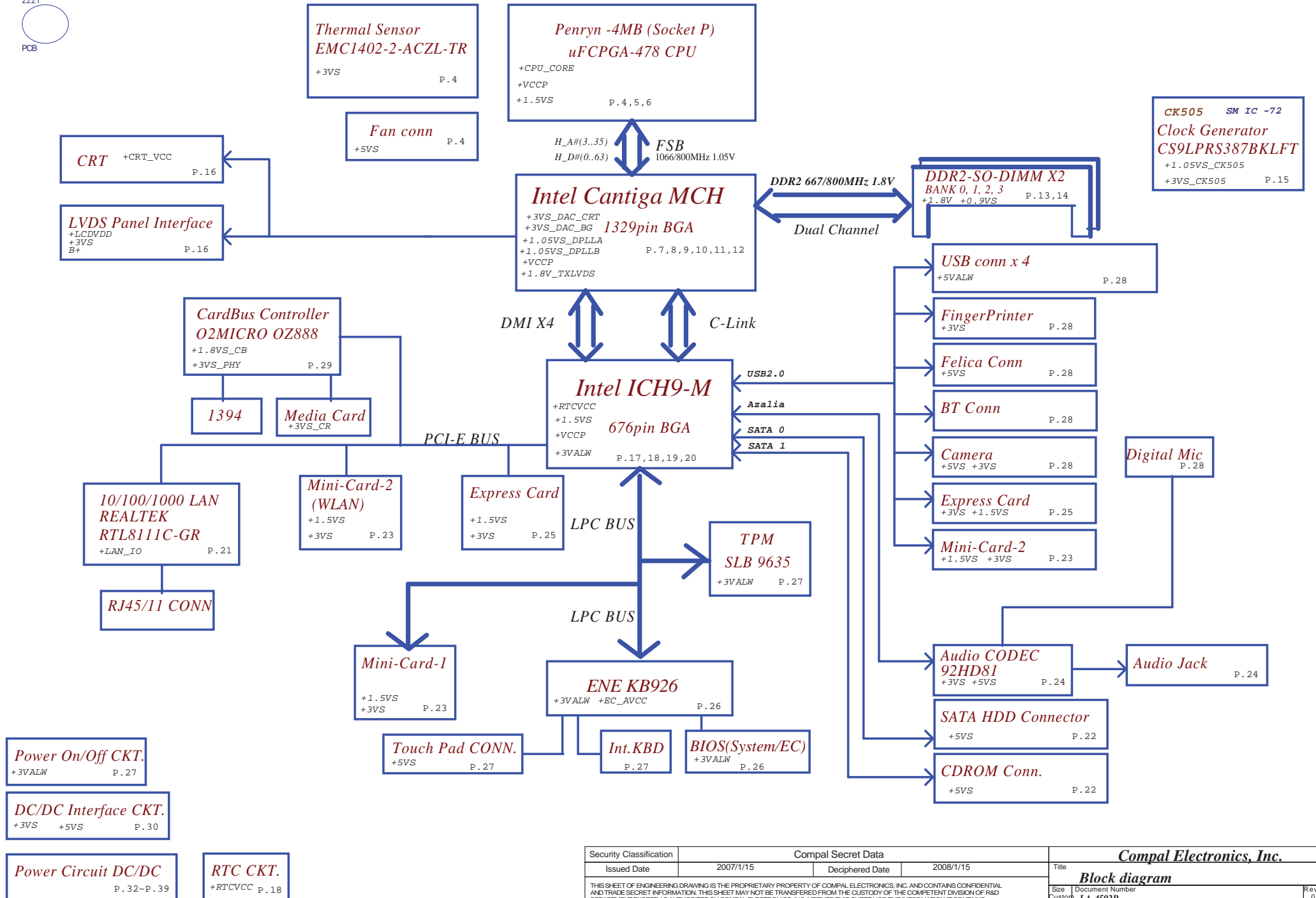
Cantiga + ICH9

2009 / 01 / 14 Rev:1.0(A00)

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	<i>Cover Sheet</i>	
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Half Penny Bridge 15.4

File Name : LA-4596P



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Issued Date	2007/1/15	Deciphered Date
		2008/1/15

Title		Compal Electronics, Inc.	
Block diagram			

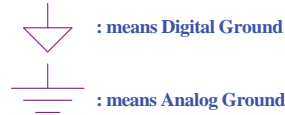
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<http://laptopmotherboard.com/html/compal.html>

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



○ : means just reserve , no build
 CONN@ : means ME CONN compont.
 TPM@:TPM compont

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
1	CAMERA	
2	JUSBP3 Top	
3	Felica	
4	Blue Tooth	
5	Finger Printer	
6	JMINI2-WLAN	
7	Express card	
8	JUSBP3 Bottom	
9	JMINI1-WWAN	
10	JUSBP4	
11	NA	

SMBUS Control Table

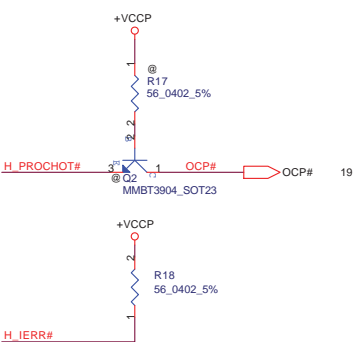
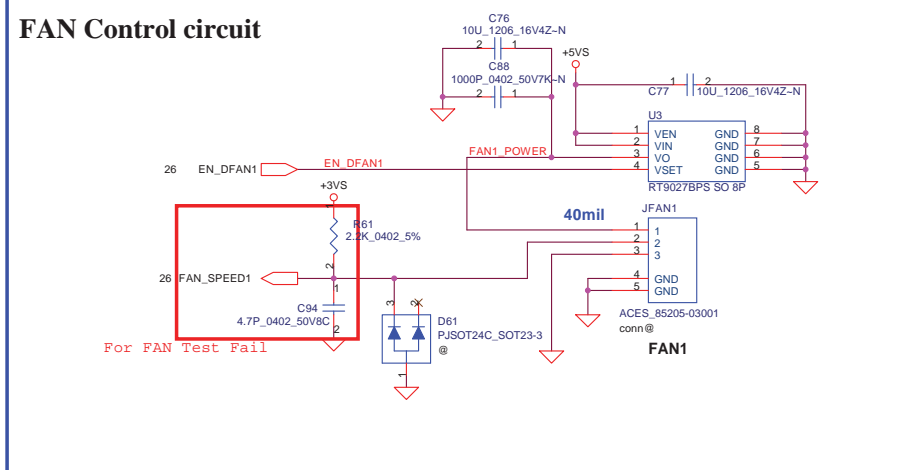
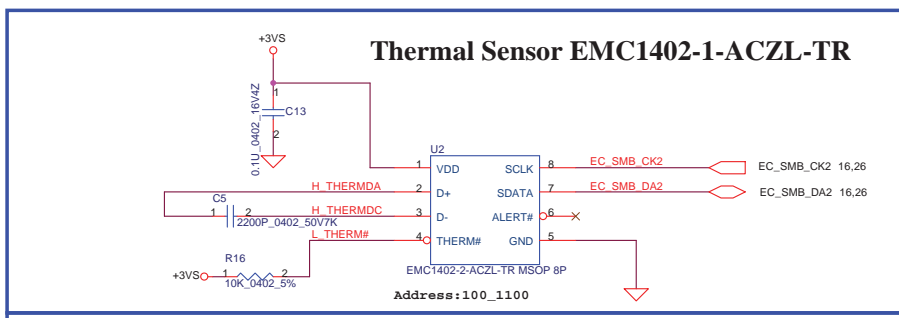
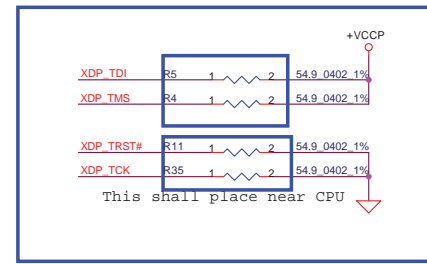
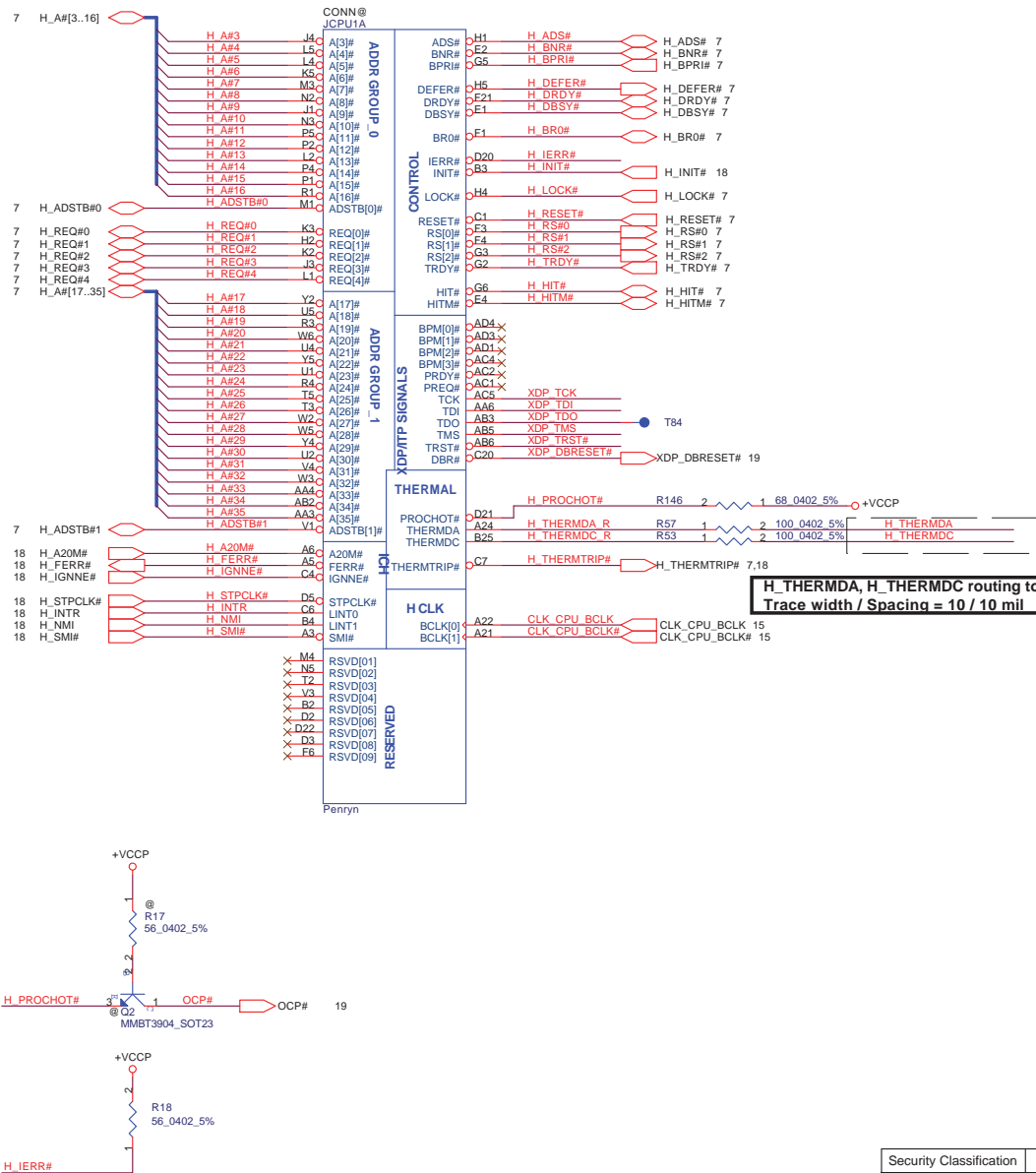
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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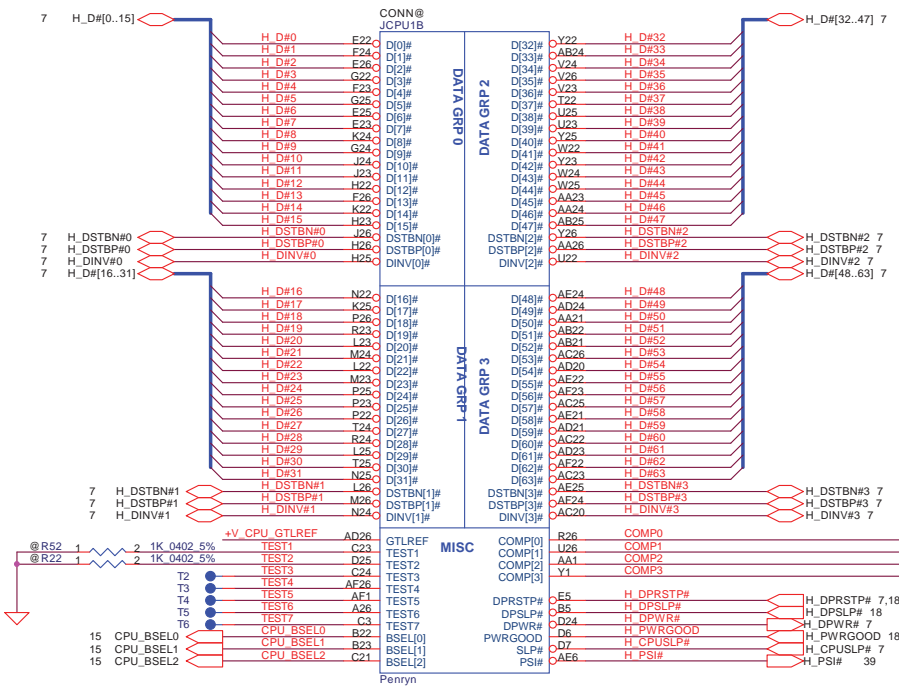
http://lap01.mh.com/compal/compal_electronics.com



H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

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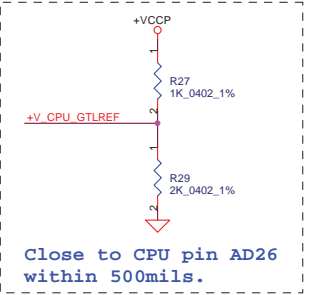
<http://laptop-motherboard.com/home.html>



layout note: Rout H_DPRSTP# from ICH9 to IMPV6 then to GMCH & CPU
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

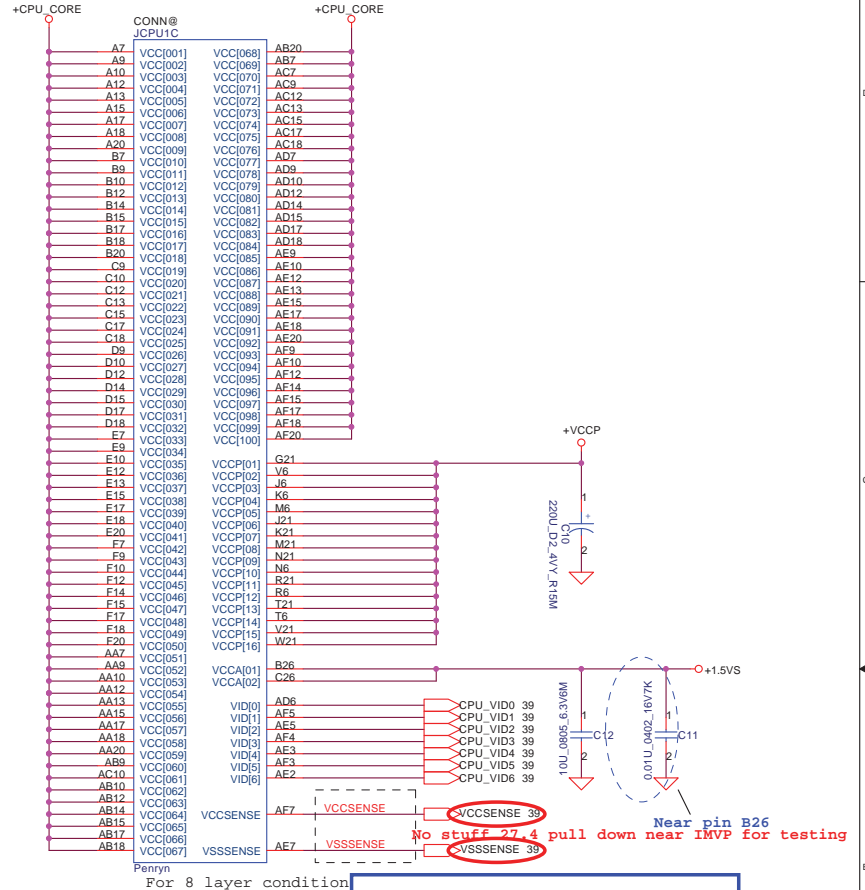
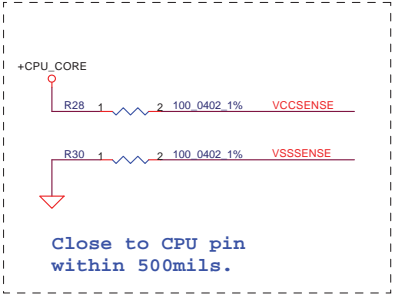
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4



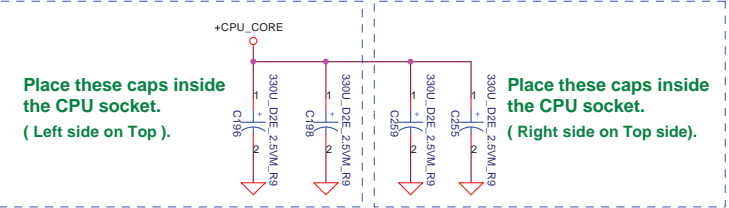
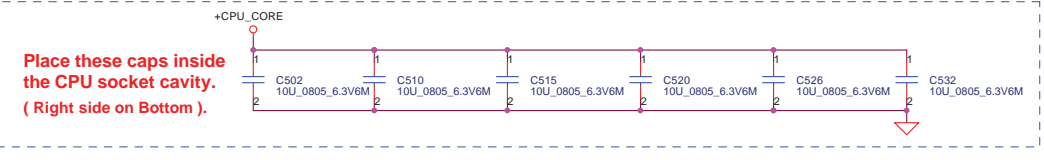
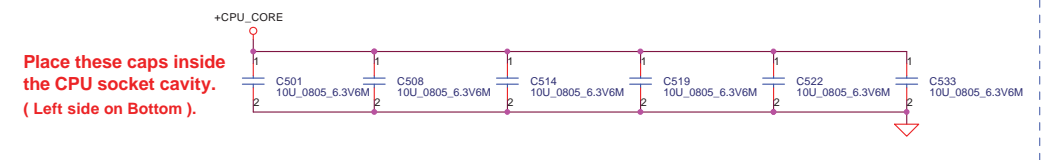
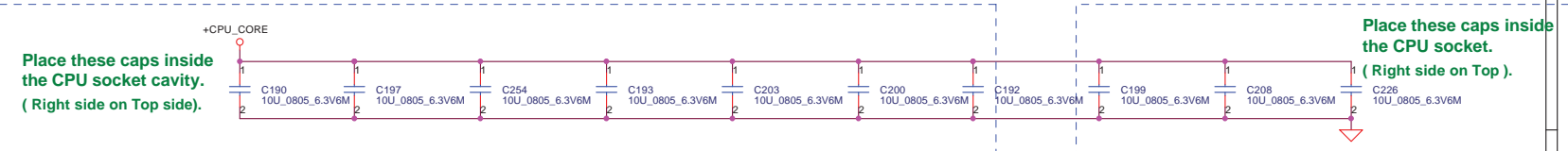
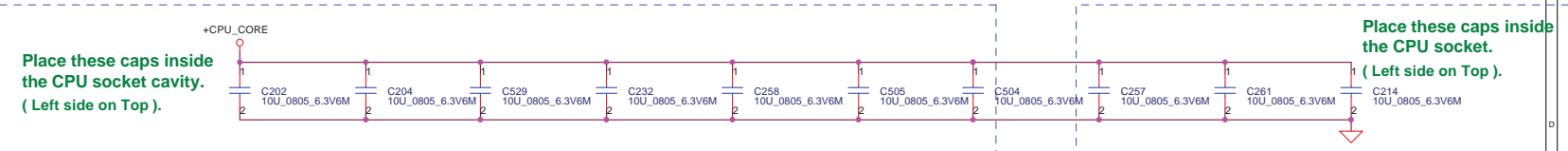
For 6 layer
 $Z=27.4 \text{ ohm}$
 VCCSENSE, VSSSENSE/ 14mils (MS),
 16mils (SL) width, 7mils space, 25mils
 space to other signals Mismatch =25mils.

Length match within 25 mils.
 The trace width/space/other is 20/7/25.



High Frequency Decoupling
10uF 0805 X5R -> 85 degree.

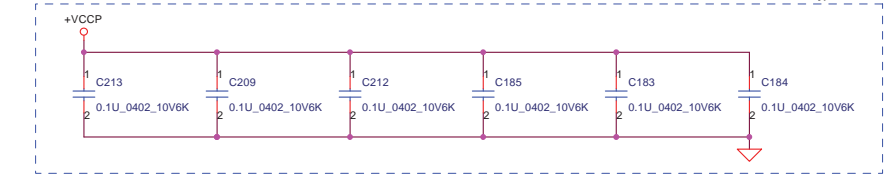
CONN@	JCPU1D				
A4	VSS001	VSS082	P6		
A8	VSS002	VSS083	P24		
A11	VSS003	VSS084	R2		
A14	VSS004	VSS085	R5		
A16	VSS005	VSS086	R22		
A19	VSS006	VSS087	R25		
A23	VSS007	VSS088	T1		
AF2	VSS008	VSS089	T4		
B6	VSS009	VSS090	T23		
B8	VSS010	VSS091	T26		
B11	VSS011	VSS092	U3		
B13	VSS012	VSS093	U6		
B16	VSS013	VSS094	U21		
B19	VSS014	VSS095	U24		
B21	VSS015	VSS096	V2		
B24	VSS016	VSS097	V5		
C5	VSS017	VSS098	V22		
C8	VSS018	VSS099	V25		
C11	VSS019	VSS100	W1		
C14	VSS020	VSS101	W4		
C16	VSS021	VSS102	W23		
C2	VSS022	VSS103	W26		
C22	VSS023	VSS104	Y3		
C25	VSS024	VSS105	Y6		
D1	VSS025	VSS106	Y21		
D4	VSS026	VSS107	Y24		
D8	VSS027	VSS108	AA2		
D11	VSS028	VSS109	AA5		
D13	VSS029	VSS110	AA8		
D16	VSS030	VSS111	AA11		
D19	VSS031	VSS112	AA14		
D23	VSS032	VSS113	AA16		
D26	VSS033	VSS114	AA19		
E3	VSS034	VSS115	AA22		
E6	VSS035	VSS116	AA25		
ER	VSS036	VSS117	AB1		
E11	VSS037	VSS118	AB4		
E14	VSS038	VSS119	AB8		
E16	VSS039	VSS120	AB11		
E19	VSS040	VSS121	AB13		
E21	VSS041	VSS122	AB16		
E24	VSS042	VSS123	AB19		
F5	VSS043	VSS124	AB23		
F8	VSS044	VSS125	AB26		
F11	VSS045	VSS126	AC3		
F13	VSS046	VSS127	AC6		
F16	VSS047	VSS128	AC8		
F19	VSS048	VSS129	AC11		
F2	VSS049	VSS130	AC14		
F22	VSS050	VSS131	AC16		
F25	VSS051	VSS132	AC19		
G4	VSS052	VSS133	AC21		
G1	VSS053	VSS134	AC24		
G23	VSS054	VSS135	AD2		
G26	VSS055	VSS136	AD5		
H3	VSS056	VSS137	AD8		
HR	VSS057	VSS138	AD11		
H21	VSS058	VSS139	AD13		
H24	VSS059	VSS140	AD19		
J2	VSS060	VSS141	AD22		
J5	VSS061	VSS142	AD25		
J22	VSS062	VSS143	AE1		
J25	VSS063	VSS144	AE4		
K1	VSS064	VSS145	AE8		
K4	VSS065	VSS146	AE11		
K23	VSS066	VSS147	AE14		
K26	VSS067	VSS148	AE16		
L3	VSS068	VSS149	AE19		
L6	VSS069	VSS150	AE23		
L21	VSS070	VSS151	AE26		
L24	VSS071	VSS152	A2		
M2	VSS072	VSS153	AF6		
M5	VSS073	VSS154	AF8		
M22	VSS074	VSS155	AF11		
M25	VSS075	VSS156	AF13		
N1	VSS076	VSS157	AF16		
N4	VSS077	VSS158	AF19		
N23	VSS078	VSS159	AF21		
N26	VSS079	VSS160	A25		
P3	VSS080	VSS161	AF25		
VSS081	VSS162				
VSS082	VSS163				



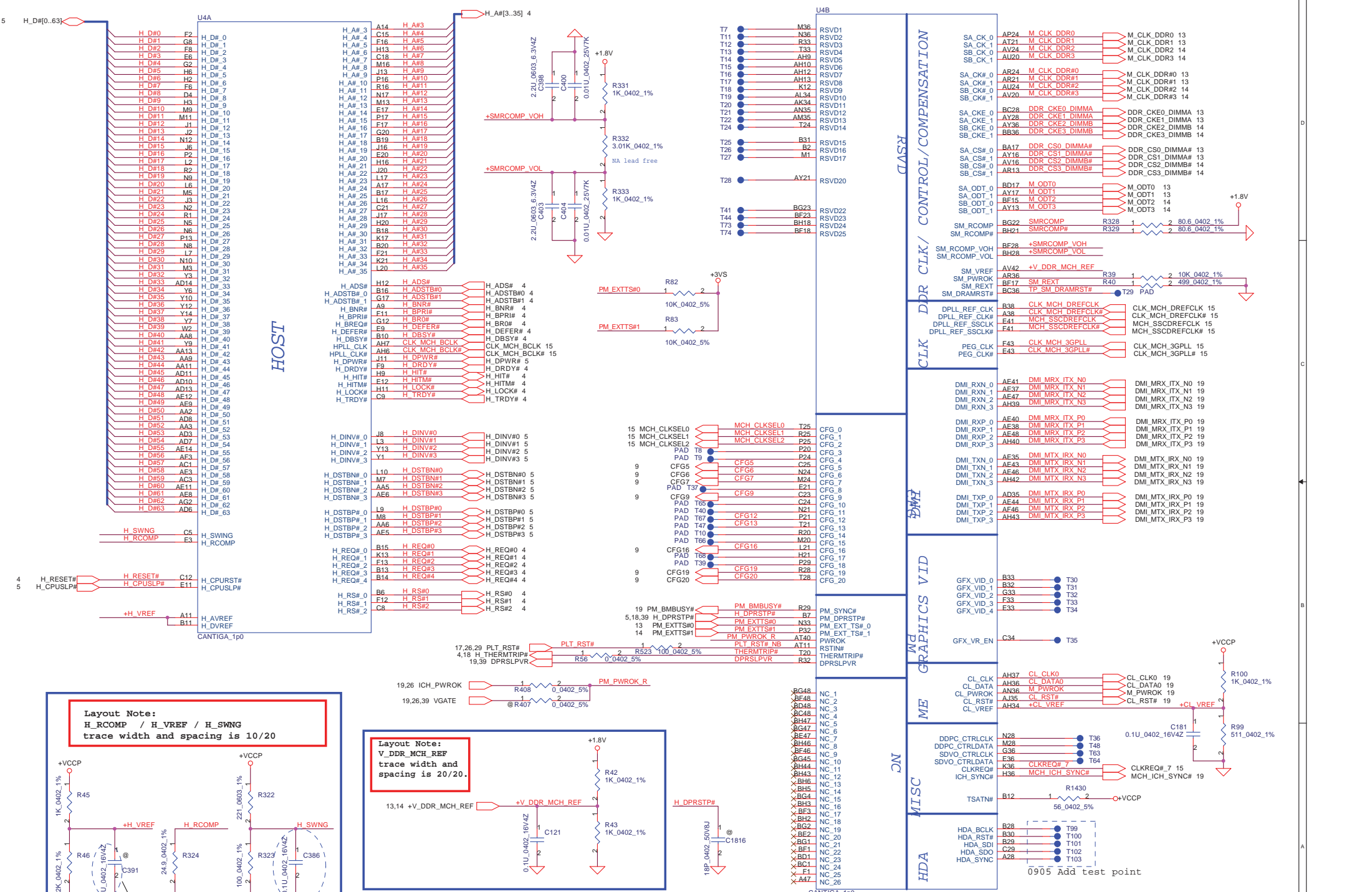
ESR <= 1.5m ohm
Capacitor > 880 uF



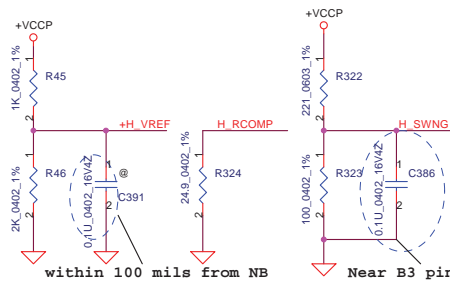
Place these inside socket cavity on L8 (North side Secondary)



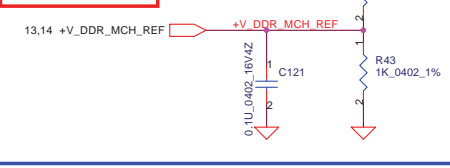
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Layout Note:
 H_RCOMP / H_VREF / H_SWNG
 trace width and spacing is 10/20

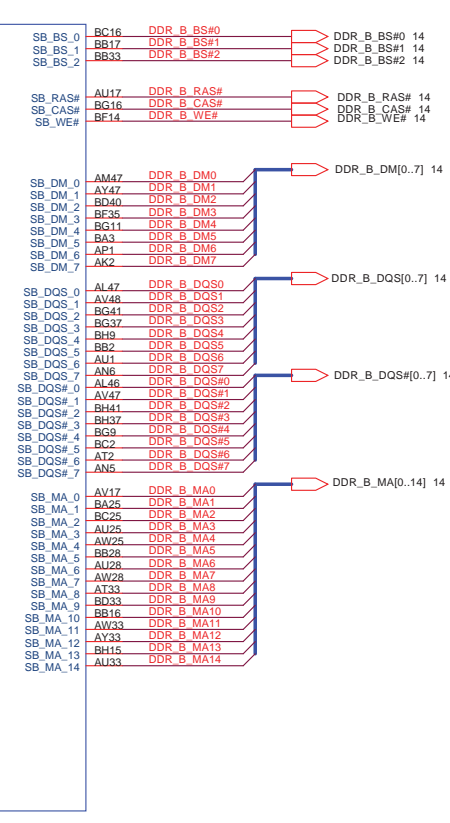
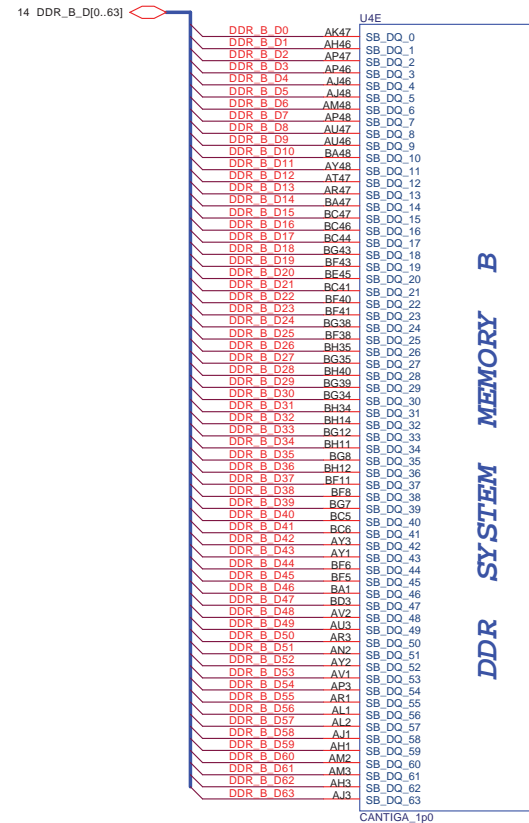
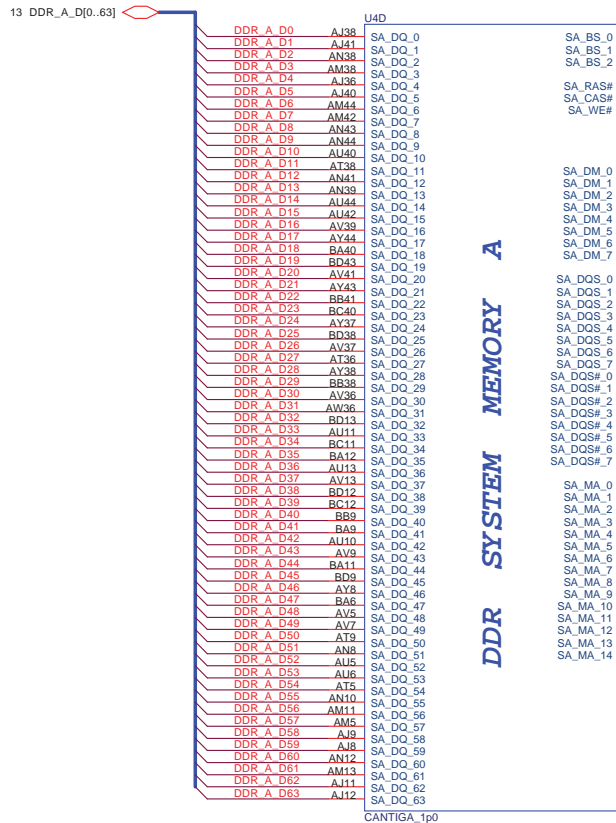


Layout Note:
 V_DDR_MCH_REF
 trace width and spacing is 20/20.

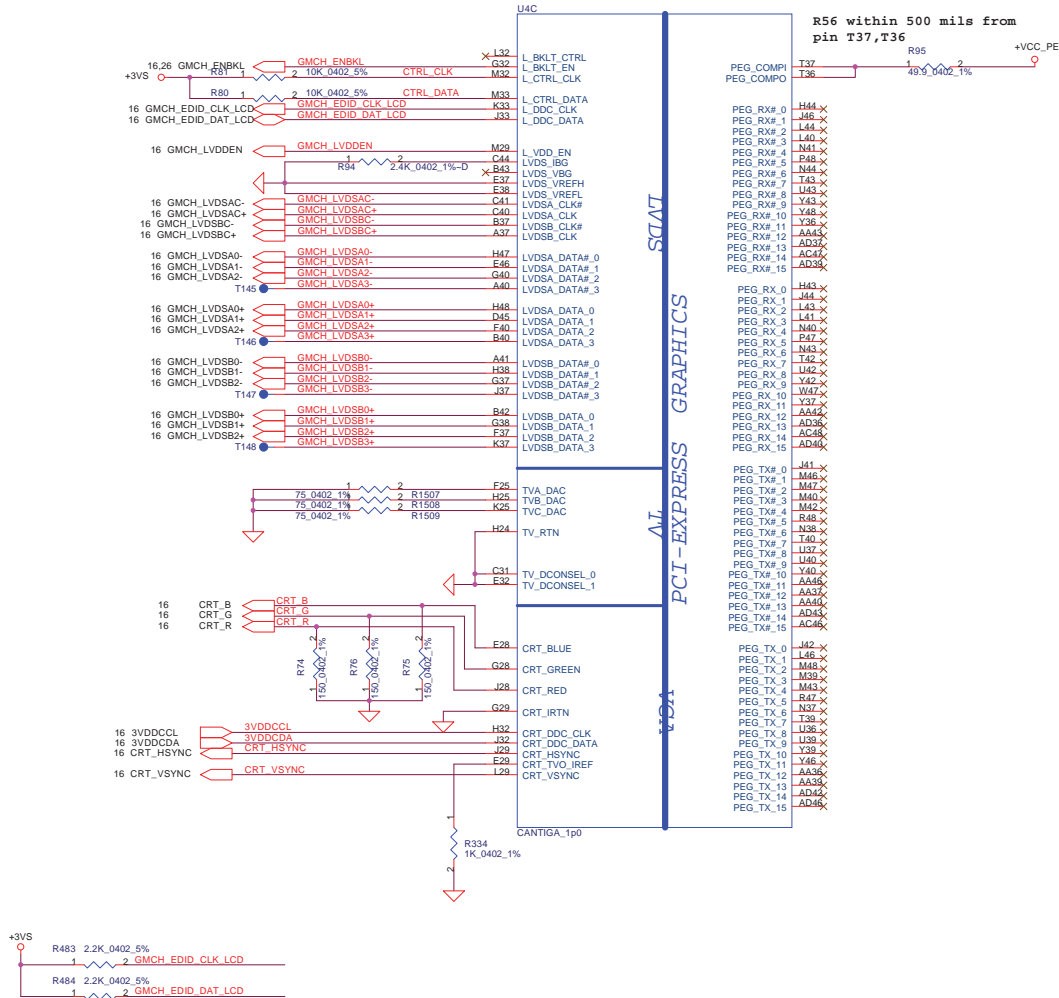


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<http://laptop.mobi.com/forums/compal/compal.com>

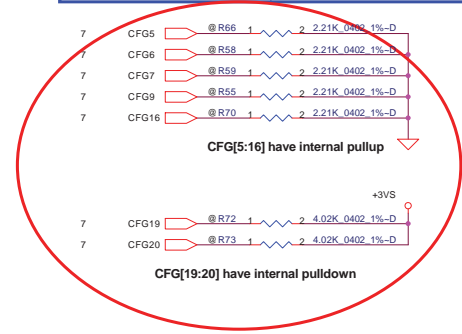


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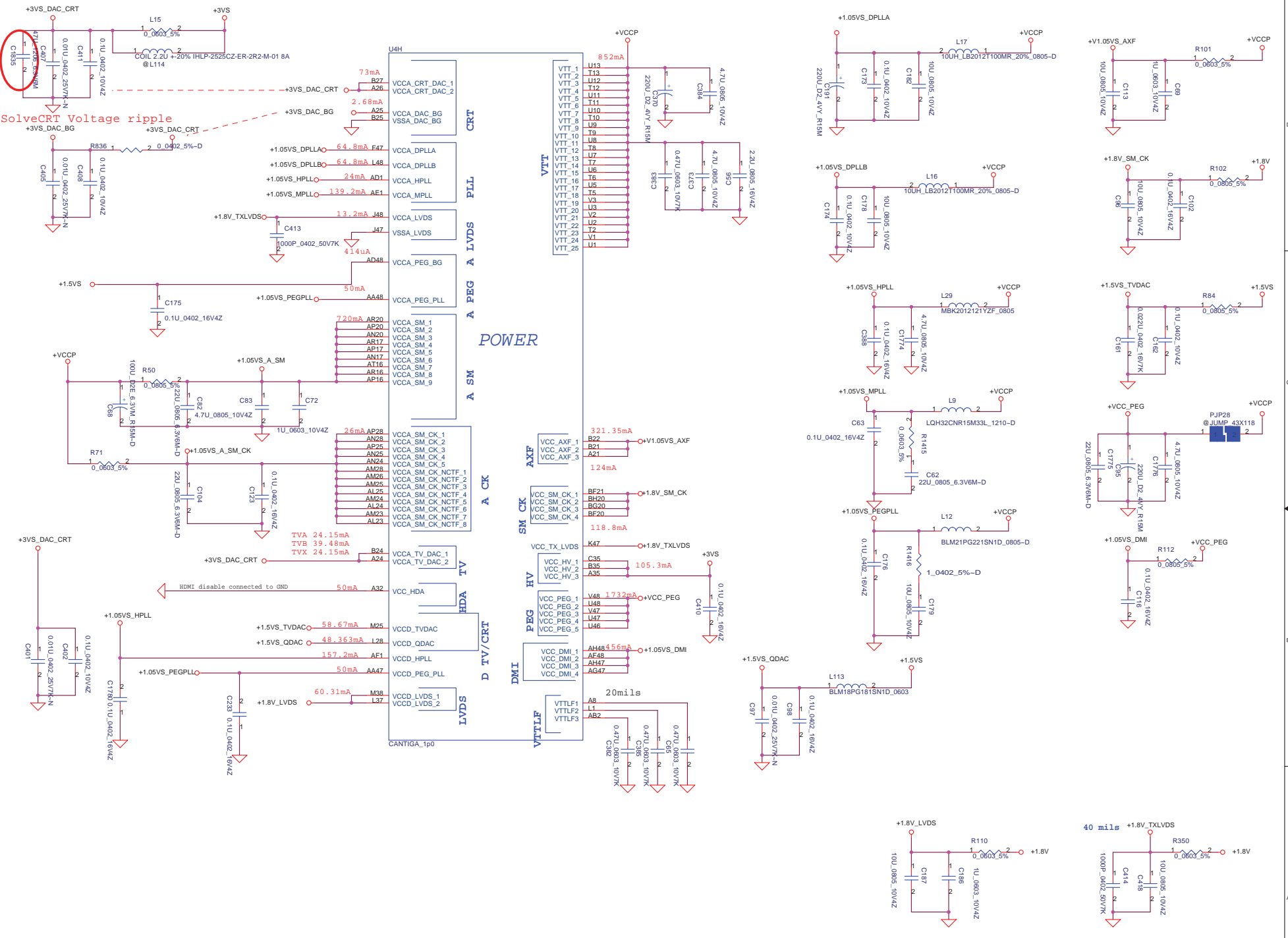
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable * 1 = The ITPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chipper suite with no confidentiality 1 = (TLS)chipper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



PCI-EXPRESS GRAPHICS

<http://laptop-motherboard.com/compal-electronics-bios-poc.com/>

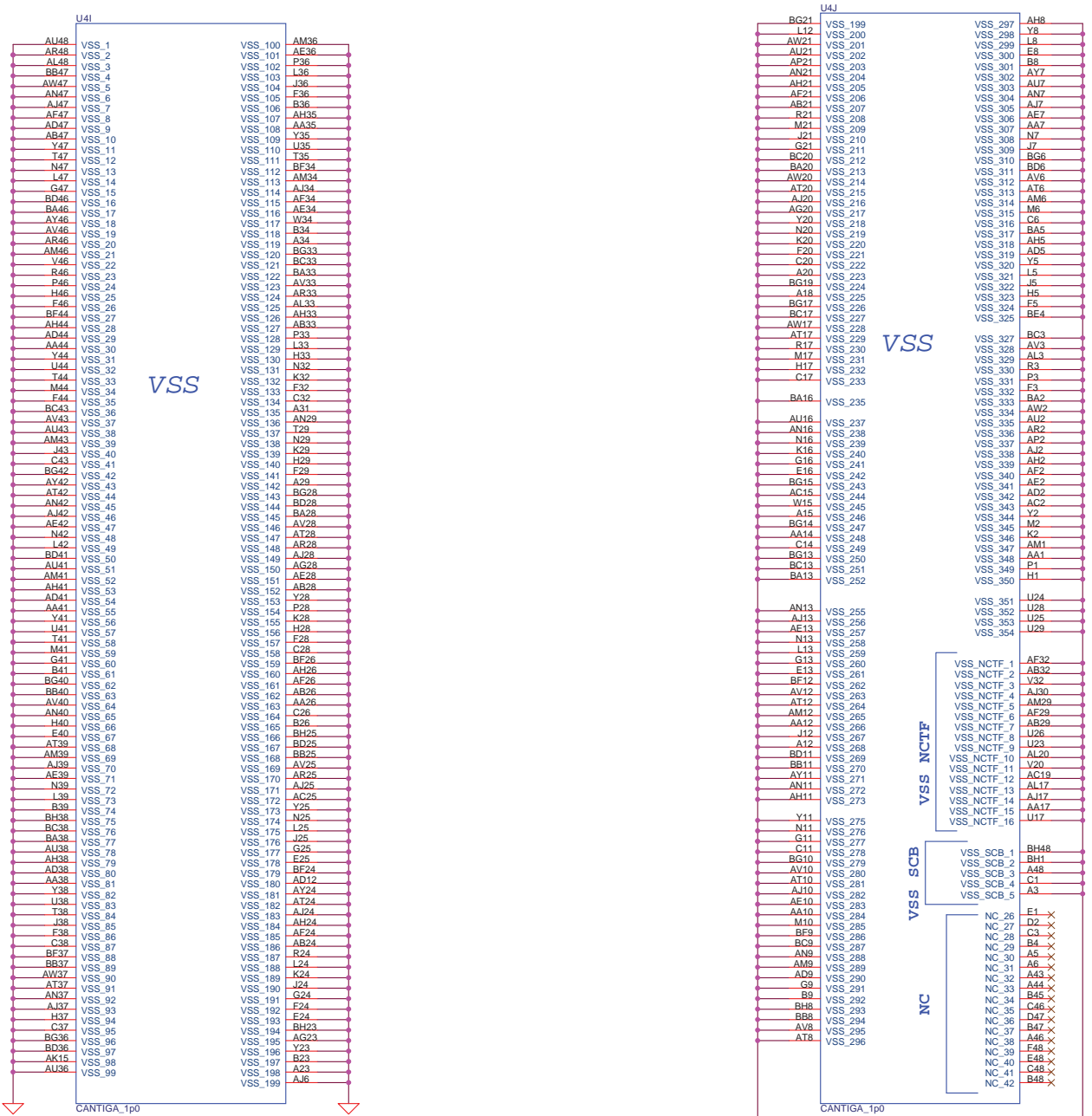


POWER

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Cantiga(4/6)-PWR	
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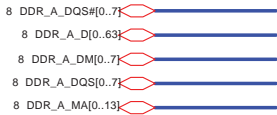
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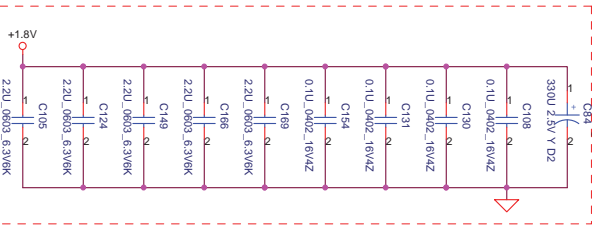
Cantiga(6/6)-PWR/GND

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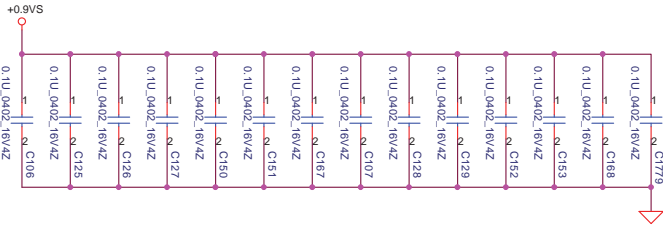
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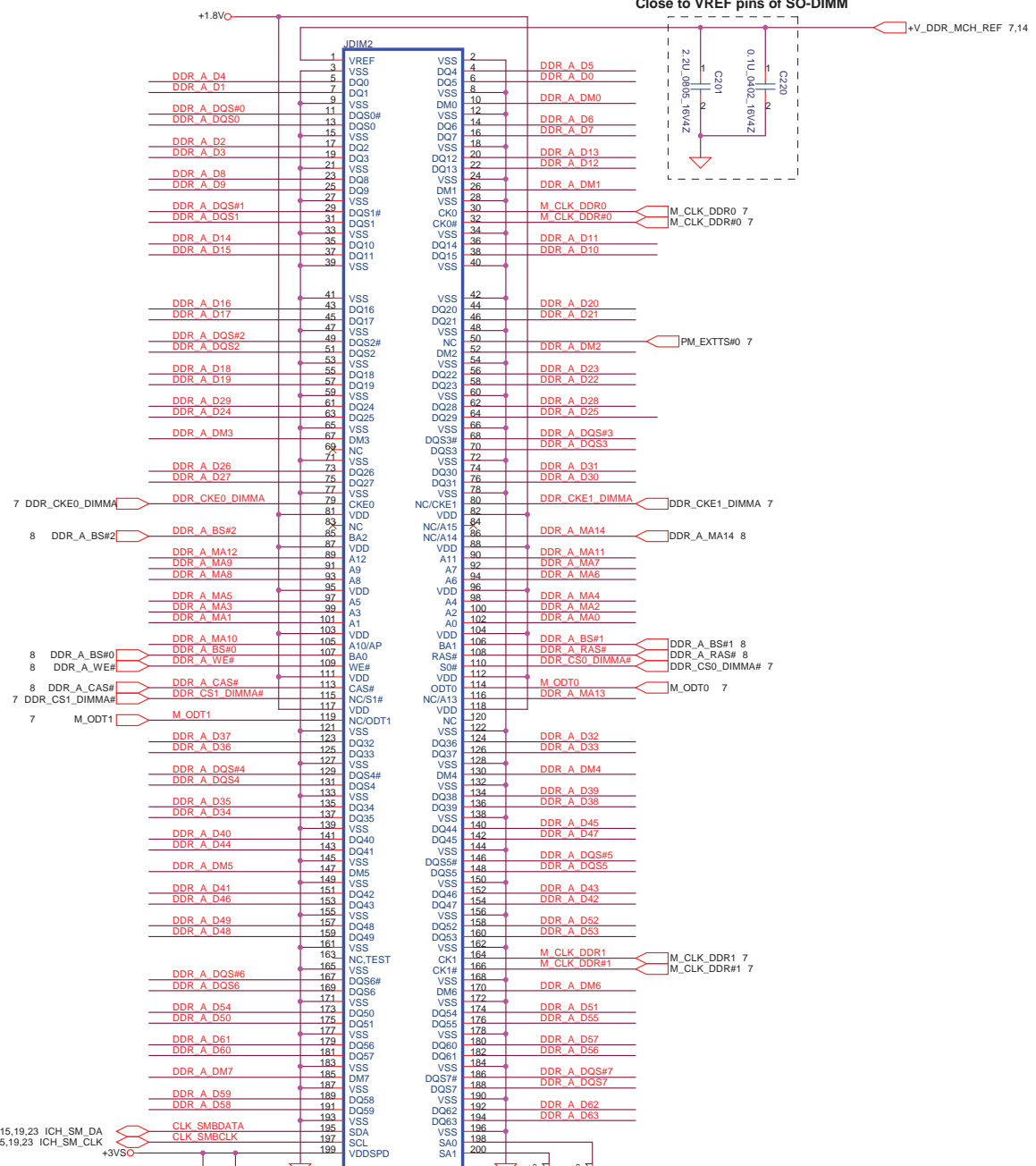
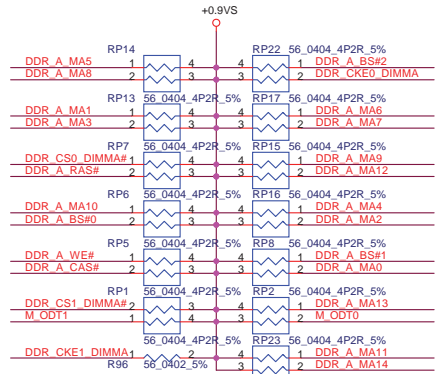
Layout Note:
Place near JDIM1



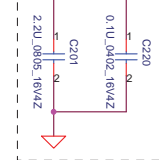
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"

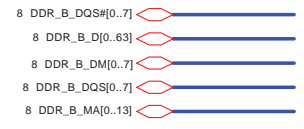


Close to VREF pins of SO-DIMM

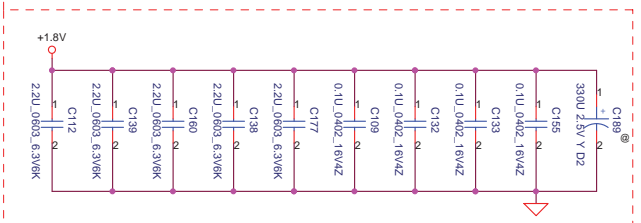


**SO-DIMM A
REVERSE
Bottom side**

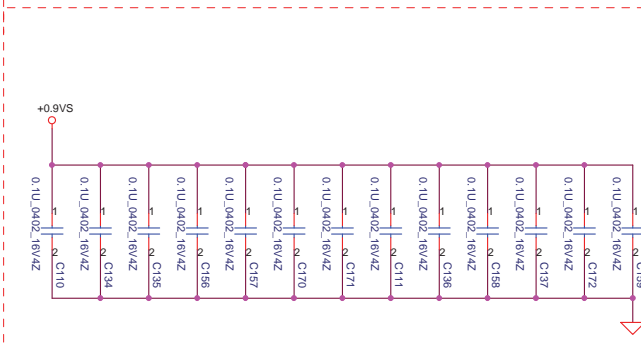
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http://www.compalelectronics.com/				LA-4592P	Rev 0.2
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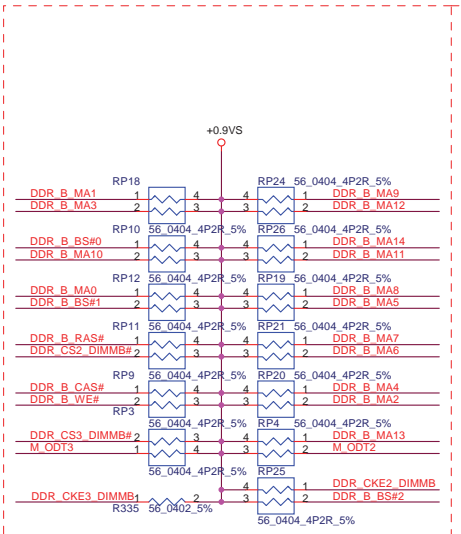
Layout Note:
Place near JDIM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



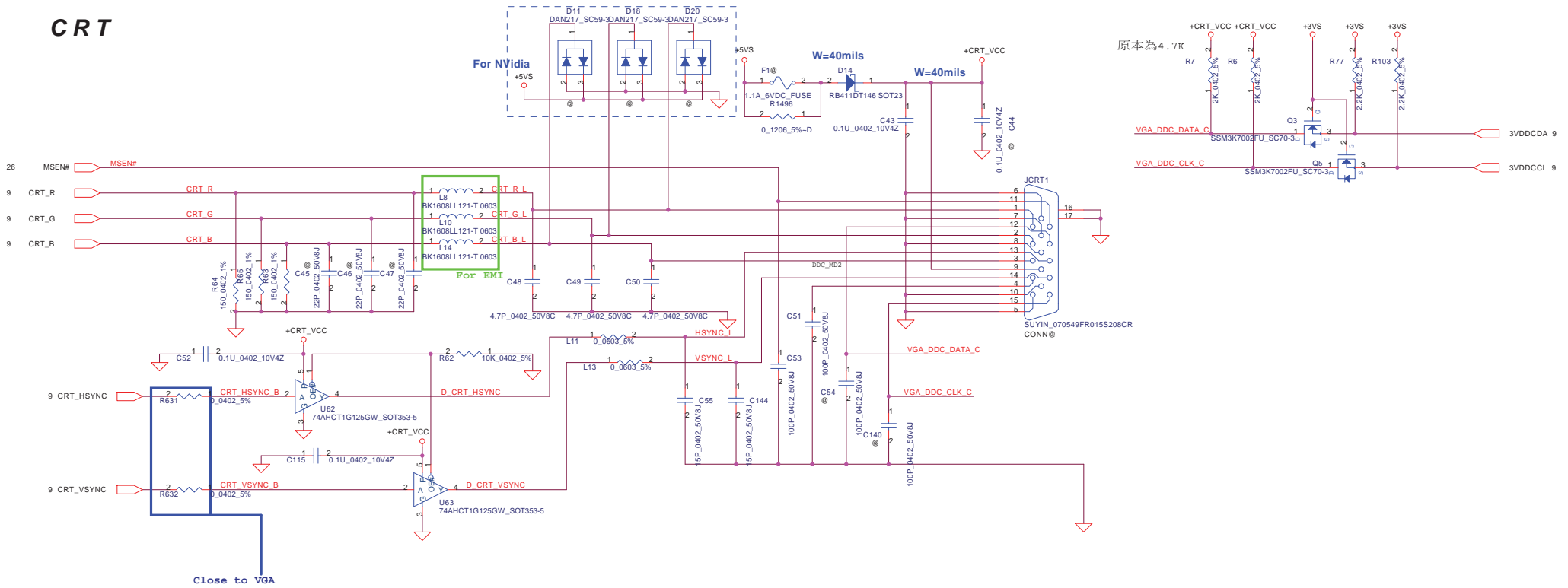
Layout Note:
Place these resistor closely JP42, all trace length Max<1.5"



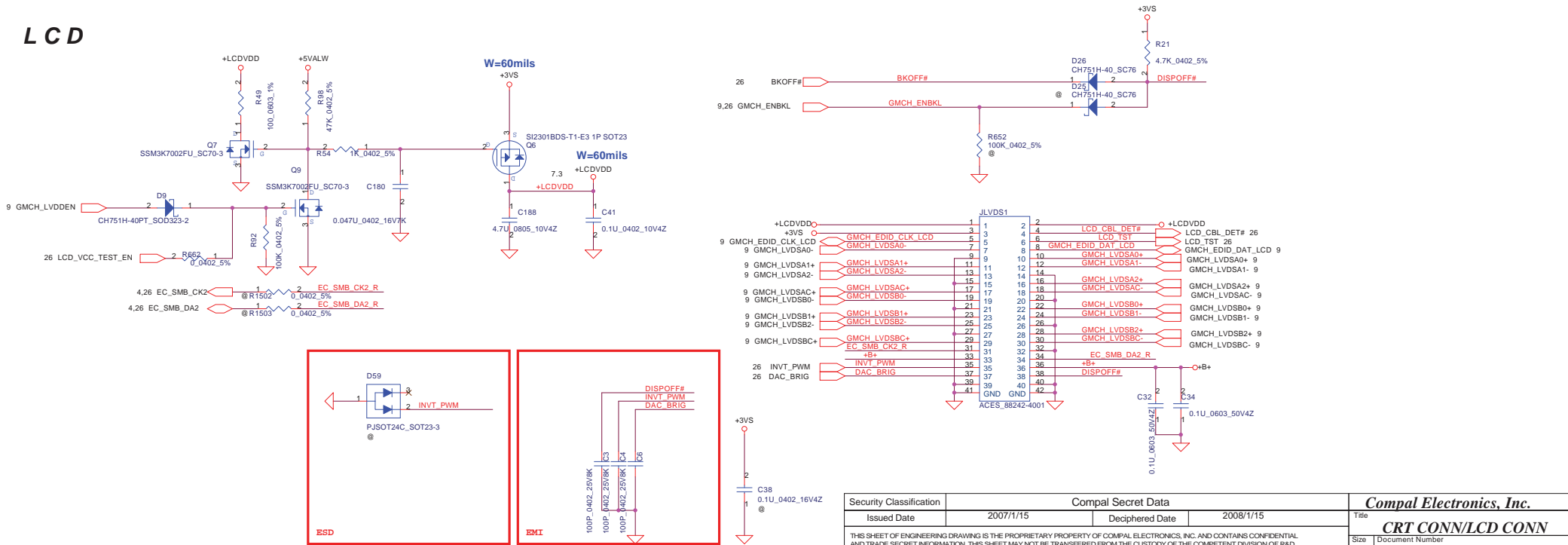
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Document Number
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DDR2 SO-DIMM II

CRT



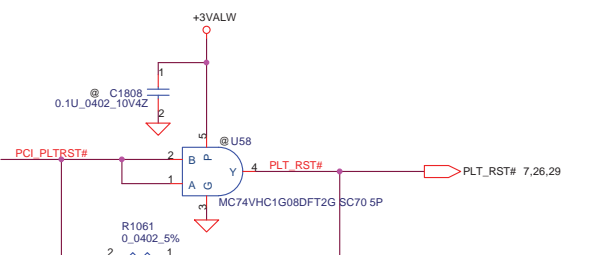
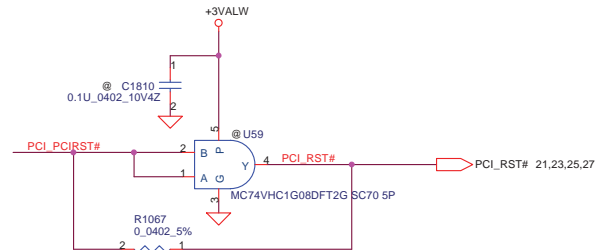
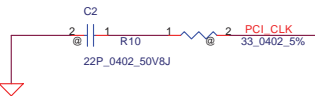
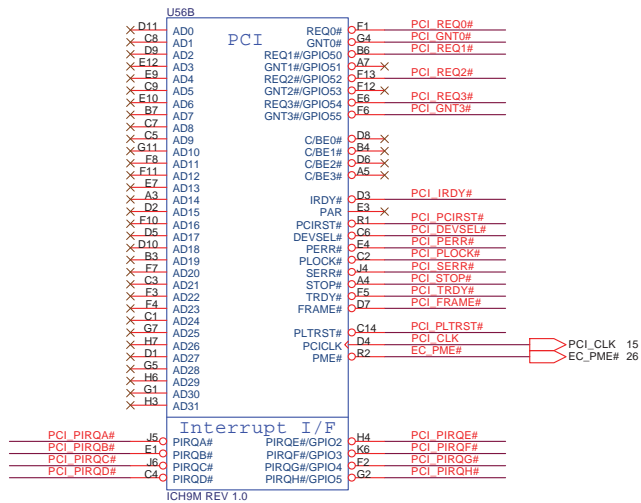
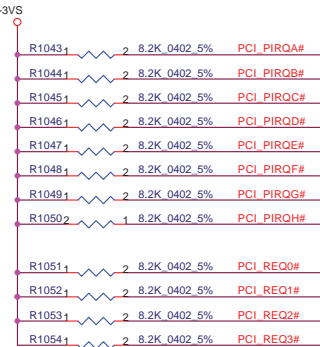
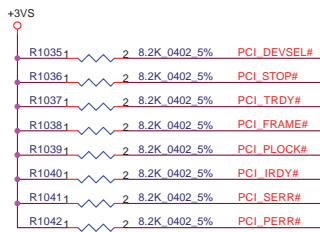
LCD



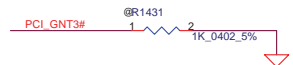
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Issued Date	2007/1/15	Deciphered Date
		2008/1/15

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CRT CONN/LCD CONN	
Size	Document Number
Custom	LA-4592P
Date:	Thursday, February 19, 2009
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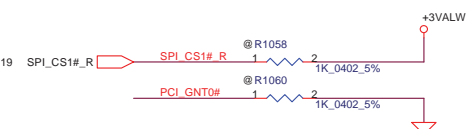
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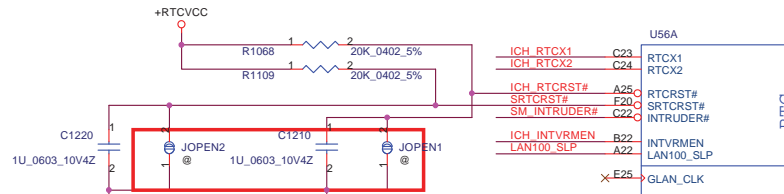
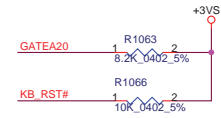
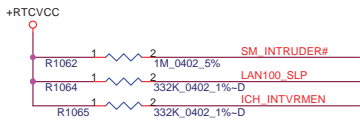


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

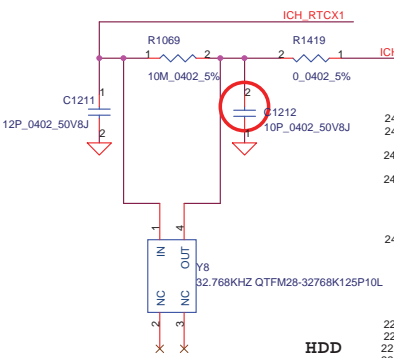


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



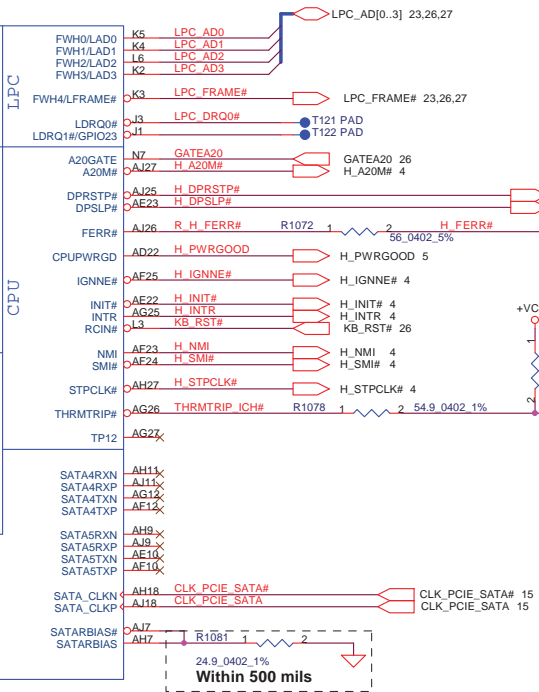
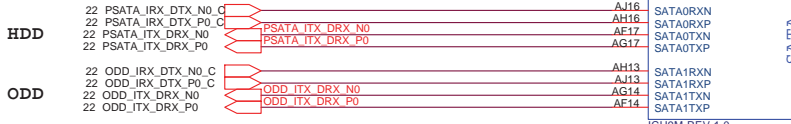


Close JOPEN1 and JOPEN2 near JMINI1



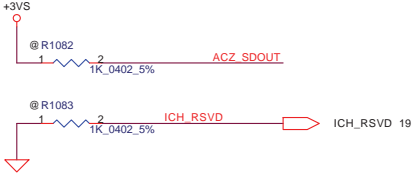
HDD

ODD



Within 500 mils

XOR CHAIN ENTRANCE STRAP:RSVD

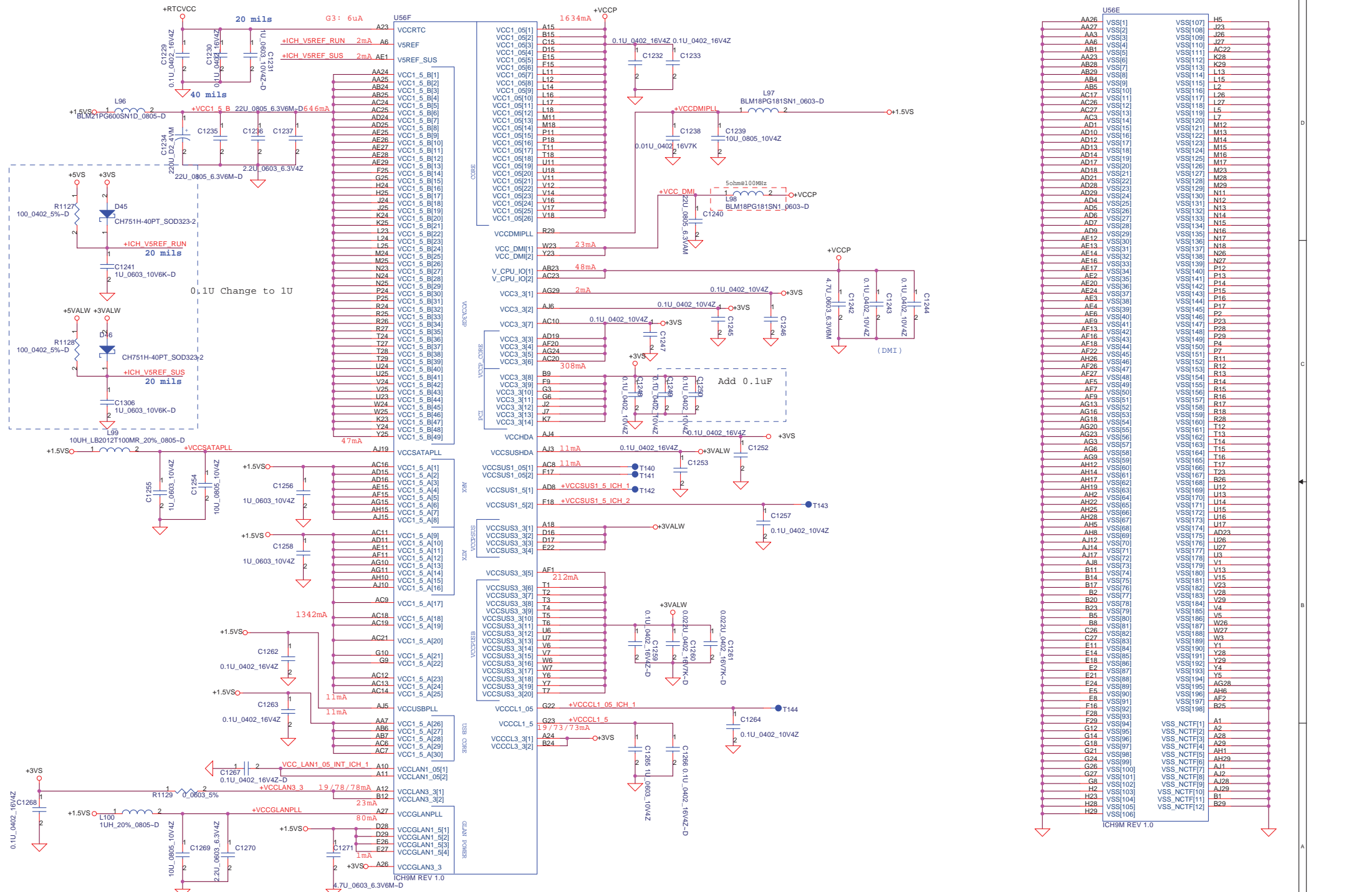


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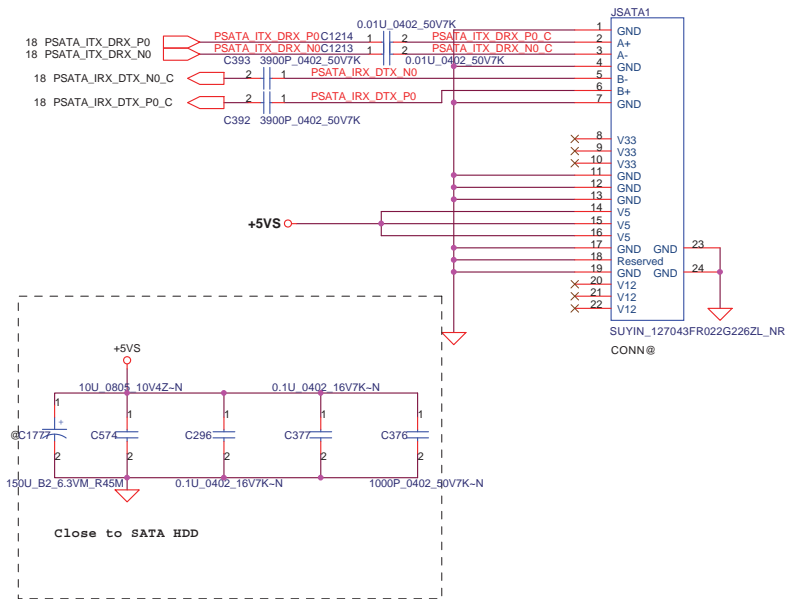
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			ICH9(2/4) LAN,HD,IDE,LPC		
Size	Document Number	Rev			
Custom	LA-4592P	0.2			
Date:	Thursday, February 19, 2009	Sheet	18	of	43

<http://laptopmotherboard.com/forums/index.php?c=6>

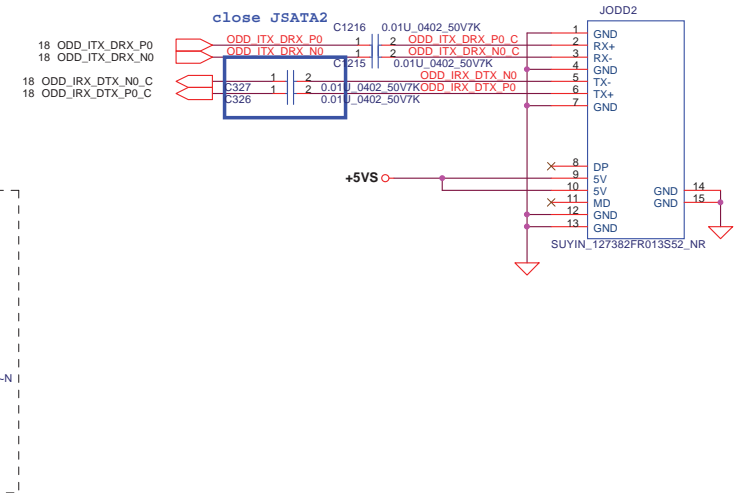


<http://laptop.mobi.com/forums/compal/ich9m.html>

SATA HDD CONN



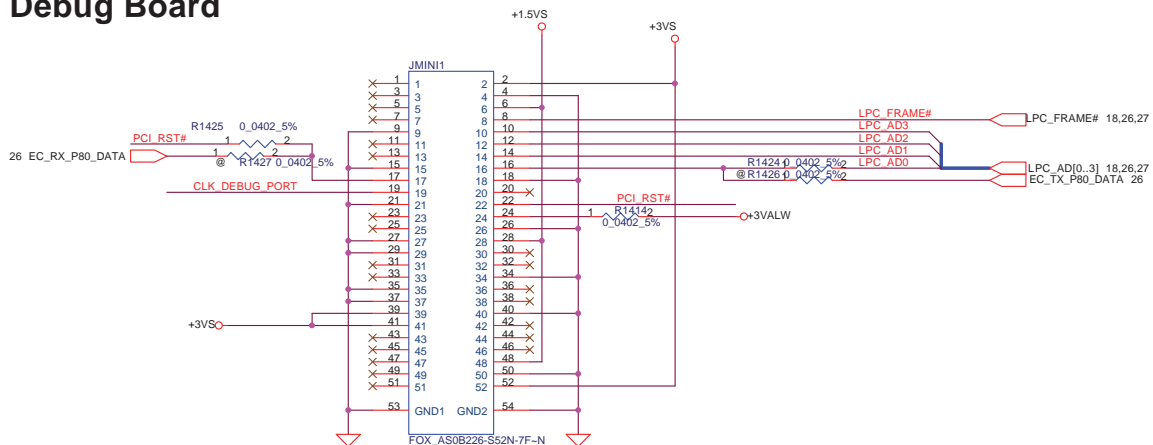
SATA ODD CONN



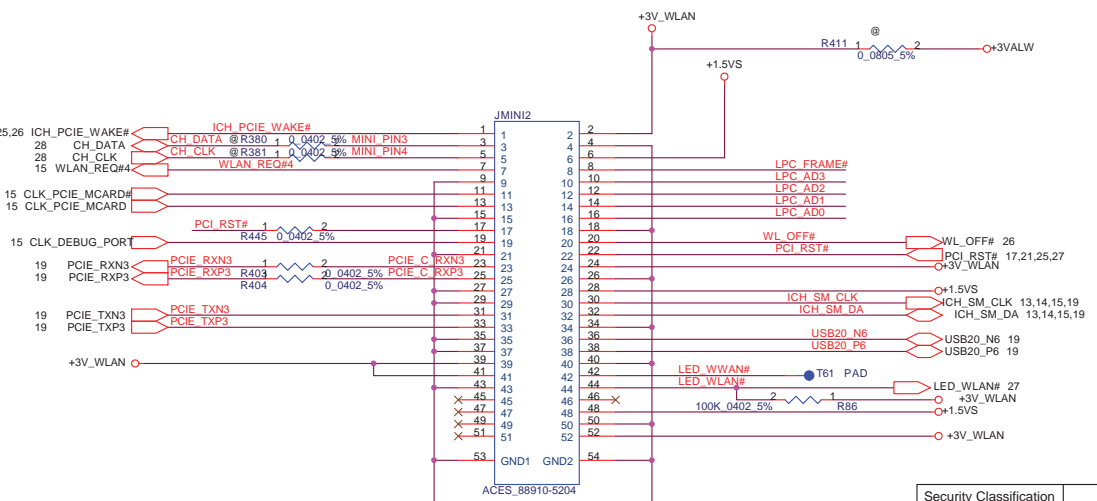
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Size	Document Number	Rev		0.2
Customer	LA-4592P			
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<http://laptop-models.com>

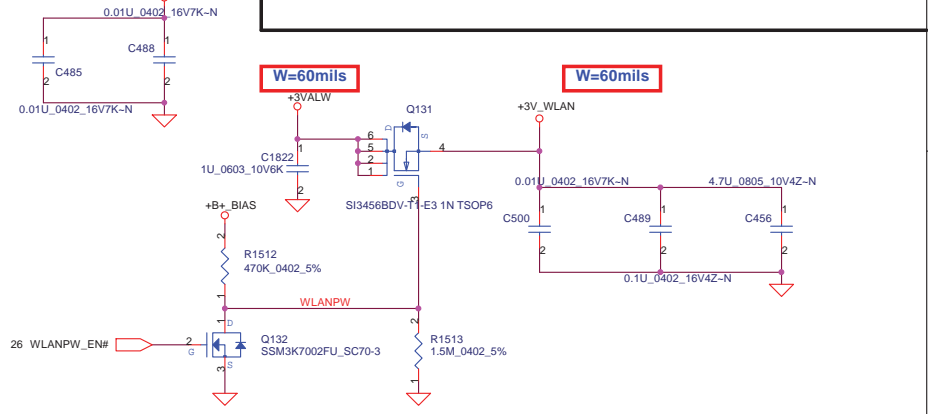
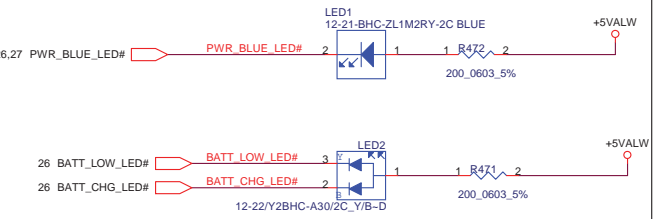
Debug Board



Mini-Express Card---WLAN



Power status (Left)



Security Classification	Compal Secret Data	
Issued Date	2007/1/15	Deciphered Date
		2008/1/15

Title **Compal Electronics, Inc.**

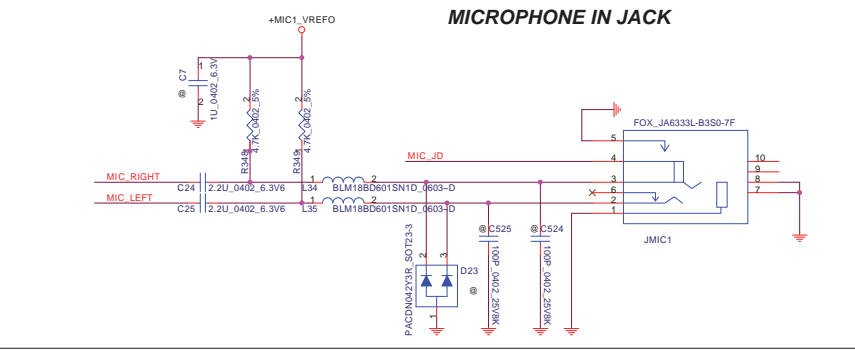
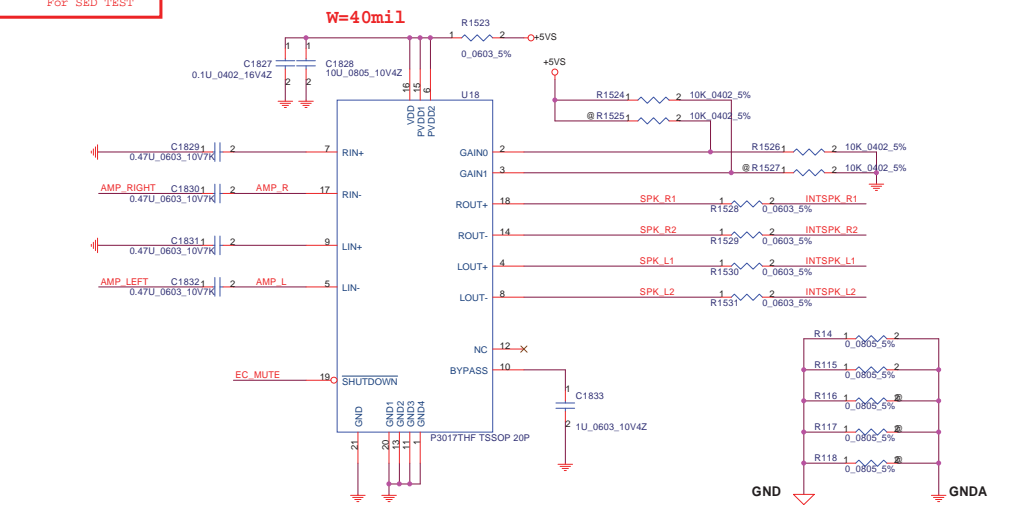
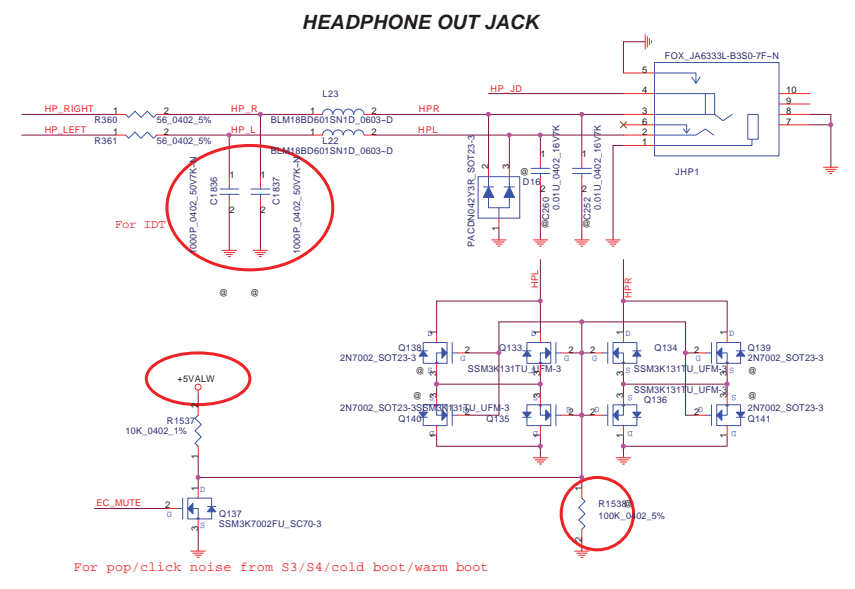
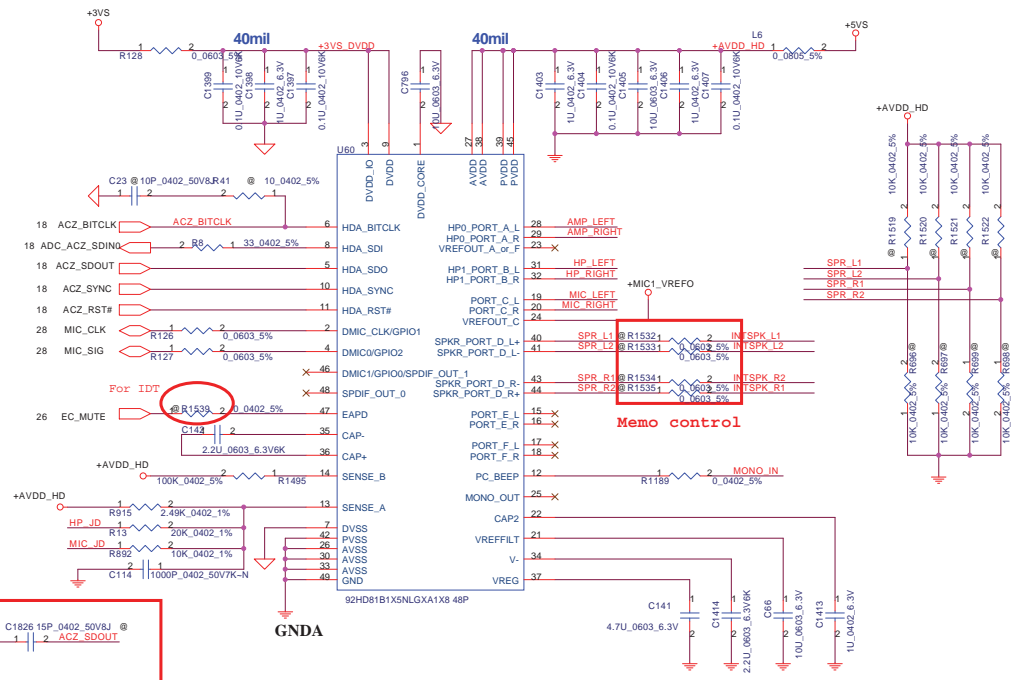
Size **Mini-Card/LED**

Customer Document Number **LA-4592P**

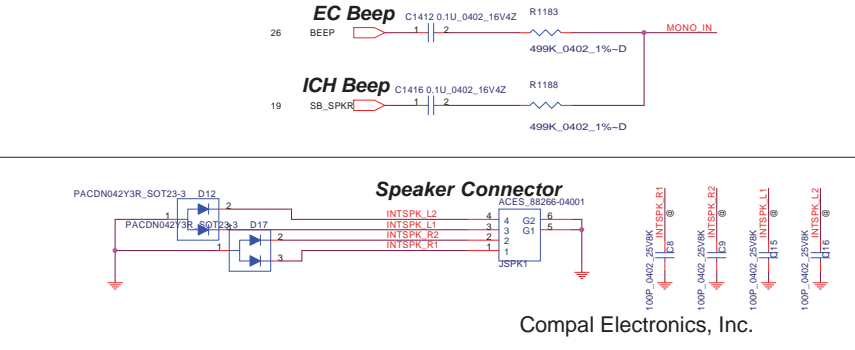
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<http://laptop motherboard schematic.blogspot.com>



GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



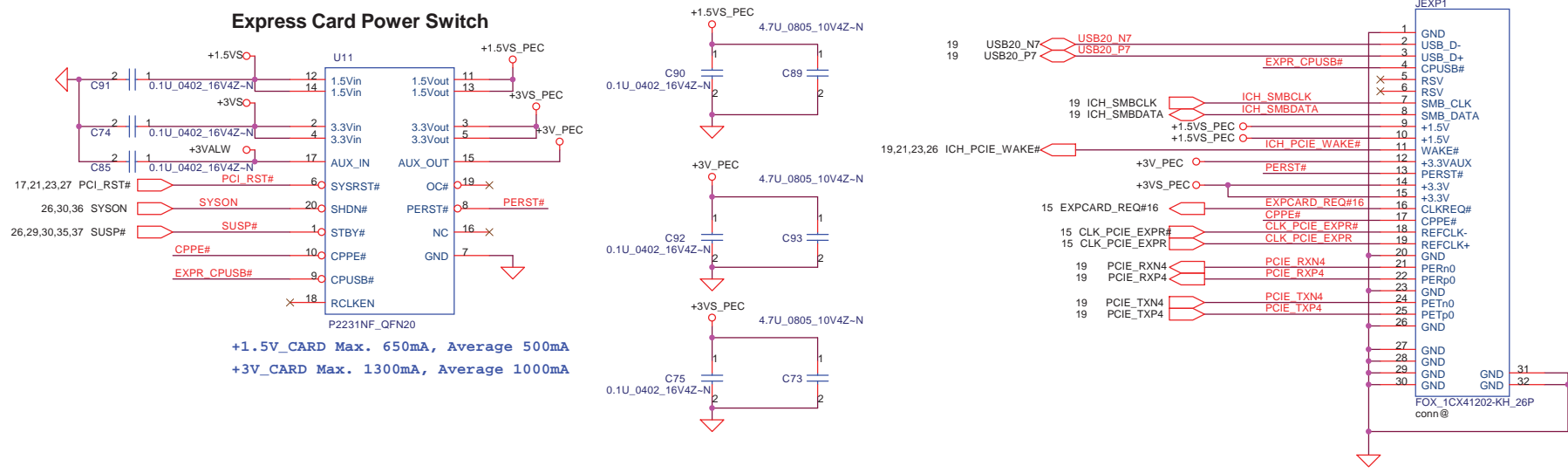
Change to 100p from 0.01u for EMI
-1012

Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off

<http://laptop-motherboard.com>

Compal Electronics, Inc.

Express card

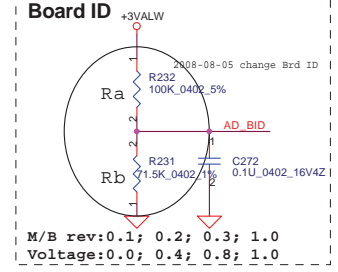
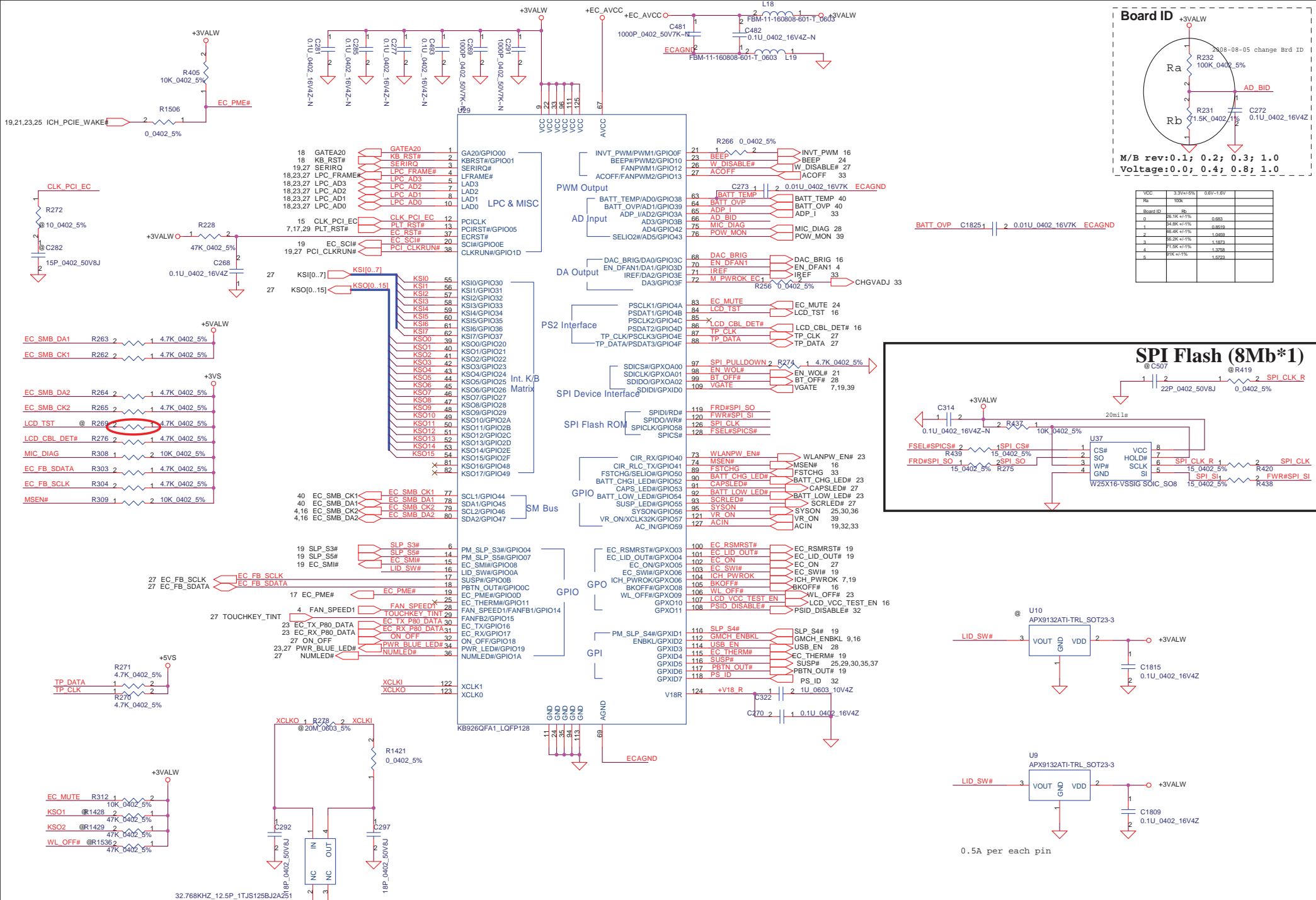


Express Card Power Switch

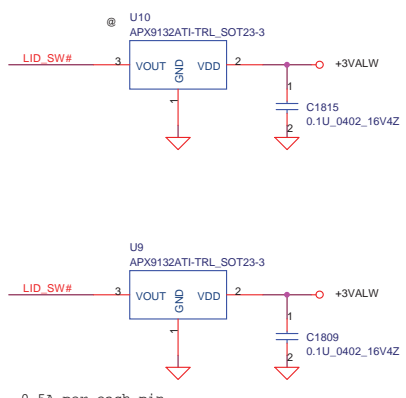
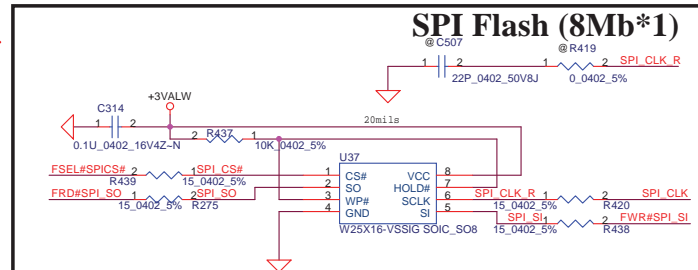
P2231NF_QFN20

+1.5V_CARD Max. 650mA, Average 500mA
 +3V_CARD Max. 1300mA, Average 1000mA

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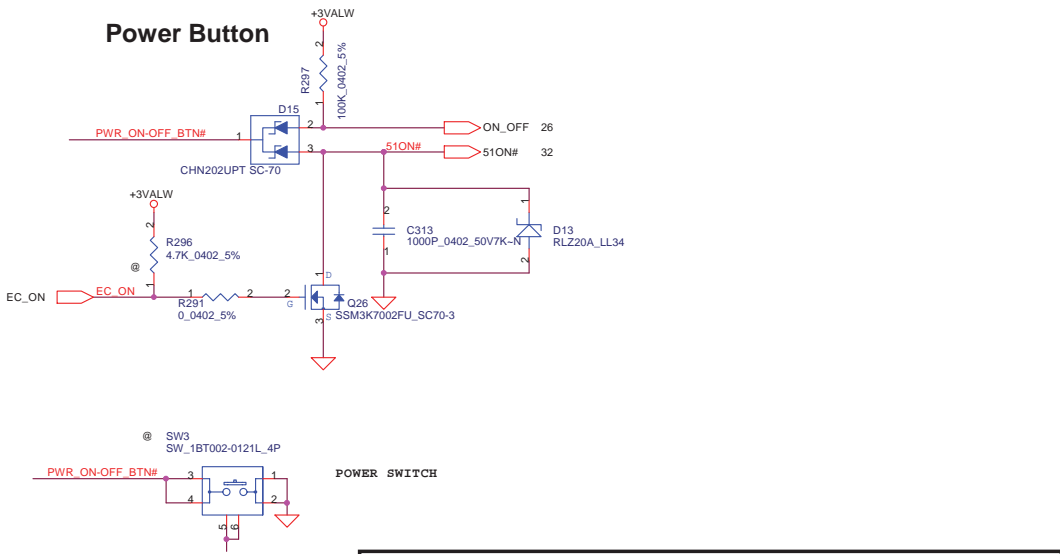
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1	0.000	0.000
2	0.000	0.000
3	0.000	0.000
4	0.000	0.000
5	0.000	0.000



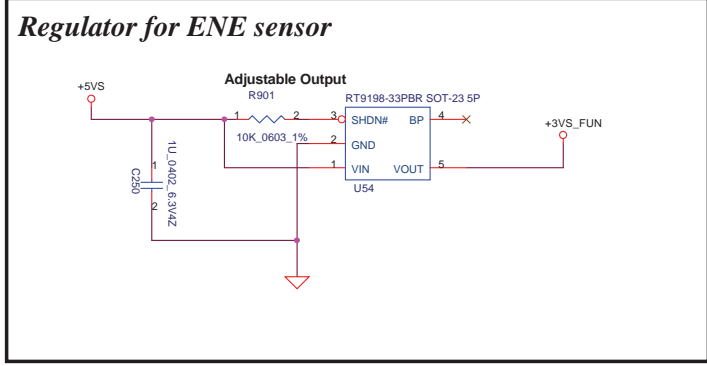
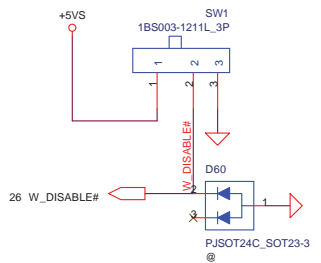
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<http://laptop-motherboard-schematic.blogspot.com/>

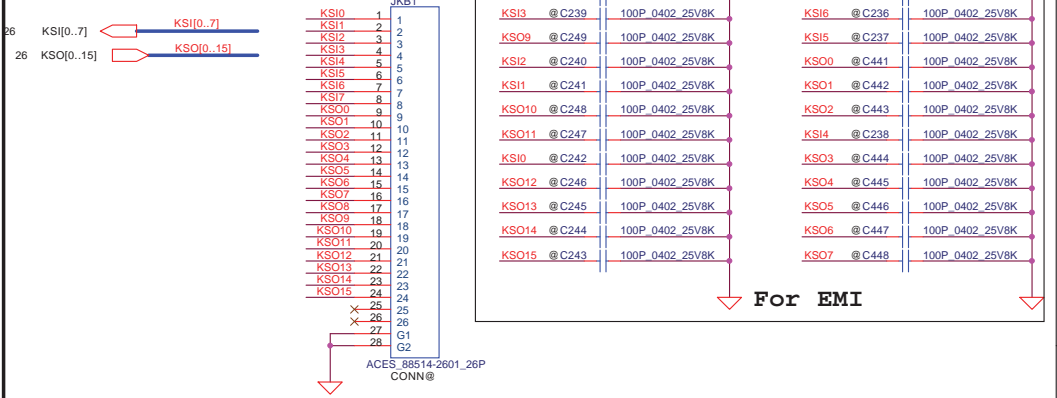
Power Button



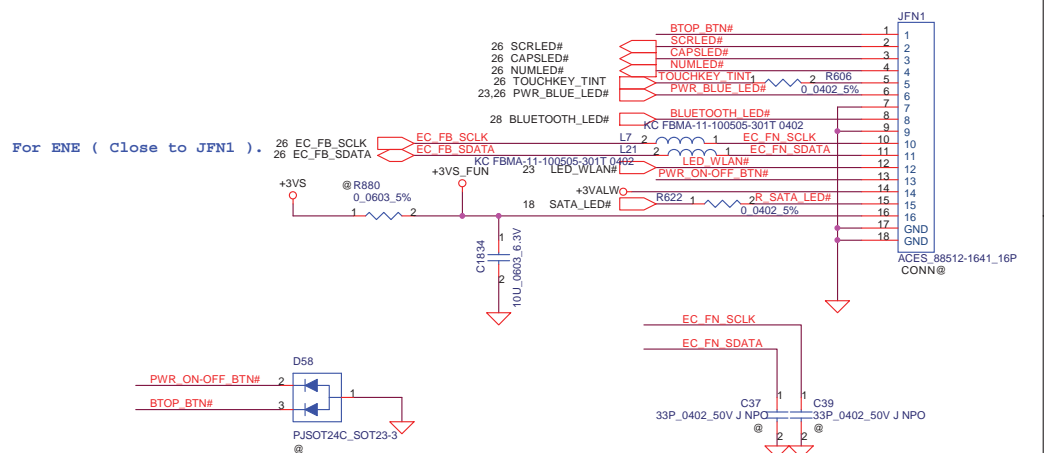
Wireless_BTN



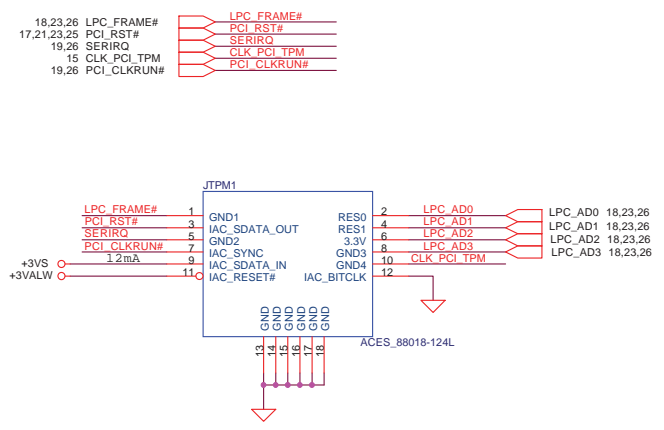
INT_KBD CONN.



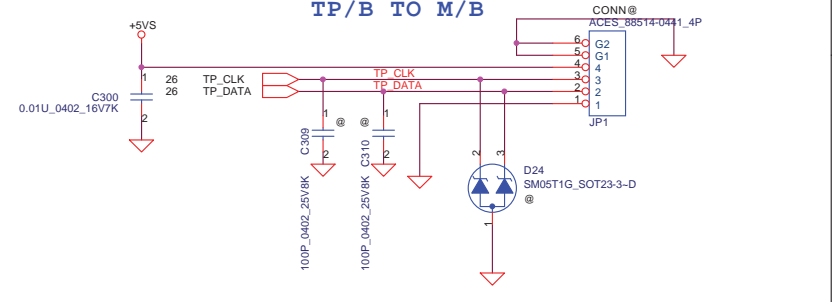
Function/B CONN.

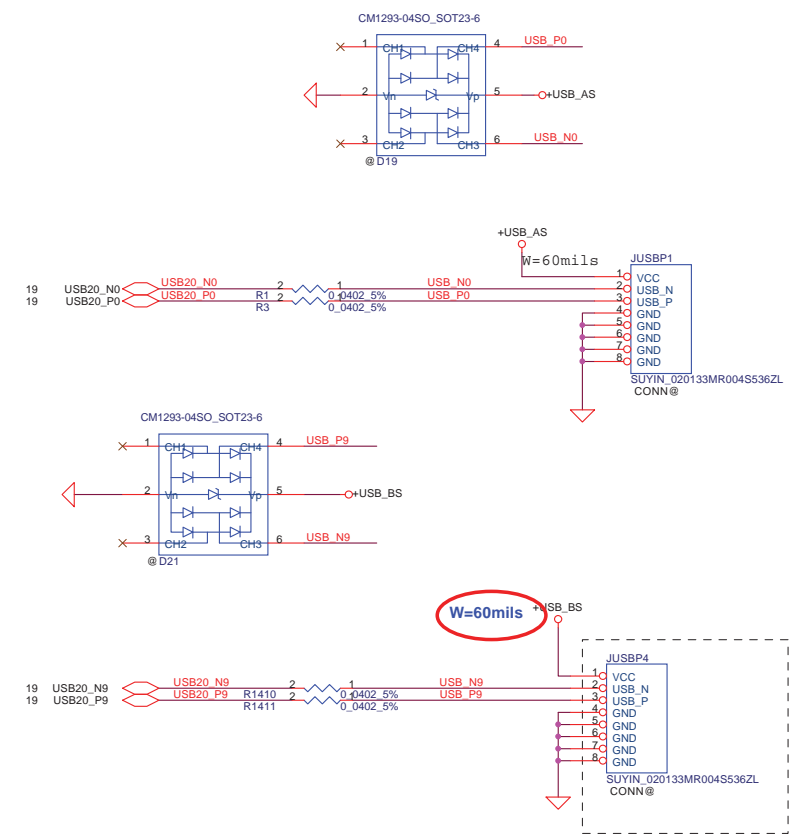
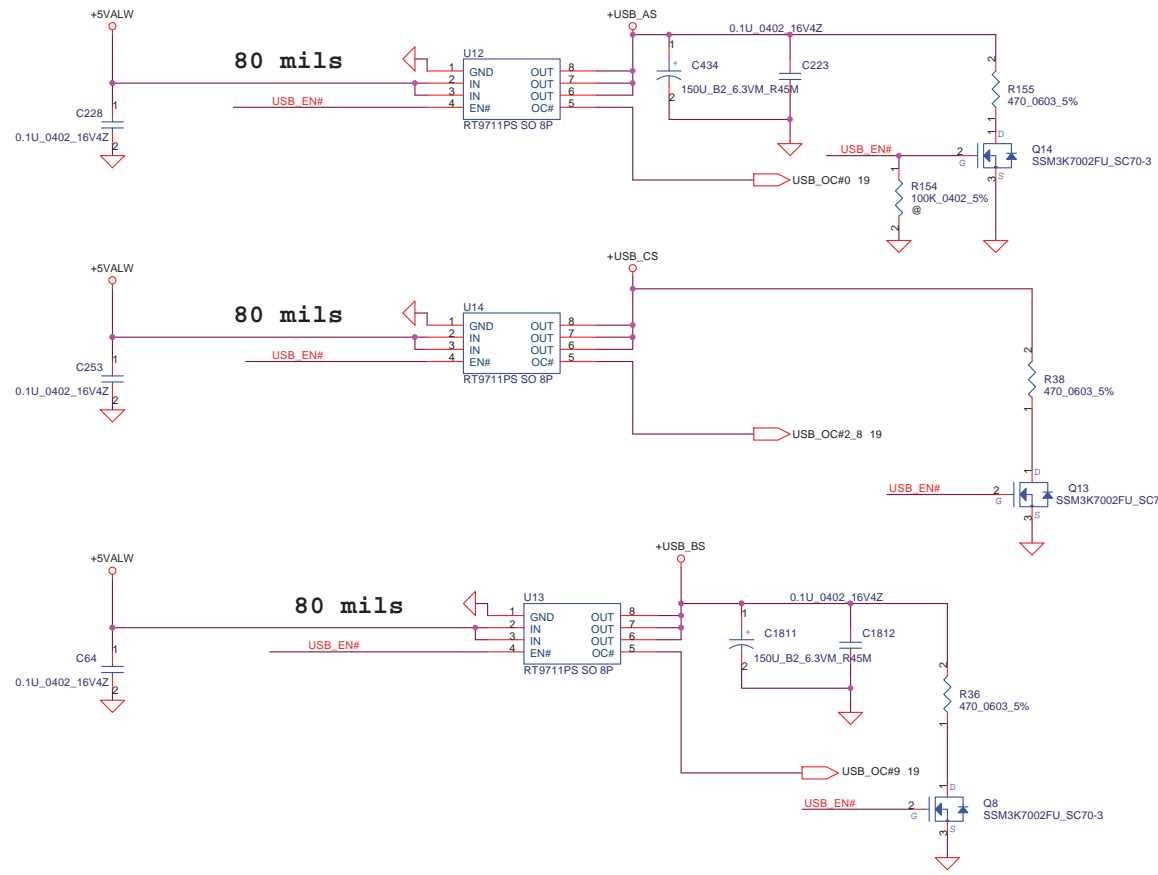


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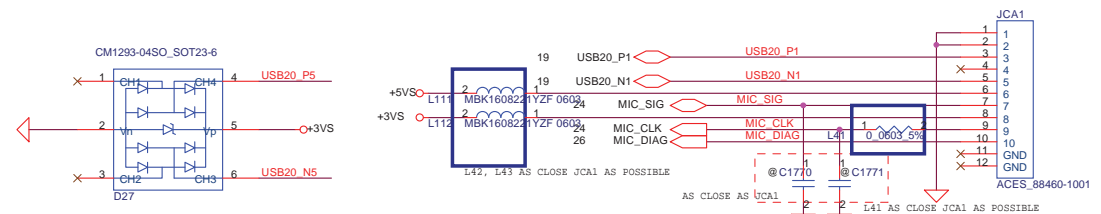


Touch PAD/B CONN.

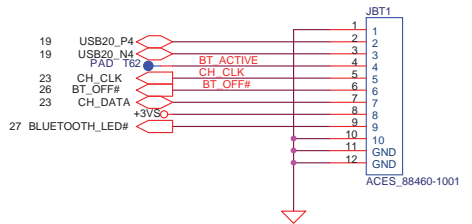




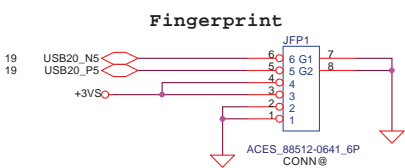
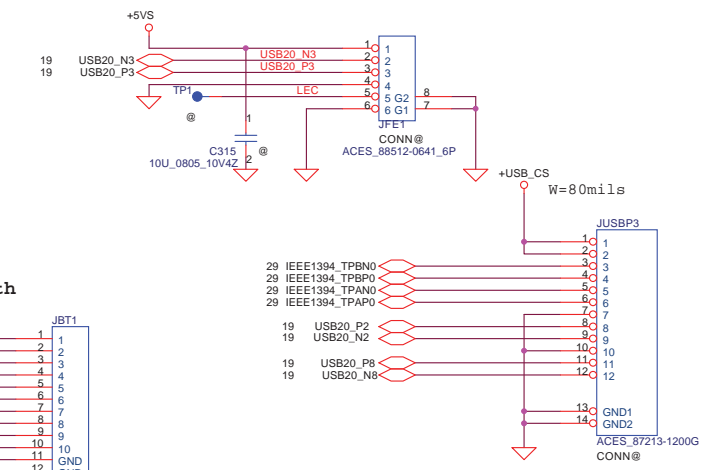
Check Module pin define Camera Conn



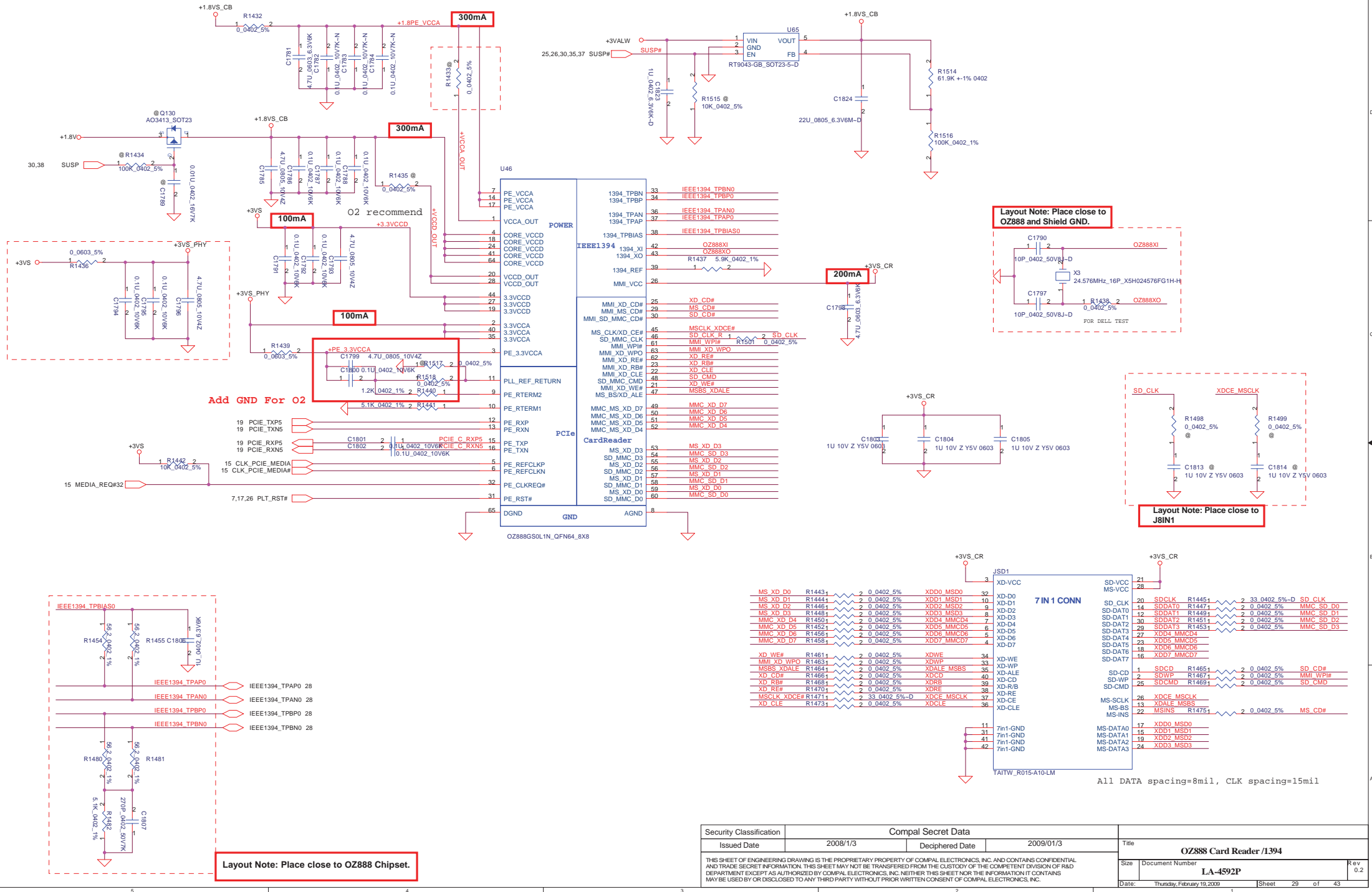
Bluetooth



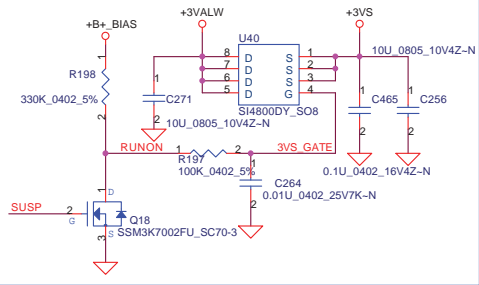
Felica Conn



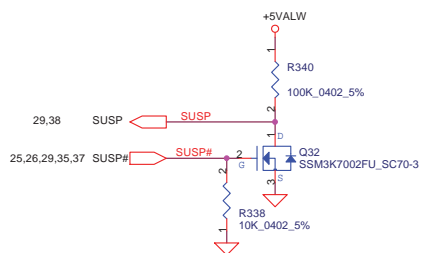
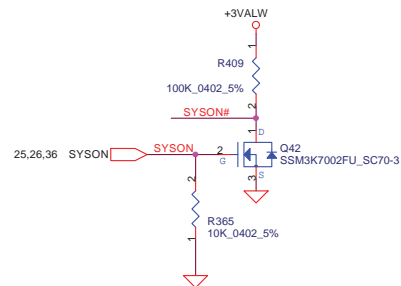
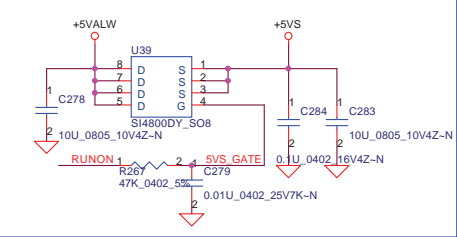
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title USB/BlueTooth/FP/Felica	
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+3VALW to +3VS Transfer

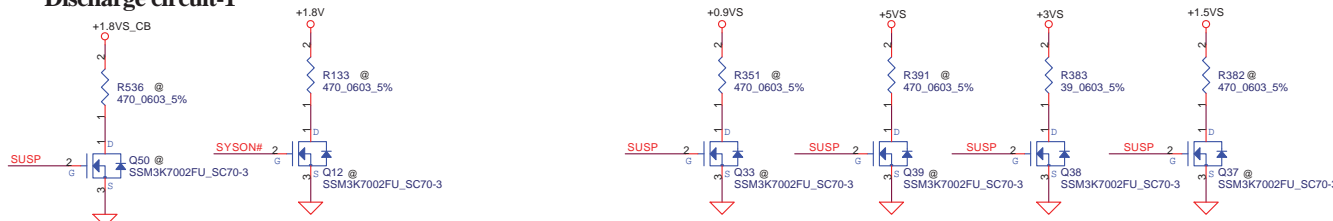


+5VALW to +5VS Transfer



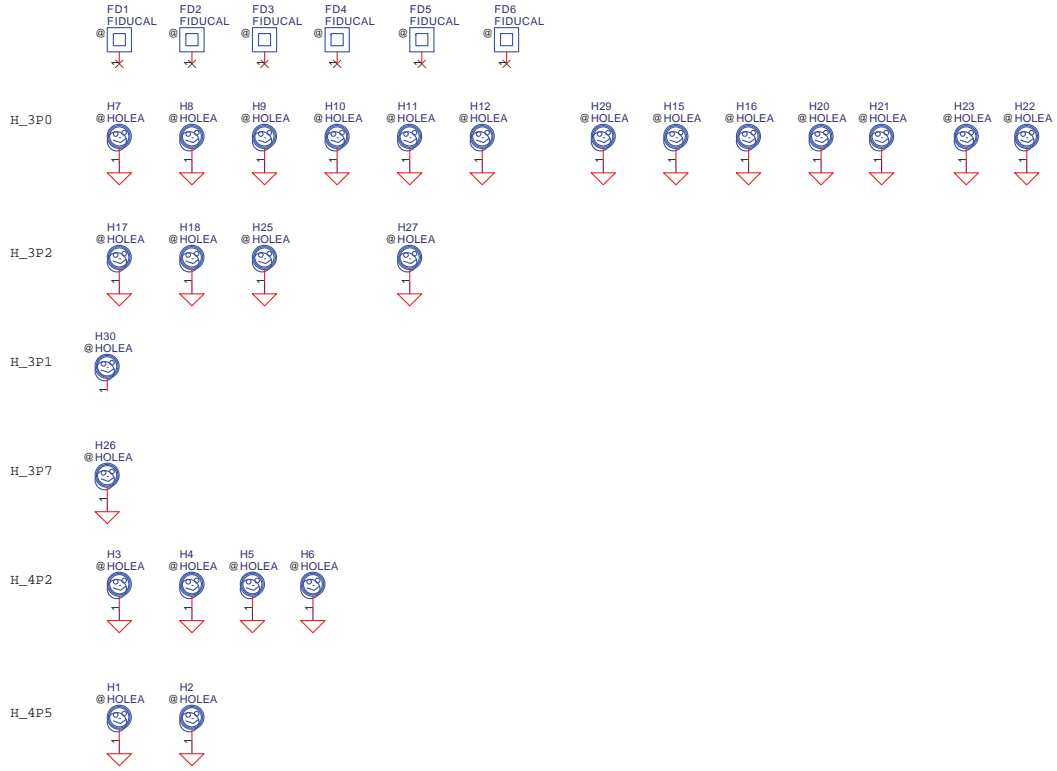
VGA Discharge circuit

Discharge circuit-1



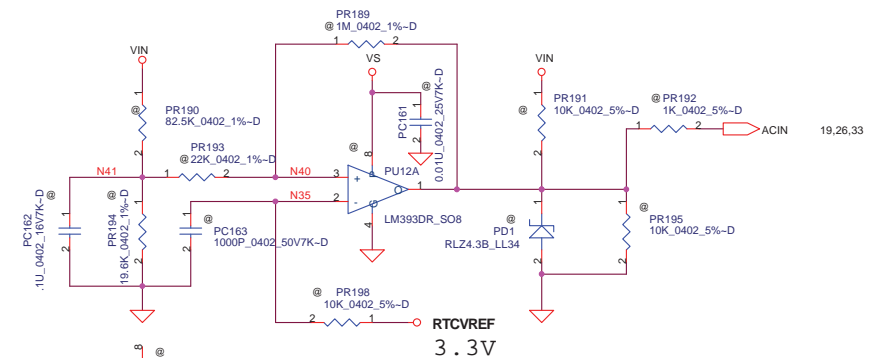
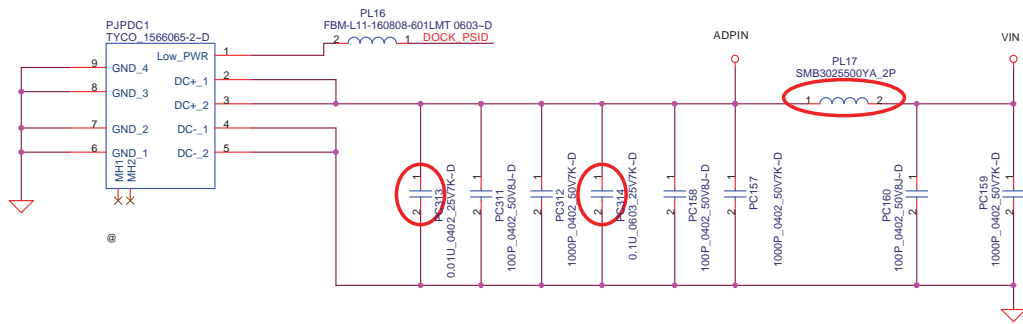
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<http://laptopmotherboard.com/html/index.php?c=6>

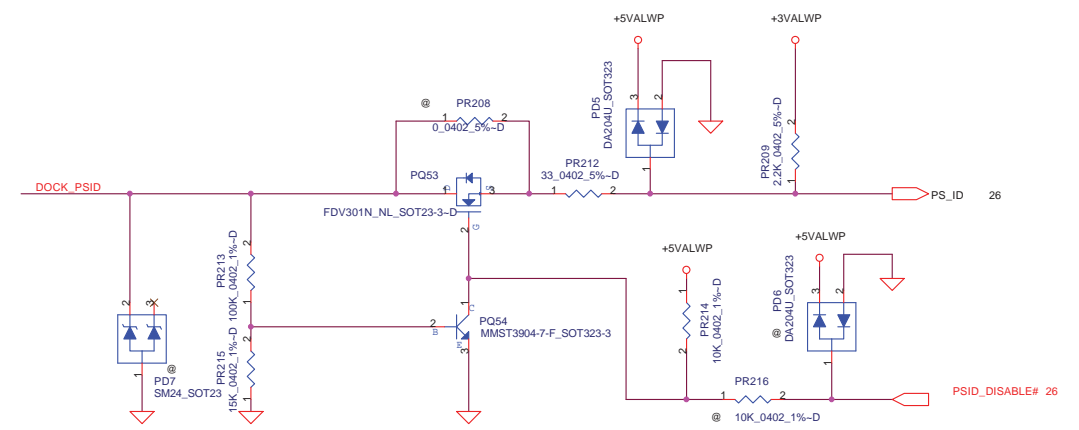
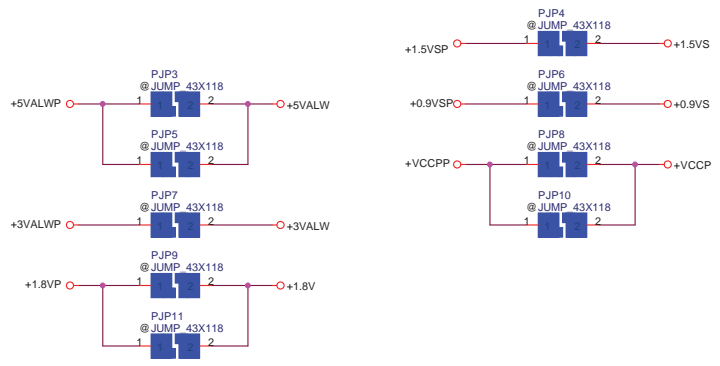
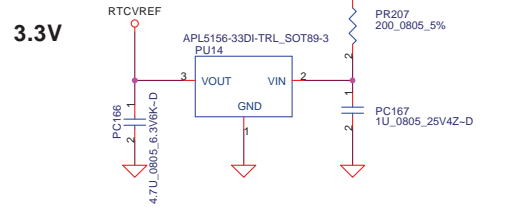
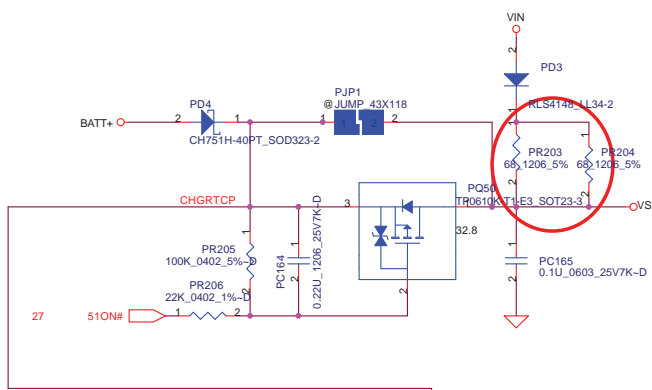


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Security Classification	Compal Secret Data		Title	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Screws
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Date: Thursday, February 19, 2009				Rev 0.2
Sheet 31 of 43				



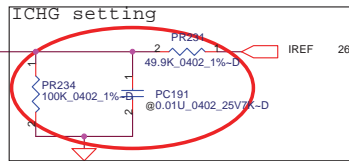
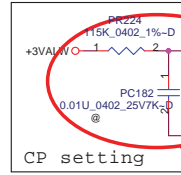
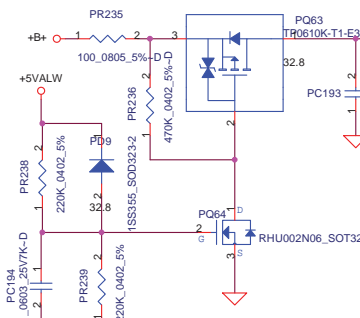
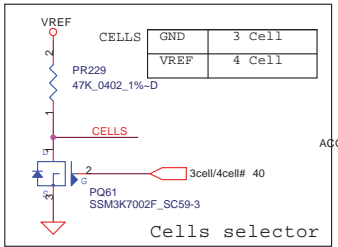
Vin Detector			
	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813



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						Customer	LA-4596P
						Date:	Thursday, February 19, 2009
						Sheet	32 of 43
						Rev	0.2

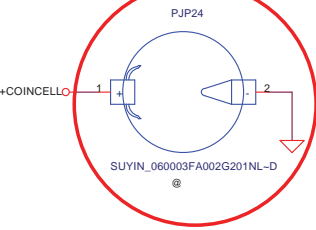
<http://laptop-models.com/compal-electronics/>

90W adapter
 $I_{charge} = (V_{rsset}/V_{vdac}) * (0.1/PR34) = 3.34A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR17) = 3.1A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



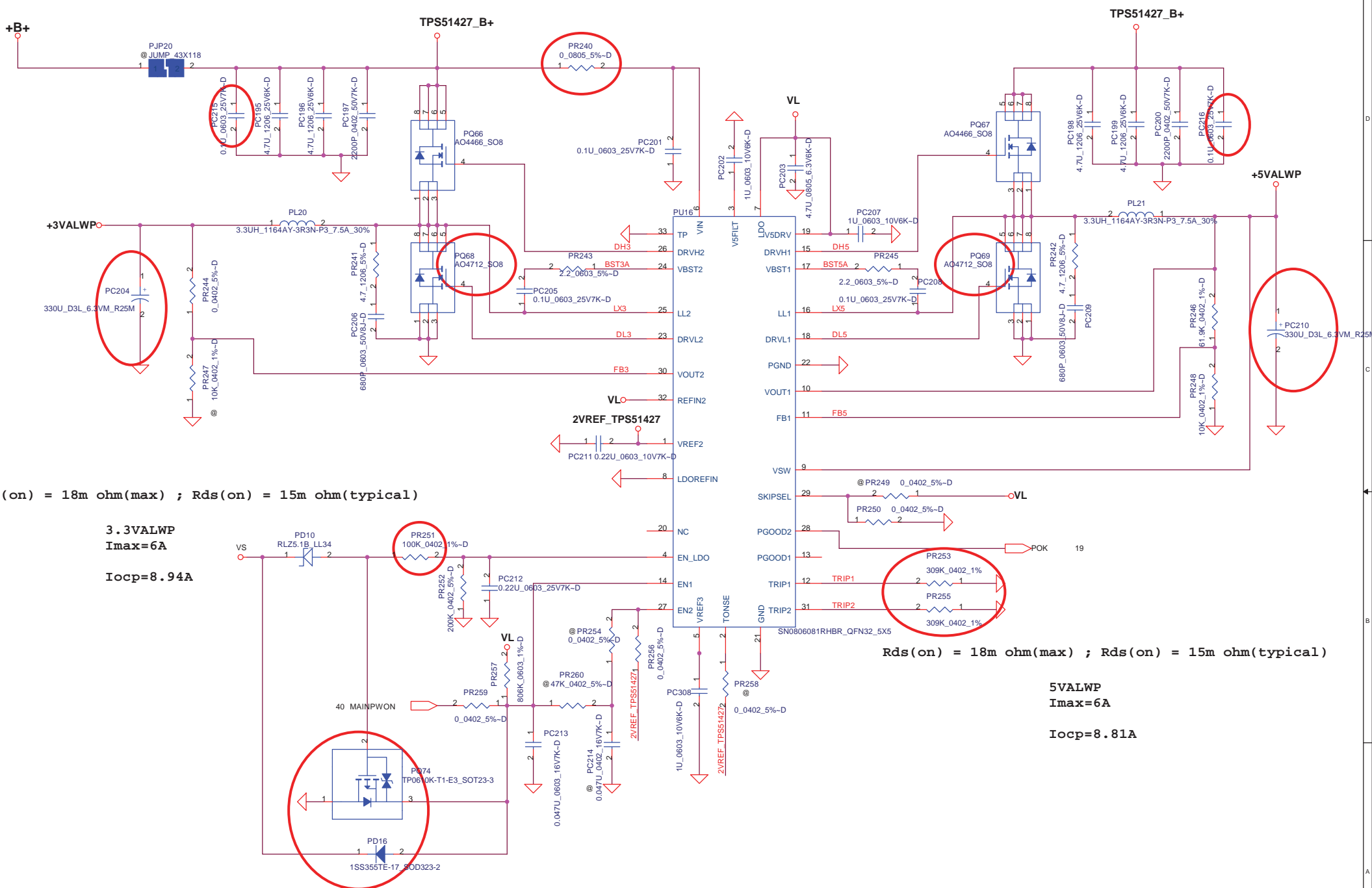
IREF	Current
2.968V	3A

COIN RTC Battery



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Issued Date	2006/10/1	Deciphered Date	2007/5/01	Title
				Charger/RTC BATTERY
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		Date: Thursday, February 19, 2009		Sheet 33 of 43

<http://laptop-motherboard.com/html/compal.html>



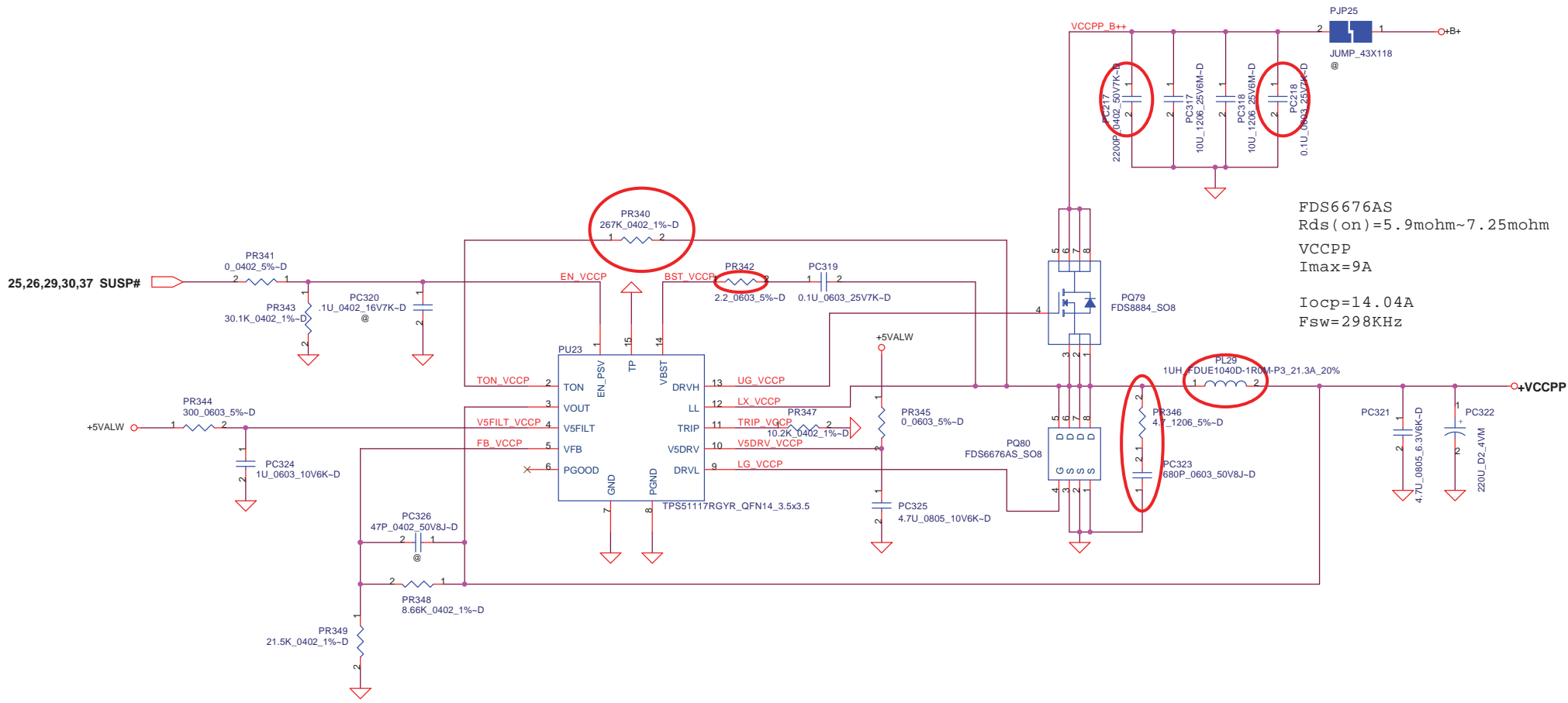
$R_{ds(on)} = 18m\ ohm(max) ; R_{ds(on)} = 15m\ ohm(typical)$

3.3VALWP
 $I_{max} = 6A$
 $I_{ocp} = 8.94A$

$R_{ds(on)} = 18m\ ohm(max) ; R_{ds(on)} = 15m\ ohm(typical)$

5VALWP
 $I_{max} = 6A$
 $I_{ocp} = 8.81A$

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Size	Custom	Document Number	LA-4596P	Rev	0.2
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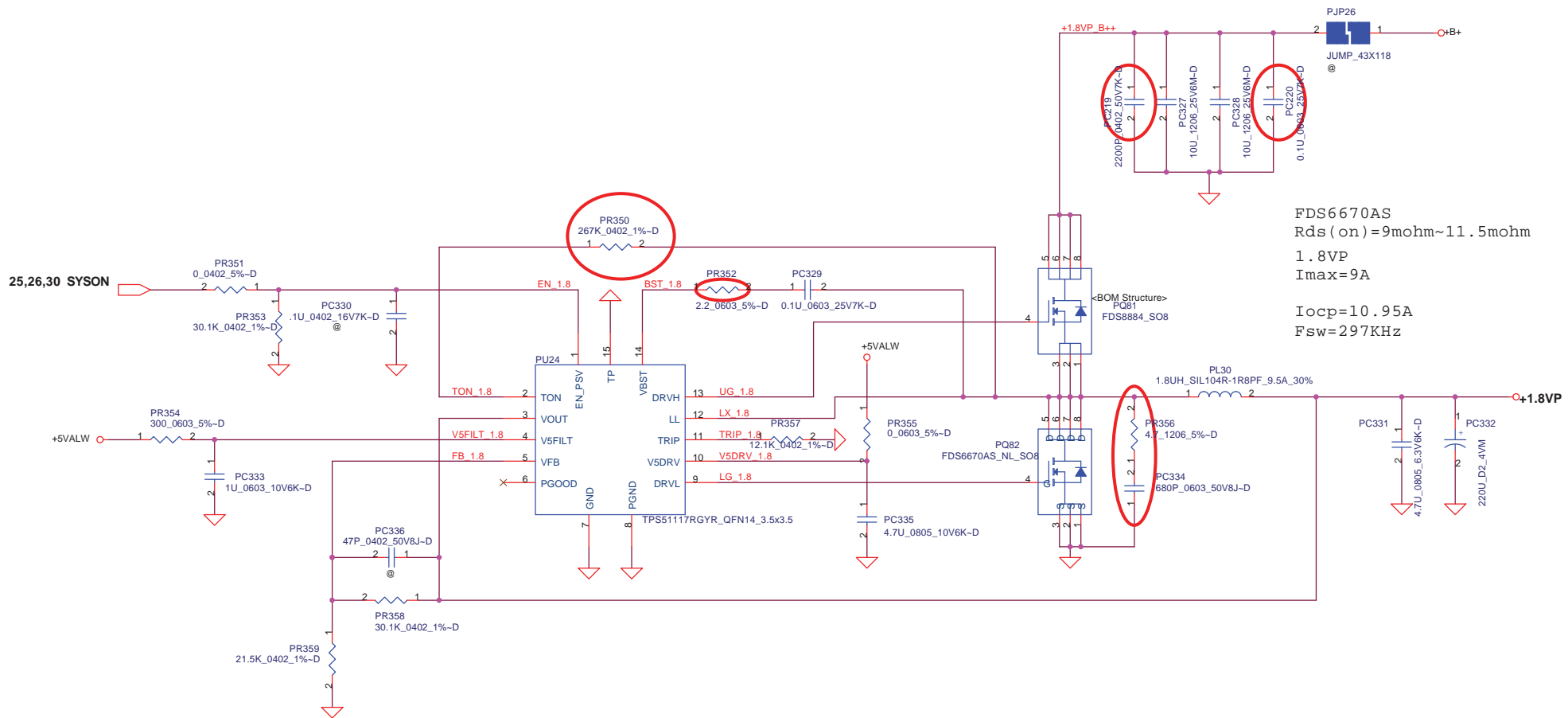


FDS6676AS
 $R_{ds(on)} = 5.9\text{mohm} \sim 7.25\text{mohm}$
VCCPP
 $I_{max} = 9\text{A}$
 $I_{ocp} = 14.04\text{A}$
 $F_{sw} = 29.8\text{KHz}$

25,26,29,30,37 SUSP#

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				Date: Thursday, February 19, 2009	

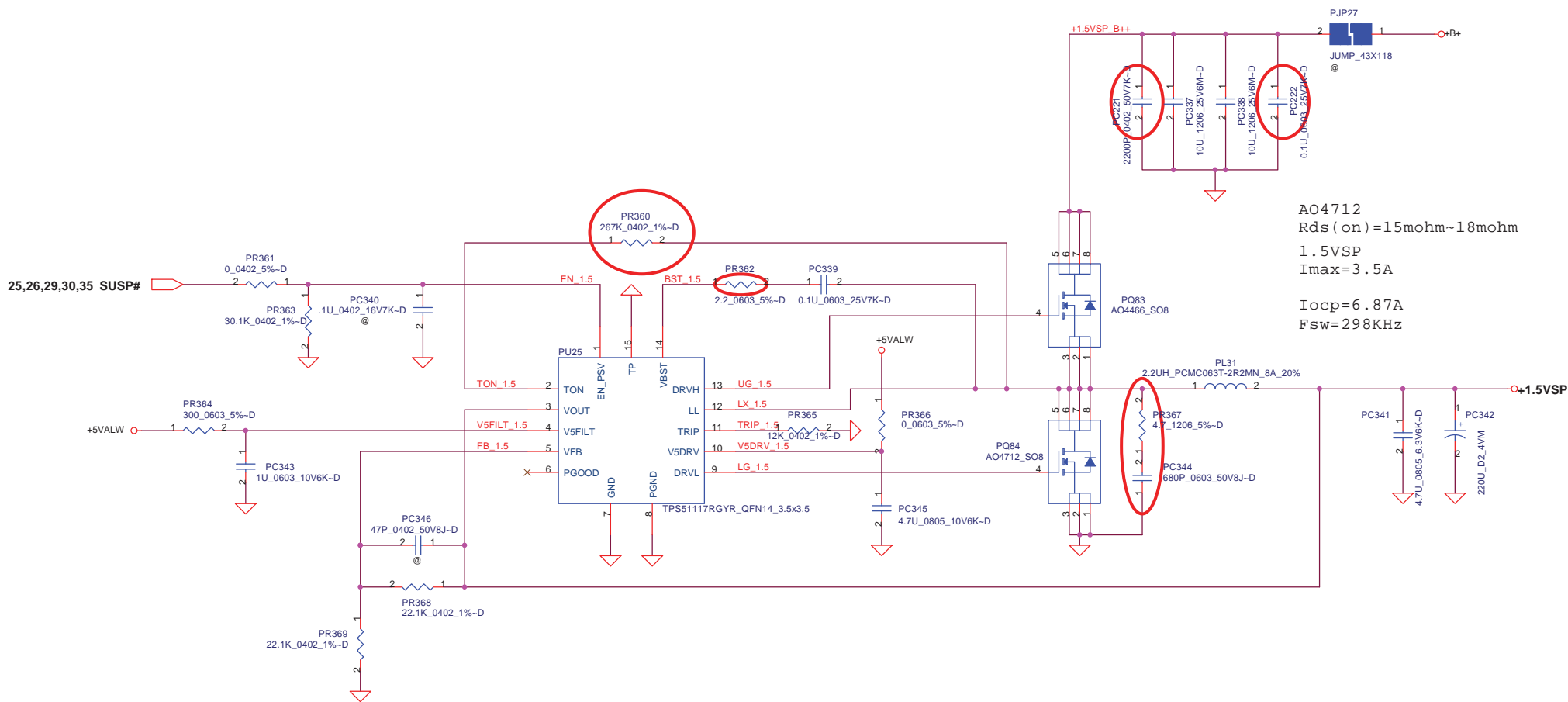
<http://rapidprotoboard.com>



FDS6670AS
 $R_{ds(on)} = 9\text{mohm} \sim 11.5\text{mohm}$
 1.8VP
 $I_{max} = 9\text{A}$
 $I_{ocp} = 10.95\text{A}$
 $f_{sw} = 297\text{KHz}$

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	LA-4596P			0.2	
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<http://laptop-motherboardschematic.blogspot.com>

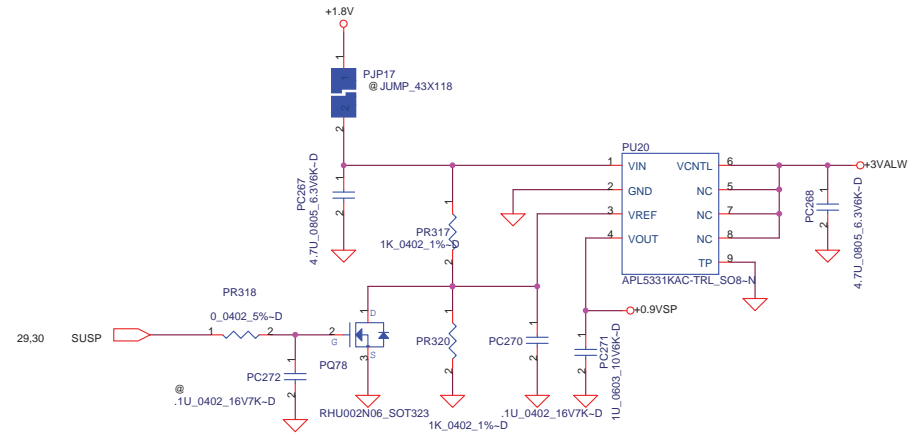


AO4712
 $R_{ds(on)} = 15\text{mohm} \sim 18\text{mohm}$
 1.5VSP
 $I_{max} = 3.5\text{A}$
 $I_{ocp} = 6.87\text{A}$
 $F_{sw} = 298\text{KHz}$

25,26,29,30,35 SUSP#

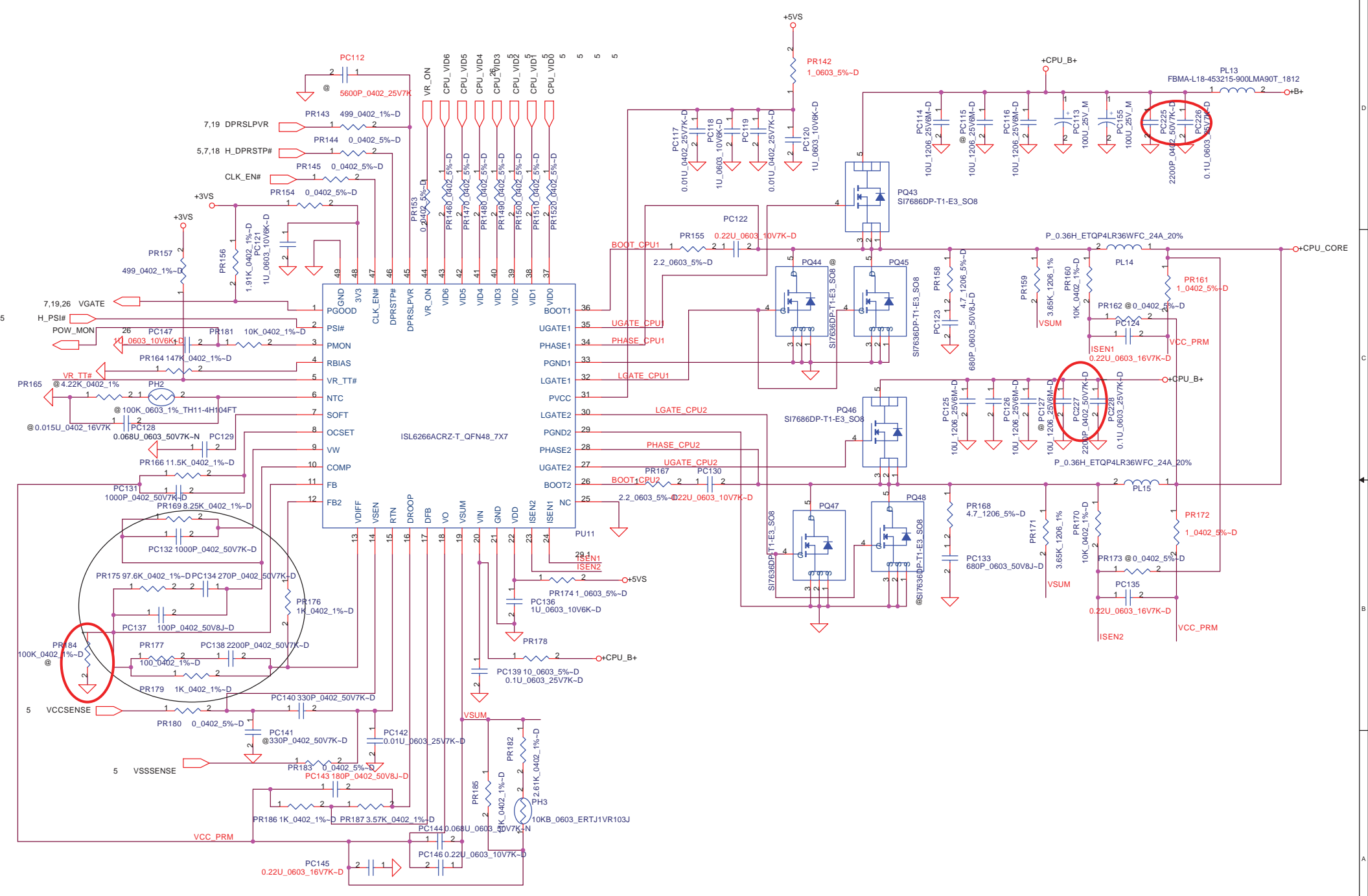
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Size	Document Number			Rev	
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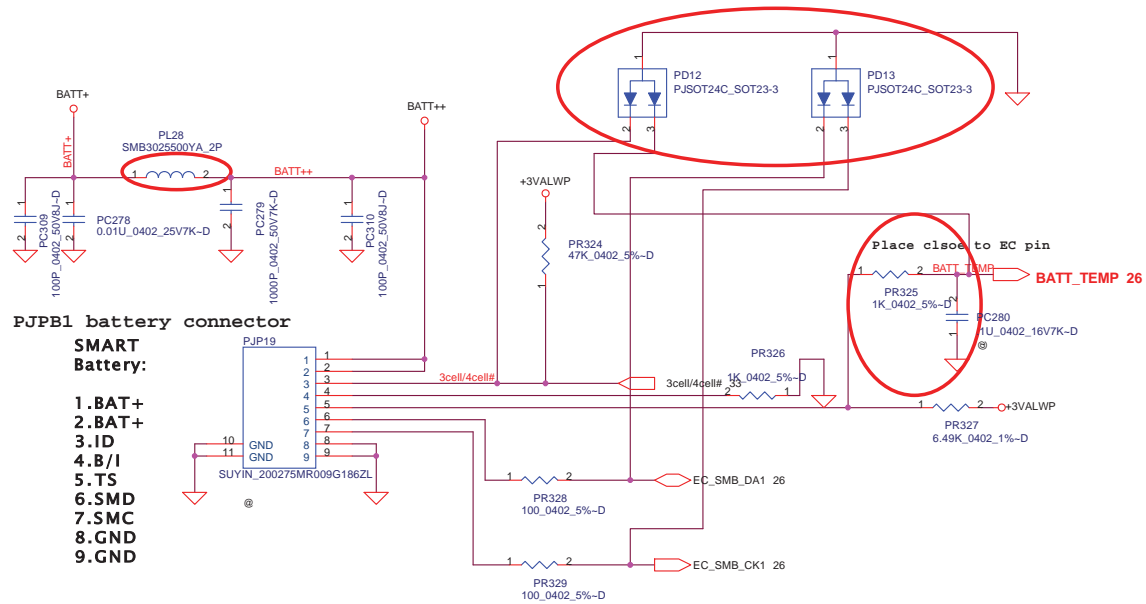


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			Size	Document Number
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<http://laptop-motherboards.com/forums/showthread.php?p=6006>

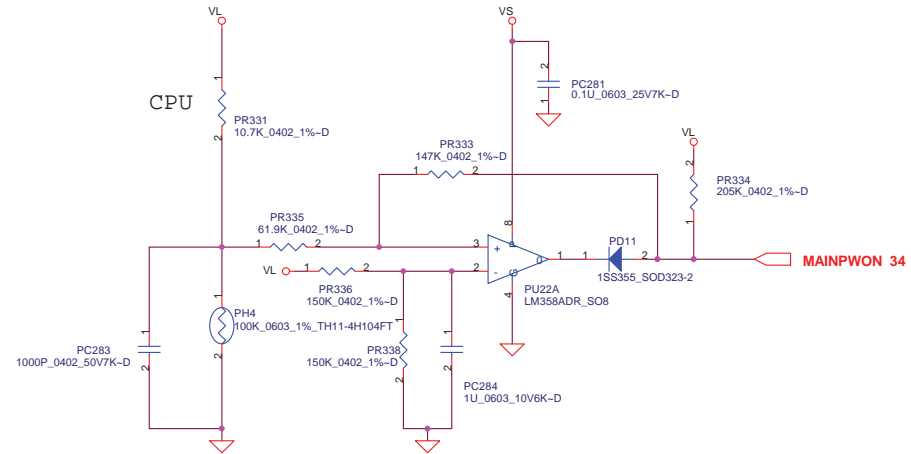
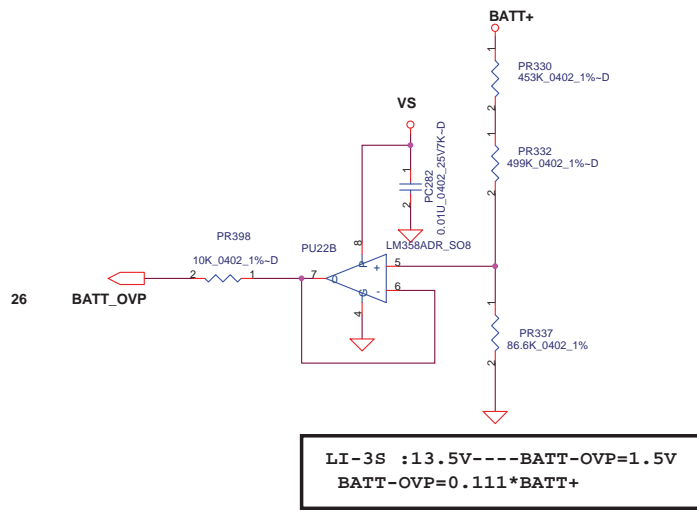


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http://astp.micromerboardschematics.blogspot.com				Custom	LA-4596P
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Battery Connect/OTP

CPU
PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C



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				BATTERY CONN
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	32	DCIN /Vin Detector	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
2			08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
3	33	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
4	40	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
5	32	DCIN /Vin Detector	08/12/12	COMPAL	increase capacitor for EMI request	add PC313 at 0.01uf and PC314 at 0.1uf	0.3
6	35	VCCPP	08/12/12	COMPAL	change resister for EMI request	change PR342 from 0 to 2.2	0.3
7	36	1.8VP	08/12/12	COMPAL	change resister for EMI request	change PR352 from 0 to 2.2	0.3
8	37	1.5VSP	08/12/12	COMPAL	change resister for EMI request	change PR362 from 0 to 2.2	0.3
9	35	VCCPP	08/12/18	COMPAL	add resister and capacitor for EMI request	add PR346 at 4.7and pc323 at 680p	0.3
10	36	1.8VP	08/12/18	COMPAL	add resister and capacitor for EMI request	add PR356 at 4.7and pc334 at 680p	0.3
11	37	1.5VSP	08/12/18	COMPAL	add resister and capacitor for EMI request	add PR367 at 4.7and pc344 at 680p	0.3
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<http://laptop-motherboard.com/html/compal.html>

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	28	USB/BT/ FP/ Felica/Camera	2008/12/02	Compal_HW	Small USB board no function	Modify Pin definition of JUSBP3	0.2
2	24	HDA-IDT_92HD81	2008/12/02	Compal_HW	R voice and L voice fail	Modify Pin definition of JSPK1	0.2
3	27	PWR_OK/ BTN/ KB / TP/TPM1.2	2008/12/02	Compal_HW	Switch function fail	Modify Pin definition of SW1	0.2
4	21	LAN-8111D	2008/12/16	Compal_HW	EMI LAN test fail	Add C1817-C1820 for LAN connector	0.2
5	23	Mini-Card/WWAN/Roboson	2008/12/16	Compal_HW	S5 wake on Wirlesslan fail	Add U89 to control wireless lan voltage	0.2
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<http://laptop motherboard schematic diagram.com>

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				0.2	
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