Confidential

Schematics
Document

Mobile AMD Athlon XP with ATI MOBILITY-U1 /ALI 1535+ core logic chip

2002-08-12

REV: 0.5

Compal Electronics, Inc.		
Title: COVER SHEET		
Size	Document Number: LA-1481 M/B	Rev: 0.5
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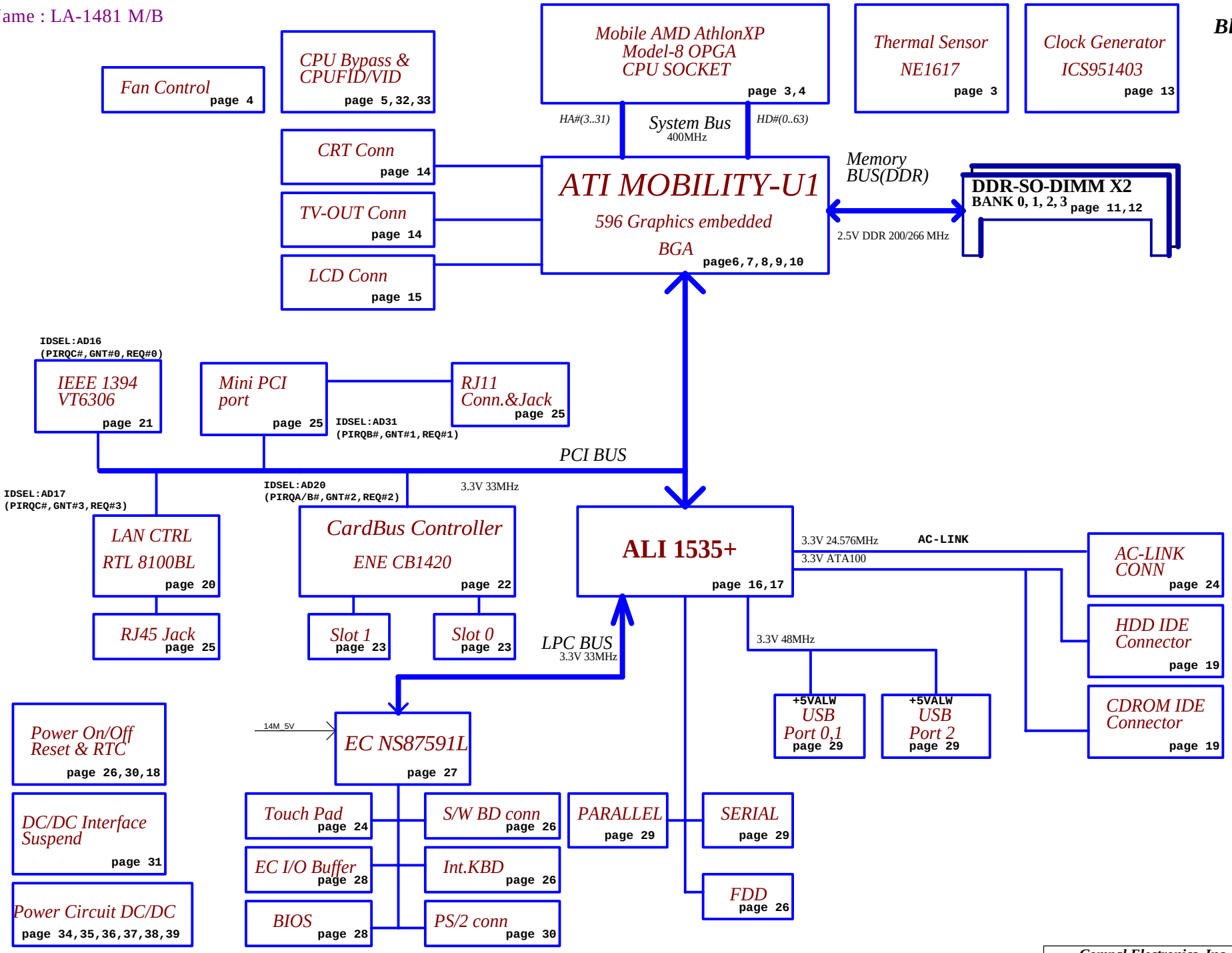
File Name : LA-1481 M/B

Block Diagram



Compal Electronics, Inc.		
Title: Block Diagram		
Size	Document Number: LA-1481 M/B	Rev: 0.3
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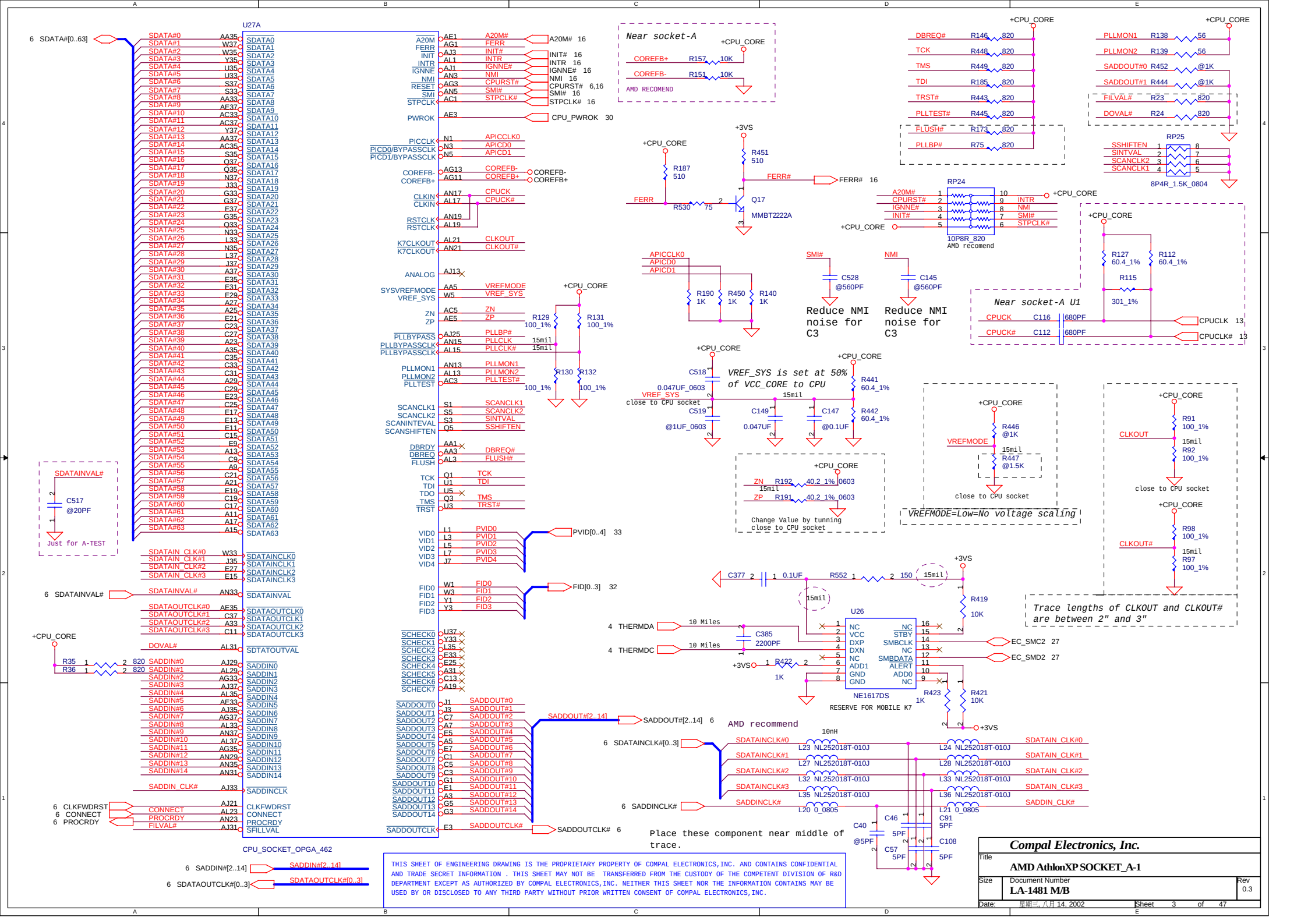

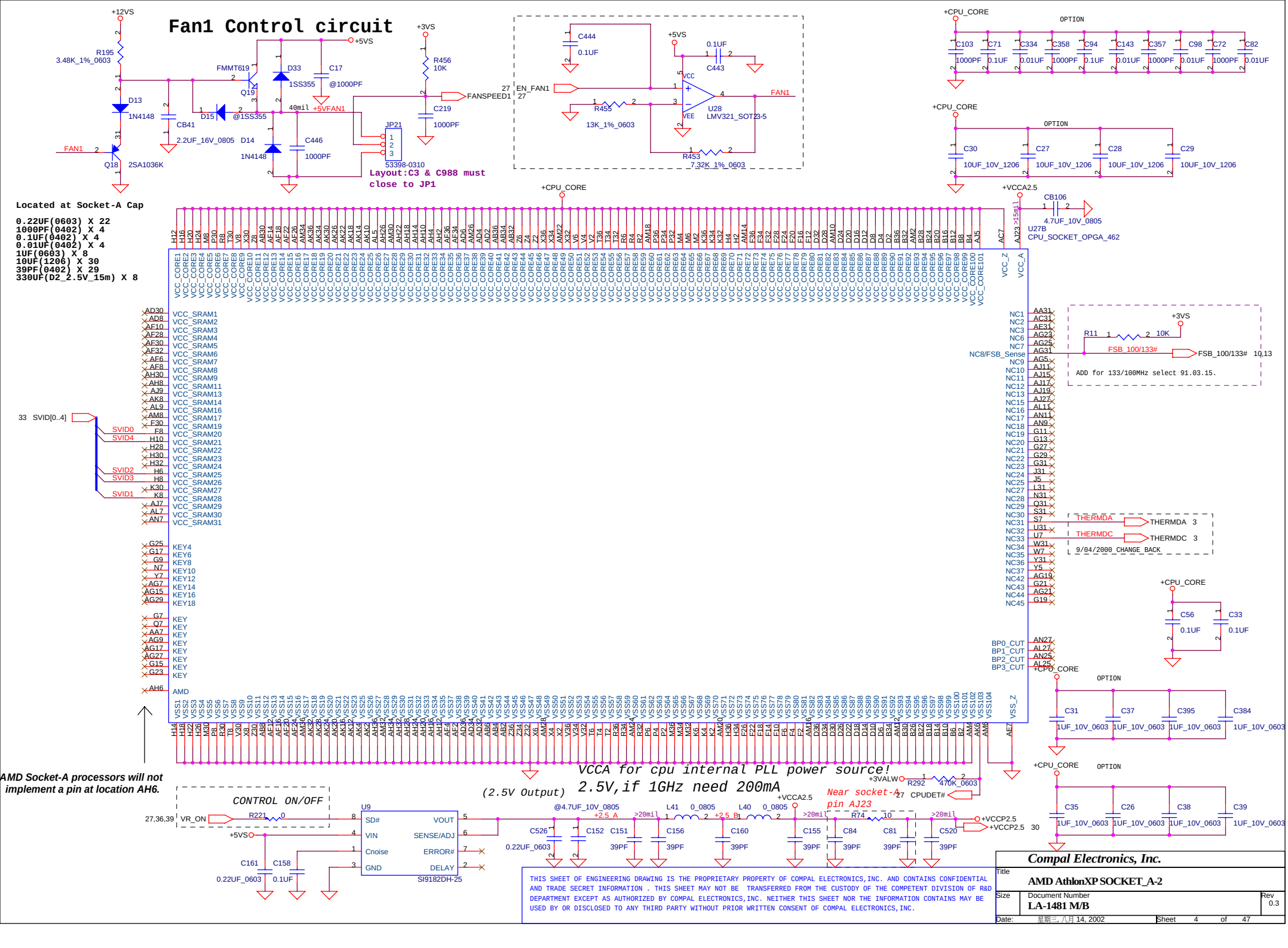
Fan1 Control circuit
Layout:C3 & C988 must close to JP1
Located at Socket-A Cap
0.22UF(0603) X 22
1000PF(0402) X 4
0.1UF(0402) X 4
0.01UF(0402) X 4
1UF(0603) X 8
10UF(1206) X 30
39PF(0402) X 29
330UF(D2_2.5V_15m) X 8
AMD Socket-A processors will not implement a pin at location AH6.
CONTROL ON/OFF
VCCA for cpu internal PLL power source!
2.5V,if 1GHz need 200mA
(2.5V Output)
Near socket-A pin AJ23
ADD for 133/100MHz select 91.03.15.
9/04/2000 CHANGE_BACK
Compal Electronics, Inc.
AMD AthlonXP SOCKET_A-2
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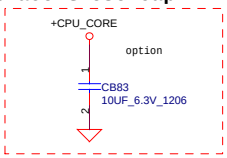
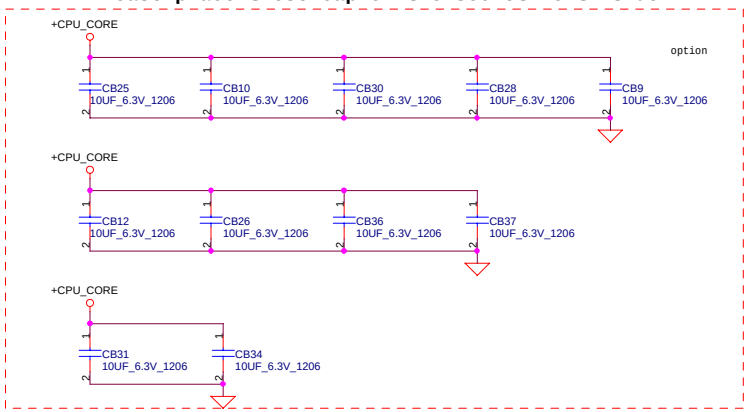
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

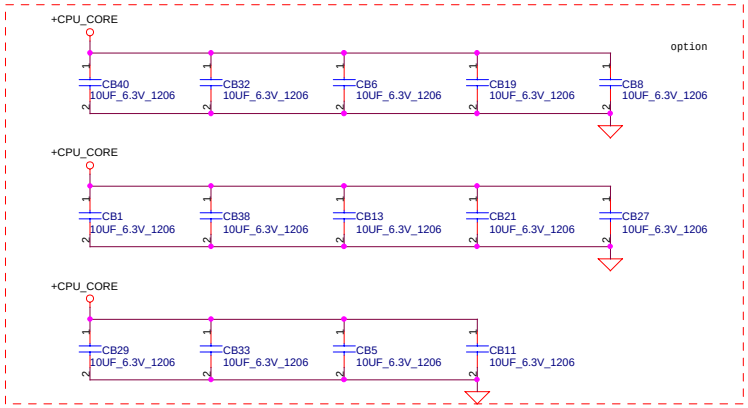
Please place these cap in the socket cavity area



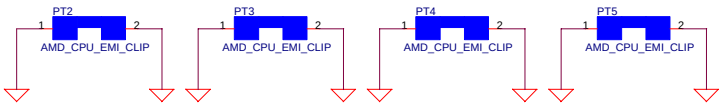
Please place these cap on the socket north side



Please place these cap on the socket south side



EMI Clip HOLE for CPU



Layout note :

Place close to CPU power and ground pin as possible (<1inch)

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Title: **CPU Bypass Cap.**

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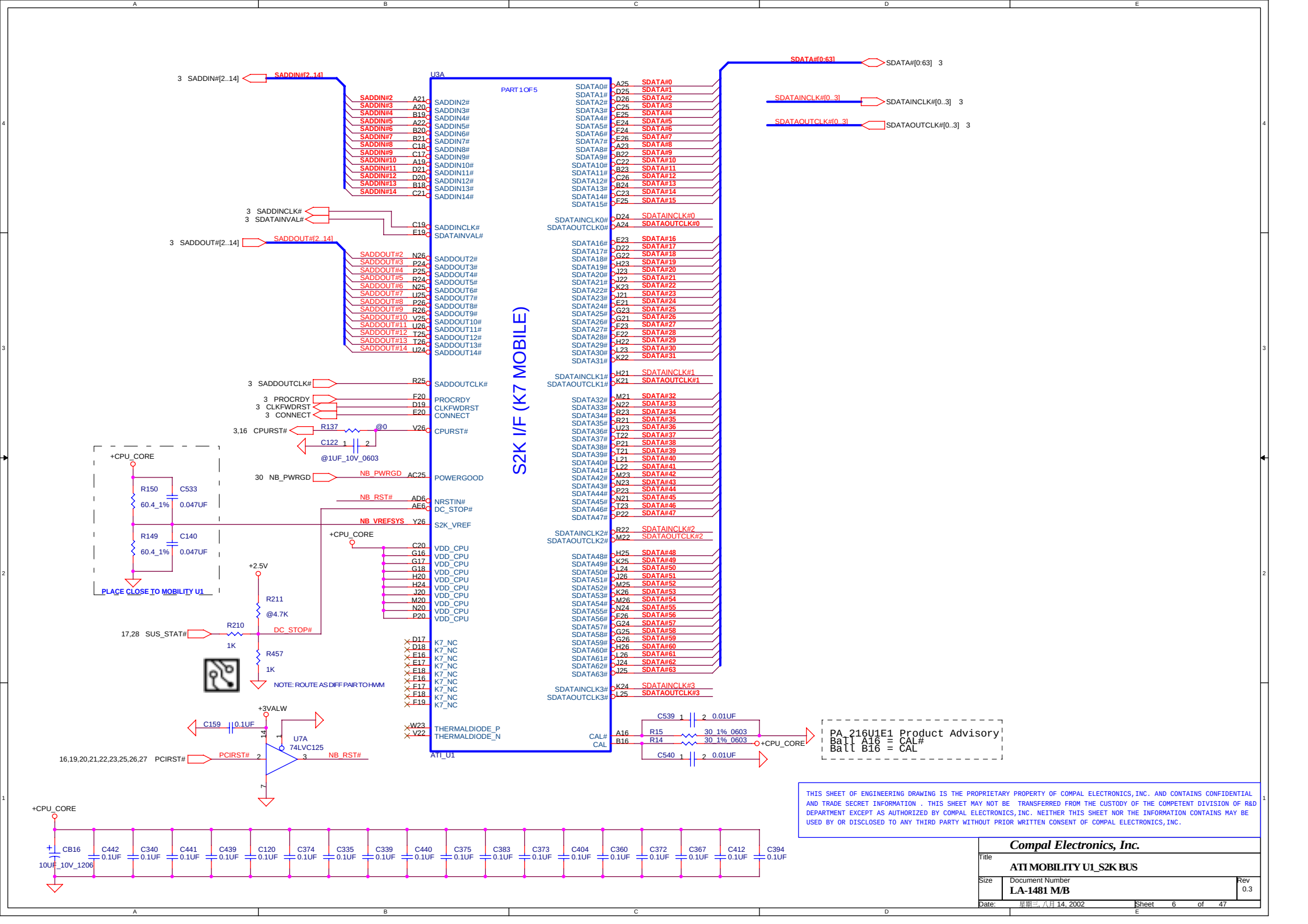

Compal Electronics, Inc.	
Title	ATI MOBILITY U1_S2K BUS
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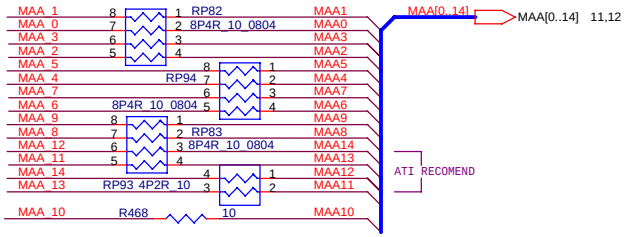
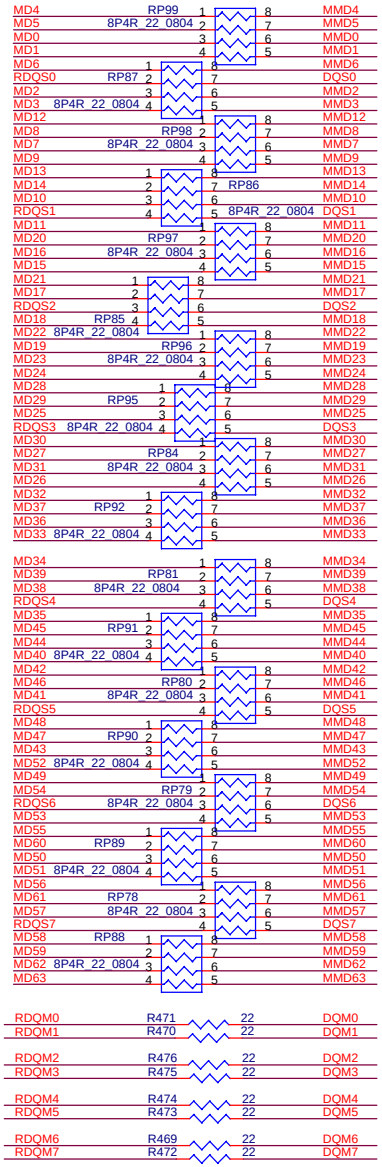
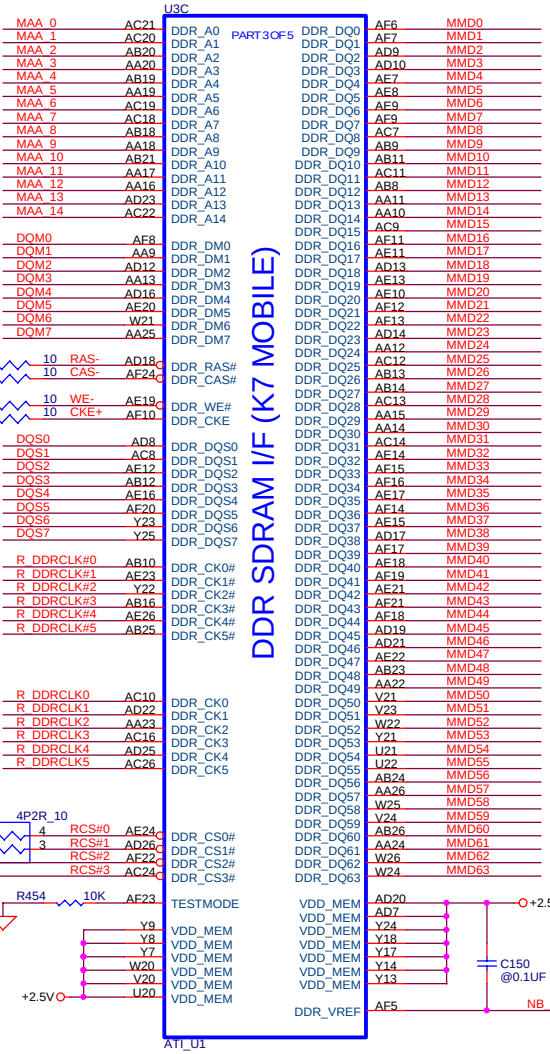
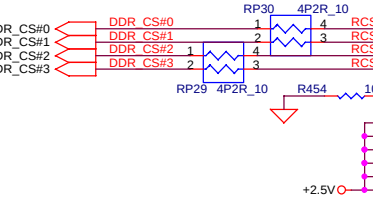
RP* place close to DIMM1

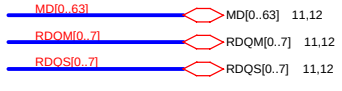


RP* PLACE CLOSE TO DIMM

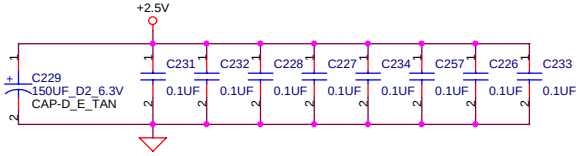




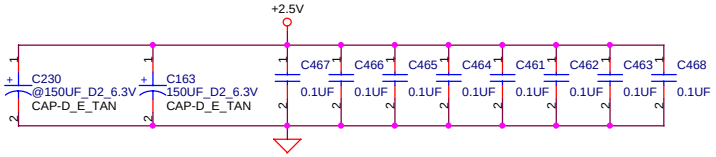


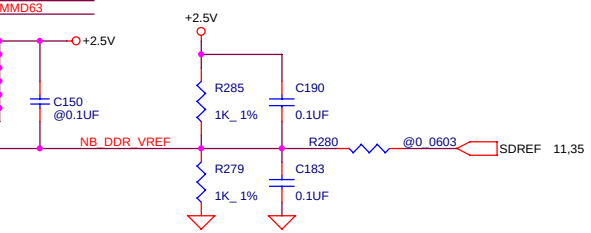


Place near SODIMM1.

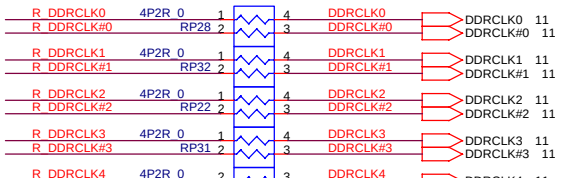


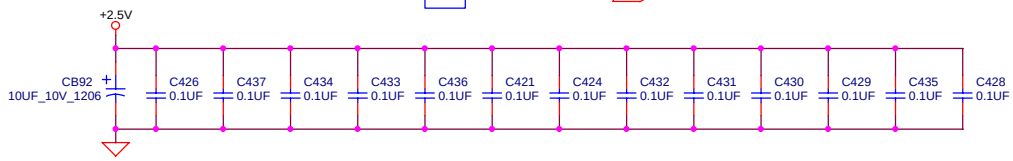
Place near SODIMM2





PLACE RPACKS CLOSE TO 1ST SO-DIMM





Compal Electronics, Inc.		
Title: ATI MOBILITY U1_DDR I/F		
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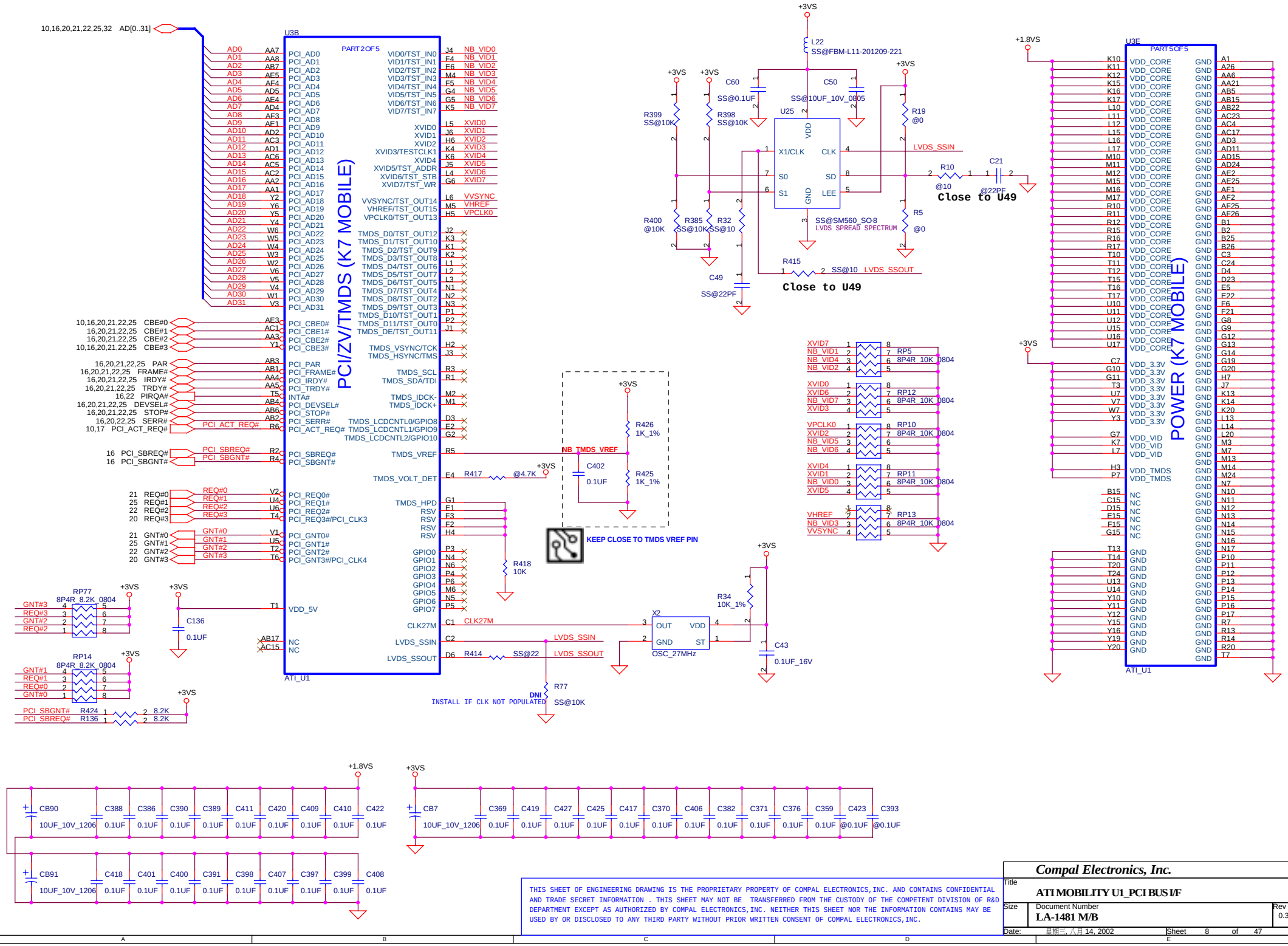

Compal Electronics, Inc.		
Title	ATI MOBILITY U1_PCI BUS I/F	
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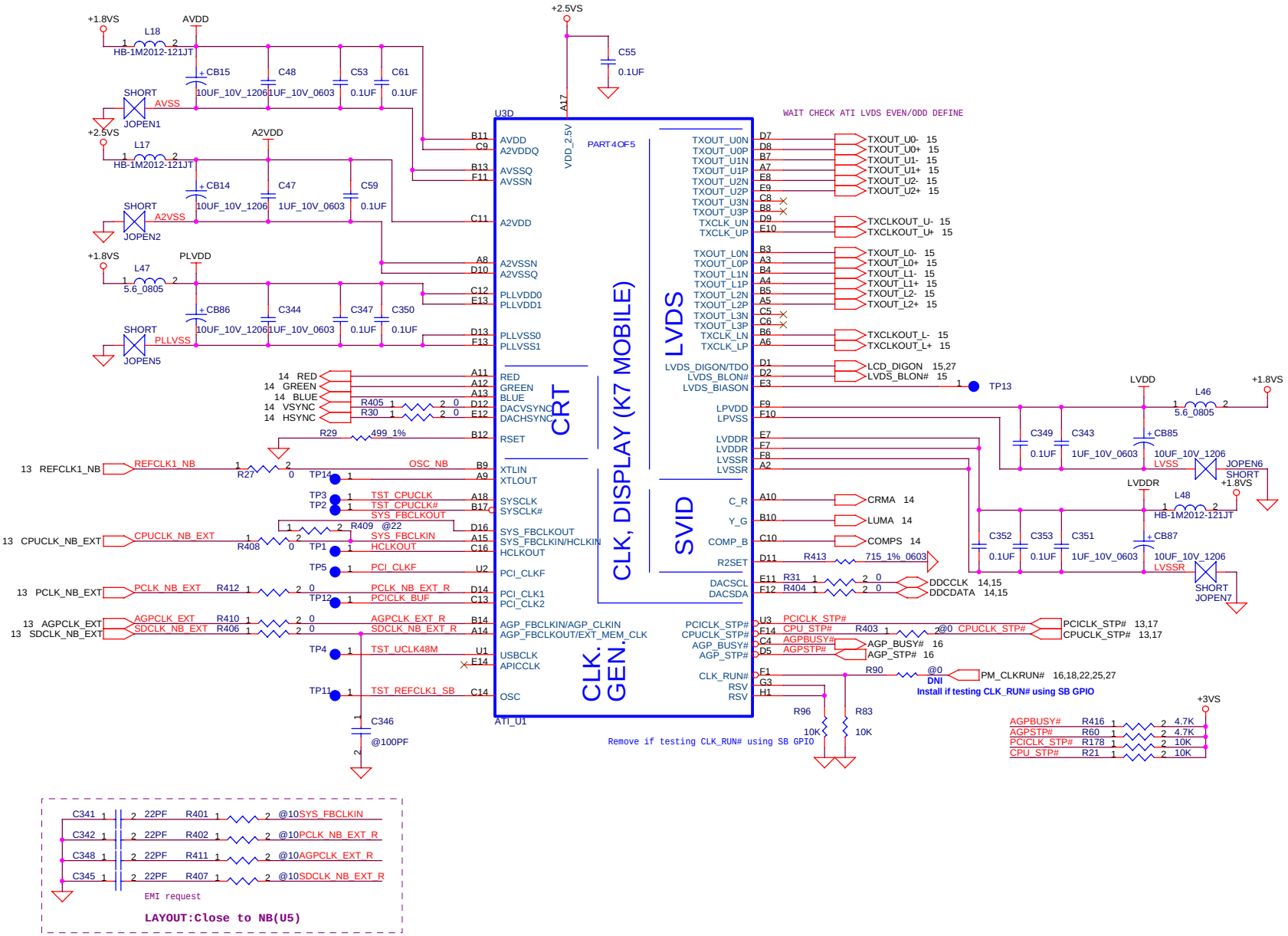
Note: AVSSQ & AVSSN require separate direct connections to GND plane (separate vias).
Note: A2VSSQ & A2VSSN require separate direct connections to GND plane (separate vias).



Compal Electronics, Inc.		
Title: ATI MOBILITY U1_CLK GEN/LVDS		
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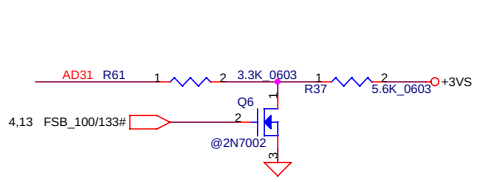


AD[31..30] : CLK SPEED

DEFAULT
- 00: 66 MHZ (1:1)
- 01: 100 MHZ (1.5:1)
- 10: 166MHZ (2.5:1)
- 11: 133 MHZ (2:1)

AD29: STRAP SET SELECTION

DEFAULT
- 0: USE FULL STRAPPING SET
- 1: USE REDUCED STRAPPING SET

AD28: SPREAD SPECTRUM ENABLE

DEFAULT
- 0: DISABLE
- 1: ENABLE

AD[27..26] : CPU S2K BUS LENGTH

DEFAULT
- 00: SHORT, NON-S2K INTERFACE
- 01: SINGLE S2K INTERFACE, CLOSE
- 10: FAR S2K INTERFACE, DUAL CPU
- 11: FARTHEST S2K INTERFACE, DUAL CPU

AD25: RESERVED

DEFAULT
- 0: ???
- 1: ???

AD24: INCLK_DELAY_ENABLE

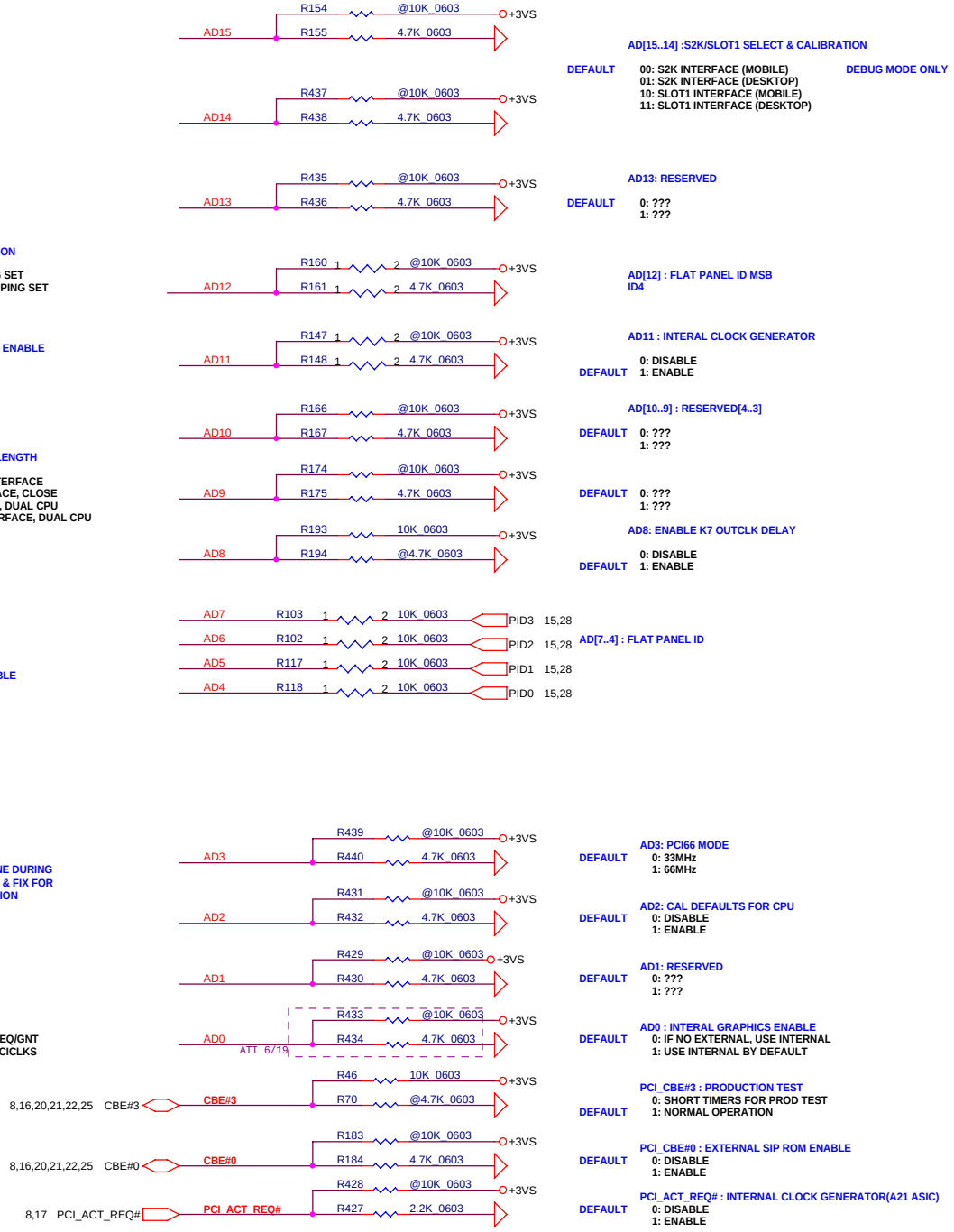
DEFAULT
- 0: DISABLE
- 1: ENABLE

AD[23..21] : SKEW ADJUST

DEFAULT 000: ??? DETERMINE DURING BRING-UP & FIX FOR PRODUCTION

AD20: PCICLK EXPANSION

DEFAULT
- 0: REQ/GNT3 USED AS REQ/GNT
- 1: REQ/GNT3 USED AS PCICLKS



AD[15..14] :S2K/SLOT1 SELECT & CALIBRATION DEBUG MODE ONLY

DEFAULT
- 00: S2K INTERFACE (MOBILE)
- 01: S2K INTERFACE (DESKTOP)
- 10: SLOT1 INTERFACE (MOBILE)
- 11: SLOT1 INTERFACE (DESKTOP)

AD13: RESERVED

DEFAULT
- 0: ???
- 1: ???

AD[12] : FLAT PANEL ID MSB
ID4

AD11 : INTERAL CLOCK GENERATOR

DEFAULT
- 0: DISABLE
- 1: ENABLE

AD[10..9] : RESERVED[4..3]

DEFAULT
- 0: ???
- 1: ???

DEFAULT
- 0: ???
- 1: ???

AD8: ENABLE K7 OUTCLK DELAY

DEFAULT
- 0: DISABLE
- 1: ENABLE

AD[7..4] : FLAT PANEL ID

AD3: PCI66 MODE

DEFAULT
- 0: 33MHz
- 1: 66MHz

AD2: CAL DEFAULTS FOR CPU

DEFAULT
- 0: DISABLE
- 1: ENABLE

AD1: RESERVED

DEFAULT
- 0: ???
- 1: ???

AD0 : INTERAL GRAPHICS ENABLE

DEFAULT
- 0: IF NO EXTERNAL, USE INTERNAL
- 1: USE INTERNAL BY DEFAULT

PCI_CBE#3 : PRODUCTION TEST

DEFAULT
- 0: SHORT TIMERS FOR PROD TEST
- 1: NORMAL OPERATION

PCI_CBE#0 : EXTERNAL SIP ROM ENABLE

DEFAULT
- 0: DISABLE
- 1: ENABLE

PCI_ACT_REQ# : INTERNAL CLOCK GENERATOR(A21 ASIC)

DEFAULT
- 0: DISABLE
- 1: ENABLE

Compal Electronics, Inc.

Title: ATI MOBILITY U1_STRAP INPUT

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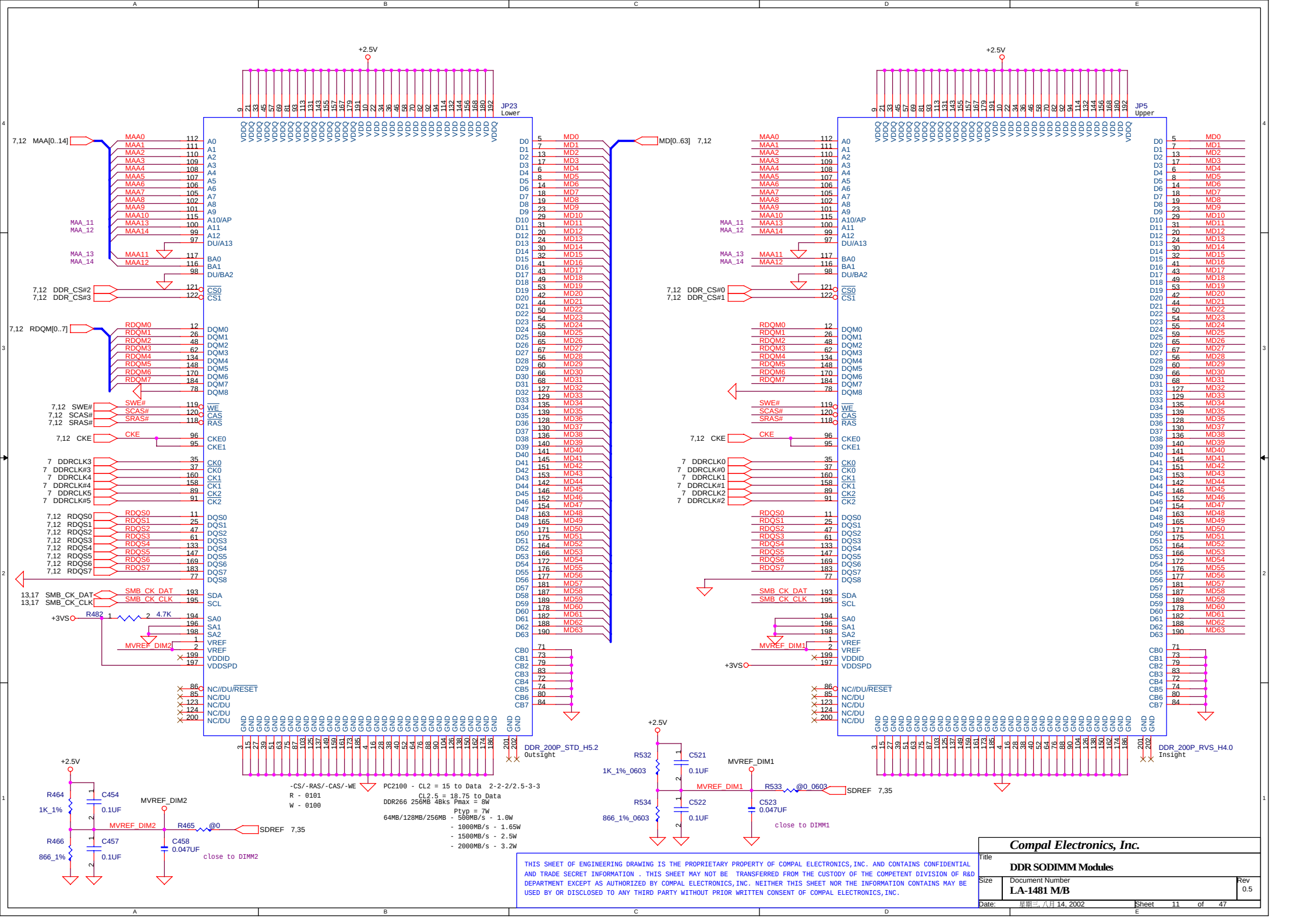

Compal Electronics, Inc.

Title: **DDR SODIMM Modules**

Size: | Document Number: **LA-1481 M/B** | Rev: 0.5

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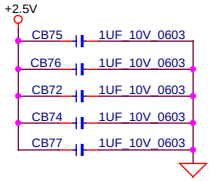
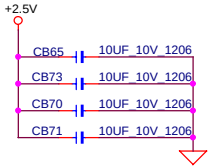
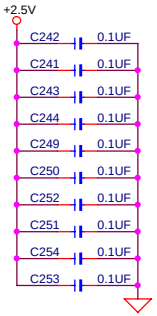
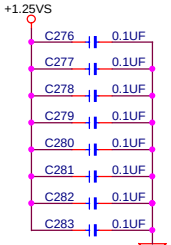
Decoupling capacitors
(Place near DDR SODIMM)

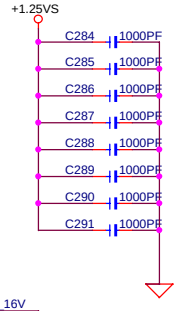


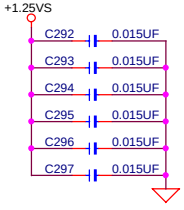


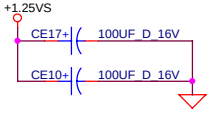


Place these decoupling capacitors close to
VTT_MEM termination resistors.





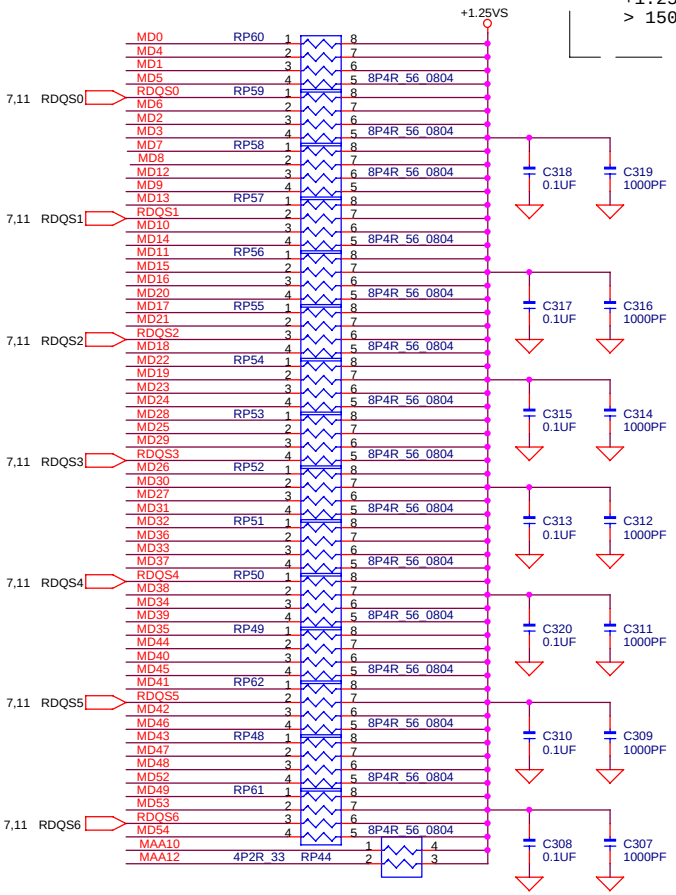


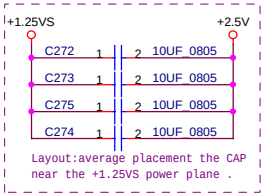


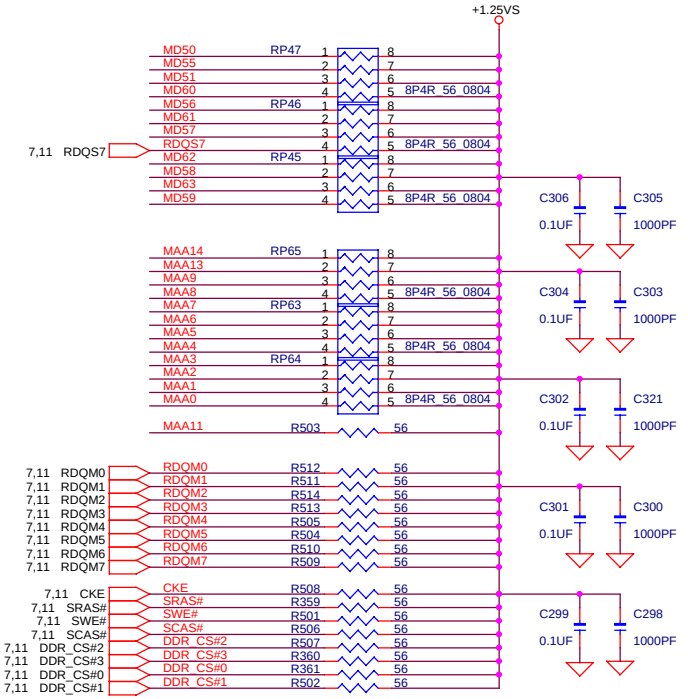
Termianation Network place closely to DIMM

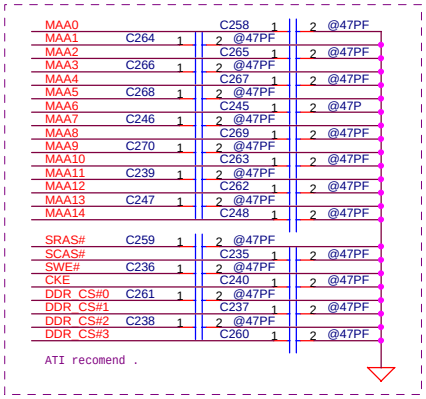
+1.25V Island
> 150ml

7,11 MD[0..63] MD[0..63]
7,11 MAA[0..14] MAA[0..14]









Compal Electronics, Inc.		
Title: DDR SDRAM Terminations		
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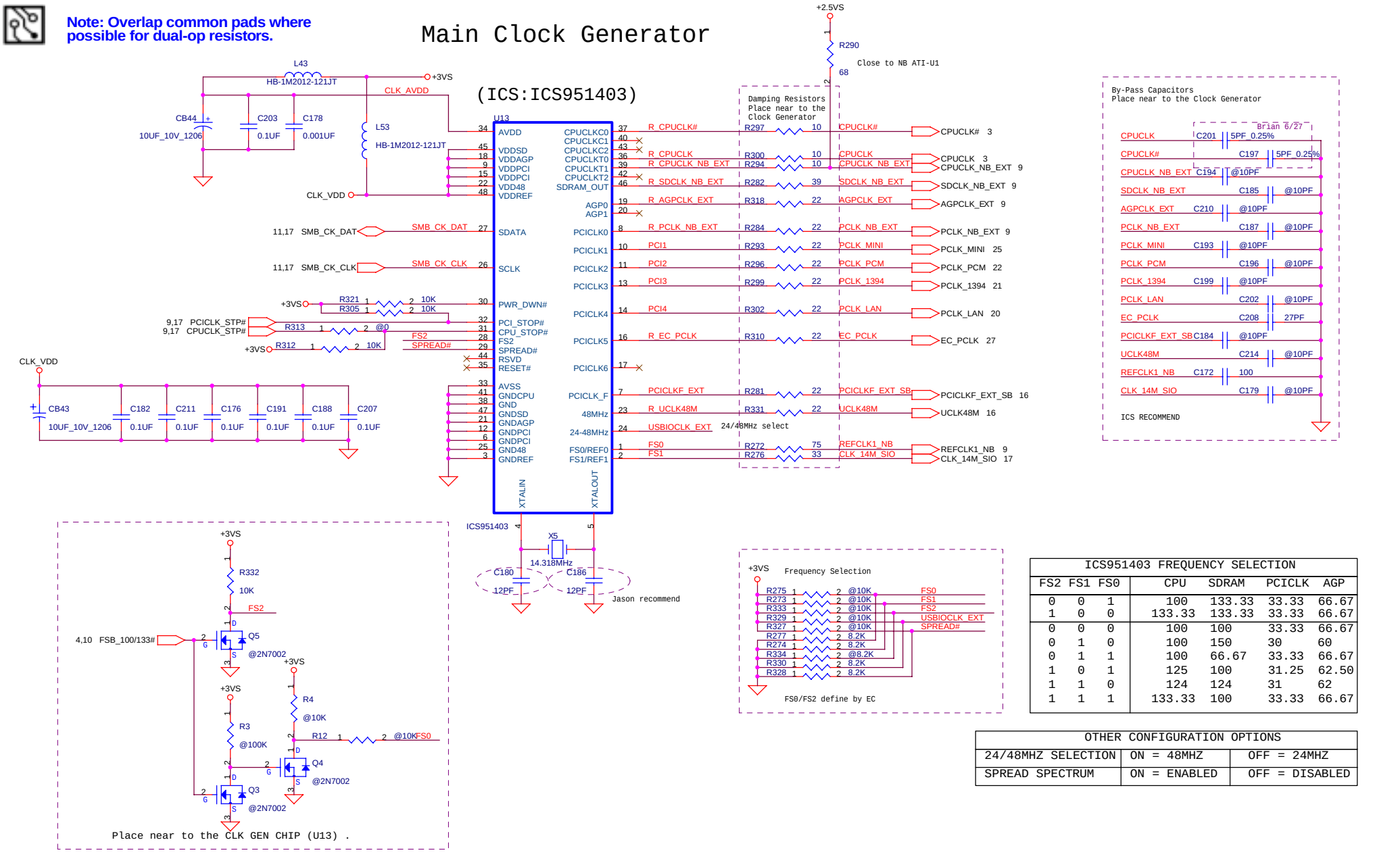
Main Clock Generator

Note: Overlap common pads where possible for dual-op resistors.

(ICS:ICS951403)



ICS951403 FREQUENCY SELECTION						
FS2	FS1	FS0	CPU	SDRAM	PCICLK	AGP
0	0	1	100	133.33	33.33	66.67
1	0	0	133.33	133.33	33.33	66.67
0	0	0	100	100	33.33	66.67
0	1	0	100	150	30	60
0	1	1	100	66.67	33.33	66.67
1	0	1	125	100	31.25	62.50
1	1	0	124	124	31	62
1	1	1	133.33	100	33.33	66.67

OTHER CONFIGURATION OPTIONS		
24/48MHZ SELECTION	ON = 48MHZ	OFF = 24MHZ
SPREAD SPECTRUM	ON = ENABLED	OFF = DISABLED

Compal Electronics, Inc.

Title: **Clock Generator**

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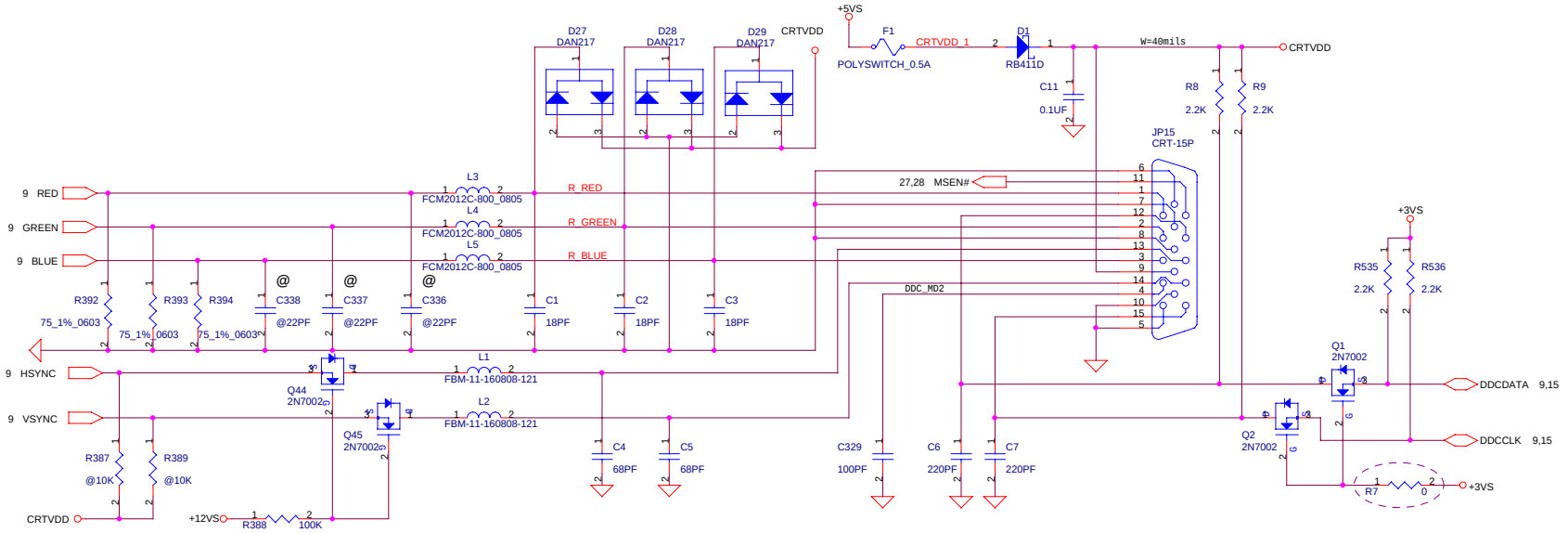
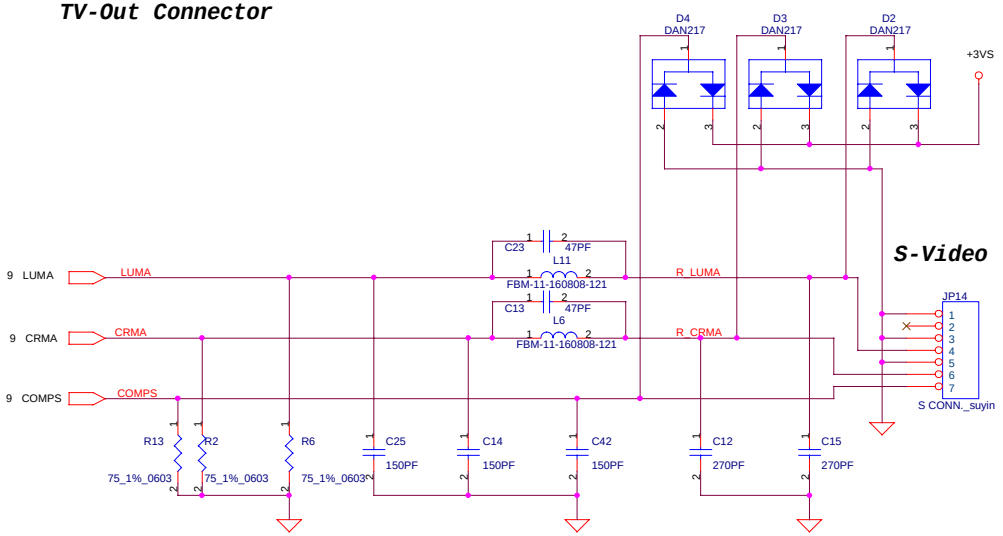
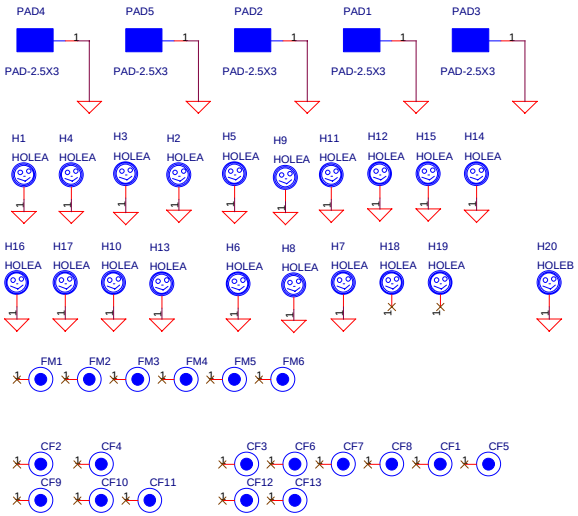
CRT Connector



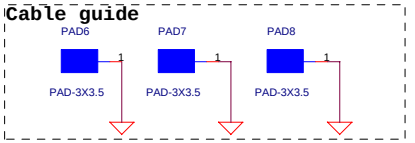
TV-Out Connector



EMI PAD around RAM DOOR



Cable guide



Compal Electronics, Inc.	
Title	CRT & TVout Connector
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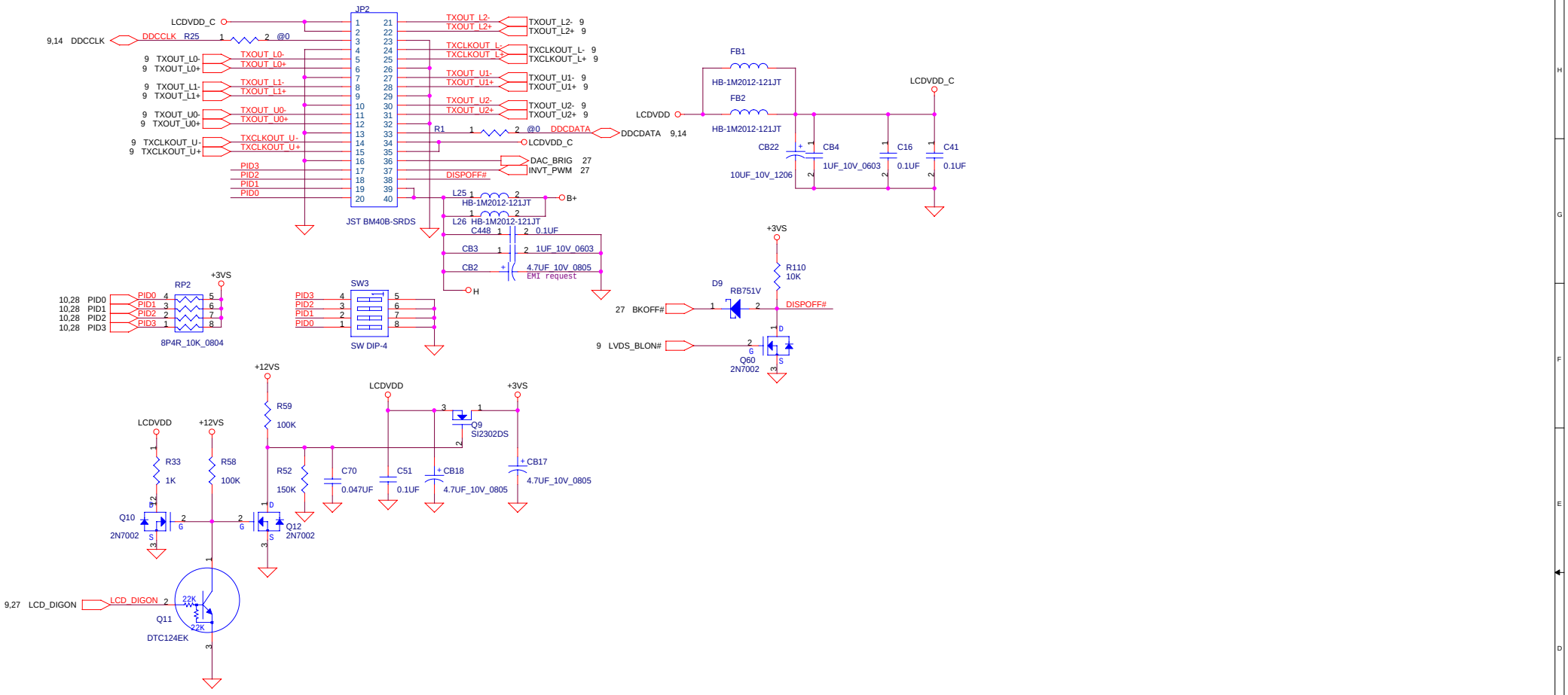

Compal Electronics, Inc.		
Title: LVDS & PID CONN.		
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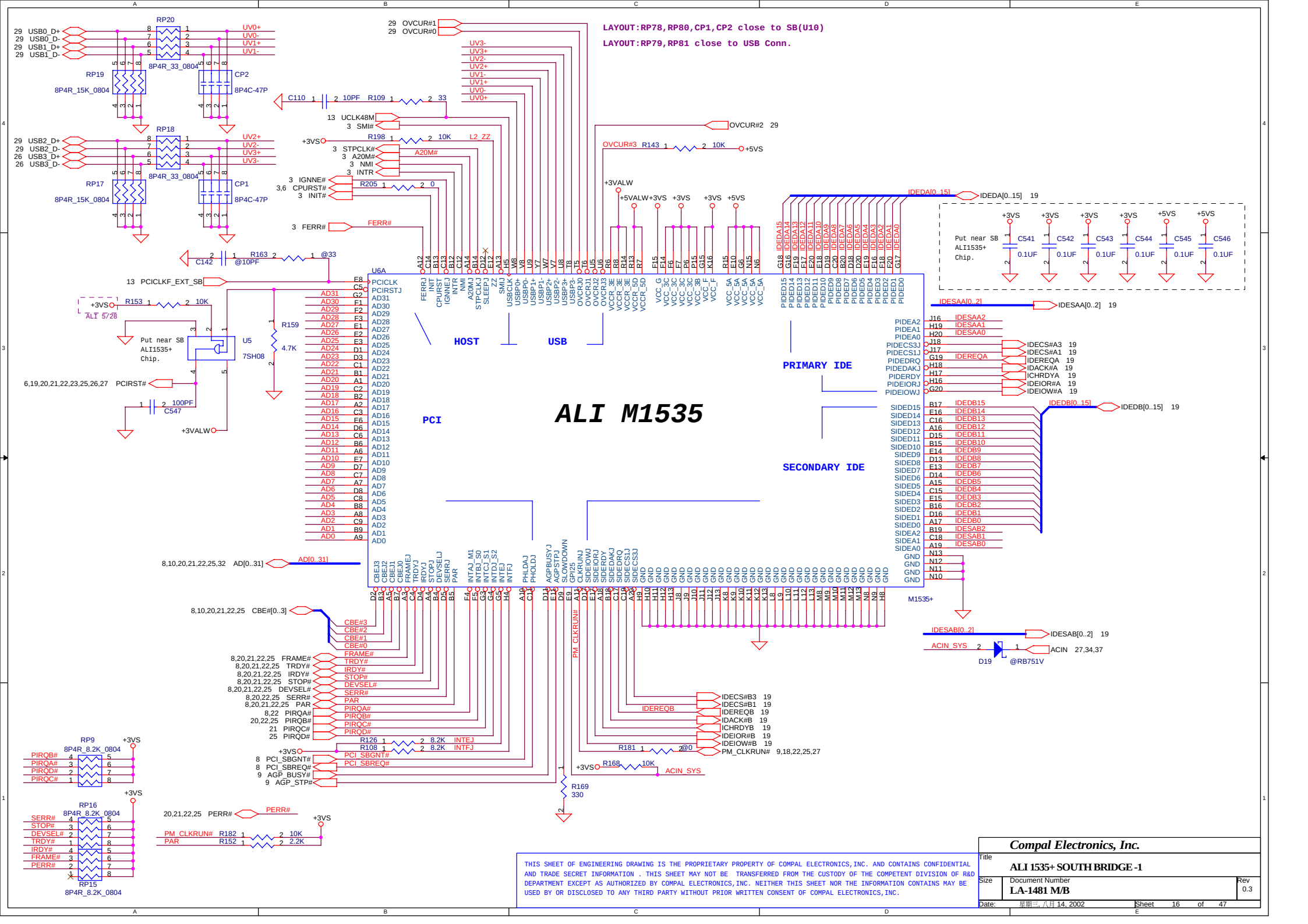

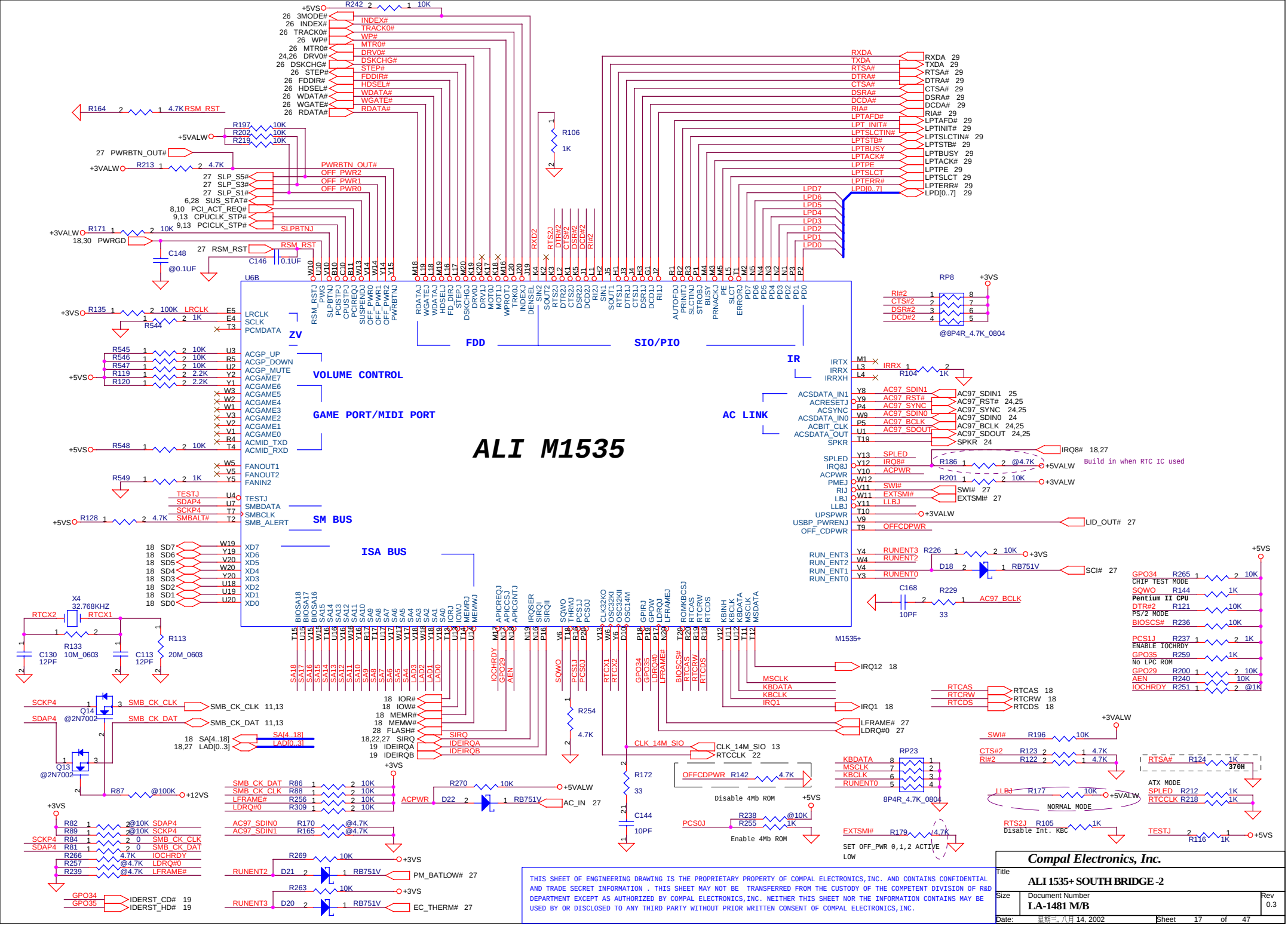

Compal Electronics, Inc.

Title: ALI 1535+ SOUTH BRIDGE -2

Size | Document Number: LA-1481 M/B | Rev: 0.3

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ISA

17 SD[0..7] — SD[0..7]

17 SA[4..18] — SA[4..18]

RP36 — 10P8R_10K

SD0	6	5	+5VS
SD1	7	4	SD6
SD2	8	3	SD3
SD5	9	2	SD7
+5VS	10	1	SD4

RP26 — 10P8R_10K

SA16	6	5	+5VS
SA17	7	4	SA5
SA18	8	3	SA7
	9	2	SA6
+5VS	10	1	SA4

RP34 — 10P8R_10K

SA13	1	10	+5VS
SA9	2	9	SA15
SA10	3	8	SA12
SA8	4	7	SA14
+5VS	5	6	SA11

RP33 — 8P4R_10K_0804

+5VS	5	4	IOW# 17
	6	3	IOR# 17
	7	2	MEMR# 17
	8	1	MEMW# 17

+5VALW

R214 1 2 10K — IRQ12 17

R180 1 2 10K — IRQ1 17

PCI

NOTE: +3V 8.2K

+3VS — R188 @10K — PM_CLKRUN# 9,16,22,25,27

R189 @1K

+3VS — R527 10K — SIRQ 17,22,27

RP35 — 8P4R_10K_0804

LAD1	4	5	+3VS
LAD2	3	6	
LAD3	2	7	
LAD0	1	8	

17,27 LAD[0..3] — LAD[0..3]

U34 — TEST_CHIP — PLACE ON TOP SIDE

TP16	1	1	TP15
TP18	2	2	TP17
TP20	3	3	TP19
TP22	4	4	TP21
TP24	5	5	TP23
TP26	6	6	TP25
TP28	7	7	TP27
	8	8	TP29

NC, NC, NC, NC, NC, NC, NC, GND

U35 — TEST_CHIP — PLACE ON BOTTOM SIDE

TP31	1	1	TP30
TP33	2	2	TP32
TP35	3	3	TP34
TP37	4	4	TP36
TP39	5	5	TP38
TP41	6	6	TP40
TP43	7	7	TP42
	8	8	TP44

NC, NC, NC, NC, NC, NC, NC, GND

CHGRTC — W=30mils — R141 200_0603 — D11 RB751V — D10 RB751V — R145 470 — J — BATT1 — RTCBATT

+RTCVCC — W=30mils — C141 0.1UF — +CB39 10UF_6.3V_1206

If no use RTC IC , change to 22UF_10V_1206

@MMBT3906 Q15 — R162 @10K — Q16 @3904 — +3VALW — R156 @51K — R158 @10K

+3VALW — D38 RB751V

17 SD[0..7] — SD[0..7]

+5VALW — C529 0.1UF

R554 @0

U32 @DS1685

OSC32O	1	24	VCC
OSC32I	2	23	SQW
SD0	3	22	VBAUX
SD1	4	21	RCLR#
SD2	5	20	VBAT
SD3	6	19	IRQ#
SD4	7	18	KS#
SD5	8	17	RD#
SD6	9	16	GND
SD7	10	15	WR#
	11	14	ALE
GND	12	13	CS#

+RTCVCC — C530 0.1UF — R560 @0 — R566 @0

+RTCVCC +RTCVCC — R556 1K — R557 1K — RCLR#

IRQ8# 17,27

+5VALW +5VS — J3 — R555 0 — R558 10K — R559 10K

RTCDS 17

RTCRW 17

RTCAS 17

+3VS — U17D 74LVC14 — R567 @0 — 17,30 PWRGD

+3VALW — R562 10K — R561 1K — J4

X8 — OSC32O — OSC32I — @32.768KHZ_10PPM — C531 10PF — C532 10PF

All parts no build in until RTC IC build in .
R560 no build in , even if RTC IC build .

Compal Electronics, Inc.

Title: PULL UP/DOWN RESISTOR&RTC

Size | Document Number: LA-1481 M/B | Rev: 0.3

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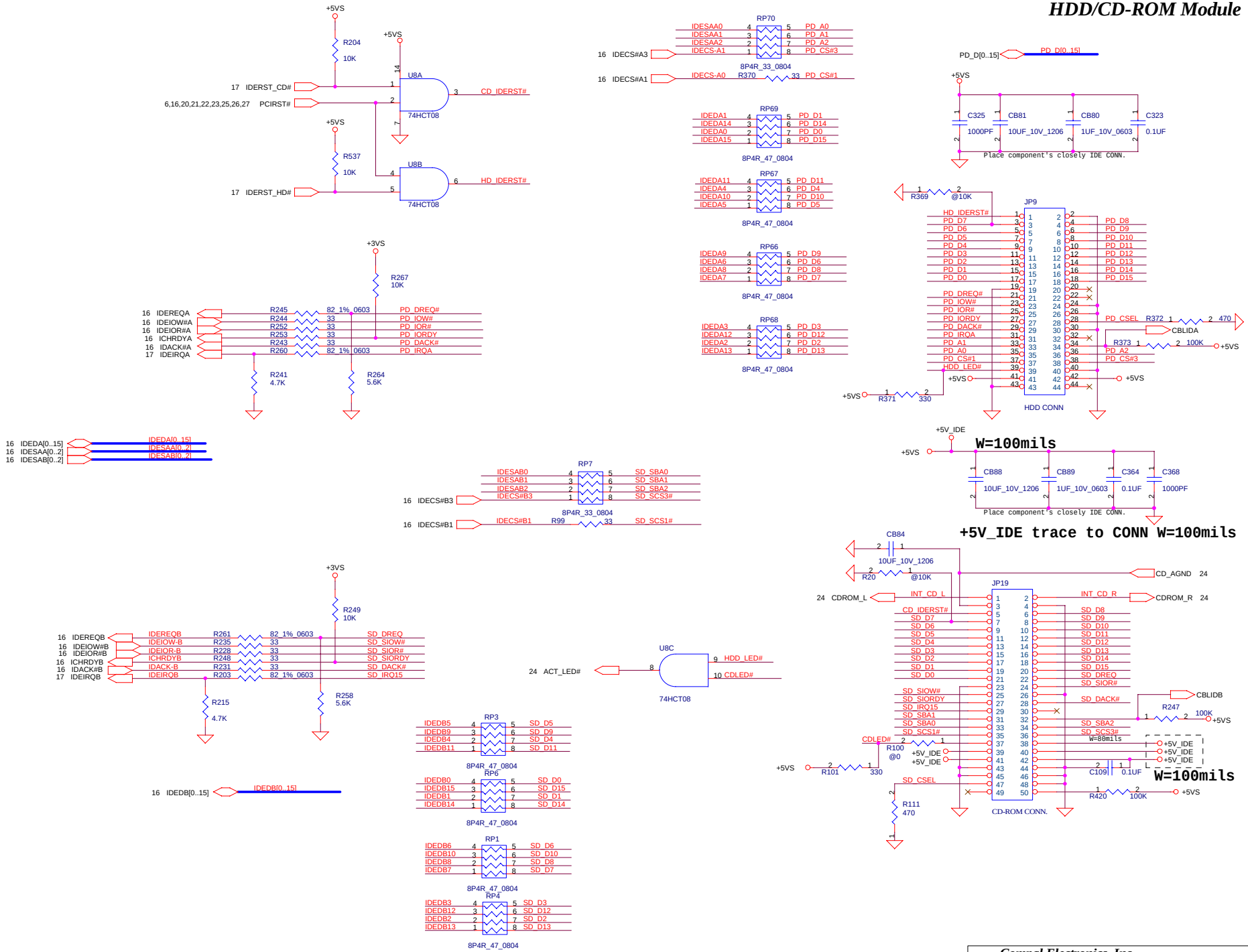
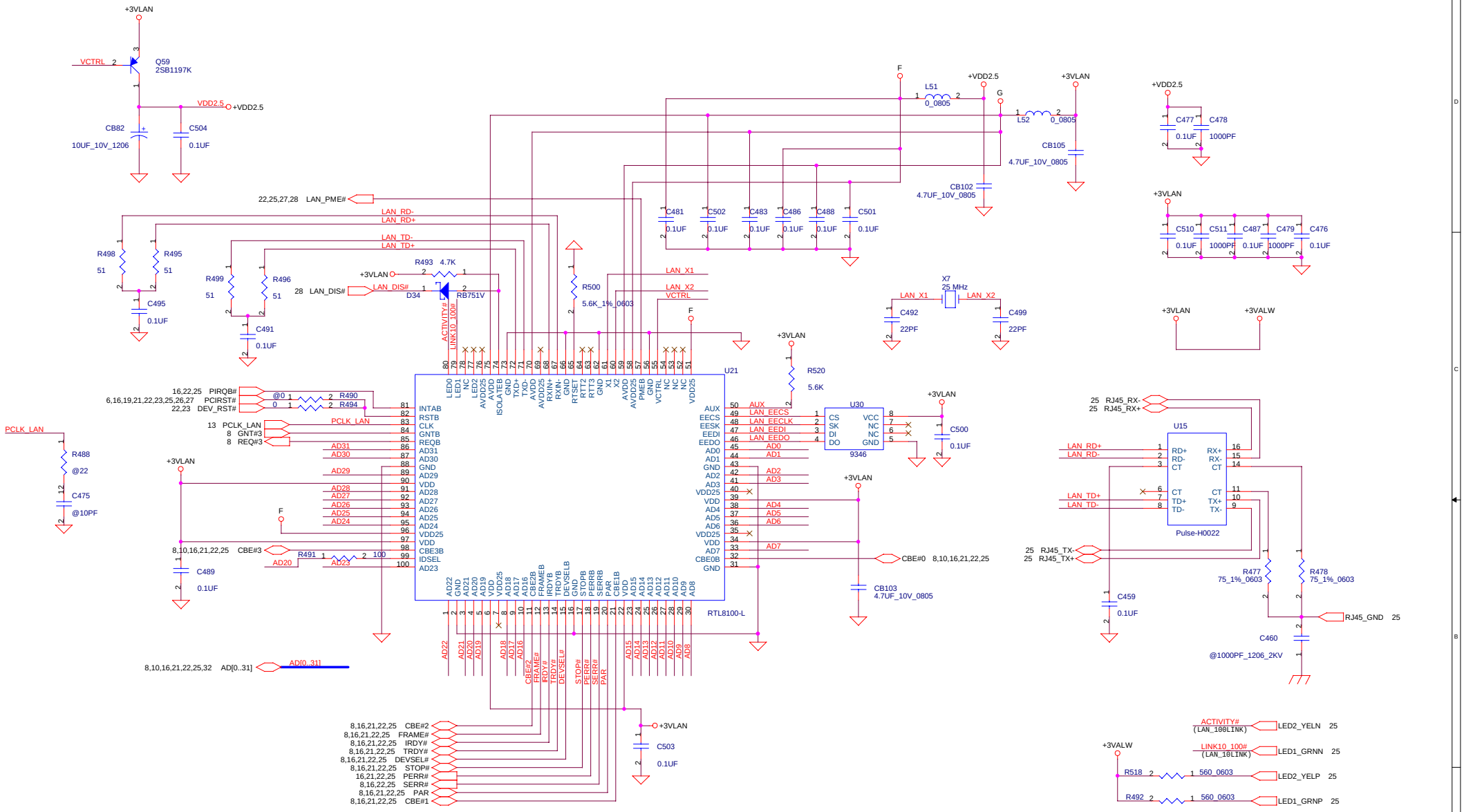
HDD/CD-ROM Module



Compal Electronics, Inc.		
Title	HDD & CDROM Connector	
Size	Document Number LA-1481 M/B	Rev 0.3
Date: 星期三, 八月 14, 2002	Sheet 19 of 47	



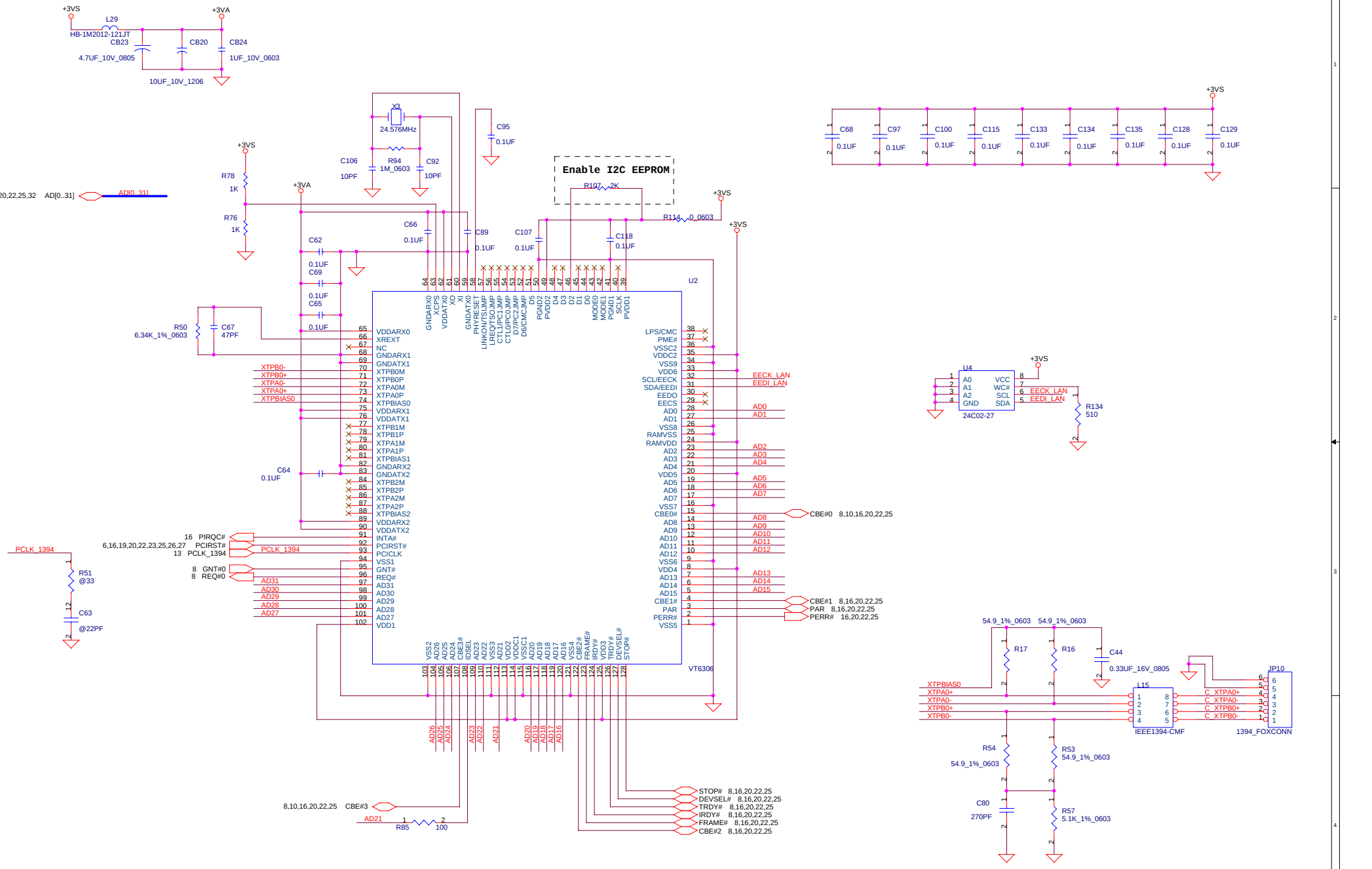
Compal Electronics, Inc.

Title: **LAN Controller**

Size | Document Number: **LA-1481 M/B** | Rev: 0.5

Date: 星期二, 八月 14, 2002 | Sheet 20 of 47

IEEE1394 Controller/PHY



Compal Electronics, Inc.	
Title	IEEE1394 Controller & PHY
Size	Document Number: LA-1481 M/B
Rev	0.3
Date:	星期三, 八月 14, 2002
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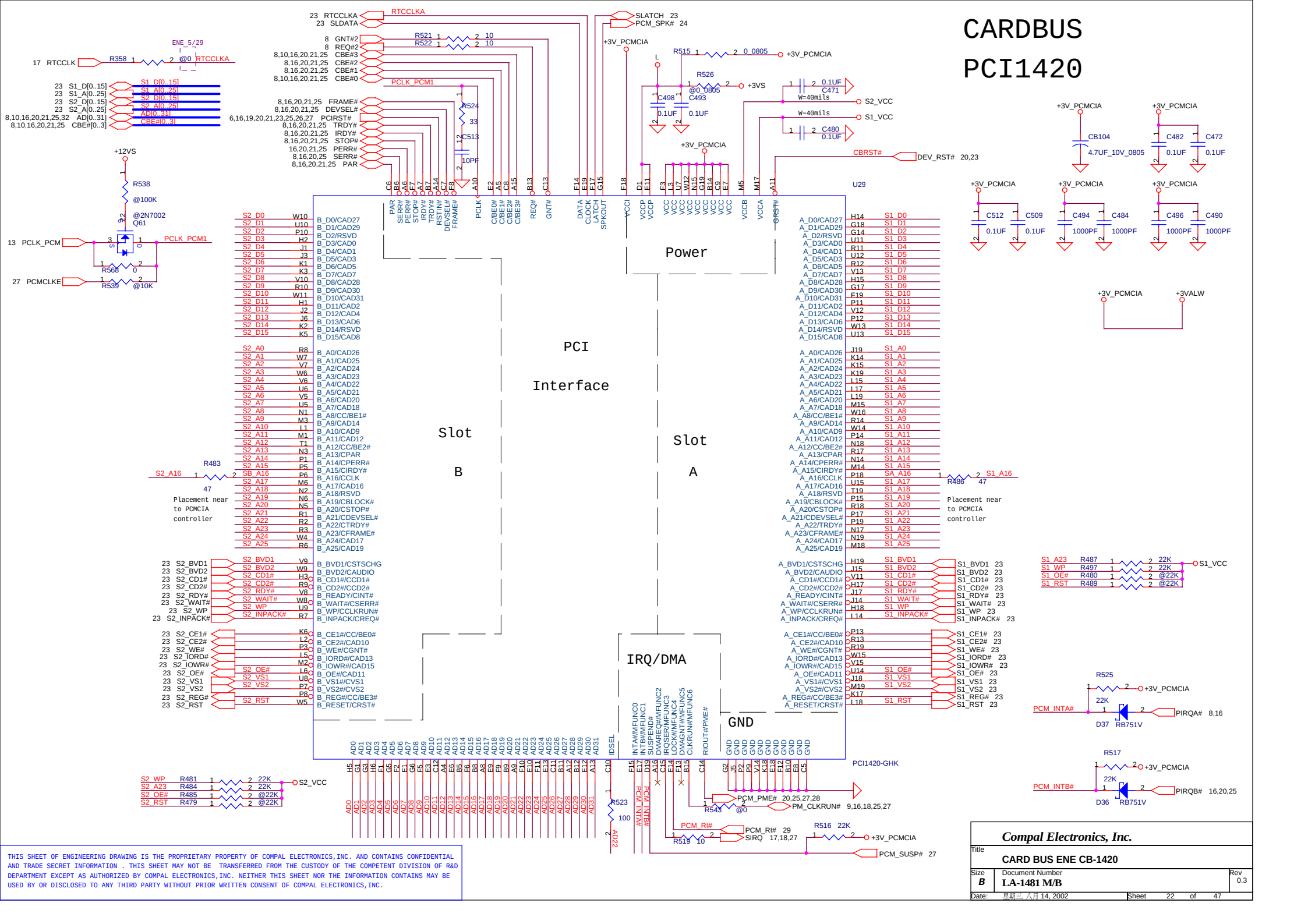
CARDBUS PCI1420



Compal Electronics, Inc.

Title	CARD BUS ENE CB-1420	
Size: B	Document Number: LA-1481 M/B	Rev: 0.3
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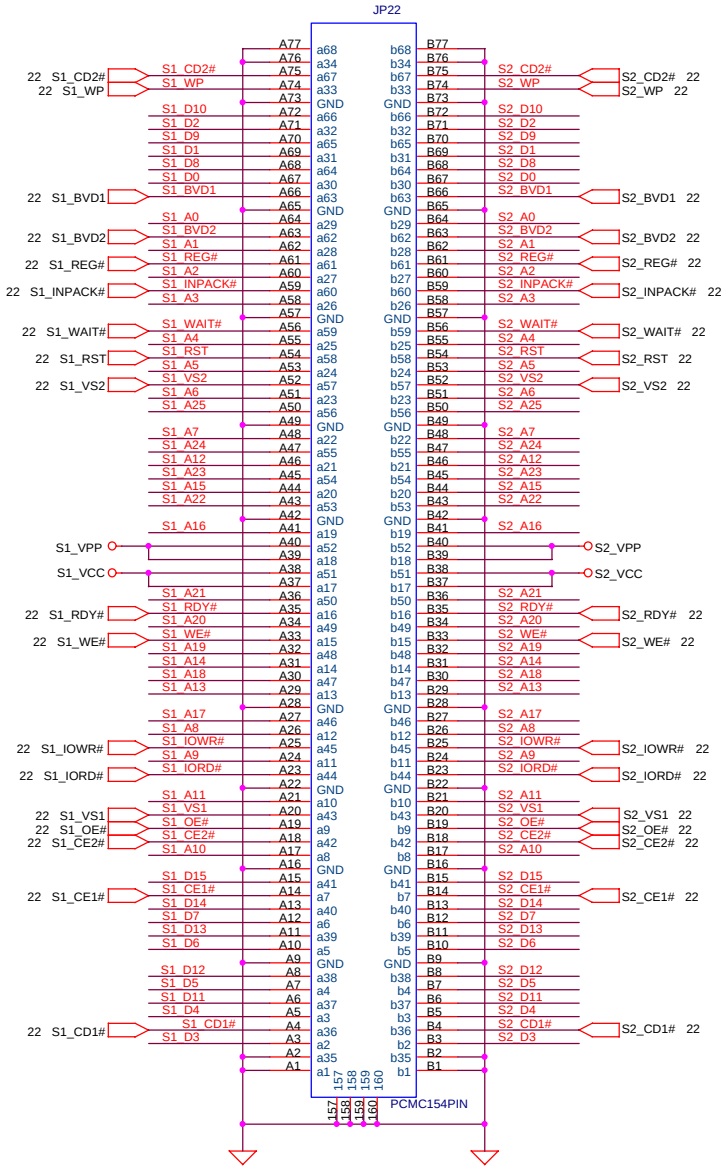
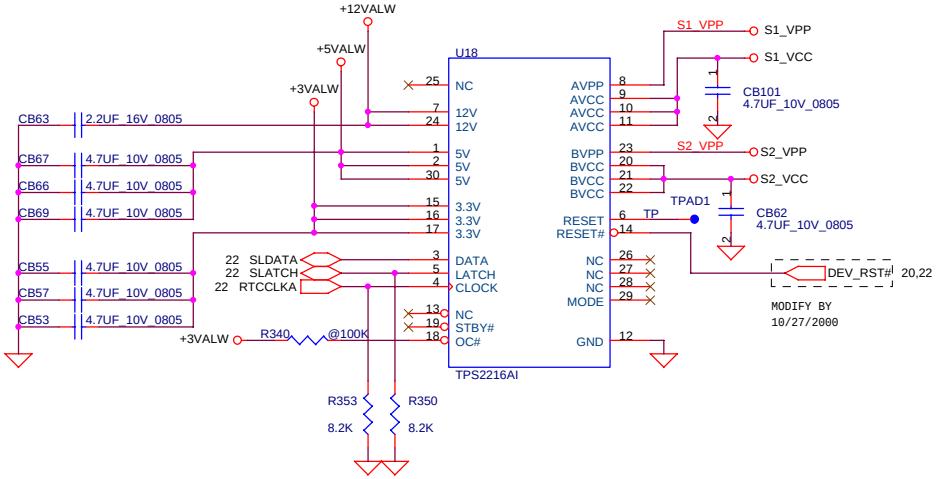
CARDBUS SOCKET

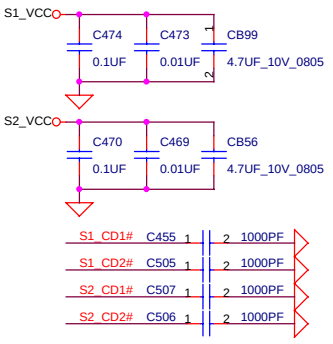


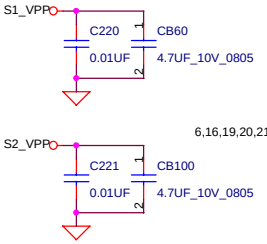
PCMCIA POWER CTRL.

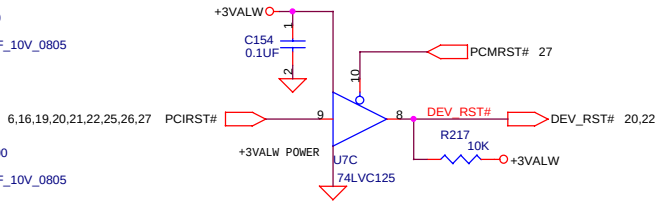
22 S1_D[0..15]
22 S1_A[0..25]
22 S2_D[0..15]
22 S2_A[0..25]

JP22A
PCMCIA_SOCKET







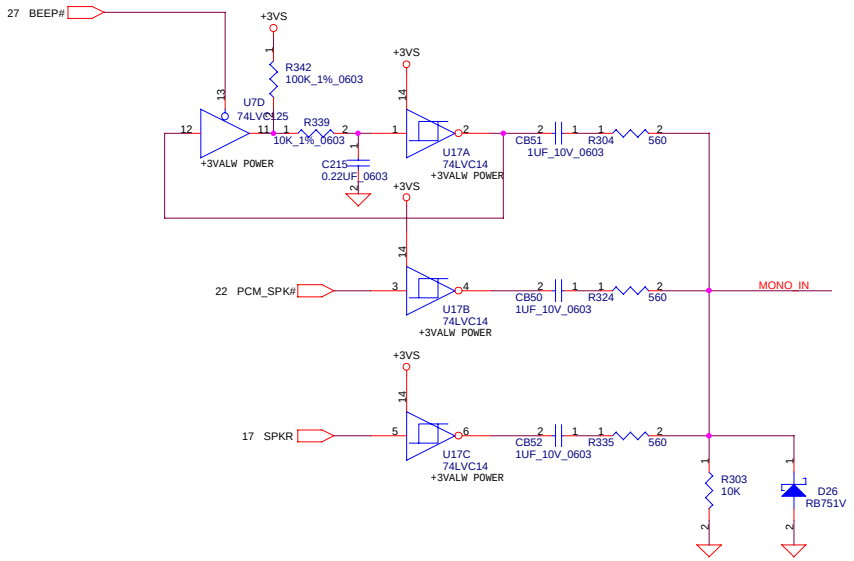


Compal Electronics, Inc.

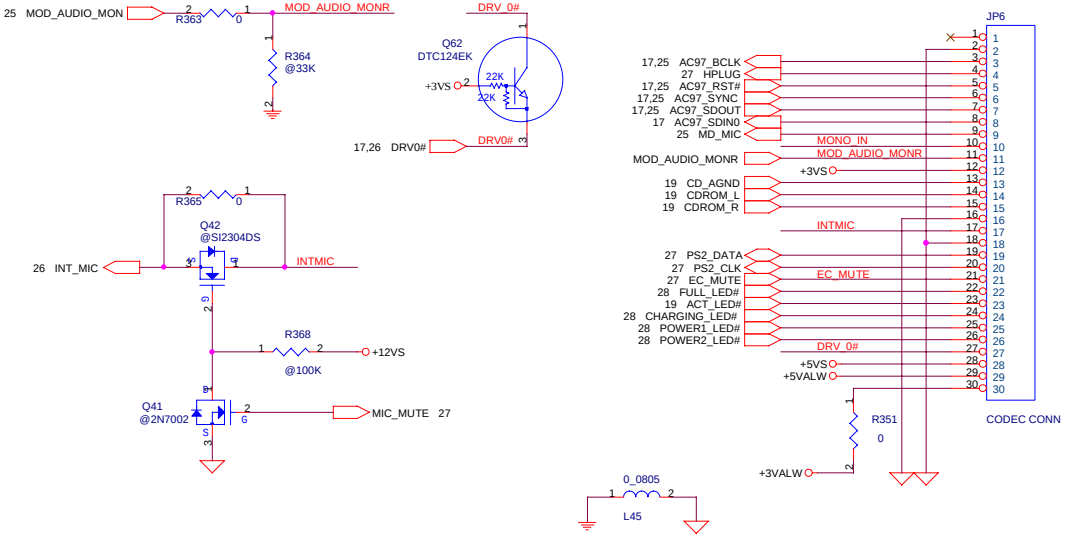
Title: CARD BUS SOCKET

Size: B | Document Number: LA-1481 M/B | Rev: 0.3

Date: 星期三, 八月 14, 2002 | Sheet 23 of 47



AC97 CODEC ALC202 CONN



Compal Electronics, Inc.	
Title	AC97 Codec
Size	Document Number: LA-1481 M/B
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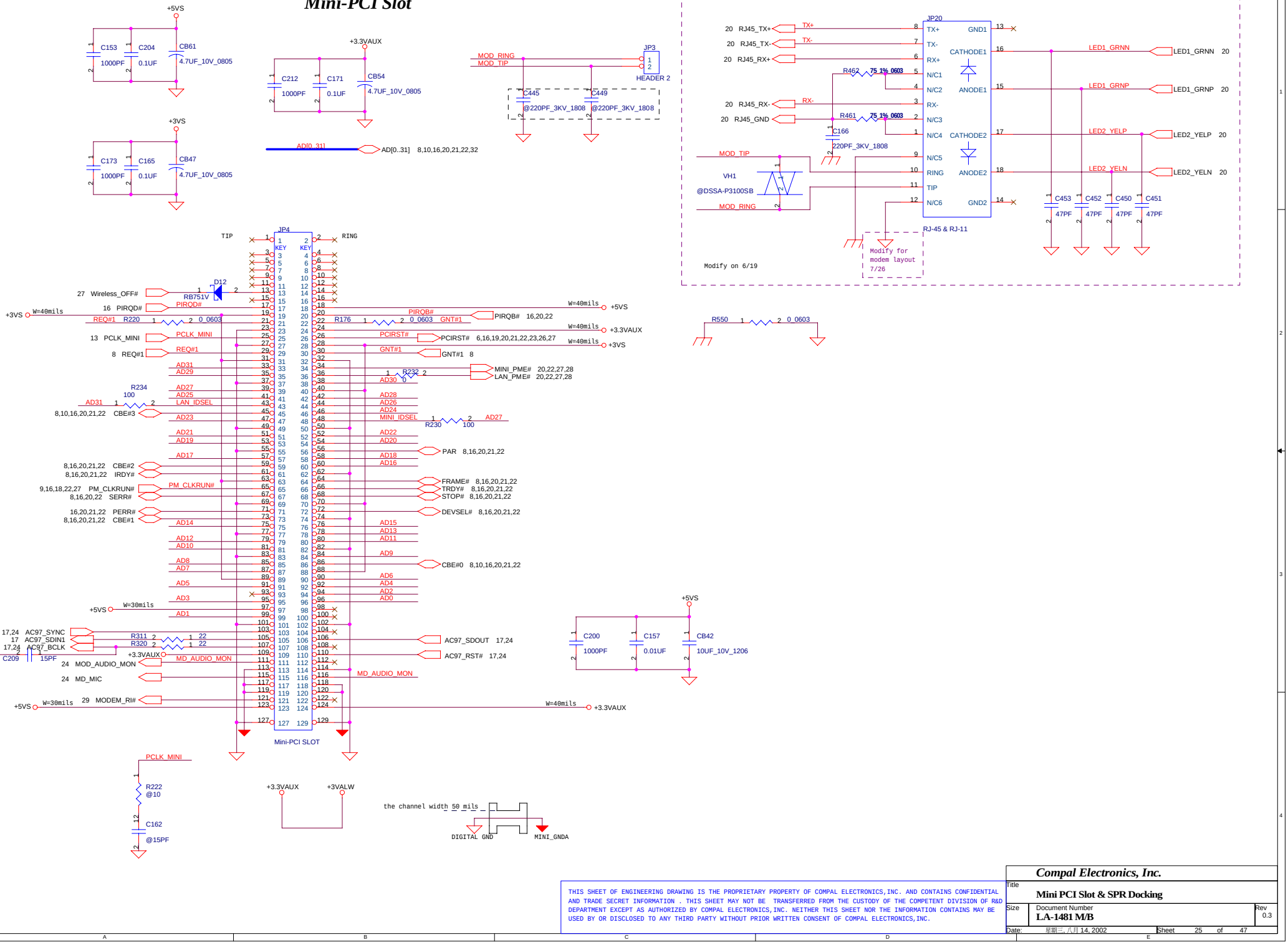
Mini-PCI Slot



Compal Electronics, Inc.		
Title: Mini PCI Slot & SPR Docking		
Size	Document Number: LA-1481 M/B	Rev: 0.3
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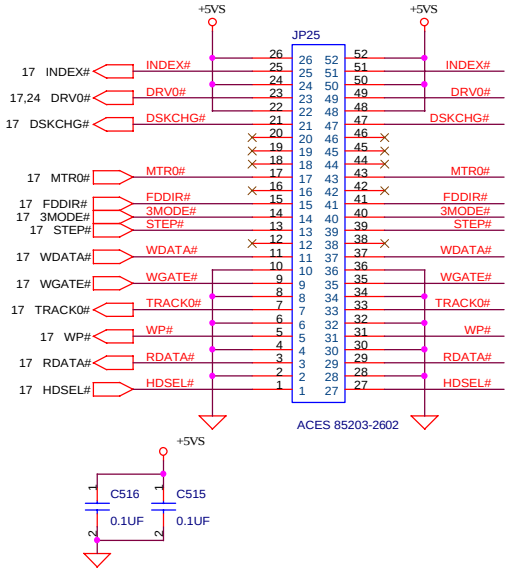
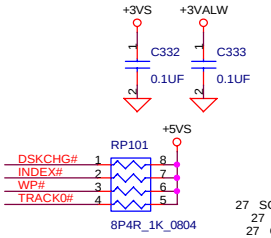
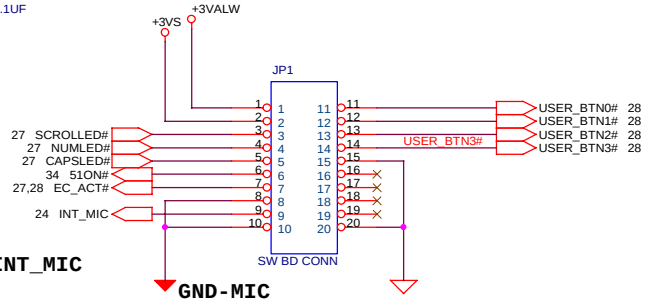
FDD CONN.



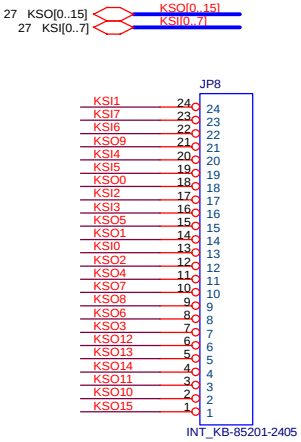


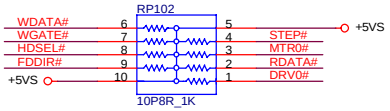
SWITCH BOARD CONN.

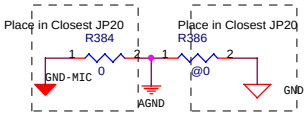


GND-MIC need around INT_MIC

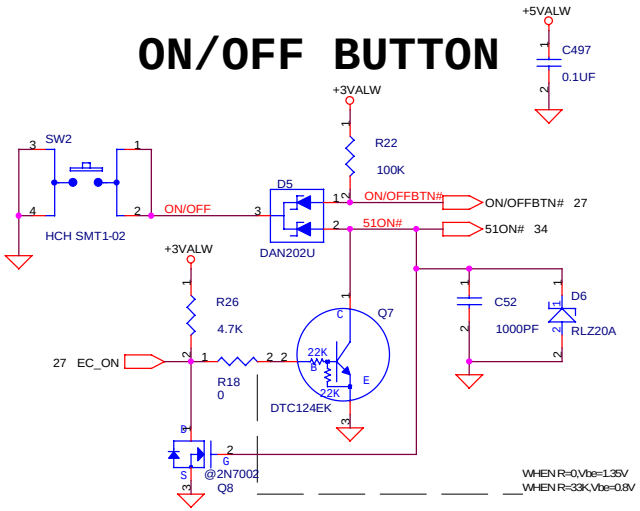
INT_KBD CONN.

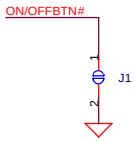




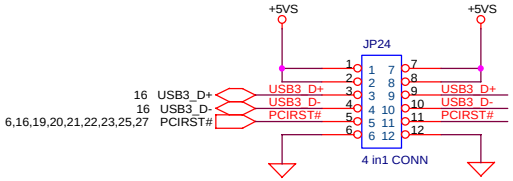


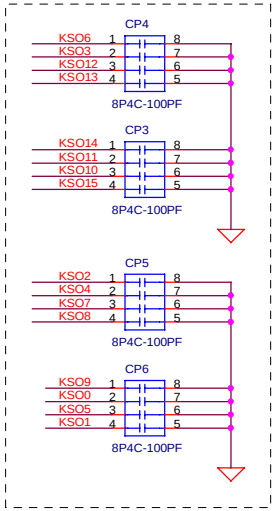
ON/OFF BUTTON





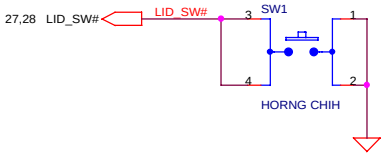
4 IN 1 CONN





NEED CLOSEST JP18 ADD BY EMI REQUEST

LID SW



Compal Electronics, Inc.		
Title: **System Connector**		
Size	Document Number: **LA-1481 M/B**	Rev: 0.3
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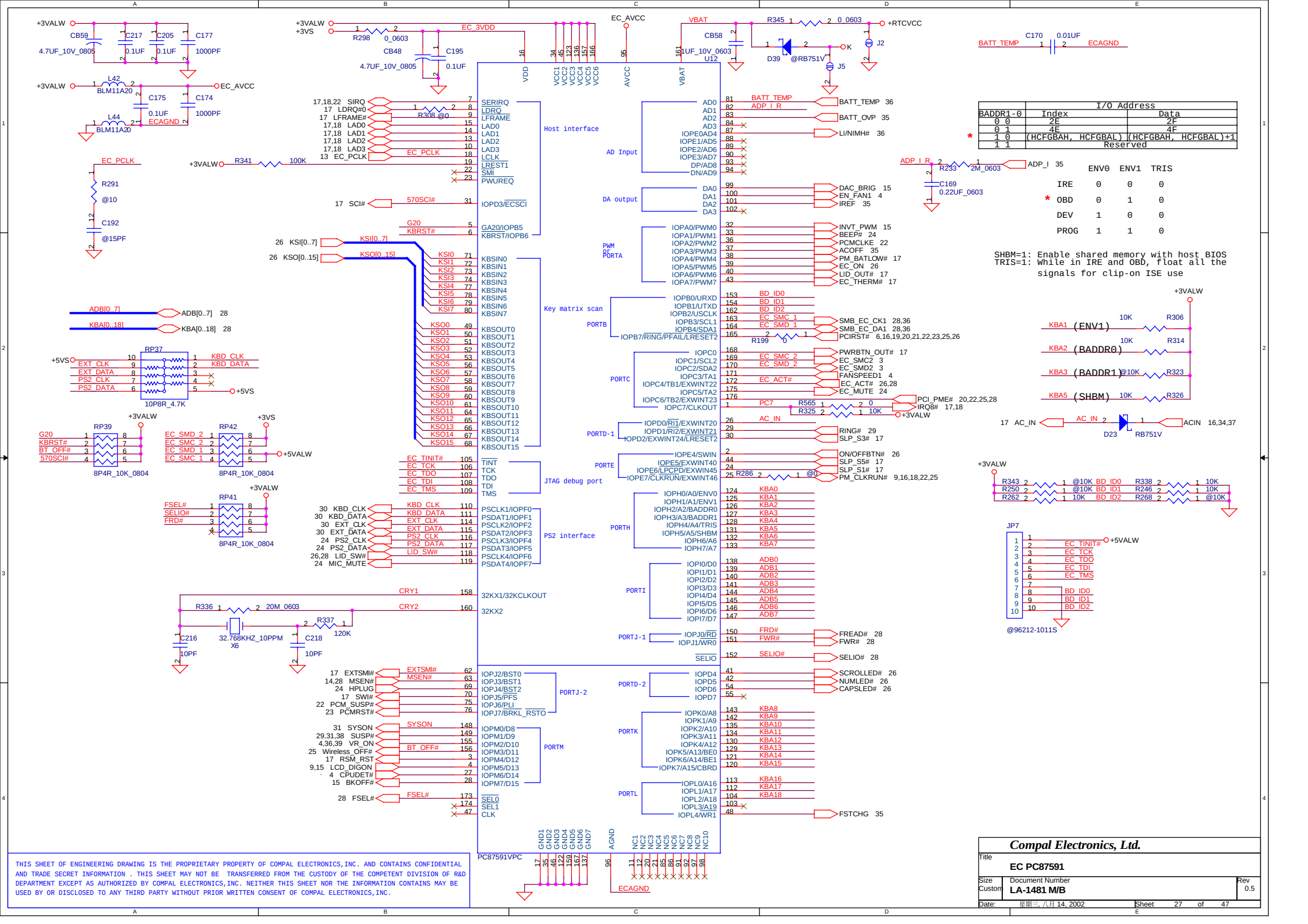
PC87591VPC
Host interface
AD Input
DA output
PWM or PORTA
Key matrix scan
PORTB
PORTC
PORTD-1
PORTE
JTAG debug port
PS2 interface
PORTH
PORTI
PORTJ-1
PORTJ-2
PORTD-2
PORTK
PORTM
PORTL
I/O Address
BADDR1-0 | Index | Data
0 0 | 2E | 2F
0 1 | 4E | 4F
1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1
1 1 | Reserved
ENV0 ENV1 TRIS
IRE 0 0 0
OBD 0 1 0
DEV 1 0 0
PROG 1 1 0
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use
@96212-1011S
Compal Electronics, Ltd.
EC PC87591
LA-1481 M/B
0.5
Date: 星期三, 八月 14, 2002
Sheet 27 of 47
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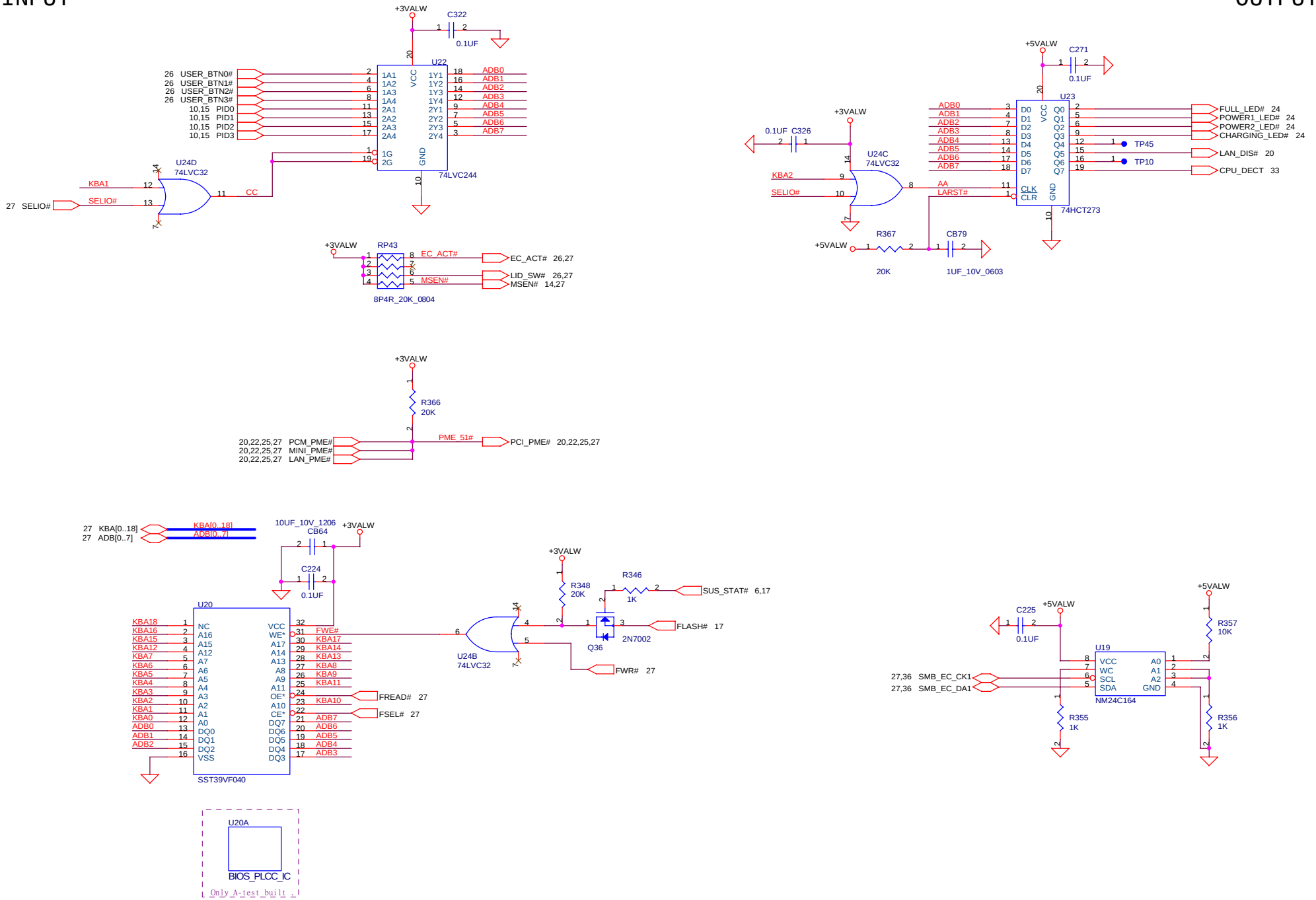
INPUT

OUTPUT



Compal Electronics, Inc.		
Title: BIOS & EC I/O Port		
Size	Document Number: LA-1481 M/B	Rev: 0.3
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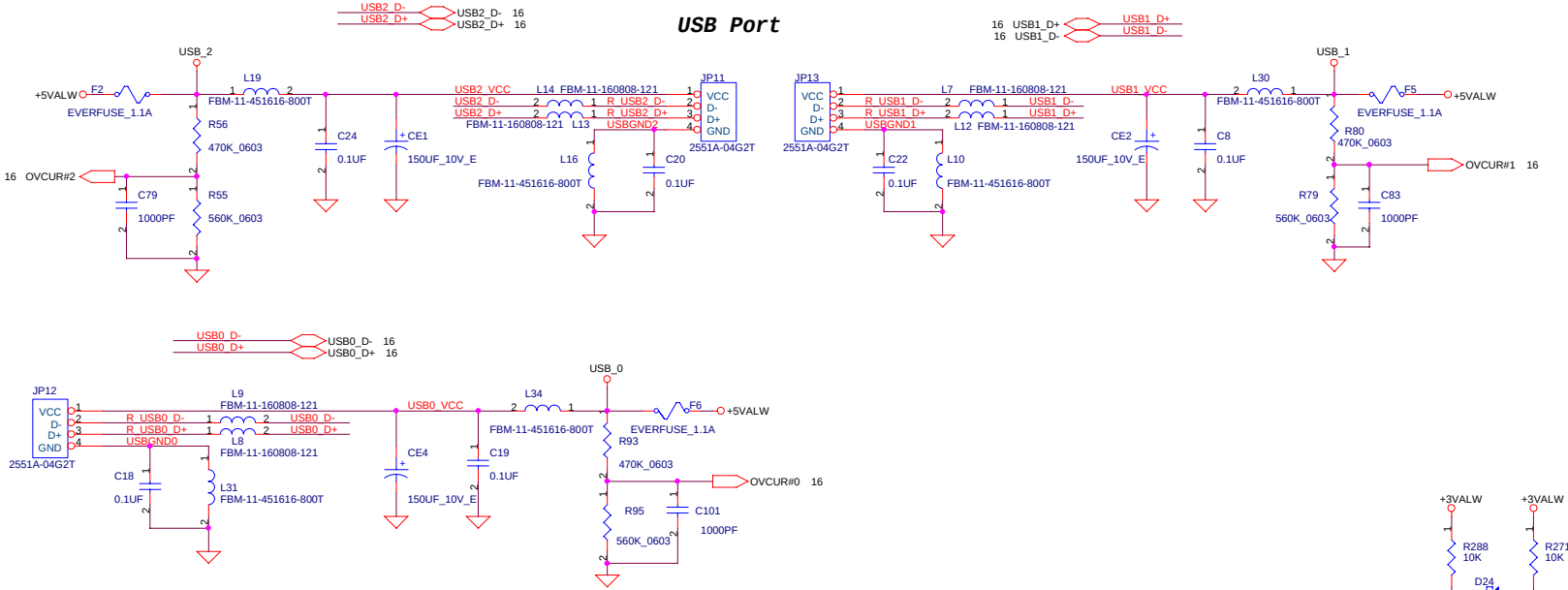
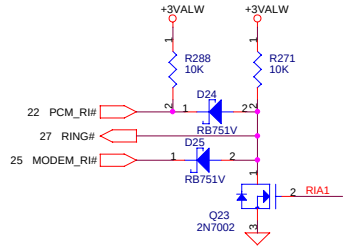
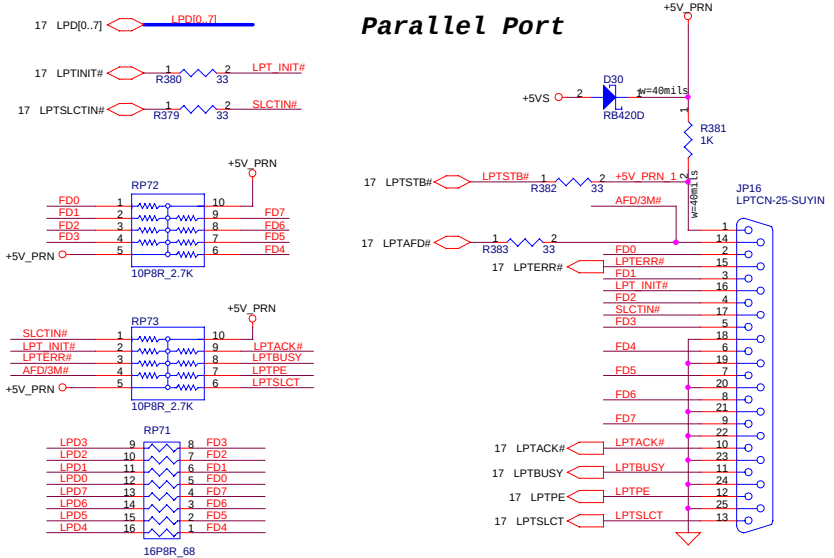
Printer Port/USB

USB Port

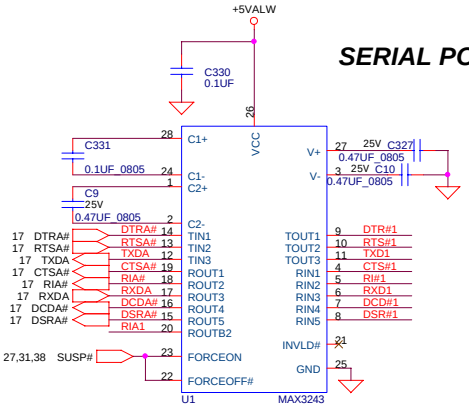


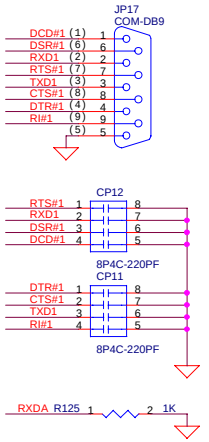


Parallel Port



SERIAL PORT





Compal Electronics, Inc.	
Title	Printer/COM/USB Port
Size	Document Number: LA-1481 M/B
Rev	0.5
Date:	星期三, 八月 14, 2002
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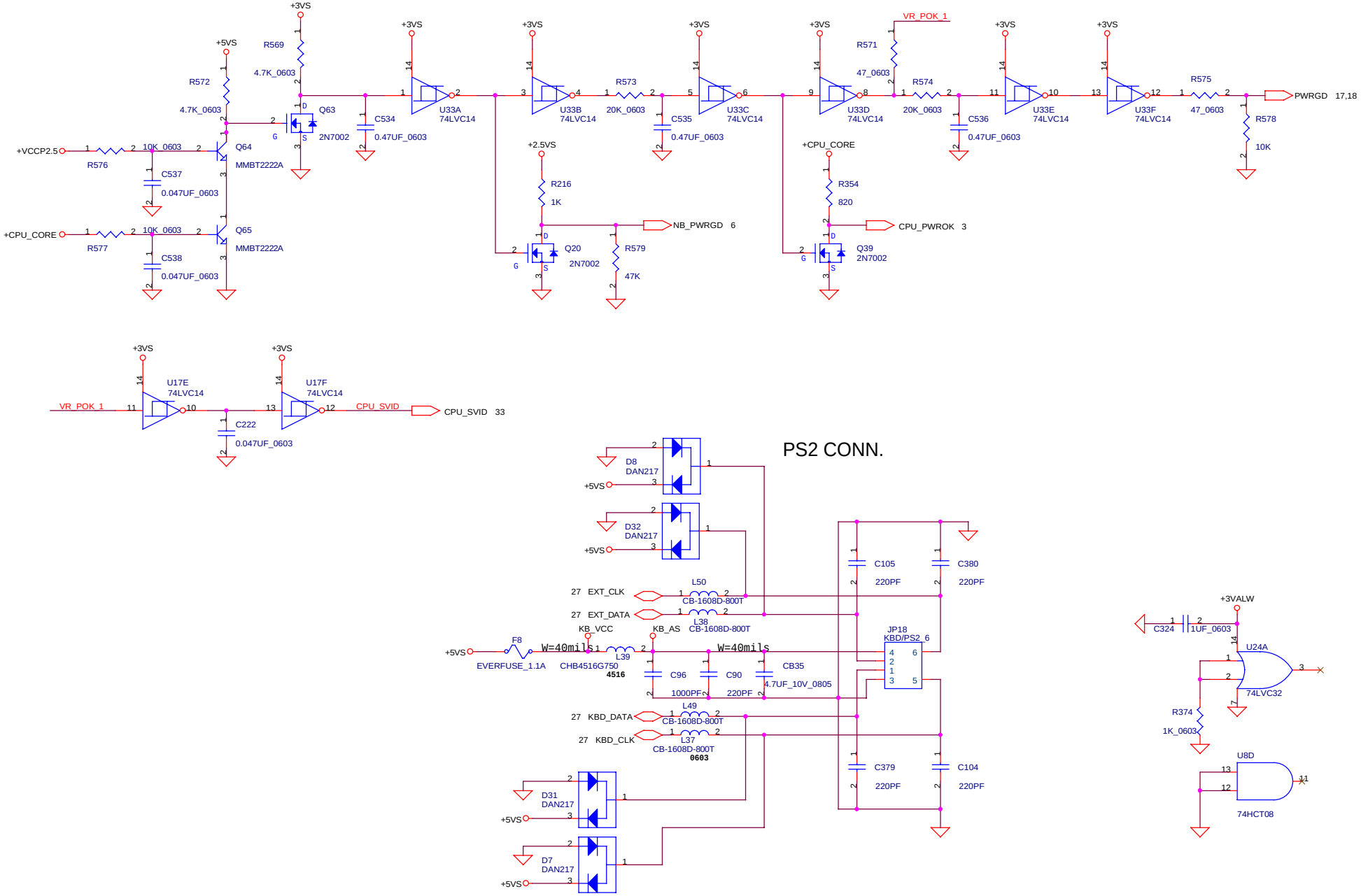
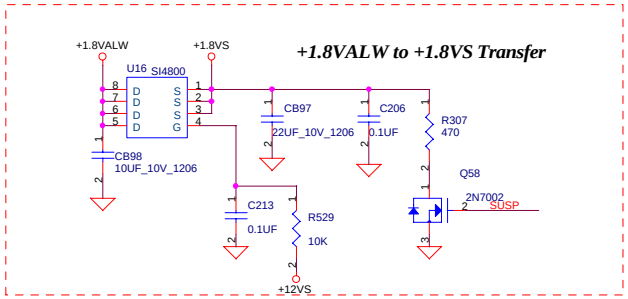
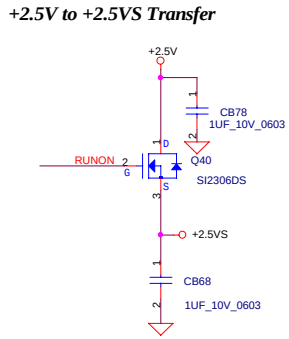
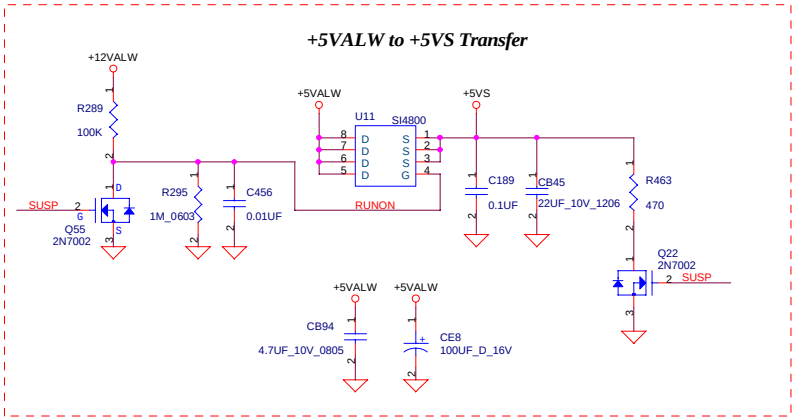
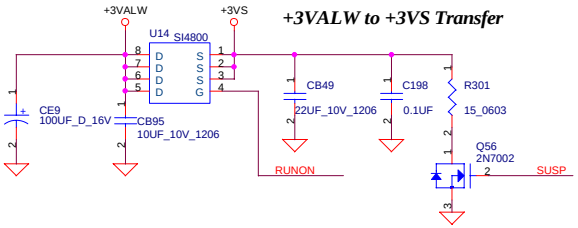


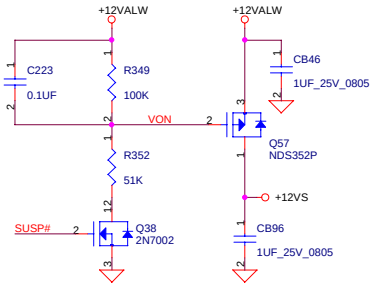
Compal Electronics, Inc.		
Title: POWER GOOD & PS2 Connector		
Size	Document Number: LA-1481 M/B	Rev: 0.5
Date: 星期三, 八月 14, 2002	Sheet 30 of 47	

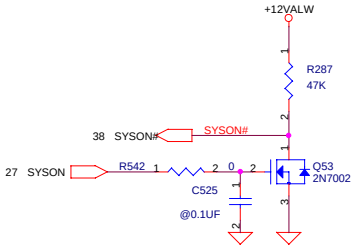


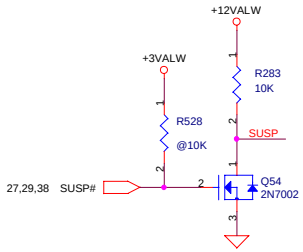












Compal Electronics, Inc.		
Title: DC/DC Circuits		
Size	Document Number: LA-1481 M/B	Rev: 0.3
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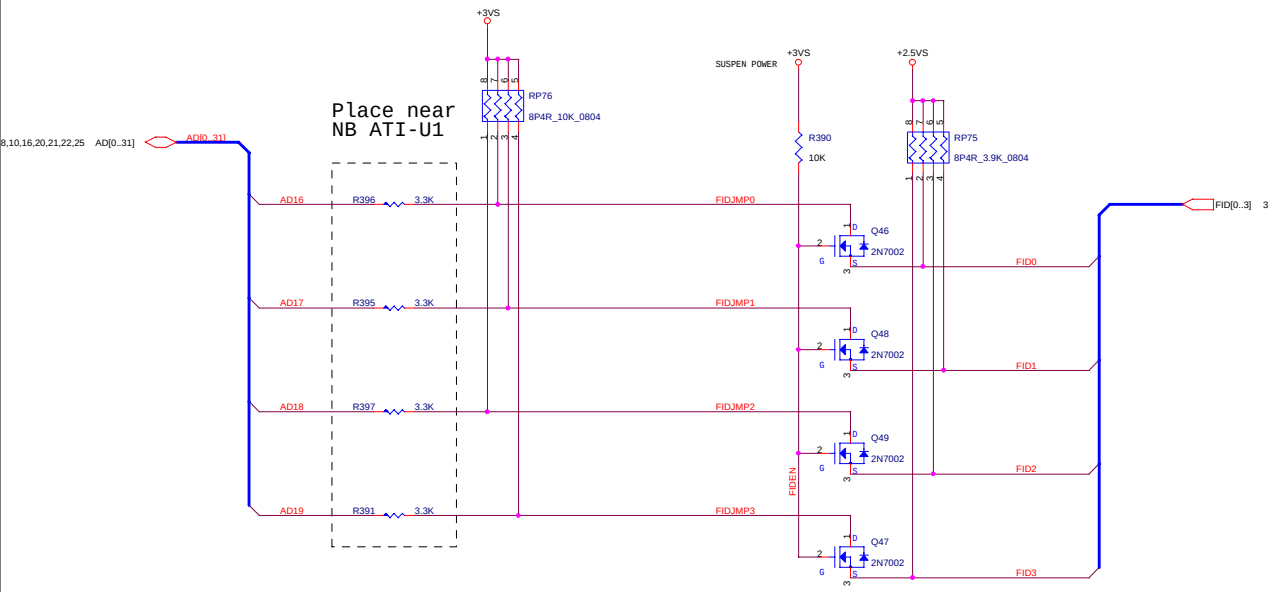
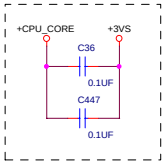
CPU FID ISOLATION



Decoupling Between Planes



ClkDiv[3] FID[3]	ClkDiv[2] FID[2]	ClkDiv[1] FID[1]	ClkDiv[0] FID[0]	Processor Clock and SYSCLK Frequency Ratio
0	0	0	0	11
0	0	0	1	11.5
0	0	1	0	12
0	0	1	1	12.5
0	1	0	0	5
0	1	0	1	5.5
0	1	1	0	6
0	1	1	1	6.5
1	0	0	0	7
1	0	0	1	7.5
1	0	1	0	8
1	0	1	1	8.5
1	1	0	0	9
1	1	0	1	9.5
1	1	1	0	10
1	1	1	1	10.5

WARNING: PRELIMINARY SCHEMATICS. FOR REFERENCE PURPOSES ONLY. DESIGN HAS NOT BEEN BUILT OR VERIFIED.

NOTE: All resistors are 5% 0603, and all capacitors are 10% 0603 unless otherwise noted.

Compal Electronics, Inc.

Title: **FID**

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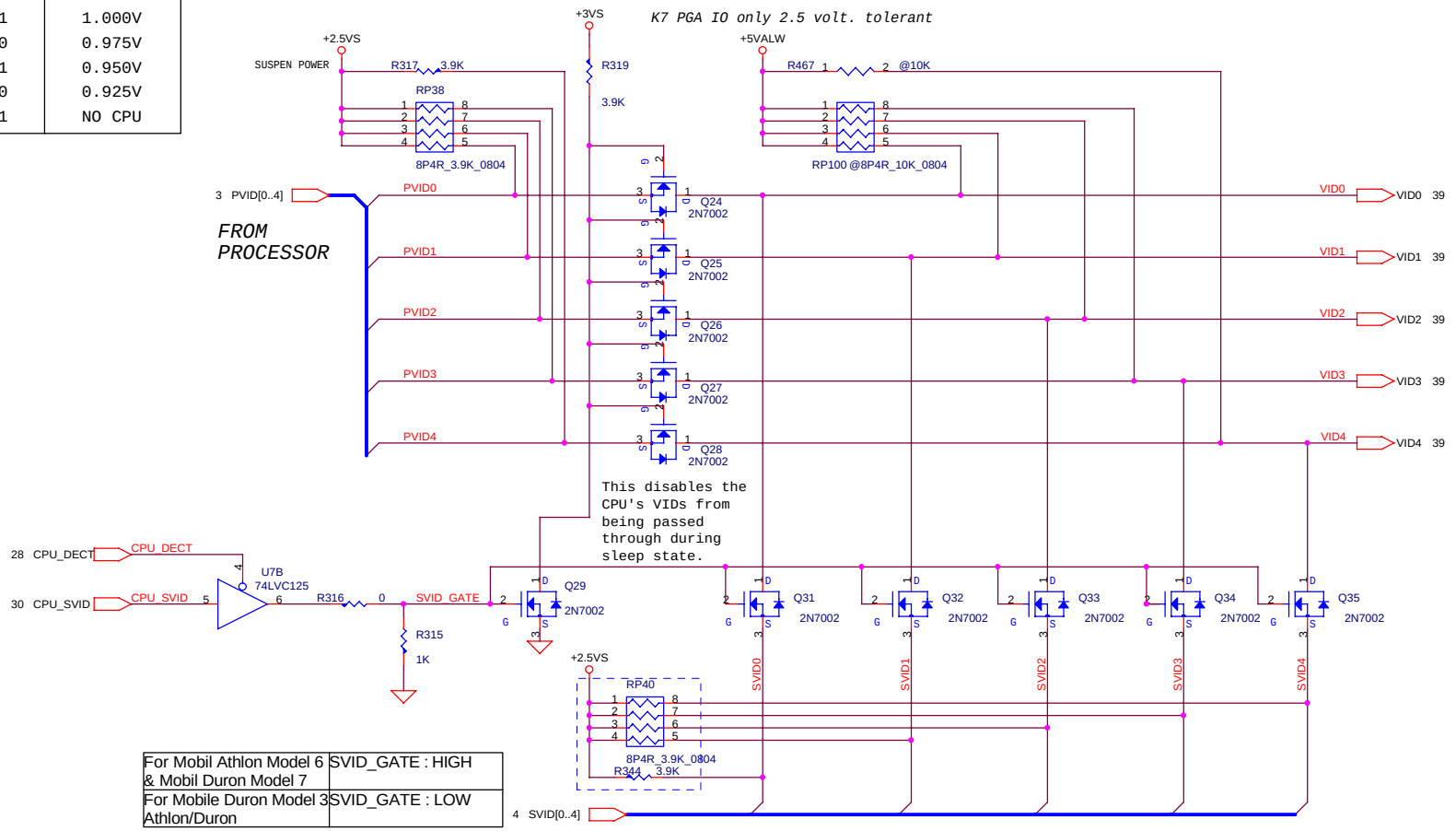
VID[4:0] Code to Voltage Definition

VID[4:0]	VCC_CORE(V)	VID[4:0]	VCC_CORE(V)
00000	2.000V	10000	1.275V
00001	1.950V	10001	1.250V
00010	1.900V	10010	1.225V
00011	1.850V	10011	1.200V
00100	1.800V	10100	1.175V
00101	1.750V	10101	1.150V
00110	1.700V	10110	1.125V
00111	1.650V	10111	1.100V
01000	1.600V	11000	1.075V
01001	1.550V	11001	1.050V
01010	1.500V	11010	1.025V
01011	1.450V	11011	1.000V
01100	1.400V	11100	0.975V
01101	1.350V	11101	0.950V
01110	1.300V	11110	0.925V
01111	NO CPU	11111	NO CPU



For Mobil Athlon Model 6 & Mobil Duron Model 7	SVID_GATE : HIGH
For Mobile Duron Model 3 Athlon/Duron	SVID_GATE : LOW

Compal Electronics, Inc.
Title: VID
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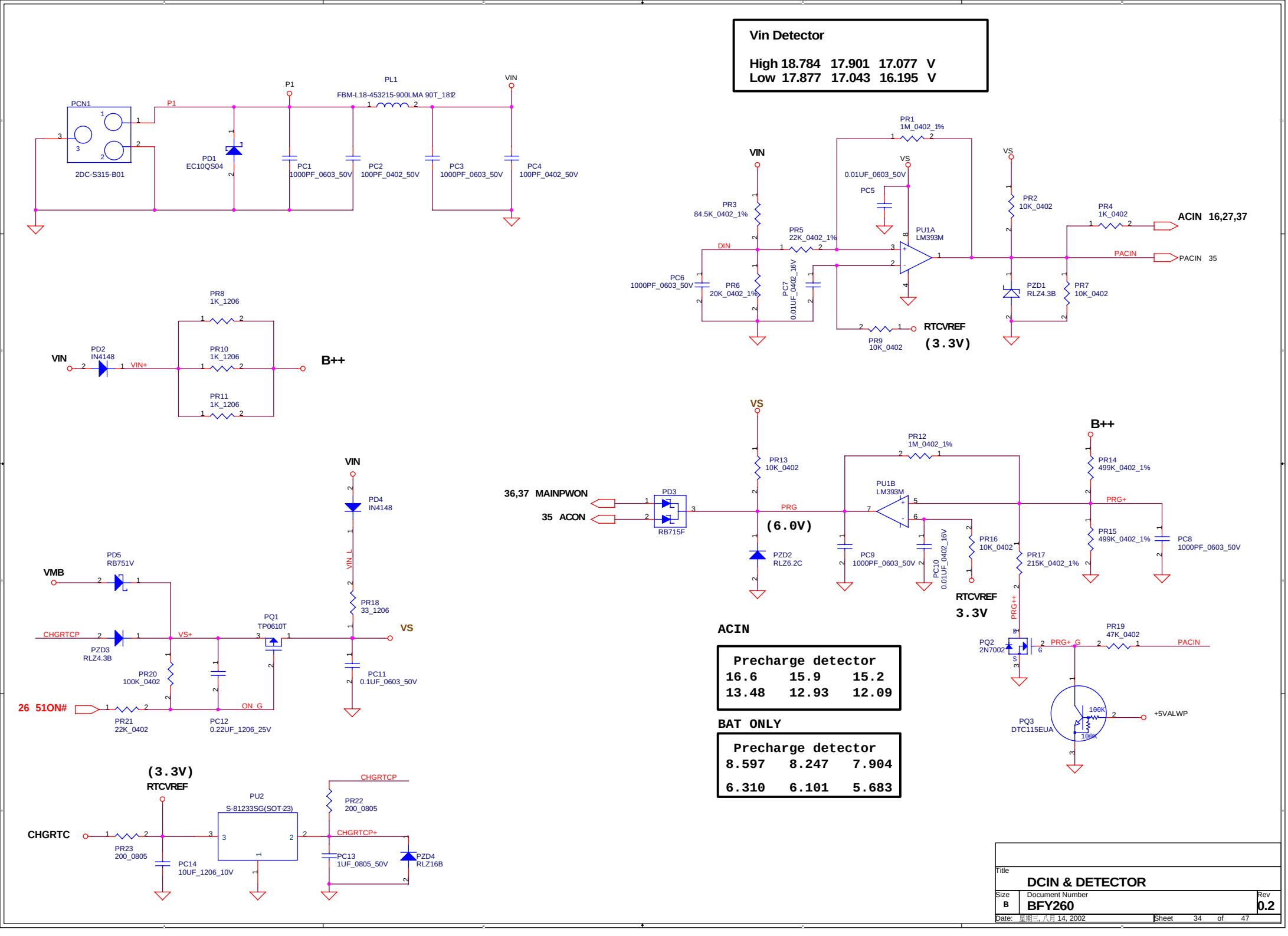
Vin Detector
High 18.784 17.901 17.077 V
Low 17.877 17.043 16.195 V
PCN1
2DC-S315-B01
PD1
EC10QS04
PC1
1000PF_0603_50V
PC2
100PF_0402_50V
PC3
1000PF_0603_50V
PC4
100PF_0402_50V
PL1
FBM-L18-453215-900LMA 90T_1812
P1
VIN
PR1
1M_0402_1%
PR2
10K_0402
PR3
84.5K_0402_1%
PR4
1K_0402
PR5
22K_0402_1%
PR6
20K_0402_1%
PR7
10K_0402
PR8
1K_1206
PR9
10K_0402
PR10
1K_1206
PR11
1K_1206
PR12
1M_0402_1%
PR13
10K_0402
PR14
499K_0402_1%
PR15
499K_0402_1%
PR16
10K_0402
PR17
215K_0402_1%
PR18
33_1206
PR19
47K_0402
PR20
100K_0402
PR21
22K_0402
PR22
200_0805
PR23
200_0805
PC5
0.01UF_0603_50V
PC6
1000PF_0603_50V
PC7
0.01UF_0402_16V
PC8
1000PF_0603_50V
PC9
1000PF_0603_50V
PC10
0.01UF_0402_16V
PC11
0.1UF_0603_50V
PC12
0.22UF_1206_25V
PC13
1UF_0805_50V
PC14
10UF_1206_10V
PD2
IN4148
PD3
RB715F
PD4
IN4148
PD5
RB751V
PU1A
LM393M
PU1B
LM393M
PU2
S-81233SG(SOT-23)
PZD1
RLZ4.3B
PZD2
RLZ6.2C
PZD3
RLZ4.3B
PZD4
RLZ16B
PQ1
TP0610T
PQ2
2N7002
PQ3
DTC115EUA
100K
DIN
PRG
PRG+
PRG++
PRG+_G
VS
VS+
VIN+
VIN_L
ON_G
CHGRTCP
CHGRTCP+
VMB
B++
ACIN 16,27,37
PACIN
PACIN 35
RTCVREF
(3.3V)
(6.0V)
36,37 MAINPWON
35 ACON
26 51ON#
CHGRTC
+5VALWP
ACIN
Precharge detector
16.6 15.9 15.2
13.48 12.93 12.09
BAT ONLY
Precharge detector
8.597 8.247 7.904
6.310 6.101 5.683
Title
DCIN & DETECTOR
Size
B
Document Number
BFY260
Rev
0.2
Date: 星期三, 八月 14, 2002
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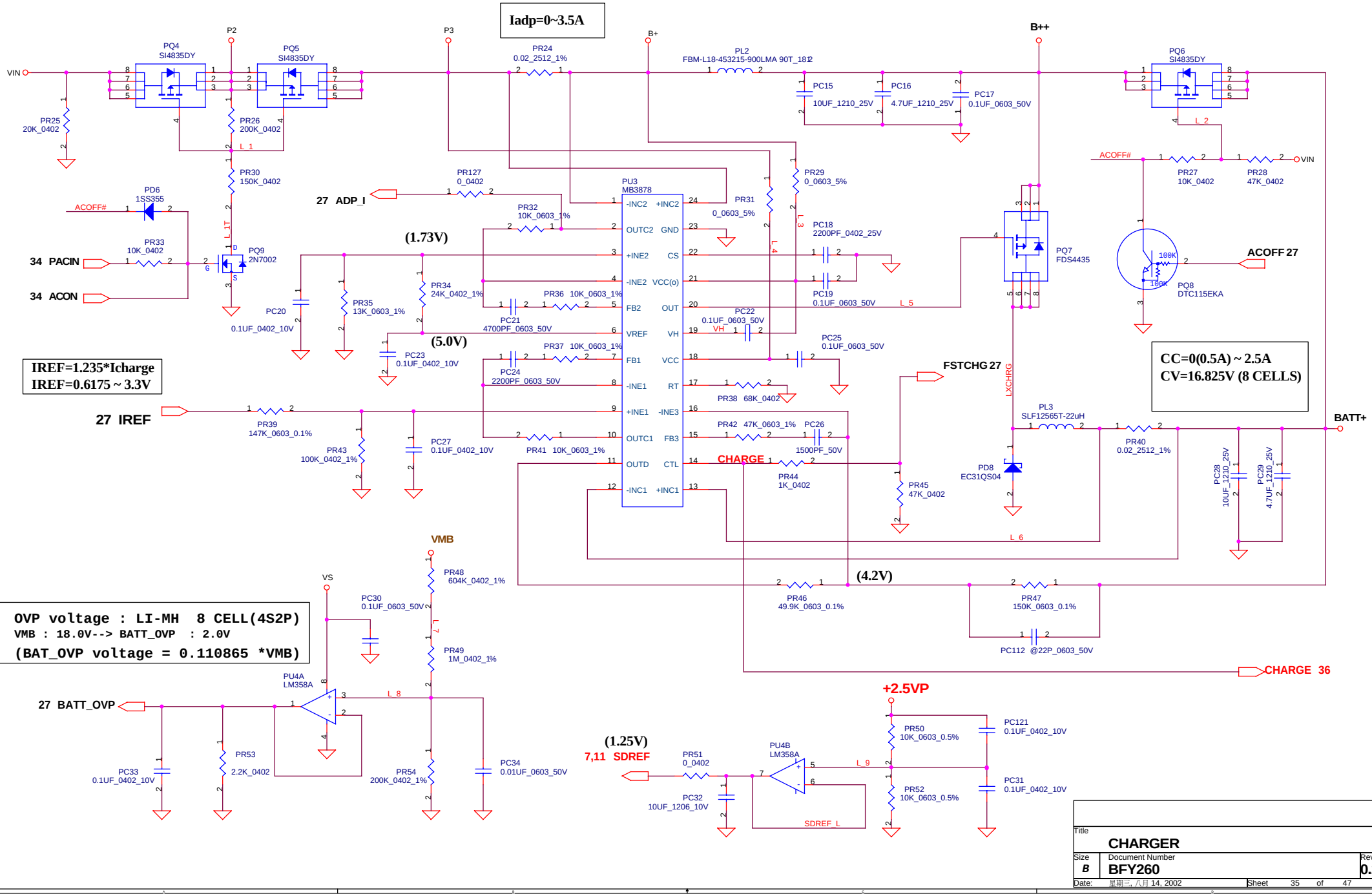
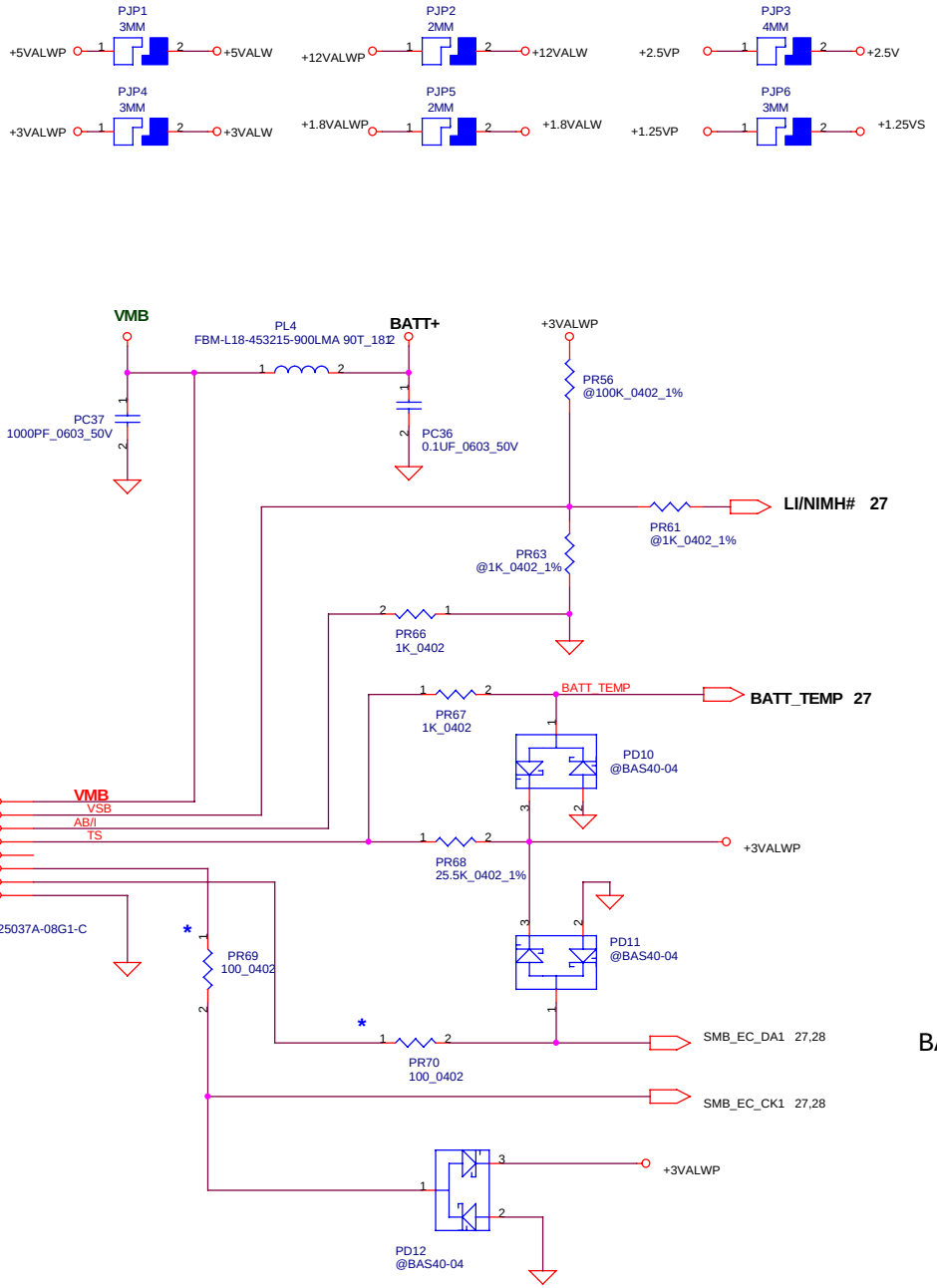
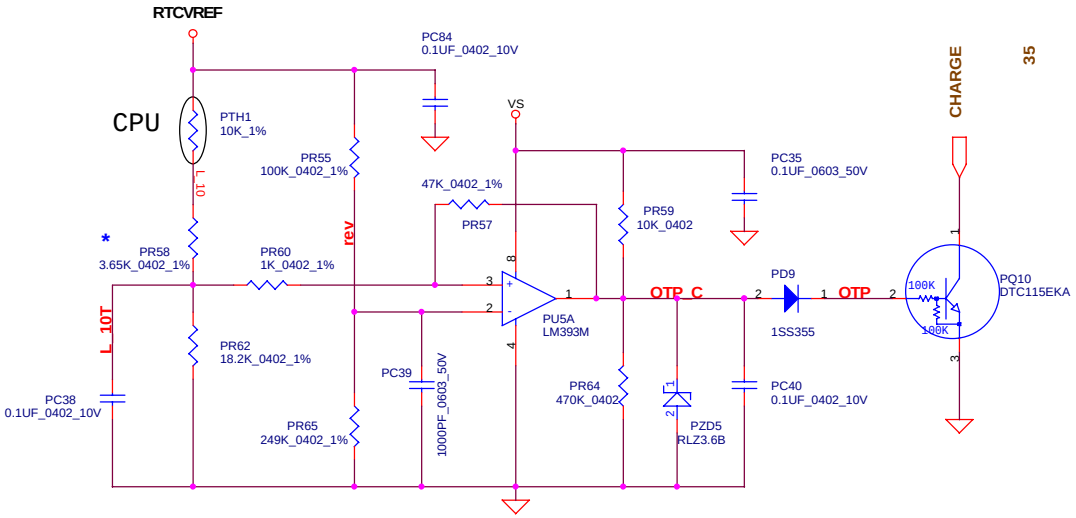


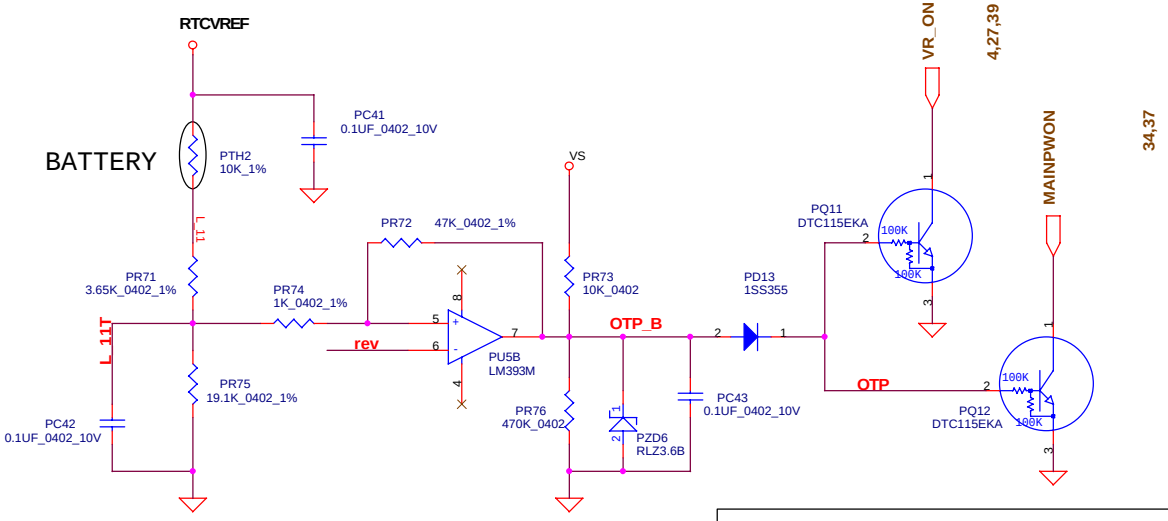
Title	CHARGER	
Size B	Document Number BFY260	Rev 0.2
Date: 星期三, 八月 14, 2002	Sheet 35 of 47	



PH1 under CPU botten side :
CPU thermal protection at 90(91)+-3 degree C
Recovery at 50(51)+-3 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 85(86)+-3 degree C
Recovery at 50(51) degree C



Title	BATTERY CONN / OTP	
Size B	Document Number BFY260	Rev 0.2
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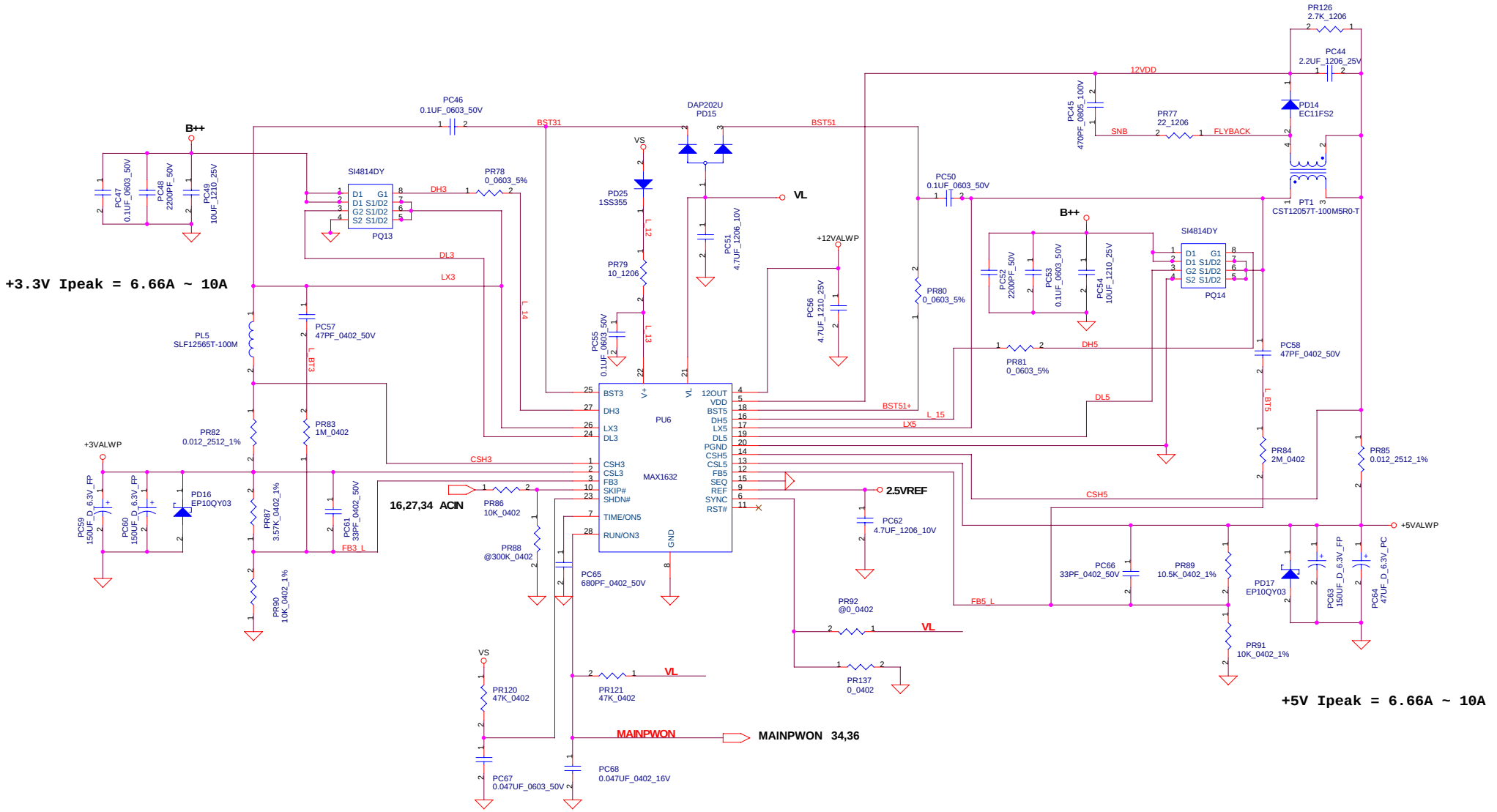

Title	3.3V / 5V / 12V	
Size	Document Number BFY260	Rev 0.2
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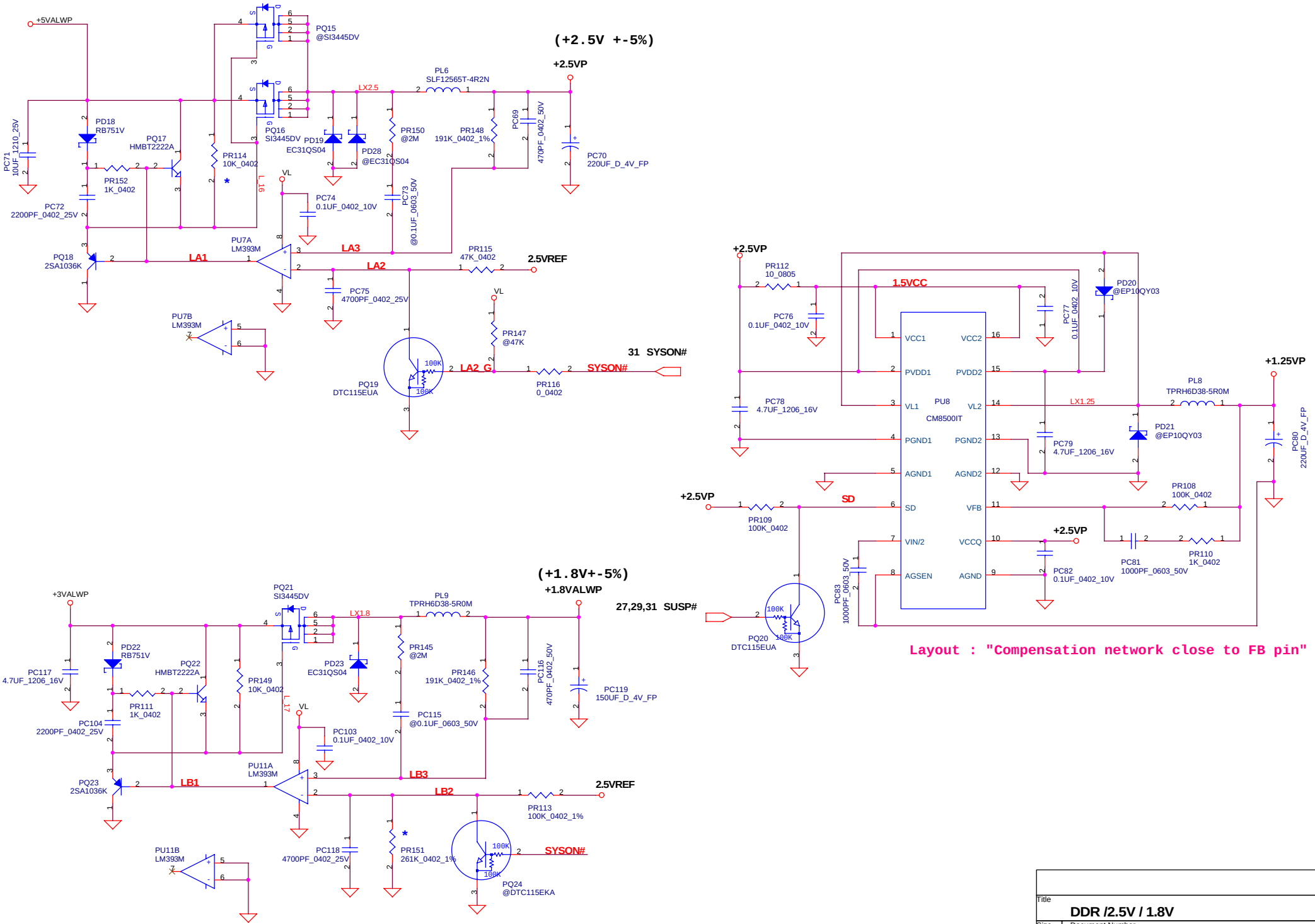
(+2.5V +-5%)
+5VALWP
+2.5VP
PQ15
@SI3445DV
PQ16
SI3445DV
PL6
SLF12565T-4R2N
LX2.5
PD18
RB751V
PQ17
HMBT2222A
PD19
EC31QS04
PD28
@EC31QS04
PR150
@2M
PR148
191K_0402_1%
PC69
470PF_0402_50V
PC70
220UF_D_4V_FP
PC71
10UF_1210_25V
PR114
10K_0402
PR152
1K_0402
PC72
2200PF_0402_25V
PC74
0.1UF_0402_10V
PC73
@0.1UF_0603_50V
PU7A
LM393M
PQ18
2SA1036K
LA1
LA2
LA3
PR115
47K_0402
2.5VREF
PC75
4700PF_0402_25V
PU7B
LM393M
PR147
@47K
PQ19
DTC115EUA
LA2_G
PR116
0_0402
31 SYSON#
SYSON#
(+1.8V+-5%)
+1.8VALWP
+3VALWP
PQ21
SI3445DV
PQ22
HMBT2222A
PD22
RB751V
PD23
EC31QS04
LX1.8
PL9
TPRH6D38-5R0M
PR145
@2M
PR146
191K_0402_1%
PC116
470PF_0402_50V
PC119
150UF_D_4V_FP
PC117
4.7UF_1206_16V
PR149
10K_0402
PR111
1K_0402
PC104
2200PF_0402_25V
PC115
@0.1UF_0603_50V
PC103
0.1UF_0402_10V
PU11A
LM393M
PQ23
2SA1036K
LB1
LB2
LB3
2.5VREF
PR113
100K_0402_1%
PU11B
LM393M
PC118
4700PF_0402_25V
PR151
261K_0402_1%
PQ24
@DTC115EKA
27,29,31 SUSP#
PR112
10_0805
PC76
0.1UF_0402_10V
1.5VCC
PD20
@EP10QY03
PC77
0.1UF_0402_10V
PU8
CM8500IT
VCC1
VCC2
PVDD1
PVDD2
VL1
VL2
PGND1
PGND2
AGND1
AGND2
SD
VFB
VIN/2
VCCQ
AGSEN
AGND
PC78
4.7UF_1206_16V
PC79
4.7UF_1206_16V
PD21
@EP10QY03
LX1.25
PL8
TPRH6D38-5R0M
+1.25VP
PC80
220UF_D_4V_FP
PR108
100K_0402
PR109
100K_0402
PC81
1000PF_0603_50V
PR110
1K_0402
PC82
0.1UF_0402_10V
PC83
1000PF_0603_50V
PQ20
DTC115EUA
Layout : "Compensation network close to FB pin"
Title
DDR /2.5V / 1.8V
Size
B
Document Number
BFY260
Rev
0.2
Date: 星期三, 八月 14, 2002
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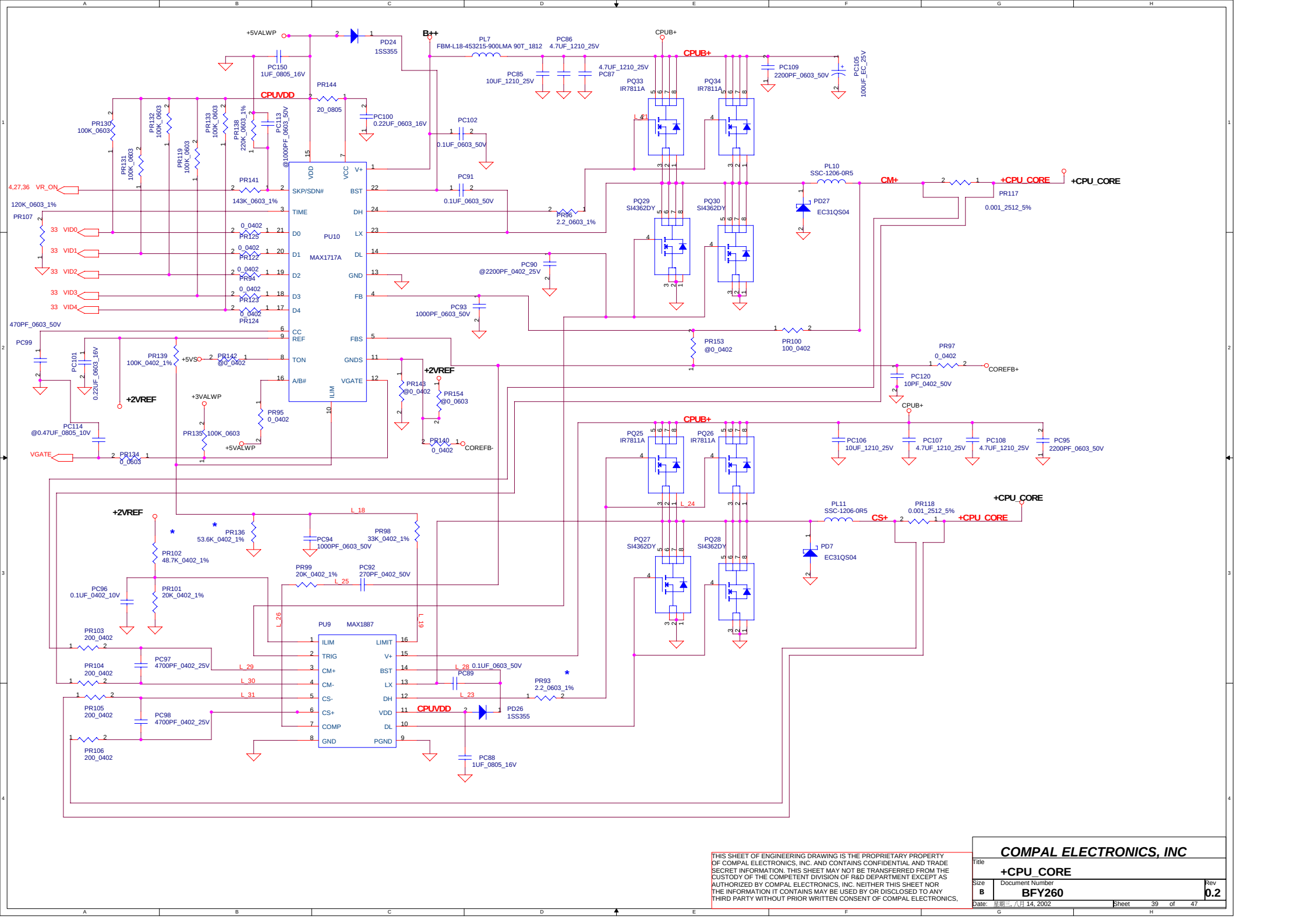

COMPAL ELECTRONICS, INC

Title: +CPU_CORE

Size: B | Document Number: BFY260 | Rev: 0.2

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Voltage Rails

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Power Plane	Description	S1	S3	S5	FUNCTION	RELATED POWER NET NAME
VIN	Adapter power supply (19V)	N/A	N/A	N/A	Pullhigh,Switch,DOCKING,VL,AC IN.	VIN+,VIN_L
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A	Pullhigh,Switch,B1+,PWR MB3887,PWR MAX1718,LCD INVERTER.	H,B++,P3,
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	Pullhigh,Switch,NB,CPU.	CS+,CM+,L_30,L_31
+3VALW	3.3V always on power rail	ON	ON	ON*	Pullhigh,Switch,PCMCIA CTRL,PCMCIA Switch,LAN	+3V_PCMCIA,S1_VCC,S2_VCC,+3VLAN(+VDD2.5,G),
+3VS	3.3V switched power rail	ON	OFF	OFF	Pullhigh,1394,NE1617,SM560,NB,DDR,CLK GEN,PID,	+3VA

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
LAN	AD20	3	PIRQB
CardBus_A SLOT	AD22	2	PIRQA
CardBus_B SLOT	AD22	2	PIRQA
Mini-PCI	AD27	1	PIRQB
Mini-PCI LAN	AD31	1	PIRQD
IEEE-1394 Controller	AD21	0	PIRQA

P.S:Default Resistor & Capacitor's package are 0402.
Default 8P4R package is 0402.

Power PIR

Item	Fixed Issue	Reason for change	Page	Modify item	MB_Ver.	Phase
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						
18						

Title	Power PIR	
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BCY26 A-TEST Modify <91.05.20.~91.06.27.

1.Modify the resistors' value for AMD recommend <Page 3> 91.05.22.
-Change R151,R157 from 10ohm to 10Kohm . (Modify CKT&BOM)

2.Modify the schematic for ATI DC_STOP# related <Page 6> 91.05.22.
-Change R210 from @1Kohm to 1Kohm . (Modify CKT&BOM)

3.Modify the Pull Low/High resistors' value to meet Compal rule <Page 17,18> 91.05.22.
-Change R122,R123,R164,R179,R266 from 10Kohm to 4.7Kohm . (Modify CKT&BOM)
-Change R239,R257 from @10Kohm to @4.7Kohm . (Modify CKT onl y)
-Change R142 from 100Kohm to 4.7Kohm . (Modify CKT&BOM)
-Change R165,R170 from @100Kohm to @4.7Kohm . (Modify CKT onl y)
-Change RP23 from 8P4R_10K_0804ohm to 8P4R_4.7K_0804ohm . (Modify CKT&BOM)
-Change R214 from 4.7Kohm to 10Kohm . (Modify CKT&BOM)

4.Modify the schematic for IDE related <Page 19> 91.05.22.
-Change D16 from RB751V to @RB751V . (Modify CKT&BOM)
-Change R101,R371 from 330ohm to 10Kohm . (Modify CKT&BOM)

5.Modify the material for shortage and layout size <Page 19> 91.05.24.
-Change R14 from 60_1%_0603 to 60.4_1%_0603 . (Modify CKT&BOM)
-Change R441,R442 from 60_1%_0603 to 60.4_1% . (Modify CKT&BOM)

A-TEST SMT BUILT

6.Correct CPU schematic <Page 4> 91.05.20.
-Connect U27.AM6 or U27.AE7 to GND . (Modify CKT& Layout)

7.Modify the schematic for PWRGD timing <Page 30> 91.05.29.
-Remove Q21(2N7002) , and then short Q21.1 and Q2 1.3 . (Modify CKT,BOM and Layout)

8.Modify the schematic for ATI strapping recommend <Page 10> 91.05.29.
-Change R43 from 10K_0603 to @10K_0603 . (Modify CKT&BO M)
-Change R67 from @10K_0603 to 10K_0603 . (Modify CKT&BO M)
-Change R433 from @10K_0603 to 10K_0603 . (Modify CKT&B OM)
-Change R434 from 10K_0603 to @10K_0603 . (Modify CKT&B OM)

9.Add the By-Pass Capacitors for improving CPUCLK differential signals <Page 13> 91.05.29.
-Change C197,C201 from @10PF to 10PF . (Modify CKT&BO M)

10.Add the By-Pass Capacitor to improve SDATAINVAL# layout length issue <Page 3> 91.05.29.
-Add a 20PF Capacitor between CPU socket(U27.AN33) and GND. (Mo dify CKT,BOM and Layout)

11.Modify the schematic for ENE (ENE has internal clock already)<Page 22> 91.05.29.
-Change R358 from 0ohm to @0ohm . (Modify CKT&BOM)

12.Modify the schematic for delay CPURST# timing (Change the signal issued from NB to SB) <Page 6,16> 91.05.29.
-Change R137 from 0ohm to @0ohm . (Modify CKT&BOM)
-Change R205 from @0ohm to 0ohm . (Modify CKT&BOM)

13.Change the value for powergood related<Page 30> 91.05.29.
-Change R224 from 10K_0603ohm to 20K_0603ohm . (Modify CKT&BOM)

14.Change the power source for ALI recommend . <Page 16> 91.06.01.
-Change R153.1's connection from +3VALW to +3VS . (Modi fy CKT&Layout)

15.Change the power source of DDCDATA/DDCCLK for ATI recommend . <Page 14> 91.06.01.
-Change R8.2 and R9.2's connection to Q1.1 and Q2.1 . (Modify CKT&Layout)
-Add R? and R? (2.2Kohm) from DDCDATA/CLK to +3VS . (Modify CKT,BOM and Lay out)
-Change R7 from 100K to 33ohm and connection from +12VS to +3VS . (Modify C KT,BOM and Layout)

16.Change the SUSP# and CLK GEN PWR_DWN# related schematic to improve the leakage issue . <Page 31,13> 91.06.03.
-Connect to +3VALW by adding R528 10Kohm . (Modify CKT,BOM and Layout)
-Change R322 from 0ohm to @0ohm . (Modify CKT&BOM)
-Change R321 from @10Kohm to 10Kohm . (Modify CKT&BOM)

~~**17.Modify LVDS_BLON# related schematic for LCD backlight issue . <Page 15,27> 91.06.03.**~~
~~-Disconnect U12.4 and LVDS_BLON# and then jump a wire from U12.4 to Q11.2 .~~
~~(Temp solution for A-TEST rework)~~

18.Modify the signal RUNON related schematic for ATI recommend power sequence (+1.8VS early to +3VS) . <Page 31> 91.06.03.
-Cut RUNON signal to C213.1 and then connect to +12VS by ad ding R529 10Kohm . (Modify CKT,BOM and Layout)

19.Modify the signal DC_STOP# related schematic for ATI recommend . <Page 6> 91.06.03.
-Change Q51 from 2N7002 to @2N7002 . (Modify CK T&BOM)
-Change R211 from 4.7Kohm to @4.7Kohm . (Modify CKT&BOM)

20.Modify the schematic for AMD recommend and layout improve . <Page 3,4> 91.06.07.
-Change R451 from 1Kohm to 510ohm . (Modify CKT&BOM)
-Add R530 75ohm between Q17.2 and the signal FERR . (Modi fy CKT,BOM and Layout)
-Add C518 1UF_0603 from VREF_SYS to +CPUCORE . (Modify CKT,BOM and Layout)
-Add C519 @1UF_0603 from VREF_SYS to GND . (Modify CKT&Layout)
-Add CB106 4.7UF_0805 from U27.AJ23(+VCCA2.5) to GND . (Modify CKT,BOM and Layout)
-Add C520 39PF from +VCCP2.5 to GND . (Modify CKT,BOM and Layout)
-Del Q50(@MMBT3904) . (Modify CKT,BOM and Layout)

21.Modify the schematic for the signal "LVDS_BLON#" related . <Page 9,27> 91.06.08.
-Change the netname from LVDS_BLON to LVDS_BLON# . (Modify CKT onl y)
-Add Q60(2N7002) and R531(10Kohm) pull high bet ween U3.D2 and LVDS_BLON# . (Modify CKT,BOM and Layout)

22.Cut the MVREF_DIM to MVREF_DIM1 and MVREF_DIM2 for ATI recommend . <Page 11> 91.06.08.
-Add the MVREF_DIM1 related schematic(R532,R533,R534,C521,C522,C523) . (Modify CKT,BOM and Layout)

23.Modify ISA pull high resistors' value . <Page 18> 91.06.08.
-Change RP36,RP26,RP34 from 10P8R_10K to 10P8R_47K . (Modify CKT,BOM and Layout)

24.Modify IDERST# related schematic . <Page 19> 91.06.08.
-Del D16,D17(RB751V) and then short the location . (Modify CKT, BOM and Layout)
-Disconnect U8.1 and U8.5 and then add R537 (10Kohm) from U8.5 to +5VS . (Modify CKT,BOM and Layout)

----PLEASE SEE NEXT PAGE

Compal Electronics, Inc.

Title	H/W2 EE Dept. PIR SHEET(1)	
Size	Document Number LA-1481 M/B	Rev 0.3
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BCY26 A-TEST Modify <91.05.20.~91.06.27.>

25.Modify PCLK_PCM related schematic . <Page 22,27> 91.06.08.
-Add the 2N7002 related schematic (add Q61,R538,R539) between the signal PCLK_PCM and U29.A10/R524.1 . (Modify CKT,BOM and L ayout)
-Del R199(@0ohm) and reconnect U12.165 to PCMCLKE . (Modify CKT,BOM and Layout)

26.Modify PM_CLKRUN# related schematic . <Page 22> 91.06.08.
-Add R543 (@0ohm) between U29.B15 and PM_CLKRUN# . (Modify CKT,BOM and Layout)

27.Modify PCM_SUSP# related schematic . <Page 22> 91.06.08.
-Del D35(RB751V) and then short the location . (Modify CKT, BOM and Layout)

28.Modify PWRGD related schematic . <Page 30> 91.06.08.
-Del U10(MAX809SEUR) . (Modify CKT,BOM and Layout)
~~-Add U31(7SH08) related schematic (Add R540,R541,C524) . (Modify CKT,BOM an d Layout)~~

29.Modify SYSON related schematic for 2.5V and 3V timing delay . <Page 31> 91.06.08.
-Add R542(0ohm) from SYSON to Q53.2 and add C525(@0.1UF) between Q53.2 and GND . (Modify CKT,BOM and Layout)

30.Modify CPU internal PLL power source related schematic . <Page 4> 91.06.08.
-Change U9 from SI9183BT-25 to SI9182DH-25 and the related sc hematic (Add C526,Del C164,C158) . (Modify CKT,BOM and Layo ut)

31.Modify SB Pull High/Low related schematic for ALI updated . <Page 17> 91.06.10.
-Add R545,R546,R547,R548(10Kohm) from U6.U3/R5/U2/T4 to +5VS . (Modify CKT,BOM and Layout)
-Add R544,R549(1Kohm) from U6.E4/Y5 to GND . (Modify CKT,BOM an d Layout)

32.Modify NB Pull Low resistors' value related schematic. <Page 10> 91.06.11.
-Change R62,R63,R65,R66,R67,R68,R71,R72,R73,R155R148,R161,R167,R175,R184,R427, R430,R432,R436,R438,R440 from 10K_0603 to 4.7K_0603 . (Modify CKT&BO M)
-Change R64,R69,R70,R194,R434 from @10K_0603 to @4.7K_0603 . (Modify CKT &BOM)

33.Modify LAN LED signals related schematic. <Page 20> 91.06.11.
-Change U21.80's connection from LED_YELP to LED2_YELN . (Modify CKT&Layout)
-Change U21.79's connection from LED1_GRNP to LED1_GRNN . (Modify CKT&Layo ut)
-Change R518.1's connection from LED2_YELN to LED2_YELP . (Modify CKT&Layout)
-Change R492.1's connection from LED1_GRNN to LED1_GRNP . (Modify CKT&Layo ut)

34.Modify NB Pull High/Low resistors' related schematic. <Page 10> 91.06.11.
-Change R160 from 10K_0603 to @10K_0603 . (Modify CKT&B OM)

35.Modify NB VDD related schematic. <Page 9> 91.06.11.
-Change R391,R395,R396,R397 from 1Kohm to 3.3Kohm . (Modify CKT&BOM)

36.Modify NB strap input related schematic. <Page 10> 91.06.12.
-Change R61 from 2.2K_0603 to 3.3K_0603 . (Modify CKT &BOM)
-Change R37 from 8.2K_0603 to 5.6K_0603 . (Modify CKT &BOM)

37.Modify VGATE related schematic . <Page 30> 91.06.12.
-Change R225 from 10K_0603 to @10K_0603 . (Modify CKT&B OM)

38.Modify CPU VID related schematic . <Page 33> 91.06.12.
-Change R467 from 10Kohm to @10Kohm . (Modify CKT&BOM)
-Change RP100 from 8P4R_10K_0804 to @8P4R_10K_0804 . (Modify CKT&BOM)

39.Modify VR_POK_1 timing related schematic . <Page 30> 91.06.12.
-Change C222 from 0.1UF_0603 to 0.047U F_0603 . (Modify CKT&BOM)

40.Modify RJ-45&11 related schematic for EMI recommend . <Page 25> 91.06.12.
-Change VH1 from DSSA-P3100SB to @DSSA-P3100SB . (Modify CKT&BOM)
-Connect LANGND and GND by add R550(0_0603ohm) . (Modify CKT,BOM an d Layout)

41.Modify BIOS FLASH# related schematic for Compal HW1 recommend . <Page 25> 91.06.12.
-Change R346 from 100Kohm to 1Kohm , and then change its connecti on from +12VS to SUS_STAT# . (Modify CKT,BOM and Layout)

42.Modify PWRGD related schematic . <Page 30> 91.06.08.
-Add U31(74LVC08) related schematic (Add C527,R551,R541) . (Modify CKT,BOM an d Layout)

43.Modify CPU Bypass Cap. related schematic for cost down . <Page 5> 91.06.14.
-Del CE13,CE14(220UF_D2_4V_25m) . (Modify CKT,BOM and Layout)
-Change CE3,CE16,CE7,CE5,CE11,CE6,CE12,CE15 from 220UF_D2_4V_25m to 330UF_D2_2.5V_15m . (Modify CKT&BOM)

44.Modify NB DC_STOP# related schematic after A-TEST verified . <Page 6> 91.06.14.
-Del DC_STOP# related schematic (Del R458,R459,R460,CB93,Q51,Q 52) . (Modify CKT,BOM and Layout)

45.Modify NB XTLOUT related schematic after A-TEST verified . <Page 9> 91.06.14.
-Del U3.A9(XTLOUT) related schematic (Del R28,X1,C54,C58,JOPEN3) . (Modify CKT,BOM and Layout)

46.Modify IRQ8# power source . <Page 17> 91.06.14.
-Change R186.2's connection from +5VALW to +3VALW . (Mo dify CKT&Layout)

47.Modify CODEC Connector's related schematic for FDD active LED function . <Page 24> 91.06.14.
-Change JP6.16 from AGND to GND . (Modify CKT &Layout)
-Change JP6.27 from LED2 to DRV_0# . (Modify CKT&Lay out)
-Add Q62(DTC124EK) . (Modify CKT,BOM and La yout)
-Change Q41 from 2N7002 to @2N7002 . (Modify CKT &BOM)
-Change Q42 from SI2304DS to @SI2304DS . (Modify CKT& BOM)
-Change R368 from 100Kohm to @100Kohm . (Modify CKT&BOM)

48.Modify JP8's library and related schematic for customer request . <Page 26> 91.06.14.
-Modify the JP8 Internal Keyboard's related schematic (Del Q43,R376,R362,R 375,R377,R378) . (Modify CKT,BOM and Layout)

49.Modify EC_SMD/EC_SMC related schematic . <Page 27> 91.06.14.
-Change RP42.7/RP42.8's connection from +5VALW to +3VS and RP42.5/ RP42.6 keep +5VALW still . (Modify CKT&Layout)

50.Modify CPU Thermal related schematic . <Page 3> 91.06.14.
-Add R552(150ohm) between +3VS and C377.1 . (Modif y CKT,BOM and Layout)
-Del Q50(@MMBT3904) . (Modify CKT,BOM and Layout)

51.Modify SMI# related schematic for noise issue . <Page 3> 91.06.14.
-Add C528(@560PF) between SMI# and GND . (Modif y CKT,BOM and Layout)

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BCY26 A-TEST Modify <91.05.20.~91.06.27.

52.Modify VR_POK related schematic . <Page 28,30> 91.06.14.

-Add the 2N7002 related schematic (add R553,Q63) b etween the signal VGATE and U31.2 . (Modify CKT,BOM and La yout)

-Add the net POK_EN from U23.12 to Q63.2 . (Mod ify CKT,BOM and Layout)

53.Modify MOD_AUDIO_MONR related schematic . <Page 24> 91.06.17.

-Change R363 from 20Kohm to 0ohm . (Modify CKT&BOM)

-Change R364 from 33Kohm to @33Kohm . (Modify CKT&BOM)

54.Modify USB ports' power source related schematic . <Page 29> 91.06.17.

-Del F7,F3,F4(@POLYSWITCH_0.75A) to +5VS . (Modify CKT,BO M and Layout)

-Change F2,F5,F6 from POLYSWITCH_0.75A to EVERFUSE_1.1A . (Modify CKT&BOM)

55.Modify RTC related schematic from IRQ8 to SIRQ . <Page 17> 91.06.17.

~~-Add R554(@0ohm) between RTC and IRQ8# . (Modi fy CKT,BOM and Layout)~~

~~-Change R186.2's connection from +3VALW to GND . (Modi fy CKT&Layout)~~

56.Modify SCI# related schematic from RUM_ENT1 to OFF_CDPWR . <Page 17> 91.06.17.

~~-Add R555(0ohm) between SCI# and OFFCDPWR . (Modify C KT,BOM and Layout)~~

~~-Change D18 from RB751V to @RB751V . (Modify CKT,BOM and La yout)~~

~~-Change R142 from 4.7Kohm to @4.7Kohm . (Modify CKT&BOM)~~

57.Change the SUSP# related schematic to improve the leakage issue by SW timing delay . <Page 31> 91.06.17.

-Change R528 from 10Kohm to @10Kohm . (Modify CKT&BOM)

58.Change the VGATE related schematic to avoid the power issue by power team . <Page 30>91.06.17.

-Change R553 from @0_0603ohm to 0_0603ohm . (Modify CKT&BOM)

-Change Q63 from 2N7002 to @2N7002 . (Modify CKT &BOM)

59.Change the ATI CAL related schematic for ATI updated . <Page 6>91.06.18.

-Change R14 from 60.4_1%_0603ohm to 30_1%_0603ohm . (Modify CKT&BOM)

60.Change the RJ45 jack related schematic for Safety team request . <Page 25>91.06.19.

-Change JP20.13,JP20.14(RJ-45 & RJ-11)'s connection fro m LANGND to NC . (Modify CKT&Layout)

-Change JP20.9,JP20.12(RJ-45 & RJ-11)'s connection from NC to LANGND . (Modify CKT&Layout)

61.Cancel modify RTC related schematic from IRQ8 to SIRQ action . <Page 17> 91.06.19.

-Del ~~R554(@0ohm)~~ , and then short RTC and IRQ8# directly . (Modif y CKT,BOM and Layout)

-Change R186.2's connection from GND to +5VALW . (Modi fy CKT&Layout)

62.Cancel modify SCI# related schematic from RUM_ENT1 to OFF_CDPWR action . <Page 17> 91.06.19.

-Del ~~R555(0ohm) b~~etween SCI# and OFFCDPWR . (Modify CKT, BOM and Layout)

-Change D18 from @RB751V to RB751V . (Modify CKT,BOM and La yout)

-Change R142 from @4.7Kohm to 4.7Kohm . (Modify CKT&BOM)

63.Modify ISA BUS pull high resistors' value for RTC related . <Page 18> 91.06.19.

-Change RP36,RP26,RP34 from 10P8R_47K to 10P8R_10K . (Modify CKT&BOM)

64.Modify RTC related schematic to fix the RTC fail isssue . <Page 17,18,24> 91.06.19.

~~-Change CB39 from 22UF_10V_1206 to 10UF_6.3V_1206 . (Modify CKT&BOM)~~

~~-Del Q15(MMBT3906),Q16(3904),R162(10Kohm),R156(51Kohm),R158(10Kohm) . (Modify CKT,BOM and Layout)~~

~~-Add RTC chip (U32,DS1685) related schematic(Add U32,C529,C530,C531,C532,R554, R555,R556,R557,R558,R559,R560,R561,R562,J3,J4,X8) . (Modify CKT,BOM an d Layout)~~

65.Modify ATI strap input related schematic for ATI updated . <Page 10> 91.06.19.

-Change R433 from 10K_0603 to @10K_0603 . (Modify CKT&B OM)

-Change R434 from @4.7K_0603 to 4.7K_0603 . (Modify C KT&BOM)

-Change R427 from 4.7K_0603 to 2.2K_0603 . (Modify CK T&BOM)

66.Modify ATI VDD related schematic . <Page 9> 91.06.19.

-Change L17,L18,L48 from BLM21A601SPT to HB-1M2012-121JT . (Modify CKT&BOM)

67.Modify ATI NB_VREFSYS related schematic for noise issue improved . <Page 6> 91.06.20.

-Change C140 from 0.047UF to 0.1UF . (Modify CKT& BOM)

-Add C533(0.1UF) between +CPU_CORE and NB_VREFSYS . (Modify CKT,BOM a nd Layout)

68.Del some +2.5VDD related CAP for cost down and free space . <Page 20> 91.06.20.

-Del C508(1000PF),C514 and C485(0.1UF) . (Modify CKT,BOM and Layout)

69.Modify RTC related schematic for ALI recommend . <Page 17,18,27> 91.06.21.

-Change RP8 from 8P4R_4.7K_0804 to @8P4R_4.7K_0804 . (Modify CKT&BOM)

-Change the net name from RTC to IRQ8# . (Modify CKT&Layout)

-Change R186 from 4.7Kohm to @4.7Kohm . (Modify CKT&BOM)

-Add Q15(MMBT3906),Q16(3904),R162,R156,R158 . (Modify CKT,BOM an d Layout)

-Add "@" mark to D38,U32,C529,R530,C531,C532,R554,R555,R558,R559,R556,R 557, R561,R562,R566,X8 for SMT no build in . (Modify CKT&BOM)

-Del RTC net to U12.23 . (Modify CKT&L ayout)

-Add R565(0ohm) between the net PC7 and IRQ8# . (Modify CKT,BOM and Layout)

-Change R325 from 100Kohm to 10Kohm . (Modify CKT&BOM)

70.Modify LREST1# related schematic for EC recommend . <Page 27> 91.06.21.

-Del Q30(@2N7002) . (Modify CKT&La yout)

71.Modify +3VS transfer related schematic . <Page 31> 91.06.21.

-Change R301 from 75ohm to 15_0603ohm . (Modify CKT,BOM and La yout)

72.Modify LAN power related schematic . <Page 20> 91.06.21.

-Change L51,L52 from 4.7UH_80mA to 0_0805ohm . (Modify CKT&BOM)

73.Modify RTC related schematic for SW team request . <Page 18> 91.06.24.

-Add R567(@0ohm) between U32.13 and U17.8 . (Modify CKT&Layout)

-Del "@" mark to D38,U32,C529,R530,C531,C532,R555,R558,R559,R556,R557,R561,R562,X8 for SMT no build in . (Modify CKT&BOM)

-Exchange J3 and R555's location and connection . (Modif y CKT&Layout)

-Change CB39 from 22UF_10V_1206 to 10UF_6.3V_1206 . (Modify CKT&BOM)

74.Modify AC97 Codec related schematic for EMI team request . <Page 13> 91.06.24.

-Change C181 from @10PF to 1000PF . (Modify CKT&BO M)

-Change R278 from 22ohm to 0ohm . (Modify CKT&BOM)

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75.Modify CLK GEN VDD related schematic for EMI team request to improve 400MHz noise . <Page 13> 91.06.24.

-Change JOPEN4(Short) to L53(HB-1M2012-121JT) . (Modify CKT,BO M and Layout)

76.Modify VREF_SYS related schematic for ATI recommend . <Page 3> 91.06.25.

-Change C149 from 0.01UF to 0.047UF . (Modify CKT&B OM)

77.Modify S2K_VREF related schematic for ATI recommend . <Page 6> 91.06.25.

-Change R149,R150 from 100_1%ohm to 60.4_1%ohm . (Modify CKT&BOM)

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BFY26 B-TEST Modify <91.06.27.~91.07.29.

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78.Modify VREF_SYS related schematic for noise improved . <Page 3> 91.06.25.

-Change C519 from @1UF_0603 to 1UF_0603 . (Modify CKT&BOM)

79.Modify CPU LCL related schematic for timing delay improved . <Page 3> 91.06.25.

-Change C40 from 5PF to @5PF . (Modify CKT&BO M)

80.Modify EC PCMCLKE related schematic for EC team request . <Page 27> 91.06.26.

-Change U12.36's connection from LED2 to PCMCLKE . (Modify CKT&Layout)

-Change U12.165's connection from PCMCLKE to PCRST# and add R199(0ohm) be tween them . (Modify CKT,BOM and Layout)

81.Modify Serial Port related schematic for CAP size. <Page 29> 91.06.26.

-Change C331 from 0.1UF to 0.1UF_0805 . (Modify CKT,BOM and Layout)

82.Modify VR_POK related schematic. <Page 30> 91.06.26.

-Change R225 from @10K_0603 to 10K_0603 . (Modify CKT&B OM)

-Change R553 from 0_0603 to @0_0603 . (Modify CKT &BOM)

-Change Q63 from @2N7002 to 2N7002 . (Modify CK T&BOM)

83.Modify CLK GEN related schematic for CAP removed because layout improve the timing issue . <Page 13> 91.06.27.

-Change C201 and C197 from 10PF to @10PF . (Modify CKT& BOM)

84.Modify LVDS spread spectrum chip (SM560) related schematic . <Page 8> 91.06.27.

-Change R400 from @0ohm to SS@10Kohm . (Modify CKT&BOM)

-Change R10 from SS@10ohm to @10ohm . (Modify CKT&BOM)

-Change C21 from SS@22PF to @22PF . (Modify CKT&BOM)

85.Modify CLK GEN related schematic for AC97 Codec clock signal disable . <Page 13> 91.06.27.

-Change R278 from 0ohm to @22ohm . (Modify CKT&BOM)

-Change C181 from 1000PF to @10PF . (Modify CKT&BO M)

86.Modify Crystal CAP value for internal review . <Page 13> 91.06.27.

-Change C180 and C186 from 10PF to 12PF . (Modify CKT&B OM)

87.Modify SODIMM2 CAP for cost down . <Page 7> 91.06.27.

-Change C230 from 150UF_D2_6.3V to @150UF_D2_6.3V . (Modify CKT&BOM)

88.Modify CRT connector related schematic . <Page 14> 91.06.27.

-Change R7 from 33ohm to 0ohm . (Modify CKT&BOM)

89.Modify Crystal CAP value for internal review . <Page 17> 91.06.27.

-Change C130 and C113 from 10PF to 12PF . (Modify CKT&B OM)

90.Modify PCLK_PCM related schematic . <Page 22> 91.06.27.

-Change R538 from 10Kohm to 100Kohm . (Modify CKT&BOM)

91.Modify BD_ID setting related schematic . <Page 27> 91.06.27.

-Change R343,R250,R268 from 10Kohm to @10Kohm . (Modify CKT&BOM)

92.Modify CAP value for cost down . <Page 6,7,8,13,20,21,25> 91.06.28.

-Change CB20,CB42,CB16,CB92,CB7,CB90,CB91,CB43,CB44,CB82 from 22U_10V_1206 to 10U_10V_1206 . (Modify CKT&BOM)

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93.Modify Spread Spectrum for Pin Define Error on S0/S1 . <Page 8> 91.07.03.

-Change R400 from SS@10Kohm to @10Kohm . (Modify CKT&BOM)

-Change R385 from @10Kohm to SS@10Kohm . (Modify CKT&BOM)

***Must modify schematic and layout when C-TEST .**

94.Modify Crystal PPM value because of RTC function . <Page 18> 91.07.03.

-Change X8 from 32.768KHZ to 32.768KHZ_10PPM . (Modify CKT&BOM)

95.Modify +RTCVCC power source related schematic . <Page 18> 91.07.03.

-Change D38 from RB751V to @RB751V . (Modify CKT&BOM)

96.Modify IDE connector related schematic . <Page 19> 91.07.03.

-Change R369,R20 from 10Kohm to @10Kohm . (Modify CKT&BOM)

-Change R373,R247 from @100Kohm to 100Kohm . (Modify CKT&BOM)

97.Modify DDR related resistors' value for ATI recommend . <Page 12> 91.07.17.

-Change R359,R360,R361,R501,R502,R503,R506,R507,R508 from 33ohm to 56ohm . (Modify CKT&BOM)

-Change RP63,RP64,RP65 from 33ohm_8P4R_0804 to 56ohm_8P4R_0804 . (Modify CKT&BOM)

98.Modify VREF_SYS related schematic to improve the noise issue for ATI recommend . <Page 3> 91.07.18.

-Change C518 from 1UF_0603 to 0.047UF_0603 . (Modify CKT&BOM)

-Change C519 from 1UF_0603 to @1UF_0603 . (Modify CKT&BOM)

-Change C147 from 0.1UF to @0.1UF . (Modify CKT &BOM)

99.Modify NB_VREFSYS related schematic to improve the noise issue for ATI recommend . <Page 6> 91.07.18.

-Change C533,C140 from 0.1UF to 0.047UF . (Modify CKT&B OM)

100.Modify SDCLK_NB_EXT related schematic to improve the clock quality for ATI recommend . <Page 9,13> 91.07.18.

-Change C346 from 100PF to @100PF . (Modify CKT&BO M)

-Change R294 from 22ohm to 10ohm . (Modify CKT&BOM)

101.Modify LCD_DIGON related schematic to fix the white screen issue temporary . <Page 9> 91.07.22.

-Change R531 from 10Kohm to @10Kohm . (Modify CKT&BOM)

-Change Q60 from 2N7002 to @2N7002 . (Modify CK T&BOM)

-Jump a wire from U3.D1 to Q60.1 . (REWORK)

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102.Modify CPUCLK related schematic for quality improved . <Page 13> 91.07.22.

~~-Change C201,C197 from @10PF to 5PF_0.25% . (Modify CK T and BOM)~~

103.Modify +RTCVCC related schematic to fix the power source issue temporary . <Page 27> 91.07.22.

~~-Del R345(0ohm_0603) and jump a wire from R345.1 to D10.1 . (Modif y BOM and REWORK)~~

104.Modify PWRGD related schematic for B-TEST improved temporary . <Page 30> 91.07.22.

~~-Jump the Q20.1's pin and connect Q20 .1's pin to R224.1 . (REWORK)~~

~~**B-TEST BOM EN2 RELEASE**~~

105.Correct SPECTRUM IC OrCAD library . <Page 8> 91.07.22.

-Change Pin7's define from S1 to S0 .

-Change Pin6's define from S0 to S1 .

106.Modify LCD_DIGON related schematic to fix the white screen issue temporary . <Page 9,15,27> 91.07.22.

-Change Q60 from @2N7002 to 2N7002 . (Modify CK T&BOM)

-Cancel the wire from U3.D1 to Q60.1 . (REWORK)

-Del R531 and redefine the Q60's related connection . (Modify CKT,BOM and Layout)

-Change U12.4's connection from LVDS_BLON# to LCD_DIGON . (Modify CK T&Layout)

107.Modify HDD related schematic for C-TEST improve . <Page 19> 91.07.23.

-Change JP9.44's connection from +5VS to NC . (Modify CKT&Layout)

108.Modify ENE CardBus Ctrl IC related schematic for new version phase in prepared . <Page 22> 91.07.23.

-Add R568(0ohm) between Q61.3 and Q61.1 . (Modify CKT,BOM and Layout)

-Change R538 from 100Kohm to @100Kohm . (Modify CKT&BOM)

-Change Q61 from 2N7002 to @2N7002 . (Modify CK T&BOM)

-Change R539 from 10Kohm to @10Kohm . (Modify CKT&BOM)

109.Modify CPUCLK related CAP value for quality improved . <Page 13> 91.07.23.

~~-Change C201,C197 from 5PF_0.25% to 10PF . (Modify CKT& BOM)~~

110.Modify SDCLK_NB_EXT damping resistor's value for quality improved . <Page 13> 91.07.23.

-Change R282 from 51ohm to 39ohm . (Modify CKT& BOM)

111.Del REFCLK0_AC97 related signal net on M/B for EMI request . <Page 13,24> 91.07.23.

-Del R278(@22ohm) and C181(@10PF) . (Modify CKT&Laout)

-Del REFCLK0_AC97 related signal net on M/B . (Modify CKT and Layout)

112.Modify modem related schematic for EMI request . <Page 25> 91.07.23.

-Change C445,C449 from 220PF_3KV_1808 to @220PF_3KV_1808 . (Modify CKT and BOM)

113.Modify +RTCVCC related schematic to fix the power source issue . <Page 27> 91.07.23.

-Add D39(RB751V) between U12.161 and K . (Modi fy CKT,BOM and Layout)

-Change R345 from 0ohm_0603 to @0ohm_0603 . (Modify CKT and BO M)

114.Modify ADP_I related schematic for clear . <Page 27> 91.07.23.

~~-Del ADP_I related signal net on M/B . (Modify CKT and Layout)~~

~~-Del R233(@2Mohm_0603) and C169(@0.22UF_0603) . (Modify CKT and Lay out)~~

115.Modify ALi Chip PCIRST# related schematic for voltage leakage issue fix . <Page 16> 91.07.23.

-Change the part from U31D(74LVC08) to U5(7SH08) and modify the r elated net connection . (Modify CKT,BOM and Layout)

116.Modify PWRGD related schematic to make time delay meet spec. . <Page 13,30> 91.07.23.

-Del U31(74LVC08),R553(@0_0603),R223(@10K),R227(4.7K),C527(1UF_0603),R224(20K _0603), C167(1UF_0603),R551(10K),R540(20K),C524(1UF_0603),R541(10K),R3 22(@0) ;
add U33(74LVC14),R576,R577(10K_0603),C537,C538(0.047UF_0603),Q64,Q65(MMBT2222A), R569,R572(4.7K_0603),C534,C535,C536(0.47UF_0603),R573,R574(20K_06 03), R570,R571,R575(47_0603) and modify the related net connection . (Modify CK T,BOM and Layout)

~~**117.Modify FERR related resistor's value . <Page 3> 91.07.23.**~~

~~-Change R530 from 75ohm to 33ohm . (Modify CKT and BOM)~~

118.Modify AMD_CPU_EMI_CLIP 's library for SMT process when C-TEST . <Page 5> 91.07.23.

-Left PT2,PT3,PT4,PT5 only and update their PCBFootPrint and library . (Modif y CKT,BOM and Layout)

119.Add TEST_CHIP on TOP/BOTTOM side for test on C-TEST . <Page 18> 91.07.23.

-Add U34,U35(TEST_CHIP) ON TOP/BOTTOM SIDE . (Modify CKT&Layou t)

120.Modify CPUCLK related schematic for quality improved . <Page 13> 91.07.24.

-Change C201,C197 from 10PF to 5PF_0.25% . (Modify CKT and BOM)

121.Add J5 for CMOS reflash used . <Page 27> 91.07.24.

-Add J5 between K to GND . (Modify CKT&Layout)

122.Del the net 1394_PME# because the function disable . <Page 21> 91.07.24.

-Del the signal net 1394_PME# from U2.37 . (Modify CKT&Layou t)

123.Modify ATI NB chip CAL related schematic for ATI recommend . <Page 6> 91.07.25.

-Add C539,C540(0.01UF) from U3.A16 and U3.B16 to GND . (Modify CKT, BOM and Layout)

124.Modify FERR related resistor's value . <Page 3> 91.07.25.

-Change R530 from 33ohm to 75ohm . (Modify CKT and BOM)

125.Modify PWRGD related schematic to make time delay meet spec. . <Page 30> 91.07.25.

-Modify Q20 and Q39 related connection . (Mod ify CKT and Layout)

-Del R570(47ohm_0603),R347(10Kohm),Q37(DTC124EK) . (Modify CKT,BOM and Layout)

126.Add some CAP for SB quality . <Page 16> 91.07.25.

-Add C541,C542,C543,C544(0.1UF) between +3VS and GND . (Mo dify CKT,BOM and Layout)

-Add C545,C546(0.1UF) between +5VS and GND . (Mo dify CKT,BOM and Layout)

127.Add ADP_I related schematic for Power team request . <Page 27> 91.07.25.

-Add ADP_I related signal net on M/B . (Modify CKT a nd Layout)

-Add R233(2Mohm_0603) and C169(0.22UF_0603) . (Modify CKT and La yout)

128.Del CPU socket related test point related to avoid power noise coupling . <Page 3> 91.07.26.

-Del TP6,TP7,TP8 . (Modify CKT&Layout)

129.Modify MVREF_DIM2 related resistors' size for layout space . <Page 11> 91.07.26.

-Change R464,R466 from @1K_1%_0603 to @1K_1% . (Modify CKT, BOM and Layout)

-Change R465 from 0ohm_0603 to 0ohm . (Modify CKT,BOM and La yout)

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BFY26 B-TEST Modify <91.06.27.~91.07.29.

130.Modify SADDINCLK# related schematic for Jason request . <Page 3> 91.07.29.
-Change L20,L21 from NL252018T-010J to 0ohm_0805 . (Modify CKT and BOM)

131.Modify NB Clock Termination related schematic to meet chip loading timing with CPU . <Page 9> 91.07.29.
-Change R401,R402,R411,R407 from 10ohm to @10ohm . (Modify CKT and BO M)

132.Modify Power Good related schematic to meet timing request . <Page 30> 91.07.30.
-Change R216's connection from +2.5V to +2.5VS . (Mo dify CKT&Layout)
-Change R216 from 4.7Kohm to 1Kohm . (Modify CKT&BOM)
-Add R579(47Kohm) between NB_PWRGD and GND . (Modify CK T,BOM and Layout)
-Add R578(10Kohm) between PWRGD and GND . (Modify CKT,BOM and Layout)

133.Modify SB related schematic for power source . <Page 16> 91.07.30.
-Change U5.5s connection from +3VS to +3VALW . (Mod ify CKT&Layout)

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134.Modify Power Good related schematic to meet timing request . <Page 30> 91.07.30.
-Del R224(20Kohm_0603) and R225(10Kohm_0603) . (Modify CKT,BOM and Layout)

135.Modify EC_PCLK by-pass CAP. related for PCICLK timing delay . <Page 13> 91.08.09.
-Change C208 from @10PF to 27PF . (Modify CKT a nd BOM)

136.Add PCIRST# by-pass CAP. . <Page 16> 91.08.09.
-Add C547(100PF) between PCIRST# and GND . (Modify CKT,BOM and Layout)

137.Correct Q63(2N7002)'s connection . <Page 30> 91.08.09.
-Change Q63.1's connection from GND to R569.2 . (M odify CKT&Layout)
-Change Q63.3's connection from R569.2 to GND . (M odify CKT&Layout)

138.Del the net 1394_PME# for schematic clear . <Page 28> 91.08.09.
-Del the net 1394_PME# . (Modify CKT&Layou t)

139.Modify +2.5_A's by-pass CAP. for material saving . <Page 4> 91.08.09.
-Change C152 from 4.7UF_10V_0805 to @4.7UF_10V_0805 . (Modify CKT an d BOM)

140.Modify LED_YELP and LED1_GRNP's resistor value for SED request . <Page 20> 91.08.09.
-Change R518,R492 from 200ohm_0603 to 560ohm_0603 . (Modify CKT and BOM)

141.Modify External RTC related schematic for the function removed . <Page 18,27> 91.08.09.
-Change U32 from DS1685 to @DS1685 . (Modify CKT and BOM)
-Change X8 from 32.768KHZ_10PPM to @32.768KHZ_10PPM . (Modify CKT and BOM)
-Change D39 from RB751V to @RB751V . (Modify CKT and BO M)
-Change R345 from @0_0603 to 0_0603 . (Modify CK T and BOM)

142.Modify FSB_100/133# related schematic for the function removed . <Page 10,13> 91.08.11.
-Change R334 from 8.2Kohm to @8.2Kohm . (Modify CKT and BOM)
-Change Q3,Q4,Q5,Q6 from 2N7002 to @2N7002 . (Modify CKT and BOM)
-Change R3 from 100Kohm to @100Kohm . (Modify CKT and BOM)
-Change R4,R12 from 10Kohm to @10Kohm . (Modify CKT and BOM)

143.Change REFCLK1_NB voltage level from +3.3V to +1.8V to meet ATI's SPEC . <Page 13> 91.08.11.
-Change R272 from 33ohm to 75ohm . (Modify CKT and BOM)
-Change C172 from @10PF to 100ohm . (Modify CKT and BOM)<Next versi on will relayout to fix that>

144.Modify +RTCVCC related schematic for clear . <Page 18> 91.08.11.
-Change Q15 from MMBT3906 to @MMBT3906 . (Modify CKT and BOM)
-Change Q16 from 3904 to @3904 . (Modif y CKT and BOM)
-Change D38 from @RB751V to RB751V . (Modify CKT and BO M)
-Change R158,R162 from 10K to @10K . (Modify CKT a nd BOM)
-Change R156 from 51K to @51K . (Modify CKT and BOM)

145.Modify DDR related schematic for quality improved . <Page 7,11,12> 91.08.12.
-Change R279,R285,R464 from @1K_1% to 1K_1% . (Modify CK T and BOM)
-Change R280,R533 from 0ohm_0603 to @0ohm_0603 . (Modify CKT and BO M)
-Change R465 from 0ohm to @0ohm . (Modify CKT and B OM)
-Change R466 from @1Kohm_1% to 866ohm_1% . (Modify CKT and B OM)
-Change R534 from @1Kohm_1%_0603 to 866ohm_1%_0603 . (Modify CKT and B OM)
-Change R532 from @1K_1%_0603 to 1K_1%_0603 . (Modify CK T and BOM)
-Change C235,C236,C237,C238,C239,C240,C245,C246,C247,C248,C258,C259,C260,C261,C262, C263,C264,C265,C266,C267,C268,C269,C270 from 47PF to @47PF . (Modify CKT and BOM)

146.Modify ENE CB1420 related schematic for ENE recommend . <Page 22> 91.08.12.
-Change R479,R480,R485,R489 from 22Kohm to @22Kohm . (Modify CKT and BOM)

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