

MODEL NAME : *PAP00*

PCB NO : *LA-6961P (DA*****)*

BOM P/N : *TBD*

<http://hobi-elektronika.net>

Dell/Compal Confidential

Schematic Document

Phantom (Huron River)

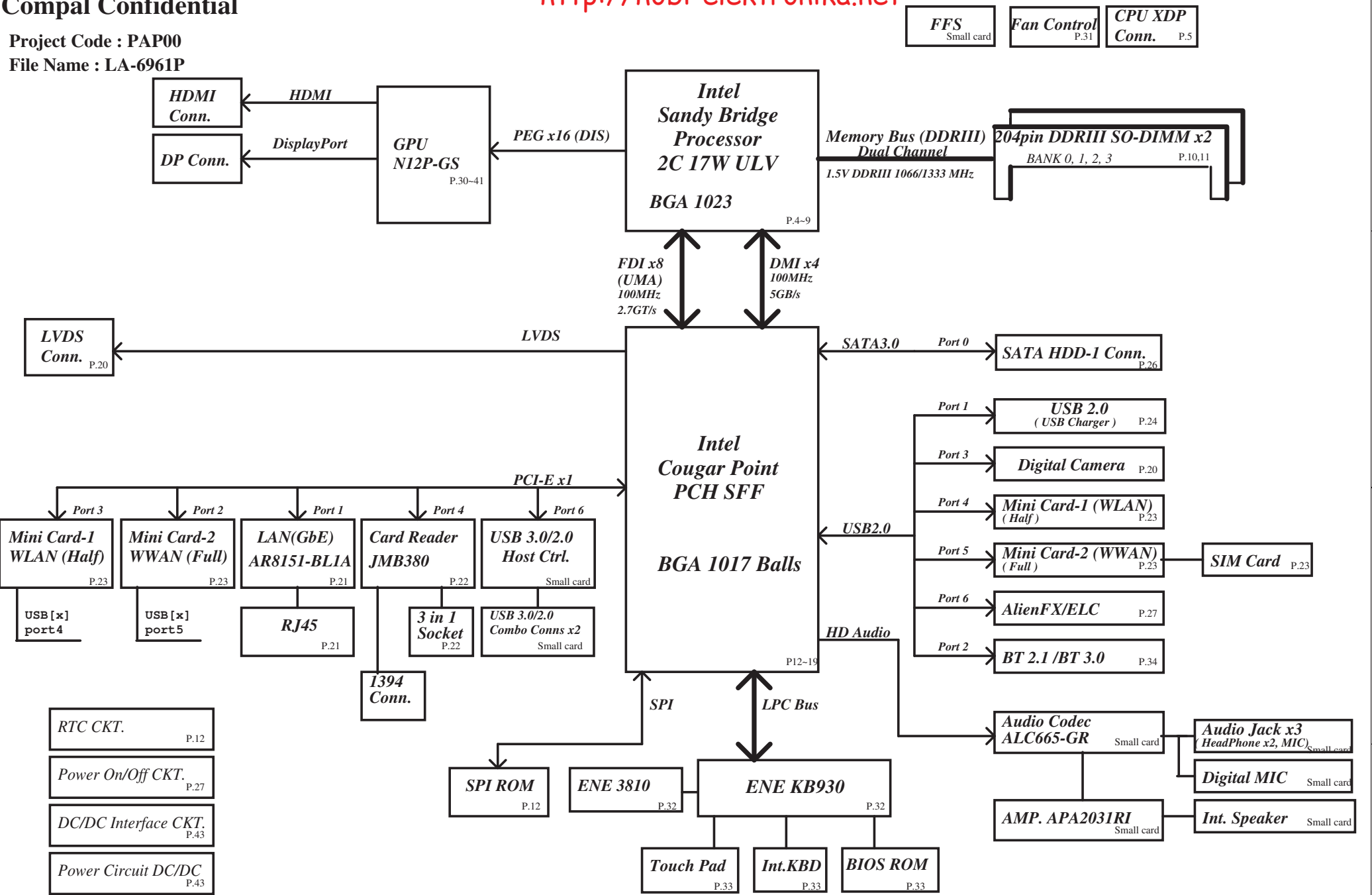
Sandy Bridge (BGA1023) + Cougar Point (SFF)

DISCRETE VGA N12P-GS (optimus)

2010-11-29

Rev: 0.4

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/07/06	Deciphered Date	2011/07/06	Title	Cover Page
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

PCH

USB PORT#	DESTINATION
0	None
1	JUSB1 (Ext Left Side)
2	Bluetooth
3	CAMERA
4	JMINI1 (WLAN)
5	JMINI2 (WWAN)
6	ELC
7	None
8	None
9	None
10	None
11	None
12	None
13	None

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	FFS	VGA Thermal Sensor	SMSC
EC_SMB_CK1 EC_SMB_DA1	KB930			V					
EC_SMB_CK2 EC_SMB_DA2	KB930								
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH	V	V			V		V	V
MEM_SMBCLK MEM_SMBDATA	PCH				V		V		

Link

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER	CLKOUT	DESTINATION
	CLKOUT_PCIE5	None	PCI0	PCH_LOOPBACK
	CLKOUT_PCIE6	USB 3.0	PCI1	EC
	CLKOUT_PCIE7	None	PCI2	None
	CLKOUT_PEG_B	None	PCI3	None
			PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	None
SATA3	None
SATA4	None
SATA5	None

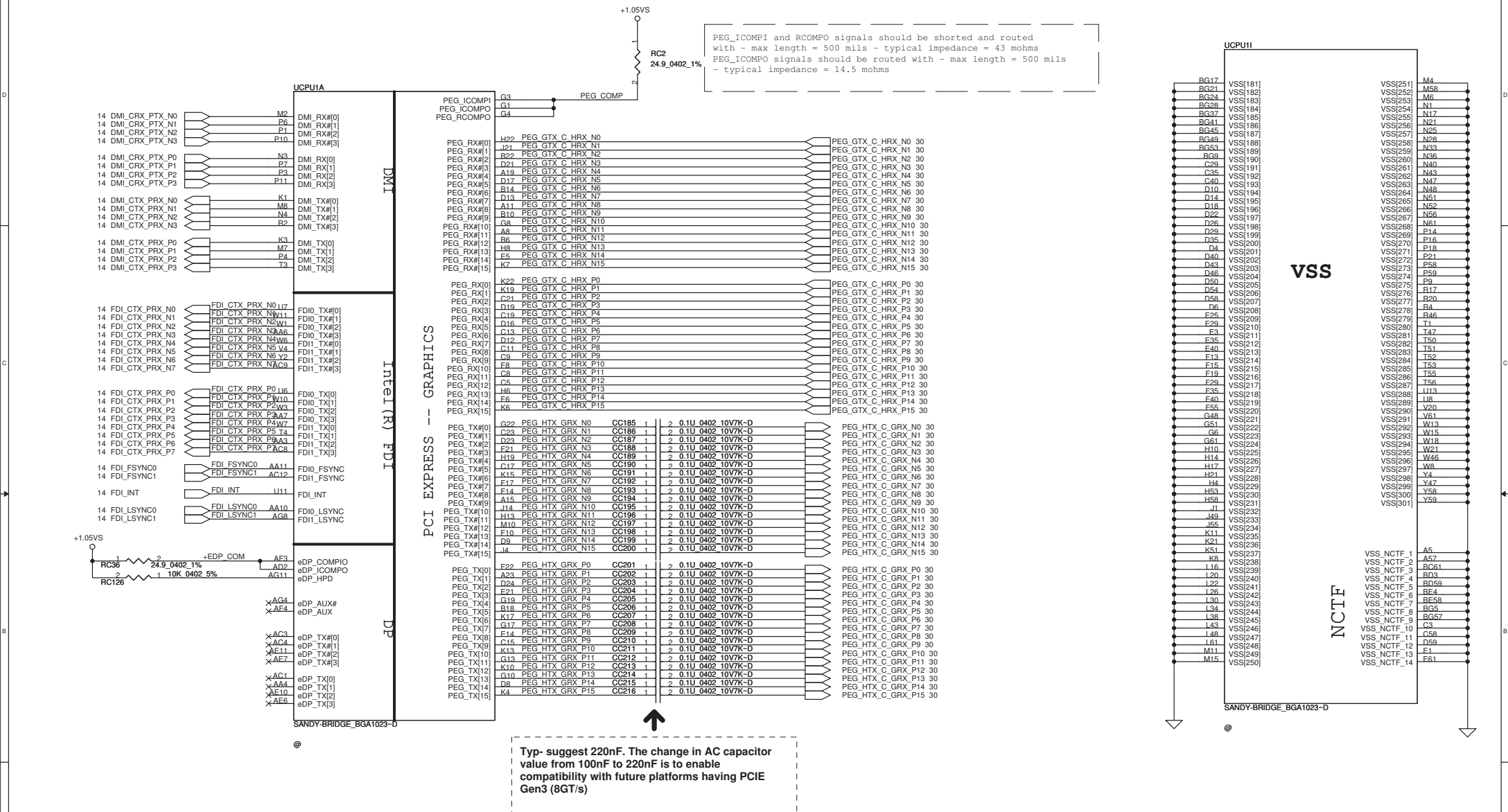
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER and 1394
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

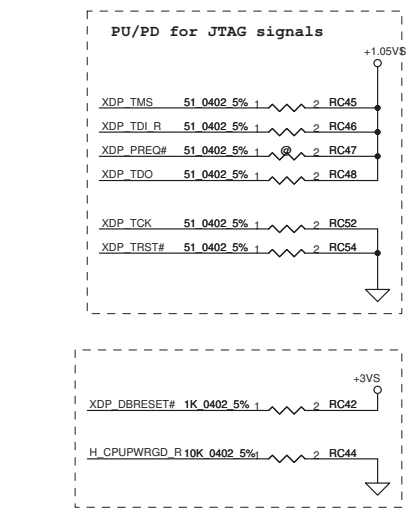
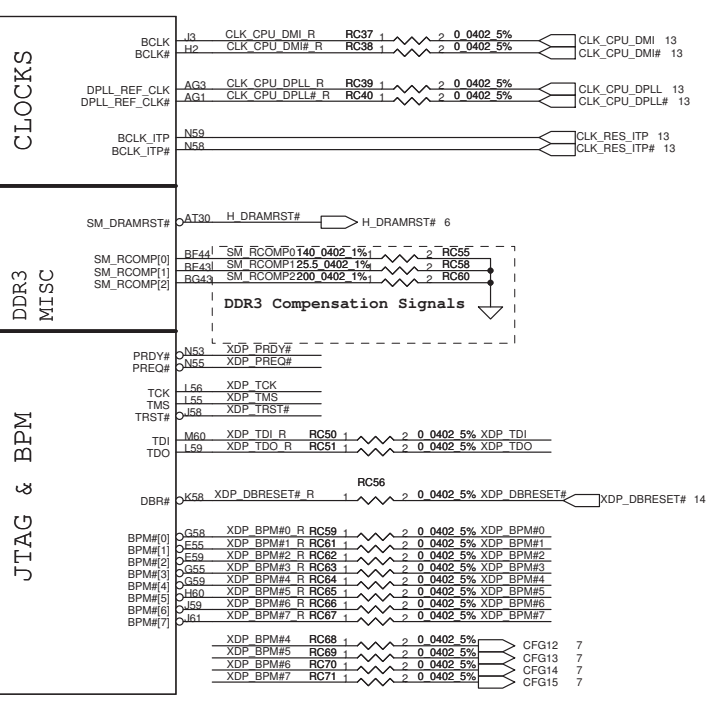
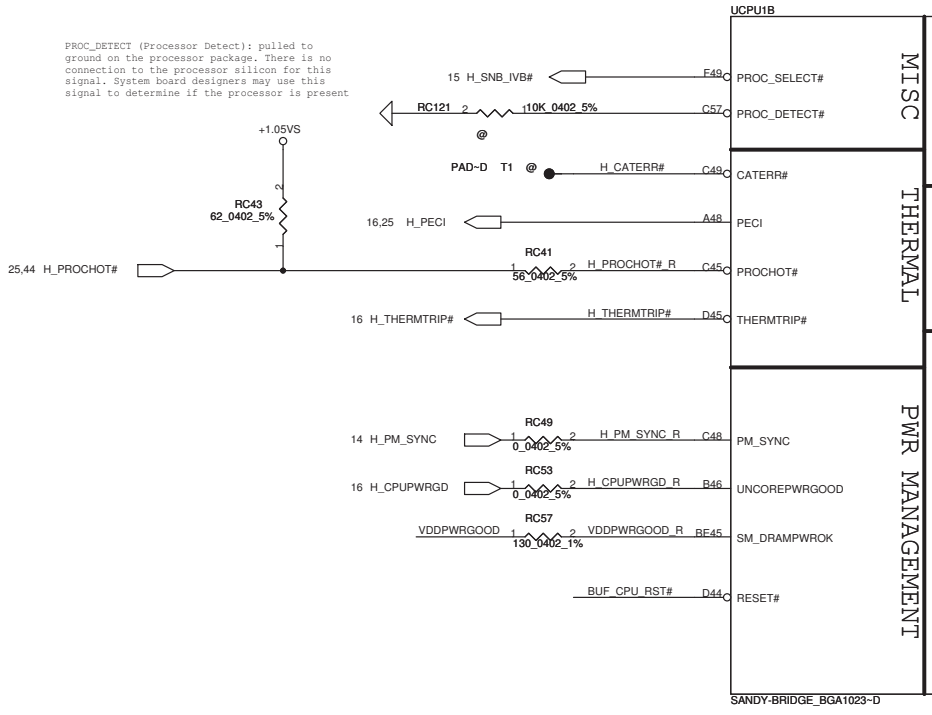
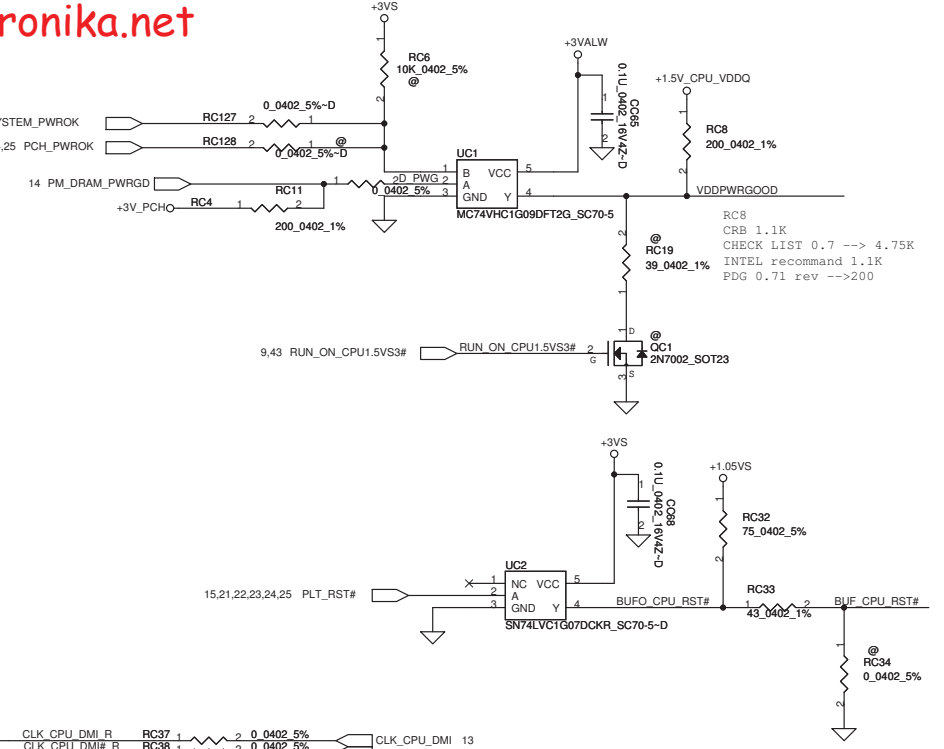
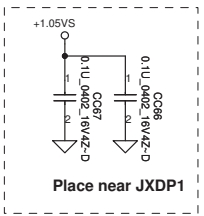
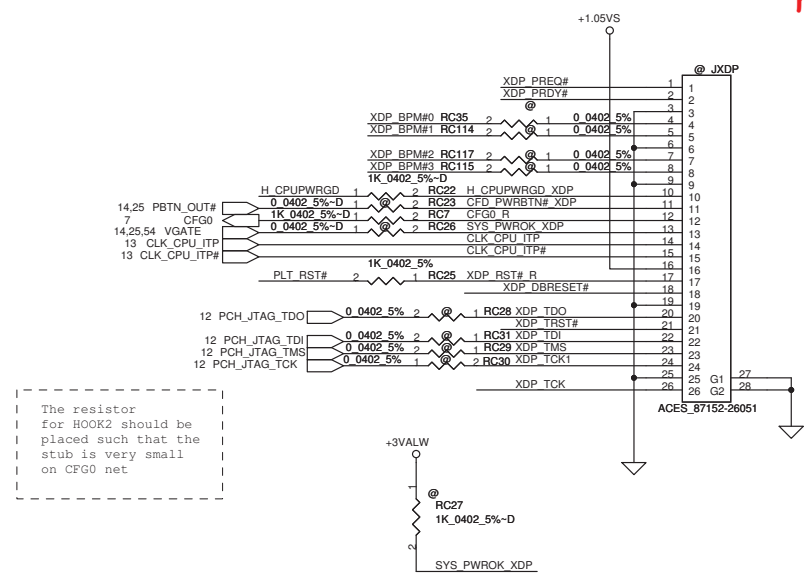
Symbol Note :

 : means Digital Ground

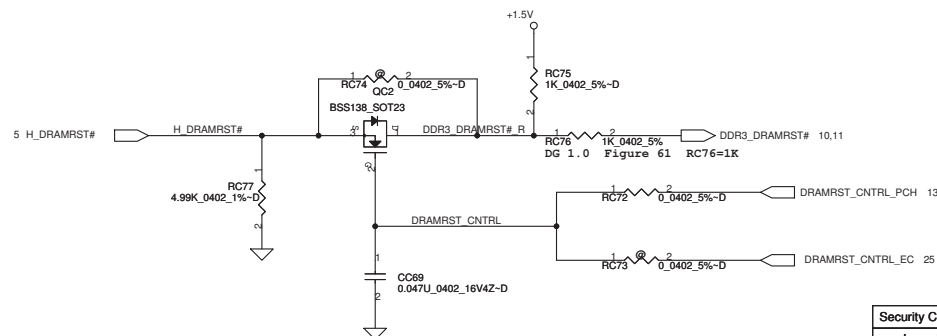
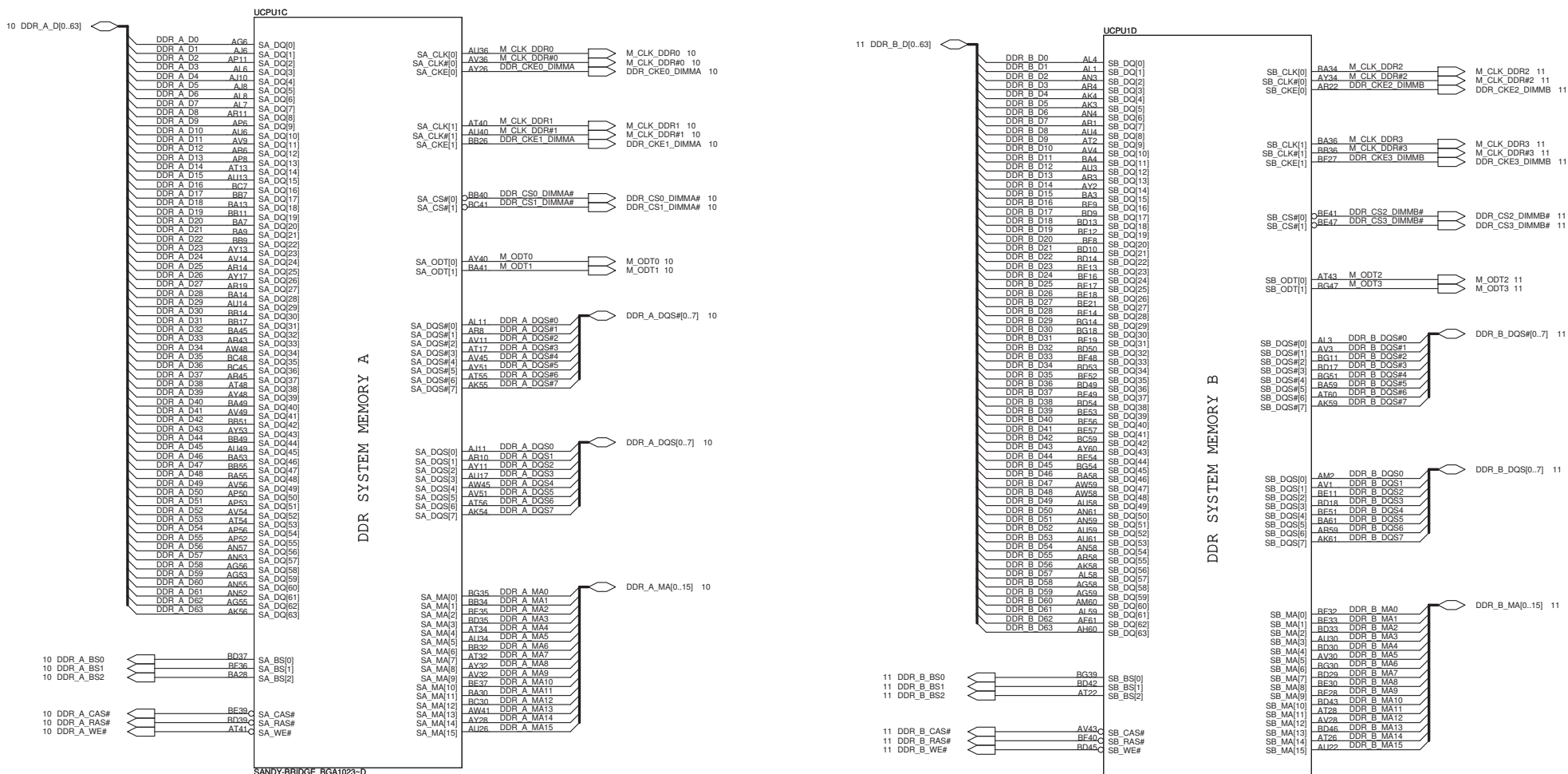
 : means Analog Ground

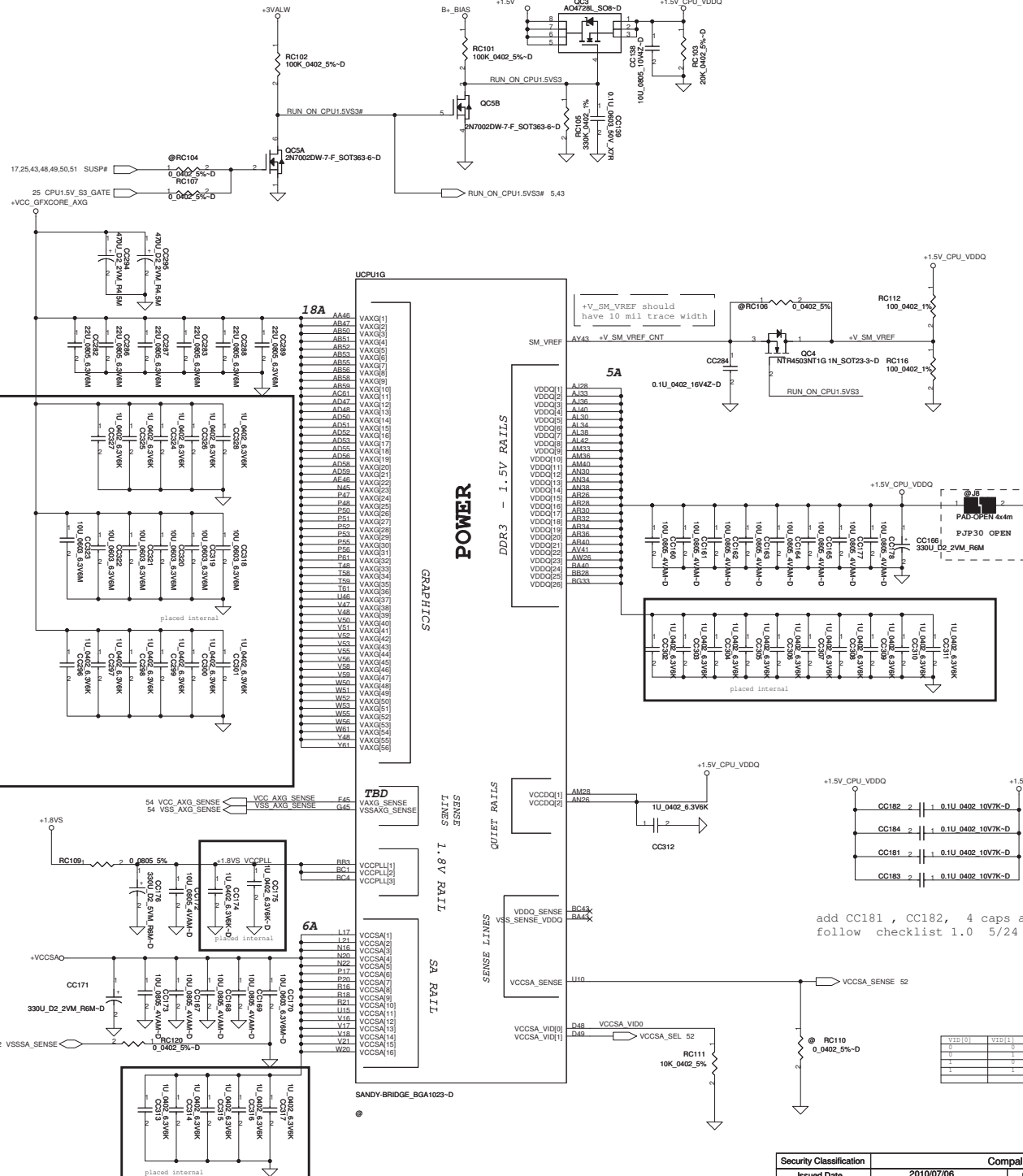
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				Size	Document Number
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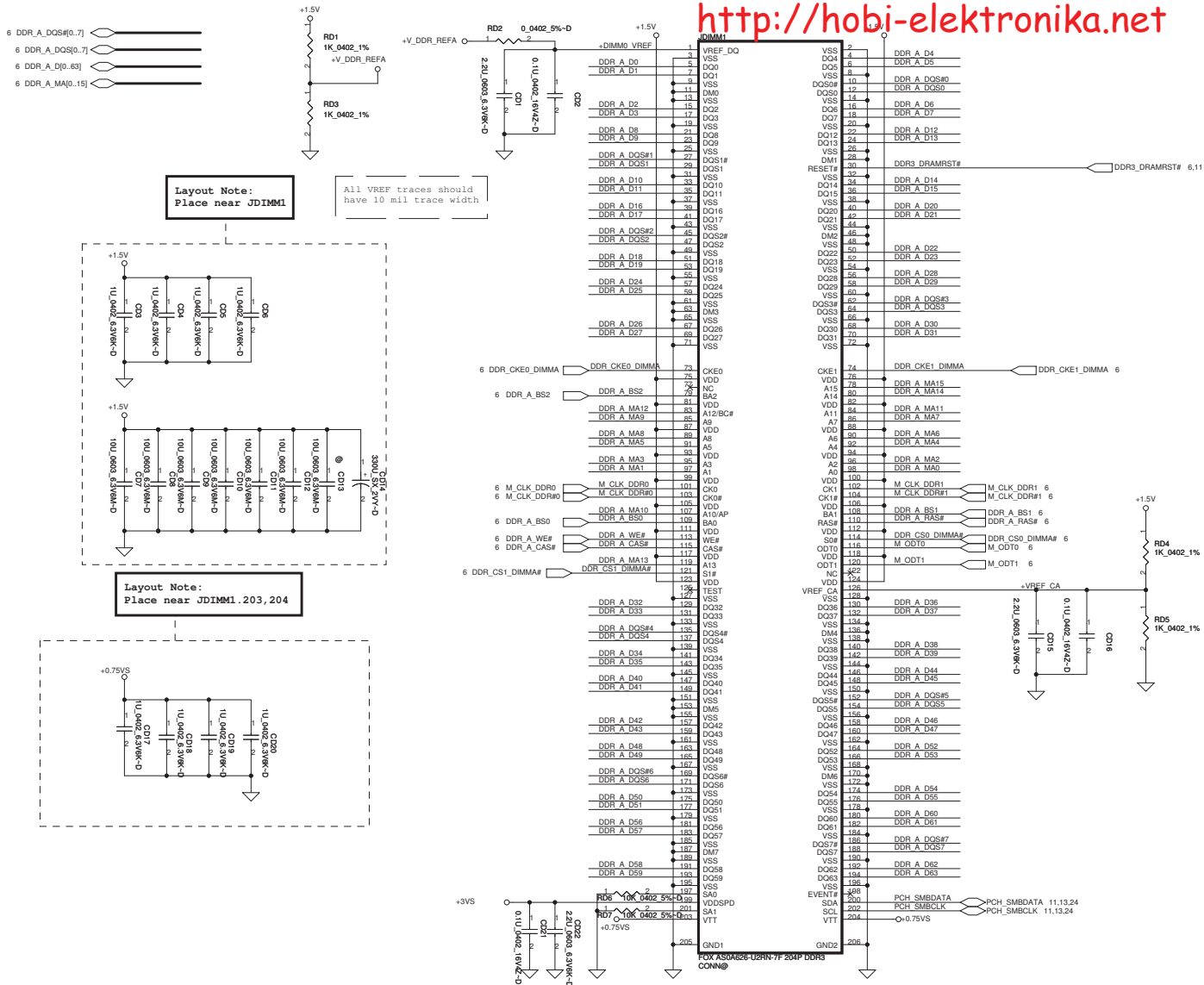
A13	VSS1(1)
A21	VSS(2)
A22	VSS(3)
A23	VSS(4)
A35	VSS(5)
A36	VSS(6)
A37	VSS(7)
A38	VSS(8)
A39	VSS(9)
A51	VSS(10)
A52	VSS(11)
A53	VSS(12)
AA13	VSS(13)
AA14	VSS(14)
AA22	VSS(15)
AA35	VSS(16)
AA36	VSS(17)
AA37	VSS(18)
AA38	VSS(19)
AA39	VSS(20)
AA51	VSS(21)
AA52	VSS(22)
AA53	VSS(23)
AB21	VSS(24)
AB22	VSS(25)
AC10	VSS(26)
AC11	VSS(27)
AC12	VSS(28)
AD10	VSS(29)
AD11	VSS(30)
AD12	VSS(31)
AD21	VSS(32)
AD22	VSS(33)
AD31	VSS(34)
AD32	VSS(35)
AE1	VSS(36)
AF1	VSS(37)
AF12	VSS(38)
AF21	VSS(39)
AF31	VSS(40)
AF41	VSS(41)
AF51	VSS(42)
AF52	VSS(43)
AF53	VSS(44)
AF54	VSS(45)
AF55	VSS(46)
AF56	VSS(47)
AF57	VSS(48)
AF58	VSS(49)
AF59	VSS(50)
AG14	VSS(51)
AG18	VSS(52)
AG23	VSS(53)
AG24	VSS(54)
AG31	VSS(55)
AG7	VSS(56)
AH3	VSS(57)
AI15	VSS(58)
AJ12	VSS(59)
AJ21	VSS(60)
AJ22	VSS(61)
AJ23	VSS(62)
AJ30	VSS(63)
AJ31	VSS(64)
AJ32	VSS(65)
AJ33	VSS(66)
AJ34	VSS(67)
AJ35	VSS(68)
AJ36	VSS(69)
AJ37	VSS(70)
AJ38	VSS(71)
AJ39	VSS(72)
AJ41	VSS(73)
AJ42	VSS(74)
AJ43	VSS(75)
AJ44	VSS(76)
AJ45	VSS(77)
AJ46	VSS(78)
AJ47	VSS(79)
AJ48	VSS(80)
AJ49	VSS(81)
AJ50	VSS(82)
AM13	VSS(83)
AM14	VSS(84)
AM22	VSS(85)
AM23	VSS(86)
AM24	VSS(87)
AM25	VSS(88)
AM26	VSS(89)
AM27	VSS(90)

VSS

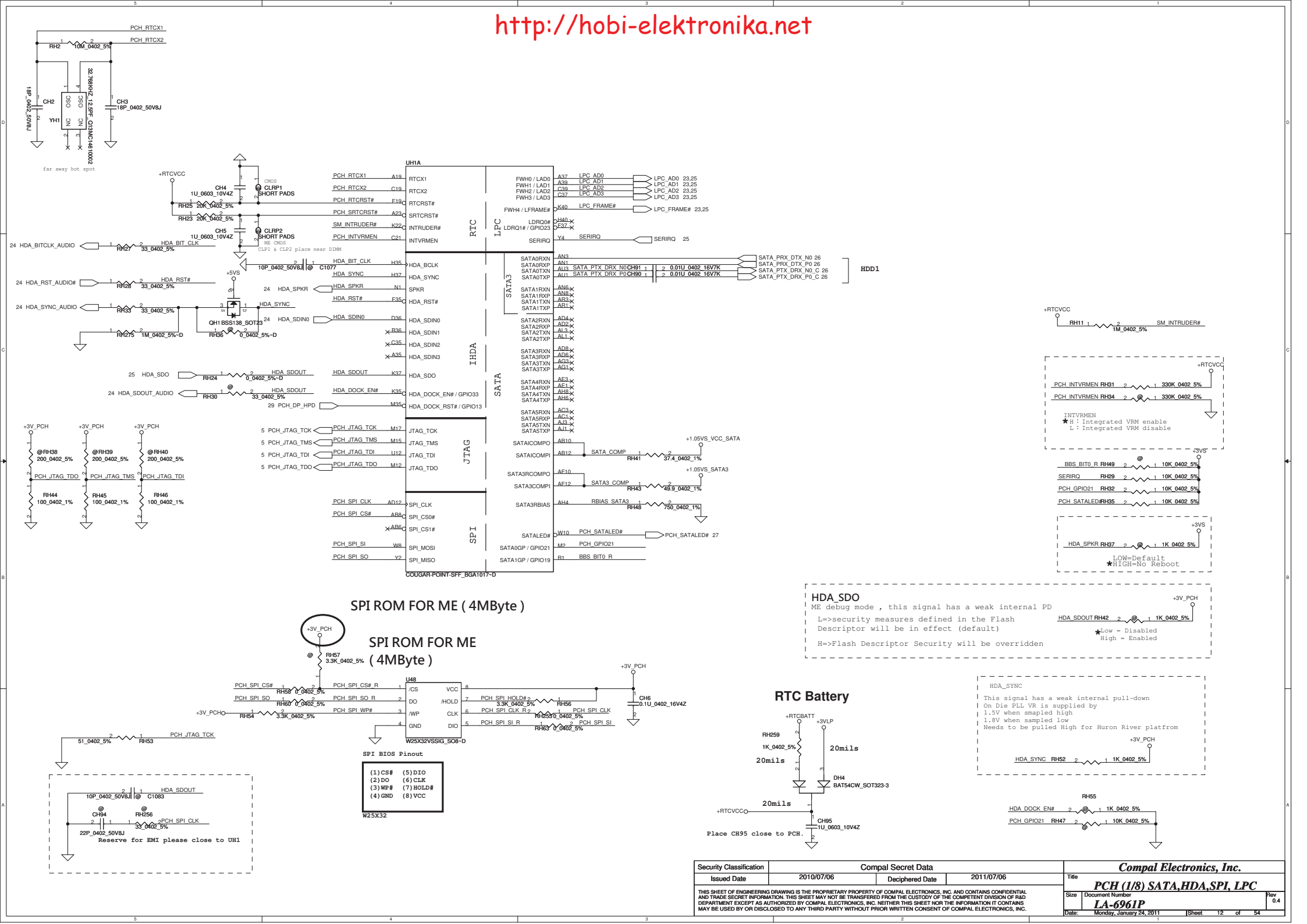
add CC181 , CC182, 4 caps are all pop.
follow checklist 1.0 5/24

VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

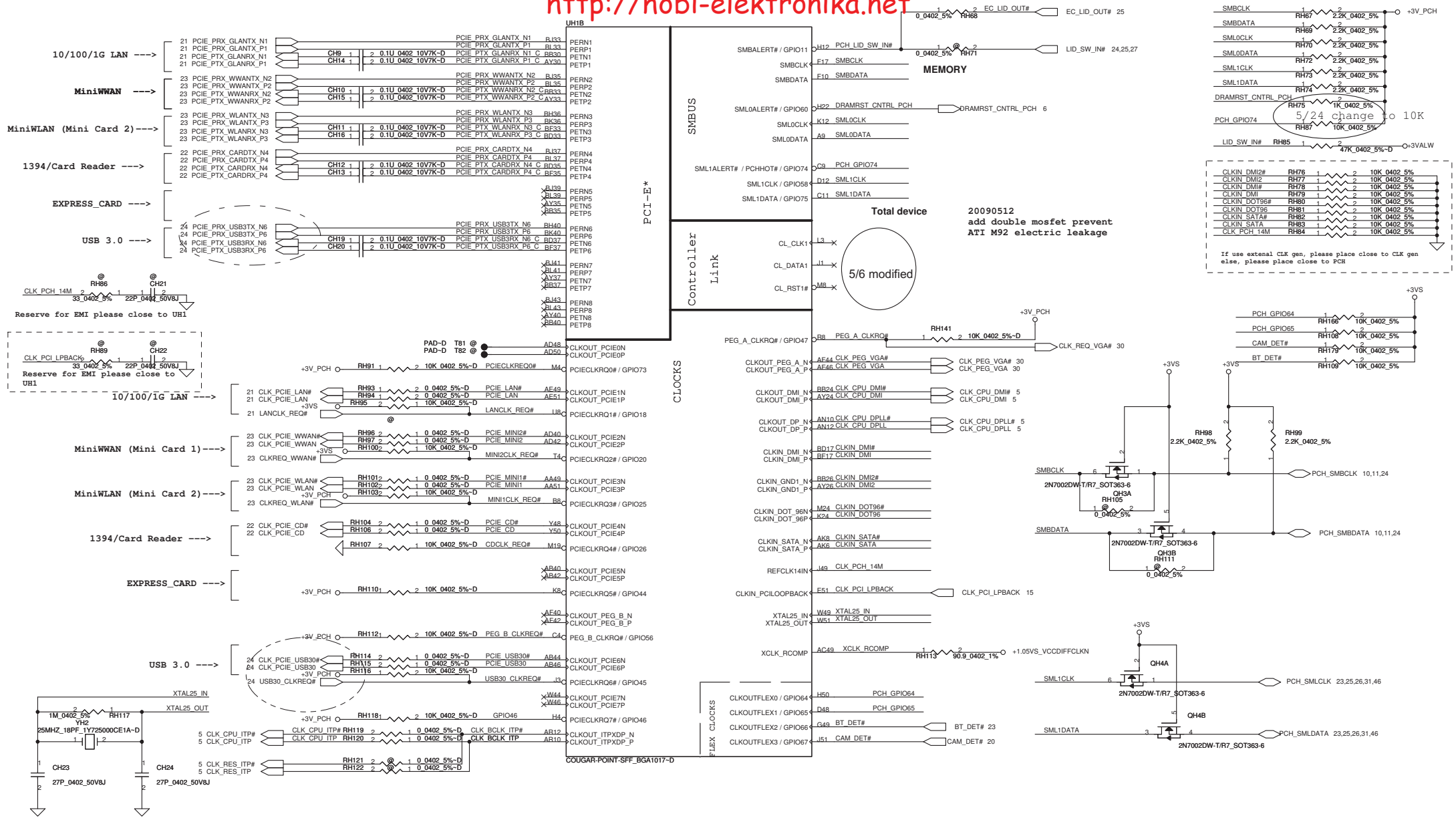
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				Size	Document Number	Rev
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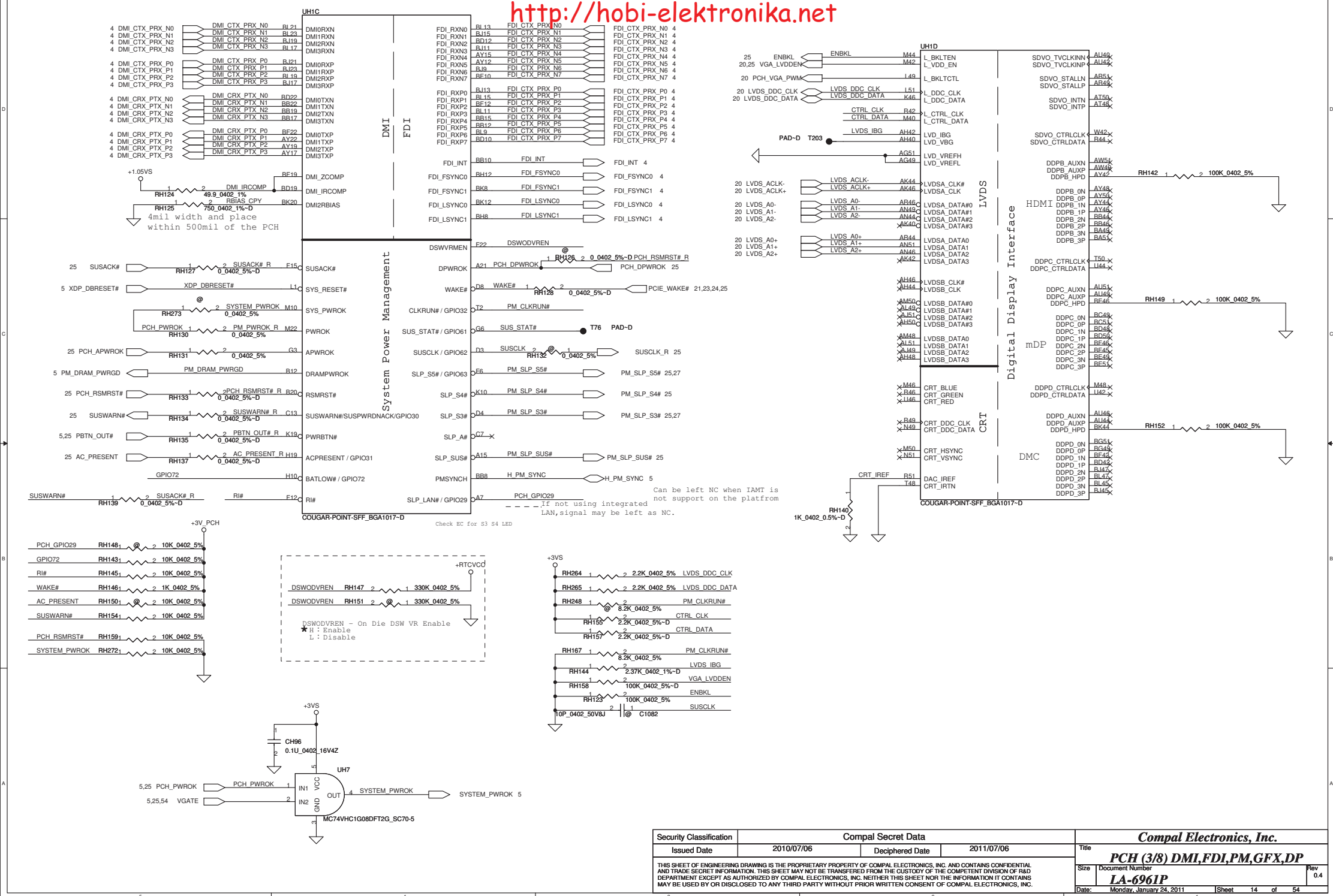


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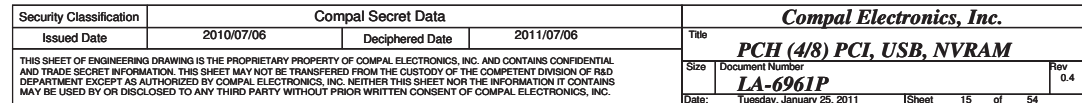


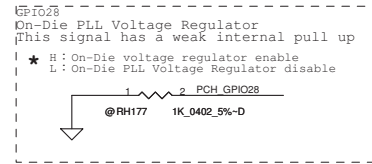
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		PCH (1/8) SATA,HDA,SPI, LPC	
2010/07/06		2011/07/06		LA-6961P	
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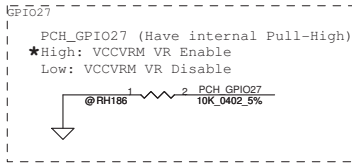
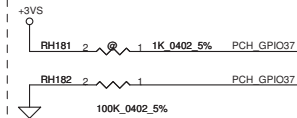
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Issued Date		2010/07/06		Deciphered Date		2011/07/06		Title		
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								Size	Document Number	Rev
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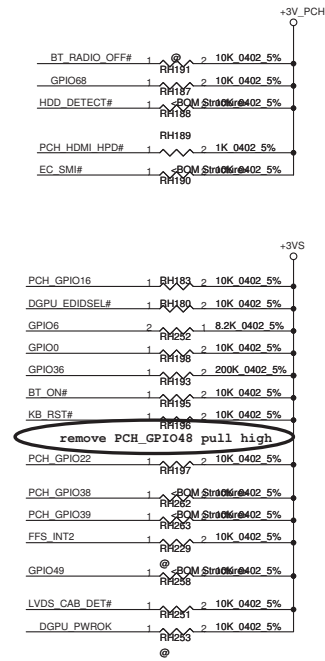
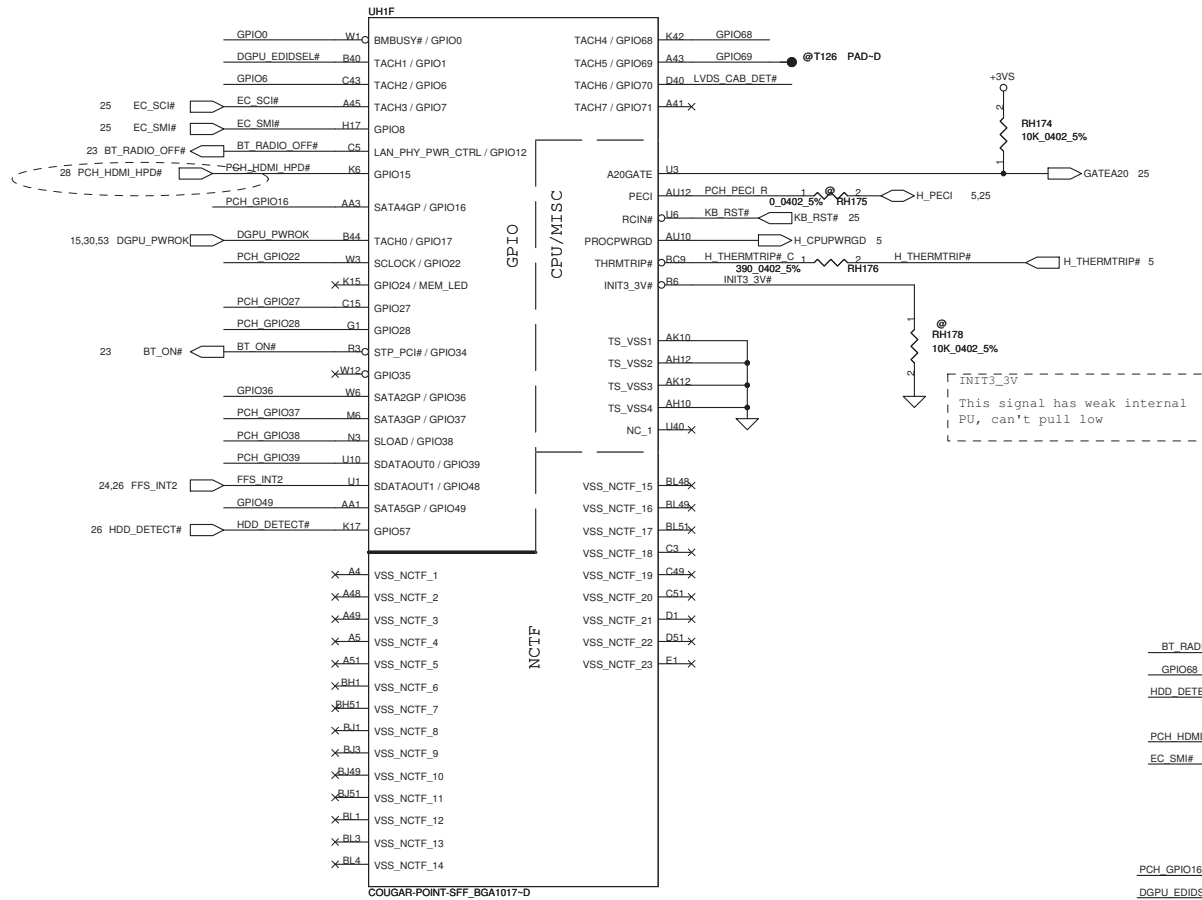
PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE

* LOW ~ Tx, Rx terminated to same voltage (DC Coupling Mode)



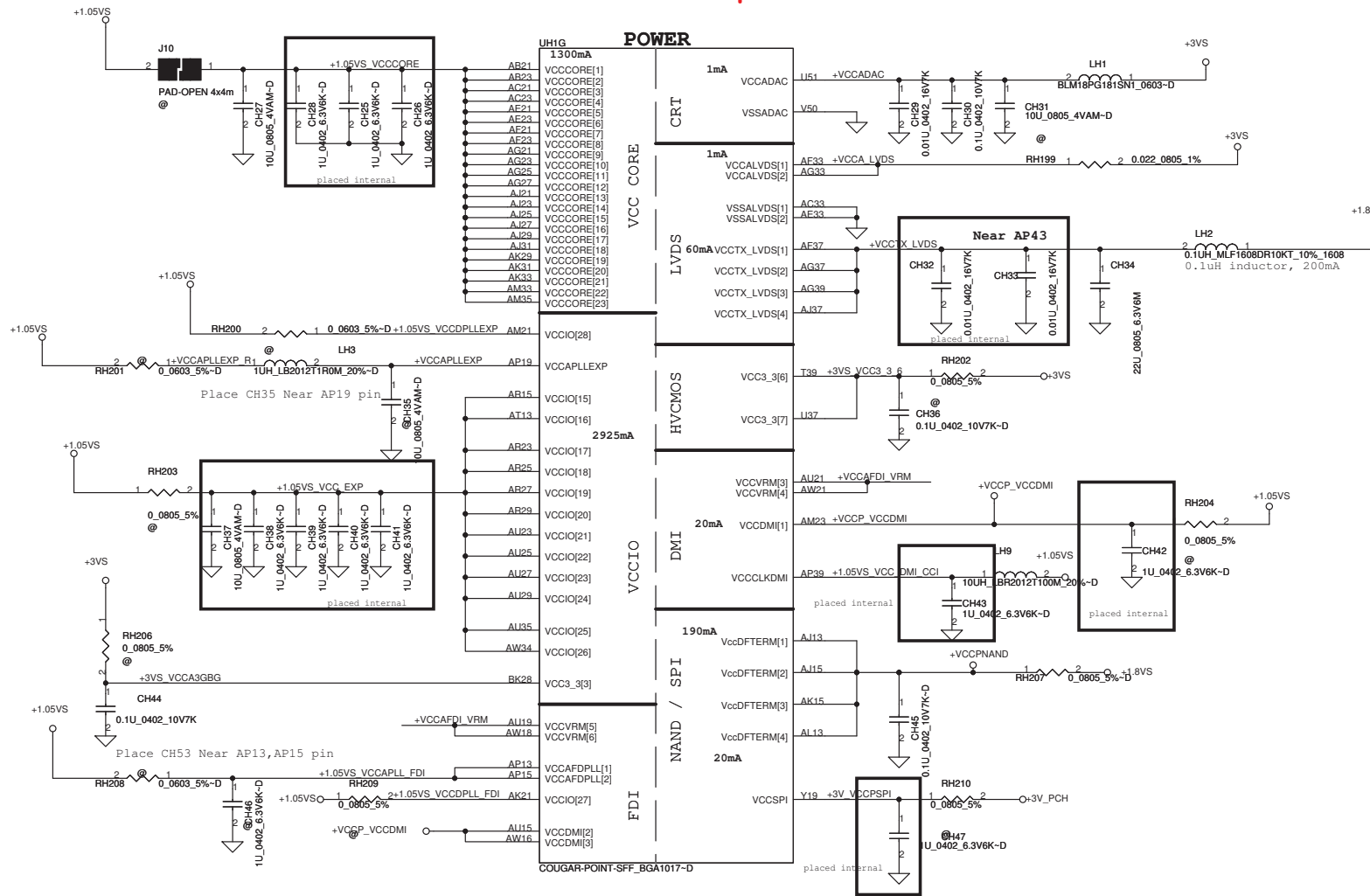
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5



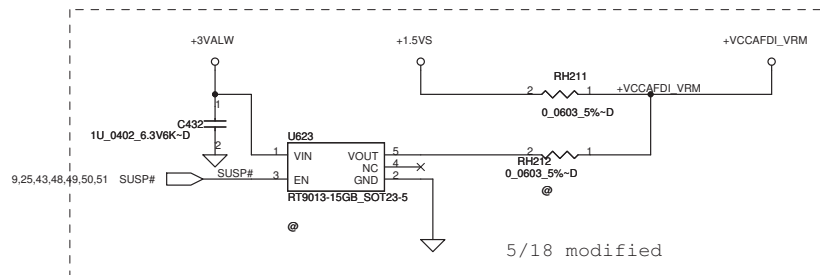
add RH185, RH229, RH251
5/25

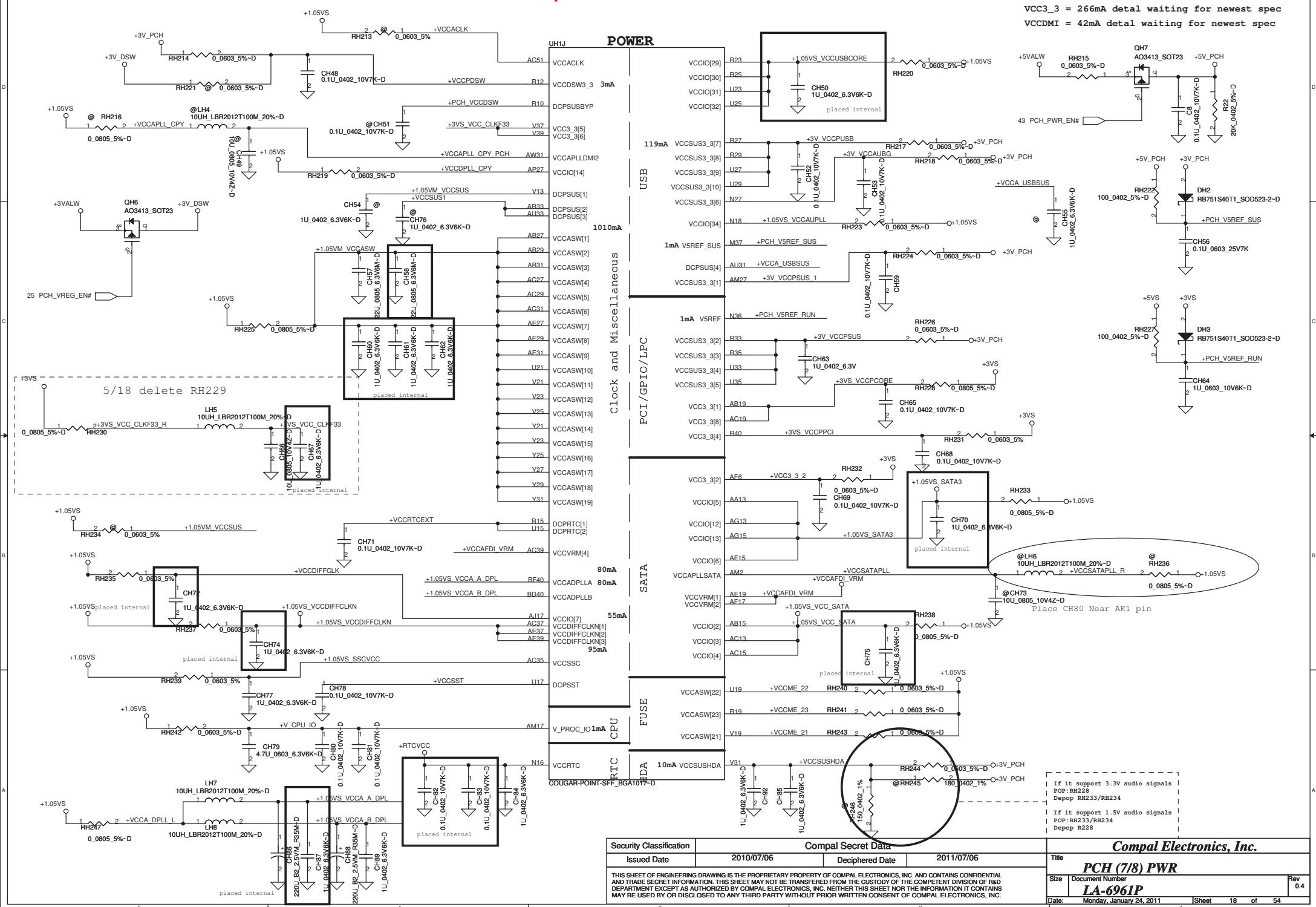
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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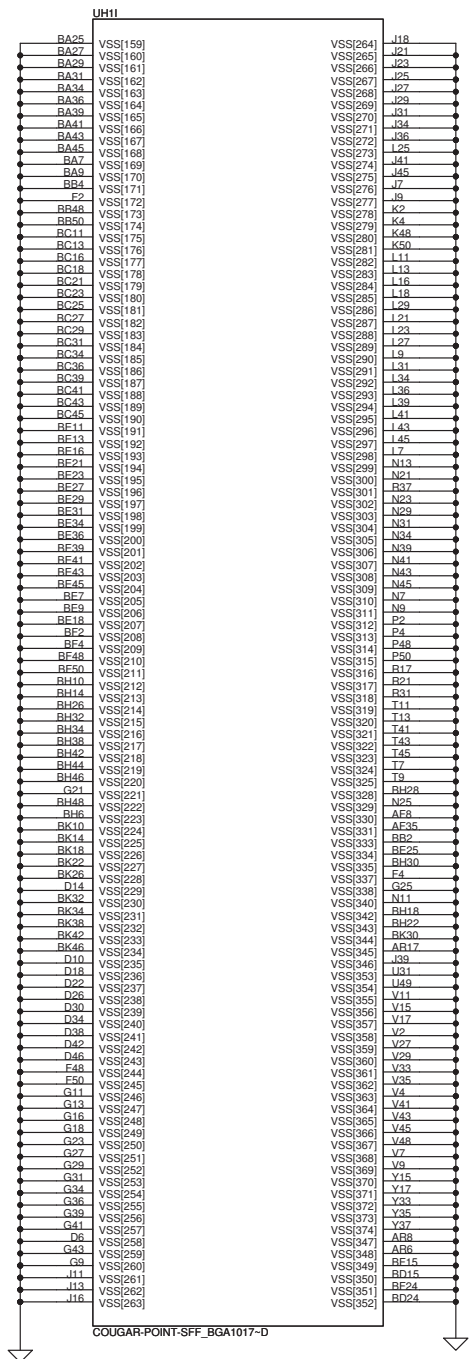
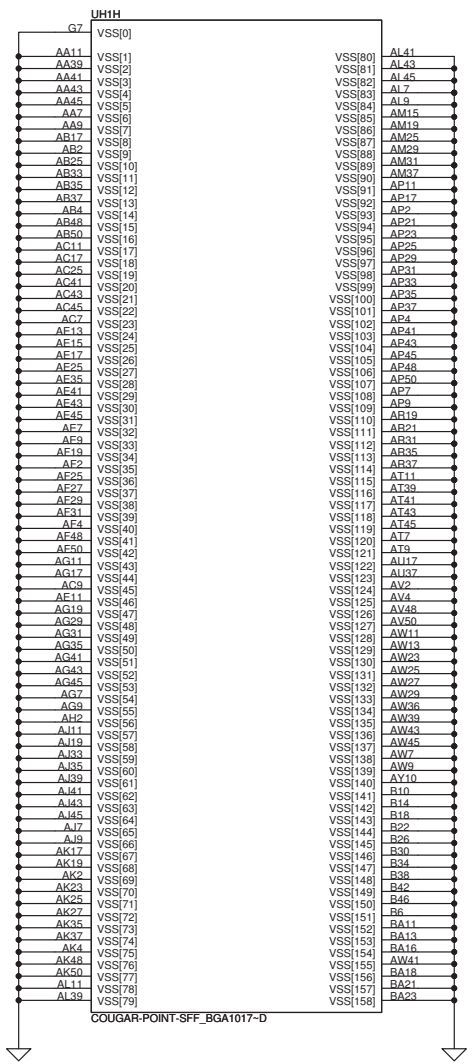


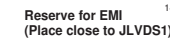
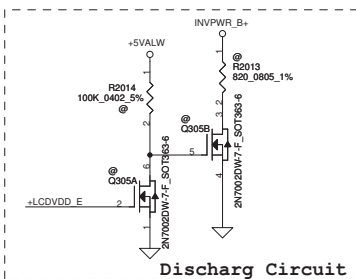
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detal waiting for newest spec

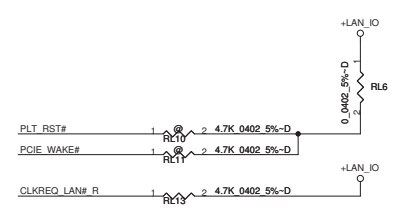




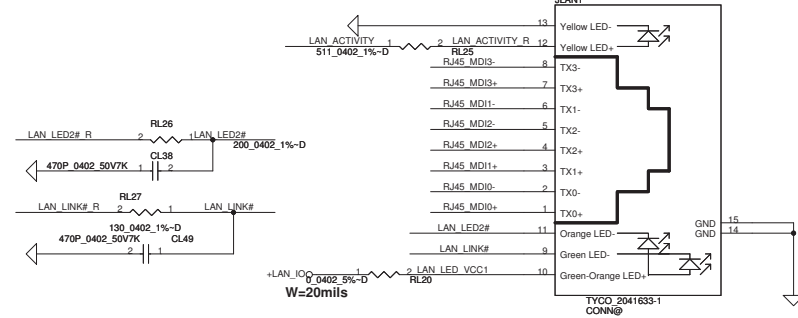
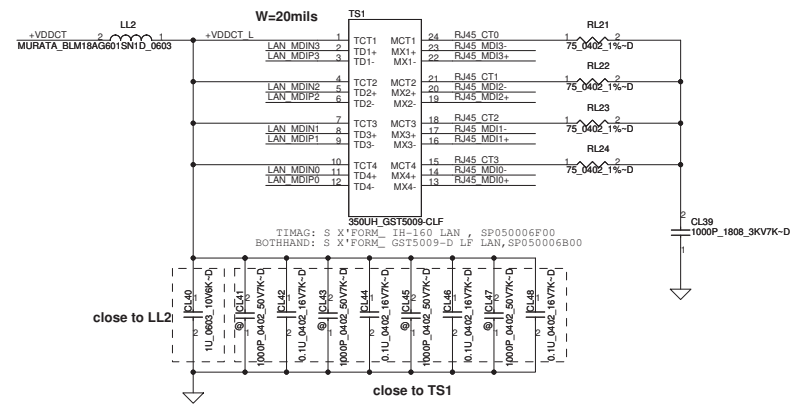
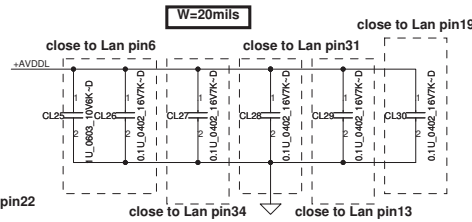
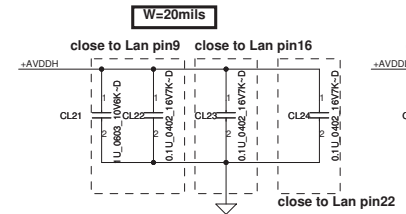
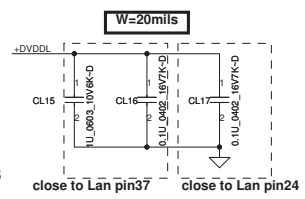
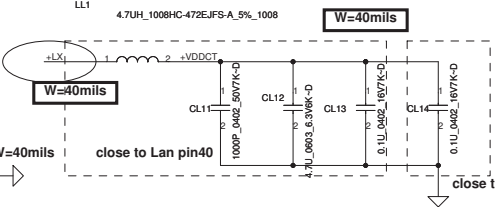
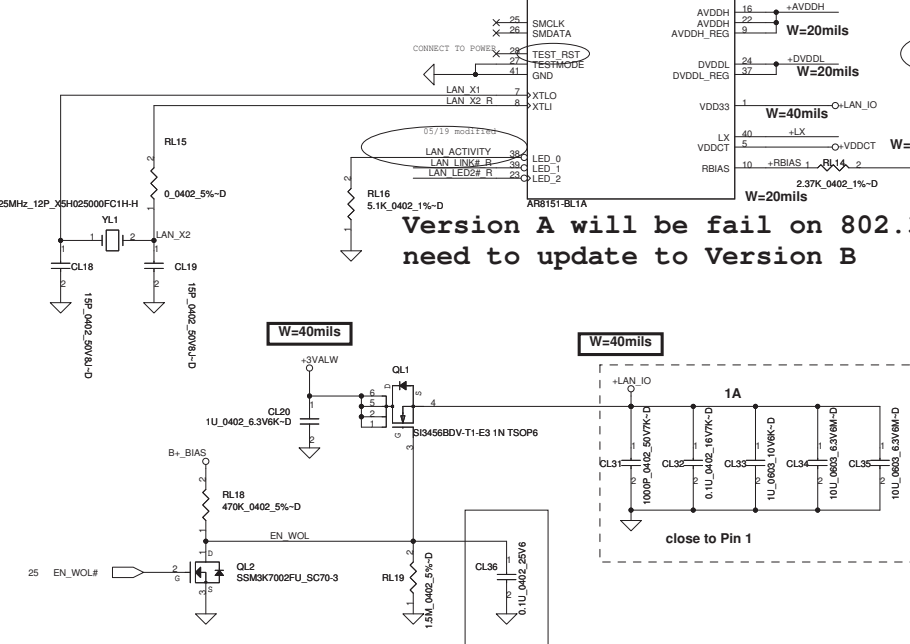


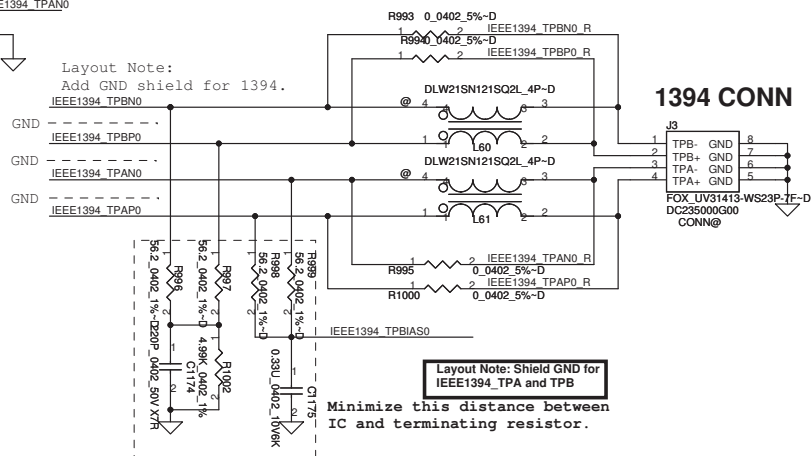
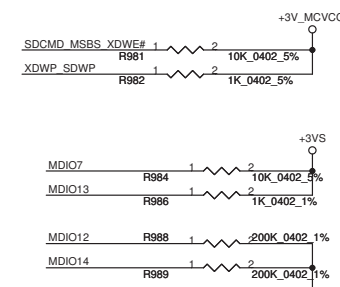
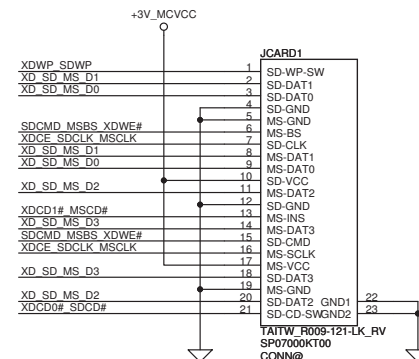
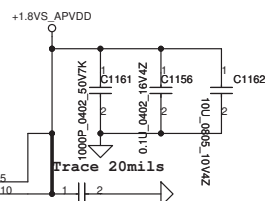
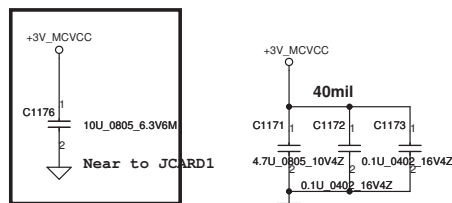
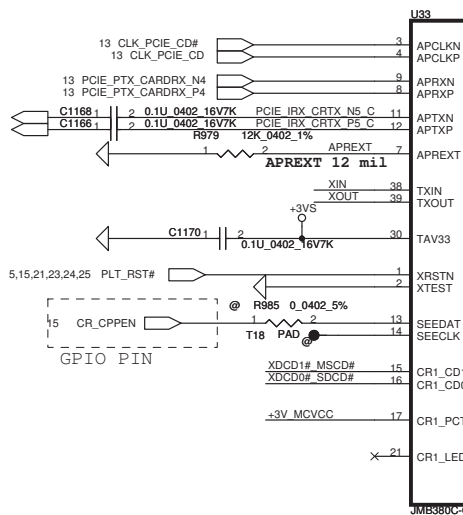
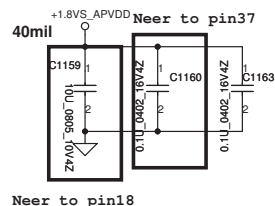


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Version A will be fail on 802.3a
need to update to Version B

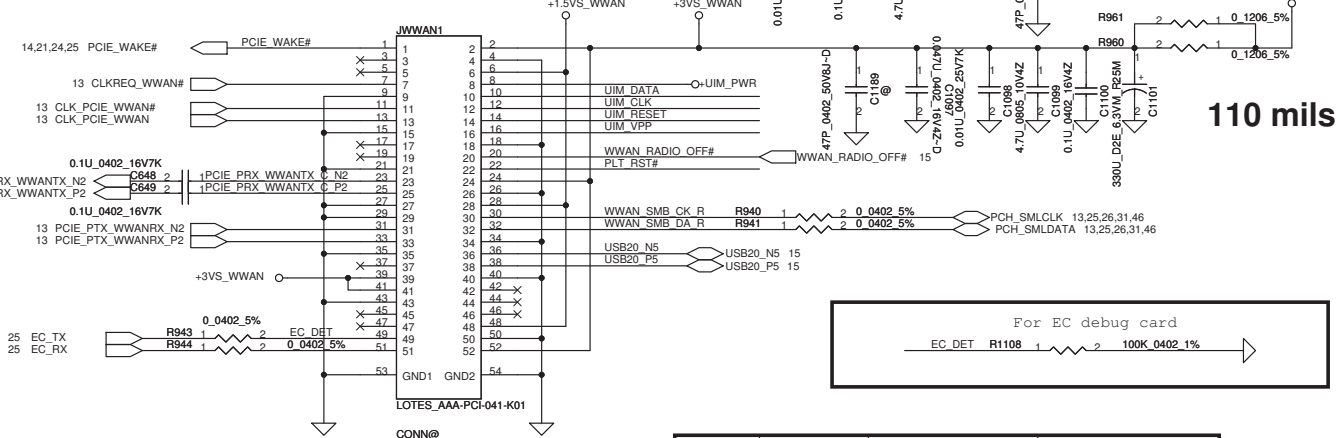




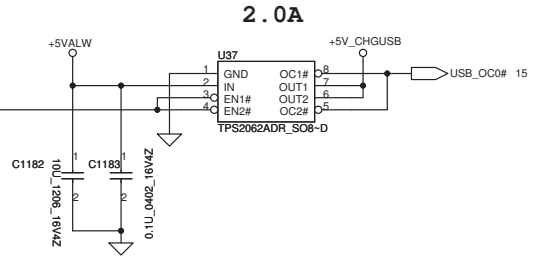
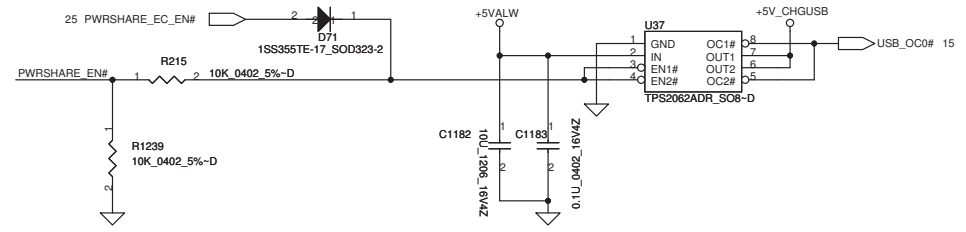
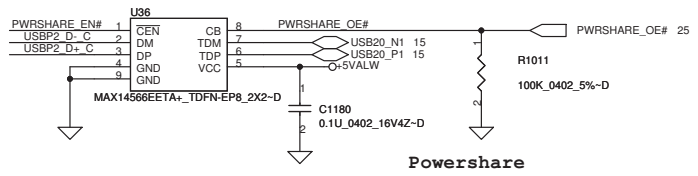
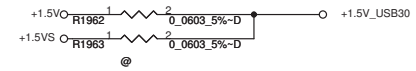
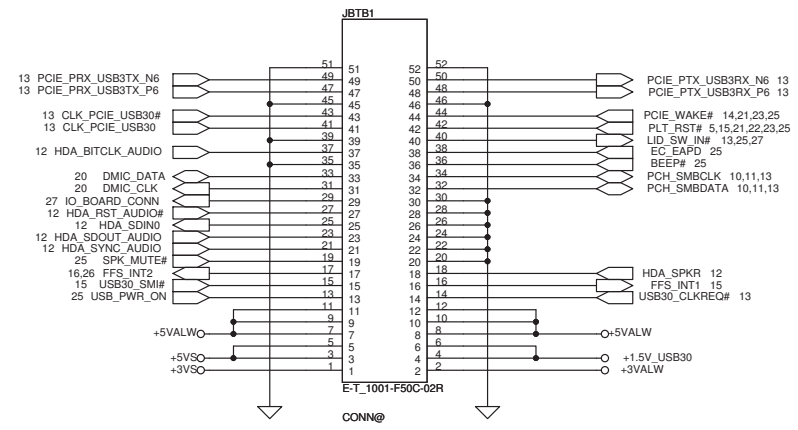
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				Custom	0.
				Document Number LA-6961P	
				Date:	Monday, January 24, 2011
				Sheet	22 of 54

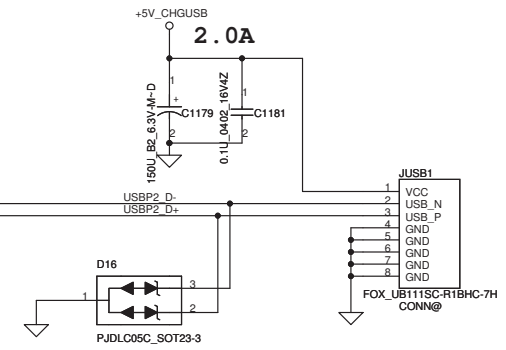
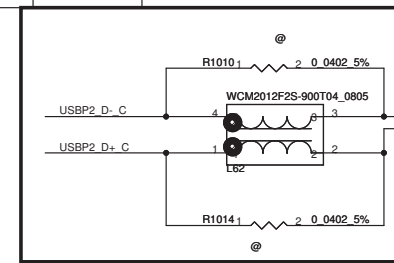
WWAN PCIE MiniCard



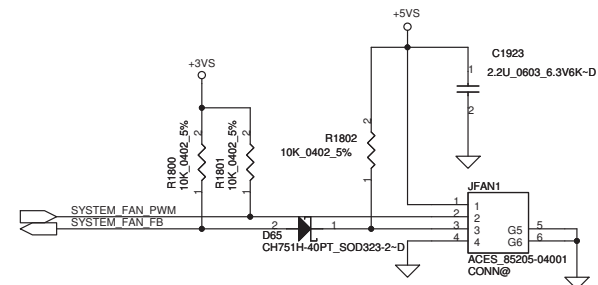
IO Board CONN



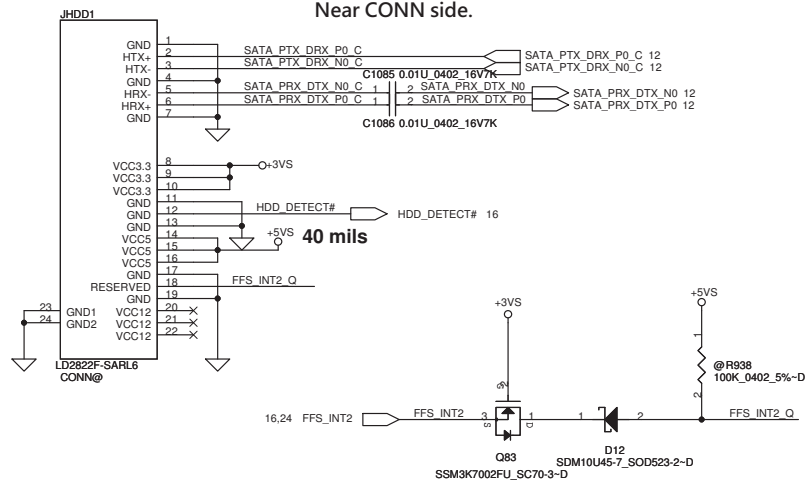
OE#	Function
L	Dect charger
H	D=1D



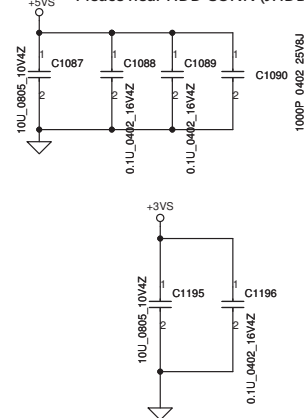




Near CONN side.



Please near HDD CONN (JHDD1)



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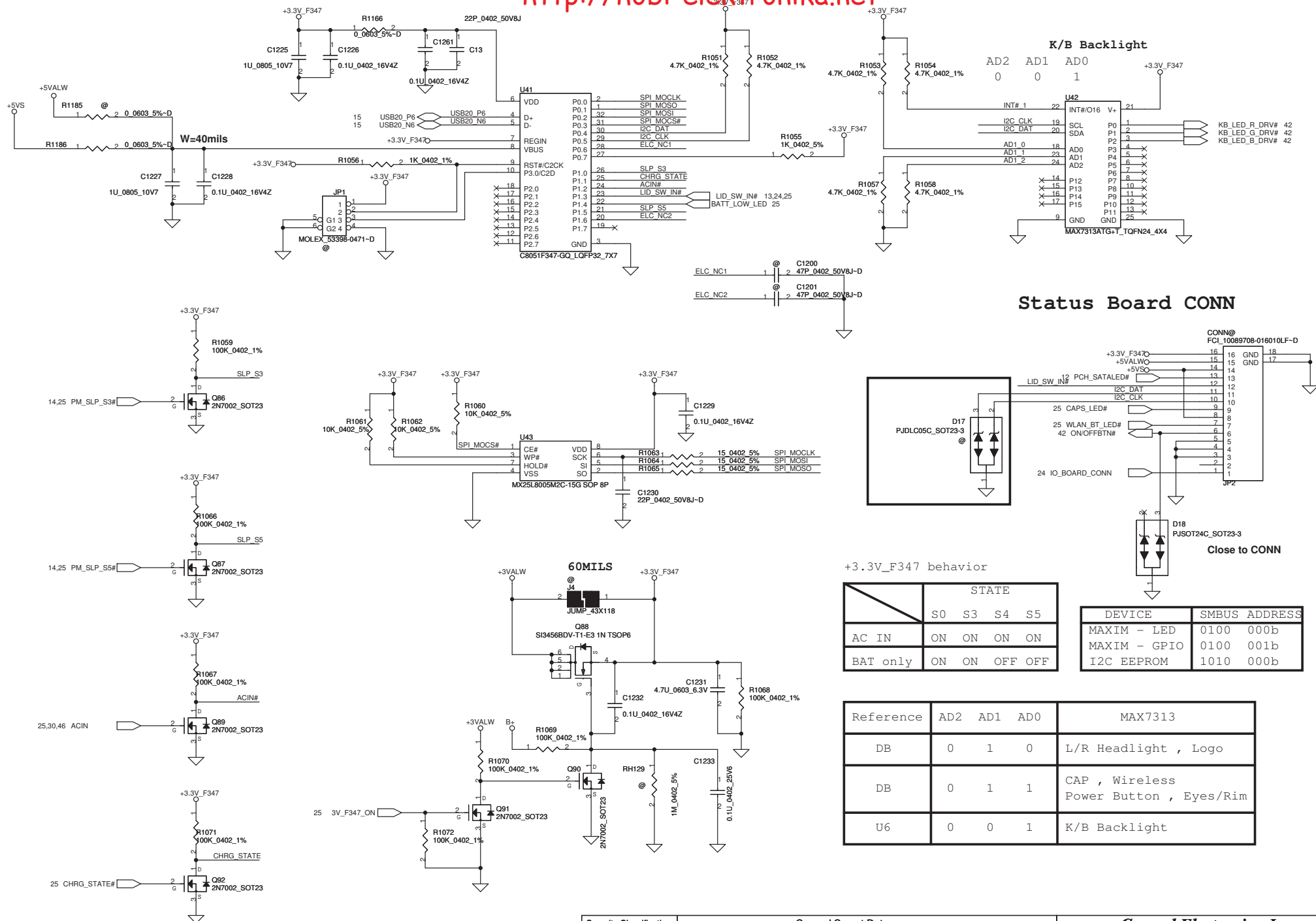
Compal Electronics, Inc.

Title **FAN 8 Thermal Sensor**

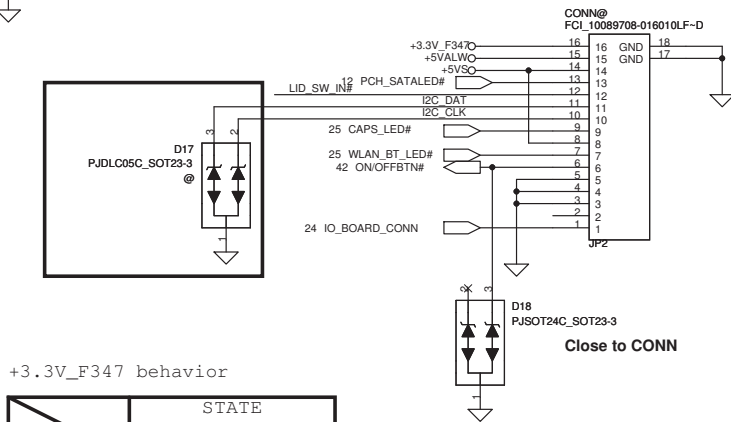
FAN & Thermal Sensor

Size	Document Number	Rev
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Status Board CONN



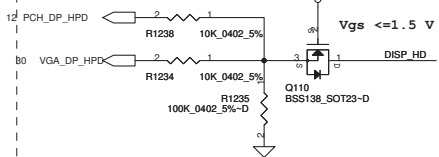
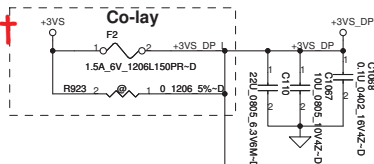
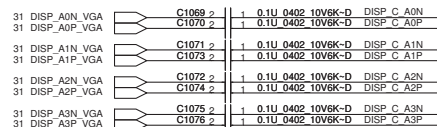
+3.3V_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

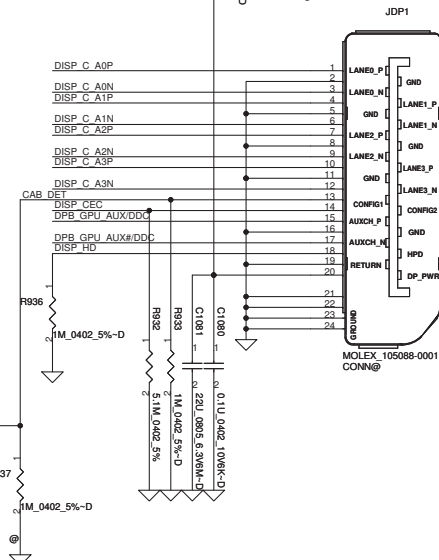
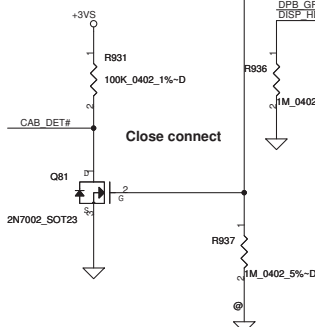
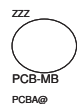
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

Reference	AD2	AD1	AD0	MAX7313
DB	0	1	0	L/R Headlight , Logo
DB	0	1	1	CAP , Wireless Power Button , Eyes/Rim
U6	0	0	1	K/B Backlight

<http://hobi-elektronika.net>

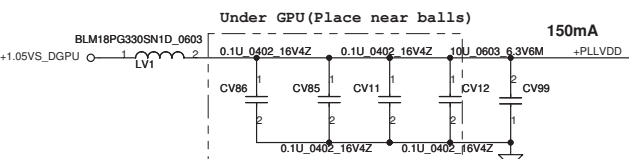


Follow Intel HPD design rev 1.6

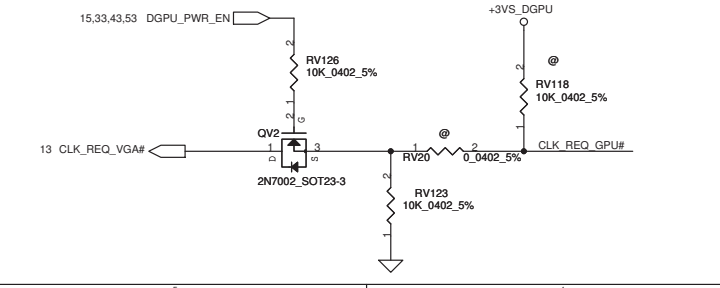
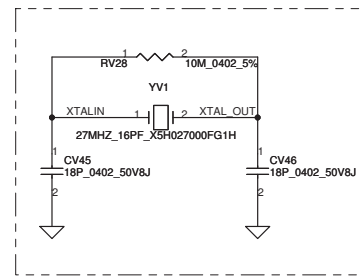
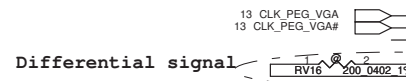


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				Date:	Monday, January 24, 2011	Sheet 29 of 54

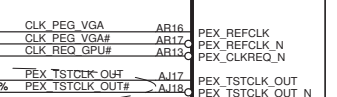


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PEG GTX C HRX P1	CV15	1	2	0.1U 0402 10V7K-D	PEG GTX CRX N1	AM18
PEG GTX C HRX N1	CV16	1	2	0.1U 0402 10V7K-D	PEG GTX CRX P1	AM19
PEG GTX C HRX P2	CV17	1	2	0.1U 0402 10V7K-D	PEG GTX CRX N2	AM20
PEG GTX C HRX N2	CV18	1	2	0.1U 0402 10V7K-D	PEG GTX CRX P2	AM21
PEG GTX C HRX P3	CV19	1	2	0.1U 0402 10V7K-D	PEG GTX CRX N3	AM22
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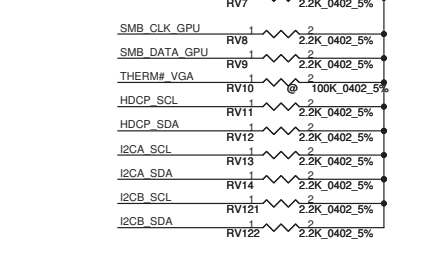
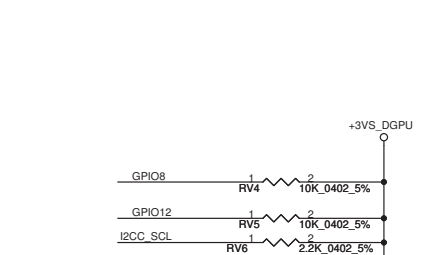
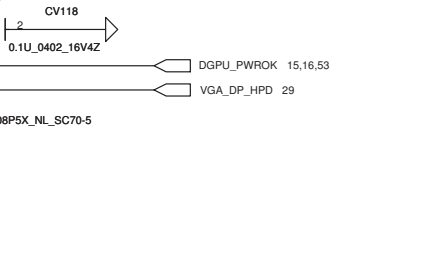
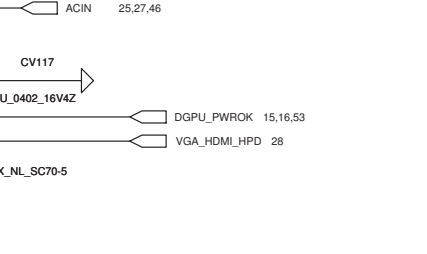
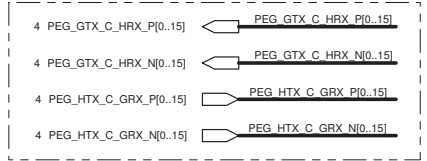
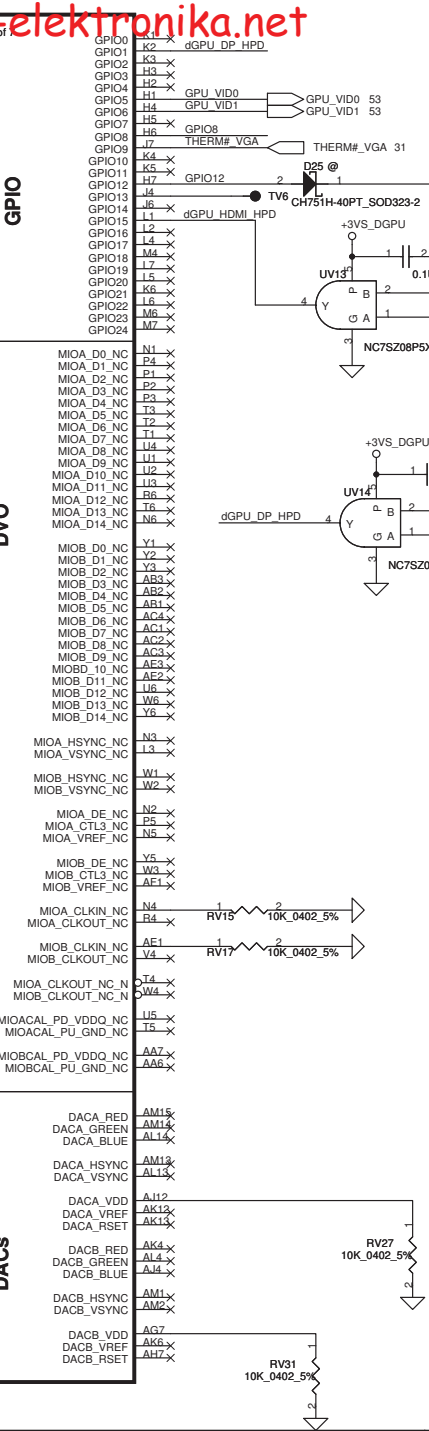
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PEG GTX CRX P15	AM46
PEG GTX CRX N15	AM47



PLLVD	AE9
SP_PLLVD	AF9
VID_PLLVD	AD9
XTALIN	R1
XTALOUT	D1
XTALSSIN	D2
XTALOUTBUFF	D1
XTAL_SSIN	D2
I2CS_SCL	F3
I2CS_SDA	F4
I2CC_SCL	G3
I2CC_SDA	G2
I2CB_SCL	G1
I2CA_SCL	G4
HDCP_SCL	F6
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N12P-GV1-A1_BGA_973P

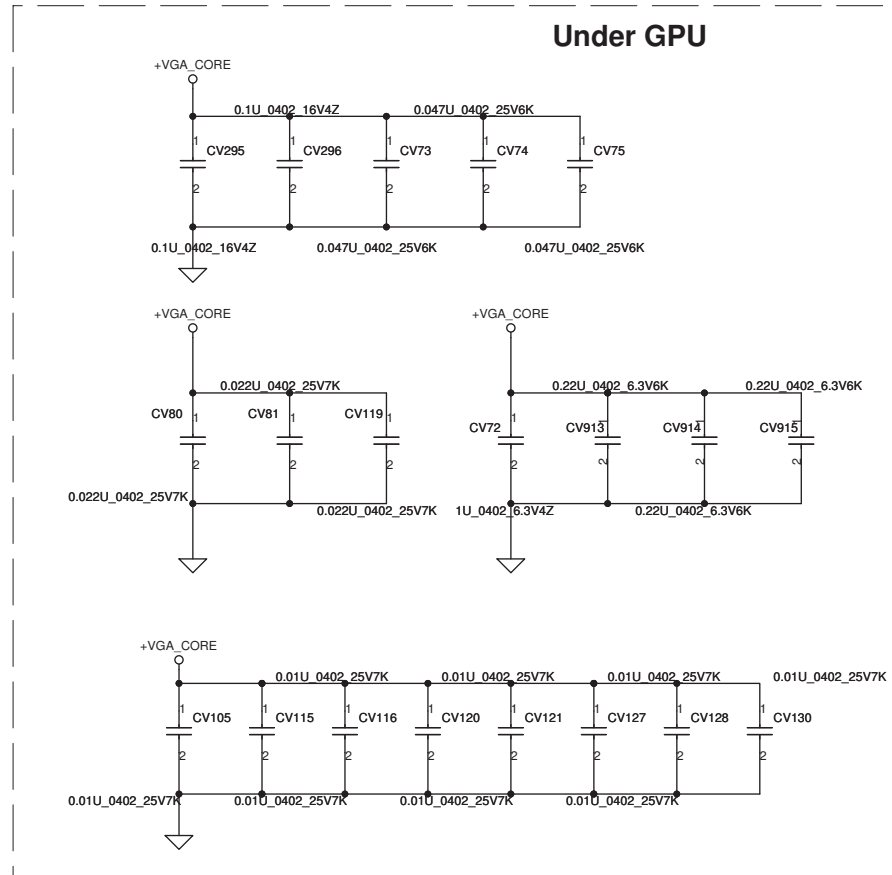
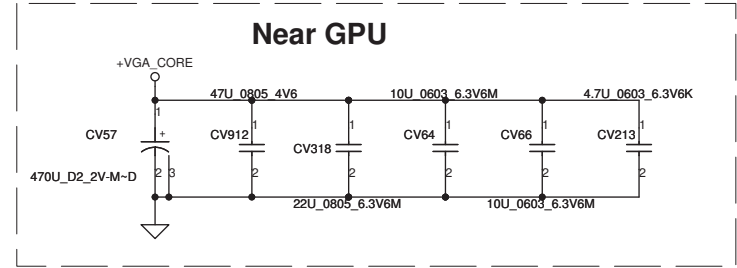
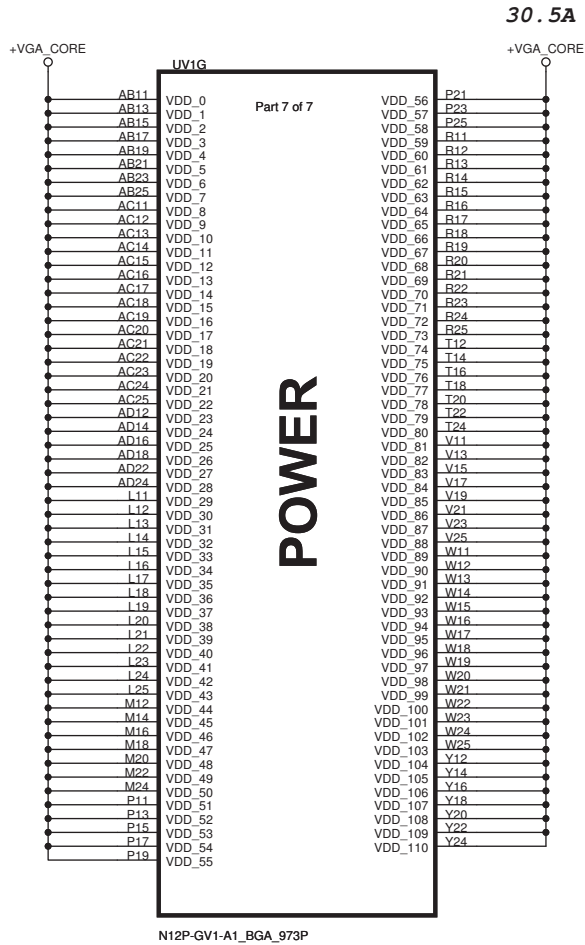
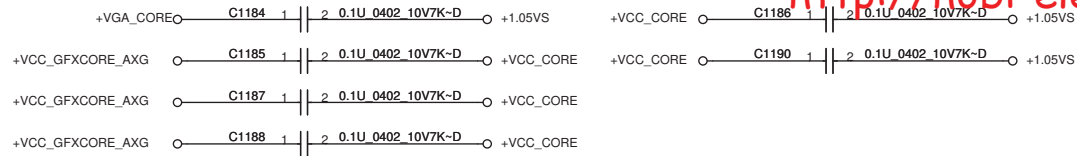


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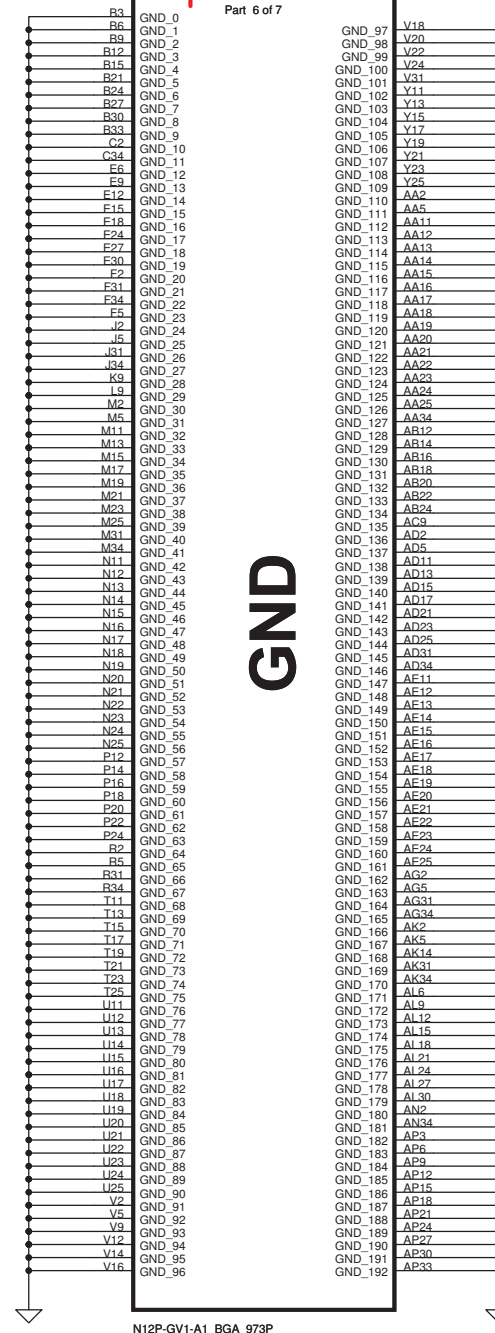
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Title	VGA(1/12)-PCIE/DAC/GPIO
Size	Document Number
Rev	LA-6961P
Date	Monday, January 24, 2011
Sheet	30 of 54



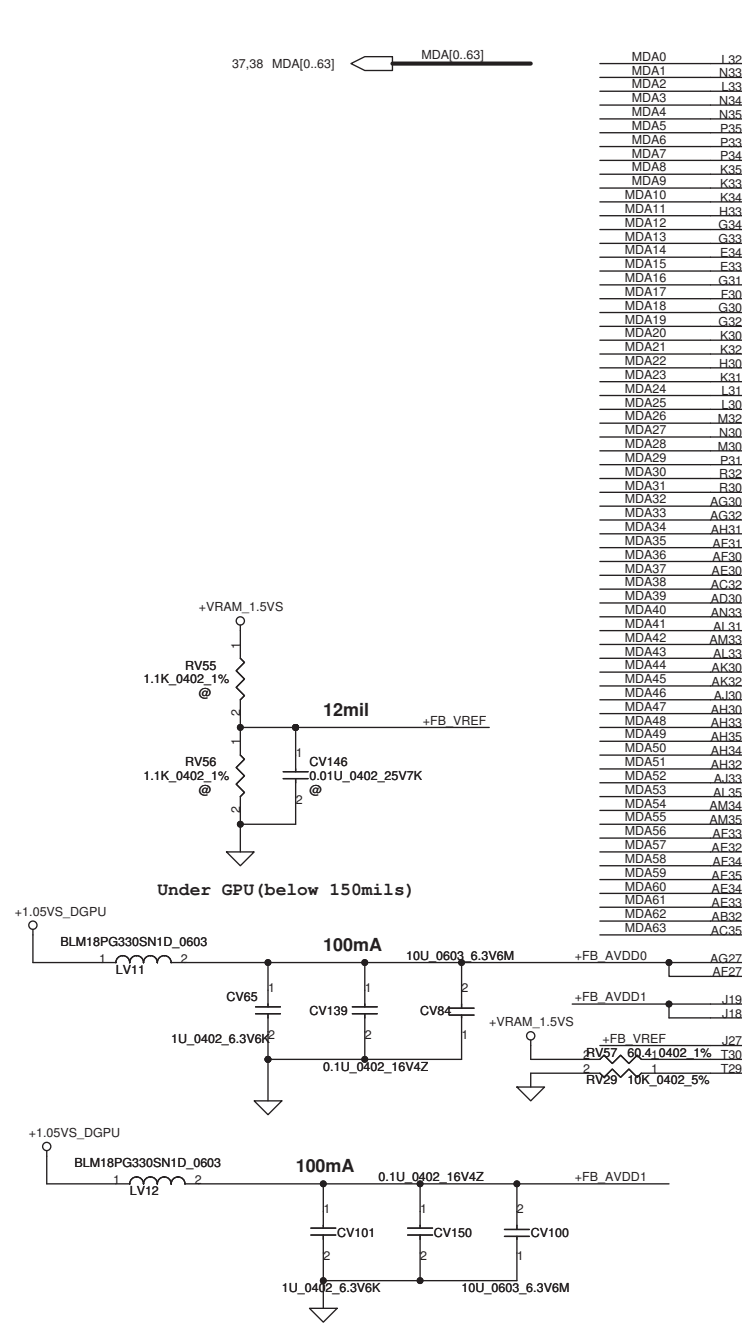
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								LA-6961P		0.4
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				Size	Document Number	Rev
					LA-6961P	0.4
				Date:	Monday, January 24, 2011	Sheet 32 of 54



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					LA-6961P
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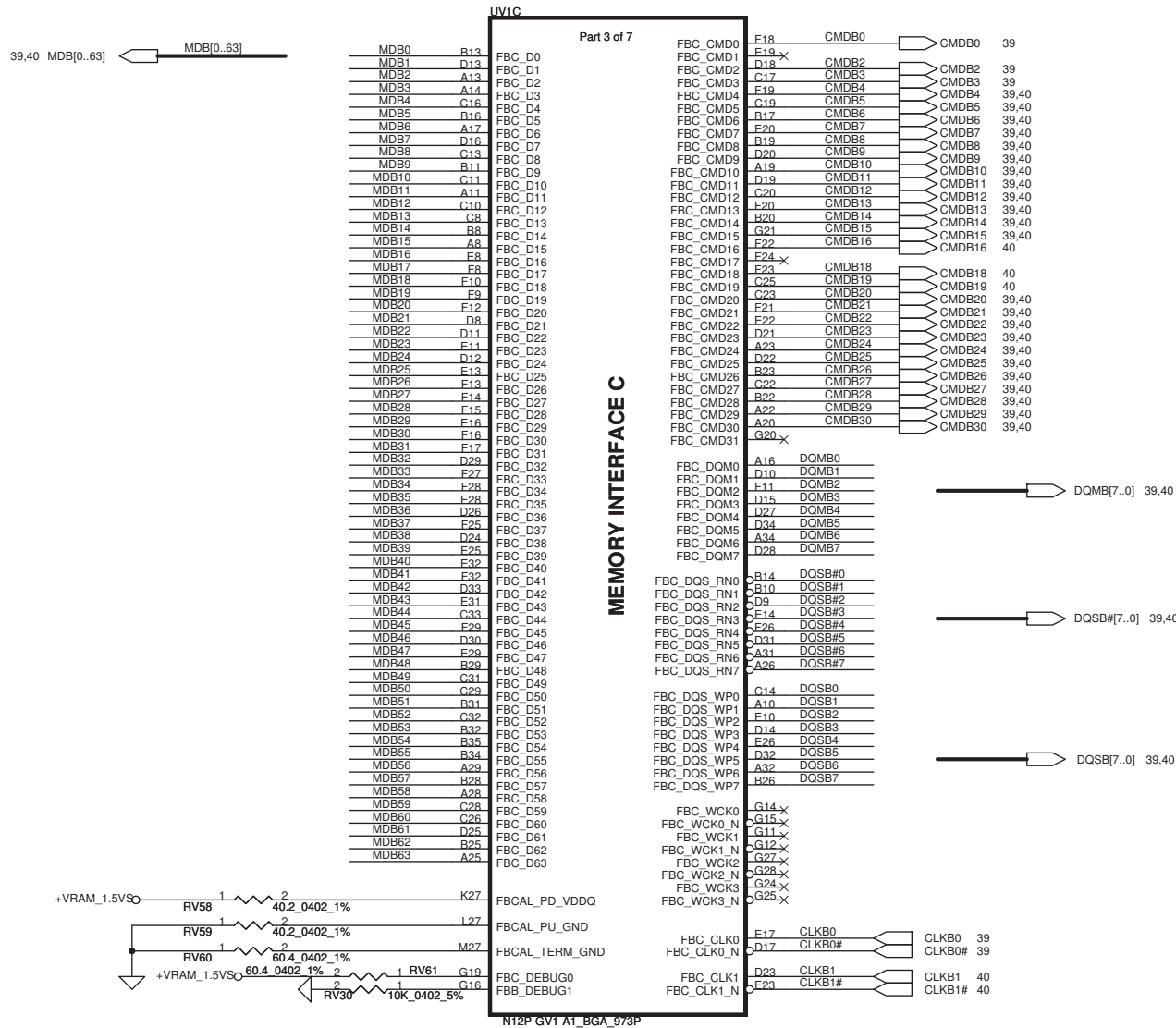


Part 2 of 7

MDA0	I32	FBA D0
MDA1	N33	FBA D1
MDA2	L33	FBA D2
MDA3	N34	FBA D3
MDA4	P35	FBA D4
MDA5	P35	FBA D5
MDA6	P33	FBA D6
MDA7	P34	FBA D7
MDA8	K35	FBA D8
MDA9	K33	FBA D9
MDA10	K34	FBA D10
MDA11	H33	FBA D11
MDA12	G34	FBA D12
MDA13	G33	FBA D13
MDA14	F34	FBA D14
MDA15	F33	FBA D15
MDA16	G31	FBA D16
MDA17	F30	FBA D17
MDA18	G30	FBA D18
MDA19	G32	FBA D19
MDA20	K30	FBA D20
MDA21	K32	FBA D21
MDA22	H30	FBA D22
MDA23	K31	FBA D23
MDA24	L31	FBA D24
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MDA26	M32	FBA D26
MDA27	N30	FBA D27
MDA28	M30	FBA D28
MDA29	P31	FBA D29
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MDA60	AE34	FBA D60
MDA61	AE33	FBA D61
MDA62	AB32	FBA D62
MDA63	AC35	FBA D63

MEMORY INTERFACE

FBA_CMD0	U30	CMDA0	CMDA0	37
FBA_CMD1	V30-X	CMDA2	CMDA2	37
FBA_CMD2	U31	CMDA3	CMDA3	37
FBA_CMD3	V32	CMDA4	CMDA4	37,38
FBA_CMD4	T35	CMDA5	CMDA5	37,38
FBA_CMD5	W32	CMDA6	CMDA6	37,38
FBA_CMD6	W33	CMDA7	CMDA7	37,38
FBA_CMD7	W31	CMDA8	CMDA8	37,38
FBA_CMD8	W34	CMDA9	CMDA9	37,38
FBA_CMD9	U34	CMDA10	CMDA10	37,38
FBA_CMD10	U35	CMDA11	CMDA11	37,38
FBA_CMD11	U32	CMDA12	CMDA12	37,38
FBA_CMD12	T34	CMDA13	CMDA13	37,38
FBA_CMD13	T33	CMDA14	CMDA14	37,38
FBA_CMD14	W30	CMDA15	CMDA15	37,38
FBA_CMD15	AB30	CMDA16	CMDA16	38
FBA_CMD16	AA30-X	CMDA18	CMDA18	38
FBA_CMD17	AB31	CMDA19	CMDA19	38
FBA_CMD18	AA32	CMDA20	CMDA20	37,38
FBA_CMD19	AB33	CMDA21	CMDA21	37,38
FBA_CMD20	Y32	CMDA22	CMDA22	37,38
FBA_CMD21	Y33	CMDA23	CMDA23	37,38
FBA_CMD22	AB34	CMDA24	CMDA24	37,38
FBA_CMD23	AB35	CMDA25	CMDA25	37,38
FBA_CMD24	Y35	CMDA26	CMDA26	37,38
FBA_CMD25	W35	CMDA27	CMDA27	37,38
FBA_CMD26	Y34	CMDA28	CMDA28	37,38
FBA_CMD27	Y31	CMDA29	CMDA29	37,38
FBA_CMD28	Y30	CMDA30	CMDA30	37,38
FBA_CMD29	W29	CMDA30	CMDA30	37,38
FBA_CMD30	Y29-X			
FBA_CMD31				
FBA_CMD32	P32	DQMA0	DQMA[7..0]	37,38
FBA_CMD33	H34	DQMA1		
FBA_CMD34	J30	DQMA2		
FBA_CMD35	P30	DQMA3		
FBA_CMD36	AE32	DQMA4		
FBA_CMD37	AL32	DQMA5		
FBA_CMD38	AL34	DQMA6		
FBA_CMD39	AE35	DQMA7		
FBA_CMD40				
FBA_CMD41	J35	DQSA#0		
FBA_CMD42	G35	DQSA#1		
FBA_CMD43	H31	DQSA#2		
FBA_CMD44	M32	DQSA#3		
FBA_CMD45	AD32	DQSA#4		
FBA_CMD46	AI31	DQSA#5		
FBA_CMD47	AI35	DQSA#6		
FBA_CMD48	AC34	DQSA#7		
FBA_CMD49				
FBA_CMD50	L34	DQSA0		
FBA_CMD51	H35	DQSA1		
FBA_CMD52	J32	DQSA2		
FBA_CMD53	N31	DQSA3		
FBA_CMD54	AE31	DQSA4		
FBA_CMD55	AI32	DQSA5		
FBA_CMD56	AI34	DQSA6		
FBA_CMD57	AC33	DQSA7		
FBA_CMD58				
FBA_CMD59	P29-X			
FBA_CMD60	B29-X			
FBA_CMD61	L29-X			
FBA_CMD62	M29-X			
FBA_CMD63	AG29			
FBA_CMD64	AH29			
FBA_CMD65	AD29			
FBA_CMD66	AE29			
FBA_CMD67				
FBA_CMD68				
FBA_CMD69				
FBA_CMD70				
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FBA_CMD311				
FBA_CMD312				



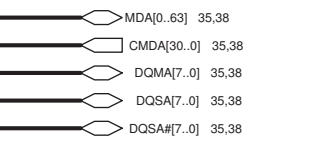
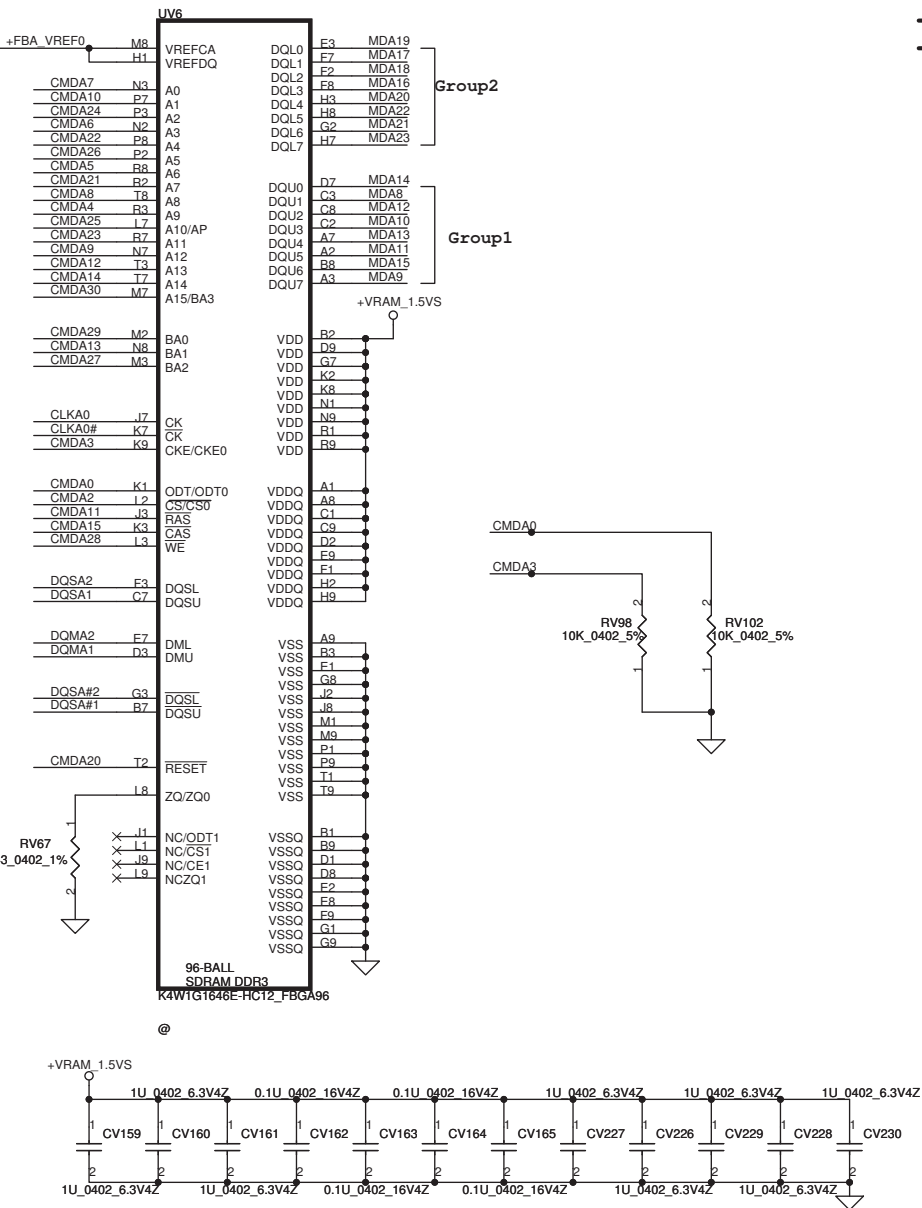
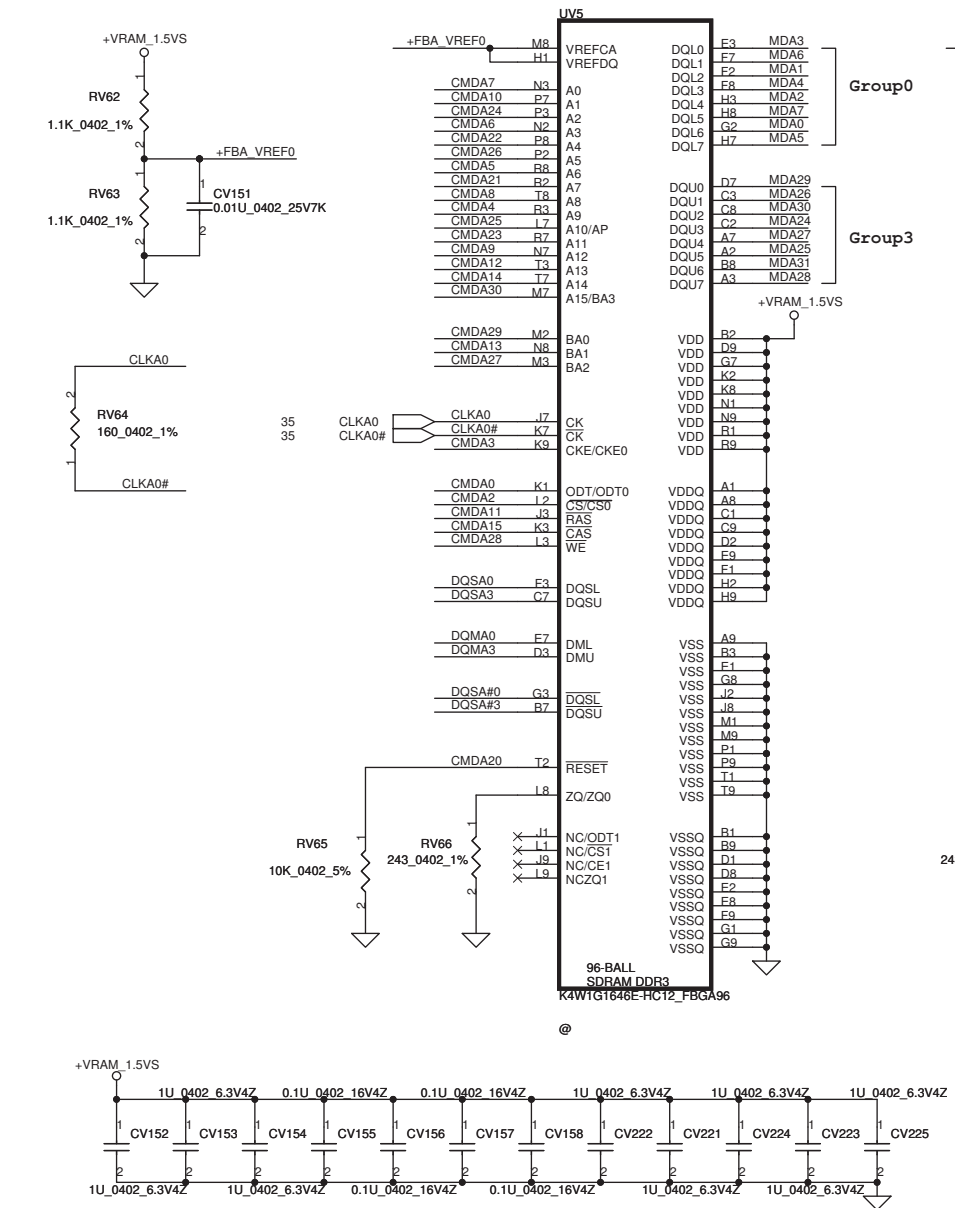
Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Title	
Issued Date	2010/05/27	Deciphered Date	2011/07/06	VGA(7/12)-MEM Interface C	
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Memory Partition A - Lower 32 bits

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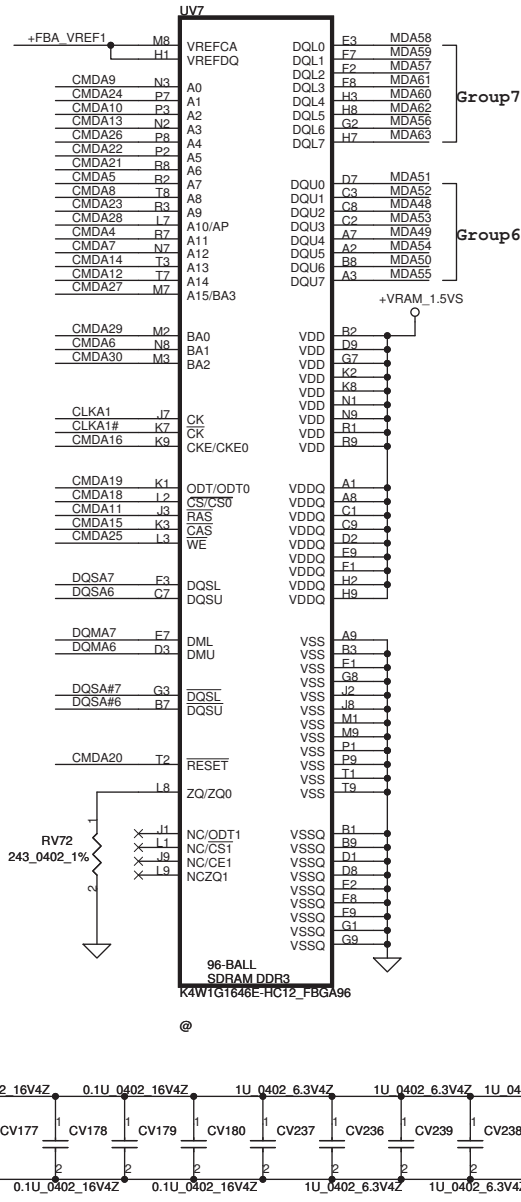
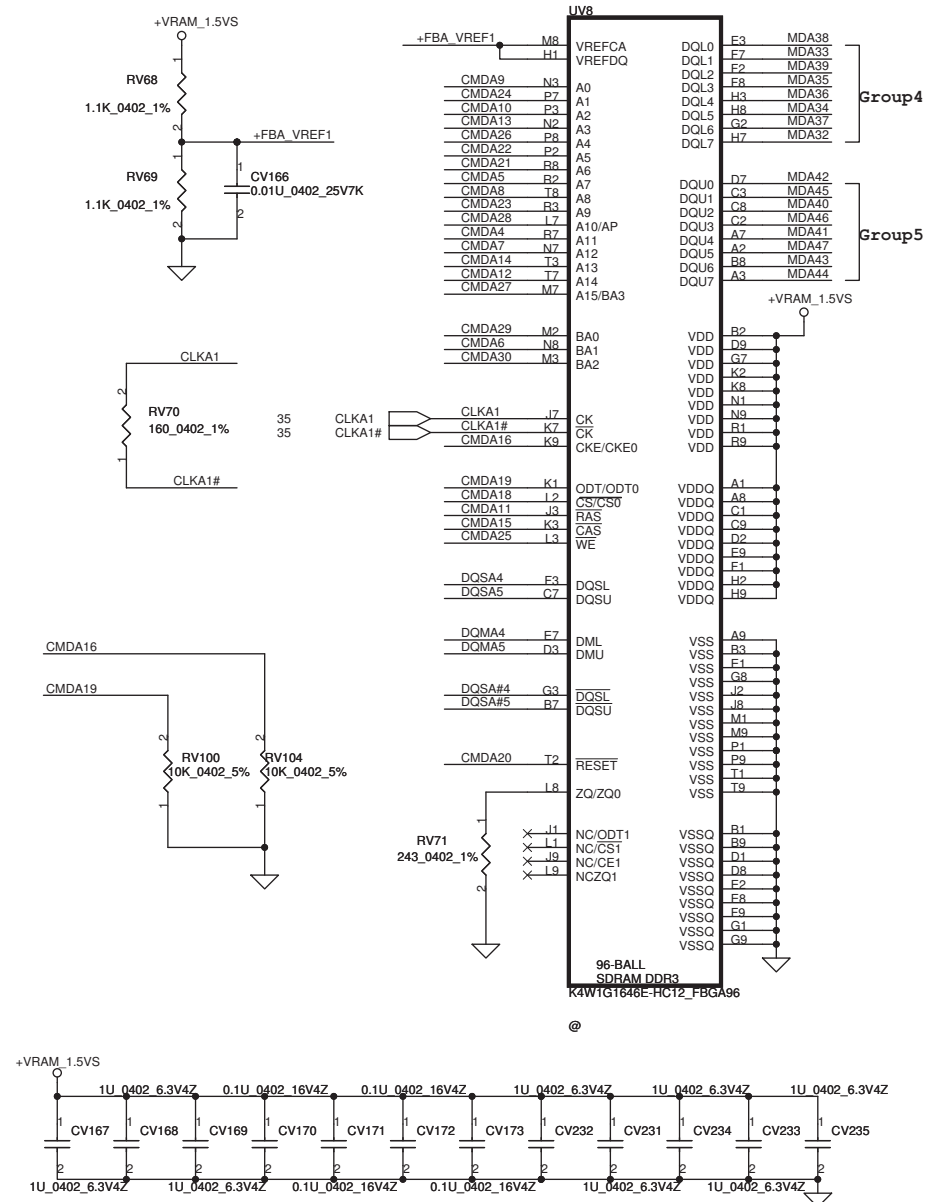


Mode E - Mirror Mode Mapping

Address	DATA	Bus
CMD8	CKE_L	35..63
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition A - Upper 32 bits

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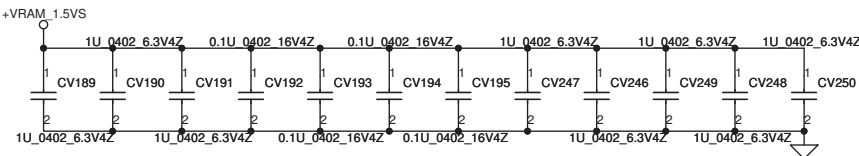
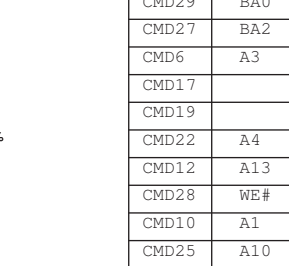
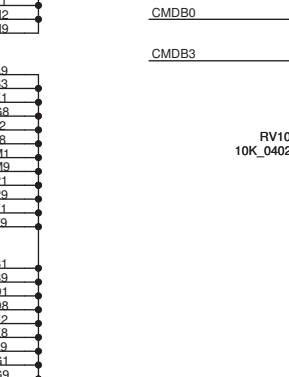


Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification				Compal Secret Data				Title			
Issued Date				2010/05/27				Deciphered Date			
2011/07/06				2011/07/06				VGA(9/12)-VRAM A Upper			
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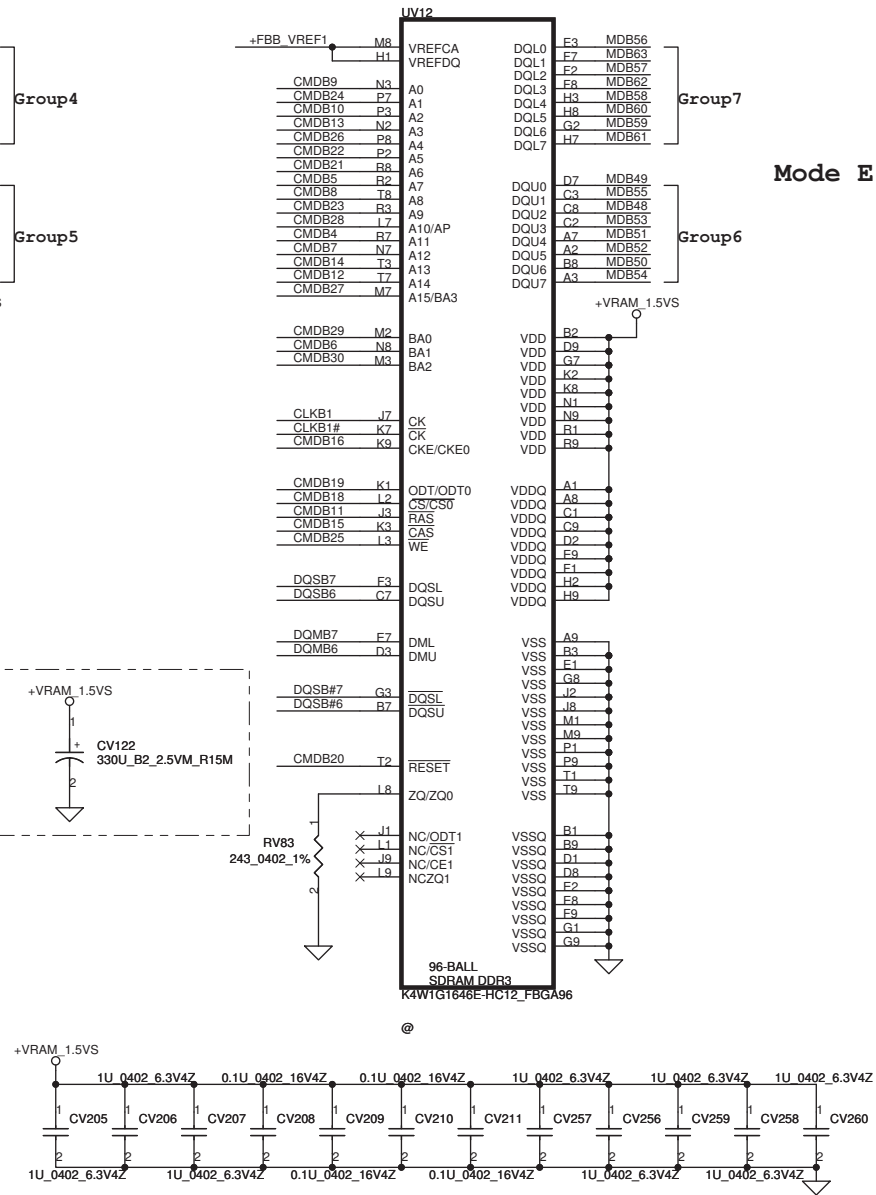
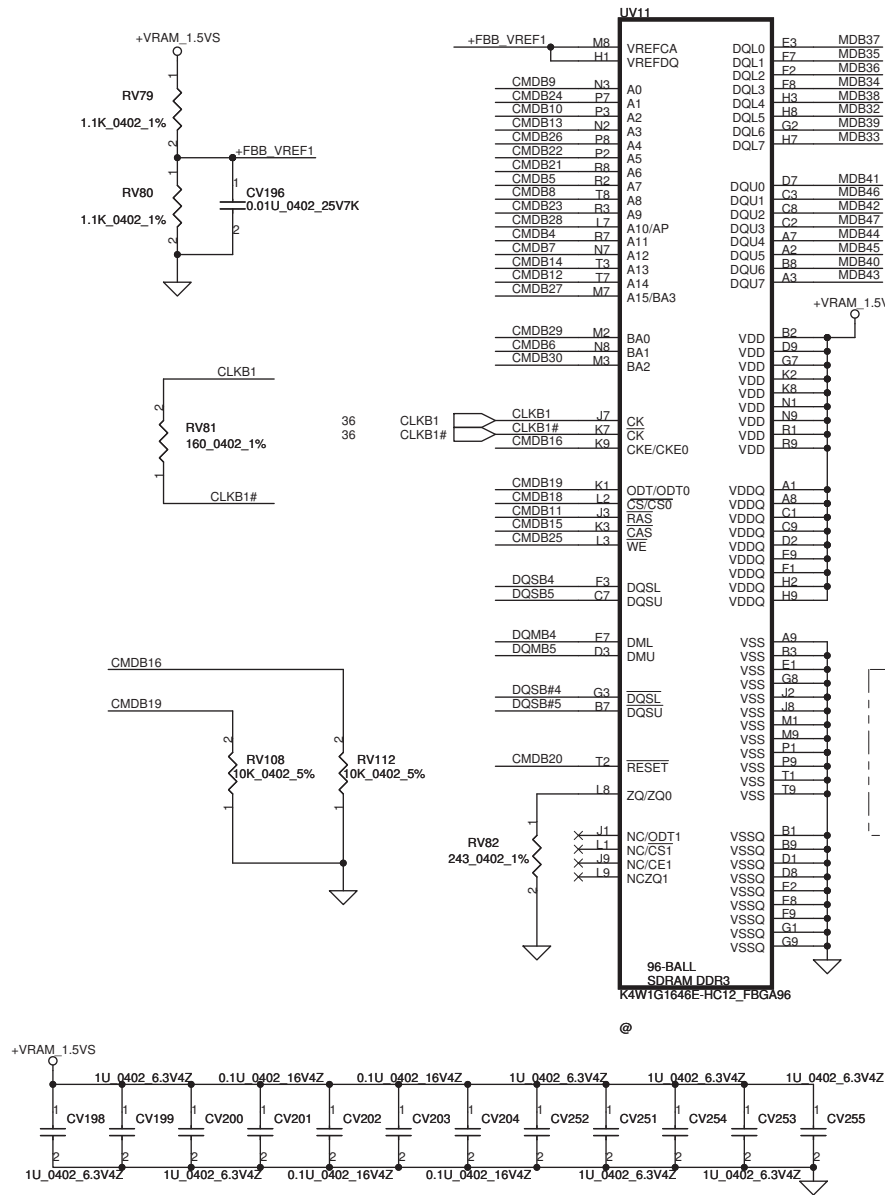
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	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition C - Upper 32 bits

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Mode E - Mirror Mode Mapping

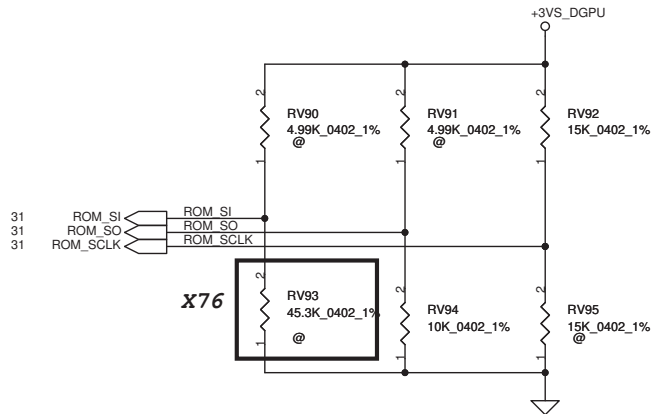
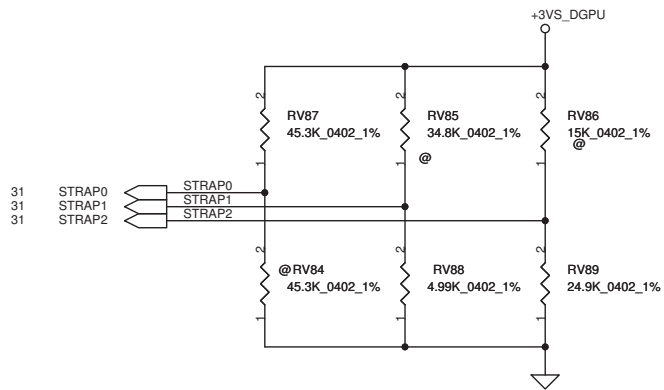
Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data				Compal Electronics, Inc.				
Issued Date		2010/05/27		Deciphered Date		2011/07/06		Title		
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								Size	Document Number	Rev
								Custom	LA-6961P	0.4
								Date:	Monday, January 24, 2011	Sheet 40 of 54

Physical Strapping pin	Physical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]
				USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K



N12P-GS-A1 :
ROM_SO : PL-10K
ROM_CLK : PH-15K
ROM_SI : PL45.3K (Samsung 2GB)
Strap 2 : PL-5K
Strap 1 : PH-35K
Strap 0 : PH-45K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646E-HC11 SA000041T00	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	PD 45.3K(SD034453280)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

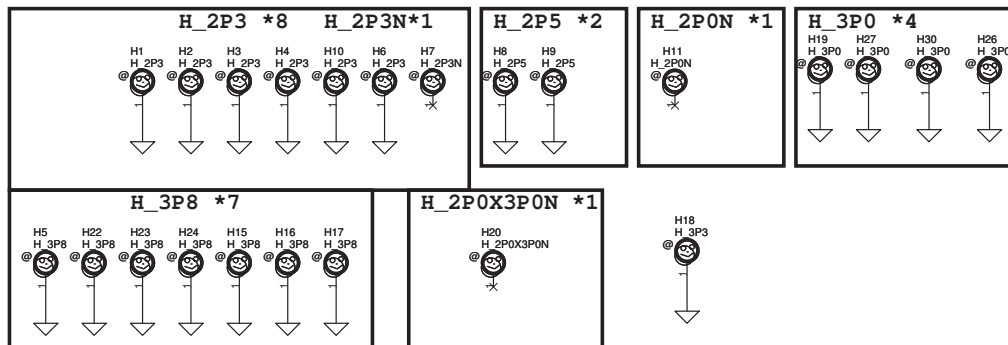
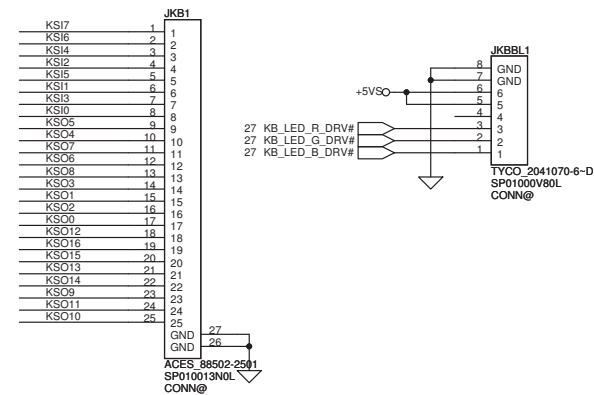
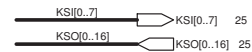
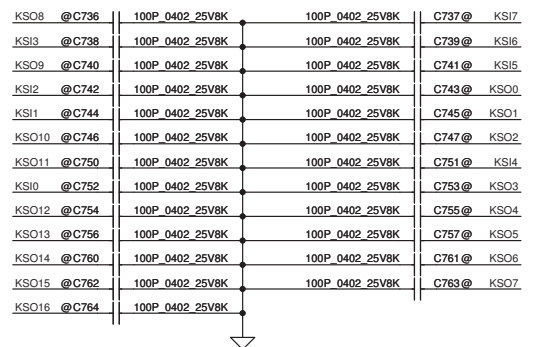
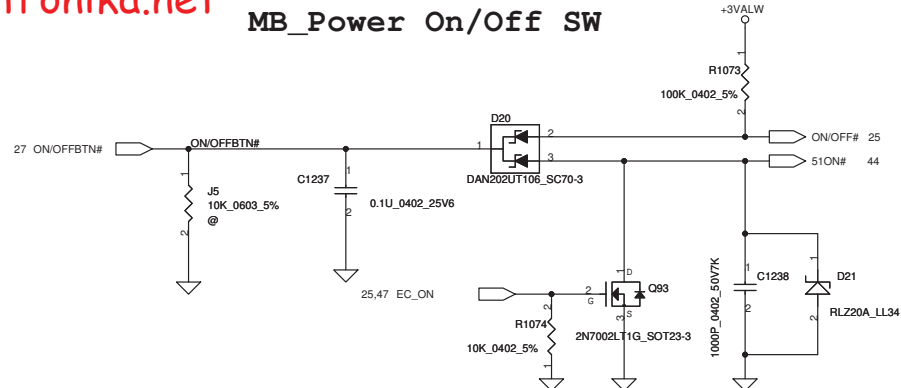
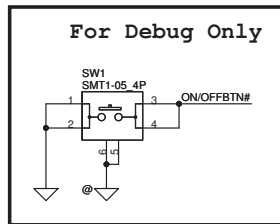
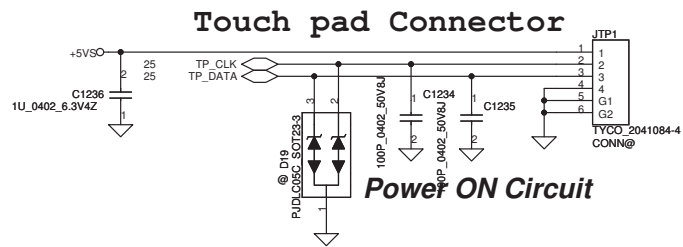
3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

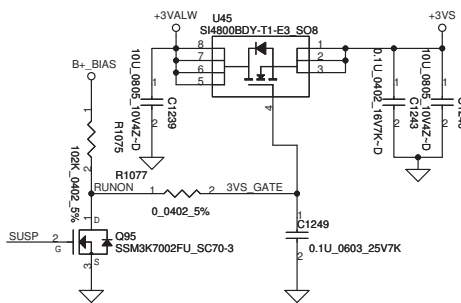
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

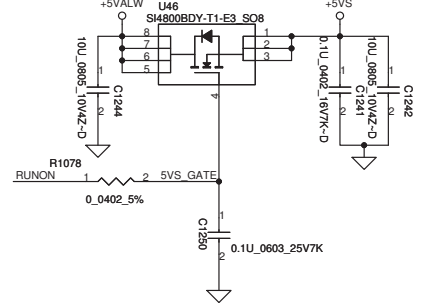


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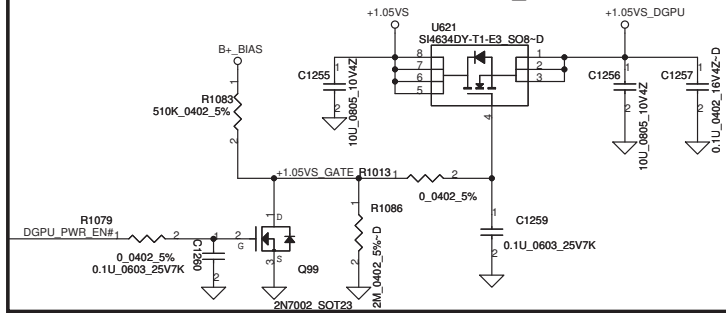
+3VALW to +3VS Transfer



+5VALW to +5VS Transfer

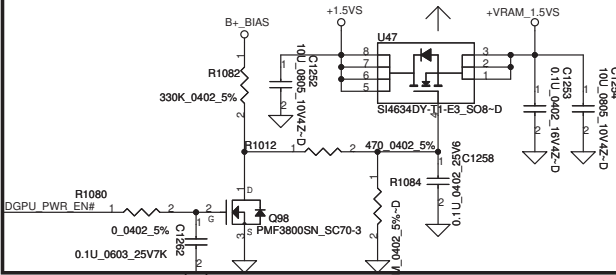


+1.05V to +1.05VS_DGPU Transfer

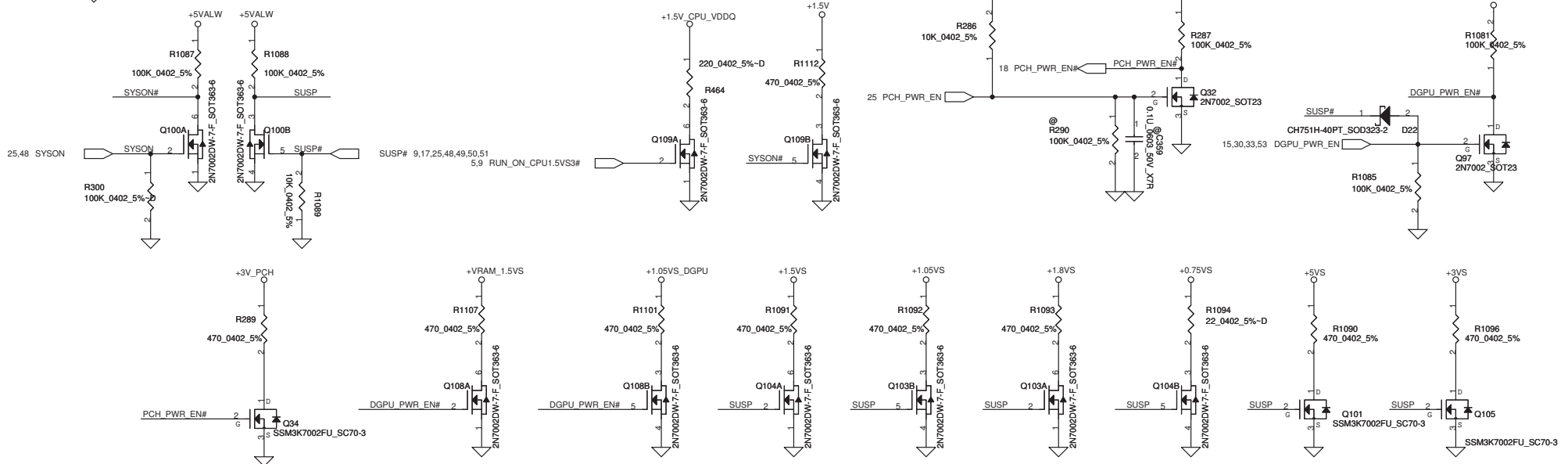
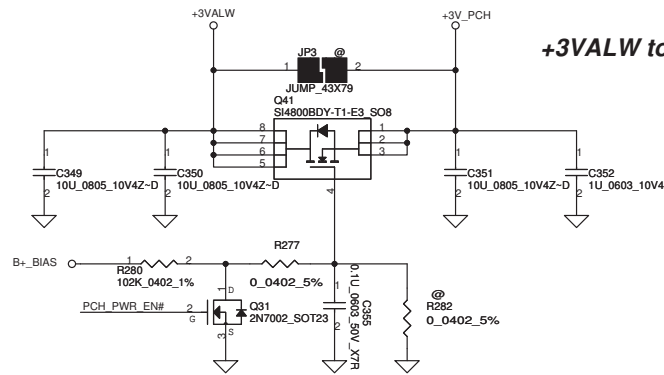


+1.5VS to +1.5VSDGPU Transfer

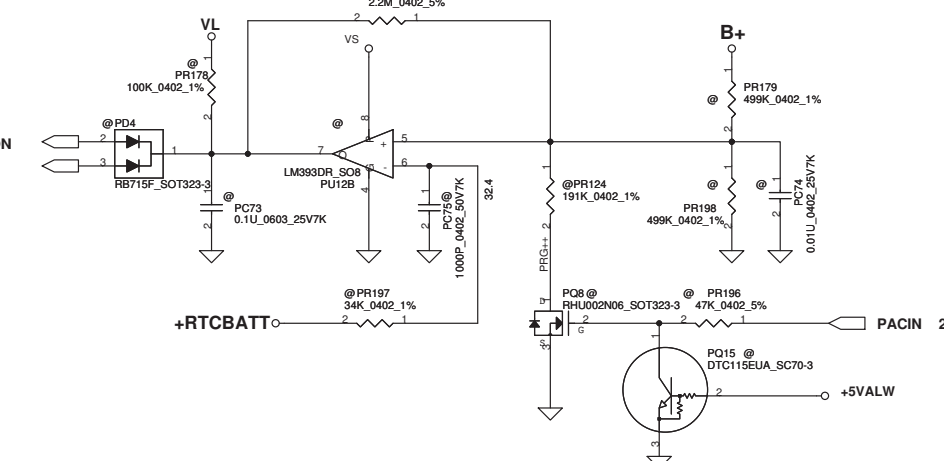
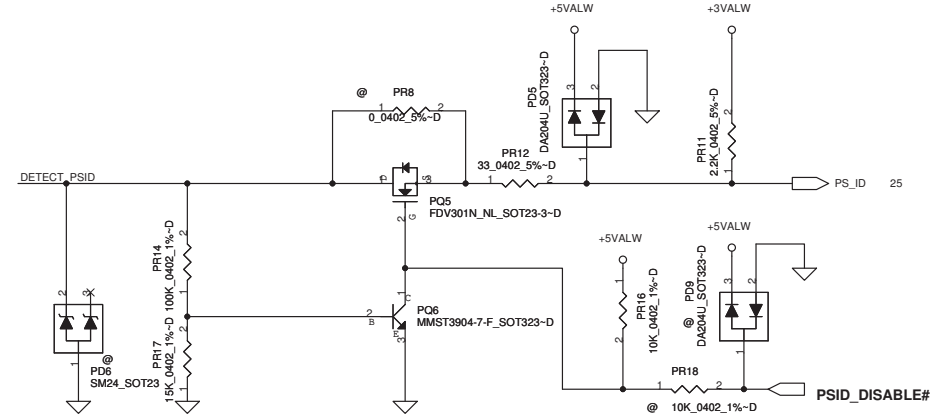
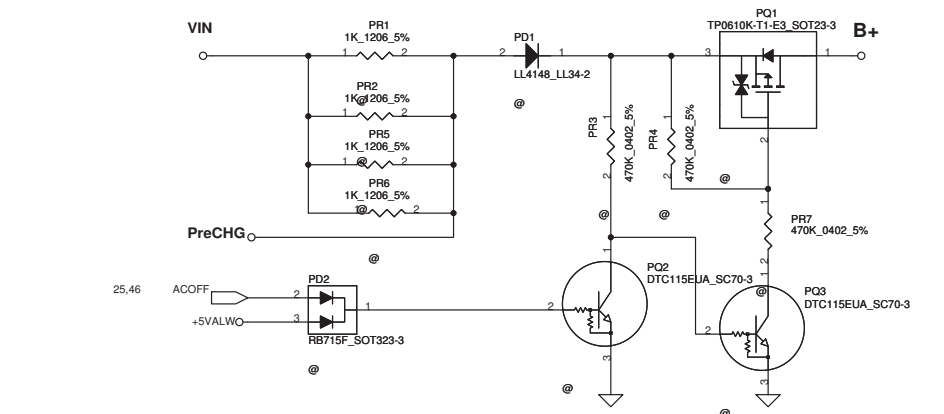
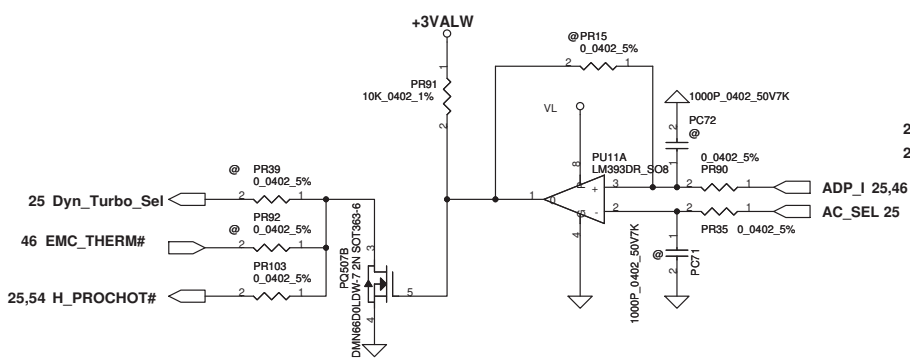
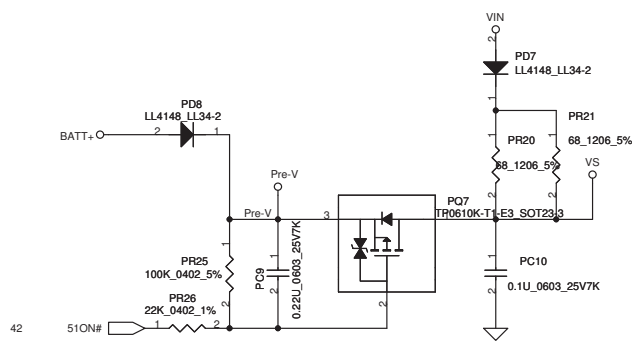
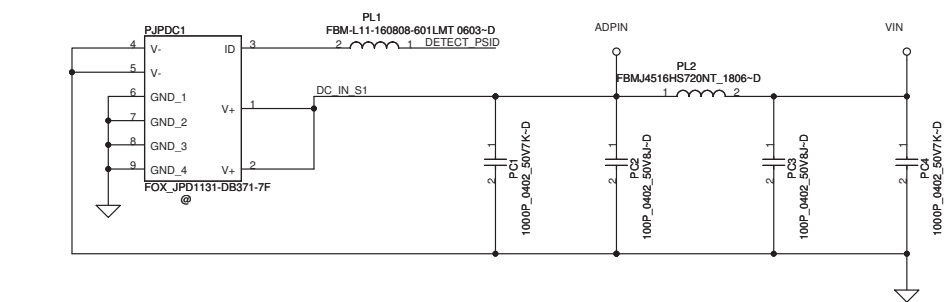
SB54392008L EOL, P/N change to SB54800038L

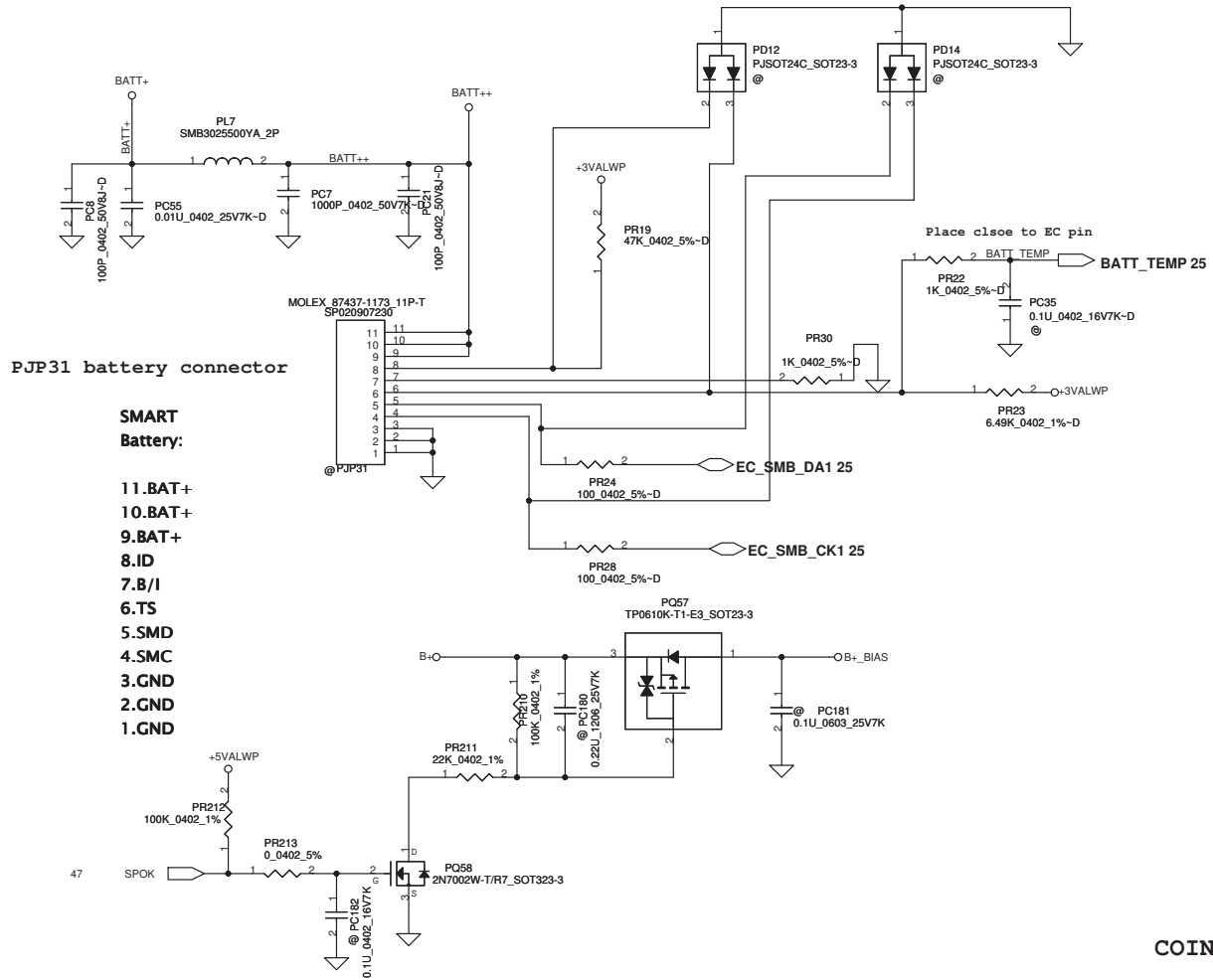


+3VALW to +3V_PCH



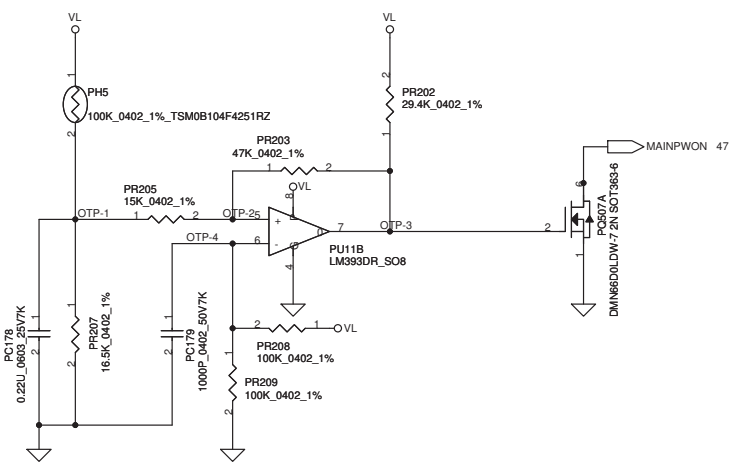
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					Size	Document Number	Rev
					Custom	LA-6961P	0.4
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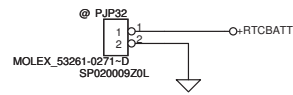


Battery Connect/OTP

PH3 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



COIN RTC Battery

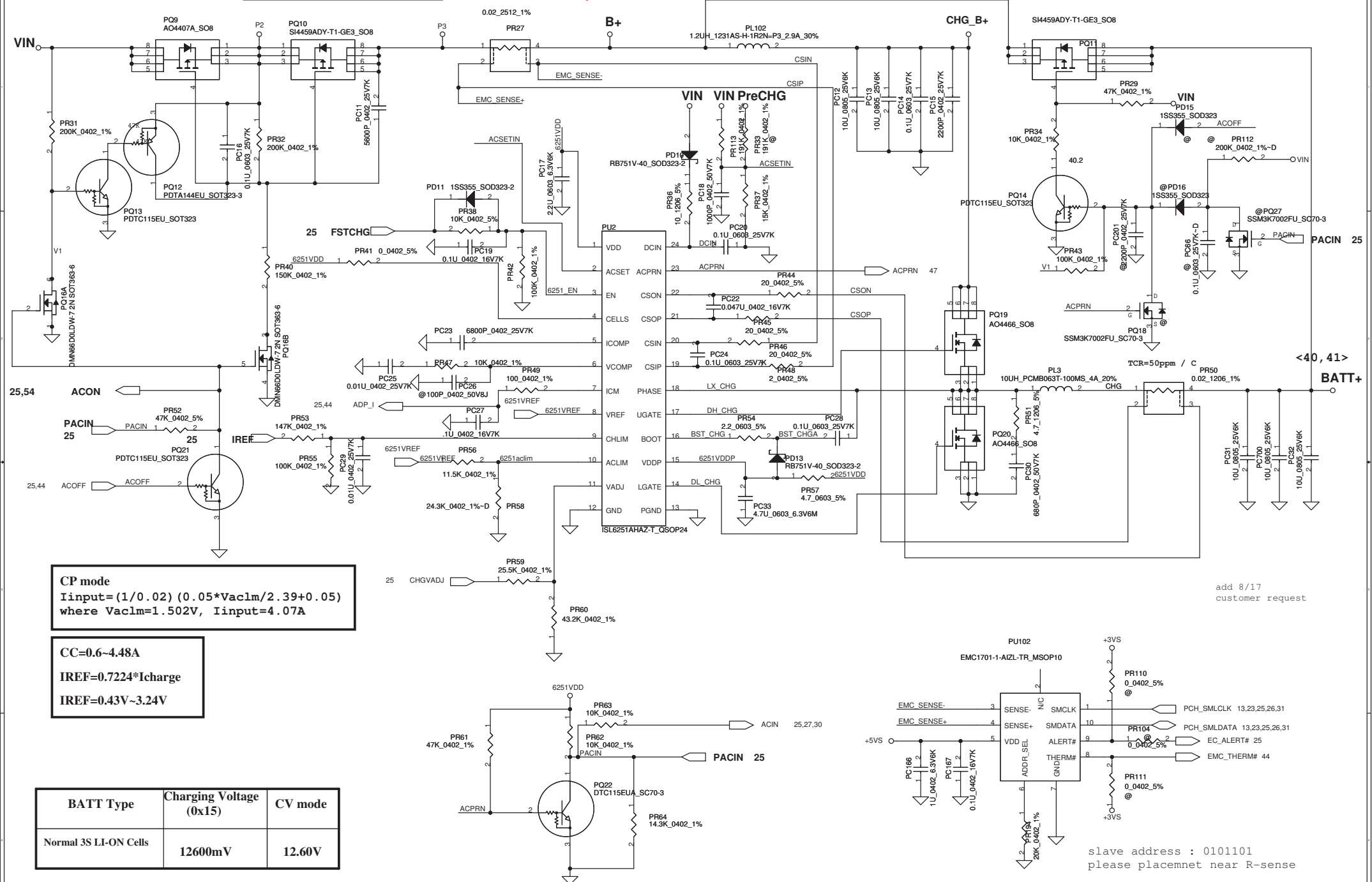


Iada=0~4.74A (90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

<http://hobi-elektronika.net>

CP = 85% Iada ; CP = 4.07A



CP mode
 $I_{input} = (1/0.02) (0.05 \cdot V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6-4.48A
 $I_{REF} = 0.7224 \cdot I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

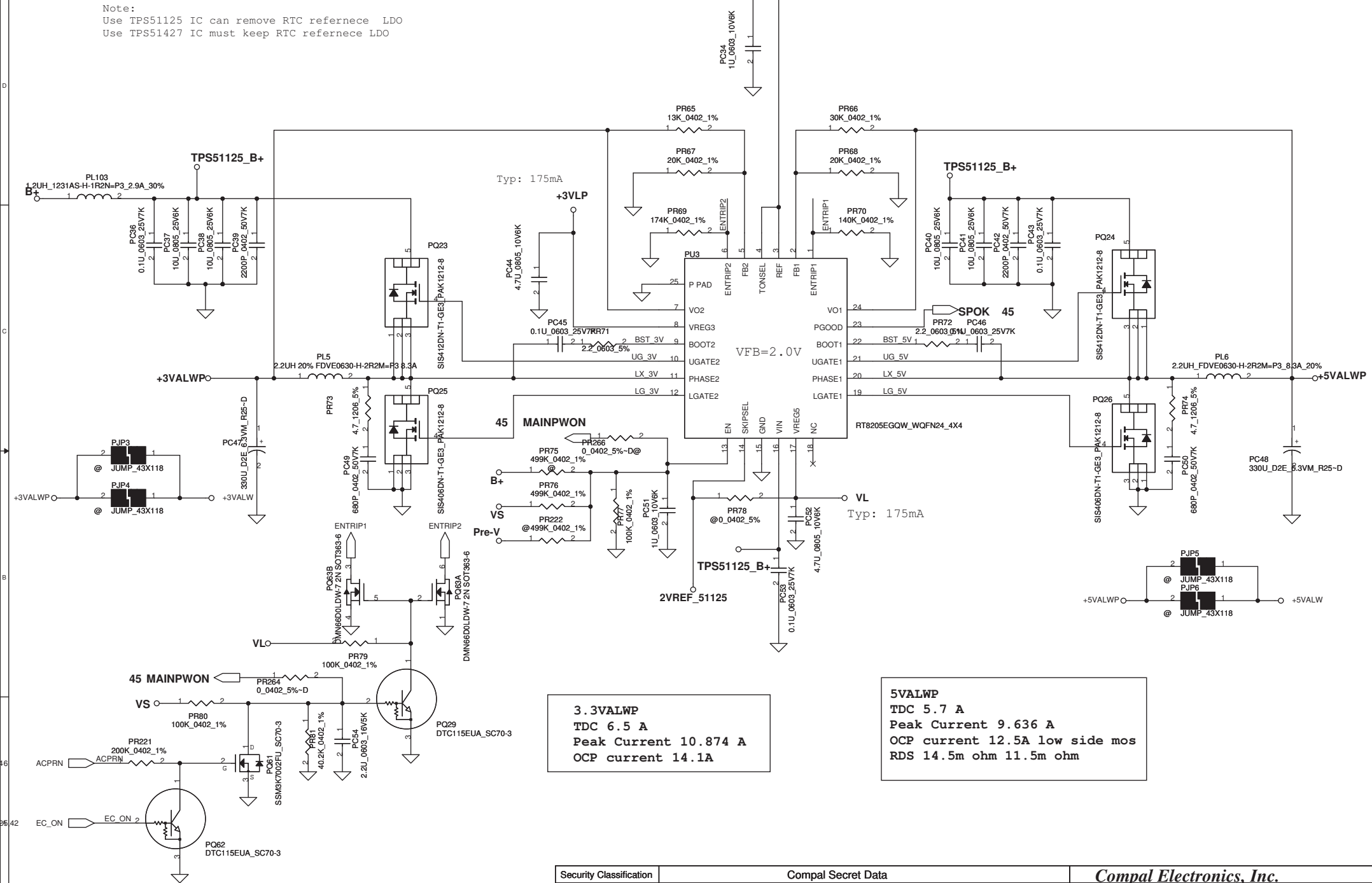
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

add 8/17
customer request

slave address : 0101101
 please placemnet near R-sense

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Size	Custom	Document Number	LA-6961P	Rev	
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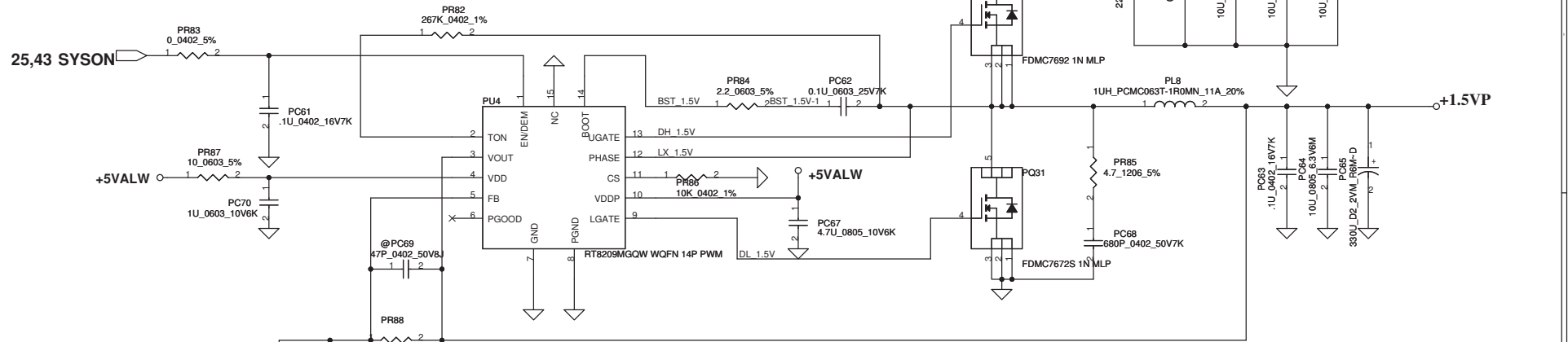
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



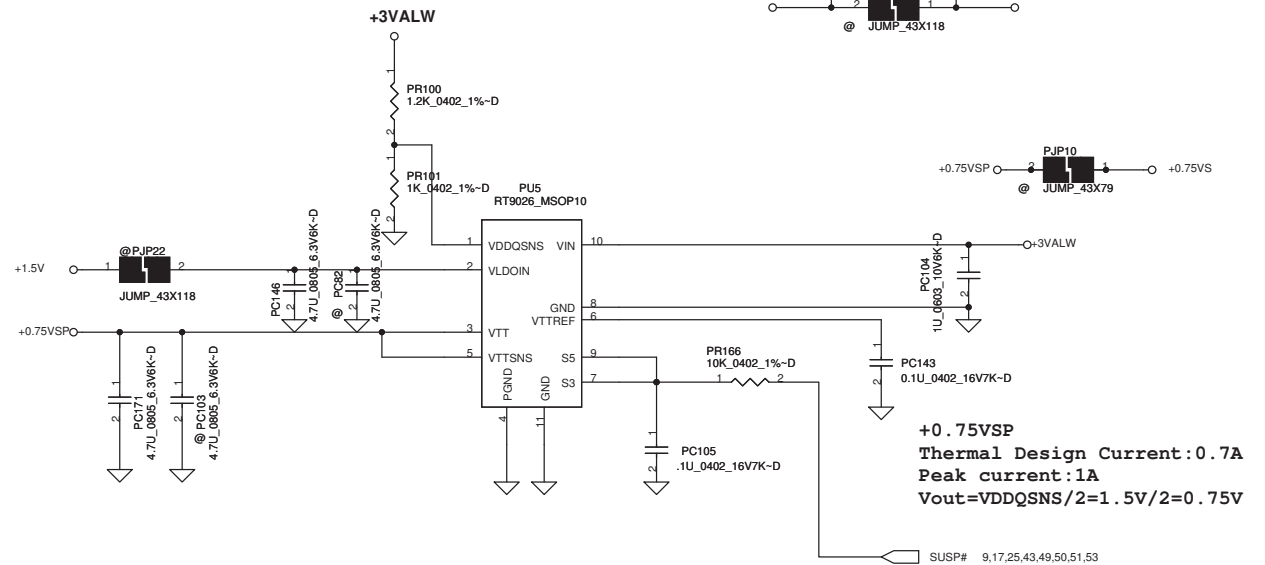
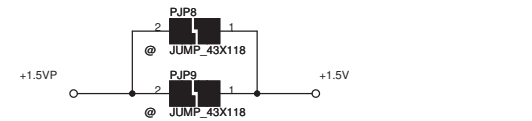
3.3VALWP
TDC 6.5 A
Peak Current 10.874 A
OCP current 14.1A

5VALWP
TDC 5.7 A
Peak Current 9.636 A
OCP current 12.5A low side mos
RDS 14.5m ohm 11.5m ohm

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				Rev	0.1

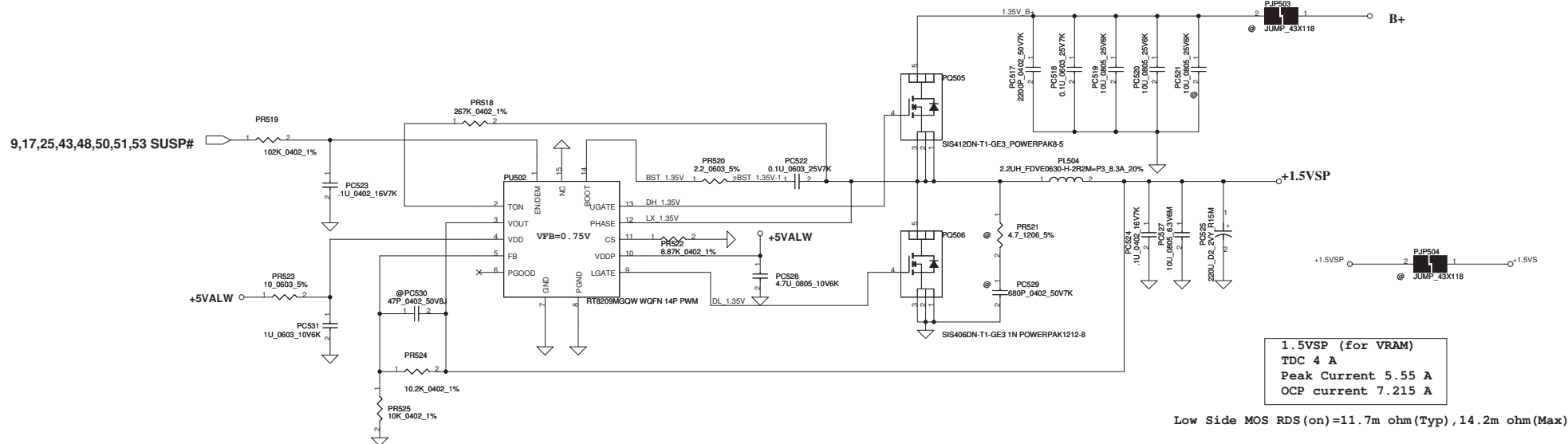


1.5VP
TDC 8.9A
Peak Current 12.72 A
OCF current 16.5A
low side mos RDS 4.5ohm 3.6ohm



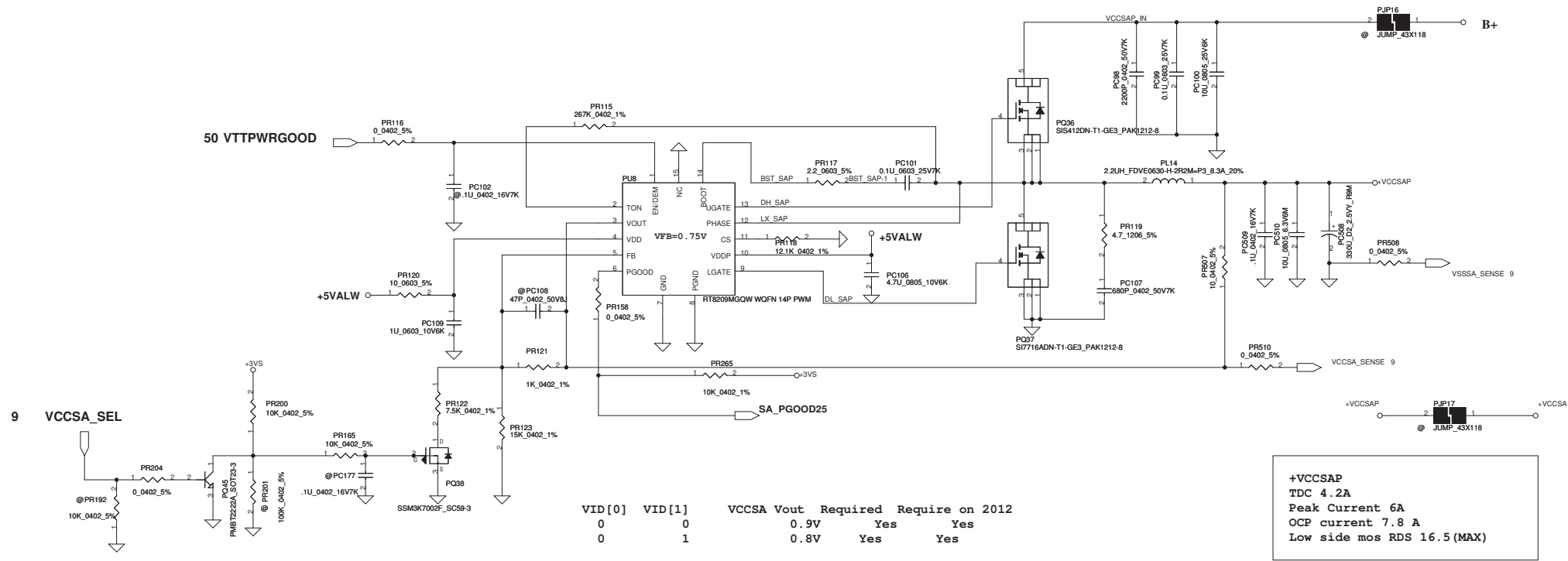
+0.75VSP
Thermal Design Current: 0.7A
Peak current: 1A
Vout=VDDQSNS/2=1.5V/2=0.75V

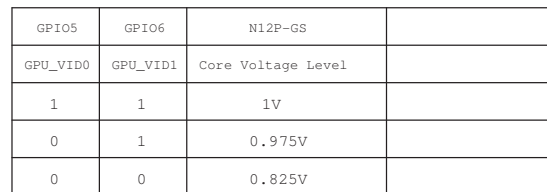
Security Classification	Compal Secret Data		Title	
Issued Date	2009/12/01	Deciphered Date	2010/05/28	PWR-+1.5VP/+0.75VSP
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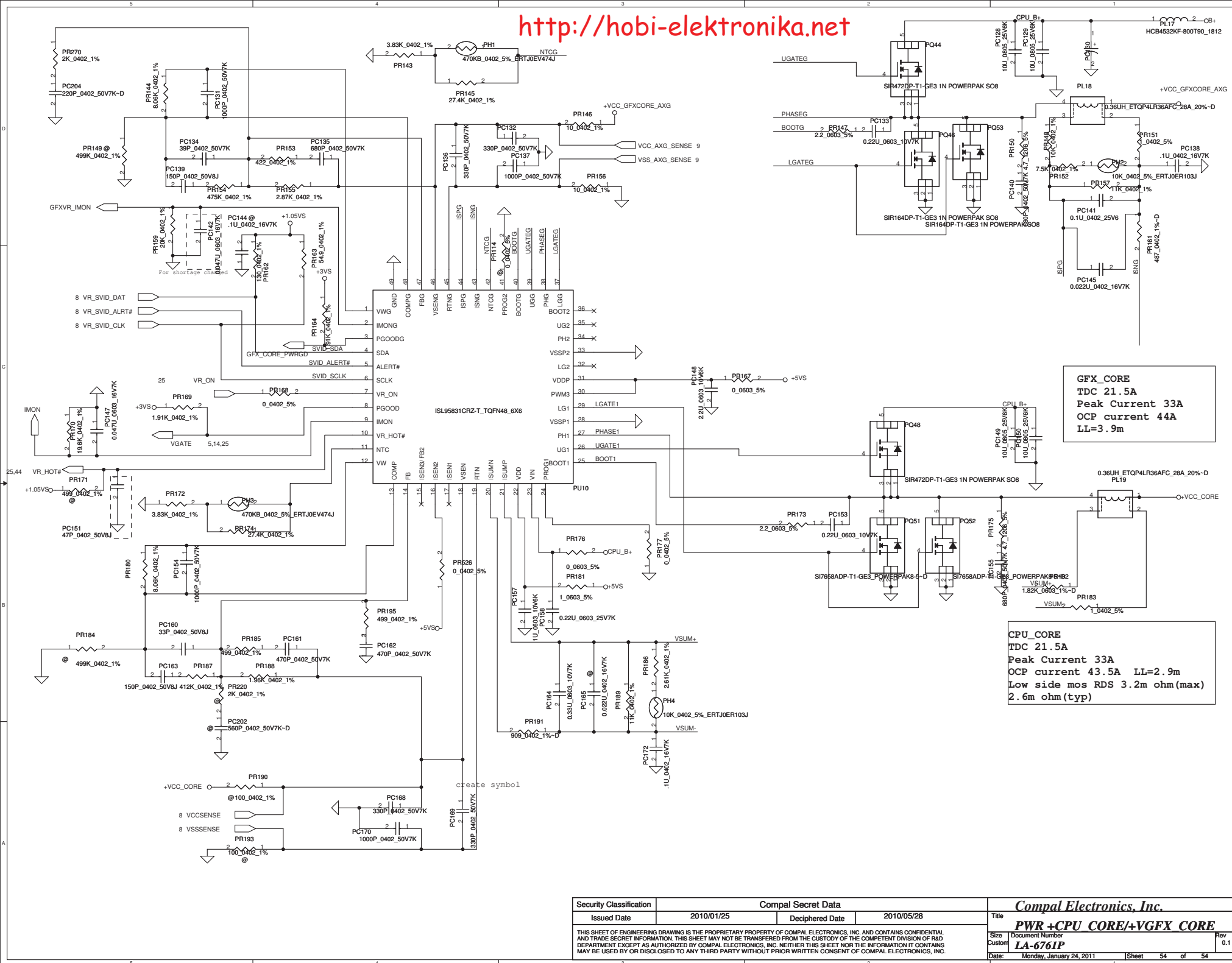
VCCP
TDC 11.5 A
Peak Current 16.458 A
OCP 21.4 currentA
low side mos RDS 4.5 ohm(MAX)
3.6ohm(MAX)

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				Size	Rev
				Custom	0.1
				Document Number	
				LA-6761P	
				Date:	Monday, January 24, 2011
				Sheet	54 of 54

Item	Reason for change	PG#	Modify List	Date	Phase
1	SYSON signal Pull low	43	Add R300	2010/10/15	PT
2	Q21 Reverse	25	Change Q21 DS pin	2010/10/15	PT
3	Fan voltage need to stable	26	Add C1923	2010/10/15	PT
4	Timing change	5	Add RC127,RC128,and Change BOM RC6 resrve	2010/10/15	PT
5	Leakge +3vs	13	Change BOM RH95 to resrve	2010/10/15	PT
6	EA crystal fail	25	Change BOM of C287,C288	2010/10/15	PT
7	EA crystal fail	13	Change BOM of CH23,CH24	2010/10/15	PT
8	EA crystal fail	21	Change BOM of CL18,CL19	2010/10/15	PT
9	High pot	21	Change CL39 to SB120102KIL	2010/10/15	PT
10	DFX request	42	Change JKB1 symbol	2010/10/15	PT
11	ME request	23	Change JBT1 symbol	2010/10/15	PT
12	PCB change version	12	Change BOM UH1 SA00004IV0L	2010/10/15	PT
13	Control LAN LED limiting light	21	Add series connection RL26,RL25,Change BOM RL20 to 0ohm	2010/10/17	PT
14	HuronRiver DG updated for HAD_SYNC pull-down 1M ohm	12	Add RH275 resistor connect to HDA_SYNC_R & GND	2010/10/17	PT
15	Control the LCD sequence for AUO requirement	20	Add R2005,R2006 to reserve EN_INVFWR & +LCDVDD solution	2010/10/17	PT
16	Control the LCD sequence for AUO requirement	20	Add R2013,R2014,Q305 to reserve INVFWR_B+ Discharge Circuit	2010/10/20	PT
17	USB3.0 controller change to UPD720200AF1DAPA	24	Add R1962,R1963 to UPD720200AF1DAPA solution	2010/10/20	PT
18	NV request	28	Change R463,R465 pin2 net to +3VS_BGPV	2010/10/22	PT
19	NV request	33	Change BOM of RV109,RV116 to 1Kohm	2010/10/22	PT
20	The double pull low	29	Change BOM R937 to Resrve	2010/10/22	PT
21	Modify screw H18 for ME request	39	Change H18 symbol	2010/10/22	PT
22	The EC request	25	Change RI095 to EC_CRY2 net,	2010/10/22	PT
23	The EC request	25	Change BOM R253 to 0ohm,RI095 to 100Kohm,C287,C288, XI resrve	2010/10/24	PT
24	The EC request	25	Change BOM R225 to 8.2kohm	2010/10/24	PT
25	The EC request	25	Change R222 to D7I	2010/10/26	PT
26	Intel request	12-19	Change BOM UH1 SA00004IV1L	2010/12/1	ST
27	Changed from +3vs to +valw to fix issue can't wake from S3 by port of USB3.0	24	Change BOM Del R1963 ,Add R1962	2010/12/1	ST
28	NV request	41	Change BOM RV88 to 4.99K ohm	2010/12/1	ST
29	Maximum derateing changed from 12V to 20V	9	Change BOM QC4 to SB00000HK0L	2010/12/1	ST
30	Maximum derateing changed from 2V to 2.5V	9	Change BOM CC176 to SGA00005H0L	2010/12/1	ST
31	EMI request	20	Add L5 to SM01000DH0L	2010/12/6	ST
32	EMI request	20	Change BOM CU63 to 100PF	2010/12/6	ST
33	EMI request	20	Change BOM CI167 to 22PF	2010/12/6	ST
34	GLAN orange LED too dark	21	Change BOM RL26 to 200ohm	2010/12/6	ST
35	The EC request	25	Add C1947 to SB07I200J6L	2010/12/8	ST
36	The safety request	12	Change DH4 pin1,2,3	2010/12/8	ST
37	The USB3_SMI# signal change to GPIO14	15	Change UH1 pin C23 and H15	2010/12/8	ST
38	The DP Power Dongle	29	Add C110	2010/12/8	ST
39	The ME request	8	Change BOM C110 to C112	2010/12/9	ST
40	For ENE EC protect	20	17I2 add D13, R395		
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					Size	Document Number	Rev
						LA-6961P	0.3
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