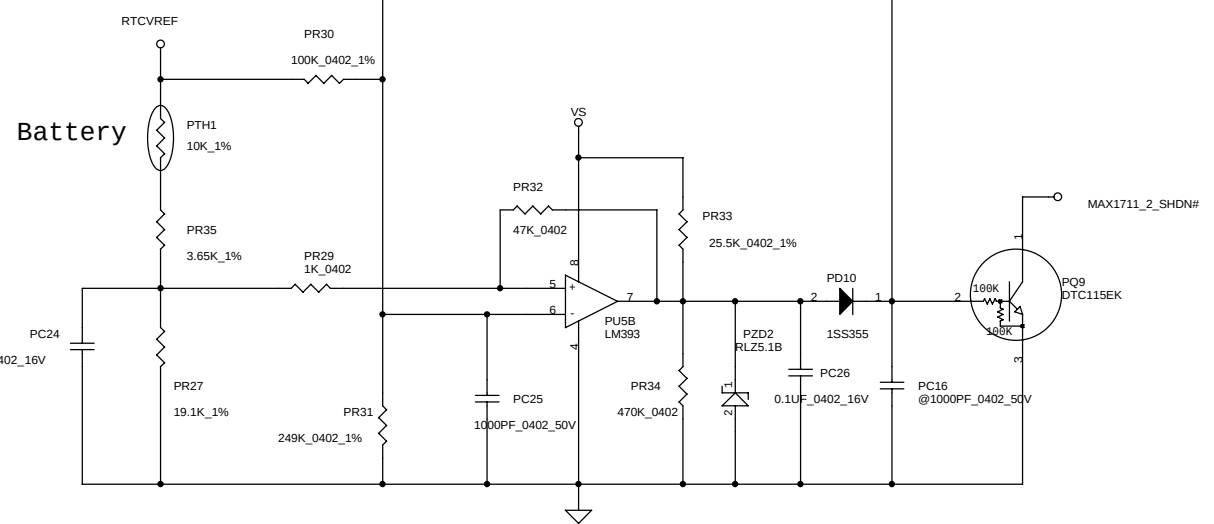
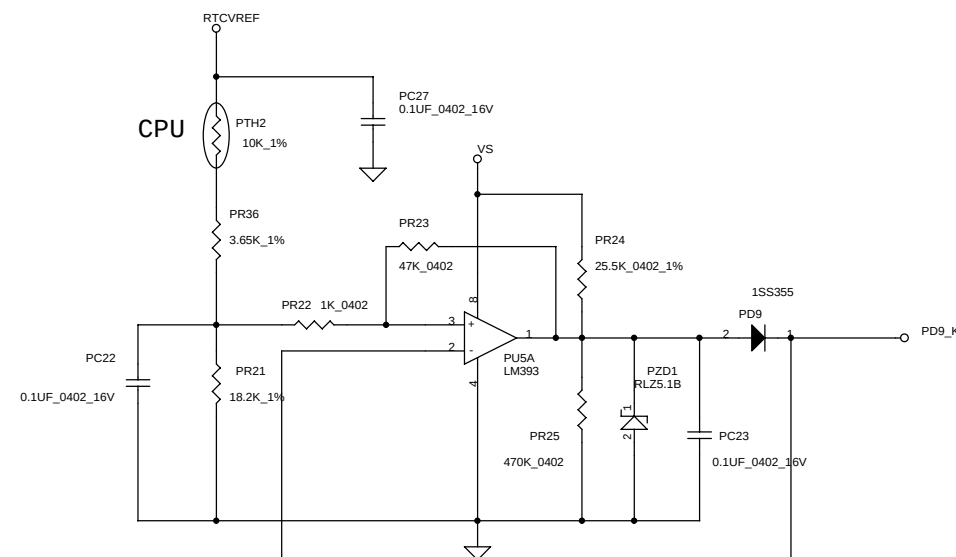
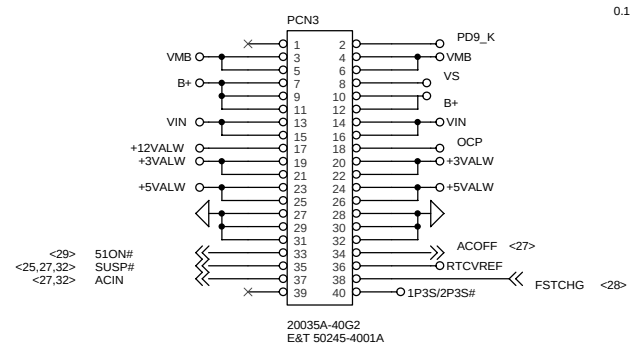
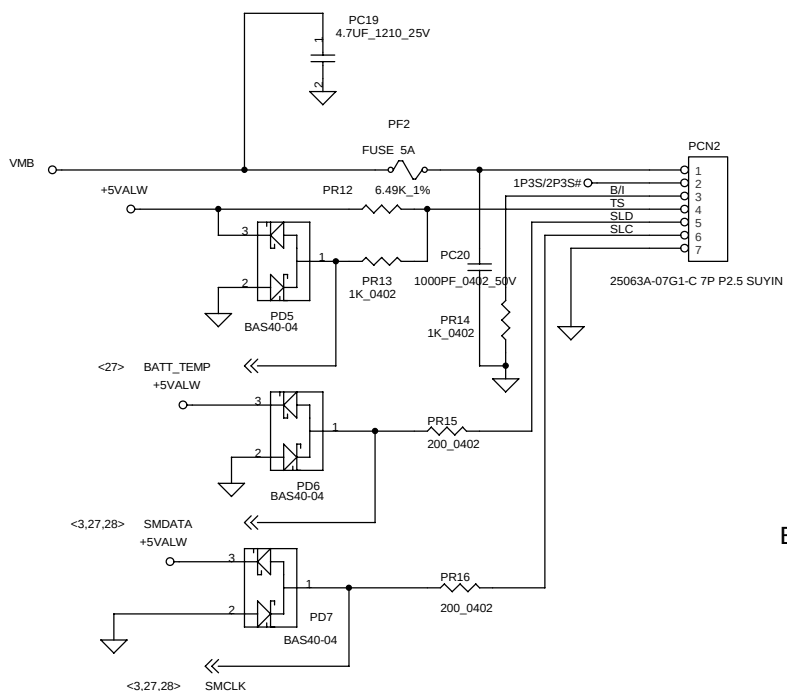
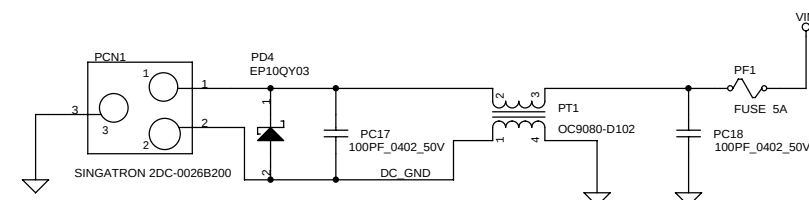




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COMPAL CONFIDENTIAL

MODEL NAME : 888J2 LA-971

REVISION HISTORY

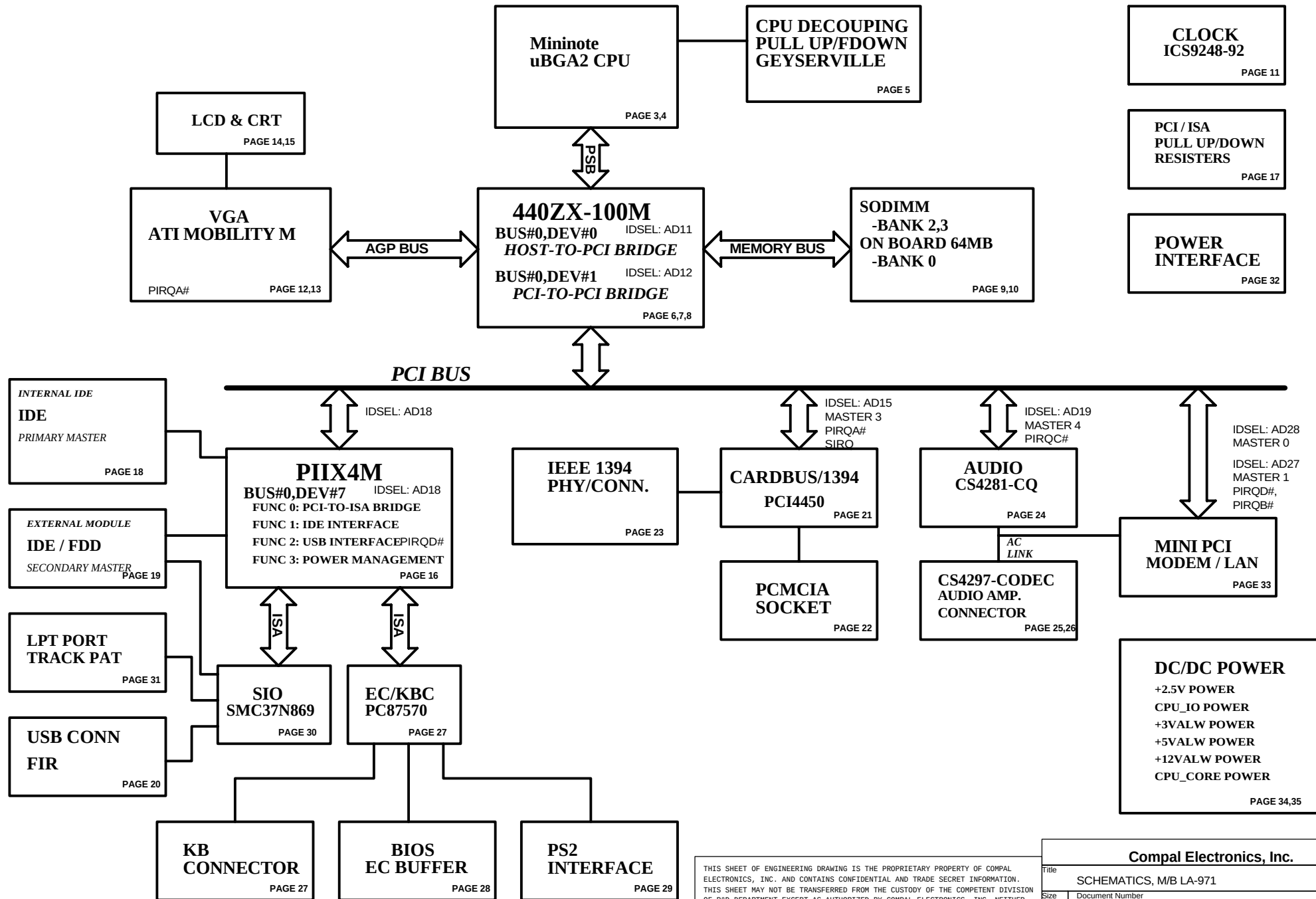
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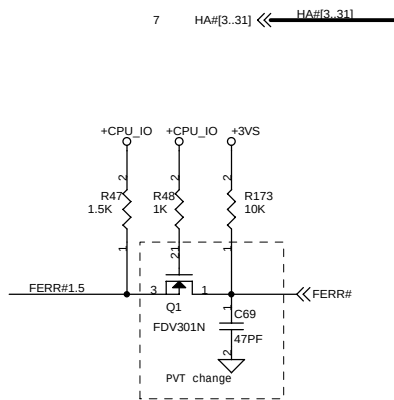
PCB No: LA971

888J2 BLOCK DIAGRAM



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7 HREQ#0 << T2
7 HREQ#1 << V4
7 HREQ#2 << V2
7 HREQ#3 << W3
7 HREQ#4 << W5
7 RP# << W2

7 ADS# << AB2

6 IERR# << AD9
7 BREQ#0 << C6
7 BPR# << U4
7 BNR# << T4
7 HLOCK# << R1

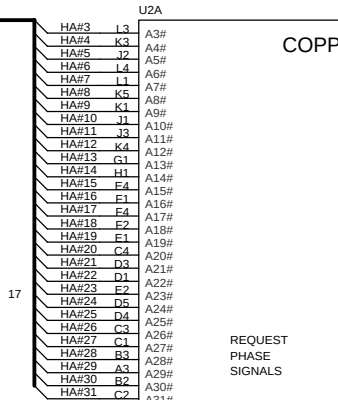
7 HIT# << V1
7 HITM# << U3
7 DEFER# << Y4

7 HTRDY# << U2
7 RS#0 << U1
7 RS#1 << AA2
7 RS#2 << W1

6 GT_A20M# << FERR#1.5
6 GT_IGNNE# << AC12
6 PWRGD_CPU << AC13
6 GT_SM# << AB10

6 PREQ# << R26
+CPU_IO << R146
R41 << 1 @56 0603 W20
R43 << 1 @10K AB12
R43 << 1 @10K AB15

6 GT_INTR << AB18
6 GT_NMI << AC19
6 GT_STPCLK# << AC11
6 SLP# << AB12



REQUEST
PHASE
SIGNALS

DATA
PHASE
SIGNALS

ERROR
SIGNALS

ARBITRATION
PHASE
SIGNALS

SNOOP PHASE
SIGNALS

RESPONSE
PHASE
SIGNALS

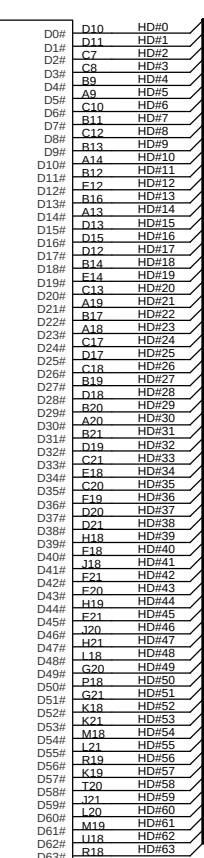
PC COMPATIBILITY
SIGNALS

DIAGNOSTIC
& TEST
SIGNALS

EXECUTION CONTROL
SIGNALS

THERMAL DIODE

BGA2_495



DEP0# << V20
DEP1# << T21
DEP2# << U21
DEP3# << B21
DEP4# << V18
DEP5# << P21
DEP6# << P20
DEP7# << U19

DBSY# << AA3
DRDY# << T1

PICCLK << Y20
PICD0 << AB21

INIT# << AC9
FLUSH# << A6

BCLK << M3

EDGCTRLN << AA16

110_1%_0603

110_1%_0603

110_1%_0603

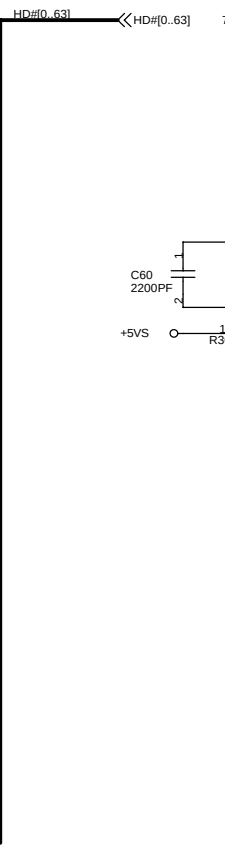
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110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603



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DEP1# << T21
DEP2# << U21
DEP3# << B21
DEP4# << V18
DEP5# << P21
DEP6# << P20
DEP7# << U19

DBSY# << AA3
DRDY# << T1

PICCLK << Y20
PICD0 << AB21

INIT# << AC9
FLUSH# << A6

BCLK << M3

EDGCTRLN << AA16

110_1%_0603

110_1%_0603

110_1%_0603

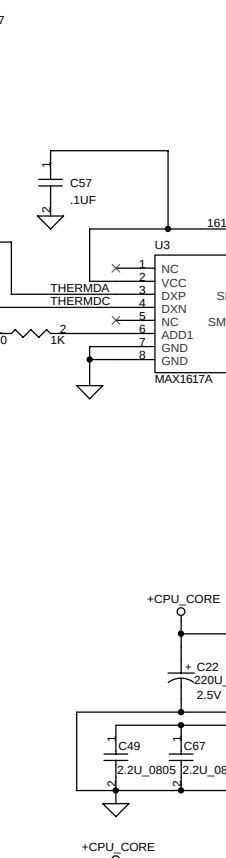
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110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603



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DEP1# << T21
DEP2# << U21
DEP3# << B21
DEP4# << V18
DEP5# << P21
DEP6# << P20
DEP7# << U19

DBSY# << AA3
DRDY# << T1

PICCLK << Y20
PICD0 << AB21

INIT# << AC9
FLUSH# << A6

BCLK << M3

EDGCTRLN << AA16

110_1%_0603

110_1%_0603

110_1%_0603

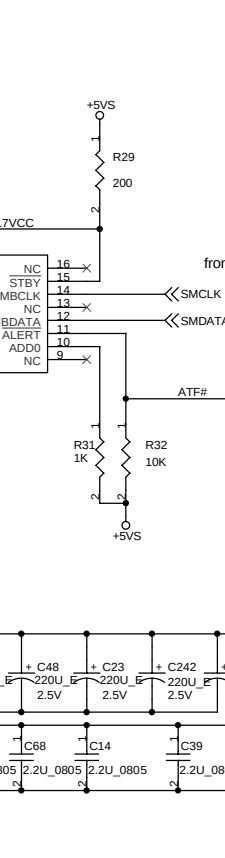
110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603



DEP0# << V20
DEP1# << T21
DEP2# << U21
DEP3# << B21
DEP4# << V18
DEP5# << P21
DEP6# << P20
DEP7# << U19

DBSY# << AA3
DRDY# << T1

PICCLK << Y20
PICD0 << AB21

INIT# << AC9
FLUSH# << A6

BCLK << M3

EDGCTRLN << AA16

110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603



DEP0# << V20
DEP1# << T21
DEP2# << U21
DEP3# << B21
DEP4# << V18
DEP5# << P21
DEP6# << P20
DEP7# << U19

DBSY# << AA3
DRDY# << T1

PICCLK << Y20
PICD0 << AB21

INIT# << AC9
FLUSH# << A6

BCLK << M3

EDGCTRLN << AA16

110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603

110_1%_0603

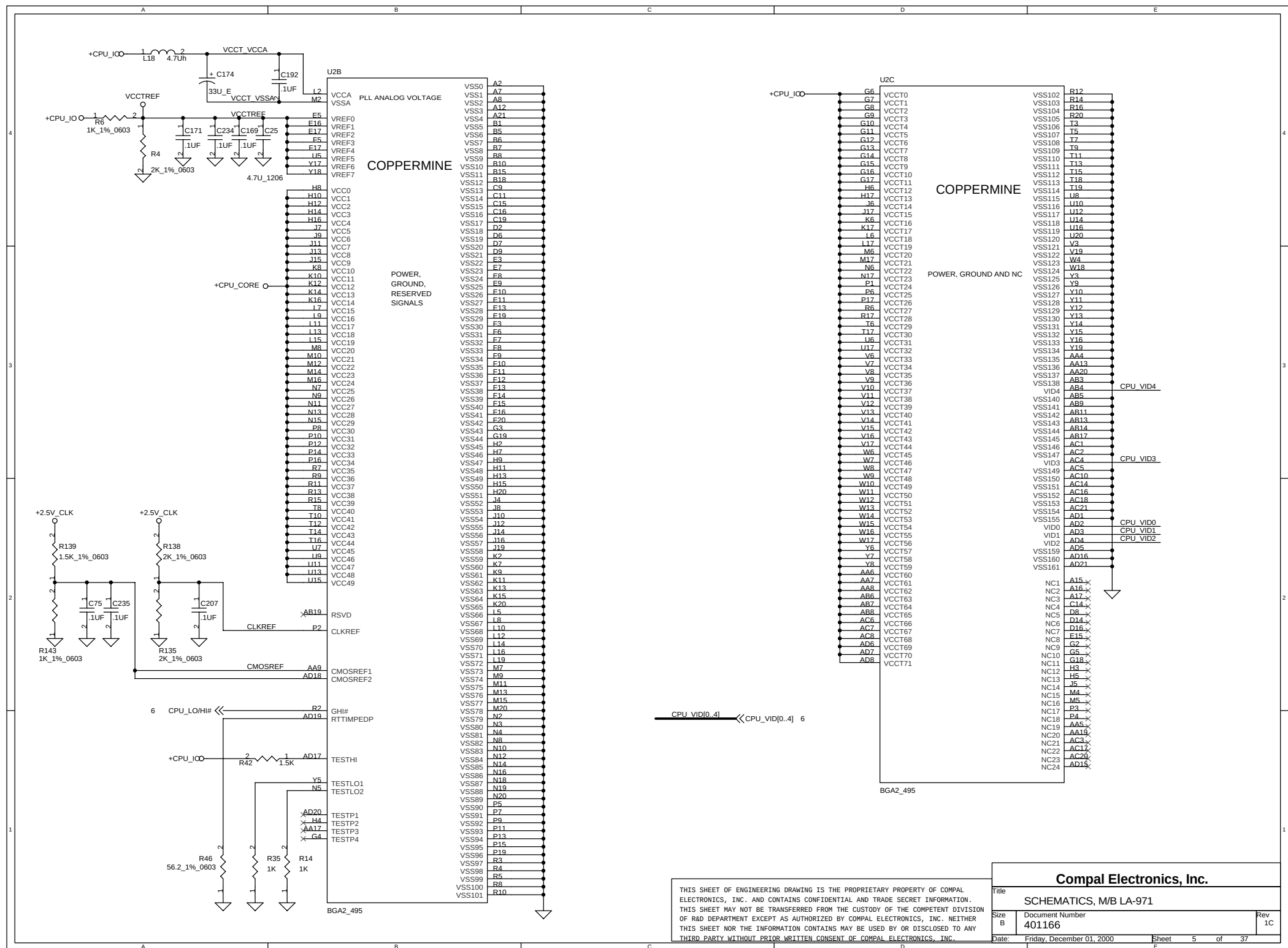
110_1%_0603

110_1%_0603

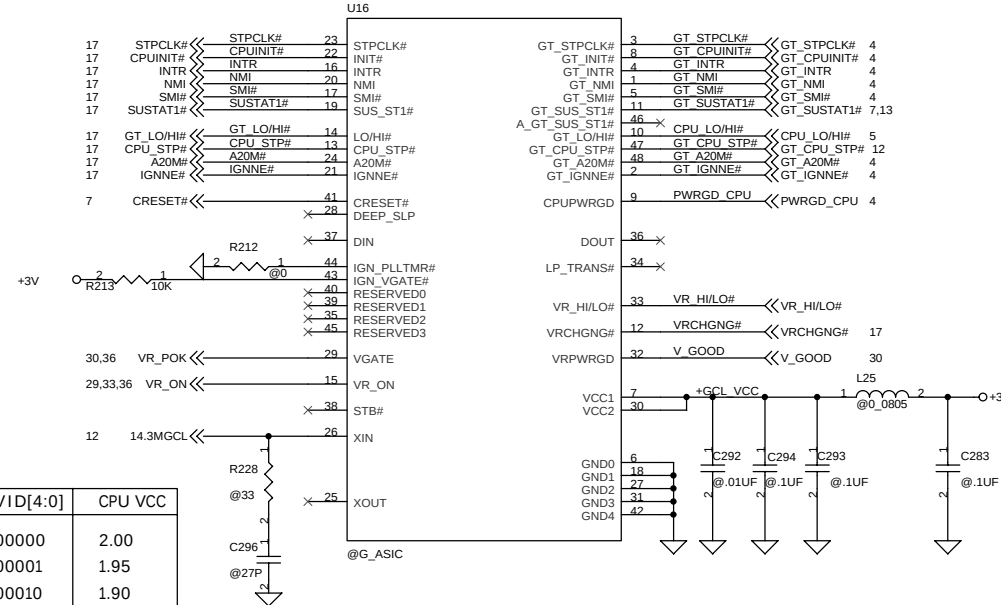
SELPSB[1:0]	STSEM BUS FREQUENCY
00	66MHZ
01	100MHZ
10	RESERVED
11	133MHZ

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With SpeedStep CPU Support:

Mount: U16: G_ASIC (SA658370000)

U15: 74CBT3383 (SA433830000)

R57, R184, R185, R216 R215: 0ohm
(1.6V for high performance)

RP56: 8P4R-4.7K

R214: 1Kohm

R242: 680ohm

R240: 4.7Kohm

R209: 100Kohm

R236: 100Kohm

R208: 1Kohm

R136: 1.5Kohm

R236: 100Kohm

R239: 1.5Kohm

R207: 100Kohm

R140: 1.5Kohm

Remove:

RP4: 8P4R-0

R54: 0ohm

RP50: 8P4R-0

RP49: 8P4R-0

R234: 0ohm

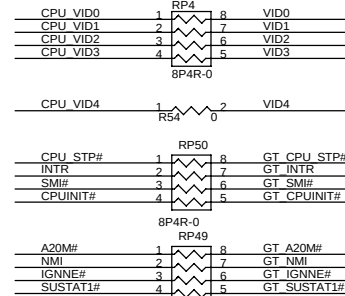
R223: 0ohm

R232: 31.6Kohm 1%

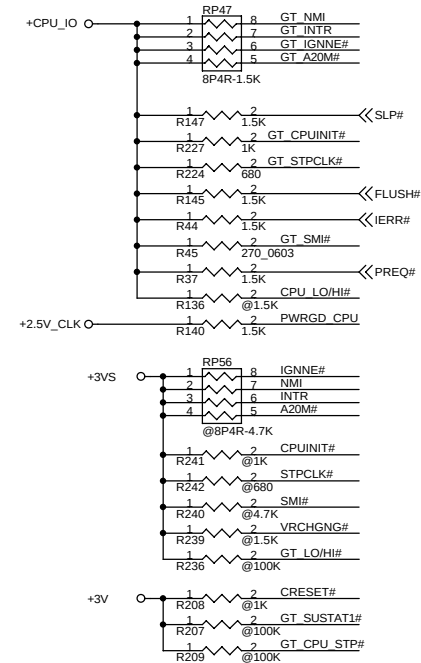
R214: 10Kohm

R231: 100Kohm 1%

without Geyserville,
GHI#(CPU_LO/HI#) can
OPEN

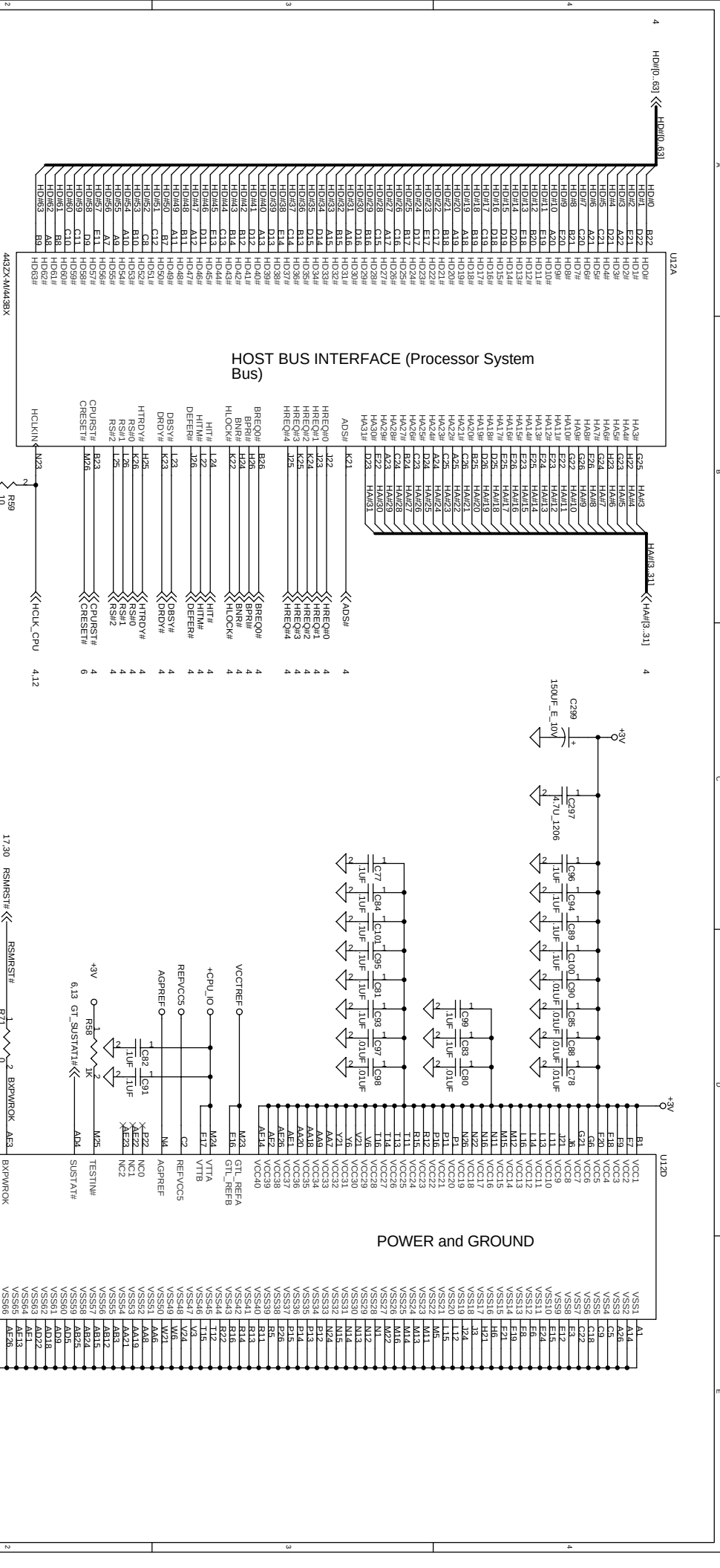


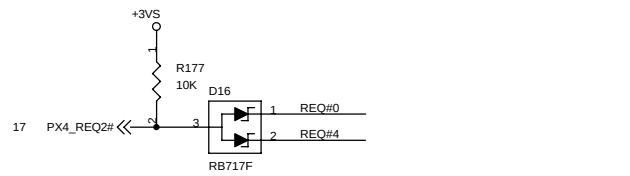
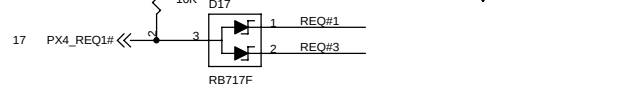
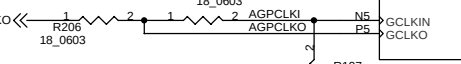
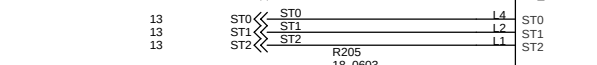
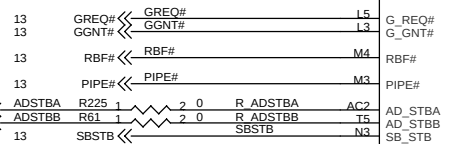
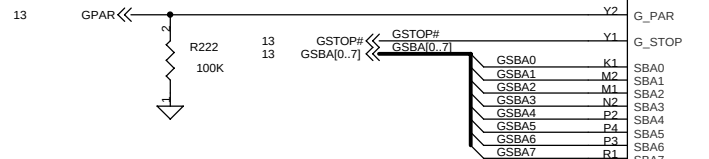
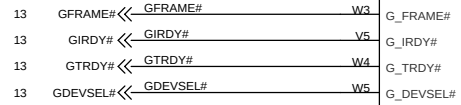
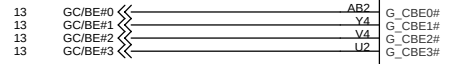
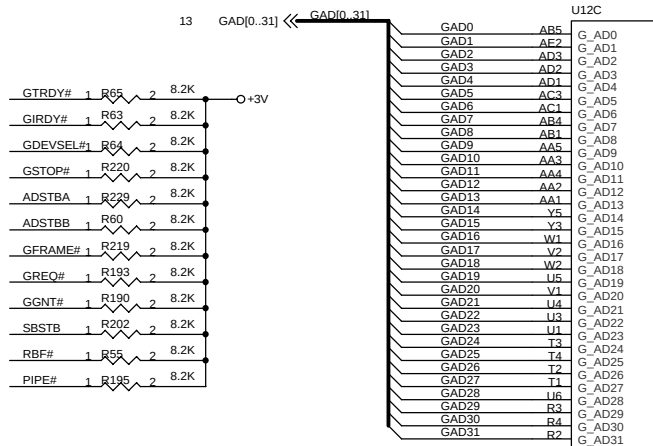
for without Geyserville



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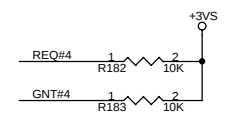
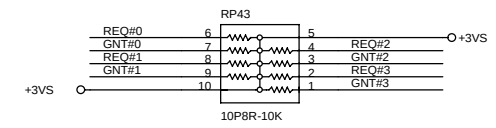
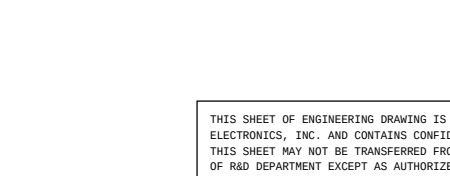
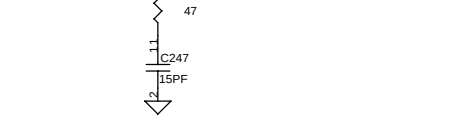
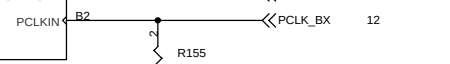
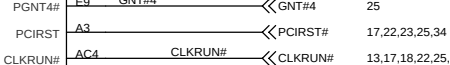
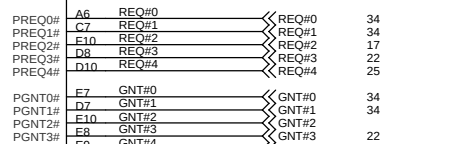
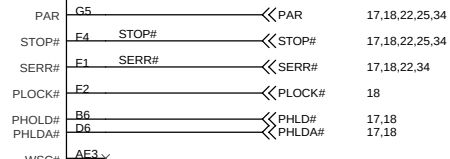
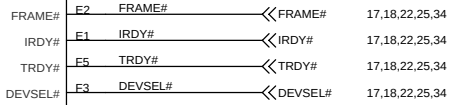
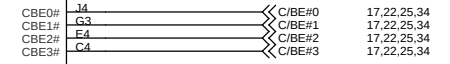
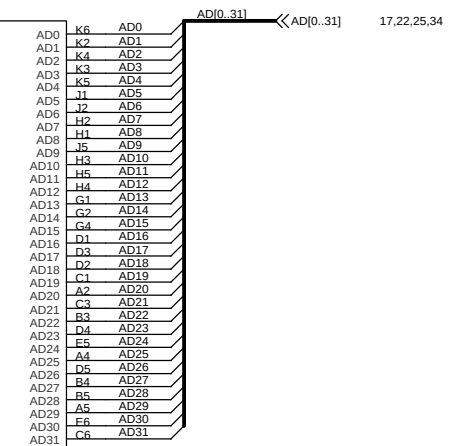
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AGP INTERFACE

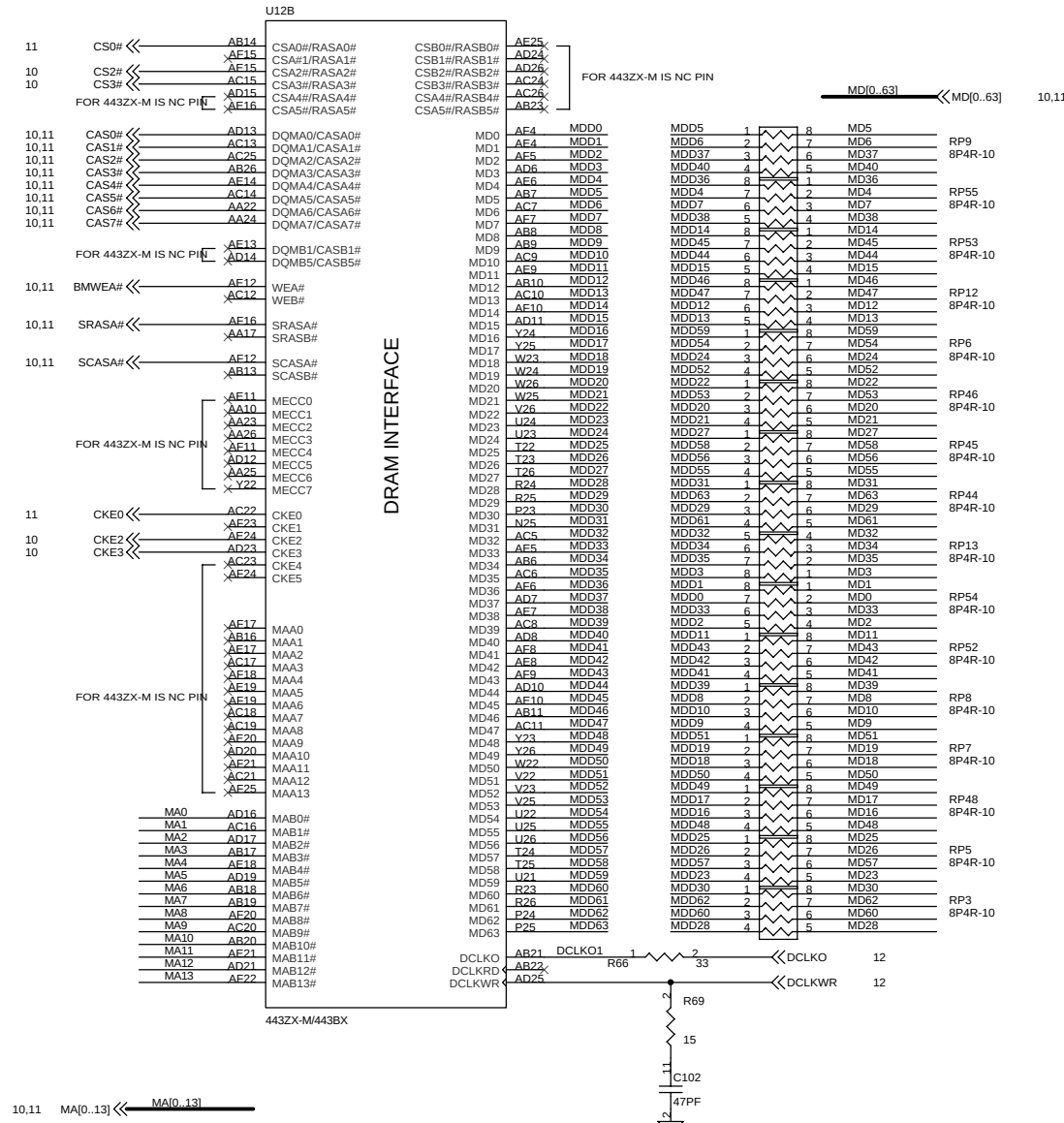
PCI INTERFACE



PCI REQ ASSIGNMENT	
REQ#0	MiniPCI(Compal)
REQ#1	MINI PCI
REQ#2	NO USED
REQ#3	PCMCIA CONTROLLER
REQ#4	PCI AUDIO

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Pin Name	Function	Low	High	Internal Resistor	Status Register
MAB12#	Host Frequency Select	66MHz	100MHz	Pull-down	NBXCFCG[13]
MAB10#	Quick Start Select	Stop Clock Mode	Quick Start Mode	Pull-down	PMCR[3]
MAB6#	Host Bus Buffer Mode Select	Desktop GTL+	Mobile Low Power GTL+	Pull-down	none

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Support 3 SDRAM CLOCK
PIN 60, 77, 78 Difference

PIN 60, 77, 78 Difference

BANK 2, 3

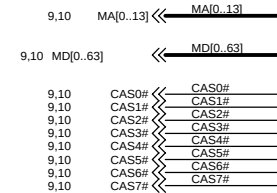
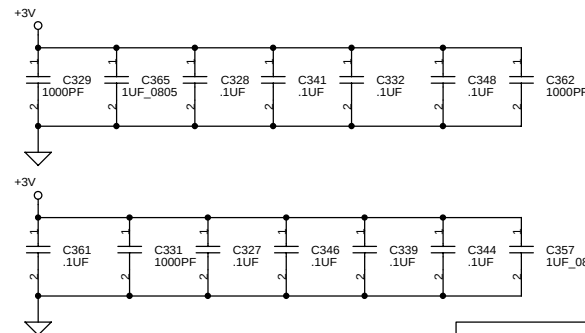
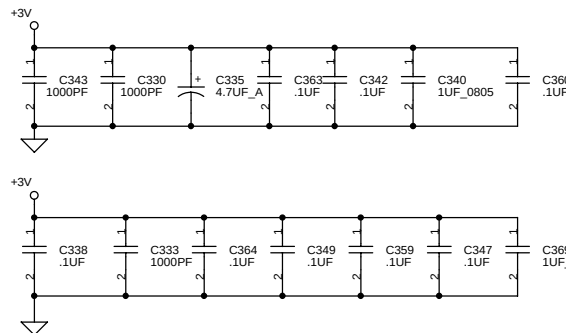
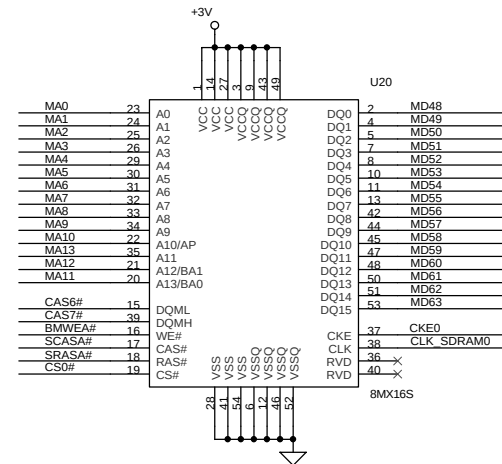
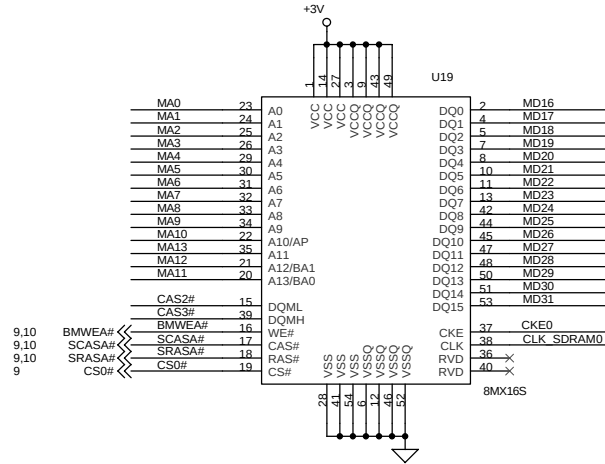
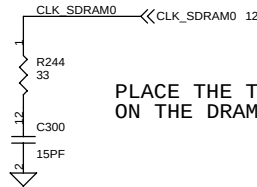
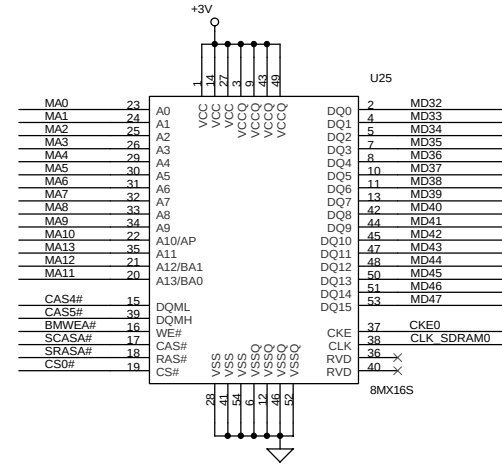
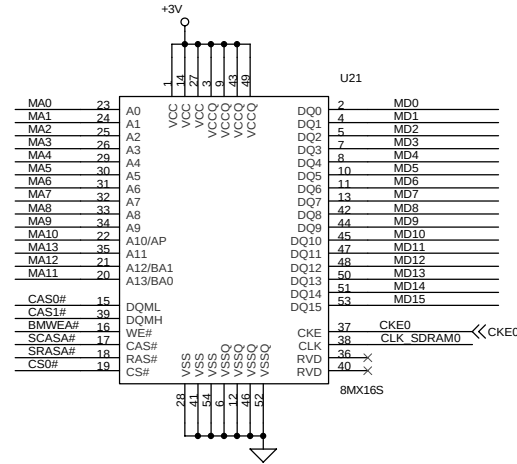


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32MB/64MB SDRAM

BANK0

64Mbit 4Mx16 : Row: MA0-MA11
Column: MA0-MA7
Bank address: 2
128Mbit 8Mx16 : Row: MA0-MA11
Column: MA0-MA8
Bank address: 2



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Size

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Rev

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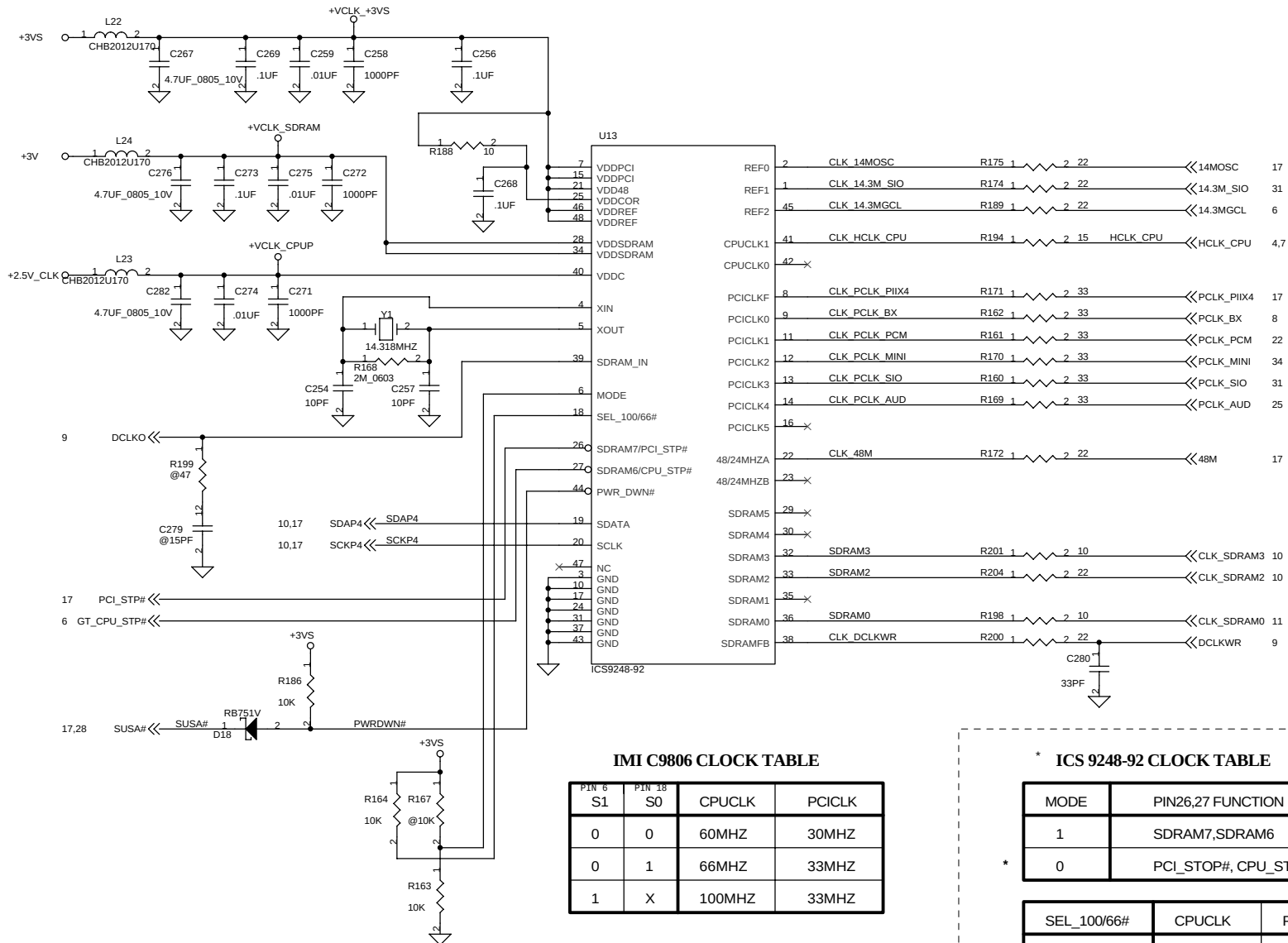
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CLOCK GENERATOR & BUFFER



IMI C9806 CLOCK TABLE

PIN 6	PIN 18	CPUCLK	PCICLK
S1	S0		
0	0	60MHZ	30MHZ
0	1	66MHZ	33MHZ
1	X	100MHZ	33MHZ

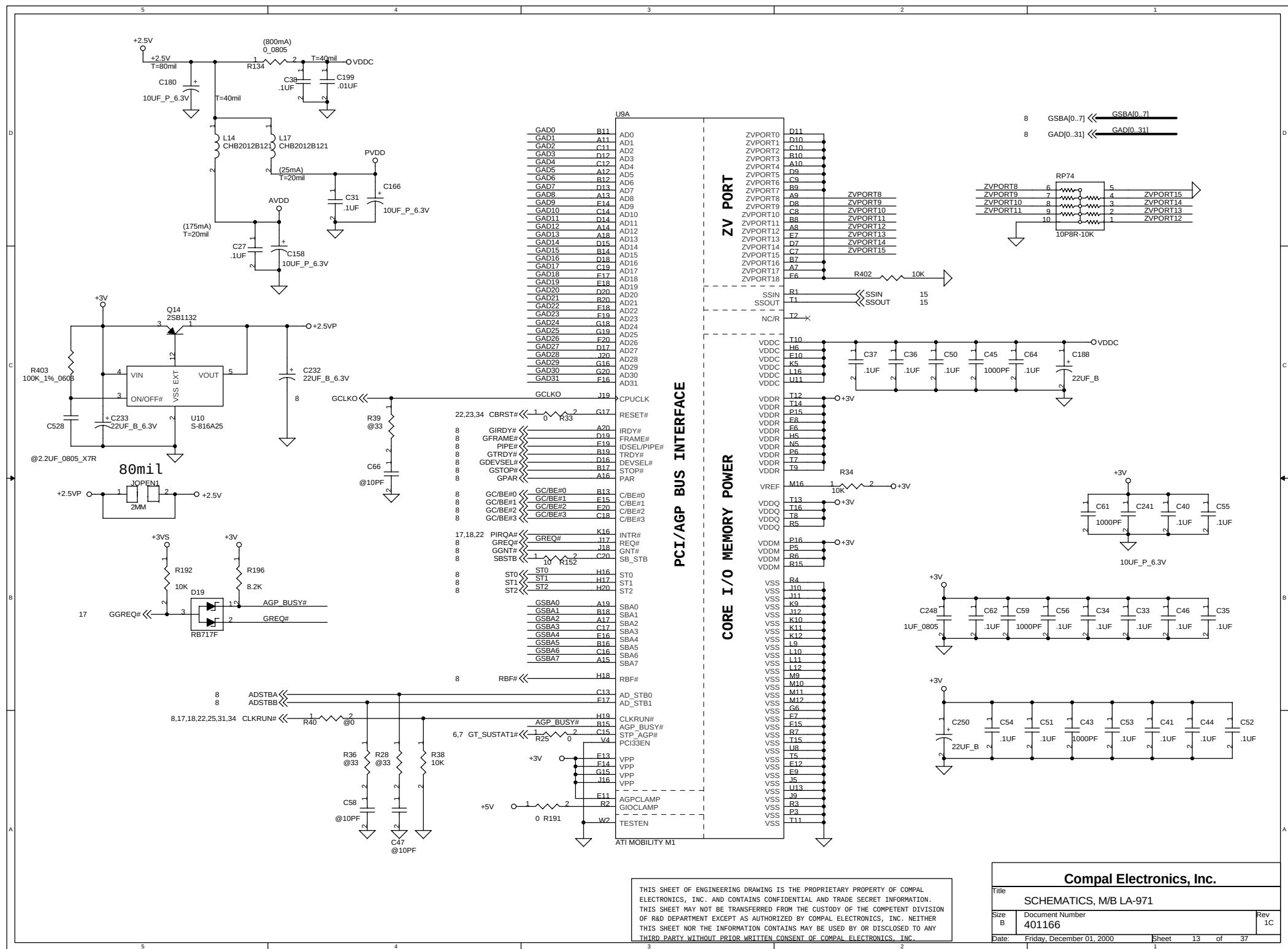
* ICS 9248-92 CLOCK TABLE

MODE	PIN26,27 FUNCTION
1	SDRAM7,SDRAM6
0	PCI_STOP#, CPU_STOP#

SEL_100/66#	CPUCLK	PCICLK
0	66.6MHZ	33.3MHZ
1	100MHZ	33.3MHZ

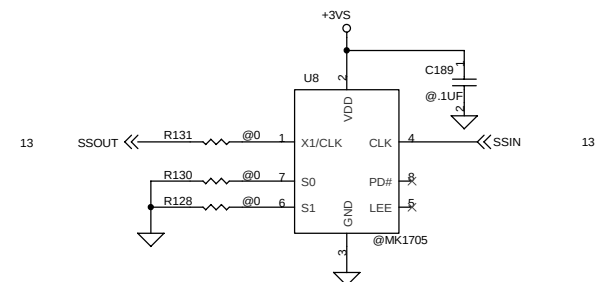
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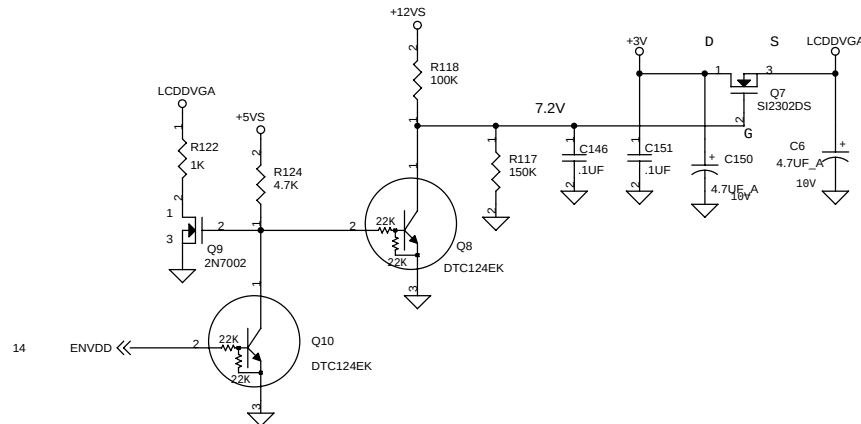


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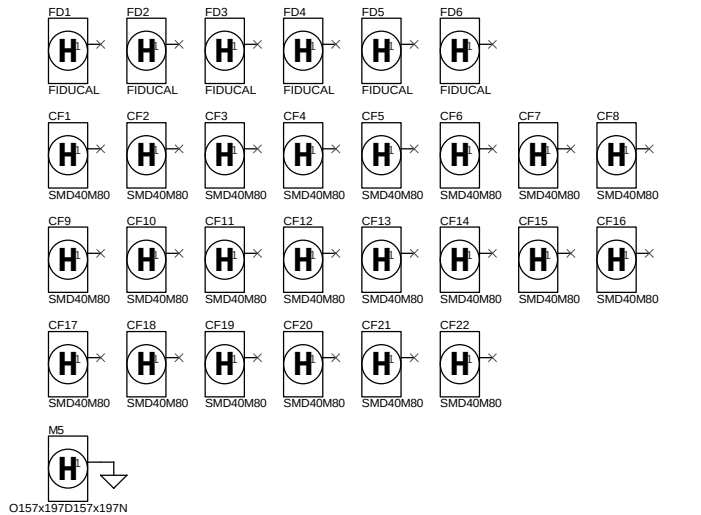
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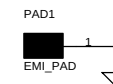
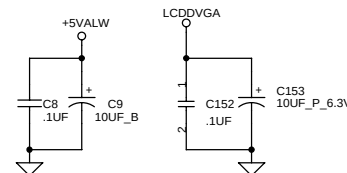
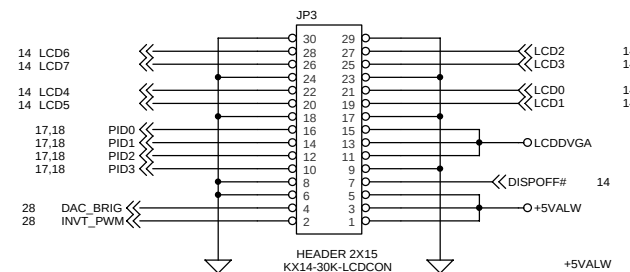
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VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +-8V

SI2302DS: N CHANNEL
VGS: 4.5V, RDS: 85 mOHM
VGS: 2.5V, RDS: 115mOHM
Id(MAX): 2.8A
VGS(MAX): +-8V

FOR LAYOUT ONLY



LCD & INVERTER Connector

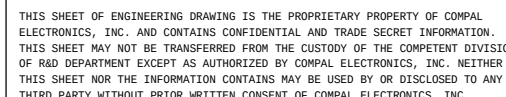


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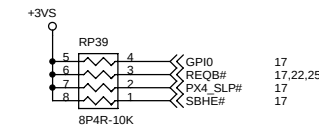
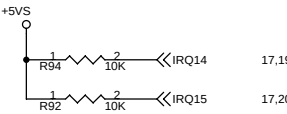
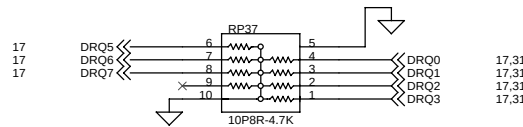
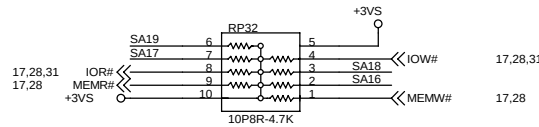
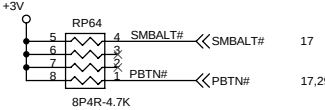
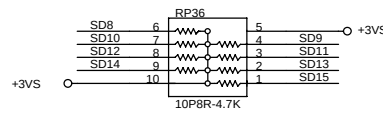
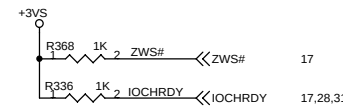
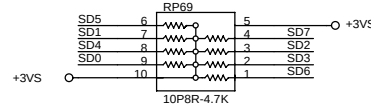
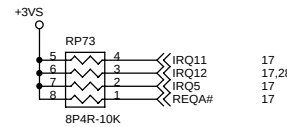
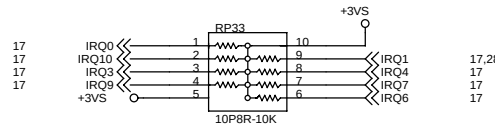
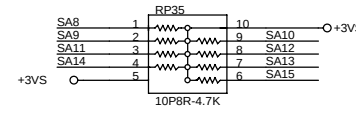
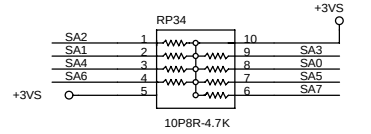
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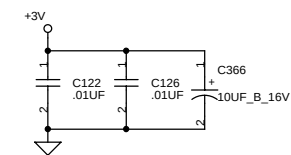
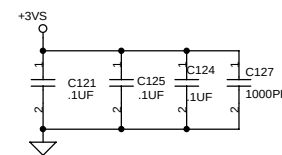
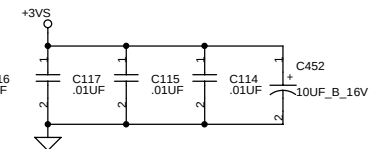
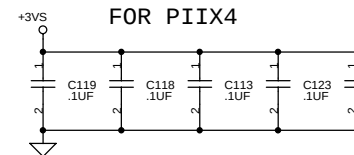
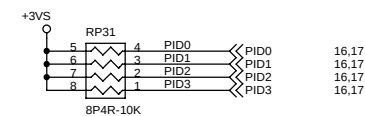
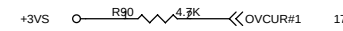
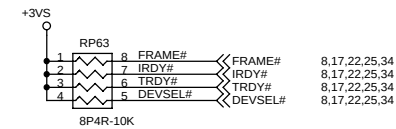
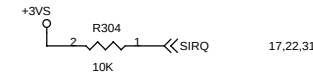
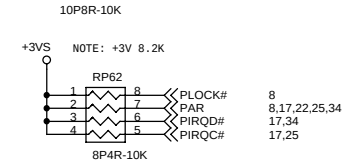
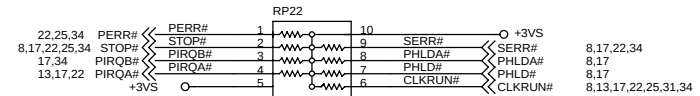


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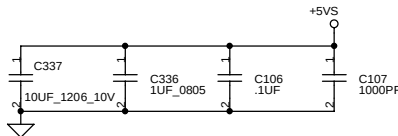
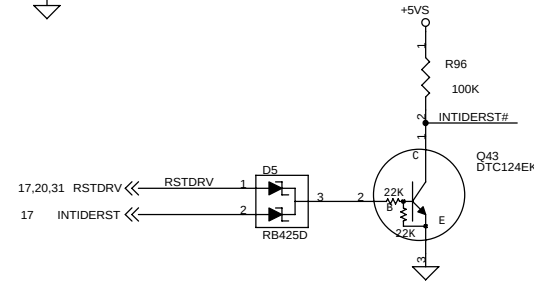
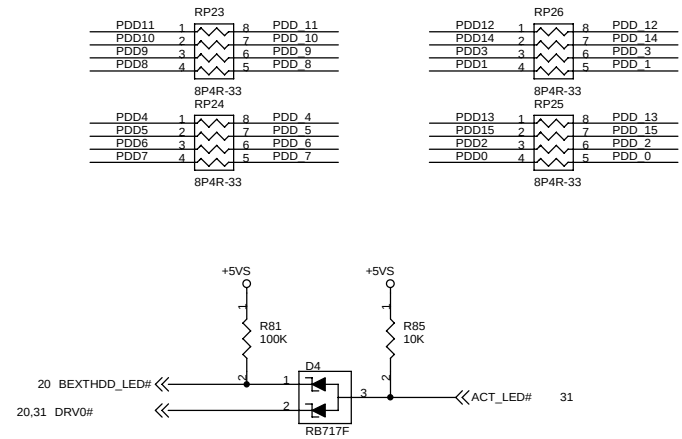
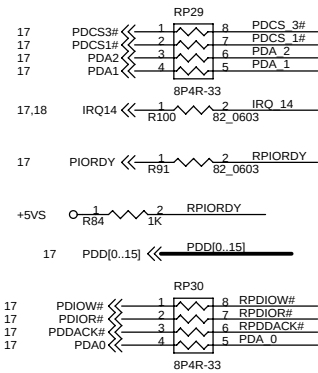
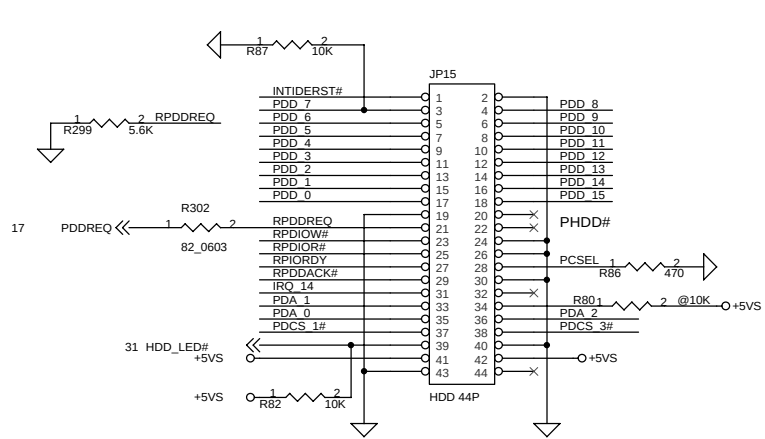
PCI



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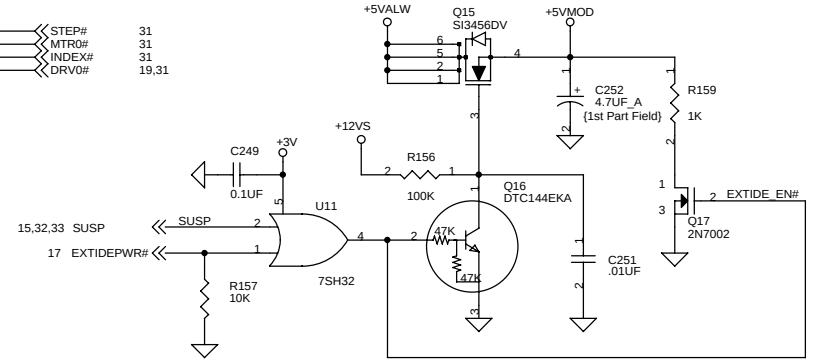
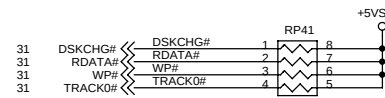
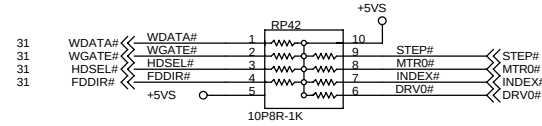
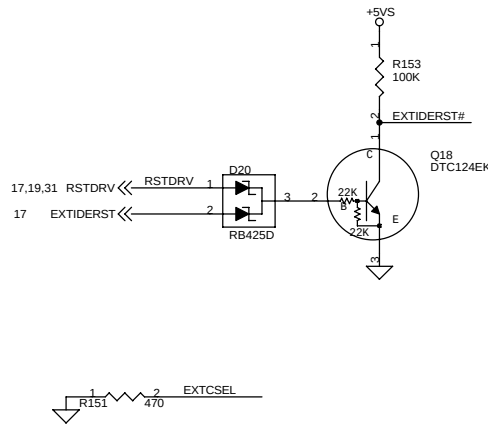
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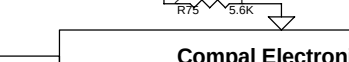
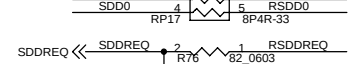
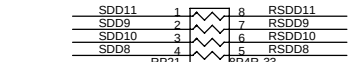
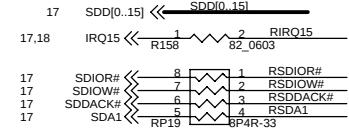
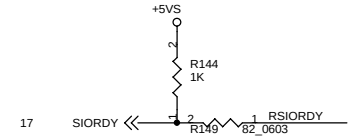
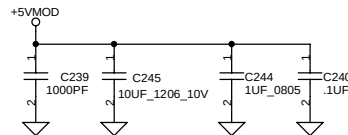
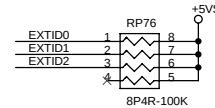
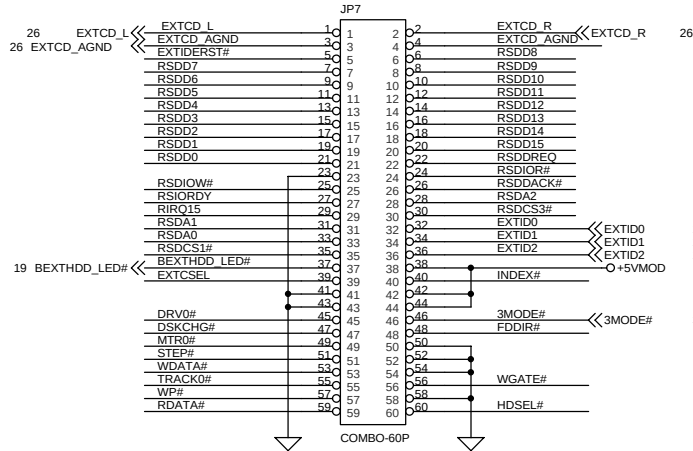


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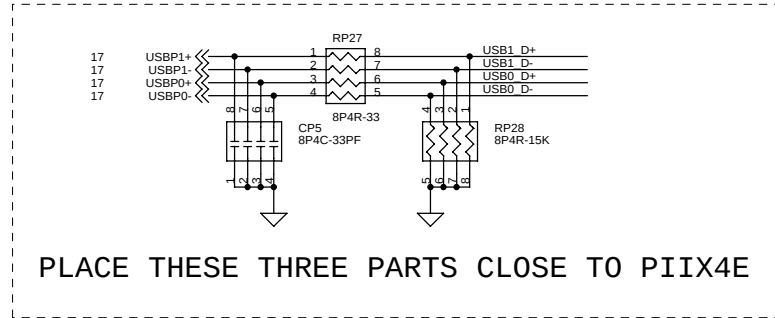


SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+20V

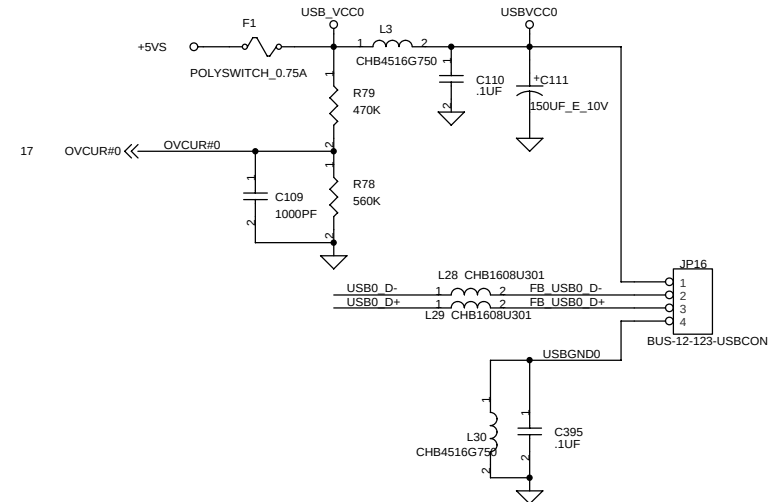


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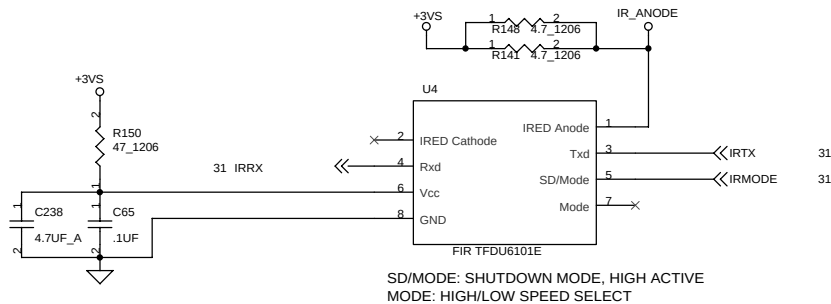
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USB CONNECTOR



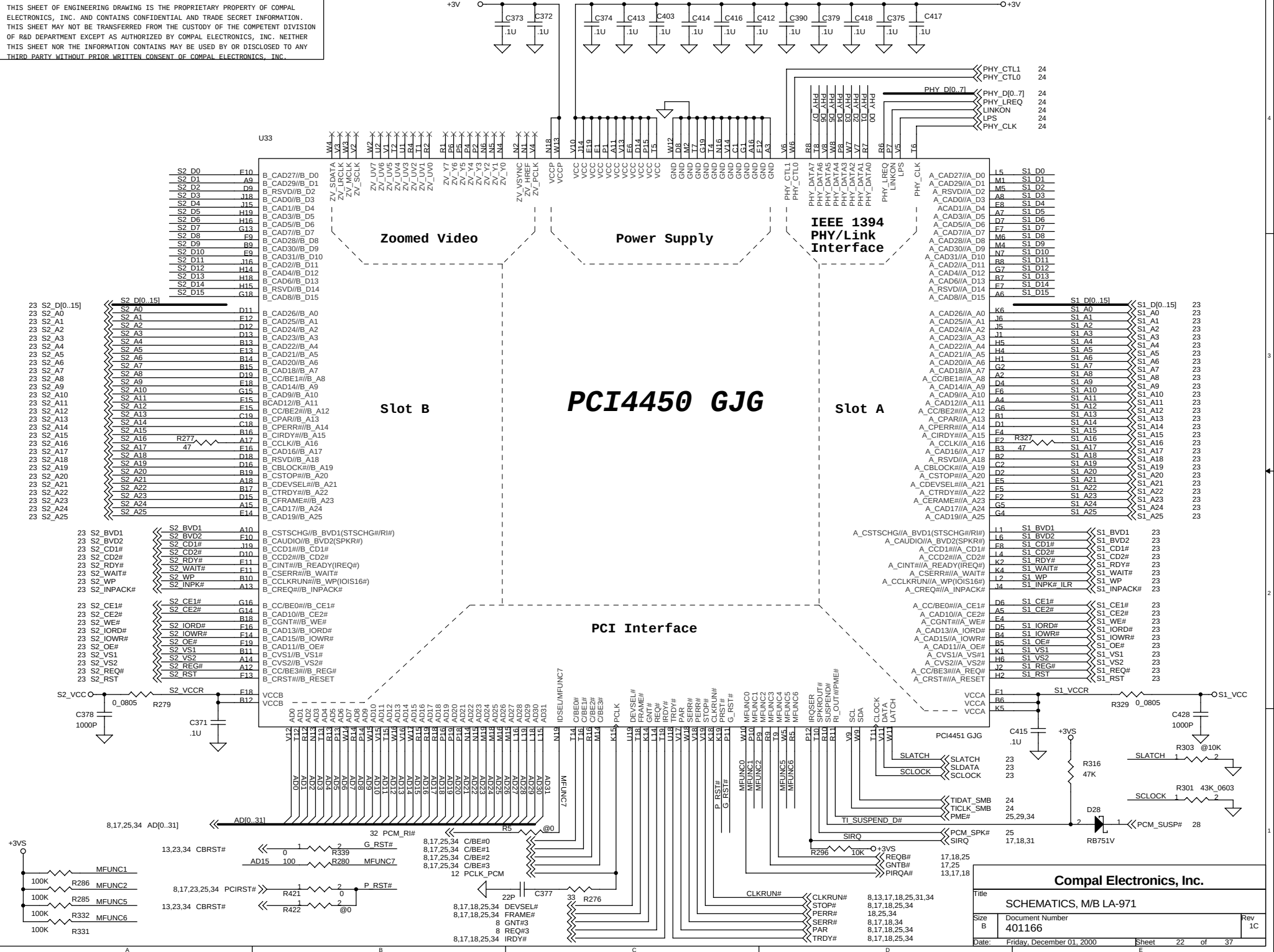
FIR Module



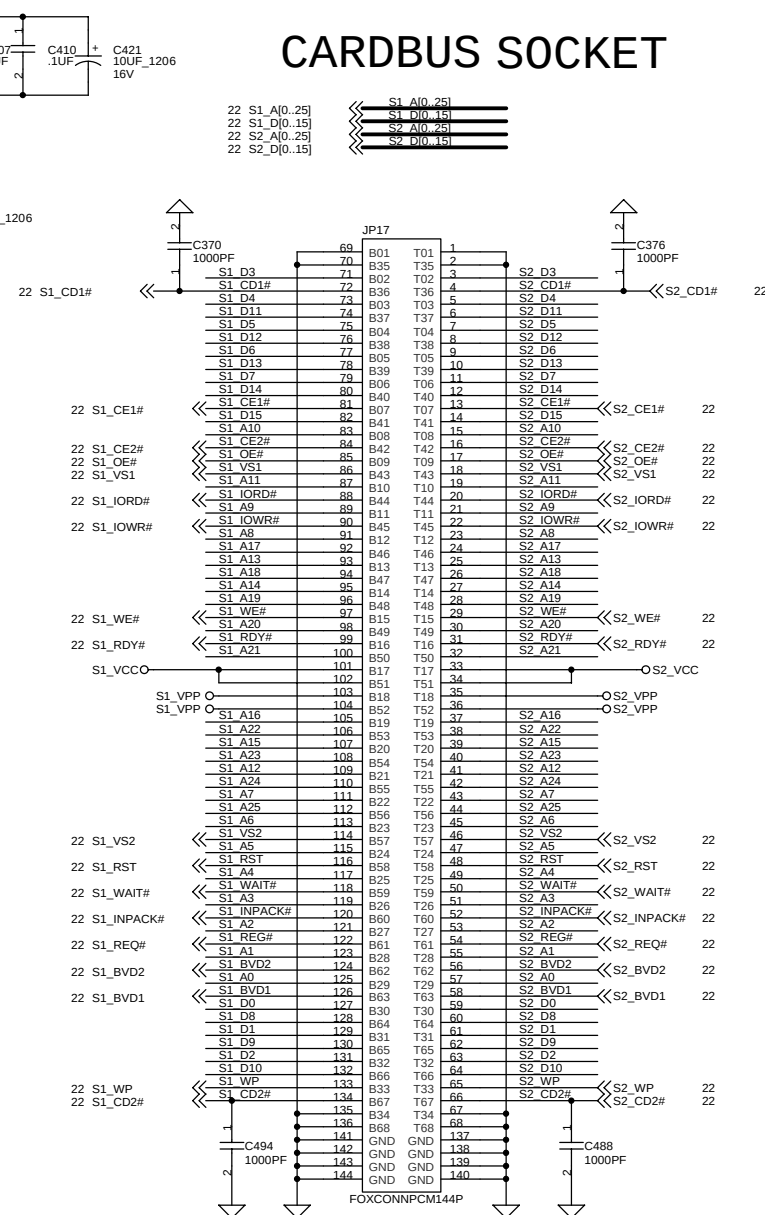
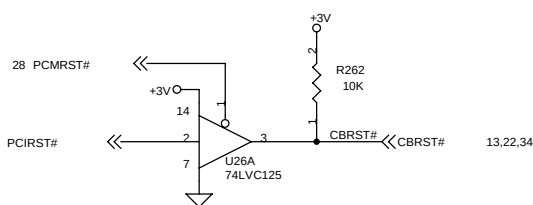
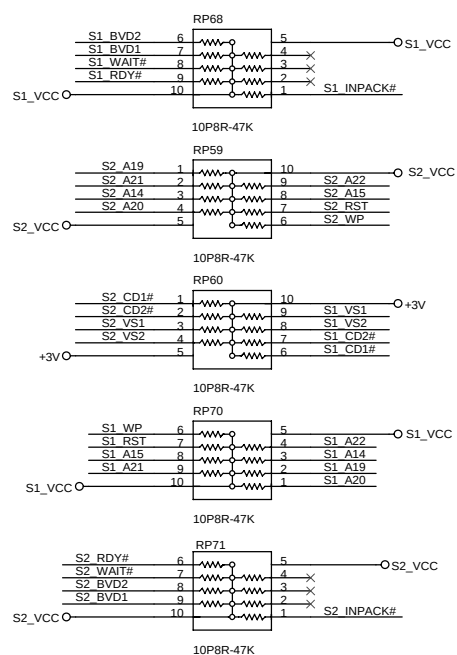
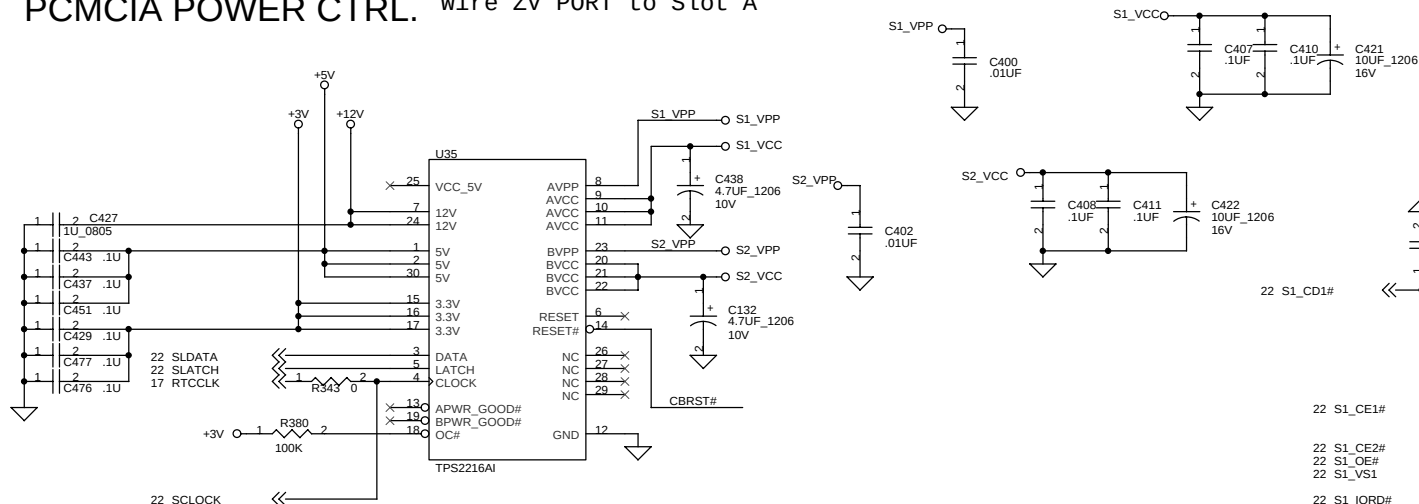
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PCMCIA POWER CTRL. Wire ZV PORT to Slot A

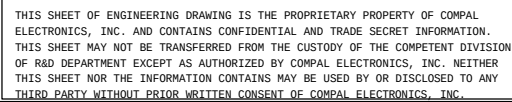


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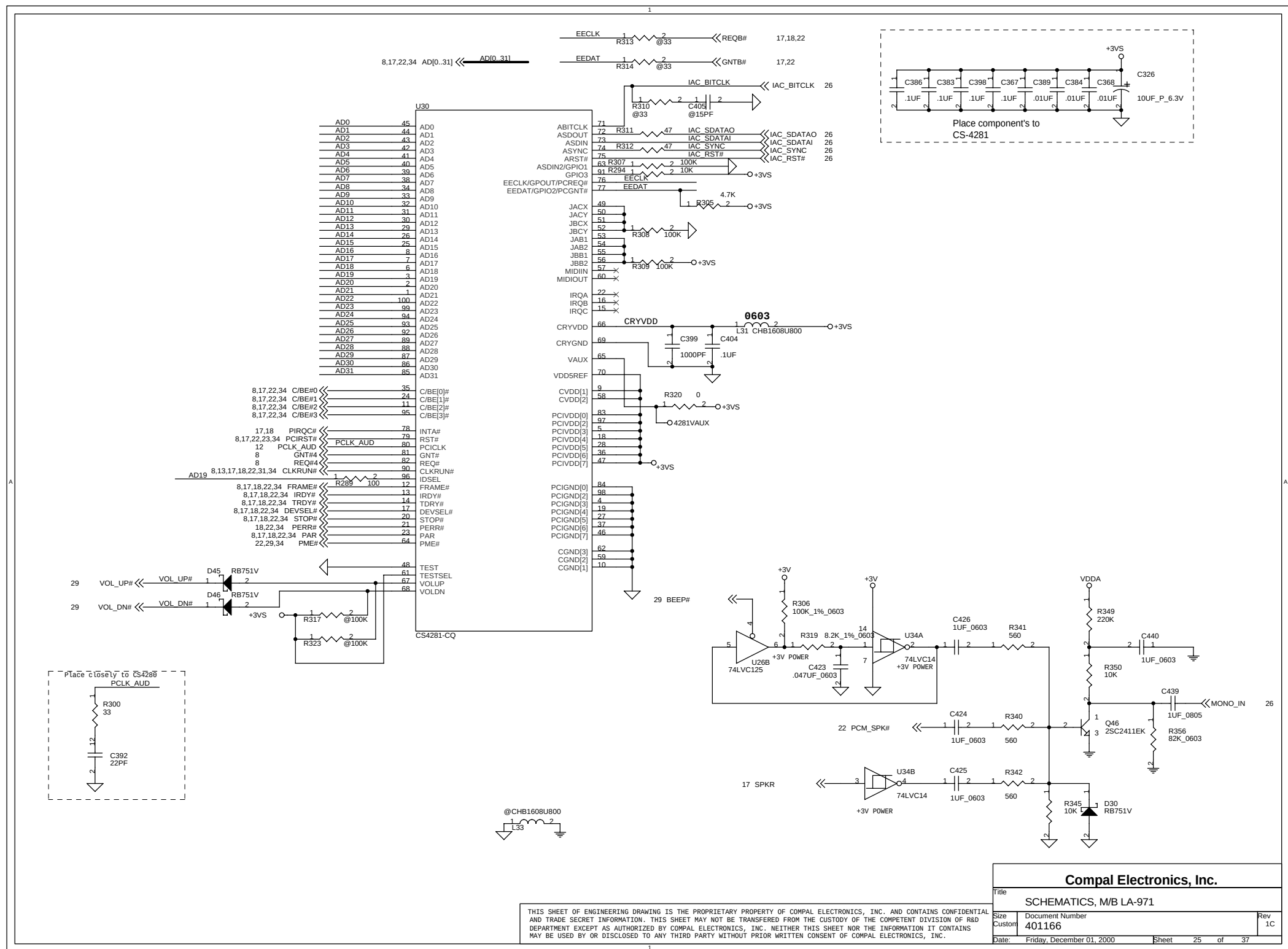
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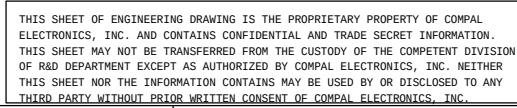
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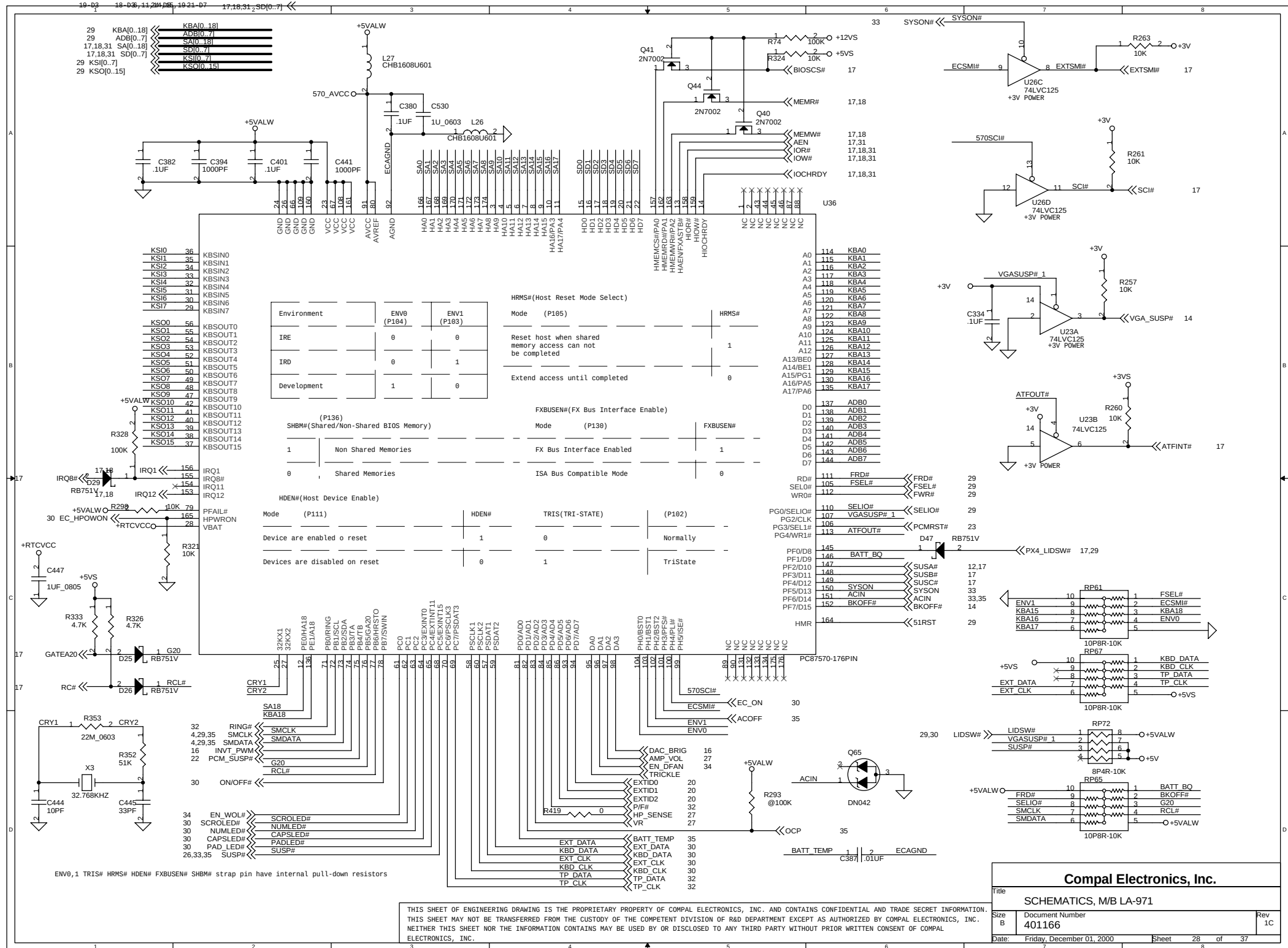


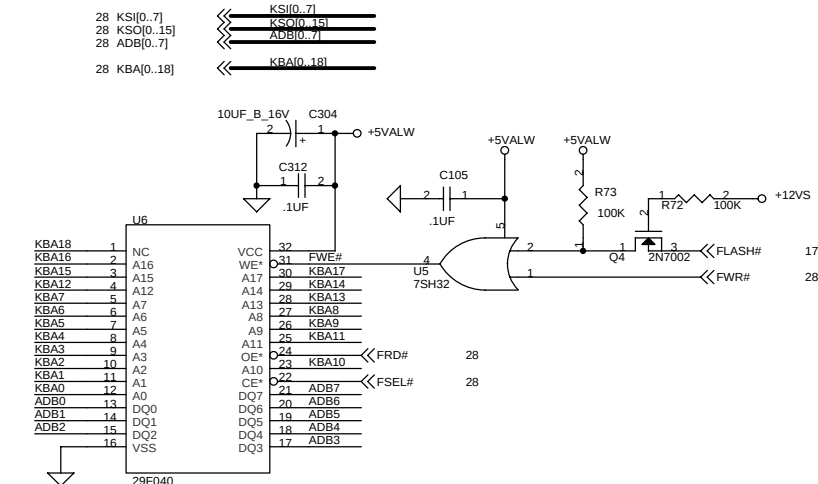
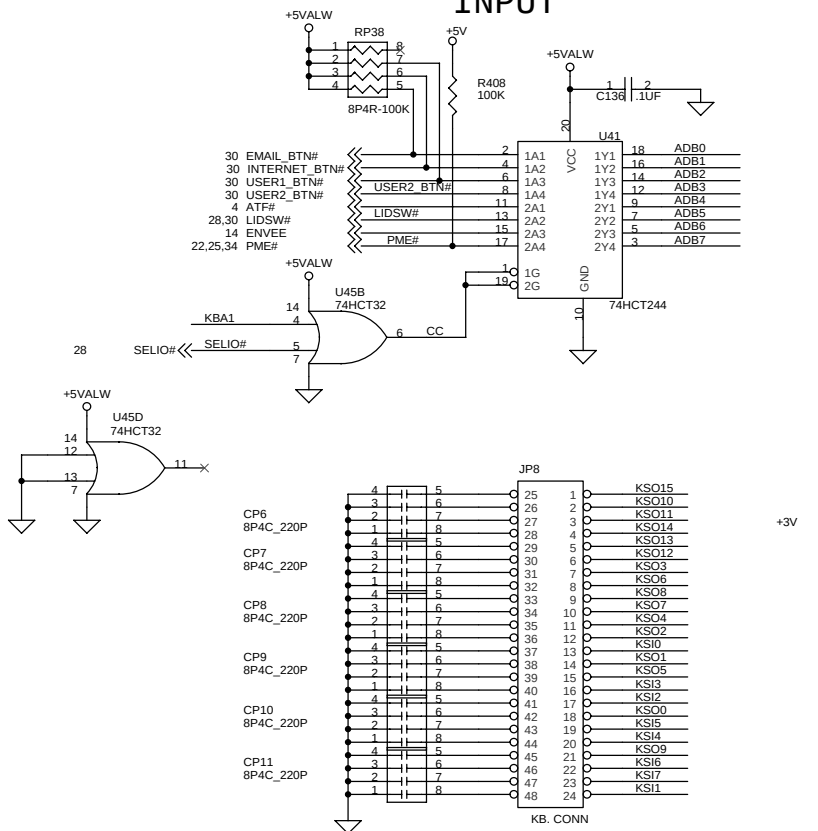
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The schematic diagram illustrates the NM24C164 address decoder circuit. It features two 74HCT273 flip-flops (U42 and U43) and two 74HCT232 decoders (U45A and U45C). The address lines (A0-A15) are generated from three input buttons (MMO_ON, PBTN#, LLBATT#) and two status LEDs (PWR_LED#, BATT_CHG_LED#). The address lines are connected to the D0-D7 inputs of the 24C164. The circuit also includes a +5VALW supply, a +3V power supply, and various passive components like resistors (R374, R106, R416) and capacitors (C502, C489, C442).

Component List:

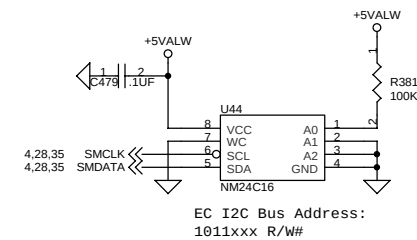
- U42: 74HCT273
- U43: 74HCT273
- U45A: 74HCT232
- U45C: 74HCT232
- U23C: 74LVC125
- R374: 1K
- R106: 10K
- R416: @0_0603
- C502: 1.1uF
- C489: 1.1uF
- C442: 1uF_0805

Pin Connections:

- U42 (74HCT273):**
 - D0: ADB0, D1: ADB1, D2: ADB2, D3: ADB3, D4: ADB4, D5: ADB5, D6: ADB6, D7: ADB7
 - Q0: PWR_LED#, Q1: BATT_CHG_LED#, Q2: PX4_RIB#, Q3: PX4_PBTN#, Q4: LLBATT#, Q5: BATT_LOW_LED#, Q6: BEEP#, Q7: (Unused)
 - CLK: LARST#, CLR: (Unused)
- U43 (74HCT273):**
 - D0: ADB0, D1: ADB1, D2: ADB2, D3: ADB3, D4: ADB4, D5: ADB5, D6: ADB6, D7: ADB7
 - Q0: (Unused), Q1: (Unused), Q2: (Unused), Q3: (Unused), Q4: (Unused), Q5: (Unused), Q6: (Unused), Q7: (Unused)
 - CLK: LARST#, CLR: (Unused)
- U45A (74HCT232):**
 - 14: KBA3, 1: SELIO#, 2: 7, 3: AA, 11: LARST#
- U45C (74HCT232):**
 - 14: KBA4, 1: SELIO#, 2: 7, 3: BB, 11: LARST#
- U23C (74LVC125):**
 - 14: +3V, 1: PX4_RIB#, 8: PX4_RI#

Address Definition:

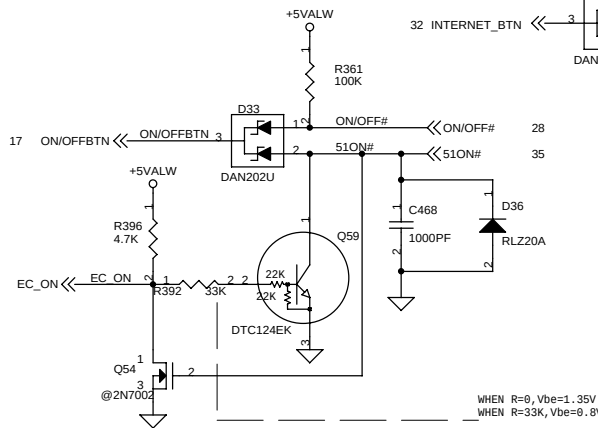
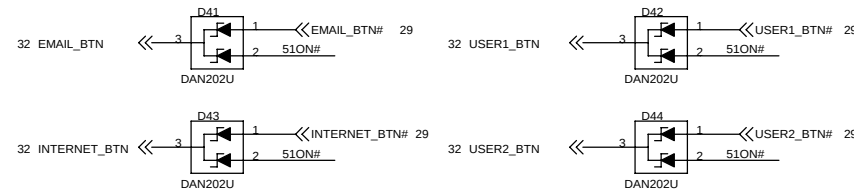
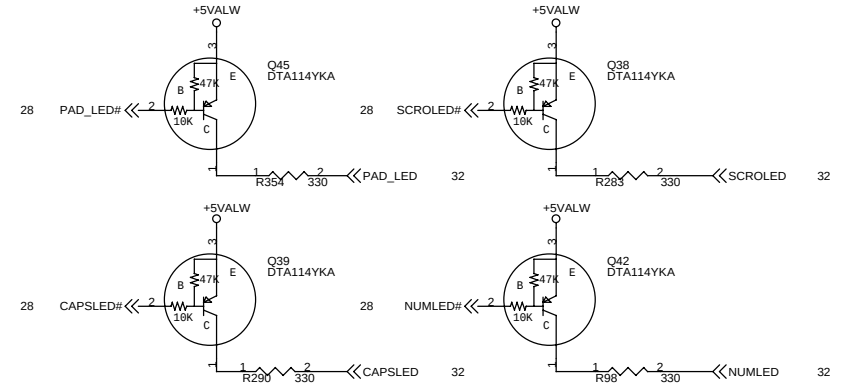
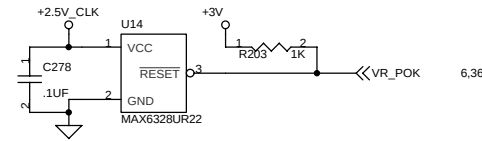
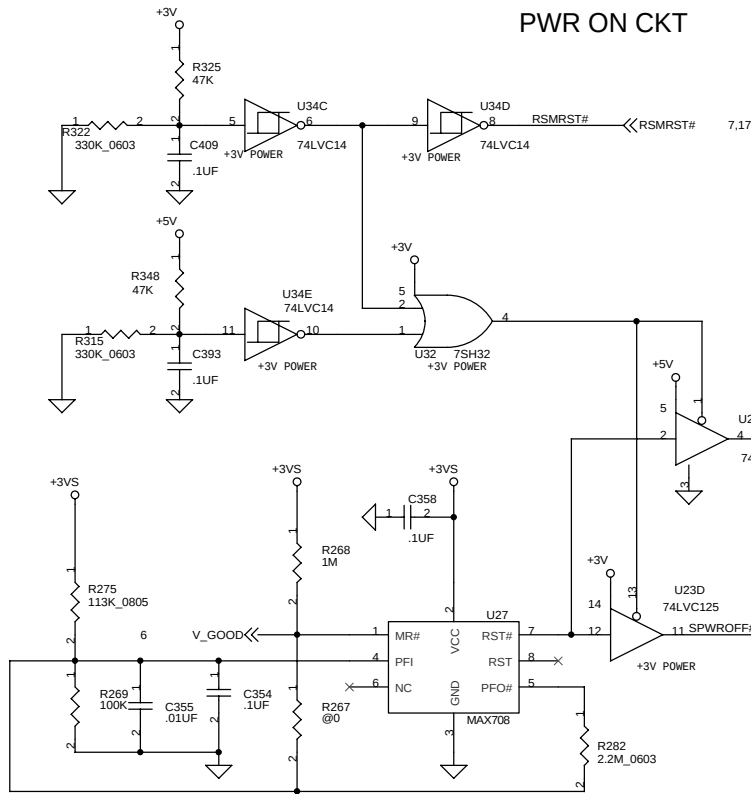
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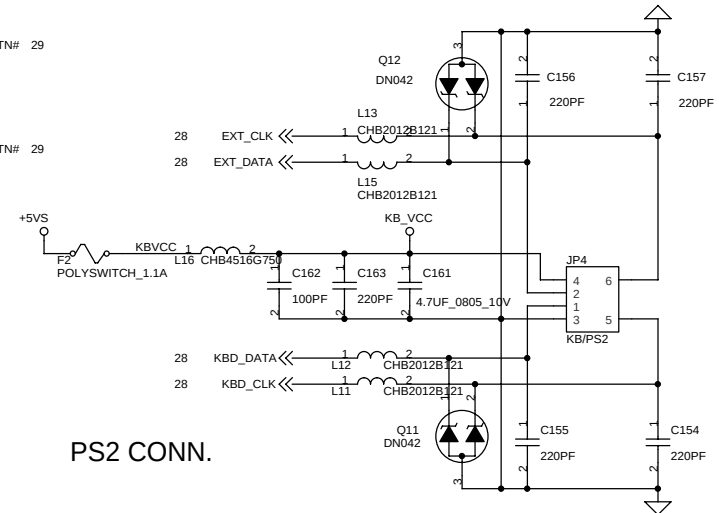
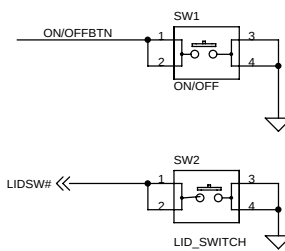
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Change R214: 4.7k -> 22k, R215: 33k -> 22k, remove Q15.

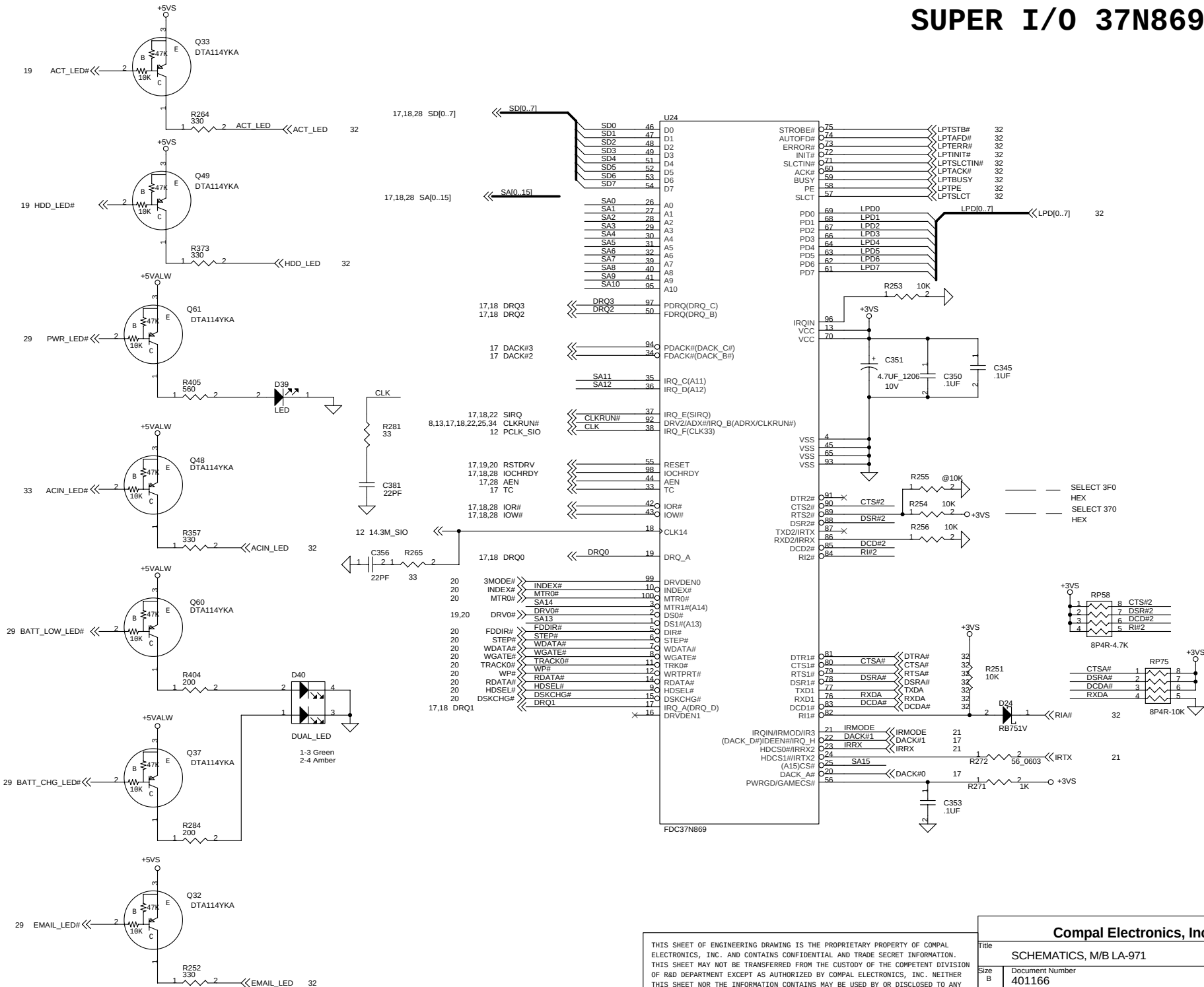
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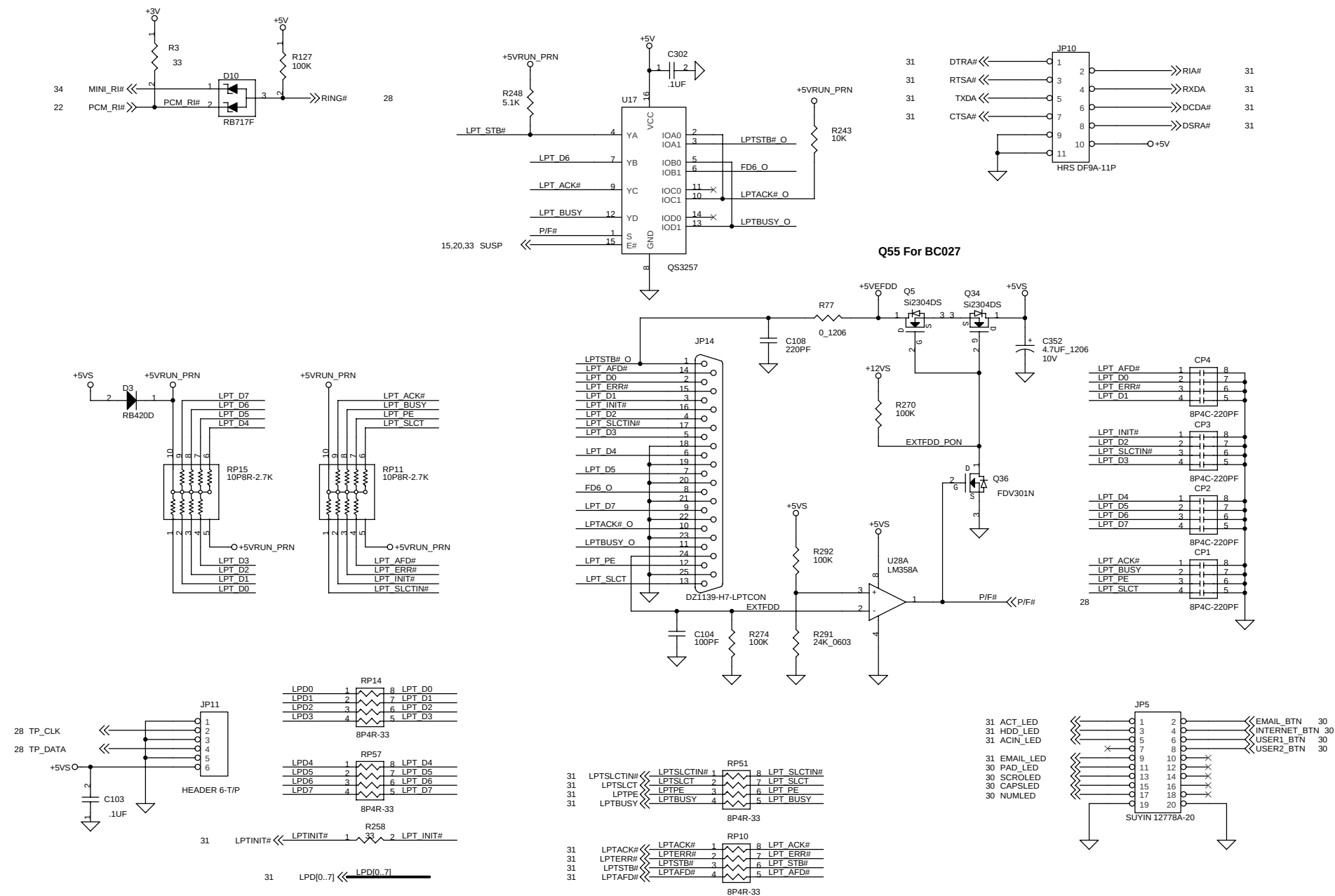
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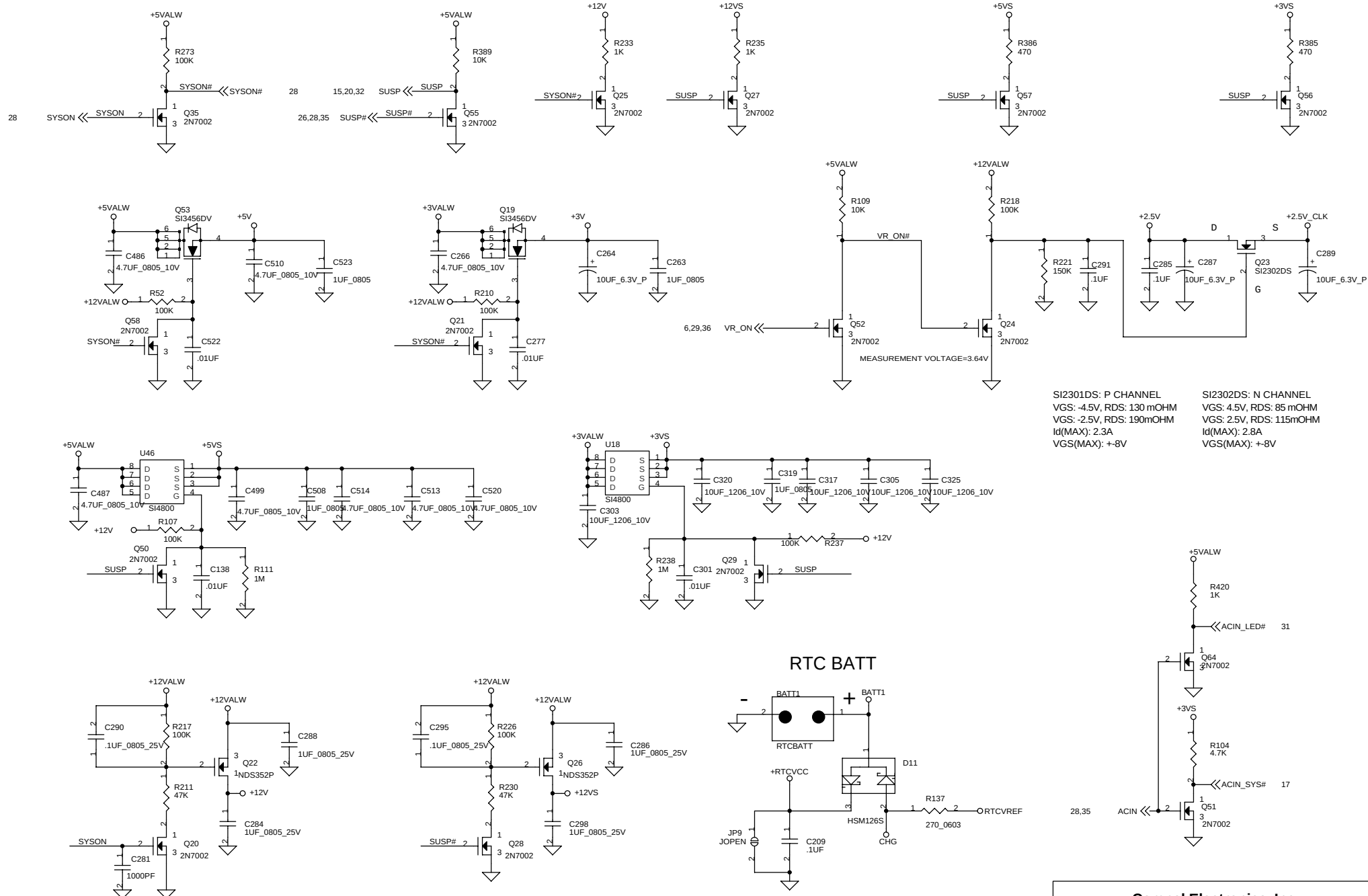


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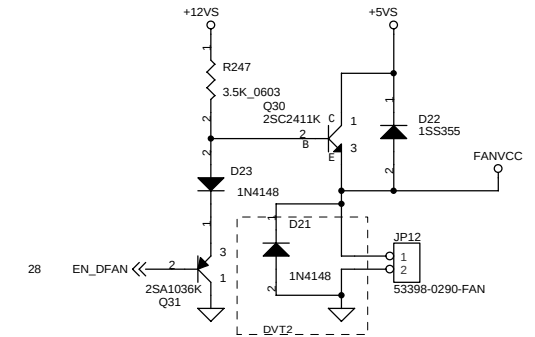
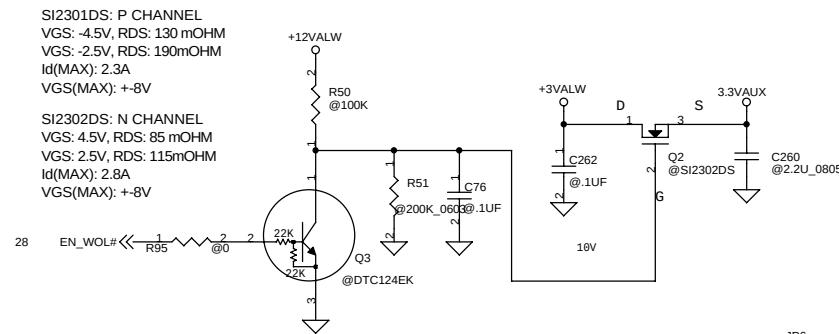
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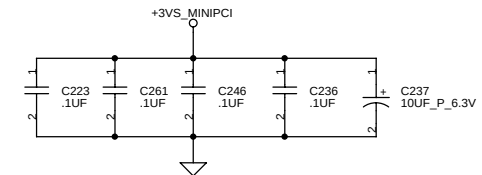
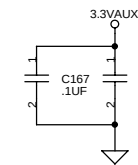
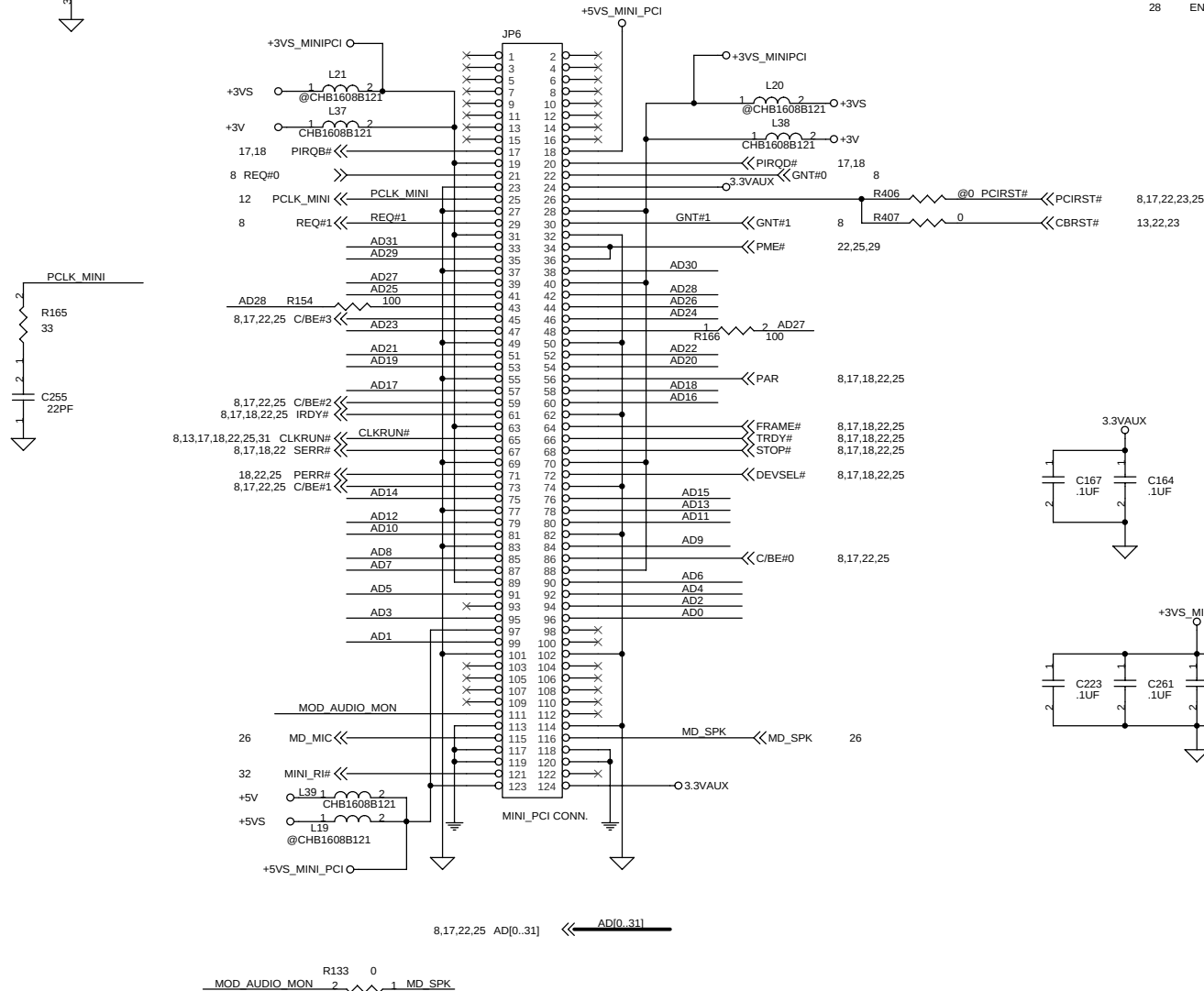


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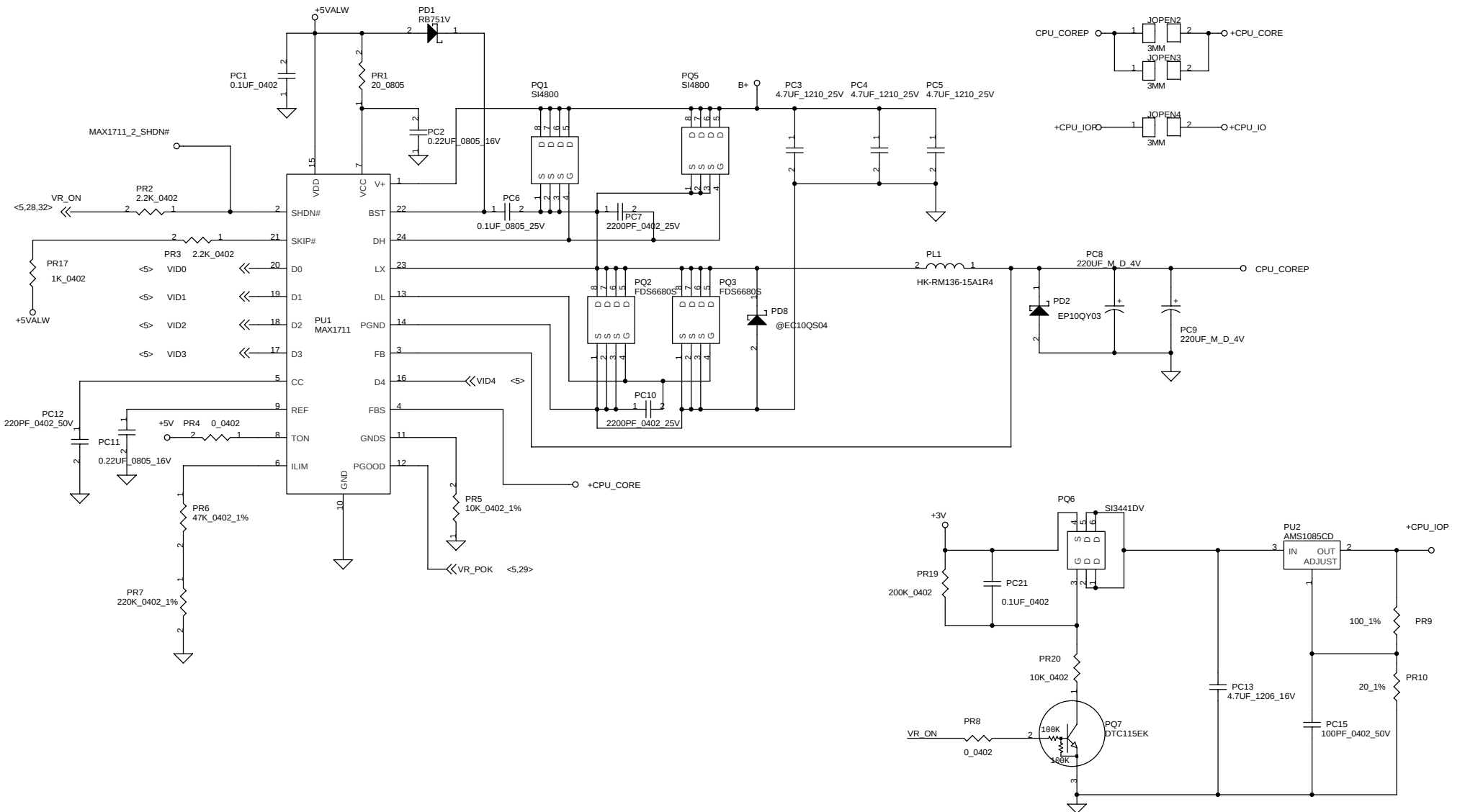
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